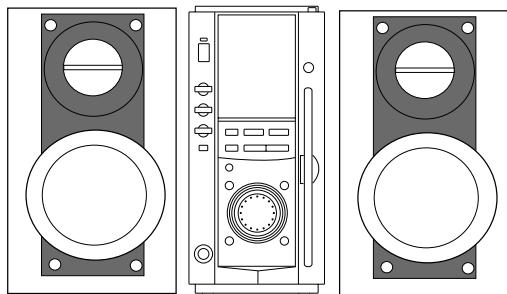




XR-MSK3

HRJ(S)

HRJ7(S)



SERVICE MANUAL

CONPACT DISC STEREO
SYSTEM

BASIC CD MECHANISM : TN-CCD1001-149M

SYSTEM	SPEAKER	REMOTE CONTROL
XR-MSK3	SX-MS7	RC-AAT20

aiwa
S/M Code No. 09-00A-351-3N1



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SPECIFICATIONS

Main unit

FM tuner section

Tuning range	87.5 MHz to 108 MHz
Usable sensitivity (IHF)	13.2 dBf
Antenna terminals	75 ohms (unbalanced)

AM tuner section

Tuning range	531 kHz to 1602 kHz (9 kHz step)
	530 kHz to 1710 kHz (10 kHz step)
Usable sensitivity	350 μ V/m
Antenna	Loop antenna

Amplifier section

Power output	Rated: 12 W + 12 W (50 Hz to 20 kHz, THD less than 1%, 6 ohms) Reference: 15 W + 15 W (1 kHz, THD 10%, 6 ohms)
Total harmonic distortion	0.15% (5 W, 1 kHz, 6 ohms, DIN AUDIO)
Input	VIDEO/AUX: 600 mV
Outputs	SPEAKERS: accept speakers of 6 ohms or more PHONES (stereo mini jack): accepts headphones of 16 ohms or more VIDEO OUT: 1 Vp-p (75 ohms) LINE OUT: 500 mV

Compact disc player section

Laser	Semiconductor laser ($\lambda = 780$ nm)
D-A converter	1 bit dual
Signal-to-noise ratio	85 dB (1 kHz, 0 dB)
Harmonic distortion	0.05% (1 kHz, 0 dB)
Wow and flutter	Unmeasurable

General

Power requirements	120 V/220-240 V AC switchable, 50/60 Hz
Power consumption	50 W
Standby power consumption	1.9 W (power-economizing mode set to ON)
Dimensions of main unit (W × H × D)	100 × 206.2 × 271.5 mm
Weight of main unit	3.8 kg

Speaker system

Cabinet type	2 way, bass reflex (magnetic shielded type)
Speakers	Woofer: 85 mm Tweeter: 22 mm dome type
Impedance	6 ohms
Output sound pressure level	86 dB/W/m
Dimensions (W × H × D)	100 × 206 × 188 mm
Weight	1.5 kg

- Design and specifications are subject to change without notice.
- The word "BBE" and the "BBE symbol" are trademarks of BBE Sound, Inc.
- Under license from BBE Sound, Inc.

ACCESSORIES LIST

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
---------	----------	-----------	-------------

1	8A-CG5-901-010	IB, H(EC)M
2	8A-CG5-951-010	RC UNIT, RC-AAT20
3	87-006-225-010	AM LOOP ANT NC2
4	87-043-115-010	ANT, FEEDER FM
5	87-050-103-010	CORD, PIN 1PY1.5M

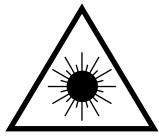
▲ 6 87-A91-017-010 PLUG, CONVERSION JT-0476

PROTECTION OF EYES FROM LASER BEAM DURING SERVICING

This set employs laser. Therefore, be sure to follow carefully the instructions below when servicing.

WARNING!!

WHEN SERVICING, DO NOT APPROACH THE LASER EXIT WITH THE EYE TOO CLOSELY. IN CASE IT IS NECESSARY TO CONFIRM LASER BEAM EMISSION. BE SURE TO OBSERVE FROM A DISTANCE OF MORE THAN 30cm FROM THE SURFACE OF THE OBJECTIVE LENS ON THE OPTICAL PICK-UP BLOCK.



- Caution: Invisible laser radiation when open and interlocks defeated avoid exposure to beam.
- Advarsel: Usynlig laserstråling ved åbning, når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

VAROITUS!

Laiteen Käyttäminen muulla kuin tässä käyttöohjeessa mainitulla tavalla saattaa altistaa käyt-täjän turvallisuusluokan 1 ylittäville näkymättömälle lasersäteilylle.

VARNING!

Om apparaten används på annat sätt än vad som specificeras i denna bruksanvisning, kan användaren utsättas för osynlig laserstrålning, som överskrider gränsen för laserklass 1.

CAUTION

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

ATTENTION

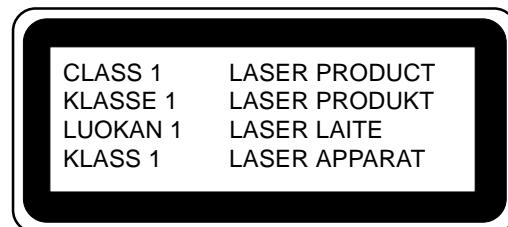
L'utilisation de commandes, réglages ou procédures autres que ceux spécifiés peut entraîner une dangereuse exposition aux radiations.

ADVARSEL

Usynlig laserstråling ved åbning, når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

This Compact Disc player is classified as a CLASS 1 LASER product.

The CLASS 1 LASER PRODUCT label is located on the rear exterior.

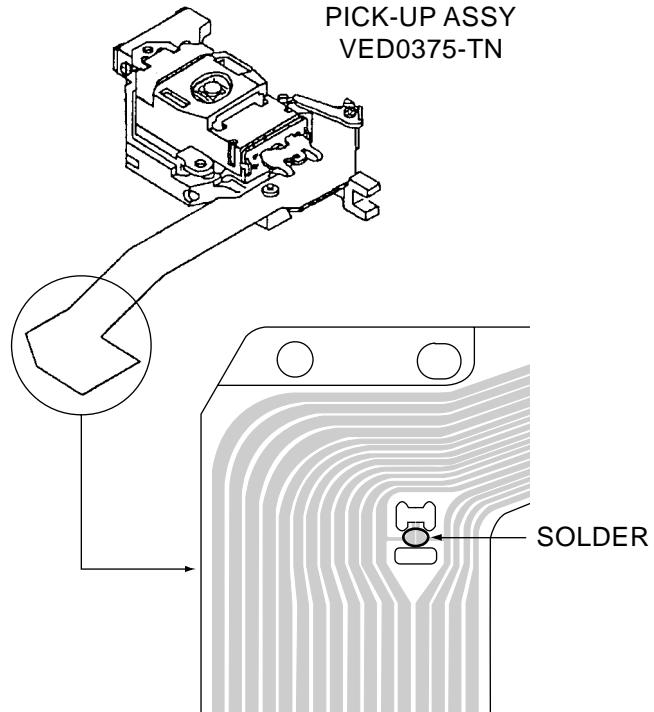


Precaution to replace Optical block

(VED0375-TN)

Body or clothes electrostatic potential could ruin laser diode in the optical block. Be sure ground body and workbench, and use care the clothes do not touch the diode.

- 1) After the connection, remove solder shown in right figure.

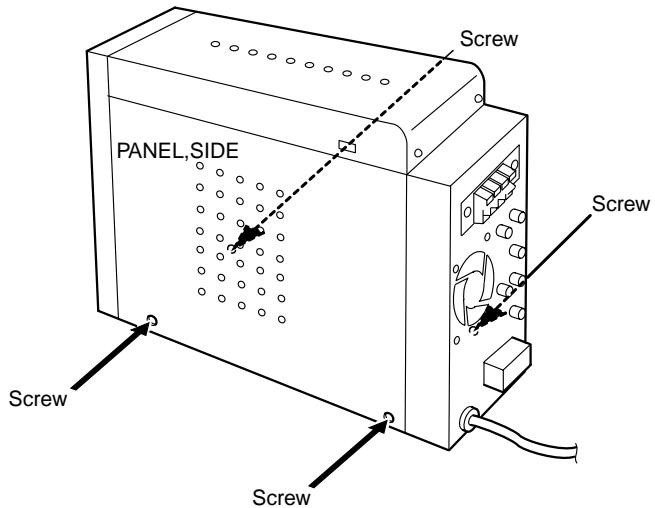


DISASSEMBLY INSTRUCTIONS

1. CD BLOCK

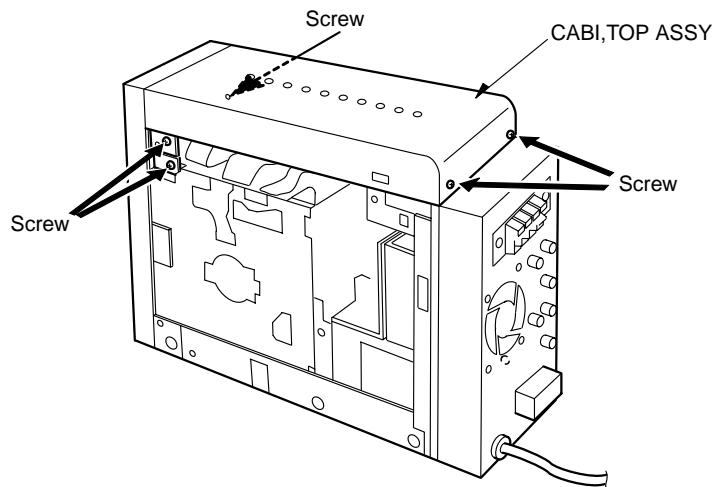
1) Remove the PANEL, SIDE.

Remove the four screws indicated by the arrows and remove the PANEL, SIDE (right and left).



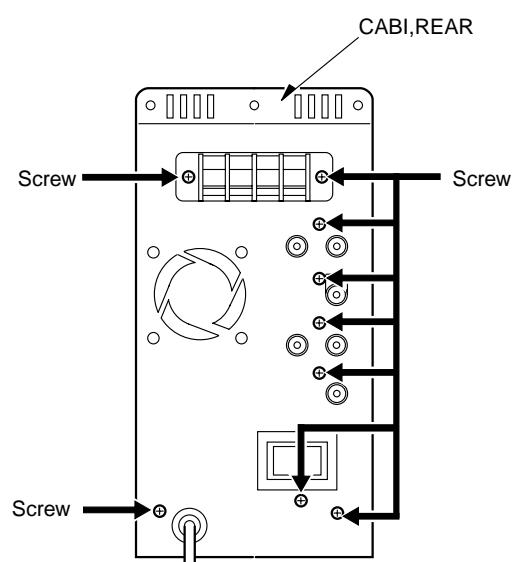
2) Remove the CABI, TOP ASSY.

Remove the five screws indicated by the arrows and remove the CABI, TOPASSY.



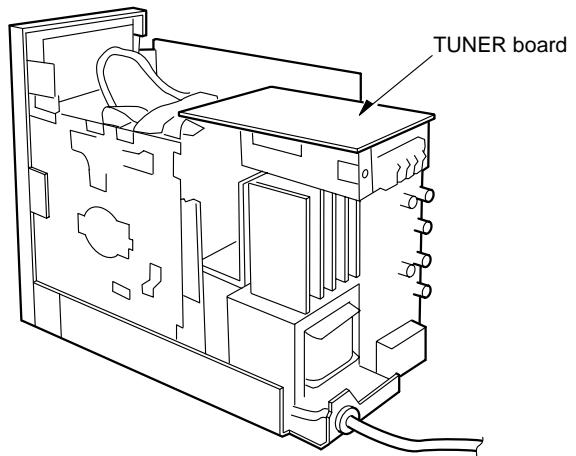
3) Remove the CABI, REAR.

Remove the nine screws indicated by the arrows and remove the CABI, REAR.



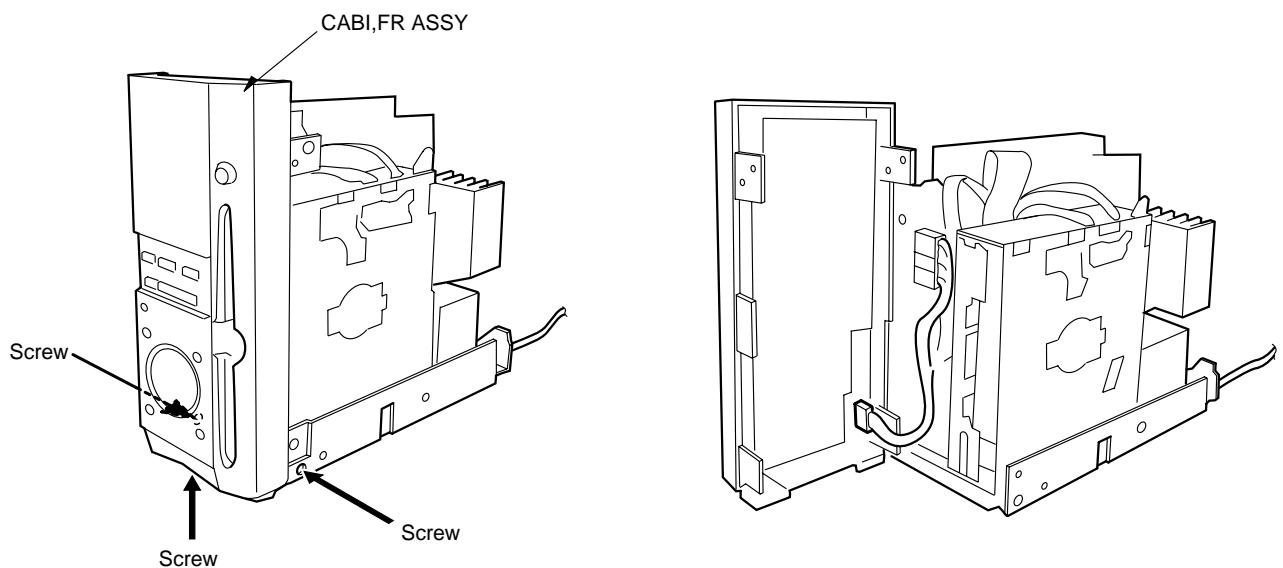
- 4) Remove the TUNER board.

Remove the TUNER board connected to the connector.



- 5) Remove the CABI, FR ASSY.

Remove the three screws indicated by the arrows and remove the CABI, FR ASSY.

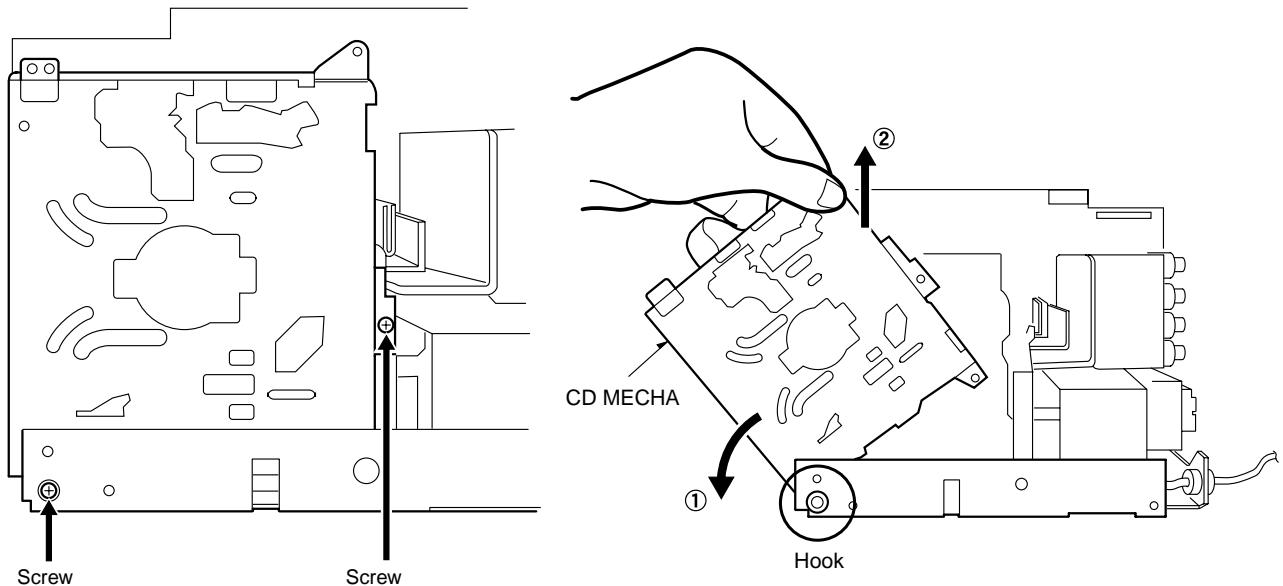


- 6) Remove the CD MECHA.

(1) Remove the two screws indicated by the arrows.

(2) Lift up the CD MECHA in the direction of arrow ① and hook in the position indicated in circle.

(3) Remove the CD MECHA in the direction of arrow ②.



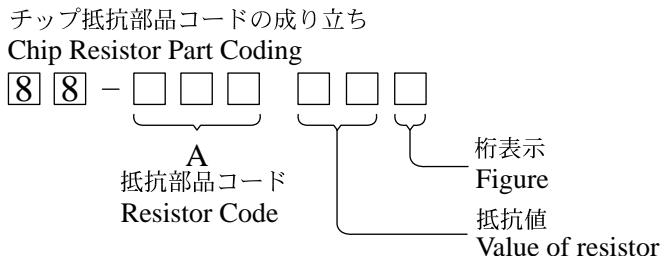
ELECTRICAL MAIN PARTS LIST

REF. NO	PART NO.	KANRI NO.	DESCRIPTION	REF. NO	PART NO.	KANRI NO.	DESCRIPTION
IC							
87-070-246-010	IC,GP1U271X			87-070-274-080	DIODE,1N4003 SEM		
87-A20-909-010	IC,LA4663			87-A40-336-080	ZENER,MTZJ27D T-72		
87-017-915-080	IC,BU4094BCF			87-A40-270-080	C-DIODE,MC2838		
87-017-585-080	IC,NJM4580E			87-A40-004-080	ZENER,MTZJ16A		
87-A21-022-040	C-IC,BA3880FS			87-070-136-080	ZENER,MTZJ5.1B		
87-A21-103-040	C-IC,MM1454XFBE			87-A40-509-080	ZENER,MTZJ6.8C		
87-A21-111-040	C-IC,M62495FP			87-A40-269-080	C-DIODE,MC2836		
8A-CG5-602-010	C-IC,CXP84332-169Q			87-A40-293-080	ZENER,DZ2.7M		
87-A21-777-040	C-IC,BA6289F			87-017-654-060	DIODE,GBU6J		
87-017-760-080	IC,M51943BML			87-A40-874-040	C-ZENER,UDZS 5.6B		
87-017-853-040	IC,NJM2100V			87-A40-335-080	ZENER,MTZJ11C		
87-A21-894-040	C-IC,UPC4742G2			87-A40-341-080	ZENER,MTZJ 36 A		
87-A20-547-010	C-IC,CXA1992AR			87-020-027-080	CHIP-DIODE 1SS184		
8A-CG5-601-030	C-IC,LC876564V-5S40			87-017-024-040	C-DIODE,DA204K		
87-A20-919-040	C-IC,BA5915FP			87-A40-180-040	C-DIODE,SB07-015C		
87-017-917-080	IC,BU4066BCF			87-001-731-080	ZENER,HZS6C2L		
87-A20-917-010	C-IC,CXD2540Q-1/2			87-017-149-080	ZENER,HZS6A2L		
8A-CG6-640-030	C-IC,UPD78016FGC-583						
87-A20-602-040	C-IC,M5291FP						
87-A20-925-040	C-IC,BA05FP			MAIN C.B			
87-A20-905-040	C-IC,BA033FP			C1	87-012-369-080	C-CAP,S 0.047-50F	
87-A20-920-010	C-IC,CL680-D1			C3	87-012-368-080	C-CAP,S 0.1-50 F	
87-A20-921-040	C-IC,SN74LVU04APW			C4	87-012-368-080	C-CAP,S 0.1-50 F	
87-A20-962-040	C-IC,MSM54V16258B/BSL			C5	87-012-368-080	C-CAP,S 0.1-50 F	
84-ZG1-695-040	C-IC,LH5V2RN1			C6	87-012-368-080	C-CAP,S 0.1-50 F	
87-A20-975-040	C-IC,SN74LV74APW			C7	87-012-369-080	C-CAP,S 0.047-50F	
87-A20-974-040	C-IC,LC74781M-9017			C8	87-012-368-080	C-CAP,S 0.1-50 F	
87-A20-918-040	C-IC,SM5878AM			C9	87-A12-033-090	CAP,E 6800-25 SMG30L	
87-A21-419-040	C-IC,NJM14558MD-TE2			C10	87-010-409-080	CAP,E 220-50 SME	
87-070-127-110	IC,LC72131 D			C11	87-010-553-080	CAP,E 47-16	
87-A20-913-010	IC,LA1837NL			C13	87-010-247-080	CAP, ELECT 100-50V	
				C14	87-010-235-080	CAP,E 470-16 SME	
				C15	87-010-387-080	CAP,E 470-25 SME	
				C24	87-016-251-080	CAP,E 220-16 M SMG	
				C27	87-012-140-080	CAP 470P	
TRANSISTOR							
89-213-702-010	TR,2SB1370E(1.8W)			C29	87-010-247-080	CAP, ELECT 100-50V	
87-A30-076-080	C-TR,2SC3052F			C30	87-016-044-080	CAP,E 100-16 5L GAS	
87-026-610-080	TR,KTC3198GR			C31	87-010-235-080	CAP,E 470-16 SME	
87-A30-075-080	C-TR,2SA1235F			C61	87-010-260-080	CAP, ELECT 47-25V	
87-A30-234-080	TR,CSC4115BC			C62	87-010-496-080	CAP,E 3.3-50 5L	
89-418-580-080	TR,2SD1858 TV2			C91	87-010-401-080	CAP, ELECT 1-50V	
87-026-245-080	TR,DTC114ES			C92	87-010-260-080	CAP, ELECT 47-25V	
87-A30-198-080	TR,KTC3199GR			C101	87-A11-242-040	CAP,E 220-10 M 5L SRM	
87-026-609-080	TR,KTA1266GR			C102	87-A11-242-040	CAP,E 220-10 M 5L SRM	
87-A30-087-080	C-FET,2SK2158			C103	87-010-196-080	CHIP CAPACITOR,0.1-25	
87-A30-073-080	C-TR,RT1N 141C			C104	87-010-993-080	CAP, CHIP 0.056	
87-A30-273-040	C-TR,DTC124EKA			C105	87-010-196-080	CHIP CAPACITOR,0.1-25	
87-A30-086-070	C-TR,CSD1306E			C106	87-010-493-040	CAP,E 0.47-50 GAS	
87-A30-072-080	C-TR,RT1P 144C			C108	87-010-157-080	C-CAP,S 18P-50 SL	
89-111-624-080	C-TR,2SA1162Y			C109	87-012-156-080	C-CAP,S 220P-50 CH	
87-026-237-080	CHIP-TR,DTC124XK			C110	87-010-196-080	CHIP CAPACITOR,0.1-25	
89-327-125-080	CHIP TR,2SC2712GR			C111	87-010-079-040	CAP,E 100-6.3 5L	
87-026-350-040	CHIP-TR,DTC114TUA			C112	87-010-194-080	CAP, CHIP 0.047	
87-026-231-080	CHIP-TRANSISTER,DTA124XK			C114	87-010-194-080	CAP, CHIP 0.047	
87-026-211-080	C-TR,DTA144EK			C115	87-010-498-040	CAP,E 10-16 GAS	
87-026-210-080	CHIP-TR,DTC144EK			C116	87-010-196-080	CHIP CAPACITOR,0.1-25	
87-A30-117-010	TR,2SA1357			C117	87-010-196-080	CHIP CAPACITOR,0.1-25	
89-111-625-080	C-TR,2SA1162GR(0.15W)			C118	87-010-196-080	CHIP CAPACITOR,0.1-25	
87-026-297-080	C-TR,DTA144TK			C129	87-010-316-080	C-CAP,S 33P-50 CH	
87-026-580-080	C-TR,DTA123JK			C201	87-010-491-040	CAP,E 0.22-50 GAS	
87-026-470-080	C-TR,HN1C03FB(0.3W)			C202	87-010-491-040	CAP,E 0.22-50 GAS	
89-327-143-080	C-TR,2SC27140			C203	87-010-178-080	CHIP CAP 1000P	
				C204	87-010-178-080	CHIP CAP 1000P	
				C205	87-010-492-040	CAP,E 0.33-50 GAS	
				C206	87-010-492-040	CAP,E 0.33-50 GAS	
DIODE							
87-020-465-080	DIODE,1SS133 (110MA)			C211	87-010-560-040	CAP,E 10-50 GAS	
87-A40-313-080	C-DIODE,MC 2840			C212	87-010-260-080	CAP, ELECT 47-25V	
87-A40-346-080	ZENER,MTZJ 8.2C			C215	87-010-405-080	CAP, ELECT 10-50V	
87-A40-345-080	ZENER,MTZJ10C			C216	87-010-405-080	CAP, ELECT 10-50V	
				C217	87-012-368-080	C-CAP,S 0.1-50 F	

REF. NO	PART NO.	KANRI NO.	DESCRIPTION	REF. NO	PART NO.	KANRI NO.	DESCRIPTION
C0828	87-010-196-080	C-CAP,S 0.1-25 Z F C2012		J0801	87-A60-702-010	TERMINAL,ANT 4P CJ-9036	
C0829	87-010-196-080	C-CAP,S 0.1-25 Z F C2012		L0771	87-A50-266-010	COIL,FM DET-2N(TOK)	
C0959	87-010-196-080	C-CAP,S 0.1-25 Z F C2012		L0772	87-A91-110-010	FLTR,PCFUZH-450 (TOK)	
C0960	87-010-196-080	C-CAP,S 0.1-25 Z F C2012		L0981	8Z-ZA1-667-010	COIL,AM PACK 4F(TOK)	
C0961	87-012-170-080	C-CAP,U 8P-50 D CH		X0721	87-A70-061-010	VIB,XTAL 4.500MHZ CSA-309	
C0963	87-010-196-080	C-CAP,S 0.1-25 Z F C2012					
CF0801	87-008-261-010	FLTR,CF SFE10.7MA5					
CF0802	87-008-261-010	FLTR,CF SFE10.7MA5					
CN0701	87-A60-700-010	CONN,13P H GRY TUC-P13X-C1					
FFE0801	A8-8ZA-194-030	8ZA-1 FEMUNM					

- Regarding connectors, they are not stocked as they are not the initial order items.
The connectors are available after they are supplied from connector manufacturers upon the order is received.

○チップ抵抗部品コード／CHIP RESISTOR PART CODE



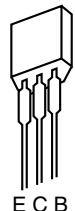
チップ抵抗
Chip resistor

容量 Wattage	種類 Type	許容誤差 Tolerance	記号 Symbol	寸法／Dimensions (mm)				抵抗コード : A Resistor Code : A
				外形/Form	L	W	t	
1/16W	1005	± 5%	CJ		1.0	0.5	0.35	104
1/16W	1608	± 5%	CJ		1.6	0.8	0.45	108
1/10W	2125	± 5%	CJ		2	1.25	0.45	118
1/8W	3216	± 5%	CJ		3.2	1.6	0.55	128

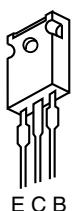
TRANSISTOR ILLUSTRATION



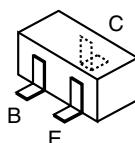
CSC4115
KTA1266
KTC3198



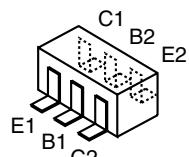
DTC114ES
KTC3199



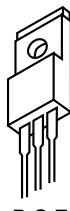
2SA1357



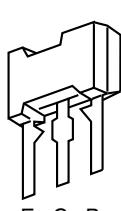
2SA1162



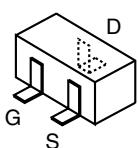
HN1C03



2SB1370



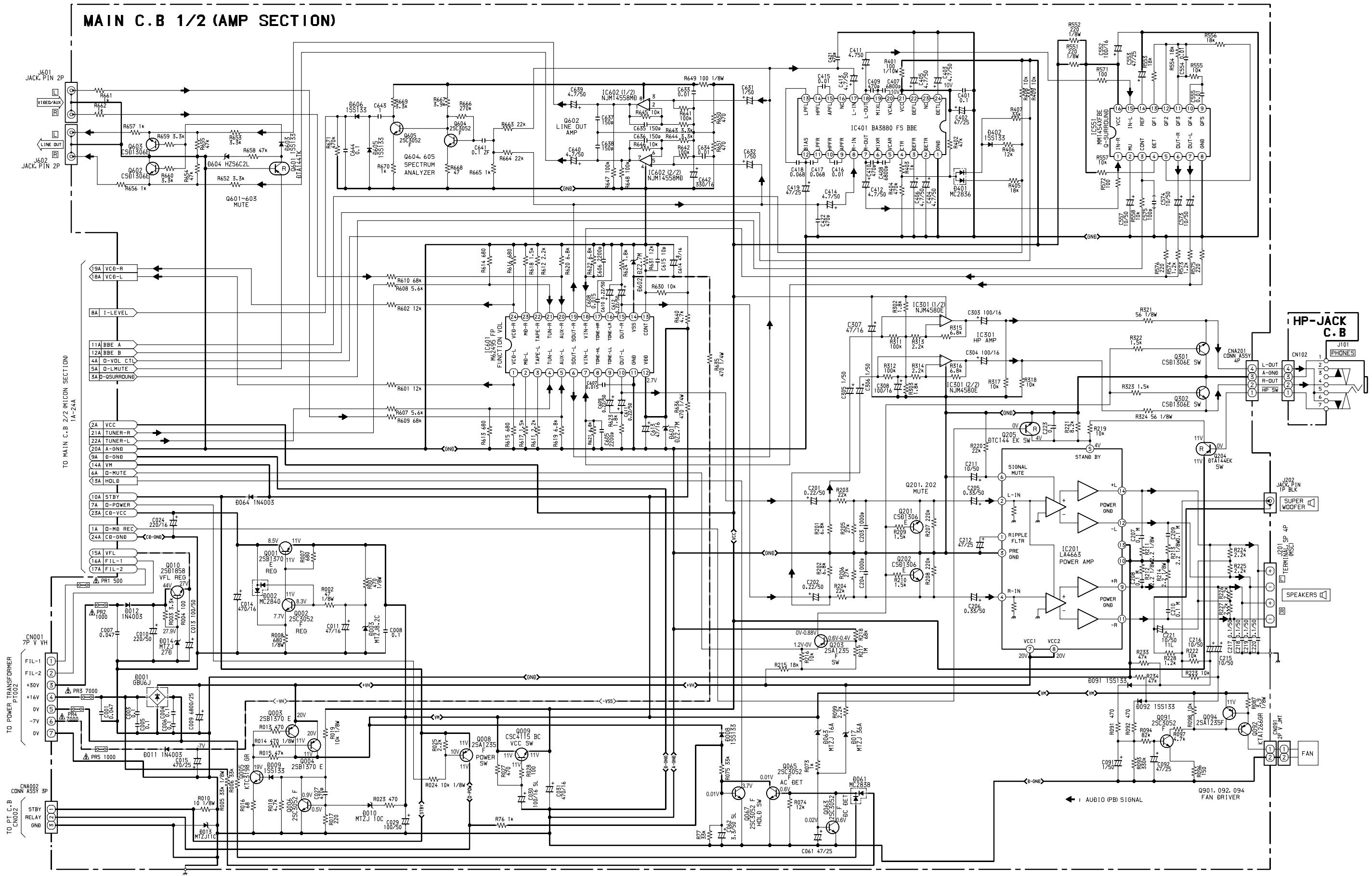
2SD1858



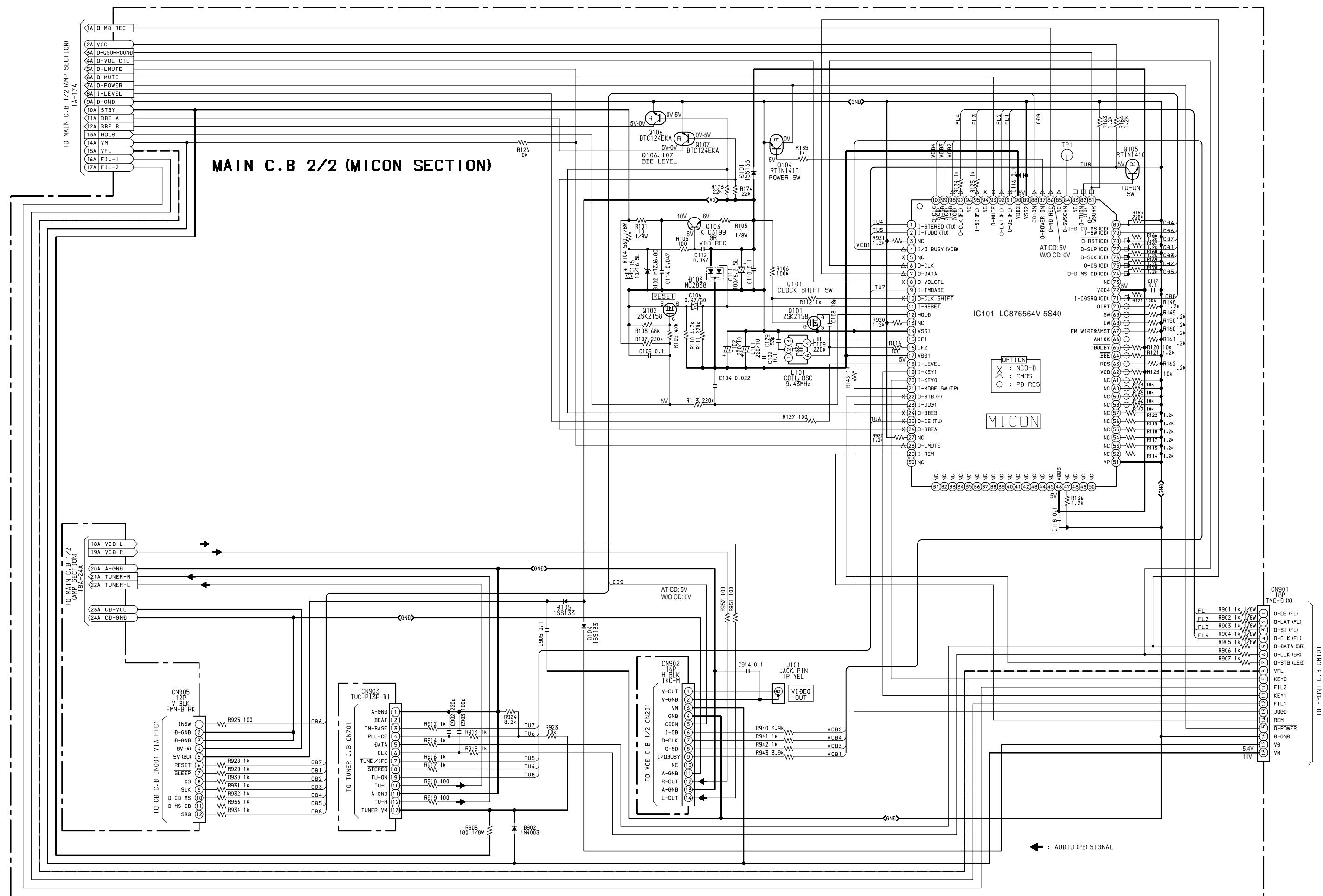
2SK2158

2SA1235
2SC2712
2SC2714
2SC3052
CSD1306
DTA123JK
DTA124XK
DTA144EK
DTA144TK
DTC114TUA
DTC124EKA
DTC124XK
DTC144EK
RT1N141C
RT1P144C

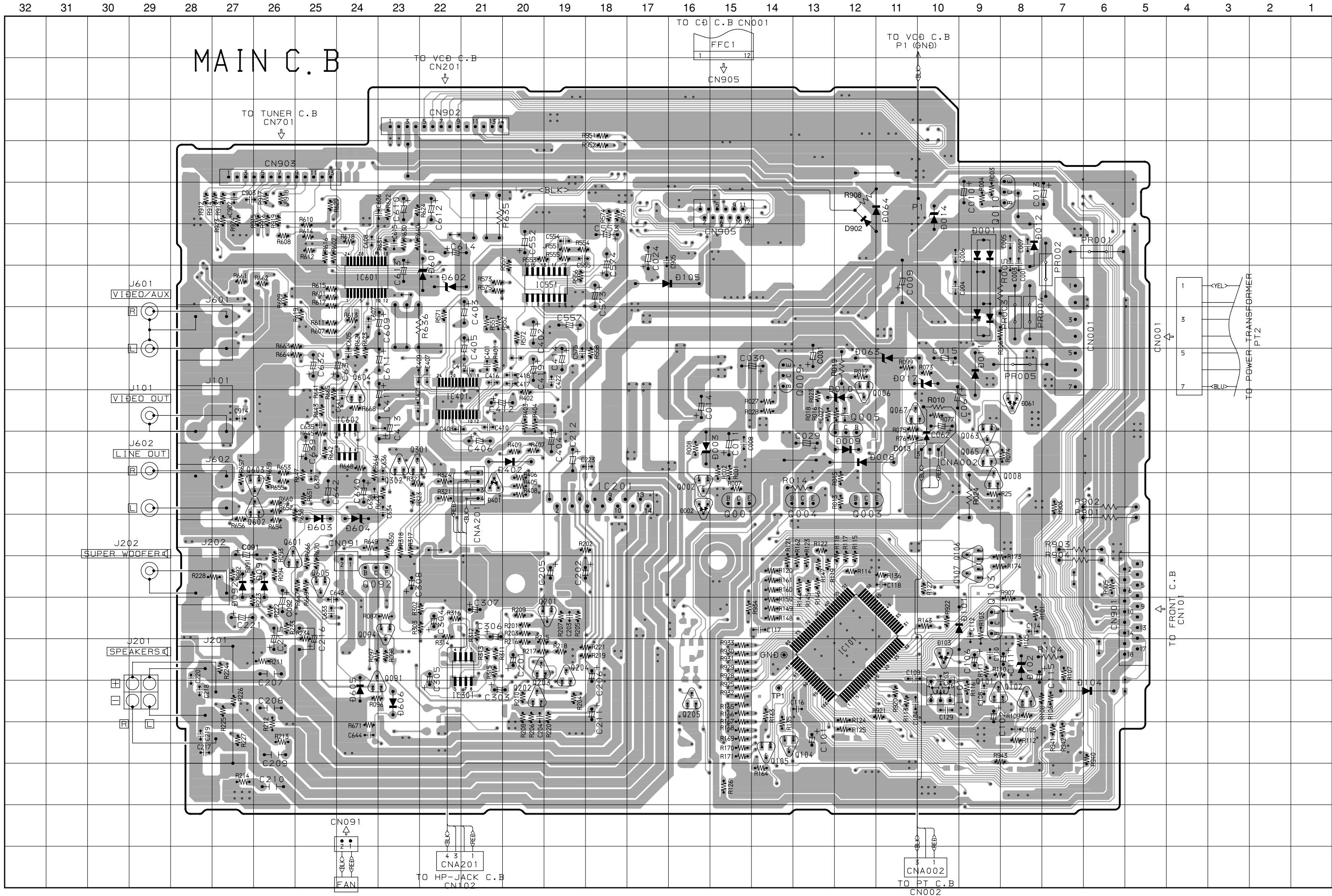
SCHEMATIC DIAGRAM - 1 (MAIN -1/2 SECTION)



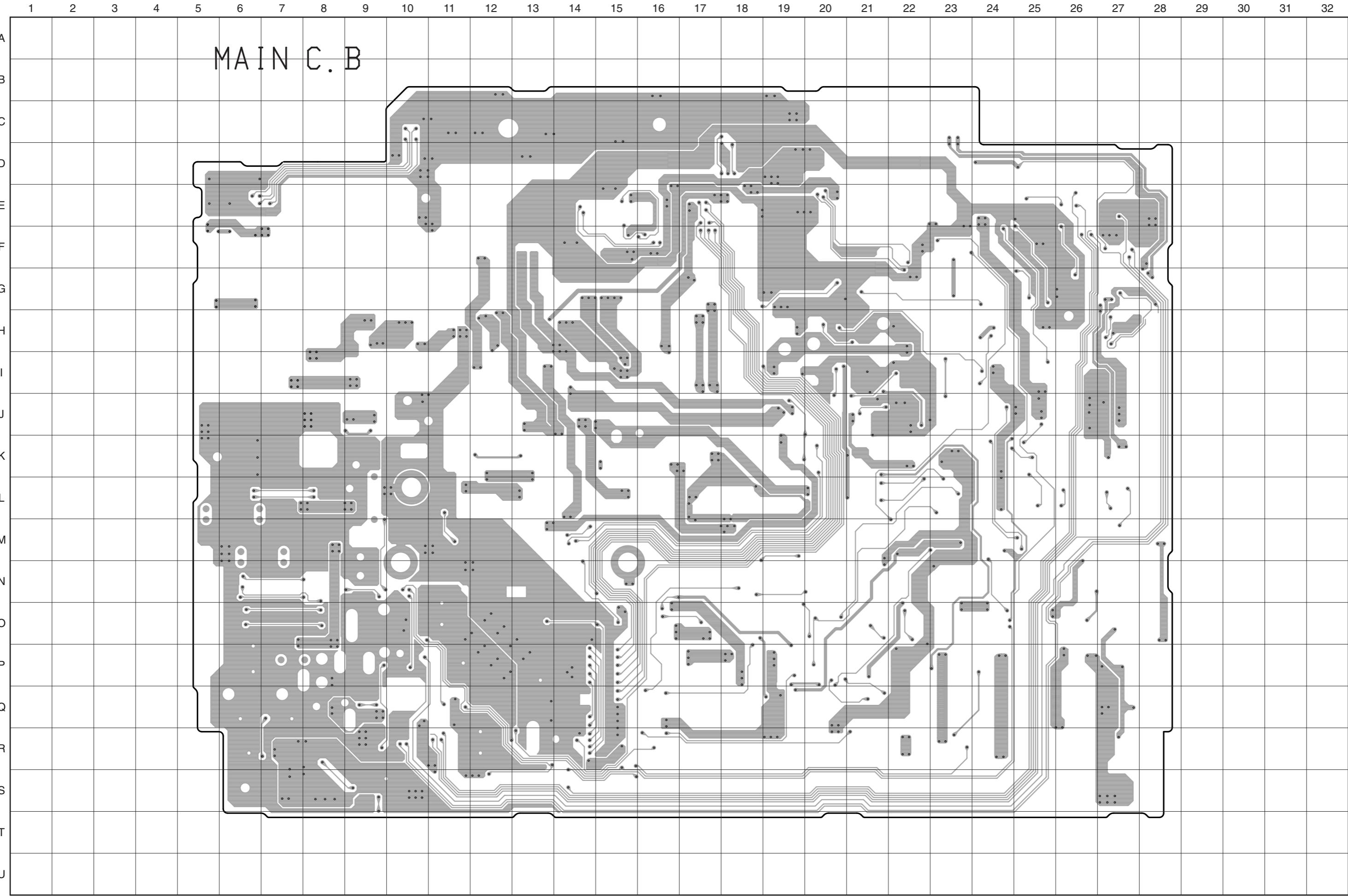
SCHEMATIC DIAGRAM - 2 (MAIN -2/2 SECTION)



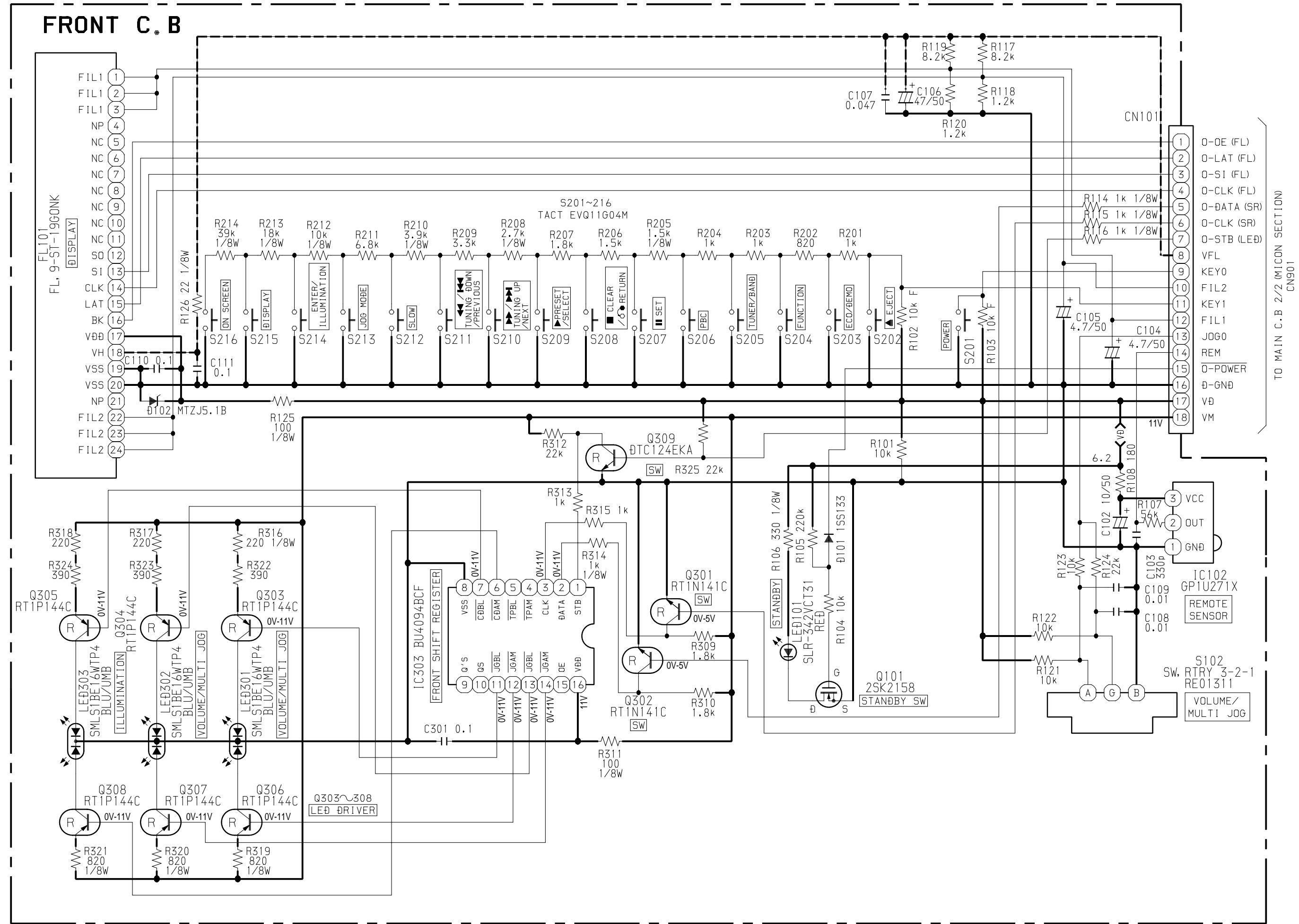
WIRING - 1 (MAIN C.B 1/2)



WIRING - 2 (MAIN C.B)



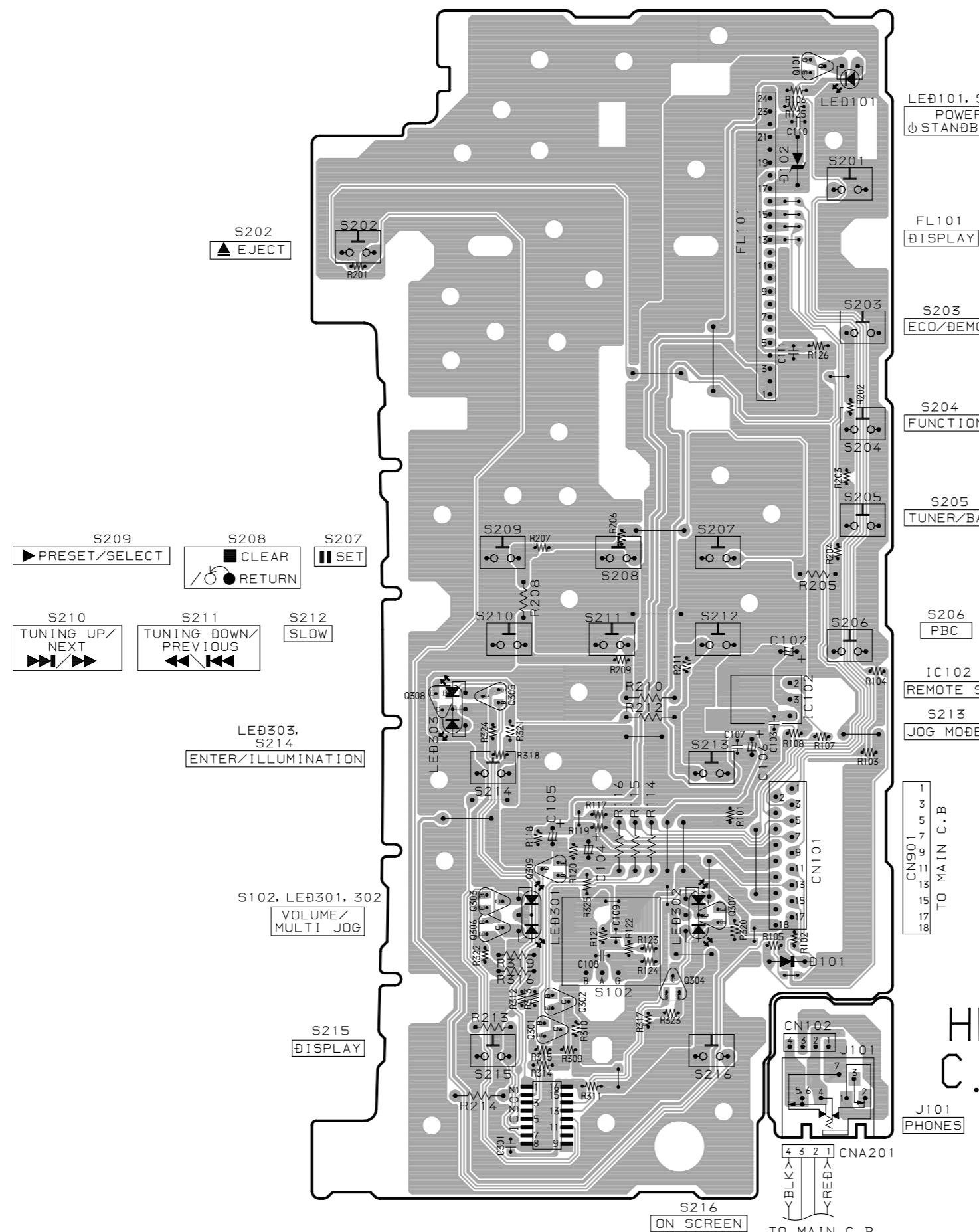
SCHEMATIC DIAGRAM - 3 (FRONT SECTION)



WIRING - 3 (FRONT, HP-JACK C.B)

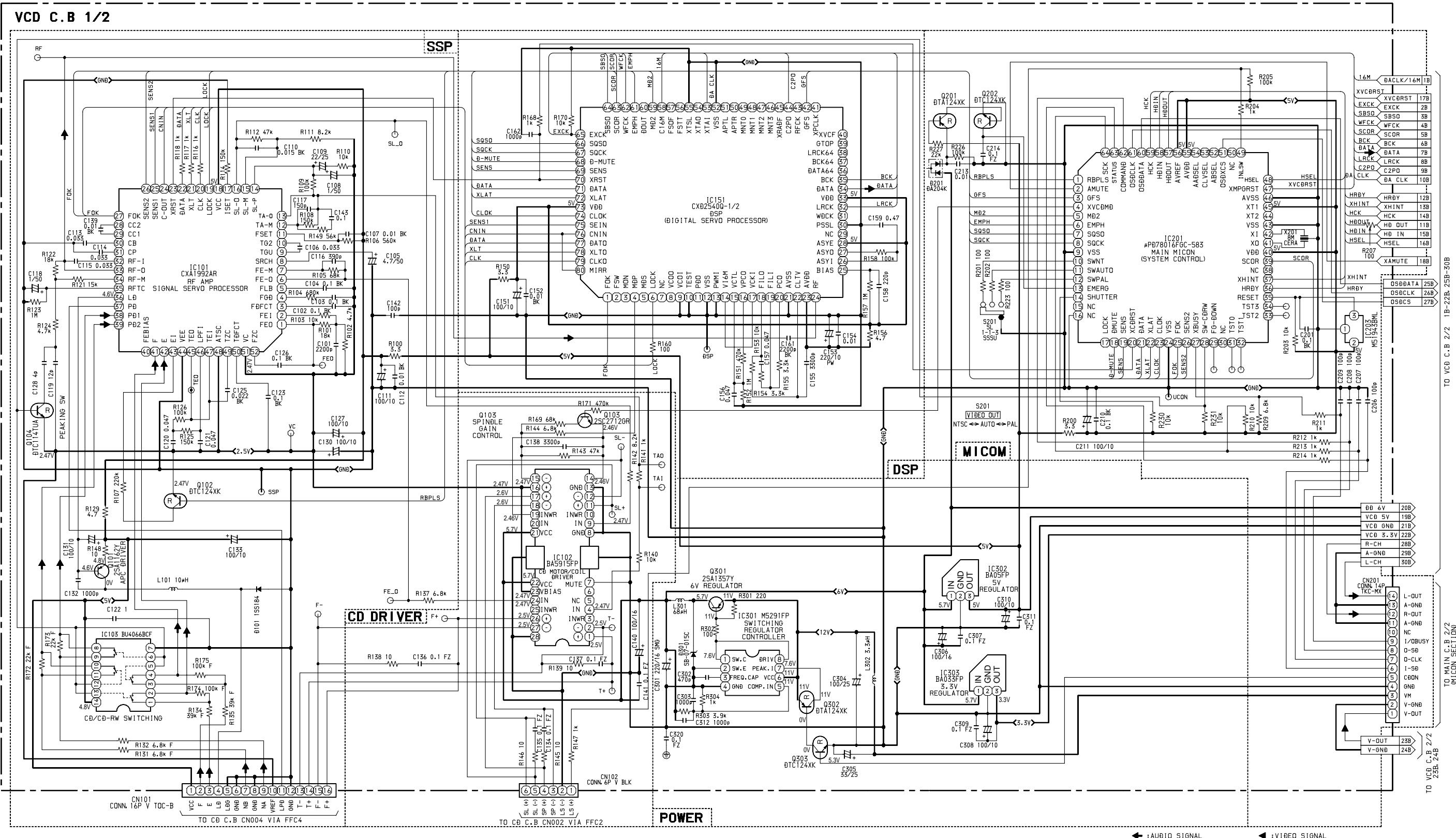
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
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FRONT C. B

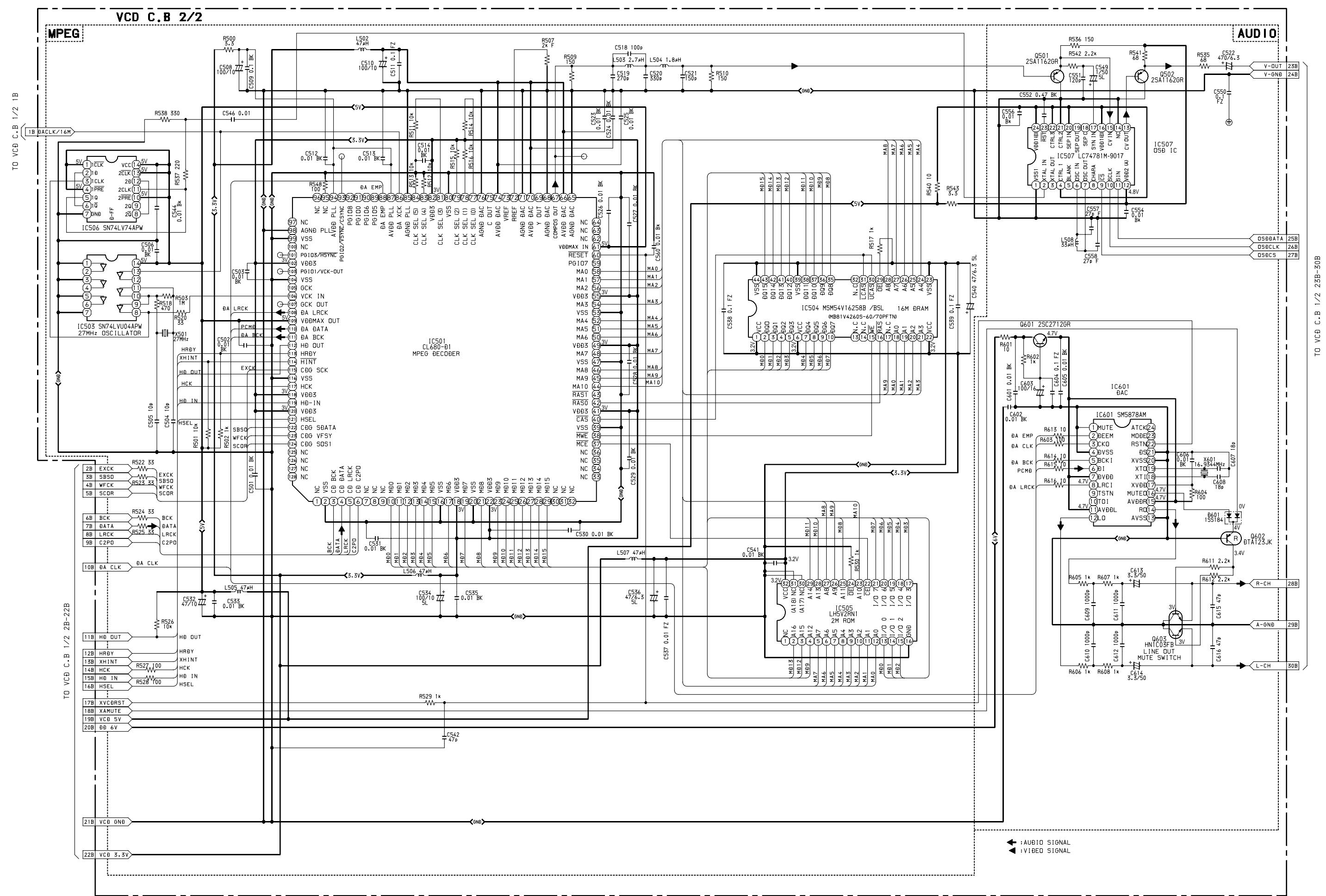


HP-JACK
C. B

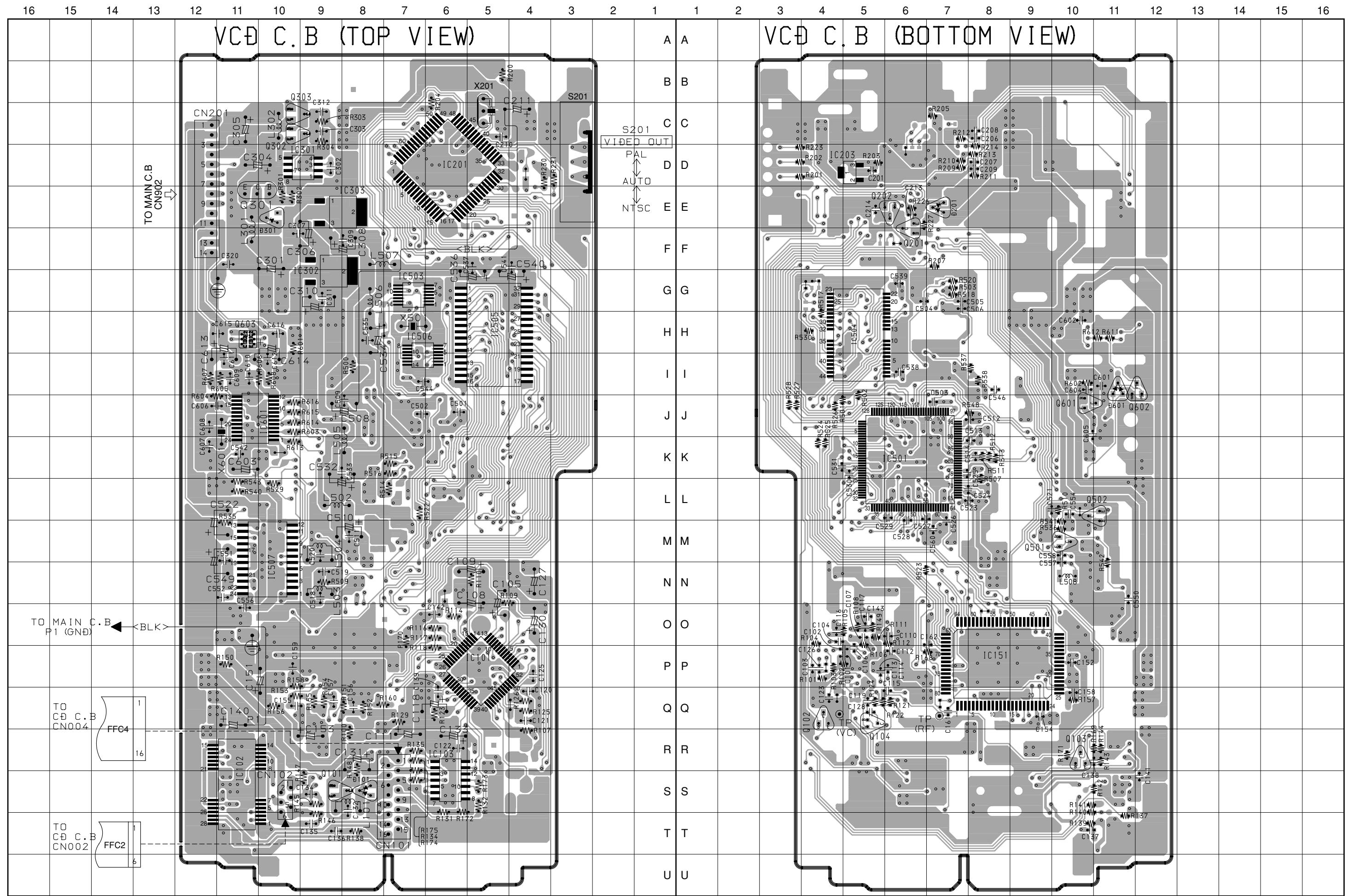
SCHEMATIC DIAGRAM - 4 (VCD-1/2 SECTION)



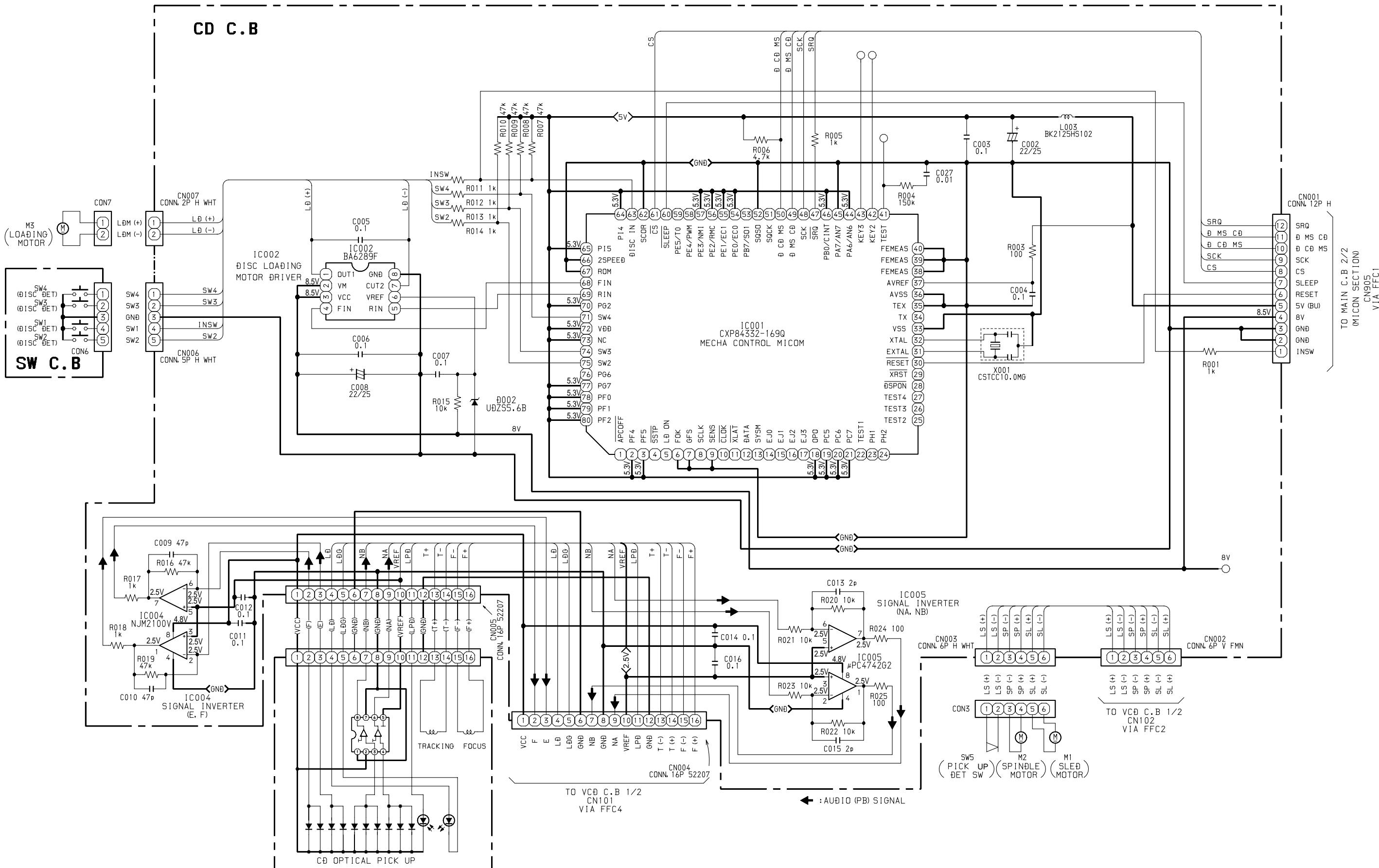
SCHEMATIC DIAGRAM - 5 (VCD-2/2 SECTION)



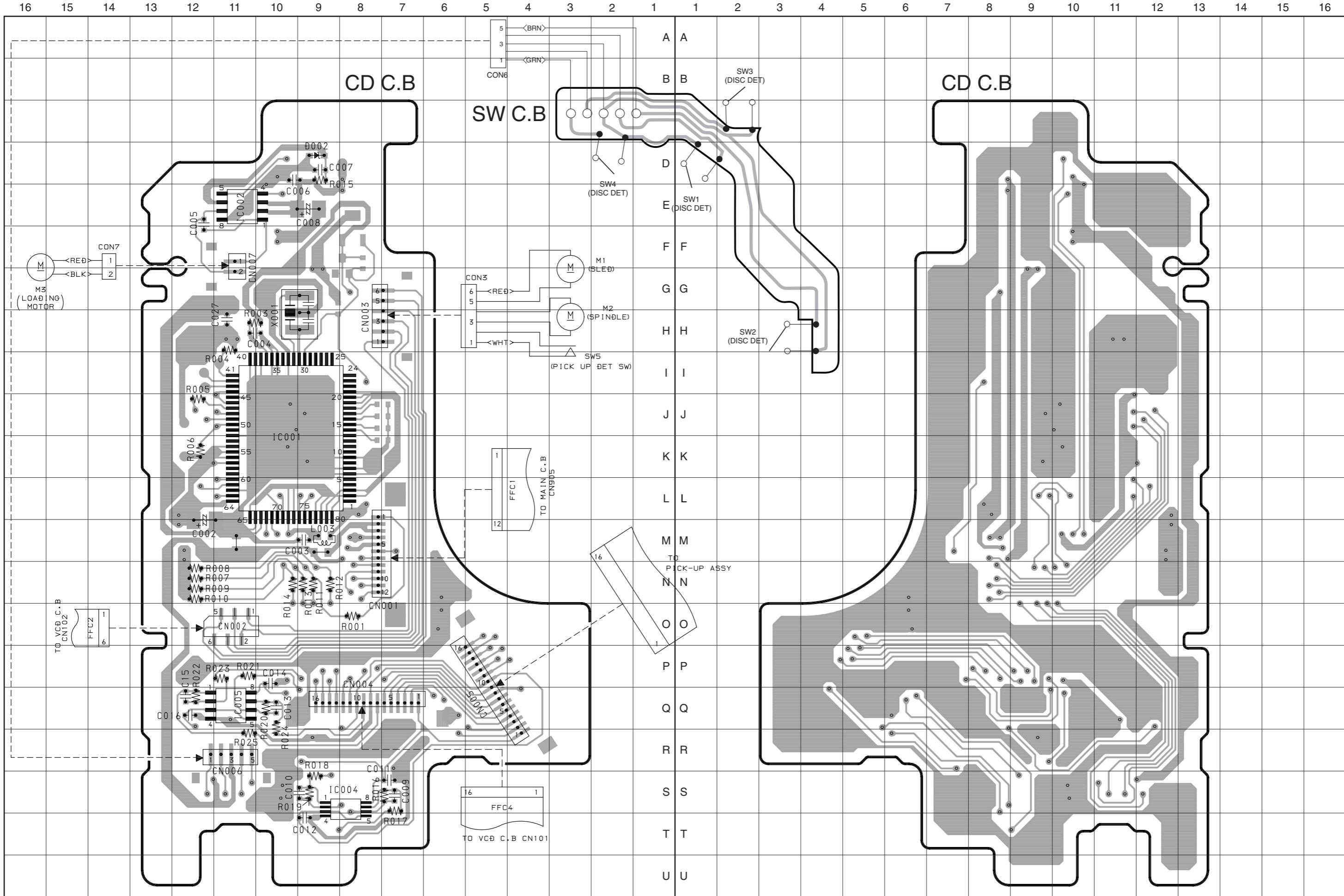
WIRING - 4 (VCD C.B.)



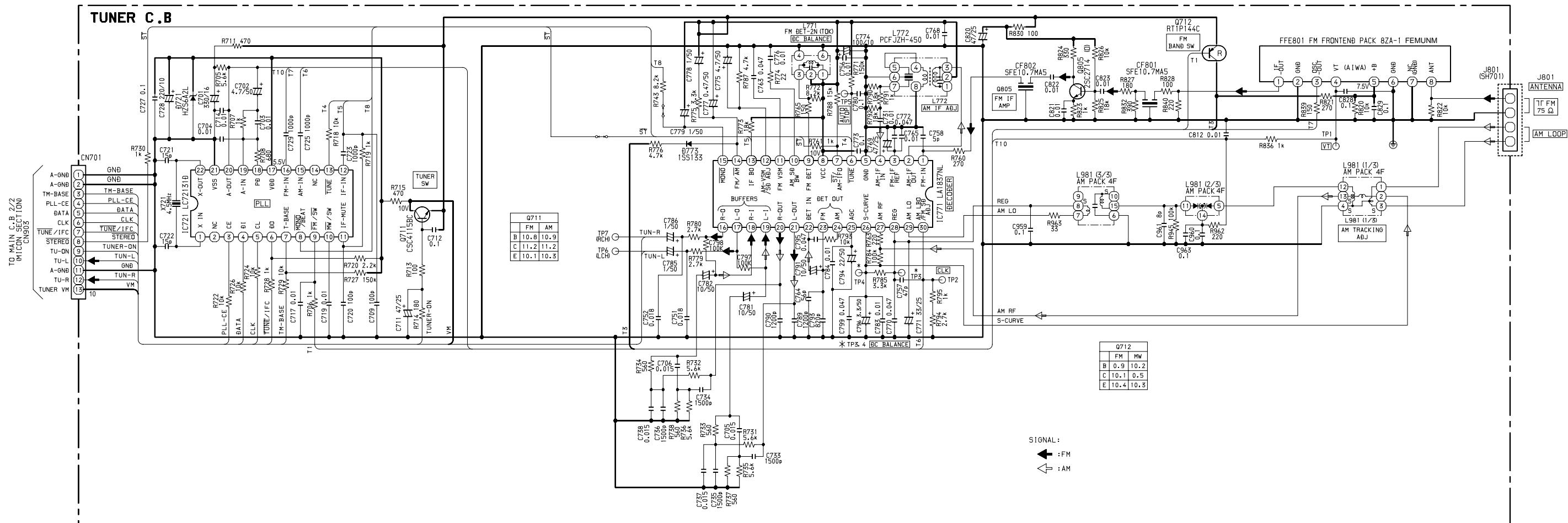
SCHEMATIC DIAGRAM - 6 (CD SECTION)



WIRING - 5 (CD C.B)

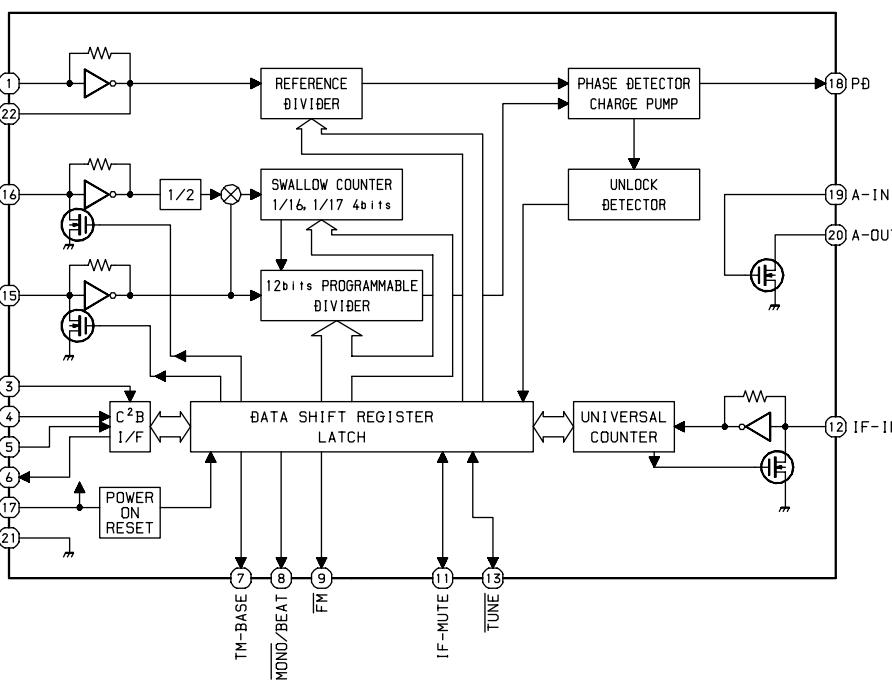


SCHEMATIC DIAGRAM - 7 (TUNER SECTION)

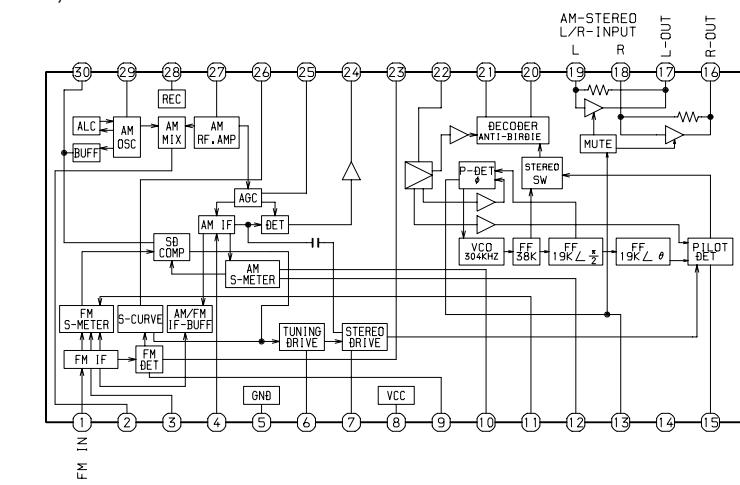


IC BLOCK DIAGRAM - 1

IC, LC72131D



IC, LA1837NL



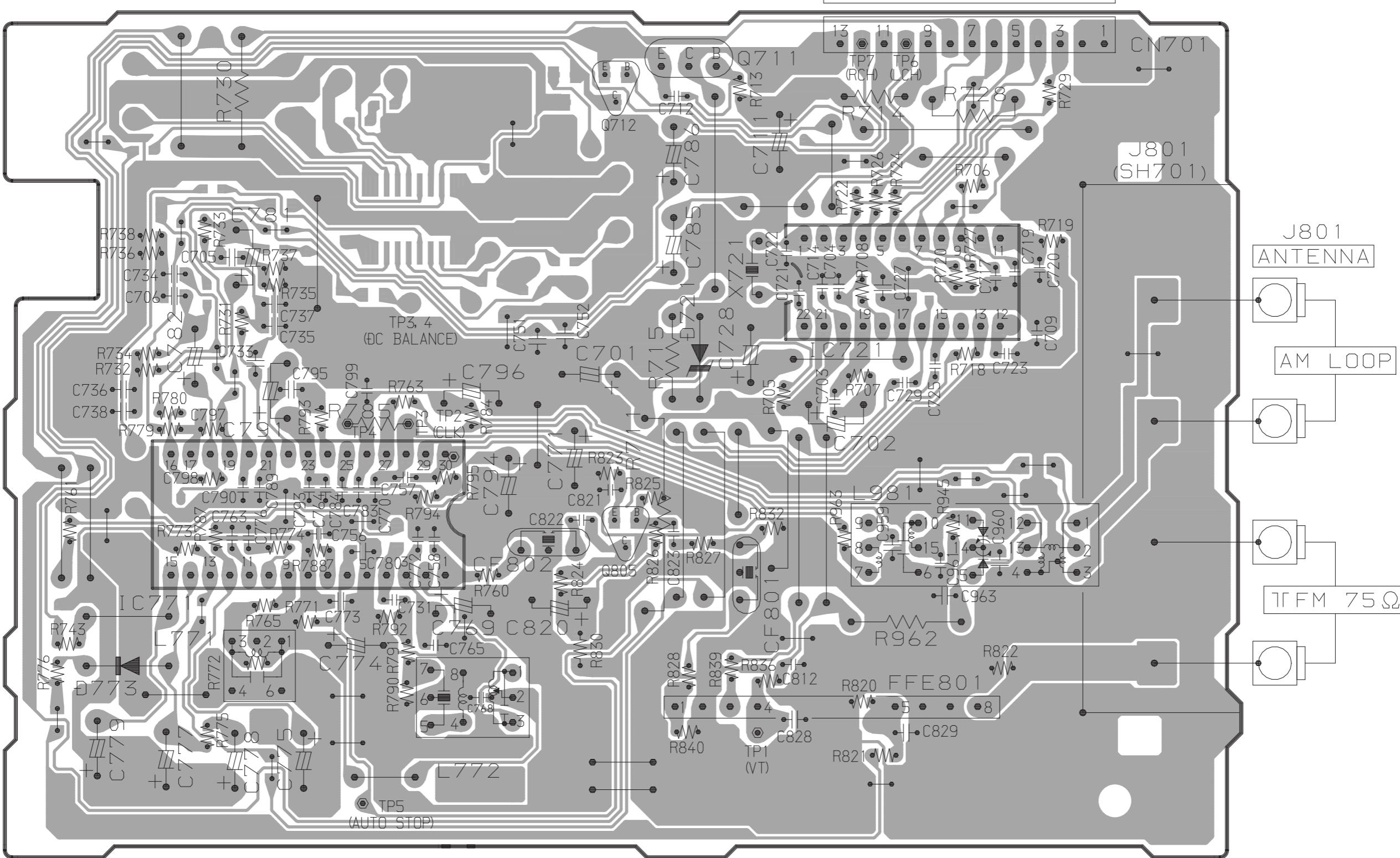
WIRING - 6 (TUNER C.B)

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
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TUNER C.B

TO MAIN C.B 2/2
(MICON SECTION)
CN903

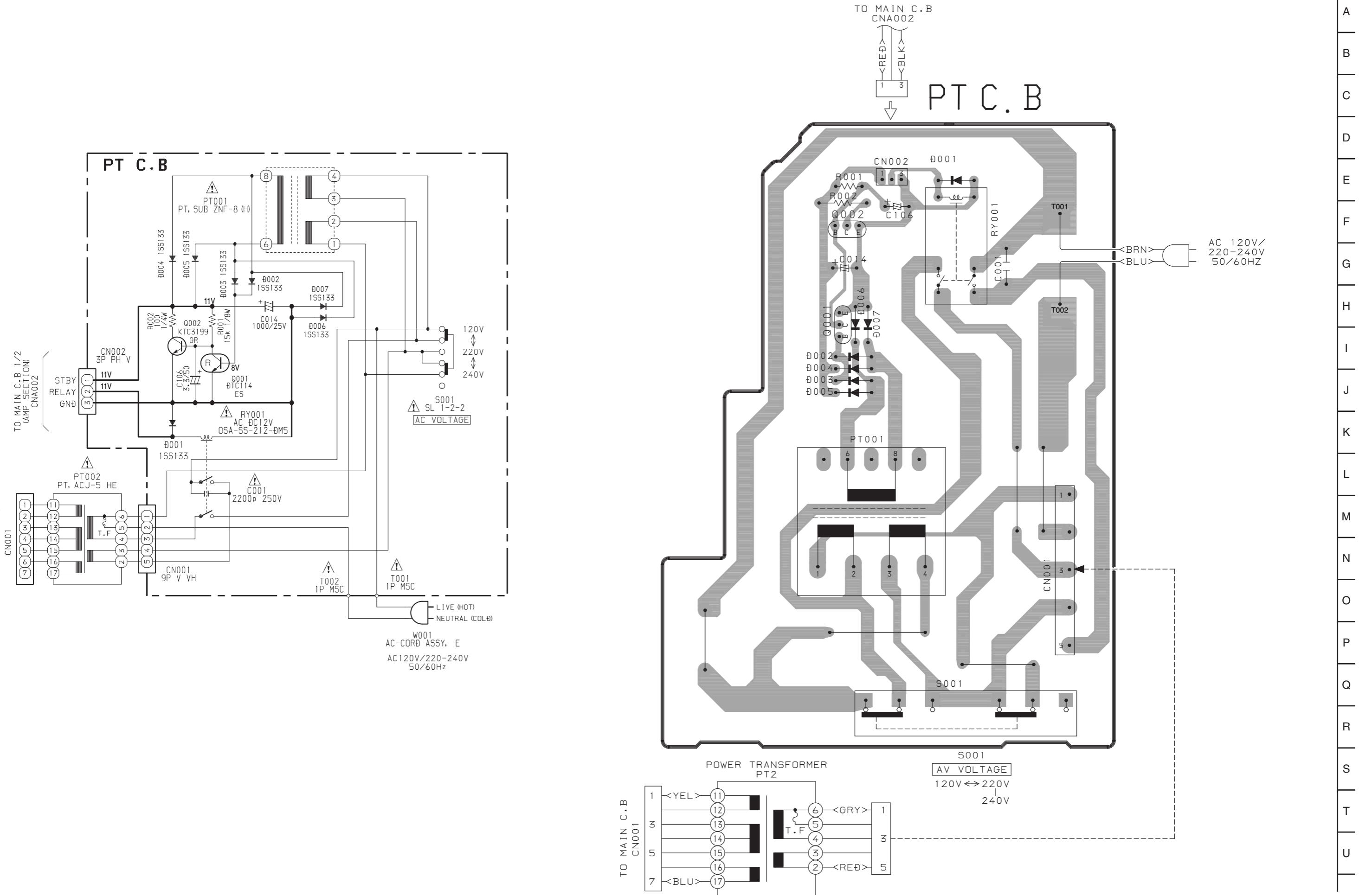
13 11 9 7 5 3 1



SCHEMATIC DIAGRAM - 8 (PT SECTION)

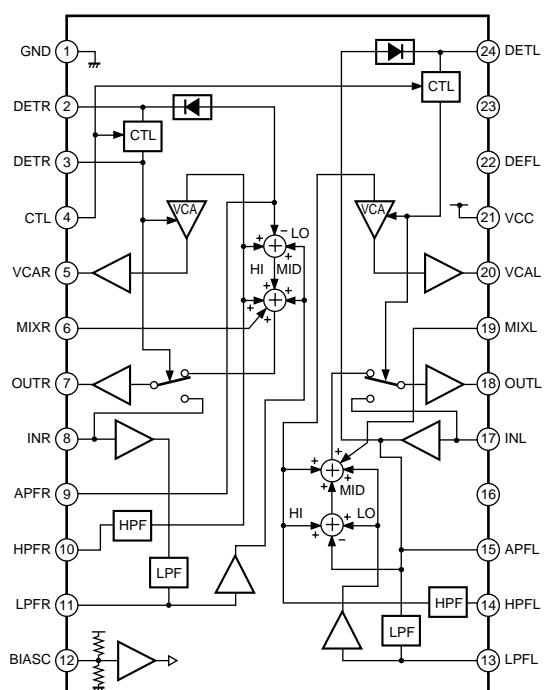
WIRING - 7 (PT C.B.)

19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

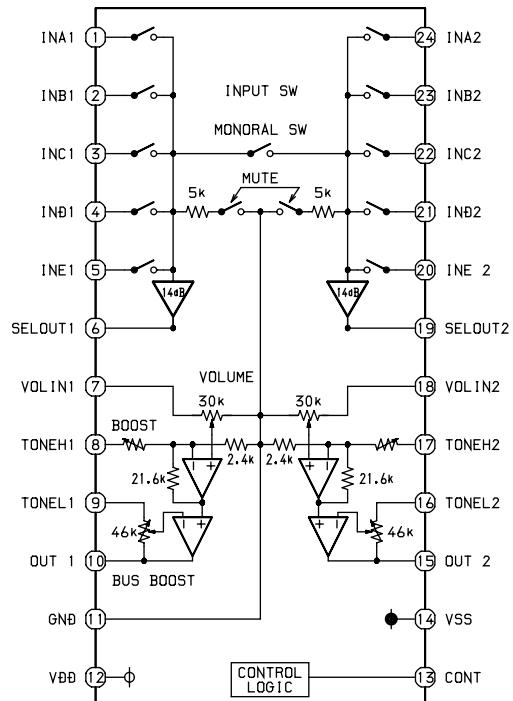


IC BLOCK DIAGRAM - 2

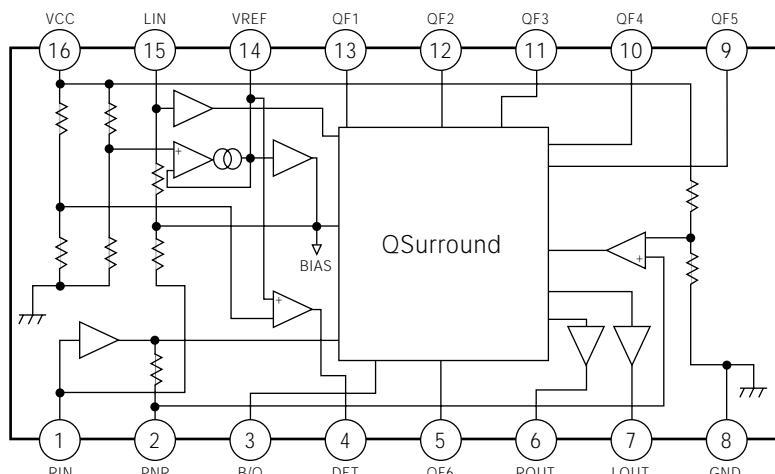
IC, BA3880FS



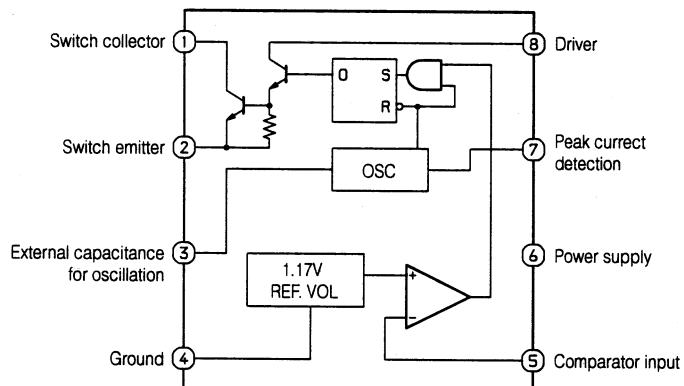
IC, M62495FP



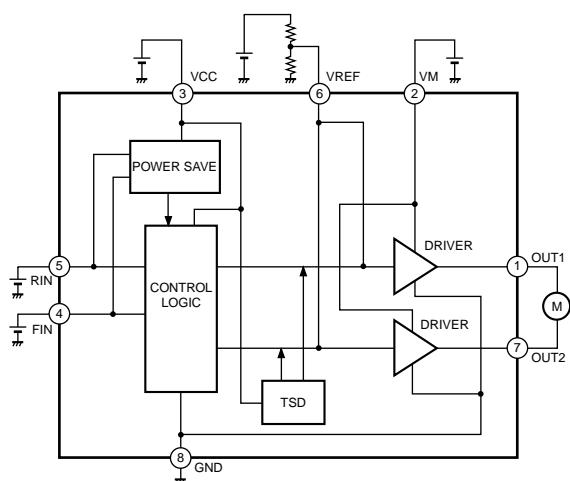
IC, MM1454XFBE



IC, M5291FP

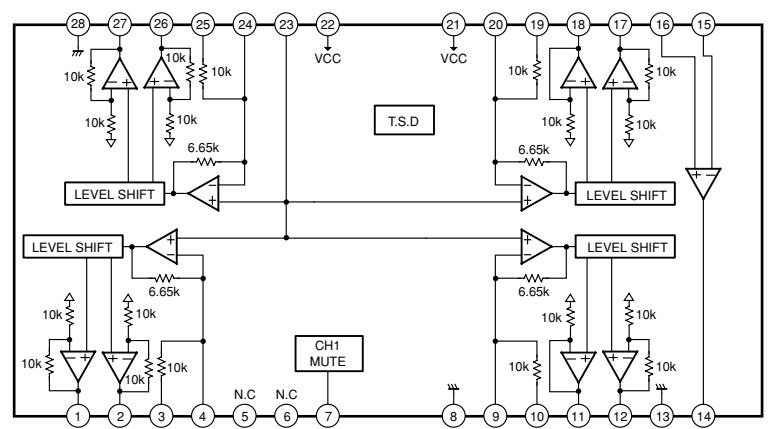
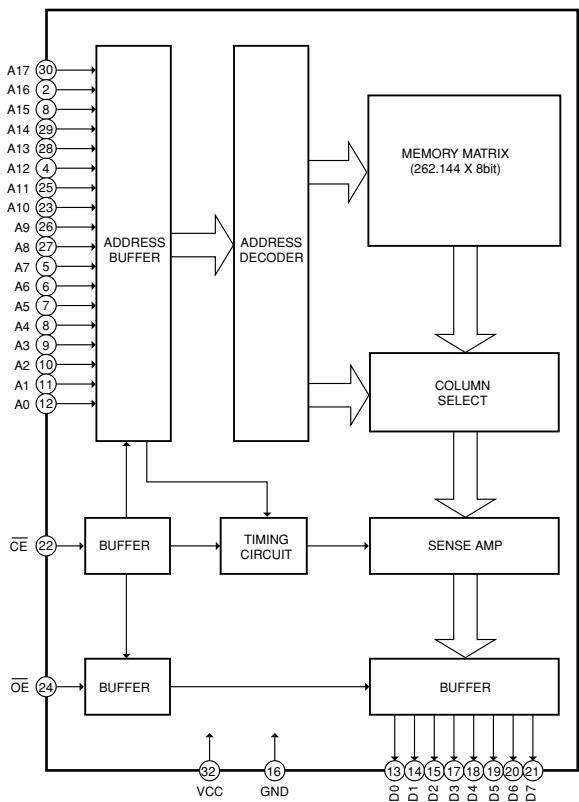


IC, BA6289F

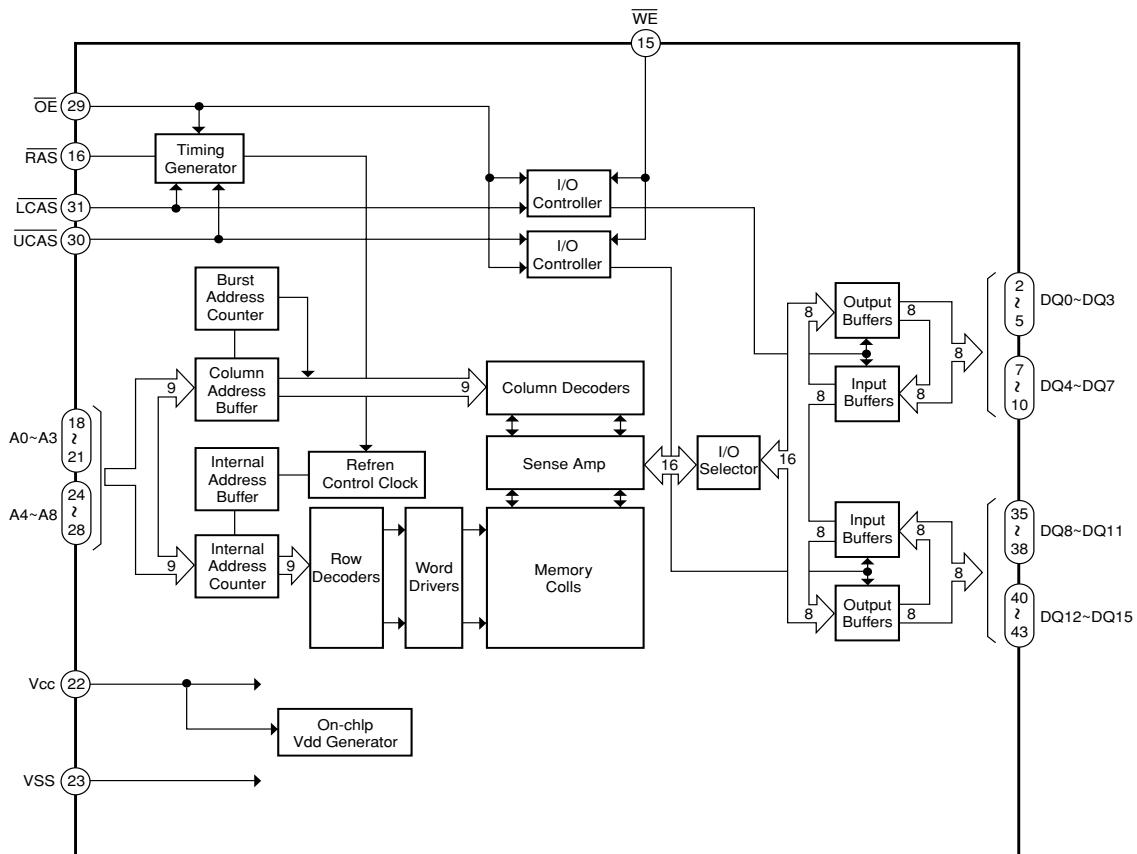


IC, LH5V2RN1

IC, BA5915FP



IC, MSM54V16258B/BSL



IC DESCRIPTION
IC, LC876580-5S40

Pin No.	Pin Name	I/O	Description
1	I-STEREO (TU)	I	Tuner stereo detection input.
2	I-TUDO (TU)	I	Connect to tuner PLL IC, LC72131D Pin 6 (DO).
3	NC	-	Not connected.
4	I/OBUSY(VCD)	I/O	BUSY port to VCD microprocessor
5	NC	-	Not connected.
6	O-CLK	O	Front shift register BU4094BCF (reversal) and tuner PLL IC, LC72131D combination clock output.
7	O-DATA	O	Front shift register BU4094BCF (reversal) and tuner PLL IC, LC72131D combination data output.
8	O-VOLCTL	O	Connect to Function VOL IC, M62495FP pin 13 (CONT).
9	I-TMBASE	I	Reference clock input. Connect to LC72131D Pin 7 (T-BASE).
10	O-CLK SHIFT	O	Clock shift control output.
11	I-RESET	I	MICON reset input.
12	HOLD	I	Hold status detection input.
13	NC	-	Not connected.
14	VSS 1	-	GND.
15	CF 1	I	Connect to 9.43MHz crystal oscillation.
16	CF 2	O	Connect to 9.43MHz crystal oscillation.
17	VDD 1	-	MICON power supply (+5V).
18	I-LEVEL	I	Level meter input (AD).
19	I-KEY1	I	Key 1: AD input.
20	I-KEY0	I	Key 0: AD input.
21	I-MODE SW(TP)	I	Deck mechanical status detection input (AD).
22	O-STB (F)	O	Front shift register BU4094BCF latch reversal output.
23	I-JOG1	I	AD input from multi jog rotary encoder output A/B.
24	O-BBEB	O	BBE control reversal output (B).
25	O-CE (TU)	O	Tuner PLL IC, LC72131D chip enable output.
26	O-BBEA	O	BBE control reversal output (A).
27	NC	-	Not connected.
28	O-LMUTE	O	Line mute output. (Not used)
29	I-REM	I	Remote controller input.
30 ~ 45	NC	-	Not connected.
46	VDD3	-	MICON power supply (+5V).
47	I-CLS (MD)	I	MD unit close detection SW input / Close at L. (Connected to GND through a resistor)
48 ~ 57	NC	-	Not connected.
58	I-SWCLS (TP)	I	Deck mechanical status detection input (SWCLS).
59	I-SWOPN (TP)	I	Deck mechanical status detection input (SWOPN).
60	I-AUTO (TP)	I	Deck mechanical status detection input (AUTO).
61	I-CAM(TP)	I	Deck mechanical status detection input (CAM).

Pin No.	Pin Name	I/O	Description
62	VCD	O	VCD detection (L: VCD present)
63	RDS	I	Initial matrix input (H: RDS) (EZ only) / Connect to GND through a resistor. (U only).
64	<u>BBE</u>	I	Initial matrix input (L: BBE).
65	<u>DOLBY</u>	I	Initial matrix input (L: DOLBY).
66	AM10K	I	Initial matrix input (H: 10K STEP / L: 9K STEP).
67	FM WIDE&AMST	I	Initial matrix input (H: FM WIDE & AM STEREO).
68	LW	I	Initial matrix input (H: LW) (EZ only) / Connect to GND through a resistor. (U only)
69	SW	I	Initial matrix input (H: SW). Connect to GND through a resistor.
70	OIRT	I	Initial matrix input (H: OIRT). Connect to GND through a resistor.
71	I-CDSRQ (CD)	I	CD data transmission request signal input.
72	VDD4	-	MICON power supply (+5V).
73	O-CDON (CD)	O	CD power supply control output. (Not used)
74	O-D MS CD (CD)	O	Transmission output to CD MICON.
75	O-CS (CD)	O	Data transmission request output to CD MICON.
76	O-SCK (CD)	O	Data reception and transmission clock output to CD MICON.
77	O-SLP (CD)	O	Sleep output to CD MICON.
78	<u>O-RST</u> (CD)	O	Reset output to CD MICON.
79	I-SWCD	I	CD disc detection switch (H: active).
80	I-D CD MS (CD)	I	Transmission data from CD MICON.
81	O-QSURR	O	Q-Surround IC control output. to GND through a resistor.
82	O-TUON (TU)	O	Tuner power supply switch output.
83	O-MOTOR (TP)	O	Deck mechanical motor control output. (Not used)
84	O-SWSCAN	O	Tuner test mode TP (used for coil adjustment point).
85	O-SREQ (MD)	O	Serial data for MD unit control transmission request. (Not used)
86	O-MD REC	O	Output H at MD REC.
87	O-POWER ON	O	Power on output.
88	CD ON	-	CD ON/OFF output (CD ON: H)
89	VSS2	-	GND.
90	VDD2	-	MICON power supply (+5V).
91	O-OE (FL)	O	Output function output to FL driver.
92	O-LAT (FL)	O	Latch output to FL driver.
93	O-MUTE	O	Main mute output.
94	<u>O-PL</u> (TP)	O	Deck mechanical plunger control output. (Not used)
95	I-SI (FL)	I	Serial data input to FL driver.
96	O-MREQ (MD)	O	Serial data for MD unit control transmission request output. (Not used)
97	O-CLK (FL)	O	Clock output to FL driver.
98	I-SD(VCD)	I	Data input from VCD microprocessor
99	O-SD(VCD)	O	Data output to VCD microprocessor
100	O-CLK(VCD)	O	Clock for communications with VCD microprocessor

IC, CXA1992AR

Pin No.	Pin Name	I/O	Description
1	FEO	O	Output terminal for focus error amplifier. Internally connected to window comparator input for bias condition.
2	FEI	I	Input terminal for focus error.
3	FDFCT	I	Capacitor connection terminal for time constant used when there is defect.
4	FGD	I	This pin is connected to GND via capacitor when high frequency gain of the focus servo is attenuated.
5	FLB	I	This is a pin where the time constant is externally connected to raise the low frequency gain of the focus servo.
6	FEO	O	Focus drive output.
7	FEM	I	Focus amplifier inverted input.
8	SRCH	I	This is a pin where the time constant is externally connected to generate the focus search waveform.
9	TGU	I	This is a pin where the selection time constant is externally connected to set the tracking servo the high frequency gain.
10	TG2	I	This is a pin where the selection time constant is externally connected to set the tracking high frequency gain.
11	FSET	I	Pin for setting peak of the phase compensator of the focus tracking.
12	TAM	I	Tracking amplifier inverted input.
13	TAO	O	Tracking drive output.
14	SLP	I	Sled amplifier non-inverted input.
15	SLM	I	Sled amplifier inverted input.
16	SLO	O	Sled drive output.
17	ISET	I	The current which determines height of the focus search, track jump and sled kick is input with external resistance connected.
18	VCC	I	Power supply.
19	LOCK	I	“L” setting starts sled disorder-prevention circuit. (No pull-up resistance) (Connected to VC)
20	CLK	I	Clock input for serial data transfer from CPU. (No pull-up resistance)
21	XLT	I	Latch input from CPU. (No pull-up resistance)
22	DATA	I	Serial data input from CPU. (No pull-up resistance)
23	XRST	I	Reset system at “L” setting. (No pull-up resistance)
24	COUT	O	Signal output for track number counting.
25	SENS1	O	FZC, DFCT1, TZC, BALH, TGH, FOH, or ATSC is output depending on the command from CPU.
26	SENS2	O	DFCT2, MIRR, BALL, TGL or FOL is output depending on the command from CPU.
27	FOK	O	Output terminal for focus OK comparator.
28	CC2	I	Input pin where the DEFECT bottom hold output is capacitance coupled.
29	CC1	O	DEFECT bottom-hold output terminal. Internally connected to interruption comparator input.
30	CB	I	Connection terminal for DEFECT bottom-hold capacitor.
31	CP	I	Connection terminal for MIRR hold-capacitor. Anti-reverse input terminal for MIRR comparator.
32	RFI	I	Input terminal by capacity combination of RF summing amplifier.
33	RFO	O	Output terminal of RF summing amplifier. Checkpoint of Eye pattern.

Pin No.	Pin Name	I/O	Description
34	RFM	I	Anti-reverse input terminal for RF summing amplifier. The gain of RF amplifier is decided by the connection resistance between RF-M and RF-O terminals.
35	RFTC	I	This is a pin where the selection time constant is externally connected to control the RF level.
36	LD	O	APC amplifier output terminal.
37	PD	I	APC amplifier input terminal.
38 ~ 39	PD1 ~ PD2	I	RFI-V amplifier inverted input pin. These pins are connected to the A+C and B+C pins of the optical pickup, receiving by currents input.
40	FEBIAS	I/O	Bias adjustment pin of the focus error amplifier. (Not used)
41 ~ 42	F ~ E	I	F and EIV amplifier inverted input pins. These pins are connected to the F and E of the optical pickup, receiving by current input.
43	EI	—	Gain adjustment pin of the I-V amplifier E. (When not in use of BAL automatic adjustment) (Not used)
44	VEE	—	GND connection pin.
45	TEO	O	Output terminal for tracking-error amplifier. Output E-F signal.
46	LPFI	I	BAL adjustment comparator input pin. (Input through LPF from TEO)
47	TEI	I	Input terminal for tracking error.
48	ATSC	I	Window-comparator input terminal for detecting ATSC.
49	TZC	I	Input terminal for tracking-zero cross comparator.
50	TDFCT	I	Capacitor connection pin for the time constant used when there is defect.
51	VC	O	Output terminal for DC voltage reduced to half of VCC+VEE.
52	FZC	I	Input terminal for focus-zero cross comparator.

Pin No.	Pin Name	I/O	Description
1	NC	—	No connection.
2	VSS	—	GND.
3	CD BCK	I	Bit clock input from CD DSP.
4	CD DATA	I	Data input from CD DSP.
5	CD LRCK	I	LRCK input from CD DSP.
6	CD C2PO	I	C2 pointer input from CD DSP.
7-9	NC	—	No connection.
10-15	MD0-MD5	I/O	DRAM/ROM interface. (DATA)
16	VSS	—	Ground.
17	MD6	I/O	DRAM/ROM interface. (DATA)
18	VDD3	—	Power supply 3.3V.
19	MD7	I/O	DRAM/ROM interface. (DATA)
20	VSS	—	Ground.
21	MD8	I/O	DRAM/ROM interface. (DATA)
22	VDD3	—	Power supply 3.3V.
23-29	MD9-MD15	I/O	DRAM/ROM interface. (DATA)
30-36	NC	—	No connection.
37	<u>MCE</u>	—	ROM chip enable.
38	<u>MWE</u>	O	DRAM write enable.
39	VSS	—	Ground.
40	<u>CAS</u>	O	DRAM/ROM interface.
41	VDD3	—	Power supply 3.3V.
42	<u>RASO</u>	O	DRAM/ROM interface.
43	<u>RASI</u>	O	
44-46	MA10-MA8	O	DRAM/ROM interface. (Address)
47	VSS	—	Ground.
48	MA7	O	DRAM/ROM interface. (Address)
49	VDD3	—	Power supply 3.3V.
50-52	MA6-MA4	O	DRAM/ROM interface. (Address)
53	VSS	—	Ground.
54	MA3	O	DRAM/ROM interface. (Address)
55	VDD3	—	Power supply 3.3V.
56-58	MA2-MA0	O	DRAM/ROM interface. (Address)
59	PGIO7	I/O	Programmable I/O.
60	<u>RESET</u>	I	Reset input.
61	VDD MAX IN	—	Power supply - VDDMAX. (5.0V)
62-64	NC	—	No connection.
65	AGND DAC	—	Analog ground.
66	A VDD DAC	—	Analog power supply (DAC) : 3.3V.
67	COMP OUT	O	Composite out.
68	AGND DAC	—	Analog ground.

Pin No.	Pin Name	I/O	Description
69	Y OUT	O	Video signal "Y" OUT.
70	AVDD DAC	—	Analog power supply (DAC) 3.3V.
71	AGND DAC	—	Analog ground.
72	R REF	I	Reference resistor input.
73	V REF	I	Voltage reference input.
74	AVDD DAC	—	Analog power supply (DAC) 3.3V.
75	C OUT	O	Video signal "C"out.
76	AGND DAC	—	Analog ground.
77-79	CLK SEL0-2	I	Clock selection input.
80	VSS	—	Ground.
81	CLK SEL3	I	Clock selection input.
82	VDD3	—	Power supply 3.3V.
83, 84	CLK SEL4, 5	I	Clock selection input.
85	AGND PLL	—	Analog ground.
86	DA XCK	I	DA XCK (16.933MHz) input.
87	AVDD PLL	—	Analog power supply 3.3V.
88	DA EMP	O	DAC-emphasis output.
89, 90	PGIO5, O6	I/O	Programmable I/O.
91	PGIO0	I/O	
92	PGIO8	I/O	
93	$\bar{V}SYNC/CSYNC$	O	$\bar{V}SYNC/CSYNC$ output.
94	AVDD PLL	—	Analog power supply (PLL) 3.3V.
95	NC	—	Not connected.
96	NC	—	Not connected.
97	NC	—	Not connected.
98	AGND PLL	—	Analog ground.
99	VSS	—	Ground.
100	NC	—	Not connected.
101	$\bar{H}SYNC$	O	$\bar{H}SYNC$ output.
102	VDD3	—	Power supply 3.3V.
103	VCK OUT	O	VCK out.
104	VSS	—	Ground.
105	GCK	I	Global clock signal input. (42.3MHz)
106	VCK IN	I	Video clock signal input. (27.0MHz)
107	GCK OUT	O	Global clock signal output. (27.0MHz)
108	DA LRCK	O	DAC-LRCK output.
109	VDD MAX OUT	—	Power supply (VDD MAX) : 5.0V.
110	DA DATA	O	DAC-PCM data output.
111	DA BCK	O	DAC-BIT clock output.
112	HD OUT	O	Micon interface. (Data out)
113	HRDY	O	Micon interface. (Host ready)

Pin No.	Pin Name	I/O	Description
114	<u>HINT</u>	O	Micon interface. (Host interrupt)
115	CDG SCK	I	CD-G serial clock input.
116	VSS	—	Ground.
117	HCK	I	Micon interface. (Host clock)
118	VDD3	—	Power supply 3.3V.
119	HD IN	I	Micon interface. (Host data in)
120	VDD3	—	Power supply 3.3V.
121	HSEL	I	Micon interface. (Host select in)
122	CDG SDATA	I	CD-G data input.
123	CDG VFSY	I	CD-G VFSY input.
124	CDG SOSI	I	CD-G SOSI input.
125-128	NC	—	Not connected.

Pin No.	Pin Name	I/O	Description
1	FOK	I	Focus OK input. Used for SENS output and the servo auto sequencer.
2	FSW	O	Spindle motor output filter switching output.
3	MON	O	Spindle motor on/off control output.
4	MDP	O	Spindle motor servo control.
5	MDS	O	
6	LOCK	O	High, when sampled value of GFS at 460Hz is high. Low, when sampled value of GFS at 460Hz is low by 8 times successively.
7	NC	—	Not used.
8	VCOO	O	Analog EFM PLL oscillation circuit output.
9	VCOI	I	Analog EFM PLL oscillation circuit input. fLOCK=8.6436MHz.
10	TEST	I	TEST pin.
11	PDO	O	Analog EFM PLL charge pump output.
12	VSS	—	GND.
13	PWMI	I	Spindle motor external control input.
14	V16M	O	VCO2 oscillation output for the wide-band EFM PLL.
15	VCTL	I	VCO2 control voltage input for the wide-band EFM PLL.
16	VPCO	O	Wide-band EFM PLL charge pump output.
17	VCKI	I	VCO2 oscillation input for the wide-band EFM PLL.
18	FILO	O	Multiplier PLL (slave=digital PLL) filter output.
19	FILI	I	Multiplier PLL filter input.
20	PCO	O	Multiplier PLL charge pump output.
21	AVSS	—	Analog GND.
22	CLTV	I	Multiplier VCO1 control voltage input.
23	AVDD	—	Analog power supply (5V).
24	RF	I	EFM signal input.
25	BIAS	I	Constant current input of the asymmetry circuit.
26	ASYI	I	Asymmetry comparator voltage input.
27	ASYO	O	EFM full-swing output.
28	ASYE	I	Low: asymmetry circuit off; high: asymmetry circuit on.
29	NC	—	Not used.
30	PSSL	I	Audio data output mode switching input. Low: serial output; high: parallel output.
31	WDCK	O	D/A interface for 48-bit slot. Word clock f=2Fs.
32	LRCK	O	D/A interface for 48-bit slot. LR clock f=Fs.
33	VDD	—	Power supply (5V).
34	DATA	O	DA16 (MSB) output when PSSL=1. 48-bit slot serial data (two's complement, MSB first) when PSSL=0.
35	BCK	O	DA15 output when PSSL=1. 48-bit slot bit clock when PSSL=0.
36	DATA64	O	DA14 output when PSSL=1. 64-bit slot serial data (two's complement, LSB first) when PSSL=0.
37	BCK64	O	DA13 output when PSSL=1. 64-bit slot bit clock when PSSL=0.
38	LRCK64	O	DA12 output when PSSL=1. 64-bit slot LR clock when PSSL=0.

Pin No.	Pin Name	I/O	Description
39	GTOP	O	DA11 output when PSSL=1. GTOP output when PSSL=0.
40	XVCF	O	DA10 output when PSSL=1. XVCF output when PSSL=0.
41	XPCLK	O	DA09 output when PSSL=1. XPLCK output when PSSL=0.
42	GFS	O	DA08 output when PSSL=1. GFS output when PSSL=0.
43	RFCK	O	DA07 output when PSSL=1. RFCK output when PSSL=0.
44	C2PO	O	DA06 output when PSSL=1. C2PO output when PSSL=0.
45	XROF	O	DA05 output when PSSL=1. XRAOF output when PSSL=0.
46	MNT3	O	DA04 output when PSSL=1. MNT3 output when PSSL=0.
47	MNT2	O	DA03 output when PSSL=1. MNT2 output when PSSL=0.
48	MNT1	O	DA02 output when PSSL=1. MNT1 output when PSSL=0.
49	MNT0	O	DA01 output when PSSL=1. MNT0 output when PSSL=0.
50	APTR	O	Aperture compensation control output. This pin outputs a high signal when the right channel is used.
51	APTL	O	Aperture compensation control output. This pin outputs a high signal when the left channel is used.
52	VSS	—	GND.
53	XTAI	I	Crystal oscillation circuit input.
54	XTAO	O	Crystal oscillation circuit output.
55	XTSL	I	Crystal selector input.
56	FSTT	O	2/3 frequency divider output for Pins 53 and 54.
57	FSOF	O	1/4 frequency divider output for Pins 53 and 54.
58	C16M	O	16.9344MHz output. (V16M output in CLV-W and CAV-W modes)
59	MD2	I	Digital-out on/off control. High: on; low: off
60	DOUT	O	Digital-out output.
61	EMPH	O	Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.
62	WFCK	I	WFCK (write frame clock) output.
63	SCOR	O	Outputs a high signal when either subcode sync S0 or S1 is detected.
64	SBSO	O	Sub P to W serial output.
65	EXCK	I	SBSO readout clock input.
66	SQSO	O	Sub Q 80-bit and PCM peak, level meter and internal status outputs.
67	SQCK	I	SQSO readout clock input.
68	D MUTE	I	High: mute; low: release
69	SENS	—	SENS output to CPU.
70	XRST	I	System reset. Reset when low.
71	DATA	O	Serial data input from CPU.
72	XLAT	O	Latch input from CPU. Serial data is latched at the falling edge.
73	VDD	—	Power supply (5V).
74	CLOK	O	Serial data transfer clock input from CPU.
75	SEIN	I	SENS input from SSP.
76	CNIN	I	Track jump count signal input.

Pin No.	Pin Name	I/O	Description
77	DATO	O	Serial data output to SSP.
78	XLTO	O	Serial data latch output to SSP. Latched at the falling edge.
79	CLKO	O	Serial data transfer clock output to SSP.
80	MIRR	I	Mirror signal input. Used when the number of tracks is 128 or more for the 2N-track jump and M track move of the auto sequencer.

Notes)

- The 64-bit slot is an LSB first, two's complement output, and the 48-bit slot is an MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window open.)
- XUGF is the negative pulse for the frame sync obtained from the EFM signal. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- GFS goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136μ.
- C2PO represents the data error status.
- XRAOF is generated when the 32K RAM exceeds the ±28F jitter margin.

Pin No.	Pin Name	I/O	Description
1	VSS1	—	GND connection terminal. (Digital ground terminal).
2	Xtal IN	I	External X'tal and capacitor for internal sync generator, or the external clock are connected to this terminal. (2fsc or 4fsc).
3	Xtal OUT	O	
4	CTRL1	I	Either the external clock input mode or the X'tal generator mode is selected by this selector terminal. L: X'tal generator mode, H: External clock input.
5	BLANK	O	Blank signal (character and the green ORed signal) is output from this terminal. (MODE 0: composite sync signal is output at H.) When reset (\overline{RST} terminal = L), the X'tal clock signal is output. (It is not output when reset by the reset command).
6	OSC IN	I	External coil and capacitor for the character output dot clock generator are connected to this terminal.
7	OSC OUT	O	
8	CHARA	O	The character signal is output from this terminal. (MOD 0: when H, the external sync signal identification signal is output from this terminal. This output signal tells whether the external sync signal is present or not. When external sync signal is present, H is output.) When reset (\overline{RST} terminal = L), the dot clock signal (LC oscillator) is output. (It is not output when reset by the reset command).
9	CS	I	Enable signal for the serial data input is input to this terminal. The serial data input is enabled at L. Pull-up resistor is built-in. (Hysteresis input).
10	SCLK	I	Clock of the serial data input is input to this terminal. Pull-up resistor is built-in. (Hysteresis input).
11	SIN	I	Serial data input terminal. Pull-up resistor is built-in. (Hysteresis input).
12	VDD2	—	Power supply for the composite video signal level adjustment. (Analog power supply).
13	CV OUT	O	Composite video signal output terminal.
14	NC	—	Connected to GND or not connected.
15	CV IN	I	Composite video signal input terminal.
16	VDD1	—	Power supply (+5V digital power supply).
17	SYN IN	I	Video signal for the internal sync separator circuit is input to this terminal. (When the internal sync separator circuit is not used, the horizontal sync signal or composite sync signal is input to this terminal).
18	SEP C	—	Internal sync separator circuit bias voltage monitoring terminal.
19	SEP OUT	O	The composite sync output signal of the internal sync separator circuit is output from this terminal. (H: MOD 1. H: during internal sync mode. L: during external sync mode.) (When internal sync separator circuit is not used, the SYN IN input signal is output from this terminal).
20	SEP IN	I	The output signal of the SEP OUT terminal is integrated so that the vertical sync signal is input to this terminal. An integrator circuit must be connected between the SEP OUT terminal and this terminal. When this terminal is not used, it must be connected to VDD1.
21	CTRL2	I	When selecting any of the NTSC or PAL or PAL-M or PAL-N system, the pin setting has priority. When L, the NTSC system is selected after resetting. Selection of either NTSC or PAL or PAL-M or PAL-N system by the command becomes effective. H: PAL-M system.
22	CTRL3	I	Controls whether or not to input the <u>VSYNC</u> signal to the SEPIN input. L: to input the <u>VSYNC</u> signal. H: not to input the <u>VSYNC</u> signal.

Pin No.	Pin Name	I/O	Description
23	<u>RST</u>	I	System reset input terminal. Pull-up resistor is built-in. (Hysteresis input).
24	VDD1	—	Power supply. (+5V digital power supply).

IC, SM5878AM

Pin No.	Pin Name	I/O	Description
1	MUTE	I	MODE = H: Soft mute ON/OFF terminal. (Mute at H). MODE = L: Attenuator level DOWN/UP terminal. (DOWN at H).
2	DEEM	I	De-emphasis ON/OFF terminal. (De-emphasis ON at H).
3	MCKO	O	Oscillator clock output. (16.9344 MHz).
4	DVSS	—	Digital VSS terminal.
5	BCKI	I	Bit clock input terminal.
6	DI	I	Serial data input terminal.
7	DVDD	—	Digital VDD terminal.
8	LRCI	I	Sample rate clock (fs) input terminal. (H = L ch/L = R ch).
9	TSTN	I	Test input. (“H” or open during normal operation)
10	TO1	O	Test output 1. (Normally low level output).
11	AVDDL	—	Analog VDD terminal. (For L ch).
12	LO	O	Left channel analog output terminal.
13	AVSS	—	Analog VSS terminal.
14	RO	O	Right channel analog output terminal.
15	AVDDR	—	Analog VDD terminal. (For R ch).
16	MUTEO	O	Infinity zero detection output.
17	XVDD	—	X’tal system VDD terminal.
18	XTI	I	X’tal oscillator terminal. (Or external clock input terminal of 16.9344 MHz).
19	XTO	O	X’tal oscillator terminal.
20	XVSS	—	X’tal system VSS terminal.
21	DS	I	Double-speed/normal playback selection. (Double-speed at H).
22	RSTN	I	Reset terminal. (Reset at L).
23	MODE	I	Soft mute/Attenuator mode selection. (Soft mute at H).
24	ATCK	I	Attenuator level setup clock (Ignored when MODE = H).

IC, μPD78016FGC-583

Pin No.	Pin Name	I/O	Description
1	RBPLS	O	RADIAL BALANCE PLUS.
2	AMUTE	O	AUDIO ANALOG MUTE (H=MUTE ON).
3	GFS	I	GFS.
4	XVCDMD	O	AUDIO/VIDEO CD MODE (L=VCD=SPINDLE GAIN UP).
5	MD2	O	DOUT MUTE CONT.
6	EMPH	I	EMPHASIS.
7	SQSO	I	SQDATA FROM CD.
8	SQCK	O	SQCLK TO CD.
9	VSS	—	GND.
10	SWNT	I	SW TV OUT MODE (L=NTSC).
11	SWAUTO	I	SW TV OUT MODE (L=NTSC/PAL AUTO).
12	SWPAL	I	SW TV OUT MODE (L=PAL).
13	EMERG	I	POWER EMERGENCY STOP (L≠3sec=STOP).
14	SHUTTER	—	CDRW:H
15	NC	—	Not used.
16	NC	—	Not used.
17	LOCK	O	GFS (FRAME SYNC) LOCK (NO USE=H).
18	DMUTE	O	DIGITAL DATA OUT MUTE.
19	SENS	I	DSP SENS1 FROM CD.
20	XCDRST	O	CD RESET.
21	DATA	O	DATA TO CD.
22	XLAT	O	XLT TO CD.
23	CLOK	O	CLK TO CD.
24	VSS	—	GND.
25	FOK	I	FOCUS OK.
26	SENS2	I	SSP SENS2 FROM CD.
27	XBUSY	I/O	READY/BUSY I/O TO HOST OD.
28	SW CDRW	—	Not used.
29	FG DOWN	—	Not used.
30	NC	—	Not connected
31	TST0	I/O	CHECK LAND.
32	TST1	I/O	
33	TST2	I/O	
34	TST3	I/O	
35	RESET	I	RESET.
36	HRDY	I	HRDY FROM CL680.
37	XHINT	I	XHINT FROM CL680.
38	NC	—	Not connected
39	SCOR	I/O	SCOR FROM CD.
40	VDD	—	5.0VDD.
41	XO	O	8.0MHz CERALOCK.

Pin No.	Pin Name	I/O	Description
42	XI	I	8.0MHz CERALOCK.
43	VSS	—	GND.
44	XT2	—	Not used.
45	XT1	I	5.0VDD.
46	AVSS	—	GND.
47	XMPGRST	O	MPEG BLOCK IC RESET.
48	HSEL	O	ADDRESS/DATA SEL TO CL680.
49	INLSW	I	INSIDE LIMIT SW .
50	NC	—	Not used.
51	OSDXCS	O	OSD CHIP SELECT.
52	ABSEL	I	CXA1992A/B SELECT (L=CXA1992A).
53	CLVSEL	I	CLV MODE SELECT (H=CLV-N).
54	AADSEL	I	AUTO ADJUST SELECT (H=AUTO ON).
55	AVDD	—	5.0VDD.
56	AVREF	—	
57	HDOUT	I	HD-OUT FROM CL680.
58	HDIN	O	HD-IN FROM CL680.
59	HCK	O	HCK TO CL680.
60	OSDDATA	O	OSD DATA.
61	OSDCLK	O	OSD CLOCK.
62	COMMAND	I	COMMAND FROM HOST .
63	STATUS	O	STATUS TO HOST.
64	SCK	I	SCK FROM HOST.

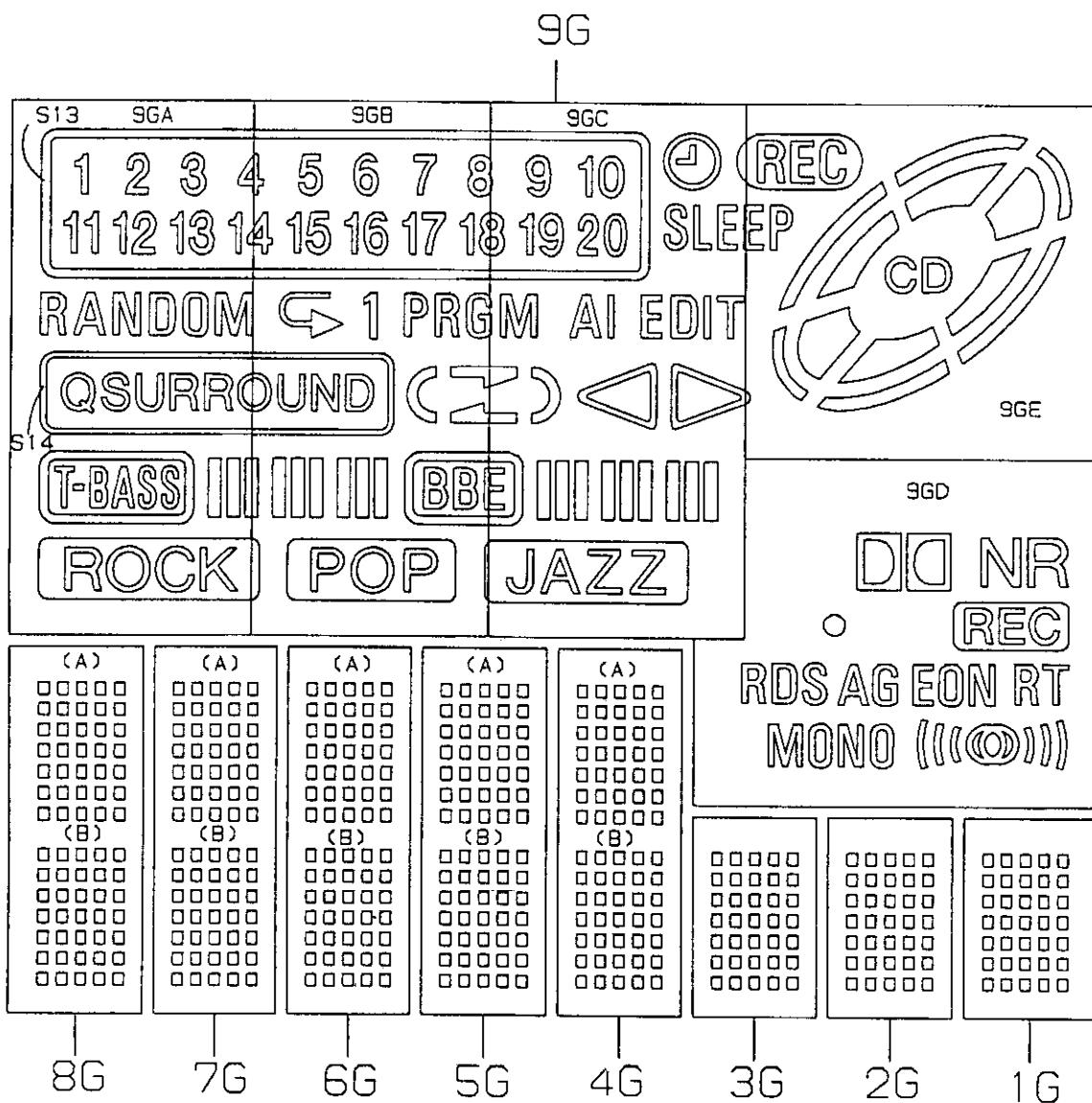
Pin No.	Pin Name	I/O	Description
1	<u>APCOFF</u>	O	Laser output control terminal (L: ON, H: OFF)
2	PF4	-	Not used
3	PF5	-	Not used
4	<u>SSTP</u>	I	RESET switch detection input L: RESET SW closed; H: RESET SW open. The reference position is determined when 'L' changes to 'H'. (Not used)
5	<u>LD ON</u>	O	RF amp mode control output L: CD-ROM laser ON; H: CD-RW laser ON; Hiz: Laser OFF
6	FOK	I	FOK signal input from CXD2587Q
7	GFS	I	GFS signal input from CXD2587Q
8	SCLK	O	Serial clock output to CXD2587Q for reading SENS serial data (Not used)
9	SENS	I	SENS serial data input to CXD2587Q
10	<u>CLOK</u>	O	Clock output for transferring serial data to CXD2587Q (Not used)
11	<u>XLAT</u>	O	Latch signal output to CXD2587Q. Latches serial data at the trailing edge. (Not used)
12	DATA	O	Serial data output to CXD2587Q (Not used)
13	SYSM	O	Muting output to CXD2587Q. L: Muting OFF; H: Muting ON (Not used)
14	EJ0	I	For setting the amount of 12-cm disc to come out when it is ejected (Not used)
15	EJ1		
16	EJ2	I	For setting the amount of 8-cm disc to come out when it is ejected (Not used)
17	EJ3		
18	OPO	I	Detects 8-cm compatible mechanism L: 8-cm compatible mechanism; H: 12-cm exclusive mechanism
19	PC5	-	Not used
20	PC6	-	Not used
21	PC7	-	Not used
22	TEST1	O	Used for debugging (Not used)
23	PH1	-	Not used
24	PH2	-	Not used
25	TEST2	O	Used for debugging (Not used)
26	TEST3		
27	TEST4		
28	<u>DPSON</u>	O	Output to control power ON/OFF of RF amp and signal processing LSI (CXD2587Q) L: Power ON; H: Power OFF (Not used)
29	<u>XRST</u>	O	Reset output to CXD2587Q (reset with 'L'). After the power supply of signal processing LSI (CXD2587Q) turns on, this pin is set to 'H' to release reset. (Not used)
30	<u>RESET</u>	I	System reset input terminal
31	EXTAL	I	Crystal oscillator circuit input
32	XTAL	O	Crystal oscillator circuit output
33	VSS	-	Ground
34	TX	O	Not used
35	TEX	I	Not used
36	AVSS	-	Ground (A/D converter)
37	AVREF	-	Reference voltage input (A/D converter)
38	FEMEAS	I	Not used

Pin No.	Pin Name	I/O	Description
39	FEMEAS	I	Not used
40	FEMEAS	I	FE level (S-curve) measurement A/D input for detecting CD-ROM or CD-RW
41	TEST	I	Test mode select port
42	KEY2	I	Test mode key input (A4)
43	KEY3	I	Test mode key input (A5)
44	PA6/AN6	I	Not used
45	PA7/AN7	I	Not used
46	PBO/CINT	I	Not used
47	<u>SRQ</u>	O	Serial data request output to system microprocessor
48	SCK	I	Clock input from system microprocessor for serial communications
49	D MS CD	I	Serial data input from system microprocessor
50	D CD MS	O	Serial data output to system microprocessor
51	SQCK	O	Clock output to CXD2587Q for reading SQSO (Not used)
52	SQSO	I	Sub-Q serial data input from CXD2587Q
53	PB7/SO1	O	Not used
54	PE0/EC0	I	Not used
55	PE1/EC1	I	Not used
56	PE2/RMC	I	Not used
57	PE3/NM1	I	Not used
58	PE4/PWM	O	Not used
59	PE5/TO	O	Not used
60	<u>SLEEP</u>	I	Interrupt input for controlling microprocessor sleep mode (CPU issues STOP command) L: CPU sleep status; H: CPU operational status (sleep mode is released by the leading edge)
61	<u>CS</u>	I	Interrupt input for serial communication request from system microprocessor (leading edge is detected)
62	SCOR	I	Sub-code sync input from CXD2587Q
63	DISC IN	I	Disc insertion detection switch input. Detected during usual operation With 8-cm disc: No disc: L; When inserted: H, After chucking: L (Caution: The no-disc status is the same as the after-chucking status.)
64	P14	I	Not used
65	P15	I	Not used
66	2SPEED	I	Standard/double-speed playback mode switching input (set when reset is released) L: Standard play; H: Double speed play
67	ROM	I	CD-ROM mode setting input (set when reset is released) L: Audio mode; H: CD-ROM mode
68	FIN	O	Loading motor driver control output
69	RIN	O	Stop: FIN=L, RIN=L, Loading: FIN=H, RIN=L, Eject: FIN=L, RIN=H
70	PG2	I	Not used
71	SW4	I	End detection when 12-cm disc is ejected
72	VDD	I	Not used
73	NC	-	Not used
74	SW3	I	Disc, chucking, release detection

Pin No.	Pin Name	I/O	Description
75	SW2	I	12-cm disc detection. End detection when 12-cm disc is ejected.
76	PG6	O	Not used
77	PG7	I	Not used
78	PF0	I	Not used
79	PF1	I	Not used
80	PF2	I	Not used

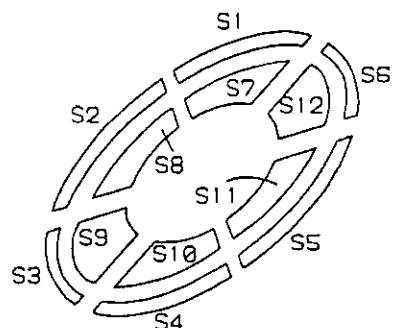
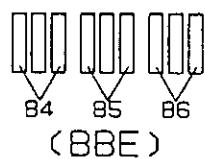
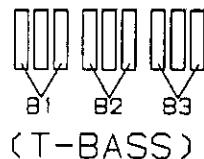
LCD DISPLAY

FL (9-ST-19GONK) GRID ASSIGNMENT AND ANODE CONNECTION



GRID ASSIGNMENT

1-1	2-1	3-1	4-1	5-1
1-2	2-2	3-2	4-2	5-2
1-3	2-3	3-3	4-3	5-3
1-4	2-4	3-4	4-4	5-4
1-5	2-5	3-5	4-5	5-5
1-6	2-6	3-6	4-6	5-6
1-7	2-7	3-7	4-7	5-7

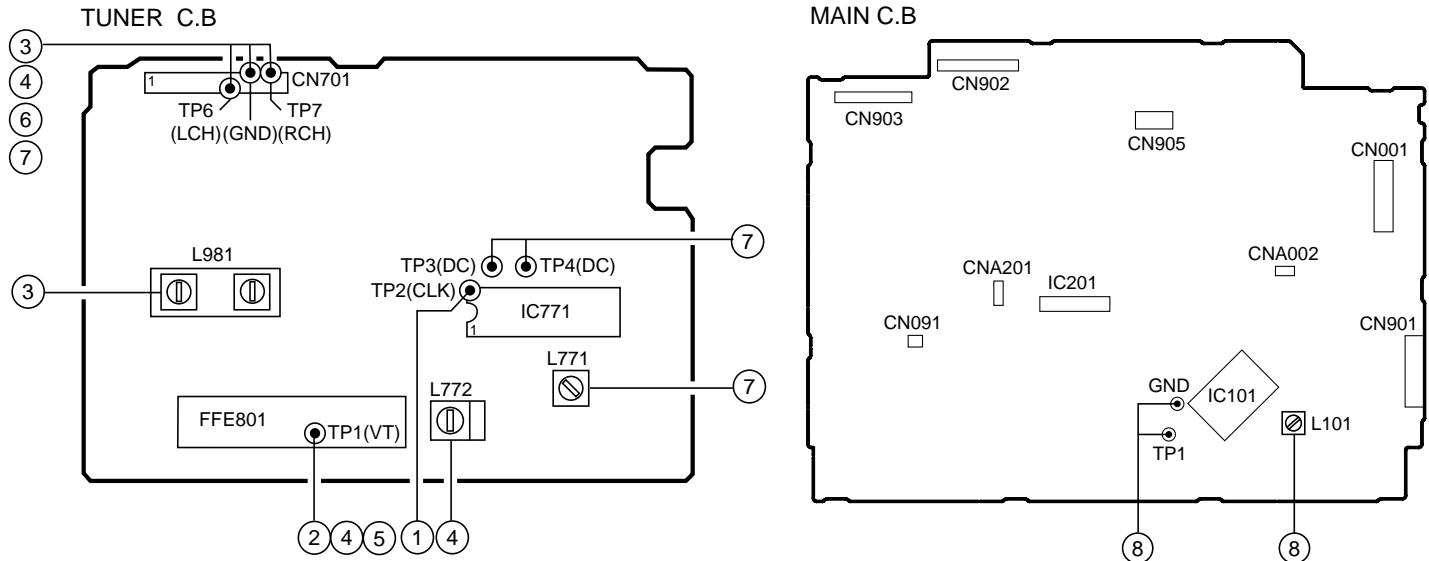


(8G~1G)

ANODE CONNECTION

	1G	2G	3G	4G	5G	6G	7G	8G	9G(A~E)
P1	-	-	-	1-1A	1-1A	1-1A	1-1A	1-1A	ROCK
P2	-	-	-	2-1A	2-1A	2-1A	2-1A	2-1A	POP
P3	-	-	-	3-1A	3-1A	3-1A	3-1A	3-1A	JAZZ
P4	-	-	-	4-1A	4-1A	4-1A	4-1A	4-1A	1
P5	-	-	-	5-1A	5-1A	5-1A	5-1A	5-1A	11
P6	-	-	-	1-2A	1-2A	1-2A	1-2A	1-2A	2
P7	-	-	-	2-2A	2-2A	2-2A	2-2A	2-2A	12
P8	-	-	-	3-2A	3-2A	3-2A	3-2A	3-2A	3
P9	-	-	-	4-2A	4-2A	4-2A	4-2A	4-2A	13
P10	-	-	-	5-2A	5-2A	5-2A	5-2A	5-2A	4
P11	-	-	-	1-3A	1-3A	1-3A	1-3A	1-3A	14
P12	-	-	-	2-3A	2-3A	2-3A	2-3A	2-3A	5
P13	-	-	-	3-3A	3-3A	3-3A	3-3A	3-3A	15
P14	-	-	-	4-3A	4-3A	4-3A	4-3A	4-3A	S13
P15	-	-	-	5-3A	5-3A	5-3A	5-3A	5-3A	6
P16	-	-	-	1-4A	1-4A	1-4A	1-4A	1-4A	16
P17	-	-	-	2-4A	2-4A	2-4A	2-4A	2-4A	7
P18	-	-	-	3-4A	3-4A	3-4A	3-4A	3-4A	17
P19	-	-	-	4-4A	4-4A	4-4A	4-4A	4-4A	8
P20	-	-	-	5-4A	5-4A	5-4A	5-4A	5-4A	18
P21	-	-	-	1-5A	1-5A	1-5A	1-5A	1-5A	9
P22	-	-	-	2-5A	2-5A	2-5A	2-5A	2-5A	19
P23	-	-	-	3-5A	3-5A	3-5A	3-5A	3-5A	10
P24	-	-	-	4-5A	4-5A	4-5A	4-5A	4-5A	20
P25	-	-	-	5-5A	5-5A	5-5A	5-5A	5-5A	RANDOM
P26	-	-	-	1-6A	1-6A	1-6A	1-6A	1-6A	C
P27	-	-	-	2-6A	2-6A	2-6A	2-6A	2-6A	1
P28	-	-	-	3-6A	3-6A	3-6A	3-6A	3-6A	PRGM
P29	-	-	-	4-6A	4-6A	4-6A	4-6A	4-6A	T-BASS
P30	-	-	-	5-6A	5-6A	5-6A	5-6A	5-6A	B1
P31	-	-	-	1-7A	1-7A	1-7A	1-7A	1-7A	B2
P32	-	-	-	2-7A	2-7A	2-7A	2-7A	2-7A	B3
P33	-	-	-	3-7A	3-7A	3-7A	3-7A	3-7A	BBE
P34	-	-	-	4-7A	4-7A	4-7A	4-7A	4-7A	B4
P35	-	-	-	5-7A	5-7A	5-7A	5-7A	5-7A	B5

ADJUSTMENT < TUNER, MAIN SECTION >



1. Clock Frequency Check

Settings : • Test point : TP2 (CLK)
Method : Set to MW 1602kHz and check that the test point is $2052\text{kHz} \pm 45\text{Hz}$.
2. MW VT Check

Settings : • Test point : TP1 (VT)
Method : Set to MW 1602kHz and check that the test point is less than 8.0V. Then set to MW 531kHz and check that the test point is more than 0.6V.
3. MW Tracking Adjustment

Settings : • Test point : TP6 (Lch), TP7 (Rch)
• Adjustment location : L981 (1/3)
Method : Set to MW 999kHz and adjust L981 (1/3) so that the test point becomes maximum.
4. AM IF Adjustment

Settings : • Test point : TP6 (Lch), TP7 (Rch)
• Adjustment location :
L772 450kHz
5. FM VT Check

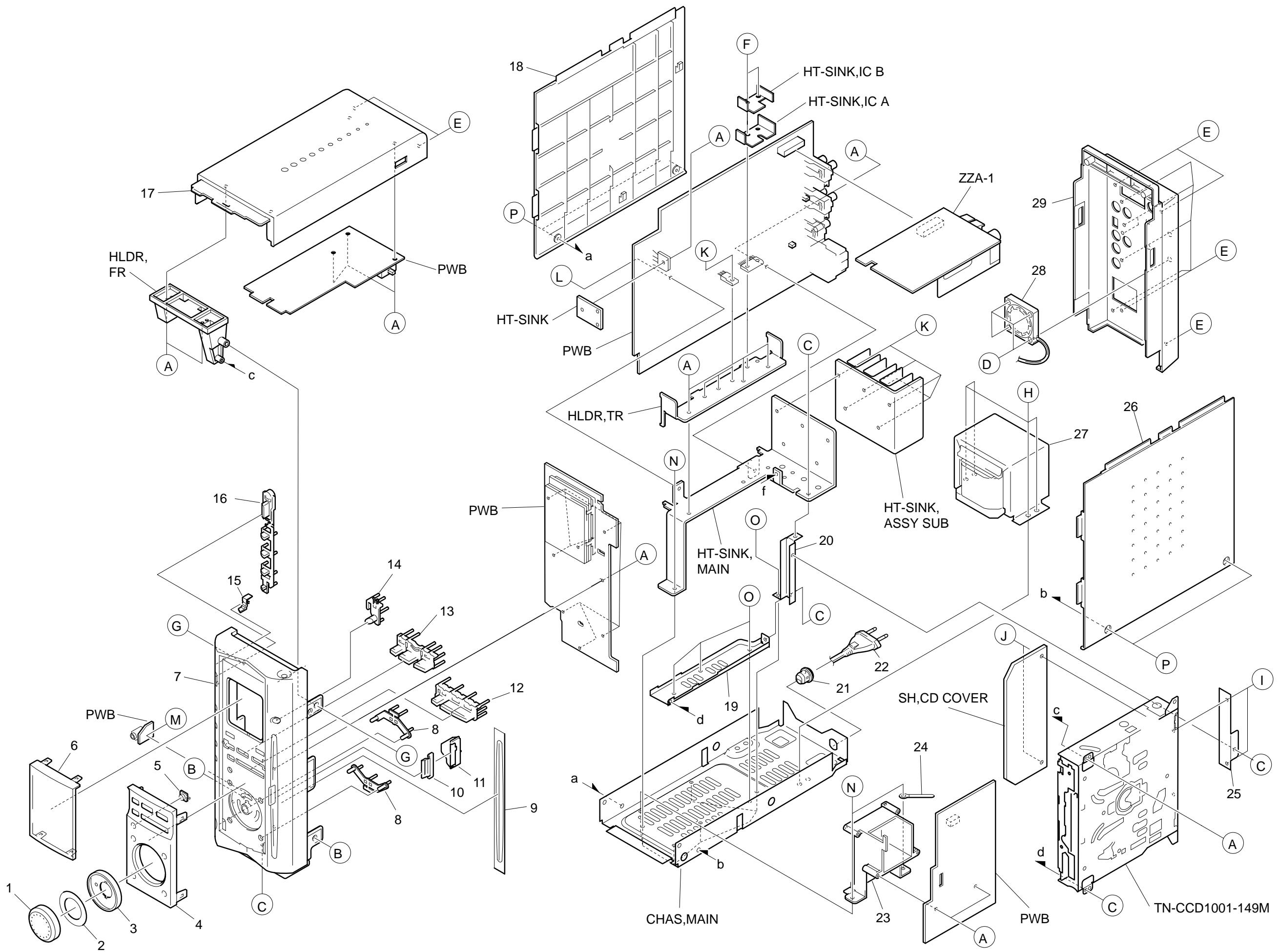
Settings : • Test point : TP1 (VT)
Method : Set to FM 108.0MHz and check that the test point is less than 8.0V. Then set to FM 87.5 MHz and check that the test point is more than 0.5V.
6. FM Tracking Check

Settings : • Test point : TP6 (Lch), TP7 (Rch)
Method : Set to FM 98.0MHz and check that the test point is less than 13dB μ V.
7. DC Balance / Mono Distortion Adjustment

Settings : • Test point : TP3,TP4 (DC balance)
TP6 (Lch), TP7 (Rch) (Distortion)
• Adjustment location : L771
• Input level : 60dB μ V
Method : Set to FM 98.0MHz and adjust L771 so that the voltage between TP3 and TP4 becomes $0V \pm 0.04V$. Next, check that the distortion is less than 1.3%.
8. MICON OSC Adjustment

Settings : • Test point : TP1
• Adjustment location : L101
Method : Insert AC plug with pressing TUNER function key. Adjust L101 so that frequency across the test point is $97.258 \pm 0.098 \text{ Hz}$ ($10.292 \sim 10.272 \text{ ms}$)

MECHANICAL EXPLODED VIEW 1/1



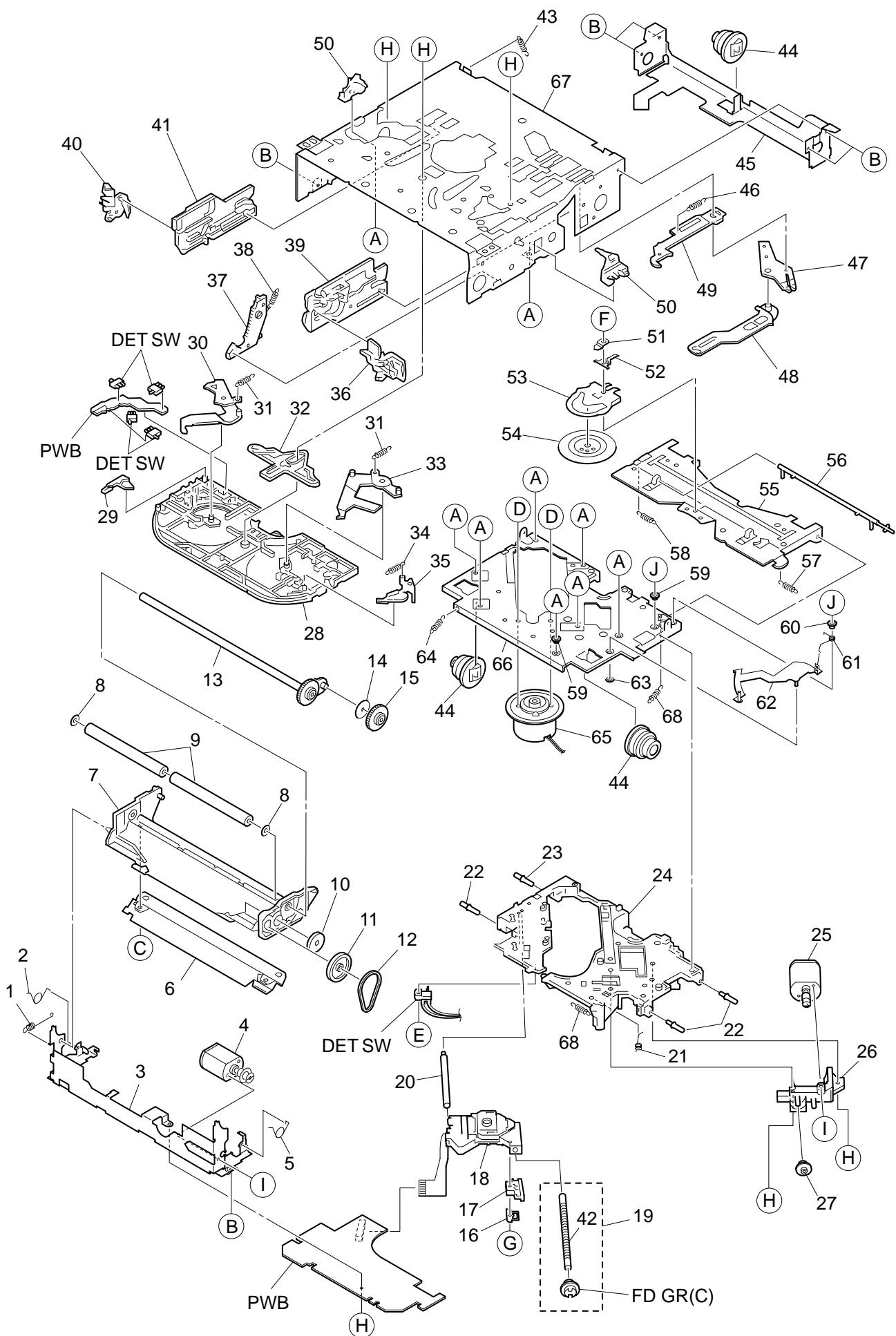
MECHANICAL MAIN PARTS LIST 1/1

REF. NO	PART NO.	KANRI NO.	DESCRIPTION	REF. NO	PART NO.	KANRI NO.	DESCRIPTION
1	8A-CJ5-016-010		KNOB,RTRY JOG	26	8A-CJ5-005-110		PANEL,SIDE R
2	8A-CJ5-217-010		PLATE,JOG	27	8A-CJ5-624-010		PT,ACJ-5 HE
3	8A-CJ5-017-010		REFLECTOR,JOG	28	8Z-CL1-663-010		FAN,MF40D-12-200MM
4	8A-CG5-004-010		PANEL,FR	29	8A-CG5-003-010		CABI,REAR H
5	8A-CJ5-019-010		LENS,SENSOR	A	87-067-579-010		TAPPING SCREW, BVT2+3-8
6	8A-CJ5-007-010		WINDOW,DISPLAY	B	87-591-094-410		TAPPING SCREW, QIT+3-6
7	8A-CG5-001-010		CABI,FR H	C	87-067-688-010		BVTT+3-6
8	8A-CJ5-012-010		KEY,ENTER	D	87-751-098-410		SCREW 3X14
9	8A-CJ5-023-010		DUST COVER, CD FELT	E	87-067-660-010		TAPPING SCREW, BVT2+3-8
10	8A-CJ5-018-010		REFLECTOR,CD	F	87-067-581-010		TAPPING SCREW, BVT2+3-15
11	8A-CJ5-215-010		GUIDE,LED CD	G	87-721-096-410		QT2+3-10 GLD
12	8A-CJ5-010-010		KEY,SKIP	H	87-078-199-010		S-SCREW, ITC+4-10 R
13	8A-CJ5-011-010		KEY,PLAY	I	87-067-421-010		VTT+2-4
14	8A-CJ5-013-010		KEY,EJECT CD	J	87-067-767-010		BVTT+2.6-6
15	8A-CJ5-015-010		REFLECTOR,POWER	K	87-067-703-010		TAPPING SCREW, BVT2+3-10
16	8A-CJ5-009-010		KEY,POWER	L	87-NF4-224-010		S-SCREW,IT3B+3-8 CU
17	8A-CG5-002-010		CABI,TOP	M	88-AR1-217-010		S-SCREW,BFT2+3-8
18	8A-CJ5-004-110		PANEL,SIDE L	N	87-B10-315-010		BVIT3B+3-8 R W/O
19	8A-CJ5-205-010		HLDR,CD A	O	87-B10-314-010		BVIT3B+3-6 R W/O
20	8A-CJ5-206-010		HLDR,CD B	P	87-067-641-010		UTT2+3-8 W/O SLOT BLK
△							
21	87-085-185-010		BUSHING, AC CORD (E)				
22	87-A80-092-010		AC CORD ASSY,E BLK SUN FAI				
23	8A-CJ5-204-010		HLDR,ECO				
24	87-064-185-010		HLDR, WIRE				
25	8A-CJ5-213-110		HLDR,MECHA CD				

COLOR NAME TABLE

Basic color symbol	Color	Basic color symbol	Color	Basic color symbol	Color
B	Black	C	Cream	D	Orange
G	Green	H	Gray	L	Blue
LT	Transparent Blue	N	Gold	P	Pink
R	Red	S	Silver	ST	Titan Silver
T	Brown	V	Violet	W	White
WT	Transparent White	Y	Yellow	YT	Transparent Yellow
LM	Metallic Blue	LL	Light Blue	GT	Transparent Green
LD	Dark Blue	DT	Transparent Orange	GM	Metallic Green
YM	Metallic Yellow	DM	Metallic Orange	PT	Transparent Pink
LA	Aqua Blue	GL	Light Green		

CD MECHANISM EXPLODED VIEW 1/1 <TN-CCD1001-149M>



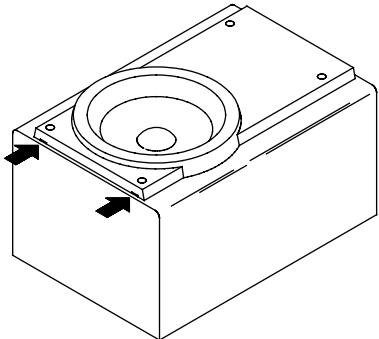
CD MECHANISM MAIN PARTS LIST 1/1 <TN-CCD1001-149M>

REF. NO	PART NO.	KANRI NO.	DESCRIPTION	REF. NO	PART NO.	KANRI NO.	DESCRIPTION
1	S3-031-110-030		EARTH SPR	41	S3-031-010-500		FIX PL(L)Z
2	S3-031-110-180		L.P SPRING(L)	42	S3-031-050-310		FD SCREW(M)
3	S3-031-110-010		FRONT BRKT	43	S3-031-010-620		BARNCE SPRING(LR)
4	S3-031-113-010		LDG MOTOR ASSY	44	S3-031-050-240		DAMPER(J)
5	S3-031-110-190		L.P SPRING(R)	45	S3-031-010-020		REAR D BRKT
6	S3-031-110-050		SUPPORT PL	46	S3-031-010-150		TRIG PL SPRING
7	S3-031-110-080		GR MT BLK	47	S3-031-010-160		TRIG ARM
8	S9-W03-302-760		NW BLUE 2.9-5-0.3	48	S3-031-010-120		TRIG LVR
9	S3-031-110-360		LDG ROLLER(P)	49	S3-031-010-550		TRIG PL(Z)
10	S3-031-110-100		LDG GR(3)	50	S3-031-010-030		DAMPER PIN
11	S3-031-110-090		LDG GR(2)	51	S3-031-050-360		STOPPER SPR
12	S3-031-110-290		LDG BELT	52	S3-031-050-190		8CM STOPPER SPR PL
13	S3-031-113-020		LDG RLR SFT ASSY	53	S3-031-050-230		CLAMPER PLATE
14	S9-W07-101-770		LUMILAR W SHIRO 2.3-9.8-0.1	54	S3-031-050-150		CLAMPER
15	S3-031-110-120		LDG GR(5)	55	S3-031-050-740		CLP ARM(A)
16	S3-031-050-300		NUT PUSH SPR PL(M)	56	S3-031-050-410		8CM STOPPER(M)
17	S3-031-050-290		PU M NUI (M)	57	S3-031-050-140		CLP ARM SPRING
18	S6-904-160-010		PICK-UP VED0375-TN	58	S3-031-050-250		CLP ARM SPR(L)
19	S3-031-053-040		FEED SCREW(M) ASSY	59	S3-031-050-700		D.S ARM COLLAR
20	S3-031-050-320		PU SHAFT(M)	60	S3-031-050-720		SP COLLAR
21	S3-031-050-330		THRUST SPR(M)	61	S3-031-050-710		D.S ARM SPR
22	S3-031-050-210		LOCK PIN	62	S3-031-055-010		DISC SUPPORT ARM ASSY
23	S3-031-050-220		LOCK PIN BL	63	S9-W02-500-900		PW CUT 2.1-4-0.5
24	S3-031-050-760		F.M. BASE(A)	64	S3-031-010-530		HUNG DOWN SPRING(A)
25	S3-031-053-010		FEED MOTOR ASSY	65	S3-031-053-050		SPINDLE MOTOR(M) ASSY
26	S3-031-050-280		FD GR BLK(M)	66	S3-031-050-730		T.T. BASE(A)
27	S3-030-050-100		PU GEAR(B)	67	S3-031-010-010		FRAME
28	S3-031-010-570		UPPER PL(A)	68	S3-031-010-610		BARNCE SPRING(R)
29	S3-031-110-420		SW ACTR(A)	A	87-253-034-410		CAMERA TAPPING SCREW B 3 M2-5
30	S3-031-010-640		SEL ARM(L8)L	B	87-251-033-410		CAMERA SCREW TS G M2-4
31	S3-031-010-540		S ARM SPRING(L8)	C	87-252-033-410		CAMERA B TAPPING SCREW M2-4
32	S3-031-010-080		SEL STOP PL	D	87-267-525-310		CAMERA SCREW M1.7-2.2
33	S3-031-010-430		SEL ARM(R)L	E	87-263-036-010		CAMERA TAPPING SCREW B 3 M2-8
34	S3-031-010-250		S.L ARM SPRING	F	S9-C42-202-010		CAMERA TAPPING SCREW S 3 M2-2
35	S3-031-010-480		S.L ARM(N)	G	S9-C45-175-030		CAMERA TAPPING SCREW P3 M1.7-5
36	S3-031-010-580		FIX ARM(R)A	H	87-351-549-310		CAMERA B TAPPING SCREW M2-5
37	S3-031-010-380		LDG GR(6)B	I	S9-P02-200-310		TAMS SCREW M2-3
38	S3-031-010-220		LDG GR(6)SPRING	J	S9-C04-205-030		CAMERA S TAPPING SCREW M2-5
39	S3-031-010-370		FIX PL(R)B				
40	S3-031-010-340		FIX ARM(L)B				

GENERAL SPEAKER DISASSEMBLY INSTRUCTIONS (FOR REFERENCE)

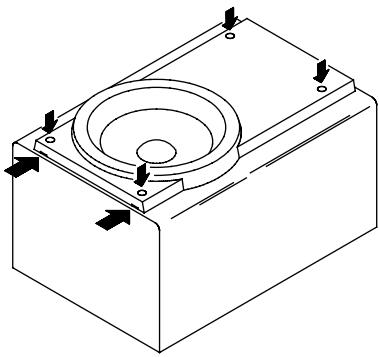
Type.1

Insert a flat-bladed screwdriver into the position indicated by the arrows and remove the panel. Remove the screws of each speaker unit and then remove the speaker units.



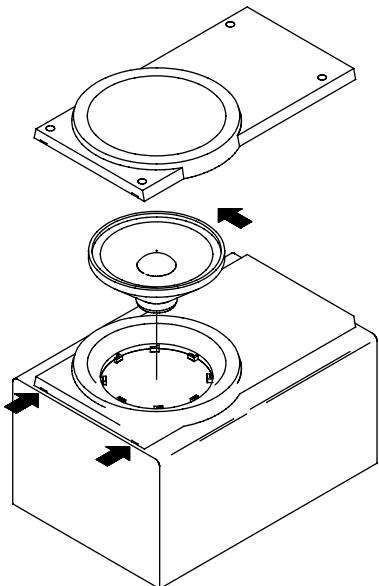
Type.2

Remove the grill frame and four pieces of rubber caps by pulling out with a flat-bladed screwdriver. Remove the screws from hole where installed rubber caps. Insert a flat-bladed screwdriver into the position indicated by the arrows and remove the panel. Remove the screws of each speaker unit and then remove the speaker units.

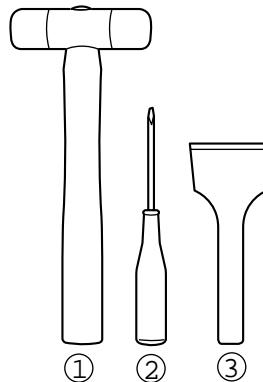


Type.3

Insert a flat-bladed screwdriver into the position indicated by the arrows and remove the panel. Turn the speaker unit to counter-clockwise direction while inserting a flat-bladed screwdriver into one of the hollows around speaker unit, and then remove the speaker unit. After replacing the speaker unit, install it turning to clockwise direction until "click" sound comes out.



Type.4



TOOLS

- ① Plastic head hammer
- ② (⊖) flat head screwdriver
- ③ Cut chisel

How to Remove the PANEL, FR

1. Insert the (⊖) flat head screwdriver tip into the gap between the PANEL, FR and the PANEL, SPKR. Tap the head of the (⊖) flat head screwdriver with the plastic hammer head, and create the clearance as shown in Fig-1.
2. Insert the cut chisel in the clearance, and tap the head of the cut chisel with plastic hammer as shown in Fig-2, to remove the PANEL, FR.
3. Place the speaker horizontally. Tap head of the cut chisel with plastic hammer as shown in Fig-3, and remove the PANEL, FR completely.

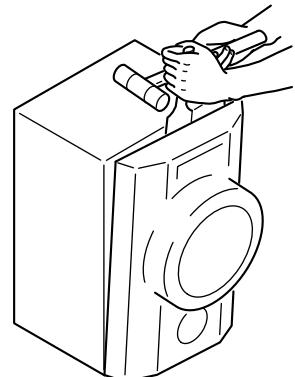
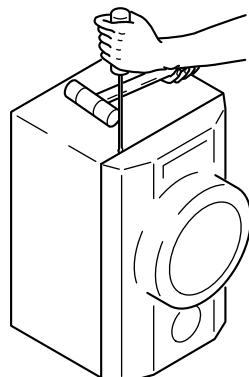


Fig-1

Fig-2

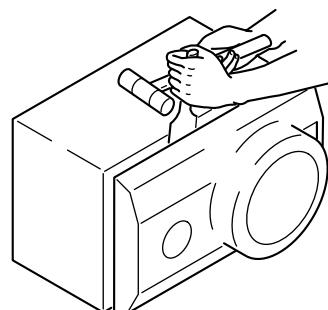


Fig-3

How to Attach the PANEL, FR

Attach the PANEL, FR to the PANEL, SPKR. Tap the four corners of the PANEL, FR with the plastic hammer to fit the PANEL, FR into the PANEL, SPKR completely.

SPEAKER MAIN PARTS LIST 1/1

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
1	8A-CJ5-422-010		GRILLE, FRAME ASSY Y
2	8A-CJ5-405-010		PANEL, SP
3	8A-CJ5-403-010		PANEL, FR
4	8A-CJ5-415-010		TERMINAL,
5	8A-CJ5-411-010		SPKR, W 87S
6	8A-CJ5-417-010		SPKR, TW 25
7	8Z-CL5-543-010		CORD, SP



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