AKAI

MODEL CD-A70

SCHEMATIC DIAGRAM AND PC BOARDS

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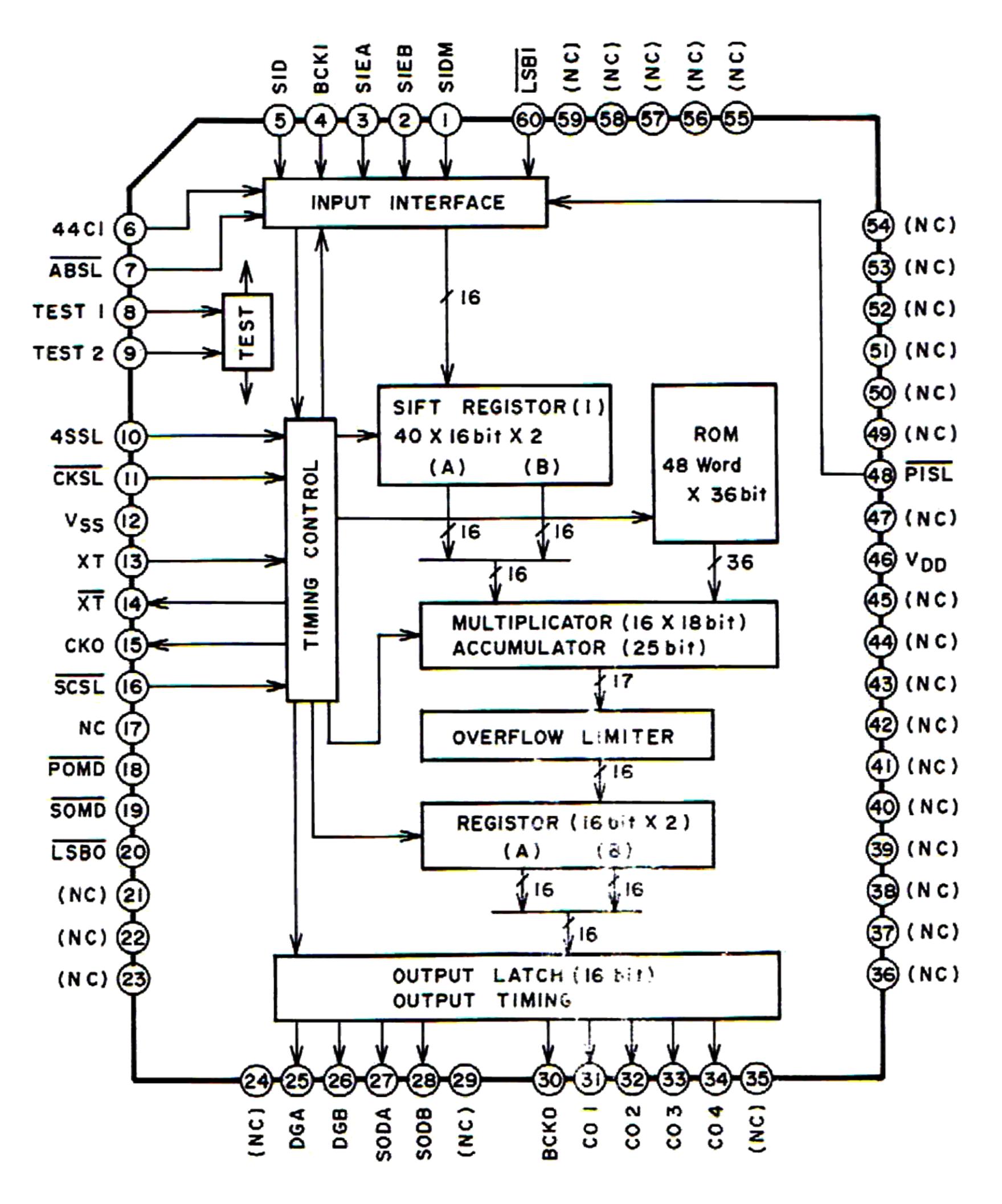
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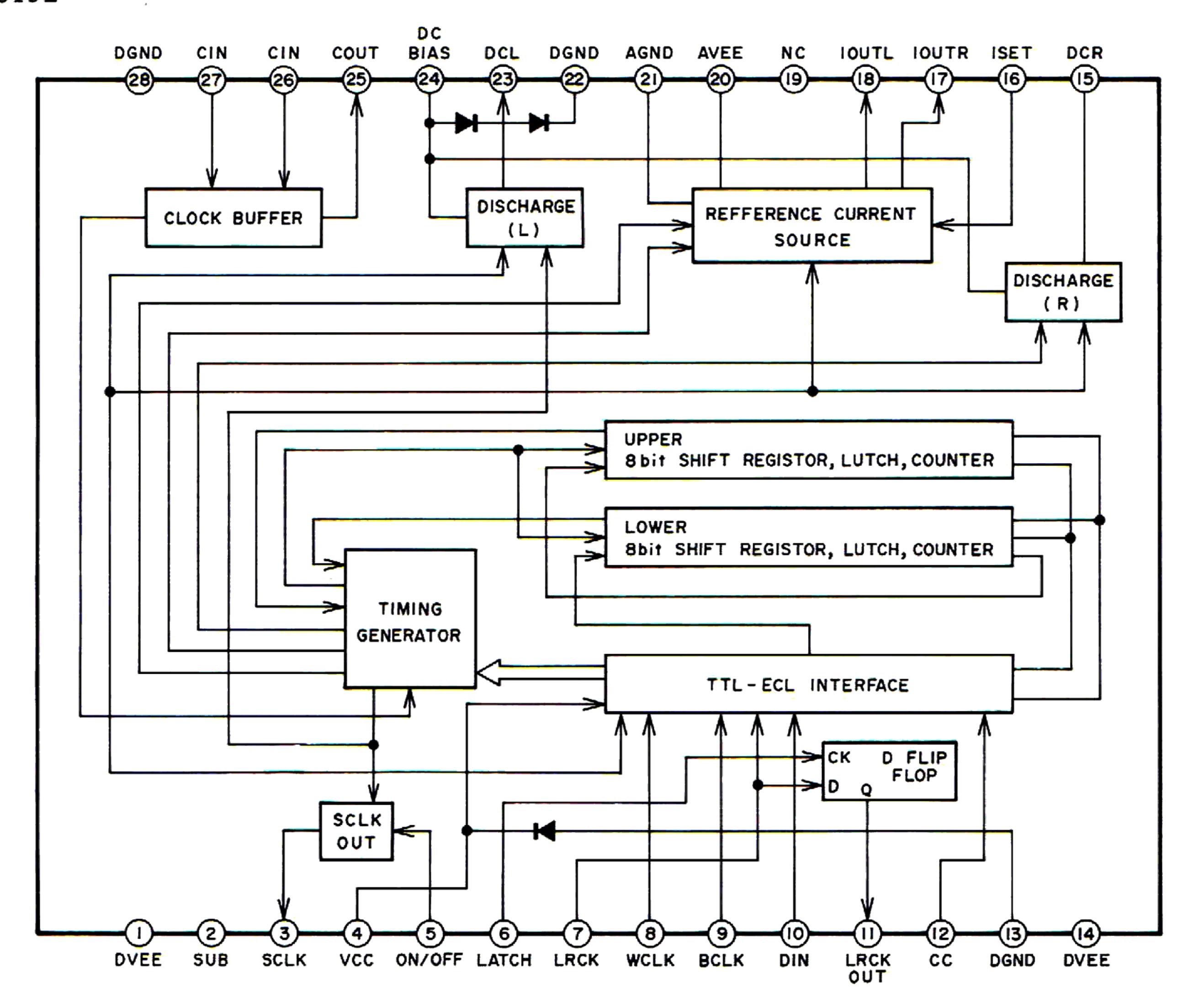
PURPOSE OF IC's

IC NO.	NAME OF IC's	PURPOSE
IC1	CX23035	EMF DEMODULATOR, ERROR DETECTION AND CORRECTION,
		FRAME SYNC DETECTION, SUB CODE DETECTION AND
		DEMODULATION, SPINDLE MOTOR SERVO
IC2	CX20108	SERVO SIGNAL PROCESSER
IC3	SRM2016C15	16K BIT RAMDAM ACCESS MEMORY
IC4	M50754-417SP	SYSTEM CONTROL (8 BIT MICROCOMPUTER)
IC5	AX80	OVER-SAMPLING DIGITAL FILTER
IC6	CX20152	16 BIT D/A CONVERTOR
IC7	MB84053B	TRIPE-2 CHANNEL MULTIPLEXER/DEMULTIPLEXER
IC8	HD6805SD	SYSTEM CONTROL (4 BIT MICROCOMPUTER)
IC9	BA6109	MOTOR CONTROL
IC10	CX20109	RF AMPLIFIER
IC11, 12	MPC4072C	DUAL LOW NOISE OPERATIONAL AMPLIFIER
IC13, 15	M5278L05	VOLTAGE REGULATOR
IC14	TA78005AP	VOLTAGE REGULATOR
IC16	TA79005	VOLTAGE REGULATOR
IC17	M5218P	DUAL LOW NOISE OPERATIONAL AMPLIFIER
IC18	TC4011BP	NAND GATE
IC19, 20, 21	M5238P	DUAL LOW NOISE OPERATIONAL AMPLIFIER
IC22	M5218L	DUAL LOW NOISE OPERATIONAL AMPLIFIER
IC23	LA7224	PRE-AMPLIFIER FOR REMOTE CONTROL
IC24	HD74LS04P	HEX INVERTER
IC101	LC7580	LCD DISPLAY DRIVER

AX-80

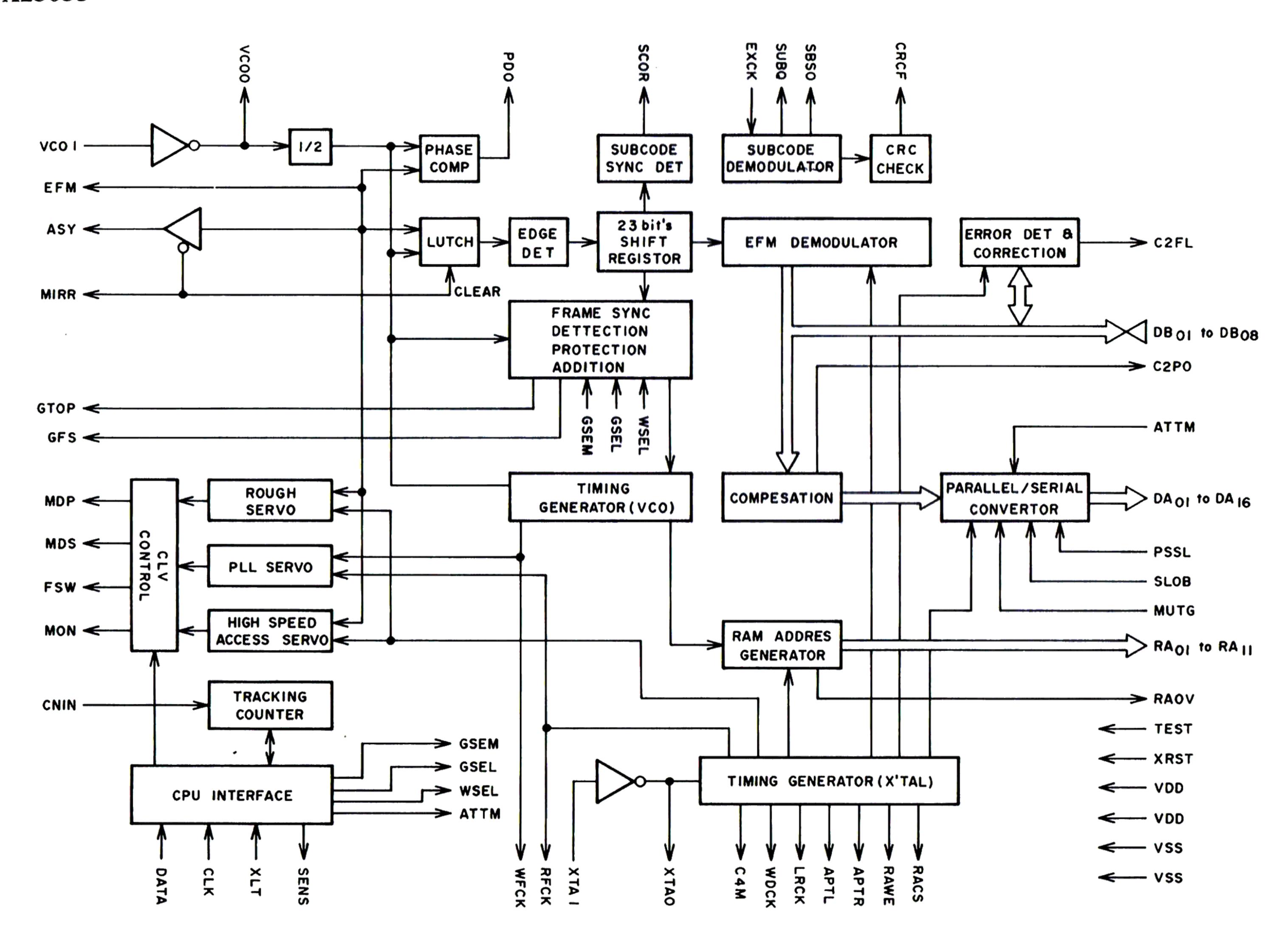


(NC): WHEN PISL = H (or OPEN)



Pin No.	Symbol	Description			
1	DV	Digital (-5V) power supply			
2	SUB	Base IC (should be connected to pin 1)			
3	SCLK	System clock OUTPUT			
4	Vcc	Vcc (+5V) for Digital			
5	ON/OFF	ON/OFF select for system clock			
6	LATCH	Clock for D type lutch			
7	LRCK	LRCK input			
8	WCLK	WCLK input			
9	BCLK	BCLK input			
10	DIN	Data input			
11	LRCKOUT	LRCK output			
12	CC	CC input			
13	DGND	Digital GND			
14	DV	Digital (-5V) power supply			
15	DCR	R CH discharge drive signal output			
16	ISET	Integrater ampere terminal			
17	IOURT	R CH current output			
18	IOUTL	L CH current output			
19	NC	No connection			
20	AV	Analgue power supply			
21	AGND	Analgue GND			
22	DGND	Digital GND			
23	DCL	L CH discharge drive signal output			
24	DCBIAS	Bias for discharge circuit			
25	COUT	Clock OSC out			
26	CIN	Clock OSC			
27	CIN	Clock OSC			
28	DGND	Digital GND			

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Pin No.	Symbol	I/O	Description	
1	FSW	Ο	Spindle motor filter switching control	
2	MON	Ο	Spindle motor ON/OFF control	
3	MDP	О	Spindle motor speed and phase control	
4	MDS	О	Spindle motor speed control	
5	EFM	I	EFM signal input	
6	ASY	О	EFM signal slice level control	
7	MIRR	I	MIRR signal input "L" on track "H" mirror	
8	VCOO	О	VCO output $f = 8.6436 \text{ MHz}$	
9	VCOI	I	VCO input	
10	TEST	I	0V (GND)	
11	PDO	О	Phase comp. output	
12	VSS		GND (0V)	
13	CLK	I	Clock signal from CPU	
14	XLT	I	Lutch signal from CPU	
15	DATA	I	Serial data from CPU	
16	XRST	I	RESET input "L" reset	
17	CNIN	I	Tracking pulse input (+5V)	
18	SENS	О	Output of CPU interface	
19	MUTG	I	Mute control signal input	
20	CRCF	О	CRC check output of the subcode Q "L" detect error	
21	EXCK	I	Clock input for Subcode serial output	
22	SBSO	О	Subcode serial output	
23	SUBQ	О	Subcode Q output	
24	SCOR	О	Subcode sync detection output	
25	WFCK	О	Not used (Write frame clock)	
26	RFCK .	Ο	Not used (Read frame clock)	
27	GTOP	О	Frame sync detection output	
28	GFS	О	"H" frame sync lock "L" frame sync unlock	

Pin No.	Symbol	I/O	Description			
29	DB08	I/O	Data 8 (MSB)			
30	DB07	I/O	Data 7	Data Bus line for the EXT. RA	M	
31	DB06	I/O	Data 6	(SRM2016C15)		
32	DB05	I/O	Data 5	(DICHIDO IO DIC)		
33	VDD		+5V			
34	DB04	I/O	Data 4	\		
35	DB03	I/O	Data 3	Data Bus line for the EXT. RA	M	
36	DB03	I/O	Data 2	(SRM2016C15)		
37	DB02 DB01	I/O	Data 1 (LSB)	(DIUVIZOTOCIO)		
38	RA01	O	ADDR01 (LSI	8))		
39	RA02	0	ADDR01 (LSI	"		
40	RA03	0	ADDR02 ADDR03			
41	RA04	$\frac{o}{o}$	ADDR03 ADDR04			
			ADDR04 ADDR05	Address signal output for the	EVT	
42	RA05		1	Address signal output for the	ELAI.	
43	RA06		ADDR06	RAM (SRM2016C15)		
44	RA07	O	ADDR07			
45	RA08	0	ADDR08			
46	RA09	O	ADDR09			
47	RA10	<u>O</u>	ADDR10			
48	RA11	<u>O</u>	ADDR11 (MS			
49	RAWE	<u>O</u>		gnal output "L" active		
50	RACS	<u>O</u>		nal output "L" active		
51	C4M	<u>O</u>	Not used			
52	VSS		GND (0V)			
53	XTAI	I	X'TAL OSC. i	nput $f = 8.4672 \text{ MHz}$		
54	XTAO	O	X'TAL OSC. output $f = 8.4672 \text{ MHz}$			
55	C2FL	O	Monitor of error detection *			
56	C2PO	O	Not used			
57	RAOV	O	Not used			
58	SLOB	I	0V (GND)			
59	PSSL	I	0V (GND)			
60	APTR	О	Not used			
61	APTL	Ο	Not used			
62	DA01	О	C1F1 *			
63	DA02	О	C1F1 *			
64	DA03	О	C2F1 *		Not used	
65	DA04	О	C2F2 *		Not used	
66	DA05	О	UGFS		Not used	
67	DA06	O		rite frame clock signal output		
68	DA07	O	 	CV 1/4 or 1/8 WFCK output		
69	DA08	Ο	 	CX 1/4 or 1/8 RFCK output		
70	DA09	O		CK 1/2 VCO output		
71	DA10	0		CK INV. LRCK (Pin 80)		
72	DA11	O	 	R 176.4 kHz strobe signal outpu	t	
73	VDD		+5V	, o, , mana our ood digital outpu	-	
74	DA12	0		rial data enable signal		
75	DA12 DA13	$\frac{0}{0}$				
76	DA13 DA14	0	DENR R-ch serial data enable signal C210 INV. C210 (Pin 77)			
77	DA14 DA15	0	Not used C210 Bit clock $f=2.1168 \text{ MHz}$			
78	DA16 WDCK		Data output Not used Worde clock output 88.2 kHz strobe signal			
79	WDCK LDCK				44.1 kHz strobe signal	
80	LRCK		Not used L-c	h. R-ch clock out	44.1 KIIZ SUIOUC SIgilai	

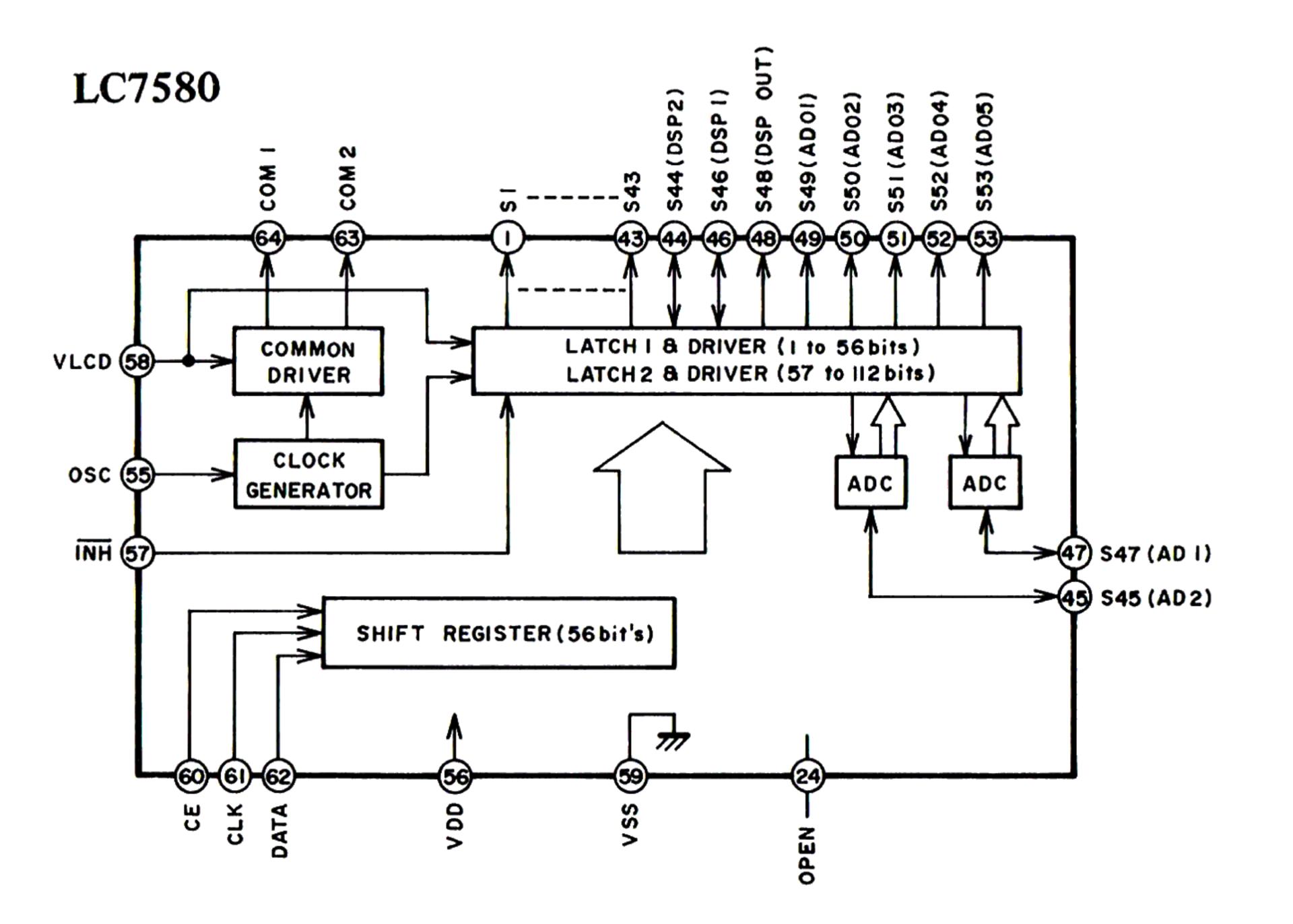
* Monitor Signal refer to Fig. 1 & Fig. 2

C1F1	C1F2	C1 Correction
О	Ο	No error
I	О	Signal error correction
О	I	Double error correction
I	I	Irretrievable error

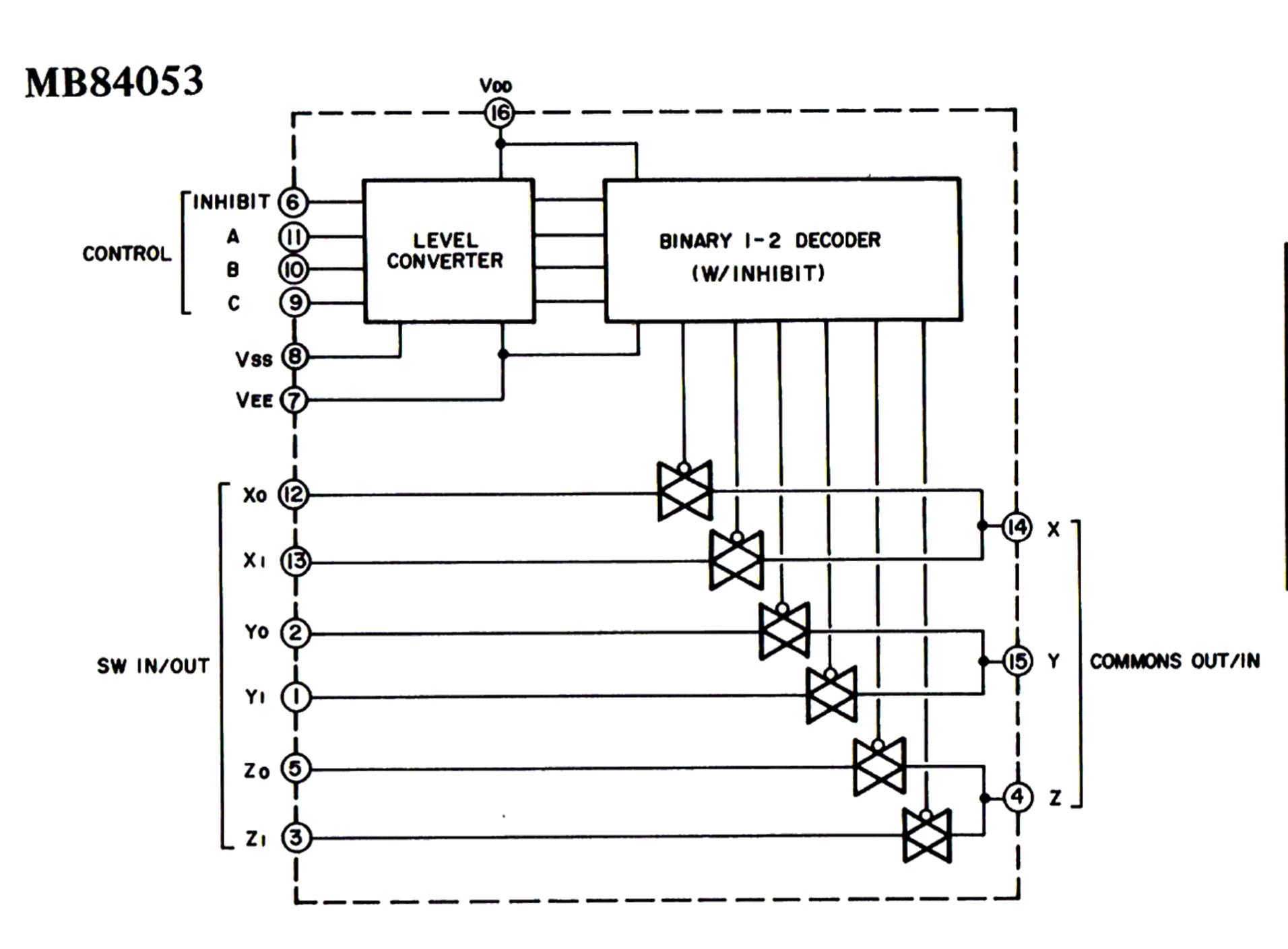
C2F1	C2F2	C2FL	C2 Correction
O	Ο	Ο	No error
I	O	0	Signal error correction
O	I	0	Double error correction
I	I	I	Irretrievable error

Fig. 1

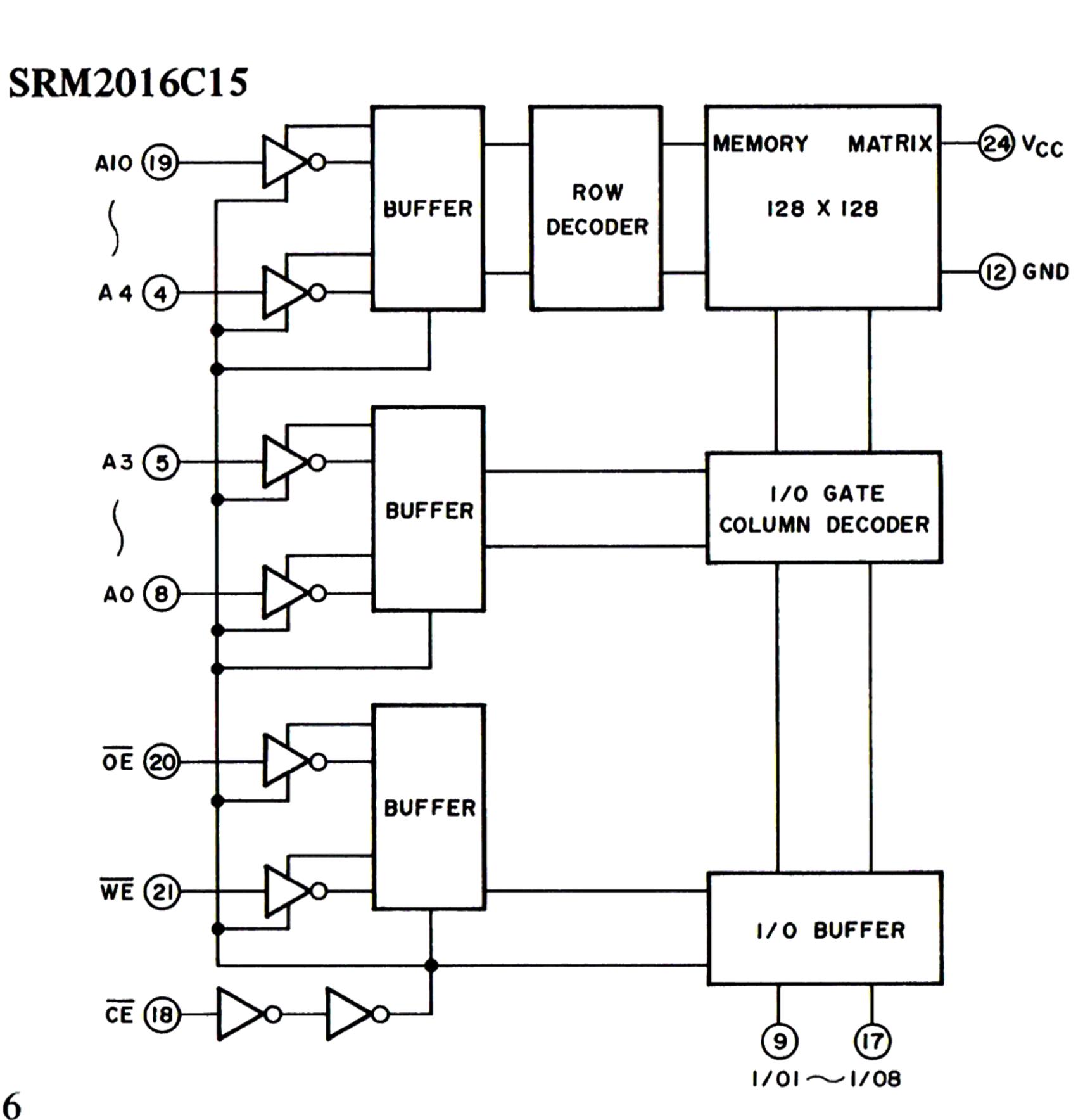
Fig. 2



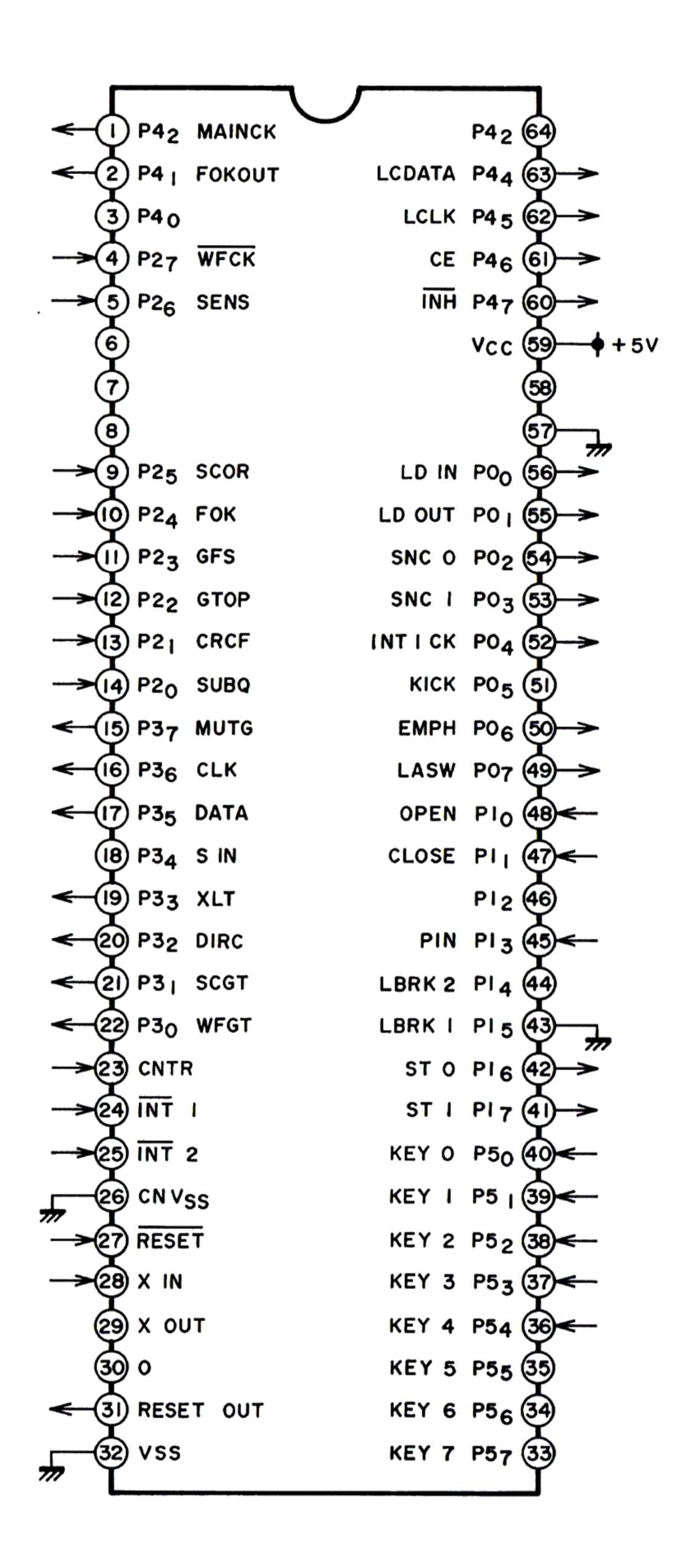
S1 ~ S43	Segment drive Output
S46 (DSP), S44 (DSP2)	Segment drive Output/DSP Input
S47 (ADI), S45 (AD2)	Segment drive Output/AD Input
S48 (DSP OUT)	Segment drive Output/DSP Output
S49 ~ S53	Segment drive Output/AD Output
COM 1, 2	Common Output
V LCD	LCD Bias voltage
OSC	OSC control
CE, CLK. Data	Serial data Input
VSS, VDD	GND, +5V
INH	Display OFF signal Input
Open	Not used



	Con	trols		**	ON" channe	. 1
INH	С	В	Α	"ON" channel		
0	0	0	0	Zo	Yo	Χo
0	0	0	1	Zo	Yo	X ₁
0	0	1	0	Zo	Y1	Χo
0	0	1	1	Zo	Yı	X ₁
0	1	0	0	Zı	Yo	Xo
0	1	0	1	Zı	Yo	Xı
0	1	1	0	Zı	Yı	Χo
0	1	1	1	Zı	Y 1	X ₁
1	_	_	_		None	

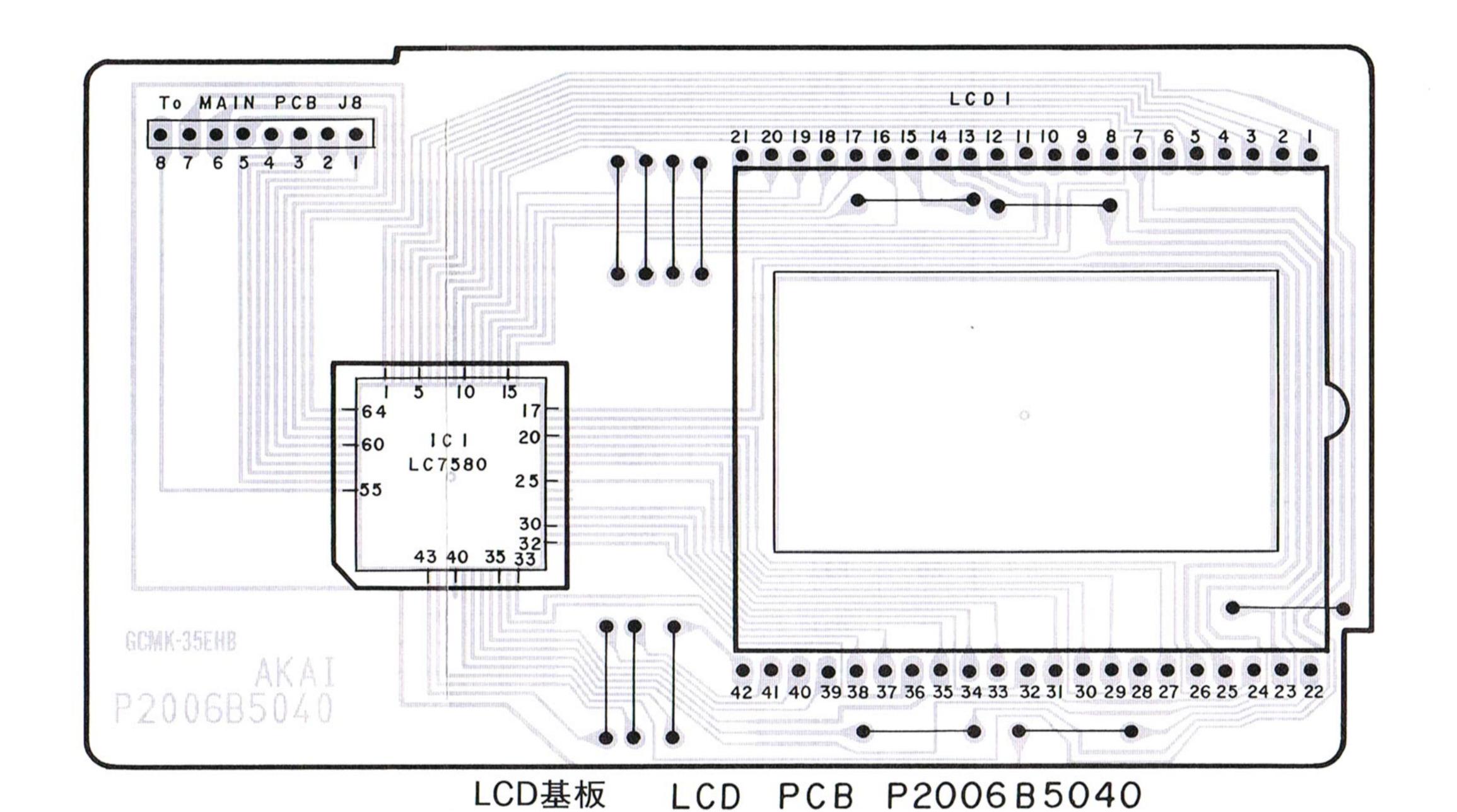


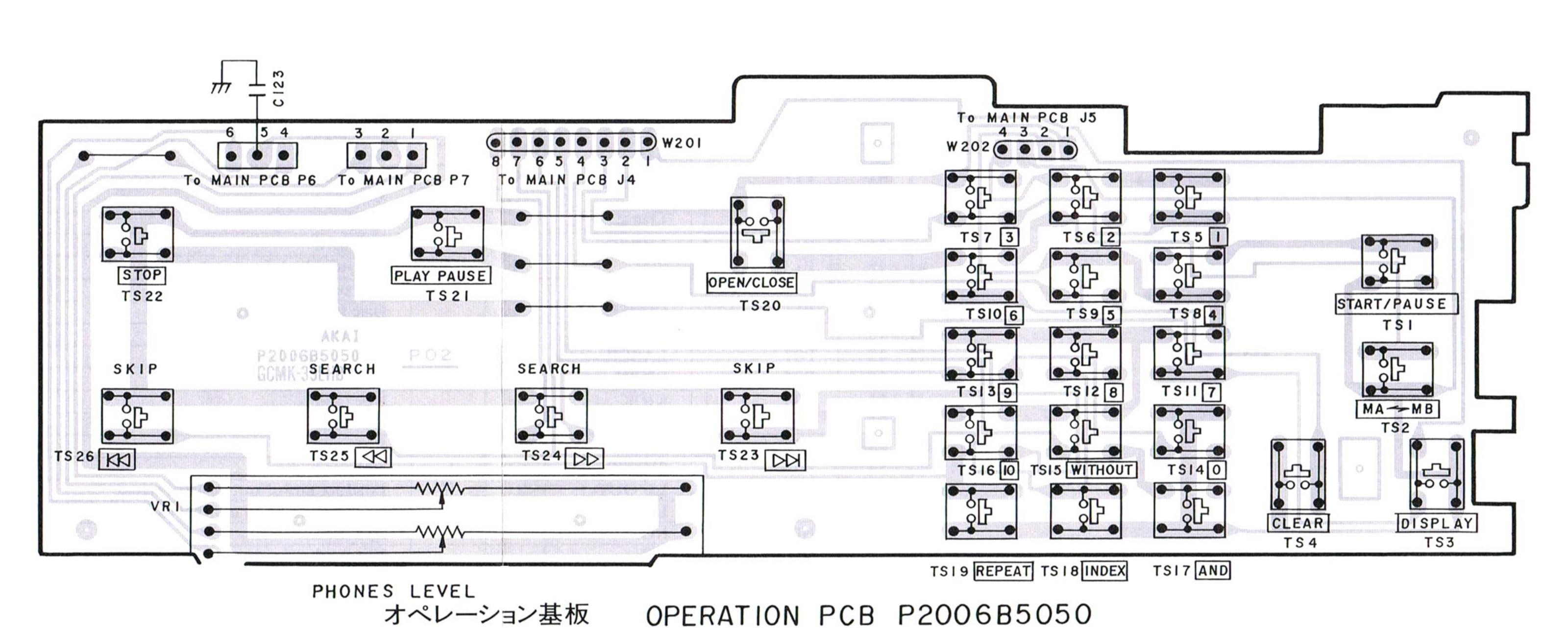
A0 ~ A10	Address input
I/O1 ~ I/O8	Data IN/OUT
CE	Chip enable signal input
WE	Write enable signal input
ŌĒ	Output enable signal input
Vcc	+5V
GND	GND

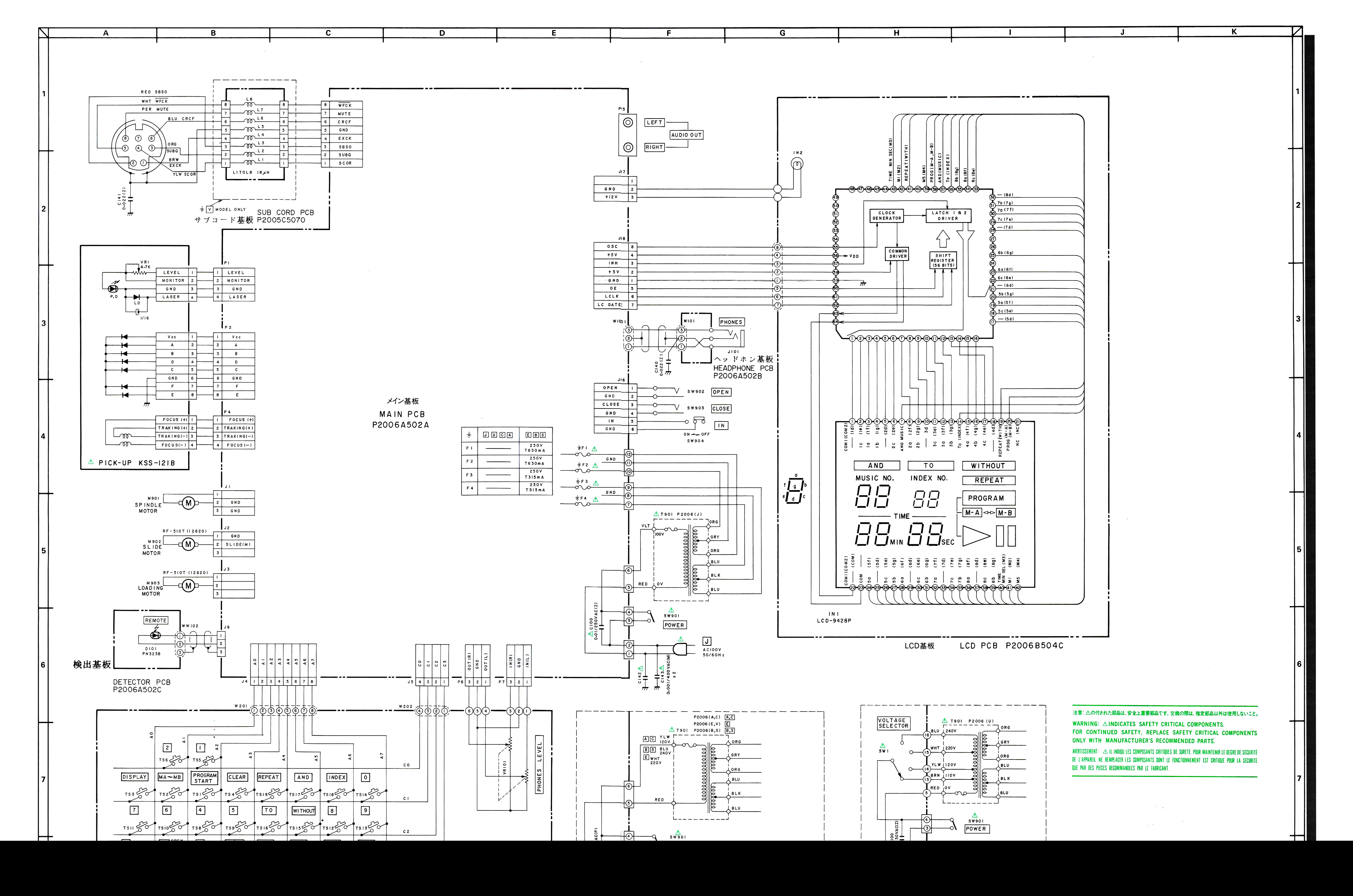


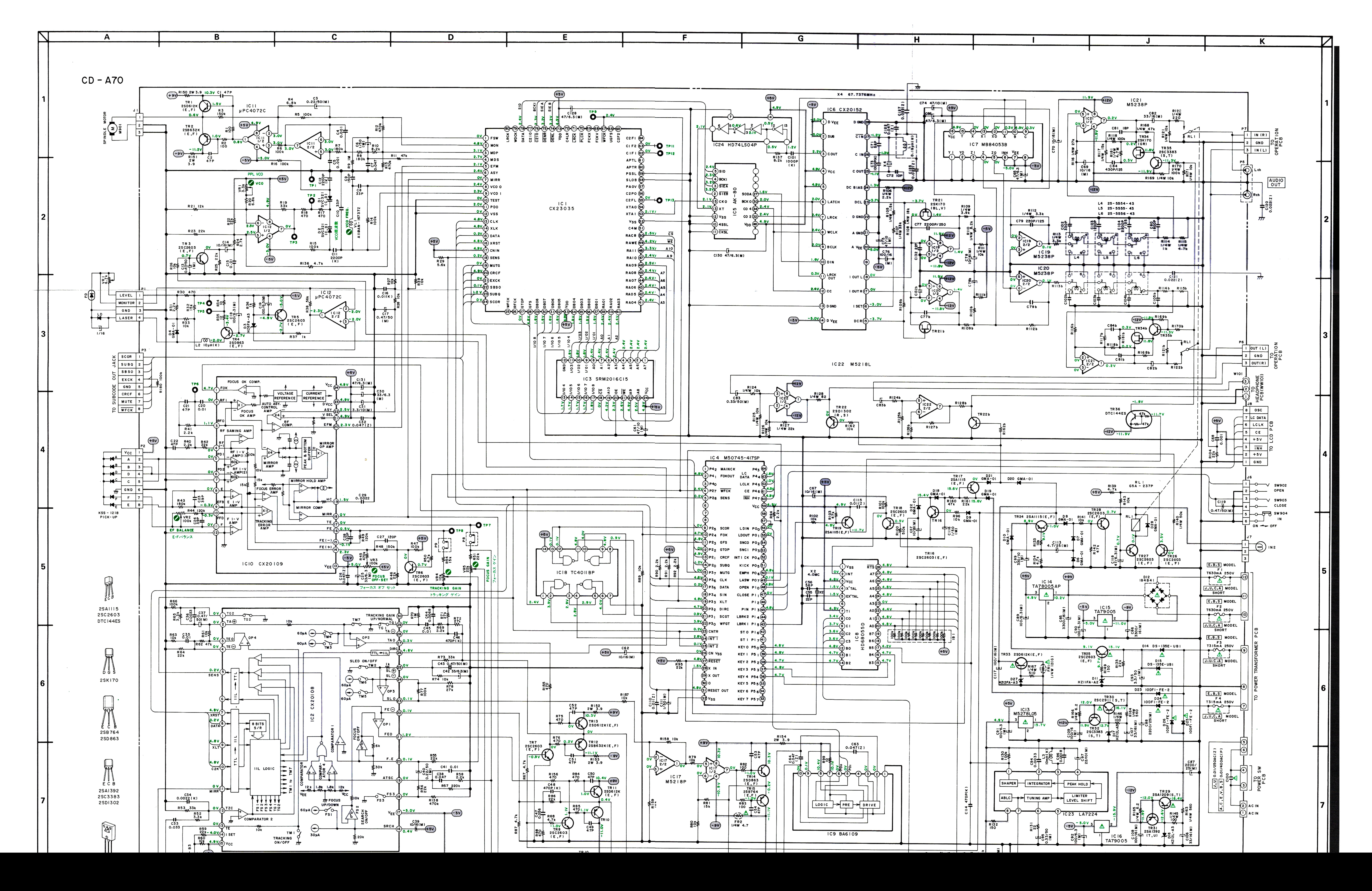
Pin No.	Symbol	Port Name	I/O	Active	Description	
1	P42	MINCK	O		Main through check	
2	P41	FOK OUT	0	Н	FZC level set H: Normal L: Off-Set (+)	
3	P40				Not used	
4	P27	WFCK	I		Write Frame clock input	
5	P26	SENS	I		Sens signal input	
6	NC				Not used	
7	NC				Not used	
8	NC				Not used	
9	P25	SCOR	I	H	Subcord detection signal input	
10	P24	FOK	I	H	Focus servo "OK" signal input	
11	P23	GFS	1	H	"H" Frame Sync. lock, "L" Frame Sync unlock	
12	P22	GTOP	1	H	Frame Sync. detection signal input	
13	P21	CRCF	<u>I</u>	H	CRC check signal input	
14	P20 P37	SUBQ	1		Subcode Q input	
16	P36	MUTG CLK	0		Mute control signal input	
17	P35	DATA	0		Clock signal output Data signal output	
18	P34	SIN	T		Not used	
19	P33	XTL	O	Ť	Lutch signal output	
20	P32	DIRC	0	T	Track jump control signal output	
	1 32	DIRC			"H" Normal "L" Track jump	
21	P31	SCGT	0	Н	Subcode gate signal output	
22	P30	WFGT	o	H	Write frame Gate signal output	
23	CNTR	CNTR	Ī		Track control signal input	
24	INT1	INT1	Ī		Subcode Q read control	
25	INT2	INT2	I		Focus control	
26	CNVss	CNVss			GND	
27	RESET	RESET			Reset signal input	
28	XIN	XIN			Clock input	
29	XOUT	XOUT			Clock output	
30	0	0	l		Not used	
31	RESET OUT	RESET OUT			Reset signal output	
32	Vss	Vss			GND	
33	P57	KEY7	I		Not used	
34	P56	KEY6	I		Not used	
35	P5 5	KEY5	<u> </u>		Not used	
36	P54	KEY4	<u>l</u>		Key input	
37	P53	KEY3	I		Key input	
38	P5 2 P5 1	KEY2 KEY1	T		Key input	
40	P50	KEY0	T		Key input	
41	P17	ST1	O	T	Key input Not used	
42	P16	ST2	0	T	Not used	
43	P15	LBRK1	T	L	GND	
44	P14	LBRK2	Ī		Not used	
45	P13	PIN	Ī		Pick-up block in switch input	
46	P12				Not used	
47	P11	CLOSE	I		Disc tray close switch input	
48	P10	OPEN	I		Disc tray open switch input	
49	P07	LASER	О	L	Laser control signal input	
50	P06	EMPH	О	L	Emphasis control signal input	
51	P05	KICK			Not used	
52	P04	INT1	О	L	Not used	
53	P03	SYNC1	О	L	Not used	
54	P02	SYNC0	0	L	Not used	
55	P01	LD OUT	0	Н	Loading motor out control signal	
56	P00	LD IN	0	H	Loading motor in control signal	
57	NC	NC			Not used	
58	NC	NC			Not used	
59	Vcc	Vcc			+5 V	
60	P47	INH	0	L	Display off signal output	
61	P46	CE	0	<u>H</u>	Chip enable Chaple Social data systems for displays	
62	P45	LCLK	0		Clock Serial data output for display	
63	P44	LCDATA	O		Data J	
64	P43				Not used	


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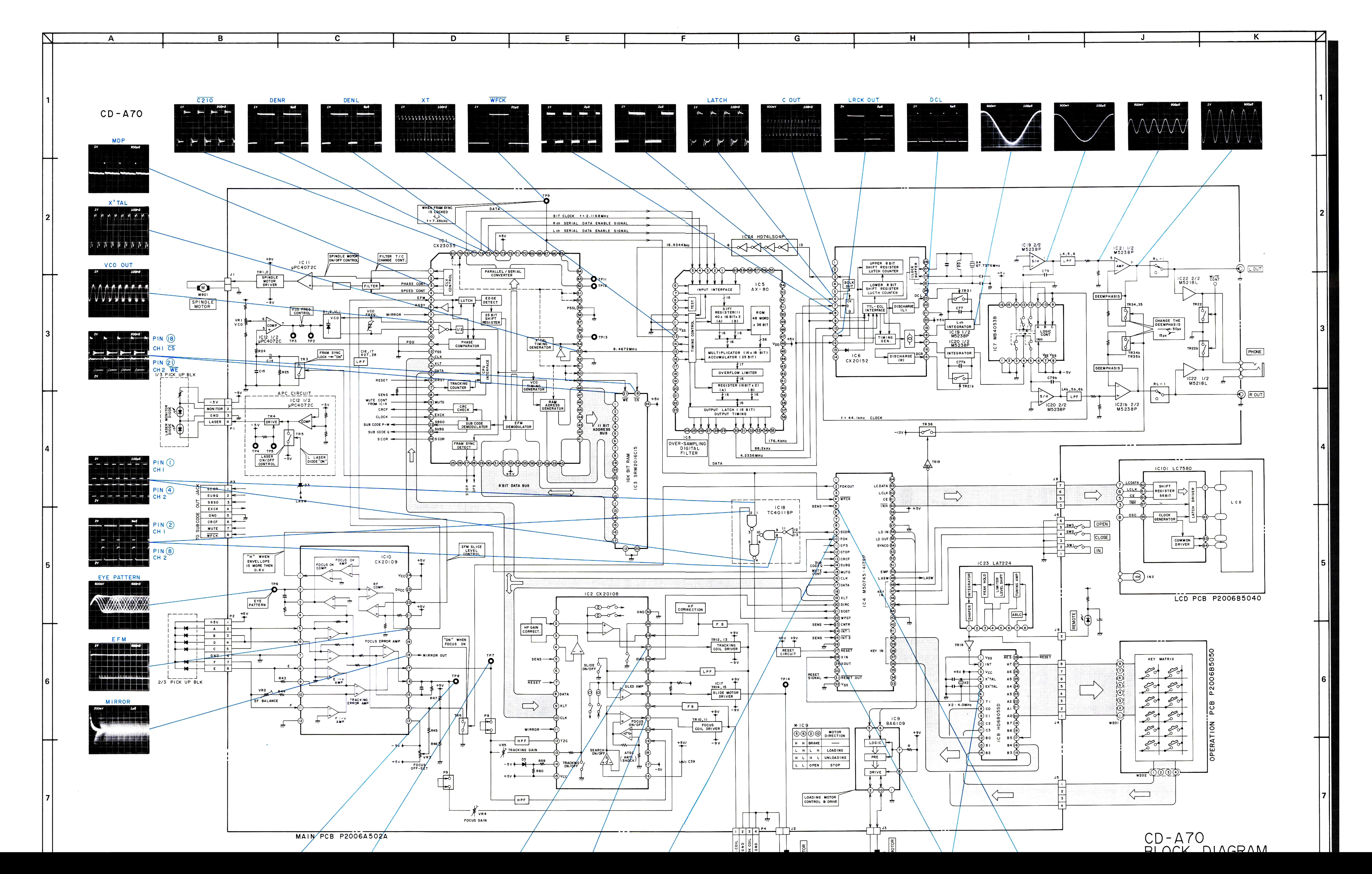


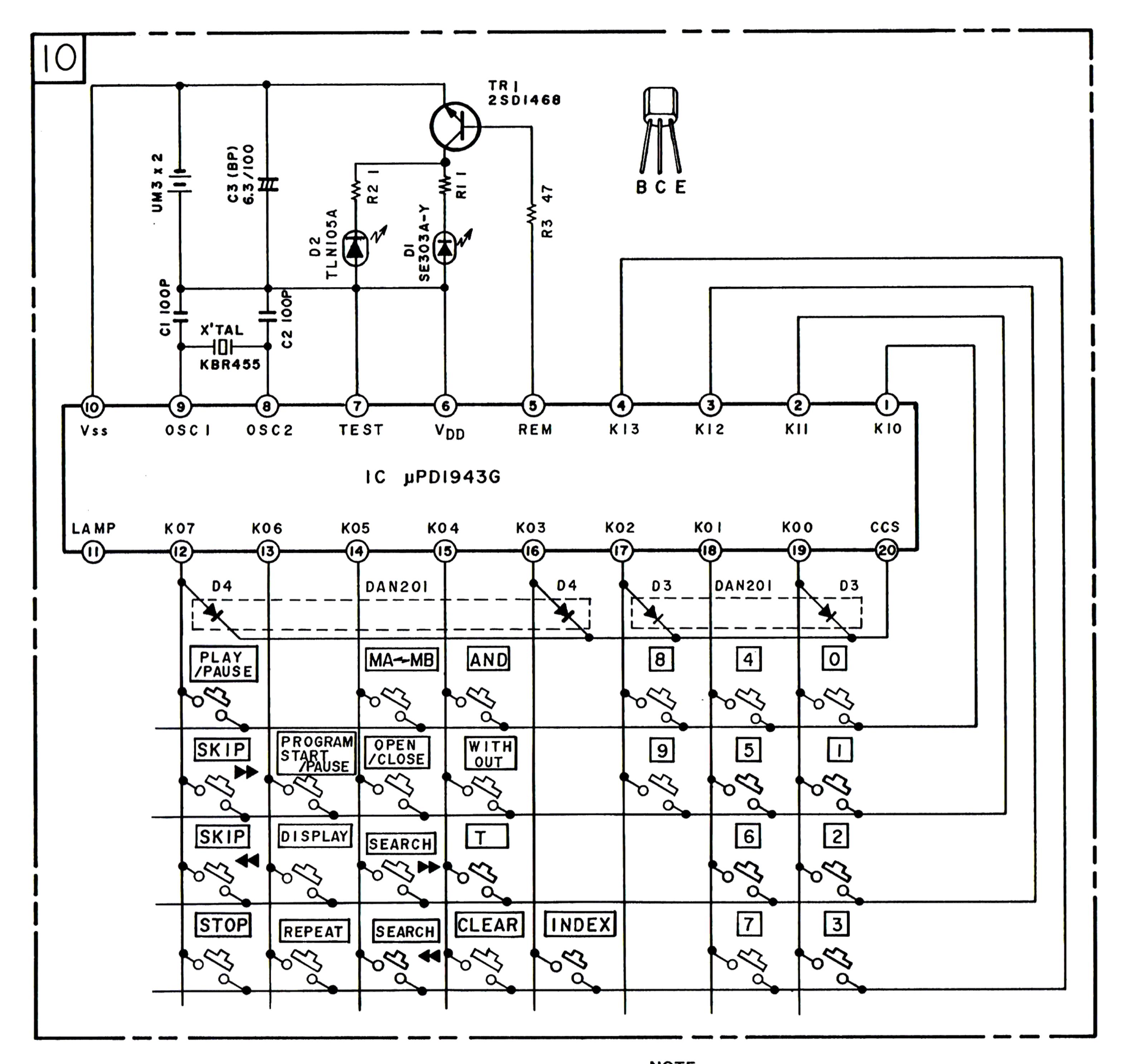












備考

C, Rの単位(特に指定された部品以外)

抵抗……ωΩ I/4W(J),(FS)記号は不燃性部品 コンデンサ……μF 50WV(J)

各電圧は、GND間のDC電圧をデジタルボルトメーターにて 測定した値です。

NOTE

UNLESS OTHERWISE SPECIFIED ALL RESISTORS IN OHMS 1/4W(J) ALL CAPACITORS IN μ F 50WV(J)

RC-700 WIRELESS REMOTE CONTROL UNIT SCHEMATIC DIAGRAM No.3-3 860418A