

ARCAM

BLACK BOX 500 D/A CONVERTOR SERVICE MANUAL

ARCAM BLAC

Issue 1 (Paul N)

Arcam Drawing

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TECHNICAL SPECIFICATIONS

Conversion system
Sampling rates accepted
Dynamic range
Signal to noise ratio
Harmonic distortion
Frequency response
Output level (0dB)

Output impedance
Minimum recommended
Mains input
Power consumption
Size W/D/H mm.

Unit Function

The BB inputs indicate which direction or direction variable recorder which direction.

The input AE emphasizes extracted.

For the noise and for three oscillators a super as the signal which has clock rate.

An event of the input reference sends a signal.

When reference incoming Class 1.

Having synclock phase v slips because phase transition.

If Synclock recover a second active unit.

If Synclock

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pulse encoder, Z704 and Z708, is latched twice with the purified clock signal. This reduces the phase noise and jitter present on the edges of the digital signal and improves the performance of the overall DAC by lowering the noise floor by a few dBs, reducing THD+N level distortion and improving the subjective sound quality.

Note: Audio signals can be extracted from this digital signal by simply passing it through a low pass filter, all the way from the output of Z502 to the output of Z501 & Z551. Hence what looks like a digital signal on an oscilloscope, looks like audio on an Audio Precision Analyzer for example. Set the low pass filter to <100KHz.

The edge-purified pulses emerging from Z502 and Z552 are then shaped so that the high level and low level of the pulse is free from ringing or any other deformation present on digital signals. It is this signal which is finally filtered in the analogue domain by Z101, Z102, Z201 and Z202.

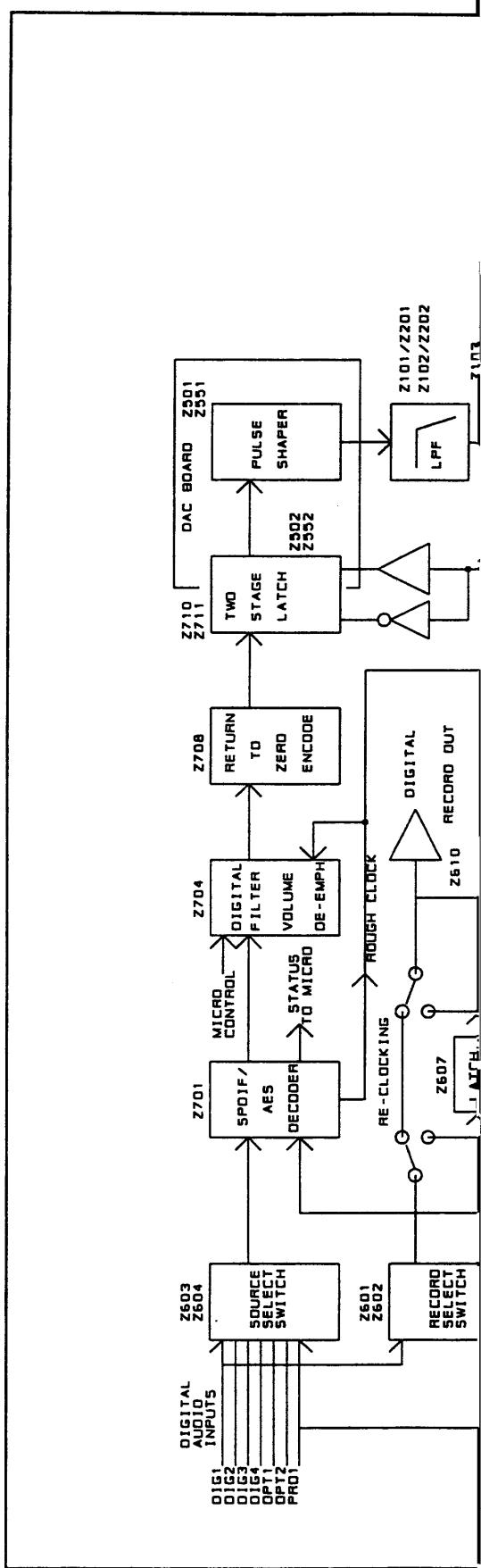


Figure 1 Bloc

Circuit Description

Input Switching (C)

The coaxial inputs from the optical input and the AES/EBU input.

Both the live and record switches, Z601 and Z602, are used for listening.

Z605 buffers the Record switch output and connects it to the digital filter, Z607 by Z606-A, otherwise it connects the AES/EBU input to drive the coaxial driver, Z608.

Digital Audio Decoding

Z701 receives the serial data from the microcontroller (pin 9 and 10). When the data is valid, Z701 enables Z702.

This is used to find the start of frame and status bits are read.

Pin 28, VERF provides the enable for the digital filter, Z704 to pass the data forward, for example to the DAC.

The rough clock is generated by Z606-C. Z606-C can break the 'no signal' condition.

this is never ever done.

The digital filter, Z704 also does the digital filtering of the bus from the micro.

Z708 chopped the digital filter outputs, i.e. they always return to ground.

latched through Z709 to the rough clock mode, or to the rough clock.

Bitstream pulse pulses

The chopped and latched digital filter outputs and Z552 to further process the edges of the data, i.e. the bitstream pulse states are supplied from the digital filter by using analogue switches as required.

Clock block (Circuit diagram sheet 9)

The clock block contains three XTAL oscillators, none operating at the same time. To select one of the three XTAL circuits, a bias voltage is applied to the base of the appropriate transistor Q301, Q302 or Q303. This causes the collector of the selected oscillator to drive through D301, D302 or D303 into R316. The other two diodes ensure that the other two XTAL circuits remain isolated. The conductive component in a Colpitts oscillator circuit. Two varicap diodes, for example, allow the frequency of the oscillator to be varied by a control voltage, FCTRL.

Q304 buffers the clock signal followed by Z302-A and Z302-B.

The clock signal used to re-latch the bitstream data is selected. If Synclock mode is not established, then Z305-C and Z305-D are bypassed.

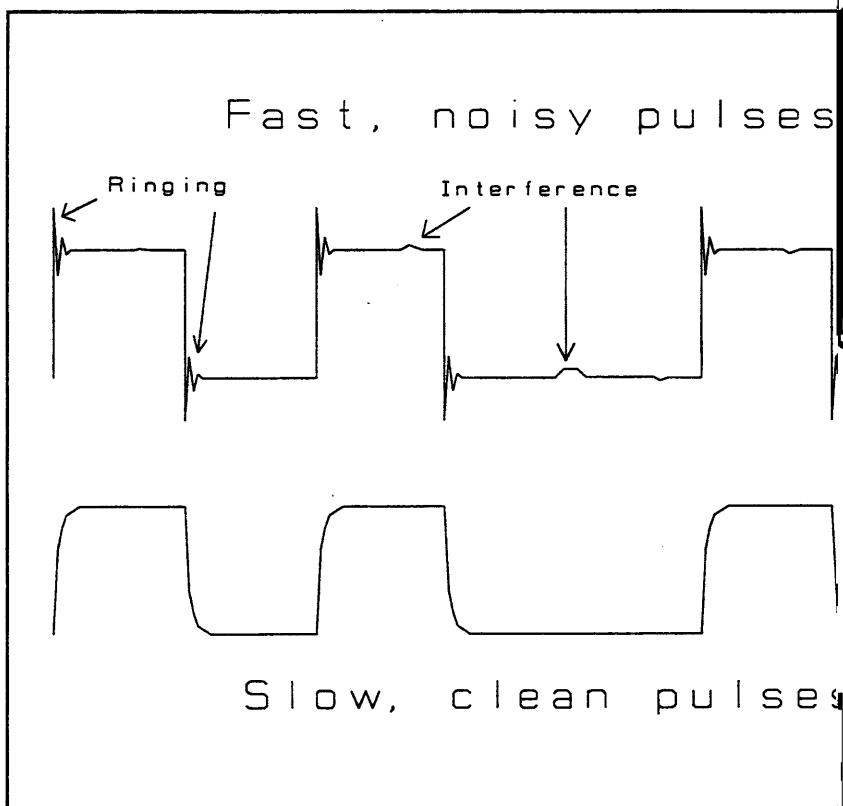


Figure 2 Pulse purifier effect

otherwise, Z305-A and Z305-B select an XTAL clock for re-latching.

Clock control unit (Circuit diagram sheet 3)

The XTAL clock is synchronised to the rough clock in one of two ways. The XTAL clock is divided by four by Z403 and sent to the digital optical transmitters. In this mode, Z405-B compares the phase of the rough clock and the DELTAF signal is used to determine if transport is locked, this will be a d.c. value between 0 and 100%.

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Audio Filter

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Change of Mains Voltage

WARNING - the unit **must** be unplugged from the mains when replacing the fuse as the mains inlet and fuse are at mains potential even with the unit switched off.

The Black Box 500 can be set for use on 230v or 115v mains supplies.

There are 2 mains fuseholders in the unit - one marked 230v (F1) & the other 115v (F2) and the fuseholder with the fuse fitted to it determines the working voltage.

To change voltage remove the fitted fuse and fit the correct fuse to the other fuseholder.

The correct fuses are: 250 mA antisurge for 230v
 500 mA antisurge for 115v

NOTE: ONLY FIT ONE FUSE AT A TIME!!

Test Points (marked on circuit diagrams)

Measurements made at 230V mains supply.

AGRND	Analogue ground	0	Vdc
ANAN16	Analogue regulated -ve supply	-15.3 +/- 0.5	Vdc
ANANPR	Analogue pre-regulated -ve supply (audio muted)	-22.0 +/- 1.0	Vdc
ANANUN	Analogue unregulated supply (audio muted)	-24.4 +/- 1.0	Vdc
ANAP16	Analogue regulated +ve supply	15.3 +/- 0.5	Vdc
ANAPPR	Analogue pre-regulated +ve supply (audio muted)	22.0 +/- 1.0	Vdc
ANAPUN	Analogue unregulated +ve supply	24.0 +/- 1.0	Vdc
BIT5V	Z710, Z711 5V supply	5.0 +/- 0.2	Vdc
BPASSN	Not bypass signal, high when Class 1 or Synclock active	0 = off, 5 = active	Vdc
BPASSP	Bypass signal, as above but inverted	"	"
DFCLK	Clock for Z711. Sampling rate times 256, square wave	5.0 +/- 0.5	Vpk
DIG1L	Coaxial SPDIF input, Dig 1, live	1.0 +/- 0.2	Vpkpk
DIG1N	Neutral for above	0 relative to above	Vdc
DIG2L	Dig 2, live	"	"
DIG2N	Dig 2, neutral	"	"
DIG3L	Dig 3, live	"	"
DIG3N	Dig 2, neutral	"	"
DIG4L	Dig 4, live	"	"
DIG4N	Dig 4, neutral	"	"
DIGF5V	Digital filter, Z704 supply	5 +/- 0.2	Vdc
DIGGND	Digital section ground connection	0	Vdc
DIGNUN	Unregulated -ve digital supply	-14.8 +/- 1.0	Vdc
DIGP8V	Pre-regulated +ve digital supply	8.2 +/- 0.5	Vdc
DIGPUN	Unregulated +ve digital supply	12.0 +/- 1.0	Vdc

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DRPOUT	Mains OK detect, goes low as soon as mains is disconnected. Must be low before DIGP8V is less than 5V after mains is removed.	0 = mains interrupt, 4.7 = mains OK.	Vdc
DSILN	Bitstream input to DAC PCB, Left cold	0 & 5 +/- 0.2	Vpk
DSILP	Bitstream input to DAC PCB, left hot	"	"
DSIRN	As above, right cold	"	"
DSIRP	As above, right hot	"	"
DSMLN	Bitstream output from DAC PCB, left cold	0 & 4 +/-0.3	Vpk
DSMLP	As above, left hot	"	"
DSMRN	As above, right cold	"	"
DSMRP	As above, right hot	"	"
FCTRL	Voltage control of XTAL frequencies on DAC PCB. Centre frequency @8.5Vdc should be accurate to <40ppm. Range from 0.8 to 17.1Vdc should be >200ppm.	0.8 to 17.1 Signal & Class 1, 8.5 +/- 0.2 Synclock	Vdc
FSENSE	XTAL oscillator monitor output from one of three XTALs on DAC PCB if selected. Square wave, at one of three frequencies.	5 +/- 0.5	Vpk
I²CCLK	I ² C Clock line. This is pulled high with a pull-up inside the micro. When clock pulses are sent this line is pulsed low.	5 +/- 0.5 (static)	Vdc
I²CDAT	I ² C Data line. Same conditions as above.	5 +/- 0.5 (static)	Vdc
KEYINT	Key pressed interrupt. Low = keypress waiting for micro.	0=key, 5=No key	Vdc
LAUDHI	Left audio output	0dB = 2.3 +/- 0.1	Vrms
LAUDLO	Left audio output	0dB = 2.3 +/- 0.1	Vrms
LED32K	32K LED drive	0 & 2(on) +/- 0.5	Vdc
LED44K	44.1K LED drive	"	"
LED48K	48K LED drive	"	"
LEDPWR	Power LED drive	"	"
LEDSIG	Signal LED drive	"	"
LEDSYN	Synclock LED drive	"	"
LEDVCO	Class 1 LED drive	"	"

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MPU5V	Micro, Z901, supply. Should remain present for several days after unit is switched off. (measure with high impedance meter! e.g. Fluke)	5 + after
MPURST	Micro reset signal. Low = reset.	0
OPT5V	Optical inputs, Z613 & Z614 supply	
OSC32N	DAC PCB 8.1920MHz XTAL oscillator select	0
OSC44N	As above, for 11.2896MHz	
OSC48N	As above for 12.2880Mhz	
PHSP5V	Phase detector, Z405 supply	
PROIL	AES/EBU input live	
PROIN	AES/EBU input neutral	0
RAUDHI	Right audio output	0dB
RAUDLO	Right audio output	0dB
RCOSC	Rough clock input to DAC PCB, square wave @ 256 sampling rate. Active when BPASSP = high.	
RECLK	Clock for record output, Z607. Square wave at 256 times sampling rate.	
RECN5V	Record output buffer, Z610, -ve supply	
RECOL	Coaxial SPDIF record output, live. Active when record select is monitoring a valid digital audio input.	70
RECON	Neutral for above	
RECP5V	Record output buffer, Z610, +ve supply	
RMODE	Remote control mode switch, Low = in, high = out	0
SCLOCK	Clock for Synclock and sampling rate measurement. Square wave at 256 times sampling rate.	
SPDIF5V	Input decoder supply, Z701	
SW5V	Input switching supply Z601 to Z605	
SYNP5V	Synclock system supply	
NTEST	Micro self test. Stays low if test fails, high when test passes. Valid >3 seconds after mains switched on.	0 =
VCO5V	Supply for VCO on Z701	
VCP17V	Supply for VCXO loop filter	

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VCXPPR	Pre-regulated supply for VCXO loop filter	32.0 +/- 2	Vdc
VFD4V7	VFD 4.7v bias for heater supply	4.7 +/- 0.5	Vdc
VFD27V	Supply for VFD driver and display	28.2 +/- 1	Vdc
VFDAC1	VFD AC heater supply #1	6.5 +/- 1 bias 1.8 +/- 0.4 supply	Vdc Vrms
VFDAC2	VFD AC heater supply #2	6.5 +/- 1 bias 1.8 +/- 0.4 supply	Vdc Vrms
VFDUN	VFD and VCXO loop filter supply, unregulated	32.5 +/- 2	Vdc

Board Connections

- SK101** Phono digital audio coaxial input, 4x audio 0dB = 2.3Vrms,
- Z401** Optical Synclock output #1, RCZ-6901 standard connector.
- Z402** Optical Synclock output #2, RCZ-6901 standard connector.
- SK601** BNC 75R coaxial digital audio record output, SPDIF standard.
- Z608** Optical digital audio output, RCZ-6901 connector.
- SK602** Digital audio input #1, BNC 75R, SPDIF standard.
- SK603** Digital audio input #2, BNC 75R, SPDIF standard.
- SK604** Digital audio inputs #3 & #4, Phono 75R, SPDIF standard.
- Z613** Optical digital audio input, RCZ-6901 connector.
- Z614** Optical digital audio input, RCZ-6901 connector.
- PL601** Digital audio input, XLR socket, AES/EBU standard.
- PL1** 115 or 230V +/-12%, 55-65Hz power inlet, IEC socket.

PLs
Pi
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PLs
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PL701		
Pin	Type	Function
1	O	Pulse stream, DSILN, left, -ve, 5V pulses, 75 to 120µs
2	O	Pulse stream, DSILP, left, +ve, 5V pulses, 75 to 120µs
3	Pwr O	+15V supply to DAC PCB
4	Pwr O	+8V supply to DAC PCB
5	O	Pulse stream, DSIRN, right, -ve, 5V pulses, 75 to 120µs
6	O	Pulse stream, DSIRP, right +ve, 5V pulses, 75 to 120µs

PL101		
Pin	Type	Function
1	I	Pulse stream, DSMLN, left, -ve, 4V pulses, 75 to 120µs
2	I	Pulse stream, DSMNP, left, +ve, 4V pulses, 75 to 120µs
3	Pwr O	0v DAC and Clock PCB Reference
4	Pwr O	0V DAC and Clock PCB Reference
5	I	Pulse stream, DSMRN, right, -ve, 4V pulses, 75 to 120µs
6	I	Pulse stream, DSMRP, right +ve, 4V pulses, 75 to 120µs

PL402		
Pin	Type	Function
1	I	Record output clock, 7 to 13MHz square wave, 5V peak
2	I	Latch #1 clock, 7 to 13MHz, square wave, 5V peak
3	I	Synclock clock, 7 to 13MHz, square wave, 5V peak
4	I	Phase detect clock, 7 to 13MHz square wave, 5V peak
5	O	Rough clock, 7 to 13MHz square wave, 5V peak
6	Pwr O	+8V supply to Clock Block

PL902			DAC/Clock PCB Clock Conn.
Pin	Type	Function	
1	O	Freq control voltage, 1 to 16Vdc Class 1 mode, 8.1	
2	O	0V = select 12.2880Mhz osc., 5V =	
3	O	0V = select 11.2896MHz osc., 5V =	
4	O	0V = select 8.19200MHz osc., 5V =	
5	O	0V = select XTAL operation, 5V = bypass	
6	O	0V = bypass XTAL clock, 5V = select X	

Service test mode

A manual test mode is provided to assist in service fault diagnosis. It is possible to force and hold a certain state, such as Synclock or XTAL, micro responding to signal drop-outs and Synclock interruptions. It is also possible to measure the crystal frequency extremes and lowest and highest extremes.

To access this special mode, press **RECORD** then **DISPLAY**. The four buttons on the left of the VFD display lights up to indicate the first level of security. Higher levels are needed to prevent accidental user access. Then press **F1** then **DOWN**. The VFD display now changes completely, The new roles are shown in figure 2.

The digits show the value that the selected crystal frequency selected. If extreme is selected then the frequency display is modified to show the resolution frequency counter. These values are for a guide only - the actual frequency has to be measured by a frequency counter. The LEDs show which XTAL is selected. The Signal LED indicates that a valid signal is being received. The front panel buttons now have different functions:

The Dig 1 - 3 buttons are the crystal frequency select.

Dig 4 is no crystal frequency.

Pro 1 is the DIRECT switch which switches on the rough clock. If selected the display the selected crystal will try to latch onto the audio data. The display button is PLAY and activates the output relays. A flash indicates the -18 dB mute is on.

OPT 1 is the VCO TRACK on and using this the vco will try to lock onto the selected crystal. OPT 2 is the Synclock DIGOUT ON and forces the Synclock output ON is lit on the display.

The volume buttons give a guide to the upper and lower extremes. The frequency should be within. Volume up is the highest extreme and

extreme.

Here is how to force various modes. The buttons below are illuminated and the mode selected.

Before entering self test mode, make sure the following buttons are illuminated:

Signal mode

Select no XTAL 0 (Dig 4)

Class-1 mode

Select appropriate XTAL 0 (Dig 4). To simulate a Class-1 output, set the output voltage for the current signal sample rate (0.5 or 17.0V) and the LC output level.

Synclock mode

Select appropriate XTAL 0 (Dig 4). Select appropriate XTAL 0 (Display). It is sometimes necessary to toggle the Synclock output so that it changes.

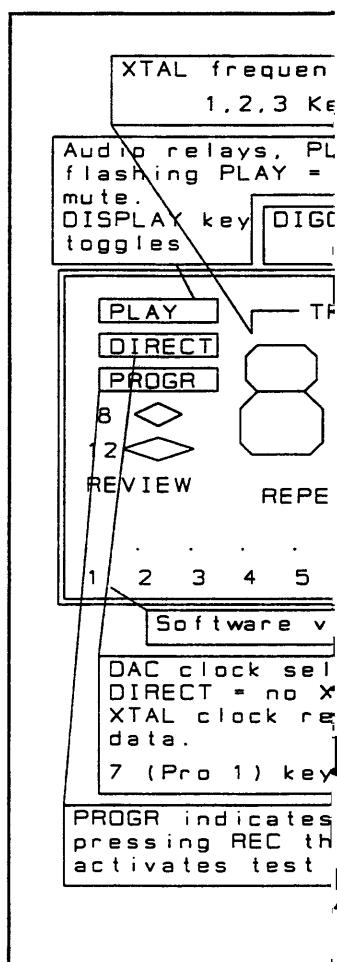


Figure 3 VFD display

DELTAF line, Z901, pin 6. These pulses are normally used by the micro to deduce that Synclock is not working.

Microprocessor pin by pin description

Since the micro is connected to most important areas of the unit, a lot of diagnostic information can be deduced from its pins with an oscilloscope. The table is shown below lists all the pins and describes the activity on them.

1	DATFILT	I/O	The data line of a three-wire serial interface to the Digital Filter chip. Information is sent to control the filter mode and volume. This line should be active when a new signal is found or the volume control is adjusted. Static high, pulses low and high when data is sent.
2	CLKFILT	O	The clock signal for the above data. Static low, pulses high to clock data.
3	RABFILT	O	The latch-in signal for the above data. Static high, low when data is being sent.
4	LOCK	I	Indicates if the XTAL PLL is locking properly. High when locked or low with no signal, sawtooth waveform when only in Signal mode.
5	REMOTE	I	RC5 codes received from display board.
6	DELTAF	I	Output from phase detector. Indicates phase of XTAL relative to incoming clock as a dc signal. The closer the phase the lower the voltage (In service mode only a triangular waveform can be seen when not locked but close to the incoming clock.)
7	ERF	I	Data error flag from SPDIF decoder. Causes immediate mute and loss of signal status.
8	NRES	I	Resets micro when low
9	XTAL	O	Chip clock resonator pin
10	EXTAL	I	Chip clock resonator pin
11	MODE 1	I	Used to set micro mode to use internal RAM and ROM and make as many IO pins available as possible. Single chip mode. Held high.
12	MODE 0	I	Used in conjunction with above. Held high.
13	NMNI	I	Key-press interrupt pin. Low indicates a key has been pressed on the display board.
14	VCC	PWR	+5v power supply to micro. C908 stores power to supply the micro RAM when the BB500 is disconnected from mains.
15	NSTBY	I	Low sends micro to sleep. This happens as soon as mains power is interrupted so that the volume, source and record selections can be saved in micro RAM.

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16	VSS	PWR	0v connection to micro
17	SRC0	O	Source selection bit 0 for Z603 and Z604
18	SRC1	O	Source selection bit 1
19	SRC2	O	Source selection bit 2
20	RECO	O	Record selection bit 0 for Z601 and Z602
21	REC1	O	Record selection bit 1
22	REC2	O	Record selection bit 2
23	n/c		
24	n/c		
25	CE/F2	I	Channel or frequency information from SPDIF decoder, Z701
26	CD/F1	I	"
27	CC/F0	I	"
28	CB/E2	I	Channel or error information from SPDIF decoder
29	CA/E1	I	"
30	NC0/E0	I	"
31	FLSEL	O	Selects whether channel or frequency and error information is output from Z701 in above signals
32	PHASE	O	Selects data phase. Not implemented in software.
33	DIGSEL	O	Selects digital audio input for digital filter
34	ADCSEL	O	Selects monitor source for digital filter
35	CLKSUB	O	Subcode clock for digital filter, not implemented in software
36	DATAO	O	Subcode data for digital filter, not implemented in software
37	I²CDAT	I/O	Data line to and from VFD display/keysan driver and OSD test jig
38	I²CCLK	I/O	Clock line for above data
39	VCC	PWR	Another power supply pin
40	RETHRU	O	Selects record output bypassing latch, Z607
41	RELTCH	O	Selects record output through latch, Z607
42	FIXF	O	Sets Voltage controlling frequency for XTAL oscillators to centre position +/- 40 ppm

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43	FPULL	O	+/- 100ppm frequency test. 0V : +100ppm, 5V : -100ppm, z : norm
44	N18dB	O	-18dB Audio output attenuator relay
45	WDOG	O	Watch dog timer pulses. No pulses cause time-out.
46	NTEST	O	Signals a micro self-test failure . Low = fail, high = pass.
47	AUDIO	O	Opens the output mute relays when high
48	VSS	PWR	Another supply pin
49	RMODE	I	Selects remote control mode from SW901
50	LEDSYN	O	Drive for SYNCLOCK LED
51	LEDSIG	O	Drive for SIGNAL LED
52	LEDVCO	O	Drive for CLASS 1 LED
53	LED32K	O	Drive for 32KHz sampling rate LED
54	LED44K	O	Drive for 44.1KHz sampling rate LED
55	LED48K	O	Drive for 48KHz sampling rate LED
56	LEDPWR	O	Drive for power LED
57	NOSC32	O	Selects 8.19200MHz XTAL when low
58	NOSC44	O	Selects 11.2896MHz XTAL when low
59	NOSC48	O	Selects 12.2880MHz XTAL when low
60	NBYPASS	O	XTAL clock bypassed for DAC when low, compliment of above
61	BYPASS	O	XTAL clock bypassed for DAC when high
62	SILENCE	I	Signal from digital filter, Z704, indicating digital silence. Causes reset of the digital filter's DC filter. See DCHLD flag on OSD screen.
63	SYN-CLOCK	O	Enables output from Z401 and Z404 of synclock clock signal
64	CLKPHS	O	Inverts phase of synclock clock output to ensure incoming data latches through Z711 and Z607 at correct data-to-clock phase

Disassembly for Service

CAUTION - ANTI STATIC PRECAUTIONS MUST BE FOLLOWED

1. Remove the top cover by removing 2 side screw screws (2 along the top edge and one at each end).
away from the unit.

Removal of Main Circuit Board

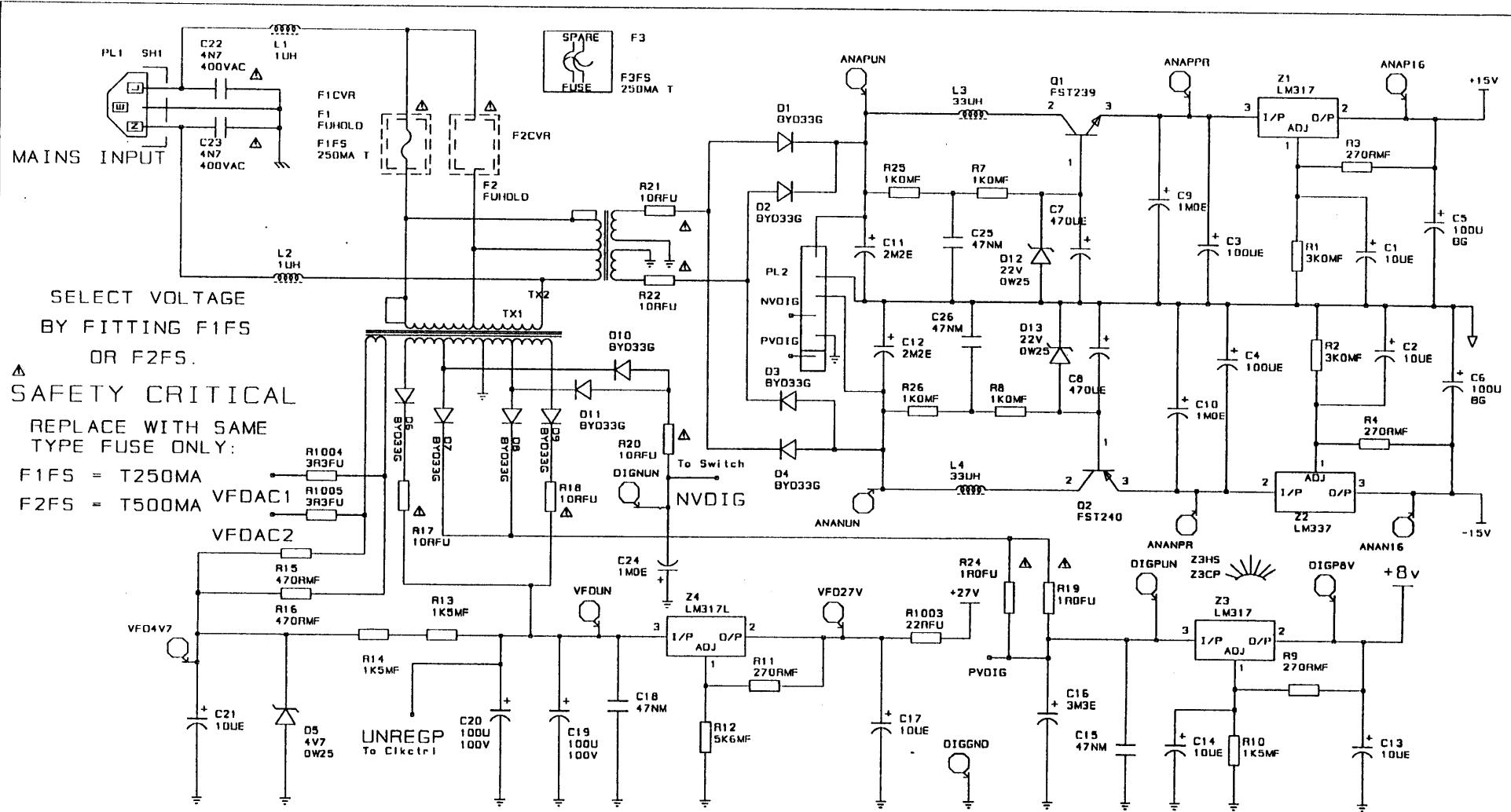
1. Remove 5 screws from the pcb (3 along the front between the transformers).
2. Remove 2 screw from the bottom edge of the rear
3. Disconnect the lead going to the display board .

The board should now be free of the chassis with the

The clock/DAC board in the "tin can" can be removed
pulling the board off its 4 six way connectors.

Removal of display PCB.

1. Remove the top cover.
2. Remove the front panel by undoing 4 screws (2 front off taking care not to damage the control buttons or switches).
3. The display pcb can now be removed by undoing the 4 screws and releasing the lead going to the main board.



ARCAM

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WATERBEACH
CAMBRIDGE
CB5 9PB

DRAWING TITLE
Black Box 500
Power Supply

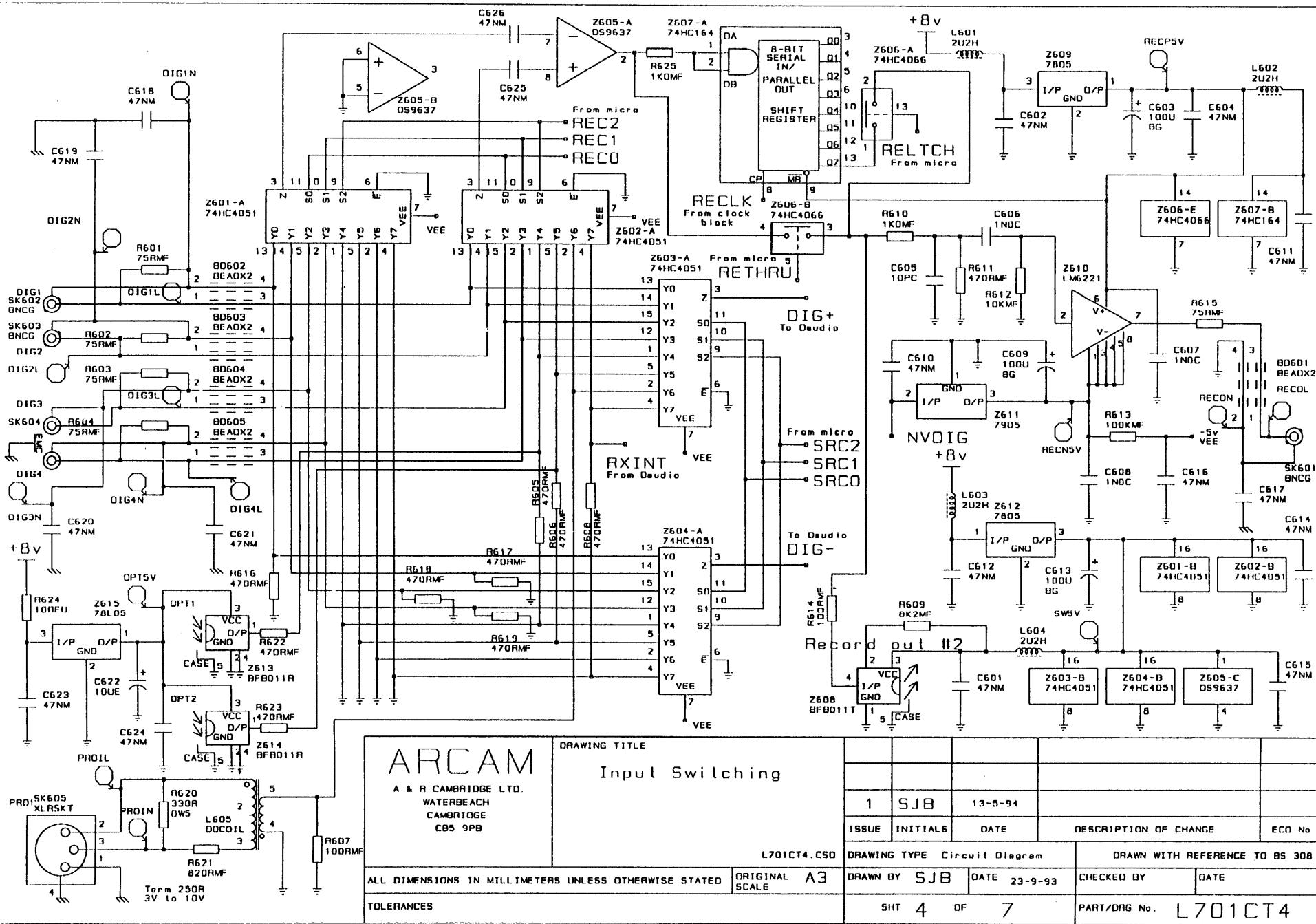
701CT1.CSD DRAWING TYPE Circuit Diagram DRAWN WITH REFERENCE TO BS 308

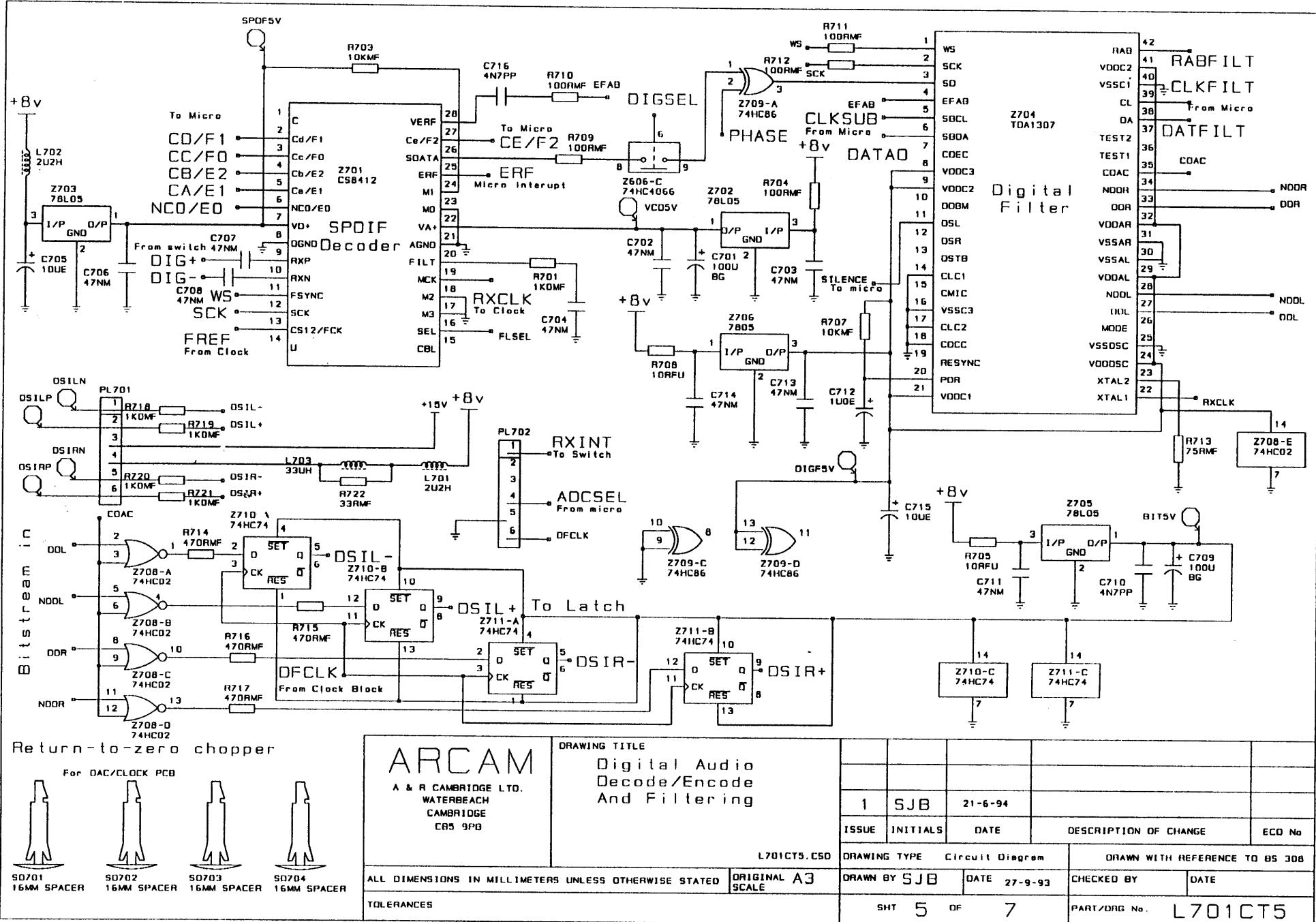
ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED ORIGINAL SCALE A3 DRAWN BY SJB DATE 12-11-93 CHECKED BY DATE

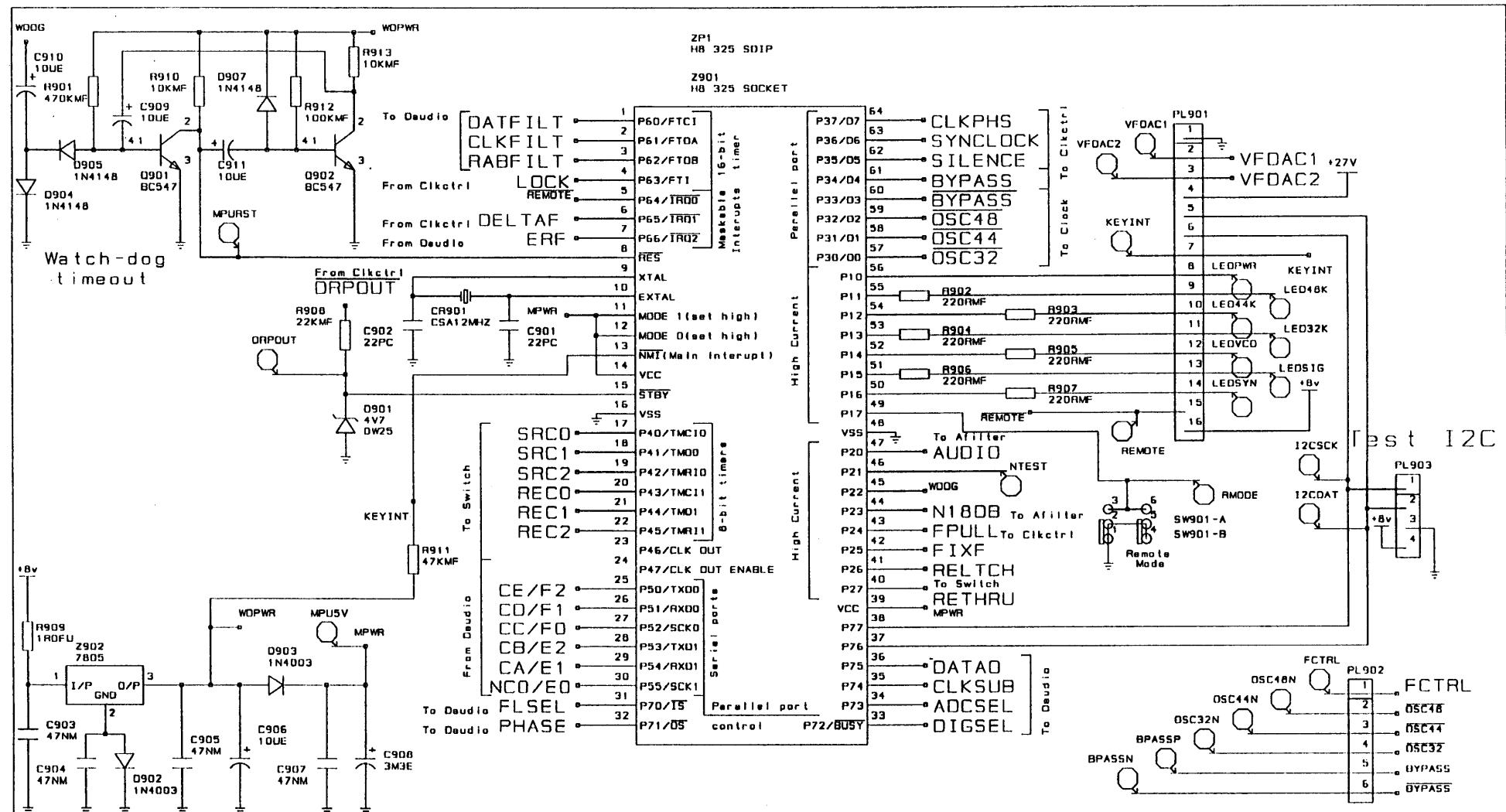
TOLERANCES SHT 1 OF 7 PART/ORG No. L701CT1

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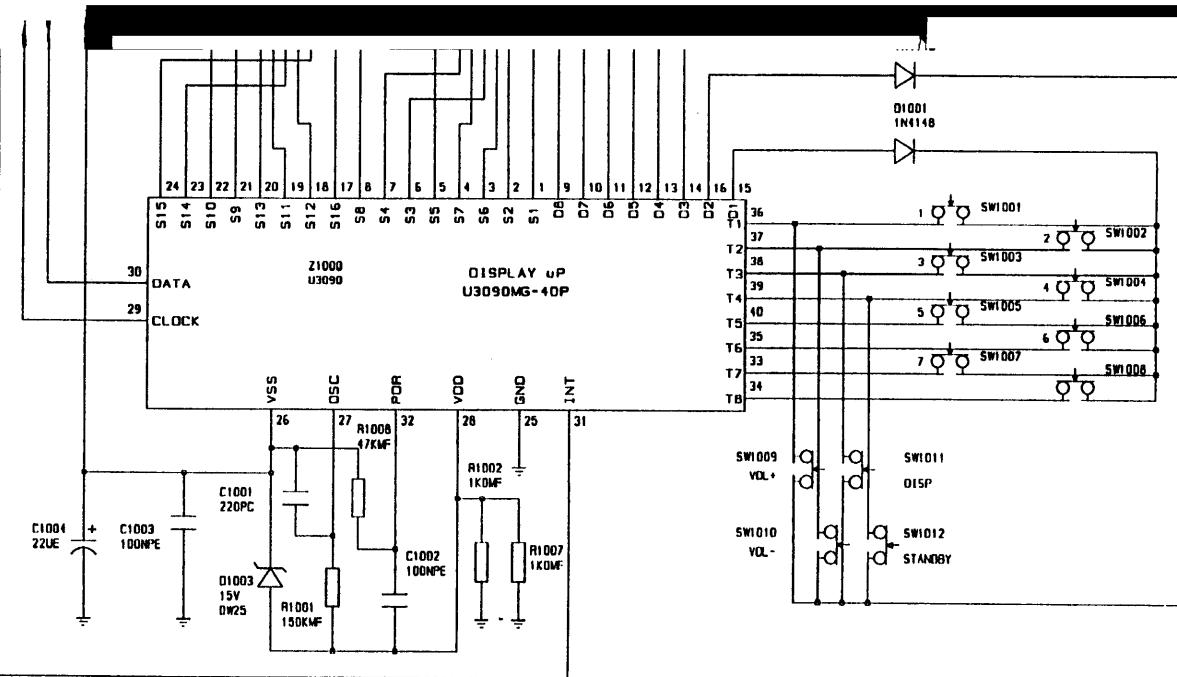
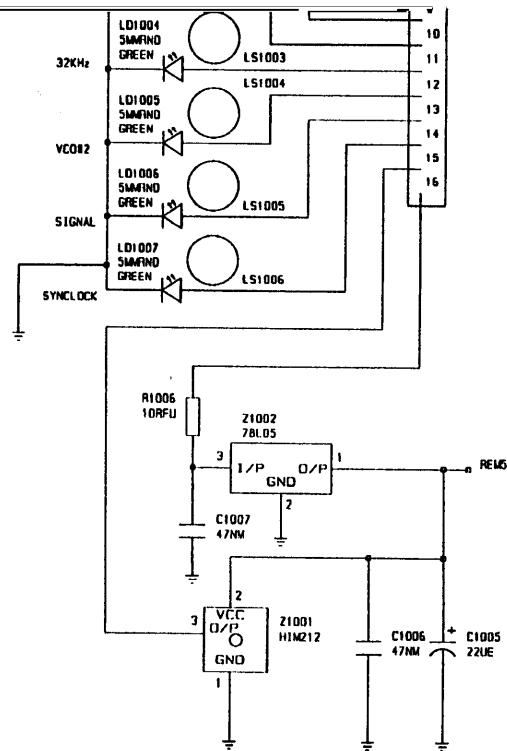
List of Circuit Diagrams
Power Supplies
Analogue Filter
Clock Control Circuit & PLL 2
Input Switching
Digital Audio Decode/Encode & Filtering
Microcontroller
Keyboard & Display Board
Bitstream Pulse Purifier
Voltage Controlled Crystal Clock Block



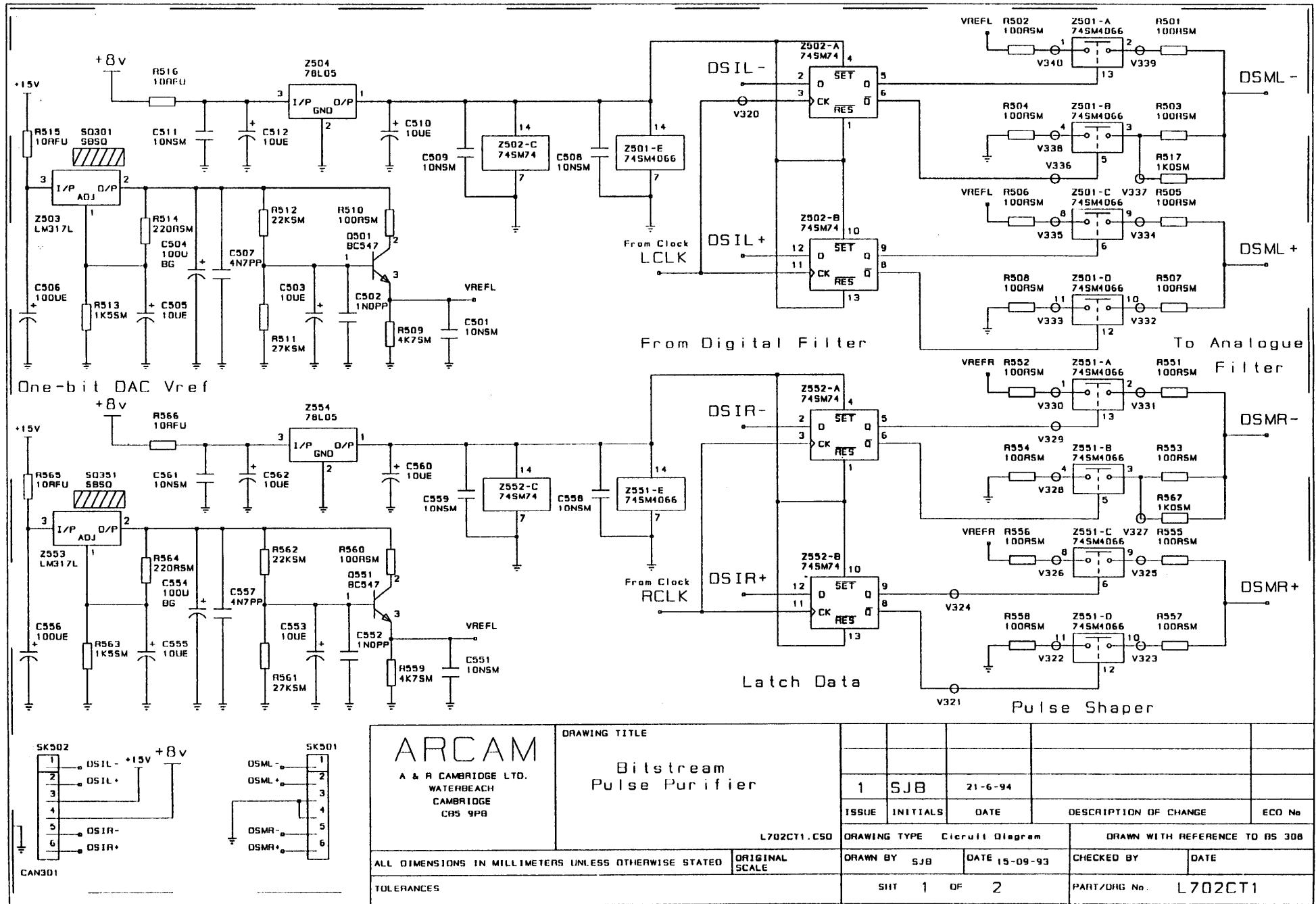


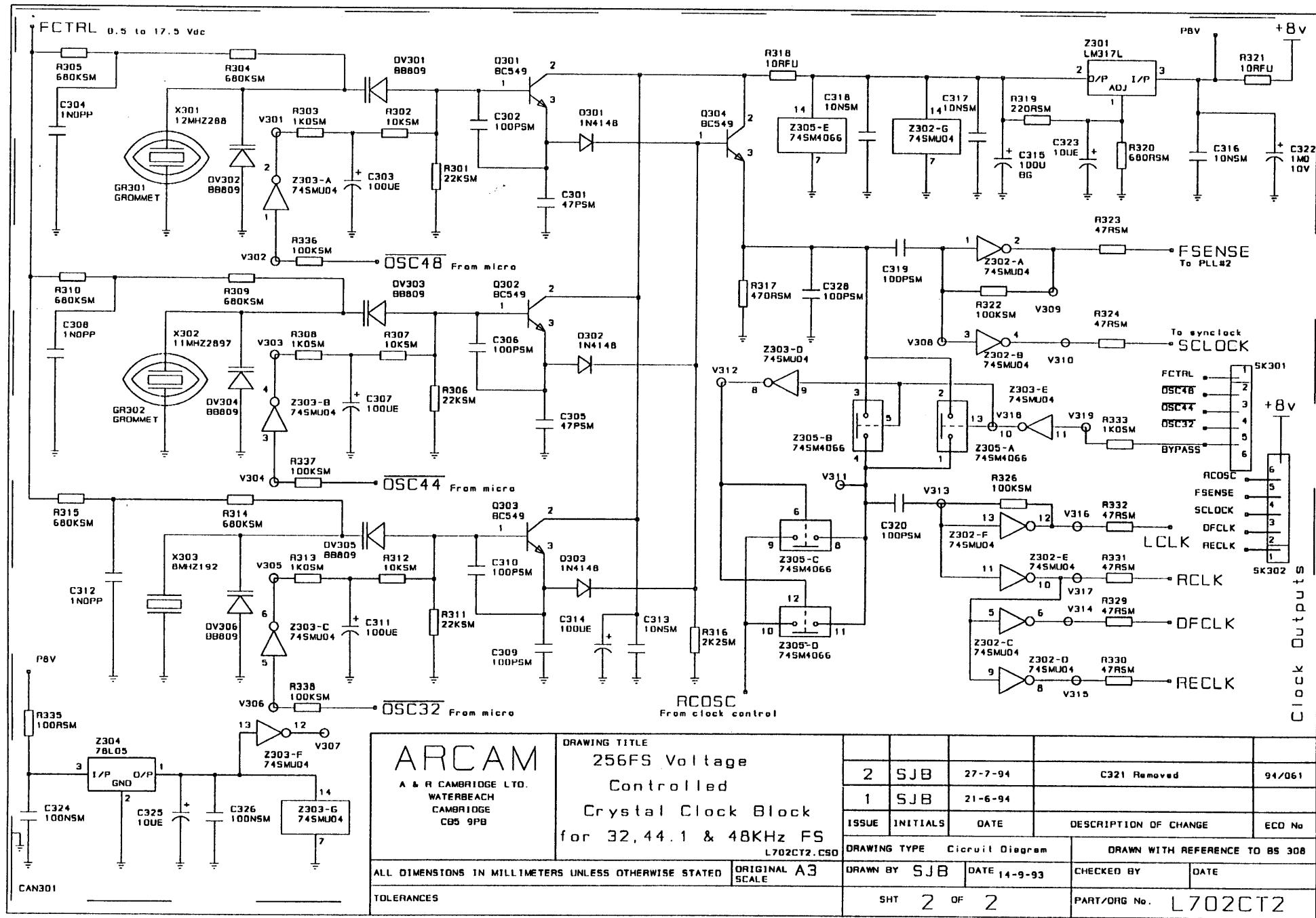


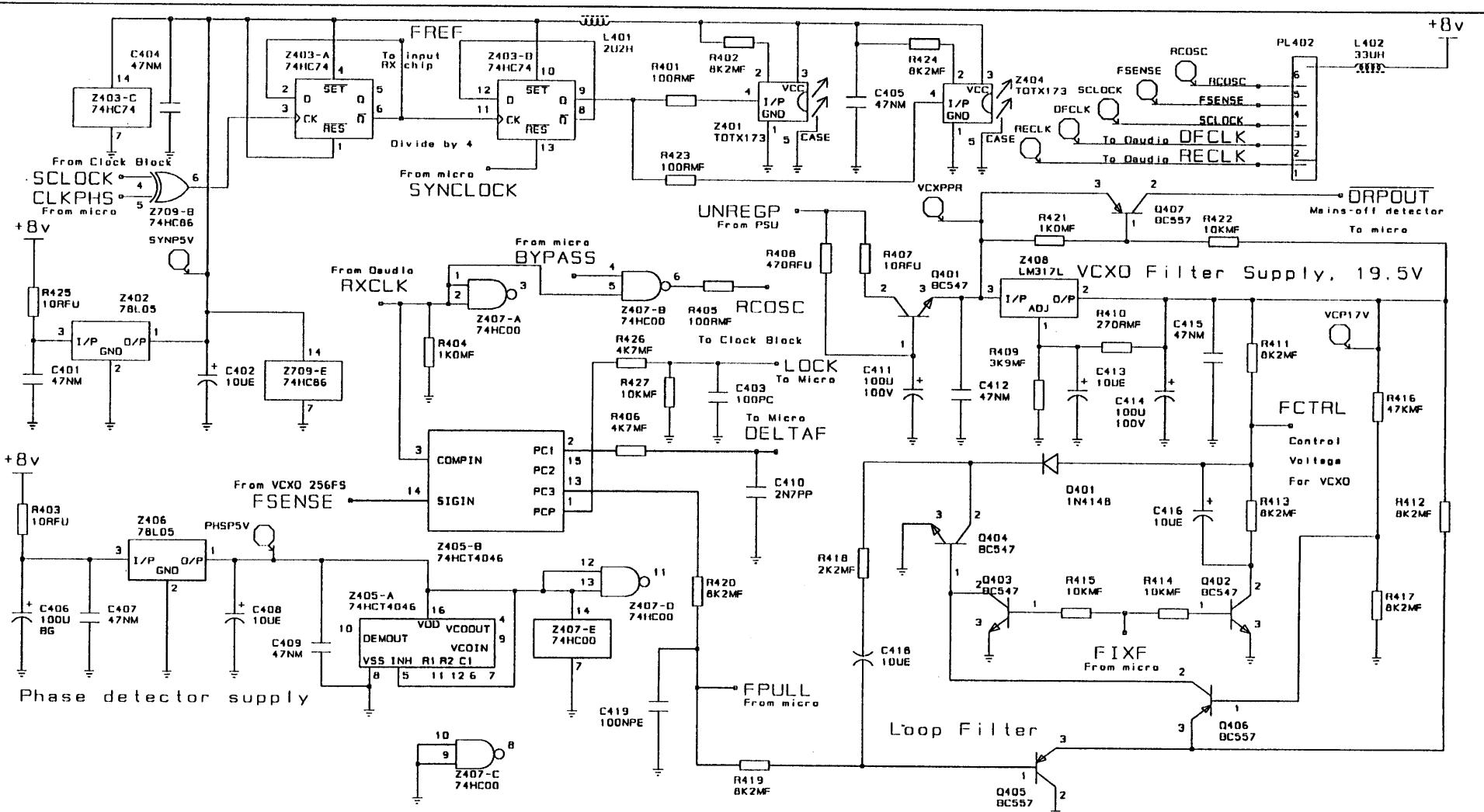
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ISSUE	INITIALS	DATE	ECO No			
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ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED		ORIGINAL SCALE A3	DRAWN BY SJB DATE 2-12-93		CHECKED BY DATE	
TOLERANCES		SHT 6 OF 7	PART/ORG No. L701CT6			



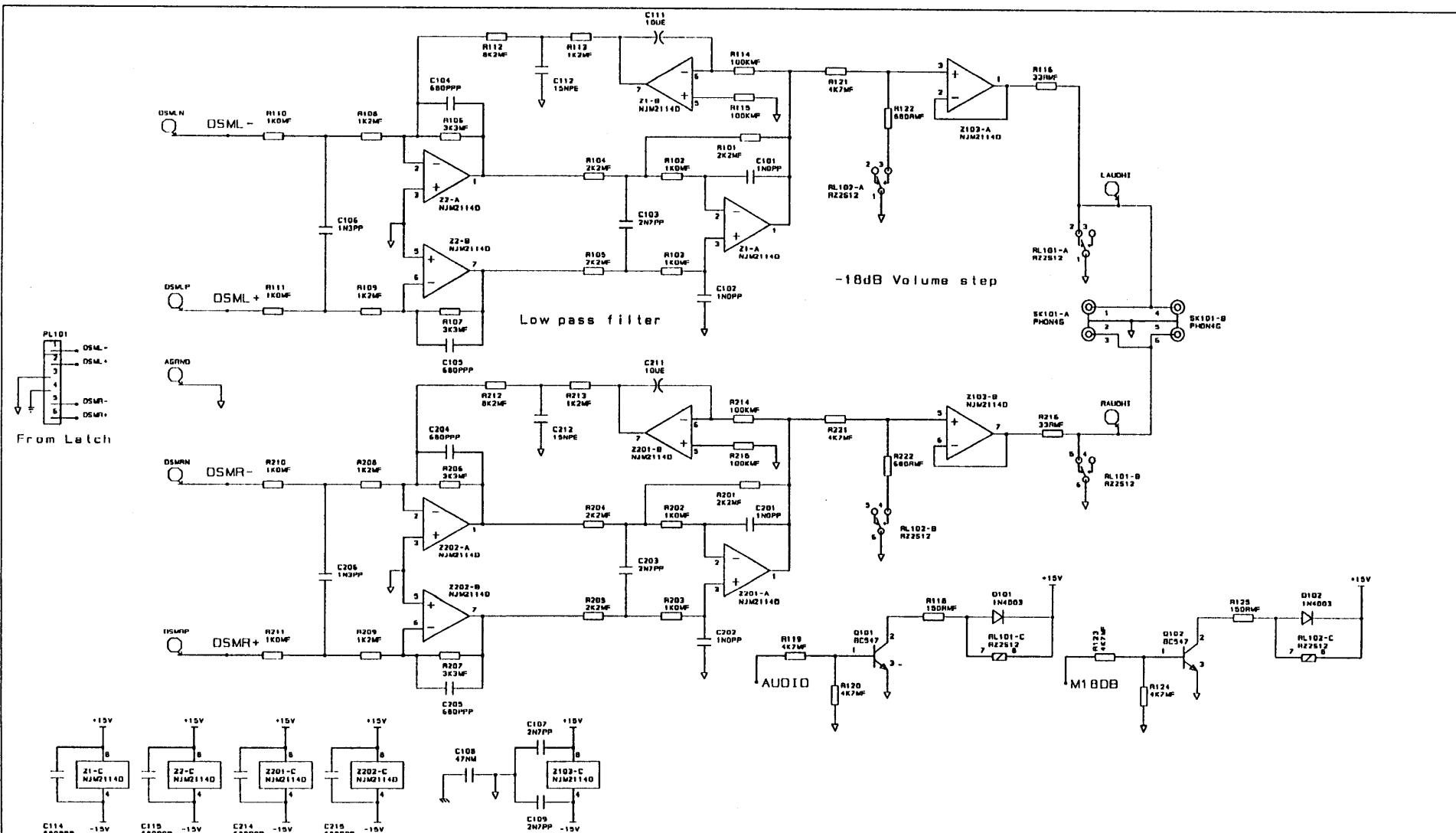
ARCAM		DRAWING TITLE							
A & R CAMBRIDGE LTD. WATERBEACH CAMBRIDGE CB5 9PB		Keyboard and Display PCB		1		SJB		13-5-94	
				ISSUE	INITIALS	DATE	DESCRIPTION OF CHANGE		ECO No
				L701C17.CSD		DRAWING TYPE Circuit Diagram		DRAWN WITH REFERENCE TO BS 308	
ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED				ORIGINAL A3 SCALE		DRAWN BY SJB		DATE 29-9-93	
TOLERANCES				SHT 7 DF 7		CHECKED BY		DATE	
						PART/ORG No.		L701CT7	







DRAWING TITLE					
Clock Control Unit and PLL#2		2	SJB	27-7-94	R409 was 3K3, now 3K9 R413 was 12K, now BK2
ISSUE	INITIALS	DATE	DESCRIPTION OF CHANGE		
L701CT3.CSD		DRAWING TYPE	Circuit Diagram		DRAWN WITH REFERENCE TO BS 308
ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED		ORIGINAL SCALE	A3	DRAWN BY SJB	DATE 16-09-93
TOLERANCES		SUIT	3	OF	7
PART/ORG No.		L701CT3			



ARCAM
A & R CAMBRIDGE
WATSBURGH
CAMBRIDGE
CB6 9PB

DRAWING TITLE
ANALOGUE FILTER

L701CT2.CD0

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

TOLERANCES

ORIGINAL A3
SCALE

DRAWN BY SJB DATE 16-09-93

CHECKED BY DATE

SJB 2 OF 7 PART/DRG No L701CT2