Arcam rDac Service manual

Andy Moore - issue 1

Overview

The rDac is a D to A convertor featuring Optical / Coaxial and USB inputs and utilizes a simple push button to cycle between the input option – when locked on to data the LED in front of the relevant source will light Green and audio should be present if the LED is RED in color the input is not locked onto relevant data.

Compatible formats include.

All PCM 2 channel

Input / bit depth	**32kHz**	**44.1kHz**	**48kHz**	**88.2kHz**	**96kHz**	**176kHz**	**192kHz**
USB 16 & 24 Bit	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	No	No
Optical 16 & 24 Bit	**Yes**	**Yes**	No	No	No	No	No
Coaxial 16 & 24 Bit	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes (1)**	**Yes (1)**
Wireless 16 Bit	No	**Yes**	No	No	No	No	No

(1) Source may not be capable of resolution

Power supply circuit page 5

A external 6v 600ma D.C power supply is used to supply the required power to the Connector at location CON400 this is then switched by the rear panel mounted power switch at location SW400, D400 is used for PSU monitor by associated circuitry formed by IC105 and IC104, D401 is used to prevent reverse bias of the PSU, the supply is then filtered by the network of L400 and C400 to form the main PSU source of +6v D.C.

The rDac features 7 separate regulated powers supplies details appear in the table below

Regulator locations	Voltage (d.c)	Components associated
REG400	+5v	Kleer option, optical input rec, LED array via IC102
REG401	+3V3	IC 100, 103, 104, 108, 107, 200, 201, 202, 203, 204, 205, 206, 301 mute circuit
REG402	+3V	SPDIF receiver
REG403	+5v	Output stage +5v
REG404	+3v3	Oscillator
REG405	+5v	DAC
IC400	-5v	Output stage -5v
IC107	+1.8	Main micro core voltage

Main micro **circuit page 2**

The main micro at location IC107 (on the diagram this is split into two area these are micro power and config + Micro I/O) we will deal with Micro power and config 1st.

Micro power and config

Two separate power supplies are required by the AT91SAM these are taken from 3V3 and 1V8 for the processor core – the micro is programmed with bespoke Arcam code the oscillator for the micro is at X101 and runs at 4MHz the TDI TDO TCK TMS ERASE NRST pins are for development Debug use and the connecter at location CON103 is not fitted to production items

Micro I/O

Pin descriptions

Pin name	Description
SPDIF INT	Interrupt flag from the SPDIF receiver
Source	To source select TACT switch
Mute RLY	Control of mute relay via TR100
DAC MUTE	DAC MUTE signal to Pin 25 of Wolfson DAC at location IC301
ENABLE KLEER	To MUX at location IC205A
ENABLE SPDIF	To MUX at location IC202A
SERIAL UC to KLEER	Serial control to KLEER wireless option
SERIAL KLEER to UC	Serial data from KLEER to UC
SCL	To EEprom at location IC108 / DAC at location IC301 / USB receiver at IC103
SDA	To EEprom at location IC108 / DAC at location IC301 / USB receiver at IC103
Enable LEDS	LEDs on control
LED 0	Binary select for LED control via 3 – 8 line decoder at location IC102
LED 1	Binary select for LED control via 3 – 8 line decoder at location IC102
LED 3	Binary select for LED control via 3 – 8 line decoder at location IC102

Input Stages and switching **Circuit pages 2 and 3**

The inputs are split into two groups with the Wolfson SPDIF receiver at location IC201 dealing with Optical and Coaxial selection whilst the MUX at locations IC202A IC202B and IC205A switch between SPDIF (opt or coax) and USB or KLEER under control from main micro.

SPDIF input

The Wolfson WM8805 SPDIF receiver supplies data in a format of Data , LRCLK, BCLK and MLCK, the output of IC201 runs directly to the DAC via the MUX at location IC202A with exception of the MCLK this take a path thru IC203 as part of the MCLK MUX between USB / KLEER and SPDIF MCLK's.

USB input

The USB data arrives at CON100 before traveling to the USB streaming control chip at location IC103 via the ESD protection Chip at location IC101 the chip is loaded with the DCS asynchronous/isochronous input system from IC100 at boot up.

IC103 has it own MCLK source at location IC204 another WM8805 this time used as an adaptive clock source the output is buffered by IC203C

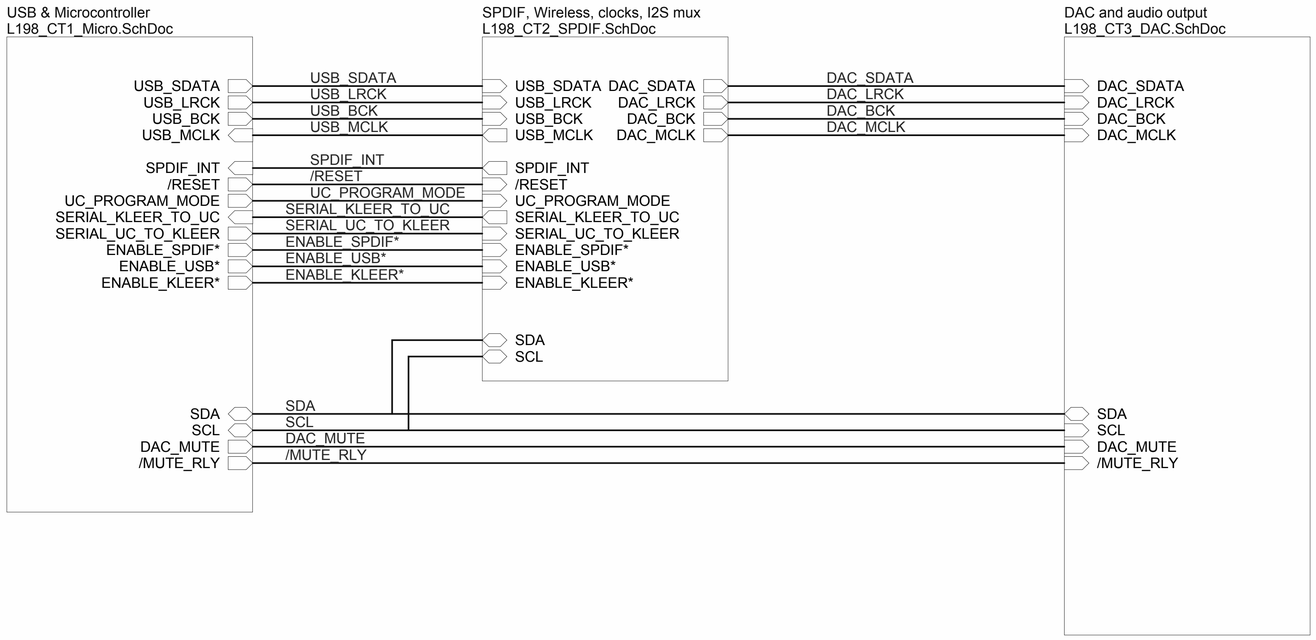
The Data , LRCLK, BCLK are switched to the DAC via IC202B with the MCLK coming via IC203.

DAC and Audio Stages **circuit page 4**

The Wolfson 8741 DAC can be found at location IC301 and takes its supplies from 3V3D and 5VDAC, data enters the chip on pins 1 – 5 and should be seen as below.

Pin loc	Signal type
Pin 1	LRCK
Pin 2	SDATA
Pin 3	BCK
Pin 5	MCLK

Analogue audio leaves the DAC as balanced pairs on pins 16 / 17 (left) and 12 / 13 (right) audio then travels thru and filter network enters the Op-amp at location IC300 a/b (L/R) and then onto IC302 a/b (L/R) output muting is twofold with both DAC mute (transistor mute) and full mute (relay) the DAC mute is provided by transistors TR302 and TR305 switching the audio down to 0v this under the control of the DAC MUTE line from IC107, the relay mute is provided by RLY300 and triggered from 2 lines one being the power detect sourced from D400 at power In – under low power the relay will close at 5.3v D.C and is flipped by IC105 in combination with IC104 the output of IC104 is low to mute the relay is switched by TR300.



U_L198_CT4_PSU
L198_CT4_PSU.SchDoc

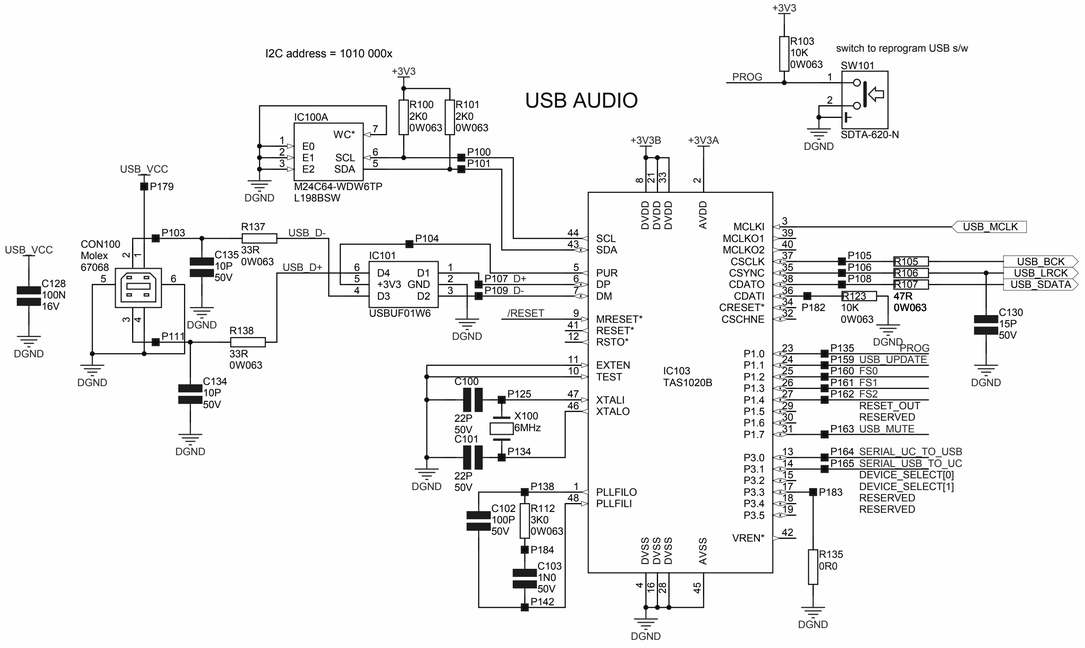
DRAWING TITLE **rDAC Top Level**						
ARCAM	**Filename:** L198_top_level.SchDoc	10_Exxx	PK	14/09/10	EMC changes from Telnova	2.0
	Notes:	10_E122	PG	08/09/10	Change X200 to 12MHz	1.1
		10_E066	PK	12/04/10	None to this sheet	1.0
		ECO No.	INITIALS	DATE	DESCRIPTION OF CHANGE	ISSUE

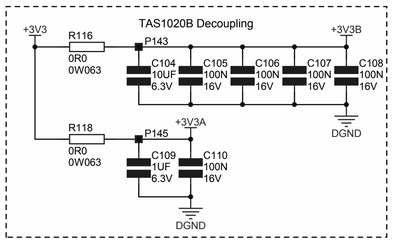
A & R Cambridge Ltd.
Pembroke Avenue
Waterbeach
Cambridge CB25 9QR

Contact Engineer: Peter Kuell	**Contact Tel:** (01223) 203207 tel No	**Printed:** 22/09/2010	**Sheet** 1 of 5	A3	**DRAWING NO.** L198CT

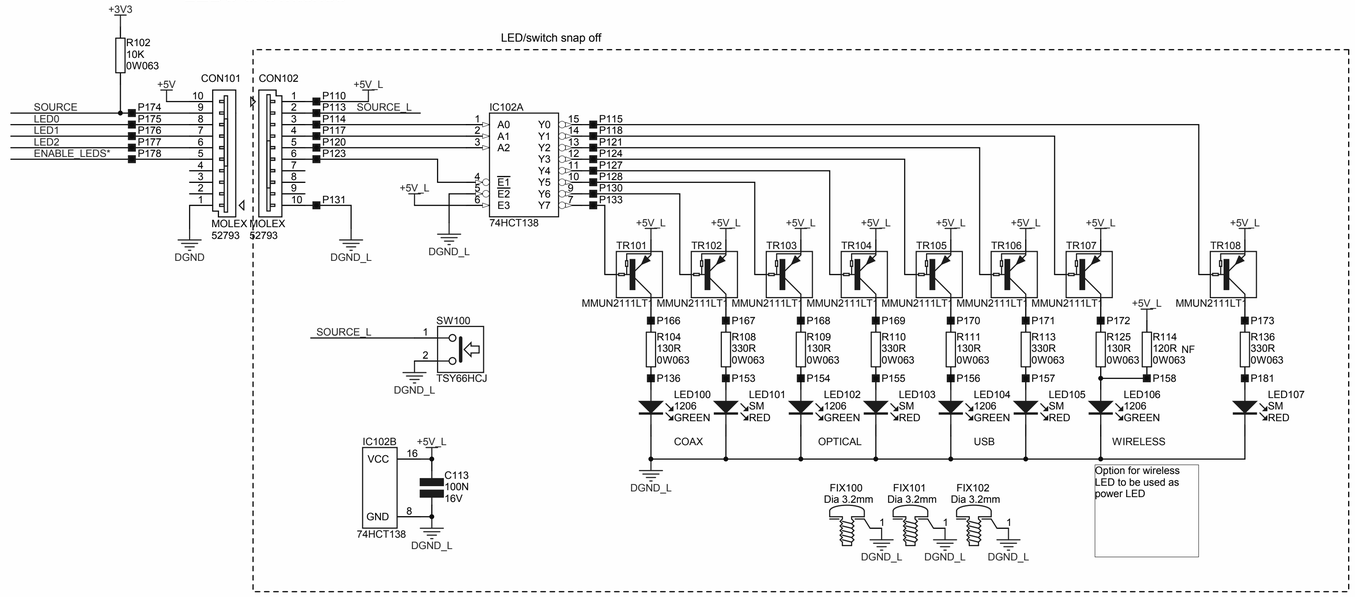
USB AUDIO

I2C address = 1010 000x

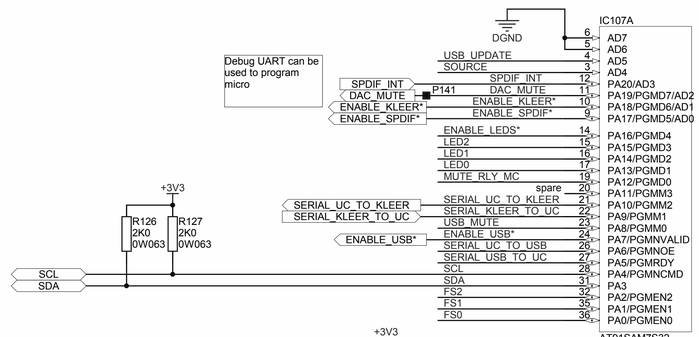




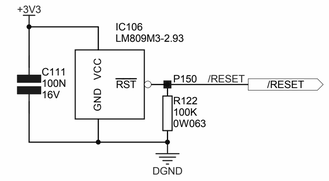
LEDS & Switches

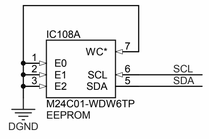


Micro I/O

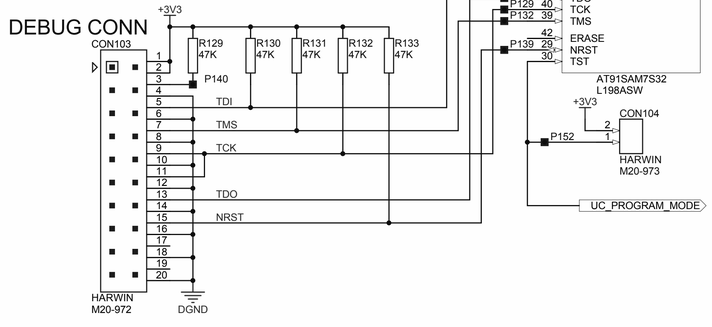


System reset



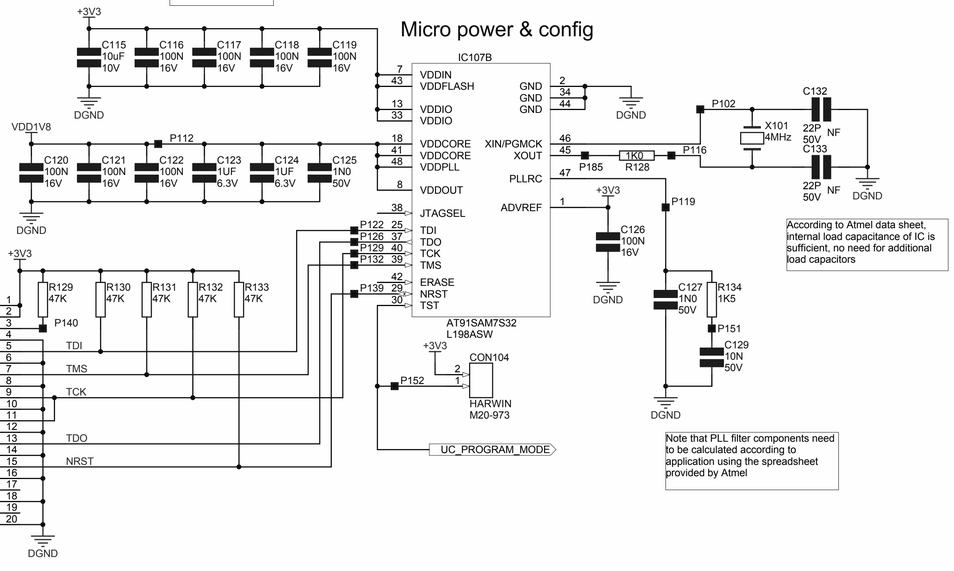


DEBUG CONN

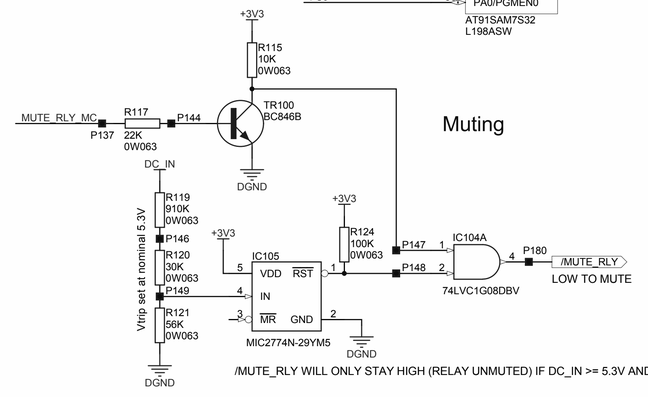


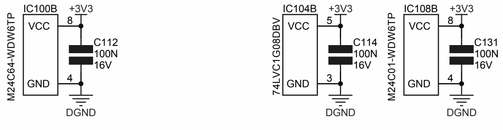
See Atmet apps note for placement of decoupling caps

Micro power & config



Muting





ITEM	QTY	PART No.	DESCRIPTION	NOTES
PCB100	1	L198PB	Blank PCB rDAC	

DRAWING TITLE

rDAC USB & Micro

ARCAM

A & R Cambridge Ltd.
Pembroke Avenue
Waterbeach
Cambridge CB25 9QR

Filename: L198_CT1_Micro.SchDoc

Notes:

ECO No.	INITIALS	DATE	DESCRIPTION OF CHANGE	ISSUE
10_E131	PK	14/09/10	EMC changes from Telnova	2.0
10_E122	PG	08/09/10	Change X200 to 12MHz	1.1
10_E066	PK	12/04/10	Green LEDs and drive resistors changed	1.0

Contact Engineer: Peter Kuell | Contact Tel: (01223) 203207 | Printed: 22/09/2010 | Sheet 2 of 5 | A2 | DRAWING NO. L198CT

SPDIF receiver

SDIN/HWMODE sets software control (pull up on other sheet)
SWIFMODE sets 2 wire software mode
CSB/GPO2 sets I2C address = 0111 010x

Optical in

COAX in

5V to 3.3V conversion

WM8805 decoupling

I2S MUX

LAYOUT NOTE:
Ensure the 2 LVC244s and the series resistors are placed close together

MCLK MUX

KLEER BOARD

buffer tr-states serial TX line of Kleer module while in programming mode

Use this connector to program & debug the Kleer module

Oscillator for USB audio

SDIN/HWMODE sets software control (pull up on other sheet)
SWIFMODE sets 2 wire software mode
CSB/GPO2 sets I2C address = 0111 011x

Master clock for USB needs to be kept at the appropriate frequency all the time, even when SPDIF input is selected

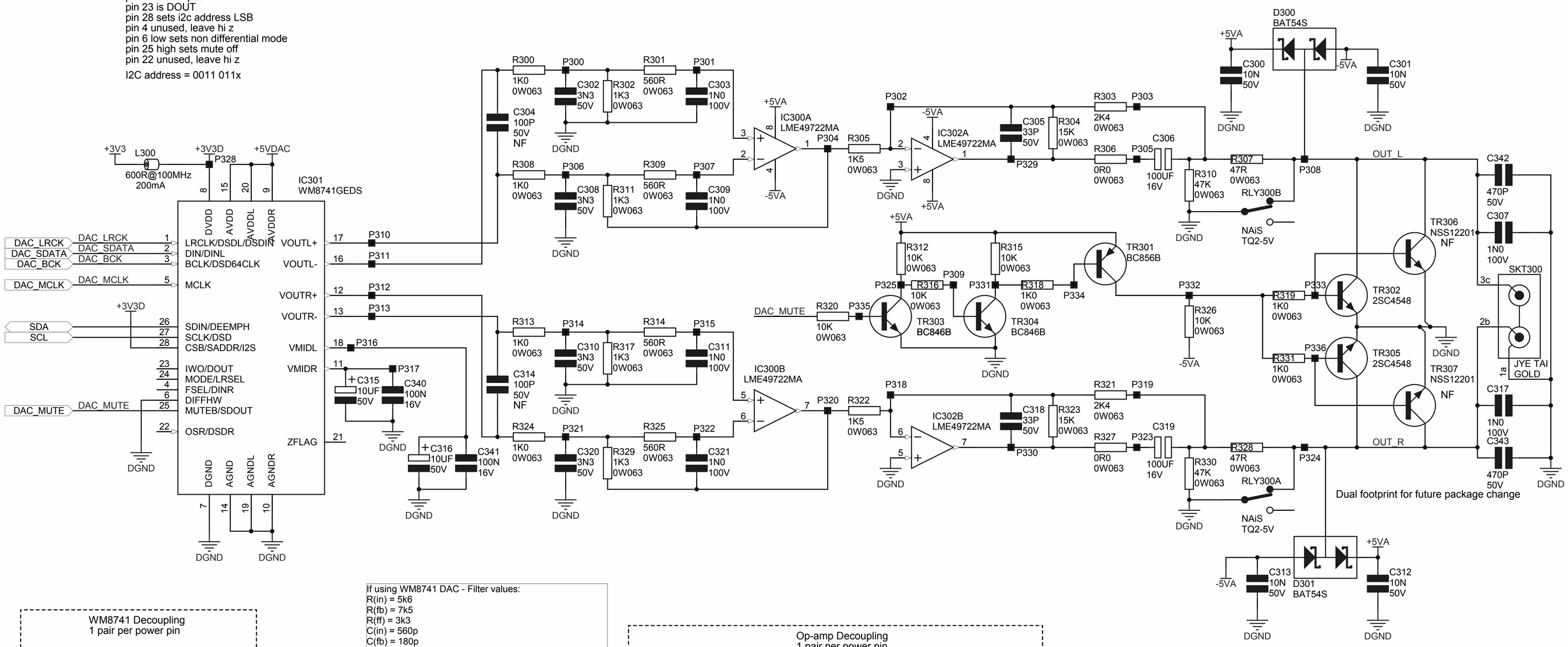
Use this connector to program the Atmel microcontroller

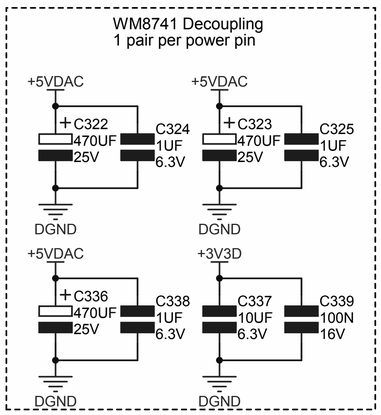
DRAWING TITLE: **rDAC SPDIF & Clocks**					
ARCAM A & R Cambridge Ltd. Pembroke Avenue Waterbeach Cambridge CB25 9QR	Filename: L198_CT2_SPDIF.SchDoc	10_E131	PK	14/09/10	EMC changes from Telnova 2.0
	Notes:	10_E122	PG	08/09/10	Change X200 to 12MHz 1.1
		10_E066	PK	12/04/10	None to this sheet 1.0
		ECO No.	INITIALS	DATE	DESCRIPTION OF CHANGE ISSUE
	Contact Engineer: Peter Kuell	Contact Tel: (01223) 203207	Printed: 22/09/2010	Sheet 3 of 5	A2 DRAWING NO. L198CT

DAC is configured in software mode

pin 24 open sets 2-wire interface mode
pin 26 SDA input
pin 27 SCL input
pin 23 is DOUT
pin 28 sets i2c address LSB
pin 4 unused, leave hi z
pin 6 low sets non differential mode
pin 25 high sets mute off
pin 22 unused, leave hi z

I2C address = 0011 011x

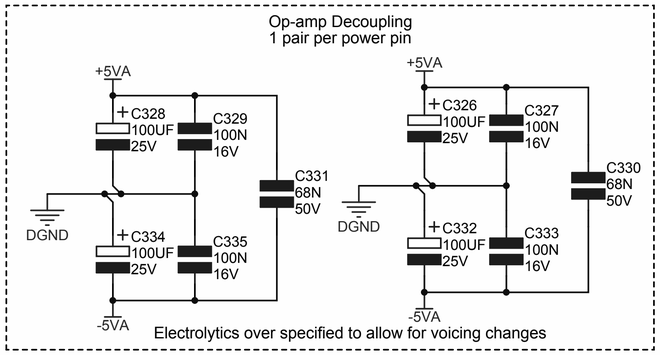


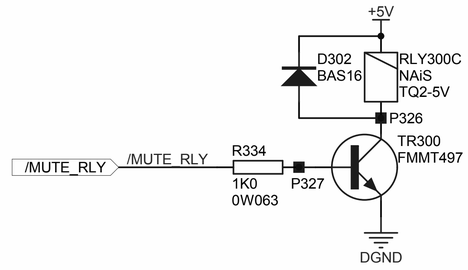


If using WM8741 DAC - Filter values:
R(in) = 5k6
R(fb) = 7k5
R(ff) = 3k3
C(in) = 560p
C(fb) = 180p

2nd order Bessel filter characteristics (from simulation):
-3dB = 78.5kHz
@20kHz = -0.175dB
@1MHz = -40.0dB
passband gain = +2.54dB
passband out level = 2.128Vrms (5.0V DAC supply)
passband out level = 2.341Vrms (5.5V DAC supply)
Group delay passband = 2.7724uS
Group delay delta = -2.0238nS
Inverting input load (min) = 3.56k

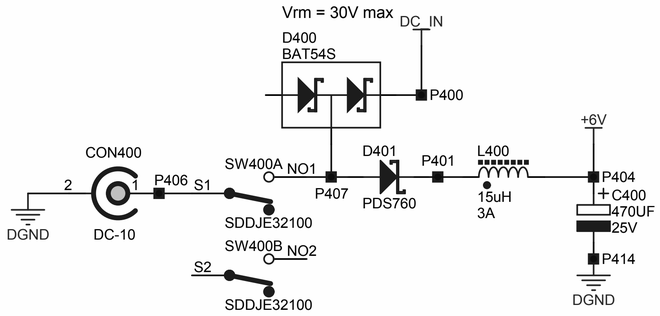
Special note about WM8741:
With non-emphasised audio data, DAC can internally reduce gain by 2dB before the digital filter to reduce disc clipping artefacts. Analogue filter has gain to compensate for this.

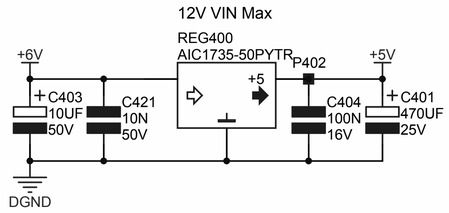


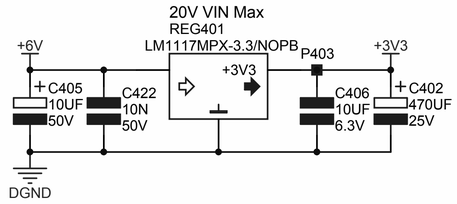


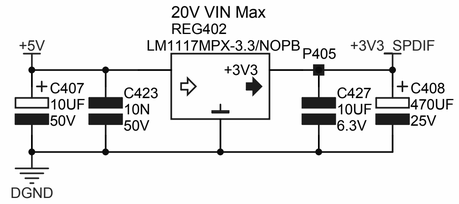
DRAWING TITLE **rDAC DAC and filter**					
ARCAM A & R Cambridge Ltd. Pembroke Avenue Waterbeach Cambridge CB25 9QR	**Filename:** L198_CT3_DAC.SchDoc	10_E131	PK	14/09/10	EMC changes from Telnova 2.0
	Notes:	10_E122	PG	08/09/10	Change X200 to 12MHz 1.1
		10_E066	PK	12/04/10	RLY300 changed to TQ through lead, correct D301 -5V connection. Dual footprint mute transistors Some filter resistor value changes 1.0
		ECO No.	INITIALS	DATE	DESCRIPTION OF CHANGE ISSUE
	Contact Engineer: Peter Kuell	Contact Tel: (01223) 203207 tel No	Printed: 22/09/2010	Sheet 4 of 5	A3 DRAWING NO. L198CT

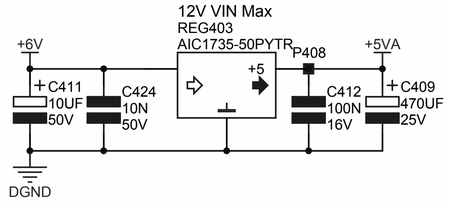
This diode is just for the power rail monitoring
which should be done before any bulk storage

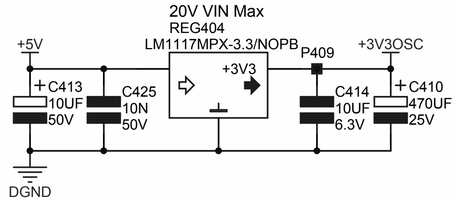


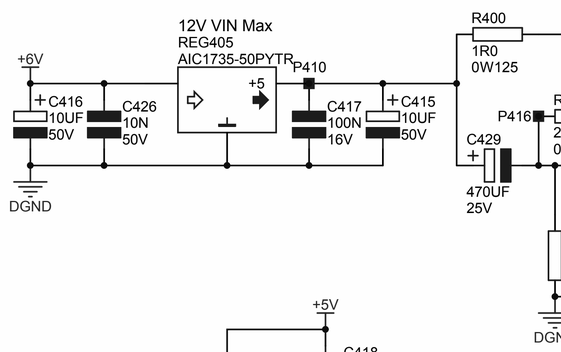


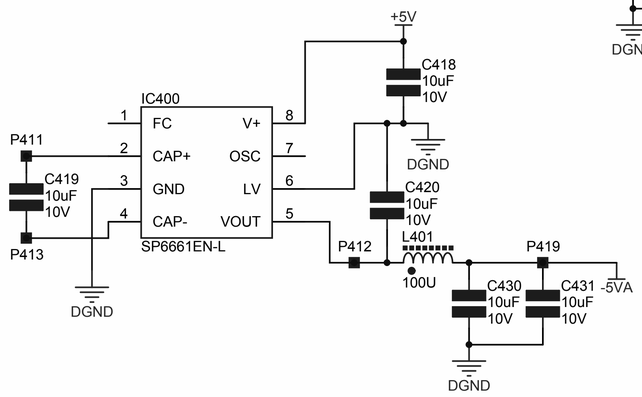


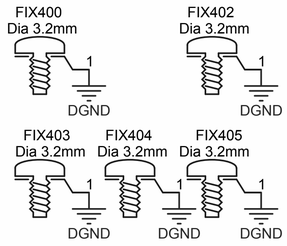


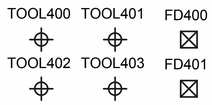




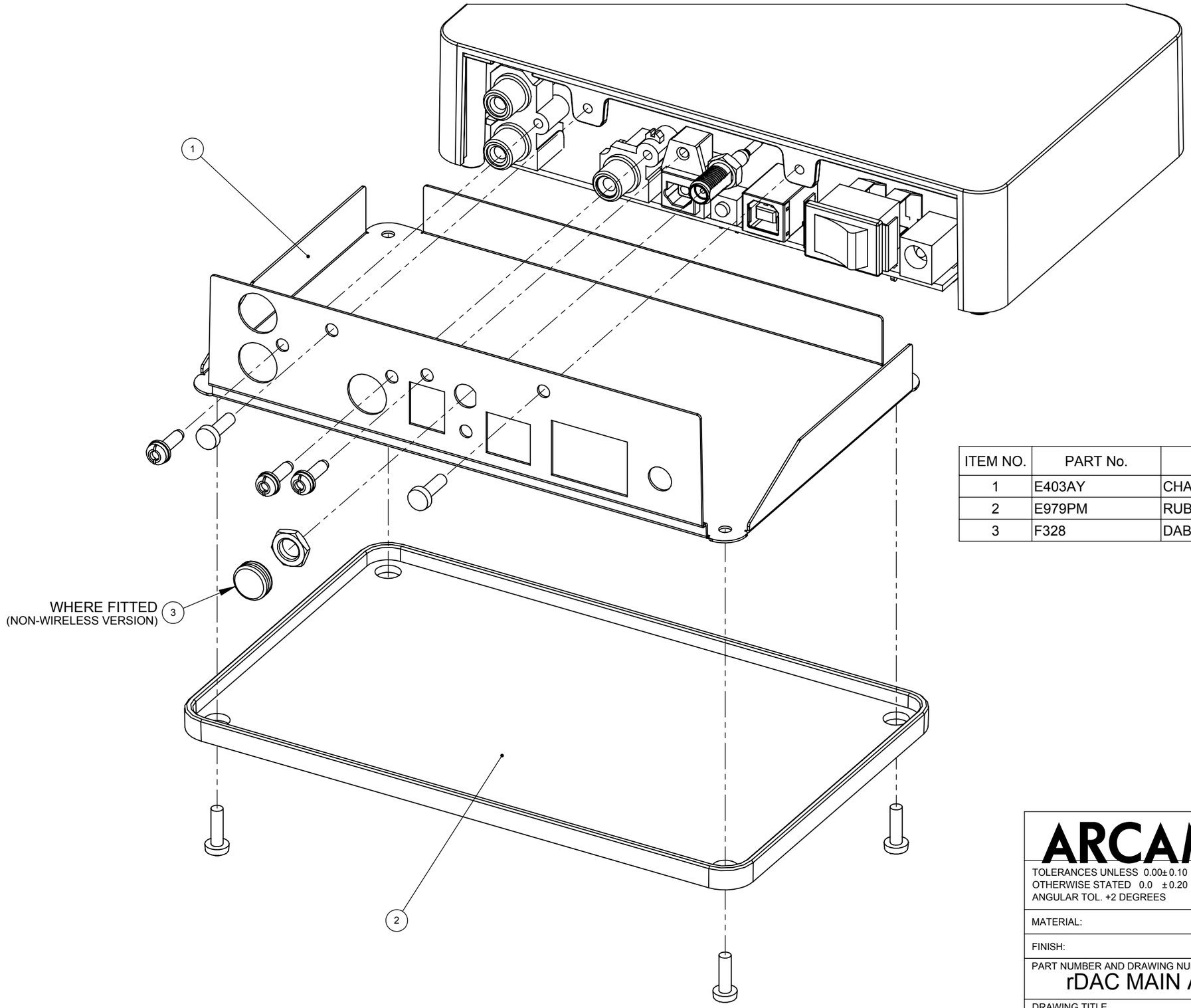








DRAWING TITLE **rDAC PSU**					
ARCAM A & R Cambridge Ltd. Pembroke Avenue Waterbeach Cambridge CB25 9QR	**Filename:** L198_CT4_PSU.SchDoc	10_E131	PK	14/09/10	EMC changes from Telnova 2.0
	Notes:	10_E122	PG	08/09/10	Change X200 to 12MHz 1.1
		10_E066	PK	12/04/10	LDO changed to AIC1735, noise finesser changes 1.0
		ECO No.	INITIALS	DATE	DESCRIPTION OF CHANGE ISSUE
	Contact Engineer: Peter Kuell **Contact Tel:** (01223) 203207 tel No	**Printed:** 22/09/2010	**Sheet** 5 of 5	A3	**DRAWING NO.** L198TCT



ITEM NO.	PART No.	DESCRIPTION	QTY
1	E403AY	CHASSIS ASSY	1
2	E979PM	RUBBER BASE	1
3	F328	DAB BUNG	1

ARCAM A & R CAMBRIDGE LTD

TOLERANCES UNLESS 0.00± 0.10
OTHERWISE STATED 0.0 ± 0.20
ANGULAR TOL. +2 DEGREES

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

DRAWN BY: MCM
DATE: 8-9-2010
CHECKED BY: MGB
ORIGINAL SCALE 1:1

MATERIAL:

FINISH:

SHT 1 OF 3

PART NUMBER AND DRAWING NUMBER
rDAC MAIN ASSEMBLY

DRAWING TITLE
BASE

A3

0 10 20 30 40 50 60 70 80 90 100

ECO NR.	DATE	CHG.	ZONE	DESCRIPTION OF CHANGE	REL.	DR.	CHK.
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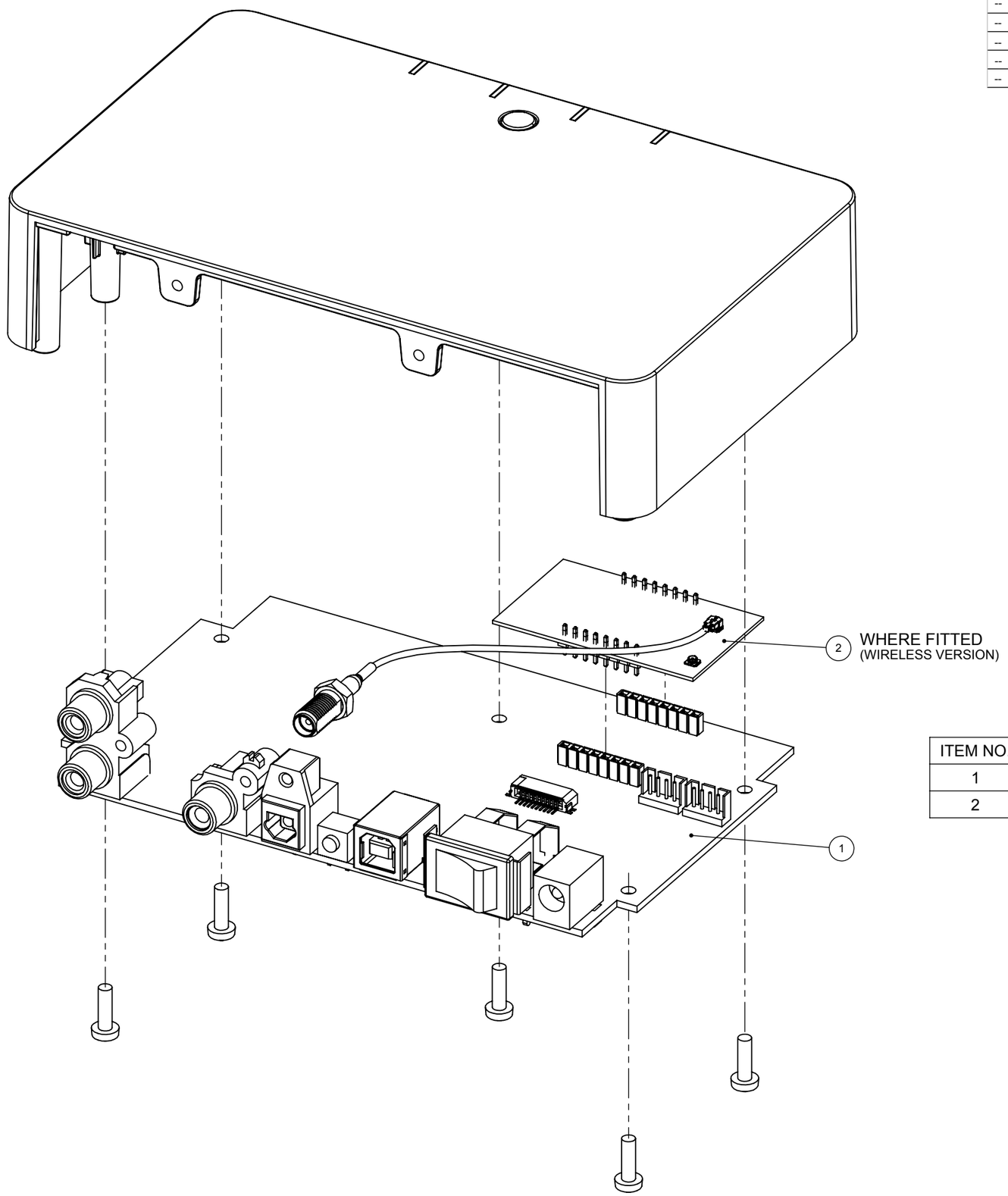

ITEM NO.	PART No.	DESCRIPTION	QTY
1	L198AY	MAIN PCB ASSY	1
2	L202AY	KLEER WIRELESS PCB	1

ARCAM A & R CAMBRIDGE LTD

TOLERANCES UNLESS 0.00± 0.10
OTHERWISE STATED 0.0 ± 0.20
ANGULAR TOL. +2 DEGREES

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

DRAWN BY: MCM
DATE: 8-9-2010
CHECKED BY: MGB
ORIGINAL SCALE 1:1

MATERIAL:

FINISH:

SHT 2 OF 3

PART NUMBER AND DRAWING NUMBER
rDAC MAIN ASSEMBLY

DRAWING TITLE
MAIN PCB

A3

0 10 20 30 40 50 60 70 80 90 100

ECO NR.	DATE	CHG.	ZONE	DESCRIPTION OF CHANGE	REL.	DR.	CHK.
--	--	--	--	--	--	--	--
--	--	--	--	--	--	--	--
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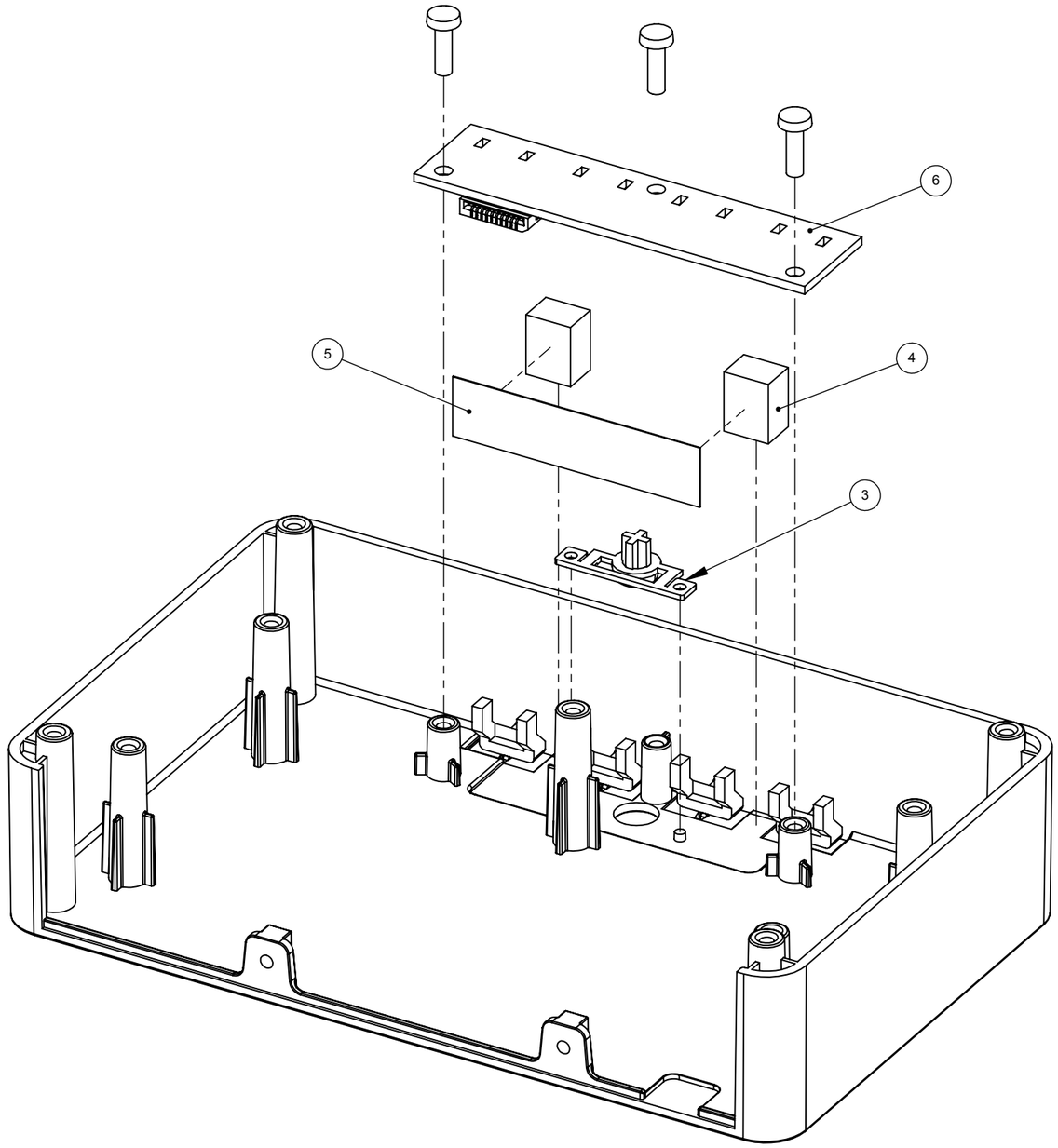
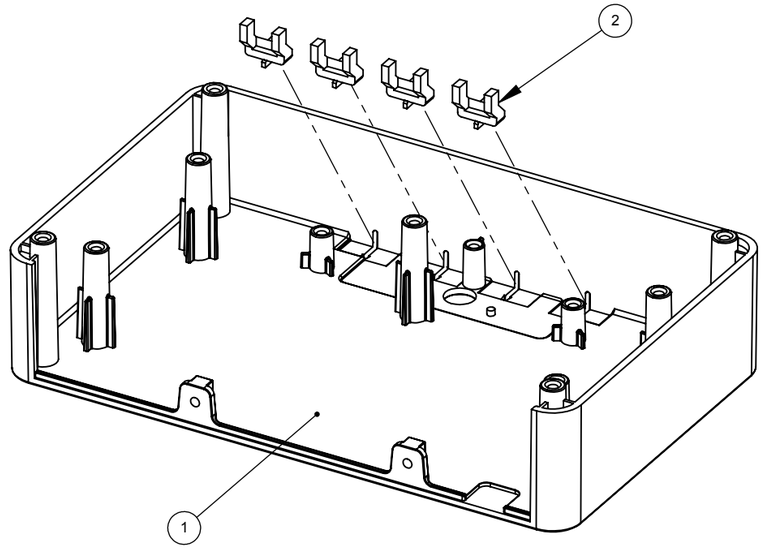
--	--	--	--	--	--	--	--





ITEM NO.	PART No.	DESCRIPTION	QTY
1	E402AY	COVER ASSY	1
2	E981PM	LIGHT PIPE	4
3	E980PM	BUTTON	1
4	E852AP	SELF-ADHESIVE FOAM PAD	2
5		TAPE	1
6	L198AY (part)	MAIN PCB - BUTTON + LEDs	1

ARCAM A & R CAMBRIDGE LTD

TOLERANCES UNLESS 0.00±0.10
OTHERWISE STATED 0.0 ±0.20
ANGULAR TOL. +2 DEGREES

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

DRAWN BY:	MCM
DATE:	8-9-2010
CHECKED BY:	MGB
ORIGINAL SCALE 1:1	
SHT 3 OF 3	

MATERIAL:

FINISH:

PART NUMBER AND DRAWING NUMBER
rDAC MAIN ASSEMBLY

DRAWING TITLE
COVER

A3

0 10 20 30 40 50 60 70 80 90 100

A&R Cambridge Ltd

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www.arcam.co.uk