

19 Series

Schematic

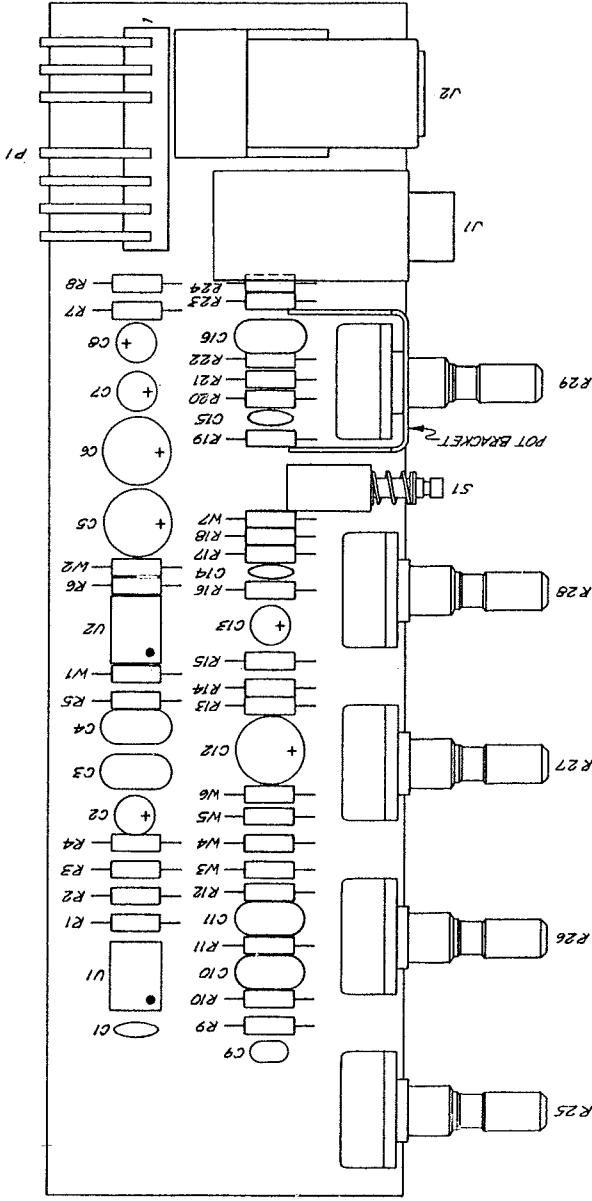
B I A M P[®]

S Y S T E M S

10074 SW Arctic Drive Beaverton, OR 97005 503-641-7287

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- P1 PIN ASSIGNMENTS:**
1. EFX BUSS
 2. MONITOR BUSS
 3. MAIN BUSS
 4. PWD
 5. SIGNAL GROUND
 6. POWER GROUND
 7. -15V
 8. +15V



REV.	E.C.D.	CHANGE	DATE	BY

ITEM	PART NO.	DESCRIPTION	SIZE	QTY.
1				
2				
3				
4				

DATE	3/6/82	DATE	3/6/82
CHECKED	JD	CHECKED	JD
ENGINEER		ENGINEER	
DESIGN		DESIGN	
MATERIAL		MATERIAL	
FINISH		FINISH	
MODEL		MODEL	
APPLICATION		APPLICATION	

BIAMP SYSTEMS INC.	ASSEMBLY A1, 619 JURUT PCB
SCALE 2X	DO NOT SCALE DRAWING
SHEET 1 OF 1	

D

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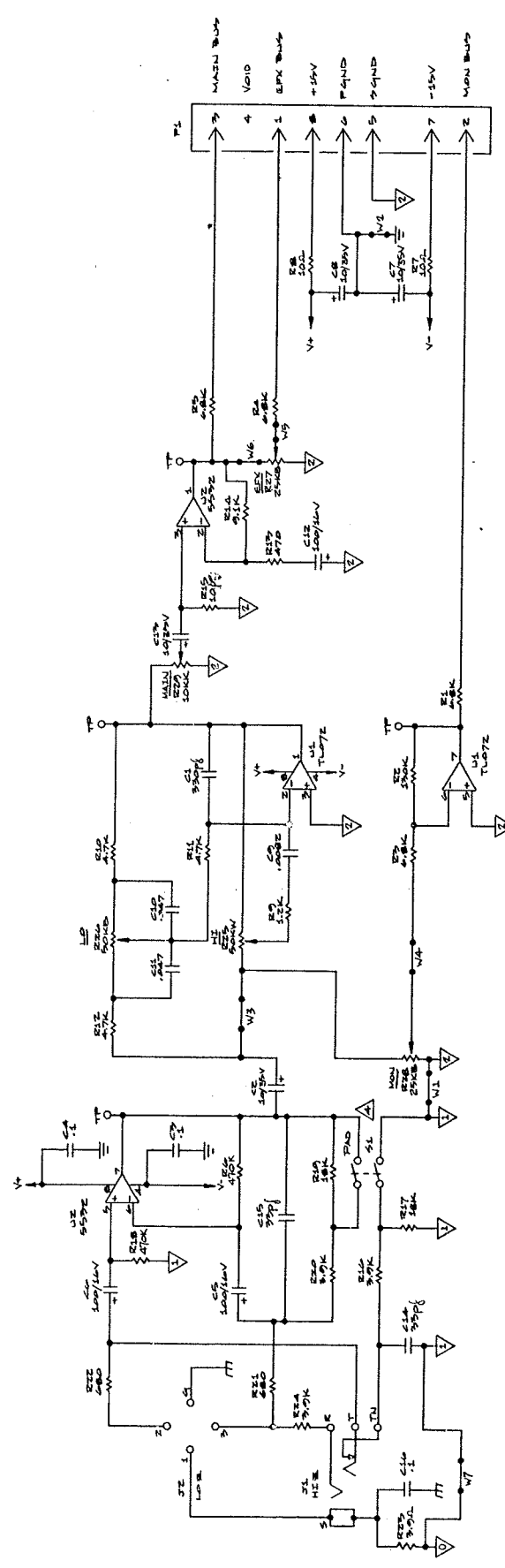
D

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- LAST G
- LAST JE
- LAST P
- LAST R
- LAST S
- LAST T
- LAST U
- LAST V
- LAST W

NOTES: UNLESS OTHERWISE SPECIFIED,
 1. ALL RESISTORS IN OHMS
 2. ALL CAPACITORS IN MICROFARADS
 3. ALL RESISTORS 1/4W ± 5%
 4. PWD ATTENUATES AS FOLLOWS WHEN DEPRESSSED:
 HI Z JACK USED: -50dBm
 HI Z JACK UNUSED: -55dBm

ITEM	PART NO.	DESCRIPTION	SIZE	QTY
1	741	OP-AMP		
2	742	OP-AMP		
3	743	OP-AMP		
4	RES	RESISTOR		
5	CAP	CAPACITOR		
6	PCB	PRINTED CIRCUIT BOARD		
7	WIRE	WIRE		
8	FLUX	FLUX		
9	WELD	WELD		
10	TEST	TEST POINT		
11	APP	APPLICATION		

BIAMP SYSTEMS INC.
 SCHEMATIC DIAGRAM
 4/19 INPUT ASSEMBLY

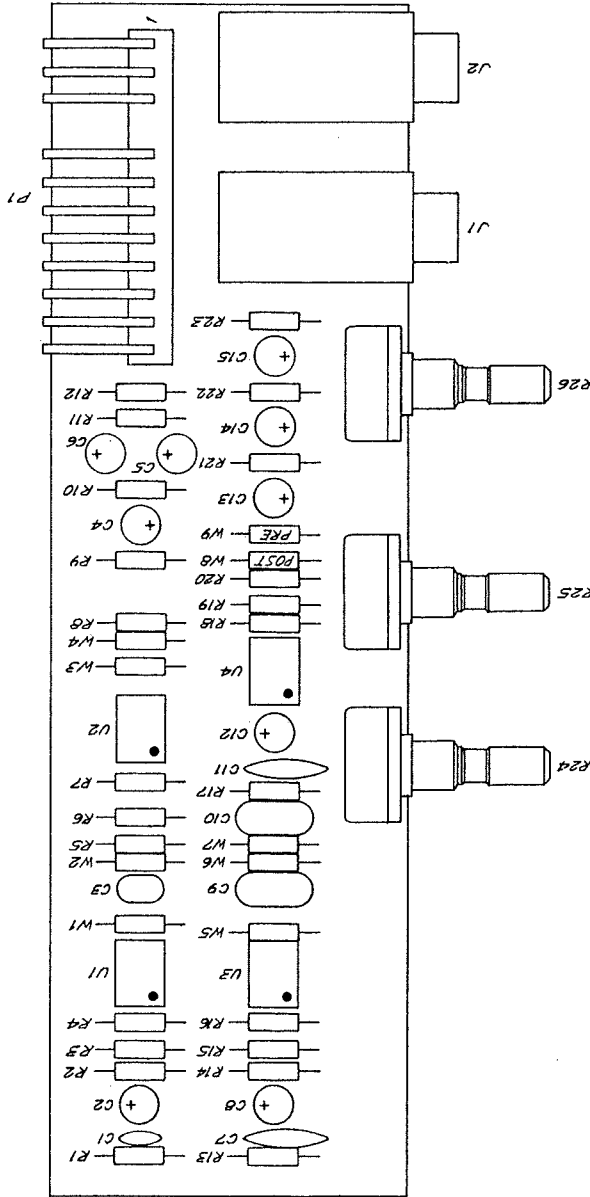
SCALE: 1/4" = 1"

DO NOT SCALE DRAWING

SHEET 1 OF 1

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- P1 PIN ASSIGNMENTS:**
1. EFFECTS BUSS
 2. MONITOR BUSS
 3. MAIN BUSS
 4. VOID
 5. SIGNAL GROUND
 6. POWER GROUND
 7. -15V
 8. +15V
 9. TAPE OUT
 10. MAIN OUT
 11. REVERB DRIVE
 12. REVERB DRIVE



REV.	E.C.D.	CHANGE	DATE	BY

ITEM	PART NO.	DATE	DESCRIPTION	SIZE	QTY.

DATE	BY	DESCRIPTION
3/12/82		
3/82		

DESIGN	APPROVED	DATE	BY

MATERIAL	FINISH	SCALE	DWG. NO.	REV.

BIAMP SYSTEMS INC.	ASSEMBLY 43, 619 MAIN PCB

MODEL	NEXT DWG.	APPLICATION	YES	NO

DO NOT SCALE DRAWING	SHEET 1 OF 1

A B C D

1

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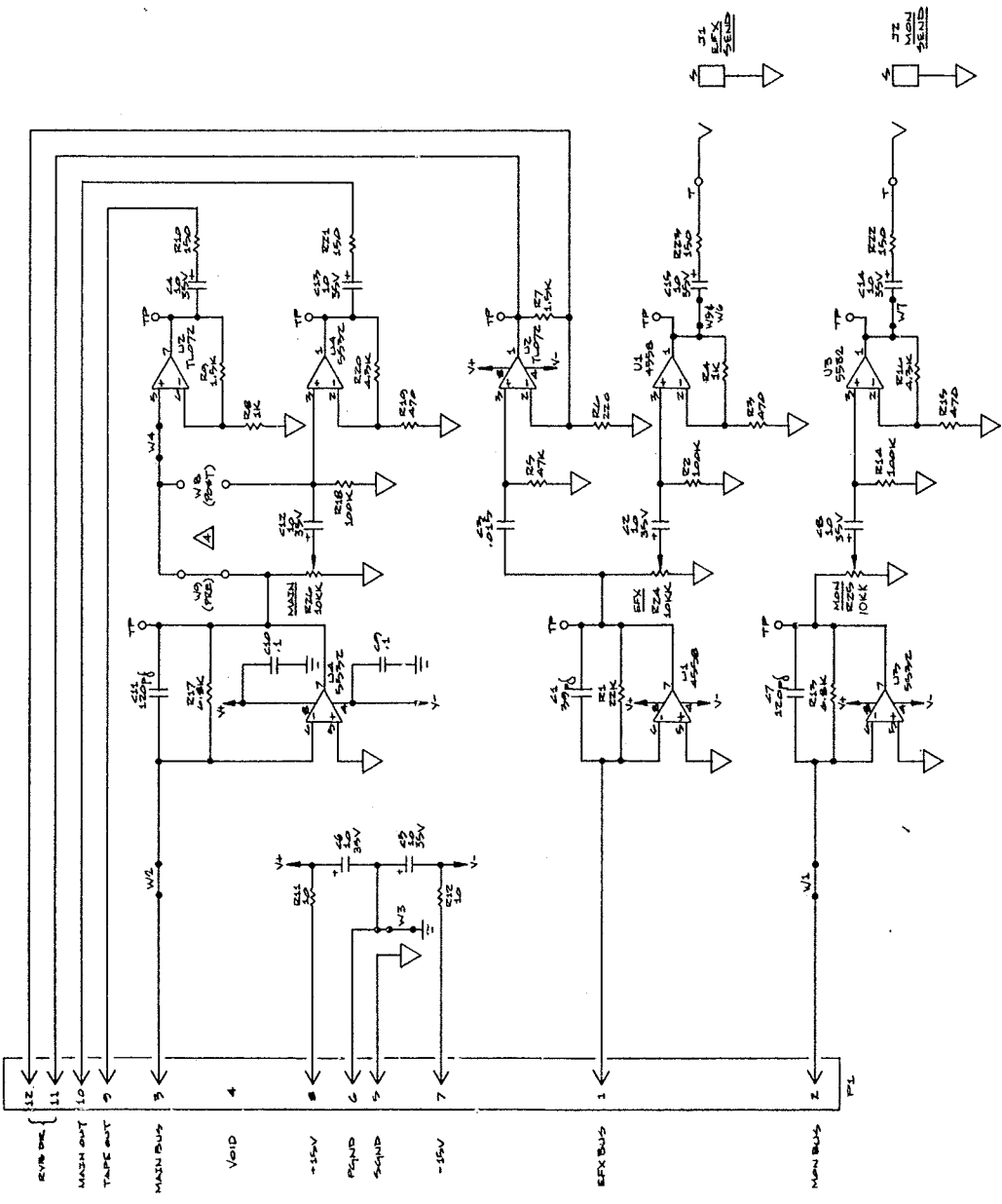
2

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3

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NOTES: UNLESS OTHERWISE SPECIFIED,
 1. ALL RESISTORS 1/4W, 5%/

2. ALL RESISTOR VALUES IN OHMS
 3. ALL CAPACITOR VALUES IN MICROSECONDS

W1 FACTORY-INSTALLED FOR PRE-MAIN-FADE TAPE OUT;
 TAPE OUT; FOR POST-MAIN-FADE TAPE OUT,
 REMOVE W1, INSTALL W2.

REV.	ECO.	CHANGE	DATE

ITEM	DESCRIPTION	QTY	UNIT

PART NO.	DESCRIPTION	QTY	UNIT

BIAMP SYSTEMS I	SCHEMATIC DIAGRAM

MODEL	REV. NO.	DATE	BY	CHKD.

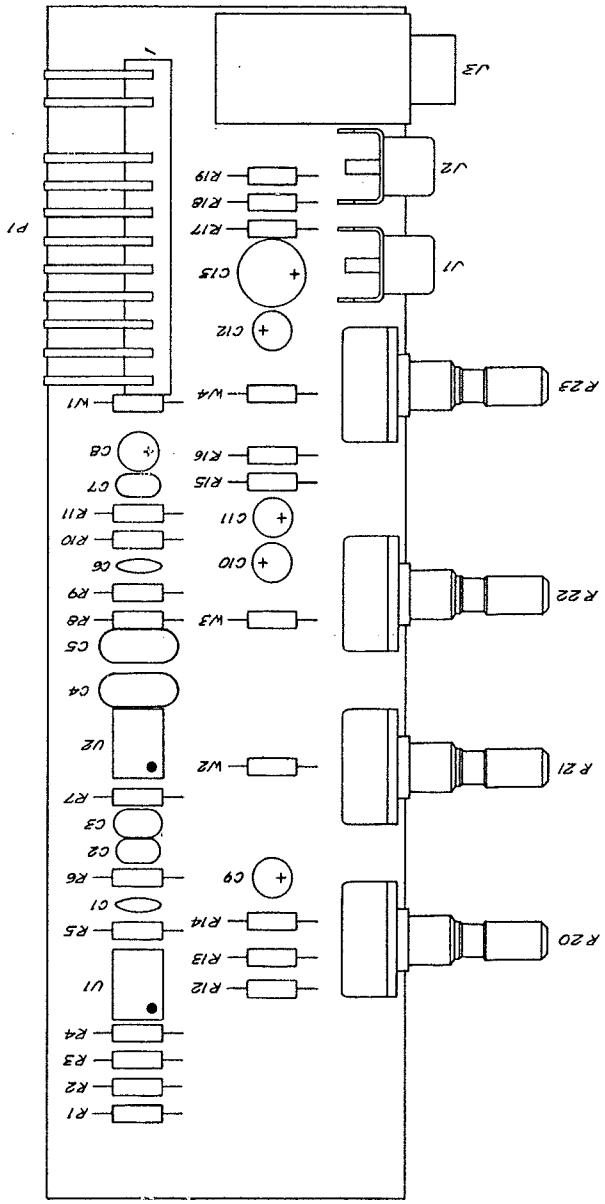
A B C D

REV. E.C.O. CHANGE DATE BY

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P1 PIN ASSIGNMENTS:

1. MONITOR
2. MAIN
3. PWD
4. SIGNAL GROUND
5. POWER GROUND
6. -15V
7. +5V
8. TAPE IN LEFT & RIGHT
9. REVERB FOOTSWITCH
10. REVERB PICK-UP +
11. REVERB PICK-UP -
12. REVERB PICK-UP -



ITEM	PART NO.	DESCRIPTION	SIZE	QTY.
BIAMP SYSTEMS INC.				
ASSEMBLY A2,619 AUX PCB				
DATE: 05/18/82	DRAWN: J.D.	ENGINEER		
CHECKED: J.D.	DESIGN			
SCALE: 2 X	SIZE: 6 1/2 x 1 1/2	REV. NO.:		
SCALE: 2 X	DO NOT SCALE DRAWING	SHEET 1 OF 1		

A B C D

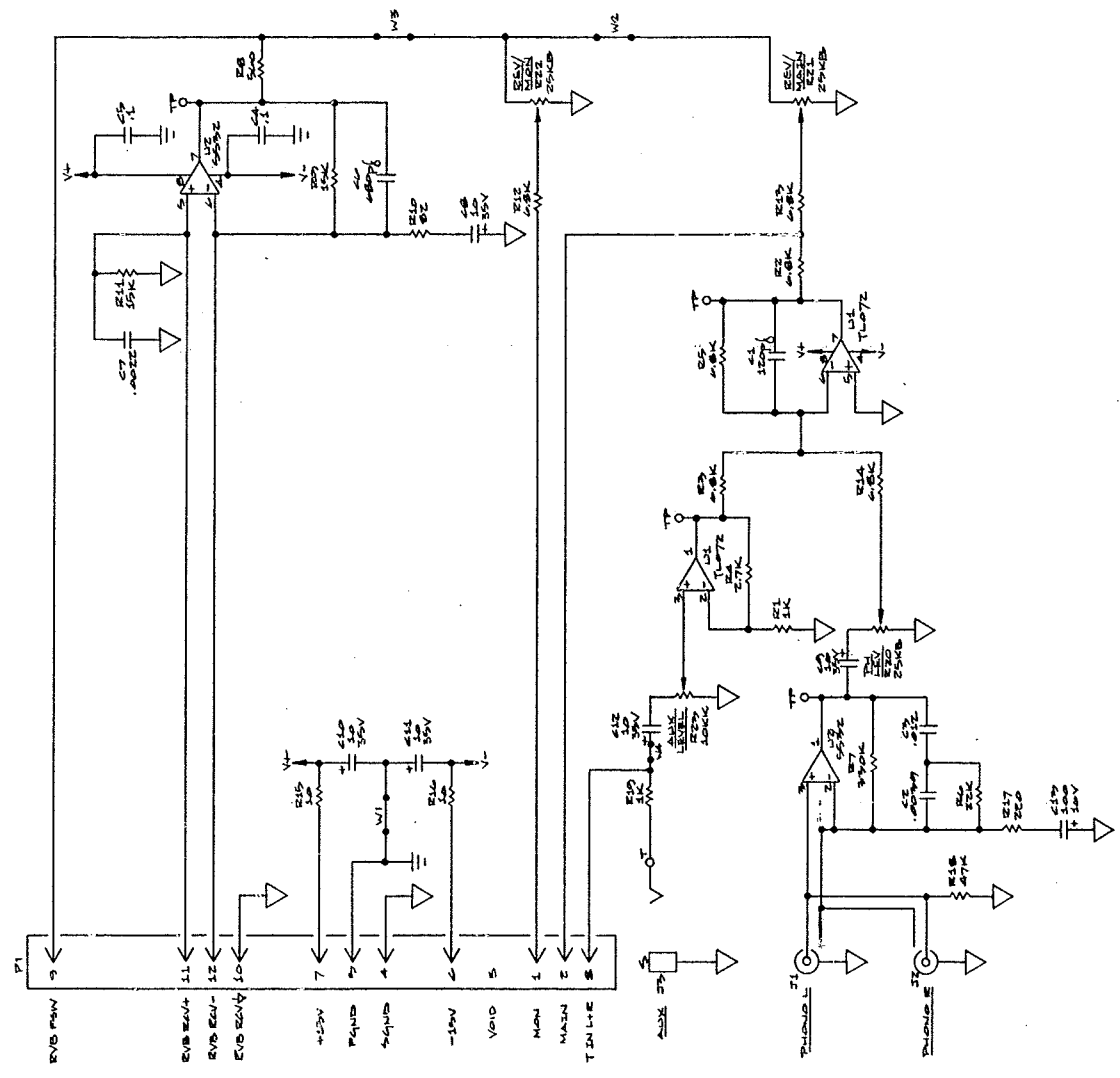
REV. A

SCALE 2 X

DO NOT SCALE DRAWING

SHEET 1 OF 1

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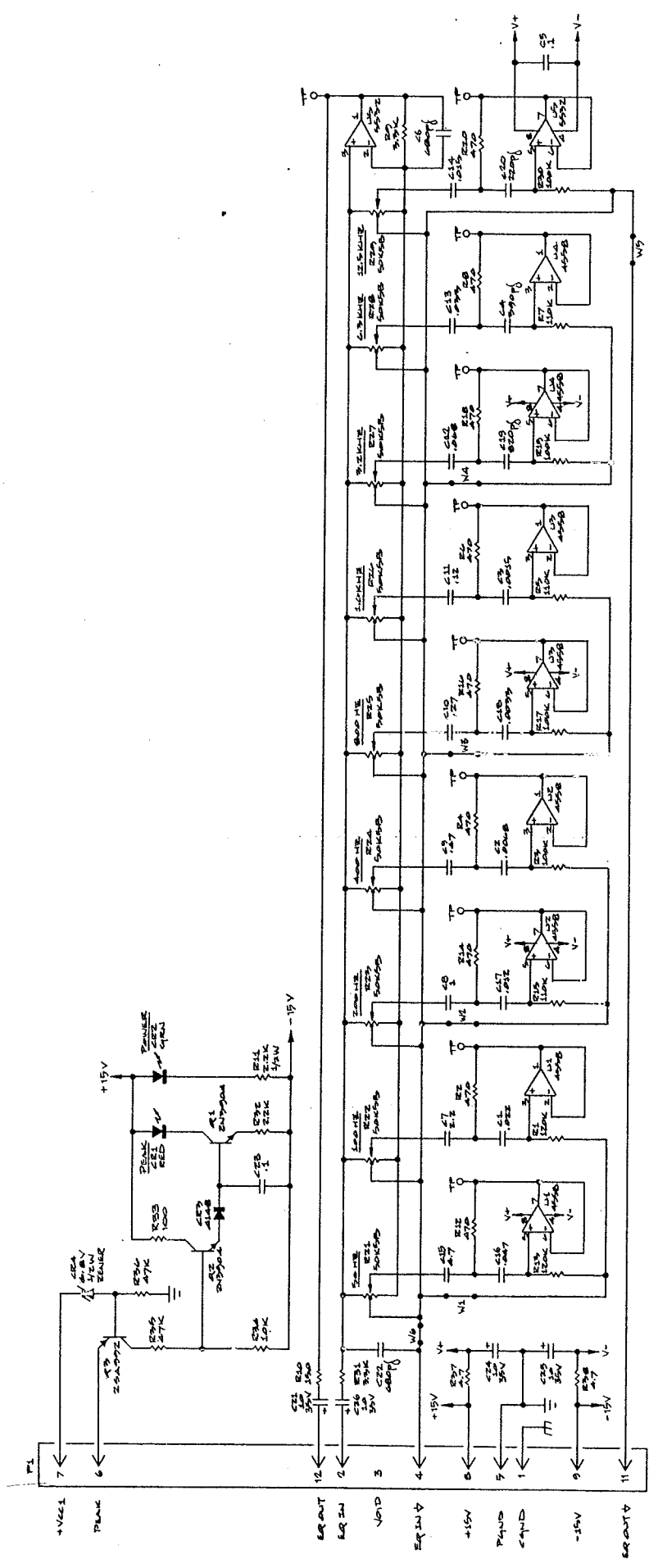
NOTES: UNLESS OTHERWISE SPECIFIED,
 1. ALL RESISTORS 1/4W, 5%
 2. ALL RESISTOR VALUES IN OHMS
 3. ALL CAPACITOR VALUES IN MICROFARADS

LAST 4
 LAST 3
 LAST 2
 LAST 1
 LAST 0
 LAST 9
 LAST 8
 LAST 7
 LAST 6
 LAST 5
 LAST 4
 LAST 3
 LAST 2
 LAST 1
 LAST 0

REV.	ECO.	CHANGED	DATE

ITEM	PART NO.	DESCRIPTION	QTY	UNIT
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BIAMP SY
 SCHEDULE 20A
 2/10/82
 SCALE 1/16" = 1"



NOTES: UNLESS OTHERWISE SPECIFIED,
 1. ALL RESISTORS 1/4W, 50PPM
 2. ALL RESISTOR VALUES IN OHMS
 3. ALL CAPACITOR VALUES IN MICROSECONDS

LAST 2
 LAST 4
 LAST 6
 LAST 8
 LAST 10
 LAST 12
 LAST 14
 LAST 16

REV.	DATE	DESCRIPTION
1	2/10/82	BIAMP SY
2	2/10/82	SCHEDULE 20A
3	2/10/82	2/10/82
4	2/10/82	2/10/82
5	2/10/82	2/10/82
6	2/10/82	2/10/82
7	2/10/82	2/10/82
8	2/10/82	2/10/82
9	2/10/82	2/10/82
10	2/10/82	2/10/82

REV.	EGG.	CHANGE	DATE	BY
9	DB6-B2	REMOVE R41 ADD NOT USED	6-82	JD

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C

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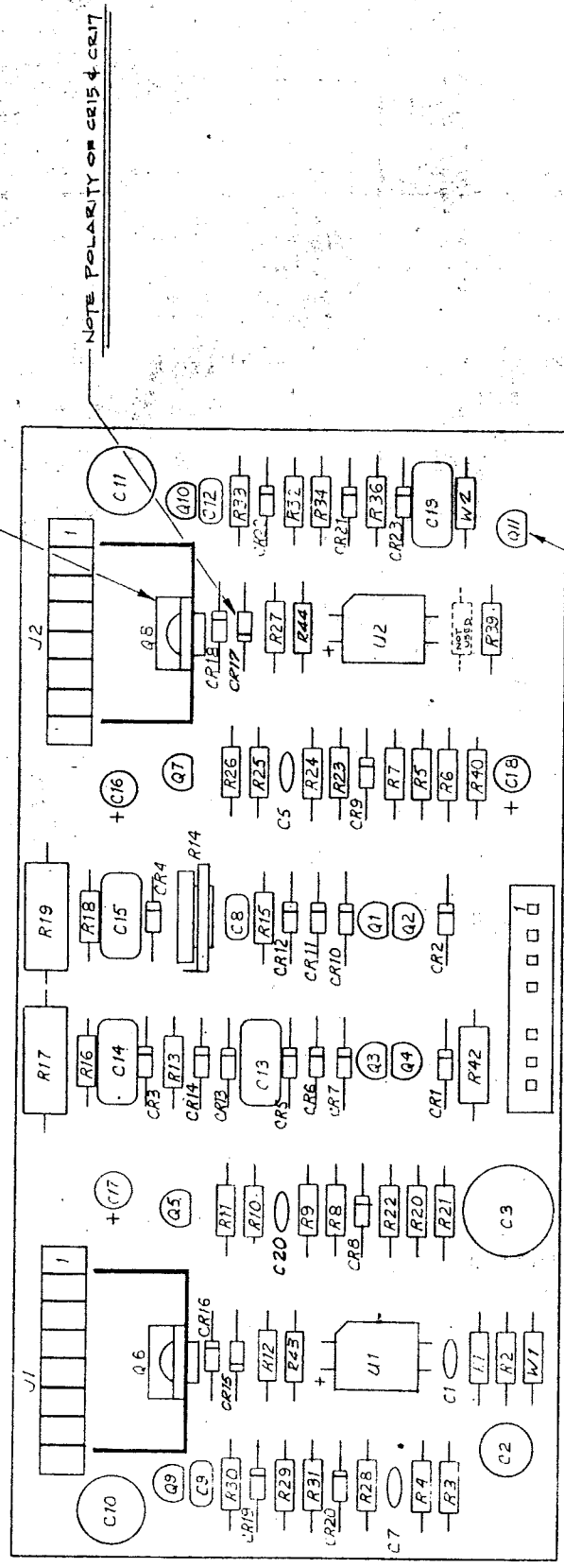
1

J1 PIN ASSIGNMENTS

1. OUTPUT
2. THERMAL RESISTOR - TS
3. THERMAL RESISTOR - T
4. +Vcc 1
5. +Vcc 2
6. +Vcc 3
7. +Vcc 4
8. +Vcc 5

J2 PIN ASSIGNMENTS

1. GROUND
2. -Vcc 1
3. -Vcc 2
4. -Vcc 3
5. OUTPUT
6. -VI SENSE
7. -DRIVE / BIAS
8. BIAS



J3 PIN ASSIGNMENTS

1. FILTERED LED CONTROL VOLTAGE
2. LED REFERENCE GROUND
3. FAST OFF CONTROL
4. +Vcc 1 LED REFERENCE VOLTAGE
5. +Vcc 2 LED REFERENCE VOLTAGE
6. +PE INPUT
7. INPUT GROUND
8. SIGNAL INPUT

NOTE:
 1. ALL COMPONENTS TO BE FULLY SEATED
 2. DOWN ON BOARD EXCEPT AS NOTED.
 3. SEE SHEET 1 FOR SCHEMATIC.

ITEM	PART NO.	DESCRIPTION	SIZE	QTY.
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES ARE DECIMALS. FRACTIONS ARE IN 16ths.	DATE: 8/28/81	BIAMP SYSTEMS INC.		
CHECKED: TP	ENGINEER: TP	ASSEMBLY #11		
DESIGN: [Signature]	DATE: 7/1/81	19 SERIES DRIVER BOARD		
FINISH: 227, 1229	SCALE: 2:1	DWG. NO. 701-0063-00		SHEET 2 OF 2
MODEL: [Blank]	SCALE: 2:1	DO NOT SCALE DRAWING		

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REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...

REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...

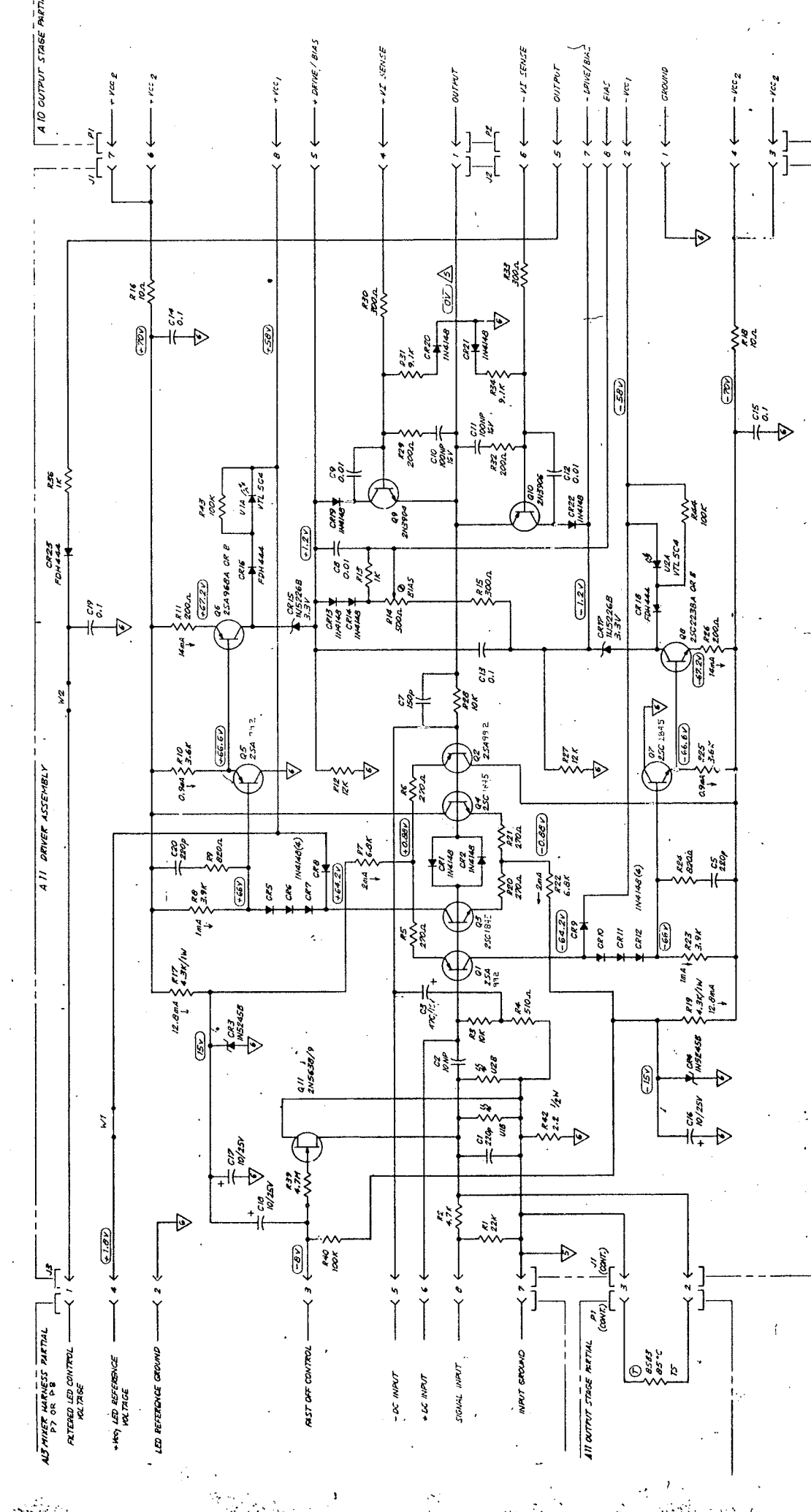
REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...

REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...

REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...

REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...

REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...



1. ALL CAPACTORS IN µM UNLESS NOTED.

2. ALL RESISTORS ARE 1/4W, 5% UNLESS NOTED.

3. CR7 IS 15-100V 1000PF 1%.

4. SEE SHEET FOR PCB ASSEMBLY.

5. MAX VOLTAGE VARIATION CAN BE ±50%VDC.

6. LINE VOLTAGE = 120VAC.

7. MAX VOLTAGE VARIATION CAN BE ±50%VDC.

8. CR1-CR4 MUST BE ASSIGNED TO SPECIFIC PAIRS.

9. ALL VOLTAGES ARE DC AND MEASURED WITH NO SIGNAL.

LAST R: 844 OMIT R41, 55, 57, 436

- C1, C2, C3
- R1, R2, R3
- U1, U2
- J1, J2

REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...

REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...

REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...

REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...

REV.	ECO	CHANGE
3	37584	...
2	37584	...
1	37584	...

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P1 PIN ASSIGNMENTS

1. OUTPUT
2. THERMAL RESISTOR - T
3. THERMAL RESISTOR - T
4. +VI SENSE
5. +VE DRIVE/BIAS
6. +VCC 2
7. +VCC 1
8. -VCC 1

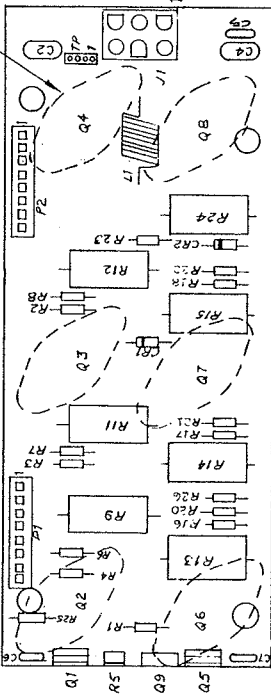
P2 PIN ASSIGNMENTS

1. GROUND
2. -VCC 1
3. -VCC 2
4. -VCC 2
5. OUTPUT
6. -VI SENSE
7. -VE DRIVE/BIAS
8. BIAS

HAND ADD SOCKETS ON BACK OF BOARD AT TIME OF AMP MODULE ASSEMBLY.

J1 PIN ASSIGNMENTS

1. -VCC 2
2. AMP GROUND
3. +VCC 2
4. -VCC 1
5. AMP OUT
6. +VCC 1



2. ALL COMPONENT TO BE FULLY SEATED DOWN ON BOARD.
 1. SEE SHEET 1 FOR SCHEMATIC.
- NOTE :

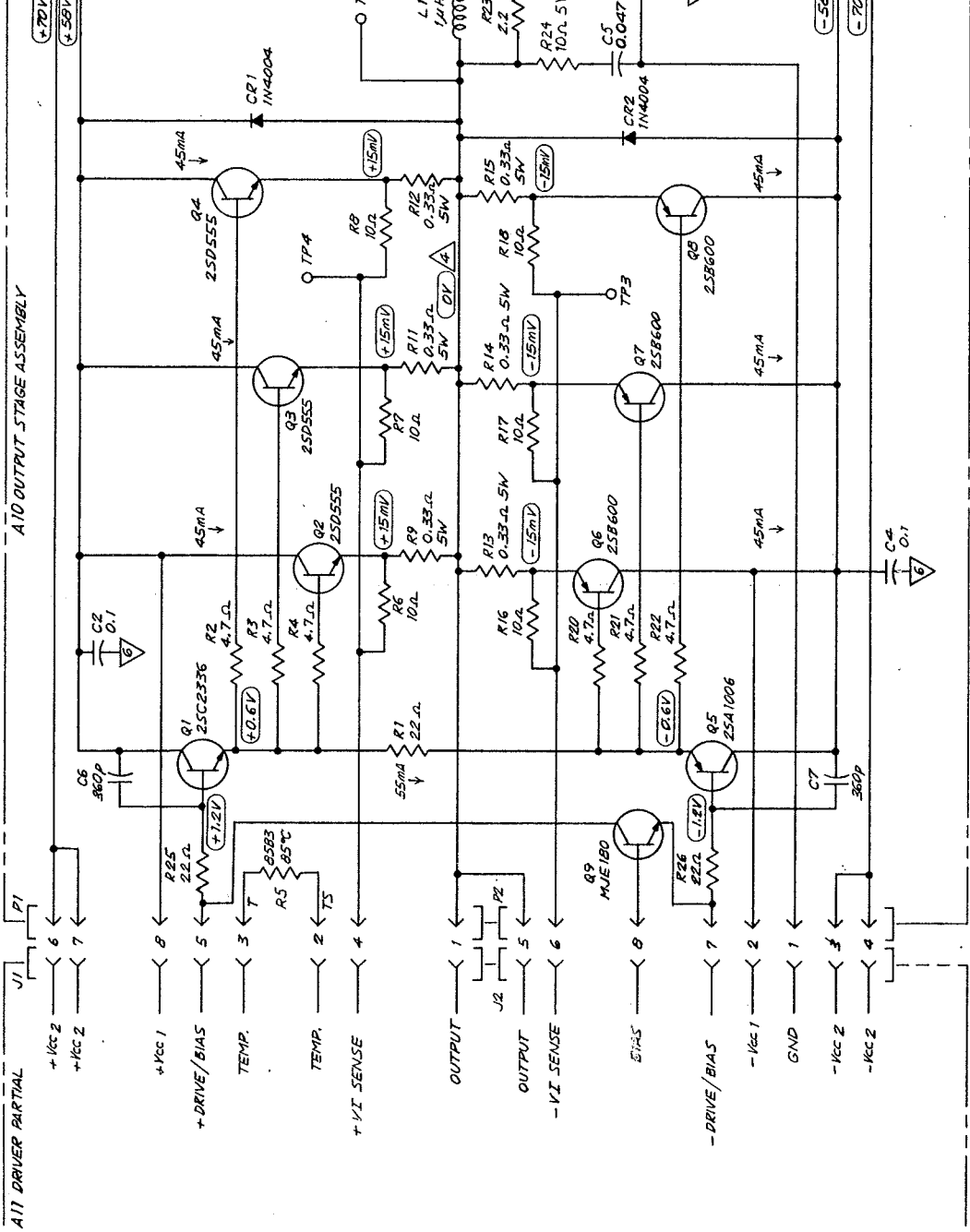
REV.	E.C.O.	CHANGE	DATE	BY
B		REMOVED C1 & C2 (D.I.P)	4/82	NL
C	250-82	RLU R20 R17 R21 R18 R22	6/82	FD

DATE	PART NO.	DESCRIPTION	SIZE	QTY.
8/24/81		BIAMP SYSTEMS INC.		
11-21-81		ASSEMBLY A 10		
		29 SERIES OUTPUT STAGE BOARD		
DESIGN	ENGINEER			
APPROVED				
DATE				
FINISH				
880 1229				
SCALE				
DO NOT SCALE DRAWING				
SHEET 2 OF 2				

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A11 DRIVER PARTIAL A10 OUTPUT STAGE ASSEMBLY A14 AMP HARNESS PARTIAL

REV. B
E.C.D.
CHANGE C.1 & C.3 (0.1MFD) ADD TP 4DATE 4/82
BY JL



- LAST R: R26
- C: C7
- CR: CR2
- Q: Q9
- L: L1
- J: J1
- P: P2

5. ALL VOLTAGES ARE DC AND MEASURED WITH NO SIGNAL; LINE VOLTAGE = 120 VAC.
4. MAX. VOLTAGE VARIATION CAN BE ±50% VDC.
3. SEE SHEET 2 FOR PCB ASSEMBLY.
2. ALL RESISTORS ARE 1/4 W, 5% UNLESS NOTED.
1. ALL CAPACITORS IN μFD UNLESS NOTED.

NOTES:

ITEM	DESCRIPTION	SIZE	QTY.
UNLESS OTHERWISE SPECIFIED, DIMENSIONS SHALL BE IN INCHES AND DECIMALS FRACTIONS UNLESS OTHERWISE SPECIFIED.			
DRYING	7 (100)		
CHECKED	TP 4		
ENGINEER			
DESIGN			
APPROVED			
DATE	10/27/82		
SCALE	1/2" = 1"		
DWG. NO.			
REV.			
MATERIAL			
FINISH			
MODEL			
HEAT DWN.			
APPLICATION			
YES			
NO			
DESCRIPTION	BIAMP SYSTEMS INC.		
SCHEMATIC - ASSEMBLY A10	29 SERIES OUTPUT STAGE BOARD		
DO NOT SCALE DRAWING	SHEET 7 OF 3		

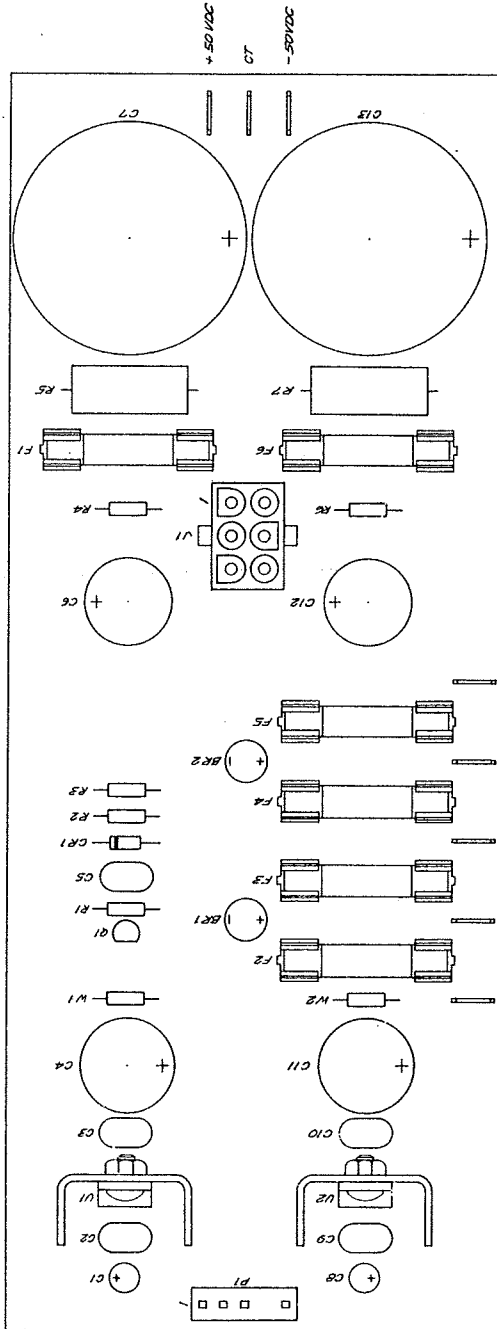
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P1 PIN ASSIGNMENTS:

1. FAST OFF
2. -15V
3. POWER GROUND
4. PWD
5. +15V

V1 PIN ASSIGNMENTS:

1. AMP GROUND
2. -VCC 1
3. -VCC 2
4. SPEAKER GROUND
5. +VCC 1
6. +VCC 2

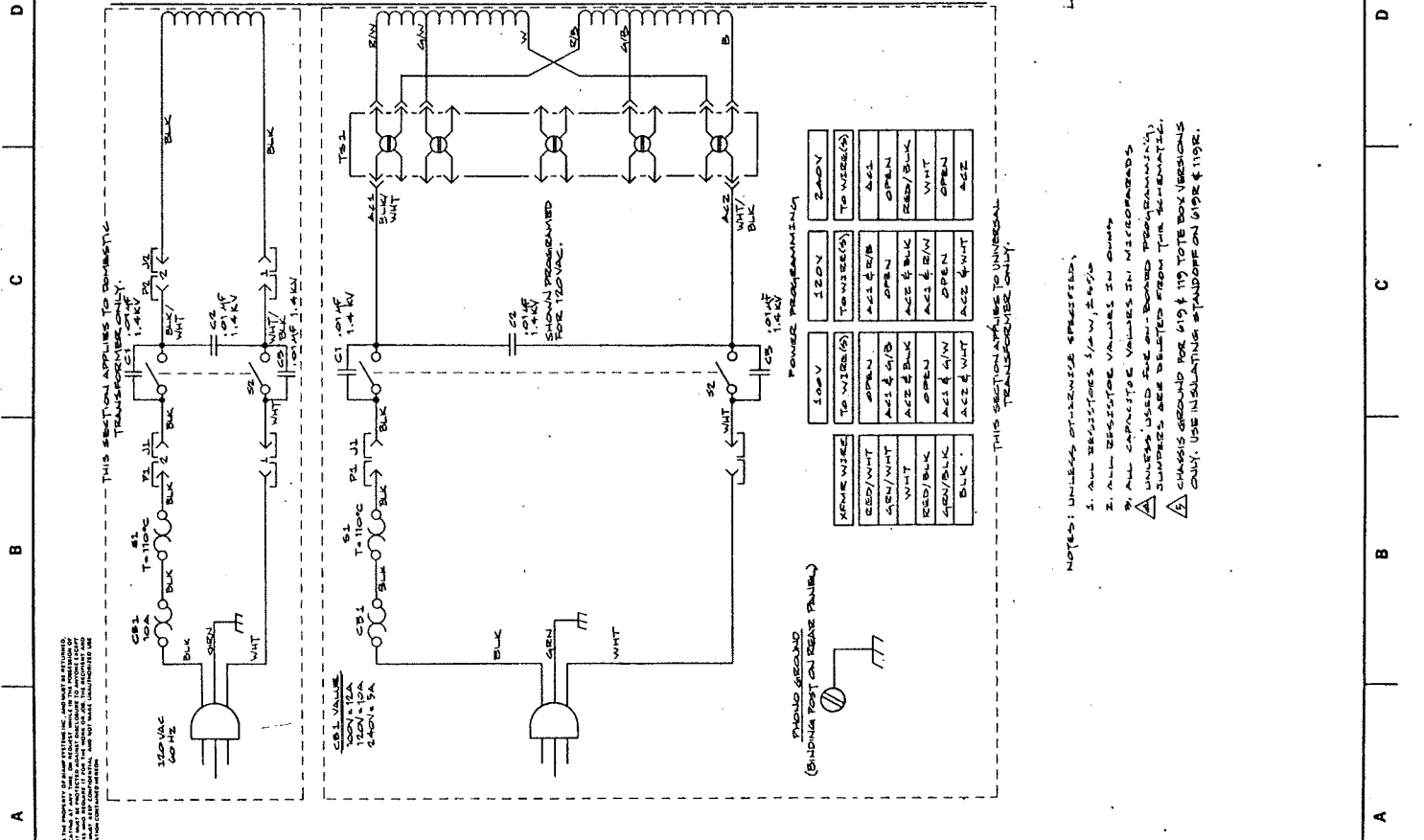
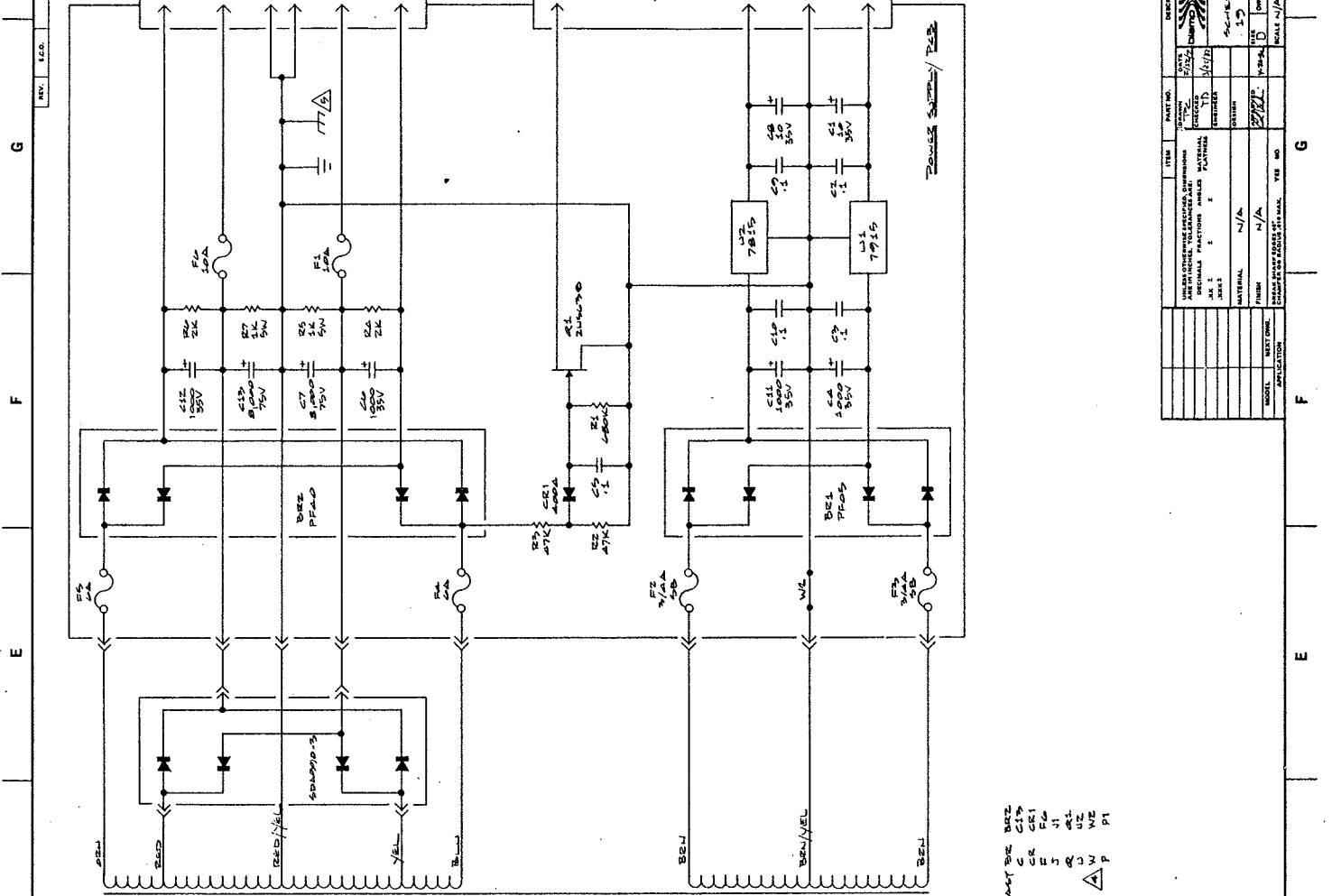


B C D E F G H

REV. E.C.D. CHANGE DATE BY

ITEM	QTY.	DESCRIPTION	SIZE	QTY.
BIAMP SYSTEMS INC.				
ASSEMBLY A 9, 19 POWER SUPPLY				
DATE	REV.	BY	DATE	BY
1971	1	JLD		
DESIGNED	CHECKED	DATE	BY	
MATERIAL				
FINISH				
TEST QTY.				
APPLICATION				
DO NOT SCALE DRAWING				
SHEET / OF 7				

B C D E F G H



- LAST BY BRZ
 C CRP
 E ELI
 S JI
 Q RI
 U WZ
 A Y
 P

NOTES: UNLESS OTHERWISE SPECIFIED,
 1. ALL RESISTORS 1/4 W, 5%
 2. ALL CAPACITORS VALUES IN MICROFARADS
 UNLESS USED FOR AN-BOARD PROGRAMMING,
 CAPACITORS ARE DELTA FROM THIS SCHEMATIC.
 CHASSIS GROUND FOR U19 & U20 TOTE BOX VERSIONS
 ONLY. USE INSULATING STANDOFF ON U19 & U20.

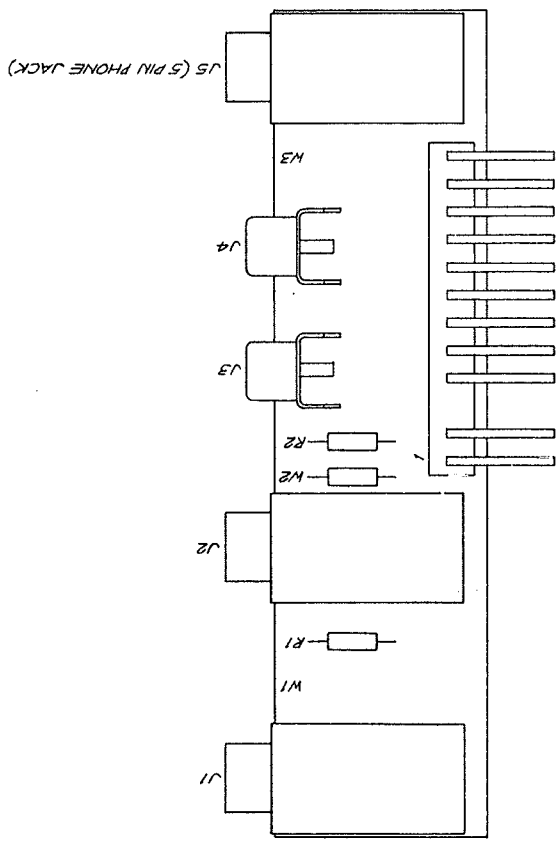
ITEM	PART NO.	DESCRIPTION	QTY
U1	7815	REGULATOR	1
U2	7915	REGULATOR	1
U3	7815	REGULATOR	1
U4	7915	REGULATOR	1
U5	7815	REGULATOR	1
U6	7915	REGULATOR	1
U7	7815	REGULATOR	1
U8	7915	REGULATOR	1
U9	7815	REGULATOR	1
U10	7915	REGULATOR	1

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1 1 2 3 4

A B C D

REV. E.C.D. CHANGE DATE BY

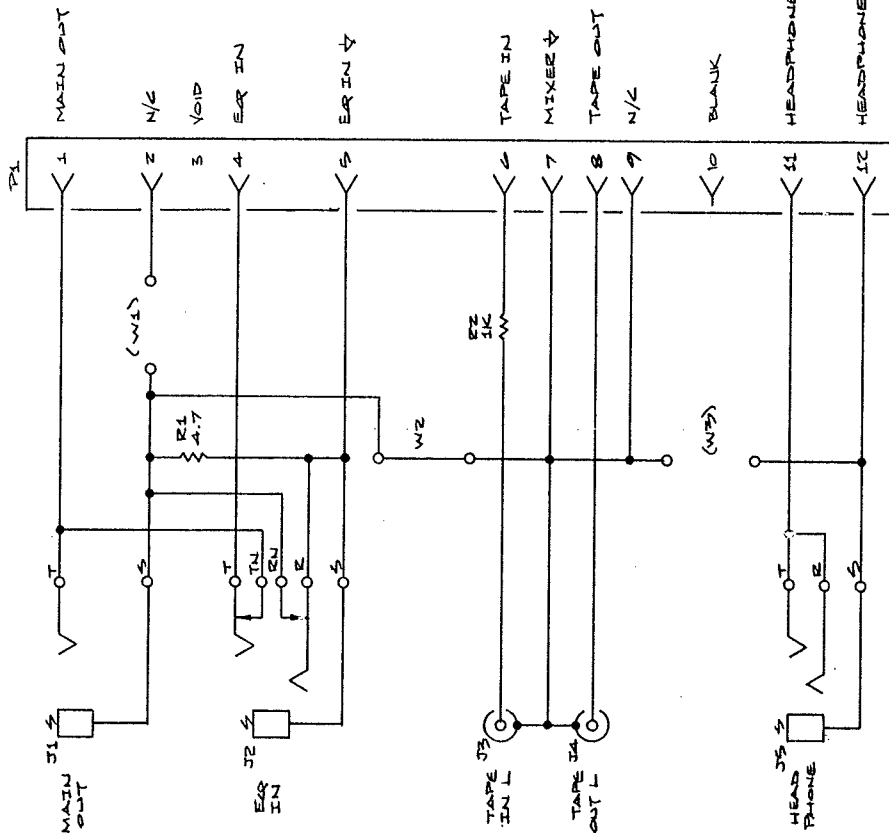


- P1 PIN ASSIGNMENTS:
1. MAIN OUT
 2. BLANK
 3. VOID
 4. ER IN
 5. ER IN GROUND
 6. TAPE IN
 7. MIXER GROUND
 8. TAPE OUT
 9. BLANK
 10. BLANK
 11. HEADPHONE OUT
 12. HEADPHONE GROUND

ITEM	PART NO.	DESCRIPTION	SIZE	QTY.
BIAMP SYSTEMS INC.				
<i>ASSEMBLY A-1, 619 JACK PCB, UPPER</i>				
DATE	5/24/70	SIZE	C	
CHECKED	SD	ENGINEER	REV. A	
DESIGN	SD	SCALE	DO NOT SCALE DRAWING SHEET 1 OF 1	
MATERIAL		FINISH		
BREAK SHARP EDGES AT RADIUS .015 MAX.				
MODEL		APP. NO.		

A B C D 1 2 3 4

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NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTORS $\frac{1}{4}W, \pm 5\%$
2. ALL RESISTOR VALUES IN OHMS

LAST J SS
LAST P P1
LAST R R2
LAST W W3

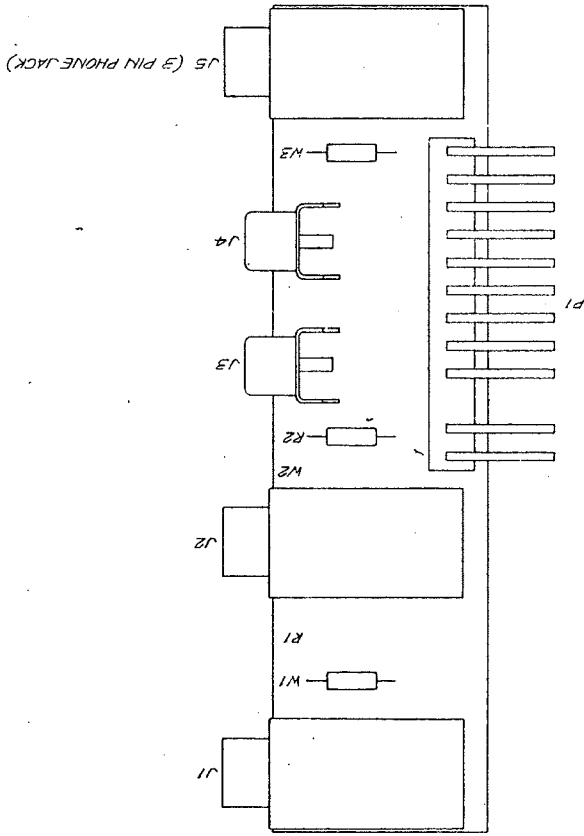
REV.	E.C.O.	CHANGE	DATE	BY
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DATE	PART NO.	DESCRIPTION	SIZE	QTY.
7/2/72		BIAMP SYSTEMS INC.		
7/2/72		SCHEMATIC DRAWING		
		5/19 UPPER DUB ASSY A4		
		REV. A		
		DWG. NO.		
		SCALE N/A		
		DO NOT SCALE DRAWING		
		SHEET 1 OF 1		

BIAMP SYSTEMS INC.

SCHEMATIC DRAWING
5/19 UPPER DUB ASSY A4
REV. A
DWG. NO.
SCALE N/A
DO NOT SCALE DRAWING
SHEET 1 OF 1

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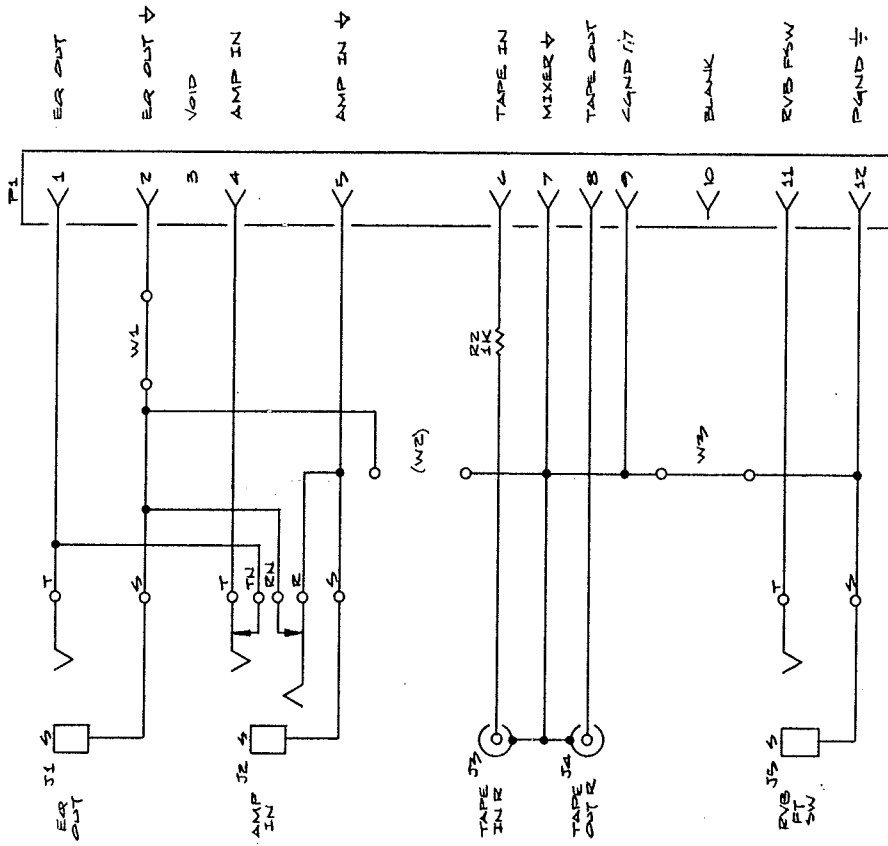
P1 PIN ASSIGNMENTS:

1. ER OUT
2. ER OUT GROUND
3. VOID
4. AMP IN
5. AMP IN GROUND
6. TAPE IN
7. MIXER GROUND
8. TAPE OUT
9. CHASSIS GROUND
10. BLANK
11. REVERB FOOTSWITCH
12. POWER GROUND

REV.	E.C.D.	CHANGE	DATE	BY

PART NO.		DESCRIPTION		SIZE	QTY.
DRAWN <input checked="" type="checkbox"/>	DATE 3-24-82	BIAMP SYSTEMS INC.			
CHECKED <input checked="" type="checkbox"/>	JD	ASSEMBLY A5, #19 JACK PCB, LOWER			
ENGINEER	DESIGN	USE	DWG. NO.	SCALE	REV. A
		4-1/2" x 10"	()	ZX	1 / 1
		MATERIAL	FINISH	DO NOT SCALE DRAWING	
MODEL	NEXT DWG.	BREAK SHARP CORNERS AT 90 DEGS.	YES		
		APPLICATION			

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NOTES: UNLESS OTHERWISE SPECIFIED,
 1. ALL RESISTORS 1/4 W, ±5%
 2. ALL RESISTOR VALUES IN OHMS

LAST J JS
 LAST P PI
 LAST R RZ
 LAST W W3

REV.	E.C.O.	CHANGE	DATE	BY

ITEM	PART NO.	DESCRIPTION	SIZE	QTY.

DATE	BY	CHECKED	ENGINEER	DESIGN
2/19/72	JJ	JD		

DESCRIPTION	DATE	BY	REV.
BIAMP SYSTEMS INC.	2/19/72	JJ	1

SCALE	N/A	DO NOT SCALE DRAWING	SHEET 1 OF 1

A B C D

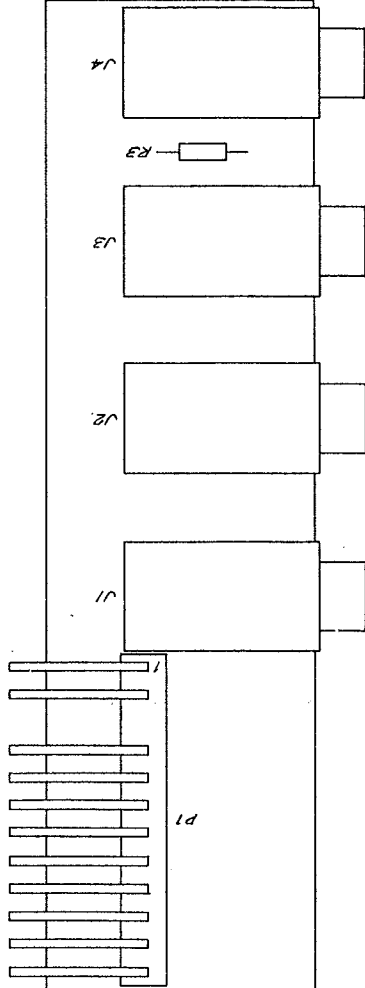
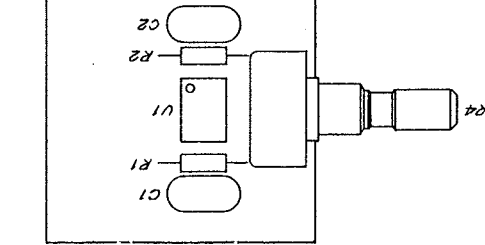
1 2 3 4

1 2 3 4

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P1 PIN ASSIGNMENTS:

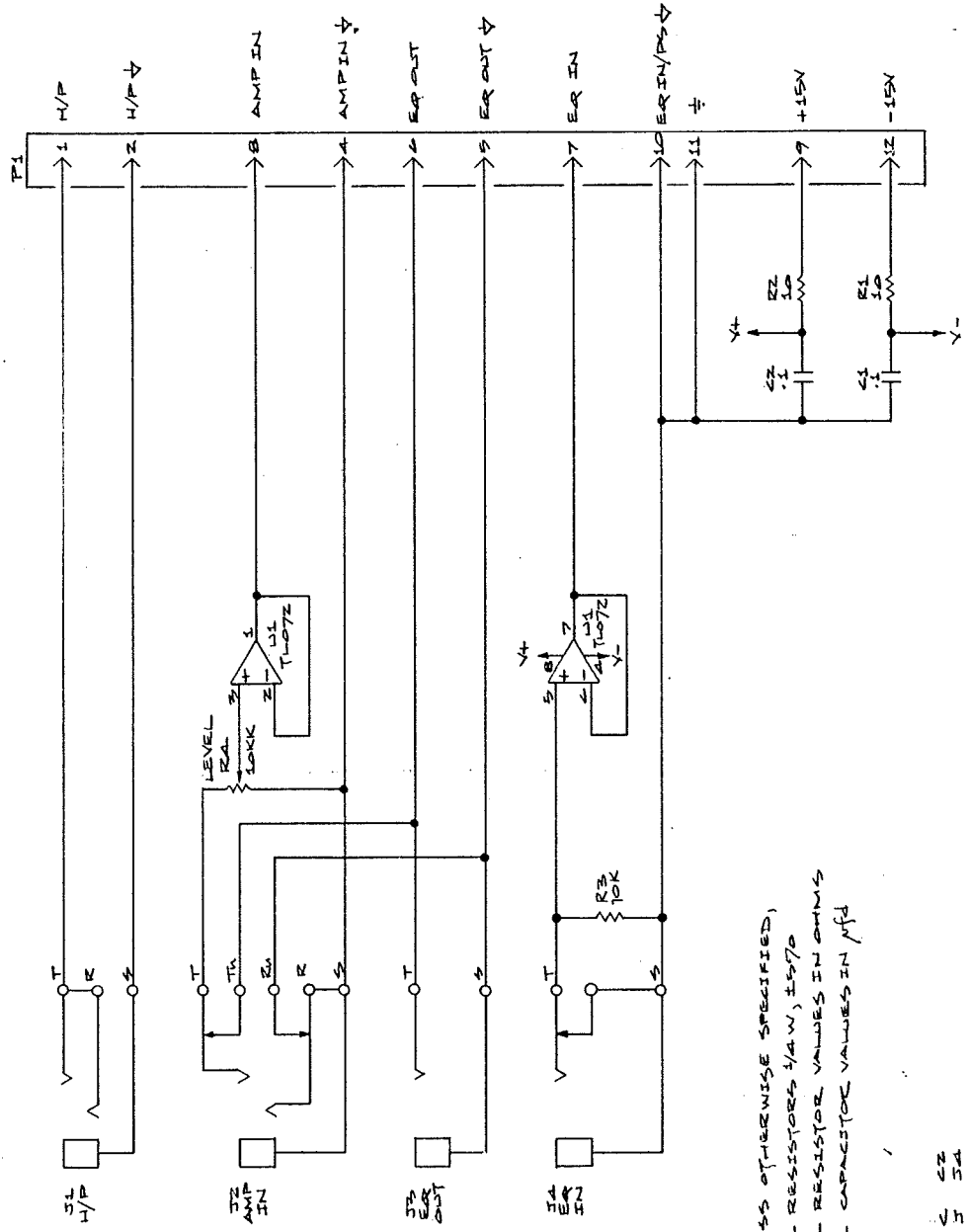
1. HEADPHONE
2. HEADPHONE GROUND
3. VOID
4. AMP IN GROUND
5. EQ OUT GROUND
6. EQ OUT
7. EQ IN
8. AMP IN
9. +15V
10. EQ IN/POWER SUPPLY GROUND
11. CHASSIS GROUND
12. -15V



REV.	E.C.D.	CHANGE	DATE	BY

DATE 5/4/72 5-11-72		PART NO. DRAWN CHECKED ENGINEER DESIGN	DESCRIPTION BIAMP SYSTEMS INC. ASSEMBLY A1, 119 JACK PC BOARD	SIZE 5/4" x 2" C	QTY. 2X
DIMENSIONS ARE IN INCHES, TOLERANCES ARE DECIMALS FRACTIONS ANGLES	MATERIAL .1005	FINISH NEXT DWG. APPLICATION	DWG. NO. SCALE	SHEET 1 OF 7	10

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NOTES: UNLESS OTHERWISE SPECIFIED,
 1. ALL RESISTORS 1/4W, 5%
 2. ALL RESISTOR VALUES IN OHMS
 3. ALL CAPACITOR VALUES IN μ F

LAST C
 LAST J
 LAST P
 LAST R
 LAST W

A B C D

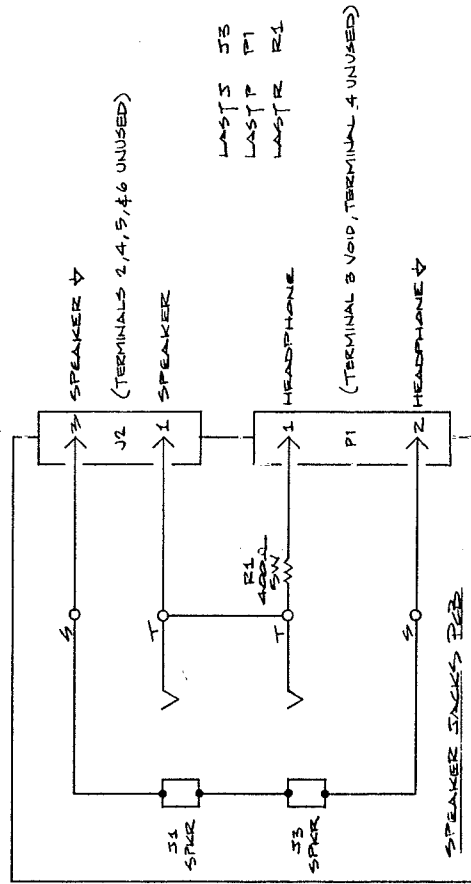
REV. EGO. DATE CHANGE BY

PART NO.		DESCRIPTION		QTY.	
DATE	7/2/72	BIAMP SYSTEMS INC.	BIAMP SYSTEMS INC.		
DRAWN	TD	CHECKED	TD		
ENGINEER		DESIGN			
MATERIAL	N/A	FINISH	N/A		
MODEL		APPLICATOR			
SCALE	N/A	SCALE	N/A		
REV.	A	DO NOT SCALE DRAWING			
SHEET	1 OF 1				

A B C D

REV. EGO. DATE CHANGE BY

THIS DRAWING IS THE PROPERTY OF BIAMP SYSTEMS INC., AND MUST BE RETURNED, WITHOUT DUPLICATION AT ANY TIME, ON REQUEST, WHILE IN THE POSSESSION OF THOSE EMPLOYEES WHO REQUIRE IT FOR THE WORK OR JOB. THE RECIPIENT AND USER SHALL BE RESPONSIBLE FOR THE PROTECTION AND NOT MAKE UNAUTHORIZED USE OF THE INFORMATION CONTAINED HEREON.



REV.	E.C.D.	CHANGE	DATE	BY

ITEM	PART NO.	DESCRIPTION	SIZE	QTY.
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES, TOLERANCES ARE DECIMALS FRACTIONS ANGLES <td></td> <td></td> <td></td> <td></td>				
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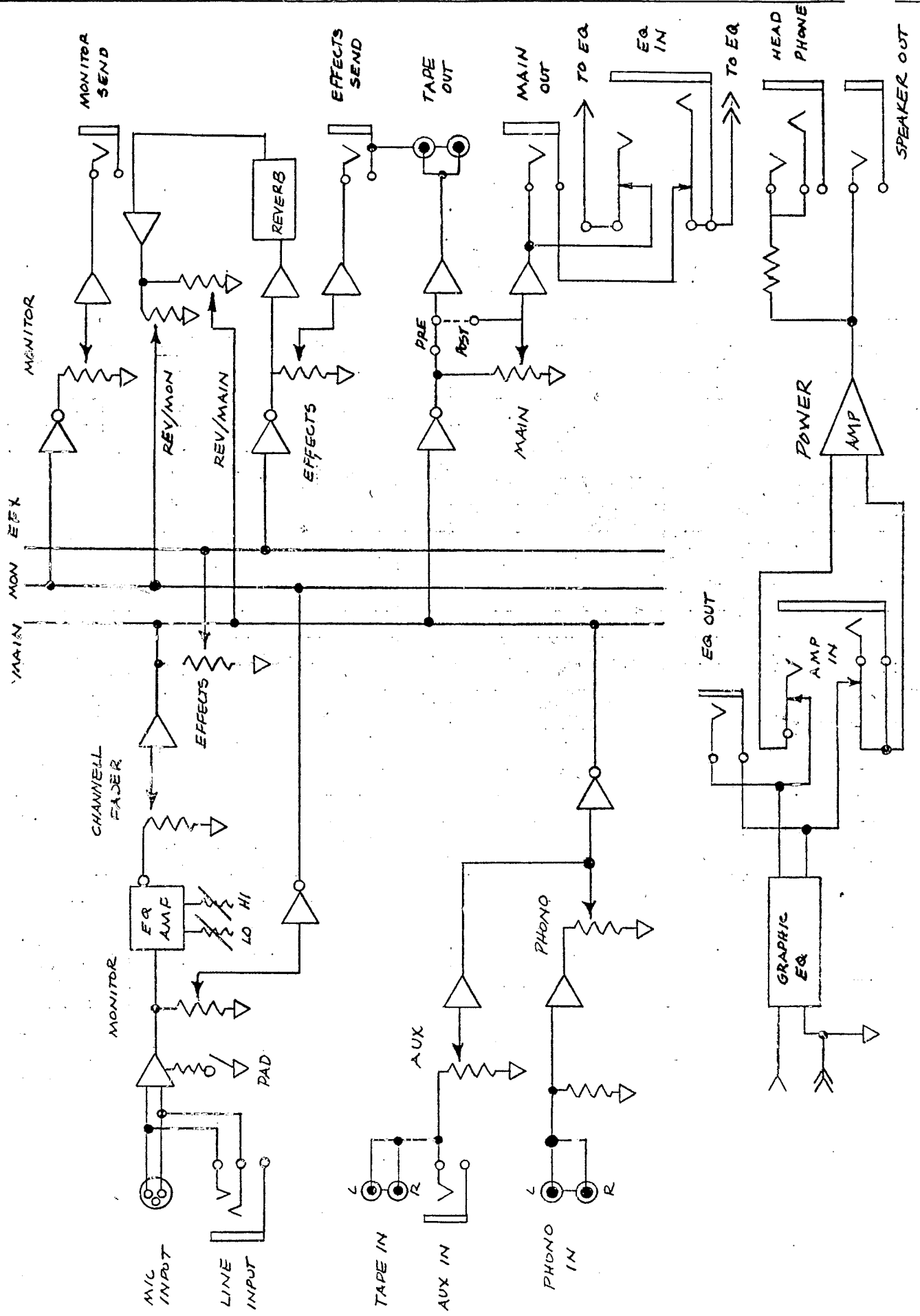
BIAMP SYSTEMS INC.
 SCHEMATIC DIAGRAM
 19 SPEAKER STACKS ASSY/A20

DATE: 7/25/72
 DRAWN BY: TD
 CHECKED BY: TD
 ENGINEER: TD
 DESIGN: TD
 UCC: #248
 C
 SCALE: N/A
 DO NOT SCALE DRAWING
 SHEET 1 OF 1

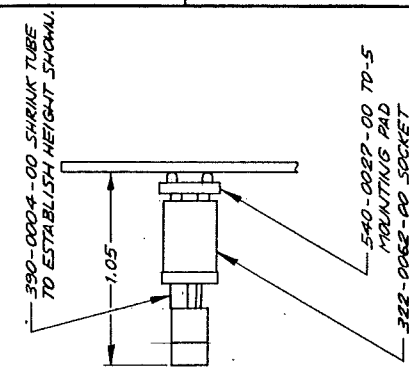
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES, TOLERANCES ARE DECIMALS FRACTIONS ANGLES
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 J&K 99
 J&K 100

MODEL: N/A
 FINISH: N/A
 ENCLOSURE FOR ROOMS 81'S MAX.
 YES NO
 APPLICATION: N/A
 SCALE: N/A
 DO NOT SCALE DRAWING
 SHEET 1 OF 1

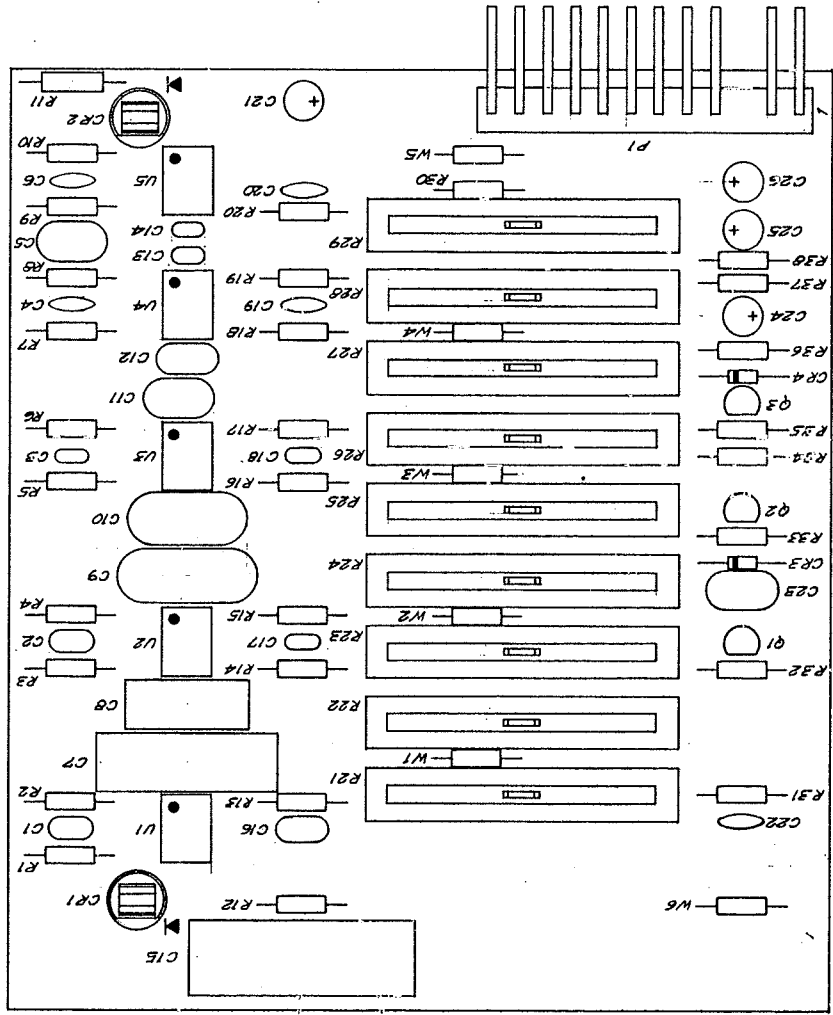
01



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- PI PIN ASSIGNMENTS:
1. CHASSIS GROUND
 2. ER IN
 3. VOID
 4. ER IN GROUND
 5. POWER GROUND
 6. PEAK
 7. +VCC 1
 8. +15V
 9. -15V
 10. BLANK
 11. ER OUT GROUND
 12. ER OUT



ITEM	PART NO.	DESCRIPTION	SIZE	QTY.
1	390-0004-00	SHRINK TUBE TO ESTABLISH HEIGHT SHOWAL		
2	540-0022P-00	TD-5 MOUNTING PAD		
3	322-0062-00	SOCKET		
BIAMP SYSTEMS INC.				
ASSEMBLY 46, 619 GRAPHIC EQ				
DRAWN: J.L. 7/10/82		DESIGNED: J.D. 5-21-82	DATE: 7-23-82	REV: A
CHECKED: J.D. 5-21-82		DESIGNED: J.D. 5-21-82	DATE: 7-23-82	REV: A
ENGINEER: J.D. 5-21-82		DESIGNED: J.D. 5-21-82	DATE: 7-23-82	REV: A
FINISH: 7-23-82		MODEL: 46	APPLICATOR: J.D.	SCALE: 2X
BREAK PARTS RADIUS .015 MAX.		YES: NO	DO NOT SCALE DRAWING	
SHEET / OF 7		7		