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Troubleshooting Guide
3.2.1 Home Entertainment System
3.2.1 GS Home Entertainment System

(US/Canada, European, UK, Australia, Japan and Dual Voltage Versions)

Service Manual

Reference Number 270000-TG1 Rev. 00
Electronic copy only

CONTENTS

3•2•1 and 3•2•1 GS Home Entertainment System Differences

The 3•2•1 and 3•2•1 GS (Gemstone) home entertainment systems share the same basic components. The bass module and bass module cable are identical. The console uses the same electronic parts and most of the same chassis parts. The differences in the console are the console firmware and the color of the silver front bezel and DVD drawer bezel. The arrays used on the two systems are different. The standard 3•2•1 system uses the larger 60mm driver arrays, and are only available in graphite. The 3•2•1 GS arrays utilize the smaller 50mm Jewel Cube® driver. These arrays are available in graphite and silver.

Software Update Information

The firmware located in the main PCB and display PCB's microprocessors can be updated by means of an update CD. These update CDs are available from Bose® Product and Technical Support at 800-233-4408 (Bose service centers only) or 800-367-4008 (Bose system owners) and are automatically sent out to customers who have purchased the 3-2-1 system, filled out and returned the software update card that came with their system literature. Service centers can also download an ISO image of the latest firmware update file from the Service web site at http://serviceops.bose.com and burn it onto a CD for use as an update disc.

Once you have the CD, simply power up the console, press the stop/eject button on the console, place the update CD into the drawer and close it and the update process will begin. When the process is complete you may remove the update CD.

Check to verify that both the display PCB firmware and the main PCB firmware have updated properly. You can do this by using the TAP commands or by a series of button presses on the console front panel. Both of these methods are outlined in the Appendix.

CAUTION: The Bose 3•2•1 and 3•2•1 GS Home Entertainment Systems contain no user-serviceable parts. To prevent warranty infractions, refer servicing to warranty service stations or factory service.

SAFETY INFORMATION

1. Parts that have special safety characteristics are identified by the ⚠ symbol on schematics or by special notes on the parts list. Use only replacement parts that have critical characteristics recommended by the manufacturer.

2. Make leakage current or resistance measurements to determine that exposed parts are acceptably insulated from the supply circuit before returning the unit to the customer.
Use the following checks to perform these measurements:

A. Leakage Current Hot Check-With the unit completely reassembled, plug the AC line cord directly into a 120V AC outlet. (Do not use an isolation transformer during this test.) Use a leakage current tester or a metering system that complies with American National Standards Institute (ANSI) C101.1 "Leakage Current for Appliances" and Underwriters Laboratories (UL) 6500 / IEC 60056 paragraph 9.1.1. With the unit AC switch first in the ON position and then in OFF position, measure from a known earth ground (metal waterpipe, conduit, etc.) to all exposed metal parts of the unit (antennas, handle bracket, metal cabinet, screwheads, metallic overlays, control shafts, etc.), especially any exposed metal parts that offer an electrical return path to the chassis. Any current measured must not exceed 0.5 milliamp. Reverse the unit power cord plug in the outlet and repeat test. ANY MEASUREMENTS NOT WITHIN THE LIMITS SPECIFIED HEREIN INDICATE A POTENTIAL SHOCK HAZARD THAT MUST BE ELIMINATED BEFORE RETURNING THE UNIT TO THE CUSTOMER.

B. Insulation Resistance Test Cold Check-(1) Unplug the power supply and connect a jumper wire between the two prongs of the plug. (2) Turn on the power switch of the unit. (3) Measure the resistance with an ohmmeter between the jumpered AC plug and each exposed metallic cabinet part on the unit. When testing 3 wire products, the resistance measured to the product enclosure should be between 2 and infinite MOhms. Also, the resistance measured to exposed input/output connectors should be between 4 and infinite MOhms. When testing 2 wire products, the resistance measured to exposed input/output connectors should be between 4 and infinite MOhms. If it is not within the limits specified, there is the possibility of a shock hazard, and the unit must be repaired and rechecked before it is returned to the customer.

ELECTROSTATIC DISCHARGE SENSITIVE (ESDS) DEVICE HANDLING

This unit contains ESDS devices. We recommend the following precautions when repairing, replacing or transporting ESDS devices:

- Perform work at an electrically grounded work station.
- Wear wrist straps that connect to the station or heel straps that connect to conductive floor mats.
- Avoid touching the leads or contacts of ESDS devices or PC boards even if properly grounded. Handle boards by the edges only.
- Transport or store ESDS devices in ESD protective bags, bins, or totes. Do not insert unprotected devices into materials such as plastic, polystyrene foam, clear plastic bags, bubble wrap or plastic trays.

THEORY OF OPERATION

1.0 Overview

Note: Refer to console schematic sheets for the following information. The information inside the brackets [ ] is the grid location on the schematic sheet for the component.

The 3-2-1 Home Entertainment system is a single-zone system consisting of the following components:

- Bass module with woofer, bass amplifier and system power supply
- Console with display and controller, IR remote receiver, DVD Player, video and audio decoders, AM/FM tuner, external video and audio source select, Videostage® audio channel expansion, spatial and array speaker processing, speaker equalization, dynamic equalization, and amplifiers for the array elements
- Two two-driver satellite speaker arrays
- IR remote transmitter

The basic elements of the console are:
- Display and display controller assembly
- DVD loader mechanism and control electronics
- DVD manager, Video and Audio decode circuit (DVD back end)
- Video encoder (video DAC)
- AM/FM Tuner
- Audio, Video source select circuitry
- External Audio, Video Inputs, Line Out, Video Out
- Audio Processor (DSP)
- Array Power Amplifiers
- Power Conditioning Circuits

2.0 Power Supply Electronics

Node Name	Voltage	Type	Input	Outputs
V_RAW	+16	~Linear	120VAC	Power Amp,+12V,+10V,+5.1V, +3.3V
+12V	+11.5	Switching	V_RAW	DVD drive motors, +9V
+10V	+10	Linear	V_RAW	AM/FM tuner, FM front-end
+9V	+9	Linear	+12	Sallen-and-Key Filter opamps, Opamp package with “Codec_bias”, Bass eq output buffer, and Analog input buffers, AV Mux
+5V	+5	Switching	V_RAW	DVD drive logic, Display Board, CODEC, Stereo DAC, SPDIF IC, EEPROM, RDS IC
+3.3V	+3.3	Switching	V_RAW	DSP, CS98000 I/O, Flash, DRAM IC’s, Quad Inverter, Quad XOR, CODEC, SPDIF, MUX, Tuner PLL IC, Video DAC, 2.5V
+2.5V	+2.5	Linear	+3.3	CS98000 core, PLL circuits

The power supply electronics are comprised of 4 main sections; switching power supplies, linear power supplies, power supply synchronization, and power fail detection. The console’s input voltage, V_RAW comes from the bass module and is nominally +16VDC. This voltage varies with load and line levels, but is limited to +18V maximum (the maximum rated operating voltage of the power amplifier). This voltage is always present whenever the bass module is plugged into the wall and so the console’s power supplies are likewise active.

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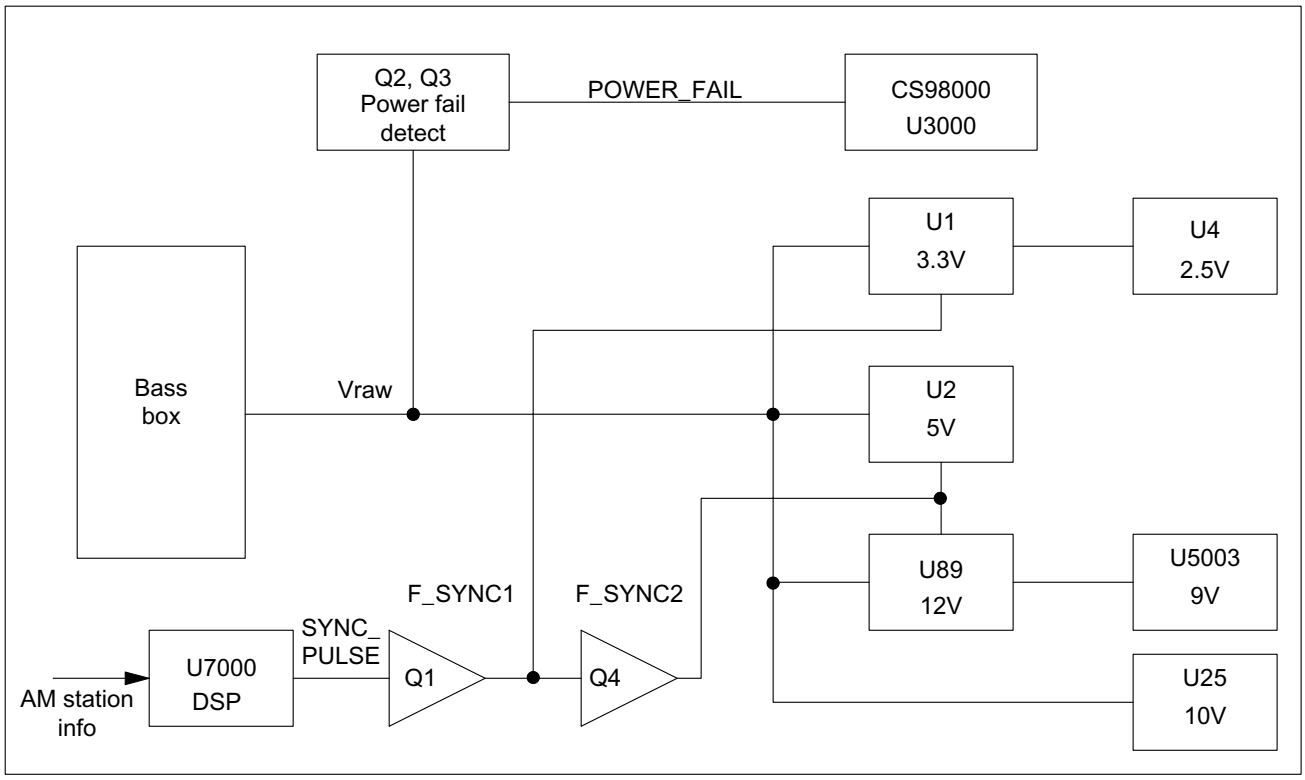
Voltage on V_RAW is modulated by the load placed on it and can temporarily dip well below +13V during audio playback at loud volumes. For this reason, the switching power supply labeled 12V is actually supplying 11.5V to maximize headroom and still comply with the DVD player's operating specifications.

The 2.5V linear regulator is connected to the 3.3V line to increase efficiency and, therefore, minimize heat dissipation. The 9V rail is derived from the +12V line for the same reason, as well as to reduce power supply ripple getting through the AV mux to its outputs. The 10V linear regulator is connected to V_RAW to provide adequate headroom.



Console Power Supply Architecture

The power supplied by each rail varies depending on what mode the system is in. A summary of typical power drawn by rail is given below. Also included for reference is the power drawn by the bass box (120V).

	RAIL							
MODE	**120V**	**Vraw**	**12V**	**5V**	**3.3V**	**10V**	**9V**	**2.5V**
Standby	21.8W	12.5W	1.3W	2.3W	3.2W	.6W *	.7W	1.2W
DVD	25.4W	15.2W	1.9W	4.0W	3.4W	.6W *	.7W	1.3W
CD	25.2W	13.4W	1.9W	4.0W	3.3W	.6W *	.7W	1.2W
FM	22.2W	12.7W	1.3W	2.5W	3.2W	.6W *	.7W	1.2W
AM	21.6W	12.3W	1.3W	2.5W	3.2W	.3W *	.7W	1.2W
AUX	22.2W	12.7W	1.3W	2.5W	3.2W	.6W *	.7W	1.2W

* The power supplied by the 10V rail is dependent on the last mode the tuner was in. Vraw, 120V, and the 10V rail all drop by approximately .3W if the tuner was in AM mode last as opposed to FM.

Note: Power supplied by rail (with system muted)

THEORY OF OPERATION

2.1. Switching Power Supplies

The switching power supplies use ST L4973D3.3 regulator ICs U1 [sheet 11, C6], U2 [sheet 11, A6], and U89 [sheet 11, D3]. The power supplies are designed as step-down Buck converters. The voltage fed back to the chip on pin 13 determines the output voltage; the chip's control circuitry will work to keep this voltage at +3.3V. The +5.1V and +12V supplies use resistor divide-down networks to obtain the +3.3V feedback voltage.

The reference designators listed below correspond to the +12V regulator on the tuner board; the designs of the +5.1V and +3.3V regulators are nearly identical.

IC Pin	Components Connected	Function
1	R89, C91	Sets switching frequency (when not controlled externally)
10	C96	Bootstrap to drive internal D-MOS
11	R100	Inhibits supply
12	R90, C93, C94	Lead-lag filter for compensation loop
13	R91, R92	Voltage feedback for control
18	C92	+5.1V for external reference
19	C95	Sets supply soft-start time constant
20	None	Supply frequency switching synchronization (see section 2.3 below)

A number of additional series inductors and parallel capacitors exist to provide filtering functions.

There are two 750 Ohm resistors (R115 and R116 [sheet11, C1]) tied between +12V and ground to keep the 12V switcher operating correctly under light load conditions. Without these ballast resistors, under light load, there is not enough current flowing to charge the bootstrap capacitor and the D-MOS does not turn on fully.

The compensation networks used for these switching power supplies have been chosen to provide stability under all conditions as well as to provide minimal RF interference to the tuner. The supplies function in both continuous and discontinuous mode depending on the load.

2.2. Linear Power Supplies

The linear power supplies are the standard 7800 series TO-220 packages with the exception of the 2.5V linear regulator (U4 [sheet 11, C3]). The 2.5V linear regulator is a low dropout surface mount with adequate topside copper to keep the IC at an acceptable temperature.

2.3. Supply Synchronization

In order to minimize input voltage ripple and EMI we have implemented a variable frequency alternate switching synchronization scheme. The DSP outputs a synchronization pulse based on the AM station to which the console is tuned. This 50% duty cycle signal is fed through two transistor stages (Q2 and Q3 [sheet 11, C/D 6/7]) which provide both buffering and inversion. The switching IC's synchronization inputs (pin 20 of U1,U2, and U89) are rising edge-triggered so duty cylce is not as important as switching frequency. When the switcher IC gets a rising edge on its synchronization input, it turns its internal D-MOS switch on. The duration of this on time relative to the switching period, or duty cycle, is directly related to input and output voltage (duty cycle = Vout/Vin). The 3.3V switcher (U1) is fed an inverted synchronization pulse relative to the 12V and 5V switchers (U89 and U2 respectively). This switching scheme serves to flatten out the input current demanded.

Since a Buck converter demands an input current equal to its output current while the D-MOS switch is on, and the 3.3V switcher outputs, approximately, the current of both the 12V and the 5V switcher, it makes sense to turn the 3.3V switcher on at a different time. By doing this the input current ripple is roughly halved. This switching scheme has the added benefit of improving the input capacitor's lifetime by reducing the self heating caused by ripple.

2.4. Power Failure Detection

It is important to detect a power failure and alert the mircoprocessor to save any relevant information and mute the power amplifiers so that no audio "pops" will be heard. The power failure detection circuit that we employ controls an edge-triggered interrupt to the CS98000 microprocessor (U3000's PIN 185 [sheet 3, C7]) to do just that. If the voltage on V_RAW falls below roughly 9V, the microprocessor will be alerted that there is a power failure occuring. The interrupt will be unasserted (go high) when V_RAW goes above 14V. This large hytsterisis is set so that dips in V_RAW caused by loud volumes will not inadvertantly trip a power fail interrupt. In a brownout condition, the system will mute with the power dip and then recover gracefully when the normal line level is restored (V_RAW goes above 14V).

3.0 Control Electronics

The majority of the control electronics are located on the Main PCB, the notable exception being the infrared transceiver module and the slave microprocessor located on the display board.

3.1 Microprocessor

U3000 is a CS98000 DVD decoder IC that also functions as the Media Center's main processor.

U3000 contains two 32-bit RISC processors, a DSP core, a memory interface which supports SDRAM and FLASH ROM, an ATAPI interface, a DMA controller, an MPEG video decoder, a digital video interface, digital audio processing, and a general purpose interface.

The MPEG video decoder in U3000 decodes the MPEG information from the DVD-ROM drive on the ATAPI bus and stores the decoded video into SDRAM for later readout to the video interface. One RISC processor runs the navigator software to access the program material from the DVD/CD or external digital audio source and manages the Video and Audio decoders to present the material. The second RISC processor runs Bose® software that handles system control, the on screen display (OSD) functions, and I/O functions including reading the console buttons, receiving the IR remote control commands, driving the OSD and LCD display on the console. The DSP core in U3000 decodes the digital audio data as required, and sends it out the digital audio interfaces. The ATAPI interface connects to the DVD-ROM drive. U3000 sends standard ATAPI control commands to the drive and receives MPEG-compressed audio, video, and control information from the drives.

3.1.1 Microprocessor clock

U3000 is clocked by a crystal inverter-oscillator whose nominal frequency is 27.000 MHz. The inverter used is internal to the DSP IC U7000 [sheet 5, C3] and is located between pins 30 and 31. An external bias resistor is not required, as an internal resistor of approximately 1M Ohm is also included internally. The crystal in the inverter's feedback path is designed for a 20pF load, achieved by the series combination of a 20pF and 22pF load capacitors C705 and C7057 and other stray board capacitance and input gate capacitance. R7070 sets the pole in the oscillator's loop response, and a 7404 inverter located in U7008 [sheet 5, B1] buffers the output between the oscillator and U3000.

THEORY OF OPERATION

After the signal is buffered by U7008, the 27 MHz clock signal (DX27MHZ) enters U3000 at pin 202 [sheet 12, C2]. From there the buffered 27 MHz clock signal exits U3000 at pin 154 [sheet 3, D6] as the signal VDO_CLK. From there VDO_CLK is sent to the video DAC U5000 pin 29 [sheet 10, C7] to drive the video circuitry. Frequency accuracy within ±50ppm of this oscillator circuit is necessary for color video operation.

3.2 Memory

The U3000 memory interface supports both SDRAM and flash memory of various sizes. Both memory ICs are connected to the same bus, and a chip select chooses between the two devices. The type of memory cycle that is run depends on which address space is needed.

3.2.1 SDRAM

U3002 [sheet 2, C2] is a 2-megaword by 32-bit synchronous dynamic random access memory SDRAM IC. For SDRAM accesses, a memory clock of about 80-100 MHz that synchronizes data access is sent to the chip at pin 68. Data commands for accesses are coded in the /RAS and /CAS signals (pins 18 and 19), and data read/write selection is done by the /WE signal (pin 17). The address to be written or read is given on the address bus (pins 25-27 and 60-66). The 32-bit data bus contains the word to be written or read after the pipeline delay of the memory chip.

3.2.2 FLASH

U3001 [sheet 2, C5] is a 1-megaword by 16-bit Flash memory IC. U3001 shares the memory address and data bus with U3002, but its cycle is different from the SDRAM: flash access is asynchronous and does not use a memory clock. Address (pins 1-9, 18-24, and 48) and chip select (pin 26) is presented to the chip, and data appears 1 access time later on the data bus. The chip select input on pin 26 of U3001 is a wired OR gate that allows output enable or write enable of U3000, causing the chip select to be asserted, or pulled low at pin 2 of U3001. The flash chip only supplies 16-bit data to U3000; the other data bus lines are not driven during flash access.

U3001 can be programmed in-circuit by U3000; this allows software updates in the field via CD-ROM. During re-programming, the operating and new program are held in SDRAM. Power failures during field Flash update could result in the Media Center being made completely inoperable.

3.3 Remote Control

3.3.1 Display Controller assembly

The Display Controller assembly provides all user interface, power management, and source management functions.

+5 volt voltage monitor. Holds the Display Controller and, indirectly, all other processing circuits in reset unless the +5 volt supply is above minimum threshold and stable.

3.3.2 Display Controller

- Monitors the /POWER_FAIL input and disables all other functions until false
- Drives the LCD Display
- Controls the Backlight LED
- Receives User commands from the IR detector and 8-button switch matrix
- Receives commands, code downloads from the TAP serial interface
- Serves as Master on both the TUNER I2C, CCB communications buss, and the 3.3v I2C communications buss

3.3.3 Communications Busses

TUNER_CLK, TUNER_DATA and TUNER_DATA_IN form either an I2C or CCB buss among the display controller U3, DVD controller U3000, tuner PLL IC U2034, RDS decoder U2033 and the serial EEPROM U6000. The display controller U3 is permanent master for either I2C or CCB buss communications. All other devices function as slaves.

The display controller U3 also functions as permanent master controller on the I2C_DATA, I2C_CLOCK lines when communicating to the DSP U7000 and the audio codec U4000.

AV_DATA and AV_CLK provide a dedicated I2C buss from the display controller U3 to the audio/video MUX U5001.

VID_DATA and VID_CLK form a high-speed I2C buss from the DVD controller U3000 to the video encoder U5000.

SI2C_DATA and SI2C_CLK form another dedicated I2C buss from the DVD controller U3000 to the S/PDIF decoder U4020.

4.0 Audio Electronics

There are four sources of audio inputs available to the 3-2-1 console audio path...

- Disc Sources (DVD/CD)
- Internal Analog (Tuner)
- External Analog (Aux In, Video 1, and Video 2)
- External Digital Audio / S/PDIF (Aux D, Video 1 D, Video 2 D, Video 1 Optical)

…as well as two sets of outputs…

- Fixed “line level” outputs (Aux Out)
- Speaker outputs including 4 sets of array outputs on the 9-pin connector and a line level “bass_eq” signal to the bass box amplifier.

Being a one-zone system, it is only necessary to process one and only one audio input to both sets of outputs. However, the number of channels of input and output usually do not match (i.e. stereo input to 4 channel+bass main output or AC3 surround sound to the 2 channel Aux Output). To marry inputs to outputs, this and other processing (VideoStage®, array processing, compression, volume control, etc.) is accomplished in the digital domain by the Audio Processor DSP (SHARC AD21065, U7000). The audio path design is therefore centered on this IC, meaning all audio signals must ultimately pass through the DSP IC. The overall intent of the IC’s of the audio path is fulfill these requirements.

THEORY OF OPERATION

4.1 Input Audio Path

For analog audio input sources (Aux In, Video 1, Video 2, and Tuner) these L and R signals are selected by the Mitsubishi A/V Mux (M52790, U5001 [sheet 10, B4]), passed though attenuation (about –1.5 dB) buffers (U5002) to the A/D portion of the CS4228 Surround sound "Codec" (U4000). These inputs are full 2Vrms line level capable where the small attenuation is necessary as distortion may occur in driving the A/D inputs single-ended with a full 2V input. These signals are converted to I2S digital audio format and sent to a dedicated input serial port (CODEC_SDOUT) of the DSP IC U7000.

Internal Disc audio source data (DVD or CD) are fed to the CS98000 DVD Decoder IC U3000 via the ATAPI interface. External digital audio is also sent to the CS98000 DVD Decoder IC via I2S (SPDIF_LRCK, SPDIF_BCKand SPDIF_DATA) from the S/PDIF receiver/mux (CS8415A, U4020). The CS98000 then can decode the desired input stream if it happens to be in a compressed audio format (AC-3, MP3, DTS, etc.). When an external source is selected with digital (S/PDIF) information available, the CS98000 queries the S/PDIF decoder IC (CS8415A) via I^2C communication to determine if the receiver has locked to the appropriate input. When it has done so, the DVD_AUDATA(0:2) path is muted while the CS8415A is reconfigured to output RMCK (see I2S communication section). The CS98000 reconfigures its master clock output to an input. It will decimate the input or decoded audio stream appropriately. After the CS8415A is properly configured for the stream rate the DVD_AUDATA(0:2) path is un-muted.

After any decompression, the data is then presented to the DSP's three other available input serial ports (DVD_AUDATA0,1,2, AUDIO_LRCK, AUDIO_BCK) in I2S format. The data present on each of these channels is dependent on the type of audio being decoded.

Format	Meaning	DVD_AUDATA 0	DVD_AUDATA 1	DVD_AUDATA 2
ACMOD0	Dual mono	Mono/Mono	None	None
ACMOD1	1/0 : C	None	None	C/None
ACMOD2	2/0 : L, R	L/R	None	None
ACMOD3	3/0 : L, C, R	L/R	None	C/None
ACMOD4	2/1 : L, R, Sur	L/R	Sur/None	None
ACMOD5	3/1 : L, C, R, Sur	L/R	Sur/None	C/None
ACMOD6	2/2 : L, R, Ls, Rs	L/R	Ls/Rs	None
ACMOD7	3/2: L, C, R, Ls, Rs, LFE	L/R	Ls/Rs	C/LFE
PCM	Stereo/matrix encoded L,R	L/R	None	None

Note: data is LRCK L/H

4.2 Output Audio Path

For the Aux Out output, the CS4340 stereo DAC U1000 [sheet 6, C4] takes MIXOUT_DATA and generates the L and R output to a full scale value of about 1.25 Vrms at an output impedance of 1.56K Ohms. The large value for this output R is for ESD protection and EMI reasons. Note there is no volume control for this output. Components tied on the output (Q1000, Q1001, etc.) are used in muting the output when audio data isn't there or errors are present in I^2S communications.

For speaker outputs the CS4228 U4000 [sheet 6, B3] is used again with its 6 D/A converters (5 are used) taking CODEC_SDIN1:3 and generating the following output signals:

Input signal	During "Left" LR clock (low)	During "Right" LR clock (high)
CODEC_SDIN1	LC (Left Center) – pin 23	RC (Right Center) – pin 24
CODEC_SDIN2	LS (Left Surround) – pin 25	RS (Right Surround) – pin 26
CODEC_SDIN3	Bass – pin 27	None

The CS4228 produces a substantial amount of out-of-audio-band (beyond 20kHz) noise (about 50mVrms) due the nature of the sigma-delta conversion DACs and lack of much filtering on the IC itself. This amount of noise was seen as serious enough to implement filtering on the outputs of the DACs before amplification. Without filtering, there would be a substantial amount of power dissipation in the amplifier stage as well.

The DAC outputs are biased to 2.3V and have a full scale output of 1.3Vrms. For the array outputs, these signals are sent through 3 orders low-pass filtering. These circuits comprise of a passive RC filter (i.e. R157, C181) and the Sallen-and-Key type 2nd order filters centered around U151 and related components. These together give a cutoff frequency of around 40kHz. These filters also attenuate the audio signals by (-)8dB before being AC coupled to the output amplifier. Thus the total gain after D-to-A conversion is 18dB (or about x8) which at full scale output can drive the speakers to 10.4Vrms. Note that for proper biasing of the op-amps a reference voltage (CODEC_BIAS) is generated (2.3V) for the inputs with one of the op-amps in U5002. The voltage gain on the output of the filter is again mainly for DC biasing and sets it to nominally 4.6V. Also note that the input bias for the amplifier IC is set to half Vraw or around 8V with no load. A similar gain structure is used for the bass output but a less complicated filter (single-pole) with a cutoff frequency of 6kHz is used to drive the BASS_EQ output to the bass box.

The /MUTE signal controls both array and bass amplifier (on /MUTE2) inputs on any normal muting condition by Pulse Width Modulating the signal to get a longer time constant that would normally be achievable with the given components. Note the muting time constant of the bass amplifier is much longer than the array amplifier, meaning that sometimes with high bass content material, the bass can be heard for a little time after the arrays have muted. /MUTE1 bypasses the normal time constant and is used as an emergency mute from the CODEC IC in case there are errors in the digital data that might cause snaps or other harsh noises to be sent to the speakers.

4.3 Digital Audio Communication (I^2S)

Digital audio data is transferred into and out of the DSP IC via 4 input and 4 output serial interfaces. The digital communication on the 3-2-1 is accomplished using the I^2S protocol. All IC's that uses digital audio have the capability in either firmware or software to communicate with I^2S. In I^2S format each data line carries two "channels" of data, a "left" signal and a "right" signal. (see the input and output paths for what data signals are actually on each I^2S line). I^2S also uses an involved clocking scheme to keep everything straight.

L/R CLOCK: The sample clock (otherwise called the L/R clock) defines the sample rate (e.g. 44.1kHz) as well as which of the two channels is "active" depending on the level of the signal. The sample rate for AUDIO_LRCK is determined by the input source and can be set to 32kHz, 44.1kHz, or 48kHz. The sample rate for SPDIF_LRCK is determined by the external digital input stream.

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BIT CLOCK: There is also a bit clock that synchronizes each bit of each sample. The 3-2-1 console uses 16 bit audio. The frequency of AUDIO_BCK is 32x the sample frequency (16 bits x 2 samples) whereas SPDIF_BCK is set for 64x the sample rate. The difference here is due to the constraints of the two IC's driving the signals. The CS98000 can handle the fact that its input bit clock 64x while it is receiving data from the S/PDIF receiver while continuing to drive its output (AUDIO_BCK) at 32x.

MASTER CLOCK: Finally, a "master clock" is necessary to drive the sigma-delta data converters (both A/D and D/A) in the system at integral rate greater than the bit clock. This clock is also necessary to drive the CS98000 input port when the S/PDIF receiver is active. I2S_MCLK is set for 256x the sample rate.

Special note on clocking: If the S/PDIF decoder is recovering a sample rate greater than 50 kHz, the CS98000 must configure it to output RMCK at 128 times the recovered data sample rate. This will permit the AUDIO_BCK, AUDIO_LRCK to run at ½ the S/PDIF sample rate. The CS98000 will decimate a high input sample stream to the ½ speed output sample rate.

DATA: The actual audio data is timed with the bit clock. The data to the 4228 and 4340 is currently being clocked in a nonideal fashion. The DSP's output serial ports must be configured to change data on a rising edge of the AUDIO_BCK whereas the 4228 and 4340 are reading the data on this edge. This means there is very little (<10ns) hold time for the data. There seems to have been no problems with this to date.

The following table is a summary of the various I2S clock and data signals…

I2S Signal	Output From	Input To	Frequency
AUDIO_LRCK	98000	DSP, 4228, 4340*	Sample rate (Fs)
AUDIO_BCK	98000	DSP, 4228, 4340*	32xFs
I2S_MCLK	98000, 8415**	4228, 4340 (MCLK), 98000**	256xFs
SPDIF_LRCK	8415	98000	Fs
SPDIF_BCK	8415	98000	64xFs
SPDIF_DATA	8415	98000	(data rate)
DVD_AUDATA0:2	98000	DSP	(data rate)
CODEC_SDIN1:3	DSP	4228	(data rate)
CODEC_SDOUT	4228	DSP	(data rate)
MIXOUT_DATA	DSP	4340	(data rate)

Note: *These signals are buffered to maintain signal integrity to the DSP. AOUT_BCK and AOUT_LRCK are the actual signals to the 4228 and 4340.

**Which MCLK signal to use is selected by the RMCK_SEL line that controls the 74125 tri-state output buffer (U4001). When the 98K is the master, it drives the "output" line (MCLK) directly. When the 8415 is the master, the input of U4001 is selected (RMCK) and the 98K line is changed to an input.

4.4 IC Configuration

The following settings are required to set the audio/communication paths properly specifically for the 3-2-1.

CS8415 (S/PDIF Receiver)

- Register 0x01 – 0x80 – I2S_MCLK is switched through to RMCK when lock is lost, Interrupt is active high.
- Register 0x02 – 0x00 – RMCK rate at 256xFs
- Register 0x06 – 0x2? – SPDIF_BCK set for 64xFs, 16-bit resolution

CS4228 (Surround CODEC)

- Register 0x01 – 0x04(Default) – MCLK rate to 256xFs, base rate mode
- Register 0x0D – 0x04 – Serial port set to I2S, BCK rate set for 32xFs
- SDOUT (pin 4) – pulled low so that a rising edge of RST the serial registers are set for I^2C.

CS4340 (Stereo DAC)

- DIF1 and DIF0 – pulled low – sets for I2S data
- DEM1 and DEM0 – pulled low – disables emphasis (performed in the DSP)

5.0 Video Electronics

Video signals may be generated internally or passed-through from a set of external (VIDEO INPUT) connectors. Internally-generated signals include DVD playback and On Screen Display (OSD) signals. OSD menus are accessed by pressing the SETTINGS button on the remote. When not playing back a DVD or generating an OSD, the Media Center defaults to passing-through external video signals. The Media Center provides both Composite and S-Video outputs for both internal and external video paths.

The video interface drives several kinds of video digital to analog converters to generate the analog video monitor drive signals. U3000 (CS98000) generates a standard ITU R.BT656 digital video data stream with embedded synchronization shown as signals VDO1:8 and VDO_CLK. This standard uses an 8 bit bus, with interleaved Y, Cr, Cb data. Synchronization information is embedded in the data stream, and exclusively uses values of 00 and FF (hex). Y values are from 1 to 254, with 1 being black. C values are from 1 to 254, with 128 being no chroma.

The video digital-to-analog converter, U5000 [sheet 10, C7], is a 44 pin quad flat pack, containing extensive video processing circuitry. This IC has the capability of generating Composite, S-Video, and Component outputs, which satisfy the requirement to provide the signals necessary for internal video. The data sheet for this part (number CS4955) shows the block diagram and signal processing circuitry inside the chip. The chip has many programmable registers inside, to set different operation modes, etc. These registers are set by the main processor over a serial I^2C bus (VID_DATA and VID_CLK, pins 32 and 33).

The CS4955 receives the ITU R.BT656 data bus, decodes the synchronization and separates the Y, Cr, and Cb values into separate data streams. The three channels of video data are processed appropriately, including Macrovision generation, and sent its digital-to-analog converters. Composite video is generated at pin 44, S-video Y and C are generated at pins 48 and 47, and RGB or YCrCb (component video) are generated at pins 39, 40, and 43 but are not used.

THEORY OF OPERATION

The CS4955 must receive a 27 Mhz signal from the clock oscillator, with an accuracy of +/- 1350 Hz. This frequency is phase lock-looped inside the CS4955 to generate the 3.579545 Mhz color subcarrier for the composite video signal, and must be of high accuracy so that all television monitors can lock onto it and be able to decode color information to display. If this accuracy is not met, there is a danger that on some monitors will not lock and produce a black-and-white image. This clock is originally generated by a 27 MHz oscillator that drives the DSP, which in turn drives the CS98000 which then drives the 4955.

To allow switching between external and internal video signals the Mitsubishi A/V mux (M52790), U5001 [sheet 10, B4], is used. The 3 video signals from the CS4955 are passed to one set of the A/V Mux inputs, and the external input video signals (CV2, Y2 and C2) are passed to another set of A/V Mux inputs. The Mux will select either set of video signals to be sent on further through the video chain. The selection is made by I^2C communication on a dedicated bus from the display controller micro to the A/V Mux IC.

After internal/external selection, the three video signals are sent to the output connectors. Because the MUX IC biases the video signals to 3Vdc for Composite and Luma, 4V for Chroma, these signals must be AC coupled. The A/V mux drives the video signal through large capacitors, and a 75 Ohm resistor (C5066, 5067, 5068 and R5086, 5087, 5088). This ensures equipment compatibility even if there are DC differences between the 3-2-1 and the driven equipment (TV). The 75 Ohm resistor provides reverse cable termination for best signal integrity. Video sent through these capacitors have low frequency drop-off, causing sag in the video signal. These capacitors should be large enough not to cause any problems in horizontal synchronization, even for rapid changes in brightness (luma) of the video.

6.0 Tuner Electronics

6.1 Control

Detailed control of the tuner is implemented by the display microprocessor U3 upon instructions from the RISC processor residing inside U3000. U3000 will issue a command via the tuner bus to tune to a specific frequency and in response to this the display micro. Will communicate with the PLL IC, U2034 [sheet 8, C4], to set the local oscillator frequency as required.

The PLL IC also has some general purpose input and output ports which the display microprocessor programs as follows:

a) $\overline{\text{FM}}$/AM	Controls Q2001 which switches power to the FM front-end and the IF amplifier. In AM mode these are both switched off.
b) $\overline{\text{AM}}$/FM	Switches the mode of detector IC U2000 and sets which output (FM : pin 23, AM : pin 24) is active. Inactive => high impedance.
c) $\overline{\text{FORCE-MONO}}$	Forces the detector IC to decode FM into monaural audio.
d) ST-LED	This input port is used to monitor the stereo indicator coming from pin 7 of U2000. The state of this pin is shown on the stereo icon display or in the OSD FM status window.
e) IF/MUTE	Pin 9 of U2034 is used to mute the audio output of the detector IC. When this pin is low audio output is enabled. When this pin is high impedance R2015 pulls the DC level of the IF/MUTE line high (>3.5v), audio is muted and the output of the FM IF buffer appears on this line. This is fed to the IF counter on pin 13. This is used during seek to determine if a valid broadcast signal is present.

THEORY OF OPERATION

6.2 FM Tuner

The FM RF signal from the antenna is input via the 3.5mm input connector J2000 [sheet 7, B8] and goes to the FM front-end module. The antenna supplied with the Media Center differs from the standard FM dipole antenna in that it contains a balanced-to-unbalanced converter which is designed to reduce the amount of interference from other electronic products.

The FM front-end contains a tuned RF amplifier an FM local oscillator and a mixer. The 10.7 MHz IF output signal (pin 7 of the module) passes through a 10.7 MHz ceramic filter, CF2000, an FM IF amplifier and then through a second ceramic filter, CF2001. Transistor Q2000 and related circuitry form the FM IF amplifier which produces about 15 dB of voltage gain and provides the proper impedance matching for the ceramic filters. These FM IF filter stages reject unwanted FM stations and noise.

The output signal from CF2001 is fed to the LA1837 AM/FM detector IC, U2000 pin1 [sheet 7, C4]. This device contains the FM IF limiter, FM detector, FM stereo MPX decoder and S-meter circuitry which is used for seek processing. The FM IF input signal to the LA1837 goes through several gain/limiter stages and then to a single-tuned, coil-based discriminator circuit. The discriminator coil, T2001 [B5], is adjusted for minimum second harmonic audio distortion. The recovered FM composite signal appears on pin 23 of U2000.

The composite audio signal is filtered by C2060 and fed back into pin 22 of U2000. The value of C2060 is chosen to optimize FM stereo separation. The stereo MPX decoding is also performed by U2000 and the decoded left and right signals are output on pins 20 and 21. The pilot PLL VCO is completely internal to the LA1837 detector IC, not requiring an external 456 kHz ceramic resonator as in older designs. The pilot PLL loop filter is formed by C2015, R2018, and C2014 on pin 14.

FM de-emphasis for the right audio channel is set by C2021, R2024 and the output impedance of pin 21 of U2000 (3.3k). Similarly for the left audio channel. For a US unit the capacitor values are set to produce 75µS de-emphasis, and for Europe/Japan they are set to produce 50µS de-emphasis. The resultant de-emphasized and amplified audio signal appears on pins 16 and 17. Signals above the audio band, including the 38 kHz sub-channel demodulation components are cut off by the input filters in U4000 and the audio DSP is used to create a notch filter at 19kHz to reject the 19 kHz pilot tone thus removing the need for external MPX filters.

The FM and AM S-meter signals, pin 11 and 12 of the LA1837 respectively, are analog voltage levels that indicate the FM IF and AM RF input signal levels. These signals are connected to the 8 bit A/D inputs of the display microprocessor. During factory tuner alignment the appropriate test signal levels are injected into the UUT and the resultant ADC values for FM stop level, FM force-mono level, FM stereo level and AM stop level are stored in non-volatile memory on the main board.

The stop level is the voltage level above which the signal strength is deemed strong enough to warrant stopping on a channel during seek. This does not mean that the unit will always stop on a station if the S-meter level is high enough since an IF count is also performed to ensure that the correct IF frequency has been obtained.

The force-mono level is the level below which the microprocessor will force the detector to decode audio information into monaural since the noise associated with decoding into stereo is deemed to be unacceptable. The stereo level is the level above which a channel which has been automatically forced into mono will return to being able to decode in stereo (if stereo material is present).

Note that switching stereo “on” via the OSD will enable the above automatic force-mono function while switching it “off” disables this automatic function and ALWAYS forces the unit into monaural decoding. Also note that the stereo icon on the front display and the stereo status flag on the OSD indicates the state of the ST-LED line which indicates detection of the 19kHz pilot tone present in stereo broadcasts. In force-mono (automatic or otherwise) this will always be low even if the actual broadcast is in stereo.

The nominal FM stop/force-mono and stereo levels are:

FM stop	30 dBf @ 98.1 MHz
FM force-mono	40 dBf @ 98.1 MHz
FM stereo	42 dBf @ 98.1 MHz

6.3 AM Tuner

The signal from the external AM loop antenna enters through the 2.5 mm AM jack, J2001 [sheet 7, D8], and is fed to the AM front end module, T2004. This module contains the varactor-tuned RF and Local Oscillator (LO) tracking circuits. This part is pre-tuned by the manufacturer for proper alignment with AM antenna (part number 199824-002), and is further adjusted during factory alignment, if necessary. The RF tuned output is fed to the AM buffer FET transistor Q2003 and the buffered output is sent to pin 27 of U2000 which contains the AM RF amplifier, mixer, IF amplifier, AM detector, and AM S-meter circuitry. The 450 kHz AM IF output signal that appears on pin 2 is filtered by the IF filter, T2000, and fed back into the IC on pin 4. The AM IF signal is demodulated by U2000 and the audio output is sent to pins 20 and 21, to pass through the low pass filter used in FM for de-emphasis.

In order to avoid having harmonics of the switching power supplies interfere with the AM tuner the switching frequency is controlled by SYNCH_PULSE, a clock output from the DSP, U7000. The display microprocessor contains a table of clock frequency vs AM channel frequency and each time a new channel is tuned, the DSP is commanded to change the SYNCH_PULSE frequency to the appropriate frequency. The frequency of SYNCH_PULSE is centered around 100 kHz.

The AM seek stop processing and factory alignment is performed in a similar fashion to FM mode processing. The nominal AM stop level is 58 dBµV/m @ 1080 kHz.

6.4 Phase-locked Loop Tuning

The AM and FM local oscillators are controlled by the PLL IC, U2034 [sheet 8, C4]. The microprocessor selects the AM or FM band and the particular frequency. The 7.2 MHz crystal, Y2000, is connected across an inverting amplifier inside U2034 to form an accurate and stable crystal oscillator. The 7.2 MHz oscillator is divided down to produce a 12.5 kHz reference frequency in FM mode and a 10 kHz reference frequency in AM mode. U2034 divides down the AM or FM LO input, compares it to the appropriate reference frequency and generates an error signal which is output on pin 19.

This error signal is integrated and amplified by an active lead-lag filter formed using an internal FET inside U2034 and associated components connected to pins 19, 20 and 21. C2051, C2039, R2037, R2036 and R2038 control the gain and pole-zero locations of the filter. The resulting signal output at pin 21 is used as a tuning voltage and is fed back to the AM and FM front-ends.

The AM tuning voltage is further filtered by R2000 and C2033 and is fed back to the common node of the varactors inside the AM front end, T2004. The tuning voltage varies the capacitance of the varactor diodes, which in turn simultaneously tunes both the AM antenna and the AM LO. In FM mode, the tuning voltage is filtered by R2033 and the input capacitance of pin 5 of the FM front-end (0.022uF). As in the AM case, the tuning voltage is fed to varactors which tune the LO frequency and RF filtering.

7.0 DVD Electronics

The DVD-ROM drive is a Toshiba model SD-M1502. The drive is capable of playing DVDs (including CSS decoding), CD-ROMs, and audio CDs. An ATAPI cable for data and separate power cable connect the drive to the Main PCB.

8.0 LCD Display

Note: Refer to the LCD display schematic sheet 1 for the following information. The information inside the brackets [ ] is the grid location on the schematic sheet for the component.

The Console display board is comprised of the uC PCB, and display parts: the display frame, LCD glass, diffuser, LED backlight, and elastomers. The frame holds all the display parts by compressing the elastomers and the twisted tabs. Behind the LCD glass is the diffuser. The diffuser serves a dual purpose: as a light diffuser to balance the light output at different viewing angles, and as a black mask around the edges to mask light leaking out. Behind the diffuser is the LED light pipe backlight. Having the smooth side of the diffuser towards the backlight helps with the overall light output. The LED light pipe is made up of a single super-bright green LED molded on its side inside a transparent plastic piece at one end. The LED light (green for US) fires off that (left) end axially down the length of the light pipe. Internal refraction keeps the light within the light pipe. Micro-lenses on the backside of the light pipe direct the light through the front of the pipe. A white reflector sheet on the backside and the non-LED end of the light pipe reflects some leakage light back to the pipe. White elastomers and white silkscreen printing on the PCB also help reflecting some light back to the pipe. There are three elastomers: two long strips for the LCD glass and one short piece for the LED light pipe. Signals and power are connected via the direction of the thin layers within the elastomers. While the two long pieces for the LCD are carbon based, the short piece for the LED is silver based. On the PCB the elastomers are compressed onto the carbon printing pads to make connections. On the LCD, the long elastomers are compressed against the shelf side of the glass, where there are exposed conductive ITO pads (faintly visible when viewed against bright light). On the LED light pipe, the short elastomer is compressed against the wrapped around LED leads in the cavity on the backside of the pipe.

The LCD is a passive matrix (4x43) alphanumeric type (two 7-segment numeric characters, eight 14-segment alphanumeric characters, and various other icons), with a total of 167 individually addressable icons. The LCD is a backlit transmissive negative-image type. The center row of alpha-numeric characters show detailed information such as titles and presets (left two numeric characters), chapters, tracks, time, volume, text, as well as system status messages, modes and selections (right 8 alpha-numeric characters).

THEORY OF OPERATION

System messages and mode selections are also displayed by icons in the surrounding area. These include: TITLE, PRESET, CHAPTER, TRACK, SETTINGS, ANGLE, SLEEP, SHUFFLE, REPEAT DISC, REPEAT TRACK, MOVIE EQ, RDS, and STEREO. Besides punctuation marks, there are also the 'play' and 'pause' graphics icons. Mode selections are displayed on the bottom row of icons: DVD, CD, AUX, VIDEO 1, VIDEO 2, AM, and FM. With the exception of either CD or DVD, all source icons are displayed to allow source selections when the system is turned on. A graphics 'box' icon around a source icon indicates that the corresponding source is selected. The LCD has a viewing area of 28mm x 100mm. It is biased for a 12 O'clock (top) viewing direction (60/60/60/20 degrees viewing angles, where 20 degree is for the bottom view).

The 167 individual icons are addressed by the LCD microcontroller (uC) U3 [C5] on the PCB. There are 4 COM lines and 43 SEG lines out of the uC. There are also 43 SEG pins on the LCD. However, there are 7 COM pins on the LCD. Some of the 7 COM pins are connected on the PCB to match the 4 COM lines on the uC. To select an icon on the matrix, the corresponding COM line and SEG line (as the matrix indices) are asserted. To select all icons of a COM line, that COM line and all the SEG lines are asserted. To select all icons associated with a SEG line, all COM lines and that SEG line are asserted. By the same token, a short or open on some lines would cause all the icons associated with those lines to light up or not light up.

The LCD is operated off a 5V drive, at 1/3 bias. While an icon is not addressed, the corresponding COM and SEG lines are refreshed with rectangular AC type DC-biased waveforms whose difference is also a rectangular AC waveform with peaks below the turn-on voltage of the icon. It's only when the icon is addressed that the difference becomes larger than the turn-on voltage for a portion of the time (1/4 duty given that the system is 1/4 multiplexed by 4 COM lines). In other words, for a selected icon the COM - SEG difference waveform would have portions reaching the peaks 0V and 5V, during 1/4 of the time. Vice versa for a non-selected icon, the COM - SEG waveform would have portions away from the peaks 0V and 5V by at least 1/3 of 5V, or 5/3 V all the time.

When the Console is turned off, both the LCD and the LED backlight are turned off. When the Console is turned on by the pressing of console buttons or remote, the LCD and the LED backlight are both turned on. The LED backlight's brightness is bright when the Console is first turned on. It remains bright for approximately 7 seconds. Afterwards it goes to normal brightness. It remains in normal brightness until the next time a console button is pressed or a remote command is received, when it goes to bright mode. The LED remains bright for approximately 7 seconds after the last key press or remote command. System initiated updates on the display such as time and track changes do not cause the LED backlight to brighten.

The uC U3's ports P30 and P31 control the LED backlight's brightness. In the normal brightness, only P31 is asserted LOW. LED current goes from +5V through the LED to BACKLIGHT and returned through P31 only. In the bright mode, both P31 and P30 are asserted LOW. A larger LED current returns through both ports. In the OFF mode, both P31 and P30 are asserted HI, resulting in zero LED current.

Console switches are connected to the uC U3 via connector J2. The 8 switches are not multiplexed but simply sampled by the uC. Each uC port connected to a switch has an internally pulled-up resistor. Closing a switch or shorting the corresponding port pin to GND is detected by the uC as a key press. IC's that hang off the uC include a reset chip U2 at port RES, and a remote sensor Q3 at port P73. Both ports are normally high and LOW active. The reset chip resets (LOW) when +5VUC drops below 4.63V nominally. A ceramic resonator CF1 provides the main clock for the uC U3, at 8MHz.

Communication with the Console main PCB is via connector J3. Off -board communication is via J1, the TAP port. Through the TAP port the system usage profile can be obtained.

9.0 Bass Module

Note: Refer to the bass module schematic sheet 1 for the following information. The information inside the brackets [ ] is the grid location on the schematic sheet for the component.

9.1 Power Supply Electronics

The bass module is a single channel system: its differential input is converted to accept a single ended bass signal from the console; the bridge output is connected to a 2 Ohm bass driver through J7 [B1]. The bass power amplifier U1 [B2] is a class AB type and is powered by a DC power supply (V). The same power supply (V) is shipped to power the console via a cable connected to the D-sub connector J6 [A6]. The bass signal and control signals from the console are sent through the same cable bundle. The console does all of the signal processing, equalization, and control. The bass module PCB supplies the main power supply (V) for the bass module and the console. The bass module PCB also amplifies the bass from the console using the same main power supply (V). The bare PCB is a universal PCB suitable for all bass module variants.

AC mains power is connected by the line cord via jack J1. A slow acting fuse F1 is connected between J1 [D7] and the locking primary connector J3 (or J2 or J4) to protect against faults. A Metal Oxide Varistor (MOV) VR1 is placed after the fuse and across the line. It is used to protect against lightning strikes and other line transients. Transformer T1 connects to primary connector J3 (or J2 or J4) and secondary connector J5. Polarized locking jack J5 ensures the correct connection of the pins from T1. Depending on the voltage variants, unique transformers, primary jacks, and if required, switches are used. F1 and VR1 [D7] also have unique values. See the bass module schematic diagram for details.

Transformer T1 has a primary winding unique for different AC mains voltage requirements. However it has about the same single secondary winding. The primary has a series thermal fuse to protect against overload and faults. The secondary winding has an optional center tap (currently not used) that can be part of a half-supply voltage circuit. There is also a Negative Temperature Coefficient (NTC) thermistor/sensor embedded inside the transformer. It is used in the power (voltage) limiting circuit in the event of overload. Large brackets and fins on the transformer help with power dissipation.

The main power supply V of the system is derived from the full wave rectifier BR1, filtering capacitor C22 and MOSFET switch Q1. It is a line frequency cycle-controlled switching power supply. By inserting the switch element Q1 in series with BR1 and C22, and controlling the OFF and ON times of Q1, a regulated maximum voltage can be obtained at V. Without the switch Q1 in series, BR1 and C22 would become a simple rectifier-capacitor AC-DC circuit, which would just full-wave rectify the secondary AC voltage of transformer T1. With Q1, the charging current is cut off when the voltage across C22 reaches a threshold (close to V). This is accomplished by the control circuit made up of ZR1, Q2 and Q3, etc.

During the rising edge of the rectified AC, when the full wave rectified output (between + and - terminals of BR1) rises beyond the zener voltage of zener diode ZR1, it is turned ‘on’ and clamped at its zener voltage (16V). The ‘turn-on’ of ZR1 causes excess current flow, which turns on Q2. The ‘turn-on’ of Q2 forces Q3 to turn ‘off’, and consequently Q1 to turn ‘off’. When Q1 turns ‘off’, the charging current is cut from C22 to prevent further charging to a higher voltage.

THEORY OF OPERATION

Normally this happens before the rectified AC climbs to its peak. V is therefore limited to approximately 16.5V (between 15.5V and 17.5V) peak. In other words, on the rising edge of the rectified AC voltage, charging of C22 is turned off after its voltage has reached V.

On the falling edge of the rectified AC voltage, charging of C22 is turned back on before the falling rectified AC voltage reaches V. The 'turn-on' of Q1 prior to reaching V is accomplished by the help of R12 and the unloading effect of the transformer T1. Right after Q1 turns 'off', the unloading of the charging current on the transformer allows the transformer to have a larger unloaded output voltage, resulting in a voltage across Q1 (i.e., the unloaded rectified AC voltage minus the voltage across C22, V). The voltage across Q1 re-biases the voltage of the zener ZR1 through R12 (and R8). The base of Q2 is biased up, resulting in an earlier 'turn-off' prior to the voltage falling to V. Consequently Q3 and Q1 turn 'on' earlier. The rest of the charging is governed by BR1: it turns 'off' after the rectified AC voltage falls below V.

After Q1 turns 'on' on the falling edge, it remains 'on' until it turns 'off' on the rising edge (after reaching V). During Q1's 'on' time, BR1 turns off on the falling edge but turns back 'on' on the rising edge. C22 is charged only when both Q1 and BR1 are on. That happens on two occasions for each half line cycle: once on the rising edge and the other on the falling edge. That means that for normal loads there are four charging periods for each line cycle. For light or no loads, Q1 sometimes turns 'on' only once in a while depending on the load. Charging may happen just on one rising or falling edge for the full line cycle. It may even happen every other cycle. Or it may happen on both edges for a half cycle but skip the next. For heavy loads Q1 stays 'on' all the time. The circuit then behaves just like a bridge (BR1) and a capacitor (C22) with Q1 shorted - the normal AC-DC charging circuit.

While in theory the above is true descriptions of the voltages, in reality there are some subtle differences in the actual circuit. For example, the 'rectified AC voltage' is not the normal waveform of the absolute value of the sine wave. When Q1 turns 'off', the back-bias through R12 actually applies the V voltage across the circuit. When BR1 is not in the conduction mode for charging C22, the back-biased V voltage powers the control circuit, creating a voltage across the + and - terminals of BR1. The voltage across + and - terminals of BR1 then looks like the larger of a normal rectified AC voltage and a flat DC voltage of approximately V. Another example is at the base of Q3. That voltage is being modulated between a Vbe (of Q3) and a Vce, sat (of Q2). Furthermore, transients are ignored in the descriptions. One of such transients is created by the 'turn-off' of the charging current on the rising edge. That transient creates a spike voltage across the whole control circuit, including Q1. Measures such as by-pass and smoothing caps (C24 and C21) are put in place. Q1's 'turn-off' is slowed down to suppress that transient and dissipate the heat. C23 is used to suppress ringing and prevent reverse-bias conditions on Q2 and Q3. C9 is used for suppression of line conducted emissions.

In the event of overload or overheating of the transformer T1, the embedded NTC thermistor that's connected to the zener bias circuit controls the output voltage at V. When the transformer overheats, the resistance of the NTC thermistor drops. At around 100 degrees C, the NTC starts to become effective in the circuit. Through R14, the NTC takes the bias current from ZR1, resulting in a lower threshold voltage for V. By the time the transformer heats to around 125 degrees C (if it does), the NTC becomes fully effective. It consequently limits the voltage at V to be below 10V. The lowered voltage at V means less power available, and less power dissipated by the transformer. The lowered power dissipation allows the transformer to cool. Eventually the system servos to such that the transformer temperature is between 100 degrees C and 125 degrees C, below its rated temperature of 130 degrees C. Under normal ambient temperature and normal loads, the voltage V is not compromised by the NTC.

THEORY OF OPERATION

9.2 Audio Signal Path

The bass module amplifier PCB utilizes a TDA 7396 IC for the bass channel audio. The equalized bass audio signal is fed from the 3-2-1 console, down the 15 pin cable, and into the bass amplifier PCB at pin 6 of J6. This single-ended bass audio signal is then fed to pin 2 of the bass channel amplifier IC, U1. The bass audio output of this IC is taken off of pins 5 and 7, which is fed to the single woofer through J7.

In addition to bass channel audio from the 3-2-1 console, the console also supplies a DC voltage level to the /MUTE input of the bass module at pin 13 of J6. This +5Vdc level is used to un-mute the bass channel amplifier IC U1, taking it out of standby. Without this DC voltage, the device will not come out of standby, and no bass channel audio will be heard. When testing the bass module without the console attached, you will need to provide this +5Vdc level to allow the bass module to un-mute. Refer to the bass module test cable fabrication instructions in the Appendix of this service manual.

Note: The /COMP signal output of the bass module at pin 12 of J6 is not used.

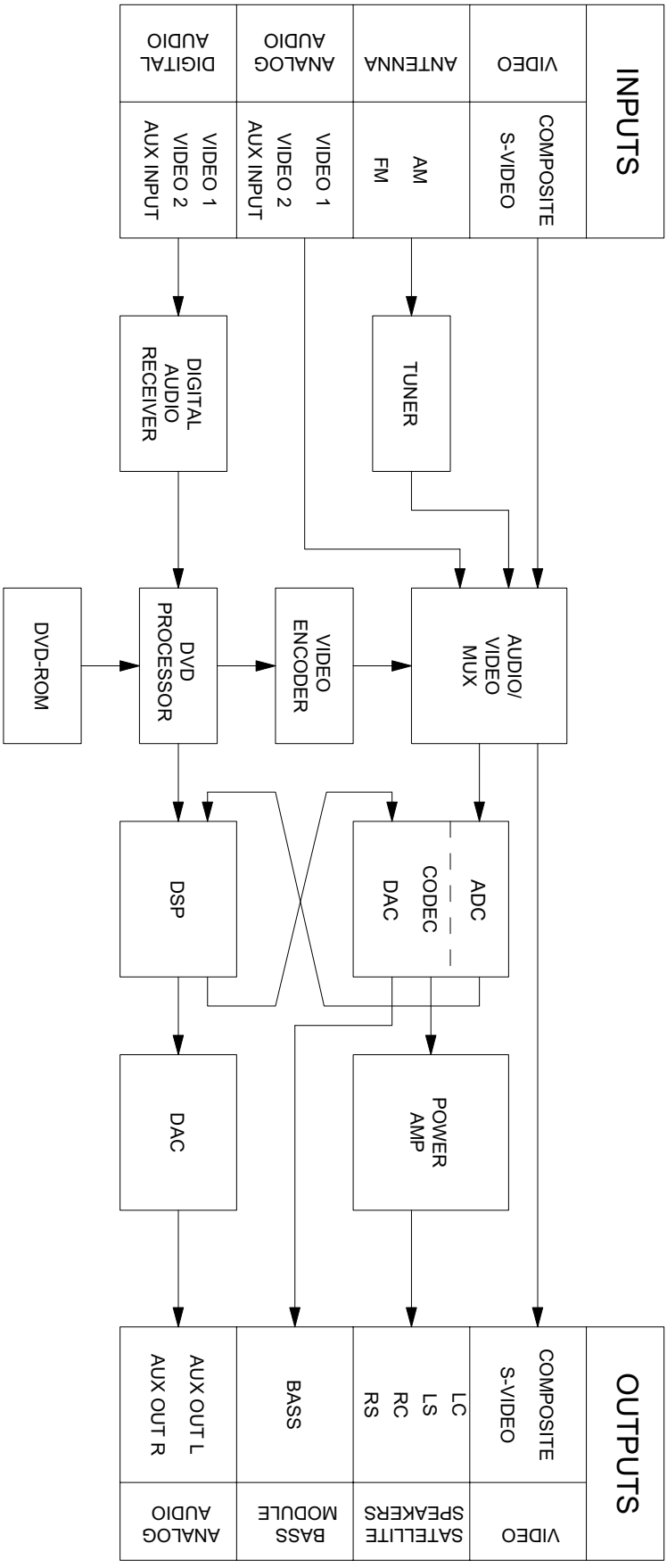


Figure 1. 3-2-1 Console Block Diagram

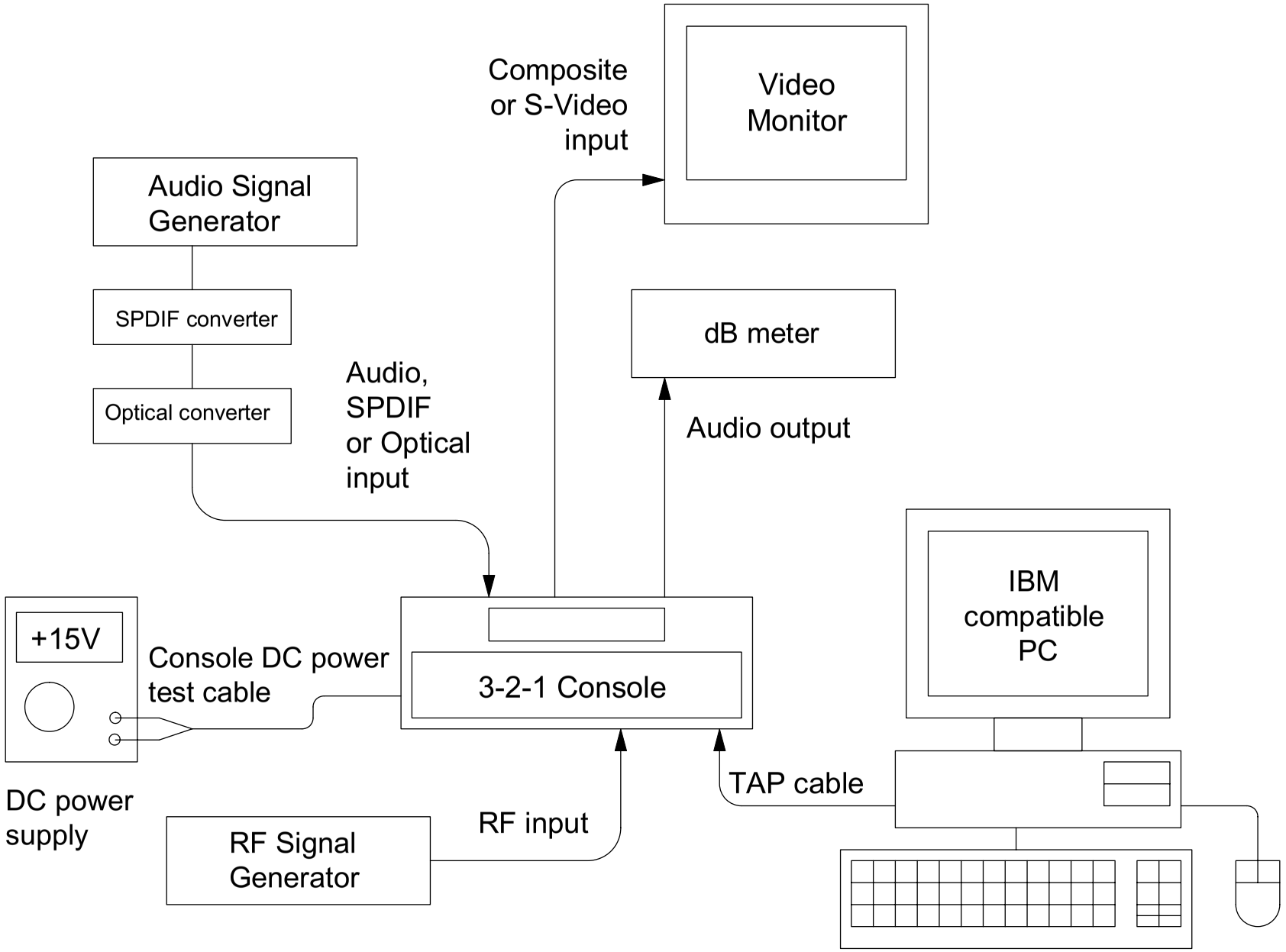


Figure 2. 3•2•1 Console Test Setup Diagram

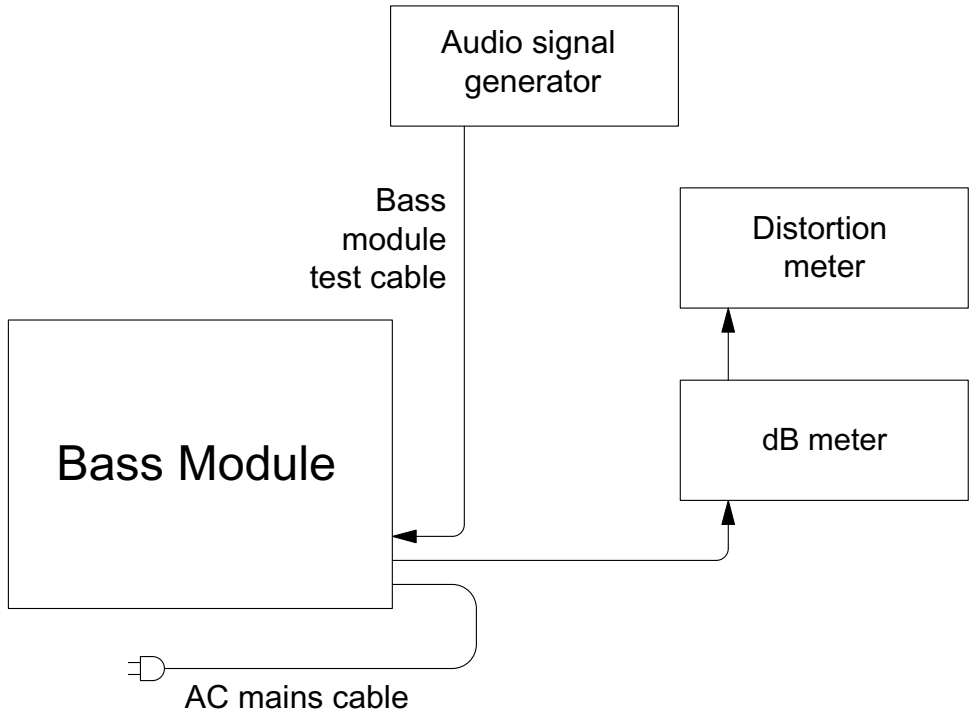


Figure 3. 3•2•1 Bass Module Test Setup Diagram

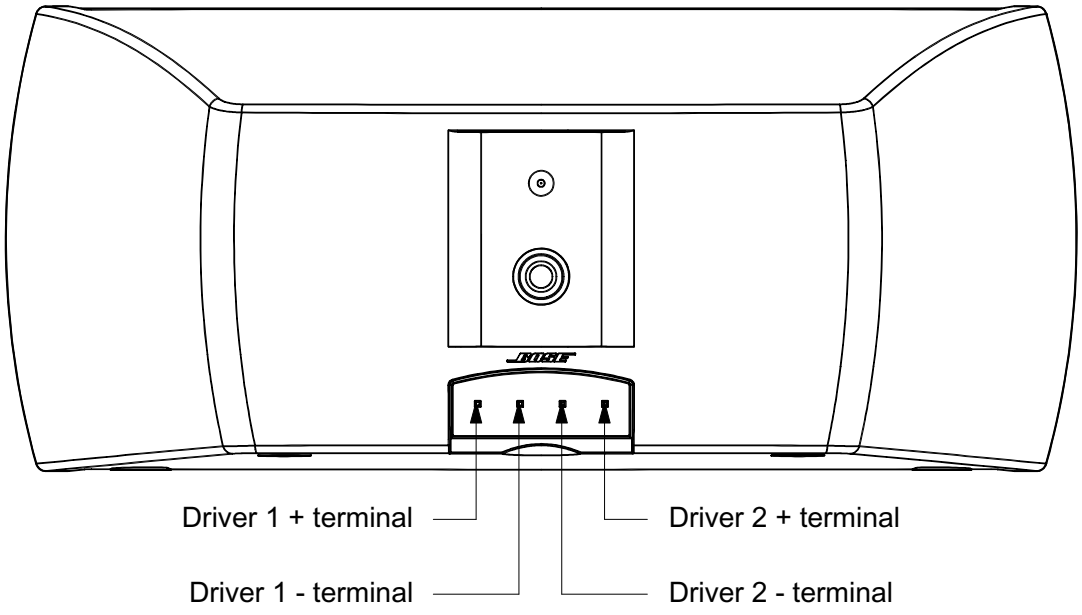


Figure 4. 3•2•1 and 3•2•1 GS Satellite Speaker Wiring Diagram

TEST PROCEDURES

Console Procedures

CAUTION: The DVD drive mechanism should not be closed by pushing it shut with no power applied to the console. Doing so could damage the drive. It must be closed with power applied so that the locking mechanism inside the drive will engage properly when the drawer is closed.

Equipment required:

Audio signal generator
Digital multimeter
Analog to S/PDIF converter
S/PDIF to optical converter
AM/FM signal generator
Video signal generator or DVD player
Abex test DVD (TDV-540A)
Video monitor
DC power supply or bass module w/cable
Composite Video cable
S-Video cable
Optical cable

Test Setup

Set up the unit under test as shown in Figure 2 for the following tests.

1. Analog Audio Test

1.1 Apply a 1 Vrms, 1 kHz signal to the left and right VIDEO 1 audio analog inputs.

1.2 On the console, select the VIDEO 1 input.

1.3 Measure the output level at the audio outputs on the console rear panel. It should be 470 mVrms ± 10%.

1.4 Repeat steps 1.1 to 1.3 for the VIDEO 2 and AUX audio analog inputs.

2. Coaxial Digital Audio Test

2.1 Connect the audio signal generator to the input of the analog to S/PDIF converter.

2.2 Connect the output of the S/PDIF converter to the VIDEO 1 coaxial digital input.

2.3 Apply a 500 mV, 1 kHz signal to the analog input of the S/PDIF converter.

2.4 On the console, select the VIDEO 1 source.

2.5 Measure the output level at the line outputs on the console rear panel. It should be 300 mVrms ± 10%.

2.6 Repeat steps 3.1 to 3.5 for the VIDEO 2 digital coaxial input.

2.7 Repeat steps 3.1 to 3.5 for the AUX digital coaxial input.

3. Optical Digital Audio Test

3.1 Connect the audio signal generator to the input of the analog to S/PDIF converter.

3.2 Connect the output of the S/PDIF converter to the input of the S/PDIF to optical converter.

3.3 Connect the output of the optical converter to the VIDEO 1 optical input.

3.4 Apply a 250 mV, 1 kHz signal to the analog input of the S/PDIF converter.

3.5 On the console, select the VIDEO 1 source.

3.6 Measure the output level at the line outputs on the console rear panel. It should be 150 mVrms ± 10%.

4. Video Tests

4.1 Connect the video generator or DVD player to the COMPOSITE VIDEO INPUT only.

4.2 Connect the video monitor to the COMPOSITE VIDEO OUTPUT.

TEST PROCEDURES

4.3 Set the video generator to display a test pattern. If using a DVD player, load a DVD disc into the tray and start playback.

4.4 On the console, select the VIDEO 1 source.

4.5 Confirm that the test pattern or DVD video appears on the video monitor and that there are no obvious video problems.

4.6 Connect the video generator or DVD player to the S-VIDEO input only.

4.7 Connect the video monitor to the S-VIDEO output.

4.8 Set the video generator to display a test pattern. If using a DVD player, load a DVD disc into the tray and start playback.

4.9 On the console, select the VIDEO 1 source.

4.10 Confirm that the test pattern or DVD video appears on the video monitor and that there are no obvious video problems.

5. Internal DVD Video Test

5.1 Load the test DVD into the console.

5.2 Connect the video monitor to the S-VIDEO output of the console.

5.3 On the 3-2-1 system remote control, press the CD/DVD button to start playback of the DVD disc.

5.4 Confirm that the test pattern or DVD video appears on the video monitor and that there are no obvious video problems.

6. DVD Audio Test

6.1 Load the test DVD into the console.

6.2 If necessary, connect the satellite arrays to the 9-pin D-sub connector.

6.3 On the 3-2-1 system remote control, press the CD/DVD button to start playback of the DVD disc.

6.4 Verify that the audio plays.

7. CD Playability Tests

Test discs required:
ABEX TCD-714R
ABEX TCD-721R
ABEX TCD-725R
ABEX TCD-732R
Philips TS4

7.1 Insert the ABEX TCD-725R test disc into the console CD/DVD tray.

- Play the defect tracking (interruption) track. Verify that the track plays properly. The nominal is a 1.0 mm defect, 0.8 mm limit.
- Play the defect tracking (black dot) track. Verify that the track plays properly. The nominal is a 1.0 mm defect, 0.8 mm limit.
- Play the defect tracking (fingerprint) track. Verfiy that the track plays properly. The nominal is a 75 um defect, 65 um limit.

7.2 Insert the ABEX TCD-721R test disc into the console CD/DVD tray. Play the defect tracking (scratch) track. Verify that the disc plays properly. The nominal is a 1.6 mm defect, 1.0 mm limit.

7.3 Insert the ABEX TCD-714R test disc into the console CD/DVD tray. Play the defect tracking (eccentric disc) track. Verify that the disc plays properly. The nominal is a 280 um defect, 210 um limit.

7.4 Insert the ABEX TCD-732R test disc into the console CD/DVD tray. Play the defect tracking (warped disc) track. Verify that the disc plays properly. The nominal is a 1.0 mm defect, 0.7 mm limit.

TEST PROCEDURES

7.5 Insert the Philips TS4 test disc into the console CD/DVD tray. Play tracks 1 through 15, verifying that each track cues up within the test limits. Nominal is 2 seconds or less, limit 3 seconds.

8. Laser Current Measurement Procedure

Note: The 3-2-1 system console CD/DVD drive uses a separate laser for each medium. You will need to perform these tests using a CD disc to measure the CD laser current and a DVD disc to measure the DVD laser current.

8.1 Remove the console top cover and DVD mechanism using Disassembly/Assembly procedure 3.

8.2 Remove the bottom cover of the CD/DVD mechanism to allow access to the board.

8.3 Connect the DVD drive to the console using the ATAPI and DVD power extender cables.

8.4 Insert a CD disc into the mechanism tray. Press the PLAY button on the console.

8.5 Measure and record the voltage at the point 5V and L5V. Be sure to use the GND pad near the 5V and L5V points.
See Figure 5.

8.6 Subtract L5V from 5V (5V-L5V) and record the laser voltage (LmV). LmV/1 Ohm equals laser current (LC).

8.7 The measured laser current value should be + 20% of the printed current rating on the pickup head (PU). See Figure 6. If the value is out of range, and the lens has been cleaned, replace the DVD drive.

8.8 Repeat steps 8.4 to 8.7 for the DVD laser assembly.

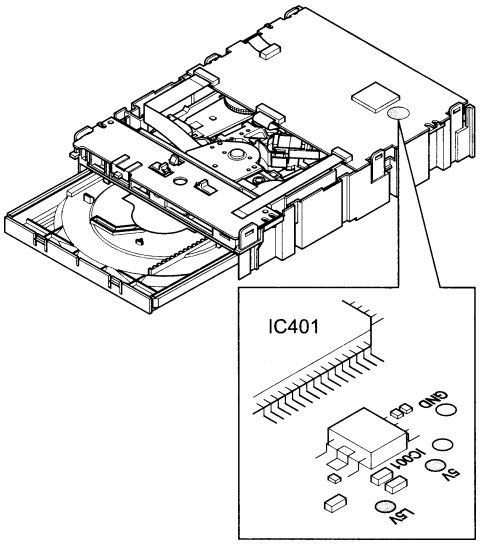


Figure 5. Laser Voltage Test Points

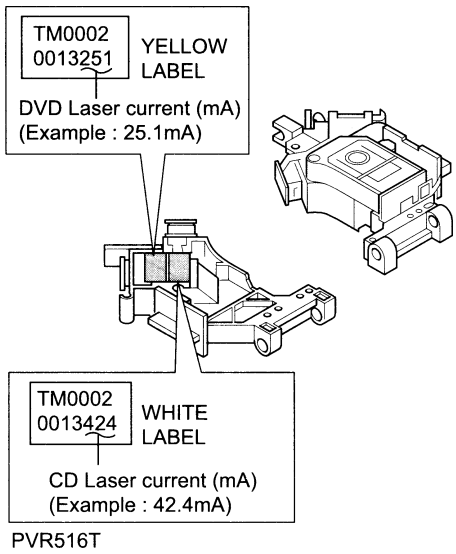


Figure 6. Laser Current Rating Label

TEST PROCEDURES

3-2-1 Console Tuner Adjustments/ Measurements

The following tests can be performed without the use of an IBM compatible PC.

AM Adjustments

For all AM alignments and tests plug the AM antenna, part number 199824-002, into the console and position it 2 feet away from the unit. Configure the AM antenna, a standard test loop and RF generator as shown below to create the specified field strength for each test. The equivalent field intensity in dBuV/m is 20 dB less than the generator output level in dBuV EMF at the receiving antenna. The signal levels given do not include this factor.

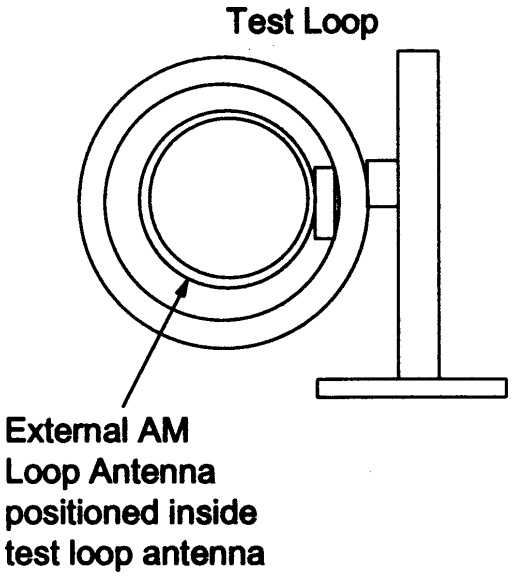


Figure 7. AM Loop Antenna Test Setup

10. AM RF Tracking

10.1 Connect an AC meter to the AUX OUT jacks.

10.2 Inject a 1500 kHz (US, Dual Voltage) or 1503 kHz (Euro, UK, AUS and Japan) RF signal at a level of 90 dBuV emf, 30% modulation, 1 kHz modulation frequency.

10.3 Tune the console to 1500 kHz or 1503 kHz (as appropriate) and adjust the red slug (T2004) for maximum audio level at the left or right audio output. Verify that the level is greater than 40 mVrms.

10.4 Change the RF frequency to 600 kHz (US, Dual) or 603 kHz (Euro, UK, AUS and Japan) and re-tune the console to 600 kHz or 603 kHz (as appropriate).

10.5 Adjust the black slug (T2004) for maximum level. Verify that the level is greater than 40 mVrms.

10.6 Repeat steps 10.2 to 10.5 until maximum audio output is obtained without the need for further adjustment.

11. AM Sensitivity

11.1 Inject a 1080 kHz RF signal at a level of 74 dBuV emf, 30% modulation, 400 Hz modulation frequency.

11.2 Tune the console to 1080 kHz.

11.3 Connect a dB meter to the audio output jacks and reference it (set to 0 dB) to the current audio output.

11.4 Remove the AM modulation and measure the audio output jacks. The reading should be less than -20 dB.

FM Adjustments

Note: Unless otherwise noted, set the RF generator for 1 kHz, mono modulation, pilot off and 75 kHz deviation. Power levels for FM testing are given in dBf at the antenna input to the unit.

Typically a test setup will consist of an RF generator with a 50 Ohm output impedance and a 50 Ohm to 75 Ohm impedance matching element. The two most commonly used impedance matching element are a resistive network which has a 5.7 dB insertion loss or a “lossless” transformer which has a 0.5 dB insertion loss.

TEST PROCEDURES

To find the required setting in dBuV emf from a given dBf value for an RF generator with a 50 Ohm output impedance use the conversions in the following table.

Using a "lossless" transformer	Subtract 1.3 dB. eg: 65dBf => set generator to 66.8 dBuV emf
Using a resistive network (5.7dB loss)	Subtract 6.5 dB eg: 65dBf => set generator to 71.5 dBuV emf

Note: For generators with RF level resolution of only 1 dB round up.

Note: For the following FM tests, you will need an antenna adapter cable, part number 261412, to go from an F connector to the 3.5mm connector used on the 3-2-1 console.

12. FM Distortion Measurement/Adjustment

12.1 Inject a 98.1 MHz (83.0 MHz Japan units), RF signal at a level of 65 dBf into J2000.

12.2 Tune the console to 98.1 MHz (83.0 MHz Japan units).

12.3 Measure the distortion plus noise (THD+N) at the audio output jacks. If it is less than or equal to 0.50%, verify that the audio level is greater than 190 mV. If these are not the measurements you have, proceed to step 12.4.

12.4 If the THD+N is greater than 0.55%, or the audio level is less than 190 mV, adjust T2001 for minimum distortion. Verify that the level is greater than 190 mV and the distortion is less than 0.55%.

13. FM Sensitivity

13.1 Inject a 98.1 MHz (83 MHz for Japan units) RF signal at a level of 19 dBf into J2000.

13.2 Measure the THD+N at the audio output jacks. It should be less than or equal to 3.0%.

14. FM Stereo Separation

14.1 Inject a 98.1 MHz (83.0 MHz Japan units) RF signal set to 1 kHz left only modulation with 10% pilot modulation and 75 kHz total deviation at a level 65 dBf into J2000.

14.2 Reference a dB meter to the level at the left audio output jack.

14.3 Switch the RF signal modulation to right only channel.

14.4 Measure the level at the left audio output jack. It should read -25 dB or less.

Computer Assisted Tuner Test Procedures

Additional Equipment Required:

- IBM Compatible PC
- Model 3-2-1 TAP cable, p/n 266603
- B+B Electronics RS-232 to TTL level shifter, model 232LPTTL

Note: Refer to the computer set up instructions in the appendix for proper connection to an IBM compatible computer.

Refer to Figure 4, AM antenna setup diagram, to achieve the proper field strength for the given RF generator setting.

Some of the commands will automatically set the calibration, requiring only an external RF signal at the input of the tuner. Other commands require the technician to make measurements and adjustments.

Before commencing with the tuner measurements/alignments enter the command LXOF to disable communication between the display microprocessor and the system microprocessor. You should receive an ACK (acknowledge) response on the computer's screen. If not then re-try until successful. To re-enable communication enter LXON.
Note: The console's display will not change to reflect the mode changes during tests.

TEST PROCEDURES

AM Adjustments

Enter the command TUAM to switch source to AM.

15. AM Alignment

15.1 Inject an 1500 kHz (US, Dual Voltage) or 1503 kHz (Euro, UK, Aus and Japan) RF signal at a level of 90 dBuV emf, 30% modulation at 1 kHz.

15.2 Enter the command TUSF15000 or TUSF15030 (as appropriate) into the computer. This will tune the unit to 1500 kHz or 1503 kHz.

15.3 You should receive the response “ACK>” (acknowledge) on the computer’s screen.

Note: If you receive an error response on the computer screen, enter the TUAM command to ensure the correct mode is selected and re-enter the command in 15.2.

To verify the AM tuning frequency enter the TUGF command to get the presently tuned frequency. The response on the computer screen should be "1500" or “1503“ followed by an “ACK>”

15.4 Using a non-metallic tuning tool, adjust the red slug of T2004 for maximum output at the audio output jacks. Verify that the level is greater than 40 mVrms.

15.5 Inject a 600 kHz (US, Dual Voltage) or 603 kHz (Euro, UK, Aus and Japan) RF signal at a level of 90 dBuV emf.

15.6 Enter the command TUSF06000 or TUSF06030 (as appropriate) into the computer. This will tune the unit to 600 kHz or 603 kHz.

15.7 You should receive an ACK response on the computer screen.

15.8 Using a non-metallic tuning tool, adjust the black slug of T2004 for maximum output at the audio output jacks. Verify that the level is greater than 40 mVrms.

15.9 Repeat steps 15.1 through 15.8 until the audio level is at a maximum without adjustment.

16. AM Stop Level

16.1 Inject a 1080 kHz RF signal at a level of 78 dBuV emf, 30% modulation at 1 kHz.

16.2 Enter the command TUSF10800 into the computer. This will tune the unit to 1080 kHz.

16.3 You should receive an “ACK>” response on the computer screen.

16.4 Enter the command TUAR. The unit will then sample the AM S-meter level, and store it in the EEPROM as the stop level and return an “ACK>” response.

16.5 Enter the command TURA to see the stored level; the response on the computer should be as follows: XX (where XX is the stored level in hexadecimal form). Enter the EECS command to write the new level setting to the EEPROM before removing power.

The current AM S-meter voltage level = 5 x (stored level in decimal) / 256. Refer to the hex to decimal to voltage tables in the appendix.

FM Tuner Tests

For all FM measurements and adjustments, the RF signal is to be connected from the signal generator to J2000 via a 50 to 75 Ohm impedance matching network.
The input levels are to be as read at the input of J2000.

TEST PROCEDURES

FM Adjustments

Enter the command TUFM to switch source to FM.

17. FM IF Centering Adjustment

17.1 Inject a 98.1 MHz (83.0 MHz Japan units), 1 kHz mono modulation, pilot OFF, 75 kHz deviation RF signal at a level of 50 dBf into J2000.

17.2 Enter the command TUSF09810 (TUSF08300 Japan units) into the computer. This will tune the unit to the appropriate frequency.

17.3 You should receive an ACK response on the computer screen.
Note: If you receive an error response on the computer screen, enter the TUFM command to ensure the correct mode is selected and re-enter the command in 17.2.

To verify the FM tuning frequency enter the TUGF command to get the presently tuned frequency. The response on the computer screen should be “98.1” ("83.0" Japan units).

17.4 Enter the command TUIF into the computer. The unit will then go through an algorithm that determines the optimum offset for the local oscillator (L.O.) setting to account for filter variances in the IF strip. This offset is then stored in the EEPROM.

17.5 Enter the command TUGI to see the stored offset; the response on the computer should be as follows: “TUGI X >” followed by an “ACK>” (where X is the stored offset). The actual frequency offset of the L.O. is this offset multiplied by 25 kHz. Valid offsets are –1, 0 or 1. Enter the EECS command to write the new level setting to the EEPROM before removing power.

18. FM Distortion Measurement/ Adjustment

18.1 Inject a 98.1 MHz (83.0 MHz Japan units), 1 kHz mono modulation, pilot OFF, 75 kHz deviation RF signal at a level of 65 dBf into J2000.

18.2 Enter the command TUSF09810 (TUSF08300 Japan units) into the computer. This will tune the unit to the appropriate frequency.

18.3 Measure the distortion plus noise (THD+N) at the audio output jacks. If it is less than or equal to 0.50%, verify that the audio level is greater than 190 mV. If these are not the measurements you have, proceed to step 18.4.

18.4 If the THD+N is greater than 0.55%, or the audio level is less than 190 mV, adjust T2001 for minimum distortion. Verify that the level is greater than 190 mV and the distortion is less than 0.55%.

19. FM Sensitivity

19.1 Inject a 98.1 MHz (83.0 MHz Japan units), 1 kHz mono modulation, pilot OFF, 75 kHz deviation RF signal at a level of 19 dBf into J2000.

19.2 Measure the THD+N at the audio output jacks. It should be less than or equal to 3.0%.

20. FM Stereo Separation

20.1 Inject a 98.1 MHz (US, Dual, Euro, UK and Aus) or 83.0 MHz (Japan) RF signal set to 1 kHz left only modulation with 10% pilot modulation and 75 kHz total deviation at a level 65 dBf into J2000.

20.2 Enter the command TUSF09810 (TUSF08300 Japan units) into the computer. This will tune the unit to the appropriate frequency.

20.3 Reference a dB meter to the left audio output jack.

20.4 Switch the RF signal modulation to right only channel.

20.5 Measure the left audio output jack. It should read -25 dB or less.

21. FM Stop Level

21.1 Inject a 98.1 MHz (83.0 MHz Japan units), 1 kHz mono modulation, pilot OFF, 75 kHz deviation RF signal at a level of 30 dBf into J2000.

21.2 Enter the command TUSF09810 (TUSF08300 Japan units) into the computer. This will tune the unit to the appropriate frequency.

21.3 You should receive an ACK response on the computer screen.

21.4 Enter the command TUFR. The unit will then sample the FM S-meter level, and store it in the EEPROM as the stop level.

21.5 Set the RF generator for 98.9 MHz (US, Dual Voltage), 98.3 MHz (Euro, UK, Aus) or 83.0 MHz (Japan), 1 kHz mono modulation, pilot OFF, 75 kHz deviation RF signal at a level of 35 dBf into J2000.

21.6 On the console, press the SEEK UP button. Verify that the unit stops at 98.9 MHz, 98.3 MHz or 83.0 MHz as appropriate.

21.7 Set the console for 98.1 MHz (US, Dual), 98.3 MHz (Euro, UK, Aus) or 83.0 MHz (Japan).

21.8 Set the RF generator for 98.9 MHz (US, Dual, Euro, UK and Aus) or 83.3 MHz (Japan), 1 kHz mono modulation, pilot OFF, 75 kHz deviation RF signal at a level of 25 dBf into J2000.

21.9 On the console, press the SEEK UP button. Verify that the unit does not stop.

Note: You can enter the command TURF to see the stored level; the response on the computer should be as follows: XX (where XX is the stored level in hexadecimal form). Enter the EECS command to write the new level setting to the EEPROM before removing power.

The current FM S-meter voltage level = 5 x (stored level in decimal) / 256. Refer to the hex to decimal to voltage tables in the appendix.

22. FM Stereo & Force Mono Threshold

22.1 Inject a 98.1MHz (83.0 MHz Japan units) RF signal set to 1kHz stereo L=-R modulation with 10% pilot modulation and 75 kHz total deviation at a level of 42 dBf into J2000.

22.2 Enter the command TUSF09810 (TUSF08300 Japan units) into the computer. This will tune the unit to the appropriate frequency.

22.3 Enter the command TUSR. The unit will then sample the FM S-meter level, and store it in the EEPROM as the stereo level.

22.4 Enter the command TURS to see the stored level; the response on the computer should be as follows: XX (where XX is the stored level in hexadecimal form).

22.5 Reduce the RF signal level by 2dB.

22.6 Enter the command TUSM. The unit will then sample the FM S-meter level, and store it in the EEPROM as the force-mono level.

Enter the command TUMS to see the stored level; the response on the computer should be as follows: XX (where XX is the stored level in hexadecimal form).

FM S-meter voltage levels for each of these settings can be calculated as per the stops level.

22.7 Inject a 98.1MHz (US, Dual, Euro, UK and Aus) or 83.0 MHz (Japan) RF signal set to 1kHz stereo L=-R modulation with 10% pilot modulation and 75 kHz total deviation at a level of 45 dBf into J2000.

22.8 Enter the command TUSF09810 (TUSF08300 Japan units) into the computer. This will tune the unit to the appropriate frequency.

22.9 Verify that the audio output level is > 400 mVrms. On the console display, verify that the STEREO LED is lit.

22.10 Decrease the RF generator level to a level of 35 dBf into J2000.

22.11 Enter the command TUSF09810 (TUSF08300 Japan units) into the computer. This will tune the unit to the appropriate frequency.

22.12 Verify that the audio output level is < 10 mVrms. On the console display, verify that the STEREO LED is not lit.

Enter the EECS command to write the new level setting to the EEPROM before removing power.

23. FM Signal to Noise Ratio

23.1 Set the RF signal generator to 98.1 MHz (83.0 MHz Japan units), 1 kHz modulation, pilot off, 75 kHz deviation and at the level that corresponds to 65 dBf into J2000.

23.2 Measure the output level at the left or right audio output jack. Reference a dB meter to this level.

23.3 Turn off the RF modulation and verify that the level drops by > 70 dB.

Bass Module Procedures

Equipment required:

- Audio signal generator
- dB Meter
- Distortion meter
- Digital multimeter
- 2 Ohm, 50 Watt load resistor
- Bass module test cable (see instructions in the appendix)

Test Setup

Refer to Figure 11 for the following tests.

1. Unpowered Transformer Impedance Test

1.1 On the bass module, set the AC mains switch to the ON position (if applicable). For the International variation, set the voltage select switch to 115V.

1.2 Using a DMM, measure the DC resistance of the transformer at the locations shown in the table below.

Transformer	Measurement location	Reading in Ohms
US/Canada	J3 pins 1 to 2	3.14 – 4.25
Euro, UK, Aus	J4 pins 1 to 2	8.3 – 11.3
	J5 pins 1 to 2	.121 – .164
	J5 pins 4 to 5	446 – 493k
Japan	J4 pins 1 to 2	2.9 – 4.0
	J5 pins 1 to 2	.121 – .164
	J5 pins 4 to 5	446 – 493k
Dual Voltage (S2 to 230V)	J2 pins 1 to 2	8.3 – 11.3
	J5 pins 1 to 2	.113 – .139
	J5 pins 4 to 5	446 – 493k

TEST PROCEDURES

2. Woofer DC Resistance Test

2.1 Remove the bass module rear enclosure using bass module disassembly/assembly procedure 1.

2.2 Remove the woofer harness from J7 on the bass module PCB. Measure the DC resistance of the woofer voice coil by measuring across the two pins of the woofer harness. It should be 1.55 Ohms ± 15%.

3. Power Up Test

3.1 Apply a short across BASS-EQ (J6 pin 6) and AGND (J6 pin 5). Apply 0 V (open the SPST mute/un-mute switch on the bass module test cable) to MUTE (J6 pin 13).

3.2 Apply AC mains voltage to the bass module.

3.3 Measure the transformer quiescent primary current. It should be < 250 mArms.

3.4 Measure the V supply voltage at J6 pins 7, 8, 14 and 15. It should be +16.5 ± 1.0 VDC. Remove the short applied in step 3.1.

3.5 Measure the J7 speaker output DC potential on each pin of the connector relative to PGND at J6 pin 2 or 3. It should be + 8.2 ± 1.0 Vdc.

4. Gain, Distortion and Mute Tests

4.1 Unplug the woofer harness connector at J7 on the bass module PCB. Connect a 2 Ohm, 50 Watt load resistor to the bass channel output to J7 on the bass module PCB.

4.2 Apply a +5 Vdc level to MUTE at J6 pin 13 (close the SPST mute/un-mute switch on the bass module test cable). This DC level will unmute the bass module amplifier.

4.3 Apply a 100 mV, 100 Hz signal between BASS-EQ (J6 pin 6) and AGND (J6 pin 5).

4.4 Reference a dB meter to the input level.

4.5 Measure the output gain level at J7. It should be +26.0 dB ± 2.0 dB.

4.6 Measure the distortion level at J7. It should be < 0.1%.

4.7 Apply a 0 Vdc level to MUTE at J6 pin 13 (open the SPST mute/un-mute switch on the bass module test cable). This DC level will mute the bass module amplifier.

4.8 Measure the mute attenuation level at J7 relative to the input level. It should be > 40 dB.

5. Air Leak Test

5.1 Apply a 200 mVrms, 45 Hz signal between BASS-EQ (J6 pin 6) and AGND (J6 pin 5).

5.2 Listen for air leaks around all cabinet seams, joints and wire harness thru-holes. Air leaks will be heard as a hissing or sputtering noise. Repair any air leaks. All repairs must be hidden.

6. Frequency Sweep Test

6.1 Apply a 350 mVrms, 10 Hz signal between BASS-EQ (J6 pin 6) and AGND (J6 pin 5).

6.2 Sweep the input frequency from 10 Hz to 500 Hz. Listen for any extraneous noises such as buzzes, rattles, ticks, port noise or distortion.

TEST PROCEDURES

Satellite Array Procedures

Notes:
- Refer to Figure 12 for the following procedures.
- The satellite arrays are non-repairable. The grilles can be replaced using the disassembly/assembly procedures.
- Each satellite array contains two identical drivers that are wired independently. You must test each of them separately unless otherwise specified.

1. DC Resistance Test

1.1 Using a DMM, measure the DC resistance of each of the array drivers. Each should measure 3.2 Ohms ± 10%.

2. Phase Test

2.1 Remove the array grille using array disassembly procedure 1.

2.2 Observing polarity, apply a +6 Vdc level to one driver on the array input connector.

2.3 Observe the Twiddler™ under test. When the DC level is applied, the driver should move outward. If it does, the Twiddler is wired correctly. If not, it is wired incorrectly. Repeat steps 2.2 and 2.3 for the other driver in the array.

3. Air Leak Test

3.1 Apply a 180 Hz, 3 Vrms signal to one of the Twiddler drivers in the satellite array for 5 seconds minimum.

3.2 Listen for air leaks around all enclosure seams, joints and the input connector. Air leaks will be heard as a hissing or sputtering noise. Repair any air leaks. All repairs must be hidden.

3.3 Listen for any rubbing or ticking noise from the Twiddler. Replace any driver that is defective.

Note: There is a normal suspension noise. To distinguish between a rub or tick and suspension noise, displace the cone slightly with your finger. If the rubbing can be made to go away or get worse, then it is a rub or tick. If the noise stays the same, it is suspension noise.

3.4 Repeat steps 3.1 to 3.3 for the other driver in the array.

4. Frequency Sweep Test

4.1 Jumper both of the drivers in a single array together. Both center pins of the array connector are negative (-). The two outer pins are the positive (+) pins.

4.2 Apply a 100 Hz, 3.0 Vrms signal to both of the array drivers.

4.3 Slowly sweep the signal generator from 100 Hz to 2.0 kHz. Listen for any extraneous noises such as buzzes, rattles, ticks, port noise or distortion. Replace any array with an extraneous noise that can be heard at a distance greater than 1 foot (0.3m).

Console Main PCB troubleshooting

Disassembly

Remove the top cover of the console using Console Disassembly procedure 1. Use the other disassembly/assembly procedures to remove the CD/DVD mechanism. Once that is out of the way, remove the casting over the main PCB. You will need to remove the clip on the amplifier IC and to pry the amplifier IC slightly away from the heatsink before you can remove the casting. Make sure that the LCD display board is still connected for troubleshooting. You will be able to power up and troubleshoot the board while it is still in the console base with the casting and heatsink removed. Do not connect the 9 pin speaker array cable to J150. Make sure the console volume level is all the way down so that the amplifier IC U150 does not overheat when operated with no heatsink on it.

Test Cables

You will need several test cables in order to be able to troubleshoot the 3•2•1 console and bass module. This is for several reasons. The tuner adjustments for the console require the use of a TAP (test access port) cable and an IBM compatible PC. The Bose® part number for the TAP cable is 266603, and it may be ordered through Bose Product and Technical Support at 800-233-4408.

You will also need an ATAPI extender cable and an extender power cable for the DVD mechanism. These are used to allow the DVD drive to be connected to the console main PCB, yet still allow access to the PCB for troubleshooting. The console will not power up without the DVD drive connected to the main PCB.

Another test cable that is useful for troubleshooting the console is a simple DC power cable. This cable and a DC power supply will allow you to power up and troubleshoot the console without the bass module attached. The part list and instructions for making this cable are in the following pages. The bass module also requires a test cable for test and troubleshooting. This is a simple cable that can be made up using the part list and instructions on the following pages.
This cable allows you to un-mute the bass module, apply an audio input signal, and check the output of the power supply circuitry in the bass module. The bass module supplies the console with its DC voltages.

Cable Extenders

The 3•2•1 system console uses a DVD mechanism that is the same style as those used in computers. You cannot operate the console without the DVD drive connected. You will need to extend the 40 pin ATAPI cable and the power cable so that you can reach the console main PCB for troubleshooting. These parts are readily available in any electronics or computer parts store.

Extending these cables will allow you to troubleshoot the main PCB with the casting removed. Observing polarity, plug one end of the longer ATAPI cable into the main PCB. Plug the other end of the ATAPI cable into the back of the CD/DVD mechanism. Refer to Figure 8. Plug one end of the extender power supply cable into the console power supply cable. Plug the other end of the power supply cable into the power connector on the back of the CD/DVD mechanism.

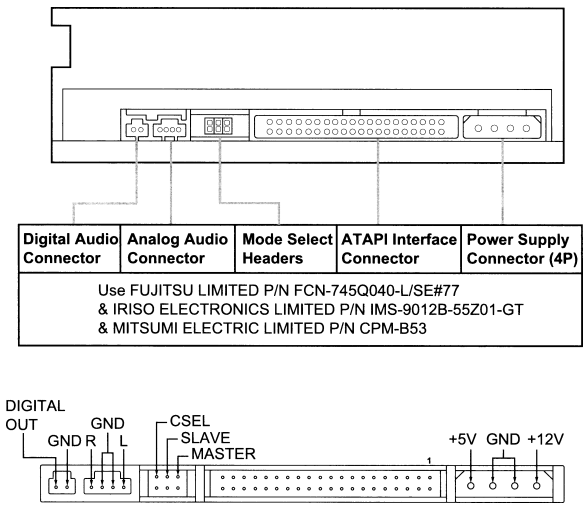


Figure 8. DVD Mechanism Rear Panel

Console Power cable

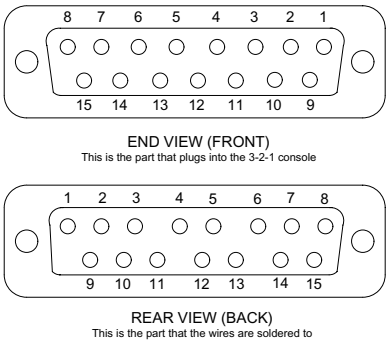
You can power up the 3•2•1 system console without the need for a bass module by making up a simple cable and using a DC power supply. The supply must be capable of putting out +15Vdc at approximately 3A.

Parts needed:

- 15 pin female subminiature D connector
- DC power supply
- 4 ft of red AWG 18 wire
- 4 ft of black AWG 18 wire

1. Twist the black and red wires together to make a twisted pair. This is to help prevent coupling noise into the console. Strip about 1/4" of insulation from one end of each of the wires.

2. On the rear of the 15 pin D-sub connector, solder the red wire to pin 7 and the black wire to pin 2. Refer to the figure below.



3. Strip about 1/2" of insulation from the other end both wires. Connect the red wire to the positive terminal and the black wire to the ground terminal of the DC power supply.

4. Plug the 15 pin D-sub connector into the rear panel of the 3-2-1 system console.

5. Turn on the DC power supply, and set the output voltage for +15Vdc.

You can now power up the 3•2•1 system console without the need for a bass module.

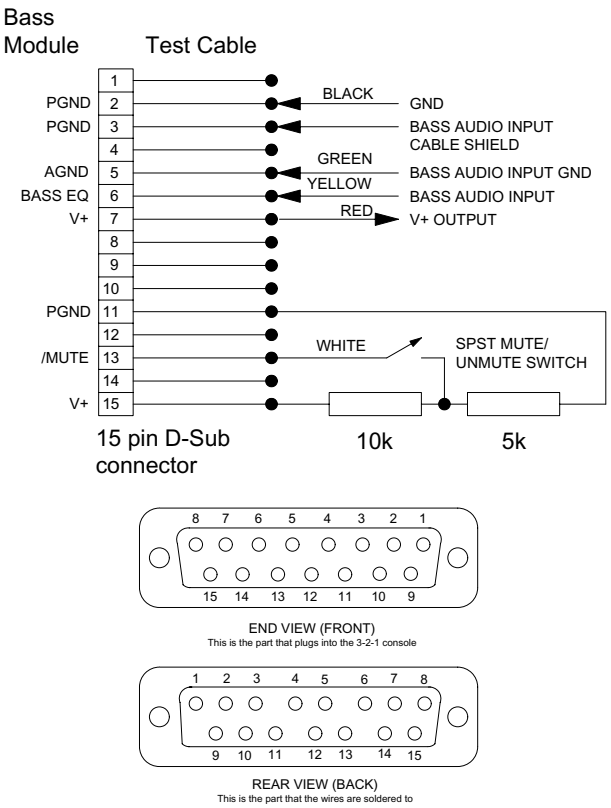


Figure 9. Bass Module Test Cable Wiring

Bass Module Test cable

You will need to be able to check the output of the bass module's power supply circuitry, as well as to input an analog audio signal to check the bass module operation. You can do this by making a simple test cable.
Note: The bass module will not un-mute without +5 Vdc on the /MUTE line at pin 13.

Parts needed:

- 1 male 15 pin subminiature D connector with solder terminals
- 1 10k Ohm, 1/4 Watt resistor
- 1 5k Ohm, 1/4 Watt resistor
- 1 ft of red AWG 18 wire
- 6 inches of black AWG 18 wire
- 4 ft of shielded twisted-pair AWG 18 wire
- 6 inches of white AWG 18 wire

Bass Module Test cable (continued)

1. Strip and tin about 1/2" of the twisted pair wires at one end of the twisted pair cable. Cut the shield back about 2" at this end. At the other end of the twisted pair cable, strip and tin about 1/4" of the twisted pair wires. Twist and tin about 1" of the shield. Solder the shield to pin 3 (PGND) of the 15 pin D-Sub connector. The shield should be grounded at the 15 pin D-Sub connector end only. This is to help prevent coupling noise into the console. Solder the positive (+) lead of the twisted pair wires to pin 6 of the 15 pin D-Sub connector. Solder the negative (-) of the twisted pair wires to pin 5 of the D-Sub connector.

2. Strip and tin about 1/4" of insulation from one end of each of the red and black wires and about 1/2" from the other ends. On the rear of the 15 pin D-sub connector, solder the red wire to pin 7 and the black wire to pin 2. The red wire at pin 7 is the +15V coming out of the bass module power supply. This voltage is also present on this connector at pins 8, 14 and 15. Be careful to not short the +15V to anything when testing. The black wire at pin 2 is connected to PGND. Pins 4, 9, 10 and 11 are also tied to PGND.

3. Twist one end of the leads of the 10k and 5k resistors together to put them in series. Strip and tin about 1/4" from both ends of the white wire. Solder one end of the white wire to the the point between the two resistors. Solder the other end of the white wire to pin 13 on the 15 pin D-Sub connector. This pin is where the +5 Vdc /MUTE input signal that normally comes from the 3-2-1 console to un-mute the bass module audio amplifier IC U1 is brought in. The bass module will not un-mute without this DC voltage level. Solder the other end of the 10k resistor to pin 15 of the D-Sub connector. Solder the other end of the 5k resistor to pin 11 of the 15 pin D-Sub connector. Solder a SPST switch in series with the white wire. This is your bass module mute/un-mute switch. When the switch is closed, you will be applying +5 Vdc to pin 13 to un-mute the bass module.

When the switch is open, you will be applying 0 Vdc to pin 13 to mute the bass module.

3•2•1 System Date of Manufacture Information

Console - The product label for the console is located on the bottom of the unit. The date of manufacture for the console is embedded in the serial number on the label. The following is an example:

Ser. No. 027748C12675109AZ

You will notice that there are four numbers underlined. This is the date of manufacture.

The way it is read is that the first digit underlined represents the year of manufacture. The 1 indicates 2001.

The next three digits are the Julian date for the day of the year. In this example that would be the 267th day of the year.

Bass Module - The date of manufacture information is embedded into the product serial number in the same format as is used for the console.

The product label for the bass module is located on the rear of the cabinet. The following is an example:

Ser. No. 027724912420677AS

You will notice that there are four numbers underlined. This is the date of manufacture.

The way it is read is that the first digit underlined represents the year of manufacture. The 1 indicates 2001.

The next three digits are the Julian date for the day of the year. In this example that would be the 242nd day of the year.

Checking Console Firmware Revisions

The 3•2•1 console uses two separate microprocessors, one located on the main PCB and another located on the display PCB.

These two versions of firmware must both be updated when an update is performed.

The revisions of firmware for each PCB must be compatible with each other. A listing of compatible revisions of each firmware will be maintained on the Bose® Service Operations web page at http://serviceops.bose.com.

If one microprocessor's firmware updated properly and the other one's didn't, then the console may fail to operate properly.

Note: Once you have successfully checked the firmware revision for either display PCB or the main PCB, you can check the other one immediately. It is not necessary to cycle the power again between tests.

Main PCB Firmware Procedure

To check the main PCB firmware from the front panel, perform the following steps:

1. Remove power from the console for at least five seconds.

2. Re-apply power, and within five seconds, press the EJECT, SKIP UP and VOLUME UP buttons all at once for at least seven seconds. You may see the display flashing during this time.

3. After seven seconds, release all of the buttons at once. You should see a display like "321 247" on the console. This example shows that version 2.47 of the main PCB firmware is installed on this particular console.

Display PCB Firmware Procedure

To check the display PCB firmware from the front panel, perform the following steps:

1. Remove power from the console for at least five seconds.

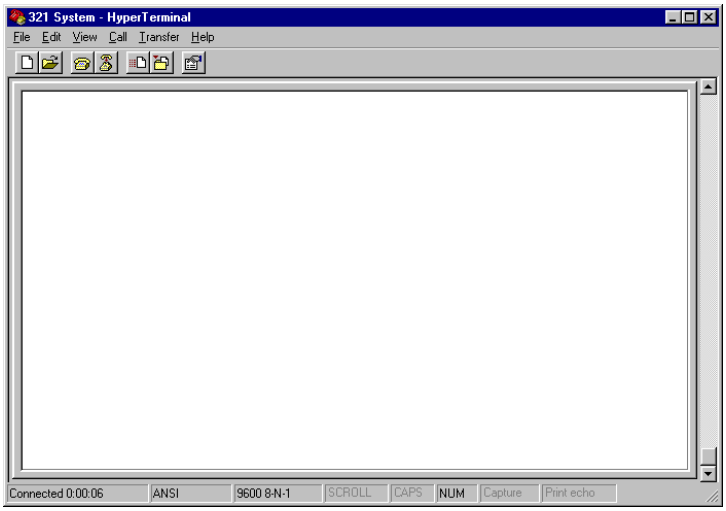
2. Re-apply power, and within five seconds, press the EJECT, SKIP UP and SOURCE DOWN buttons all at once for at least seven seconds. You may see the display flashing during this time.

3. After seven seconds, release all of the buttons at once. You should see a display like "03.52:7321" on the console. This example shows that version 3.52 of the display PCB firmware is installed on this particular console.

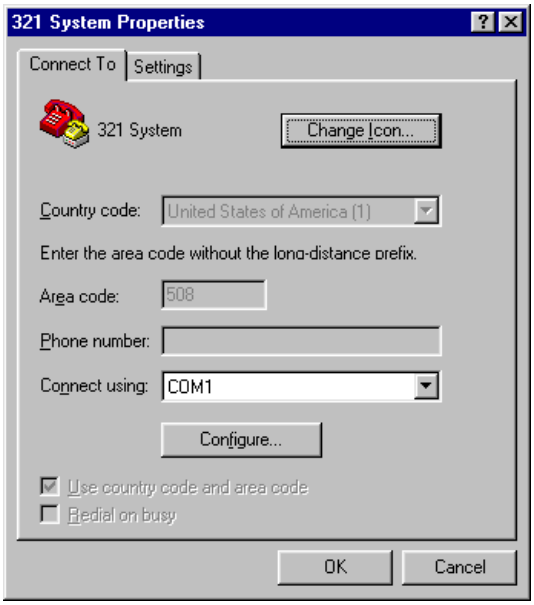
Computer Setup Procedure

Use this procedure to set up your IBM compatible PC for communication with the 3•2•1 system console.

1. Open a terminal window, as shown at right, in either Terminal or Hyperterm, as applicable for the version of Microsoft® Windows® you are using on your PC.

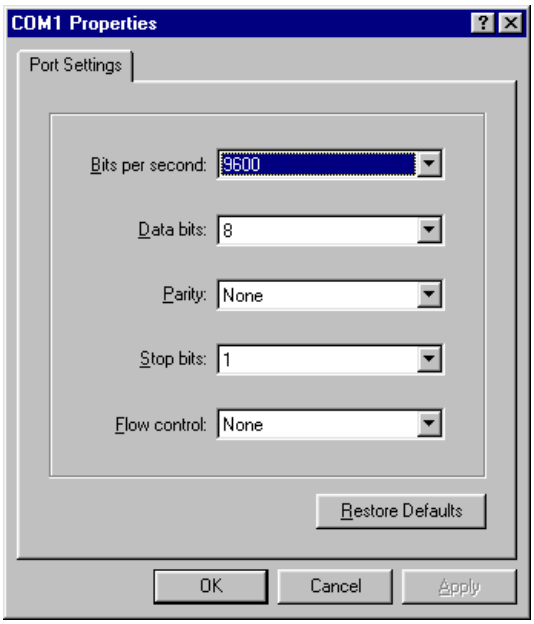


2. In the terminal window, click on FILE, then PROPERTIES. Set the properties in the dialog box as shown at right.



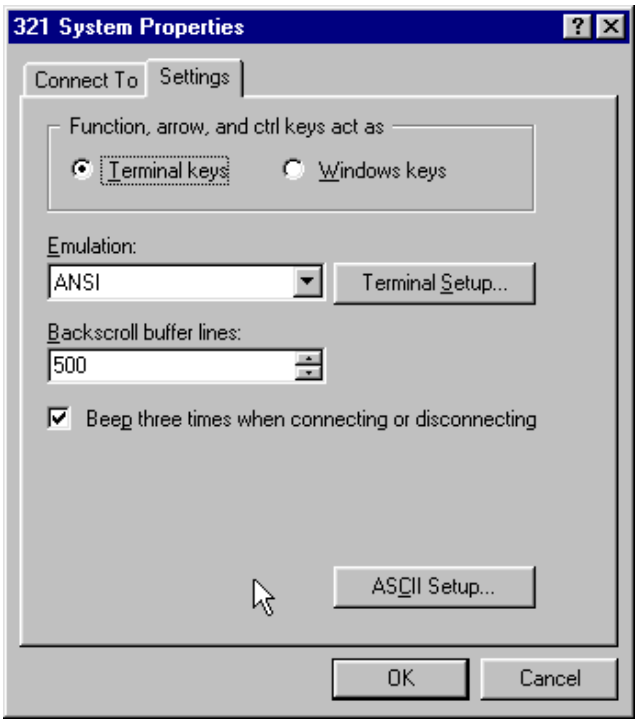
3. In the properties dialog box shown in step 2, click on CONFIGURE to set the COM1 Properties as shown at right. Click OK to return to the properties dialog box.

See the next page for the conclusion of this setup procedure.

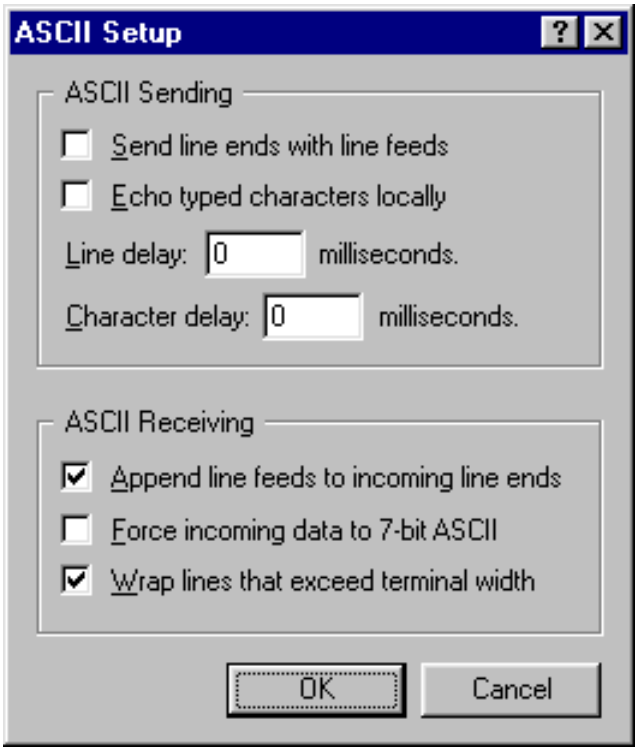


Computer Setup Procedure (continued)

4. In the properties dialog box, click on the SETTINGS tab and set the controls as shown in the example at right.
Note: Be sure to check "Beep three times when connecting or disconnecting".



5. In the properties dialog box under the SETTINGS tab, click on the ASCII Setup button and set the controls to look like the example at right. Click OK to return to the properties dialog box.



6. Once you have made all of the settings in the properties dialog box, click OK to close it. You have now configured your PC to communicate with the 3•2•1 system console. To connect to the console under test, in the terminal window, click on CALL, then CONNECT and listen for 3 beeps. This will tell you that the PC is connected to communicate with the console. When you have completed your session, click on CALL, then DISCONNECT to end communication with the console.

Console TAP Commands

The 3•2•1 console can be controlled by means of test access port (TAP) commands via the 3•2•1 system TAP cable, part number 266603, from one of the computer's serial data ports to the TAP port located on the LCD display PCB. This port can be accessed from the outside of the console without disassembling the unit. You will need the TAP cable and a RS-232 to TTL converter, such as the B+B Electronics model 232LPTTL. You can purchase the converter online at http://www.bb-elec.com.

The communication link for the TAP facility is:
Via a three wire TTL electrical interface (Transmit data, Receive data, Ground).
Logically inverted receive and transmit signals from RS-232 specification.
Same asynchronous character / timing construction as RS-232 specification requires.

The computer serial data port used for communication should be configured as follows:
Half-Duplex operation
9600 baud
8-bits / data character
1 stop bit
No parity
The console echoes all commands

Refer to the computer setup procedure earlier in this section for instructions.

There is no special action required to put the 3•2•1 console into TAP mode. Once power is applied TAP control may be used.

The 3•2•1 console does not respond to multiple commands simultaneously. The user must receive an acknowledgement (ack) prior to issuing the next TAP command.

The tables on the following pages list the TAP commands broken down into the various subsections of console functions.

TAP Commands for control of the 3•2•1 media center

Note: In the following tables, (\r) denotes carriage return, (b) denotes space, all other characters are ASCII in the cases shown.

Tuner Subsystem

Message Function	***Command from External***	***3-2-1 Response***	***Comments***
Get Tuner Region	TGTR\r	Tuner region code: nn	Returns tuner region nn. 00=US, 01=Japan, 02=Europe
Set Tuner Region	ETWR01nn\r	ACK	Sets tuner region nn. 00=US, 01=Japan, 02=Europe
Get Tuner status	TUGS\r	NEWLINE Jjkk ACK	"jj' is an ascii hex representation of the signal strength in the form of the S-meter reading. "kk" is an ascii hex representation of a byte which decodes as follows: bits 7 through 4 are not used. Bit 3 is *stereo_strong* which is 1 when the signal is above stereo threshold. Bit 2 is *in_stereo* which is 1 when in stereo mode. Bit 1 is *RDS_present* which is 1 when RDS is present. Bit 0 (LSB) is *signal_strong* which is 1 when the signal is above the stop level.
Select FM Band	TUFM\r	ACK	Subsequent Tuner functions operate on the FM band.
Set Frequency	TUSFdddds\r	(ACK) or (NACK)	NACK indicates invalid frequency mddds is an ASCII representation of frequency (without decimal point). The left-most four digits (mddd) are used for all settings except FM in Europe. 06100 is 610 kHz in AM, 10710 is 107.1 MHz in FM in the US. 10715 is 107.15 MHz in FM in Europe.
Get Frequency (AM)	TUGF\r	(ddd) or (dddd)	Frequency < =999 kHz Frequency =>1000 kHz
Get Frequency (FM US/Japan)	TUGF\r	(dd.d) or (ddd.d)	Frequency <= 99.9 MHz Frequency =>100.0 MHz
Get Frequency (FM Europe)	TUGF\r	(·dd.dd) or (ddd.dd)	Frequency <= 99.99 MHz Frequency =>100.00 MHz
Display RDS strings **Note:** This command will work on European units only.	TUDR\r	 PS data; …ssssssss PTY data; …iiii PTYN data; …tttttttt RT data; …rrrrrrrr	Returns all RDS strings. 0 to 8 characters 0 to 16 characters 0 to 8 characters 0 to 64 characters

TAP Commands for control of the 3•2•1 media center (continued)

Note: In the following tables, (\r) denotes carriage return, (b) denotes space, all other characters are ASCII in the cases shown.

Tuner Subsystem (continued)

Message Function	***Command from External***	***3-2-1 Response***	***Comments***
Seek Up	TUSP\r	(1 SACK) or (0 SNACK)	"s" is ASCII 1 if seek resulted in a station found. "s" is ASCII 0 if no station found.
Seek Down	TUSD\r	(1 SACK) or (0 SNACK)	"s" is ASCII 1 if seek resulted in a station found. "s" is ASCII 0 if no station found
Store AM stop level manually	TUATkk\r	ACK	"kk" is stop level in ASCII hex 0-0xFF.
Store FM stop level manually	TUFTkk\r	ACK	"kk" is stop level in ASCII hex 0-0xFF
Store Stereo Threshold level manually	TUSTkk\r	ACK	"kk" is threshold level in ASCII hex 0-0xFF.
Store force-mono Threshold level manually	TUMTkk\r	ACK	"kk" is threshold level in ASCII hex 0-0xFF.
Read s-meter and store as AM stop level	TUAR\r	ACK	
Read s-meter and store as FM stop level	TUFR\r	ACK	
Read s-meter and store as stereo threshold level	TUSR\r	ACK	
Read s-meter and store as force-mono threshold level.	TUMR\r	ACK	
Get AM stop level	TURA\r	kk ACK	"kk" is AM stop level in ASCII hex 00-0xFF.
Get FM stop level	TURF\r	kk ACK	"kk" is FM stop level in ASCII hex 00-0xFF.
Get stereo Threshold level	TURS\r	kk ACK	"kk" is stereo threshold level in ASCII hex 00-0xFF.
Get force-mono Threshold level	TURM\r	kk ACK	"kk" is force-mono threshold level in ASCII hex 00-0xFF.
Store IF offset –50kHz	TUI1\r	ACK	Sets IF Offset and Stores 25 kHz muliplier = - 2
Store IF offset -25kHz	TUI2\r	ACK	Sets IF Offset and Stores 25 kHz muliplier = - 1

TAP Commands for control of the 3•2•1 media center (continued)

Note: In the following tables, (\r) denotes carriage return, (b) denotes space, all other characters are ASCII in the cases shown.

Tuner Subsystem (continued)

Message Function	*Command from External*	*3-2-1 Response*	*Comments*
Store IF offset 0.00 kHz	TUI3\r	ACK	Sets IF Offset and Stores 25 kHz muliplier = 0
Store IF offset +25kHz	TUI4\r	ACK	Sets IF Offset and Stores 25 kHz muliplier = 1
Store IF offset +50kHz	TUI5\r	ACK	Sets IF Offset and Stores 25 kHz muliplier = 2
Store IF offset automatically	TUIF\r	ACK	Determines, sets and stores correct IF offset multiplier automatically.
Get IF offset multiplier	TUGI\r	TUGI·····j> ACK	"j" is an ASCII character which is the IF offset multiplier. (integer -2 to 2)

Audio Control Subsystem

Message Function	*Command from External*	*3-2-1 Response*	*Comments*
Set Volume	AUSVnn\r	(ACK) or (NACK)	"nn" hex ASCII representation of volume value to set to in 3-2-1. (00h-63h) NACK indicates invalid value. Value represents display value of volume only.
Get Volume	AUGV\r	nn ACK	"nn" hex ASCII representation of volume value.
Set Balance	AUBAnn\r	(ACK) or (NACK)	"nn" hex ASCII representation of balance value to set to in 3-2-1. (+/-9) NACK indicates invalid value.
Get Balance	AUGL\r	nn ACK	"nn" hex ASCII representation of balance value.
Set Surround	AUSSnn\r	(ACK) or (NACK)	"nn" hex ASCII representation of surround value to set to in 3-2-1. (+/-9) NACK indicates invalid value.
Get Surround	AUGS\r	nn ACK	"nn" hex ASCII representation of surround value.
Set Treble	AUSTnn\r	(ACK) or (NACK)	"nn" hex ASCII representation of treble value to set to in 3-2-1 (+/-9). NACK indicates invalid value.
Get Treble	AUGT\r	nn ACK	"nn" hex ASCII representation of treble value.
Set Bass	AUSBnn\r	(ACK) or (NACK)	"nn" hex ASCII representation of bass value to set to in 3-2-1 (+/-9). NACK indicates invalid value.
Get Bass	AUGB\r	nn ACK	"nn" hex ASCII representation of bass value.

TAP Commands for control of the 3•2•1 media center (continued)

Note: In the following tables, (\r) denotes carriage return, (b) denotes space, all other characters are ASCII in the cases shown.

LCD Display Subsystem

Message Function	***Command from External***	***3-2-1 Response***	***Comments***
Disable normal LCD output and blank LCD	LCOF\r	ACK	
Turn on all LCD segments and bright backlight	LCON\r	ACK	
Turn on LCD diagonal test pattern and dim backlight	LCPO\r	ACK	
Back-light dim.	LCBD\r	ACK	
Back-light bright.	LCBB\r	ACK	
Back-light off.	LCBF\r	ACK	

EEPROM Subsystem

Message Function	***Command from External***	***3-2-1 Response***	***Comments***
Write EEPROM data and checksums	EECS\r	ACK or NACK	Copies all data from mirror RAM to EEPROM and calculates/stores checksums. **Note:** You MUST issue this command when setting AM and FM stop levels, FM IF centering and FM stereo and force-mono threshold. Failure to do so will result in your changes being lost when power is removed.

TAP Commands for control of the 3•2•1 media center (continued)

Note: In the following tables, (\r) denotes carriage return, (b) denotes space, all other characters are ASCII in the cases shown.

Software Subsystem

Message Function	***Command from External***	***3-2-1 Response***	***Comments***
Get Main and Display firmware revisions	MMMD\r	xxxxxx yyy	xxxxxx is the main revision yyy is the display revision
Get Main Firmware Revision and Checksum	MMMN\r	MNRV321 vvv>	vvv is the version number.
Get Display Firmware Revision and Checksum	MMDY\r	DYRVrrrrcccc> ACK	rrrr is the ASCII representation of the revision. cccc is the hex checksum.
Get Disc drive region information: Firmware versions except 01.03.01 and 51.02.06	MRGN\r	MRGNaabbcc ddee>	aa-vendor reset = [0-4] bb-user change = [0-5] cc-type code = if user = [2-5] then 1 if user = 1 then 2 if user = 0 then 3 dd = region mask not set = FF Region 0 = FE Region 1 = FD Region 2 = FB Region 3 = F7 Region 4 = EF Region 5 = DF Region 6 = BF ee = rpc scheme = 01
Get Disc Drive region information: Firmware version 01.03.01 and 51.02.06	MRGN\r	MRGNrffffv	r = 1-6; DVD region code ffff = 1B06; last four characters of DVD firmware version. v = 0,1; NTSC, PAL video format.

TAP Commands for control of the 3•2•1 media center (continued)

Note: In the following tables, (\r) denotes carriage return, (b) denotes space, all other characters are ASCII in the cases shown.

DVD Backend Subsystem

Message Function	***Command from External***	***3-2-1 Response***	***Comments***
Pass DVD Backend TAP command	LXTPxx\r	ACK	"xx" are hex characters that signify Luxsonor TAP command per the following table.

DVD Backend TAP Codes (used with LXTP command above)

0x"XX"	Description
02	Test video pattern OFF.
03	Test video pattern ON.
09	Set DVD region 1
0A	Set DVD region 2
0B	Set DVD region 3
0C	Set DVD region 4
0D	Set DVD region 5
0E	Set DVD region 6
80	Set default video to NTSC
81	Set default video to PAL

TAP Commands for control of the 3•2•1 media center (continued)

Note: In the following tables, (\r) denotes carriage return, (b) denotes space, all other characters are ASCII in the cases shown.

Remote Control Simulation

Message Function	***Command from External***	***3-2-1 Response***	***Comments***
Remote control button simulation	REMTcc\r	(ACK) or (NACK)	NACK indicates invalid command. cc is the ASCII decimal representation of the specified button (supplied with leading zeroes) from the following table.

Remote Control Button Codes

Button	***Code***	***Button***	***Code***	***Button***	***Code***
K_POWER	01	K_VOLDN	16	K_SEVEN	31
K_CD	02	K_MUTE	17	K_EIGHT	32
K_AUX	03	K_STPOPEN	18	K_NINE	33
K_VID1	04	K_NAVUP	19	K_MENU	34
K_VID2	05	K_NAVDN	20	K_EXIT	35
K_AM	06	K_ENTER	21	K_REWND	36
K_FM	07	K_NAVRT	22	K_FASTFW	37
K_PSPLAY	08	K_NAVLT	23	K_PAUSE	38
K_SKIPL	09	K_ZERO	24	K_EXTRA	39
K_SKIPR	10	K_ONE	25	K_NOKEY	40
K_STOP	11	K_TWO	26	K_CDMODE	41
K_PRESETUP	12	K_THREE	27	K_REPEAT	42
K_PRESETDN	13	K_FOUR	28	ANY_MODAL	43
K_SETUP	14	K_FIVE	29		
K_VOLUP	15	K_SIX	30		

TAP Commands for control of the 3•2•1 media center (continued)

Note: In the following tables, (\r) denotes carriage return, (b) denotes space, all other characters are ASCII in the cases shown.

Audio Processing Subsystem

Message Function	***Command from External***	***3-2-1 Response***	***Comments***
Reset the audio DSP	RE\r		
Balance command	BA v\r		"v" is a value between –10 and 10.
Clip disable	CL m\r		"m" is the clip detector processing mode. It is either ON or OFF.
Set Compressor mode	CO m\r		"m" is either ON or OFF. A space toggles the mode.
Set Decoder mode	DE m\r		"m" is the mode. AC3 decodes AC3 stream, PCM decodes the PCM stream and AUTO lets the software select the decoder automatically.
Echo enable command	EC m\r		"m" is the echo mode. ON echoes the characters out the RS-232 port. OFF means no characters are sent out the RS-232 port
Mute outputs	MU c v\r		"c" specifies which channel to mute. The values are L,C,R,LS,RS,B or ALL. "v" is either ON (muted) or OFF (un-muted). All channels can be controlled individually with a comma separated string of values. The assumed order is as above.
Ooze setting	OO v\r		"v" is a value between –10 and 6.
Set presentation mode	PM mm\r		"mm" is the presentation mode. 4W is 4 axis wide, 2W is two axis wide, 4N is four axis narrow and 2N is two axis narrow.
Surround balance control	SB v\r		"v" is a value between –10 and 10.
Set Surround level	SL v\r		"v" is a value between –10 and 6.
Source select	SO c s\r		"c" is the channel specified. Choices are L,C,R,LS,RS,B. "s" is the source for the channel. Choices are D for digital, A for analog, S for 1kHz sine, DL for digital left, C for center, DR for digital right, LS for left surround, RS for right surround, LFE, AL for analog left and AR for analog right.

TAP Commands for control of the 3•2•1 media center (continued)

Note: In the following tables, (\r) denotes carriage return, (b) denotes space, all other characters are ASCII in the cases shown.

Audio Processing Subsystem (continued)

Message Function	***Command from External***	***3-2-1 Response***	***Comments***
Request status information	ST\r		Displays console status information.
Set Tone controls	TO c,v\r		"c" is the control to be changed. The controls are B (bass), T (treble) and FE (film EQ). "v" is the value to set the control to. For B and T, the value is a number between –128 and 127. For FE, the values can be: ON for Film EQ on, OFF for film EQ off, BON for bass boost from film EQ on, BOFF which turns off the film EQ bass boost, HON for HF cut from film EQ on and HOFF which turns off the film EQ HF cut.
Set volume	VO c v\r		"c" is the channel to be modified. The choices are L,C,R,LS,RS,B or ALL. "v" is the attenuation value in dB down from maximum.

Tuner S-Meter Hexidecimal to Decimal to Voltage Conversion Charts:

HEX	Decimal	S-Meter Voltage Level
0	0	0.000V
1	1	0.020V
2	2	0.039V
3	3	0.059V
4	4	0.078V
5	5	0.098V
6	6	0.117V
7	7	0.137V
8	8	0.156V
9	9	0.176V
A	10	0.195V
B	11	0.215V
C	12	0.234V
D	13	0.254V
E	14	0.273V
F	15	0.293V
10	16	0.312V
11	17	0.332V
12	18	0.352V
13	19	0.371V
14	20	0.391V
15	21	0.410V
16	22	0.430V
17	23	0.449V
18	24	0.469V
19	25	0.488V
1A	26	0.508V
1B	27	0.527V
1C	28	0.547V
1D	29	0.566V
1E	30	0.586V
1F	31	0.605V
20	32	0.625V
21	33	0.645V
22	34	0.664V
23	35	0.684V
24	36	0.703V
25	37	0.723V
26	38	0.742V
27	39	0.762V
28	40	0.781V
29	41	0.801V
2A	42	0.820V
2B	43	0.840V
2C	44	0.859V

HEX	Decimal	S-Meter Voltage Level
2D	45	0.879V
2E	46	0.898V
2F	47	0.918V
30	48	0.938V
31	49	0.957V
32	50	0.977V
33	51	0.996V
34	52	1.016V
35	53	1.035V
36	54	1.055V
37	55	1.074V
38	56	1.094V
39	57	1.113V
3A	58	1.133V
3B	59	1.152V
3C	60	1.172V
3D	61	1.191V
3E	62	1.211V
3F	63	1.230V
40	64	1.250V
41	65	1.270V
42	66	1.289V
43	67	1.309V
44	68	1.328V
45	69	1.348V
46	70	1.367V
47	71	1.387V
48	72	1.406V
49	73	1.426V
4A	74	1.445V
4B	75	1.465V
4C	76	1.484V
4D	77	1.504V
4E	78	1.523V
4F	79	1.543V
50	80	1.562V
51	81	1.582V
52	82	1.602V
53	83	1.621V
54	84	1.641V
55	85	1.660V
56	86	1.680V
57	87	1.699V
58	88	1.719V
59	89	1.738V

Tuner S-Meter Hexidecimal to Decimal to Voltage Conversion Charts (continued):

HEX	Decimal	S-Meter Voltage Level
5A	90	1.758V
5B	91	1.777V
5C	92	1.797V
5D	93	1.816V
5E	94	1.836V
5F	95	1.855V
60	96	1.875V
61	97	1.895V
62	98	1.914V
63	99	1.934V
64	100	1.953V
65	101	1.973V
66	102	1.992V
67	103	2.012V
68	104	2.031V
69	105	2.051V
6A	106	2.070V
6B	107	2.090V
6C	108	2.109V
6D	109	2.129V
6E	110	2.148V
6F	111	2.168V
70	112	2.188V
71	113	2.207V
72	114	2.227V
73	115	2.246V
74	116	2.266V
75	117	2.285V
76	118	2.305V
77	119	2.324V
78	120	2.344V
79	121	2.363V
7A	122	2.383V
7B	123	2.402V
7C	124	2.422V
7D	125	2.441V
7E	126	2.461V
7F	127	2.480V
80	128	2.500V
81	129	2.520V
82	130	2.539V
83	131	2.559V
84	132	2.578V
85	133	2.598V
86	134	2.617V
87	135	2.637V

HEX	Decimal	S-Meter Voltage Level
88	136	2.656V
89	137	2.676V
8A	138	2.695V
8B	139	2.715V
8C	140	2.734V
8D	141	2.754V
8E	142	2.773V
8F	143	2.793V
90	144	2.812V
91	145	2.832V
92	146	2.852V
93	147	2.871V
94	148	2.891V
95	149	2.910V
96	150	2.930V
97	151	2.949V
98	152	2.969V
99	153	2.988V
9A	154	3.008V
9B	155	3.027V
9C	156	3.047V
9D	157	3.066V
9E	158	3.086V
9F	159	3.105V
A0	160	3.125V
A1	161	3.145V
A2	162	3.164V
A3	163	3.184V
A4	164	3.203V
A5	165	3.223V
A6	166	3.242V
A7	167	3.262V
A8	168	3.281V
A9	169	3.301V
AA	170	3.320V
AB	171	3.340V
AC	172	3.359V
AD	173	3.379V
AE	174	3.398V
AF	175	3.418V
B0	176	3.438V
B1	177	3.457V
B2	178	3.477V
B3	179	3.496V
B4	180	3.516V
B5	181	3.535V

Tuner S-Meter Hexidecimal to Decimal to Voltage Conversion Charts (continued):

HEX	Decimal	S-Meter Voltage Level
B6	182	3.555V
B7	183	3.574V
B8	184	3.594V
B9	185	3.613V
BA	186	3.633V
BB	187	3.652V
BC	188	3.672V
BD	189	3.691V
BE	190	3.711V
BF	191	3.730V
C0	192	3.750V
C1	193	3.770V
C2	194	3.789V
C3	195	3.809V
C4	196	3.828V
C5	197	3.848V
C6	198	3.867V
C7	199	3.887V
C8	200	3.906V
C9	201	3.926V
CA	202	3.945V
CB	203	3.965V
CC	204	3.984V
CD	205	4.004V
CE	206	4.023V
CF	207	4.043V
D0	208	4.062V
D1	209	4.082V
D2	210	4.102V
D3	211	4.121V
D4	212	4.141V
D5	213	4.160V
D6	214	4.180V
D7	215	4.199V
D8	216	4.219V
D9	217	4.238V
DA	218	4.258V
DB	219	4.277V
DC	220	4.297V
DD	221	4.316V
DE	222	4.336V
DF	223	4.355V
E0	224	4.375V
E1	225	4.395V
E2	226	4.414V
E3	227	4.434V

HEX	Decimal	S-Meter Voltage Level
E4	228	4.453V
E5	229	4.473V
E6	230	4.492V
E7	231	4.512V
E8	232	4.531V
E9	233	4.551V
EA	234	4.570V
EB	235	4.590V
EC	236	4.609V
ED	237	4.629V
EE	238	4.648V
EF	239	4.668V
F0	240	4.688V
F1	241	4.707V
F2	242	4.727V
F3	243	4.746V
F4	244	4.766V
F5	245	4.785V
F6	246	4.805V
F7	247	4.824V
F8	248	4.844V
F9	249	4.863V
FA	250	4.883V
FB	251	4.902V
FC	252	4.922V
FD	253	4.941V
FE	254	4.961V
FF	255	4.980V

Console Main PCB Video Troubleshooting and Waveforms

Note: Refer to the 3•2•1 Console schematics for the following information.

The video circuitry will not operate without the 27 MHz video clock signal VDO_CLK. This signal originates at crystal Y7056 [sheet 5, B3], fed out as signal XM27HZ over to inverter U7008 [sheet 5, B1] and output as signal DX27MHZ. This clock signal is then sent over to pin 202 of the DVD decoder IC U3000 [sheet 12, B/C2]. It is fed out of U3000 as the buffered 27 MHz clock signal VDO_CLK at pin 154 [sheet 3, D6]. From there VDO_CLK is fed to the Video DAC U5000 [sheet 10, C7], input as pin 33.

The video data bitstream signals VDO-0 to VDO-7 are fed to the Video DAC from the DVD decoder IC U3000 [sheet 3, C/D6].

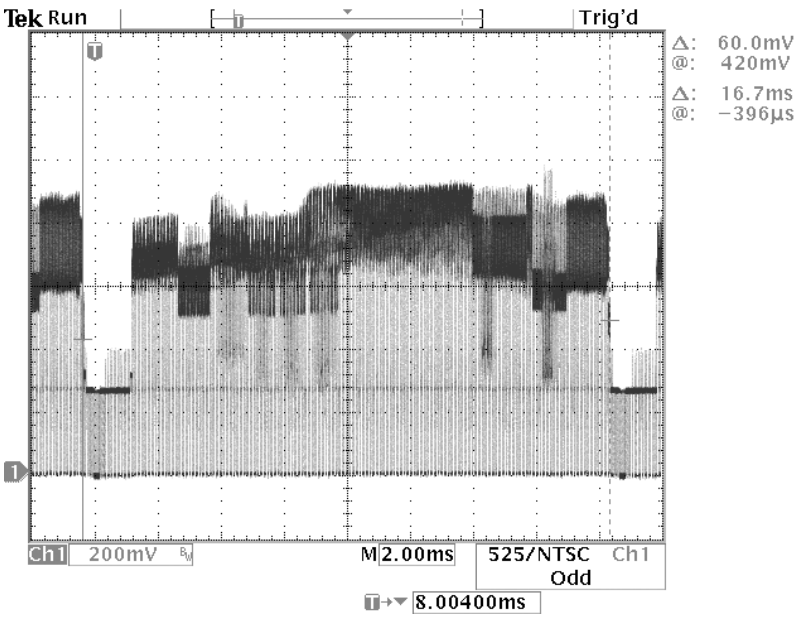
The Video DAC takes the digital video bitstreams and converts them to the formats for both the composite and S-Video outputs. Video signals are made up of Luminance (Y) information (black and white) and Chrominance (C) information (color). Both of these signals combined make up composite video (CV). S-Video uses the same signals, but keeps them separate until they sent to the video monitor, resulting in better video fidelity. Combining these two signals before the video monitor results in some overall signal degradation.

We will start by checking the waveforms coming out of the Video DAC U5000 [sheet 10, B/C/D7]. You will need a 100 MHz oscilloscope with video triggering and a DC coupled scope probe to get these waveforms.

Remove the top cover of the console, the DVD drive and the casting using the console disassembly/assembly procedures in this manual. Connect the bass module to the console using the system cable, or you can apply power using the test cable described earlier in the appendix. Do not connect the array speakers to the console.

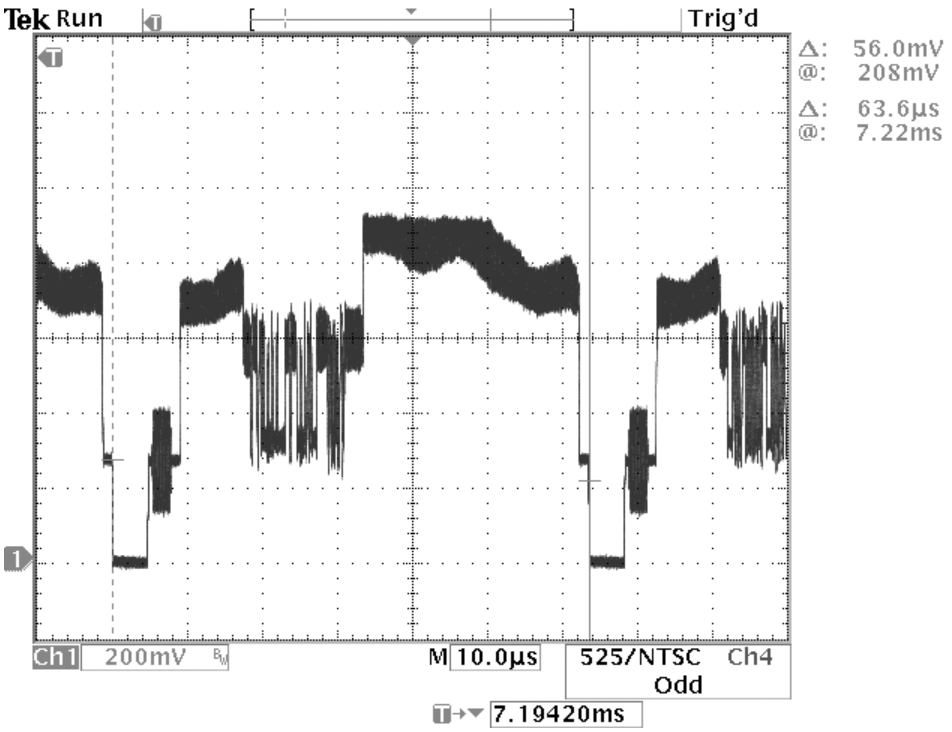
Apply power to the console and set the output volume all the way down to avoid overheating the amplifier IC. Select the AUX input and press SETTINGS. This will start the video circuitry running without the need for a DVD to be playing or a source to be plugged into the console.

We will check the composite video (CV) output of the Video DAC U5000 at pin 44 first [sheet 10, C7]. The filter network composed of inductor L5000 and associated components filter out any residual 27 MHz artifacts. The signal at TP575 should look like the wavform at right.



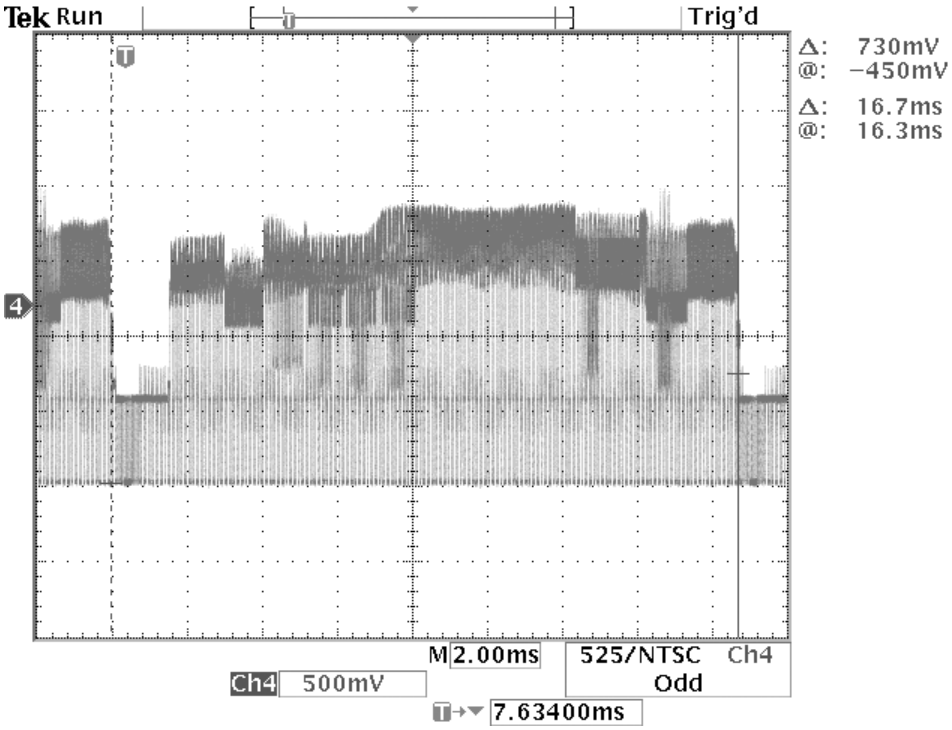
Composite Video Signal at TP575 from pin 44 of U5000

Below is the signal at TP575 again, but expanded to show the detail of the waveform.



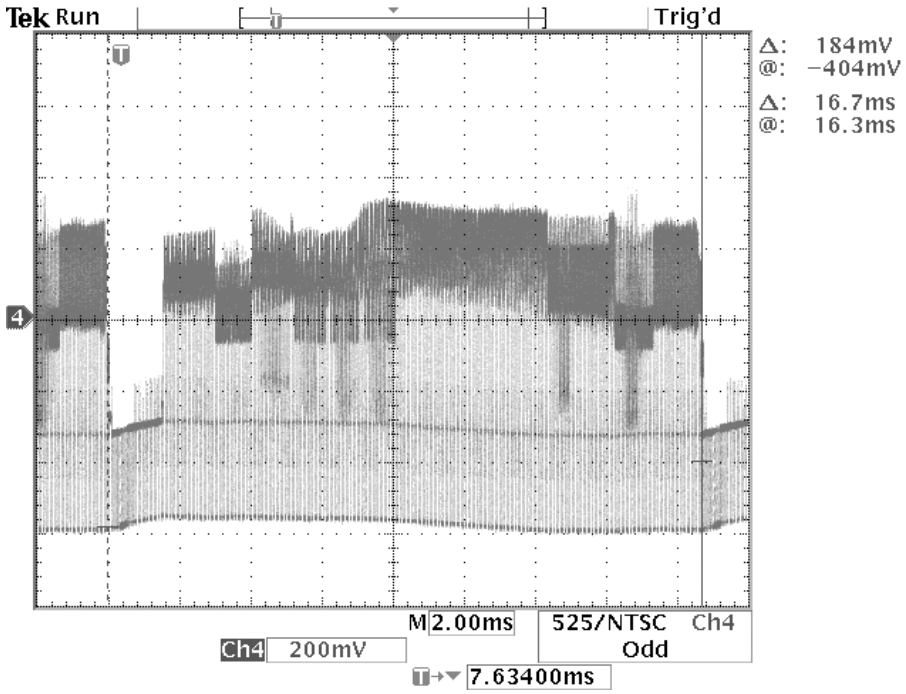
Composite Video Signal (expanded) at pin 44 of U5000

Below is the unloaded composite video (CV) signal output which originates at pin 26 of U5001, the A/V MUX located at grid coordinates [sheet 10, D1]. This waveform was taken at the composite video output RCA jack at J5001 on the console rear panel. You can also see it at TP684 on the main PCB.



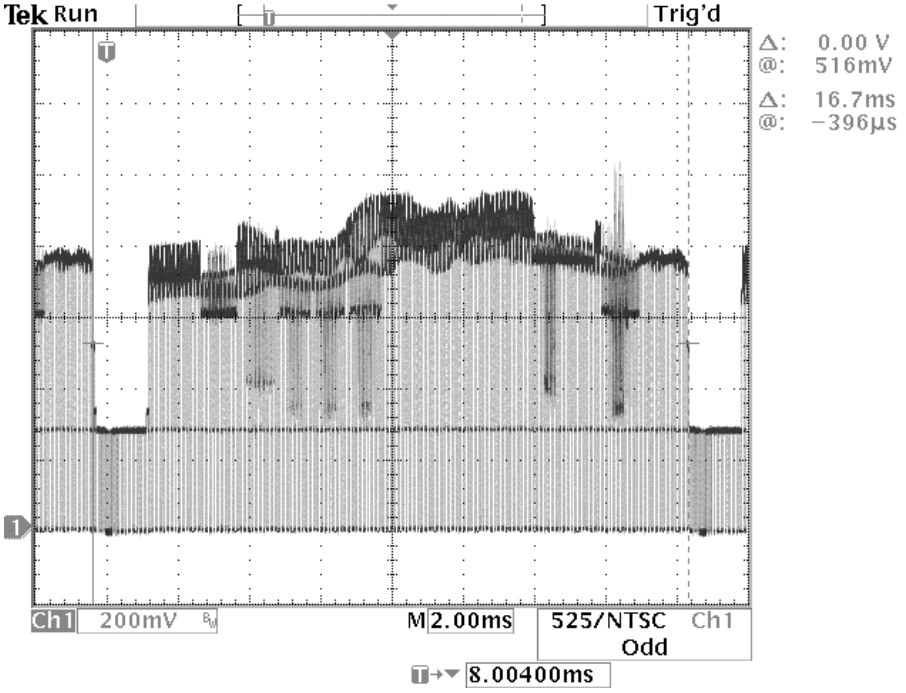
Composite Video Signal from pin 26 of U5001 (unloaded)

Below is the 75 Ohm loaded composite video (CV) signal output which originates at pin 26 of U5001, the A/V MUX located at grid coordinates [sheet 10, D1]. Note that the amplitude is about half that of the unloaded waveform on the previous page. This waveform was taken at the composite video output RCA jack at J5001 on the console rear panel.



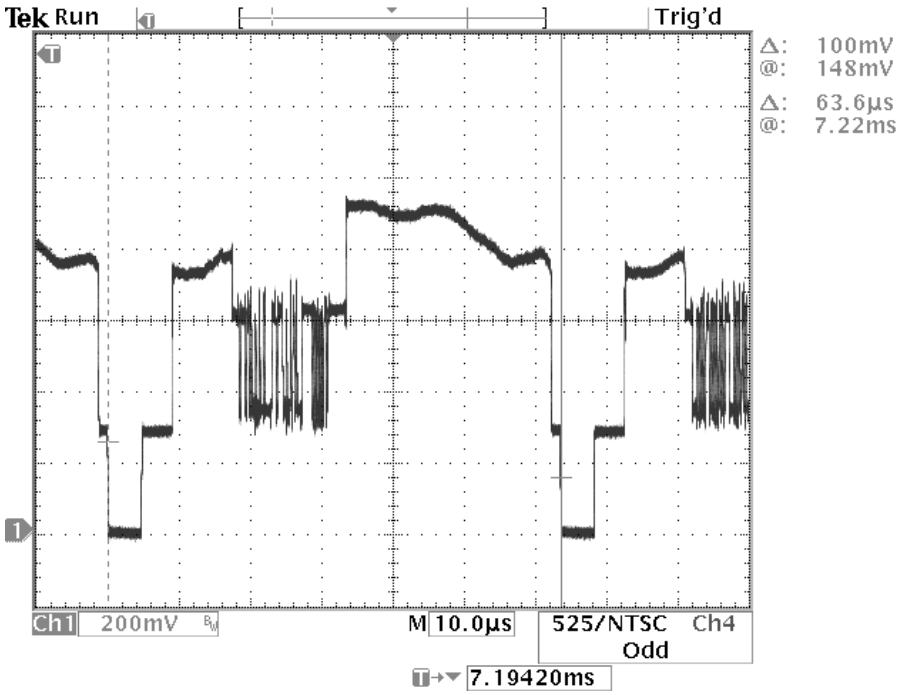
Composite Video Signal from pin 26 of U5001 (75 Ohm load)

We will now look at the signal path for the luminance (Y) video information, which is the black and white component of the S-Video signal. This waveform originates at the Video DAC U5000 at pin 48 (TP139).



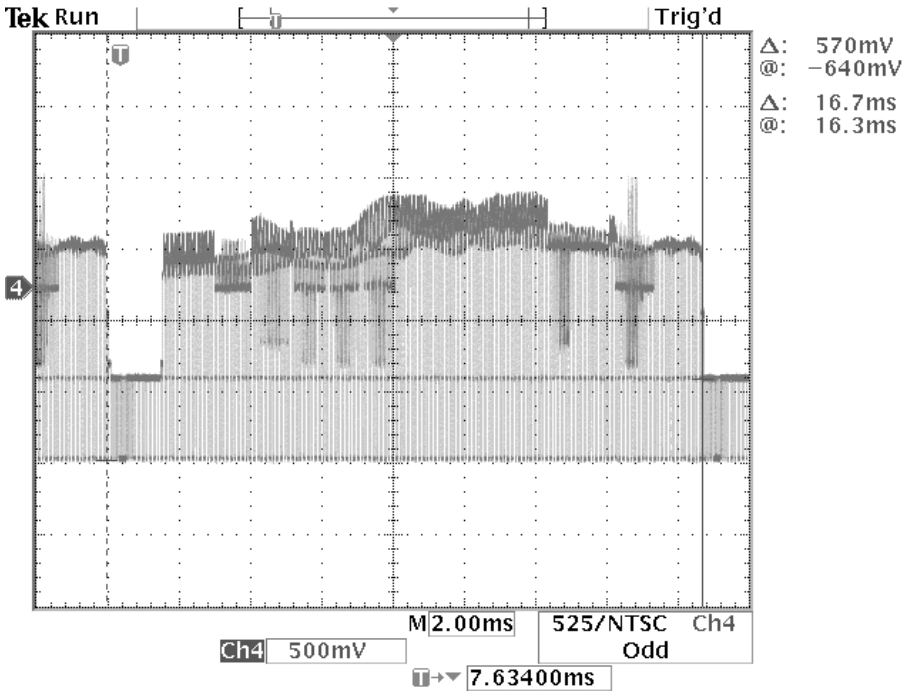
Luminance Video Signal from pin 48 of U5000

This is the same luminance (Y) video signal as the previous one, but expanded to show waveform detail. This waveform originates at the Video DAC U5000 at pin 48 (TP139).



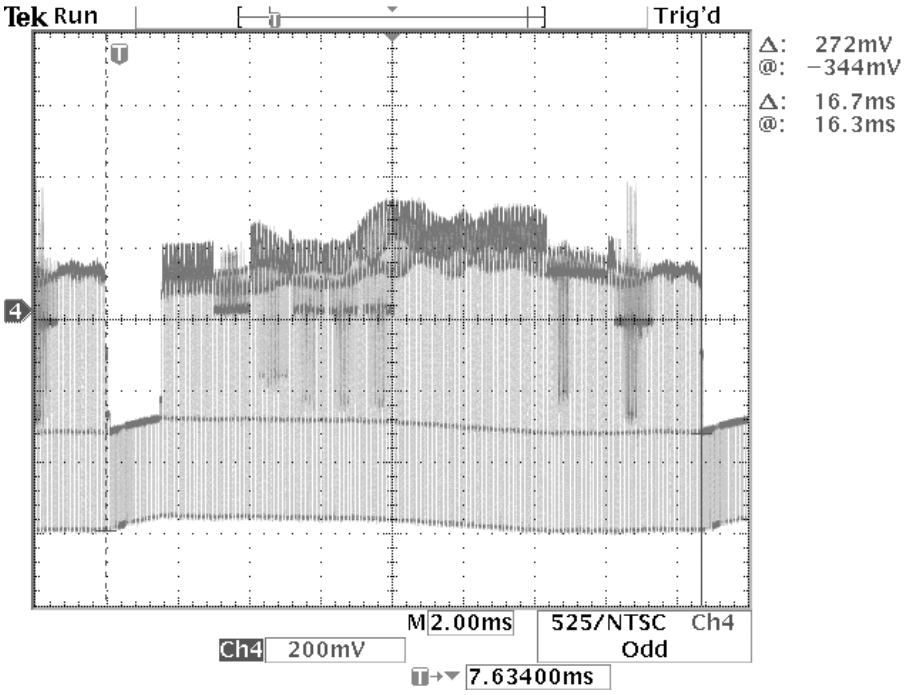
Luminance Video Signal (expanded) from pin 48 of U5000

Below is the luminance (Y) video signal as seen at pin 3 of the S-Video output DIN jack. This is with no load on the output. The signal originates at U5001 pin 22.



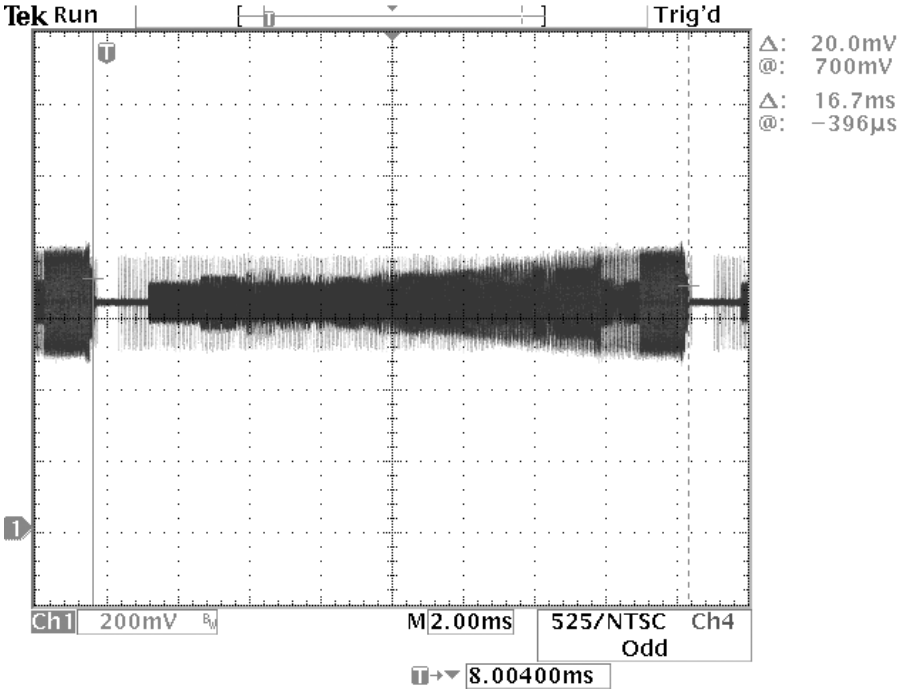
Luminance Video Signal (unloaded) S-Video DIN Connector pin 3

Below is the same luminance (Y) video signal as on the previous page, but with a 75 Ohm load. It is taken at pin 3 of the S-Video output DIN jack. Note that the waveform amplitude is about half that of the previous waveform. The signal originates at U5001 pin 22.



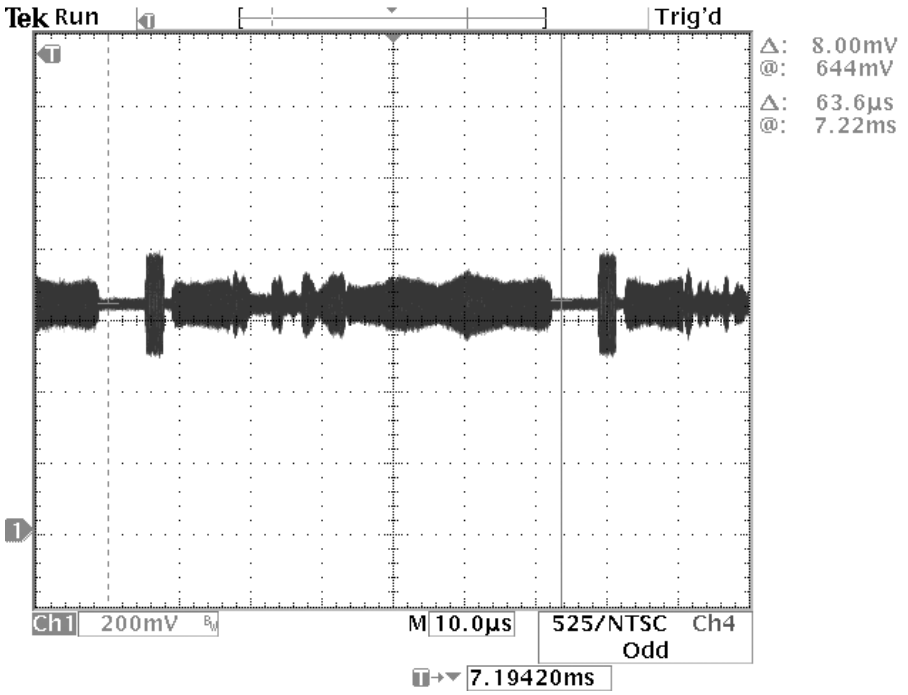
Luminance Video Signal (75 Ohm load) S-Video DIN Connector pin 3

We will now look at the signal path for the chrominance (C) video information, which is the color component of the S-Video signal. The waveform below originates at the Video DAC U5000 at pin 47 (TP516).



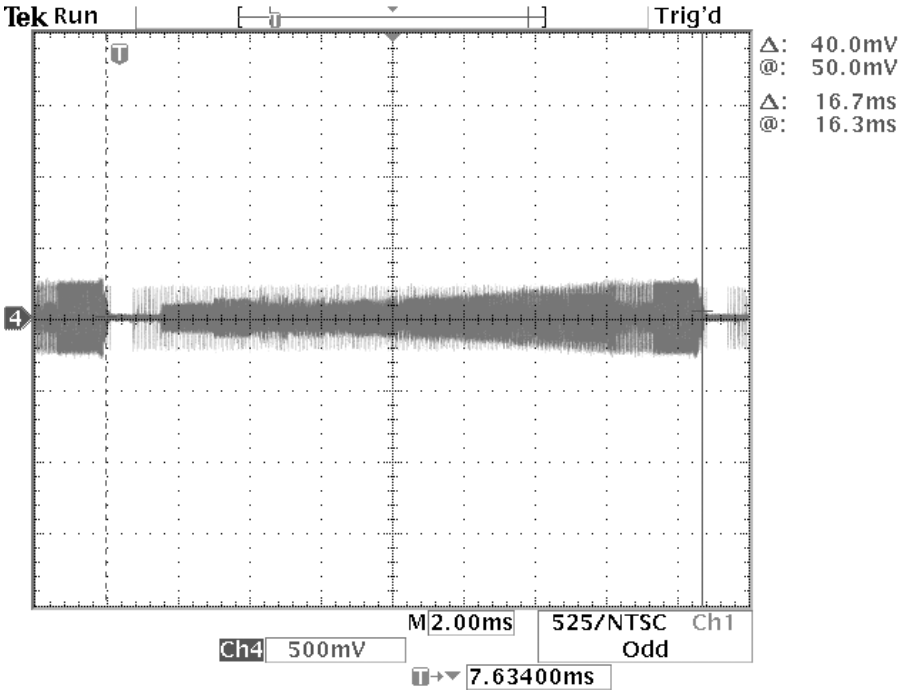
Chrominance Video Signal at U5000 pin 47 (TP516)

This is the same chrominance (C) video signal as the previous one, but expanded to show waveform detail. This waveform originates at the Video DAC U5000 at pin 47 (TP516).



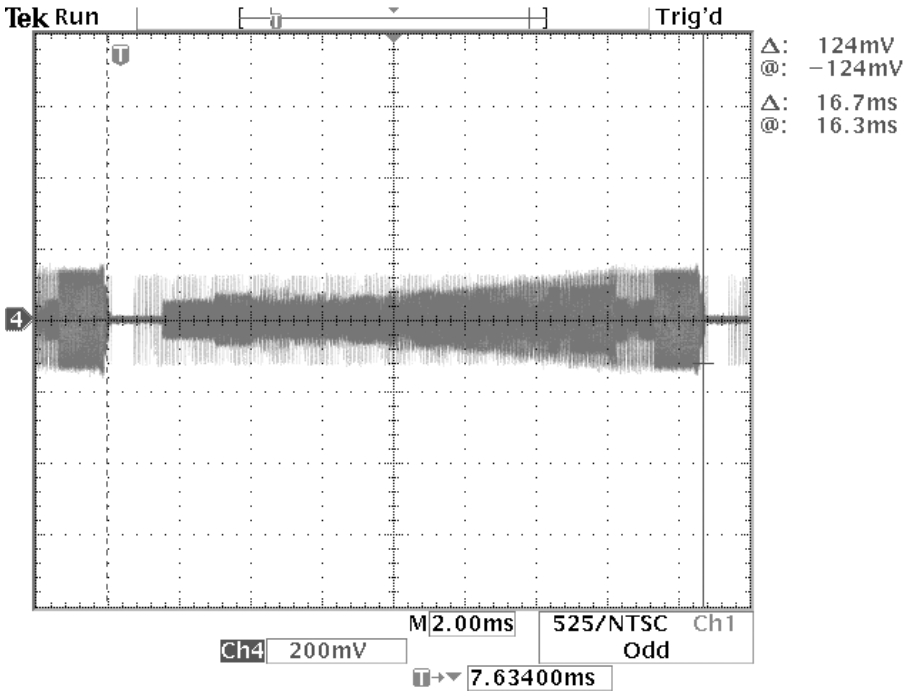
Chrominance Video Signal (expanded) at U5000 pin 47 (TP516)

Below is the chrominance (C) video signal as seen at pin 4 of the S-Video output DIN jack. This is with no load on the output. The signal originates at U5001 pin 24.



Chrominance Video Signal (unloaded) S-Video DIN Connector pin 4

Below is the same chrominance video signal (C) as on the previous page, but with a 75 Ohm load. It is taken at pin 4 of the S-Video output DIN jack. Note that the waveform amplitude is about half that of the previous waveform. The signal originates at U5001 pin 24.



Chrominance Video Signal (75 Ohm load) S-Video DIN Connector pin 4

Bass Module Troubleshooting Information

Note: Refer to the bass module amplifier board schematic sheet for the following information.

The bass module amplifier board uses two different ground potentials. When troubleshooting, be careful that you are using the correct ground (reference) point. The ground point for the power supply circuitry is at the negative (-) side of bridge BR1. When troubleshooting, be sure to reference your tests to the negative side of BR1. Be sure to float the ground on your test equipment, including your oscilloscope. You can do this by using an 3 prong to 2 prong AC adapter plug that does not have a ground pin. The ground reference used on the bass module is at a DC voltage level.

This circuitry creates the +16 VDC voltage used by the console, which is seen at the positive side of C22. The system ground point is PGND.

Common Problems:

- Q1 MOSFET shorts DRAIN to SOURCE. Rarely opens. If Q1 were to short, the symptom would be that the power supply output voltage at V (TP5) would be $\geq$ 22 Vdc. This voltage is used by the console and could cause distortion at high volume levels or the console to shut down, or both.
- Q2 and Q3 fail. PNP transistors short and open. Sometimes need to replace both at the same time instead of one at a time.
- U1 Power amplifier. TDA7396 fails.
- ZR1 16 V Zener diode fails. Zener ZR1 controls the turn on / turn off of Q2, Q3 and Q1.
- BR1 Bridge rectifier fails.

Changing the 3•2•1 Console Region Code

Note: You can only change the region code for a console a total of 4 times. After that the console will set the region code to the last one changed to permanently.

1. Connect the B+B RS-232 to TTL converter to one of the serial data ports on the back of your IBM compatible PC. Connect the TAP interface cable, part number 266603, to the B+B converter. Plug the other end of the cable into J1 of the 3-2-1 console display board. This connector can be accessed from outside the cabinet, under the right side of the front of the console.

2. Set up your computer as shown in the computer setup procedure in the appendix of this manual.

3. Power up the 3•2•1 system console. On the PC, open the terminal window that you have set up using the computer setup procedure. Open the connection between the PC and the console.

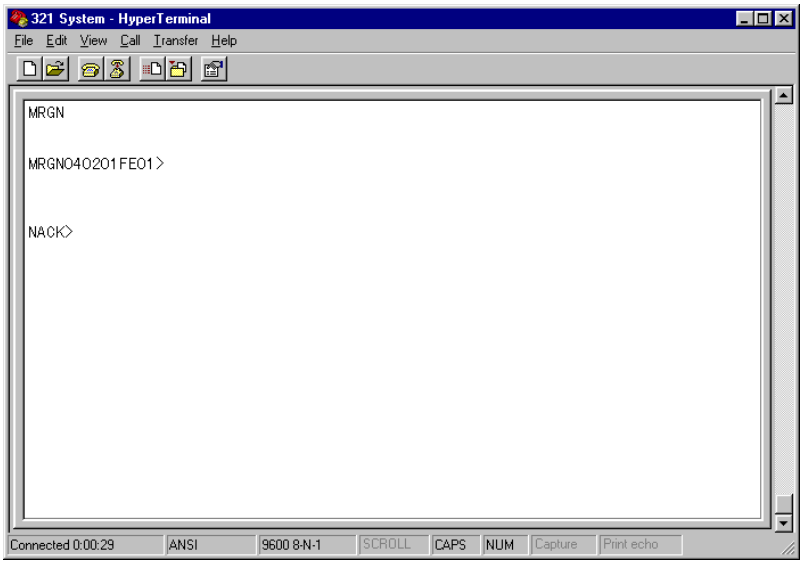
4. On the console, place a DVD disc of the region that you want to change to into the console tray. For example, if you wanted to change a region code 1 console to region 2, you would place a region code 2 DVD disc into the console. Let the disc spin up. The display will read "loading".

Changing the 3•2•1 Console Region Code (continued)

5. On the PC, type in the applicable TAP command from the table below and press ENTER on the keyboard. The region code will have changed to the new region. See the table below.

Regions Covered	Region Code	Command	MRGN Command Response
U.S., Canada, Puerto Rico	1	LXTP09	MRGN04xx01FE01
Europe, Middle East, Japan	2	LXTP0a	MRGN04xx01FD01
Southeast Asia, Hong Kong, Taiwan	3	LXTP0b	MRGN04xx01FB01
Central America, Mexico, South America, Australia, New Zealand	4	LXTP0c	MRGN04xx01F701
Russia, Africa (except Egypt and South Africa), India, Pakistan	5	LXTP0d	MRGN04xx01EF01
China	6	LXTP0e	MRGN04xx01DF01

Table 1. Region Code Tap Commands and Responses



You can check to see what region code your console is set to by typing in the MRGN command in the terminal window. The console will respond with a message similar to the one at right.

At right you will see that the console has responded MRGN040201FE01. The first two characters after the MRGN are 04, and they indicate the number of times that the drive manufacturer can reset the drive. It will almost always be 04. The next two characters are the number of times remaining that a service center can reset the region code. In this example there are two more changes (02) remaining. The next two characters (01) are the type code, which indicates the status of the drive: 00 = no drive region set; 01 = drive region set; 02 = drive region set /w additional restrictions (last chance), 03 = drive region has been set permanently. This number increments when the drive approaches the last time it can be changed before it is set permanently to the selected region. The next two characters are an eight bit hexidecimal representation of the region that the drive is currently set to. In the example, the FE corresponds to region 1. The other regions are listed in the table above. The last two characters are for the CSS encryption. For all units in the field, these two characters will always be 01.

Parental Control Information

The parental control circuitry prevents unauthorized viewing of DVDs above a user specified setting. The user is required to set a four number password for DVDs with ratings above the rating set by the user. If a user forgets what his four number password is, he/she will not be able to view movies above the set rating. If a customer has forgotten his password, there is a generic password that can be used to bypass the lock-out. The password is BOSE (2673), as spelled on a telephone. Once the original password has been bypassed, the customer can set a new one. The parental control settings used in the 3-2-1 Home Entertainment System are from 1 to 8, with 8 being the lowest security and 1 the highest. See the table below for an listing of the settings and how they correspond to the various Motion Picture Association of America (MPAA) ratings.

DVD Rating	General Description of Rating	MPAA Rating
8	Unrated (generally most restricted)	
7	Adult audiences	NC-17
6	Mature audiences	R
5	Mature teenage audiences	
4	Teenage audiences	PG-13
3	Mature young audiences	PG
2	Most audiences	
1	General (unrestricted audiences)	G

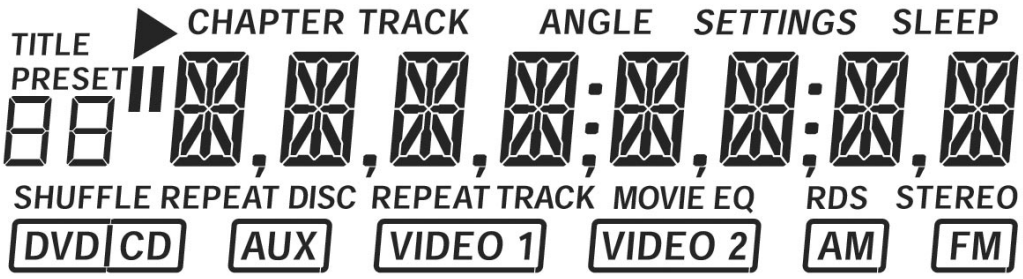
Table 2. 3•2•1 Console DVD Parental Control Rating Codes

Console Display Test

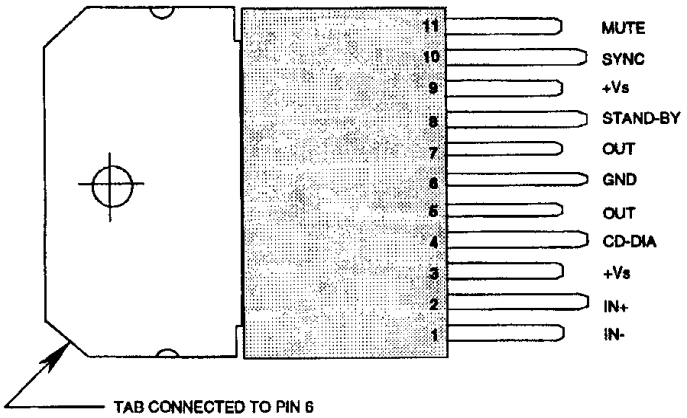
Using this procedure, you will be able to verify that all of the console LCD elements work properly by lighting all of them at once. Use the following steps.

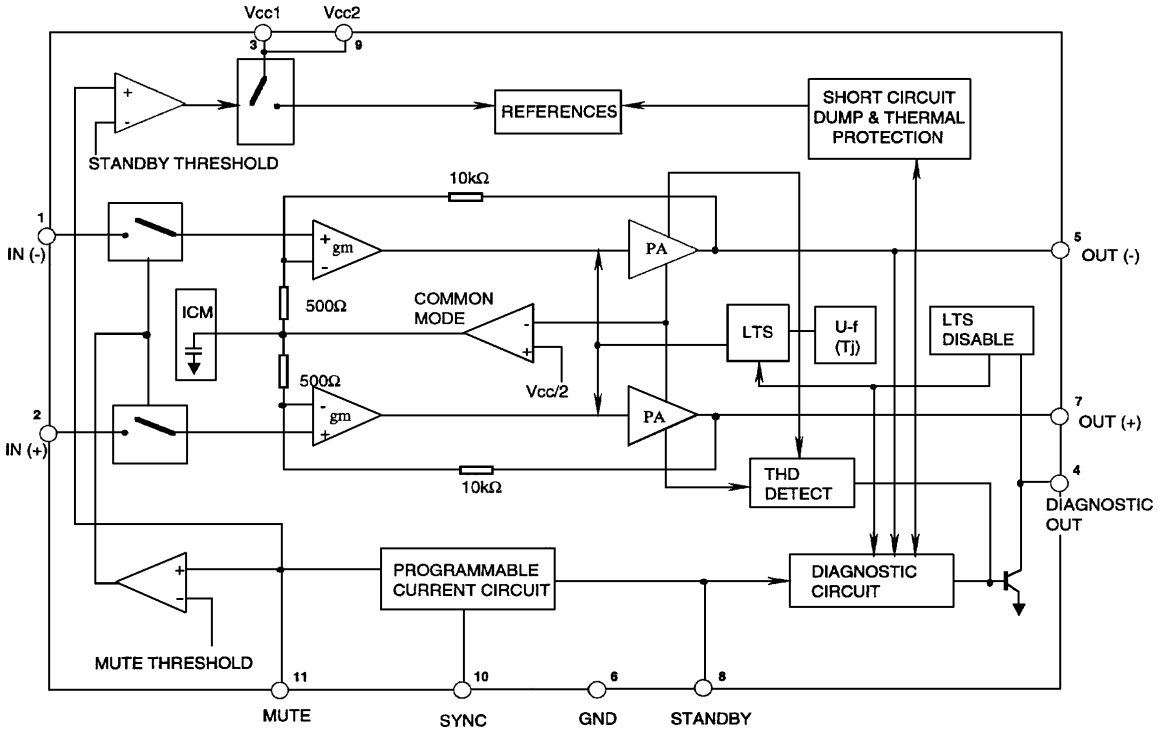
1. Remove AC mains power to the bass module.

2. Re-apply AC mains power to the bass module. Within 10 seconds of re-applying power, press the right hand three buttons on the top of the console at the same time. All of the LCD display segments should light as shown in the figure below.
Note: The RDS segment is used on European models only.

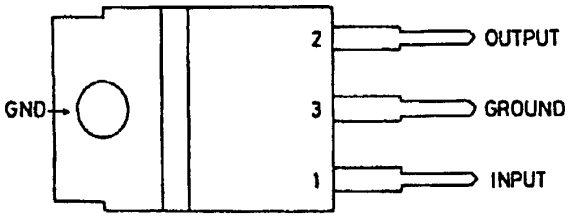


INTEGRATED CIRCUIT DIAGRAMS

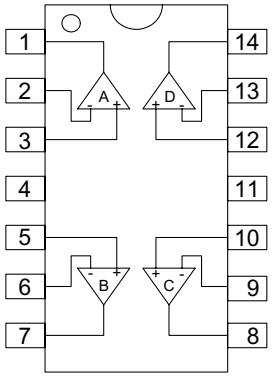




Bose® P/N: 177279, TDA 7396 Power Amplifier



Bose P/N: 178352-09, LM78M09 Regulator;
Bose P/N: 178352-10, LM78M10 Regulator

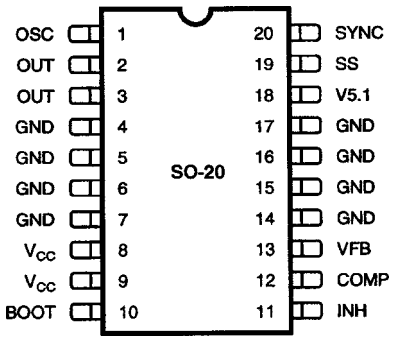


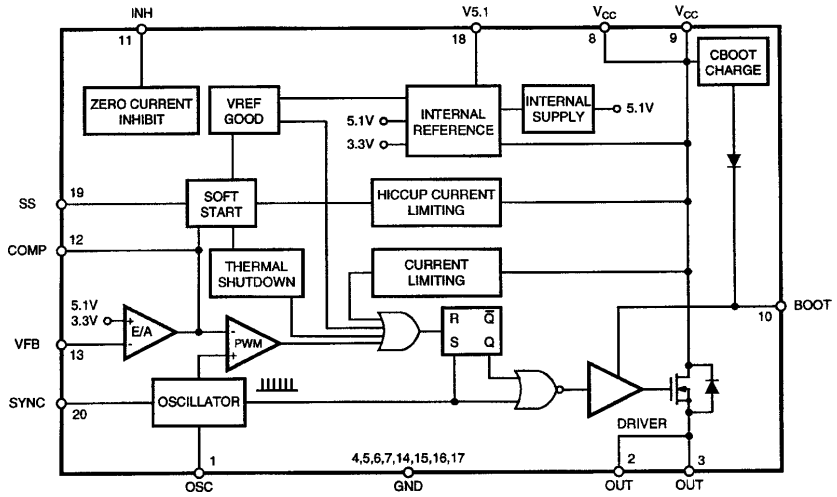
PIN FUNCTION

1. A OUTPUT
2. A -INPUT
3. A +INPUT
4. +Vcc
5. B +INPUT
6. B -INPUT
7. B OUTPUT
8. C OUTPUT
9. C -INPUT
10. C +INPUT
11. -Vcc
12. D +INPUT
13. D -INPUT
14. D OUTPUT

Bose P/N: 194024, NJM3403, Quad Op-amp

INTEGRATED CIRCUIT DIAGRAMS

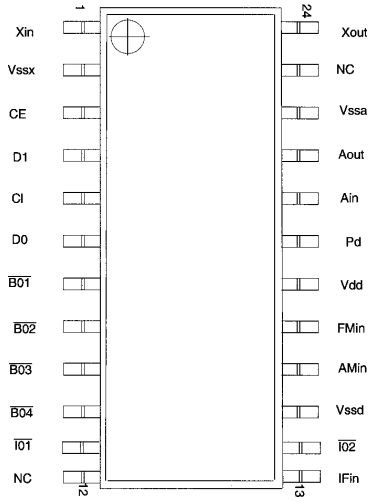


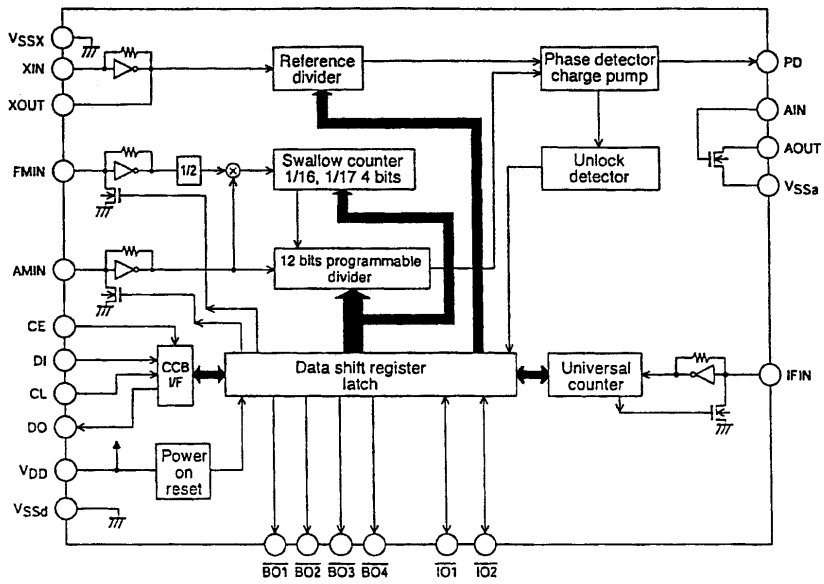


193846-001	Name	Description
12	COMP	E/A output to be used for frequency compensation
11	INH	A logic signal (active high) disables the device (sleep mode operation) if not used it must be connected to GND; if floating the device will be disabled
10	BOOT	A capacitor connected between this pin and the output will permit direct drive of the internal D-MOS.
20	SYNC	Input/Output synchronization
8,9	Vcc	Unregulated DC input voltage
2,3	OUT	Stepdown regulator output
13	VFB	Stepdown feedback input. A voltage divider is required when greater than 5.1V output levels is needed. For voltages below 3.3V the maximum power dissipation of the package must be observed.
18	V5.1	Reference voltage externally available
4,5,6,7,14,15,16, 17	GND	Signal ground
1	OSC	An external resistor connected between the unregulated input voltage and pin1 and a capacitor connected from pin1 to GND will set the switching frequency (line feed forward is automatically obtained)
19	SS	Soft start time constant. A capacitor connected between this terminal and ground determines the soft start time.

Bose® P/N: 193846-001, 3.0V Regulator

INTEGRATED CIRCUIT DIAGRAMS



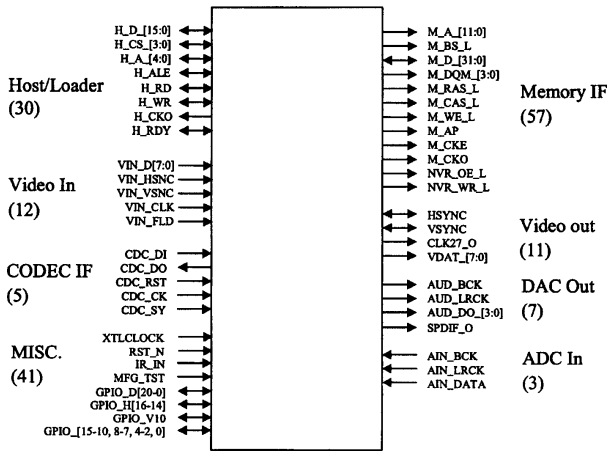


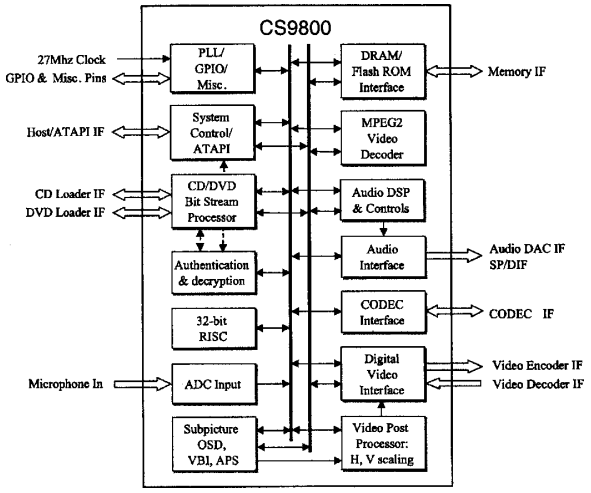
Pin name	Pin No. LC72121M	Type	Function
XIN XOUT	1 24	Xtal	• Crystal oscillator element connections (4.5 or 7.2 MHz)
FMIN	17	Local oscillator signal input	• FMIN is selected when DVS in the serial data is set to 1. • Input frequency: 10 to 160 MHz • The signal is passed through an internal divide-by-two prescaler and then input to the swallow counter. • The divisor can be set to a value in the range 272 to 65535. Since the internal divide-by-two prescaler is used, the actual divisor will be twice the set value.
AMIN	16	Local oscillator signal input	• AMIN is selected when DVS in the serial data is set to 0. • When SNS in the serial data is set to 1: • Input frequency: 2 to 40 MHz • The signal is input to the swallow counter directly. • The divisor can be set to a value in the range 272 to 65535. The set value becomes the actual divisor. • When SNS in the serial data is set to 0: • Input frequency: 0.5 to 10 MHz • The signal is input to a 12-bit programmable divider directly. • The divisor can be set to a value in the range 4 to 4095. The set value becomes the actual divisor.
CE	3	Chip enable	• This pin must be set high to enable serial data input (DI) or serial data output (DO).
DI	4	Input data	• Input for serial data transferred from the controller
CL	5	Clock	• Clock used for data synchronization for serial data input (DI) and serial data output (DO).
DO	6	Output data	• Output for serial data transmitted to the controller. The content of the data transmitted is determined by DOC0 through DOC2.
V_{DD}	18	Power supply	• LC72121 power supply (V_{DD} 2.7 to 3.6 V) • The power on reset circuit operates when power is first applied.
V_{SSX}	2	Ground	• Ground for the crystal oscillator circuit
V_{SSa}	22	Ground	• Ground for the low-pass filter MOS transistor
V_{SSd}	15	Ground	• Ground for the LC72121 digital systems other than those that use V_{SSa} or V_{SSX}.

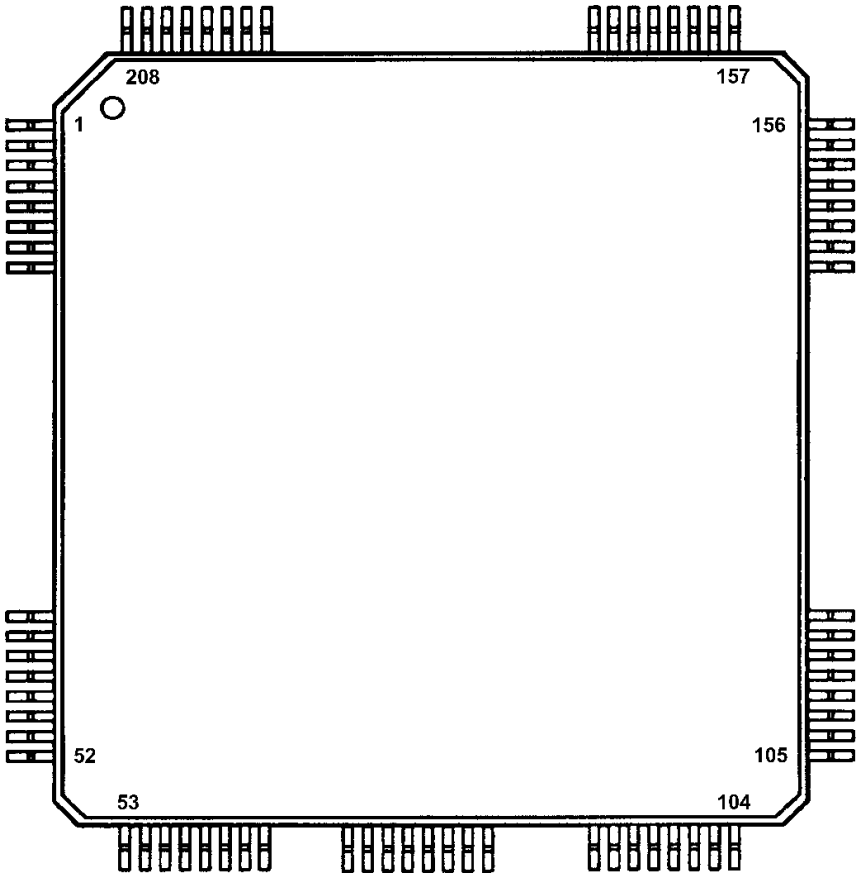
Pin name	Pin No. LC72121M	Type	Function
$\overline{IO1}$ $\overline{IO2}$	11 14	I/O port	• Shared function I/O ports • The pin function is determined by IOC1 and IOC2 in the serial data. When the data value 0: Input port When the data value 1: Output port • When specified to function as an input port: The input pin state is reported to the controller through the DO pin. When the input state is low: The data will be 0: When the input state is high: The data will be 1: • When specified to function as an output port: The output state is determined by IO1 and IO2 in the serial data. When the data value is 0: The output state will be the open circuit state. When the data value is 1: The output state will be a low level. • These pins are set to input mode after a power on reset.
$\overline{BO1}$ $\overline{BO2}$ $\overline{BO3}$ $\overline{BO4}$	7 8 9 10	Output port	• Output-only ports • The output state is determined by BO1 through BO4 in the serial data. When the data value is 0: The output state will be the open circuit state. When the data value is 1: The output state will be a low level. • A time base signal (8 Hz) is output from $\overline{BO1}$ when TBC in the serial data is set to 1.
PD	19	Charge pump output	• PLL charge pump output A high level is output when the frequency of the local oscillator signal divided by N is higher than the reference frequency, and a low level is output when that frequency is lower. This pin goes to the high-impedance state when the frequencies match.
AIN AOUT	20 21	Low-pass filter amplifier transistor	• Connections for the MOS transistor used for the PLL active low-pass filter.
IFIN	13	IF counter	• The input frequency range is 0.4 to 12 MHz • The signal is passed directly to the IF counter. • The result is output, MSB first, through the DO pin. • Four measurement periods are supported: 4, 8, 32, and 64 ms.
NC	12 23	NC pin	• No connection

Bose® P/N: 199693, PLL Frequency Synthesizer, MPF-24

INTEGRATED CIRCUIT DIAGRAMS







Bose® P/N: 254107-001, DVD Decoder, CS98000

Pin	Signal Name	Type	Description
87, 83, 79, 76, 74, 71, 68, 64, 67, 70, 72, 75, 78, 80, 86, 88, 60, 56, 54, 49, 46, 44, 40, 33, 37, 42, 45, 48, 51, 55, 59. 62	M_D[31..0]	B	Memory Data Bus. CS98000 can use all 32 bits or can use only M_D[15..0], in which case M_D[31..16] can be left un-connected.
2, 3, 5, 6, 7, 9, 10, 11, 13, 14, 15, 16	M_A[11..0]	O	Memory Address Bus. Connect in order starting with M_A[0] to all RAM address pins not already connected to M_BS_L or M_AP. Unused upper M_A pins unconnected.
19	M_CKO	O	Memory Clock
22	M_CKE	O	Memory Clock Enable
21	M_BS_L	O	Bank Selection. Always connect to RAM BS or BS0 pin.
23	M_AP	O	Memory Auto Pre-charge. Always connect to RAM AP pin.
24	M_RAS_L	O	Memory Row Address Strobe
25	M_CAS_L	O	Memory Column Address Strobe
27	M_WE_L	O	Memory Write Enable
32, 31, 29, 28	M_DQM[3..0]	O	IO Mask of Data Bus M_DQM[3] -> M_D[31:24]

SDRAM Interface

Pin	Signal Name	Type	Description
60, 56, 54, 49, 46, 44, 40, 33, 37, 42, 45, 48, 51, 55, 59. 62	M_D[15..0]	B	Memory Data Bus. Use M_D[7:0] for 8-bit interface
2, 3, 5, 6, 7, 9, 10, 11, 13, 14, 15, 16	M_A[11..0]	O	Memory Address Bus[11..0]
74, 71, 68, 64, 67, 70, 72, 75, 78, 80, 86, 88	M_D[27..16]	O	Memory Address Bus[23..12] For 16-bit data mode, M_D[26:16] is upper word address. For 8-bit data mode, M_D[27:16] is upper byte address.
83	M_D[30]	O	Address decode low. Copy of address MSB.
87	M_D[31]	O	Address decode high. Compliment of address MSB.
60	NVM_WE_L	O	NVRAM Write Enable.
62	NVM_OE_L	O	ROM/NVRAM Output Enable.

ROM/NVRAM Interface

Pin	Signal Name	Type	Description
154	CLK27_O	O	27 Mhz Clock Output.
159	HSYNC	B	Horizontal Sync. Output when the CS98000 is the video master, input when the video encoder is master.
162	VSYNC	B	Vertical Sync. Output when the CS98000 is the video master, input when the video encoder is master.
173, 172, 170, 169, 167, 166, 165, 163	VDAT[7..0]	O	Video Data Output[7..0] in Cb,Y,Cr,Y format.

Video Output Interface

Pin	Signal Name	Type	Description
145	VIN_CLK	I	Video Input Clock.
153	VIN_VSNC	I	Video Input Vertical Sync.
160	VIN_HSNC	I	Video Input Horizontal Sync.
207	VIN_FLD	I	Video Input Clock.
198, 193, 189, 184, 179, 175, 168, 164	VIN_D [7..0]	I	Video Data Input[7..0] in Cb,Y,Cr,Y format.

Video Input Interface

Pin	Signal Name	Type	Description
191	AUD_XCLK	B	Audio 256x/384x Clock input or output to Serial DAC. When output, is generated from CS98000 internal PLL.
124	AUD_BCK	O	Audio Bit Clock output to serial DAC.
128	AUD_LRCK	O	Audio Out Left/Right Clock to serial DAC.
135	AUD_DO_0	O	Audio Serial Data Out[0].
136	AUD_DO_1	O	Audio Serial Data Out[1].
133	AUD_DO_2	O	Audio Serial Data Out[2].
177	AUD_DO_3	O	Audio Serial Data Out[3].
204	SPDIF_O	O	S/PDIF Output
137	AIN_BCK	I	Audio Input Bit Clock. The CS98000 can be programmed to use the Audio Output function's internally generated bit clock, in which case this pin is not required.
139	AIN_LRCK	I	Audio Input Left/Right Clock. The CS98000 can be programmed to use the Audio Output function's internally generated LR clock, in which case this pin is not required.
140	AIN_DATA	I	Audio Input Data from Serial ADC.

Audio Output Interface

Pin	Signal Name	Type	Description
142	CDC_DI	I	Serial Data Input from Modem CODEC
144	CDC_DO	O	Serial Data Output to Modem CODEC
146	CDC_RST	O	Reset Output to Modem CODEC
147	CDC_CK	I	Serial Bit Clock input from Modem CODEC
148	CDC_SY	B	Frame Sync, output when CS98000 is master, input when CODEC is master.

AC97/CODEC Interface

Pin	Signal Name	Type	Description
111, 115, 101, 106	H_CS[3..0]	O	Host Chip Select[3..0]. The host master can be programmed to use a different protocol for each of the 4 chip selects
85	H_ALE	O	Host address latch enable. Used for modes which multiplex upper address information onto the data lines
92	H_RD	O	Host Read Request.
93	H_WR	O	Host Write Request.
95	H_RDY	I	Host Ready. Connect to pull-up or pull-down if host is not used.
120	H_CKO	O	Host clock out, required for some synchronous slaves
102, 107, 97, 99, 100	H_A[4..0]	O	Host Address[4..0].
109, 110, 112, 113, 114, 116, 117, 118, 121, 122, 123, 125, 127, 130, 132, 134	H_D[15..0]	B	Host Data Bus[15..0]. These pins can also output Host Address during the address phase for multiplexed address/data mode. Tie together to pull-up or pull-down if host is not used.

Host Master Interface

Pin	Signal Name	Type	Description
121, 122, 123, 125, 127, 130, 132, 134	H_D[7:0]	I	DVD_Data[7:0] – DVD data port parallel data input from loader
118	H_D[8]	O	Control port clock to loader
117	H_D[9]	I	Control port ready signal from loader
116	H_D[10]	O	Control port serial command to loader
114	H_D[11]	I	Control port serial status from loader
113	H_D[12]	I	CD error signal from loader
112	H_D[13]	I	CD clock from loader
110	H_D[14]	I	CD left/right clock from loader
109	H_D[15]	I	CD serial data from loader
106	H_CS_0	I	DVD data start sector signal from loader
101	H_CS_1	I	DVD data error signal from loader
95	H_RDY	O	DVD data ready signal to loader
93	H_WR	I	DVD data enable signal from loader
92	H_RD	I	DVD data clock from loader

DVD I/O Channel Interface

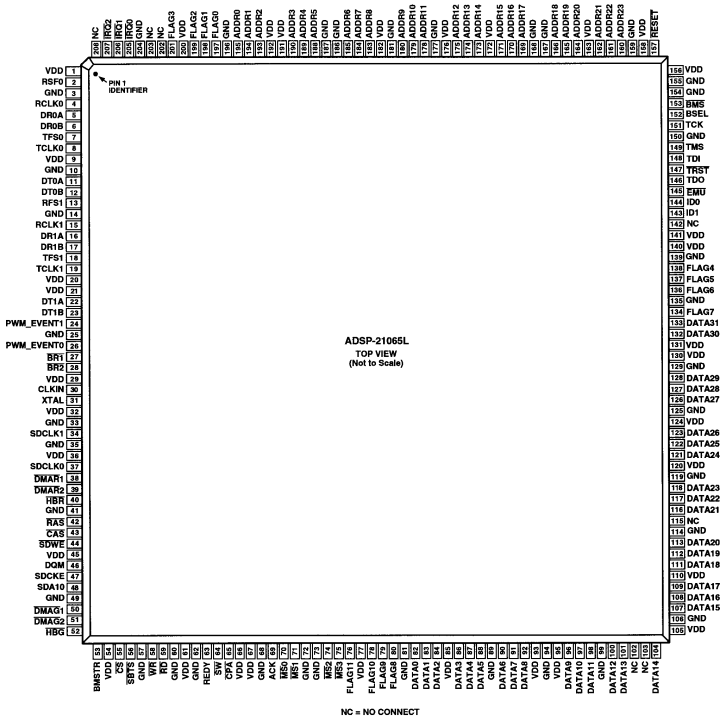
Pin	Signal Name	Type	Description
26,17,4,12,8, 150, 151, 152, 155, 65, 69, 73, 77, 61, 57, 50, 47, 43, 39, 34, 30	GPIO_D[20:0]	B	21 General purpose I/O's
98, 94, 89	GPIO_H[16:14]	B	3 General purpose I/O's
149	GPIO_V10	B	General purpose I/O
199, 197, 196, 195, 194, 192	GPIO_[15:10]	B	6 General purpose I/O's
190, 188	GPIO_[8:7]	B	2 General purpose I/O's
195, 183, 181	GPIO_[4:2]	B	3 General purpose I/O's
174	GPIO_0	B	General purpose I/O

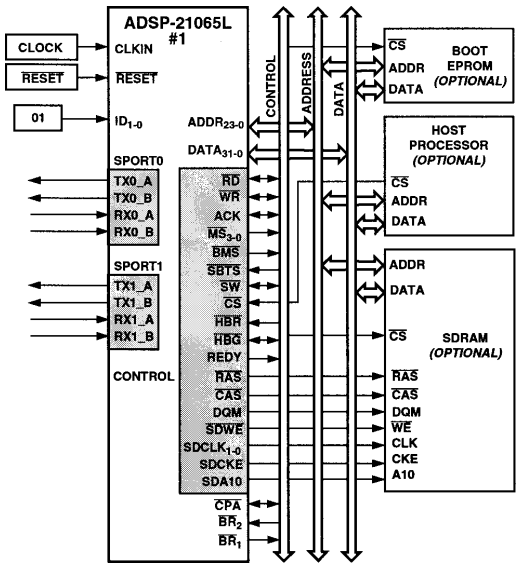
General Purpose I/O Interface

Pin	Signal Name	Type	Description
1, 105, 158	VDD_PLL		2.5V for internal PLLs
41, 66, 84, 108, 129, 141, 161, 178, 203	VDD_CORE		2.5V for internal core logic
20, 38, 91, 131, 180	VDD_IO		3.3V for I/O's
104, 157, 208	VSS_PLL		Ground for internal PLLs
36, 63, 82, 103, 126, 138, 158, 176, 200	VSS_CORE		Ground for internal core logic
18, 35, 58, 96, 119, 143, 182	VSS_IO		Ground for I/O's

Power and Ground

INTEGRATED CIRCUIT DIAGRAMS





Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VDD	43	$\overline{\text{CAS}}$	85	VDD	127	DATA28	169	ADDR17
2	RFS0	44	$\overline{\text{SDWE}}$	86	DATA3	128	DATA29	170	ADDR16
3	GND	45	VDD	87	DATA4	129	GND	171	ADDR15
4	RCLK0	46	DQM	88	DATA5	130	VDD	172	VDD
5	DR0A	47	SDCKE	89	GND	131	VDD	173	ADDR14
6	DR0B	48	SDA10	90	DATA6	132	DATA30	174	ADDR13
7	TFS0	49	GND	91	DATA7	133	DATA31	175	ADDR12
8	TCLK0	50	$\overline{\text{DMAG1}}$	92	DATA8	134	FLAG7	176	VDD
9	VDD	51	$\overline{\text{DMAG2}}$	93	VDD	135	GND	177	GND
10	GND	52	$\overline{\text{HBG}}$	94	GND	136	FLAG6	178	ADDR11
11	DT0A	53	BMSTR	95	VDD	137	FLAG5	179	ADDR10
12	DT0B	54	VDD	96	DATA9	138	FLAG4	180	ADDR9
13	RFS1	55	$\overline{\text{CS}}$	97	DATA10	139	GND	181	GND
14	GND	56	$\overline{\text{SBTS}}$	98	DATA11	140	VDD	182	VDD
15	RCLK1	57	GND	99	GND	141	VDD	183	ADDR8
16	DR1A	58	$\overline{\text{WR}}$	100	DATA12	142	NC	184	ADDR7
17	DR1B	59	$\overline{\text{RD}}$	101	DATA13	143	ID1	185	ADDR6
18	TFS1	60	GND	102	NC	144	ID0	186	GND
19	TCLK1	61	VDD	103	NC	145	$\overline{\text{EMU}}$	187	GND
20	VDD	62	GND	104	DATA14	146	TDO	188	ADDR5
21	VDD	63	REDY	105	VDD	147	$\overline{\text{TRST}}$	189	ADDR4
22	DT1A	64	$\overline{\text{SW}}$	106	GND	148	TDI	190	ADDR3
23	DT1B	65	$\overline{\text{CPA}}$	107	DATA15	149	TMS	191	VDD
24	PWM_EVENT1	66	VDD	108	DATA16	150	GND	192	VDD
25	GND	67	VDD	109	DATA17	151	TCK	193	ADDR2
26	PWM_EVENT0	68	GND	110	VDD	152	BSEL	194	ADDR1
27	$\overline{\text{BR1}}$	69	ACK	111	DATA18	153	$\overline{\text{BMS}}$	195	ADDR0
28	$\overline{\text{BR2}}$	70	$\overline{\text{MS0}}$	112	DATA19	154	GND	196	GND
29	VDD	71	$\overline{\text{MS1}}$	113	DATA20	155	GND	197	FLAG0
30	CLKIN	72	GND	114	GND	156	VDD	198	FLAG1
31	XTAL	73	GND	115	NC	157	$\overline{\text{RESET}}$	199	FLAG2
32	VDD	74	$\overline{\text{MS2}}$	116	DATA21	158	VDD	200	VDD
33	GND	75	$\overline{\text{MS3}}$	117	DATA22	159	GND	201	FLAG3
34	SDCLK1	76	FLAG11	118	DATA23	160	ADDR23	202	NC
35	GND	77	VDD	119	GND	161	ADDR22	203	NC
36	VDD	78	FLAG10	120	VDD	162	ADDR21	204	GND
37	SDCLK0	79	FLAG9	121	DATA24	163	VDD	205	$\overline{\text{IRQ0}}$
38	$\overline{\text{DMAR1}}$	80	FLAG8	122	DATA25	164	ADDR20	206	$\overline{\text{IRQ1}}$
39	$\overline{\text{DMAR2}}$	81	GND	123	DATA26	165	ADDR19	207	$\overline{\text{IRQ2}}$
40	$\overline{\text{HBR}}$	82	DATA0	124	VDD	166	ADDR18	208	NC
41	GND	83	DATA1	125	GND	167	GND		
42	$\overline{\text{RAS}}$	84	DATA2	126	DATA27	168	GND		

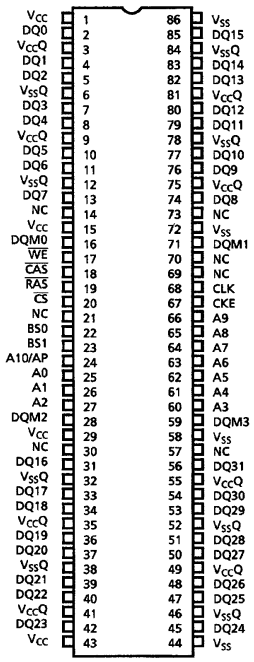
Bose® P/N: 254191, DSP, ADSP21065LKS

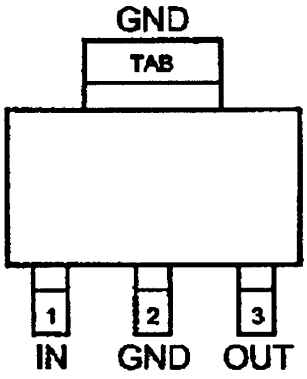
INTEGRATED CIRCUIT DIAGRAMS

PIN NAMES

A0~A10	Address
BS0, BS1	Bank Select
DQ0~DQ31	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0~3	Output disable/Write Mask
CLK	Clock inputs
CKE	Clock enable
V_{CC}	Power (+3.3V)
V_{SS}	Ground
$V_{CC}Q$	Power (+3.3V) (for I/O buffer)
$V_{SS}Q$	Ground (for I/O buffer)
NC	No Connection

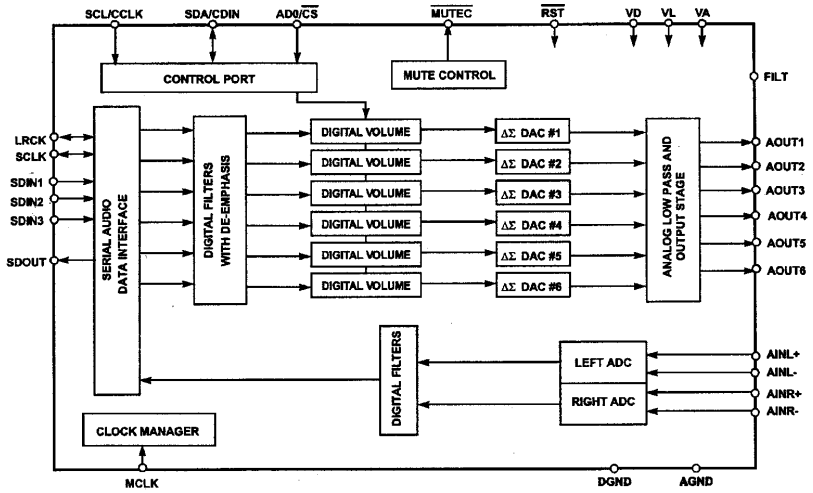
PIN ASSIGNMENT (TOP VIEW)

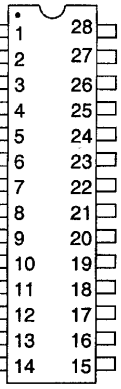




Bose® P/N: 254182, SDRAM, 64MBIT

Bose P/N: 258495-001, 2.5V Regulator

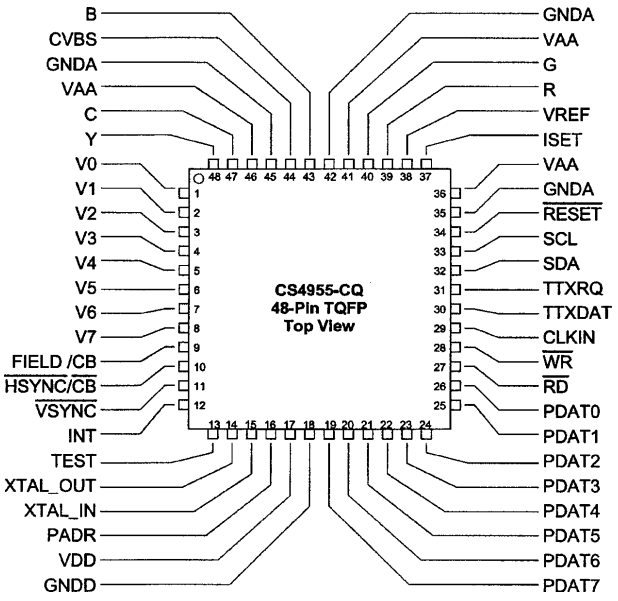


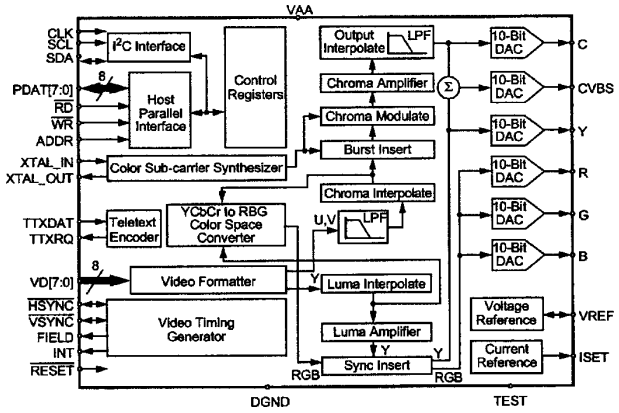


Serial Audio Data In 3	**SDIN3**	1	28	**SUB**	Analog Out #6,Subwoofer
Serial Audio Data In 2	**SDIN2**	2	27	**CENTER**	Analog Out #5, Center
Serial Audio Data In 1	**SDIN1**	3	26	**SR**	Analog Out #4, Surround Right
Serial Audio Data Out	**SDOUT**	4	25	**SL**	Analog Out #3, Surround Left
Serial Clock	**SCLK**	5	24	**FR**	Analog Out #2, Front Right
Left/Right Clock	**LRCK**	6	23	**FL**	Analog Out #1, Front Left
Digital Ground	**DGND**	7	22	**AGND**	Analog Ground
Digital Power	**VD**	8	21	**VA**	Analog Power
Digital Interface Power	**VL**	9	20	**AINL+**	Left Channel Analog Input+
Master Clock	**MCLK**	10	19	**AINL-**	Left Channel Analog Input-
SCL/CCLK	**SCL/CCLK**	11	18	**FILT**	Internal Voltage Filter
SDA/CDIN	**SDA/CDIN**	12	17	**AINR-**	Right Channel Analog Input-
AD0/$\overline{CS}$	**AD0/$\overline{CS}$**	13	16	**AINR+**	Right Channel Analog Input+
Reset	**RST**	14	15	**MUTEC**	Mute Control

Bose P/N: 254192, CODEC, CS4228A-KS

INTEGRATED CIRCUIT DIAGRAMS

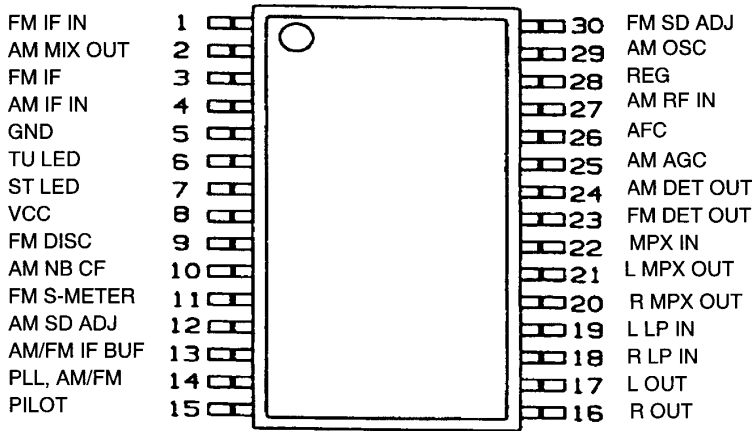


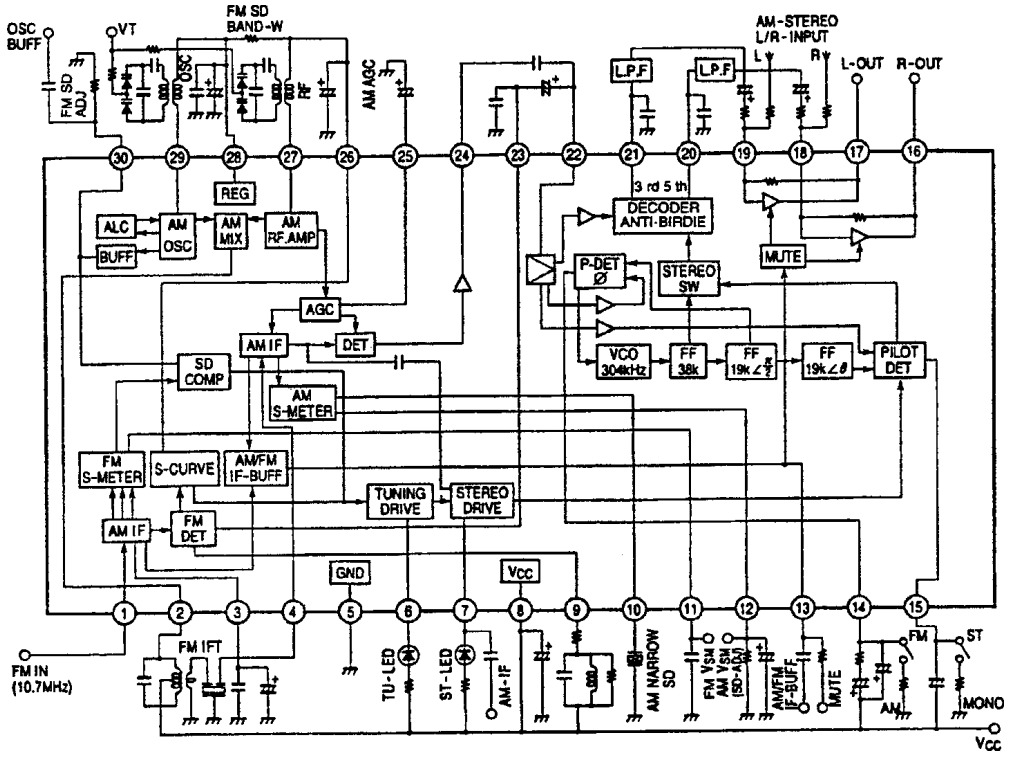


Pin Name	Pin Number	Type	Description
V [7:0]	8, 7, 6, 5, 4, 3, 2, 1	IN	Digital video data inputs
CLK	29	IN	27 MHz input clock
PADDR	16	IN	Address enable line
XTAL_IN	15	IN	subcarrier crystal input
XTAL_OUT	14	OUT	subcarrier crystal output
$\overline{\text{HSYNC}}/\overline{\text{CB}}$	10	I/O	Active low horizontal sync, or composite blank signal
$\overline{\text{VSYNC}}$	11	I/O	Active low vertical sync.
FIELD/CB	9	OUT	Video field ID. Selectable polarity or composite blank
$\overline{\text{RD}}$	27	IN	Host parallel port read strobe, active low
$\overline{\text{WR}}$	28	IN	Host parallel port write strobe, active low
PDAT [7:0]	19, 20, 21, 22, 23, 24, 25, 26	I/O	Host parallel port/ general purpose I/O
SDA	32	I/O	I^2C data
SCL	33	IN	I^2C clock input
CVBS	44	CURRENT	Composite video output
Y	48	CURRENT	Luminance analog output
C	47	CURRENT	Chrominance analog output
R	39	CURRENT	Red analog output
G	40	CURRENT	Green analog output
B	43	CURRENT	Blue analog output
VREF	38	I/O	Internal voltage reference output or external reference input
ISET	37	CURRENT	DAC current set
TTXDAT	30	IN	Teletext data input
TTXRQ	31	OUT	Teletext request output
INT	12	OUT	Interrupt output, active high
$\overline{\text{RESET}}$	34	IN	Active low master RESET
TEST	13	IN	TEST pin. Ground for normal operation
VAA	36, 41, 46	PS	+ 5 V or + 3.3 V supply (must be same as VDD)
GNDD	18	PS	Ground
VDD	17	PS	+5 V or 3.3 V supply (must be same as VAA)
GNDA	35, 42, 45	PS	Ground

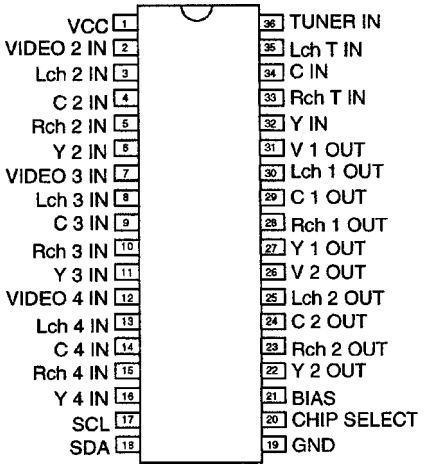
Bose® P/N: 256088-001, Digital Video Encoder, CS4955-CQ

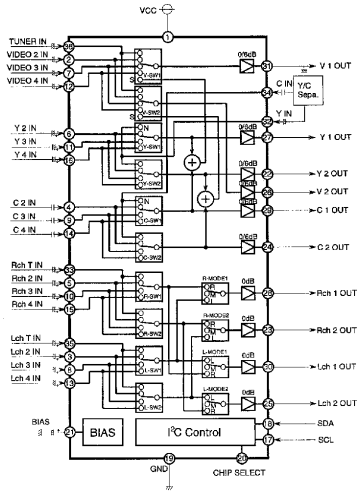
INTEGRATED CIRCUIT DIAGRAMS





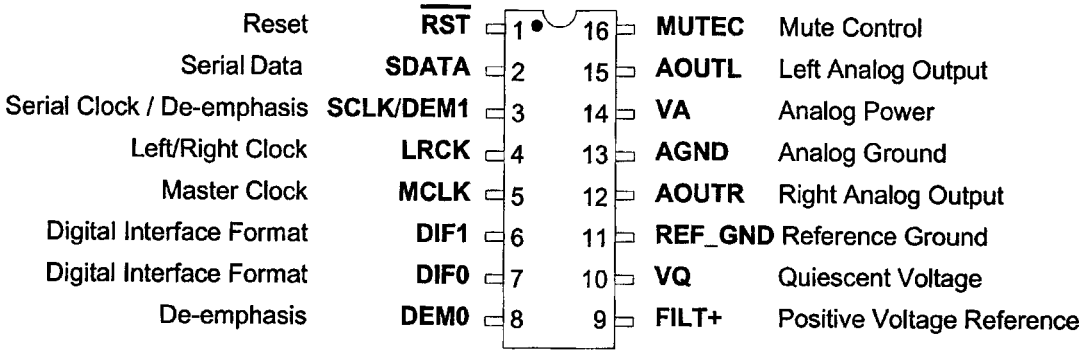
Bose® P/N: 254561-001, AM/FM Tuner, MFP-30S

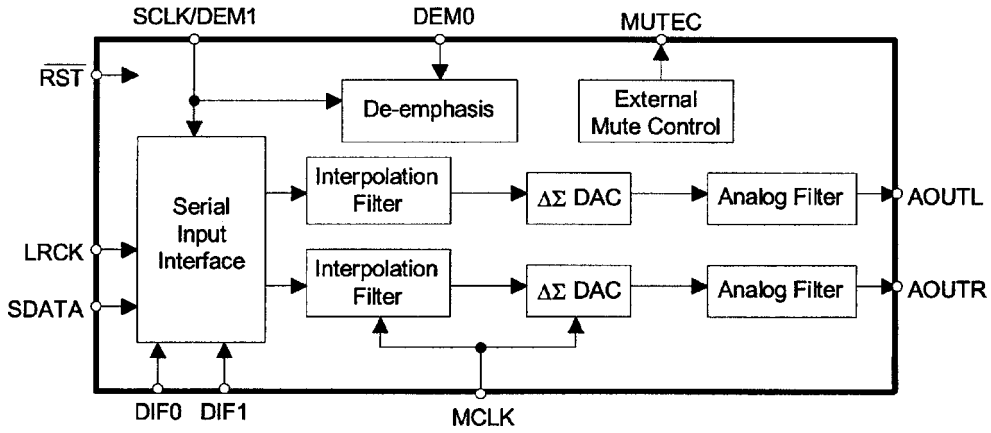




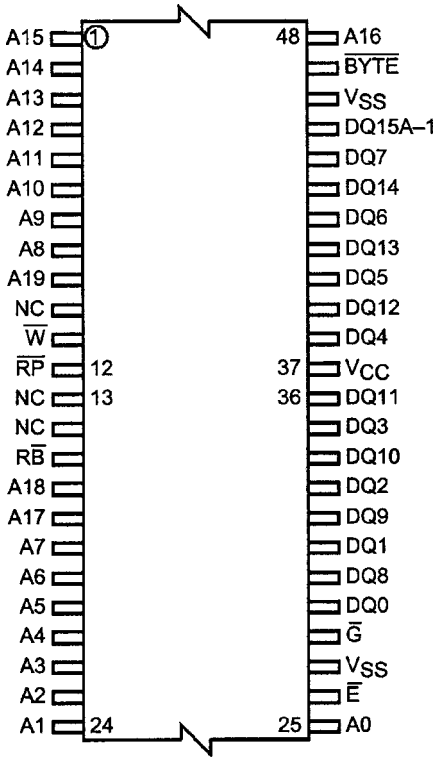
Bose P/N: 259495-001, Audio/Video Switch, 4 Input, 2 Channel, SSOP36

INTEGRATED CIRCUIT DIAGRAMS

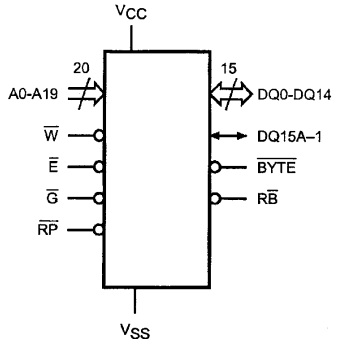




Bose® P/N: 256087-001, DAC, CS4340-KS

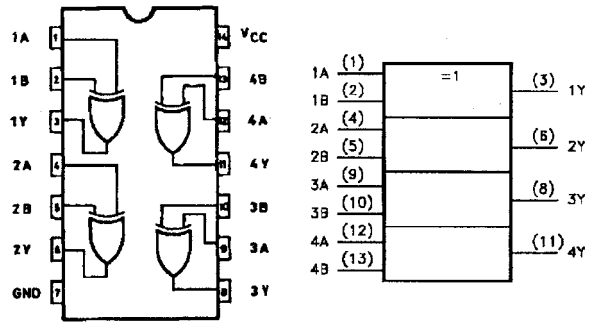


A0-A19	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A–1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$\overline{RB}$	Ready/Busy Output (Not available on SO44 package)
$\overline{BYTE}$	Byte/Word Organization Select
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Don't Use as internally connected



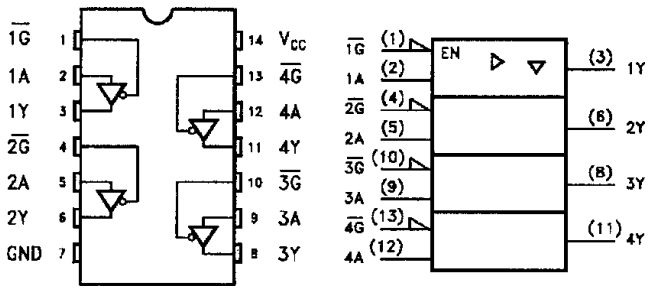
Bose P/N: 256089-003, Flash Memory, 16M, 3.3V, TSSOP

INTEGRATED CIRCUIT DIAGRAMS



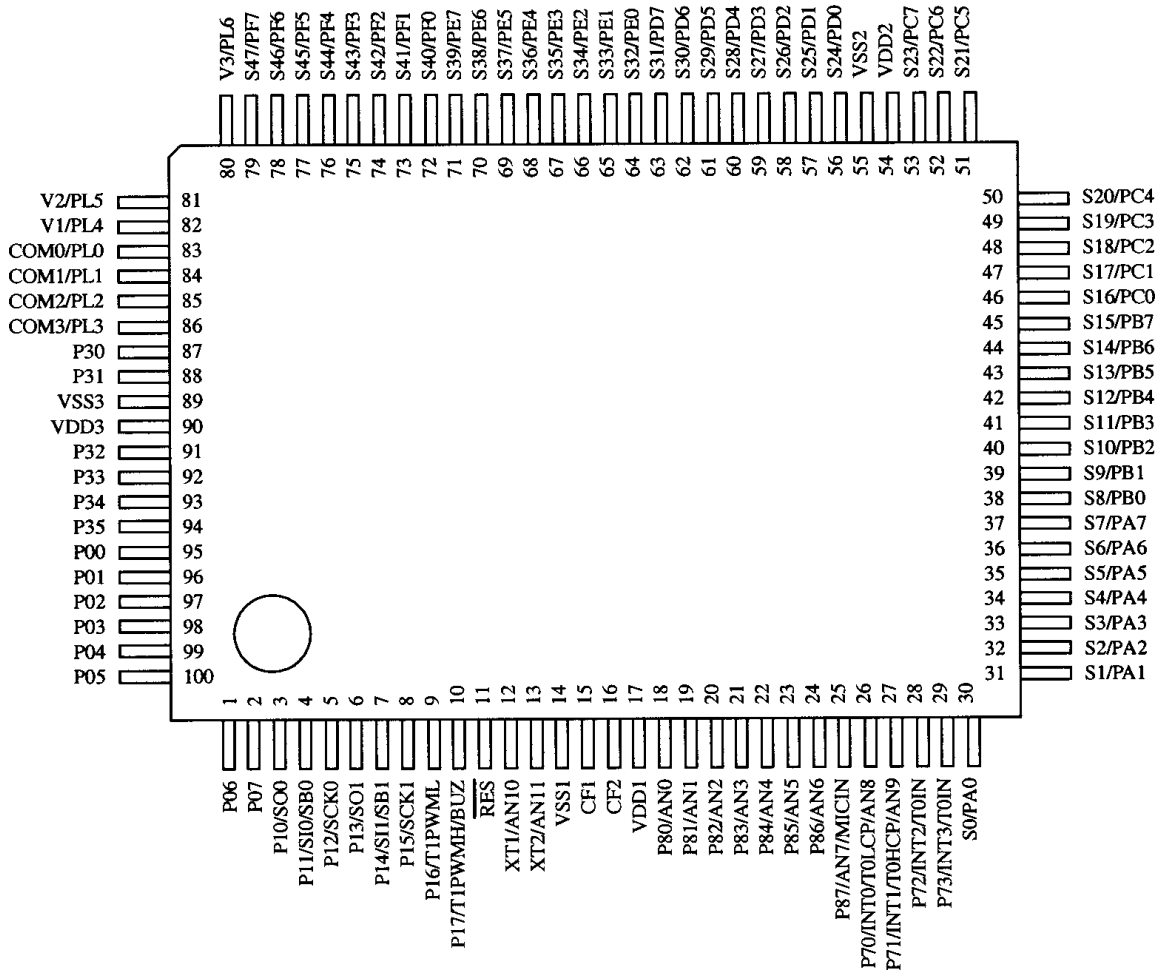
Pin #	Pin Name	Function
1	1A	Data Input A
2	1B	Data Input B
3	1Y	Data Output Y
4	2A	Data Input A
5	2B	Data Input B
6	2Y	Data Output Y

Bose® P/N: 259548-001 Quad Exclusive OR



PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$\overline{1G}$ TO $\overline{4G}$	Output Enable Input
2, 5, 9, 12	1A TO 4A	Data Inputs
3, 6, 8, 11	1Y TO 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

Bose P/N: 263182-001 Quad Buffer



Bose P/N: 256088-001, Digital Video Encoder, CS4955-CQ

INTEGRATED CIRCUIT DIAGRAMS

Pin Number	Name	Function/Description
01	P06	8-bit input/output port (Port 0) Data direction is programmable in nibble units (P04-07) Use of pull up resistor can be specified in nibble units (P04-07) Input for HOLD release Input for port 0 interrupt Output can be programmed CMOS or Nch-open drain
02	P07	
03	P10/SO0	8-bit input/output port (Port 1) data direction is programmable for each bit Use of pull up resistor can be specified for each bit individually Other pin functions: P10 SIO0 data output P11 SIO0 data input or bus input/output P12 SIO0 clock input/output P13 SIO1 Data output P14 SIO1 data input or bus input/output P15 SIO1 clock input/output P16 Timer 1PWML output P17 Timer 1 PWMH output/Buzzer output Output can be programmed CMOS or Nch-open drain
04	P11/SI0/SB0	
05	P12/SCK0	
06	P13/SO1	
07	P14/SI1/SB1	
08	P15/SCK1	
09	P16/T1PWML	
10	P17/T1PWMH/BUZ	
11	$\overline{RES}$	Reset input terminal
12	XT1/AN10	Input for 32.768 kHz crystal oscillation Other functions: general purpose input port AD input port: AN10 When not in use connect to VDD1
13	XT2/AN11	Output for 32.768 kHz crystal oscillation Other functions: General purpose input port AD input port: AN11 When not in use set to oscillation mode and leave open
14	VSS1	Power Supply (-)
15	CF1	Input terminal for ceramic oscillator
16	CF2	Output terminal for ceramic oscillator
17	VDD1	Power Supply (+)

Pin Number	Name	Function/Description
18	P80/AN0	8-bit input/output port (Port 8) Input/output can be specified for each bit individually Other functions: AD input port: AN0 to AN7 Small signal detector input port: MICIN (P87) Output is Nch-open drain
19	P81/AN1	
20	P82/AN2	
21	P83/AN3	
22	P84/AN4	
23	P85/AN5	
24	P86/AN6	
25	P87/AN7/MICIN	
26	P70/INT0/T0LCP/AN8	4-bit input/output port (Port 7) Data direction can be specified for each bit Use of pull-up resistor can be specified for each bit individually Other function: P70: INT0 input/HOLD release input/Timer 0L capture input/ output for watchdog timer. P71: INT1 input/HOLD release input/Timer 0H capture input P72: INT2 input/HOLD release input/Timer 0 event input/Timer 0L capture input P73: INT3 Input (noise rejection filter attached)/Timer 0 event input/Timer 0H capture input. AD input port: AN8 (P70), AN9 (P71) P70 output is Nch-open drain P71,P72,P73 outputs are CMOS Interrupt detection selection (see Section 1.5 table)
27	P71/INT1/T0HCP/AN9	
28	P72/INT2/T0IN	
29	P73/INT3/T0IN	
30	S0/PA0	Segment output for LCD Can be used as general purpose input/output port (PA) Output is CMOS
31	S1/PA1	
32	S2/PA2	
33	S3/PA3	
34	S4/PA4	
35	S4/PA5	
36	S6/PA6	
37	S7/PA7	

Pin Number	Name	Function/Description
38	S8/PB0	Segment output for LCD Can be used as general purpose input/output port (PB) Output is CMOS
39	S9/PB1	
40	S10/PB2	
41	S11/PB3	
42	S12/PB4	
43	S13/PB5	
44	S14/PB6	
45	S15/PB7	

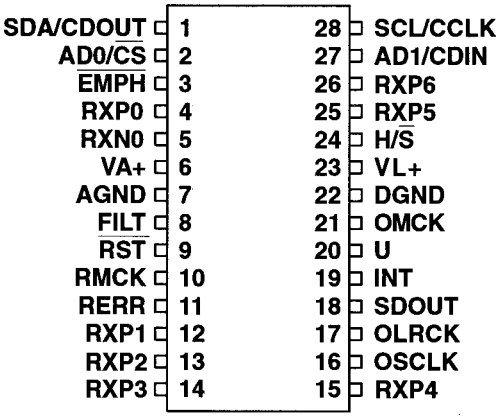
Pin Number	Name	Function/Description
46	S16/PC0	Segment output for LCD Can be used as general purpose input/output port (PC) Output is CMOS
47	S17/PC1	
48	S18/PC2	
49	S19/PC3	
50	S20/PC4	
51	S21/PC5	
52	S22/PC6	
53	S23PC7	
54	VDD2	Power Supply (+)
55	VSS2	Power Supply (-)
56	S24/PD0	Segment output for LCD Can be used as general purpose input/output port (PD) Output is CMOS
57	S25/PD1	
58	S26/PD2	
59	S27/PD3	
60	S28/PD4	
61	S29/PD5	
62	S30/PD6	
63	S31/PD7	

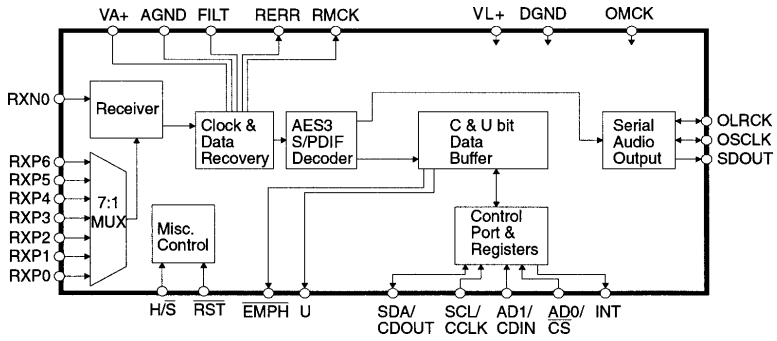
Pin Number	Name	Function/Description
64	S32/PE0	Segment output for LCD Can be used as general purpose input/output port (PE) Output is CMOS
65	S33/PE1	
66	S34/PE2	
67	S35/PE3	
68	S36/PE4	
69	S37/PE5	
70	S38/PE6	
71	S39/PE7	
72	S40/PF0	Segment output for LCD Can be used as general purpose input/output port (PF) Output is CMOS
73	S41/PF1	
74	S42/PF2	
75	S43/PF3	
76	S44/PF4	
77	S45/PF5	
78	S46/PF6	
79	S47/PF7	
80	V3/PL6	LCD output bias power supply Can be used as general purpose input port (PL)
81	V2/PL5	
82	V1/PL4	
83	COM0/PL0	Common output for LCD Can be used as general purpose input port (PL)
84	COM1/PL1	
85	COM2/PL2	
86	COM3/PL3	
87	P30	6-bit Input/output port (Port 3) Data direction can be specified for each bit Use of pull up resistor can be specified for each bit individually Output can be programmed CMOS or Nch-open drain
88	P31	
89	VSS3	Power supply (-)
90	VDD3	Power supply (+)
91	P32	6-bit Input/output port (Port 3) Data direction can be specified for each bit Use of pull up resistor can be specified for each bit individually Output can be programmed CMOS or Nch-open drain
92	P33	
93	P34	
94	P35	

Pin Number	Name	Function/Description
95	P00	8-bit input/output port (Port 0) data direction is programmable in nibble units (P00-03, P04-07) Use of pull up resistor can be specified in nibble units (P00-03, P04-07) Input for HOLD release Input for port 0 interrupt Output can be programmed CMOS or Nch-open drain
96	P01	
97	P02	
98	P03	
99	P04	
100	P05	

Bose® P/N: 256088-001, Digital Video Encoder, CS4955-CQ

INTEGRATED CIRCUIT DIAGRAMS

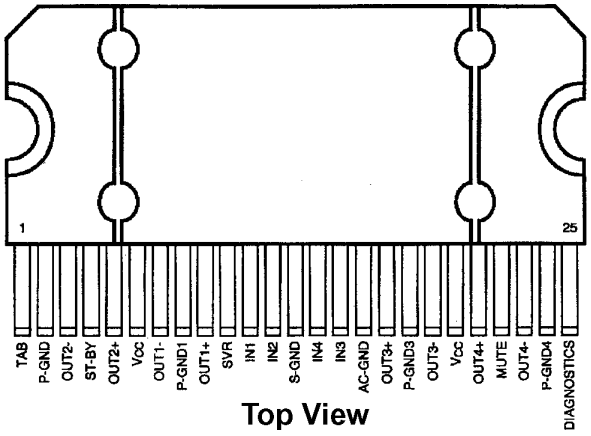




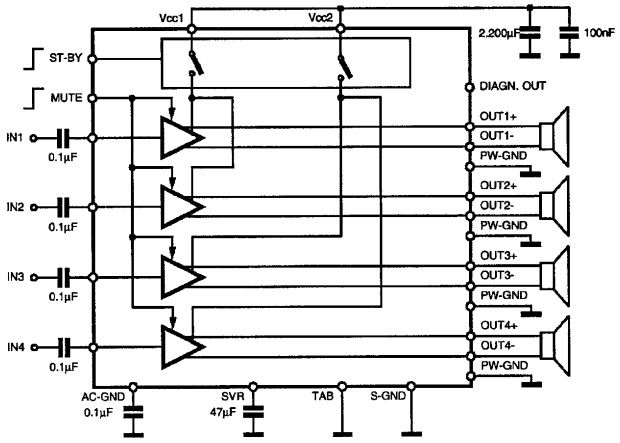
SDA/CDOUT	1	**Serial Control Data I/O (Two-Wire) / Data Out (SPI)** (*Input/Output*) - In Two-Wire mode, SDA is the control I/O data line. SDA is open drain and requires an external pull-up resistor to VL+. In SPI mode, CDOUT is the output data from the control port interface on the CS8415A
AD0/CS	2	**Address Bit 0 (Two-Wire) / Control Port Chip Select (SPI)** (*Input/Output*) - A falling edge on this pin puts the CS8415A into SPI control port mode. With no falling edge, the CS8415A defaults to Two-Wire mode. In Two-Wire mode, AD0 is a chip address pin. In SPI mode, CS is used to enable the control port interface on the CS8415A
EMPH	3	**Pre-Emphasis** (*Output*) - EMPH is low when the incoming Channel Status data indicates 50/15 µs pre-emphasis. EMPH is high when the Channel Status data indicates no pre-emphasis or indicates pre-emphasis other than 50/15 µs. This is also a start-up option pin, and requires a 47 kΩ resistor to either VL+ or DGND, which determines the AD2 address bit for the control port in Two-Wire mode
RXP0 **RXN0**	4 5	**AES3/SPDIF Receiver Port** (*Input*) - Differential line receiver inputs carrying AES3 data. RXP0 may be used as a single-ended input as part of 7:1 S/PDIF Input MUX. If RXP0 is used in MUX, RXN0 must be ac coupled to ground.
RXP1 **RXP2** **RXP3** **RXP4** **RXP5** **RXP6**	12 13 14 15 25 26	**Additional AES3/SPDIF Receiver Port** (*Input*) - Single-ended receiver inputs carrying AES3 or S/PDIF digital data. These inputs, along with RXP0, comprise the 7:1 S/PDIF Input Multiplexer and select line control is accessed using the MUX2:0 bits in the Control 2 register. Please note that any unused inputs should be tied to ground.
VA+	6	**Positive Analog Power** (*Input*) - Positive supply for the analog section. Nominally +5 V. This supply should be as quiet as possible since noise on this pin will directly affect the jitter performance of the recovered clock
AGND	7	**Analog Ground** (*Input*) - Ground for the analog circuitry in the chip. AGND and DGND should be connected to a common ground area under the chip.
FILT	8	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and ground.
RST	9	**Reset** (*Input*) - When RST is low, the CS8415A enters a low power mode and all internal states are reset. On initial power up, RST must be held low until the power supply is stable, and all input clocks are stable in frequency and phase.
RMCK	10	**Input Section Recovered Master Clock** (*Input/Output*) - Input section recovered master clock output when PLL is used. Frequency defaults to 256x the sample rate (Fs) and may be set to 128x. When the PLL is bypassed by using the RXD0 bit in the Clock Source Control register, an external clock of 256 Fs may be applied to this pin
RERR	11	**Receiver Error** (*Output*) - When high, indicates a problem with the operation of the AES3 receiver. The status of this pin is updated once per sub-frame of incoming AES3 data. Conditions that can cause RERR to go high are: validity, parity error, bi-phase coding error, confidence, QCRC and CCRC errors, as well as loss of lock in the PLL. Each condition may be optionally masked from affecting the RERR pin using the Receiver Error Mask Register. The RERR pin tracks the status of the unmasked errors: the pin goes high as soon as an unmasked error occurs and goes low immediately when all unmasked errors go away
OSCLK	16	**Serial Audio Output Bit Clock** (*Input/Output*) - Serial bit clock for audio data on the SDOUT pin
OLRCK	17	**Serial Audio Output Left/Right Clock** (*Input/Output*) - Word rate clock for the audio data on the SDOUT pin. Frequency will be the output sample rate (Fs)
SDOUT	18	**Serial Audio Output Data** (*Output*) - Audio data serial output pin
INT	19	**Interrupt** (*Output*) - Indicates errors and key events during the operation of the CS8415A. All bits affecting INT may be unmasked through bits in the control registers. The condition(s) that initiated interrupt are readable through a control register. The polarity of the INT output, as well as selection of a standard or open drain output, is set through a control register. Once set true, the INT pin goes false only after the interrupt status registers have been read and the interrupt status bits have returned to zero
U	20	**User Data** (*Output*) - Outputs User data from the AES3 receiver.
OMCK	21	**System Clock** (*Input*) - When the OMCK System Clock Mode is enabled using the SWCLK bit in the Control 1 register, the clock signal input on this pin is output through RMCK. OMCK serves as reference signal for OMCK/RMCK ratio expressed in register 0x1E
DGND	22	**Digital Ground** (*Input*) - Ground for the digital circuitry in the chip. DGND and AGND should be connected to a common ground area under the chip.
VL+	23	**Positive Digital Power** (*Input*) - Positive supply for the digital section. Typically +3 to +5 V.
H/S	24	**Hardware/Software Mode Control** (*Input*) - Determines the method of controlling the operation of the CS8415A, and the method of accessing CS and U data. In software mode, device control and CS and U data access is primarily through the control port, using a microcontroller. Hardware mode provides an alternate mode of operation and access to the CS and U data through dedicated pins. This pin should be permanently tied to VL+ or DGND
AD1/CDIN	27	**Address Bit 1 (Two-Wire) / Serial Control Data In (SPI)** (*Input*) - In Two-Wire mode, AD1 is a chip address pin. In SPI mode, CDIN is the input data line for the control port interface
SCL/CCLK	28	**Control Port Clock** (*Input*) - Serial control interface clock and is used to clock control data bits into and out of the CS8415A. In Two-Wire mode, SCL requires an external pull-up resistor to VL+

Bose® P/N: 254193-001, SPDIF Receiver, CS8415A

INTEGRATED CIRCUIT DIAGRAMS

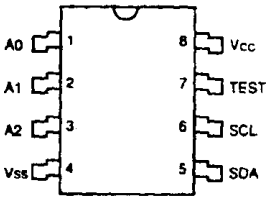


Top View

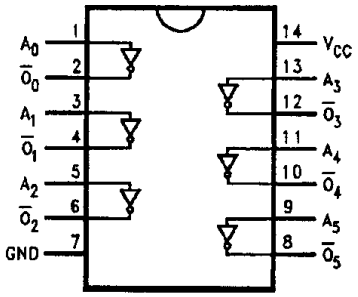


Bose® P/N: 254541-001, Power Amplifier, 4x30W, HSIP2

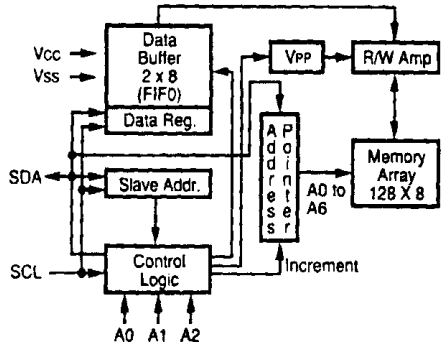
SOIC Package



PIN FUNCTION TABLE	
Name	**Function**
A0, A1, A2	Chip Address Inputs
V_{ss}	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
V_{cc}	+5 V Power Supply
Test	Tie to V_{cc} or V_{ss}



BLOCK DIAGRAM



Pin Descriptions

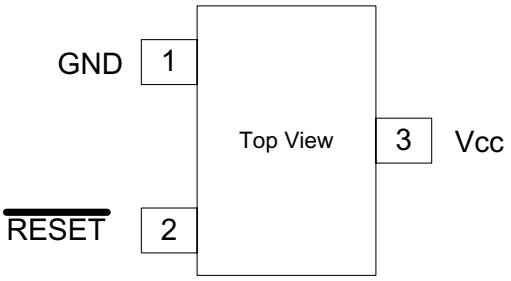
Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

A	$\overline{O}$
L	H
H	L

Bose P/N: 184044, EEPROM, 24C01A

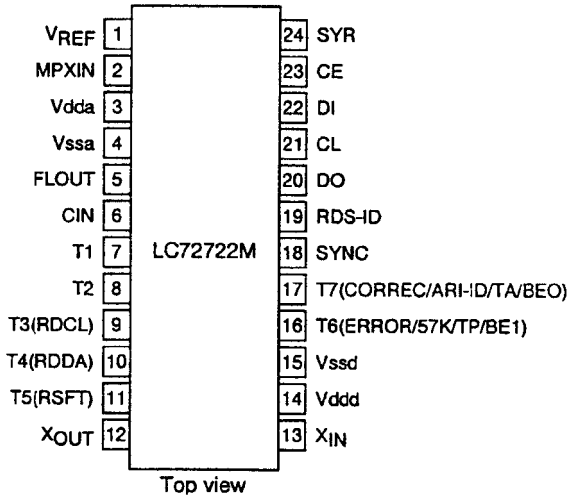
Bose P/N: 258464, 5V Inverter, 74VCHU04



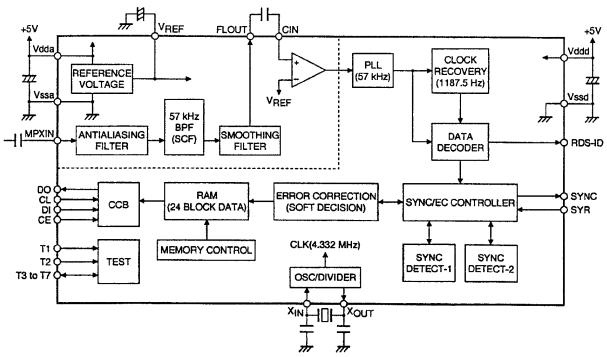
Pin Function
1. GND
2. RESET
   Output remains low while Vcc is below the reset threshold, and for a period of time after Vcc rises above the reset threshold.
3. Vcc Supply voltage

Bose P/N: 191158-01, MAX809 Reset IC

INTEGRATED CIRCUIT DIAGRAMS



Top view



Pin Number	Name	I/O	Description
1	VREF	Output	Reference voltage output (Vdda/2)
2	MPX IN	Input	Baseband (multiplexed) signal input
3	Vdda	—	Analog system power supply (+5V)
4	Vssa	—	Analog system ground
5	FLOUT	Output	Subcarrier output (filter output)
6	CIN	Input	Subcarrier input (comparator input)
7	T1	Input	Test input (this pin shall always be grounded)
8	T2	Input	Test input (standby control) 0 = normal control, 1 = standby state (crystal oscillator stopped)
9	T3 (RDCL)	I/O*	Test I/O (RDS clock output)
10	T4 (RDDA)	I/O*	Test I/O (RDS data output)
11	T5 (RSFT)	I/O*	Test I/O (soft-decision control data output)
12	XOUT	Output	Crystal oscillator output (4.332/8.664MHz)
13	XIN	Input	Crystal oscillator input (external reference signal)
14	Vddd	—	Digital system power supply (+5V)
15	Vssd	—	Digital system ground
16	T6 (ERROR/57K/TP/BE1)	I/O*	Test I/O (Error status output, regenerated carrier output, TP output, error block count output).
17	T7 (CORREC/ARI-IDT/TA/BEO	I/O*	Test I/O (Error correction status output, SK detection output TA output, error block count)
18	SYNC	I/O*	Block synchronization detection output
19	RDS-ID	Output	RDS detection output
20	DO	Output	Data output
21	CL	Input	Clock input
22	DI	Input	Data input
23	CE	Input	Chip enable
24	SYR	Input	Synchronization and RAM address reset (active high)

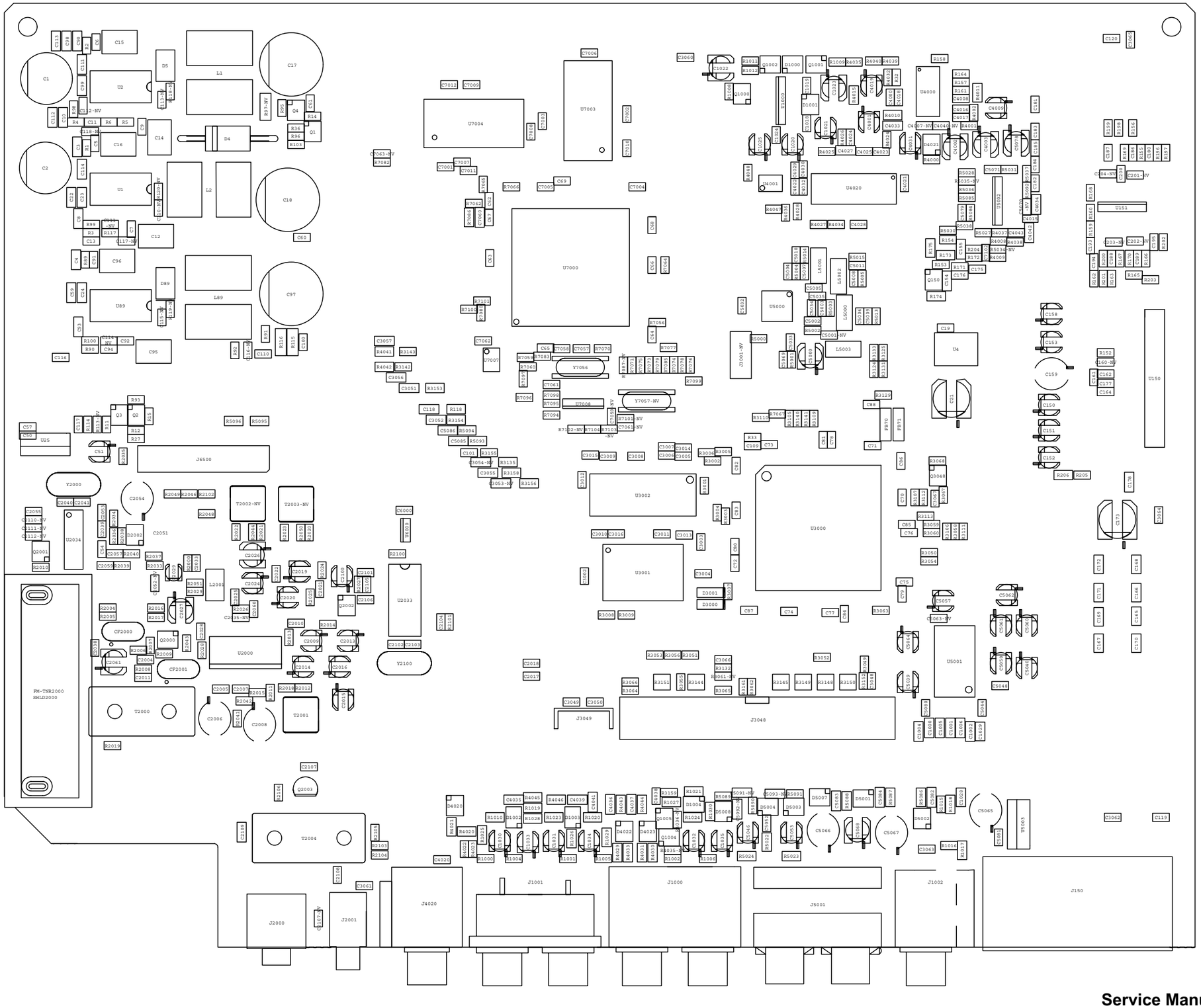
* Normally function as an output pin. Used as I/O pin in test mode, which is not available in user application.

Bose® P/N: 254562-001, LC72722M, RDS Signal Processor

SPECIFICATIONS AND FEATURES SUBJECT TO CHANGE WITHOUT NOTICE

Bose Corporation
The Mountain
Framingham Massachusetts USA 01701

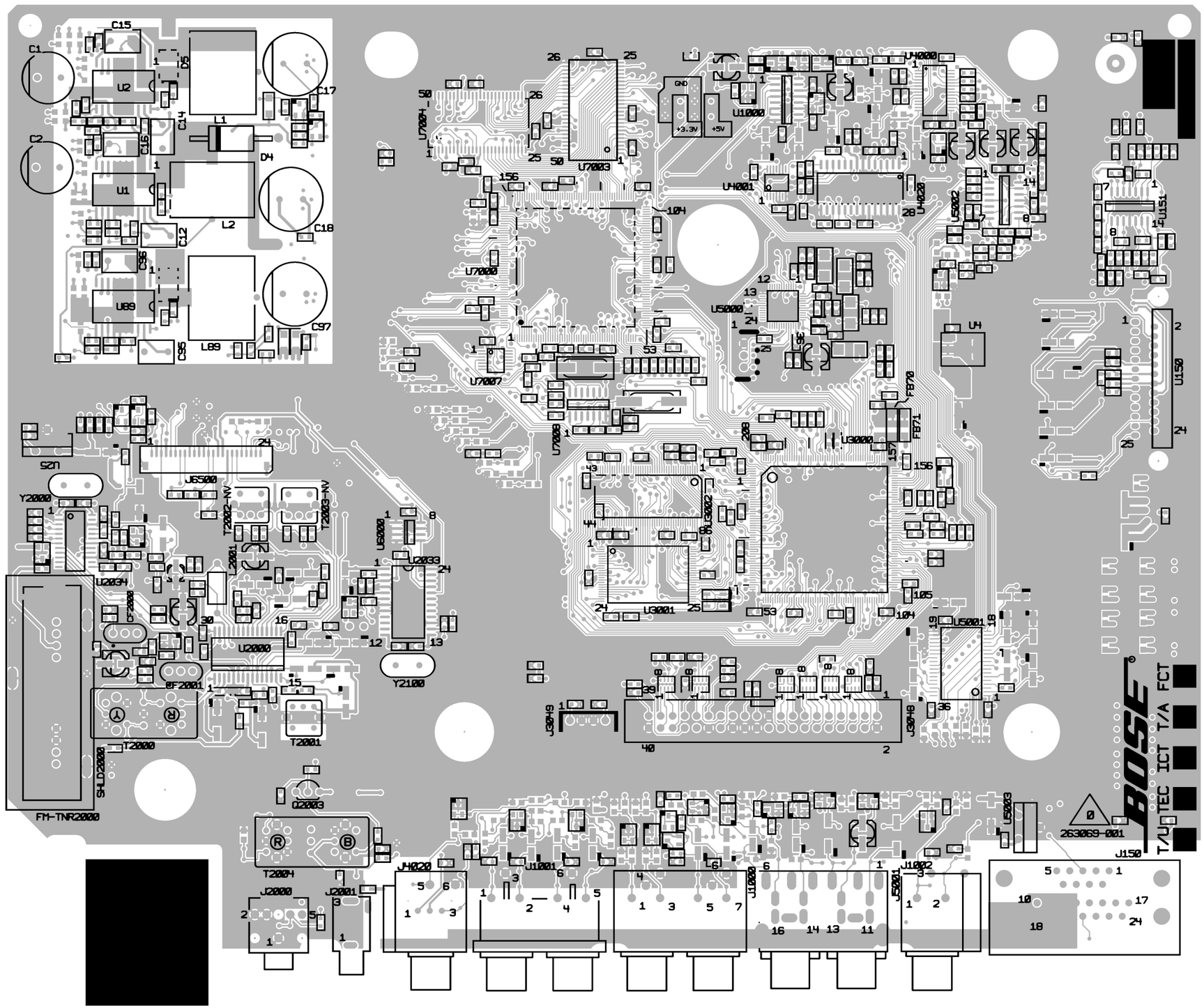
Reference Number 270000-TG1 Rev. 00 9/2003 (H)
Service web site: http://serviceops.bose.com
For technical assistance or part orders, call 1-800-233-4408



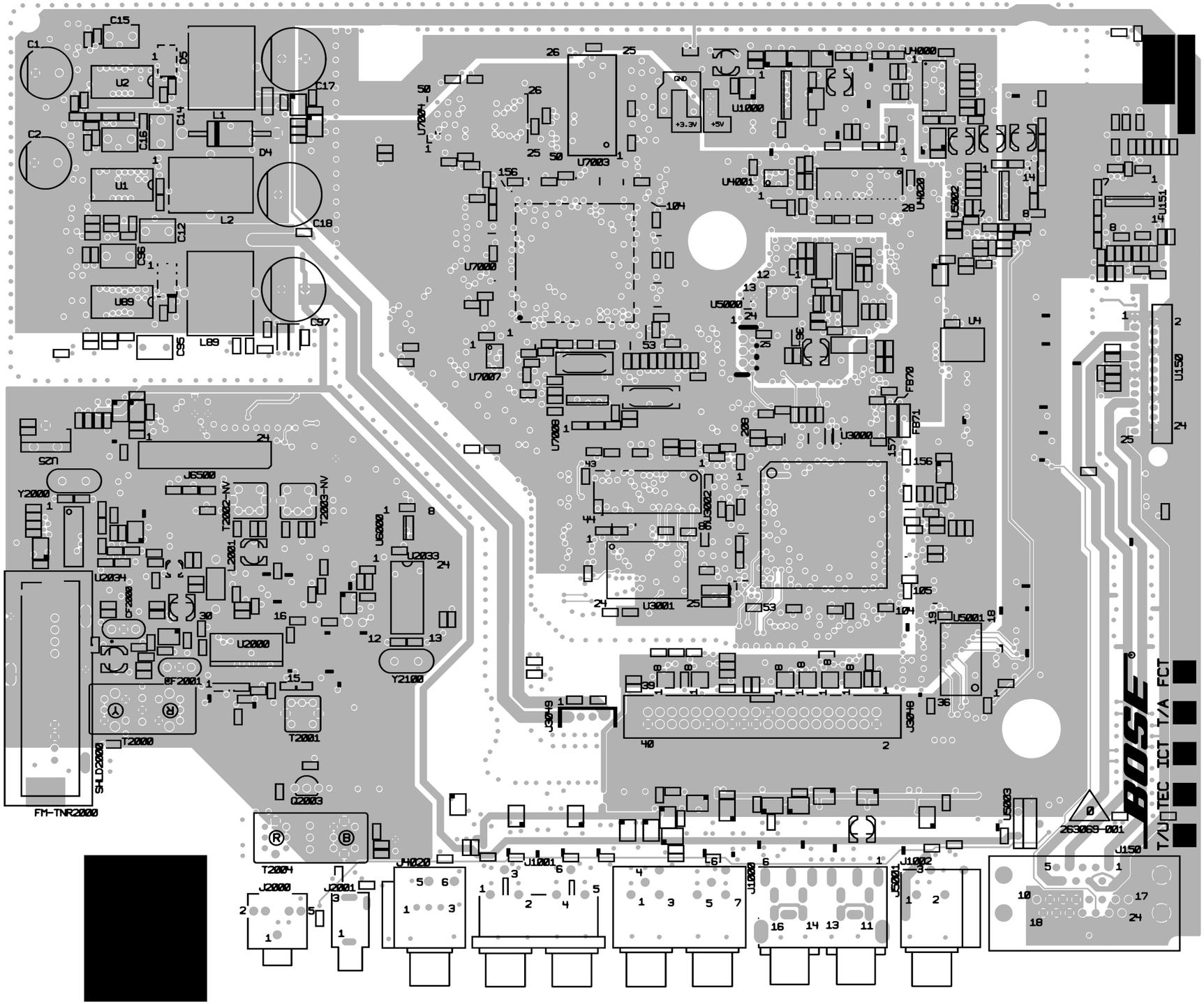
BOSE®

3-2-1 Home Entertainment System
Console Main PCB
Component Layout Diagram
PCB P/N: 263069-001 Rev. 0-2
Sheet 1 of 5

Service Manual Part Number 263493 Rev. 01

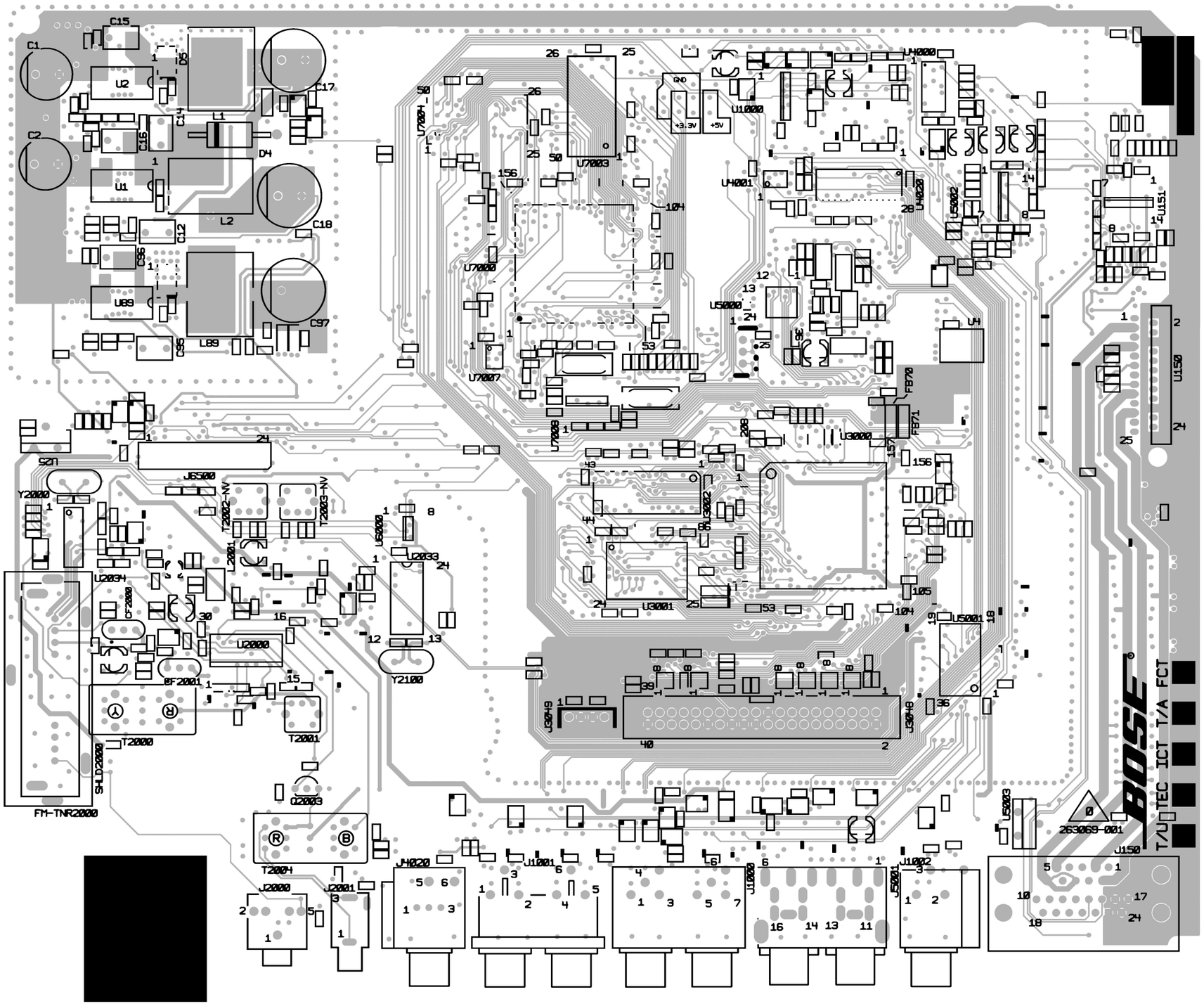


3-2-1 Home Ent. System
Console Main PCB
Component and Top Etch
Layout Diagram
PCB P/N: 263069-001 Rev. 0-2
Sheet 2 of 5



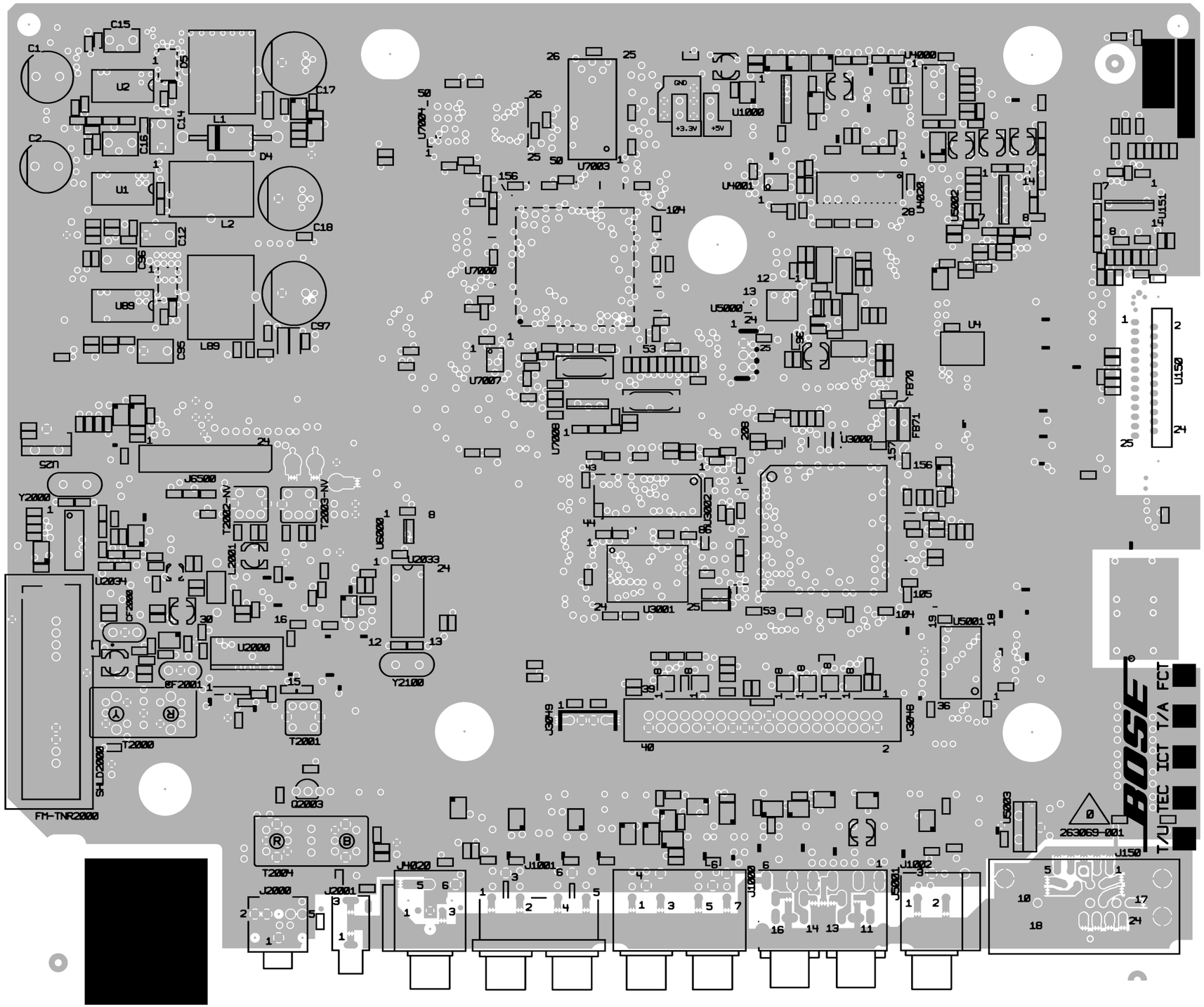
BOSE

3-2-1 Home Ent. System
Console Main PCB
Component and Internal Etch 1
Layout Diagram
PCB P/N: 263069-001 Rev. 0-2
Sheet 3 of 5



BOSE

3-2-1 Home Ent. System
Console Main PCB
Component and Internal Etch 2
Layout Diagram
PCB P/N: 263069-001 Rev. 0-2
Sheet 4 of 5



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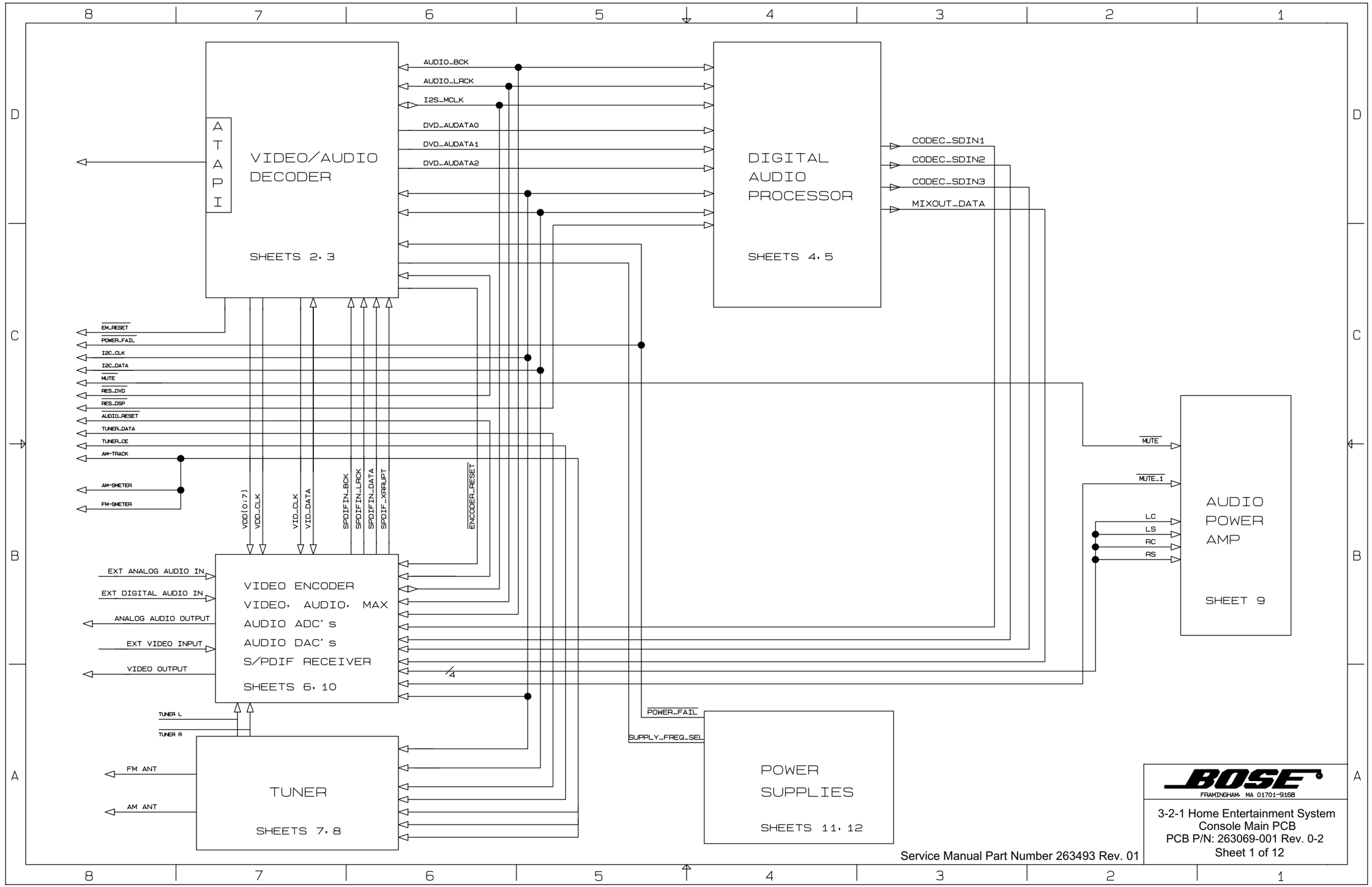
3-2-1 Home Ent. System
Console Main PCB
Component and Bottom Etch
Layout Diagram
PCB P/N: 263069-001 Rev. 0-2
Sheet 5 of 5

Service Manual Part Number 263493 Rev. 01


VIDEO/AUDIO DECODER
ATAPI
SHEETS 2, 3
DIGITAL AUDIO PROCESSOR
SHEETS 4, 5
AUDIO_BCK
AUDIO_LRCK
I2S_MCLK
DVD_AUDATA0
DVD_AUDATA1
DVD_AUDATA2
CODEC_SDIN1
CODEC_SDIN2
CODEC_SDIN3
MIXOUT_DATA
EM_RESET
POWER_FAIL
I2C_CLK
I2C_DATA
MUTE
RES_DVD
RES_DSP
AUDIO_RESET
TUNER_DATA
TUNER_CE
AM-TRACK
AM-SMETER
FM-SMETER
VDD[0:7]
VDD_CLK
VID_CLK
VID_DATA
SPDIFIN_BCK
SPDIFIN_LRCK
SPDIFIN_DATA
SPDIF_XRRUPT
ENCODER_RESET
EXT ANALOG AUDIO IN
EXT DIGITAL AUDIO IN
ANALOG AUDIO OUTPUT
EXT VIDEO INPUT
VIDEO OUTPUT
VIDEO ENCODER
VIDEO, AUDIO, MAX
AUDIO ADC's
AUDIO DAC's
S/PDIF RECEIVER
SHEETS 6, 10
4
TUNER L
TUNER R
FM ANT
AM ANT
TUNER
SHEETS 7, 8
MUTE
MUTE_1
LC
LS
RC
RS
AUDIO POWER AMP
SHEET 9
POWER_FAIL
SUPPLY_FREQ_SEL
POWER SUPPLIES
SHEETS 11, 12
BOSE
FRAMINGHAM, MA 01701-9168
3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 1 of 12
Service Manual Part Number 263493 Rev. 01

DEBUG CONNECTOR
TP611 TP610
148591-03
J3001-NV
GND
VID_CLK TP608 TP496
TP495
VID_DATA TP609
1
2
3

MD(0-31)
MA(0-11)

U3000
LS588
MA(11) TP492
MA(10)
MA(9)
MA(8)
MA(7)
MA(6)
MA(5)
MA(4)
MA(3)
MA(2)
MA(1)
MA(0)
MCKO R3003 33 TP45
MBSL
MCKE R3004 33 TP46
MAP R3001 33 TP47
MRASL R3005 33 TP48
MCASL R3002 33 TP49
MWEL R3006 33 TP50
DQM(0) TP340
DQM(1) TP341
DQM(2) TP342
DQM(3) TP343
DQM(0-3)
R3007 33
TP43
+3.3V R3008 10K
2_M_A_11
3_M_A_10
5_M_A_9
6_M_A_8
7_M_A_7
9_M_A_6
10_M_A_5
11_M_A_4
13_M_A_3
14_M_A_2
15_M_A_1
16_M_A_0
19_M_CKO
21_M_BS_L
22_M_CKE
23_M_AP
24_M_RAS_L
25_M_CAS_L
27_M_WE_L
28_DQM_0
29_DQM_1
31_DQM_2
32_DQM_3
81_NVR_WR_L
90_NVR_OE_L
M_D_31_87 TP428 MD(31)
M_D_30_83 TP427 MD(30)
M_D_29_79 TP426 MD(29)
M_D_28_76 TP425 MD(28)
M_D_27_74 TP424 MD(27)
M_D_26_71 TP423 MD(26)
M_D_25_68 TP422 MD(25)
M_D_24_64 TP421 MD(24)
M_D_23_67 TP420 MD(23)
M_D_22_70 TP419 MD(22)
M_D_21_72 TP418 MD(21)
M_D_20_75 TP417 MD(20)
M_D_19_78 TP416 MD(19)
M_D_18_80 TP415 MD(18)
M_D_17_86 TP414 MD(17)
M_D_16_88 TP413 MD(16)
M_D_15_60 TP412 MD(15)
M_D_14_56 TP411 MD(14)
M_D_13_54 TP410 MD(13)
M_D_12_49 TP409 MD(12)
M_D_11_46 TP408 MD(11)
M_D_10_44 TP407 MD(10)
M_D_9_40 TP406 MD(9)
M_D_8_33 TP405 MD(8)
M_D_7_37 TP404 MD(7)
M_D_6_42 TP403 MD(6)
M_D_5_45 TP402 MD(5)
M_D_4_48 TP401 MD(4)
M_D_3_51 TP400 MD(3)
M_D_2_55 TP399 MD(2)
M_D_1_59 TP397 MD(1)
M_D_0_62 TP398 MD(0)

+3.3V
C3002 .047uF GND
+3.3V

U3001 FLASH
256089
1_A15
2_A14
3_A13
4_A12
5_A11
6_A10
7_A9
8_A8
9_A19
10_NC
11_WE
12_RESET
13_NC
14_NC
15_RY_BY
16_A18
17_A17
18_A7
19_A5
20_A5
21_A4
22_A3
23_A2
24_A1
A16_48
BYTE_47
Vss_46
DQ15_A-1_45
DQ7_44
DQ14_43
DQ6_42
DQ13_41
DQ5_40
DQ12_39
DQ4_38
Vcc_37
DQ11_36
DQ3_35
DQ10_34
DQ2_33
DQ9_32
DQ1_31
DQ8_30
DQ0_29
OE_28
Vss_27
CE_26
A0_25
TP725
MD(19) MD(18) MD(17) MD(16)
MA(11) MA(10) MA(9) MA(8)
MD(23) MD(24)
MD(25)
MD(22) MD(21)
MA(7) MA(6) MA(5) MA(4) MA(3) MA(2) MA(1)
MD(20) MD(15) MD(7) MD(14) MD(6) MD(13) MD(5) MD(12) MD(4) MD(11) MD(3) MD(10) MD(2) MD(9) MD(1) MD(8) MD(0)
MA(0)
TP51
TP42
TP44
D3000Schottky
D3001Schottky
+3.3V R3009 1K
LAB TEST CONNECTOR

C3005 .047uF
C3006 .047uF
C3007 .047uF
C3003 .047uF
C3008 .047uF
C3004 .047uF
C3009 .047uF
C3010 .047uF
C3011 .047uF
C3012 .047uF
GND

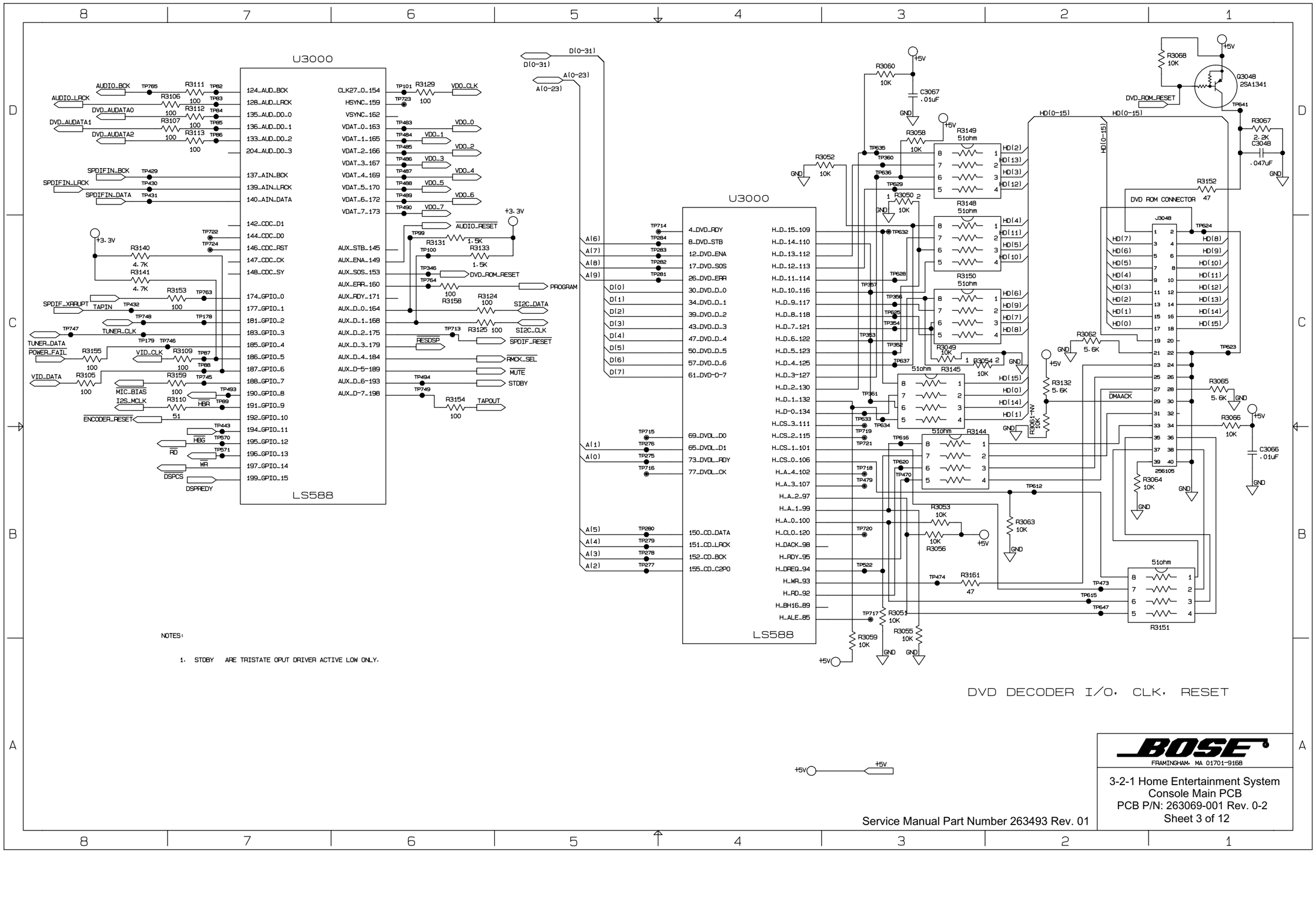
DRAM U3002
TC59S6432CFT
1_Vcc
2_DQ0
3_Vcc
4_DQ1
5_DQ2
6_VssQ
7_DQ3
8_DQ4
9_VccQ
10_DQ5
11_DQ6
12_VssQ
13_DQ7
14_Nc
15_Vcc
16_DQM0
17_WE
18_CAS
19_RAS
20_CS
21_NC
22_BS0
23_BS1
24_A10_AP
25_A0
26_A1
27_A2
28_DQM2
29_Vcc
30_NC
31_DQ16
32_VssQ
33_DQ17
34_DQ18
35_VccQ
36_DQ19
37_DQ20
38_VssQ
39_DQ21
40_DQ22
41_VccQ
42_DQ23
43_Vcc
Vss_86
DQ15_85
VssQ_84
DQ14_83
DQ13_82
VccQ_81
DQ12_80
DQ11_79
VssQ_78
DQ10_77
DQ9_76
VccQ_75
DQ8_74
NC_73
Vss_72
DQM1_71
NC_70
NC_69
CLK_68
CKE_67
A9_66
A8_65
A7_64
A6_63
A5_62
A4_61
A3_60
DQM3_59
Vss_58
NC_57
DQ31_56
VccQ_55
DQ30_54
DQ29_53
VssQ_52
DQ28_51
DQ27_50
VccQ_49
DQ26_48
DQ25_47
VssQ_46
DQ24_45
Vss_44
+3.3V
+3.3V
MD(0) MD(1) MD(2) MD(3) MD(4) MD(5) MD(6) MD(7)
MD(16) MD(17) MD(18) MD(19) MD(20) MD(21) MD(22) MD(23)
MD(15) MD(14) MD(13) MD(12) MD(11) MD(10) MD(9) MD(8)
MD(31) MD(30) MD(29) MD(28) MD(27) MD(26) MD(25) MD(24)
MWEL TP388
MCASL TP387
MRASL TP386
MBSL TP385
MA(10) TP384
MAP TP383
MA(0) TP382
MA(1) TP381
MA(2) TP380
TP497
TP396 MCKE
TP395 MA(9)
TP394 MA(8)
TP393 MA(7)
TP392 MA(6)
TP391 MA(5)
TP390 MA(4)
TP389 MA(3)
DQM(0) DQM(1) DQM(2) DQM(3)
C3013 .047uF
C3014 .047uF
C3015 .047uF
C3016 .047uF
GND

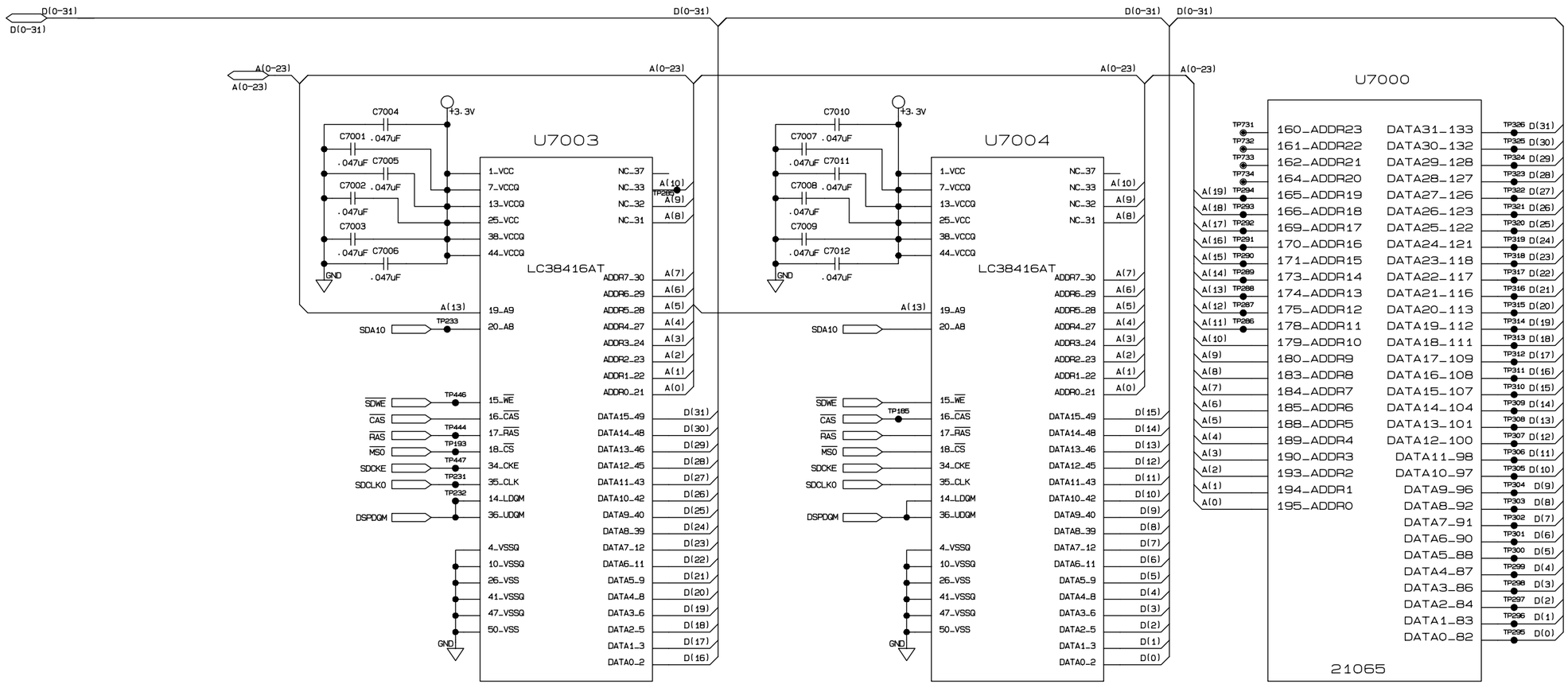
DVD DECODER
MEMORY INTERFACE

Service Manual Part Number 263493 Rev. 01

BOSE
FRAMINGHAM, MA 01701-9168

3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 2 of 12

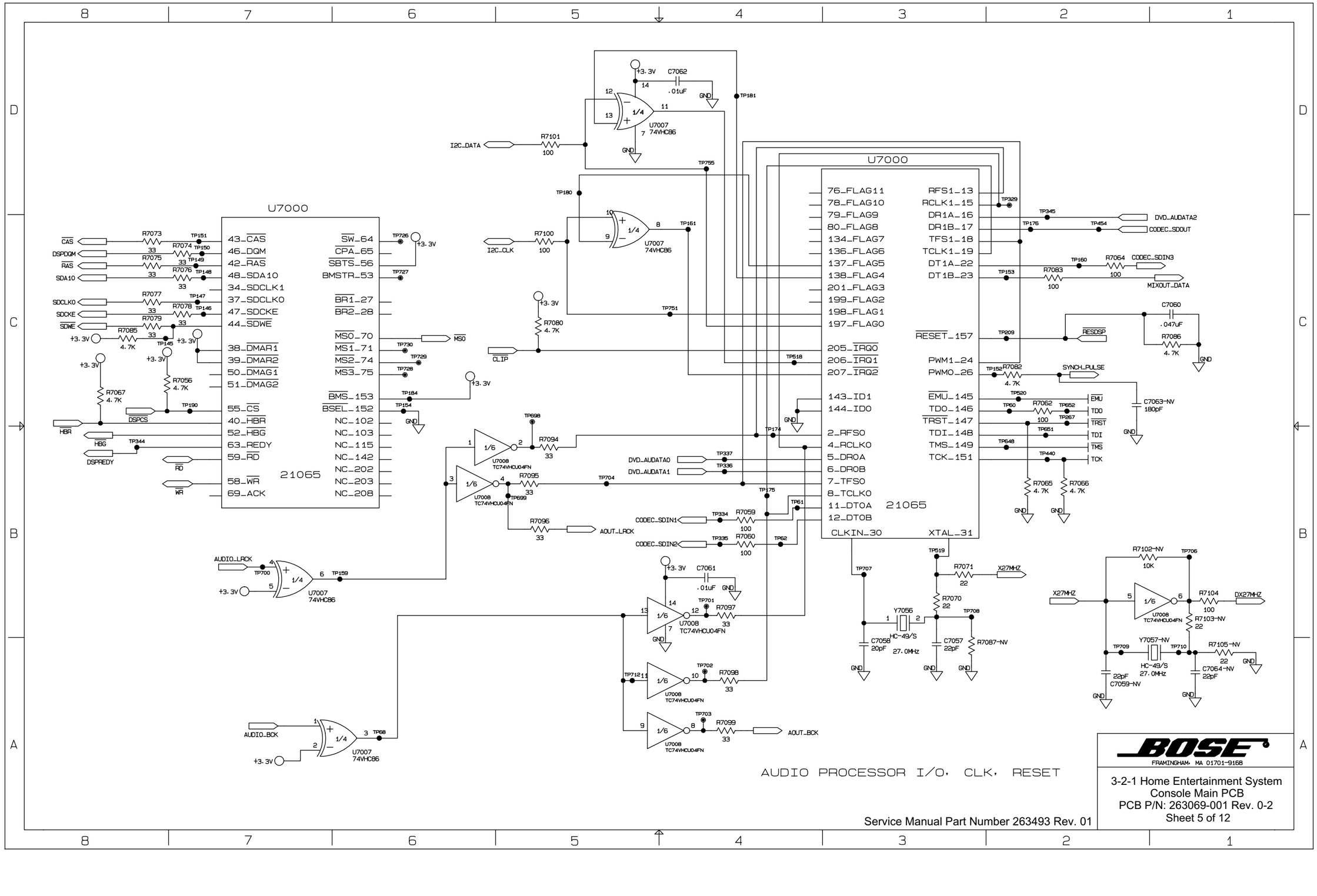

U3000
LS588
AUDIO_BCK
AUDIO_LRCK
DVD_AUDATA0
DVD_AUDATA1
DVD_AUDATA2
SPDIFIN_BCK
SPDIFIN_LRCK
SPDIFIN_DATA
SPDIF_XRAUPT
TAPIN
TUNER_CLK
TUNER_DATA
POWER_FAIL
VID_CLK
VID_DATA
MIC_BIAS
I2S_MCLK
ENCODER_RESET
HBG
RD
WR
DSPCS
DSPRDY
HBR
124_AUD_BCK
128_AUD_LRCK
135_AUD_DO_0
136_AUD_DO_1
133_AUD_DO_2
204_AUD_DO_3
137_AIN_BCK
139_AIN_LRCK
140_AIN_DATA
142_CDC_D1
144_CDC_D0
146_CDC_RST
147_CDC_CK
148_CDC_SY
174_GPIO_0
177_GPIO_1
181_GPIO_2
183_GPIO_3
185_GPIO_4
186_GPIO_5
187_GPIO_6
188_GPIO_7
190_GPIO_8
191_GPIO_9
192_GPIO_10
194_GPIO_11
195_GPIO_12
196_GPIO_13
197_GPIO_14
199_GPIO_15
CLK27_0_154
HSYNC_159
VSYNC_162
VDAT_0_163
VDAT_1_165
VDAT_2_166
VDAT_3_167
VDAT_4_169
VDAT_5_170
VDAT_6_172
VDAT_7_173
AUX_STB_145
AUX_ENA_149
AUX_SOS_153
AUX_ERR_160
AUX_RDY_171
AUX_D_0_164
AUX_D_1_168
AUX_D_2_175
AUX_D_3_179
AUX_D_4_184
AUX_D_5_189
AUX_D_6_193
AUX_D_7_198
VDO_CLK
VDO_0
VDO_1
VDO_2
VDO_3
VDO_4
VDO_5
VDO_6
VDO_7
AUDIO_RESET
DVD_ROM_RESET
PROGRAM
RESDSP
SI2C_DATA
SI2C_CLK
SPDIF_RESET
RMCK_SEL
MUTE
STDBY
TAPOUT
D(0-31)
A(0-23)
A(6)
A(7)
A(8)
A(9)
A(1)
A(0)
A(5)
A(4)
A(3)
A(2)
4_DVD_RDY
8_DVD_STB
12_DVD_ENA
17_DVD_SOS
26_DVD_ERR
30_DVD_D_0
34_DVD_D_1
39_DVD_D_2
43_DVD_D_3
47_DVD_D_4
50_DVD_D_5
57_DVD_D_6
61_DVD_D_7
69_DVDL_D0
65_DVDL_D1
73_DVDL_RDY
77_DVDL_CK
150_CD_DATA
151_CD_LRCK
152_CD_BCK
155_CD_C2PO
H_D_15_109
H_D_14_110
H_D_13_112
H_D_12_113
H_D_11_114
H_D_10_116
H_D_9_117
H_D_8_118
H_D_7_121
H_D_6_122
H_D_5_123
H_D_4_125
H_D_3_127
H_D_2_130
H_D_1_132
H_D_0_134
H_CS_3_111
H_CS_2_115
H_CS_1_101
H_CS_0_106
H_A_4_102
H_A_3_107
H_A_2_97
H_A_1_99
H_A_0_100
H_CLO_120
H_DACK_98
H_RDY_95
H_DREQ_94
H_WR_93
H_RD_92
H_BH16_89
H_ALE_85
HD(0-15)
DVD ROM CONNECTOR
J3048
DMAACK
51ohm
R3149
R3148
R3150
R3145
R3144
R3151
+5V
+3.3V
GND
NOTES:
1. STDBY ARE TRISTATE OPUT DRIVER ACTIVE LOW ONLY.
DVD DECODER I/O, CLK, RESET
BOSE
FRAMINGHAM, MA 01701-9168
3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 3 of 12
Service Manual Part Number 263493 Rev. 01



AUDIO PROCESSOR MEMORY INTERFACE

BOSE
FRAMINGHAM, MA 01701-9168

3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 4 of 12



AUDIO PROCESSOR I/O, CLK, RESET

BOSE
FRAMINGHAM, MA 01701-9168

3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 5 of 12

AUDIO PATH
RECORD OUT DAC

EXTERNAL ANALOG INPUT MUX

AUDIO INPUT, ADC, DAC

U1000 CS4340-KS

U4000 CS4228

U4020 CS8415A

U4001 74lcx125

Q1000 2SC4695

Q1001 2SC4695

Q1002 2SA1341

Q1004 2SA1341

Q1005 2SA1341

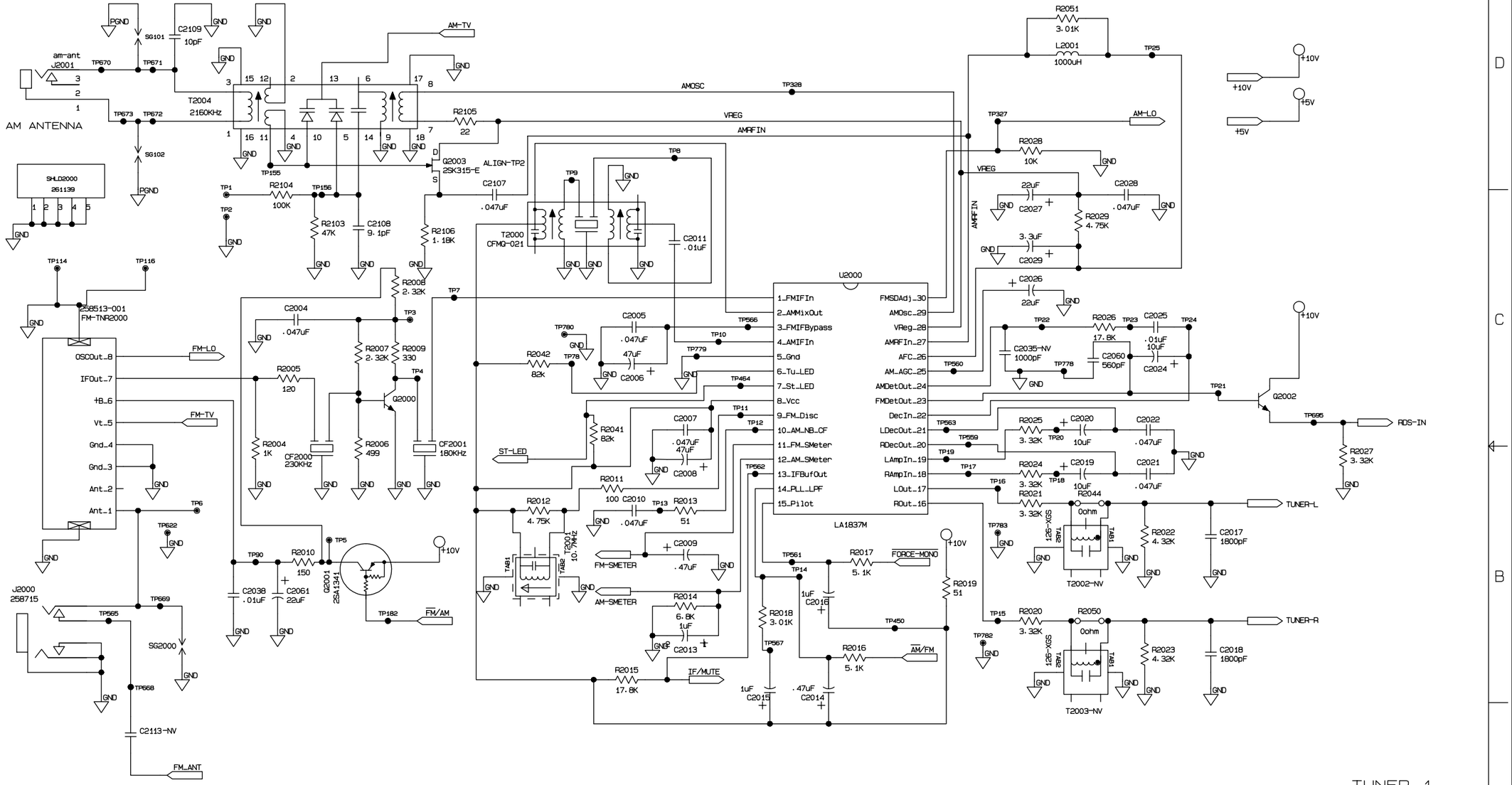
U5002 NJM3403AM

J1002 260134

Service Manual Part Number 263493 Rev. 01

BOSE
FRAMINGHAM, MA 01701-9168

3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 6 of 12



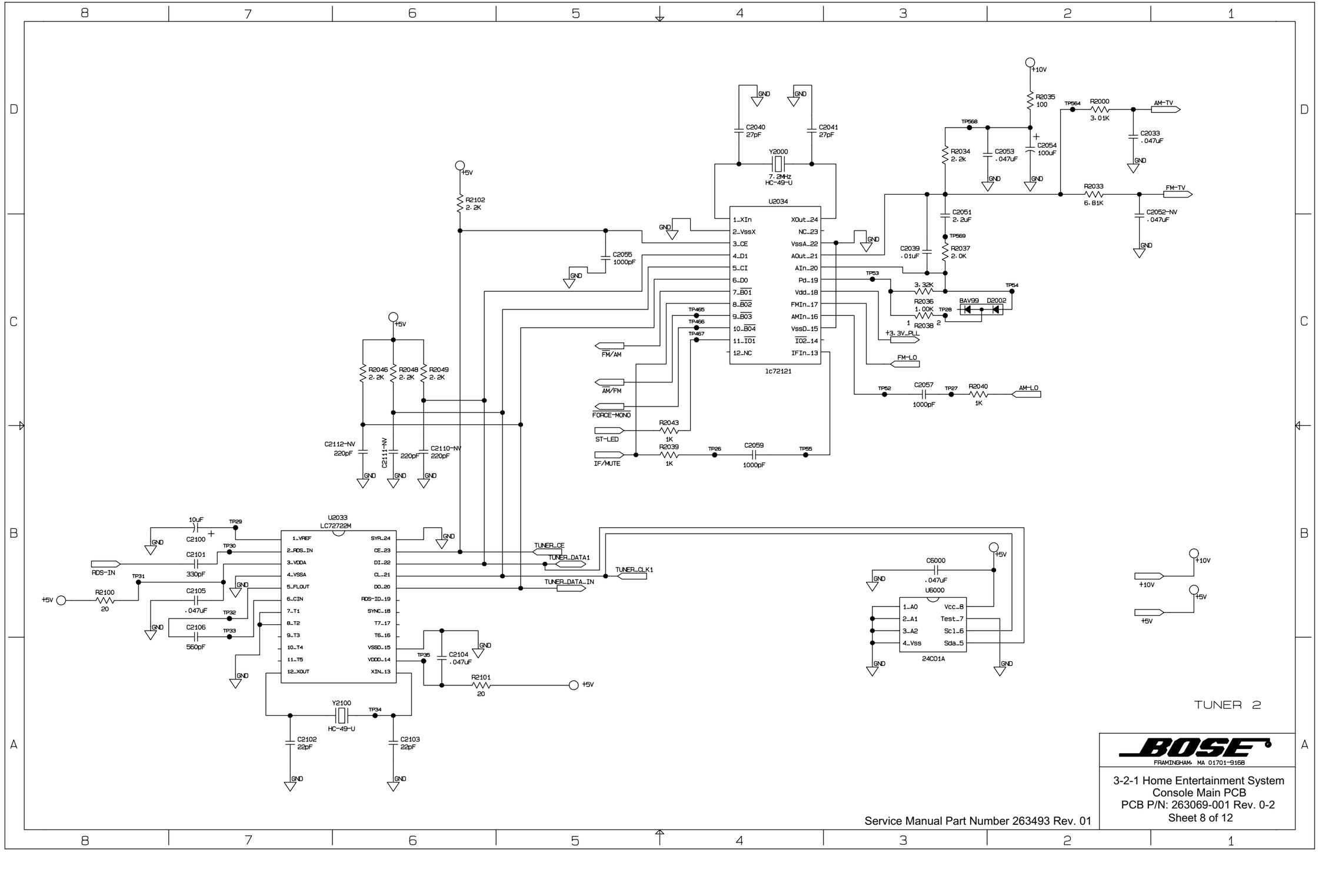
NOTES:

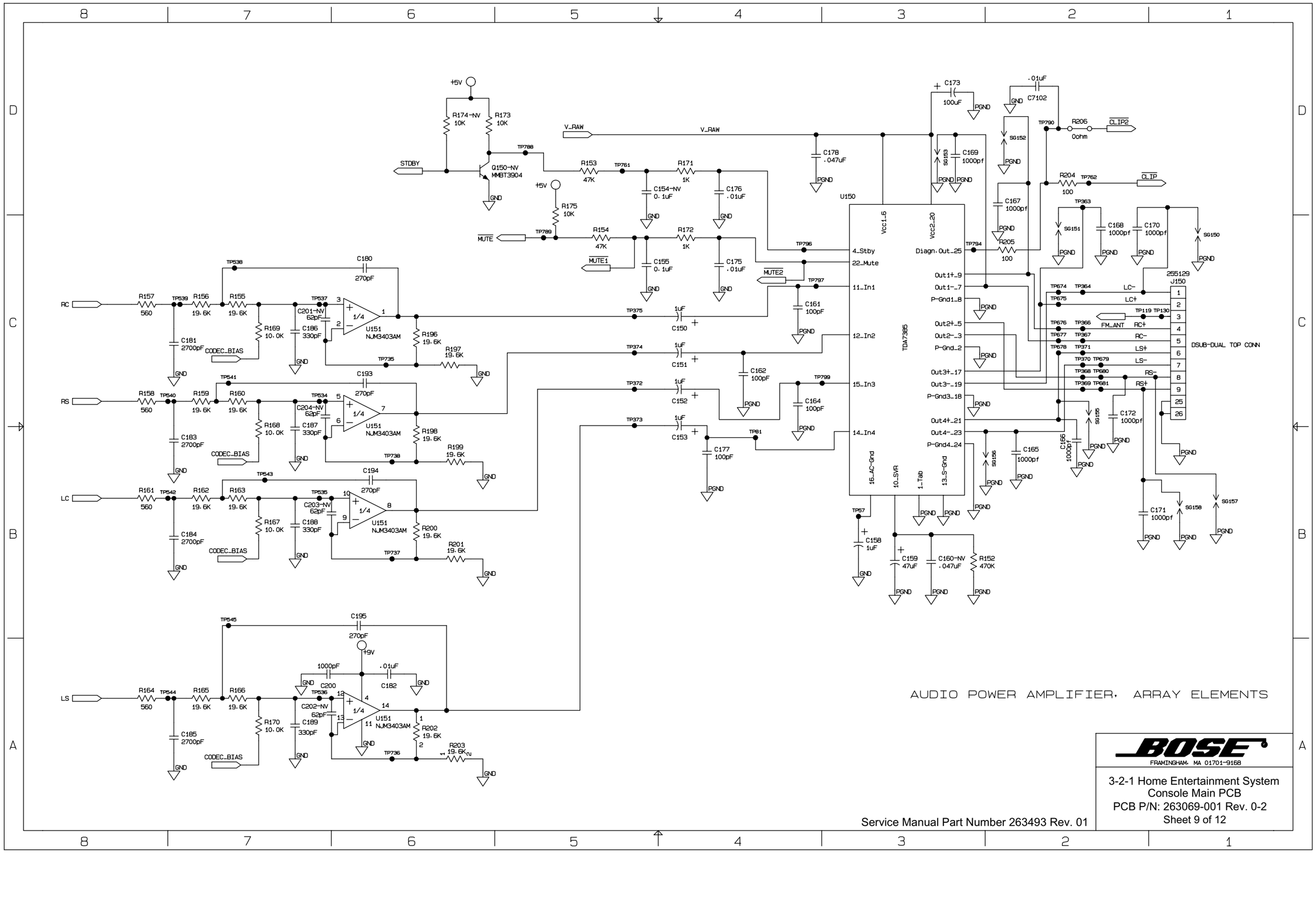
1. European version: C2021,C2022 = 0.033uF
   FM Front End = PT258513-2
2. Japan version: C2021,C2022 = 0.033uF
   FM Front End = PT258513-3
3. Zero ohm jumpers in lieu of T2002 and T2003 when digital filter used.

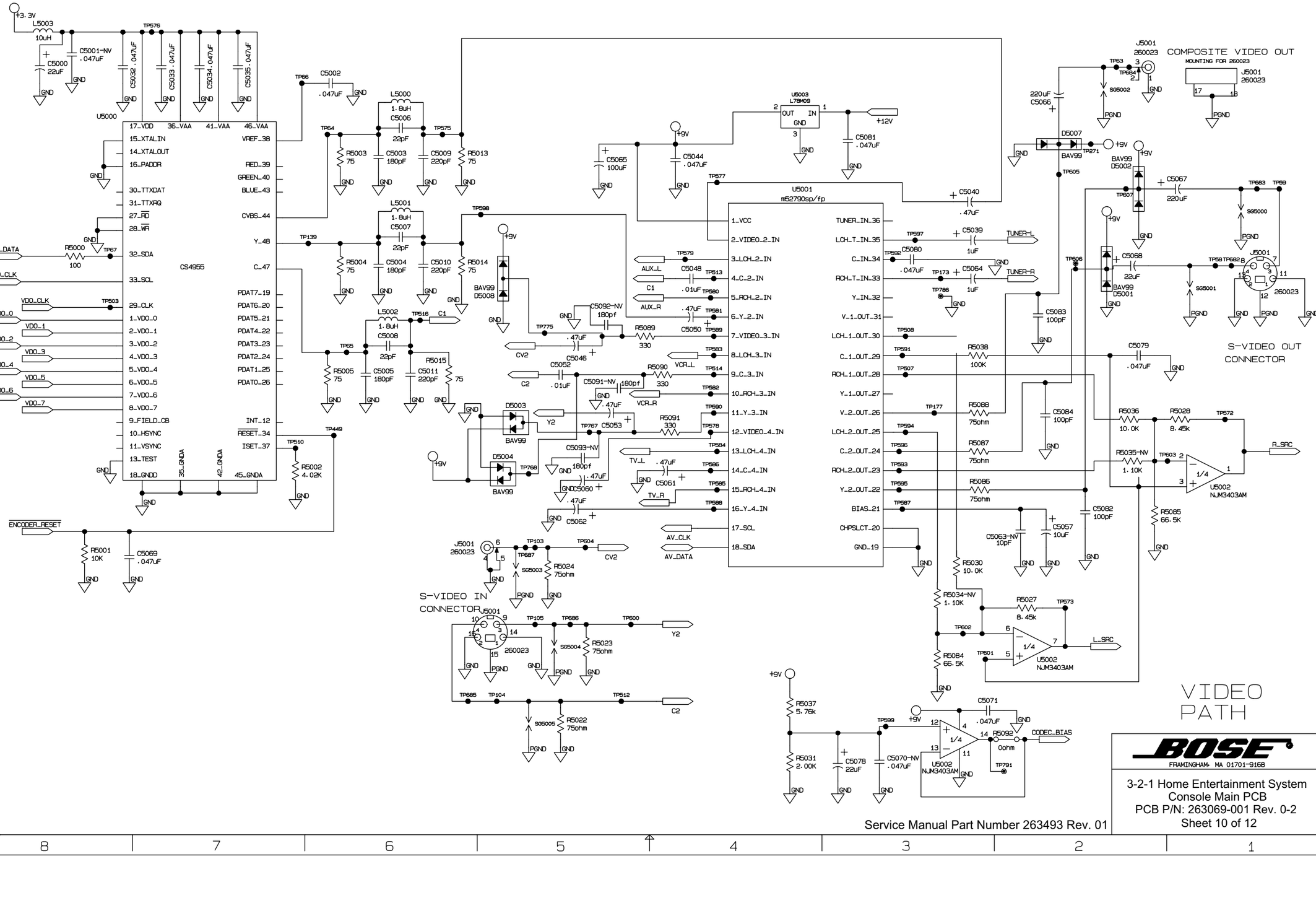
TUNER 1

BOSE
FRAMINGHAM, MA 01701-9168

3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 7 of 12


+10V
R2035
100
TP564
R2000
3.01K
AM-TV
C2033
.047uF
GND
TP568
R2034
2.2K
C2053
.047uF
C2054
100uF
R2033
6.81K
FM-TV
C2052-NV
.047uF
C2051
2.2uF
TP569
R2037
2.0K
C2039
.01uF
C2040
27pF
C2041
27pF
Y2000
7.2MHz
HC-49-U
U2034
1_XIn
2_VssX
3_CE
4_D1
5_CI
6_D0
7_B01
8_B02
9_B03
10_B04
11_I01
12_NC
XOut_24
NC_23
VssA_22
AOut_21
AIn_20
Pd_19
Vdd_18
FMIn_17
AMIn_16
VssD_15
I02_14
IFIn_13
lc72121
+5V
R2102
2.2K
C2055
1000pF
TP53
TP54
3.32K
R2036
1.00K
TP28
R2038
BAV99
D2002
+3.3V_PLL
FM-LO
TP52
C2057
1000pF
TP27
R2040
1K
AM-LO
TP465
TP466
TP467
FM/AM
AM/FM
FORCE-MONO
ST-LED
IF/MUTE
R2043
1K
R2039
1K
TP26
C2059
1000pF
TP55
R2046
2.2K
R2048
2.2K
R2049
2.2K
C2112-NV
220pF
C2111-NV
220pF
C2110-NV
220pF
U2033
LC72722M
1_VREF
2_RDS_IN
3_VDDA
4_VSSA
5_FLOUT
6_CIN
7_T1
8_T2
9_T3
10_T4
11_T5
12_XOUT
SYR_24
CE_23
DI_22
CL_21
DO_20
RDS-ID_19
SYNC_18
T7_17
T6_16
VSSD_15
VDDD_14
XIN_13
10uF
C2100
TP29
TP30
C2101
330pF
RDS-IN
TP31
R2100
20
C2105
.047uF
TP32
C2106
560pF
TP33
TP35
C2104
.047uF
R2101
20
Y2100
TP34
HC-49-U
C2102
22pF
C2103
22pF
TUNER_CE
TUNER_DATA1
TUNER_CLK1
TUNER_DATA_IN
C6000
.047uF
U6000
1_A0
2_A1
3_A2
4_Vss
Vcc_8
Test_7
Scl_6
Sda_5
24C01A
GND
TUNER 2
BOSE
FRAMINGHAM, MA 01701-9168
3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 8 of 12
Service Manual Part Number 263493 Rev. 01


AUDIO POWER AMPLIFIER, ARRAY ELEMENTS
BOSE
FRAMINGHAM, MA 01701-9168
3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 9 of 12
Service Manual Part Number 263493 Rev. 01
U150
TDA7385
U151
NJM3403AM
J150
255129
DSUB-DUAL TOP CONN
V_RAW
STDBY
MUTE
MUTE1
MUTE2
CLIP2
CLIP
FM_ANT
CODEC_BIAS
PGND
GND



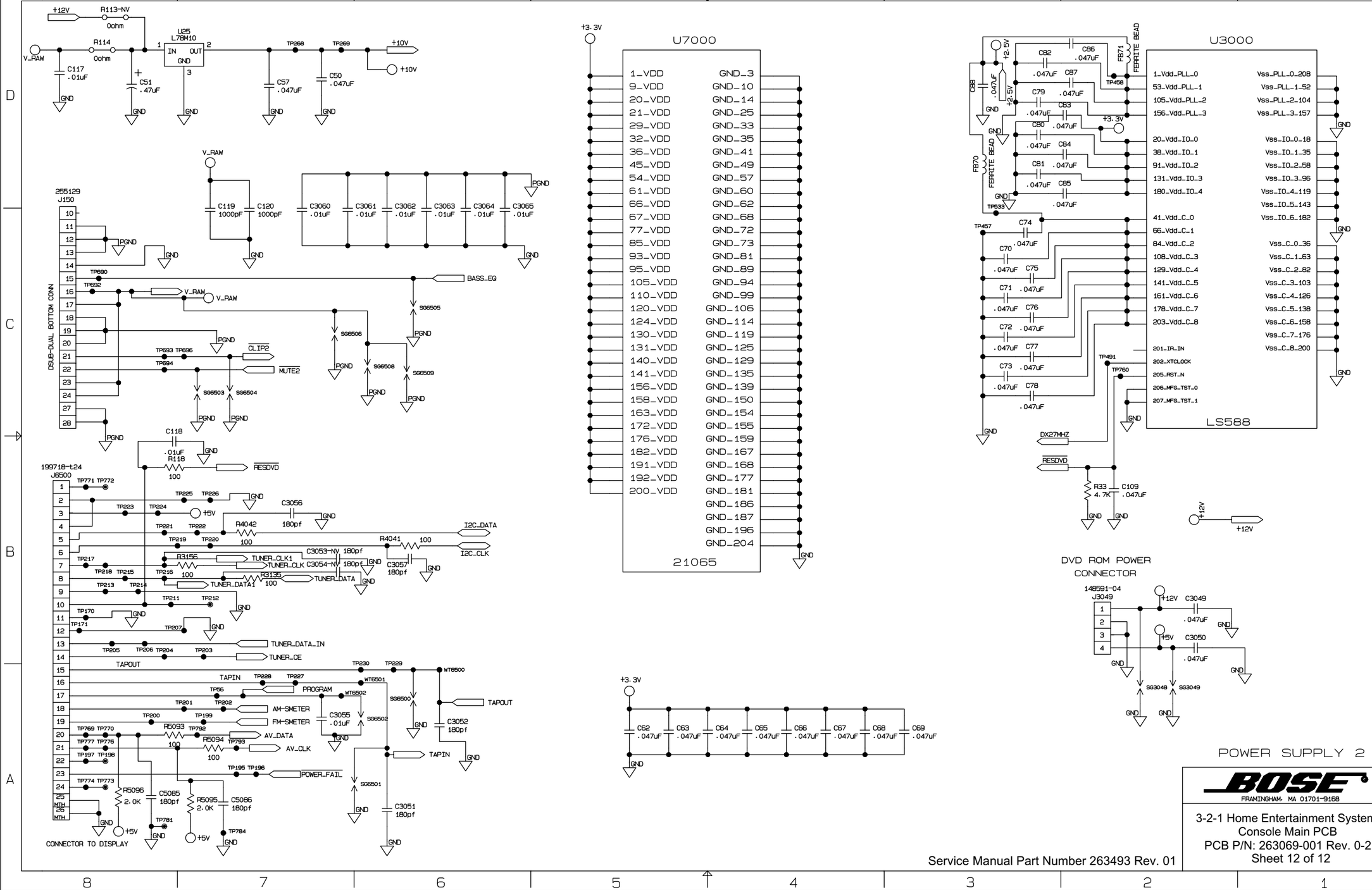
3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 10 of 12

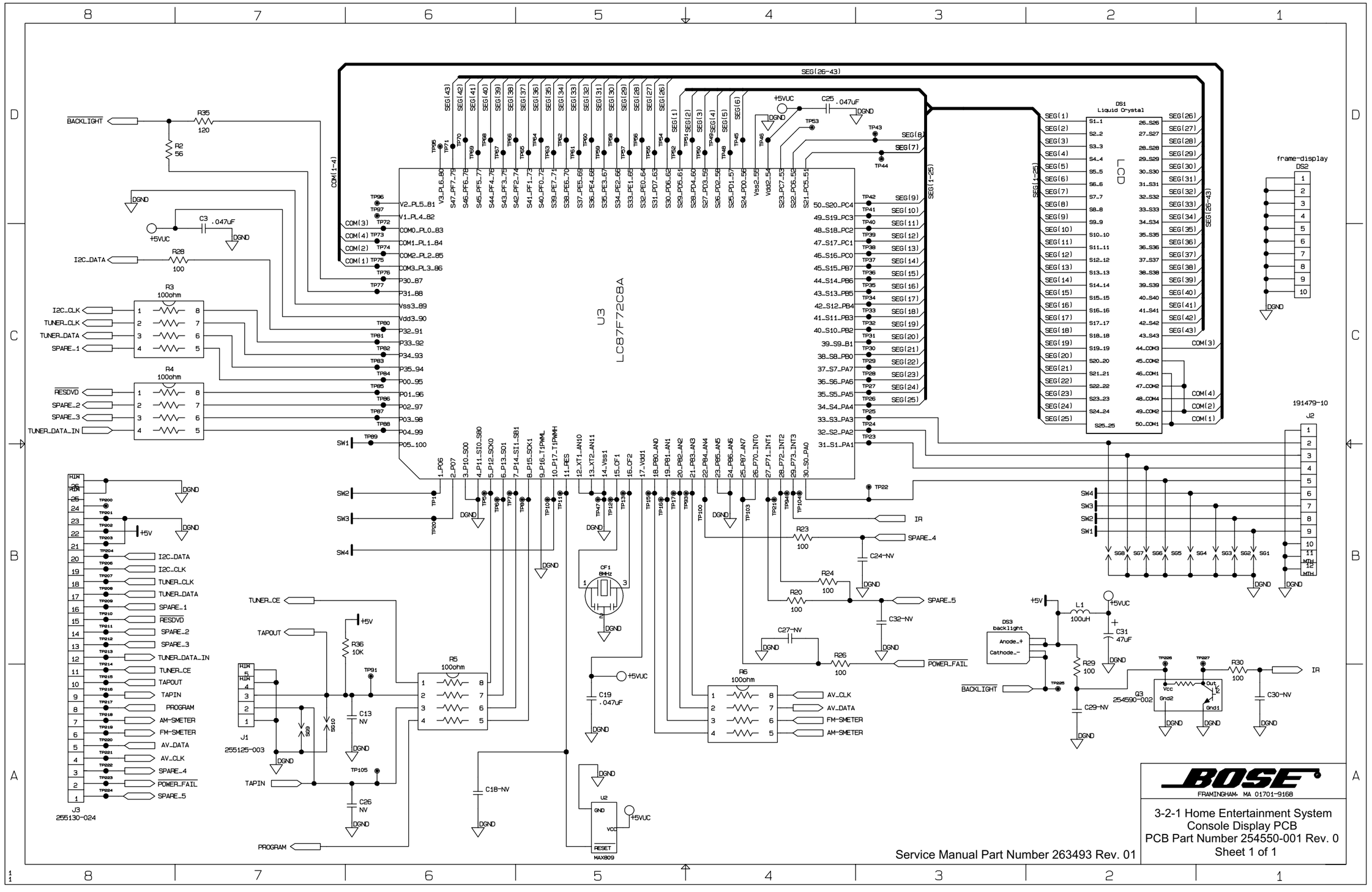
POWER SUPPLY 1

BOSE
FRAMINGHAM, MA 01701-9168

3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 11 of 12

Service Manual Part Number 263493 Rev. 01


+12V
R113-NV
0ohm
U25
L78M10
IN
OUT
GND
R114
0ohm
V_RAW
C117
.01uF
C51
.47uF
TP268
TP269
+10V
C57
.047uF
C50
.047uF
C119
1000pF
C120
1000pF
C3060
.01uF
C3061
.01uF
C3062
.01uF
C3063
.01uF
C3064
.01uF
C3065
.01uF
PGND
255129
J150
DSUB-DUAL BOTTOM CONN
BASS_EQ
SG6505
SG6506
SG6508
SG6509
SG6503
SG6504
CLIP2
MUTE2
C118
.01uF
R118
100
RESDVD
199718-t24
J6500
CONNECTOR TO DISPLAY
I2C_DATA
I2C_CLK
R4042
R4041
100
180pf
C3053-NV
C3054-NV
C3056
C3057
R3156
R3135
TUNER_CLK1
TUNER_CLK
TUNER_DATA1
TUNER_DATA
TUNER_DATA_IN
TUNER_CE
TAPOUT
TAPIN
PROGRAM
AM-SMETER
FM-SMETER
AV_DATA
AV_CLK
POWER_FAIL
WT6500
WT6501
WT6502
SG6500
SG6502
SG6501
C3055
.01uF
C3052
180pf
C3051
180pf
R5093
R5094
R5096
2.0K
R5095
2.0K
C5085
180pf
C5086
180pf
U7000
1_VDD
9_VDD
20_VDD
21_VDD
29_VDD
32_VDD
36_VDD
45_VDD
54_VDD
61_VDD
66_VDD
67_VDD
77_VDD
85_VDD
93_VDD
95_VDD
105_VDD
110_VDD
120_VDD
124_VDD
130_VDD
131_VDD
140_VDD
141_VDD
156_VDD
158_VDD
163_VDD
172_VDD
176_VDD
182_VDD
191_VDD
192_VDD
200_VDD
GND_3
GND_10
GND_14
GND_25
GND_33
GND_35
GND_41
GND_49
GND_57
GND_60
GND_62
GND_68
GND_72
GND_73
GND_81
GND_89
GND_94
GND_99
GND_106
GND_114
GND_119
GND_125
GND_129
GND_135
GND_139
GND_150
GND_154
GND_155
GND_159
GND_167
GND_168
GND_177
GND_181
GND_186
GND_187
GND_196
GND_204
21065
C62
C63
C64
C65
C66
C67
C68
C69
.047uF
U3000
LS588
FB71
FERRITE BEAD
FB70
C82
C86
C87
C88
C79
C83
C80
C84
C81
C85
C74
C70
C75
C71
C76
C72
C77
C73
C78
TP458
TP533
TP457
TP491
TP760
1_Vdd_PLL_0
53_Vdd_PLL_1
105_Vdd_PLL_2
156_Vdd_PLL_3
20_Vdd_IO_0
38_Vdd_IO_1
91_Vdd_IO_2
131_Vdd_IO_3
180_Vdd_IO_4
41_Vdd_C_0
66_Vdd_C_1
84_Vdd_C_2
108_Vdd_C_3
129_Vdd_C_4
141_Vdd_C_5
161_Vdd_C_6
178_Vdd_C_7
203_Vdd_C_8
201_IR_IN
202_XTCLOCK
205_RST_N
206_MFG_TST_0
207_MFG_TST_1
Vss_PLL_0_208
Vss_PLL_1_52
Vss_PLL_2_104
Vss_PLL_3_157
Vss_IO_0_18
Vss_IO_1_35
Vss_IO_2_58
Vss_IO_3_96
Vss_IO_4_119
Vss_IO_5_143
Vss_IO_6_182
Vss_C_0_36
Vss_C_1_63
Vss_C_2_82
Vss_C_3_103
Vss_C_4_126
Vss_C_5_138
Vss_C_6_158
Vss_C_7_176
Vss_C_8_200
DX27MHZ
RESDVD
R33
4.7K
C109
.047uF
+2.5V
+3.3V
+12V
DVD ROM POWER
CONNECTOR
148591-04
J3049
C3049
C3050
SG3048
SG3049
POWER SUPPLY 2
BOSE
FRAMINGHAM, MA 01701-9168
3-2-1 Home Entertainment System
Console Main PCB
PCB P/N: 263069-001 Rev. 0-2
Sheet 12 of 12
Service Manual Part Number 263493 Rev. 01


U3
LC87F72C8A
SEG(26-43)
SEG(1-25)
COM(1-4)
DS1
Liquid Crystal
LCD
frame-display
DS2
191479-10
J2
J3
255130-024
J1
255125-003
BACKLIGHT
I2C_DATA
I2C_CLK
TUNER_CLK
TUNER_DATA
SPARE_1
RESDVD
SPARE_2
SPARE_3
TUNER_DATA_IN
TUNER_CE
TAPOUT
TAPIN
PROGRAM
AM-SMETER
FM-SMETER
AV_DATA
AV_CLK
SPARE_4
POWER_FAIL
SPARE_5
IR
+5VUC
+5V
DGND
R35
120
R2
56
C3 .047uF
R28
100
R3
100ohm
R4
100ohm
R5
100ohm
R6
100ohm
R36
10K
R23
100
R24
100
R20
100
R26
100
R29
100
R30
100
C24-NV
C32-NV
C27-NV
C29-NV
C30-NV
C13
NV
C18-NV
C25
NV
C19
.047uF
C31
47uF
L1
100uH
CF1
6MHz
SW1
SW2
SW3
SW4
DS3
backlight
Anode_+
Cathode_-
Q3
254590-002
U2
MAX809
RESET
Vcc
Gnd1
Gnd2
Out
BOSE
FRAMINGHAM, MA 01701-9168
3-2-1 Home Entertainment System
Console Display PCB
PCB Part Number 254550-001 Rev. 0
Sheet 1 of 1
Service Manual Part Number 263493 Rev. 01

	120V US	100V JAPAN	230V EURO	115V/230V DUAL
S1	———	———	266092-001	———
S2	———	———	———	266091-001
F1	T2.5A 135677-09 (135678-09)	T2.5A 135677-09 (135678-09)	T1.25A L 177311-01250	T2.5A 135677-09 (135678-09)
J1	260116-001	260116-001	260116-001	260116-001
J2	———	———	———	178742-5
J3	193369-002	193369-002	———	———
J4	———	———	193369-002	———
TRANSFORMER	258862-001	261278-001	261276-001	261277-001
VR1	170186	170189	170189	170189
C22	261614-153EB3	———	———	———
C26	———	261614-223EB3	261614-223EB3	261614-223EB3
R12	121245-221000	121245-22264R9	121245-22264R9	121245-22264R9

S2 SHOWN IS 115V SELECTED

Service Manual Part Number 263493 Rev. 01

FRAMINGHAM, MA 01701-9168

3-2-1 Home Entertainment System
Bass Module PCB
Part Number 254574-001 Rev. 1
Sheet 1 of 1

	120V US	100V JAPAN	230V EURO	115V/230V DUAL
S1	———	———	266092-001	———
S2	———	———	———	266091-001
F1	T2.5A 135677-09 (135678-09)	T2.5A 135677-09 (135678-09)	T1.25A L 177311-01250	T2.5A 135677-09 (135678-09)
J1	260116-001	260116-001	260116-001	260116-001
J2	———	———	———	178742-5
J3	193369-002	193369-002	———	———
J4	———	———	193369-002	———
TRANSFORMER	258862-001	261278-001	261276-001	261277-001
VR1	170186	170189	170189	170189
C22	261614-153EB3	———	———	———
C26	———	261614-223EB3	261614-223EB3	261614-223EB3
R12	121245-221000	121245-22264R9	121245-22264R9	121245-22264R9

Service Manual Part Number 263493 Rev. 01

BOSE
FRAMINGHAM, MA 01701-9168

3-2-1 Home Entertainment System
Bass Module PCB
Part Number 266469-001 Rev. 0
Sheet 1 of 1

	120V US	100V JAPAN	230V EURO	115V/230V DUAL
S1	———	———	266092-001	———
S2	———	———	———	266091-001
F1	T2.5A 135677-09 (135678-09)	T2.5A 135677-09 (135678-09)	T1.25A L 177311-01250	T2.5A 135677-09 (135678-09)
J1	260116-001	260116-001	260116-001	260116-001
J2	———	———	———	178742-5
J3	193369-002	193369-002	———	———
J4	———	———	193369-002	———
TRANSFORMER	258862-001	261278-001	261276-001	261277-001
VR1	170186	170189	170189	170189
C22	261614-153EB3	———	———	———
C26	———	261614-223EB3	261614-223EB3	261614-223EB3
R12	121245-2210O0	121245-2226R9	121245-2226R9	121245-2226R9

S2 SHOWN IS 115V SELECTED

Service Manual Part Number 263493 Rev. 01

BOSE
FRAMINGHAM, MA 01701-9168

3-2-1 Home Entertainment System
Bass Module PCB
Part Number 268858-001 Rev. 0
Sheet 1 of 1