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Troubleshooting Guide

Powered Acoustimass® -25 and -30 Series II Speaker System AM-25P II/ AM-30P II Digital Bass Module

Part Number 199401-TG1 Rev. 00

Troubleshooting Guide Overview

This troubleshooting guide is divided into three sections. The section that you use will be determined by the items available to you for use in troubleshooting. Section 1 allows for limited troubleshooting due to limited availability of items. Section 3 is the most complete troubleshooting section.

Section 1: Bass Box Only Procedures is to be used if you have a bass module to troubleshoot, but no head unit or PC to turn the bass module on. It will take you through a troubleshooting process which will allow you to power up the amplifier PCB by itself, as well as some troubleshooting procedures for the Digital Signal Processor PCB, should it be at fault.

Section 2: Bass Box with a Head Unit Procedures is to be used if you have a bass module and a head unit, but no PC. In this section you will be able to connect an audio signal to the head unit and turn the bass module on. This will allow you to signal trace and troubleshoot the amplifier PCB and the Digital Signal Processor PCB.

Section 3: Computer Aided Troubleshooting Procedures is to be used if you have a PC that can be used to communicate with the Digital Signal Processor PCB of the bass module, and is the preferred method of troubleshooting. In this section you will be able to determine the EQ curve of the module under test as well as put the module into different test modes for easier troubleshooting.

There is an Appendix at the back of this guide containing information such as simplified schematic diagrams, block diagrams, frequency response curves, tables, and computer setup information. See the table of contents for a complete listing.

Table of Contents

Table of Contents (continued)

Section 1

Bass Box Only Procedures

Section 1 Contents

Click here to return to the main table of contents

Test Set-up Parameters and Equipment

Use the disassembly/assembly procedures found in the AM25/30P Series II service manual part number 199401, to access the PCBs.

Speaker Output Loading:

Unless testing the amplifier for its rated power output, all tests are to be performed with the speaker outputs unloaded. The amplifier can be tested with loads as long as the PCB is still mounted in its heatsink.

Left Front Output:	8 Ohm, 1%, 50W
Right Front Output:	8 Ohm, 1%, 50W
Center Output:	8 Ohm, 1%, 50W
Left Surround Output:	8 Ohm, 1%, 50W
Right Surround Output:	8 Ohm, 1%, 50W
Bass Channel Output:	4 Ohm, 1%, 100W

Equipment Requirements:

Test Cable part number 199527

Test Set-up

1. Set up the bass box as shown in the Test Setup Diagram, (Figure 45. in the Appendix)

Note: Since you have only the bass box for troubleshooting and are not using a PC to communicate with the module, you will not use the connectors for the PC, the audio jacks or the digital input jack on the test cable. You will use the 3.5mm mono jack and the 9 Volt battery to turn the module on.

When the module is powered on using the battery or a DC power supply, it will come up with the amplifiers muted. You will not be unmuting the amplifiers and passing an audio signal while performing the tests in this section.

If the module passes the tests in this section, you can use the amplifier test procedures to test the amplifier board on its own and verify that it is okay.

Bass Box Only Troubleshooting Procedures

1. Module Power-up

1.1 With the top cover removed and the line cord connected to an AC mains source, connect the 9 Volt battery to the 3.5 mm mono plug, TIP (+) RING (-), located on the test cable. This will power up the module.
Note: If you disconnect AC mains from the module, you will need to disconnect and reconnect the 9 Volt battery to the 3.5 mm plug to get the module to power up again.

2. Check for Voltage at the Transformer

2.1 Check for voltage at the transformer secondary. If there is voltage at the transformer secondary, skip to procedure 4. If there is no voltage on the transformer secondary, continue on to step 2.2.

Bass Box Only Test Procedures

2.2 Check for AC mains voltage, 120 or 240 VAC at the transformer primary. If there is voltage at the transformer primary, remove AC mains power and check the thermal fuse in the transformer primary. Replace the transformer if the internal fuse is open.
If there is no voltage at the transformer primary, proceed as follows.

2.2.1 Check the fuse located on the PCB.
2.2.2 Ensure that the 18 conductor ribbon cable is fully seated.
2.2.3 With the line cord connected, connect the 10V turn-on signal to the 3.5 mm mono plug located on the test cable. Check the voltage at U300 pin 1.
If it is ~1.25 VDC, U300 should be on, turning triac D302 on. Go to procedure 4.
If it is ~0.8 VDC, the opto-coupler U300 is crowbarred off keeping triac D302 off, which connects AC mains voltage to the transformer primary. Disconnect power to the bass module and go to procedure 3.

3. U300 Crowbarred Off, Triac D302 Off
Note: Refer to Figure 50. Protection Circuit Simplified Schematic Diagram in the Appendix for an overview of the protection circuit.

3.1 If the bass module crowbars off (shuts off) immediately (<50 msec) after applying the 10V turn-on signal, check the “protect” signal at J8 pin 6. If the voltage on J8 pin 6 is greater than approximately +0.7 VDC, it will turn on Q202 and if the voltage is less than approximately -0.7V, it will turn on Q203. Turning on either Q202 or Q203 causes Q202 and Q203 to latch and this will activate the crowbar. If there is a fault condition at J8 pin 6, check the ±12 VDC, ±17 VDC and ±34 VDC power supplies. If the ±12 VDC power supply is not working and the ±34 VDC power supply is working, check resistive fuses R714 and R713 located on the amplifier PCB. A failed component could be causing one or more of these supplies to sag, causing the unit to crowbar off. If the DC power supplies are working, continue onto step 3.2.

3.2 DC offset at the output of the bass amplifier J703 pin 2 (+) and pin 1 (-) will produce a fault condition ‘protect” voltage (greater than approximately ± 0.7 VDC) at J8 pin 6. Check the components in the bass amplifier with an Ohmmeter.

3.3 If the bass module crowbars off after approximately 3 seconds, there could be DC offset on one or more satellite outputs. The satellite outputs are summed through the “speaker output DC offset” circuit (SD251571, grid location A7). The output of this circuit, P66, is sent to the microcontroller U202 pin 25. In normal operation, the voltage at U202 pin 25 should be 2.5 VDC. If the voltage strays more than 1 VDC from the normal 2.5 VDC, microcontroller U202 pulls pin 39 (P22) to ground (normally high impedance) pulling R308 to ground latching the circuit consisting of Q302 and Q303 (SD251571, grid location B4). This latch circuit, when latched, will shut off the opto-isolator U300, which will shut off the triac D302 disconnecting AC from the primary of the transformer.
Note: U202 pin 26 is connected to U202 pin 39. The head unit does not send an “ON” command to the bass module. The uC knows when the power has just come up by watching the status of the 10V turn-on voltage via pin 26, which is connected to the same circuit mentioned above that the uC uses to shut down the triac.

3.4 If everything checks out up to this point and the bass module is not crowbarred off, then go to procedure 4.

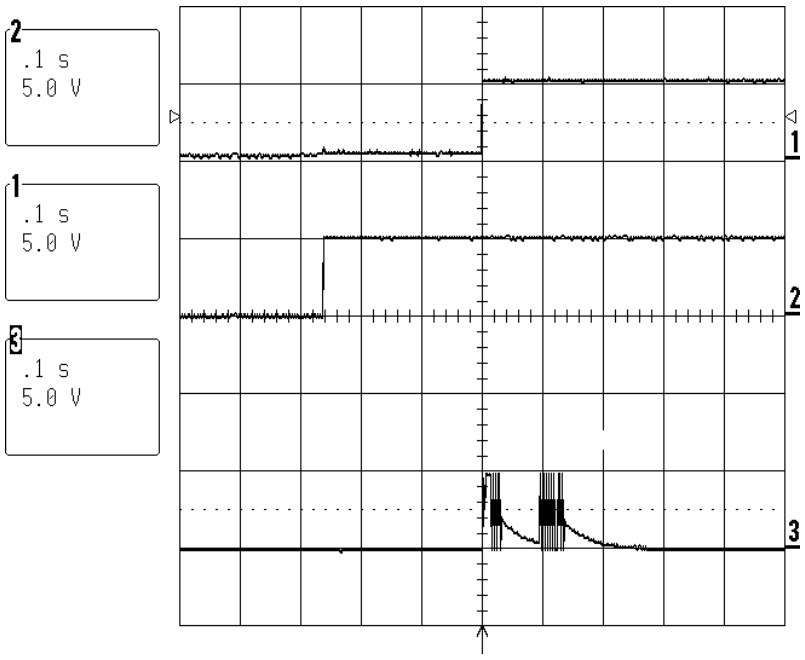
Bass Box Only Test Procedures

4. Microprocessor Circuit Check

4.1 The serial data output leaves the DSP PCB at J5 pin 11 (U202 pin 43, signal name “TTY OUT”) and the boot prompt can be checked here at power-up with an oscilloscope. The first thing the uC is supposed to do when it comes out of reset is to print the following to the “debug” output J5 pin 11.

**
%0001#01

This is visible as two bursts of activity. One immediately following the rising edge of the RESET line (**) and one about 50 msec later (%0001#01). After printing the boot prompt, the uC will only print error codes. Thus, a lack of activity on this signal after the initial two bursts is expected. Short bursts of activity is likely to be the uC printing out an error code. Refer to Figure 1.



Upper trace: RESET (active low) pulse U202 pin 14 or U200 pin 2
Middle trace: +5V supply
Lower trace: Serial data from uC, J5 pin 11

Figure 1. Scope Photo of Boot Prompt at J5 Pin 11

4.2 If there is no boot prompt at U202 pin 43, then check for the following; +5 VDC at U202 pin 40 and U202 pin 18, 8 MHz clock on both sides of X600, reset pulse at power-up at U202 pin 14. If the +5 VDC, 8 MHz clock and reset pulse are okay and there is no boot prompt, then the uC has failed. Replace the uC U202.

4.3 If everything looks okay up to this point, you can go to the amplifier hookup procedures and the amplifier test procedures to test the amplifier board on its own if you suspect it is the problem. If you suspect the DSP board, you can go to the DSP troubleshooting procedures to further troubleshoot the DSP board, or you can send it in for repair or replacement.

Amplifier PCB Hook-Up Procedures

This procedure will allow you to connect and operate the amplifier PCB by itself, with no DSP board connected. This will enable you to determine whether the amplifier PCB or the DSP PCB is defective.

If you can turn the the amplifier PCB on, and perform the test procedures later in this section, then the amplifier PCB should be fine and the DSP board is most likely at fault. You can isolate the failure on the DSP board further using the DSP troubleshooting procedures later in this section.

Below is a picture of the cable for the audio outputs on the amplifier PCB which will be connected to J701 on the amp PCB. This cable can be built using the interconnect cable, Bose® part number 190701-001, and soldering wires to the connector end.

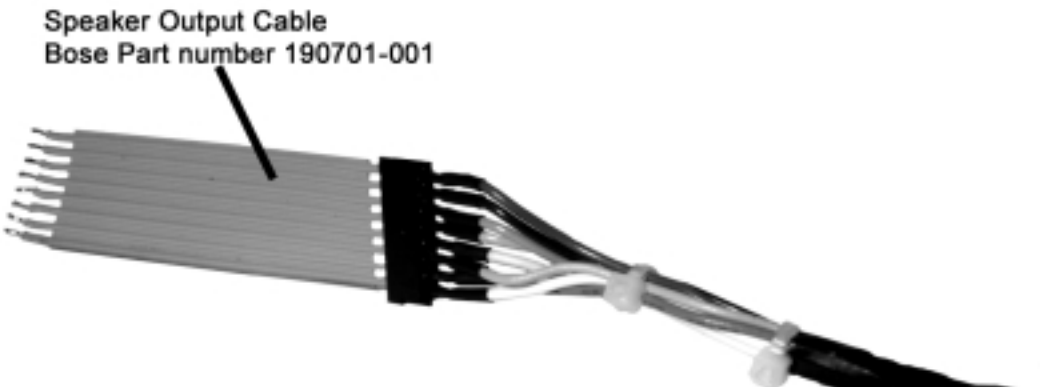


Figure 2. Cable for Amplifier Output Connection at J701

Figure 3. Output Wire Connection View at J701

Amplifier PCB Hook-Up Procedures

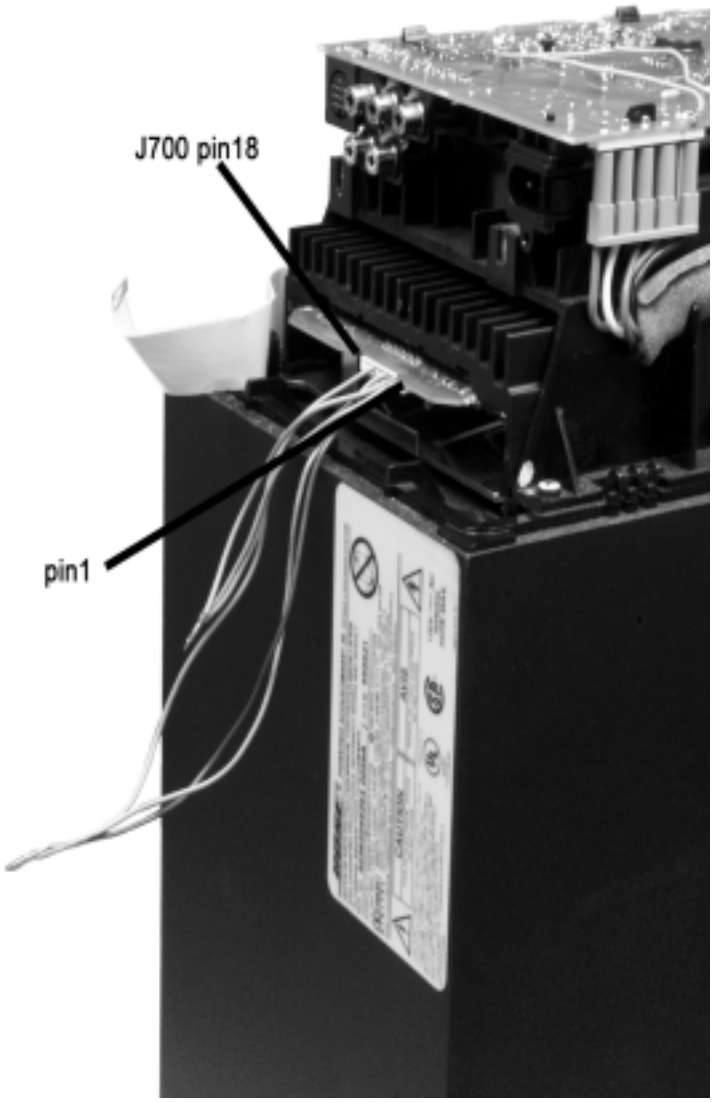


Figure 4. Input Wire Connection View at J700

1. Remove the top cover assembly using the disassembly/assembly procedures located in the service manual part number 199401. The first PCB board you see is the DSP PCB (it has a shield on it). Disconnect the gray interconnect cable from the top PCB. Disconnect the white ribbon cable from the bottom PCB (amplifier board).

2. Connect individual 22 AWG, solid core wires to connector J700 at the L/R/C/LS/RS output jack. This is the location where the white ribbon cable was connected. Connect the 8-wire test cable (see Figure 2) to the 8-wire gray cable coming from the amplifier PCB. Refer to Figure 4 and the Input Connector Table on page 11 for the following instructions. Connect a wire to pins 2, 3 and 4 of the connector J700. These are the mute lines used for un-muting the amplifier outputs. Connect individual wires to pins 12 (right channel), 10 (left channel), 9 (center channel), 8 (bass channel), 7 (left surround) and 6 (right surround). Leave the woofer connector where it is. You should connect the wires one channel at a time. Connect a single wire to pin 11 for a signal ground and connect a jumper wire from the audio signal ground to the shield on the DSP PCB.

Amplifier PCB Hook-Up Procedures

3. Jumper point A to point B on the PCB as shown in Figure 5 below. Point A is the fuse clip and Point B is J7 pin 1. There are two versions of the Triac, one is a through hole device and the other is a surface mount device. This procedure will work with either version.

4. Connect an oscilloscope to the pair of wires for the channel under test as wired in step 2. Refer to the Output Connector Table on page 11 for the for a listing of the correct pair of wires to test the channel desired (L, R, C, LS or RS).

5. Apply a 250 Hz, 63 mVrms signal to the input wires connected in step 2, and connect the audio signal generator ground to pin 11 and the shield.

6. Apply AC mains voltage to the AC input jack. Be careful around the connector J7 on the top PCB. This connector has the line voltage on it.

7. Connect a +5 Volt DC supply to connector J700 pins 2, 3 and 4 (+5 volt mute lines). This will unmute the amplifiers.

8. At this point you should be able to hear audio coming out of the bassbox and/or see a sinewave on the oscilloscope. Check all of the outputs. If you can pass an audio signal through all six outputs, check the outputs at the ribbon cable at J701 with a satellite speaker (or an 8 Ohm load). Using the Amplifier Test Procedures on page 12, check each of the outputs for proper operation. If all channels are operating to specification with the loads according to the test procedures then you can assume the DSP PCB to be defective.

9. At this point, you can go to the DSP PCB troubleshooting procedures, or replace the DSP PCB.

10. If there is no output from the satellite or bass channels, then you will need to troubleshoot the amplifier PCB.

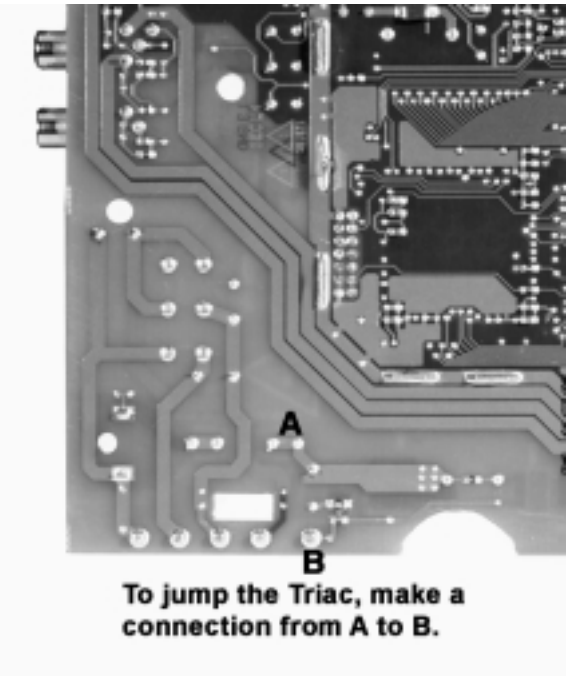


Figure 5. Triac Jumping View on DSP PCB

Amplifier PCB Hook-Up Procedures

Input Connector Table

J700	Description	Note
Pin 1	Not used	
Pin 2	Logic signal +5Volts	
Pin 3	Logic signal +5Volts	
Pin 4	Logic signal +5Volts	
Pin 5	Left and right audio return	
Pin 6	Right surround audio input	
Pin 7	Left surround audio input	
Pin 8	Bass audio input	
Pin 9	Center audio input	
Pin 10	Left audio input	
Pin 11	Input ground reference	
Pin 12	Right audio input	
Pin 13	Protect	
Pin 14	-12 Volts	
Pin 15	Input ground reference	
Pin 16	+17 Volts (fused)	
Pin 17	Input ground reference	
Pin 18	+12 Volts	

Output Connector Tables

J701	Description	Note
Pin 1	Center channel audio return	
Pin 2	Left audio output	
Pin 3	Center audio output	
Pin 4	Right audio output	
Pin 5	Left and right audio return	
Pin 6	Right surround audio return	
Pin 7	Left/right surround audio return	
Pin 8	Left surround audio output	

J703	Description	Note
Pin 1	Bass audio return	
Pin 2	Bass audio output	

Amplifier Test Procedures

Note: Unless you are testing the amplifier for its rated power output, all tests are to be performed with the speaker outputs unloaded. The amplifier can be tested with loads as long as the PCB is still mounted in its heatsink.

Speaker Load Table

Output	Location	Recommended Load
Bass Channel output	J703 pin 2 **+**, J703 pin 1 **-**	4 Ohm, 1%, 100 Watts
Left Channel output	J701 pin 2 **+**, J701 pin 5 **-**	8 Ohm, 1%, 50 Watts
Right Channel output	J701 pin 4 **+**, J701 pin 5 **-**	8 Ohm, 1%, 50 Watts
Center Channel output	J701 pin 3 **+**, J701 pin 1 **-**	8 Ohm, 1%, 50 Watts
Left Surround output	J701 pin 8 **+**, J701 pin 7 **-**	8 Ohm, 1%, 50 Watts
Right Surround output	J701 pin 6 **+**, J701 pin 7 **-**	8 Ohm, 1%, 50 Watts

1. Bass Channel Gain Test

1.1 Apply a 200 mVrms, 300 Hz signal to the input wires for the bass channel input at connector J700 pins 8 (signal) and 11 (ground). Also ground pin 11 to the shield.

1.2 Reference a dB meter to the input. Measure the gain at the output. It should be +21.5 dB ± 2 dB.

1.3 Change the input signal to 20 Hz. Reference a dB meter to the input. Measure the gain at the output. It should be +21.5 dB ± 2 dB.

2. Left, Right, Center and Surround Channel Gain Test

2.1 Apply a 200 mVrms, 100 Hz signal to the input wires on connector J700 pins 6 (RS), 7 (LS), 9 (C), 10 (L), 12 (R) and pin 11 (ground).

2.2 Reference a dB meter to the input. Measure the gain at the output of each channel. It should be +11.5 dB ± 2 dB.

2.3 Change the input signal to 15 kHz. Reference a dB meter to the input. Measure the output of each channel. It should be +11.5 dB ± 2 dB.

3. Bass Channel Distortion Test

3.1 Connect a 4 Ohm load to the Bass channel output at J703 pins 1 (-) and 2 (+).

3.2 Apply a 100 mVrms, 100 Hz signal to the input wires for the bass channel input at connector J700 pins 8 (+) and 11 (-).

3.3 Measure the distortion at bass channel output. It should be <0.4% at 0.5 Watts output.

3.4 Change the input level to 1.35 Vrms.

3.5 Measure the distortion at the bass channel output. It should be <0.3% at 65 Watts output.

4. Left, Right, Center and Surround Channel Distortion Test

4.1 Connect each of the outputs to an 8 Ohm load. Apply a 533 mVrms, 1 kHz signal to the input wires at connector J700 pins 6, 7, 9, 10, 12 and 11.

4.2 Measure the distortion at the outputs. It should be < 0.3% at 0.5 Watts output.

4.3 Change the input level to 4.1 Vrms.

4.4 Measure the distortion at the outputs. It should be < 0.3% at 30 Watts output.

5. DC Offset Test

5.1 Disconnect all loads. Ground all audio inputs and apply a 5 Volt DC signal to the mute lines pins 2, 3 and 4.

5.2 Measure the DC offset on all the outputs, it should be < 20 mVdc.

DSP PCB Troubleshooting Procedures

DSP PCB Troubleshooting Procedure Setup

1. Remove all test cables used in the amplifier test procedures, if necessary, and reassemble the electronics module, leaving the top cover off. Refer to the Digital Bass Box service manual, Bose® part number 199401 for disassembly/assembly procedures.

2. Using the test cable, part number 199527, connect the module as shown in Figure 45. Test Setup Diagram shown in the appendix. Using this setup, the amplifiers will not be un-muted, so you won't be able to pass an audio signal through the module, but the voltages and signals shown in the DSP troubleshooting section will be present. You will not be connecting a PC or an audio or digital signal source. You will use the 3.5mm mono jack and a 9 Volt battery to turn the module on after applying AC mains power through the power cord.

Note: If you disconnect AC mains from the module, you will need to disconnect and reconnect the 9 Volt battery to the 3.5 mm plug to get the module to power up again.

1. Quick Check/Possible Problems With DSP PCB

1.1 Because the DSP IC's legs are very fine, there is a chance for shorts or opens. Probing can result in shorting them. Boot data can be garbled due to a short or open on the DSP IC pins.

1.2 The 40 MHz oscillator, CR400, might not be working.

1.3 There might be a broken "via" in the PCB. This is a hole in the PCB that connects traces on the top side of the PCB to traces on the bottom side of the PCB. This type of problem can be difficult to isolate.

1.4 If the problem has not been isolated, go to procedure 2.

Note: Refer to Figure 8. DSP PCB Test Point Locations Layout Diagram, Solder Side on page 19 for the following procedures.

2. Miscellaneous DSP PCB Troubleshooting Tips

2.1 +17V, ±12V Power Supplies

The PCB draws power from three different supplies:

2.1.1 +17V unregulated, at about 250 mA when everything is running normally. The +17V supplies the unregulated voltages for the two voltage regulators on this PCB: the +5V linear regulator U1, and the 3.3V switching regulator U500. The +17V is brought onto the PCB from J8 pin 3.
Note that the +17V unregulated supply can vary from about +17V to as low as +10V, depending on conditions. On the bench, the value may be more typically +15V or so. Whatever the exact voltage, in this document it will be referred to as the "+17V" supply.

2.1.2 ±12V, at about 40 mA or so. The ± 12V supplies are for the op-amps U103 — U105. +12V is brought onto the PCB from J8 pin 1, and -12V is supplied from J8 pin 5.

2.2 +5V Supply

Check the +5V supply first, since the +5V powers the microcontroller and without it, nothing else works. Check the following points:

2.2.1 At the input side to the +5V regulator U1. This is a typical 7805 3-terminal linear regulator, so it needs at least 7.5V at the input to stay in regulation. If there is +17V at J8 pin 3, but no voltage at the input side of U1, check the components in between (R10 and R11, large SMD resistors on the bottom side).

2.2.2 At the output side of the +5V regulator. Check that the 5V output is clean and that the regulator is not oscillating. The regulated +5V is supplied to the rest of the PCB via a couple of filter components, so check for +5V at the following points:

2.2.3 U102 pin 20; if no +5V here, check L200 (bottom side, between U101 and U104).

2.2.4 U100 pin 40; if no +5V here, check both L2 (top side, near U100 pin 20) and L1 (bottom side, directly under U100).

2.3 8 MHz Clock

The micro requires an 8 MHz clock to run. This clock is developed by an internal oscillator which requires an external ceramic resonator (X600). Check for the 8 MHz clock at:

2.3.1 Ceramic resonator X600 (top side, next to U202). There should be a roughly sinusoidal waveform, 0V to 5V, on both sides of X600. See Figure 51 in the Appendix.
If there is no 8 MHz clock, possible causes are:
- No +5V; check L200.
- Poor soldering

If the 8 MHz clock is present at X600, and its amplitude is roughly 5Vpp, but the microcontroller won't issue a boot prompt or turn on the 3.3V power supply, possible causes are:
- Dead micro.
- A missing RESET pulse at power up. Power the board down and back up again, and verify that the micro is getting a healthy RESET pulse at power up. The reset IC (U200, SOT-23 bottom side) should hold the micro's RESET input (pin 14) low for about 250 msec after the +5V supply has stabilized. The RESET input should transition from low to high cleanly and briskly. If it appears to be floating, check R280.

2.4 3.3V Supply

The 3.3V supply is supplied by the switching regulator IC U500. This IC works by rapidly switching its output between +17V and ground; the output filter (L500 and C500) blocks the 100 KHz switching waveform and passes only the average 3.3 VDC.
Note that the micro can turn U500 on or off, via one of its output ports (U202 pin 41) and Q500. U500 powers up off with its "soft-start" node (pin 19) clamped to ground, which inhibits operation, and it remains in this state until the micro boots successfully and pulls the base of Q500 to ground. The point to remember is that the 3.3V supply does not power up until after the micro boots successfully. Assuming that the micro does boot successfully, check U500 for the following waveforms at the following points:

2.4.1 +17V on both sides of the surface-mount inductor L501 (top side).

2.4.2 5.1 VDC at U500 pin 18. This is a reference voltage generated by U500. Its presence here on pin 18 will show that U500 is getting power.

2.4.3 Check that U500 pin 11 is connected to ground. This pin is U500's ENABLE input; if it isn't grounded, U500 shuts down.

2.4.4 Check that the base of Q500 (bottom side) or U202 pin 41 (same node) is pulled to ground. If Q500 is turned on, U500 shuts down. This node is pulled up to +5V with R282 (sheet 2); the micro pulls this node low after it boots. If the micro doesn't boot, U500 never turns on.

2.4.5 100 KHz switching waveform on the +17V side of the toroidal inductor L500. This waveform should switch rapidly (<100 nsec) between about -0.35V and VCC, with an average DC voltage of 3.3V, Figure 40. If the voltage at this node dips well below -0.35V, then check D500 (bottom side).

2.4.6 If still no luck, check L500. If it's a toroidal inductor, check that it's properly soldered to the PCB.

2.5 11.2896 MHz Codec Clock

If the micro and DSP appear to have booted properly, check the codec U100 for signs of health. The codec does not power up in a useful state all by itself; the micro must program a number of internal registers via the I 2 C buss inputs to the codec . (I 2 C is a 2 wire serial buss; one line for the data, one line for the clock.) To quickly determine if the codec was properly initialized by the micro, check for;

2.5.1 0V — 5V, 11.28 MHz sine wave on both terminals of the crystal CR100. If the 11.28 MHz clock, Figure 38, is not oscillating, possible causes might be:

- No +5V power to the codec U100. Check both power pins (19 and 40). If there's power on one but not the other, check L1 and R3 (bottom side, directly under U100).
- I 2 C data or clock signals missing. Check for digital activity (0V — 5V) on these signal paths:

  U202_32 — R253 — U100_4
  U202_33 — R265 — U100_3

Once the micro boots, there is a fair amount of regular activity on these two lines. The micro checks the codec's error status register about every 5 msec , so if these lines are silent, suspect a bad micro or a broken connection somewhere in between the micro and the codec. Also, the micro will output an error code if it detects an on going problem with the I 2 C.

- A problem in the network of components around CR100, R175, R176, C139, C140. Check CR100
- Codec power-down input at pin 8. Normally, this signal is pulled up for proper codec operation. When this pin is low, the codec enters a low-power reset state. The micro will pulse this line low for a few msec to reset it prior to initialization.

If this line is held continuously low for some reason, the codec's oscillator won't operate, and the analog reference voltage (about 2.3V) at pin 16 disappears.

If the 11.28 MHz codec clock is oscillating, then verify the following digital output signals from the codec:

2.5.2 Bit clock at R186, U100_38: 11.2896 MHz square wave

2.5.3 Frame clock at R185, U100_37: 44.1 KHz square wave

2.5.4 Output data, U100_36: “irregular” digital activity at R187, similar to Figure 44.

2.6 Codec Revision Code

The CS4226 codecs must be rev. G or higher. Specifically, the rev. code must NOT be “C”. The rev. letter is the letter immediately preceding the date code silkscreened on the IC, e.g.
CRYSTAL (logo)
CS4226-KQ EP (part number)
JTAAXG9819 (rev. G, date code 9819 [19th week of ‘98])

2.7 DSP 40 MHz Clock

2.7.1 The DSPs run on a 40 MHz clock; the easiest place to check for this is at J401_4 (J401 is the un-loaded 14-pin connector between DSP2 and the shield fence). This is a buffered version of the 40 MHz clock that drives the DSP. This clock has very fast edges (3 nsec rise times), so if you’re using a low-quality scope probe, don’t be too alarmed by what you see. A cheap scope probe or a long or missing ground lead will distort this signal beyond recognition. In this case, it’s ugly, but it’s not a serious issue, all you’re trying to do is verify that the clock is oscillating. However, pay attention to the frequency, this is a third overtone oscillator, which means it may prefer to oscillate at 13.333 MHz (40/3). If the network of components around CR400 is incorrect in some way, it may prefer to oscillate at some frequency unrelated to what’s printed on the crystal.

2.7.2 40 MHz clock frequency at U104 pin 4: 40 MHz

If there’s no 40 MHz clock at all:
- Check U400 (LCX00) for proper soldering, and check for 3.3V on U400_14.
- Check to make certain that all the components around the crystal (C402, C403, R411, R412, R409 — bottom side, under CR400) are OK.

2.8 DSP Reset Pulse

Check for a clean reset DSP reset pulse at the collector of Q200 (top side, near U102). At power-up, Q200 is biased on, driving the collector low, until the micro boots properly. After the micro boots, it turns Q200 off and allows the DSP reset line to be pulled high. This signal is digital, and should be either at 0V or at 3.3V.

2.9 Digital One-shot U106

U106 is a flip-flop wired up to produce a narrow pulse on the falling edge of the 44.1 KHz clock. Without the signal that this IC produces, the DSP can’t send or receive from the codec properly. Inputs to U106:

2.9.1 U106 pin 1: 44.1 KHz clock

2.9.2 U106 pin 5: 11.28 MHz clock

2.9.3 Output from U106 pin 13: 100 nsec pulse, at 44.1 KHz rate, similar to Figure 42.

2.10 5V / 3.3V Level Translators

The micro (U202) and the codec (U100) run on +5V, while the DSPs run on 3.3V. There are a couple of level-translator ICs required to bridge this gap:

U101, a 74LCX244, a 3.3V part which has “5V tolerant” inputs.
U102, a 74ACT244, a 5V part with input logic thresholds that are compatible with 3V logic (“TTL”, or 0.8V/1.5V).

Since there’s a problem somewhere on the PCB, it isn’t safe to assume that you’ll be able to observe any digital activity on the pins listed below, although normally there would be. Mainly what we’re looking for is evidence that a buffer gate isn’t buffering; i.e., a signal is present on the input, but there’s no similar signal on the output.

From the codec U100 to DSP1:
U101_13 —> U101_7
U101_15 —> U101_5
U101_17 —> U101_3

From DSP1 to the codec U100
U102_2 —> U102_18
U102_4 —> U102_16

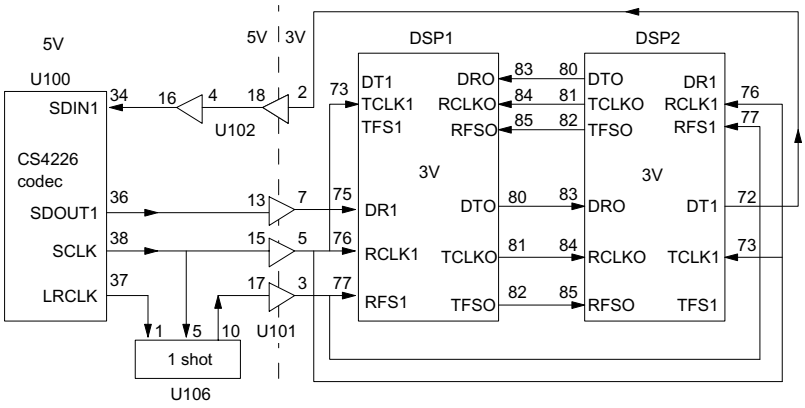


Figure 6. Codec to DSP, Digital Audio Signal Path

From the micro to DSP1:
U101_4 —> U101_16
U101_2 —> U101_18

From DSP1 to the micro:
U102_15 —> U102_5
U102_17 —> U102_3

From the micro to DSP2:
U101_8 —> U101_12
U101_6 —> U101_14

From DSP2 to the micro:
U102_11 —> U102_9
U102_13 —> U102_7

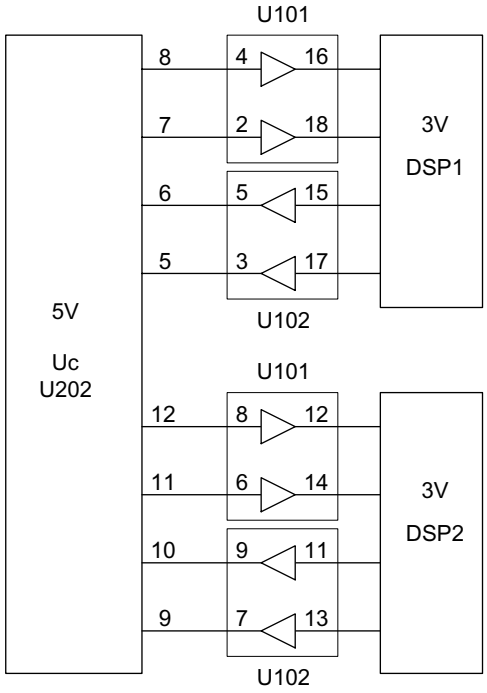


Figure 7. Micro to/from DSPs

2.11 Evidence that the DSPs have booted

2.11.1 DSP Output Ports

Observe the following signals as the power to the PCB comes up:
U102_15
U102_11
These signals are part of the communications buss between each DSP and the microcontroller, and are pulled up to +3.3V by resistors. One of the very first things that either DSP will try to do is talk to the micro, which initially requires pulling these signal lines low.
If DSP1 is working, U102_15 will show some activity about 100 msec after the 3.3V supply comes up.

If DSP2 is working, U102_11 will show some activity about 100 msec after the 3.3V supply comes up.
If these signals power up to 3.3V and sit there doing nothing, then one or both of the DSPs failed to boot.

2.11.2 Boot Activity on External Address Buss

The DSPs have no internal program ROM, and must boot from the external PROM.
The boot happens in two stages. First, a short (256 words) boot loader program is loaded automatically; second, the boot loader program is executed. Typically, the boot loader program loads the other 99% percent of the PROM contents into the DSPs.

The first stage of the boot is hard-wired into the DSPs, so as long as the DSPs have power, a 40 MHz clock, and a few other signals, the first stage of the boot always happens when the reset line goes high. However, the second stage happens only if the boot loader program actually works, which of course it won't if the DSPs are trying to boot from an empty or damaged PROM, or if the data lines or address lines between the PROM and the DSPs are shorted together.

Observe the activity on PROM pin 30 at power-up. A successful boot will show a flurry of activity about 30 msec long immediately following the release of the DSP reset line (collector of Q200). An unsuccessful short boot won't last more than 300 usec. If it becomes clear that the DSPs aren't booting, the problem might be caused by:

- Solder problems affecting the fine pitch leads on the DSPs. This is the most common source of DSP boot errors. Examine the leads of each DSP under an illuminated magnifying glass, checking for shorts (which are usually pretty easy to see) and opens (which sometimes are not).

- Solder problems affecting the 4 resistor r-packs. These are attached to some critical DSP buss signals, so a loose connection here can cause problems.

DSP PCB Troubleshooting Procedures

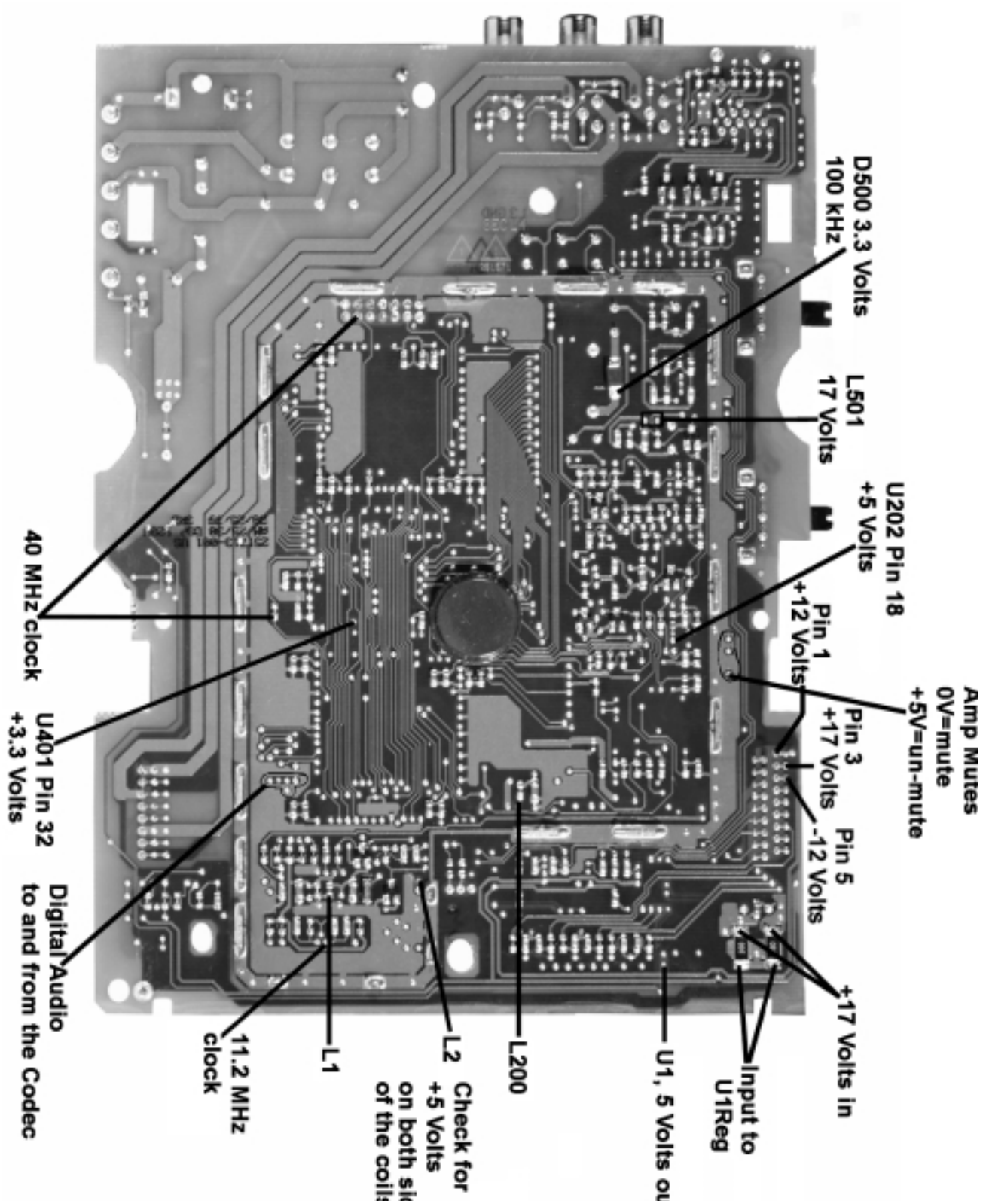
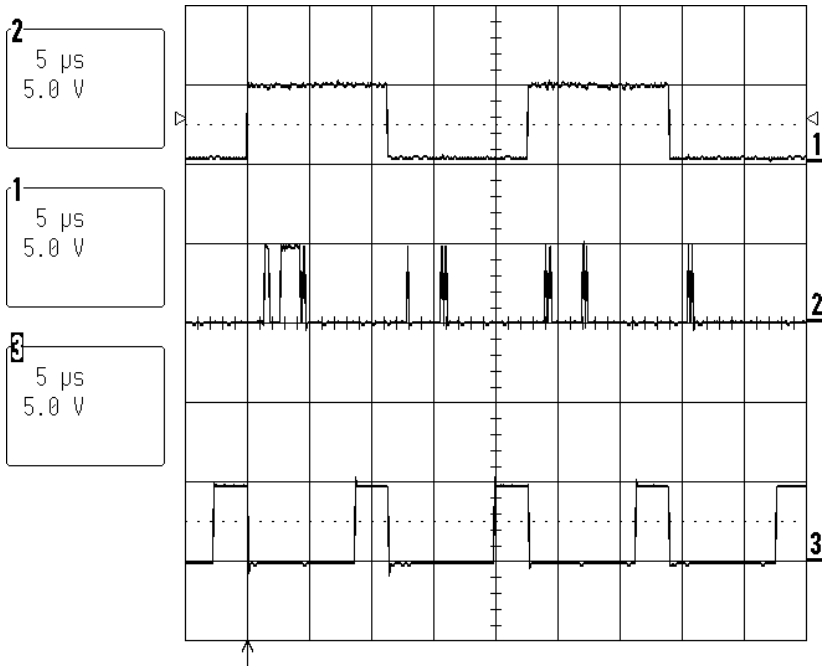


Figure 8. DSP PCB Test Point Locations Layout Diagram, Solder Side

Scope Photos

The bass module is muted when it is first powered up and will not un-mute until it receives an “un-mute” or “volume up” command.

Muted data consists of all zeroes; this condition is shown in the lower trace of the codec (U100) scope photo, mute condition.



Upper trace: LR_CLK (U100 pin 37) 44.1 kHz square wave
Middle trace: SDOUT1 (U100 pin 36) serial data out
Lower trace: SDIN1 (U100 pin 34) serial data in

Figure 9. Codec (U100) Scope Photo, Mute Condition

The significance of the SDOUT1 signal (U100 pin 36) is that it represents the digital audio data at the start of the digital audio signal path. This data is transmitted serially to the DSP1, which requires three signals to accept it:

SCLK (U100 pin 38): to clock the serial data in
LRCLK (U100 pin 37): to indicate the start of each audio sample
SDOUT1 (U100 pin 36): the serial audio data

The significance of the SDIN1 signal (U100 pin 34) is that it represents the output of the digital audio signal chain. The data is shifted out from DSP2 using the clock signals mentioned above. If this signal is dead, DSP2 is most likely not running. See Figure 44.

Scope Photos

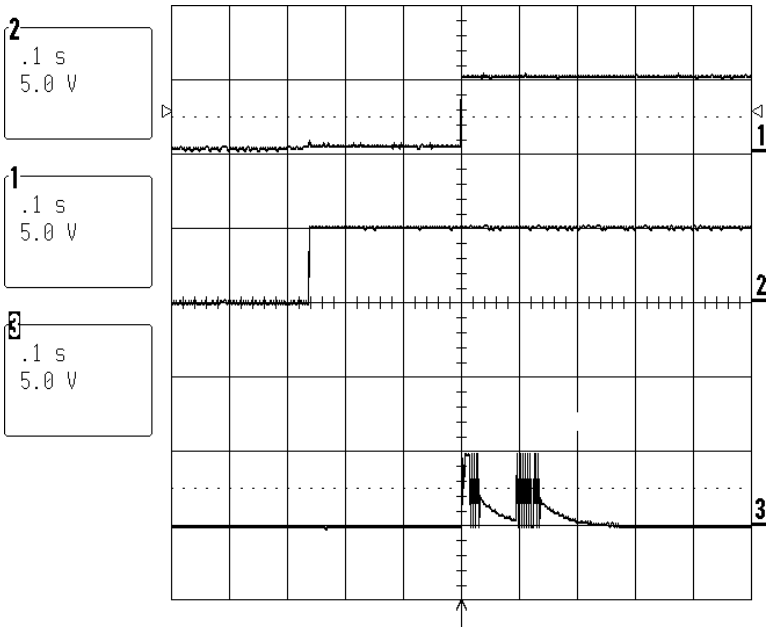


Figure 10. Microcontroller (U202) Scope Photo, Power Up

Upper trace: RESET pulse (active low), U202 pin 14 or U200 pin 2
Middle trace: +5V supply
Lower trace: Serial data from uC, J5 pin 11

The first thing the microcontroller supposed to do when it comes out of reset is to print the following to the debug output J5 pin 11.

**
%0001#01

This is clearly visible as two bursts of activity (4800 BAUD), one immediately following the rising edge of the reset line (**) and one approximately 50 msec later (%0001#01).

After printing the boot prompt, the Uc will only print error codes. Thus, a lack of activity on this signal after the initial two bursts is expected. Short bursts of activity is likely to be the uC printing out error codes.

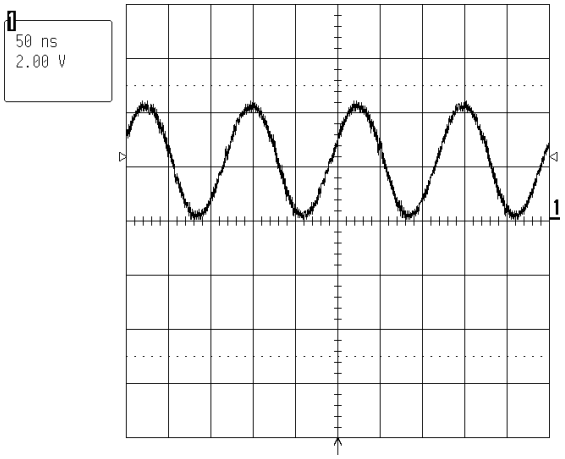


Figure 11. Microcontroller 8 MHz clock at U202 pin 39

Section 2

Bass Module with Head Unit Procedures

Section 2 Contents

Click here to return to the main table of contents

Normal System Operation Description

Basic System Operation

The Lifestyle® Series II system uses digital signal processing to bring even greater realism and impact to both movies and music recordings. Built-in Dolby Digital (AC-3) decoding delivers up to 5.1 discrete audio channels (i.e., five for the independent Satellite Speakers and one for rich bass from the Acoustimass® module) from DVD, digital TV, next-generation cable boxes, and satellite receivers. With analog formats, as well as for two-channel PCM and Dolby Digital bitstreams, Videostage® decoding directs stereo information to the surround channels, so the sound of stereo broadcasts and rented or recorded tapes can approach that of your DVD discs.

In addition, Videostage decoding processes a one-channel program and directs five-channel sound to five independent speakers. Dialogue remains locked on-screen, while music and ambient effects fill the room to increase the listening enjoyment.

The Lifestyle® Series II systems offers the option of listening in 5, 3 or 2-speaker mode. The system turns on in Surround (5-speaker) mode. For most video material (mono, stereo, or surround), listening in 5 or 3-speaker mode helps anchor the dialogue to the picture while providing a fuller sound.

Enhanced Mode for Movie Soundtracks (Film EQ)

Pressing the VIDEO 1, VIDEO 2, or AUX turns the system on in enhanced mode, with bass and treble settings specially designed for proper playback of movie soundtracks. Press the same button (VIDEO 1, VIDEO 2, or AUX) again to alternate between enhanced mode for movies and standard mode for other listening. Pressing TAPE turns the system on in standard mode. Press TAPE again to alternate between enhanced mode for movies and standard mode for other listening.
Note: Enhanced mode provides more bass and treble, as is specified for proper playback of movie sound.

Dynamic Range Compression

Dynamic Range compression automatically adjusts the volume to allow you to hear soft sounds (particularly dialogue) and to prevent you from being overwhelmed by a loud special effect (i.e., an explosion). This feature is engaged when you turn on the system, but you may turn it on (one chime) or off (two chimes) (see explanation table on the next page) using the STEREO two-speaker button.

Simulated Surround for Mono Movie Material

Bose® Videostage decoding can process a one-channel program into five-speaker sound directing the signals so that dialogue remains locked on-screen, while music and ambient effects fill the room. You experience a surround sensation, providing extra enjoyment when you watch older (i.e., pre-stereo) movies. This feature can be used for mono TV, FM, and AM programs. Press the SURROUND (5-speaker) button to turn it on (one chime) or off (two chimes). This feature is automatically engaged when a Dolby Digital bitstream indicates that it contains a mono program.

Connection of Bass Module Using a CD-5/CD-20 Music Center

Test Setup Procedures

Connect the input cable, part number, (253346 for the CD-20) or (253347 for the CD-5) to the music center and the bass module. Connect the power supply to the music center and the line cord to the bass module. Connect a satellite speaker to one of the output RCA connectors on the bass module.

Apply a 100 mVrms, 250 Hz signal to the left and right AUX input on the music center. Turn the music center on and adjust the volume to maximum using the either the remote control or the buttons on the music center's control panel. The remote control would be the best option.

Turn the system on by selecting the Aux button on the remote, and listen for audio from the bass box as well as the satellite speaker.

If you hear audio using the remote control and a satellite speaker, check the outputs for left, right and center channel. Follow the instructions (from the owners manual) listed below for proper system function. If no audio output, go to the DSP troubleshooting section.

Enhanced Mode Table

Source	Default Mode	Change Mode
Video 1, Video 2, or Aux	Enhanced mode	Select the same source for standard mode
Tape	Standard mode	Select the same source for enhanced mode
CD and AM/FM	Standard mode	Cannot change mode in these sources

Dynamic Range Compression Table

Source	Dynamic Range Compression	Change Dynamic Range
Video 1, Video 2, or Aux	On by default	Press and hold the STEREO (2-speaker) button until two chimes are heard
CD, AM/FM, or Tape	Off by default	Press and hold the STEREO (2-speaker) button until one chime is heard

Simulated Surround (mono into 5 speakers)

Audio Source	Simulated Surround	Change Simulated Surround
Mono Dolby Digital	On by default	Press and hold the SURROUND (5-speaker) button until two chimes are heard (OFF)
Any other audio source	Off by default	Press and hold the SURROUND (5-speaker) button until one chime is heard (ON)

Reset Factory Speaker Level Settings

Selection	Reset Factory Settings
Center Speaker Level	Press STEREO and CENTER (3-speaker) button until you hear a 3 note chime
Surround Speaker Level	Press SURROUND (5-speaker) button until you hear a 3 note chime

Bass Box Troubleshooting Procedures

1. Check for Voltage at the Transformer

1.1 With the bass module completely assembled and the cover off, check for voltage at the transformer secondary. If there is voltage at the transformer secondary, skip to procedure 3. If there is no voltage on the transformer secondary, continue on to step 1.2.

1.2 Check for AC mains voltage, 120 or 240 VAC at the transformer primary.
If there is voltage at the transformer primary, check the thermal fuse in the transformer primary and replace the transformer if it is open.
If there is no voltage at the transformer primary, proceed as follows.

1.2.1 Check the fuse located on the PCB.
1.2.2 Ensure that the 18 conductor ribbon cable is fully seated.
1.2.3 With the line cord connected, connect the 10V turn-on signal to the 3.5 mm mono plug located on the test cable. Check the voltage at U300 pin 1.
If it is ~1.25 VDC, U300 should be on, turning triac D302 on. Go to procedure 3.
If it is ~0.8 VDC, the opto-coupler U300 is crowbarred off keeping triac D302 off, which connects 120 VAC to the transformer primary. Disconnect power to the bass module and go to procedure 2.

2. U300 Crowbarred Off, Triac D302 Off
Note: Refer to Figure 50. Protection Circuit Simplified Schematic Diagram in the Appendix for an overview of the protection circuit.

2.1 If the bass module crowbars off (shuts off) immediately (<50 msec), check the “protect” signal at J8 pin 6. If the voltage on J8 pin 6 is greater than approximately +0.7 VDC, it will turn on Q202 and If the voltage is less than approximately -0.7V, it will turn on Q203. Turning on either Q202 or Q203 causes Q202 and Q203 to latch and this will activate the crowbar. If there is a fault condition at J8 pin 6, check the ±12 VDC, ±17 VDC and ±34 VDC power supplies. If the ±12 VDC power supply is not working and the ±34 VDC power supply is working, check resistive fuses R714 and R713 located on the amplifier PCB. A failed component could be causing one or more of these supplies to sag, causing the unit to crowbar off. If the DC power supplies are working, continue onto step 2.2.

2.2 DC offset at the output of the bass amplifier J703 pin 2 (+) and pin 1 (-) will produce a fault condition “protect” voltage (greater than approximately ±0.7 VDC) at J8 pin 6. Check the components in the bass amplifier with an Ohmmeter.

2.3 If the bass module crowbars off after approximately 3 seconds there could be DC offset on one or more satellite outputs. The satellite outputs are summed through the “speaker output DC offset” circuit (SD251571, grid location A7). The output of this circuit, P66, is sent to the microcontroller U202 pin 25. In normal operation, the voltage at U202 pin 25 should be 2.5 VDC. If the voltage strays more than 1 VDC from the normal 2.5 VDC, microcontroller U202 pulls pin 39 (P22) to ground (normally high impedance) pulling R308 to ground latching the circuit consisting of Q302 and Q303 (SD251571, grid location B4). This latch circuit, when latched, will shut off the opto-isolator U300, which will shut off the triac D302 disconnecting AC from the primary of the transformer.
Note: U202 pin 26 is connected to U202 pin 39. The head unit does not send an “ON” command to the bass module. The uC knows when the power has just come up by watching the status of the 10V turn-on voltage via pin 26, which is connected to the same circuit mentioned above that the uC uses to shut down the triac.

Bass Box Troubleshooting Procedures

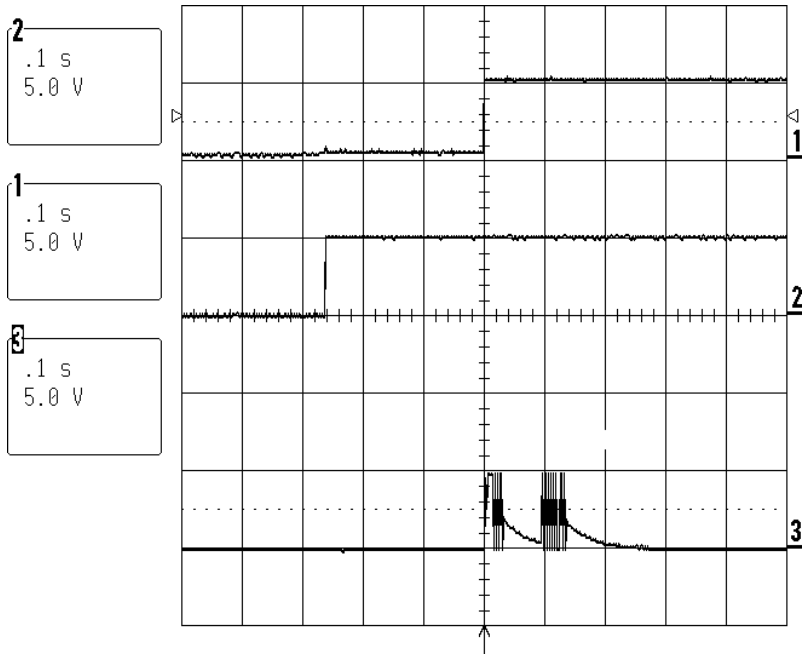
Note: Refer to Figure 15. DSP PCB Test Point Locations Layout Diagram, Solder Side on page 34 for the following procedures.

3. Microprocessor Circuit Check

3.1 The serial data output leaves the DSP PCB at J5 pin 11 (U202 pin 43, TTY OUT) and the boot prompt can be checked here at power-up with an oscilloscope. The first thing the uC is supposed to do when it comes out of reset is to print the following to the “debug” output J5 pin 11.

**
%0001#01

This is visible as two bursts of activity. One immediately following the rising edge of the RESET line (**) and one about 50 msec later (%0001#01). After printing the boot prompt, the uC will only print error codes. Thus, a lack of activity on this signal after the initial two bursts is expected. Short bursts of activity is likely to be the uC printing out an error code. Refer to Figure 12.



Upper trace: RESET (active low) pulse U202 pin 14 or U200 pin 2
Middle trace: +5V supply
Lower trace: Serial data from uC, J5 pin 11

Figure 12. Scope Photo of Boot Prompt at J5 Pin 11

3.2 If there is no boot prompt at U202 pin 43, then check for the following; +5 VDC at U202 pin 40 and U202 pin 18, 8 MHz clock on both sides of X600, reset pulse at power-up at U202 pin 14. If the +5 VDC, 8 MHz clock and reset pulse are okay and there is no boot prompt, then the Uc has failed. Replace the Uc U202.

Bass Box Troubleshooting Procedures

4. No Audio at Speaker Outputs

4.1 If there is no audio from the speaker outputs when an analog signal is applied to the input of the bass module, follow the audio signal path through the system. Refer to the following table. If there is audio from the speaker outputs when an analog signal is used but not when a SPDIF (Sony/Philips Digital Interface Format) signal is used, go to procedure 5.

Verify	At Location	Note
Signal at input connector	J5 pin 9 (L) and pin 1 (R)	DIN input connector
Digital data from codec	U100 pin 38 (sclk) U100 pin 37 (frame_sync) U100 pin 36 (data from codec)	For pin 38 see Fig 34 For pins 37 and 36, see Fig 33
Digital data from DSP to codec	U100 pin 34	See Figure 33
Codec output	U100 pin 21 (right surround) U100 pin 22 (bass) U100 pin 23 (center) U100 pin 24 (left surround) U100 pin 25 (left) U100 pin 26 (right)	High frequency noise, 2.3 Vdc bias
Buffers output	U103 pin 1 (left) U103 pin 7 (right) U103 pin 8 (center) U103 pin 14 (left surround) U104 pin 1 (right surround) U104 pin 7 (bass)	Gain of 6, no DC bias, less high frequency noise
Output at connector	J8 pin 9 (left) J8 pin 7 (right) J8 pin 10 (center) J8 pin 12 (left surround) J8 pin 13 (right surround) J8 pin 11 (bass)	Analog audio exits the DSP PCB at this point to enter the amplifier PCB
Amplifier mutes okay	J8 pin 17 (bass, left, right) J8 pin 16 (center) J8 pin 15 (left surround, right surround)	0V = muted 5V = un-muted

5. No Audio Output when using a SPDIF Input
(Figure 54, Digital Signal Path from Input Jack to CODEC Simplified Schematic Diagram)

5.1 Apply a SPDIF signal to the bass module SPDIF input and adjust the volume on the head-unit to maximum.

5.2 Check SPDIF signal path;
- J5 pin 4
- U100 pin 42 (if codec is in digital mode there should be 2.3 VDC on U100 pin 42).

5.3 Verify the DC voltage on the PLL line is clean; indicates that the PLL has locked onto the SPDIF signal. U100 pin 17.

5.4 Capture the PLL tuning voltage as it goes from 0V (analog mode) to about 2V (digital mode). Voltage should slew and settle within about 5 msec. Any AC on the tuning line after the initial 10 msec, indicates a stability problem with the PLL circuit.

5.5 Verify that there is no error bit output from the codec. U100 pin 30 should be 0V.

5.6 Verify that the uC can see the SPDIF input. Check the voltage at the collector of Q201 and U200 pin 23. The voltage should be < 1 VDC, if there is an SPDIF present and > 4VDC if there is no SPDIF.

5.7 If the problem can't be located, go to procedure 6.

6. Quick Check/Possible Problems With DSP PCB

6.1 Because the DSP IC's legs are very fine, there is a chance for shorts or opens. Probing them can result in shorting them. Boot data can be garbled due to a short or open on the DSP IC pins.

6.2 The 40 MHz oscillator, CR400, might not be working.

6.3 There might be a broken "via" in the PCB. This is a hole in the PCB that connects traces on the top side of the PCB to traces on the bottom side of the PCB. This type of problem can be difficult to isolate.

6.4 If the problem has not been isolated, go to procedure 7.

7. Miscellaneous DSP PCB Troubleshooting Tips

7.1 +17V, ±12V Power Supplies

The PCB draws power from three different supplies:

7.1.1 +17V unregulated, at about 250 mA when everything is running normally. The +17V supplies the unregulated voltages for the two voltage regulators on this PCB: the +5V linear regulator U1, and the 3.3V switching regulator U500. The +17V is brought onto the PCB from J8 pin 3. Note that the +17V unregulated supply can vary from about +17V to as low as +10V, depending on conditions. On the bench, the value may be more typically +15V or so. Whatever the exact voltage, in this document it will be referred to as the "+17V" supply.

7.1.2 ±12V, at about 40 mA or so. The ± 12V supplies are for the op-amps U103 — U105. +12V is brought onto the PCB from J8 pin 1, and -12V is supplied from J8 pin 5.

7.2 +5V Supply

Check the +5V supply first, since the +5V powers the microcontroller, and without it, nothing else works. Check the following points:

7.2.1 At the input side to the +5V regulator U1. This is a typical 7805 3-terminal linear regulator, so it needs at least 7.5V at the input to stay in regulation. If there is +17V at J8 pin 3, but no voltage at the input side of U1, check the components in between (R10 and R11, large SMD resistors on the bottom side).

7.2.2 At the output side of the +5V regulator. Check that the +5V output is clean and that the regulator is not oscillating. The regulated +5V is supplied to the rest of the PCB via a couple of filter components, so check for +5V at the following points:

7.2.3 U102 pin 20; if no +5V here, check L200 (bottom side, between U101 and U104).

7.2.4 U100 pin 40; if no +5V here, check both L2 (top side, near U100 pin 20) and L1 (bottom side, directly under U100).

7.3 8 MHz Clock

The micro requires an 8 MHz clock to run. This clock is developed by an internal oscillator which requires an external ceramic resonator (X600). Check for the 8 MHz clock at:

7.3.1 Ceramic resonator X600 (top side, next to U202). There should be a roughly sinusoidal waveform, 0V to 5V, on both sides of X600.
If there is no 8 MHz clock, possible causes are:
- No +5V; check L200.
- Poor soldering
- If the 8 MHz clock is present at X600, and its amplitude is roughly 5Vpp, but the micro controller won't issue a boot prompt or turn on the 3.3V power supply, possible causes are:
- Dead micro.
- A missing RESET pulse at power up. Power the board down and back up again, and verify that the micro is getting a healthy RESET pulse at power up. The reset IC (U200, SOT-23 bottom side) should hold the micro's RESET input (pin 14) low for about 250 msec after the +5V supply has stabilized. The RESET input should transition from low to high cleanly and briskly — if it appears to be floating, check R280.

7.4 3.3V Supply

The 3.3V supply is supplied by the switching regulator IC U500. This IC works by rapidly switching its output between +17V and ground; the output filter (L500 and C500) blocks the 100 KHz switching waveform and passes only the average 3.3 VDC. Note that the micro can turn U500 on or off, via one of its output ports (U202 pin 41) and Q500. U500 powers up off with its "soft-start" node (pin 19) clamped to ground, which inhibits operation, and it remains in this state until the micro boots successfully and pulls the base of Q500 to ground. The point to remember is that the 3.3V supply does not power up until after the micro boots successfully.
Assuming that the micro does boot successfully, check U500 for the following waveforms at the following points (refer to sheet 5 of the schematic):

7.4.1 +17V on both sides of the surface-mount inductor L501 (top side).

7.4.2 5.1 VDC at U500 pin 18. This is a reference voltage generated by U500. Its presence here on pin 18 will show that U500 is getting power.

7.4.3 Check that U500 pin 11 is connected to ground. This pin is U500's ENABLE input; if it isn't grounded, U500 shuts down.

7.4.4 Check that the base of Q500 (bottom side) or U202 pin 41 (same node) is pulled to ground. If Q500 is turned on, U500 shuts down. This node is pulled up to +5V with R282 (sheet 2); the micro pulls this node low after it boots. If the micro doesn't boot, U500 never turns on.

7.4.5 100 KHz switching waveform, Figure 40, on the +17V side of the toroidal inductor L500. This waveform should switch rapidly (<100 nsec) between about -0.35V and VCC, with an average DC voltage of 3.3V. If the voltage at this node dips well below -0.35V, then check D500 (bottom side).

7.4.6 If still no luck, check L500. If it's a toroidal inductor, check that it's properly soldered to the PCB.

7.5 11.2896 MHz Codec Clock

If the micro and DSP appear to have booted properly, but no audio signal passes through the PCB, check the codec U100 for signs of health. The codec does not power up in a useful state all by itself; the micro must program a number of internal registers via the I 2 C buss inputs to the codec . (I 2 C is a 2 wire serial buss; one line for the data, one line for the clock.) To quickly determine if the codec was properly initialized by the micro, check for;

7.5.1 0V — 5V, 11.28 MHz sine wave on both terminals of the crystal CR100.
If the 11.28 MHz clock, Figure 38, is not oscillating, possible causes might be:
- No +5V power to the codec U100. Check both power pins (19 and 40). If there's power on one but not the other, check L1 and R3 (bottom side, directly under U100).
- I 2 C data or clock signals missing. Check for digital activity (0V — 5V) on these signal paths.
  U202_32 — R253 — U100_4
  U202_33 — R265 — U100_3

Once the micro boots, there is a fair amount of regular activity on these two lines. The micro checks the codec's error status register about every 5 msec , so if these lines are silent, suspect a bad micro or a broken connection somewhere in between the micro and the codec. Also, the micro will output an error code if it detects an ongoing problem with the I 2 C buss, such as:
- A problem in the network of components around CR100, R175, R176, C139, C140. Check CR100
- Codec power-down input at pin 8. Normally, this signal is pulled up for proper codec operation. When this pin is low, the codec enters a low-power reset state. The micro will pulse this line low for a few msec to reset it prior to initialization. If this line is held continuously low for some reason, the codec's oscillator won't operate, and the analog reference voltage (about 2.3V) at pin 16 disappears.

If the 11.28 MHz codec clock is oscillating, then verify the following digital output signals from the codec:

7.5.2 Bit clock at R186, U100_38: 11.2896 MHz square wave

7.5.3 Frame clock at R185, U100_37: 44.1 KHz square wave

7.5.4 Output data, U100_36: "irregular" digital activity at R187, similar to Figure 44.

7.6 Input analog signal path to codec

Apply a 1 Vrms, 1 kHz signal to both the L an R inputs to the PCB (J5 pins 9 and 1), and check for the signal at the two analog inputs to the codec (pins 13 and 14).

7.6.1 Gain from J5 to U100: -6 dB

7.6.2 DC bias at U100 pins 13 and 14: 2.3V

If you don't see any signal at the codec inputs, trace the analog signal path through from J5 (sheet 1 of schematic) to figure out where it disappears. Also, check the ± 12V power supplies on the op-amps.

7.7 Codec Revision Code

The CS4226 codecs must be rev. G or higher. Specifically, the rev. code must NOT be "C".
The rev. letter is the letter immediately preceding the date code silkscreened on the IC, e.g.
CRYSTAL (logo)
CS4226-KQ EP (part number)
JTAAXG9819 (rev. G, date code 9819 [19th week of '98])

7.8 DSP 40 MHz Clock

7.8.1 The DSPs run on a 40 MHz clock; the easiest place to check for this is at J401_4. (J401 is the un-loaded 14-pin connector between DSP2 and the shield fence.) This is a buffered version of the 40 MHz clock that drives the DSP. This clock has very fast edges (3 nsec rise times), so if you're using a low-quality 'scope probe, don't be too alarmed by what you see. A cheap 'scope probe or a long or missing ground lead will distort this signal beyond recognition. In this case, it's ugly, but it's not a serious issue — all you're trying to do is verify that the clock is oscillating. However, pay attention to the frequency — this is a third overtone oscillator, which means it may prefer to oscillate at 13.333 MHz (40/3). If the network of components around CR400 is incorrect in some way, it may prefer to oscillate at some frequency unrelated to what's printed on the crystal.

7.8.2 40 MHz clock frequency at U104 pin 4: 40 MHz

If there's no 40 MHz clock at all,
- Check U400 (LCX00) for proper soldering, and check for 3.3V on U400_14.
- Check to make certain that all the components around the crystal (C402, C403, R411, R412, R409 — bottom side, under CR400) are OK.

7.9 DSP Reset Pulse

Check for a clean DSP reset pulse at the collector of Q200 (top side, near U102). At power-up, Q200 is biased on, driving the collector low, until the micro boots properly. After the micro boots, it turns Q200 off and allows the DSP reset line to be pulled high. This signal is digital, and should be either at 0V or at 3.3V.

7.10 Digital One-shot U106

U106 is a flip-flop wired up to produce a narrow pulse on the falling edge of the 44.1 KHz clock. Without the signal that this IC produces, the DSP can't send or receive from the codec properly. Inputs to U106:

7.10.1 U106 pin 1: 44.1 KHz clock

7.10.2 U106 pin 5: 11.28 MHz clock

Output from U106:

7.10.3 U106 pin 13: 100 nsec pulse, at 44.1 KHz rate

7.11 5V / 3.3V Level Translators

The micro (U202) and the codec (U100) run on +5V, while the DSPs run on 3.3V. There are a couple of level-translator ICs required to bridge this gap:

U101 a 74LCX244, a 3.3V part which has “5V tolerant” inputs.
U102 a 74ACT244, a 5V part with input logic thresholds that are compatible with 3V logic (“TTL”, or 0.8V/1.5V).

Since there’s a problem somewhere on the PCB, it isn’t safe to assume that you’ll be able to observe any digital activity on the pins listed below, although normally there would be. Mainly what we’re looking for is evidence that a buffer gate isn’t buffering; i.e., a signal is present on the input, but there’s no similar signal on the output.

From the codec U100 to DSP1:
U101_13 —> U101_7
U101_15 —> U101_5
U101_17 —> U101_3

From DSP1 to the codec U100
U102_2 —> U102_18
U102_4 —> U102_16

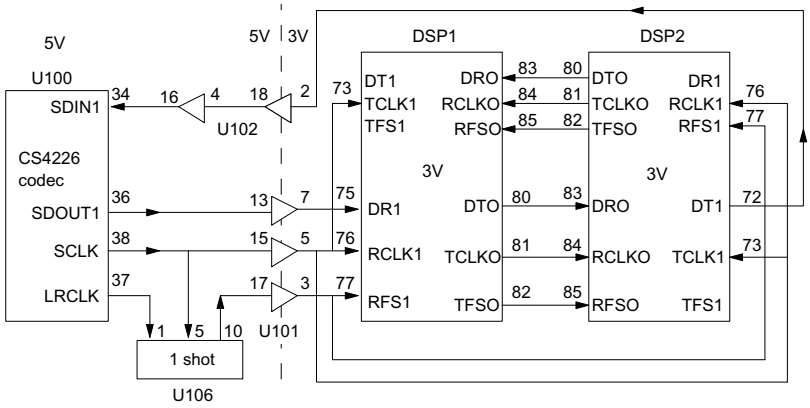


Figure 13. Codec to DSP, Digital Audio Signal Path

From the micro to DSP1:
U101_4 —> U101_16
U101_2 —> U101_18

From DSP1 to the micro:
U102_15 —> U102_5
U102_17 —> U102_3

From the micro to DSP2:
U101_8 —> U101_12
U101_6 —> U101_14

From DSP2 to the micro:
U102_11 —> U102_9
U102_13 —> U102_7

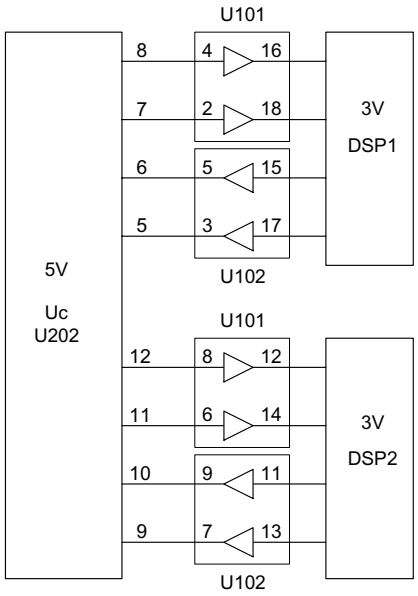


Figure 14. Micro to/from DSPs

7.12 Evidence that the DSPs have booted

7.12.1 DSP Output Ports

Observe the following signals as the power to the PCB comes up:
U102_15
U102_11
These signals are part of the communications buss between each DSP and the microcontroller, and are pulled up to +3.3V by resistors. One of the very first things that either DSP will try to do is talk to the micro, which initially requires pulling these signal lines low.
If DSP1 is working, U102_15 will show some activity about 100 msec after the 3.3V supply comes up.

If DSP2 is working, U102_11 will show some activity about 100 msec after the 3.3V supply comes up.
If these signals power up to 3.3V and sit there doing nothing, then one or both of the DSPs failed to boot.

7.12.2 Boot Activity on External address Buss

The DSPs have no internal program ROM, and must boot from the external PROM. The boot happens in two stages. First, a short (256 words) boot loader program is loaded automatically; second, the boot loader program is executed. Typically, the boot loader program loads the other 99% percent of the PROM contents into the DSP.

The first stage of the boot is hard-wired into the DSP, so as long as the DSP has power, a 40 MHz clock, and a few other signals, the first stage of the boot always happens when the reset line goes high. However, the second stage happens only if the boot loader program actually works, which of course it won't if the DSP is trying to boot from an empty or damaged PROM, or if the data lines or address lines between the PROM and the DSP are shorted together.

Observe the activity on PROM pin 30 (ADD 17) at power-up. A successful boot will show a flurry of activity about 30 msec long immediately following the release of the DSP reset line (collector of Q200). An unsuccessful short boot won't last more than 300 usec. If it becomes clear that the DSPs aren't booting, the problem might be caused by:

- Solder problems affecting the fine pitch leads on the DSPs. This is the most common source of DSP boot errors. Examine the leads of each DSP under an illuminated magnifying glass, checking for shorts (which are usually pretty easy to see) and opens (which sometimes are not).

- Solder problems affecting the 4 resistor r-packs. These are attached to some critical DSP buss signals, so a loose connection here can cause problems.

DSP PCB Troubleshooting

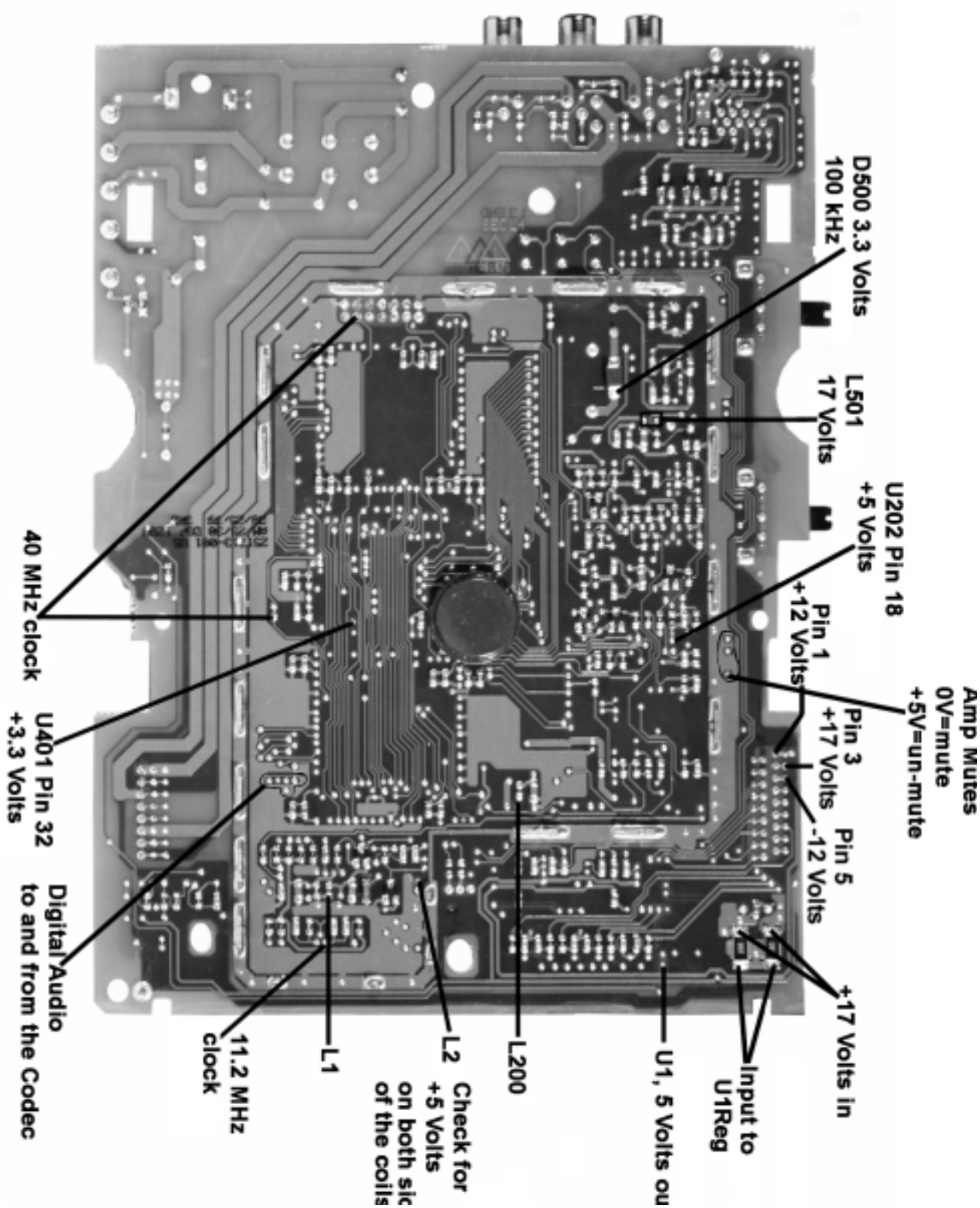


Figure 15. DSP PCB Test Point Locations Layout Diagram, Solder Side

Scope Photos

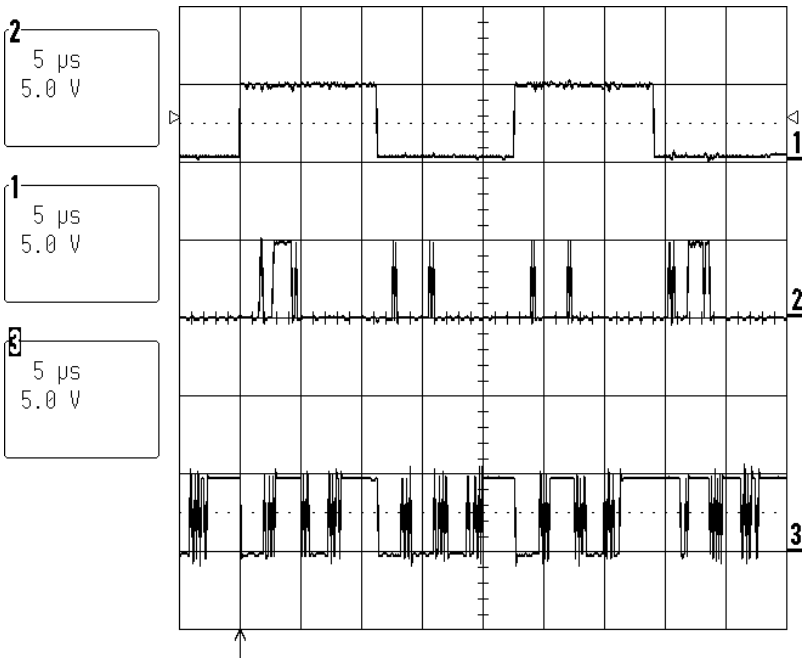


Figure 16. Codec (U100) Scope Photo, Un-mute Condition

Upper trace: LR_CLK (U100 pin 37) 44.1 kHz square wave
Middle trace: SDOUT1 (U100 pin 36) serial data out
Lower trace: SDNIN1 (U100 pin 34) serial data in

For each period of the 44.1 KHz clock, there are 256 bits of data clocked in/out. The first bit of the data stream starts at the falling edge for LRCLK. The data falls into six time slots as follows:

Serial data out:

32 bits of LEFT ADC input, followed by
32 bits of AUX ADC input (not used), followed by
64 bits of nothing, followed by
32 bits of RIGHT ADC input, followed by
32 bits of AUX ADC input (not used), followed by
64 bits of nothing
Total: 64 bits from the codec

Serial data in:

32 bits of RIGHT SURROUND DAC input, followed by
32 bits of CENTER DAC input, followed by
32 bits of LEFT DAC input, followed by
32 bits of nothing, followed by
32 bits of BASS DAC input, followed by
32 bits of LEFT SURROUND DAC input, followed by
32 bits of RIGHT DAC input, followed by
32 bits of nothing
Total: 256 bits to the codec

Scope Photos

On the lower trace of Figure 16, you can see the six packets of audio data embedded in the bit stream. The bass module is muted when it is first powered up and will not un-mute until it receives an “un-mute” or “volume up” command.

Muted data consists of all zeroes; this condition is shown in the lower trace of the codec (U100) scope photo, mute condition, Figure 17.

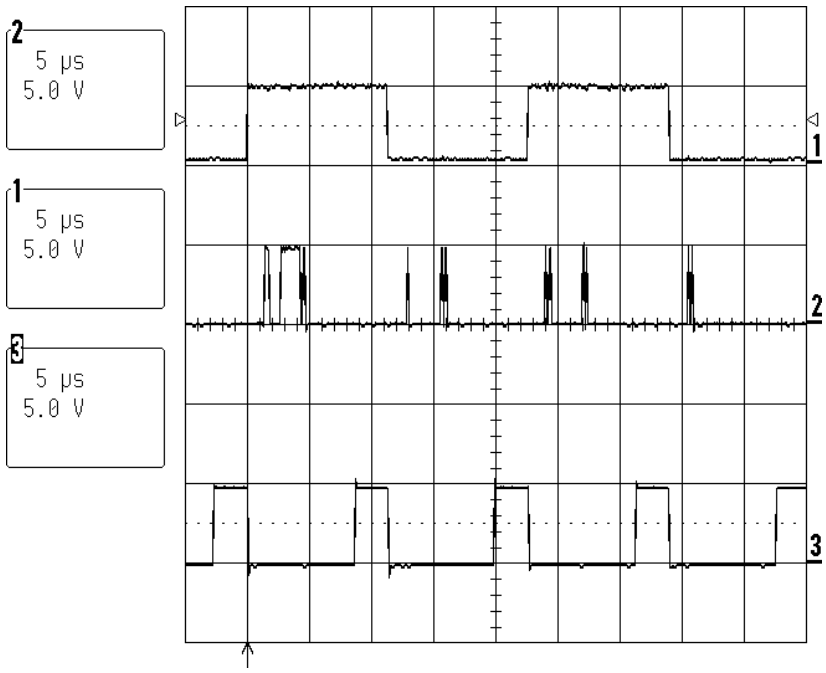


Figure 17. Codec (U100) Scope Photo, Mute Condition

The significance of the SDOUT1 signal (U100 pin 36) is that it represents the digital audio data at the start of the digital audio signal path. This data is transmitted serially to the DSP1, which requires three signals to accept it:

SCLK (U100 pin 38): to clock the serial data in
LRCLK (U100 pin 37): to indicate the start of each audio sample
SDOUT1 (U100 pin 36): the serial audio data

The significance of the SDIN1 signal (U100 pin 34) is that it represents the output of the digital audio signal chain. The data is shifted out from DSP2 using the clock signals mentioned above. If this signal is dead, DSP2 is most likely not running. See Figure 44.

Scope Photos

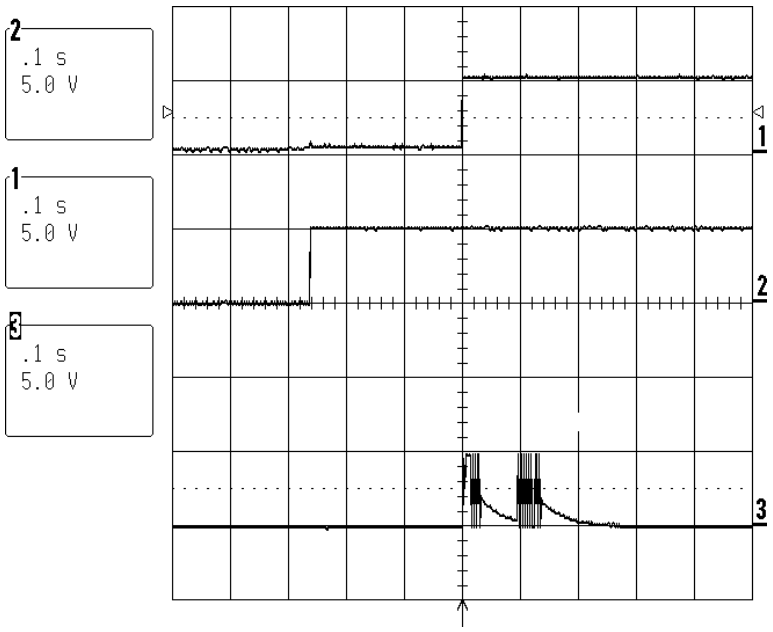


Figure 18. Microcontroller (U202) Scope Photo, Power Up

Upper trace: RESET pulse (active low), U202 pin 14 or U200 pin 2
Middle trace: +5V supply
Lower trace: Serial data from uC, J5 pin 11

The first thing the microcontroller supposed to do when it comes out of reset is to print the following to the debug output J5 pin 11.

**
%0001#01

This is clearly visible as two bursts of activity (4800 baud), one immediately following the rising edge of the reset line (**) and one approximately 50 msec later (%0001#01).

After printing the boot prompt, the Uc will only print error codes. Thus, a lack of activity on this signal after the initial two bursts is expected. Short bursts of activity is likely to be the uC printing out error codes.

Scope Photos

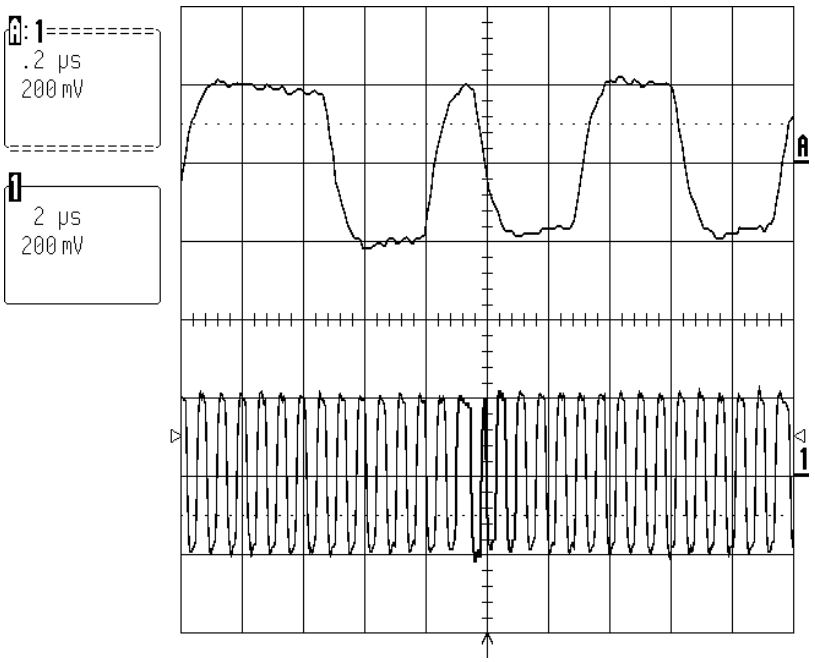


Figure 19. SPDIF Signal at U100 pin 42

Upper trace: Detail
Lower trace: SPDIF signal at the codec's SPDIF input (U100 pin 42)

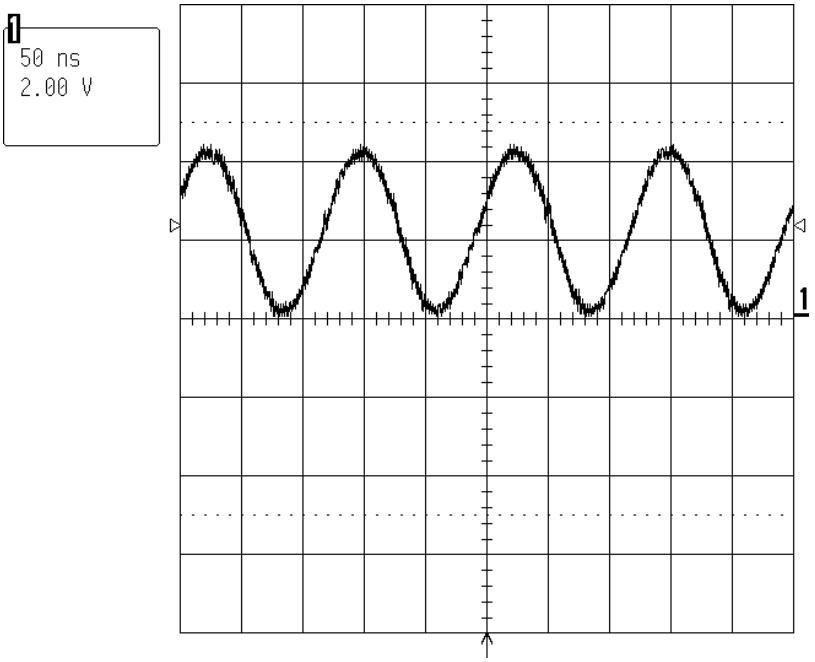


Figure 20. Microcontroller 8 MHz clock at U202 pin 39

Scope Photos

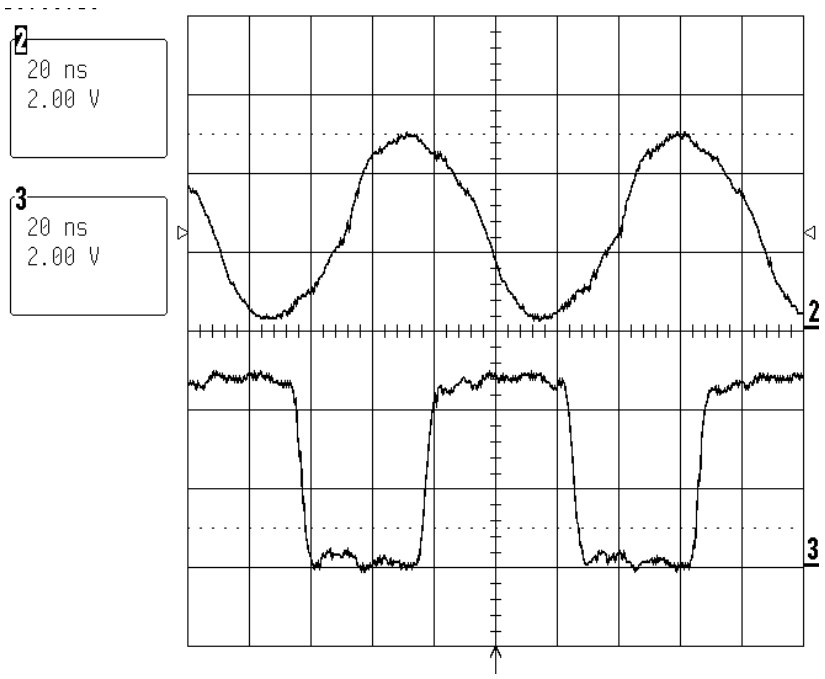


Figure 21. Codec 11.2896 MHz Clock

Upper trace: Signal at CR100 crystal (U100 pin 29)
Lower trace: Buffered digital SCLK output (U100 pin 38)

This is the bit clock used to clock serial data in/out of the codec (see Codec (U100) Scope Photo, Un-mute condition and Codec (U100) Scope Photo, Mute condition)

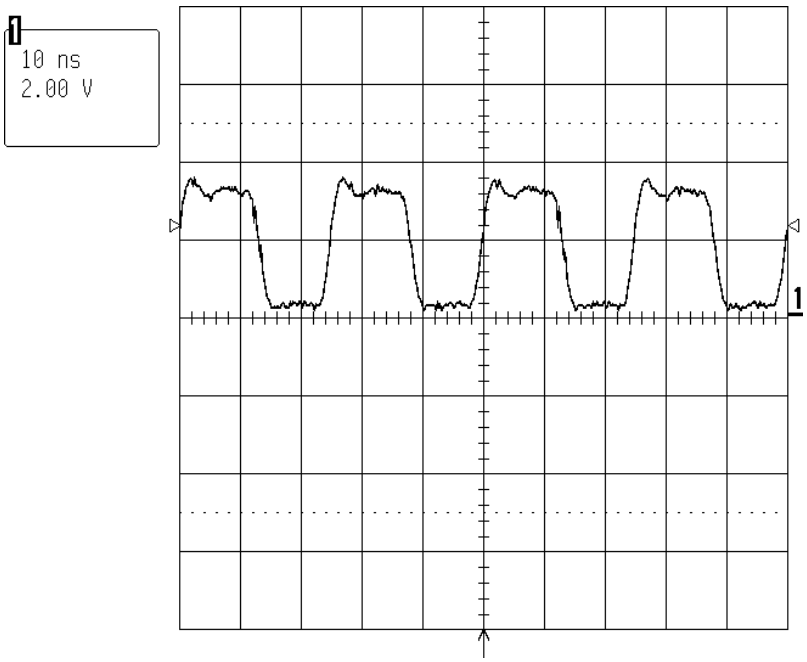


Figure 22. 40 MHz DSP clock

Buffered output at J401 pin 4 (14 pin unloaded connector)

Scope Photos

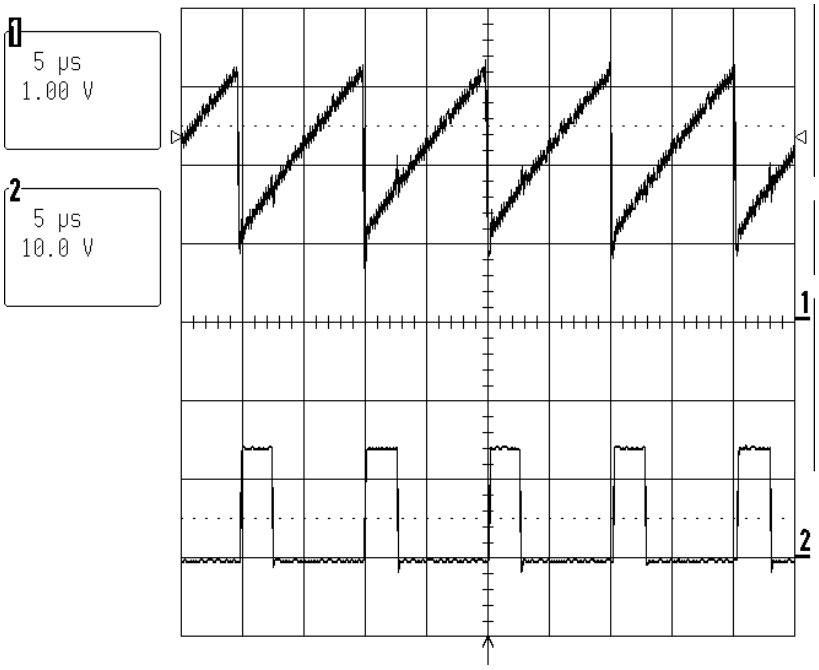


Figure 23. 3.3V Switching Power Supply Signals

Upper trace: U500 pin 1
Lower trace: U500 pin 2

The 100 kHz pulse train developed at U100 pin 2 (the lower trace) is applied to the output filter L500/C500. The average DC voltage of this pulse train is 3.3V, which can be found on the other side of L500.

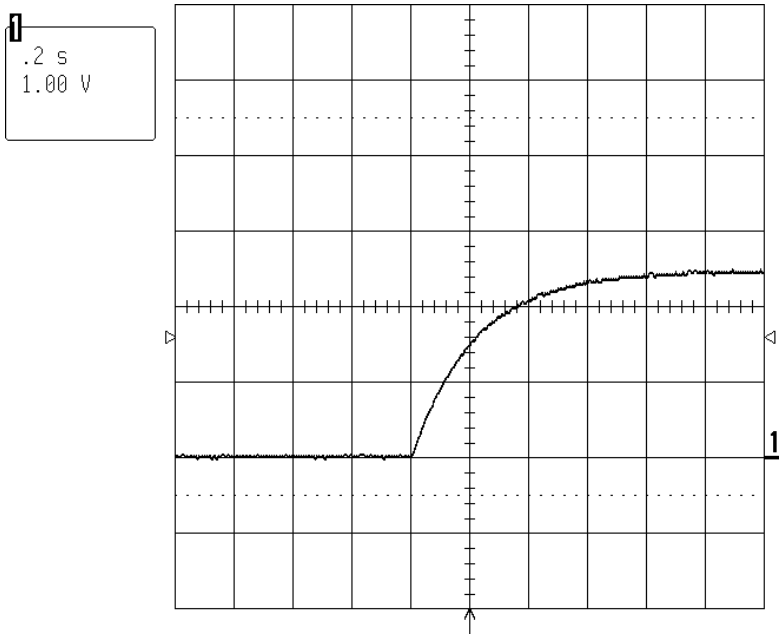


Figure 24. Power Up Condition at U202 Pin 25

U202 pin 25 monitors the satellite DC offset circuit. Normal condition: 2.5 VDC. Fault condition: If the voltage strays more then ±1 VDC from the normal condition of 2.5 VDC, U202 will pull pin 39 to ground, shutting off the unit.

Scope Photos

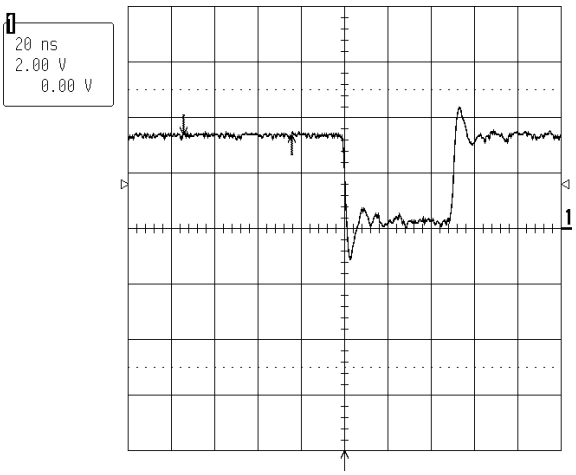


Figure 25. Transmit Frame Sync

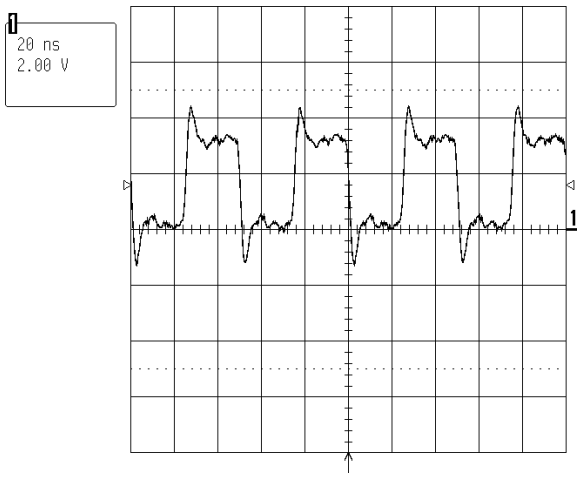


Figure 26. Serial Data Clock

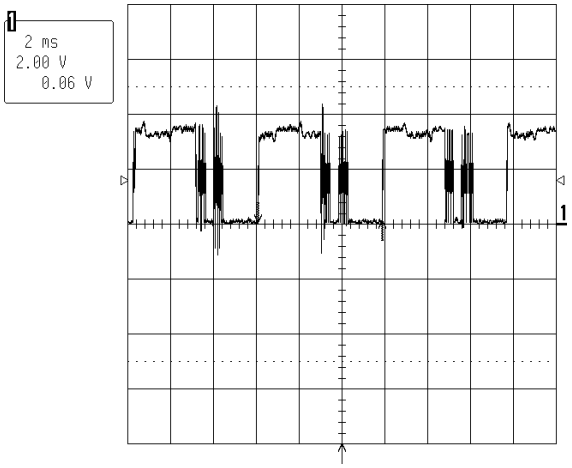


Figure 27. Audio Data

The audio serial data transmitted from DSP1 to DSP2 is sent via a high speed serial link, which requires 3 signals to operate.

- Serial Data Clock: This clock will either be 40 MHz (older software revision) or 20 MHz (version 30 and above).

- Transmit Frame Sync: A semi-periodic 50 nsec or 25 nsec pulse (depending on if it is a 40 MHz or 20 MHz clock).

- Audio Data: This is sent over in bursts which have a fundamental pattern rate of about 5.8 msec. Audio data is digitally processed in blocks of 256 samples. 256/44.1 kHz equals 5.8 msec.

These three signals are unlikely to resemble the scope photos unless DSP1 is processing data. The presence of these three signals indicates that DSP1 has booted successfully.

Section 3

Computer Aided Troubleshooting

Section 3 Contents

Click here to return to the main table of contents

Test Setup Parameters and Equipment

Use the dissasembly/assembly procedures found in the AM25/30P Series II service manual part number 199401, to access the PCBs.

Speaker Output Loading:

Load the ouputs only when testing the bass module for its rated power output. To reduce overheating of the outputs all testing should be done with the ouputs unloaded.

Left Front Output:	8 Ohm, 1%, 50W
Right Front Output:	8 Ohm, 1%, 50W
Center Output:	8 Ohm, 1%, 50W
Left Surround Output:	8 Ohm, 1%, 50W
Right Surround Output:	8 Ohm, 1%, 50W
Bass Channel Output:	4 Ohm, 1%, 100W

Equipment Requirements:

- A terminal emulator or in Microsoft® Windows® 95 or 98 use “Hyperterm”
- A SPDIF digital signal source or a DVD player, or item 4 in below table
- Audio signal generator, oscilloscope, dB meter and a multi-meter
- Items listed in the following table

Item Number	Description	Bose® Part Number	Manufacturer
1	RS232 to TTL converter	254751	B+B Electronics
2	Power Supply for RS232	254752	B+B Electronics
3	25 to 9 Pin PC serial port cable	254858	Bose
4	SPDIF Digital Signal Converter	254753	Flying Calf
5	Test Cable	199527	Bose

Test Setup Procedure

(see Figure 45. Test Setup Diagram, located in the Appendix)

Using the test cable, part number 199527, plug the 13-pin din connector into the bassbox.
Connect the RS232 (B+B TTL232 converter) to the 25-pin D connector on the test cable.
Connect the RS232 box to its power supply.
Connect the 25-pin to 9-pin cable to your PC’s serial port.
Open “Hyperterm” (used with Windows® 95 or 98) or other terminal emulator on your IBM compatible P.C.
Perform the Computer Setup Procedure located in the Appendix.

Connect an audio signal generator to the RCA input jacks on the test cable 199527.
To test the SPDIF input, connect the SPDIF output from an SPDIF converter, or from a DVD player, to the female RCA on the test cable 199527.
To turn the bass module on, connect a 10 VDC supply (9V battery will work) to the 3.5 mm jack on the test cable 199527.

Troubleshooting Procedures

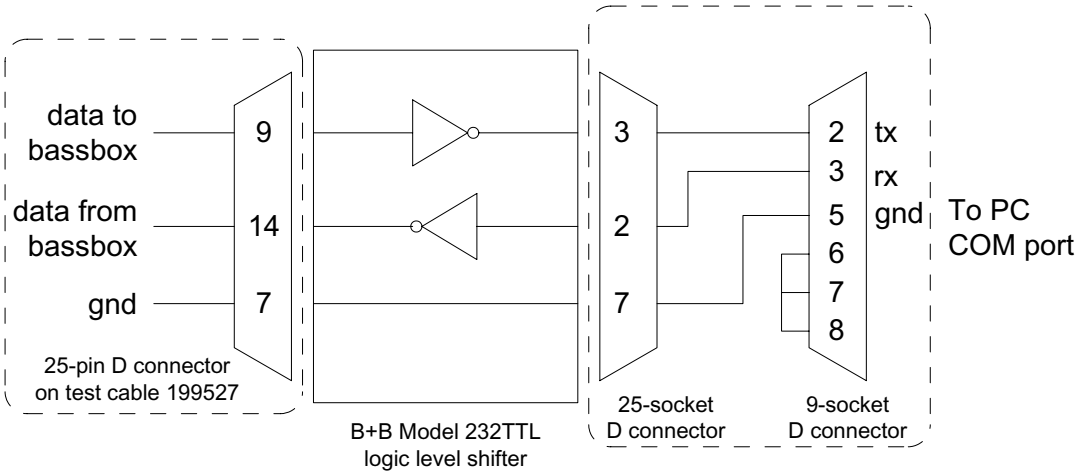


Figure 28. 25 Pin to 9 Pin Serial Data Cable

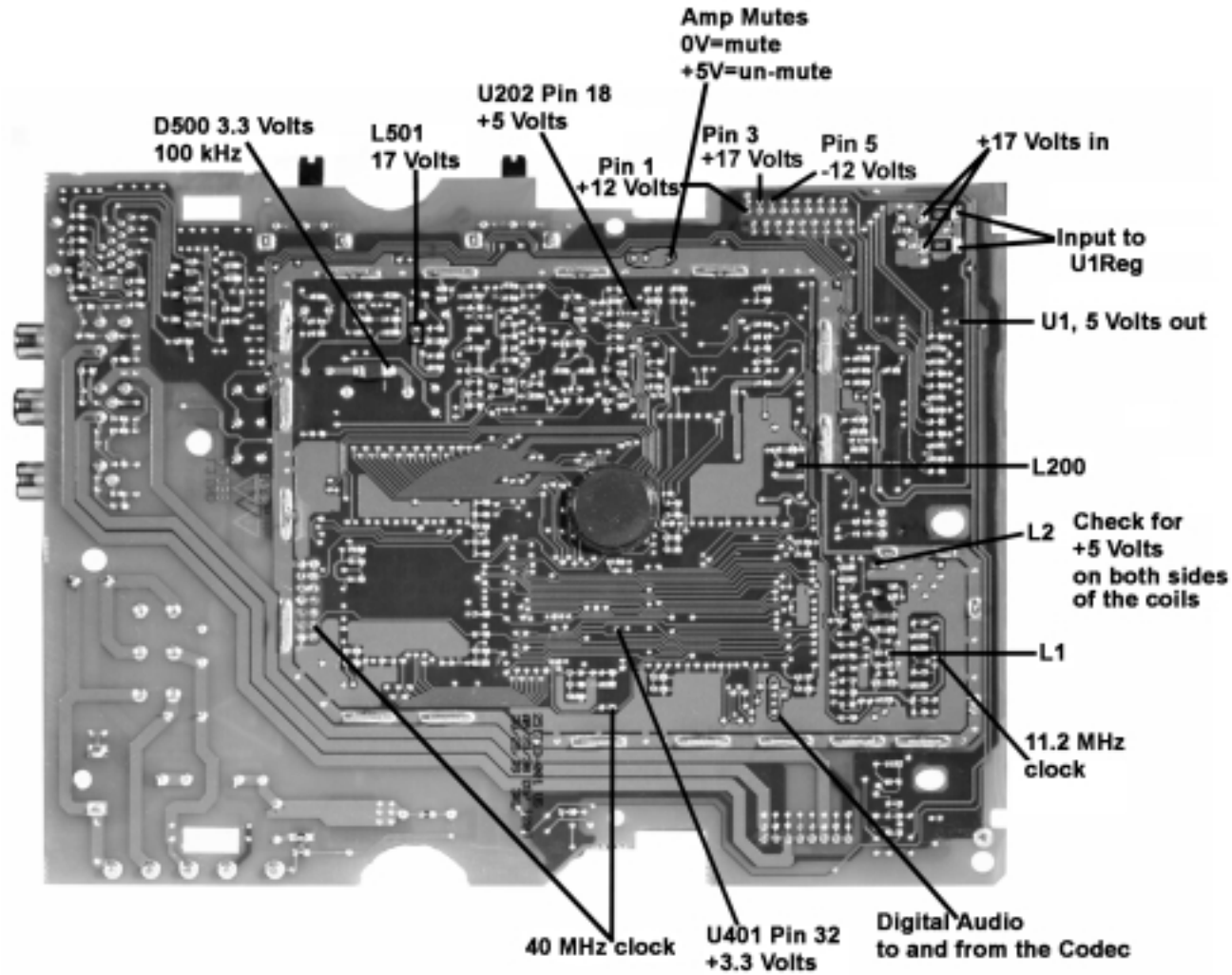


Figure 29. DSP PCB Test Point Locations Layout Diagram, Solder Side

Troubleshooting Procedures

Note: Refer to Figure 29. DSP PCB Test Point Locations Layout Diagram, Solder Side for the following procedures.

1. Check for a Boot Prompt

1.1 With the module completely assembled and the cover removed, connect the the line cord to an AC mains source and connect the 9 Volt battery to the 3.5 mm mono plug located on the test cable. This will power up the module.
Note: If you disconnect AC mains from the module, you will need to disconnect and reconnect the 9 Volt battery to the 3.5 mm plug to get the module to power up again.

1.2 The computer should display something similar to the following. Wait at least 5 seconds to see if the Microcontroller (Uc) returns an error code.

**
#0001%01

The two stars mean that the uC has powered up.

The four digit hex number after the pound sign indicates the number of times the unit has received an “off” command from the head unit. There is no correct answer, it will vary from bass module to bass module. The two digits after the percent sign indicates what equalization curve the DSPs were programmed to run. Refer the following table.

Code	Equalization Curve
00	Lifestyle® 12, 25 Series I
01	Lifestyle® 12, 25 Series II, US
02	Lifestyle® 30 Series II, US
11	Lifestyle® 12, 25 Series II, EU/AUS
12	Lifestyle® 30 Series II, EU/AUS

Why check for a boot prompt?
The boot prompt shows that the uC is functioning. Without a functioning uC, nothing else works.

No boot prompt?
After checking the test cable connection from the computer to the bass module, go to procedure 2.

Boot prompt okay, no error codes?
Go to procedure 6. An error code consists of a text string proceeded by two dashes and followed by two plus signs (--11++).

Boot prompt with error codes?
If the uC is functioning, it can return an error code that will help you determine the fault.
An error code consists of a text string proceeded by two dashes and followed by two plus signs (--11++). If you received an error code with the boot prompt, go to procedure 5.

2. Check for Voltage at the Transformer

2.1 Check for voltage at the transformer secondary. If there is voltage at the transformer secondary, skip to procedure 4. If there is no voltage on the transformer secondary, continue on to step 2.2.

Troubleshooting Procedures

2.2 Check for AC mains voltage, 120 or 240 VAC, at the transformer primary.
If there is voltage at the transformer primary, check the thermal fuse in the transformer primary and replace the transformer if it is open.
If there is no voltage at the transformer primary, proceed as follows.

2.2.1 Check the fuse located on the PCB.

2.2.2 Ensure that the 18 conductor ribbon cable is fully seated.

2.2.3 With the line cord connected, connect the 10V turn-on signal to the 3.5 mm mono plug located on the test cable. Check the voltage at U300 pin 1.
If it is ~1.25 VDC, U300 should be on, turning triac D302 on. Go to procedure 4.
If it is ~0.8 VDC, the opto-coupler U300 is crowbarred off keeping triac D302 off, which connects AC mains voltage to the transformer primary. Disconnect power to the bass module and go to procedure 3.

3. U300 Crowbarred Off, Triac D302 Off

3.1 If the bass module crowbars off (shuts off) immediately (<50 msec), check the “protect” signal at J8 pin 6. If the voltage on J8 pin 6 is greater than approximately +0.7 VDC, it will turn on Q202 and If the voltage is less than approximately -0.7V, it will turn on Q203. Turning on either Q202 or Q203 causes Q202 and Q203 to latch and this will activate the crowbar. If there is a fault condition at J8 pin 6, check the ±12 VDC, ±17 VDC and ±34 VDC power supplies. If the ±12 VDC power supply is not working and the ±34 VDC power supply is working, check resistive fuses R714 and R713 located on the amplifier PCB. A failed component could be causing one or more of these supplies to sag, causing the unit to crowbar off. If the DC power supplies are working, continue onto step 3.2.

3.2 DC offset at the output of the bass amplifier J703 pin 2 (+) and pin 1 (-) will produce a fault condition ‘protect” voltage (greater than approximately ±0.7 VDC) at J8 pin 6. Check the components in the bass amplifier with an Ohmmeter.

3.3 If the bass module crowbars off after approximately 3 seconds and the computer displays an error code “--S2++” on its screen, there could be DC offset on one or more satellite outputs. The satellite outputs are summed through the “speaker output DC offset” circuit (SD251571, grid location A7). The output of this circuit, P66, is sent to the microcontroller U202 pin 25. In normal operation, the voltage at U202 pin 25 should be 2.5 VDC. If the voltage strays more than 1 VDC from the normal 2.5 VDC, microcontroller U202 pulls pin 39 (P22) to ground (normally high impedance) pulling R308 to ground latching the circuit consisting of Q302 and Q303 (SD251571, grid location B4). This latch circuit, when latched, will shut off the opto-isolator U300, which will shut off the triac D302 disconnecting AC from the primary of the transformer.
Note: U202 pin 26 is connected to U202 pin 39. The head unit does not send an “ON” command to the bass module. The uC knows when the power has just come up by watching the status of the 10V turn-on voltage via pin 26, which is connected to the same circuit mentioned above that the uC uses to shut down the triac.

3.4 If after checking everything listed in procedure 3 it is determined that the bass module is not crowbarred off and there is no boot prompt showing on the computer screen, the bass box to PC link might be bad. Go to procedure 4.

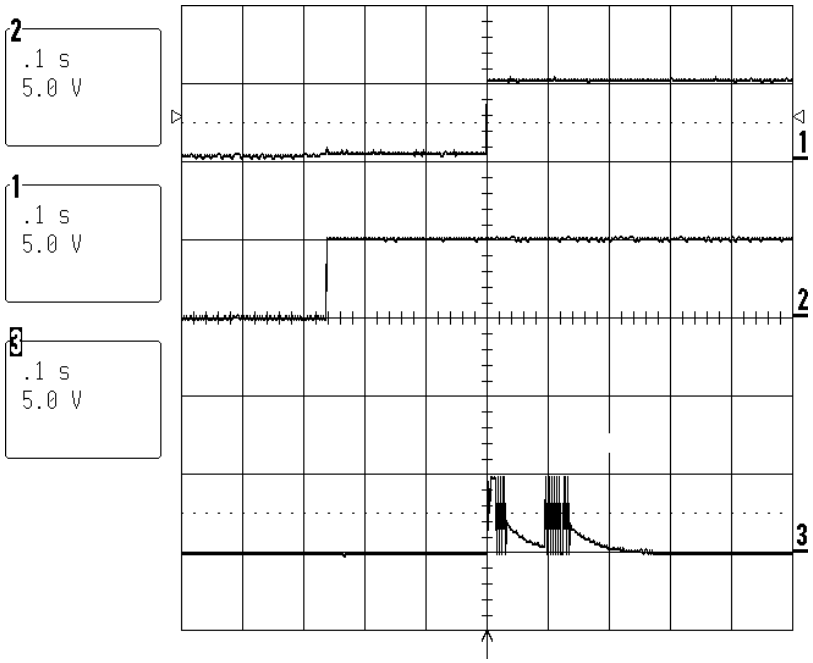
Troubleshooting Procedures

4. Microcontroller Circuit Check

4.1 The serial data output leaves the DSP PCB at J5 pin 11 (U202 pin 43, TTY OUT) and the boot prompt can be checked here at power-up with an oscilloscope. The first thing the uC is supposed to do when it comes out of reset is to print the following to the “debug” output J5 pin 11.

**
%0001#01

This is visible as two bursts of activity. One immediately following the rising edge of the RESET line (**) and one about 50 msec later (%0001#01). After printing the boot prompt, the uC will only print error codes. Thus, a lack of activity on this signal after the initial two bursts is expected. Short bursts of activity is likely to be the uC printing out an error code. Refer to Figure 30.



Upper trace: RESET (active low) pulse U202 pin 14 or U200 pin 2
Middle trace: +5V supply
Lower trace: Serial data from uC, J5 pin 11

Figure 30. Scope Photo of Boot Prompt at J5 Pin 11

4.2 If there is no boot prompt at U202 pin 43, then check for the following; +5 VDC at U202 pin 40 and U202 pin 18, 8 MHz clock on both sides of X600, reset pulse at power-up at U202 pin 14.
If the +5 VDC, 8 MHz clock and reset pulse are okay and there is no boot prompt, then the Uc has failed. Replace the Uc U202.

Troubleshooting Procedures

5. Boot Prompt Returned with an Error Code

5.1 Connect AC mains voltage to the bass box, and then connect the 10V turn-on signal to the 3.5 mm mono plug located on the test cable. Wait at least 5 seconds for error codes to appear. Refer to the following table for an explanation of the error codes.

Error Code	Description	Action
--11++	Uc can't communicate with the DSPs. One or both DSPs are dead, probably due to failure to boot	
--12++	Error with DSP1 communication	
--14++	DSP1 has failed to receive good audio data from the codec.	Check the clock, fram_sync or audio data signals from codec.
--22++	Error with DSP2 communication. Generally due to boot failure.	
--25++	DSP2 failed to acknowledge mute request. Generally due to boot failure.	
--C1++	I2C (I squared C) communication with codec failed.	Check I2C buss from micro (U202) to codec (U100); U202 pin 32 to U100 pin 4, U202 pin 33 to U100 pin 3.
--C2++	Codec voltage reference (2.3 V at U100 pin 16) out-of-bounds.	Check for 2.3 V at U202 pin 24.
--C3++	Codec clock error.	
--C4++	Codec PLL error.	
--I6++	EEPROM initialization error. The data in the non-volatile memory (EEPROM U201) is corrupted and all data was re-written with default values.	This error always occurs whenever a blank EEPROM is encountered, which happens the first time the DSP PCB is powered-up, or when the EEPROM is deliberately erased.
--E4++	EEPROM checksum error. Data appears to be reasonably OK, but the checksum is apparently corrupted.	Initializing the EEPROM (error –16++ above) does not re-calculate the checksum so this error happens the second time the DSP PCB is powered-up.
--S1++	Severe over-temperature.	Check the voltage at U202 pin 21. (TAP command "ad2"), check against R207 graph. Check threshold in EEPROM (address 0A, data 3C).
--S2++	DC offset on satellite channels.	Check satellite amplifiers with an Ohmmeter. Check voltage on U202 pin 25 (TAP command "ad 6") it should be "7F" (2.5V).
--S3++	Uc thinks the 3.3V power supply is out-of-bounds.	Check 3.3V supply U101 pin 20 against uC ADC port U202 pin 22 (TAP command "ad 3", normal is "A8").

Troubleshooting Procedures

6. Boot Prompt Okay, No Error Codes

6.1 Check the software revision by entering the TAP command “tv” into the computer. You do this by typing the command in the terminal window and pressing the ENTER key. The modules response will show up in the terminal window. The computer should return two numbers, i.e. 2300/2300; the first set of numbers is the rev. of the uC (rev. 23) and the second set is the rev. of the DSP (rev. 23). Ignore the zeros. The uC rev. should be equal to or greater than 23 and the DSP rev. should be equal to or greater than 23. If they are not, the microcontroller U202 and the DSPs external PROM U401 should be replaced.
If both numbers are displayed, both the uC and the DSPs have booted. If only the first number is displayed (e.g. “2300/”), then the DSP is not responding. Go to procedure 11, Miscellaneous DSP PCB Troubleshooting Tips. If the uC and the DSP check good, go to procedure 7.

7. Microcontroller and DSP are Okay, No Audio Output From One or More Channels

7.1 Apply a 200 Hz, 50 mVrms signal to the left and right inputs.

7.2 Put the bass module into “test mode 6” by entering the following TAP commands into the PC;

rs	(system reset)
sk 31,3f, ff	(un-mute power amplifiers)
tn 6,0,0,0,0,0,0,0,0	(test mode 6)

This will pass the left audio input to the bass output and the right audio input to all 5 satellite outputs with no signal processing, no equalization and no volume control.

7.3 Reference a dB meter to the applied signal. Measure the bass and satellite outputs.
- Bass gain = 31 ± 2 dB (from audio input to speaker output, in test mode 6)
- Satellite gain = 21 ± 2 dB

7.4 If the 200 Hz signal does not appear at all speaker outputs, go to procedure 8.
If the 200 Hz signal does appear at all speaker outputs, the bass module is working and able to pass an analog signal. If there is no output when only using a SPDIF (Sony/Philips Digital Interface Format) input, go to procedure 9.

Troubleshooting Procedures

8. No Audio at Speaker Outputs

8.1 If there is no audio from the speaker outputs when an analog signal is applied to the input of the bass module, follow the audio signal path through the system. Refer to the following table. If there is audio from the speaker outputs when an analog signal is used but not when a SPDIF (Sony/Philips Digital Interface Format) signal is used, go to procedure 9.

Verify	At Location	Note
Signal at input connector	J5 pin 9 (L) and pin 1 (R)	DIN input connector
Digital data from codec	U100 pin 38 (sclk) U100 pin 37 (frame_sync) U100 pin 36 (data from codec)	For pin 38 see Fig 34 For pins 37 and 36, see Fig 33
Digital data from DSP to codec	U100 pin 34	See Figure 33
Codec output	U100 pin 21 (right surround) U100 pin 22 (bass) U100 pin 23 (center) U100 pin 24 (left surround) U100 pin 25 (left) U100 pin 26 (right)	High frequency noise, 2.3 Vdc bias
Buffers output	U103 pin 1 (left) U103 pin 7 (right) U103 pin 8 (center) U103 pin 14 (left surround) U104 pin 1 (right surround) U104 pin 7 (bass)	Gain of 6, no DC bias, less high frequency noise
Output at connector	J8 pin 9 (left) J8 pin 7 (right) J8 pin 10 (center) J8 pin 12 (left surround) J8 pin 13 (right surround) J8 pin 11 (bass)	Analog audio exits the DSP PCB at this point to enter the amplifier PCB
Amplifier mutes okay	J8 pin 17 (bass, left, right) J8 pin 16 (center) J8 pin 15 (left surround, right surround)	0V = muted 5V = un-muted

9. No Audio output when using a SPDIF Input

9.1 Apply a SPDIF signal to the bass module SPDIF input and enter the following TAP commands into the PC;
rs (reset)
sk 31, 11, 0f (-10dB volume)
sk 51, af, ff (AUX input)
verify audio at speaker outputs and no codec-related error codes (see procedure 5 for error codes).

9.2 Check SPDIF signal path (Figure 54);
• J5 pin 4
• U100 pin 42 (if codec is in digital mode there should be 2.3 VDC on pin 42).

9.3 Verify the DC voltage on the PLL line is clean; indicates that the PLL has locked onto the SPDIF signal.

9.4 Capture the PLL tuning voltage as it goes from 0V (analog mode) to about 2V (digital mode). Voltage should slew and settle within about 5 msec. Any AC on the tuning line after the initial 10 msec indicates a stability problem in the PLL circuit.

9.5 Verify that there is no error bit output from the codec. U100 pin 30 should be 0V.

9.6 Verify that the uC can see the SPDIF input. Check the voltage at the collector of Q201 and U200 pin 23. The voltage should be < 1 VDC, if there is an SPDIF present and > 4VDC if there is no SPDIF.

9.7 If the problem cannot be located, go to procedure 10.

10. Quick Check/Possible Problems With DSP PCB

10.1 Because the DSP IC's legs are very fine, there is a chance for shorts or opens. Probing the DSP IC's legs can cause shorts. Boot data can be garbled due to a short or open on the DSP IC pins. This type of error is generally indicated by the "--11++" error code.

10.2 The 40 MHz oscillator, CR400, might not be working.

10.3 There might be a broken "via" in the PCB. This is a hole in the PCB that connects traces on the top side of the PCB to traces on the bottom side of the PCB. This type of problem can be difficult to isolate.

10.4 If the problem has not been isolated, go to procedure 11.

11. Miscellaneous DSP PCB Troubleshooting Tips

11.1 +17V, ±12V Power Supplies

The PCB draws power from three different supplies:

11.1.1 +17V unregulated, at about 250 mA when everything is running normally. The +17V supplies the unregulated voltages for the two voltage regulators on this PCB: the +5V linear regulator U1, and the 3.3V switching regulator U500. The +17V is brought onto the PCB from J8 pin 3.

Note that the +17V unregulated supply can vary from about +17V to as low as +10V, depending on conditions. On the bench, the value may be more typically +15V or so. Whatever the exact voltage, in this document it will be referred to as the "+17V" supply.

11.1.2 ±12V, at about 40 mA. The ± 12V supplies are for the op-amps U103 — U105. +12V is brought onto the PCB from J8 pin 1, and -12V is supplied from J8 pin 5.

11.2 +5V Supply

Check the +5V supply first, since the +5V powers the micro and without the micro, nothing else works. Check the following points:

11.2.1 At the input side to the +5V regulator U1. This is a typical 7805 3-terminal linear regulator, so it needs at least 7.5V at the input to stay in regulation. If there is +17V at J8 pin 3, but no voltage at the input side of U1, check the components in between (R10 and R11, large SMD resistors on the bottom side).

11.2.2 At the output side of the +5V regulator. Check that the 5V output is clean and that the regulator is not oscillating. The regulated +5V is supplied to the rest of the PCB via a couple of filter components, so check for +5V at the following points:

11.2.3 U102 pin 20; if no +5V here, check L200 (bottom side, between U101 and U104).

11.2.4 U100 pin 40; if no +5V here, check both L2 (top side, near U100 pin 20) and L1 (bottom side, directly under U100).

11.3 8 MHz Clock

The micro requires an 8 MHz clock to run. This clock is developed by an internal oscillator which requires an external ceramic resonator (X600). Check for the 8 MHz clock at:

11.3.1 Ceramic resonator X600 (top side, next to U202). There should be a roughly sinusoidal waveform, 0V to 5V, on both sides of X600.
If there is no 8 MHz clock, possible causes are:
- No +5V; check L200.
- Poor soldering

If the 8 MHz clock is present at X600, and its amplitude is roughly 5Vpp, but the microcontroller won't issue a boot prompt or turn on the 3.3V power supply, possible causes are:
- Dead micro.
- A missing RESET pulse at power up. Power the board down and back up again, and verify that the micro is getting a healthy RESET pulse at power up. The reset IC (U200, SOT-23 bottom side) should hold the micro's RESET input (pin 14) low for about 250 msec after the +5V supply has stabilized. The RESET input should transition from low to high cleanly and briskly — if it appears to be floating, check R280.

11.4 3.3V Supply

The 3.3V supply is supplied by the switching regulator IC U500. This IC works by rapidly switching its output between +17V and ground; the output filter (L500 and C500) blocks the 100 kHz switching waveform and passes only the average 3.3 VDC. Note that the micro can turn U500 on or off, via one of its output ports (U202 pin 41) and Q500. U500 powers up off with its "soft-start" node (pin 19) clamped to ground, which inhibits operation, and it remains in this state until the micro boots successfully and pulls the base of Q500 to ground. The point to remember is that the 3.3V supply does not power up until after the micro boots successfully.
Assuming that the micro does boot successfully, check U500 for the following waveforms at the following points (refer to sheet 5 of the schematic):

11.4.1 +17V on both sides of the surface-mount inductor L501 (top side).

11.4.2 5.1 VDC at U500 pin 18. This is a reference voltage generated by U500. Its presence here on pin 18 will show that U500 is getting power.

11.4.3 Check that U500 pin 11 is connected to ground. This pin is U500's ENABLE input; if it isn't grounded, U500 shuts down.

11.4.4 Check that the base of Q500 (bottom side) or U202 pin 41 (same node) is pulled to ground. If Q500 is turned on, U500 shuts down. This node is pulled up to +5V with R282 (sheet 2); the micro pulls this node low after it boots. If the micro doesn't boot, U500 never turns on.

11.4.5 100 kHz switching waveform, Figure 40, on the +17V side of the toroidal inductor L500. This waveform should switch rapidly (<100 nsec) between about -0.35V and VCC, with an average DC voltage of 3.3V. If the voltage at this node dips well below -0.35V, then check D500 (bottom side).

11.4.6 If still no luck, check L500. If it's a toroidal inductor, check that it's properly soldered to the PCB.

11.5 11.2896 MHz Codec Clock

If the micro and DSP appear to have booted properly, but no audio signal passes through the PCB, check the codec U100 for signs of health. The codec does not power up in a useful state all by itself; the micro must program a number of internal registers via the I 2 C buss inputs to the codec . (I 2 C is a 2 wire serial buss; one line for the data, one line for the clock.) To quickly determine if the codec was properly initialized by the micro, check for;

11.5.1 0V — 5V, 11.28 MHz sine wave, Figure 38, on both terminals of the crystal CR100.
If the 11.28 MHz clock is not oscillating, possible causes might be:
- No +5V power to the codec U100. Check both power pins (19 and 40). If there's power on one but not the other, check L1 and R3 (bottom side, directly under U100).
- I 2 C data or clock signals missing. Check for digital activity (0V — 5V) on these signal paths.
  U202_32 — R253 — U100_4
  U202_33 — R265 — U100_3
- Poor soldering

If the 8 MHz clock is present at X600, and its amplitude is roughly 5Vpp, but the micro controller won't issue a boot prompt or turn on the 3.3V power supply, possible causes are:
- Dead micro.
- A missing RESET pulse at power up. Power the board down and back up again, and verify that the micro is getting a healthy RESET pulse at power up. The reset IC (U200, SOT-23 bottom side) should hold the micro's RESET input (pin 14) low for about 250 msec after the +5V supply has stabilized. The RESET input should transition from low to high cleanly and briskly — if it appears to be floating, check R280.

Once the micro boots, there is a fair amount of regular activity on these two lines. The micro checks the codec's error status register about every 5 msec , so if these lines are silent, suspect a bad micro or a broken connection somewhere between the micro and the codec. Also, the micro will output an error code if it detects an on going problem with the I 2 C.

• A problem in the network of components around CR100, R175, R176, C139, C140. Check CR100

• Codec power-down input at pin 8. Normally, this signal is pulled up for proper codec operation. When this pin is low, the codec enters a low-power reset state. The micro will pulse this line low for a few msec to reset it prior to initialization. If this line is held continuously low for some reason, the codec's oscillator won't operate, and the analog reference voltage (about 2.3V) at pin 16 disappears.

If the 11.28 MHz codec clock is oscillating, then verify the following digital output signals from the codec:

11.5.2 Bit clock at R186, U100_38: 11.2896 MHz square wave

11.5.3 Frame clock at R185, U100_37: 44.1 KHz square wave

11.5.4 Output data, U100_36: "irregular" digital activity at R187, similar to Figure 44.

11.6 Input analog signal path to codec

Apply a 1 VRMS signal to both the L an R inputs to the PCB (J5 pins 9 and 1), and check for the signal at the two analog inputs to the codec (pins 13 and 14).

11.6.1 Gain from J5 to U100: -6 dB

11.6.2 DC bias at U100 pins 13 and 14: 2.3V

If you don't see any signal at the codec inputs, trace the analog signal path through from J5 (sheet 1 of the schematic) to figure out where it disappears. Also, check the ± 12V power supplies on the op-amps.

11.7 Codec Revision Code

The CS4226 codecs must be rev. G or higher. Specifically, the rev. code must NOT be "C". The rev. letter is the letter immediately preceding the date code silkscreened on the IC, e.g.
CRYSTAL (logo)
CS4226-KQ EP (part number)
JTAAXG9819 (rev. G, date code 9819 [19th week of '98])

11.8 DSP 40 MHz Clock

11.8.1 The DSPs run on a 40 MHz clock; the easiest place to check for this is at J401_4. (J401 is the unloaded 14-pin connector between DSP2 and the shield fence.) This is a buffered version of the 40 MHz clock that drives the DSP. This clock has very fast edges (3 nsec rise times), so if you're using a low-quality 'scope probe, don't be too alarmed by what you see. A cheap 'scope probe or a long or missing ground lead will distort this signal beyond recognition.

In this case, it's ugly, but it's not a serious issue — all you're trying to do is verify that the clock is oscillating. However, pay attention to the frequency — this is a third overtone oscillator, which means it may prefer to oscillate at 13.333 MHz (40/3). If the network of components around CR400 is incorrect in some way, it may prefer to oscillate at some frequency unrelated to what's printed on the crystal.

11.8.2 40 MHz clock frequency at U104 pin 4: 40 MHz

If there's no 40 MHz clock at all,
- Check U400 (LCX00) for proper soldering, and check for 3.3V on U400_14.
- Check to make certain that all the components around the crystal (C402, C403, R411, R412, R409 — bottom side, under CR400) are OK.

11.9 DSP Reset Pulse

Check for a clean DSP reset pulse at the collector of Q200 (top side, near U102). At power-up, Q200 is biased on, driving the collector low, until the micro boots properly. After the micro boots, it turns Q200 off and allows the DSP reset line to be pulled high. This signal is digital, and should be either at 0V or at 3.3V. Typing "rc" in the computer will produce two narrow (about 50 usec) DSP reset pulses.

11.10 Digital One-shot U106

U106 is a flip-flop wired up to produce a narrow pulse on the falling edge of the 44.1 KHz clock. Without the signal that this IC produces, the DSP can't send or receive from the codec properly. Inputs to U106:

11.10.1 U106 pin 1: 44.1 KHz clock

11.10.2 U106 pin 5: 11.28 MHz clock

Output from U106:

11.10.3 U106 pin 13: 100 nsec pulse, at 44.1 KHz rate, similar to Figure 42.

11.11 5V / 3.3V level translators

The micro (U202) and the codec (U100) run on +5V, while the DSPs run on 3.3V. There are a couple of level-translator ICs required to bridge this gap:

U101, a 74LCX244, a 3.3V part which has "5V tolerant" inputs.
U102, a 74ACT244, a 5V part with input logic thresholds that are compatible with 3V logic ("TTL", or 0.8V/1.5V).

Since there's a problem somewhere on the PCB , it isn't safe to assume that you'll be able to observe any digital activity on the pins listed on the next page, although normally there would be. Mainly what we're looking for is evidence that a buffer gate isn't buffering; i.e., a signal is present on the input, but there's no similar signal on the output.

Troubleshooting Procedures

From the codec U100 to DSP1: (See Figure 31 below)
U101_13 —> U101_7
U101_15 —> U101_5
U101_17 —> U101_3

From DSP1 to the codec U100
U102_2 —> U102_18
U102_4 —> U102_16

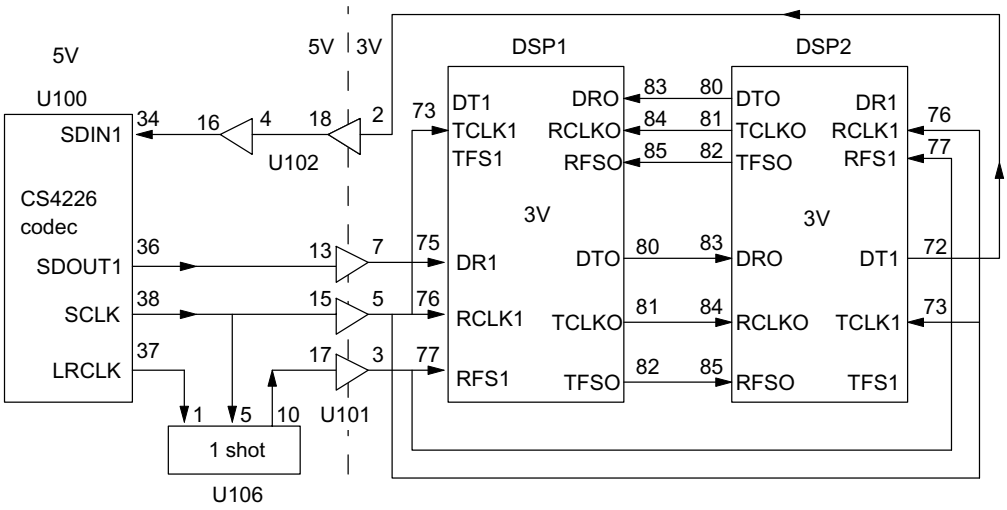


Figure 31. Codec to DSP, Digital Audio Signal Path

From the micro to DSP1:
U101_4 —> U101_16
U101_2 —> U101_18

From DSP1 to the micro:
U102_15 —> U102_5
U102_17 —> U102_3

From the micro to DSP2:
U101_8 —> U101_12
U101_6 —> U101_14

From DSP2 to the micro:
U102_11 —> U102_9
U102_13 —> U102_7

(See Figure 32 at right)

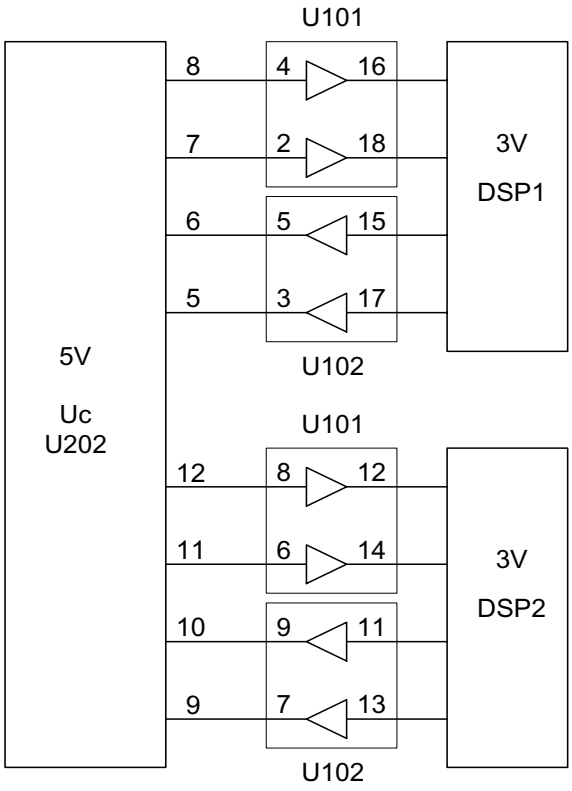


Figure 32. Micro to DSPs

11.12 Evidence that the DSPs have booted

11.12.1 Error codes

Check for the absence of any error codes following the boot prompt. Error codes in the teens or twenties (e.g., “—12++” or “—22++”) indicate that the micro is having trouble communicating with either DSP.

11.12.2 tv command

To see if the micro can talk to DSP1, issue a “tv” command, and expect to see something like “1400/1400” in reply. These two numbers represent the revision codes of the micro controller firmware (the first number) and the DSP firmware (the second number). If both numbers are reported back, then the DSPs have (probably) booted successfully.

11.12.3 DSP Output Ports

Observe the following signals as the power to the PCB comes up:
U102_15
U102_11
These signals are part of the communications buss between each DSP and the microcontroller, and are pulled up to +3.3V by resistors. One of the very first things that either DSP will try to do is talk to the micro, which initially requires pulling these signal lines low. If DSP1 is working, U102_15 will show some activity about 100 msec after the 3.3V supply comes up. If DSP2 is working, U102_11 will show some activity about 100 msec after the 3.3V supply comes up. If these signals power up to 3.3V and sit there doing nothing, then one or both of the DSPs failed to boot.

11.12.4 Boot Activity on External Address Buss

The DSPs have no internal program ROM, and must boot from the external PROM. The boot happens in two stages. First, a short (256 words) boot loader program is loaded automatically; second, the boot loader program is executed. Typically, the boot loader program loads the other 99% percent of the PROM contents into the DSP.

The first stage of the boot is hard-wired into the DSP, so as long as the DSP has power, a 40 MHz clock, and a few other signals, the first stage of the boot always happens when the reset line goes high. However, the second stage happens only if the boot loader program actually works, which of course it won’t if the DSP is trying to boot from an empty or damaged PROM, or if the data lines or address lines between the PROM and the DSP are shorted together.

Observe the activity on PROM pin 30 at power-up. A successful boot will show a flurry of activity about 30 msec long immediately following the release of the DSP reset line (collector of Q200). An unsuccessful short boot won’t last more than 300 usec. If it becomes clear that the DSPs aren’t booting, the problem might be caused by:

- Solder problems affecting the fine pitch leads on the DSPs. This is the most common source of DSP boot errors. Examine the leads of each DSP under an illuminated magnifying glass, checking for shorts (which are usually pretty easy to see) and opens (which sometimes are not).

- Solder problems affecting the 4 resistor r-packs. These are attached to some critical DSP buss signals, so a loose connection here can cause problems.

Scope Photos

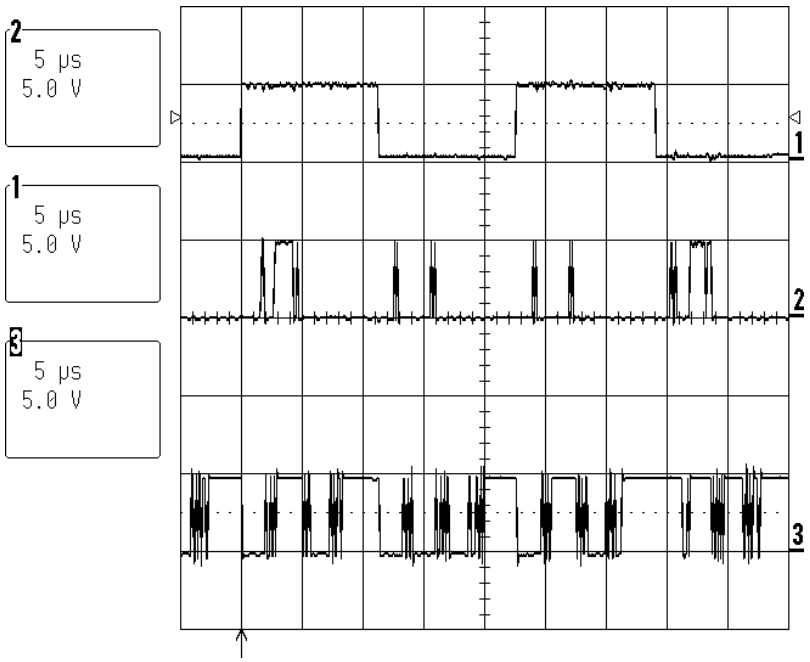


Figure 33. Codec (U100) Scope Photo, Un-mute Condition

Upper trace: LR_CLK (U100 pin 37) 44.1 kHz square wave
Middle trace: SDOUT1 (U100 pin 36) serial data out
Lower trace: SDIN1 (U100 pin 34) serial data in

For each period of the 44.1 KHz clock, there are 256 bits of data clocked in/out. The first bit of the data stream starts at the falling edge for LRCLK. The data falls into six time slots as follows:

Serial data out:

32 bits of LEFT ADC input, followed by
32 bits of AUX ADC input (not used), followed by
64 bits of nothing, followed by
32 bits of RIGHT ADC input, followed by
32 bits of AUX ADC input (not used), followed by
64 bits of nothing
Total: 64 bits from the codec

Serial data in:

32 bits of RIGHT SURROUND DAC input, followed by
32 bits of CENTER DAC input, followed by
32 bits of LEFT DAC input, followed by
32 bits of nothing, followed by
32 bits of BASS DAC input, followed by
32 bits of LEFT SURROUND DAC input, followed by
32 bits of RIGHT DAC input, followed by
32 bits of nothing
Total: 256 bits to the codec

Scope Photos

On the lower trace of Figure 33, you can see the six packets of audio data embedded in the bit stream. The bass module is muted when it is first powered up and will not un-mute until it receives an “un-mute” or “volume up” command.

Muted data consists of all zeroes; this condition is shown in the lower trace of the codec (U100) scope photo, mute condition.

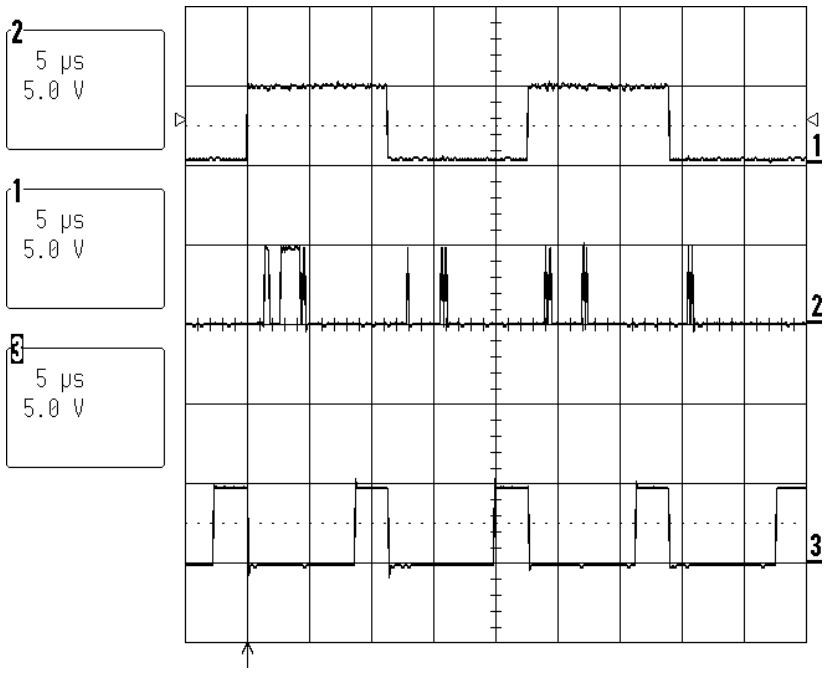


Figure 34. Codec (U100) Scope Photo, Mute Condition

The significance of the SDOUT1 signal (U100 pin 36) is that it represents the digital audio data at the start of the digital audio signal path. This data is transmitted serially to the DSP1, which requires three signals to accept it:

SCLK (U100 pin 38): to clock the serial data in
LRCLK (U100 pin 37): to indicate the start of each audio sample
SDOUT1 (U100 pin 36): the serial audio data

The significance of the SDIN1 signal (U100 pin 34) is that it represents the output of the digital audio signal chain. The data is shifted out from DSP2 using the clock signals mentioned above. If this signal is dead, DSP2 is most likely not running.

Scope Photos

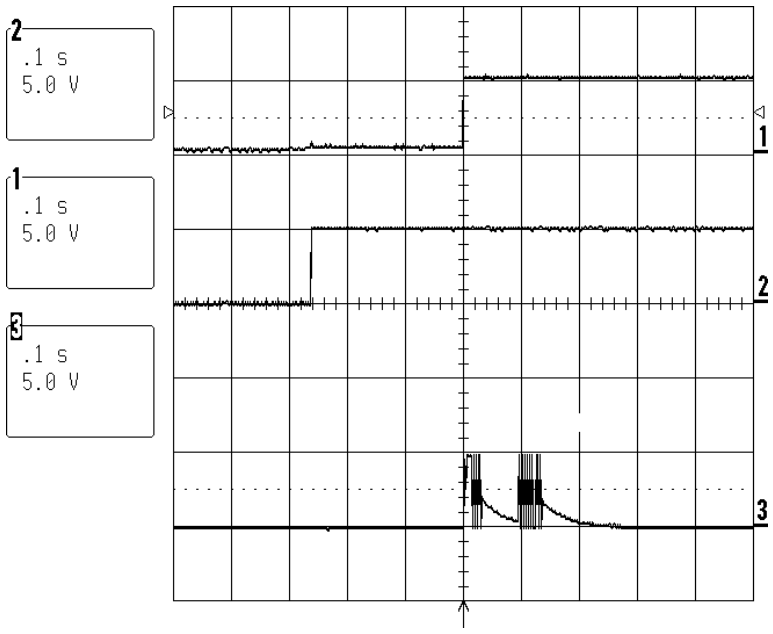


Figure 35. Microcontroller (U202) Scope Photo, Power Up

Upper trace: RESET pulse (active low), U202 pin 14 or U200 pin 2
Middle trace: +5V supply
Lower trace: Serial data from uC, J5 pin 11

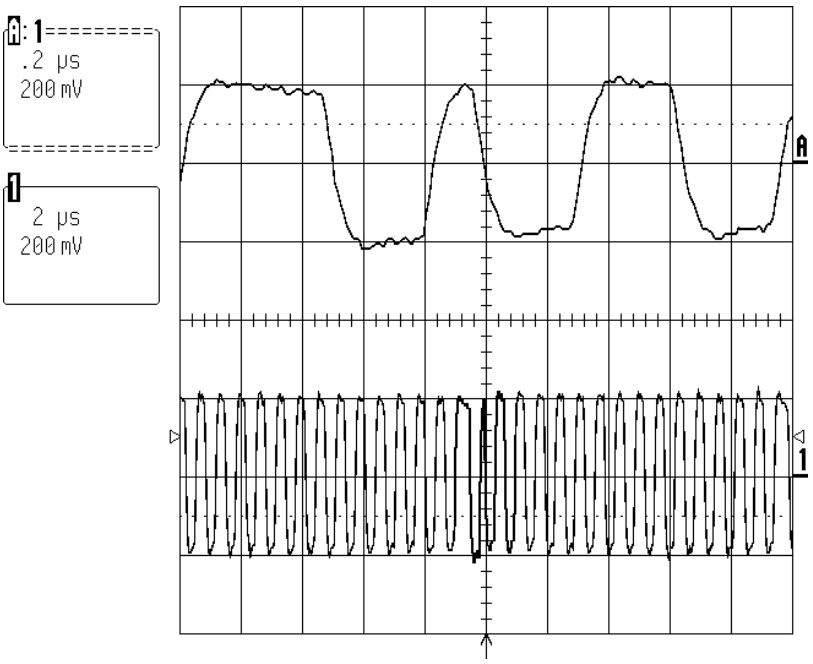
The first thing the microcontroller supposed to do when it comes out of reset is to print the following to the debug output J5 pin 11.

**
%0001#01

This is clearly visible as two bursts of activity (4800 baud), one immediately following the rising edge of the reset line (**) and one approximately 50 msec later (%0001#01).

After printing the boot prompt, the Uc will only print error codes. Thus, a lack of activity on this signal after the initial two bursts is expected. Short bursts of activity is likely to be the uC printing out error codes.

Scope Photos



Upper trace: Detail
Lower trace: SPDIF signal at the codec's SPDIF input (U100 pin 42)

Figure 36. SPDIF Signal at U100 pin 42

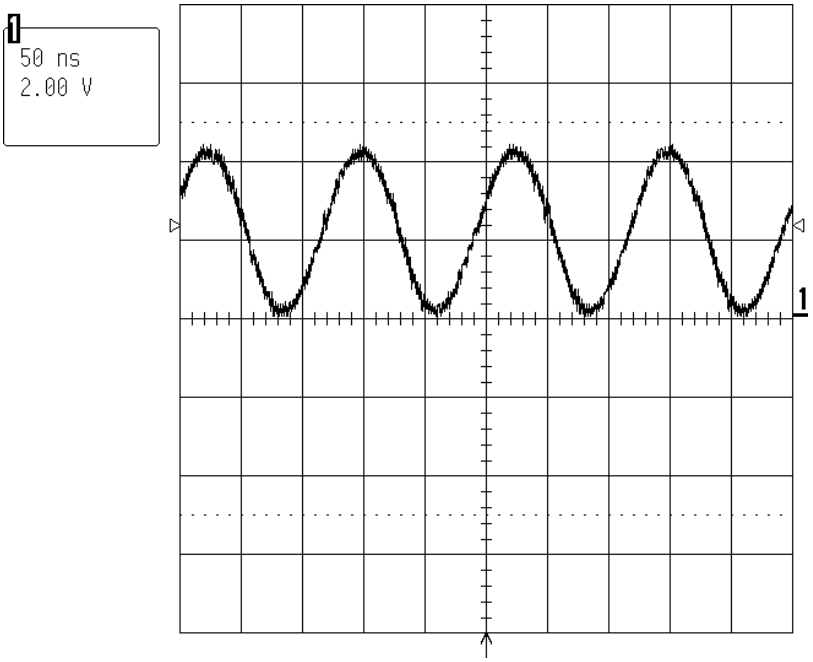
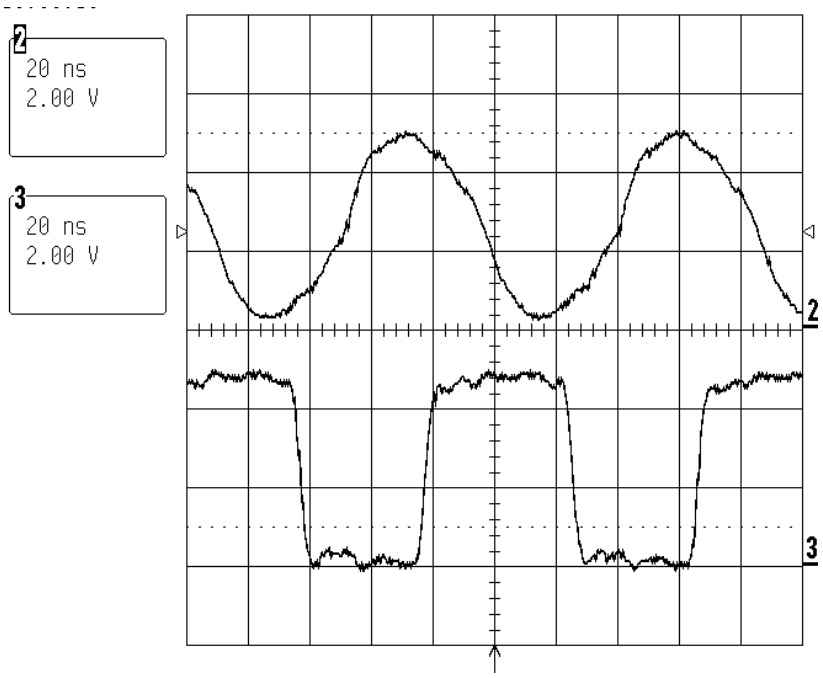


Figure 37. Microcontroller 8 MHz clock at U202 pin 39

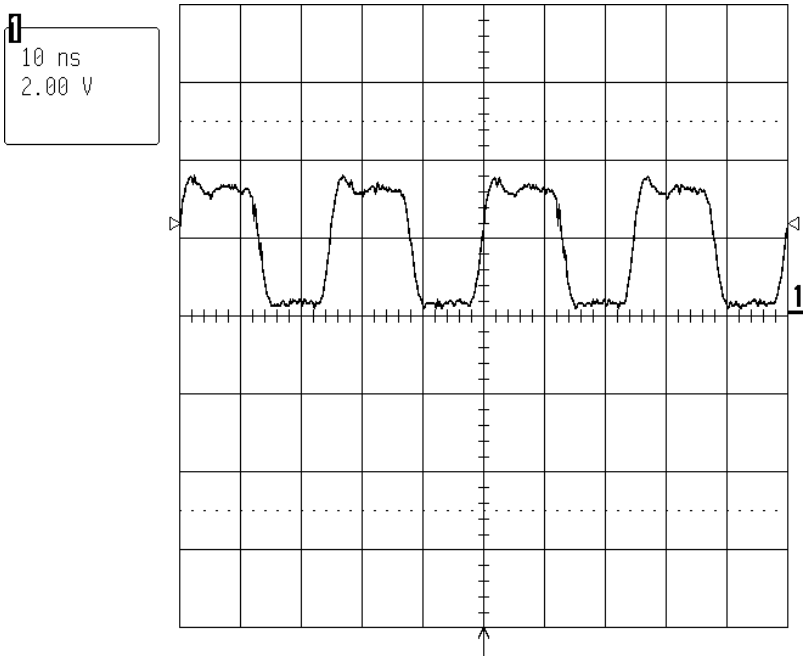
Scope Photos



Upper trace: Signal at CR100 crystal (U100 pin 29)
Lower trace: Buffered digital SCLK output (U100 pin 38)

This is the bit clock used to clock serial data in/out of the codec (see Codec (U100) Scope Photo, Un-mute condition and Codec (U100) Scope Photo, Mute condition)

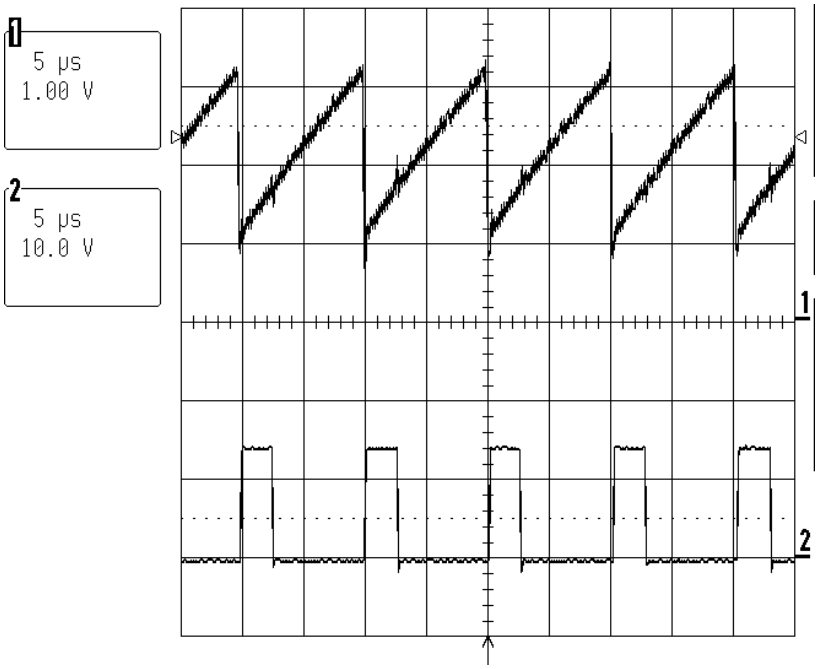
Figure 38. Codec 11.2896 MHz Clock



Buffered output at J401 pin 4 (14 pin unloaded connector)

Figure 39. 40 MHz DSP clock

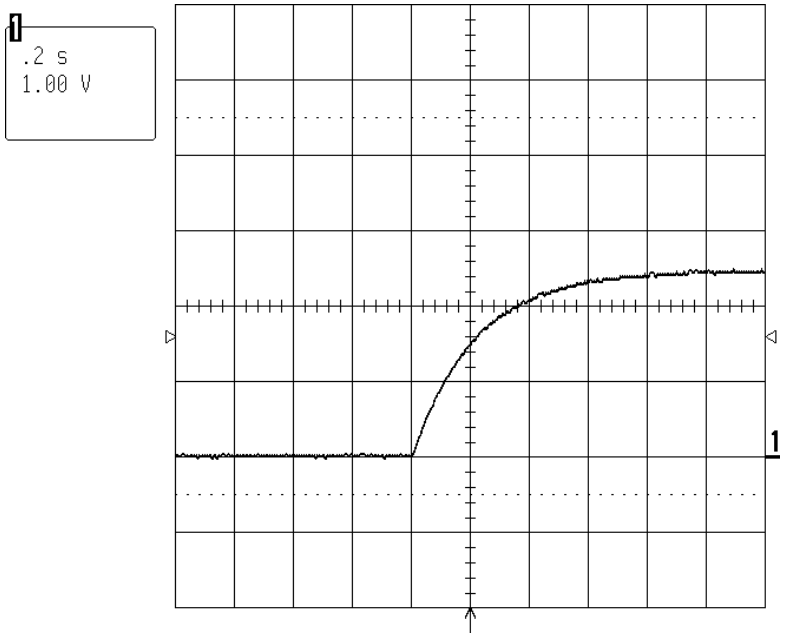
Scope Photos



Upper trace: U500 pin 1
Lower trace: U500 pin 2

The 100 kHz pulse train developed at U100 pin 2 (the lower trace) is applied to the output filter L500/C500. The average DC voltage of this pulse train is 3.3V, which can be found on the other side of L500.

Figure 40. 3.3V Switching Power Supply Signals



U202 pin 25 monitors the satellite DC offset circuit. Normal condition: 2.5 VDC. Fault condition: If the voltage strays more than ±1 VDC from the normal condition of 2.5 VDC, U202 will pull pin 39 to ground, shutting off the unit.

Figure 41. Power Up Condition at U202 Pin 25

Scope Photos

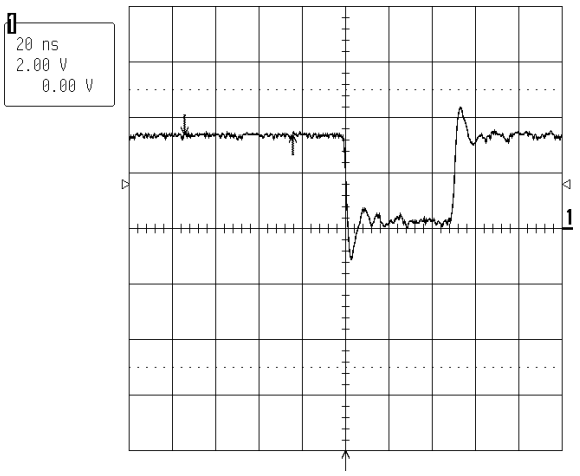


Figure 42. Transmit Frame Sync

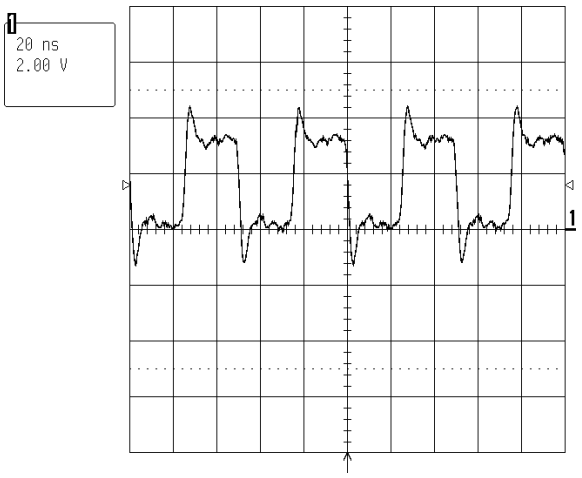


Figure 43. Serial Data Clock

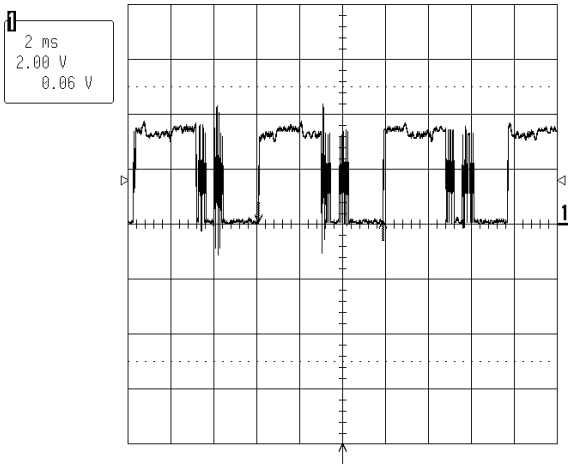


Figure 44. Audio Data

The audio serial data transmitted from DSP1 to DSP2 is sent via a high speed serial link, which requires 3 signals to operate.

- Serial Data Clock: This clock will either be 40 MHz (older software revision) or 20 MHz (version 30 and above).

- Transmit Frame Sync: A semi-periodic 50 nsec or 25 nsec pulse (depending on if it is a 40 MHz or 20 MHz clock).

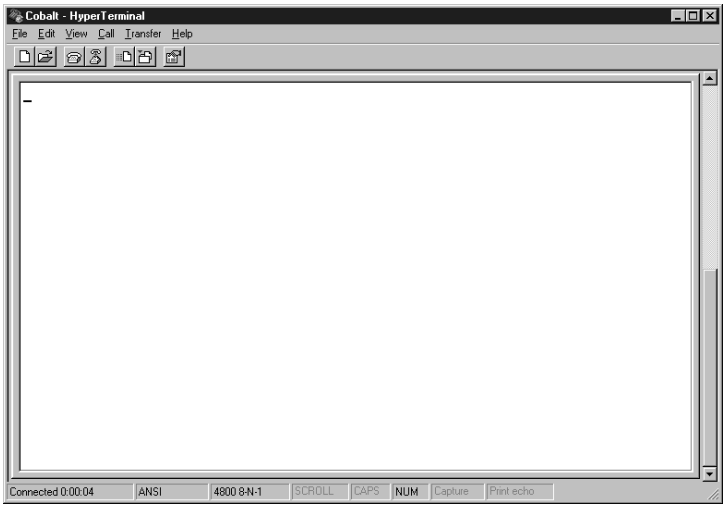
- Audio Data: This is sent over in bursts which have a fundamental pattern rate of about 5.8 msec. Audio data is digitally processed in blocks of 256 samples. 256/44.1 kHz equals 5.8 msec.

These three signals are unlikely to resemble the scope photos unless DSP1 is processing data. The presence of these three signals indicates that DSP1 has booted successfully.

Appendix

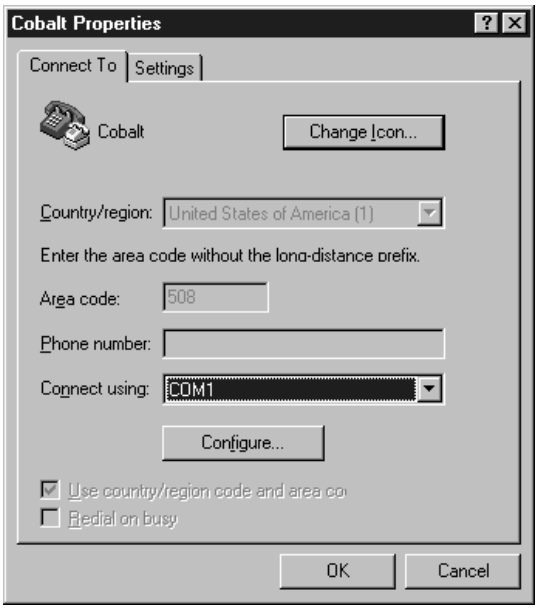
Computer Setup Procedure

Use this procedure to configure your IBM compatible PC for communication with the digital bass module.



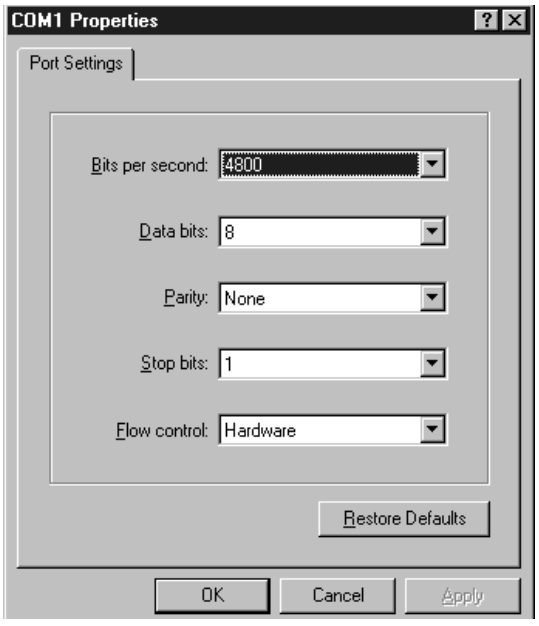
1. Open a terminal window, as shown at right, in either Terminal or Hyperterm, as applicable for the version of Microsoft® Windows® you are using on your PC.

2. In the terminal window, click on File, then Properties. Set the Test Properties in the dialog box as shown at right.



3. In the Test Properties dialog box shown in step 2, click on Configure to set the COM 1 Properties as shown at right. Click OK to return to the Test Properties dialog box.

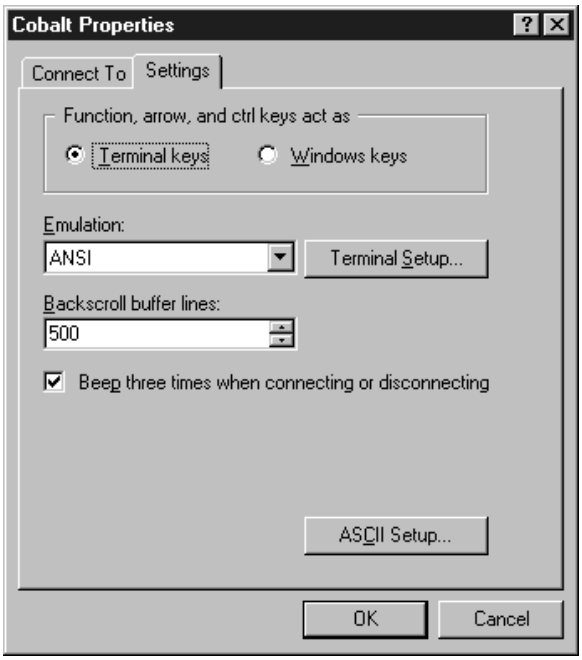
See the next page for the conclusion of this procedure.



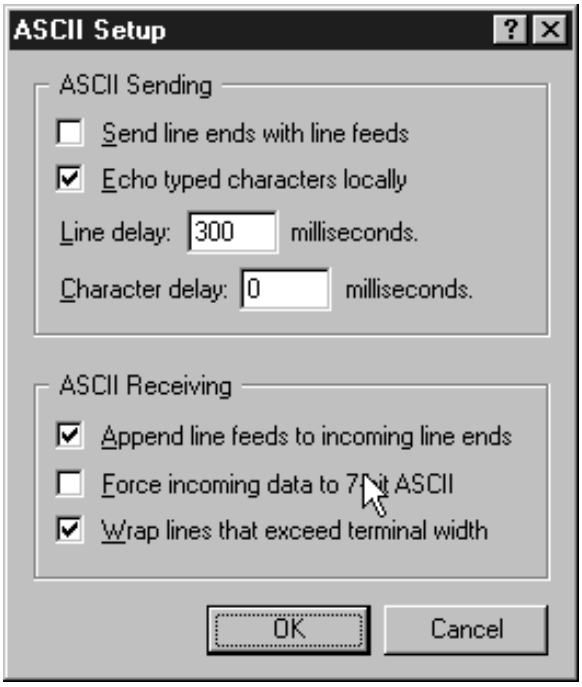
Appendix

Computer Setup Procedure (continued)

4. In the Test Properties dialog box, click on the Settings tab and set the controls as shown in the example at right.
Note: Be sure to check “Beep three times when connecting or disconnecting”.



5. In the Test Properties dialog box under the settings tab, click on the ASCII Setup button and set the controls to look like the dialog box at right. Click OK to return to the Test Properties dialog box.



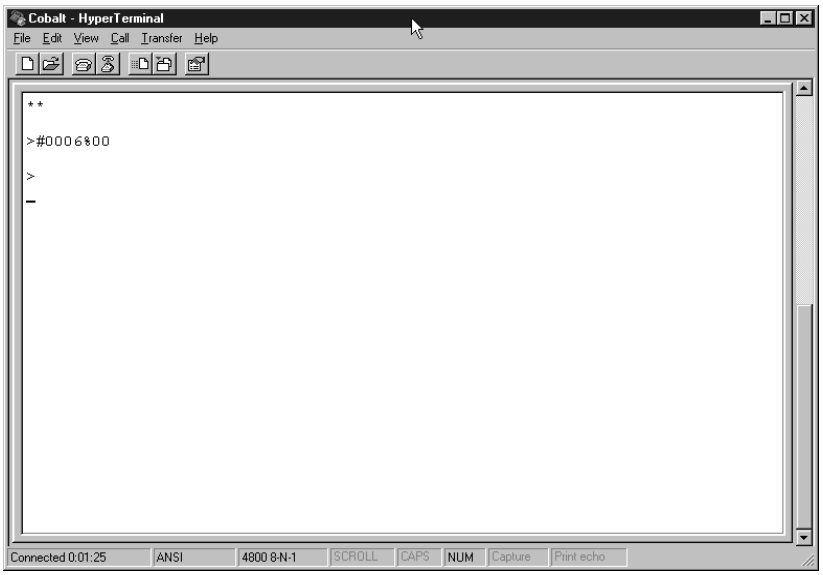
6. Once you have made all of the settings in the Test Properties dialog box, click OK to close it. You have now configured your PC to communicate with the digital bass module. To connect to the module under test, in the terminal window, click on Call, then Connect, and listen for 3 beeps. This will tell you that the PC is connected to communicate with the module.

Appendix

Computer Terminal Window Example Screens

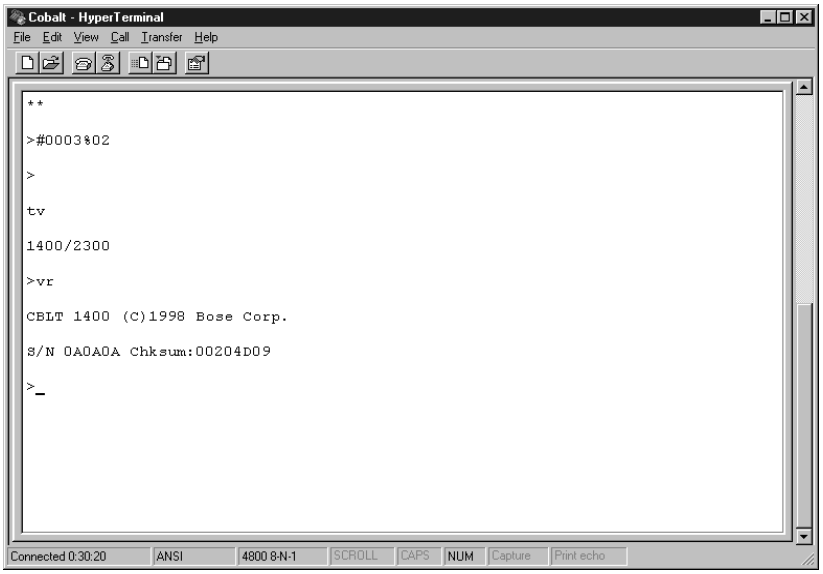
Module Turn-on Boot Prompt

At turn-on, the module will send the information shown in the window at right to the terminal window on your computer.
In this case, the response from the module tells you that the DSPs have booted (**) and that the module has received an OFF command from the head unit six times (0006) and is using the EQ (00) for the Lifestyle® Series I satellite speakers.



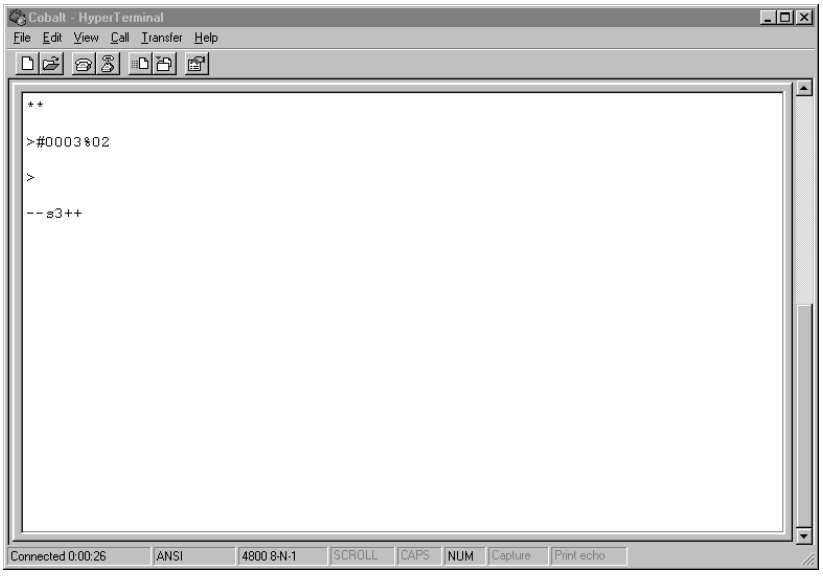
Module Response to Entered Commands

In this terminal window, after the boot prompt, you can see that the commands “tv” and “vr” have been entered, and we see the module’s responses to those commands. TV is the command to print firmware revisions. VR is the command to print the microcontroller checksum. Refer to the TAP Commands tables in the Appendix for a complete list of commands.



Error Code Response at Turn-on Boot Prompt

In this terminal window at right, we see the boot prompt, and we also see the error code --s3++.
Refer to the table on page 48 for a listing of error codes and their meaning.



Appendix

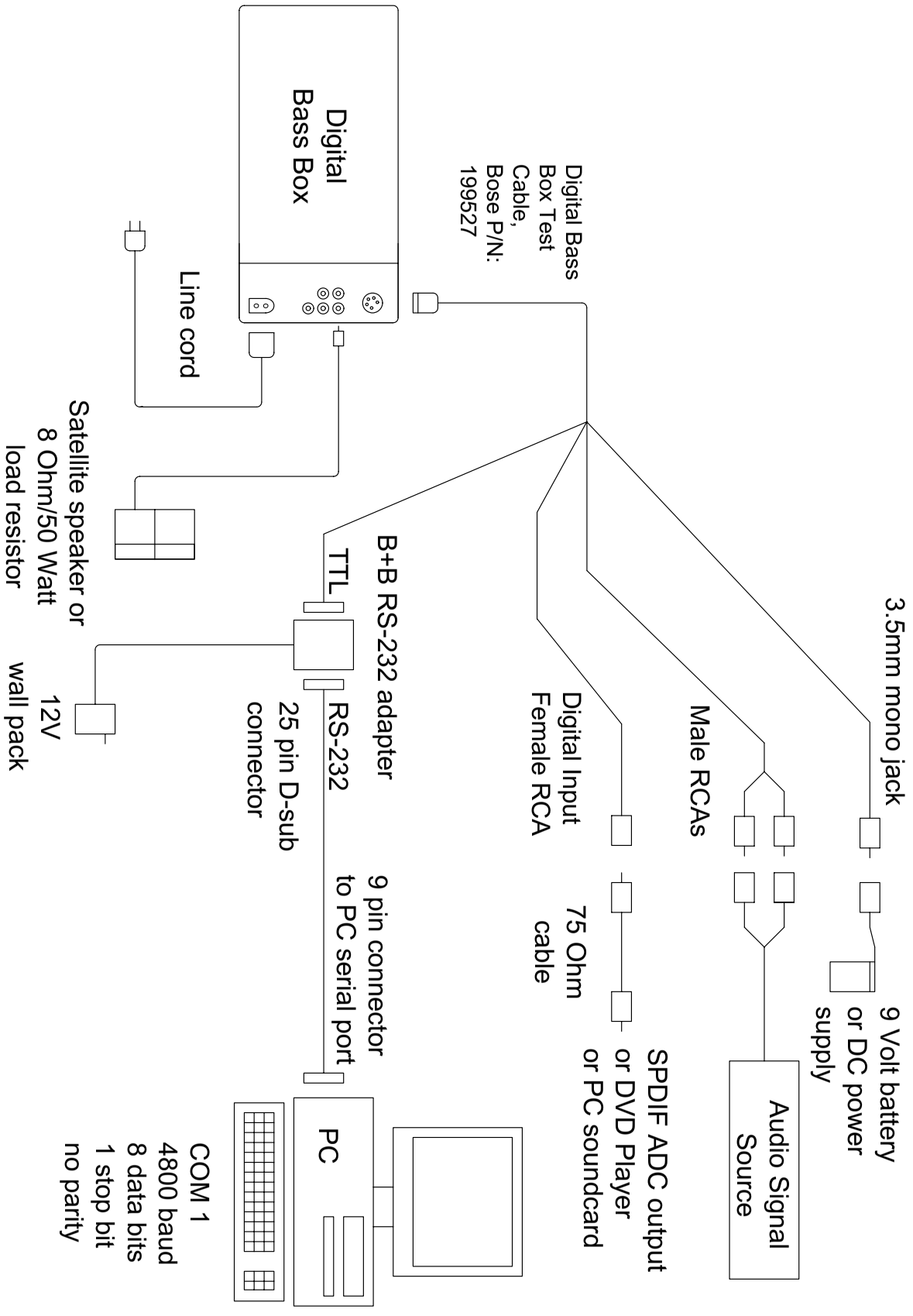


Figure 45. Test Setup Diagram

Appendix

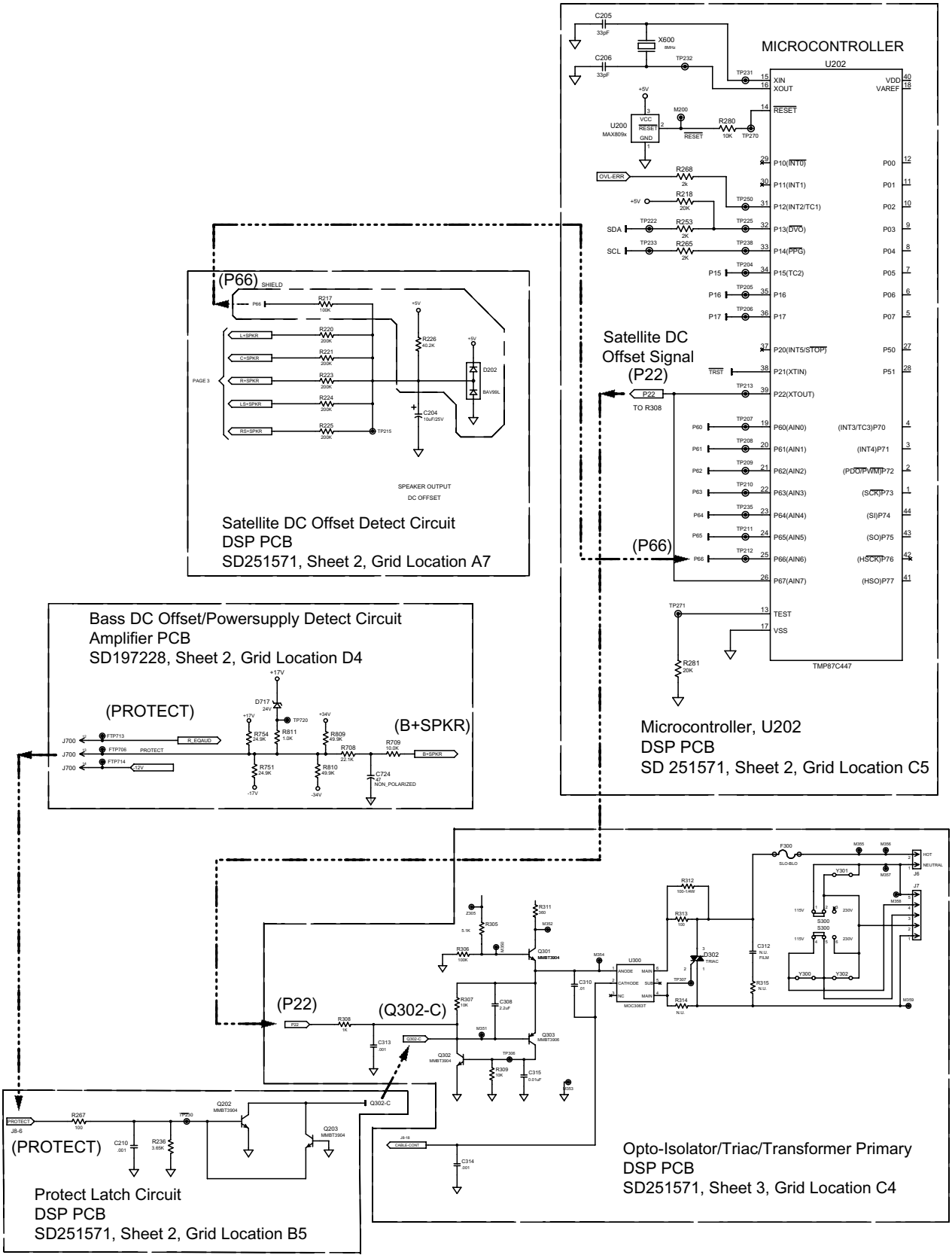


Figure 46. Fault Circuits

Appendix

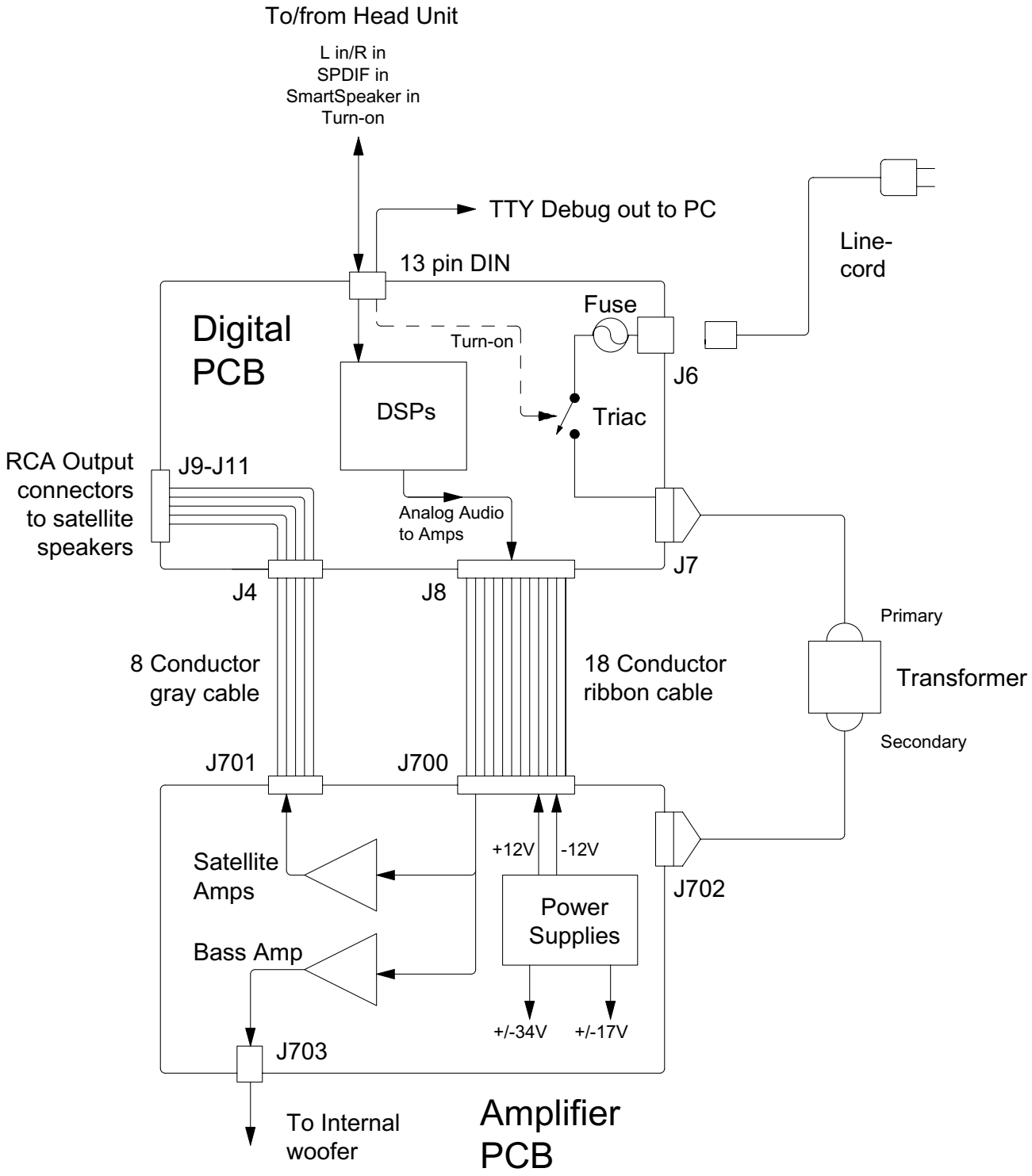


Figure 47. DSP PCB and Amplifier PCB Interconnection Diagram

Appendix

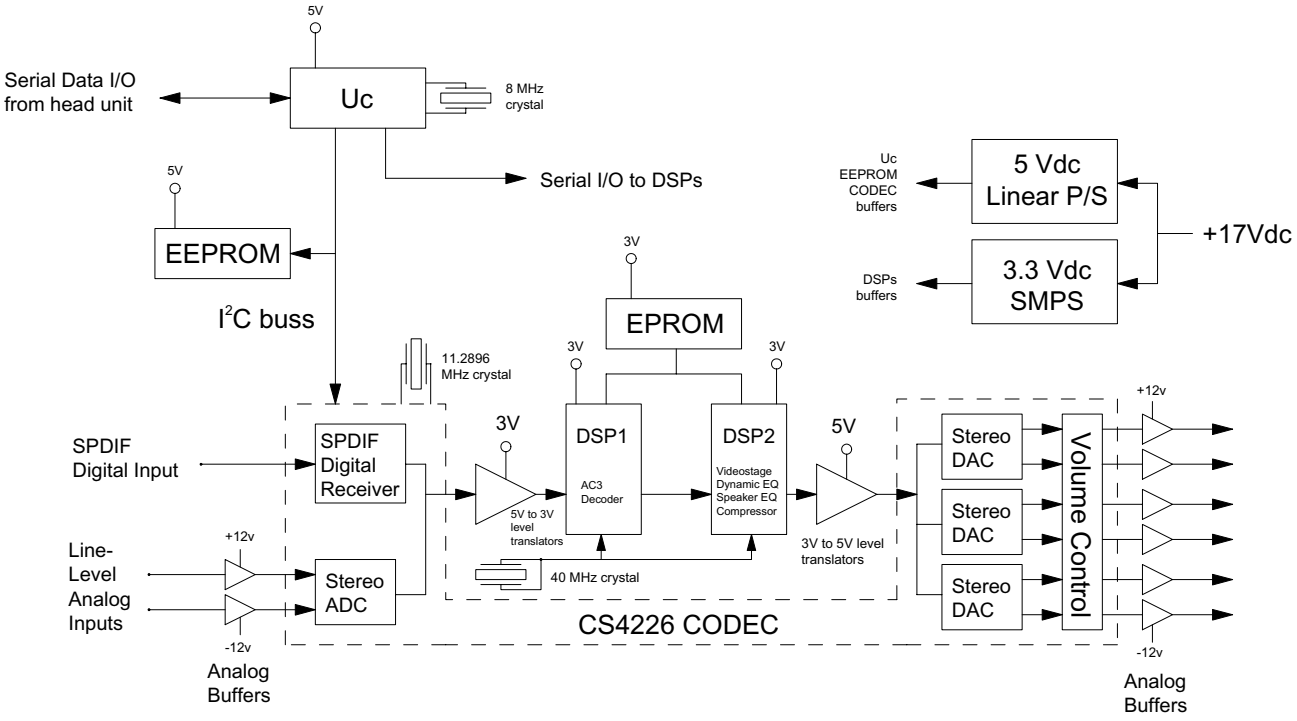


Figure 48. DSP PCB Basic Block Diagram

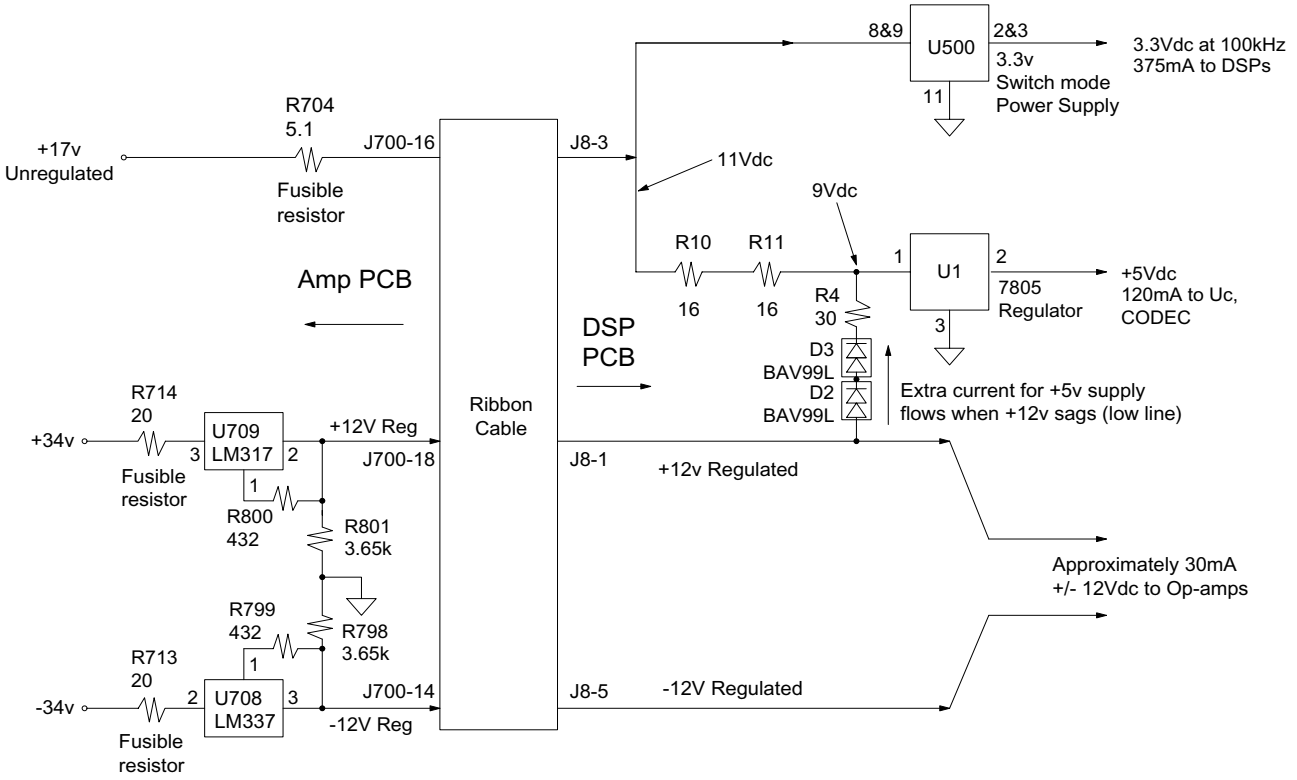


Figure 49. DC Power Supplies Simplified Schematic Diagram

Appendix

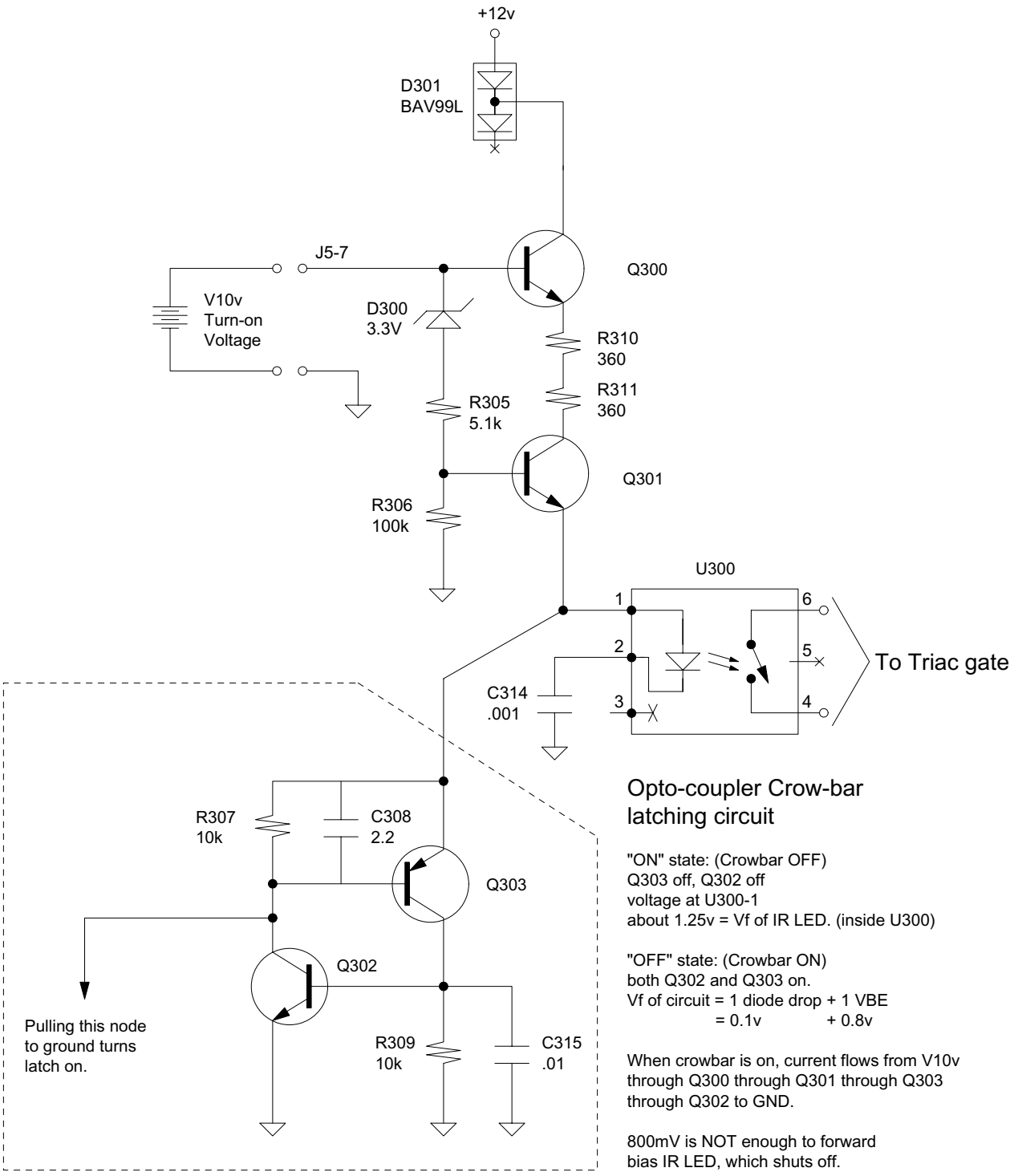


Figure 50. Protection Circuit Simplified Schematic Diagram

Appendix

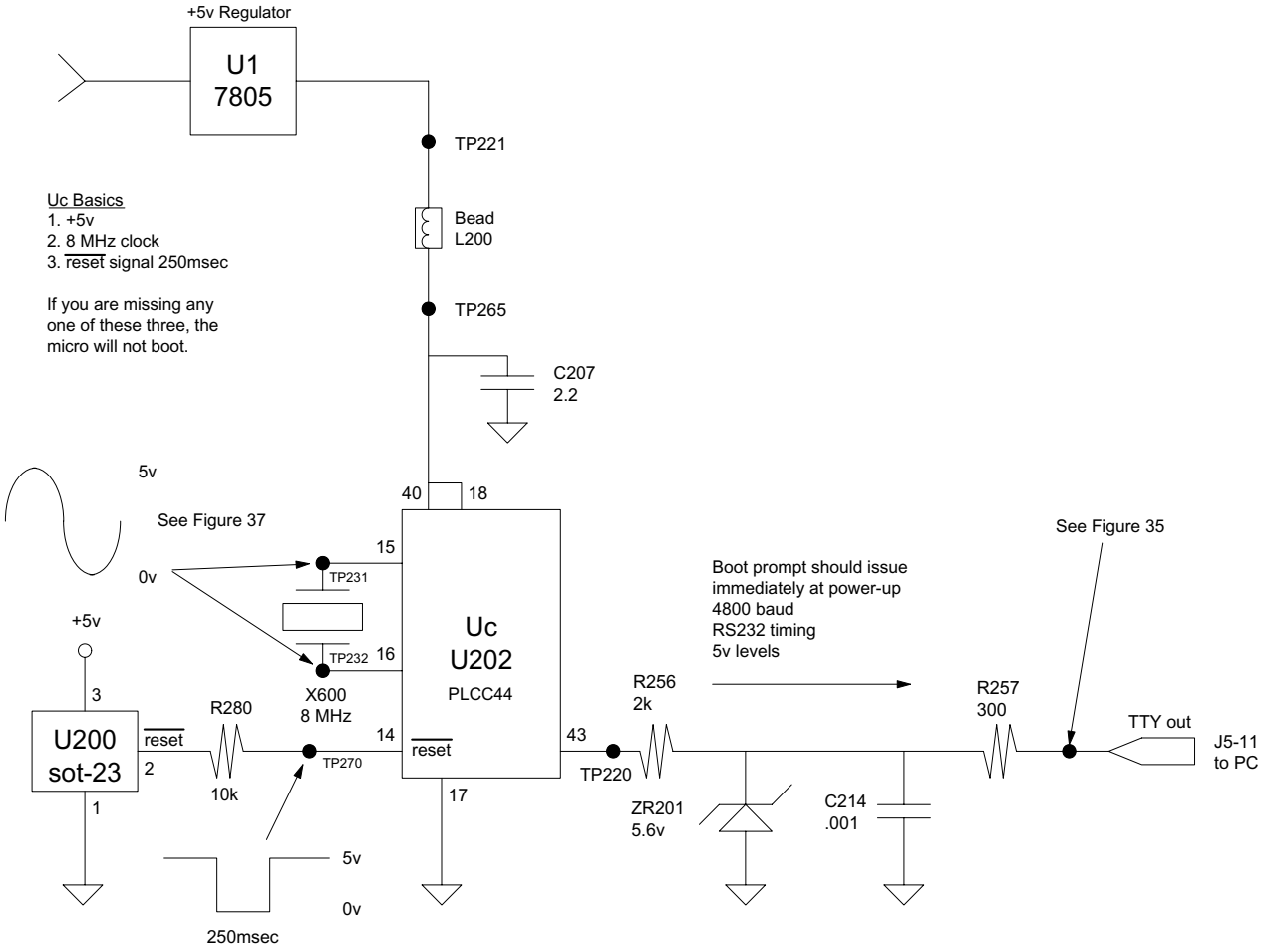


Figure 51. Microcontroller U202 Basic Block Diagram

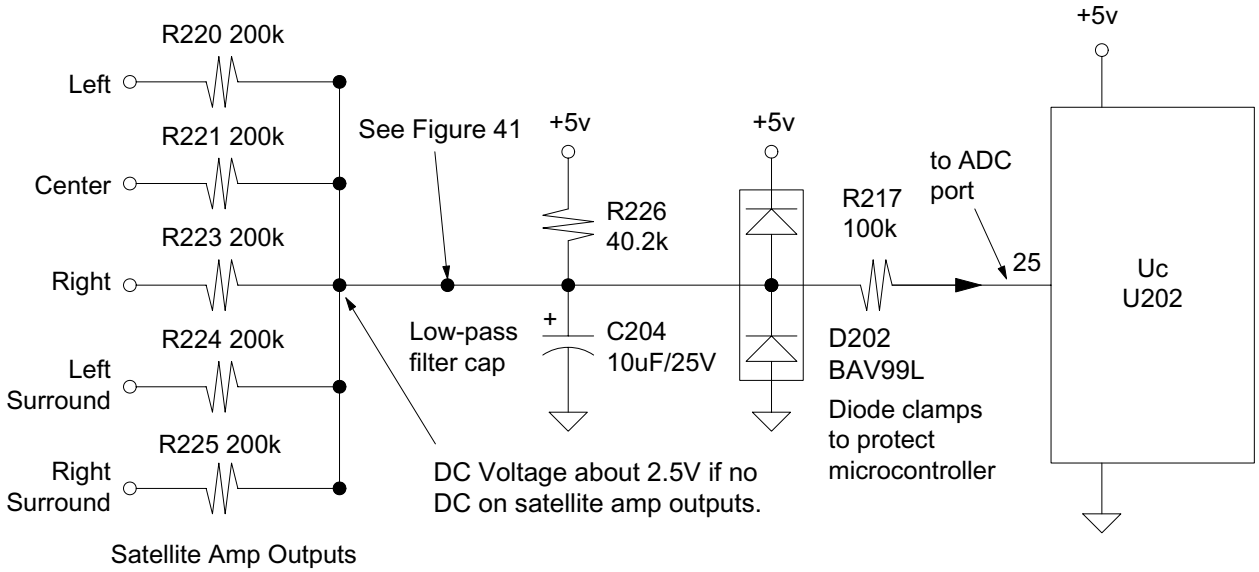


Figure 52. Satellite Amplifier DC Offset Detector Simplified Schematic Diagram

Appendix

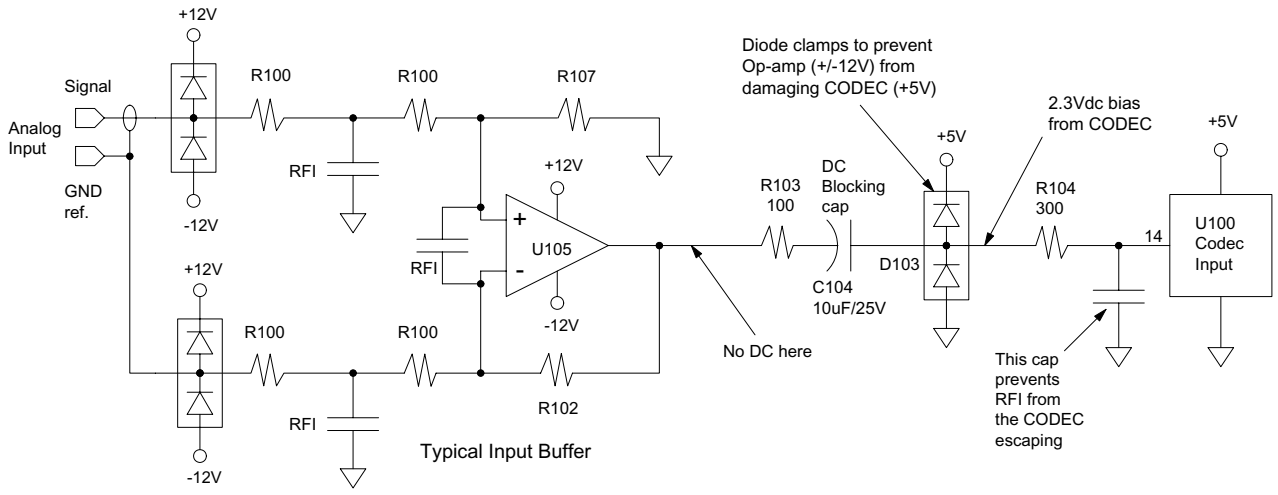


Figure 53. Analog Signal Path from Input Jacks to CODEC Simplified Schematic Diagram

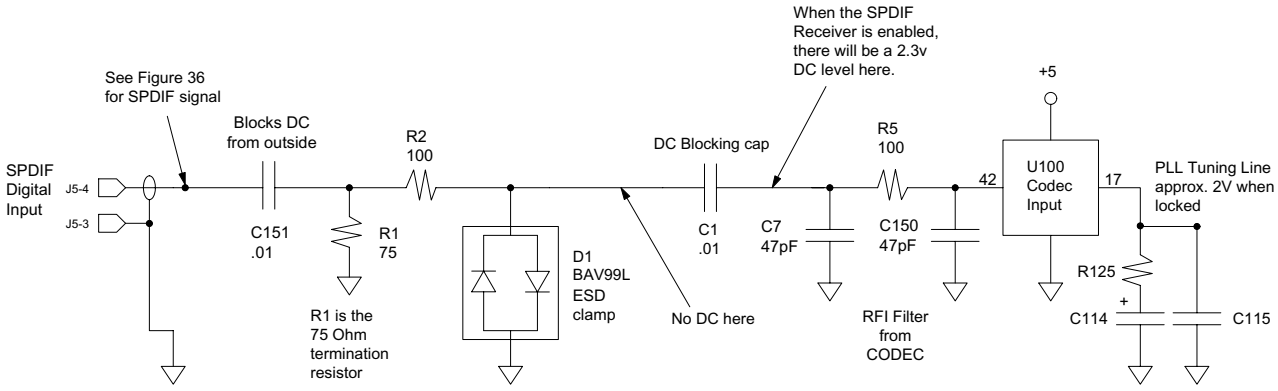


Figure 54. Digital Signal Path from Input Jack to CODEC Simplified Schematic Diagram

Appendix

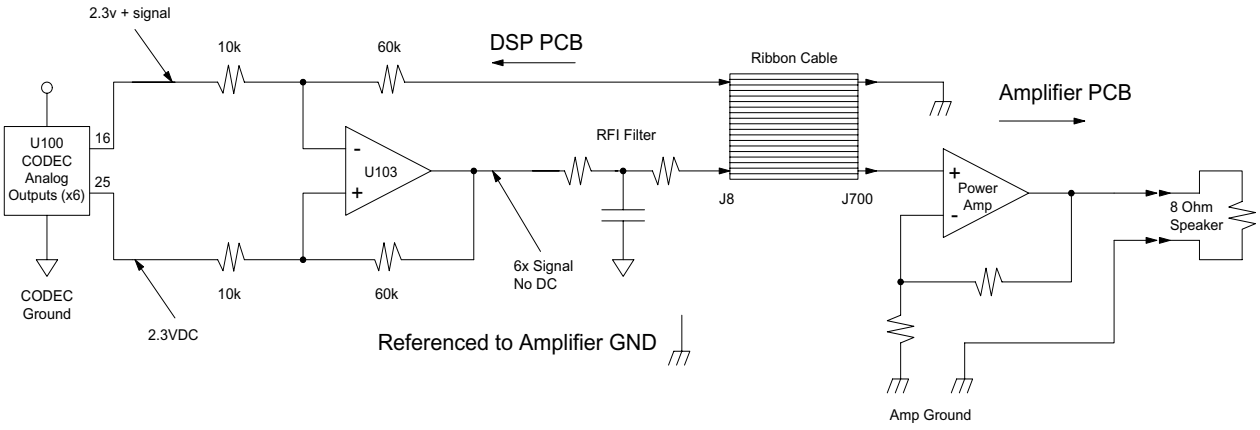
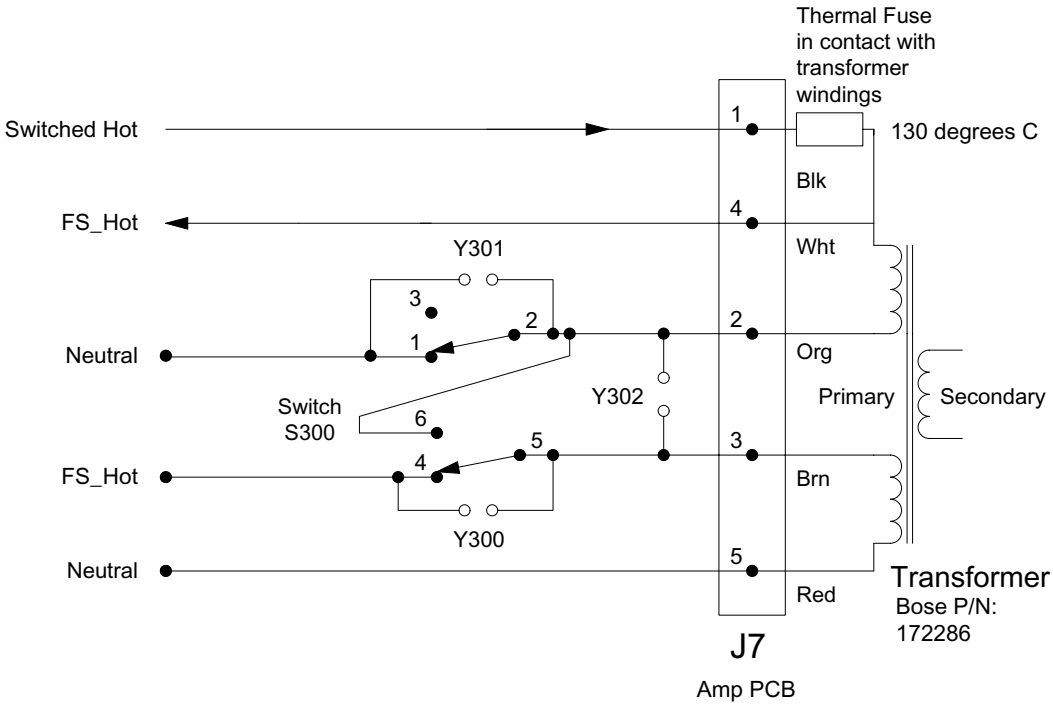
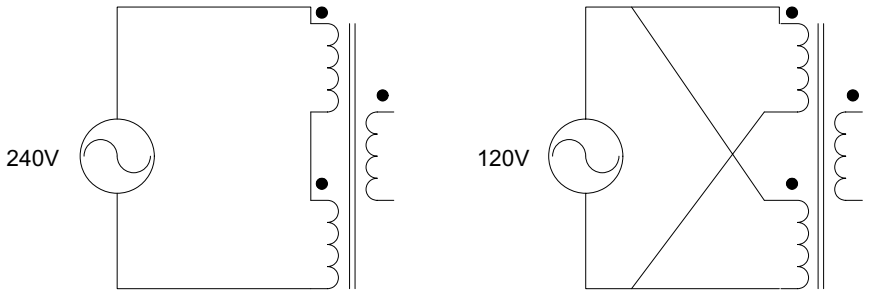


Figure 55. Analog Signal Path from CODEC to Satellite Simplified Schematic Diagram





Dual-Voltage Connections

Figure 56. Transformer Wiring Diagram

Appendix

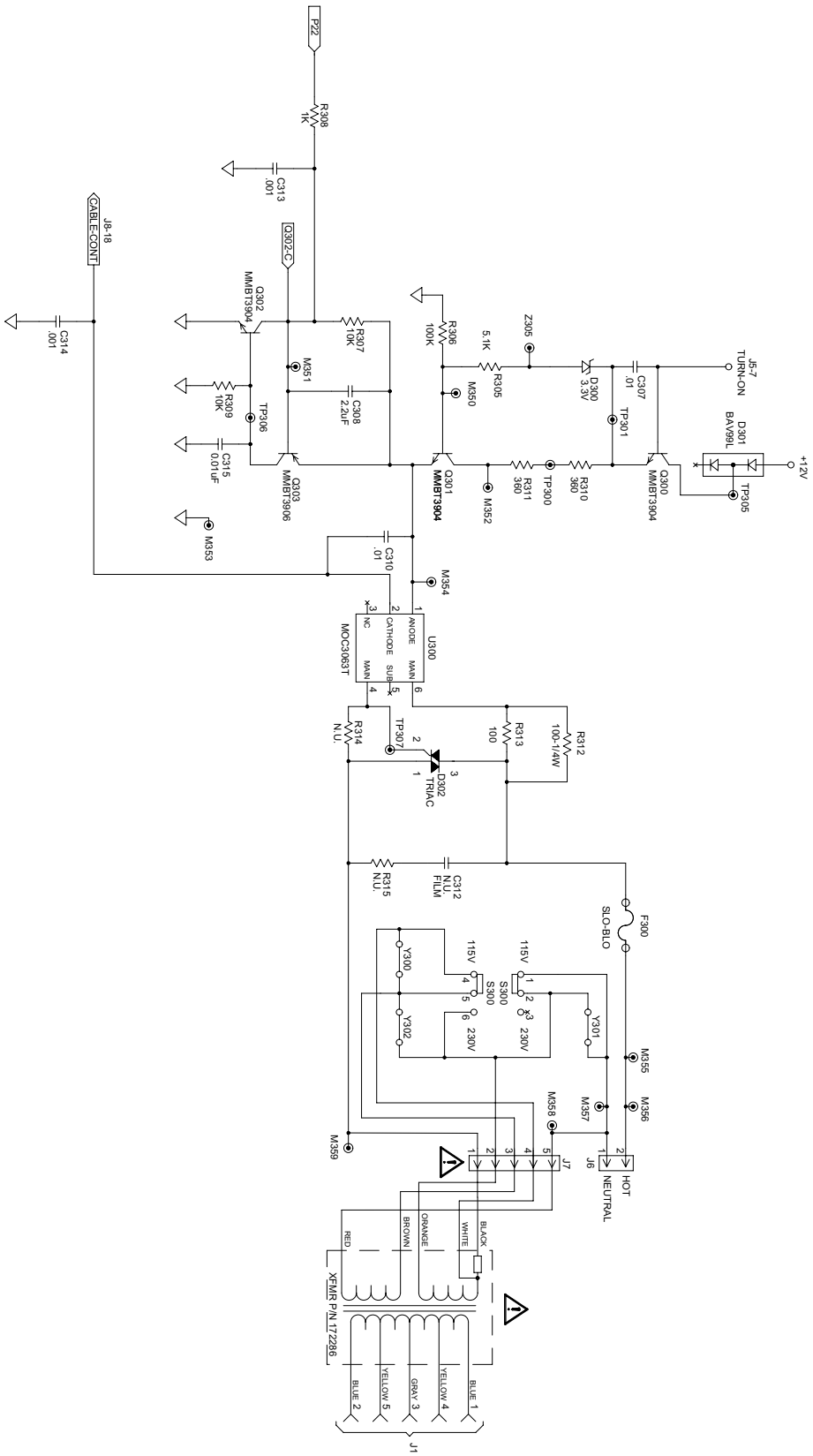


Figure 57. Digital Bass Module Overall Turn-on Circuit Schematic Diagram

Appendix

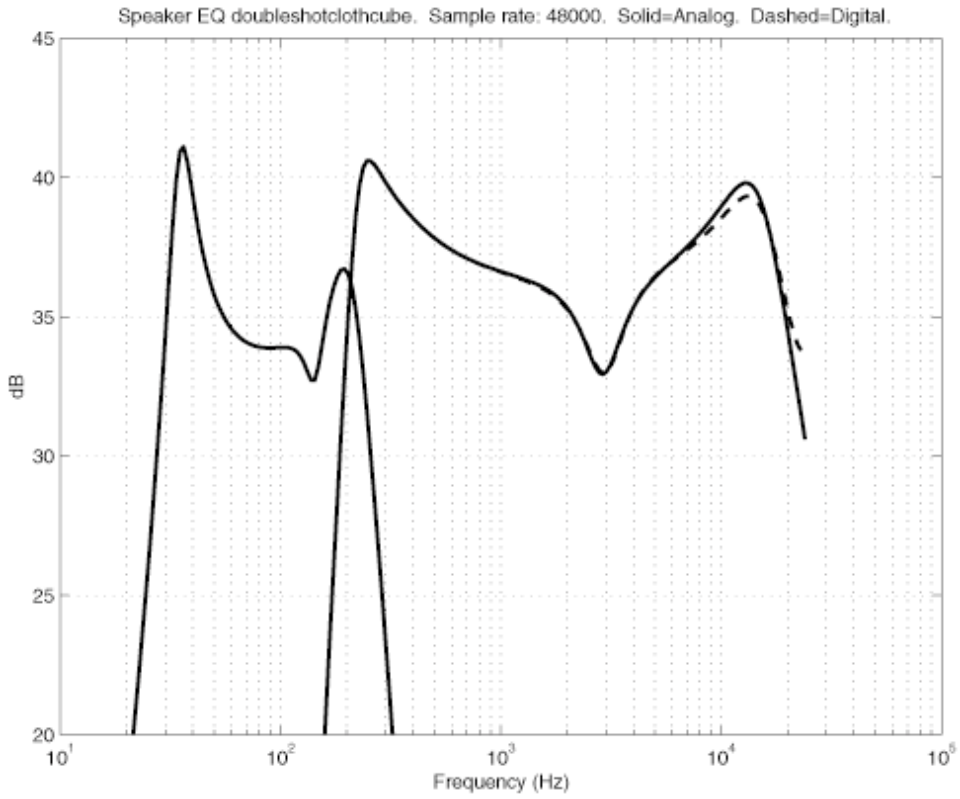


Figure 58. Lifestyle® 12 and 25 Series II Overall Frequency Response Curve

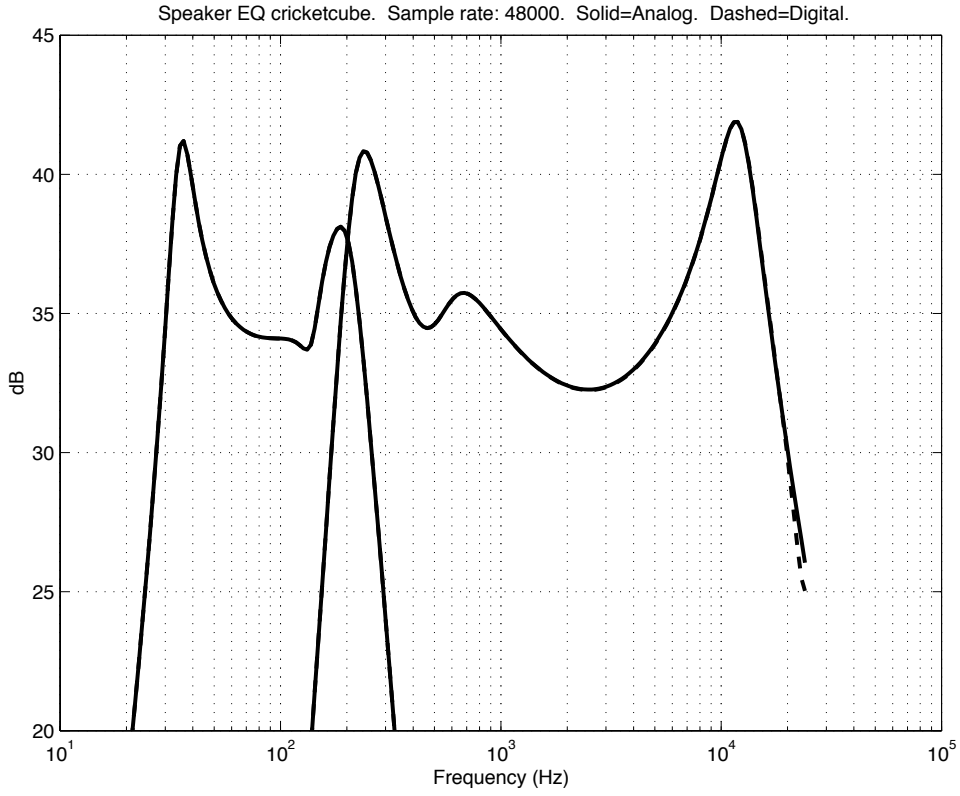


Figure 59. Lifestyle® 30 Series II Overall Frequency Response Curve

Appendix

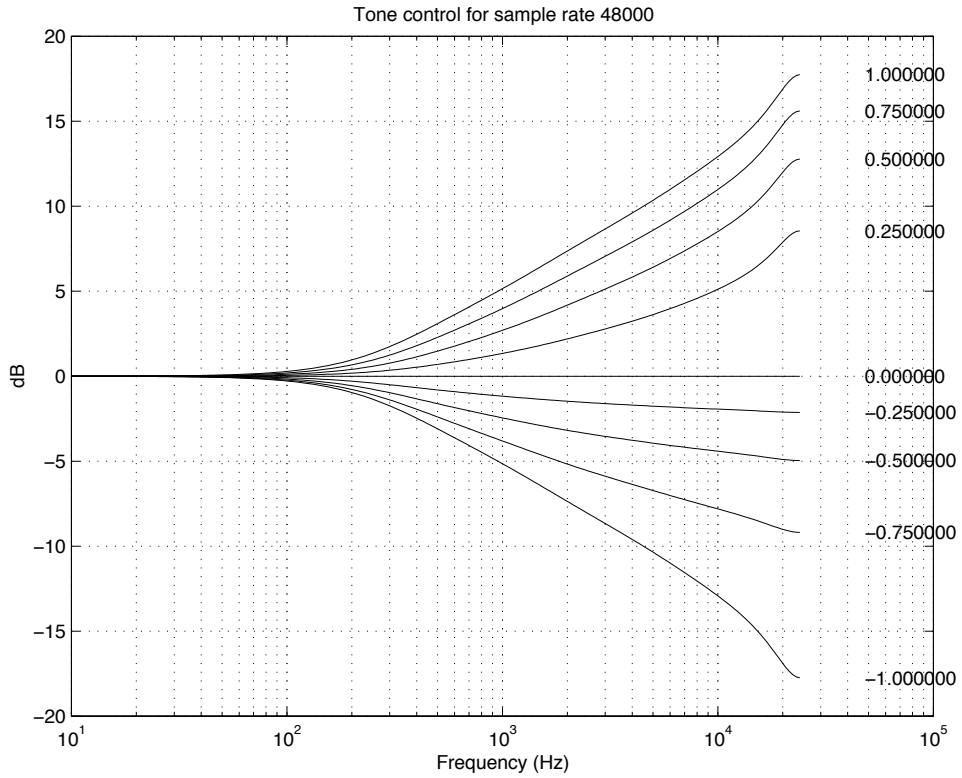


Figure 60. Lifestyle® Series II Tone Control Frequency Response Curve

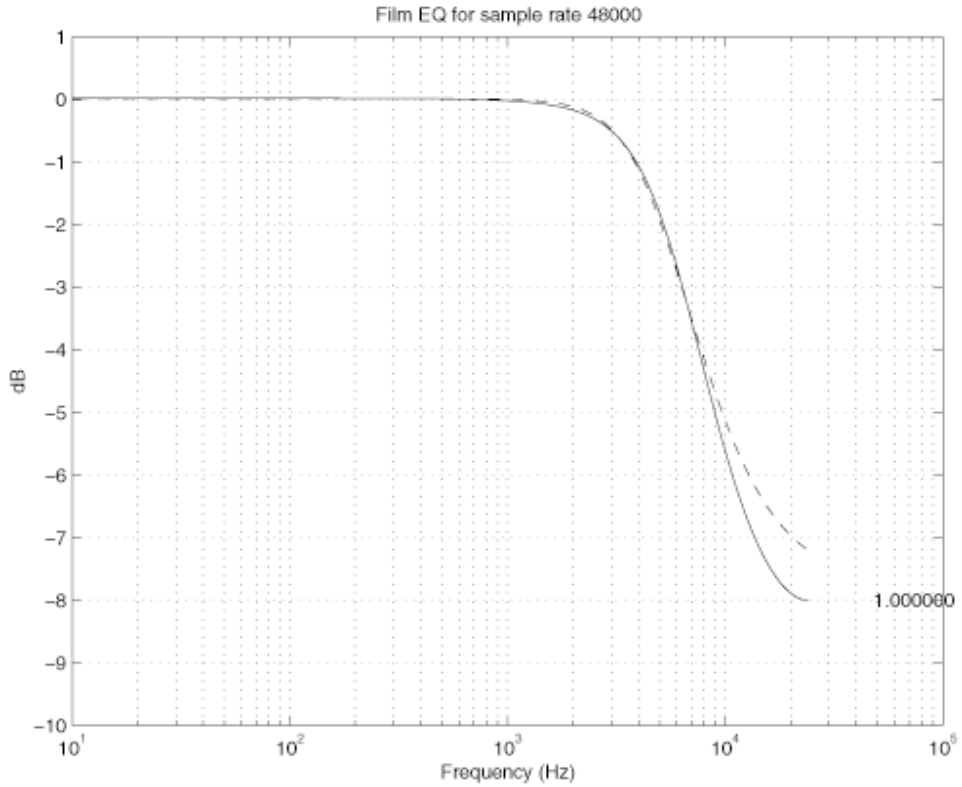


Figure 61. Lifestyle® Series II Film EQ Frequency Response Curve

Appendix

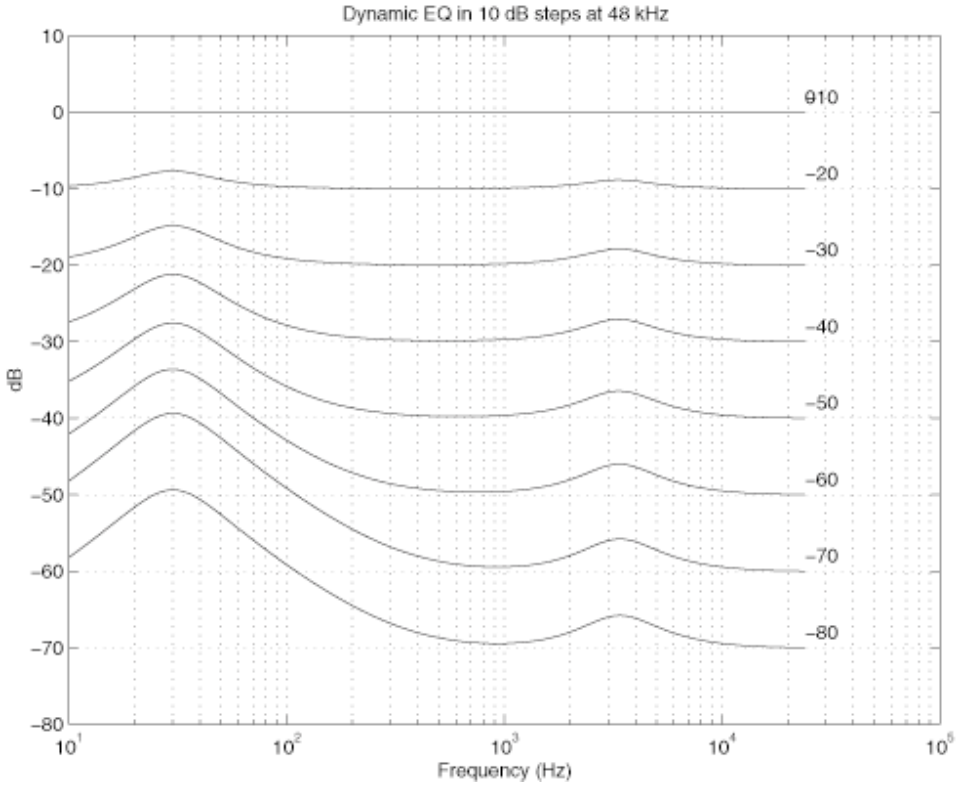


Figure 62. Lifestyle® Series II Dynamic EQ Frequency Response Curve

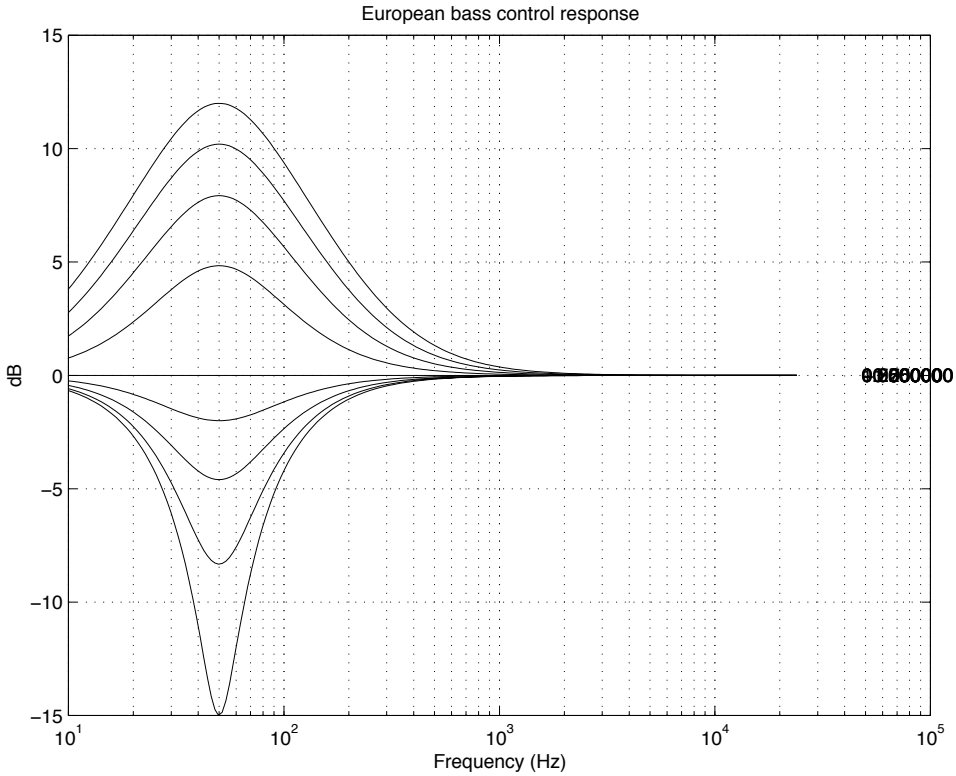


Figure 63. Lifestyle® Series II 240 Volt Bass Frequency Response Curve

Appendix

SPDIF

Sony/Philips Digital Interface Format (SPDIF). A common format for sending 24-bit, two channel digital audio down a single coax cable (or twisted pair, or optical fiber).

The SPDIF signal can also carry Dolby Digital data instead of a stereo signal. The Dolby Digital data is highly compressed, thus lowering the required bit rate for 5-channel surround, which is how a system designed to carry two-channel data can be used to carry more than two channel's of audio.

The SPDIF signal has the following characteristics:

The bit rate is 64 bits * 48,000 audio samples per second, or about 3 Mbits per second. This requires roughly 10 MHz of bandwidth. Cabling with a characteristic impedance of 75 Ohms is used to prevent ringing and reflections and from distorting the digital signal. The signal source has a source impedance of 75 Ohms and the cable is terminated at the bass box with a 75 Ohm load. It has generally the same cabling and termination requirements as a video signal.

Without a SPDIF receiver to extract the digital audio data, the SPDIF bit-stream, there's not much you can check with just an oscilloscope except for;
a) Bit times; 162 nsec or 325 nsec for 1's and 0's
b) Clean rising and falling edges
c) peak-peak voltage of about 500 mV into 75 Ohms

TTL to RS232 Converter

The serial port uses ±12V inverted logic where logical 0 = +12V and logical 1 = -12V. The bass box uses "TTL" logic where logical 0 = 0V and logical 1 = +5V. The B+B converter box simply inverts and level-shifts the data flowing both ways.

Full details of the converter are available at www.bb-elec.com. Search in the converters section for the Model 232TTL.

TAP Commands

TAP Command	Description
tv	print firmware revisions
vr	print uC checksum
rs	reset pcb
rc	reset DSPs
rd	reset codec
de	dump the contents of EEPROM
we xx,yy	write data "xx" (hex) to EEPROM address "yy" (hex)
ce 0	re-calculate and store EEPROM checksum
ef xx	fill EEPROM with data "xx" (hex)
sk 51,af,ff	select AUX input (digital)
sk 61,af,ff	select VID1 input (analog)

Appendix

TAP Commands (continued)

TAP Command	Description
ad x	print uC ADC port voltage, where "x" equals: 0 bass pot position 1 treble pot position 2 thermistor voltage 3 3.3V supply 4 SPDIF detect 5 codec reference voltage 6 twiddler DC offset 7 turn-on signal (result is 8-bit, 0 = 0V, FF = 5V)
sk 42,af,ff	select TAPE input (analog)
sk 31,1f,ff	volume up 1dB
sk 31,2f,ff	volume down 1dB
sk 31,1x,xf	set volume to -xx volume e.g., sk 31,10,0f 00dB sk 31,11,2f -12dB sk 31,13,4f -34dB
sk 31,9f,ff	center/surround volume up (3-speaker / 5-speaker)
sk 31,af,ff	center/surround volume down
sk 31,9x,xf	set center/surround volume e.g., sk 31,90,0f +7dB sk 31,90,1f +6dB sk 31,90,7f 0dB sk 31,91,4f -7dB sk 31,91,5f -8dB
sk 31,4f,ff	mute
sk 31,3f,ff	un-mute
sk 31,d0,2f	select 2-speaker mode
sk 31,d0,3f	select 3-speaker mode
sk 31,d0,4f	select 5-speaker mode
sk 3f,6f,ff	off
tn 3,0,0,0,0,0,0,0,0	passthrough, with all signal processing
tn 6,0,0,0,0,0,0,0,0	passthrough, with no signal processing
tn 0,0,0,0,0,0,0,0,0	exit test mode, restore normal signal processing
tn 4,0,0,0,0,0,0,0,0	request DSP checksum calculation
dp 10,0,2,0,12	fetch and print DSP checksum calculation
dp 10,0,0,0,0	peek at DSP 1 address 0
dp 20,0,0,0,0	peek at DSP 2 address 0
sk 31,ex,yf	x = 8 2-speaker x = 9 3-speaker x = A 5 speaker y = 4 single bits, as follows DRC off/on 1_to_5 off/on

Appendix

Hex Notation

Hex is an alphanumeric code representing a four bit binary number:

0000 = “0” = 0
0001 = “1” = 1
etc.
1001 = “9” = 9
1010 = “A” = 10
1011 = “B” = 11
1100 = “C” = 12
1101 = “D” = 13
1110 = “E” = 14
1111 = “F” = 15

Hex notation is in common use among people who deal with binary numbers a lot, e.g. assembly language programmers. There are a couple conventions for indicating that a text string is meant to be interpreted as a hex number. One way is to proceed the hex string with a ”0x”; another way is to add a ‘h” at the end. E.g. “0x0809” or “0809h” is definitely not the same numerical quantity as the decimal 809. It is easy for numbers to misinterpreted. On the other hand, “F3” is obviously a hex number.

So, 000E (hex) = 0000 0000 0000 1110 (16 bit binary) = 14 (decimal). The bass module has been powered off 15 times.

Note: The first number only increments when you issue an “off” command from the head unit. Pulling the plug and shutting off the bass box directly will not affect this number.

Firmware CHECKSUMS

uC (U202)

Bose® part number	Uc (U202) firmware rev.	CHECKSUM
250591	v. 14	0x17c896
251561	v. 20	0x17b2e0
251707	v. 22	0x17ae1e
251707	v. 23	0x17f409
252941	v. 28	0x1fcafa
254101	v. 30	0x18cc52

DSP (U400)

Bose part number	DSP (U400) firmware rev.	CHECKSUMS
250592	v. 14	0x24D3AAF (or 0x7EF7C2)
251560	v. 20	0x25DE79E (or 0x8FA4B1)
251708	v. 21	0x25E2C24
252942	v. 23	0x261EAA3
254102	v. 30	0x262D4D8

Appendix

Diagnostic voltages available at the uC ADC ports

uC (U202) ADC ports

TAP command	Description
"ad 0"	bass pot
"ad 1"	treble pot
"ad 2"	thermistor (see thermistor readings in appendix)
"ad 3"	3.3V
"ad 4"	SPDIF sense (< 1V = SPDIF, > 3V = no SPDIF)
"ad 5"	codec ref. voltage (2.3V)
"ad 6"	satellite offset (nominally 2.5V)
"ad 7"	10V turn-on

Two digit hex to voltage conversion

HEX	Decimal	U202 ADC port voltage
0	0	0.000V
1	1	0.020V
2	2	0.039V
3	3	0.059V
4	4	0.078V
5	5	0.098V
6	6	0.117V
7	7	0.137V
8	8	0.156V
9	9	0.176V
A	10	0.195V
B	11	0.215V
C	12	0.234V
D	13	0.254V
E	14	0.273V
F	15	0.293V
10	16	0.312V
11	17	0.332V
12	18	0.352V
13	19	0.371V
14	20	0.391V
15	21	0.410V
16	22	0.430V
17	23	0.449V
18	24	0.469V
19	25	0.488V
1A	26	0.508V
1B	27	0.527V

HEX	Decimal	U202 ADC port voltage
1C	28	0.547V
1D	29	0.566V
1E	30	0.586V
1F	31	0.605V
20	32	0.625V
21	33	0.645V
22	34	0.664V
23	35	0.684V
24	36	0.703V
25	37	0.723V
26	38	0.742V
27	39	0.762V
28	40	0.781V
29	41	0.801V
2A	42	0.820V
2B	43	0.840V
2C	44	0.859V
2D	45	0.879V
2E	46	0.898V
2F	47	0.918V
30	48	0.938V
31	49	0.957V
32	50	0.977V
33	51	0.996V
34	52	1.016V
35	53	1.035V
36	54	1.055V
37	55	1.074V

Appendix

Two digit hex to voltage conversion (continued)

HEX	Decimal	U202 ADC port voltage
38	56	1.094V
39	57	1.113V
3A	58	1.133V
3B	59	1.152V
3C	60	1.172V
3D	61	1.191V
3E	62	1.211V
3F	63	1.230V
40	64	1.250V
41	65	1.270V
42	66	1.289V
43	67	1.309V
44	68	1.328V
45	69	1.348V
46	70	1.367V
47	71	1.387V
48	72	1.406V
49	73	1.426V
4A	74	1.445V
4B	75	1.465V
4C	76	1.484V
4D	77	1.504V
4E	78	1.523V
4F	79	1.543V
50	80	1.562V
51	81	1.582V
52	82	1.602V
53	83	1.621V
54	84	1.641V
55	85	1.660V
56	86	1.680V
57	87	1.699V
58	88	1.719V
59	89	1.738V
5A	90	1.758V
5B	91	1.777V
5C	92	1.797V
5D	93	1.816V
5E	94	1.836V
5F	95	1.855V
60	96	1.875V
61	97	1.895V
62	98	1.914V
63	99	1.934V
64	100	1.953V

HEX	Decimal	U202 ADC port voltage
65	101	1.973V
66	102	1.992V
67	103	2.012V
68	104	2.031V
69	105	2.051V
6A	106	2.070V
6B	107	2.090V
6C	108	2.109V
6D	109	2.129V
6E	110	2.148V
6F	111	2.168V
70	112	2.188V
71	113	2.207V
72	114	2.227V
73	115	2.246V
74	116	2.266V
75	117	2.285V
76	118	2.305V
77	119	2.324V
78	120	2.344V
79	121	2.363V
7A	122	2.383V
7B	123	2.402V
7C	124	2.422V
7D	125	2.441V
7E	126	2.461V
7F	127	2.480V
80	128	2.500V
81	129	2.520V
82	130	2.539V
83	131	2.559V
84	132	2.578V
85	133	2.598V
86	134	2.617V
87	135	2.637V
88	136	2.656V
89	137	2.676V
8A	138	2.695V
8B	139	2.715V
8C	140	2.734V
8D	141	2.754V
8E	142	2.773V
8F	143	2.793V
90	144	2.812V
91	145	2.832V

Appendix

Two digit hex to voltage conversion (continued)

HEX	Decimal	U202 ADC port voltage
92	146	2.852V
93	147	2.871V
94	148	2.891V
95	149	2.910V
96	150	2.930V
97	151	2.949V
98	152	2.969V
99	153	2.988V
9A	154	3.008V
9B	155	3.027V
9C	156	3.047V
9D	157	3.066V
9E	158	3.086V
9F	159	3.105V
A0	160	3.125V
A1	161	3.145V
A2	162	3.164V
A3	163	3.184V
A4	164	3.203V
A5	165	3.223V
A6	166	3.242V
A7	167	3.262V
A8	168	3.281V
A9	169	3.301V
AA	170	3.320V
AB	171	3.340V
AC	172	3.359V
AD	173	3.379V
AE	174	3.398V
AF	175	3.418V
B0	176	3.438V
B1	177	3.457V
B2	178	3.477V
B3	179	3.496V
B4	180	3.516V
B5	181	3.535V
B6	182	3.555V
B7	183	3.574V
B8	184	3.594V
B9	185	3.613V
BA	186	3.633V
BB	187	3.652V
BC	188	3.672V
BD	189	3.691V
BE	190	3.711V

HEX	Decimal	U202 ADC port voltage
BF	191	3.730V
C0	192	3.750V
C1	193	3.770V
C2	194	3.789V
C3	195	3.809V
C4	196	3.828V
C5	197	3.848V
C6	198	3.867V
C7	199	3.887V
C8	200	3.906V
C9	201	3.926V
CA	202	3.945V
CB	203	3.965V
CC	204	3.984V
CD	205	4.004V
CE	206	4.023V
CF	207	4.043V
D0	208	4.062V
D1	209	4.082V
D2	210	4.102V
D3	211	4.121V
D4	212	4.141V
D5	213	4.160V
D6	214	4.180V
D7	215	4.199V
D8	216	4.219V
D9	217	4.238V
DA	218	4.258V
DB	219	4.277V
DC	220	4.297V
DD	221	4.316V
DE	222	4.336V
DF	223	4.355V
E0	224	4.375V
E1	225	4.395V
E2	226	4.414V
E3	227	4.434V
E4	228	4.453V
E5	229	4.473V
E6	230	4.492V
E7	231	4.512V
E8	232	4.531V
E9	233	4.551V
EA	234	4.570V
EB	235	4.590V

Appendix

Two digit hex to voltage conversion (continued)

HEX	Decimal	U202 ADC port voltage
EC	236	4.609V
ED	237	4.629V
EE	238	4.648V
EF	239	4.668V
F0	240	4.688V
F1	241	4.707V
F2	242	4.727V
F3	243	4.746V
F4	244	4.766V
F5	245	4.785V
F6	246	4.805V
F7	247	4.824V
F8	248	4.844V
F9	249	4.863V
FA	250	4.883V
FB	251	4.902V
FC	252	4.922V
FD	253	4.941V
FE	254	4.961V
FF	255	4.980V

Thermistor readings (TAP command "ad2")

Temperature	Decimal	Hex (code out)	Temperature	Decimal	Hex (code out)
0 C	249.0	0xF9	21 C	207.0	0xCF
1 C	247.0	0xF7	22 C	205.0	0xCD
2 C	245.0	0xF5	23 C	203.0	0xCB
3 C	243.0	0xF3	24 C	201.0	0xC9
4 C	241.0	0xF1	25 C	199.0	0xC7
5 C	239.0	0xEF	26 C	197.0	0xC5
6 C	237.0	0xED	27 C	195.0	0xC3
7 C	235.0	0xEB	28 C	193.0	0xC1
8 C	233.0	0xE9	29 C	191.0	0xBF
9 C	231.0	0xE7	30 C	189.0	0xBD
10 C	229.0	0xE5	31 C	187.0	0xBB
11 C	227.0	0xE3	32 C	185.0	0xB9
12 C	225.0	0xE1	33 C	183.0	0xB7
13 C	223.0	0xDF	34 C	181.0	0xB5
14 C	221.0	0xDD	35 C	179.0	0xB3
15 C	219.0	0xDB	36 C	177.0	0xB1
16 C	217.0	0xD9	37 C	175.0	0xAF
17 C	215.0	0xD7	38 C	173.0	0xAD
18 C	213.0	0xD5	39 C	171.0	0xAB
19 C	211.0	0xD3	40 C	169.0	0xA9
20 C	209.0	0xD1	41 C	167.0	0xA7

Appendix

Thermistor readings (TAP command "ad2")

Temperature	Decimal	Hex (code out)
42 C	165.0	0xA5
43 C	163.0	0xA3
44 C	161.0	0xA1
45 C	159.0	0x9F
46 C	157.0	0x9D
47 C	155.0	0x9B
48 C	153.0	0x99
49 C	151.0	0x97
50 C	149.0	0x95
51 C	147.0	0x93
52 C	145.0	0x91
53 C	143.0	0x8F
54 C	141.0	0x8D
55 C	139.0	0x8B
56 C	137.0	0x89
57 C	135.0	0x87
58 C	133.0	0x85
59 C	131.0	0x83
60 C	129.0	0x81
61 C	127.0	0x7F
62 C	125.0	0x7D
63 C	123.0	0x7B
64 C	121.0	0x79
65 C	119.0	0x77
66 C	117.0	0x75
67 C	115.0	0x73
68 C	113.0	0x71
69 C	111.0	0x6F
70 C	109.0	0x6D
71 C	107.0	0x6B
72 C	105.0	0x69
73 C	103.0	0x67
74 C	101.0	0x65
75 C	99.0	0x63
76 C	97.0	0x61
77 C	95.0	0x5F
78 C	93.0	0x5D
79 C	91.0	0x5B
80 C	89.0	0x59
81 C	87.0	0x57
82 C	85.0	0x55
83 C	83.0	0x53
84 C	81.0	0x51
85 C	79.0	0x4F
86 C	77.0	0x4D
87 C	75.0	0x4B
88 C	73.0	0x49

Temperature	Decimal	Hex (code out)
89 C	71.0	0x47
90 C	69.0	0x45
91 C	67.0	0x43
92 C	65.0	0x41
93 C	63.0	0x3F
94 C	61.0	0x3D
95 C	59.0	0x3B
96 C	57.0	0x39
97 C	55.0	0x37
98 C	53.0	0x35
99 C	51.0	0x33
100 C	49.0	0x31

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