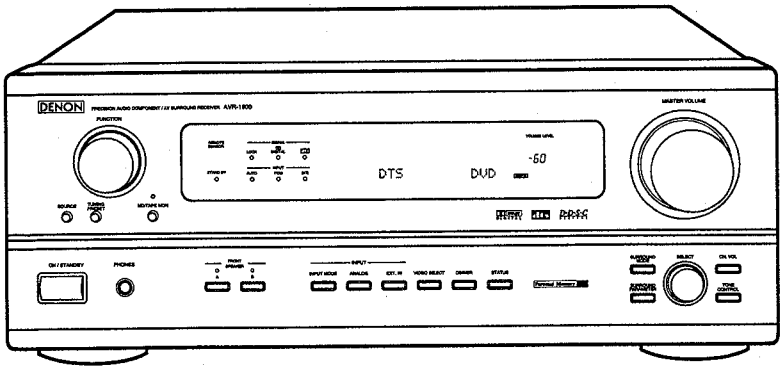
DENON

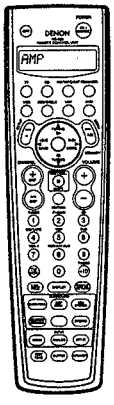
Hi-Fi Component

SERVICE MANUAL

MODEL AVR-1800/87

AV SURROUND RECEIVER





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● **Some illustrations using in this service manual are slightly different from the actual set.**

NIPPON COLUMBIA CO., LTD.

SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Before returning the unit to the customer, make sure you make either (1) a leakage current check or (2) a line to chassis resistance check. If the leakage current exceeds 0.5 milliamps, or if the resistance from chassis to either side of the power cord is less than 460 kohms, the unit is defective.

SPECIFICATIONS

AUDIO SECTION

(Power Amplifier)

Rated output:	Stereo (2ch driven):		
(All properties shown are only for the power amplifier stage.)	75 W + 75 W	(8 Ω/ohms, 20 Hz ~ 20 kHz with 0.05 % T.H.D.)	
	110 W + 110 W	(6 Ω/ohms, 1 kHz with 0.7 % T.H.D.)	
Dynamic power:	100 W × 2 ch (8 Ω/ohms)		
	145 W × 2 ch (4 Ω/ohms)		
	170 W × 2 ch (2 Ω/ohms)		
Output terminals:	Surround/Center:	6 ~ 16 Ω/ohms	
	Front: A or B	6 ~ 16 Ω/ohms	
	A + B	8 ~ 16 Ω/ohms	

(Analog)

Input sensitivity/input impedance:	200 mV/47 kΩ/kohms
Frequency response:	10 Hz ~ 50 kHz: +0, –3 dB
S/N:	102 dB
Distortion:	0.01 % (20 Hz ~ 20 kHz)
Rated output/maximum output:	1.2 V/7 V

(Digital)

D/A output:	Rated output – 2 V (at 0 dB playback) Total harmonic distortion - 0.008% (1 kHz, at 0 dB) S/N ratio – 102 dB Dynamic range - 96 dB
Digital input:	Format – Digital audio interface

(Phono equalizer (PHONO input-REC OUT))

Input sensitivity:	2.5 mV
RIAA deviation:	±1 dB (20 Hz to 20 kHz)
Signal-to-noise ratio:	74 dB (A weighting, with 5 mV input)
Rated output/Maximum output:	150 mV/7 V
Distortion factor:	0.03% (1 kHz, 3 V)

VIDEO SECTION

(Standard Video Jacks)

Input/output level and impedance:	1 Vp-p, 75 Ω/ohms
Frequency response:	5 Hz ~ 10 MHz – +0, –3 dB

TUNER SECTION

	[FM] (Note: µV at 75 Ω/ohms, 0 dBf = 1 × 10^{-15} W)	[AM]
Receiving range:	87.50 MHz ~ 107.90 MHz (for North America model) 87.50 MHz ~ 108.00 MHz (for Europe, China, Hong Kong, Taiwan R.O.C. and Multiple voltage models)	520 kHz ~ 1710 kHz (for North America model) 522 kHz ~ 1611 kHz (for Europe, China, Hong Kong, Taiwan R.O.C. and Multiple voltage models)
Usable sensitivity:	1.0 µV (11.2 dBf)	18 µV
50 dB quieting sensitivity:	MONO 1.6 µV (15.3 dBf) STEREO 23 µV (38.5 dBf)	
S/N ratio:	MONO 80 dB STEREO 75 dB	
Total harmonic distortion (at 1 kHz):	MONO 0.15 % STEREO 0.3 %	

GENERAL

Power supply:	AC120 V, 60 Hz (for North America and Taiwan R.O.C. models) AC230 V, 50 Hz (for Europe model) AC220 V, 50 Hz (for China model) AC115/230 V, 50/60 Hz (for Hong Kong and Multiple voltage models)
Power consumption:	4.5 A (for North America model) 270 W (for Europe, China, Hong Kong, Taiwan R.O.C. and Multiple voltage models)
Maximum external dimensions:	434 (W) × 171 (H) × 416 (D) mm (17-3/32″ × 6-47/64″ × 16-3/8″)
Weight:	11.4 kg (25 lbs. 2 oz.)

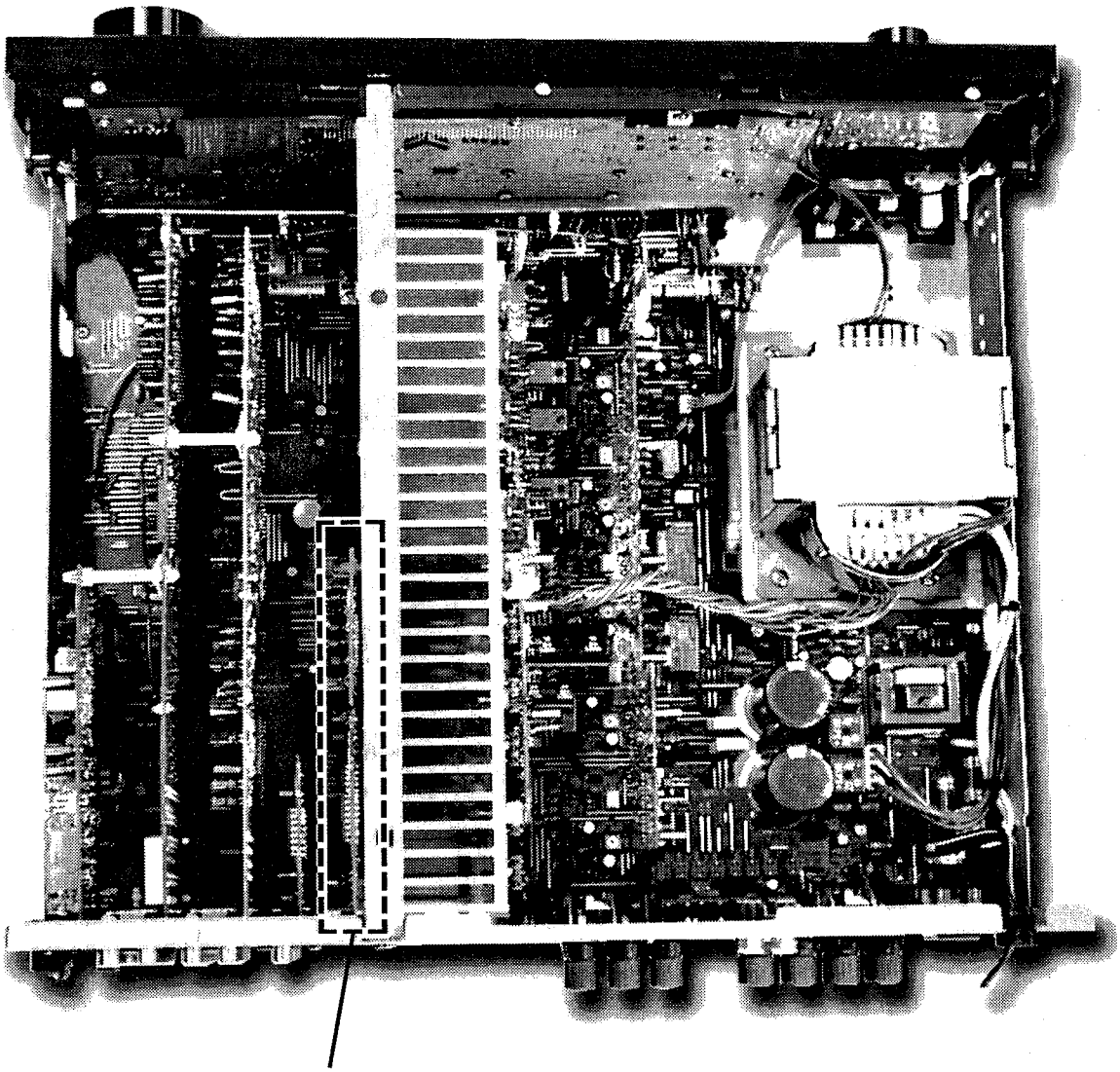
REMOTE CONTROL UNIT (RC-863: for North America, China, Hong Kong, Taiwan R.O.C. and Multiple voltage models) (RC-868: for Europe model)

Batteries:	R6P/AA Type (three batteries)
External dimensions:	61 (W) × 230 (H) × 34 (D) mm (2-13/32″× 9-1/16″ × 1-11/32″)
Weight:	200 g (Approx. 7 oz.) (including batteries)

WIRE ARRANGEMENT

If wire bundles are untied or moved to perform adjustment or parts replacement etc.,be sure to rearrange them neatly as they were originally bundled or placed afterward.
Otherwise, incorrect arrangement can be a cause of noise generation.

Wire arrangement viewed from the top

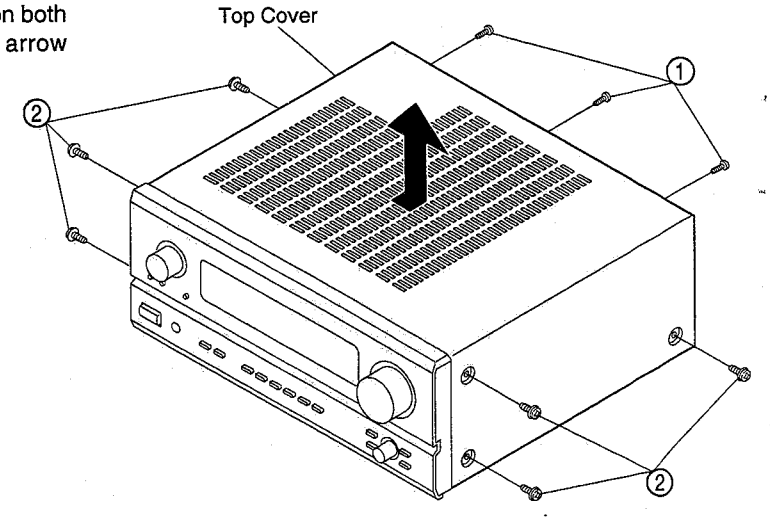


DISASSEMBLY

(Follow the procedure below in reverse order when reassembling)

1. Top Cover

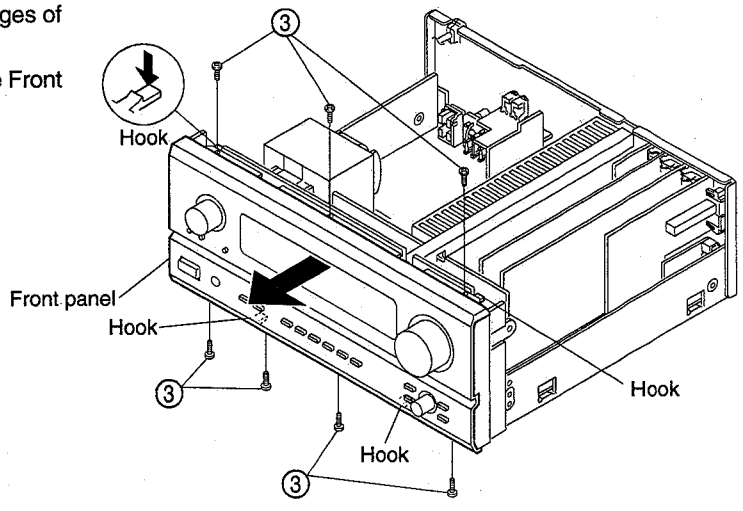
Remove 3 screws ① on the rear and 6 screws ② on both sides to detach the Top Cover as shown in the arrow direction.



2. Front Panel

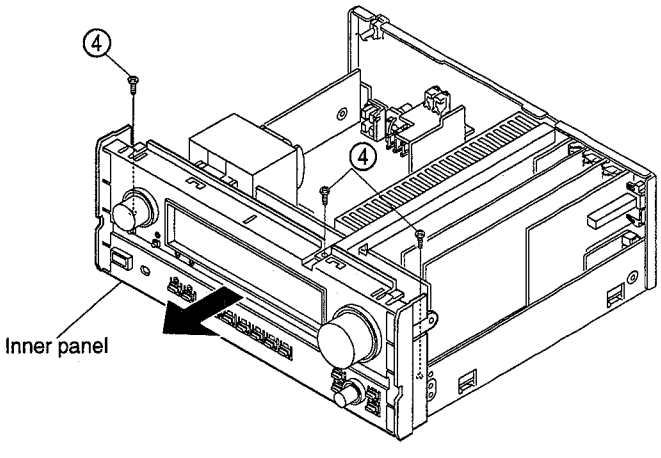
(1) Remove 7 screws ③ from the top and bottom edges of the Front Panel.

(2) Release 4 top and bottom hooks, then detach the Front Panel as shown in the arrow direction.



3. Inner Panel

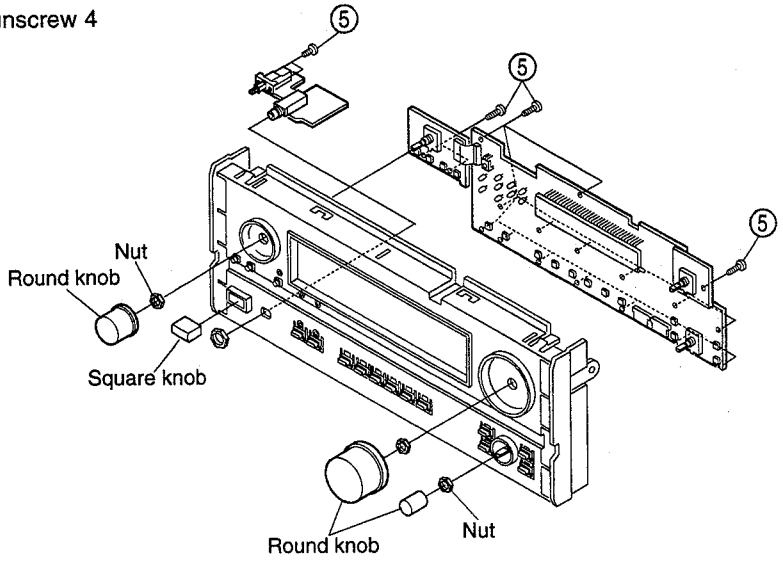
Pull out the Inner Panel in the arrow direction after removing 3 screws ④.



4. Inner Panel Ass'y

(1) Remove 3 round and 1 square knobs, and unscrew 4 nuts.

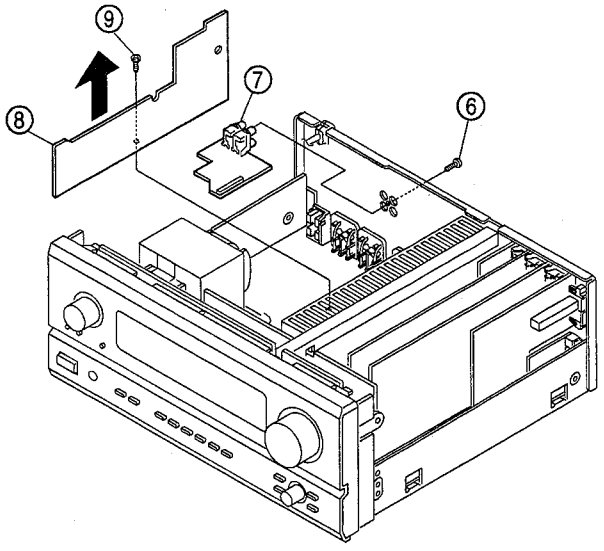
(2) Remove 19 screws ⑤ fixing each P.W.B.



5. Amp Unit

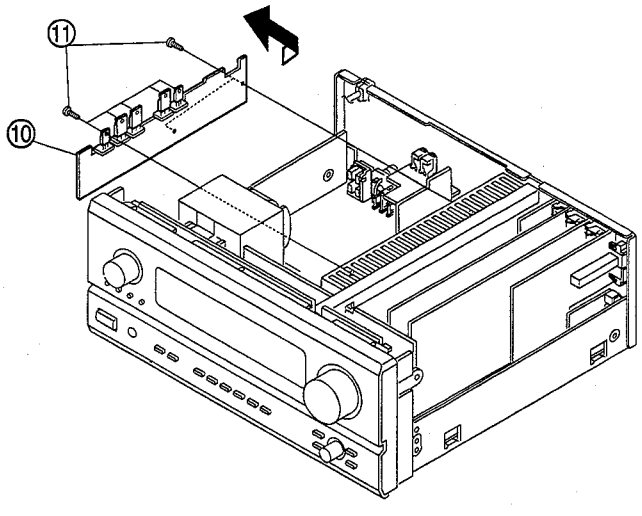
(1) Remove 1 screw ⑥ to detach Pre-out Unit ⑦.

(2) Take off the Amp Unit ⑧ as shown in the arrow direction after removing 1 screw ⑨.



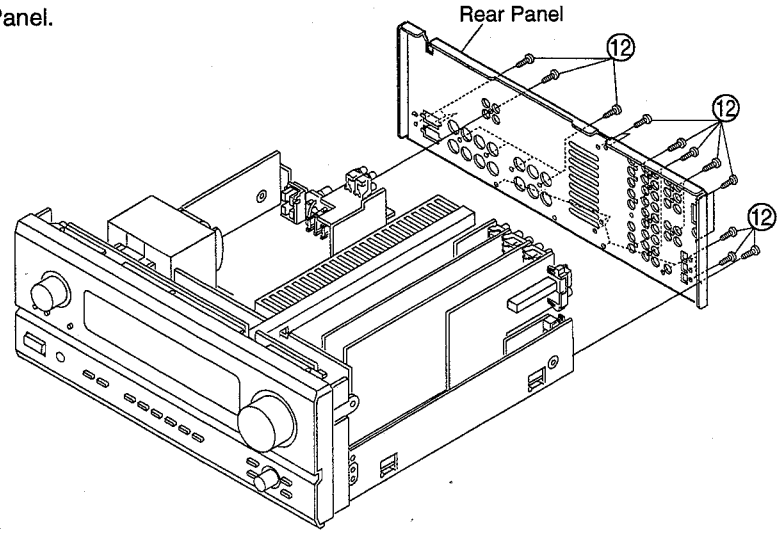
6. Regulator Unit

Take off the Regulator Unit ⑩ as shown in the arrow direction after removing 8 screws ⑪.



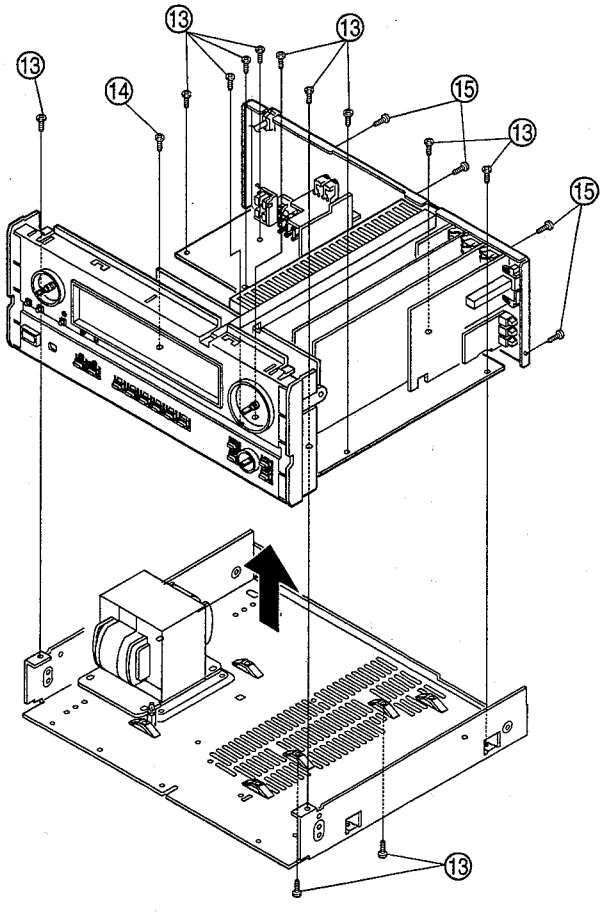
7. S-Video / C-video / Audio-in & DSP / Ext-in & VR / Digital-in / Tuner Unit

(1) Remove 32 screws ⑫ to detach the Rear Panel.
(2) Take off the objective P.W.B. upward.



8. How to Check Power Amp / μ-com Unit with Power-on

(1) Remove 12 screws ⑬, 1 screw ⑭, and 4 screws ⑮ fixing to the Chassis.
(2) Pull up the Unit to separate from the Chassis.

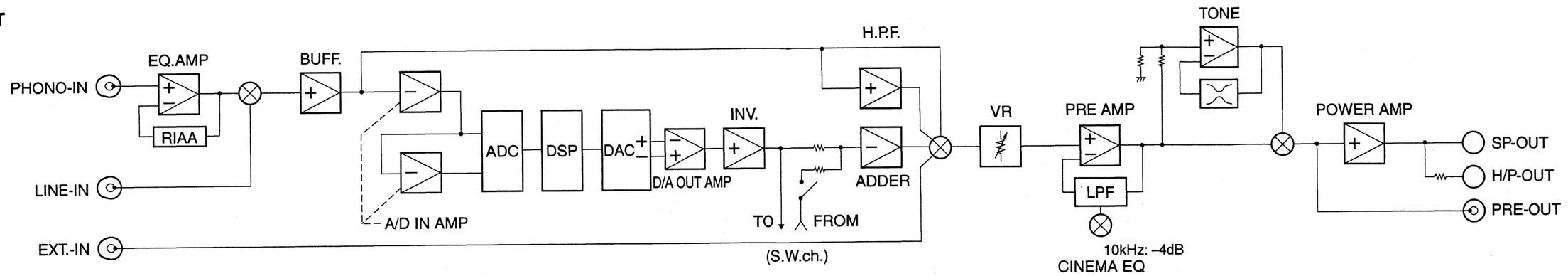


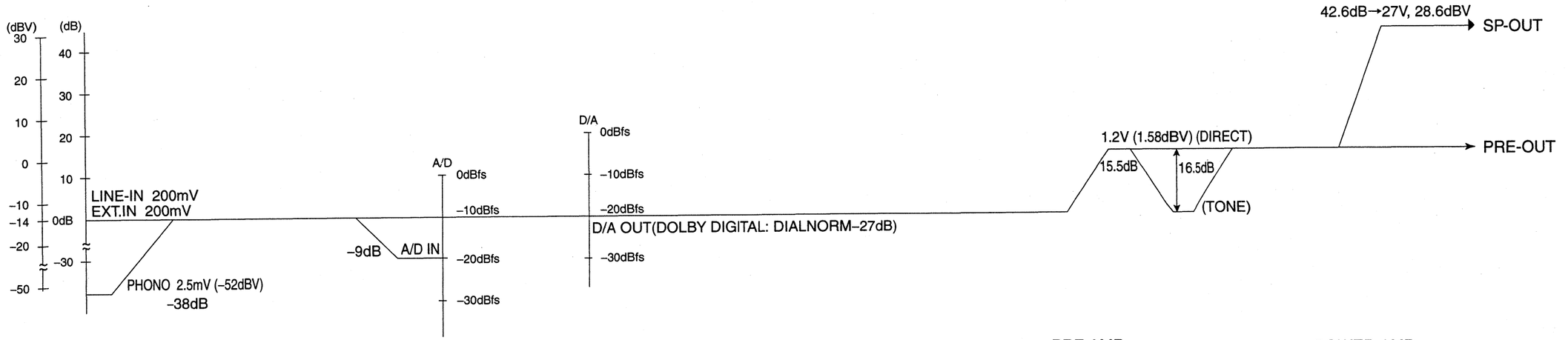
LEVEL DIAGRAM

1 2 3 4 5 6 7 8

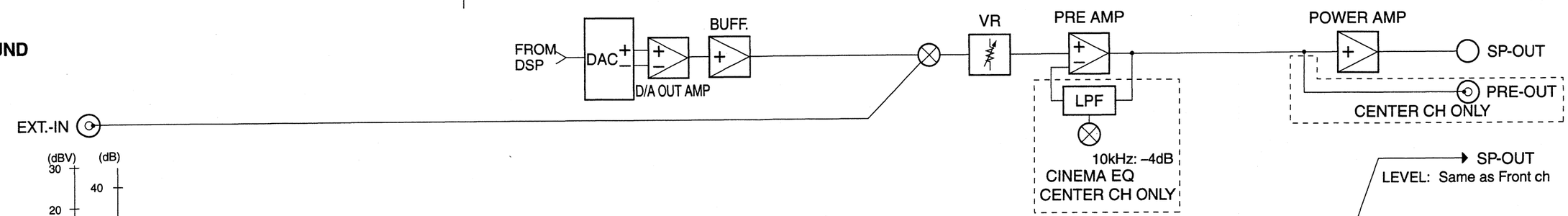
A B C D E

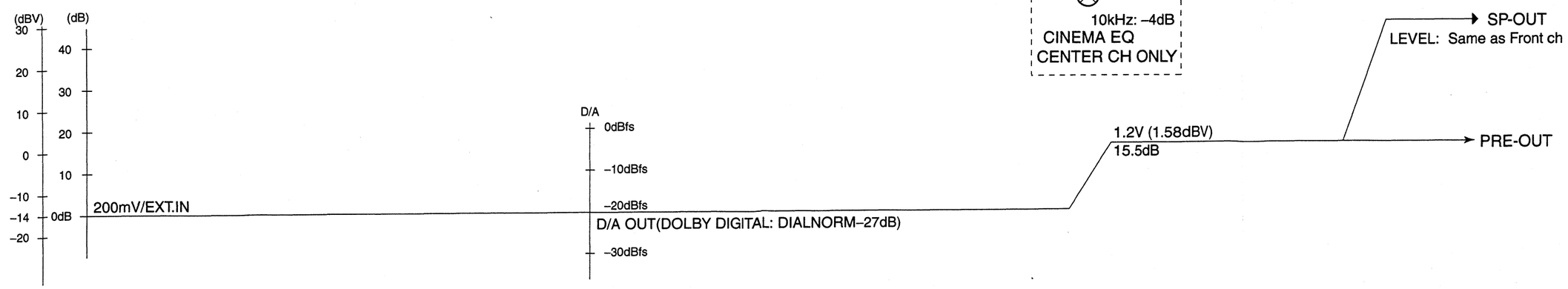
FRONT

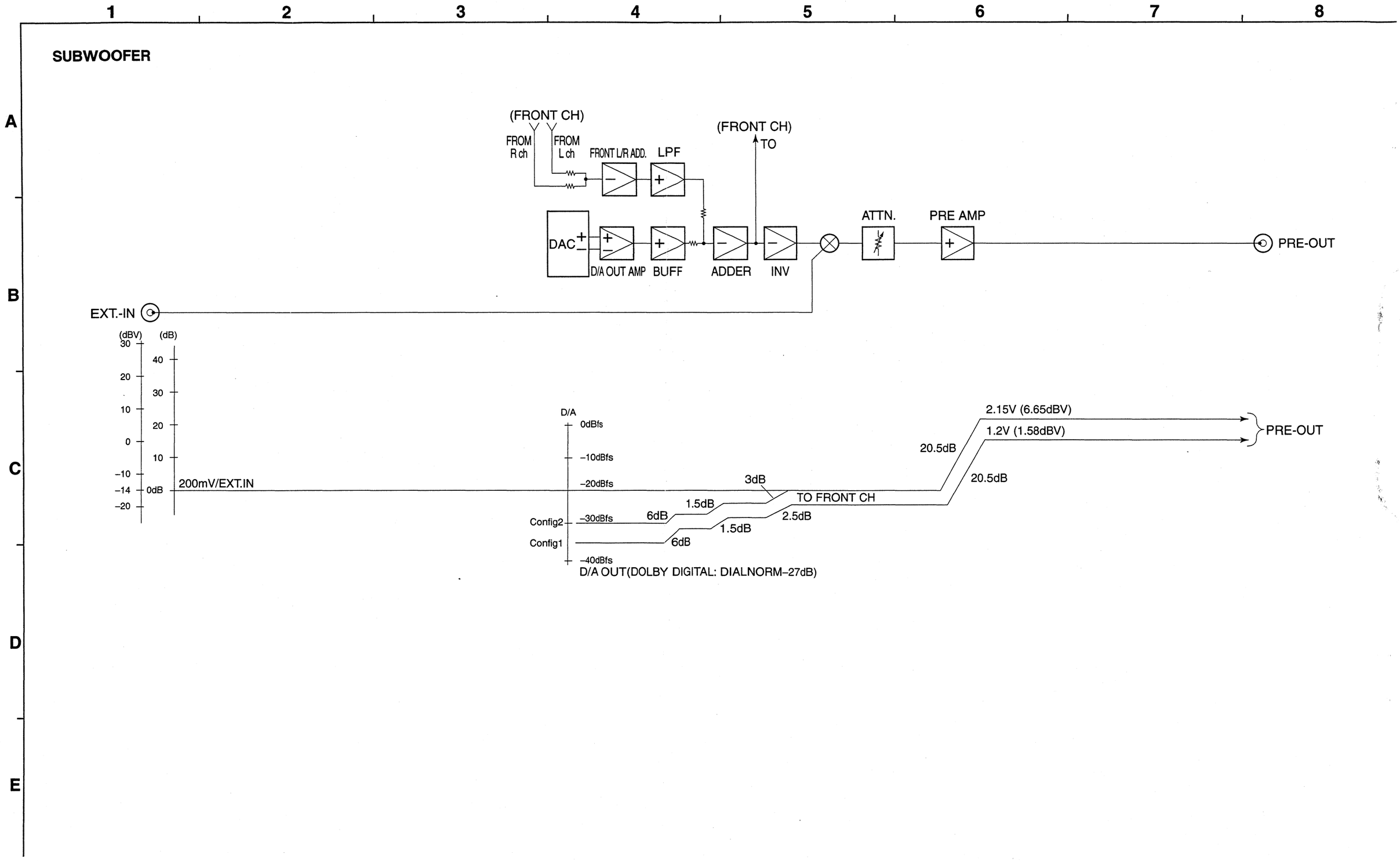




CENTER SURROUND

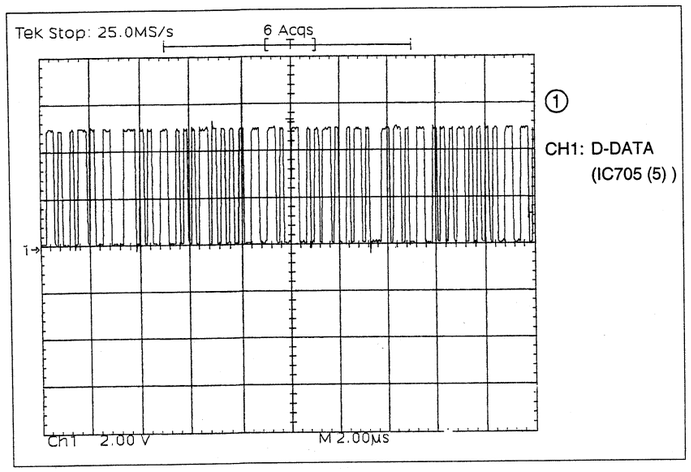


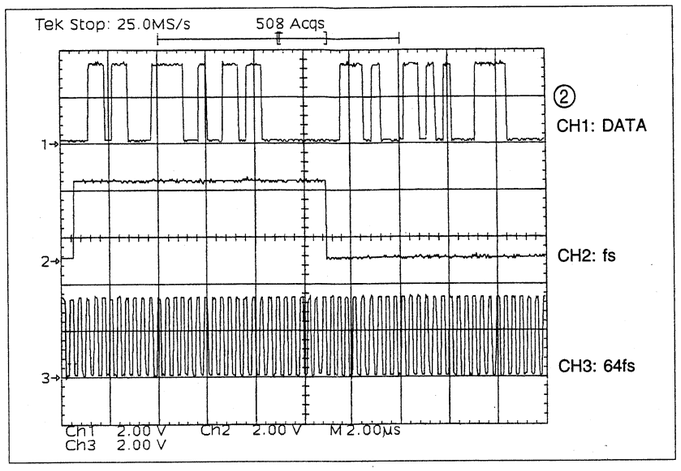


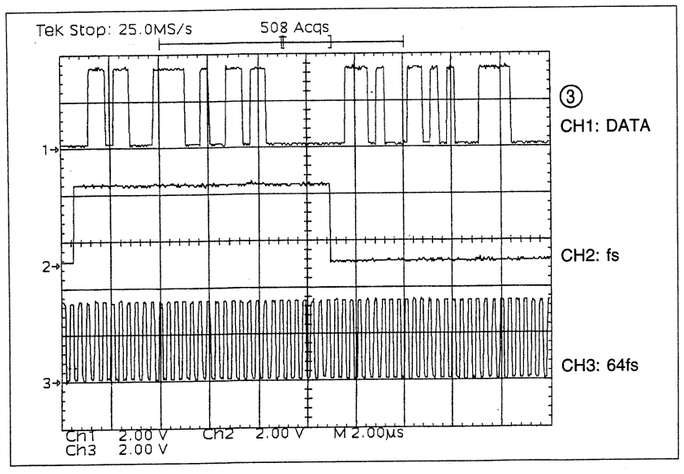

1
2
3
4
5
6
7
8
A
B
C
D
E
SUBWOOFER
(FRONT CH)
FROM R ch
FROM L ch
FRONT L/R ADD.
LPF
(FRONT CH)
TO
DAC
D/A OUT AMP
BUFF
ADDER
INV
ATTN.
PRE AMP
PRE-OUT
EXT.-IN
(dBV)
(dB)
30
20
10
0
−10
−14
−20
40
30
20
10
0dB
200mV/EXT.IN
D/A
0dBfs
−10dBfs
−20dBfs
−30dBfs
−40dBfs
Config2
Config1
3dB
6dB
1.5dB
6dB
1.5dB
2.5dB
TO FRONT CH
20.5dB
20.5dB
2.15V (6.65dBV)
1.2V (1.58dBV)
PRE-OUT
D/A OUT(DOLBY DIGITAL: DIALNORM−27dB)

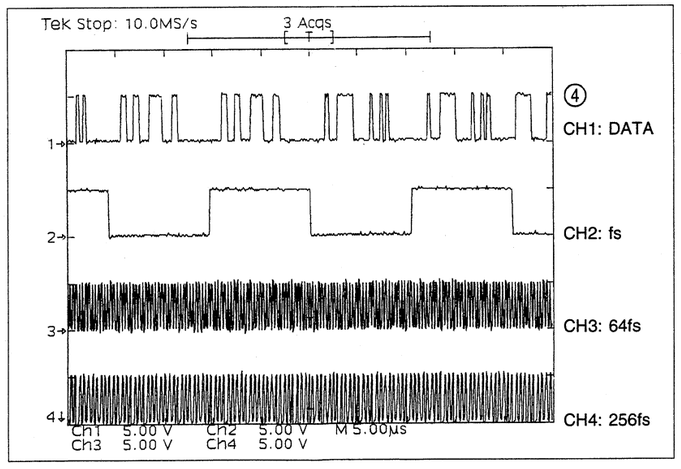
CLOCK FLOW & WAVE FORM IN DIGITAL BLOCK

Wave Form

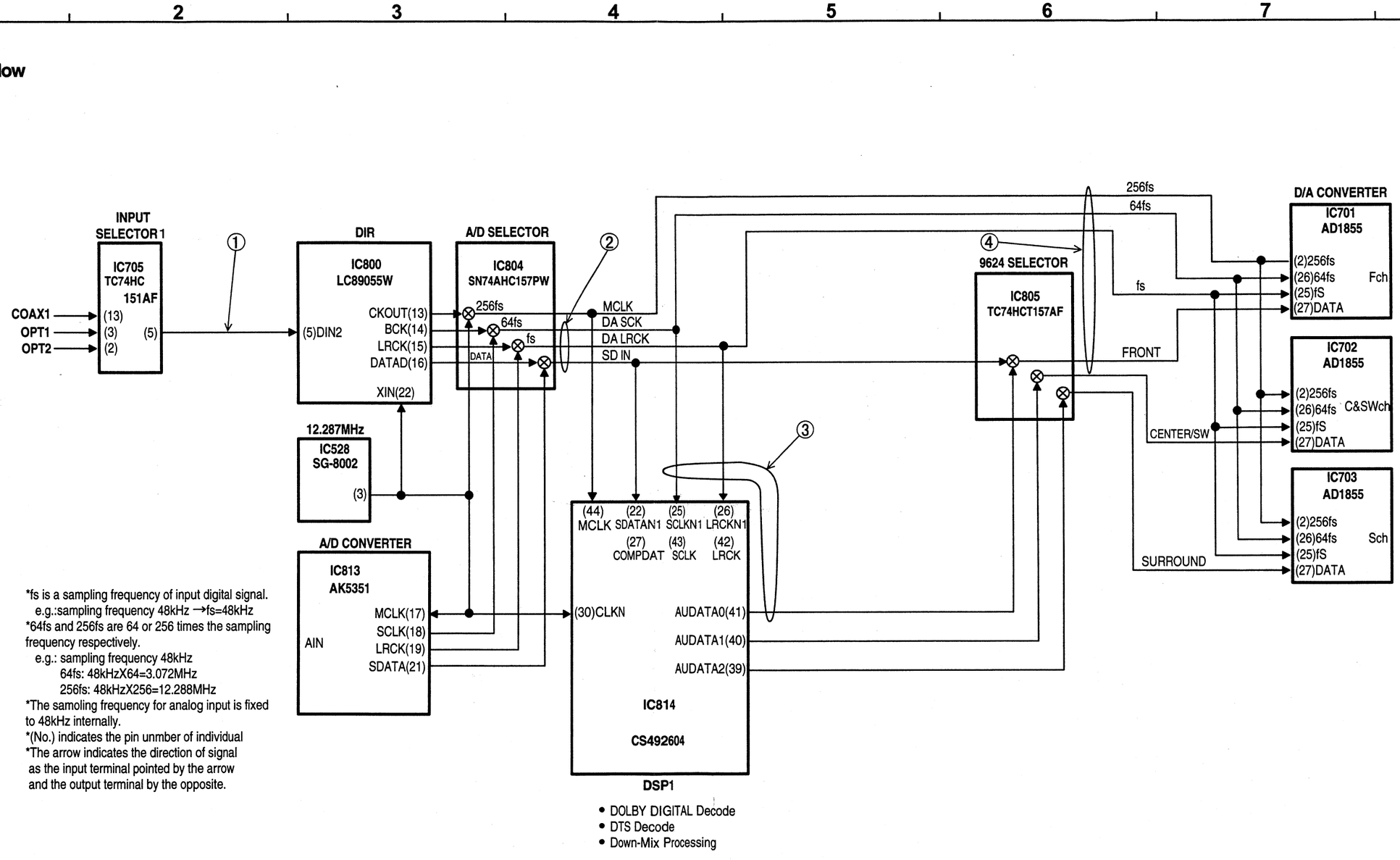








Clock Flow



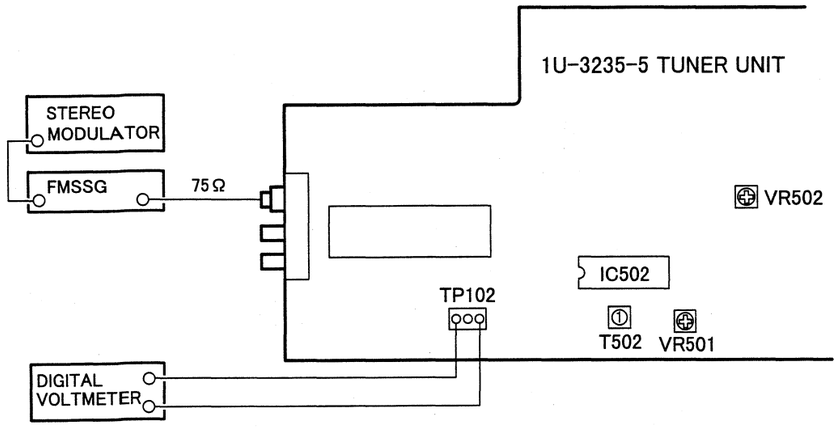
*fs is a sampling frequency of input digital signal.
e.g.:sampling frequency 48kHz →fs=48kHz
*64fs and 256fs are 64 or 256 times the sampling frequency respectively.
e.g.: sampling frequency 48kHz
64fs: 48kHzX64=3.072MHz
256fs: 48kHzX256=12.288MHz
*The samoling frequency for analog input is fixed to 48kHz internally.
*(No.) indicates the pin unmber of individual
*The arrow indicates the direction of signal as the input terminal pointed by the arrow and the output terminal by the opposite.

ADJUSTMENT

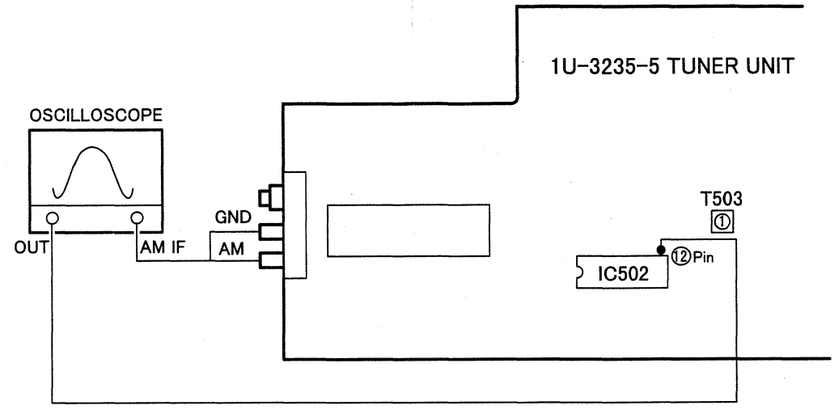
Tuner Section

CONNECTION DIAGRAM OF MEASURING INSTRUMENTS

● FM



● AM



FM/MPX ALIGNMENT

Step	Alignment Item	Tuning Frequency Setting	Input					Output		Adjust		Remarks
			Type	Frequency	Input Level	Modulation	Coupling	Type	Connect to	Points	Adjust to	
1	Tuning Center	98.1 MHz	FM SSG	98.1 MHz	60 dBμ	None	Antenna Terminal	Digital Voltmeter	TP102	T502	± 50mV	Function : FM Mode : Auto
2	Separation	98.1 MHz	FM SSG	98.1 MHz	60 dBμ	Stereo (L) 1kHz 100%	Antenna Terminal	AC Voltmeter	AUDIO OUT Terminal (R)	VR502	Maximum Separation	—
3	Signal Level	98.1 MHz	FM SSG	98.1 MHz	20 dBμ	Off	Antenna Terminal	—	—	VR501	Light "TUNED" FLD Character	—

AM ALIGNMENT

Step	Alignment Item	Frequency	Input	Output		Adjustment		Remarks
				Type	Connect to	Points	Adjust to	
1	IF	—	IF SWEEP (Input level is not over to work A.G.C.)	Oscilloscope	IC502 12Pin	T503	Maximum height and best symmetry curve	

Audio Section

Idling Current (1U-3232-1)

Required measurement equipment : DC Voltmeter

Preparation

(1) Avoid direct blow from an air conditioner or an electric fan, and adjust the unit at normal room tempereture 15 °C ~ 30 °C (59 °F ~ 86 °F).

(2) Presetting
- POWER (Power sourse switch) → OFF
- SPEAKER (Speaker terminal) → No load (Do not connect speaker, dummy resistor, etc.)

Adjustment

(1) Remove top cover and set VR501, VR502, VR503, VR504, VR505, on 1U-3232-1 (Power Unit) at counterclockwise (◯) fully.

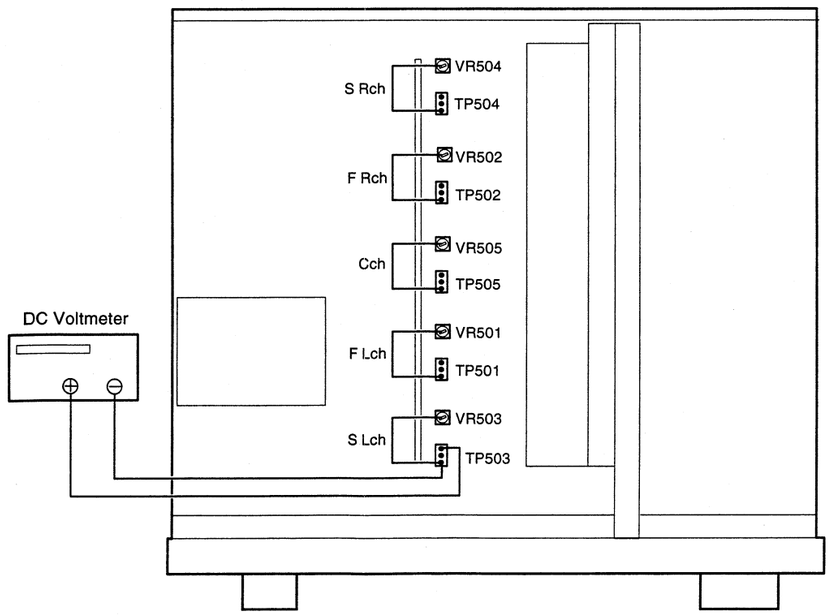
(2) Connect DC Voltmeter to test points (FRONT-Lch: TP501, FRONT-Rch: TP502, CENTER ch: TP505, SURROUND-Lch: TP503, SURROUND-Rch: TP504).

(3) Connect power cord to AC Line, and turn power switch "ON".

(4) Presetting. MASTER VOLUME : "---" counterclockwise (◯ min.)
MODE : 5CH STEREO
FUNCTION : CD

(5) Allow 2 minutes, and turn VR501 clockwise (◯) and adjust the TEST POINT voltage to 1.5 mV ±0.5 mV DC.

(6) After 10 minutes from preset, turn VR501 to set the voltage to 3 mV ±0.5 mV DC.
(7) Adjust the Variable Resistors of other channels in the same way.
(8) After 5 minutes from (6), turn VR501 to set the voltage to 3 mV ±0.5 mV DC.
(9) Adjust the Variable Resistors of other channels in the same way.

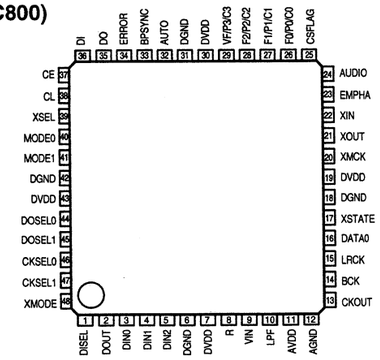


SEMICONDUCTORS

● IC's

Note: Abbreviation ahead of IC No. indicates the name of P.W.B.
PO: Power P.W.B.
EX: Exit in P.W.B.
CO: Control P.W.B.
RE: Regulator P.W.B.
AU: Audio/DSP P.W.B.

LC89055W (AU: IC800)

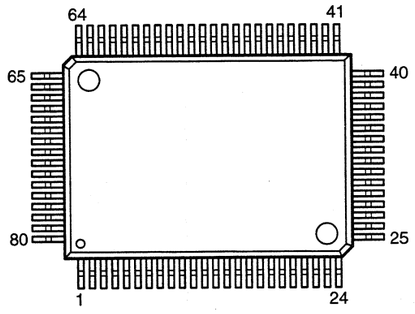


LC89055W Terminal Function

Pin No.	Pin Name	I/O	Function
1	DISEL	I	Data input terminal (select input pin of DIN0, DIN1)
2	DOUT	O	Input bi-phase data through output terminal
3	DIN0	I	Amp built-in coaxial/optical input correspond data input terminal
4	DIN1	I	Amp built-in coaxial/optical input correspond data input terminal
5	DIN2	I	Optical input correspond data input terminal
6	DGND		Digital GND
7	DVDD		Digital power supply
8	R	I	VCO gain control input terminal
9	VIN	I	VCO free-run frequency setting input terminal
10	LPF	O	PLL loop filter setting terminal
11	AVDD		Analog power supply
12	AGND		Analog GND
13	CKOUT	O	Clock output terminal (256fs, 384fs, 512fs, X'tal osc., VCO free-run osc.)
14	BCK	O	64fs clock output terminal
15	LRCK	O	fs clock output terminal (L: Rch, H: Lch, I2S: Reverse)
16	DATAO	O	Data output terminal
17	XSTATE	O	Input data detecting result output terminal
18	DGND		Digital GND
19	DVDD		Digital power supply
20	XMCK	O	X'tal osc. clock output terminal (24.576MHz or 12.288MHz)
21	XOUT	O	X'tal osc. connection output terminal
22	XIN	I	X'tal osc. connection output terminal
23	EMPHA	O	Emphasis information output terminal of channel status
24	AUDIO	O	Bit1 output terminal of channel status
25	CSFLAG	O	Top 40bit revise flag output terminal of channel status
26	F0/P0/C0	O	Input fs cal. sig. out / data type out / input word inf. output terminal
27	F1/P1/C1	O	Input fs cal. sig. out / data type out / input word inf. output terminal
28	F2/P2/C2	O	Input fs cal. sig. out / data type out / input word inf. output terminal
29	VF/P3/C3	O	Validity flag out / data type out / input word inf. output terminal
30	DVDD		Digital power supply
31	DGND		Digital GND
32	AUTO	O	Non PCM burst data transfer detect sig. output terminal
33	BPSYNC	O	Non PCM burst data preamble Pa, Pb, Pc, Pd sync sig. output terminal
34	ERROR	O	PLL lock error, data error flag output terminal
35	DO	O	CPU I/F read data output terminal
36	DI	I	CPU I/F write data input terminal
37	CE	I	CPU I/F chip enable input terminal
38	CL	I	CPU I/F clock input terminal
39	XSEL	I	Frequency select input pin of XIN X'tal osc. (24.576MHz or 12.288MHz)
40	MODE0	I	Mode setting input terminal
41	MODE1	I	Mode setting input terminal
42	DGND		Digital GND
43	DVDD		Digital power supply
44	DOSEL0	I	Data output format select input terminal
45	DOSEL1	I	Data output format select input terminal
46	CKSEL0	I	Output clock select input terminal
47	CKSEL1	I	Output clock select input terminal
48	XMODE	I	Reset input terminal

* For latch-up countermeasure, set digital (DVDD) and analog (AVDD) power on/off in the same timing.

TMP88CU74F
(CO: IC303)



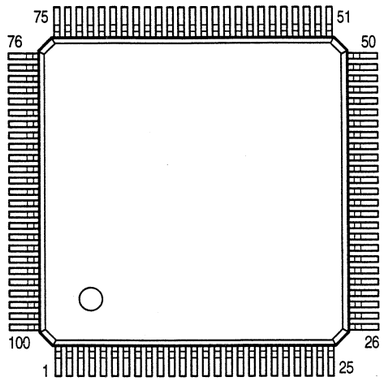
TMP88CU74F Terminal Function

Pin No.	Name	Symbol	I/O	Type	Op	Det	Res	Init	Function
1	P02/S01	RDS RESET	O	C	—	—	Z	L	RDS reset output (LC7074)
2	P03		O	C	—	—	Z	L	Fixed to L
3	P04	ST/MONO	O	C	—	—	Z	L	STEREO/MONO control signal, L: STEREO
4	P05	PLFL DATA	O	C	—	—	Z	L	PLL, FL control terminal (LC72131 & LC75721NE)
5	P06	PLL STB	O	C	—	—	Z	L	PLL control terminal (LC72131)
6	P07	PLFL CLK	O	C	—	—	Z	L	PLL, FL control terminal (LC72131 & LC75721NE)
7	Vss	Vss	I	—	GND	—	—	L	GND
8	Xout	Xout	O	—	—	—	—	—	XTAL
9	Xin	Xin	I	—	—	—	—	—	XTAL
10	RESET_	RESET_	I	—	Eu	Lv	L	—	Reset input
11	P22/XTOUT	TUNED_	I	—	Eu	Lv	Z	—	Tuning detect, L: Tuned
12	P21/XTIN	STEREO_	I	—	Eu	Lv	Z	—	L: At stereo receive
13	TEST	TEST	I	—	GND	S	—	—	Connect to GND
14	P20/INT5_	B.DOWN_	I	—	Eu	Lv	Z	—	Power down detect, L: Power down
15	P10/INT0_	PROTECT_	I	—	Ed	E&L	Z	—	PROTECTION detect input, H: Detect
16	P11/INT1	RDS START	I	—	—	—	Z	L	RDS data input (LC7074)
17	P12		O	C	—	—	Z	L	Fixed to L
18	P13		O	C	—	—	Z	L	Fixed to L
19	P14		O	C	—	—	Z	L	Fixed to L
20	P15/INT3	REMOCON	I	—	Ed	E&L	Z	—	Remote control signal input
21	P16/INT2	ACK	O	C	—	—	Z	L	MAIN-SUB CPU comm. control terminal
22	P17/INT4	REQ	I	—	Eu	—	Z	L	MAIN-SUB CPU comm. control terminal
23	P30/SCL	SI	I	C					MAIN-SUB CPU comm. control terminal
24	P31/SDA	SO	O	C					MAIN-SUB CPU comm. control terminal
25	P32/SCK0_	CLK	O	C					MAIN-SUB CPU comm. control terminal
26	P40/AIN0	MODE	I	—	Eu	Lv	Z	—	Destination switching input
27	P41/AIN1	KEY1	I	—	Eu	Lv	Z	—	Button input 1
28	P42/AIN2	KEY2	I	—	Eu	Lv	Z	—	Button input 2
29	P43/AIN3	KEY3	I	—	Eu	Lv	Z	—	Button input 3
30	P44/AIN4	FUNC STB1	O	C	—	—	Z	—	Function control output (TC9274N), INPUT
31	P45/AIN5	FUNC/T. CON CLK	O	C	—	—	Z	L	Function control output (TC9274N, TC9273), TONE control output (TC9184P)
32	P46/AIN6	FUNC/T. CON DATA	O	C	—	—	Z	L	Function control output (TC9274N, TC9273), TONE control output (TC9184P)
33	P47/AIN7	FUNC STB2	O	C	—	—	Z	L	Function control output (NJU7313), 6CH EXT. IN
34	P50/AIN8	E.VOL STB	O	C	—	—	L	L	Elect. volume control output (TC9459)
35	P51/AIN9	TONE STB	O	C	—	—	L	L	TONE control output (TC9184P)
36	P52/AIN10	E.VOL DATA	O	C	—	—	L	H	Elect. volume control output (TC9459)
37	P53/AIN11	E.VOL CLK	O	C	—	—	L	H	Elect. volume control output (TC9459)
38	VASS	VASS	I						Ref. volt (GND)
39	VAREF	VAREF	I						Ref. volt (VDD)
40	VDD	VDD	I						Power supply
41	P60	FL CE	O	P	Ed	S	L	H	FL display control output (LC75712NE)
42	P61	FL RES	O	P	Ed	S	L	H	FL display control output (LC75712NE)
43	P62		O	P	Ed	—	Z	L	Fixed to L
44	P63	FA-RELAY	O	P	Id	—	L	L	Front SP relay A control terminal, L: Mute
45	P64	FB-RELAY	O	P	Id	—	L	L	Front SP relay B control terminal, L: Mute
46	P65	C-RELAY	O	P	Id	—	L	L	Center SP relay control terminal, L: Mute
47	P66	S-RELAY	O	P	Id	—	L	H	Surround SP relay control terminal, L: Mute
48	P67	PRE F MUTE	O	P	Ed	—	L	H	Front PRE OUT mute control terminal, L: Mute
49	P70	PRE C MUTE	O	P	Ed	—	L	L	Center PRE OUT mute control terminal, L: Mute
50	P71	PRE S MUTE	O	P	Ed	—	L	L	Surround PRE OUT mute control terminal, L: Mute
51	P72	SUB WOOFER MUTE	O	P	Ed	—	L	H	Sub-woofer PRE OUT mute control terminal, L: Mute
52	P73	H/P RELAY	O	P	Id	—	L	H	H/P OUT relay control terminal, L: Mute
53	P74	EXP OE	O	P	Ed	—	L	H	Port expander control terminal (TC4094B)
54	P75	EXP CLK	O	P	Ed	—	L	L	Port expander control terminal (TC4094B)
55	P76	EXP DATA	O	P	Ed	—	L	L	Port expander control terminal (TC4094B)
56	P77	EXP STB	O	P	Ed	—	L	L	Port expander control terminal (TC4094B)
57	P80	POWER	O	P	Id	—	L	H	Power relay control output, H: ON
58	P81	RESET2	O	P	Id	—	L	L	Reset signal output to sub-CPU, H: Reset
59	P82	SUB-CPU-B-DOWN	O	P	Id	—	L	L	B-DOWN signal output to sub-CPU
60	P83	TAPE MON. LED	O	P	Id	—	L	L	TAPE MONITOR LED indicator control, H: MONITOR
61	P84	STANDBY	O	P	Id	—	L	H	Standby LED drive output H: Light
62	P85	(DIRECT)	O	P	Id	—	L	L	DIRECT relay control, H: DIRECT
63	P86	(S1)	O	P	Id	—	L	—	Video signal switching control output
64	P87	(S2)	O	P	Id	—	L	—	Fixed to L
65	P90	TUNER MUTE	O	P	Ed	—	L	H	TUNER mute control terminal, H: Mute
66	P91		O	P	Id	—	L	H	Not Used
67	P92		O	P	Id	Lv	Z	—	Fixed to L
68	P93		O	P	Id	Lv	Z	—	Fixed to L
69	P94		O	P	Id	Lv	Z	—	Fixed to L
70	P95	SEL A (M)	I	—	Eu	Lv	Z	—	Master volume rotation detect input (rotary encoder)
71	P96	SEL B (M)	I	—	Eu	Lv	Z	—	Master volume rotation detect input (rotary encoder)
72	P97	CINEMA EQ	O	P	Eu	Lv	Z	L	CINEMA EQ control output, H: ON
73	PD0	VOL MUTE	O	P	Ed	—	L	L	Master volume minimum control, L: Min.
74	PD1	SEL C (S)	I	—	Eu	Lv	Z	—	Surround mode rotation detect input (rotary encoder)
75	PD2	SEL D (S)	I	—	Eu	Lv	Z	—	Surround mode rotation detect input (rotary encoder)
76	PD3	SEL E (F)	I	—	Eu	Lv	Z	—	Input selector switch rotation detect input (rotary encoder)
77	PD4	SEL F (F)	I	—	Eu	Lv	Z	—	Input selector switch rotation detect input (rotary encoder)
78	Vkk	Vkk	—	—	—	—	—	—	GND fixed
79	P00/SCK1_	RDS CLK	I	—	—	S	Z	—	RDS clock input (LC7074)
80	P01/SI1	RDS DATA	I	—	—	S	Z	—	RDS data input (LC7074)

NOTE:

Pin No. : Terminal number of microcomputer.
Port Name : The name entered in the data sheet of microcomputer.
Symbol : Symbolized interface function.
I/O : Input or out of part.
"I" = Input port
"O" = Output port
Type : Composition of port in case of output port.
"C" = CMOS output
"N" = NMOS open drain output
"P" = PMOS open drain output
Op : Pull up/Pull down selection information.
"Iu" = Inner microcomputer pull up
"Id" = Inner microcomputer pull down
"Eu"= External microcomputer pull up
"Ed"= External microcomputer pull down
Det : Indicates judging state of input port. Level detection is "LV"; Edge detection is "Ed"; Detection by both shifting is "E&L"; Serial data detection is "S" (Serial data output is also "S").
Res : State at reset.
"H" = Outputs High Level at reset
"L" = Outputs Low Level at reset
"Z" = Becomes High impedance mode at reset
Ini : Initial output state.
Function : Function and logical level explanation of signals to be interface.

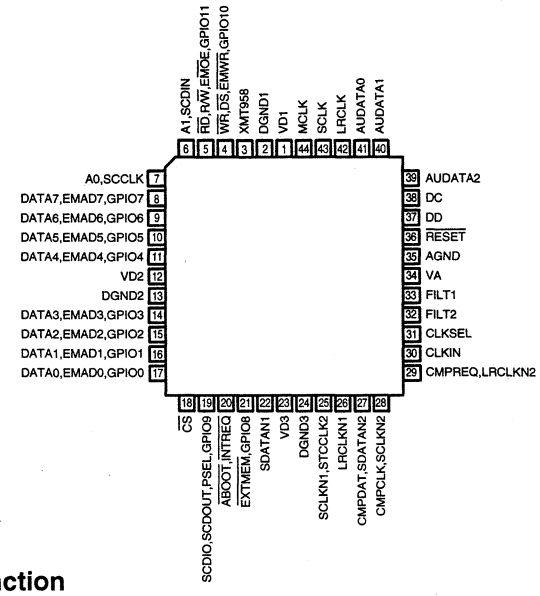
TMP93CS41F (AU: IC301)



TMP93CS41F Terminal Function

Pin No.	Name	Symbol	I/O	Type	Op	Det	Res	Init	Function
1	V REFL		—	—	—	—	—	—	A/D ref. GND
2	A Vss	←	—	—	—	—	—	—	A/D GND
3	A Vcc	←	—	—	—	—	—	—	AD +5V
4	_NMI		I	—	—	—	—	—	Not used (fixed to H)
5	P70/TI0	C15	O	C	—	—	L	L	Fixed to L (DSP ROM address cont. out bit 15, not used)
6	P71/TO1	C16	O	C	—	—	L	L	DSP program ROM address cont. output bit 16
7	P72/TO2	C17	O	C	—	—	L	L	DSP program ROM address cont. output bit 17
8	P73/TO3		O	C	—	—	L	L	
9	P80/INT4/TI4	_INTREQ	I/O	C	Eu	E↓&L	Z	—	DSP request input and cont. output (L: Rq & cont.)
10	P81/INT5/TI5	B. DOWN_	I	—	Eu	E↑&L	Z	—	Power down detect (H: Detected)
11	P82/TO4	DSP SS	O	C	—	—	H	H	DSP chip select cont. output (L: Data out)
12	P83/TO5	_REQ	O	C	Eu	—	H	L	MAIN-SUB CPU comm. control output (L: Comm. request from sub)
13	P84/INT6/TI6	_ACK	I	—	Eu	E↓&L	—	—	MAIN-SUB CPU comm. control input (L: Ack. return from main)
14	P85/INT7/TI7	ERR	I	—	—	E↑&L	—	—	DIR control input terminal (LC89055Q)(H: ERR)
15	P86/TO6	_DSP RESET	O	C	—	—	L	L	DSP reset output terminal (L: Reset)
16	P87/INT0	_CS	I	—	—	E↑&L	—	—	DIR control input terminal (LC89055Q), when CH status change L→H
17	P90/TXD0	SI	O	C					MAIN-SUB CPU comm. control terminal (data output)
18	P91/RXD0	SO	I	—					MAIN-SUB CPU comm. control terminal (data input)
19	P92/_CTS0/SCLK0	CLK	I	C					MAIN-SUB CPU comm. control terminal (I2C clock in/output)
20	P93/TXD1	DSP DATA	O	C	—	—	L	L	DSP data output terminal
21	P94/RXD1	DSP SO	I	—	—	Lv	—	—	DSP status data input terminal
22	P95/SCLK1	DSP CLK	O	C	—	—	Z	L	DSP data clock output terminal
23	AM8/_16	←	—	—	—	—	—	—	Fixed to +5V
24	CLK		O	C	Eu	—	—	—	
25	Vcc	←	—	—	—	—	—	—	+5V
26	Vss	I/O1	—	—	—	—	—	—	GND
27	X1	Xin	I	—	—	—	—	—	X'tal connection
28	X2	Xout	O	—	—	—	—	—	X'tal connection
29	_EA	←	—	—	—	—	—	—	Fixed to GND
30	_RESET	RESET2_	I	—	Eu	Lv	L	—	Reset input (controlled by main CPU)
31	P96/XT1	A/D RESET	O	N	Eu	—	H	H	A/D control terminal (L: Reset)
32	P97/XT2		O	C	Ed	—	L	L	
33	TEST1	←	I	—	—	—	—	—	Connected to TEST2
34	TEST2	←	I	—	—	—	—	—	Connected to TEST1
35	PA0	DINA	O	C	Ed	—	L	L	Digital input switching control output
36	PA1	DINB	O	C	Ed	—	L	L	Digital input switching control output
37	PA2	DINC	O	C	Ed	—	L	L	Digital input switching control output
38	PA3		O	C	Ed	—	L	L	
39	PA4	DIRECT	O	C	Ed	—	L	L	Digital direct data switch cont. terminal (H: Direct)
40	PA5		O	C	Ed	—	L	L	
41	PA6	DEEMP	O	C	Ed	—	L	L	DAC de-emphasis filter cont. out terminal (H: ON)
42	PA7/SCOUT	96k-DAC	O	C	—	—	Z	L	DAC control terminal (H: Sample frequency 96kHz)
43	ALE	←	O	C	—	—	L	L	Address latch enable
44	Vcc		—	—	—	—	—	—	+5V
45	P00/AD0	AD0	I/O	C	—	—	Z	L	EPROM data in D0 / address out A0
46	P01/AD1	AD1	I/O	C	—	—	Z	L	EPROM data in D1 / address out A1
47	P02/AD2	AD2	I/O	C	—	—	Z	L	EPROM data in D2 / address out A2
48	P03/AD3	AD3	I/O	C	—	—	Z	L	EPROM data in D3 / address out A3
49	P04/AD4	AD4	I/O	C	—	—	Z	L	EPROM data in D4 / address out A4
50	P05/AD5	AD5	I/O	C	—	—	Z	L	EPROM data in D5 / address out A5
51	P06/AD6	AD6	I/O	C	—	—	Z	L	EPROM data in D6 / address out A6
52	P07/AD7	AD7	I/O	C	—	—	Z	L	EPROM data in D7 / address out A7
53	P10/AD8/A8	A8	O	C	—	—	Z	L	EPROM address out A8
54	P11/AD9/A9	A9	O	C	—	—	Z	L	EPROM address out A9
55	P12/AD10/A10	A10	O	C	—	—	Z	L	EPROM address out A10
56	P13/AD11/A11	A11	O	C	—	—	Z	L	EPROM address out A11
57	P14/AD12/A12	A12	O	C	—	—	Z	L	EPROM address out A12
58	P15/AD13/A13	A13	O	C	—	—	Z	L	EPROM address out A13
59	P16/AD14/A14	A14	O	C	—	—	Z	L	EPROM address out A14
60	P17/AD15/A15	A15	O	C	—	—	Z	L	EPROM address out A15
61	_WDTOUT	←	O	C	—	—	Z	H	Watch dog output
62	Vss	←	—	—	—	—	—	—	GND
63	Vcc	←	—	—	—	—	—	—	+5V
64	P20/A0/A16	A16	O	C	—	—	Z	L	EPROM address out A16
65	P21/A1/A17	DIR CLK	O	C	—	—	Z	L	DIR control terminal (LC89055Q) control clock output
66	P22/A2/A18	DIR CE	O	C	—	—	Z	L	DIR control terminal (LC89055Q) control chip enable output
67	P23/A3/A19	DIR MOSI	O	C	—	—	Z	L	DIR control terminal (LC89055Q) control data output
68	P24/A4/A20	DIR MISO	I	—	—	Lv	—	—	DIR control terminal (LC89055Q) control data input
69	P25/A5/A21	SW-SUM	O	C	—	—	L	L	Subwoofer output summation cont. output
70	P26/A6/A22	DAC-RESET	O	C	—	—	L	H	DAC control terminal (L: Power down mode, ↑(rising edge) Reset)
71	P27/A7/A23	SEL CK	O	C	—	—	Z	L	ADC/DIR data clock switching control terminal (L: ADC)
72	P30/_RD	_RD	O	C	—	—	Z	L	Flash memory control terminal
73	P31/_WR	_WR	O	C	—	—	Z	L	Flash memory control terminal
74	P32/_HWR	CSI	I	—	—	Lv	—	—	DIR control input terminal (L: PCM)
75	P33/_WAIT	ERR MUTE_	O	C	—	—	L	L	Pop noise preventive mute control output (L: Mute)
76	P34/_BUSRQ		O	C	—	—	Z	L	
77	P35/_BUSRQ	DIG. (AC3) MUTE	O	C	—	—	Z	L	Digital mute control output (L: AC-3 or DTS decode enable)
78	P36/_R/W		O	C	—	—	Z	L	
79	P37/_RAS	DIR RESET	O	C	—	—	Z	L	DIR control output (LC89055Q) (L: Reset)
80	P40/_CS0/_CAS0		O	C	—	—	Z	L	
81	P41/_CS1/_CAS1		O	C	—	—	Z	L	
82	P42/_CS2/_CAS2	_CS0	O	C	—	—	Z	L	Flash memory control terminal
83	P60/PG00	DSP C. RESET	O	C	—	—	Z	L	DSP reset output terminal (L: Reset)
84	P61/PG01	SCDOUT	I	—	—	Lv	—	—	DSP status data input terminal
85	P62/PG02	DSP_C. CS	O	C	—	—	Z	L	DSP chip select cont. output (L: Data out)
86	P63/PG03	DSP C. CLK	O	C	—	—	Z	L	DSP data clock output terminal
87	P64/PG10	SCDIN	O	C	—	—	Z	L	DSP data output terminal
88	P65/PG11		O	C	—	—	Z	L	
89	P66/PG12		O	C	—	—	Z	L	
90	P67/PG13		O	C	—	—	Z	L	
91	Vss	←	—	—	—	—	—	—	GND
92	P50/AN0		I	—	Eu	Lv	Z	—	
93	P51/AN1		I	—	Eu	Lv	Z	—	
94	P52/AN2	EMP	I	—	—	Lv	—	—	H: EMP on
95	P53/AN3	96K DET	I	—	—	Lv	—	—	96k signal detect input, H: 96k
96	P54/AN4		I	—	Eu	Lv	Z	—	
97	P55/AN5		I	—	Eu	Lv	Z	—	
98	P56/AN6		I	—	Eu	Lv	Z	—	
99	P57/AN7		I	—	Eu	Lv	Z	—	
100	V REFH	←	—	—	—	—	—	—	AD ref. +5V

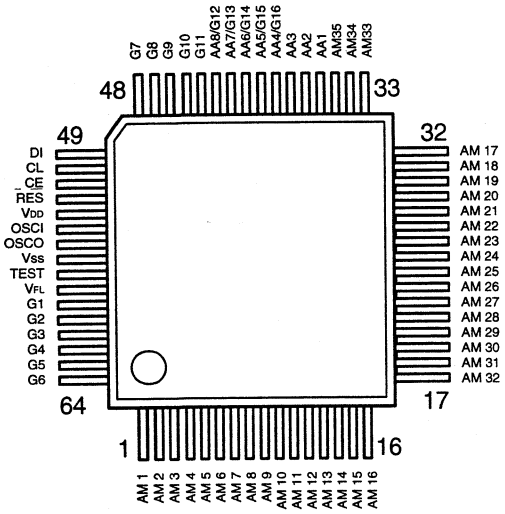
CS492604-CLR
(AU: IC814)



CS492604-CLR Terminal Function

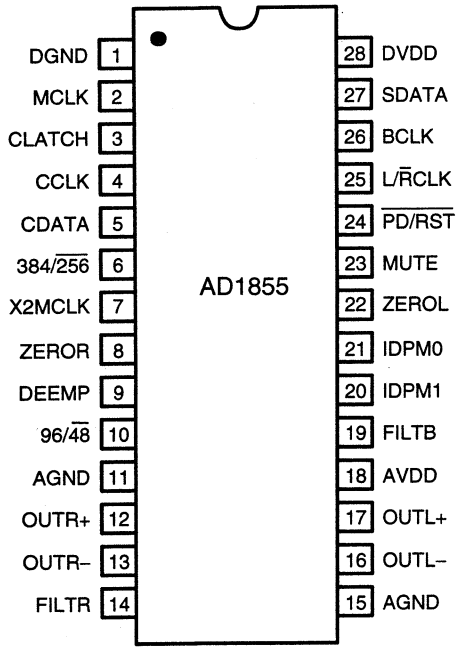
Pin No.	Pin Name	Function
1	VD1	Digital positive supply
2	DGND1	Digital supply ground
3	XMT958	SPDIF transmitter output
4	$\overline{WR}$, $\overline{DS}$, $\overline{EMWR}$, GPIO10	Host write strobe or host data strobe or external memory write enable or general purpose input & output number10
5	$\overline{RD}$, R/$\overline{W}$, $\overline{EMOE}$, GPIO11	Host parallel output enable or host parallel R/$\overline{W}$ or external memory outout enable or general purpose input & output number11
6	A1, SCDIN	Host adddress bit one or SPI serial control data input
7	A0, SCCLK	Host parallel address bit zero or serial control port clock
8	DATA7, EMAD7, GPIO7	
9	DATA6, EMAD6, GPIO6	
10	DATA5, EMAD5, GPIO5	
11	DATA4, EMAD4, GPIO4	
12	VD2	Digital positive supply
13	DGND2	Digital supply ground
14	DATA3, EMAD3, GPIO3	
15	DATA2, EMAD2, GPIO2	
16	DATA1, EMAD1, GPIO1	
17	DATA0, EMAD0, GPIO0	
18	$\overline{CS}$	Host parallel chip select, host serial SPI chip select
19	SCDIO, SCDOUT, PSEL, GPIO9	Serial control port data input and output, parallel port type select
20	$\overline{INTREQ}$, $\overline{ABOOT}$	Control port interrupt request, automatic boot enable
21	$\overline{EXTMEM}$, GPIO8	External memory chip select or general purpose input & output number 8
22	SDATAN1	PCM audio data input number one
23	VD3	Digital positive supply
24	DGND3	Digital supply ground
25	SCLKN1, STCCLK2	PCM audio input bit clock
26	LRCLKN1	PCM audio input sample rate clock
27	CMPDAT,SDATAN2	PCM audio data input number two
28	CMPCLK, SCLKN2	PCM audio input bit clock
29	CMPREQ, LRCLKN2	PCM audio input sample rate clock
30	CLKIN	Master clock input
31	CLKSEL	DSP clock select
32	FILT2	Phase locked loop filter
33	FILT1	Phase-locked loop filter
34	VA	Analog positive supply
35	AGND	Analog supply ground
36	$\overline{RESET}$	Master reset input
37	DD	Reserved
38	DC	Reserved
39	AUDATA2	Digital audio output 2
40	AUDATA1	Digital audio output 1
41	AUDATA0	Digital audio output 0
42	LRCLK	Audio output sample rate clock
43	SCLK	Audio output bit clock
44	MCLK	Audio master clock

LC75721E (EX: IC101)



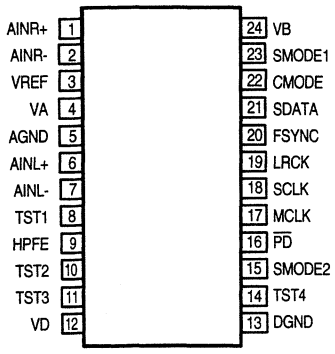
Symbol	Function
V_{DD}	Power terminal +5V
Vss	Power terminal GND
V_{FL}	Power terminal FL drive
DI CL CE	Serial data transfer terminal DI: Data CL: Clock CE: Chip enable
OSCI OSCO	External CR connecting terminal
$\overline{RES}$	System reset terminal
AM1~AM35 AA1~AA3	Anode output terminal
AA4/G16 AA5/G15 AA6/G14 AA7/G13 AA8/G12	Anode/Grid output terminal
G1~G11	Grid output terminal
TEST	LSI test terminal

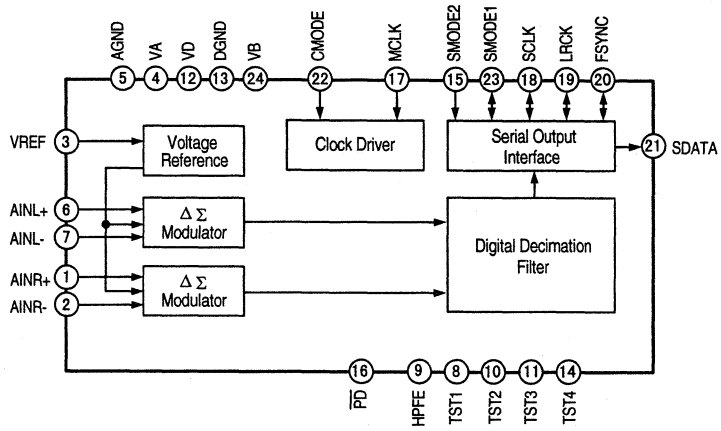
AD1855 (AU: IC701, 702, 703)



Pin No.	Name	I/O	Description
1	DGND	I	Digital Ground.
2	MCLK	I	Master Clock Input.
3	CLATCH	I	Latch input for control data.
4	CCLK	I	Control clock input for control data.
5	CDATA	I	Serial control input.
6	384/256	I	Selects the master clock mode.
7	X2MCLK	I	Selects internal clock doubler (LO) or internal clock=MCLK (HI)
8	ZEROR	O	Right Channel Zero Flag Output.
9	DEEMP	I	De-Emphasis.
10	96/48	I	Selects 48 kHz (LO) or 96 kHz Sample Frequency Control.
11,15	AGND	I	Analog Ground.
12	OUTR+	O	Right Channel Positive line level analog output.
13	OUTR–	O	Right Channel Negative line level analog output.
14	FILTR	O	Voltage Reference Filter Capacitor Connection.
16	OUTL–	O	Left Channel Negative line level analog output.
17	OUTL+	O	Left Channel Positive line level analog output.
18	AVDD	I	Analog Power supply.
19	FILTB	O	Filter Capacitor connection.
20	IDPM1	I	Input serial data port mode control one.
21	IDPM0	I	Input serial data port mode control zero.
22	ZEROL	O	Left Channel Zero Flag output.
23	MUTE	I	Mute. Assert HI to mute both stereo analog outputs.
24	PD/RST	I	Power-Down/Reset.
25	L/RCLK	I	Left/Right clock input for input data.
26	BCLK	I	Bit clock input for input data.
27	SDATA	I	Serial input.
28	DVDD	I	Digital Power Supply.

AK5351 (AU: IC813)

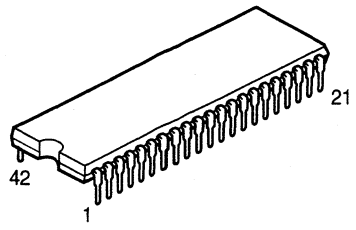


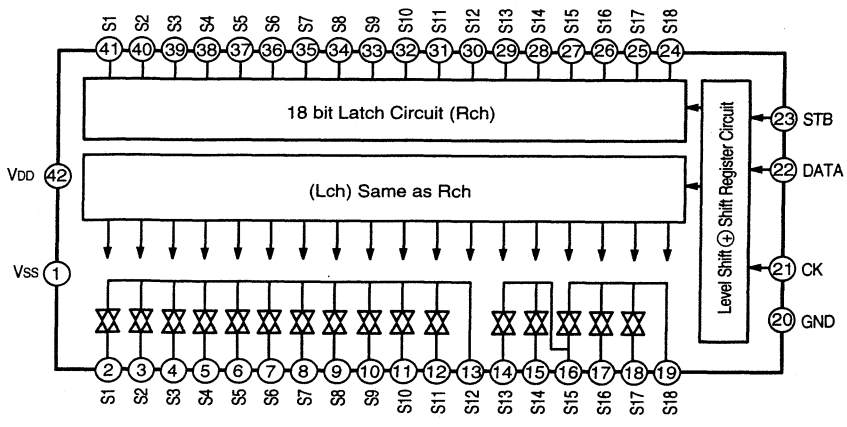


AK5351 Terminal Function

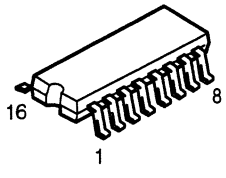
Pin No.	Symbol	I/O	Function
1	AINR+	I	Rch analog non-inverted input pin.
2	AINR−	I	Rch analog inverted input pin
3	VREF	O	Vref. output pin (VA-2.6V)
4	VA	—	Analog part power supply pin (+5V)
5	AGND	—	Analog ground pin
6	AINL+	I	Lch analog non-inverted input pin
7	AINL−	I	Lch analog inverted input pin
8	TST1		Test pin
9	HPFE	I	Hi-pass filter enable pin, "H": ON, "L": OFF
10	TST2		Test pin
11	TST3		Test pin
12	VD	—	Digital part power supply pin (+5V)
13	DGND	—	Digital ground pin
14	TST4		Test pin
15	SMODE2	I	Interface clock select pin
16	PD	I	Power down pin, "L": power down mode
17	MCLK	I	Master clock input pin, CMODE="H": 384fs, "L": 256fs
18	SCLK	I/O	Serial data clock pin
19	LRCK	I/O	Input channel select pin
20	FSYNC	I/O	Frame sync clock pin
21	SDATA	O	Serial data output pin
22	CMODE	I	Master clock select pin, "H": MCLK=384fs, "L": 256fs
23	SMODE1	I	Interface clock select pin
24	VB	—	Bulk power supply pin (+5V)

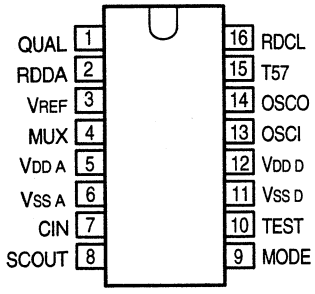
TC9274N-011 (AU: IC107)





Europe model only
SAA6579T (CO: IC301)

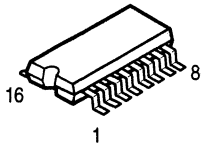


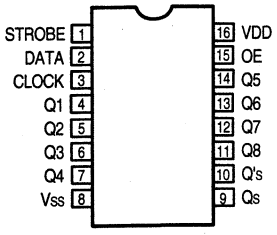


SAA6579T Terminal Function

Pin No.	Symbol	Function
1	QUAL	Quality indication output.
2	RDDA	RDS data output.
3	VREF	Reference voltage output (0.5 VDD A).
4	MUX	Multiplex signal input.
5	VDD A	+5V power supply for analog part.
6	VSS A	Ground for analog part (0V).
7	CIN	Subcarrier input to comparator.
8	SCOUT	Subcarrier ouput of reconstruction filter.
9	MODE	Oscillation mode/test control input.
10	TEST	Test enable input.
11	VSS D	Ground for digital part (0V).
12	VDD D	+5V power supply for digital part.
13	OSCI	Oscillator input.
14	OSCO	Oscillator output.
15	T57	57kHz clock signal output.
16	RDCL	RDS clock output.

TC4094BF (CO: IC304, EX: IC103)





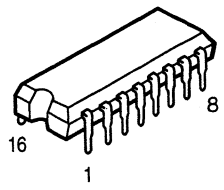
CO: IC304

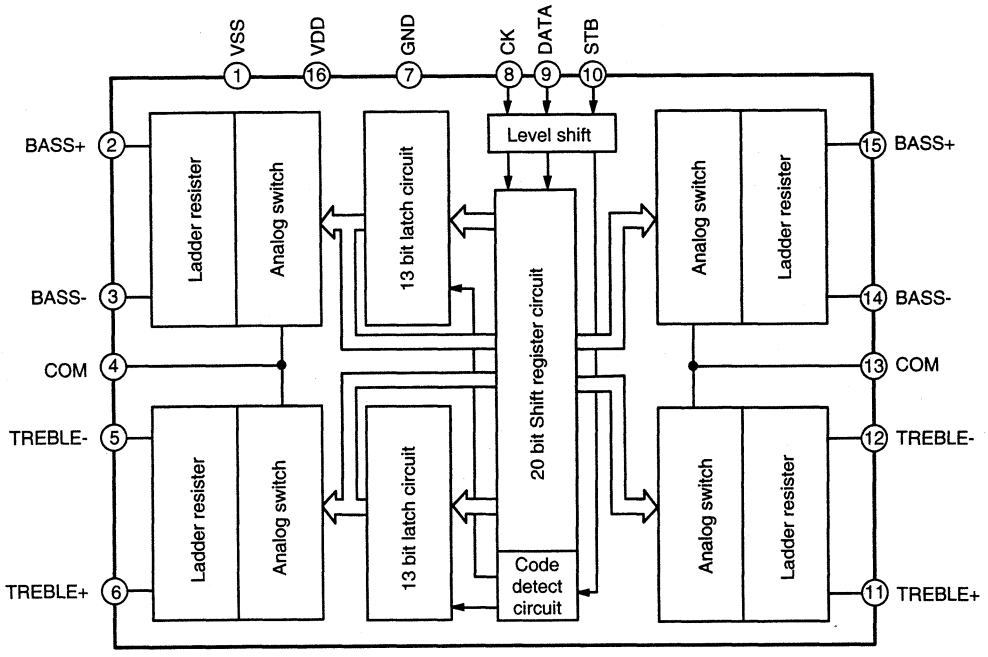
Port	Symbol	Function
Q1	A	Video input switching
Q2	B	Video input switching
Q3	C	Video input switching
Q4	D	Video output switching
Q5	E	Video output switching
Q6	F	Video output switching (DVD/TV)
Q7	G	Video output switching (DVD/TV)
Q8	Not Used	

EX: IC103

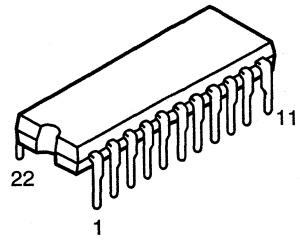
Port	Symbol	Function
Q1	LOCK LED	"LOCK" LED drive output (H: Lock)
Q2	DOLBY DIGITAL LED	"DOLBY DIGITAL" LED drive output (H: D.Digital)
Q3	dts LED	"dts" LED drive output (H: dts)
Q4	AUTO LED	"AUTO" LED drive output (H: input mode "AUTO")
Q5	DTS LED	"DTS" LED drive output (H: input mode "DTS")
Q6	PCM LED	"PCM" LED drive output (H: input mode "PCM")
Q7	FRONT SP-A LED	"FRONT SPEAKER A" LED drive output
Q8	FRONT SP-B LED	"FRONT SPEAKER B" LED drive output

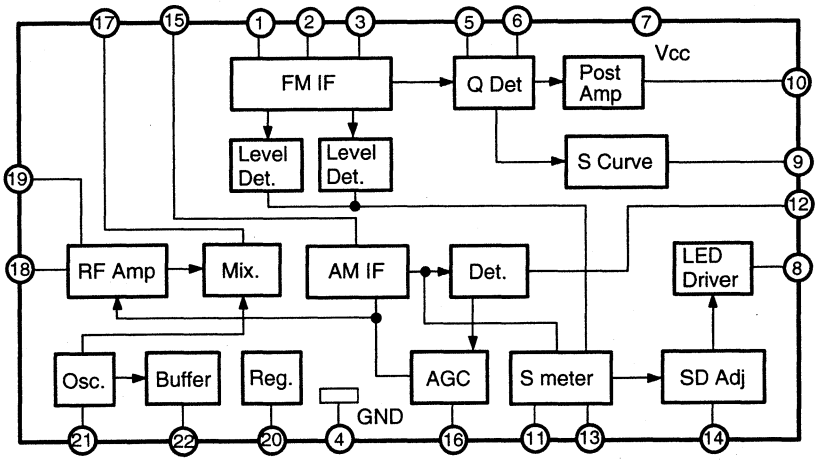
TC9184AP (CO: IC102)



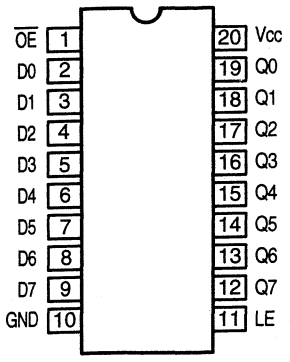


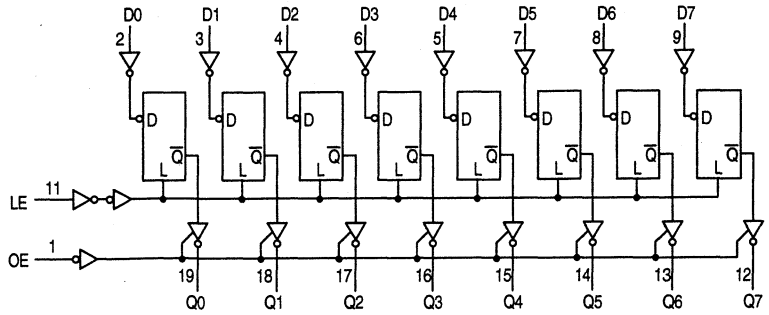
LA1265 (S) (RE: IC502)



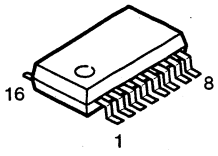


SN74LV573ANS (AU: IC302)

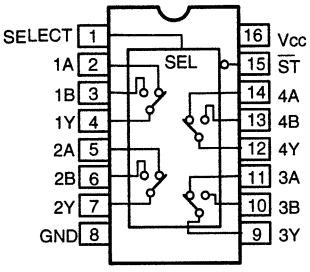




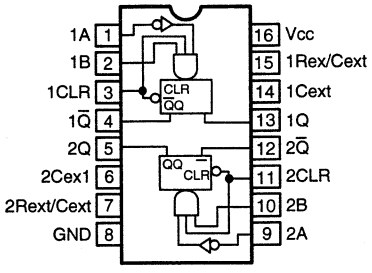
SN74AHC157PW
(AU: IC804)
TC74VHC123AFT
(AU: IC801, 806)
TC74HC151AF
(CO: IC705)
TC74HCT157AF
(AU: IC805)



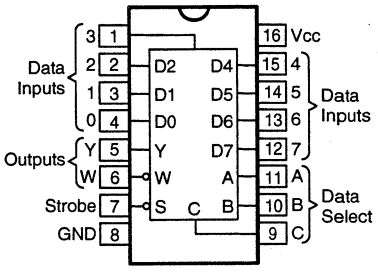
SN74AHC157PW



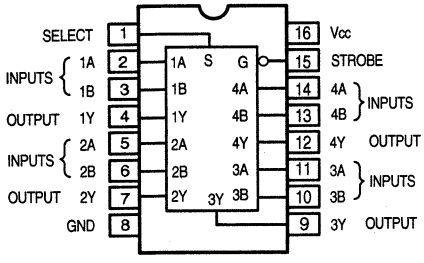
TC74VHC123AFT



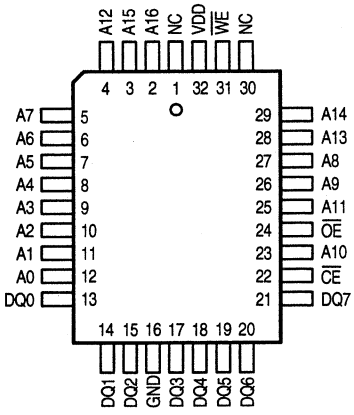
TC74HC151AF



TC74HCT157AF



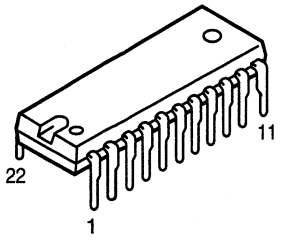
W29EE011P-90 (AU: IC303)
W29C020P-90 (AU: IC817)

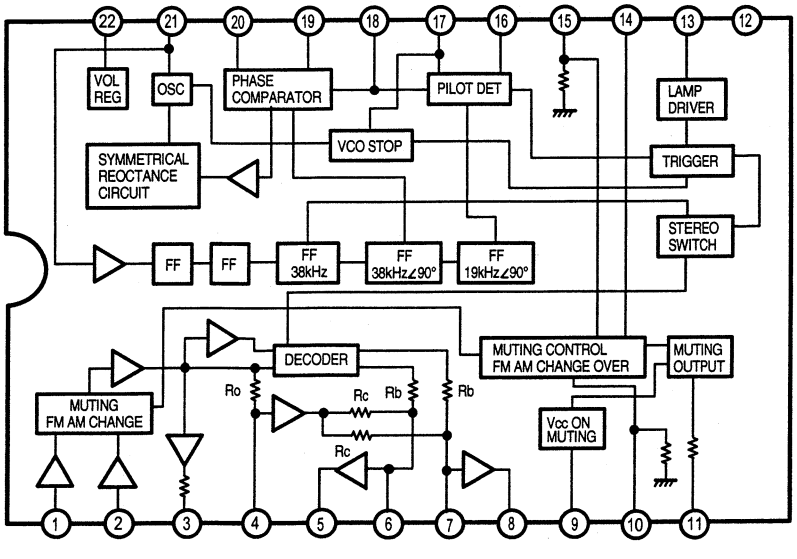


Terminal Function

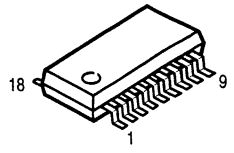
Name	Function
A0 - A16	Address input
DQ0 - DQ7	Data in/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{DD}	Power terminal
GND	GND
NC	No connection

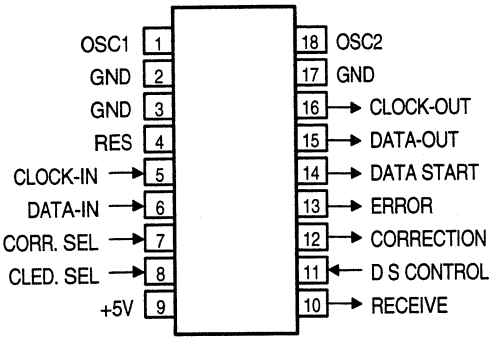
LA3401
(RE: IC503)



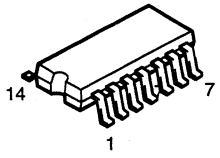


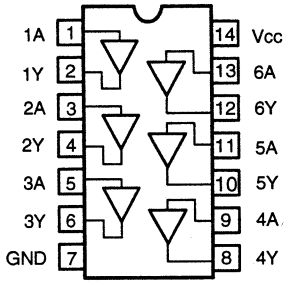
LC7074M (CO: IC302)
(Europe model only)



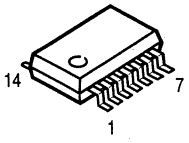


TC74HCT7007AF
(AU: IC821)

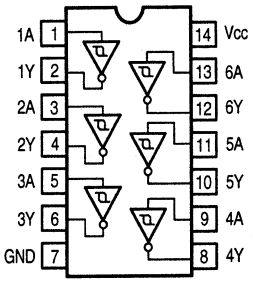




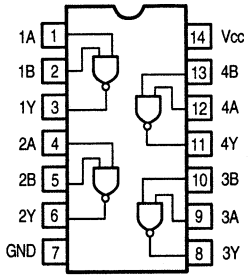
SN74LV14APW (AU: IC809)
SN74LV00APW (AU: IC807, 808)
TC74HCU04AF (CO: IC704)



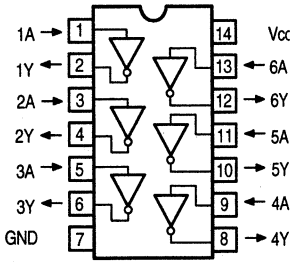
SN74LV14APW



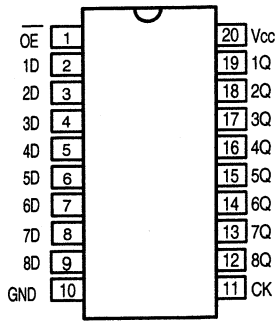
SN74LV00APW



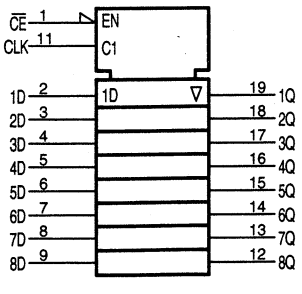
TC74HCU04AF



SN74AHC574APW
(AU: IC815, 816)



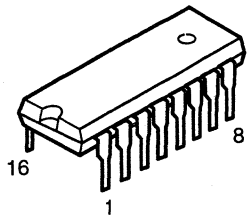
Logic symbol

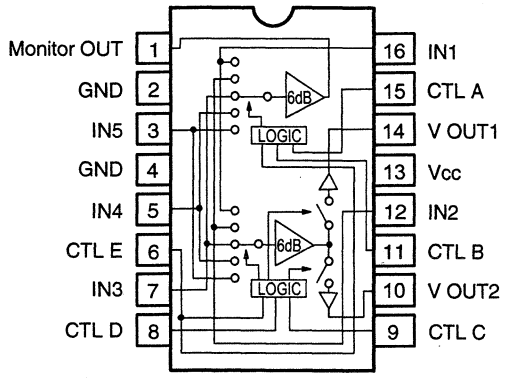


Function Table
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q0
H	X	X	Z

BA7625
(PO: IC402, 450)





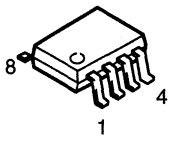
A	B	E	MONITOR OUT
L	L	*	IN 1
H	L	*	IN 2
L	H	*	IN 3
H	H	L	IN 4
H	H	H	IN 5

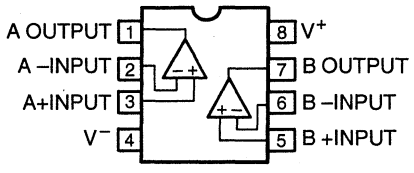
C	D	E	V OUT 1
L	L	*	—
H	L	*	IN 2
L	H	*	IN 3
H	H	L	IN 4
H	H	H	IN 5

C	D	E	V OUT 2
L	L	*	IN 1
H	L	*	—
L	H	*	IN 3
H	H	L	IN 4
H	H	H	IN 5

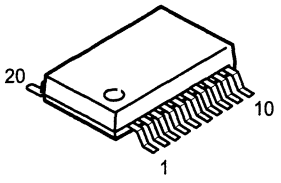
Note 1: * mark means that feasible for either H or L.
Note 2: Each input terminal is provided with sink chip clamp (BA7625).
Each input terminal takes 20kohm at the end (BA7626).

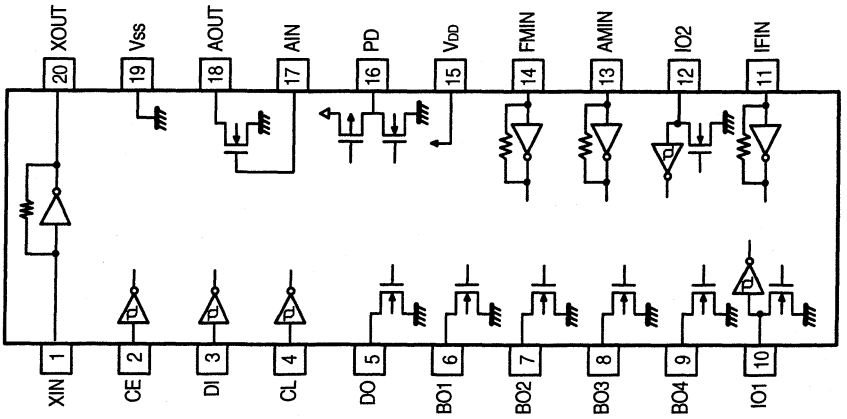
BA4510F (AU: IC811, 812)
NJM2068MD (EX: IC301~304,308~310,701,801~803)
(CO: IC103,104)
(AU: IC106,109,731~733,)



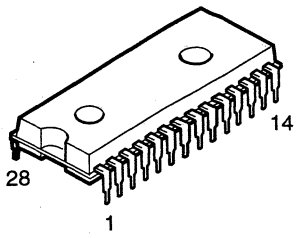


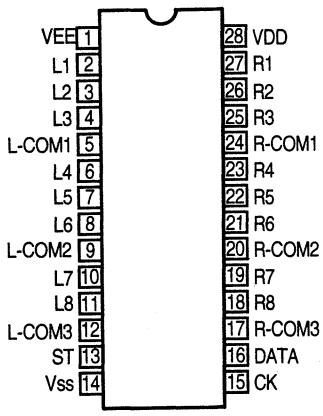
LC72131M (RE: IC507)

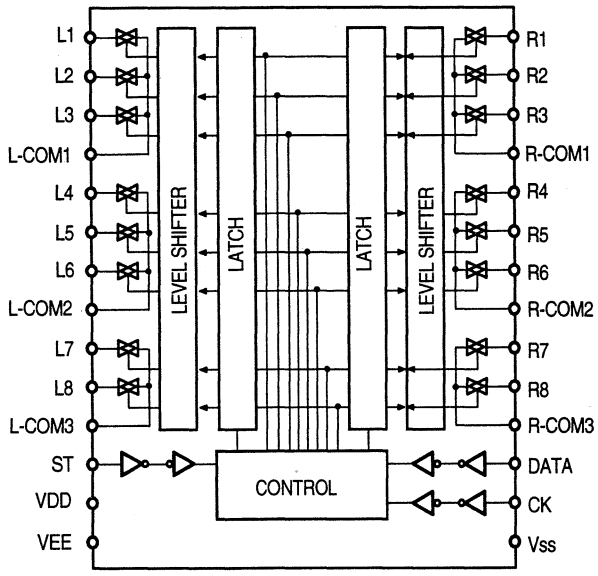




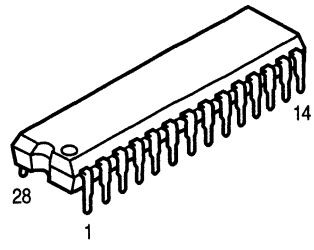
NJU7313AL (EX: IC311)

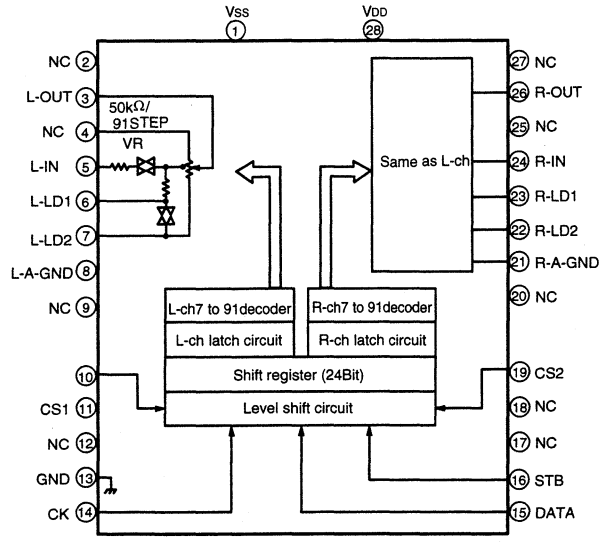




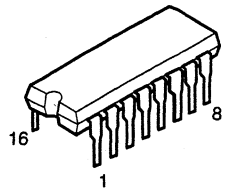


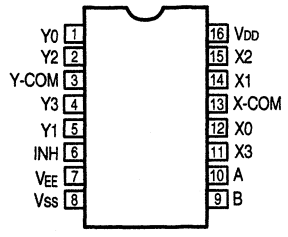
TC9459N (EX: IC805~807)

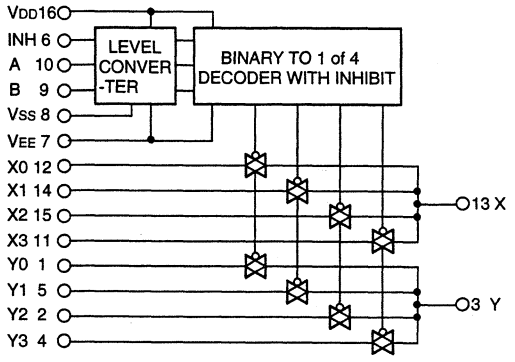




BU4052BC (PO: IC401)





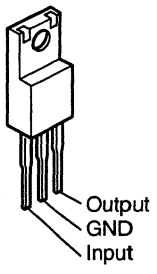


TRUTH TABLE

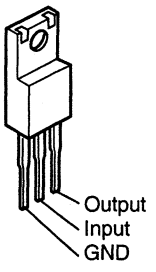
INHIBIT	A	B	ON SWITCH
L	L	L	X0 Y0
L	H	L	X1 Y1
L	L	H	X2 Y2
L	H	H	X3 Y3
H	X	X	NONE

X: don't Care

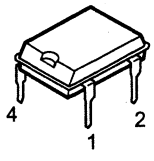
NJM7805FA (S) (RE: IC902, 903)
NJM7806FA (S)
(PO: IC502)
(RE: IC904)
NJM7812FA (S) (RE: IC906)
BA033T (AU: 819)

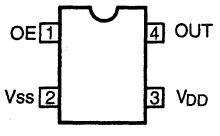


NJM7912FA (RE: IC907)



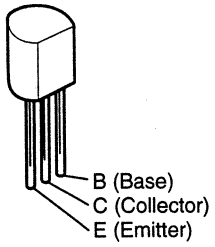
SG-8002DCPT (12.287MHz)
(AU: XL802)



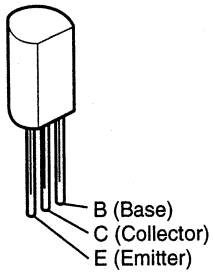


● TRANSISTORS

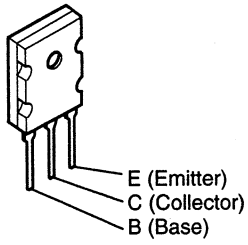
2SA970 (BL)
2PA1015GR
2SA988 (E/F)
2SC1841 (E/F)
2SC2878 (A/B)
2PC1815 (BL)



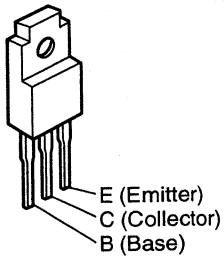
2SC2705 (O) / (Y)



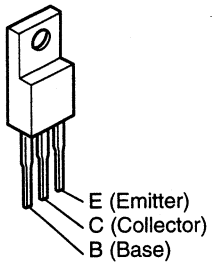
2SA1491
2SC3855



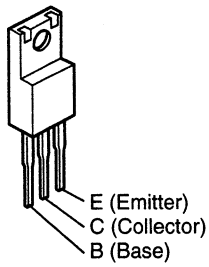
2SB1186A
2SD1763A



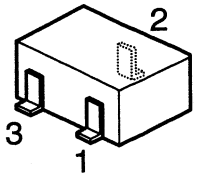
2SA1670 (O/P/Y)



2SC4495



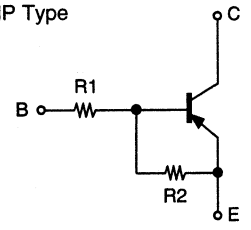
DTA114TK
DTA114EK
DTA144EK
DTC114EK
DTC144EK
DTC323TK
RN2402



1: GND/Emitter
2: Out/Collector
3: In/Base

DTA114TK
DTA114EK
DTA144EK
RN2402

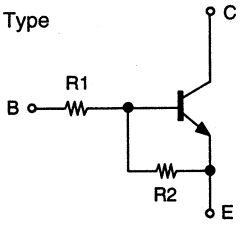
PNP Type



	R1	R2
DTA114TK	10kohm	–
DTA114EK	10kohm	10kohm
DTA144EK	47kohm	47kohm
RN2402	10kohm	10kohm

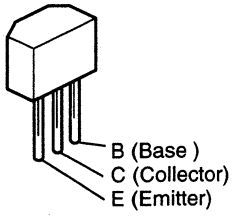
DTC114EK
DTC144EK
DTC323TK

NPN Type

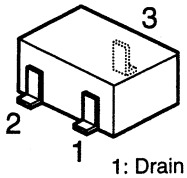


	R1	R2
DTC114EK	10kohm	10kohm
DTC144EK	47kohm	47kohm
DTC323TK	2.2kohm	–

2SA933S (S)
2SC3311A
2SC1645S (B)

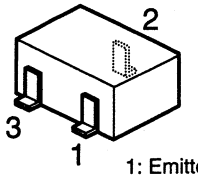


2SK209 (GR)



1: Drain
2: Source
3: Gate

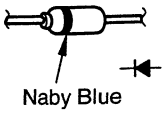
2SA1182 Y/O
2SC2996 (Y)
2SC3326 (A/B)
2SD601A



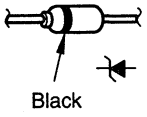
1: Emitter
2: Collector
3: Base

● DIODES (included LED)

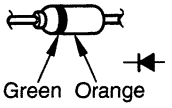
1SS270A



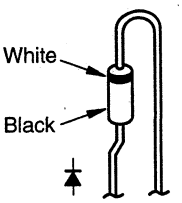
MTZJ3.3A MTZJ7.5A
MTZJ5.6A MTZJ9.1A
MTZJ6.2A MTZJ36A



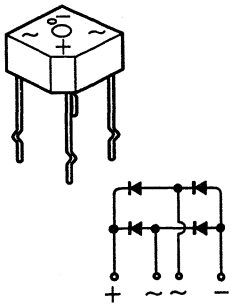
1SR35-400A



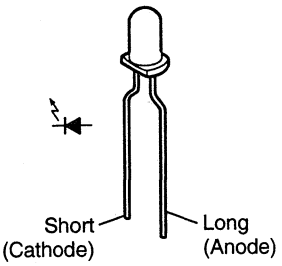
DSM1D2(Type 3)



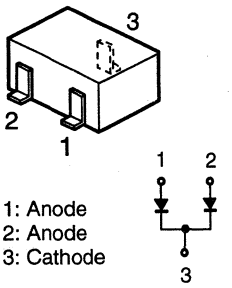
S4VB20



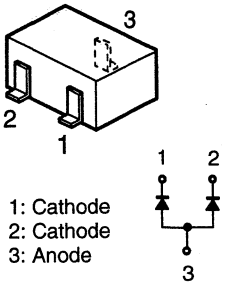
SEL1210S (Red)
SEL4214S



DAN202K

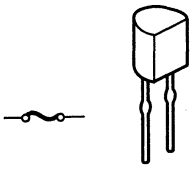


DAP202K



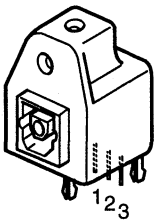
● IC PROTECTOR

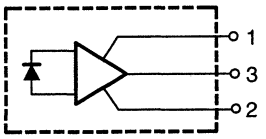
ICP-N15 (PO: IC501)



● OPTICAL

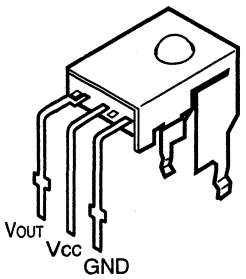
INPUT
GP1F37R1 (CO: IC702, 703)

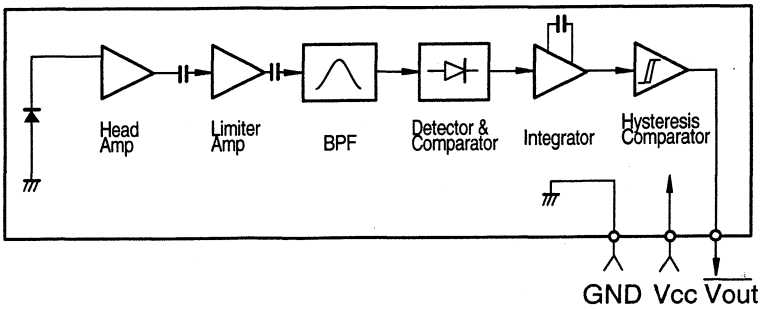




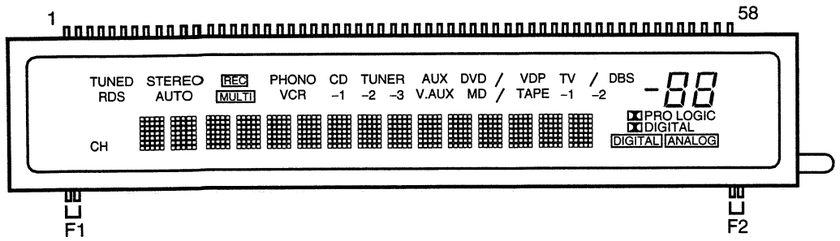
● OTHERS

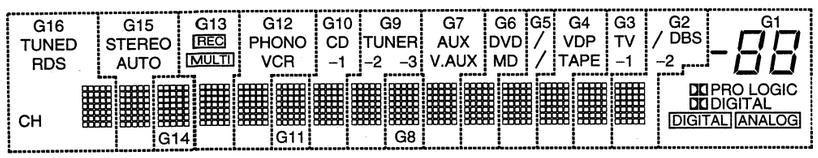
GP1U271X (Remote Control Sensor)
(EX: IC102)

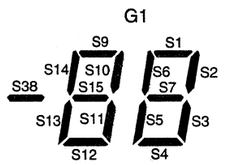


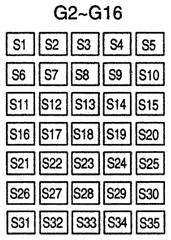


● FL DISPLAY CM1690C (VI : FL101)









Pin Assignment

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
CONNECTION	F1	F1	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18
PIN NO.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
CONNECTION	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32	S33	S34	S35	S36	S37	S38
PIN NO.	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58		
CONNECTION	G16	G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	F2	F2		

F1,F2 : Filament
G1~G16 : Grid
S1~S38 : Anode

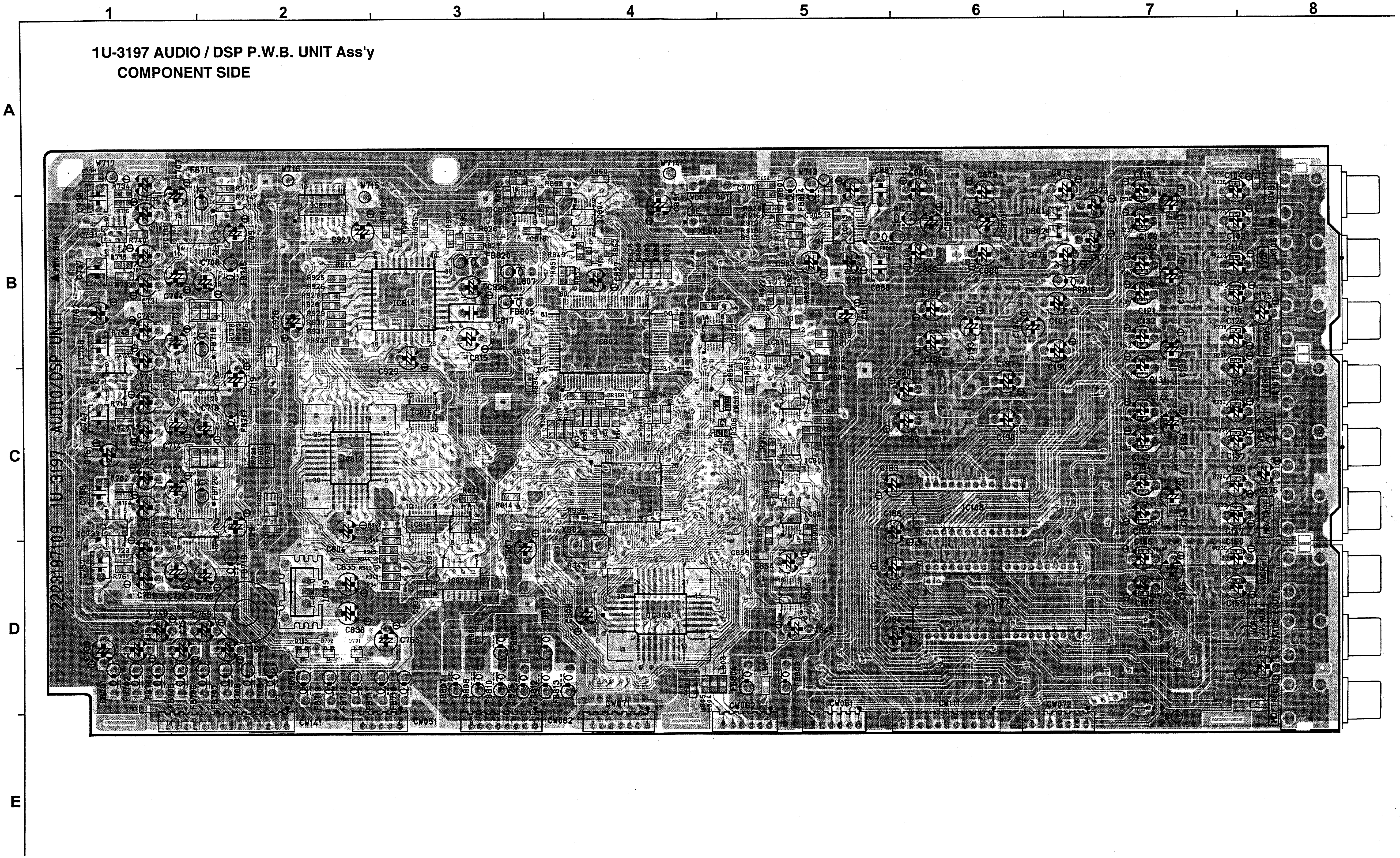
Anode & Grid Assignment

	G1	G2~G16		G1	G2~G16		G1	G2~G16		G1	G2~G16
S1	S1	S1	S10	S10	S10	S19	——	S19	S28	——	S28
S2	S2	S2	S11	S11	S11	S20	——	S20	S29	——	S29
S3	S3	S3	S12	S12	S12	S21	——	S21	S30	——	S30
S4	S4	S4	S13	S13	S13	S22	——	S22	S31	——	S31
S5	S5	S5	S14	S14	S14	S23	——	S23	S32	——	S32
S6	S6	S6	S15	S15	S15	S24	——	S24	S33	——	S33
S7	S7	S7	S16	——	S16	S25	——	S25	S34	——	S34
S8		S8	S17	DIGITAL	S17	S26	——	S26	S35	——	S35
S9	S9	S9	S18	PRO LOGIC	S18	S27	——	S27			

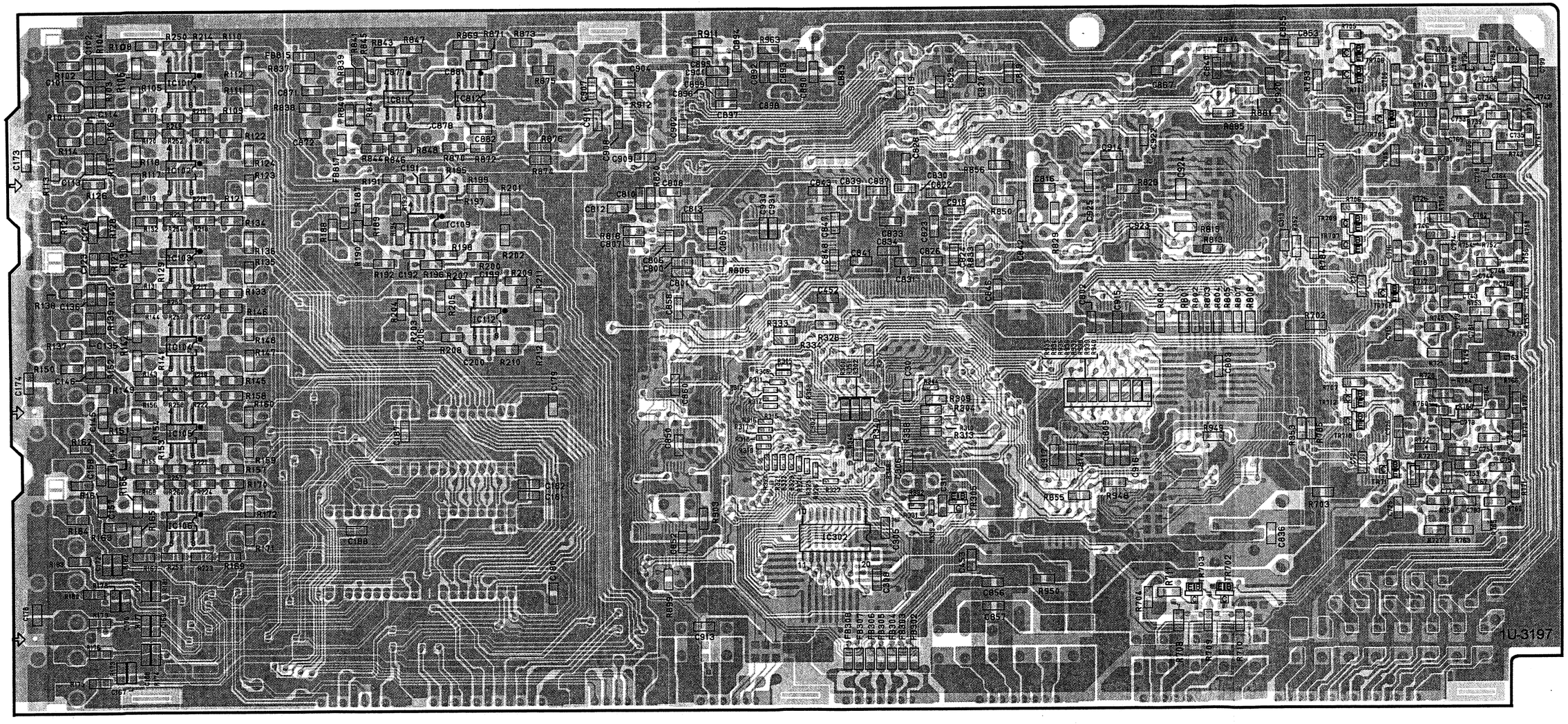
	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G15	G16
S36	DIGITAL	/	TV	VDP	/(DVD)	DVD	AUX	——	TUNER	CD	——	PHONO	REC	——	STEREO	TUNED
S37	ANALOG	–2	–1	TAPE	/(MD)	MD	V.AUX	——	–2	–1	——	VCR	MULTI	——	AUTO	RDS
S38	S38	DBS	——	——	——	——	——	——	–3	——	——	——	——	——	——	CH

PRINTED WIRING BOARDS

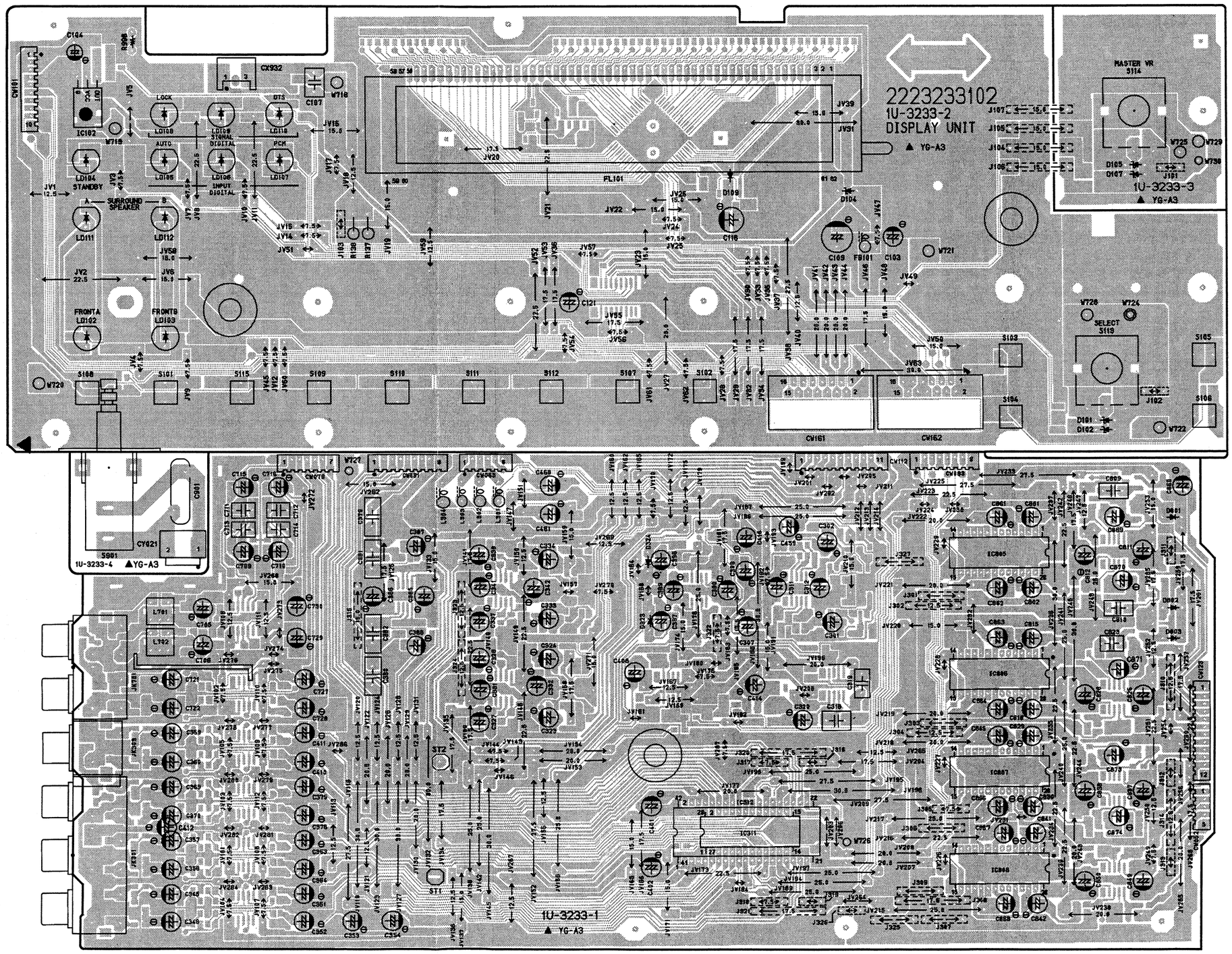
1U-3197 AUDIO / DSP P.W.B. UNIT Ass'y
COMPONENT SIDE



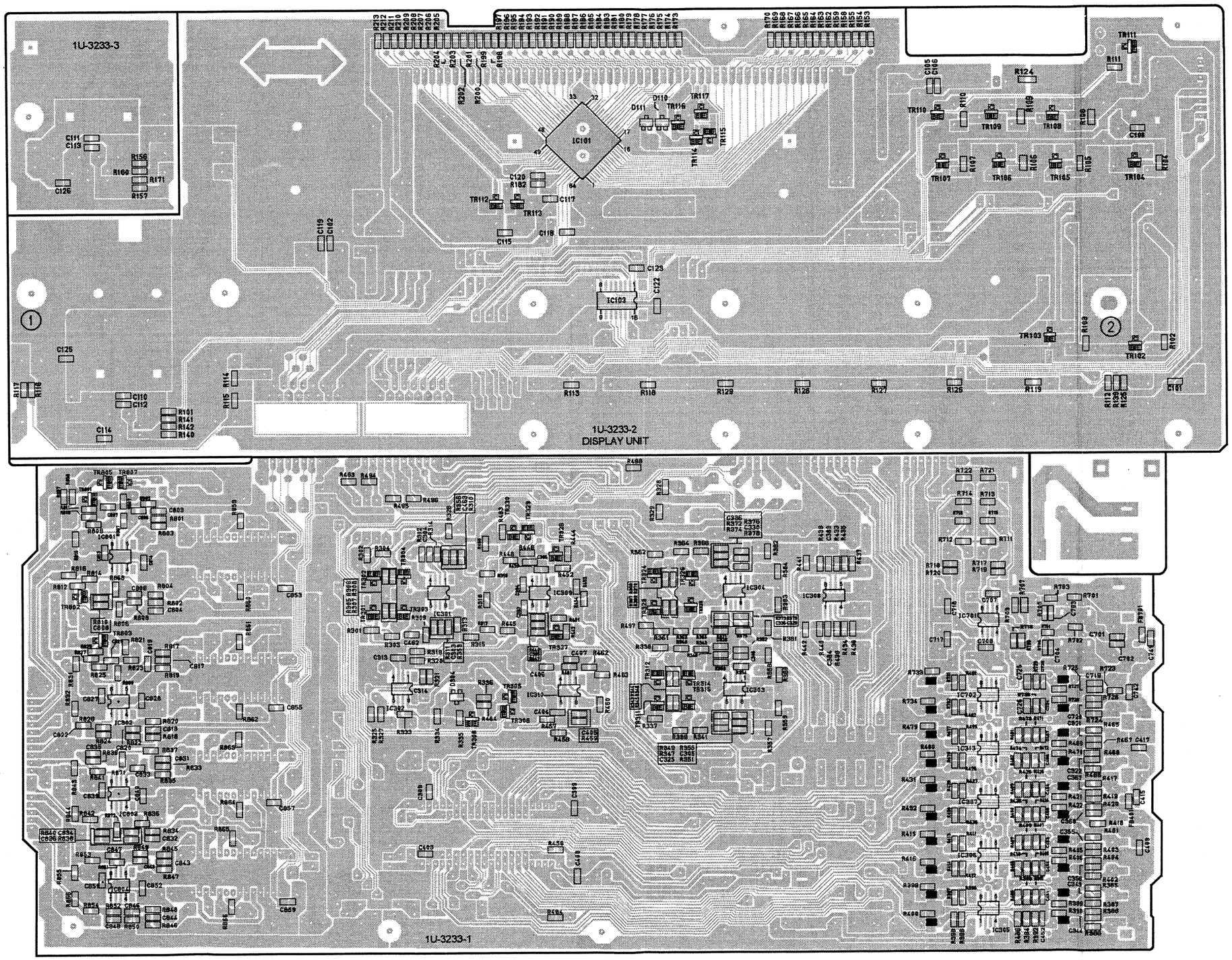
FOIL SIDE



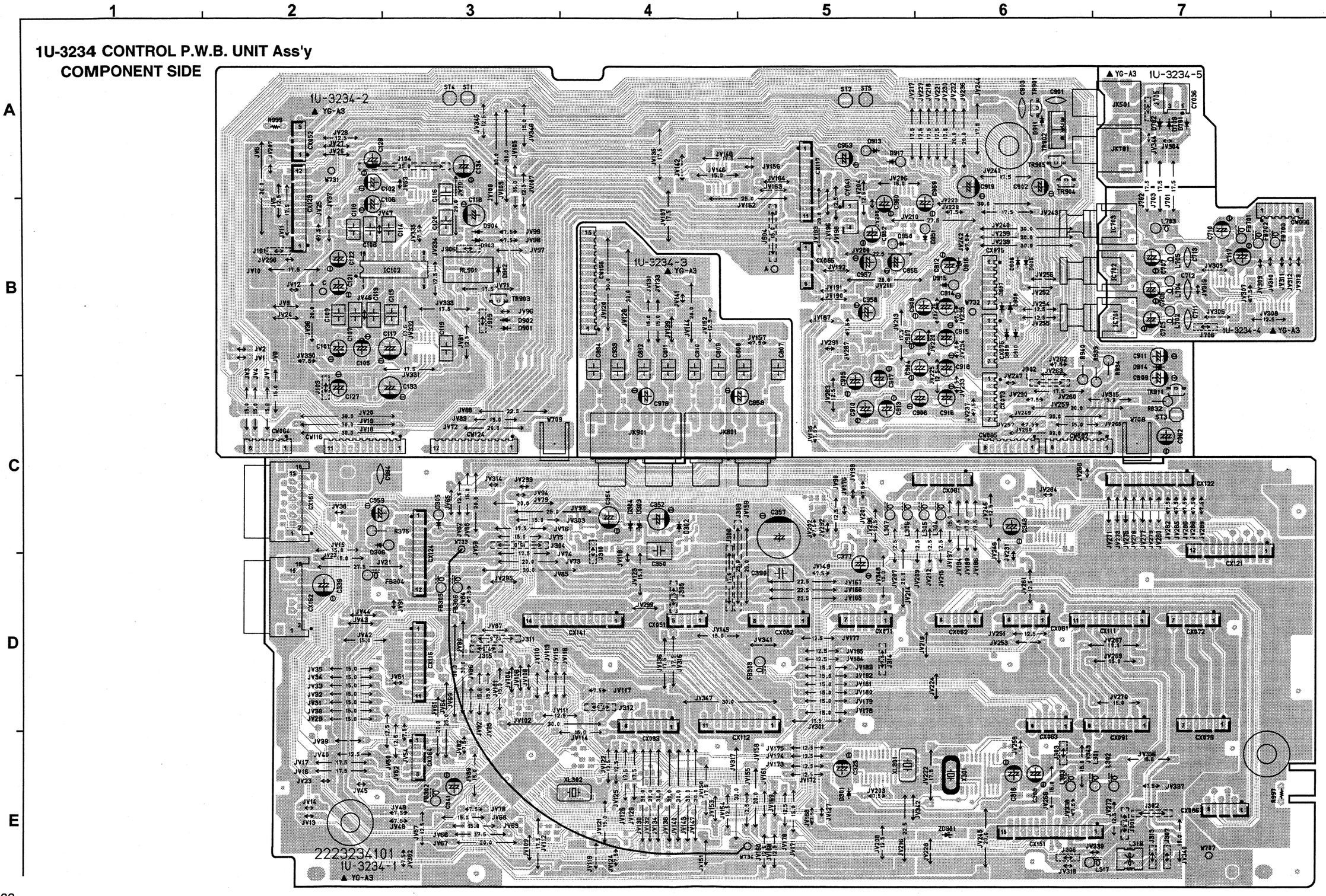
1U-3233 EXT. IN P.W.B. UNIT Ass'y
COMPONENT SIDE



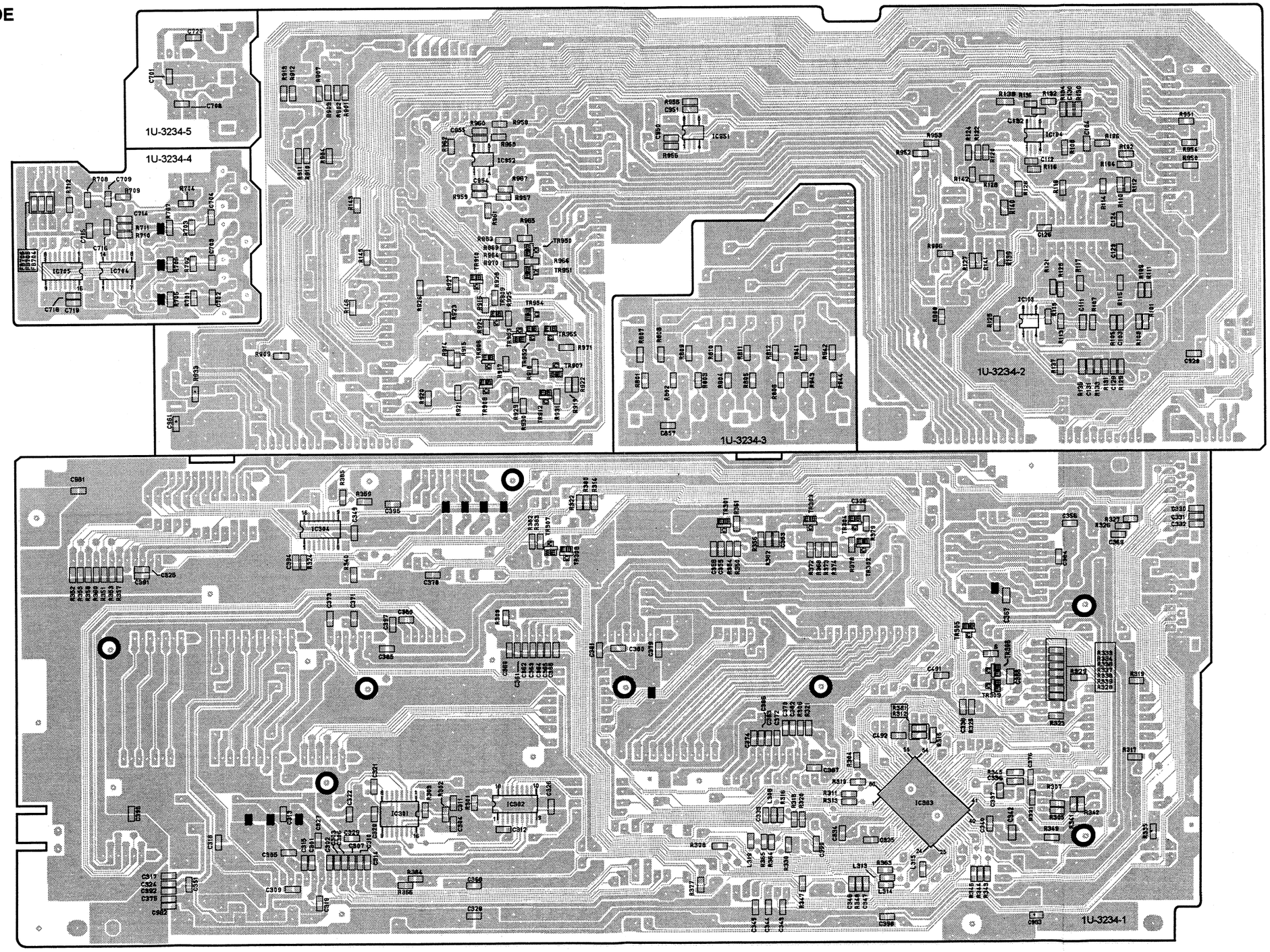
FOIL SIDE



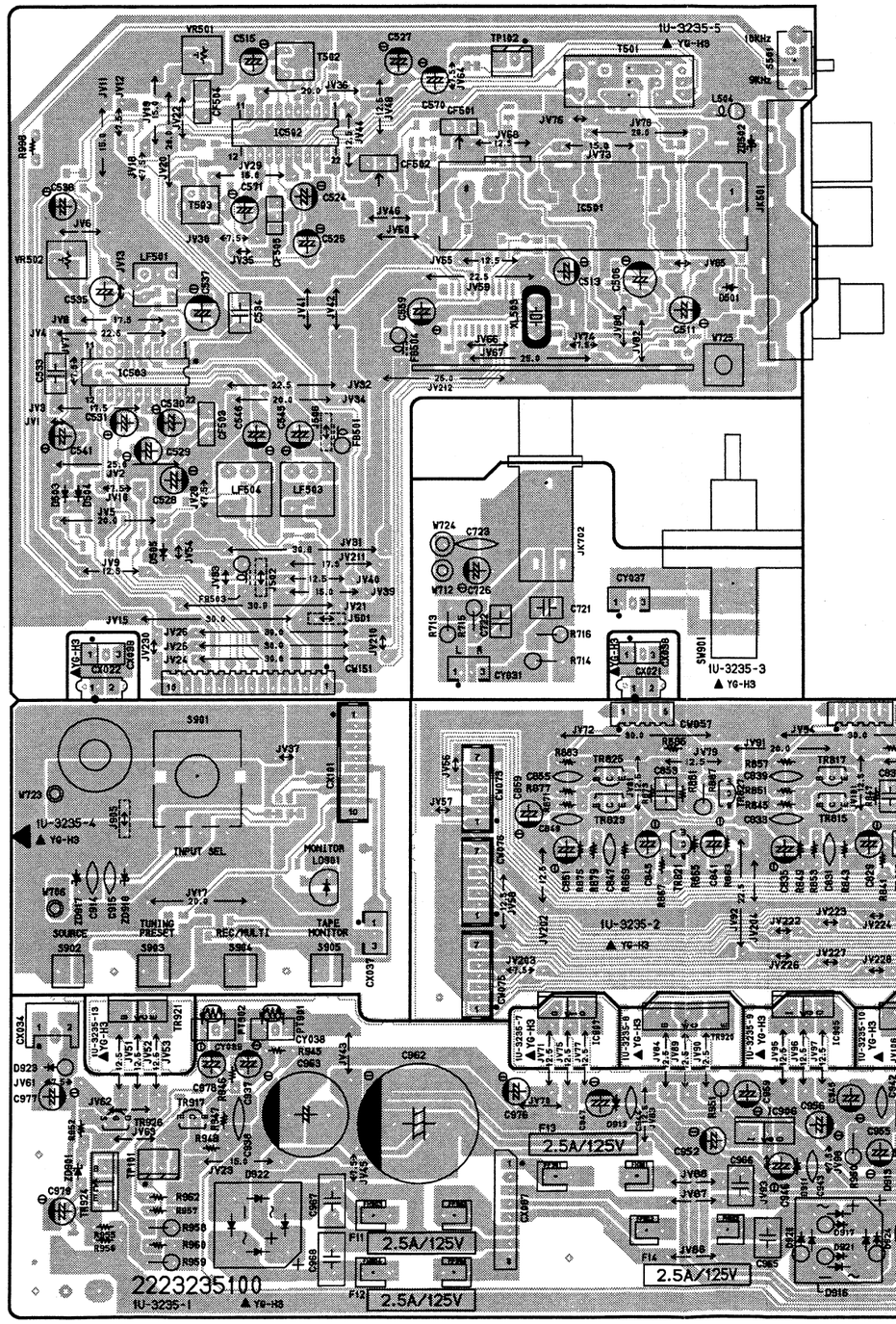
1U-3234 CONTROL P.W.B. UNIT Ass'y
COMPONENT SIDE

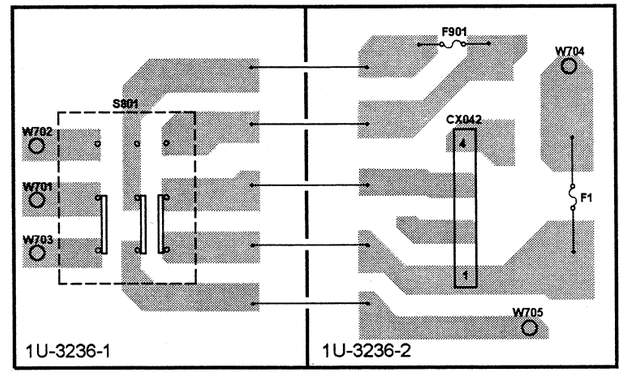


FOIL SIDE



1U-3235 REGULATOR P.W.B. UNIT Ass'y
1U-3236 VOLTAGE SELECT P.W.B. UNIT Ass'y (Asia model & Hong Kong model only)
COMPONENT SIDE

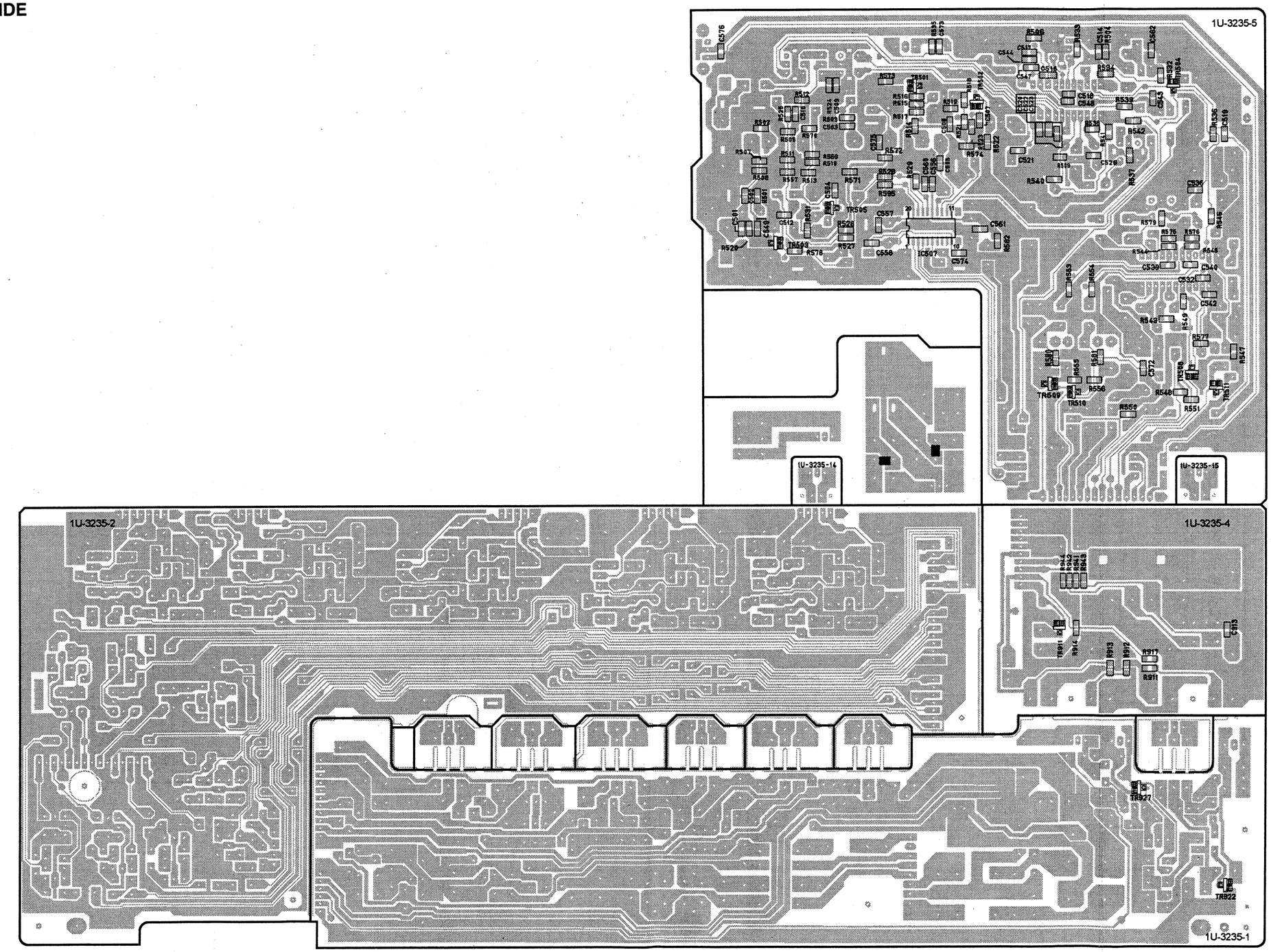




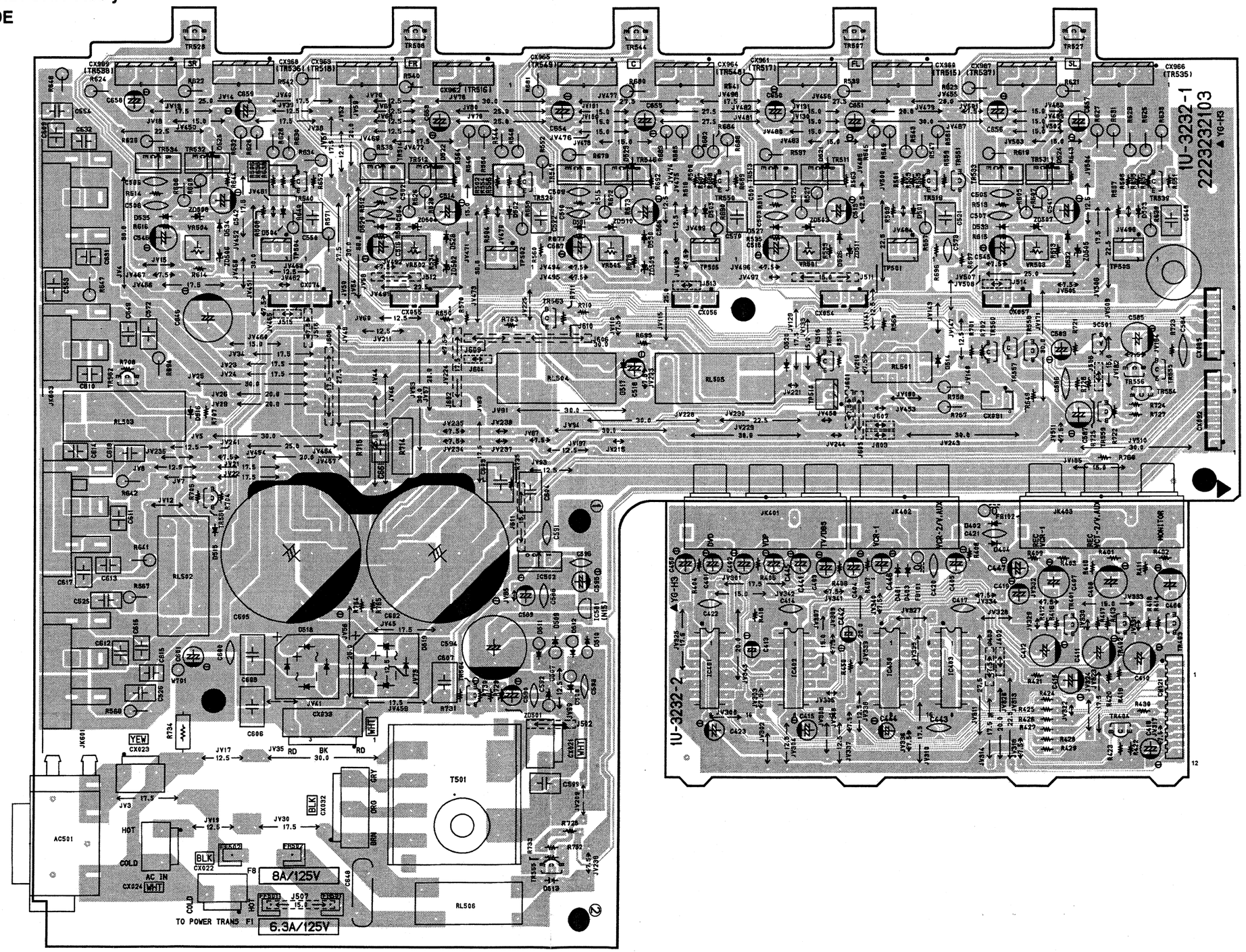
1 2 3 4 5 6 7 8

A B C D E

FOIL SIDE



1U-3232 POWER P.W.B. UNIT Ass'y
COMPONENT SIDE



MEMO: