DENO-00450

DENON

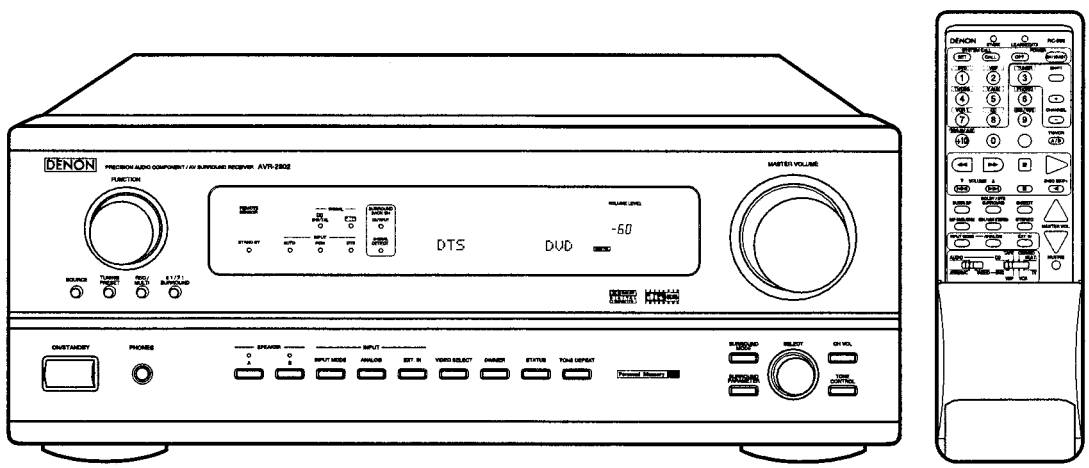
For U.S.A., Canada, Europe, Asia, China, Hong Kong & Taiwan R.O.C. model

Hi-Fi Component

SERVICE MANUAL

MODEL AVR-2802/982

AV SURROUND RECEIVER



● Some illustrations using in this service manual are slightly different from the actual set.

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SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Before returning the unit to the customer, make sure you make either (1) a leakage current check or (2) a line to chassis resistance check. If the leakage current exceeds 0.5 milliamps, or if the resistance from chassis to either side of the power cord is less than 460 kohms, the unit is defective.

SPECIFICATIONS

■ AUDIO SECTION

● Power Amplifier

Rated output:	Front:	90W + 90W (8Ω/ohms, 20Hz ~ 20kHz with 0.05% T.H.D.) 135W + 135W (6Ω/ohms, 1kHz with 0.7% T.H.D.) 150W + 150W (6Ω/ohms, EIAJ)
	Center:	90W (8Ω/ohms, 20Hz ~ 20kHz with 0.05% T.H.D.) 135W (6Ω/ohms, 1kHz with 0.7% T.H.D.) 150W (6Ω/ohms, EIAJ)
	Surround:	90W + 90W (8Ω/ohms, 20Hz ~ 20kHz with 0.05% T.H.D.) 135W + 135W (6Ω/ohms, 1kHz with 0.7% T.H.D.) 150W + 150W (6Ω/ohms, EIAJ)
	Surround Back:	90W (8Ω/ohms, 20 Hz ~ 20kHz with 0.05% T.H.D.) 135W (6Ω/ohms, 1kHz with 0.7% T.H.D.) 150W (6Ω/ohms, EIAJ)
Dynamic power:		120W × 2ch (8Ω/ohms) 170W × 2ch (4Ω/ohms) 200W × 2ch (2Ω/ohms)
Output terminals:	Front:	A or B 6 ~ 16Ω/ohms A + B 8 ~ 16Ω/ohms
		Center, Surround, Surr.Back: 6 ~ 16Ω/ohms

● Analog

Input sensitivity/input impedance:	200mV/47kΩ/kohms
Frequency response:	10Hz ~ 100kHz: +0, –3dB (DIRECT mode)
S/N:	102dB (DIRECT mode)
Distortion:	0.005% (20Hz ~ 20kHz) (DIRECT mode)
Rated output:	1.2V

● Digital

D/A output:	Rated output — 2V (at 0dB playback) Total harmonic distortion — 0.008% (1 kHz, at 0 dB) S/N ratio — 102dB Dynamic range — 96dB
Digital input:	Format — Digital audio interface

● Phono equalizer (PHONO input — REC OUT)

Input sensitivity:	2.5mV
RIAA deviation:	±1dB (20Hz to 20kHz)
Signal-to-noise ratio:	74dB (A weighting, with 5mV input)
Rated output/Maximum output:	150mV/7V
Distortion factor:	0.03% (1kHz, 3V)

■ VIDEO SECTION

● Standard video jacks

Input/output level and impedance:	1Vp-p, 75Ω/ohms
Frequency response:	5Hz ~ 10MHz — +0, –3dB

● S-video jacks

Input/output level and impedance:	Y (brightness) signal — 1Vp-p, 75Ω/ohms C (color) signal — 0.286Vp-p, 75Ω/ohms
Frequency response:	5Hz ~ 10MHz — +0, –3dB

● Color component video jacks

Input/output level and impedance:	Y (brightness) signal — 1Vp-p, 75Ω/ohms PB/CB (blue) signal — 0.7Vp-p, 75Ω/ohms PR/CR (red) signal — 0.7Vp-p, 75Ω/ohms
Frequency response:	5Hz ~27MHz — +0, –3dB

■ TUNER SECTION

	[FM] (note: μV at 75Ω/ohms, 0dBf=1 × 10^{-15} W)	[AM]
Receiving Range:	87.50MHz ~ 107.90MHz (for U.S.A., Canada and multiple voltage models) 87.50MHz ~ 108.00MHz (for Europe, Asia, China, Hong Kong, Taiwan R.O.C. and Multiple voltage models)	520kHz ~ 1710kHz (for U.S.A., Canada and Multiple voltage models) 522kHz ~ 1611kHz (for Europe, Asia, China, Hong Kong, Taiwan R.O.C. and multiple voltage models)
Usable Sensitivity:	1.0μV (11.2dBf)	18μV
50dB Quieting Sensitivity:	MONO: 1.6μV (15.3dBf) STEREO: 23μV (38.5dBf)	
S/N (IHF-A):	MONO: 77dB STEREO: 72dB	
Total Harmonic Distortion (at 1kHz):	MONO: 0.15% STEREO: 0.3%	

■ GENERAL

Power supply:	AC120V, 60Hz (for U.S.A., Canada and Taiwan R.O.C. models) AC230V, 50Hz (for Europe model) AC220V, 50Hz (for China model) AC115V/230V, 50/60Hz (for Asia, Hong Kong and Multiple voltage models)
Power consumption:	5.0A (for U.S.A.& Canada model) 270W (for Europe, Asia, China, Hong Kong and Multiple voltage models) 650W (for Taiwan R.O.C. model) 2.0W Max (Standby)
Maximum external dimensions:	434 (W) × 171 (H) × 416 (D)mm (17-3/32″ × 6-11/32″ × 16-3/8″)
Weight:	11.5kg (25 lbs 6 oz)

■ REMOTE CONTROL UNIT (RC-903: for U.S.A., Canada, Asia, China, Hong Kong, Taiwan R.O.C. and Multiple voltage models) (RC-904: for Europe model)

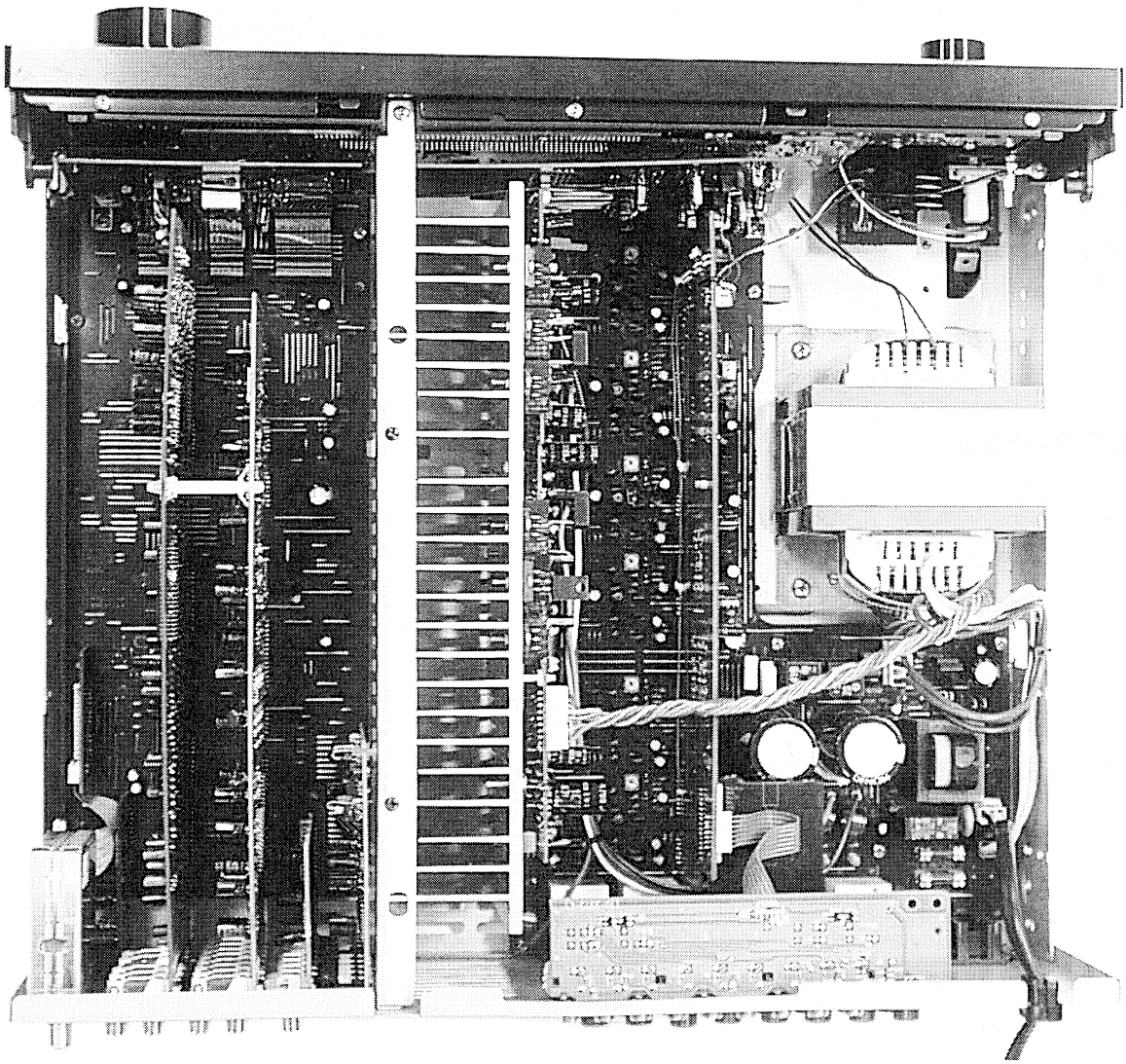
Batteries:	R6P/AA Type (three batteries)
External dimensions:	70 (W) × 215 (H) × 24 (D)mm (2-3/4″ × 8-15/32″ × 15/16″)
Weight:	200g (Approx. 7 oz) (including batteries)

* For purposes of improvement, specifications and design are subject to change without notice.

WIRE ARRANGEMENT

If wire bundles are untied or moved to perform adjustment or parts replacement etc.,be sure to rearrange them neatly as they were originally bundled or placed afterward.
Otherwise, incorrect arrangement can be a cause of noise generation.

Wire arrangement viewed from the top

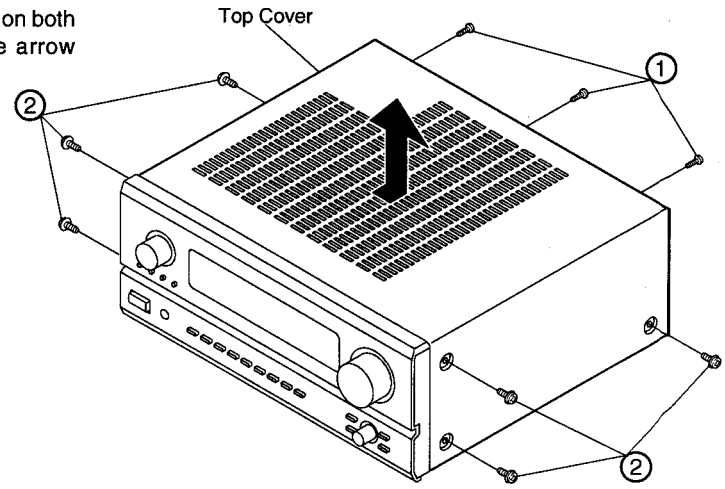


DISASSEMBLY

(Follow the procedure below in reverse order when reassembling)

1. Top Cover

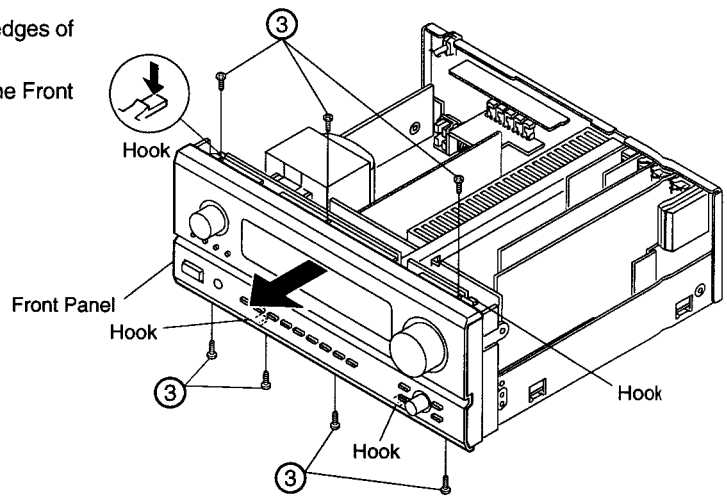
Remove 3 screws ① on the rear and 6 screws ② on both sides to detach the Top Cover as shown in the arrow direction.



2. Front Panel

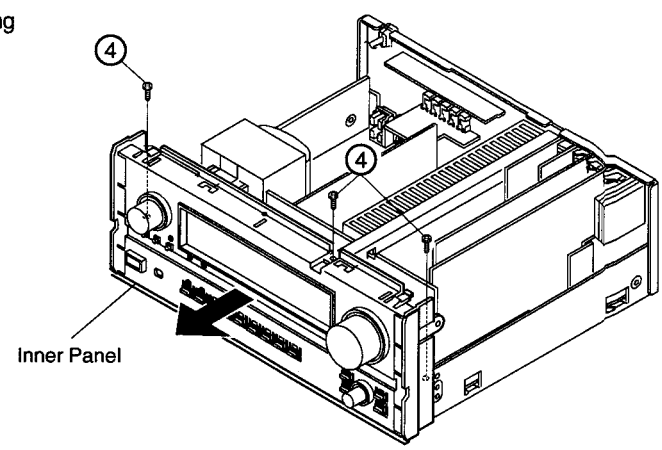
(1) Remove 7 screws ③ from the top and bottom edges of the Front Panel.

(2) Release 4 top and bottom hooks, then detach the Front Panel as shown in the arrow direction.



3. Inner Panel

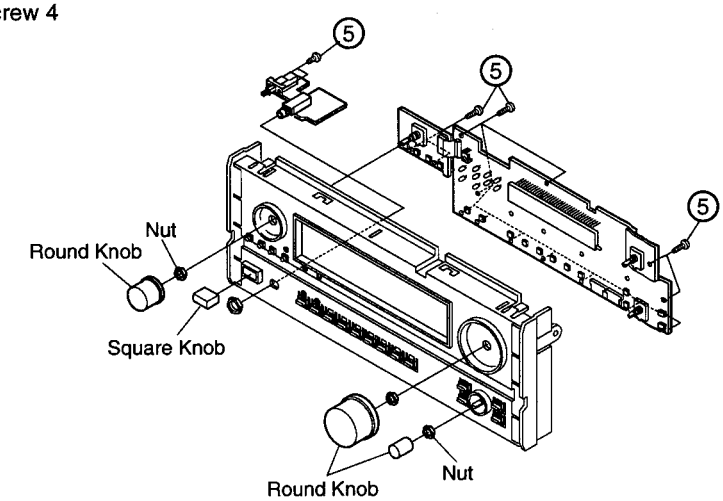
Pull out the Inner Panel in the arrow direction after removing 3 screws ④.



4. Inner Panel Ass'y

(1) Remove 3 round and 1 square knobs, and unscrew 4 nuts.

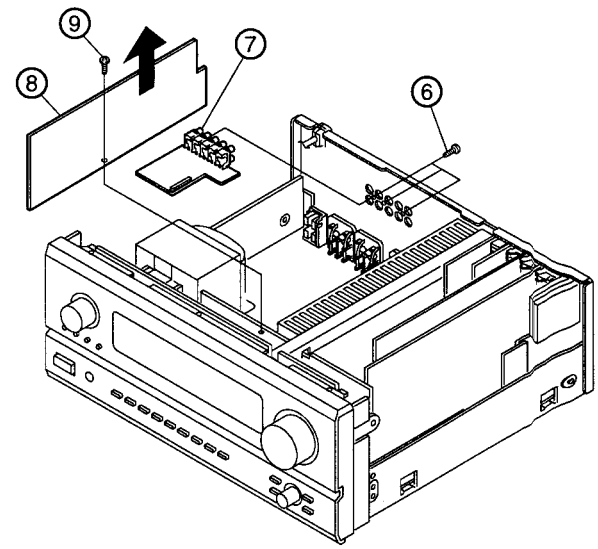
(2) Remove 15 screws (5) fixing each P.W.B.



5. Amp Connect Unit

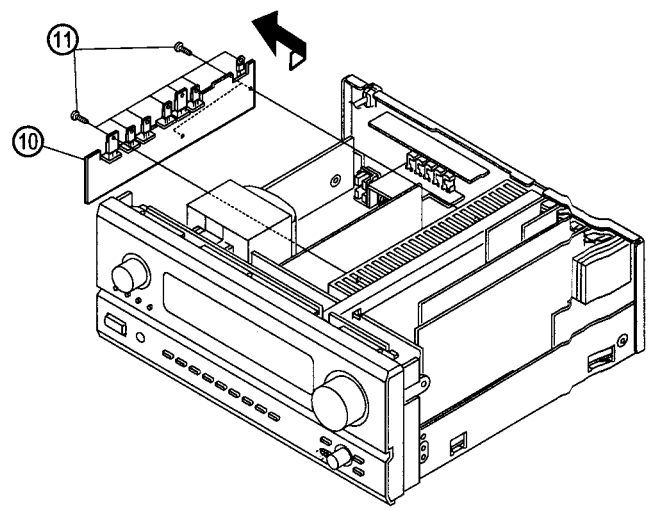
(1) Remove 3 screw (6) to detach Pre-out Unit (7).

(2) Take off the Amp Connect Unit (8) as shown in the arrow direction after removing 1 screw (9).



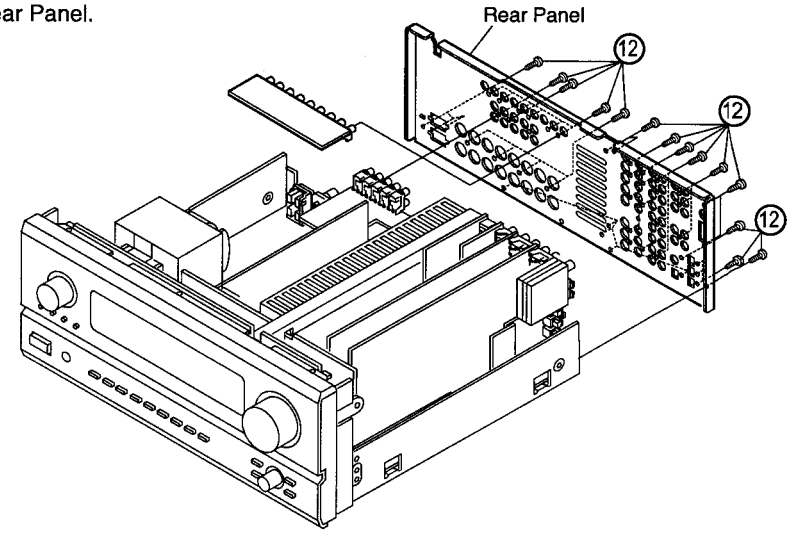
6. Regulator Unit

Take off the Regulator Unit (10) as shown in the arrow direction after removing 9 screws (11).



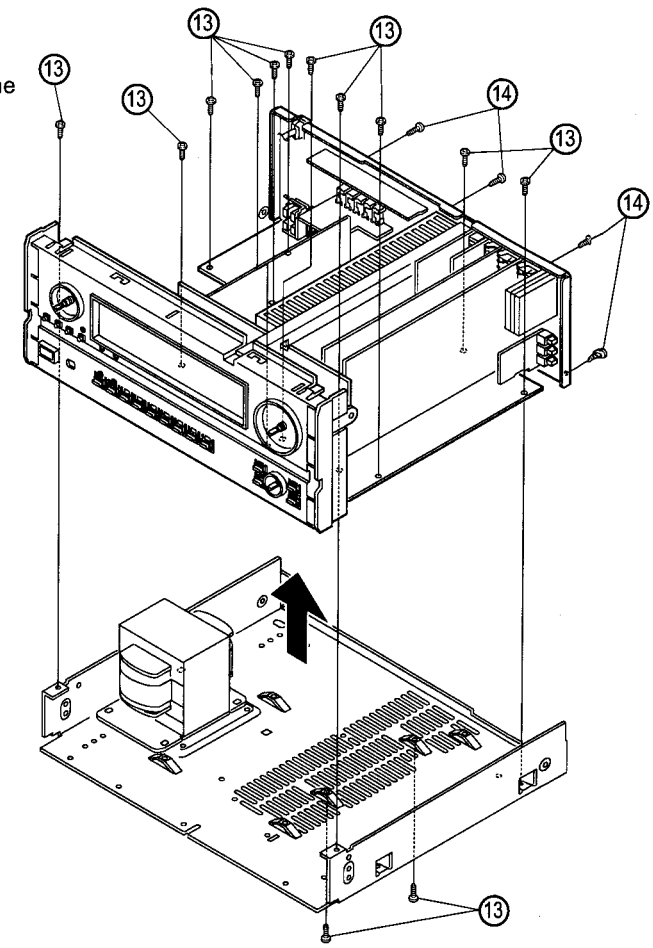
7. Component-Video/S-Video / C-video / Audio & DSP / Ext-in VR / Digital-in / AM FM Tuner Unit

(1) Remove 44 screws ⑫ to detach the Rear Panel.
(2) Take off the objective P.W.B. upward.



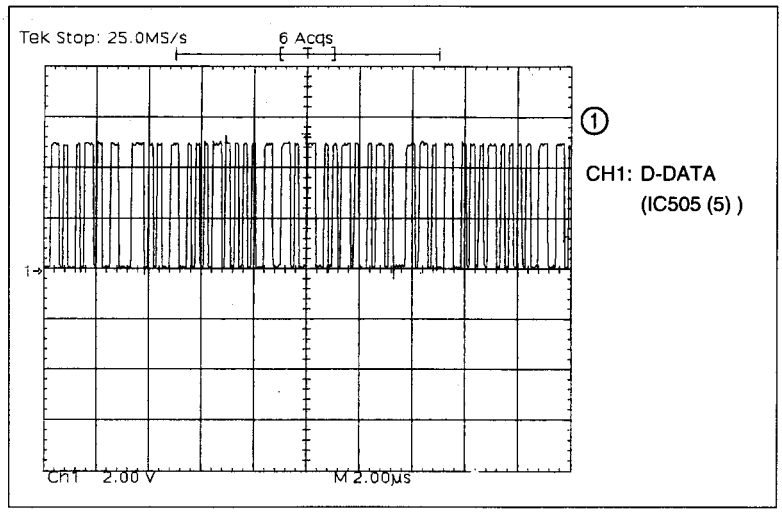
8. How to Check Power / Control Unit with Power-on

(1) Remove 13 screws ⑬,and 4 screws ⑭ fixing to the Chassis.
(2) Pull up the Unit to separate from the Chassis.

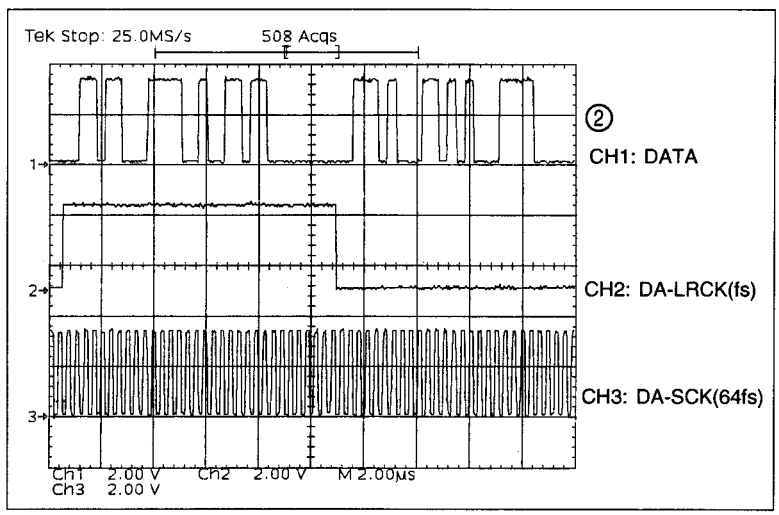


CLOCK FLOW & WAVE FORM IN DIGITAL BLOCK

Wave Form



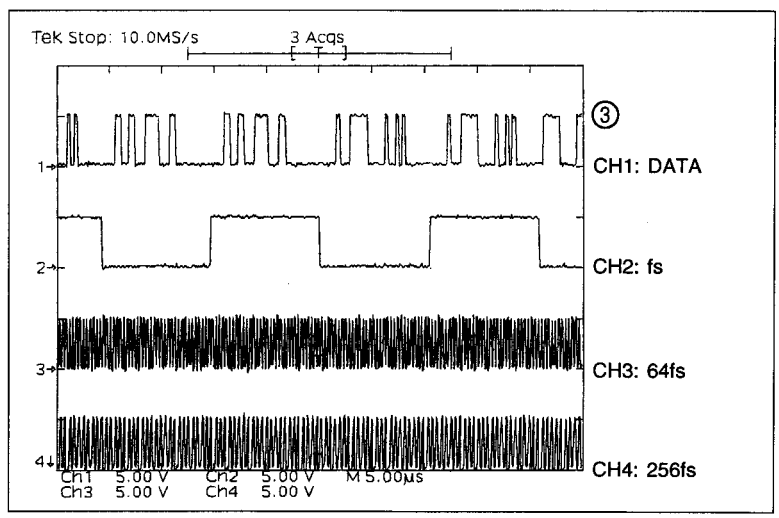
① CH1: D-DATA (IC505 (5))



② CH1: DATA

CH2: DA-LRCK(fs)

CH3: DA-SCK(64fs)



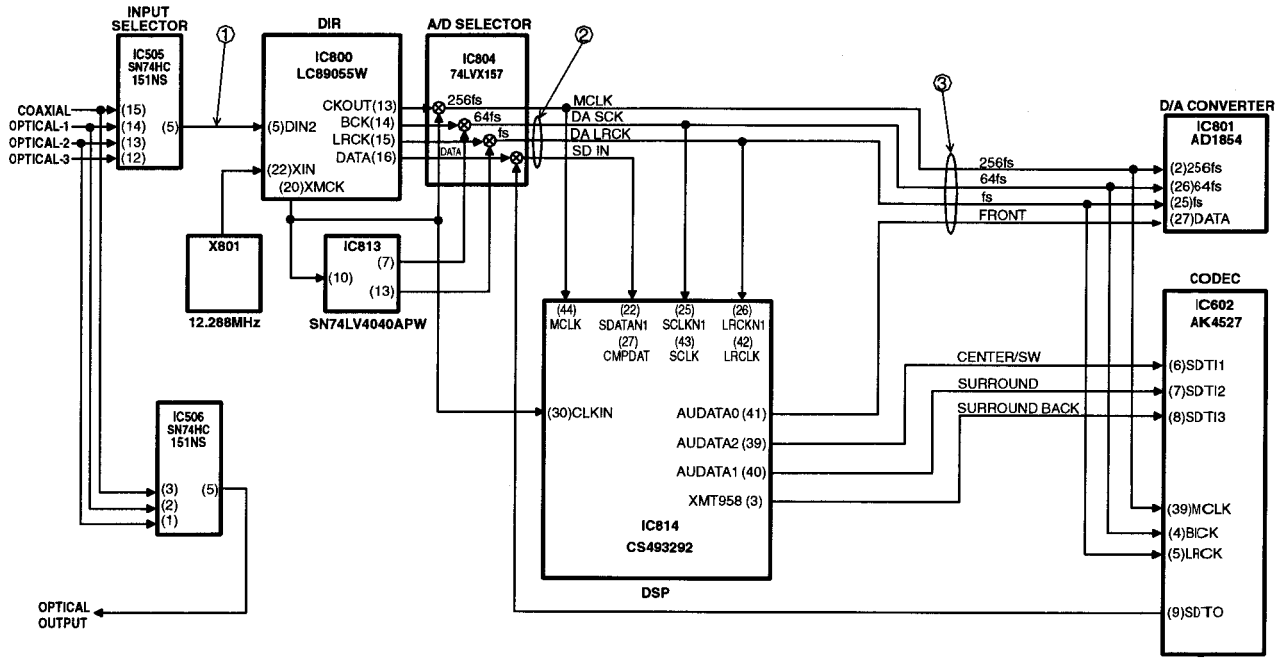
③ CH1: DATA

CH2: fs

CH3: 64fs

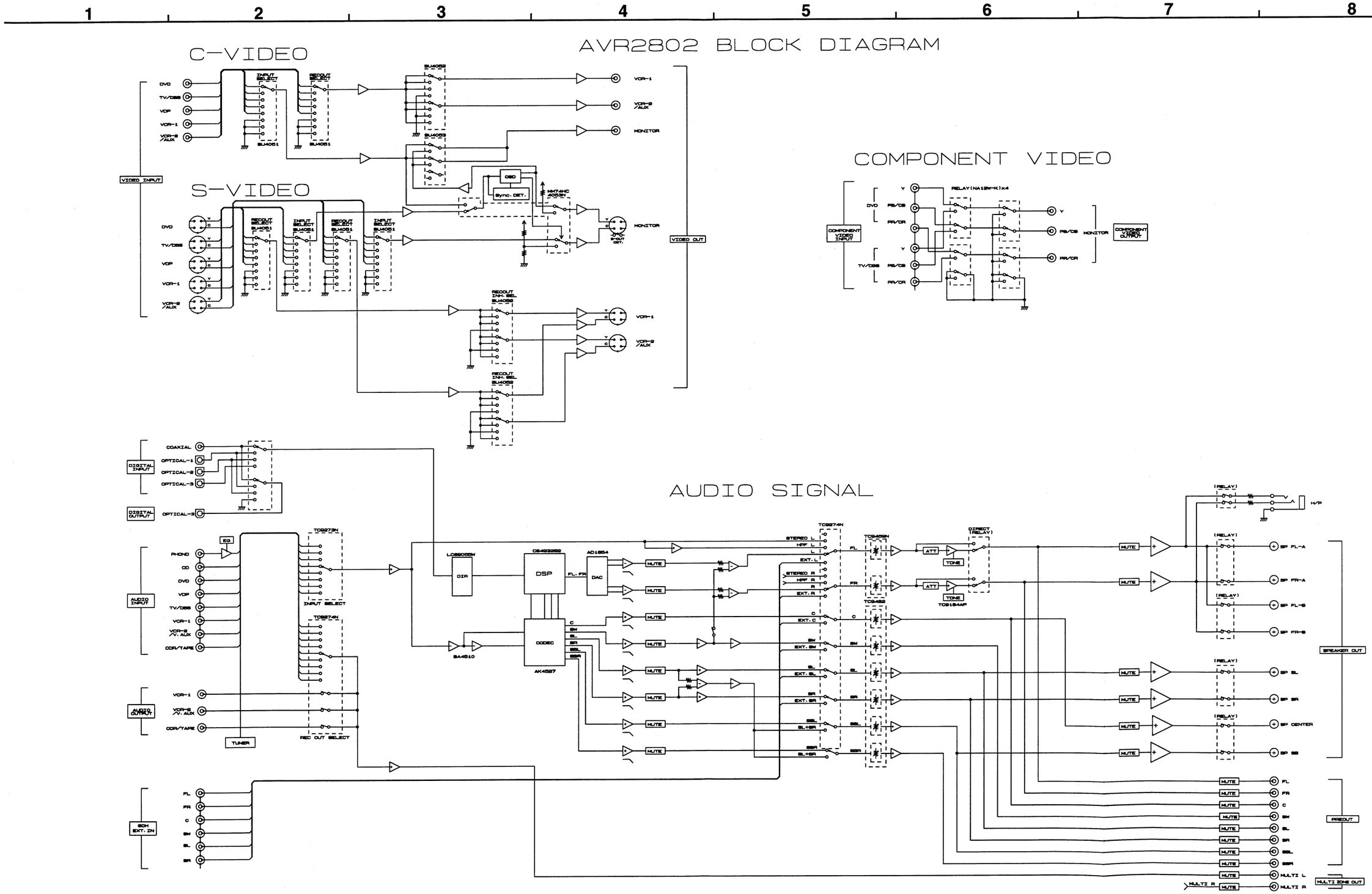
CH4: 256fs

Clock Flow

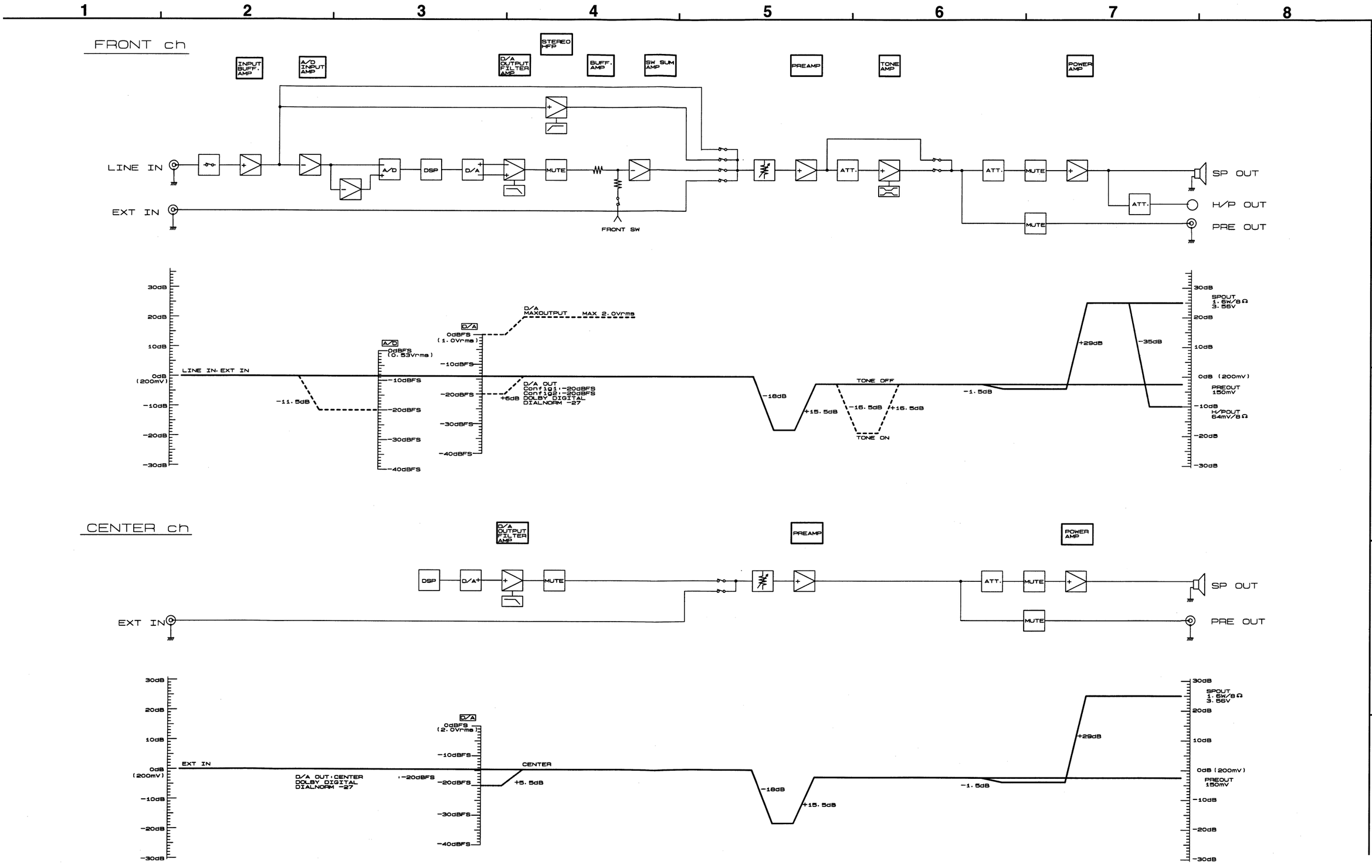


* fs is a sampling frequency of input digital signal.
  e.g.:sampling frequency 48kHz fs=48kHz
* 64fs and 256fs are 64 or 256 times the sampling frequency respectively.
  e.g.: sampling frequency 48kHz
  64fs: 48kHz x 64=3.072MHz
  256fs: 48kHz x 256=12.288MHz
* The sampling frequency for analog input is fixed to 48kHz internally.
* (No.) indicates the pin number of individual.
* The arrow indicates the direction of signal as the input terminal pointed by the arrow and the output terminal by the opposite.

BLOCK DIAGRAM



LEVEL DIAGRAMS (1/3)

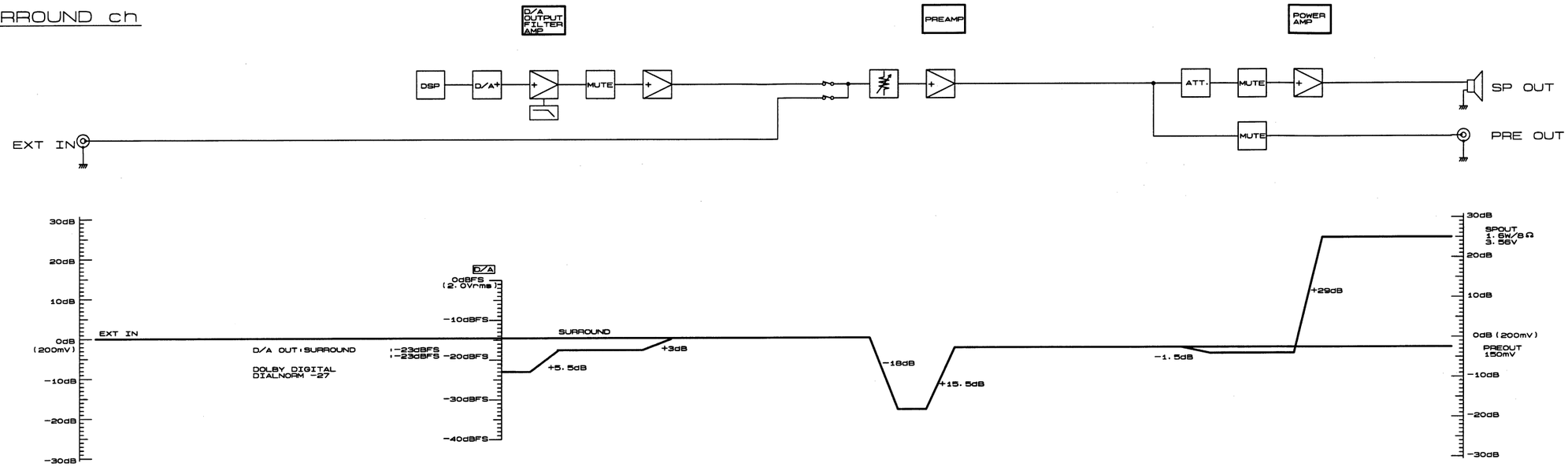


LEVEL DIAGRAMS (2/3)

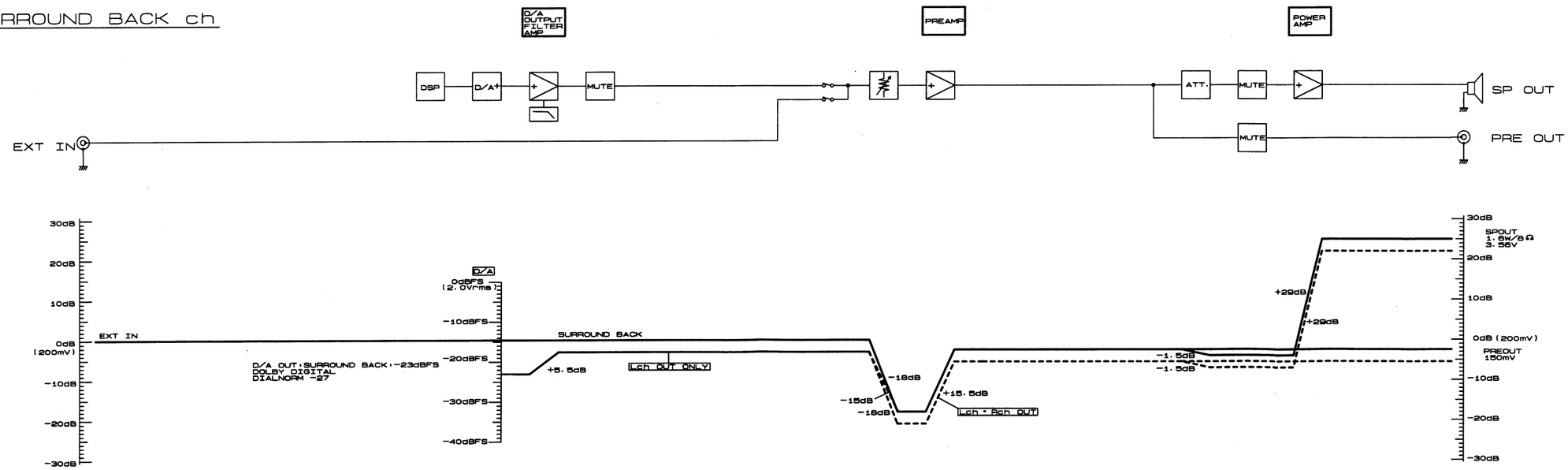
1 2 3 4 5 6 7 8

A B C D E

SURROUND ch



SURROUND BACK ch

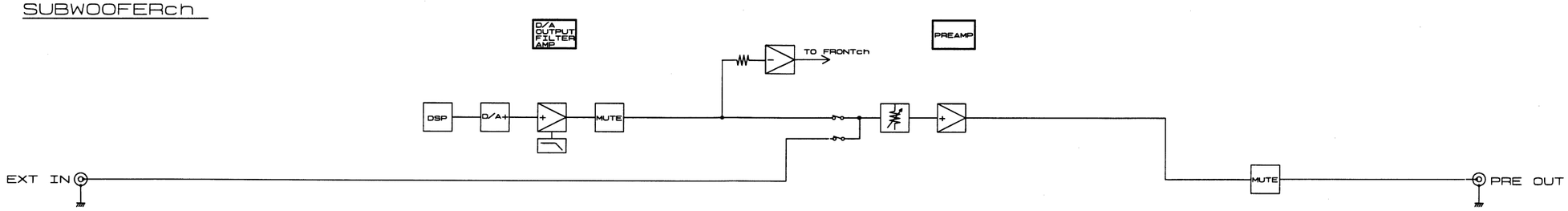


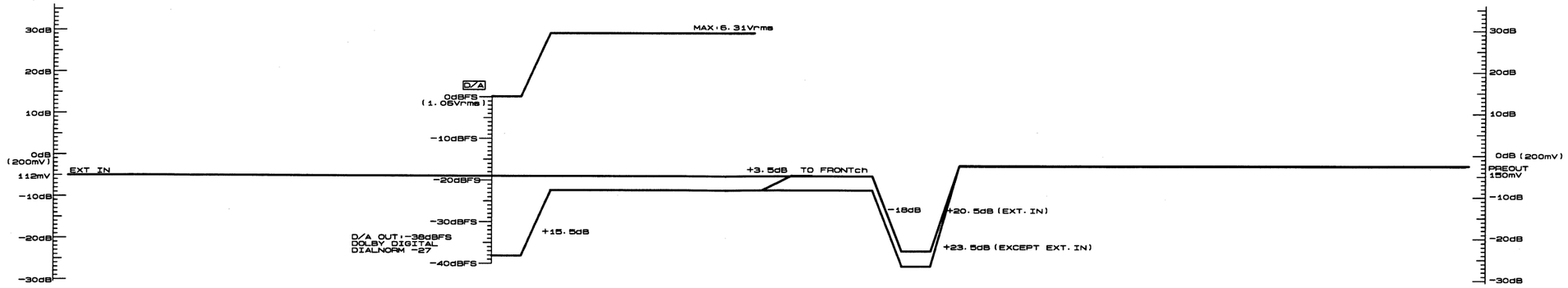
LEVEL DIAGRAMS (3/3)

1 2 3 4 5 6 7 8

A B C D E

SUBWOOFERch



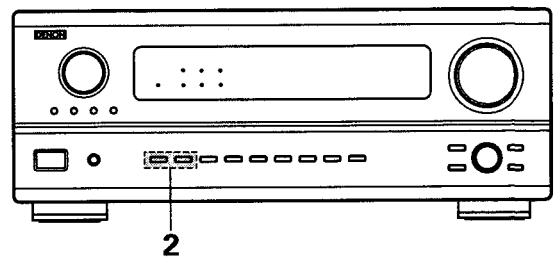


CAUTION IN SERVICING

● Initializing AV SURROUND RECEIVER

AV SURROUND RECEIVER initialization should be performed when the μcom, peripheral parts of μcom, and DSP P.W.B. are replaced.

1. Switch off the unit and remove the AC cord from the wall outlet.
2. Hold the following A button and B button, and plug the AC cord into the outlet.
3. Check that the entire display is flashing with an interval of about 1 second, and release your fingers from the 2 buttons and the microprocessor will be initialized.



Note: • If step 3 does not work, start over from step 1.
• All user settings will be lost and its factory setting will be recovered when this initialization mode. So make sure to memorize your setting for restoring after the initialization.

ADJUSTMENT

Idling Current (1U-3368-1)

Required measurement equipment : DC Voltmeter

Preparation

(1) Avoid direct blow from an air conditioner or an electric fan, and adjust the unit at normal room tempereture 15 °C ~ 30 °C (59 °F ~ 86 °F).

(2) Presetting
- POWER (Power sourse switch) → OFF
- SPEAKER (Speaker terminal) → No load (Do not connect speaker, dummy resistor, etc.)

Adjustment

(1) Remove top cover and set VR101, VR102, VR201, VR202, VR301, VR401, on 1U-3368-1 (Power Unit) at fully counterclockwise (↺).

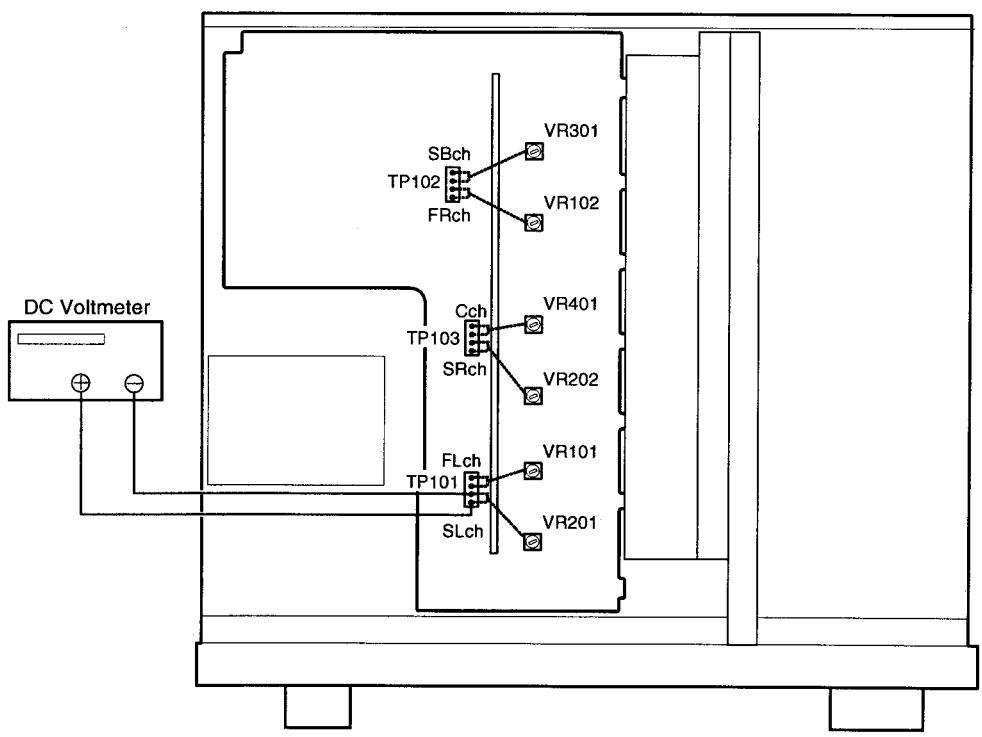
(2) Connect DC Voltmeter to test points (FRONT-Lch: TP101, FRONT-Rch: TP102, CENTER ch: TP103, SURROUND-Lch: TP101, SURROUND-Rch: TP103, SURROUND BACK-ch: TP102).

(3) Connect power cord to AC Line, and turn power switch "ON".

(4) Presetting. MASTER VOLUME : "---" counterclockwise (↺ min.)
MODE : 6CH STEREO
FUNCTION : CD

(5) Allow 2 minutes, and turn VR101 clockwise (↻) to adjust the TEST POINT voltage to 6.5 mV ±0.5 mV DC.

(6) After 10 minutes from preset, turn VR101 to set the voltage to 8 mV ±0.5 mV DC.
(7) Adjust the Variable Resistors of other channels in the same way.
(8) After 5 minutes from (6), turn VR101 to set the voltage to 8 mV ±0.5 mV DC.
(9) Adjust the Variable Resistors of other channels in the same way.



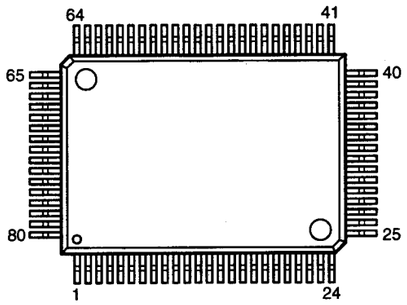
SEMICONDUCTORS

● IC's

Note: Abbreviation ahead of IC No. indicates the name of P.W.B.

PO: Power P.W.B. RE: Regulator P.W.B.
EX: Exit in P.W.B. AU: Audio/DSP P.W.B.
CO: Control P.W.B.

TMP88CU74F
(CO: IC303)



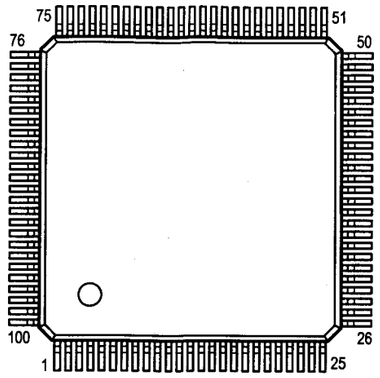
TMP88CU74F Terminal Function

Pin No.	Name	Symbol	I/O	Type	Op	Det	Res	Init	Function
1	P02/S01	RDS RESET	O	C	—	—	Z	L	RDS reset output (LC72720)
2	P03	OSD RST	O	C	—	—	Z	H	OSD control output (M35015)
3	P04	PLL DATA	I	—	—	—	—	—	PLL Serial data input terminal (LC72131)
4	P05	PLFLRDS DATA	O	C	—	—	Z	L	PLL, FL, RDS control terminal (LC72131 & LC75721, LC72720)
5	P06	PLL STB	O	C	—	—	Z	L	PLL control terminal (LC72131)
6	P07	PLFLRDS CLK	O	C	—	—	Z	L	PLL, FL, RDS control terminal (LC72131 & LC75721, LC72720)
7	Vss	Vss	I	—	GND	—	—	L	GND
8	Xout	Xout	O	—	—	—	—	—	XTAL
9	Xin	Xin	I	—	—	—	—	—	XTAL
10	RESET_	RESET_	I	—	Eu	Lv	L	—	Reset input
11	P22/XTOUT	TUNED_	I	—	Eu	Lv	Z	—	Tuning detect, L: Tuned
12	P21/XTIN	STEREO_	I	—	Eu	Lv	Z	—	L: At stereo receive
13	TEST	TEST	I	—	GND	S	—	—	Connect to GND
14	P20/INT5_	B.DOWN_	I	—	Eu	Lv	Z	—	Power down detect, L: Power down
15	P10/INT0_	PROTECT_	I	—	Ed	E&L	Z	—	PROTECTION detect input, H: Detect
16	P11/INT1	RDS DATA	I	—	—	—	Z	L	RDS data input (LC72720)
17	P12	OSD CLK	O	C	—	—	Z	H	OSD control output (M35015)
18	P13	OSD CS	O	C	—	—	Z	H	OSD control output (M35015)
19	P14	OSD DATA	O	C	—	—	Z	L	OSD control output (M35015)
20	P15/INT3	REMOCON	I	—	Ed	E&L	Z	—	Remote control signal input
21	P16/INT2	ACK	O	C	—	—	Z	L	MAIN-SUB CPU comm. control terminal
22	P17/INT4	REQ	I	—	Eu	—	Z	L	MAIN-SUB CPU comm. control terminal
23	P30/SCL	SI	I						MAIN-SUB CPU comm. control terminal
24	P31/SDA	SO	O	C					MAIN-SUB CPU comm. control terminal
25	P32/SCK0_	CLK	O	C					MAIN-SUB CPU comm. control terminal
26	P40/AIN0	MODE	I	—	Eu	Lv	Z	—	Destination switching input
27	P41/AIN1	KEY1	I	—	Eu	Lv	Z	—	Button input 1
28	P42/AIN2	KEY2	I	—	Eu	Lv	Z	—	Button input 2
29	P43/AIN3	KEY3	I	—	Eu	Lv	Z	—	Button input 3
30	P44/AIN4	FUNC STB1	O	C	—	—	Z	L	Function control output, REC OUT (TC9274-011), EXT/SOURCE (TC9274-017)
31	P45/AIN5	FUNC/T. CON CLK	O	C	—	—	Z	L	Function control output (TC9274N, TC9273), TONE control output (TC9184P)
32	P46/AIN6	FUNC/T. CON DATA	O	C	—	—	Z	L	Function control output (TC9274N, TC9273), TONE control output (TC9184P)
33	P47/AIN7	E.VOL STB4	O	C	—	—	Z	L	Elect. volume control output (TC9482)
34	P50/AIN8	E.VOL STB1	O	C	—	—	L	L	Elect. volume control output (TC9459)
35	P51/AIN9	TONE STB	O	C	—	—	L	L	TONE control output (TC9184P)
36	P52/AIN10	E.VOL DATA	O	C	—	—	L	H	Elect. volume control output (TC9459, TC9482)
37	P53/AIN11	E.VOL CLK	O	C	—	—	L	H	Elect. volume control output (TC9459, TC9482)
38	VASS	VASS	I						Ref. volt (GND)
39	VAREF	VAREF	I						Ref. volt (VDD)
40	VDD	VDD	I						Power supply
41	P60	FL CE	O	P	Ed	S	L	H	FL display control output (LC75721NE)
42	P61	FL RES	O	P	Ed	S	L	H	FL display control output (LC75721NE)
43	P62	FUNC STB2	O	P	Ed	—	Z	L	Function control output (TC9273), INPUT (TC9273)
44	P63	FA-RELAY	O	P	Id	—	L	L	Front SP relay A control terminal, L: Mute
45	P64	FB-RELAY	O	P	Id	—	L	L	Front SP relay B control terminal, L: Mute
46	P65	C-RELAY	O	P	Id	—	L	L	Center SP relay control terminal, L: Mute
47	P66	S-RELAY	O	P	Id	—	L	H	Surround SP relay control terminal, L: Mute
48	P67	PRE F MUTE	O	P	Ed	—	L	H	Front PRE OUT mute control terminal, L: Mute
49	P70	PRE C MUTE	O	P	Ed	—	L	L	Center PRE OUT mute control terminal, L: Mute
50	P71	PRE S MUTE	O	P	Ed	—	L	L	Surround PRE OUT mute control terminal, L: Mute
51	P72	SUB WOOFER MUTE	O	P	Ed	—	L	H	Sub-woofer PRE OUT mute control terminal, L: Mute
52	P73	H/P RELAY	O	P	Id	—	L	H	H/P OUT relay control terminal, L: Mute
53	P74	EXP OE	O	P	Ed	—	L	H	Port expander control terminal (BU4094)
54	P75	EXP CLK	O	P	Ed	—	L	L	Port expander control terminal (BU4094)
55	P76	EXP DATA	O	P	Ed	—	L	L	Port expander control terminal (BU4094)
56	P77	EXP STB	O	P	Ed	—	L	L	Port expander control terminal (BU4094)
57	P80	POWER	O	P	Id	—	L	H	Power relay control output, H: ON
58	P81	RESET2	O	P	Id	—	L	L	Reset signal output to sub-CPU, H: Reset
59	P82	PRE S.BACK MUTE	O	P	Id	—	L	L	Surround Back PRE PUT mute control terminal, L: Mute
60	P83	S.BACK VOL MUTE	O	P	Id	—	L	L	Surround Back volume mute, L: Mute
61	P84	STANDBY	O	P	Id	—	L	H	Standby LED drive output H: Light
62	P85	S.BACK RELAY	O	P	Id	—	L	L	Surround Back SP relay control terminal, L: Mute
63	P86	LED CK	O	P	Id	—	L	L	LED control terminal (BU2090F)
64	P87	LED DATA	O	P	Id	—	L	L	LED control terminal (BU2090F)
65	P90	TUNER MUTE	O	P	Ed	—	L	H	TUNER mute control terminal, L: Mute
66	P91	MULTI MUTE	O	P	Id	—	L	H	MULTI PREOUT mute control terminal, L: Mute
67	P92	S MONI DET	I	—	Eu	Lv	Z	—	S monitor connection detect input, L: Connected
68	P93	S SIG DET	I	—	Eu	Lv	Z	—	S signal detect input, H: Detected
69	P94	SYNC DET.	I	—	Eu	Lv	Z	—	Sync detect input, H: Ext. sync
70	P95	SEL A (M)	I	—	Eu	Lv	Z	—	Master volume rotation detect input (rotary encoder)
71	P96	SEL B (M)	I	—	Eu	Lv	Z	—	Master volume rotation detect input (rotary encoder)
72	P97	CINEMA EQ	O	P	Eu	Lv	Z	L	CINEMA EQ control output, H: ON
73	PD0	VOL MUTE	O	P	Ed	—	L	L	Master volume minimum control, L: Min.
74	PD1	SEL C (S)	I	—	Eu	Lv	Z	—	Surround mode rotation detect input (rotary encoder)
75	PD2	SEL D (S)	I	—	Eu	Lv	Z	—	Surround mode rotation detect input (rotary encoder)
76	PD3	SEL E (F)	I	—	Eu	Lv	Z	—	Input selector switch rotation detect input (rotary encoder)
77	PD4	SEL F (F)	I	—	Eu	Lv	Z	—	Input selector switch rotation detect input (rotary encoder)
78	Vkk	Vkk	—	—	—	—	—	—	GND fixed
79	P00/SCK1_		O	C	—	—	Z	L	
80	P01/SI1	RDS CE	O	C	—	—	Z	L	RDS data output (LC72720)

NOTE:

Pin No. : Terminal number of microcomputer.
Port Name : The name entered in the data sheet of microcomputer.
Symbol : Symbolized interface function.
I/O : Input or out of part.
"I" = Input port
"O" = Output port
Type : Composition of port in case of output port.
"C" = CMOS output
"N" = NMOS open drain output
"P" = PMOS open drain output
Op : Pull up/Pull down selection information.
"Iu" = Inner microcomputer pull up
"Id" = Inner microcomputer pull down
"Eu" = External microcomputer pull up
"Ed" = External microcomputer pull down
Det : Indicates judging state of input port. Level detection is "LV"; Edge detection is "Ed";
Detection by both shifting is "E&L"; Serial data detection is "S" (Serial data output is also "S").
Res : State at reset.
"H" = Outputs High Level at reset
"L" = Outputs Low Level at reset
"Z" = Becomes High impedance mode at reset
Ini : Initial output state.
Function : Function and logical level explanation of signals to be interface.

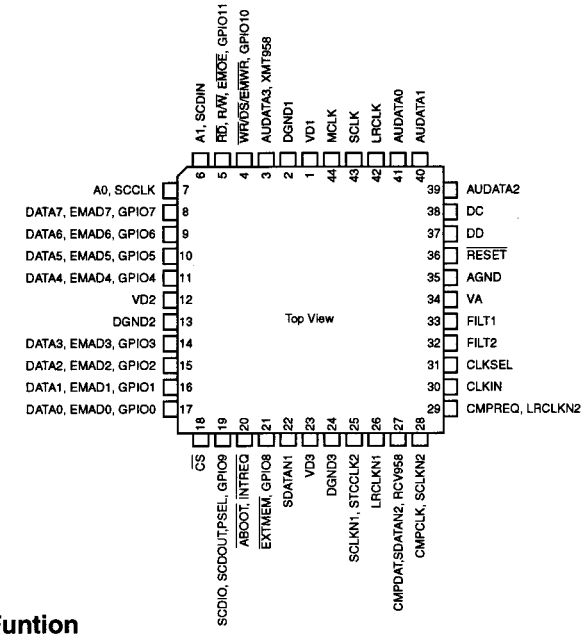
TMP93CS40F (AU: IC301)



TMP93CS40F Terminal Function

Pin No.	Name	Symbol	I/O	Type	Op	Det	Res	Init	Function
1	V REFL		—	—	—	—	—	—	A/D ref. GND
2	A Vss	←	—	—	—	—	—	—	A/D GND
3	A Vcc	←	—	—	—	—	—	—	AD +5V
4	_NMI		I	—	—	—	—	—	Not used (fixed to H)
5	P70/TI0	C15	O	C	Ed	—	L	L	Fixed to L (DSP ROM address cont. out bit 15, not used)
6	P71/TO1	C16	O	C	Ed	—	L	L	DSP program ROM address cont. out bit 16
7	P72/TO2	C17	O	C	Ed	—	L	L	DSP program ROM address cont. out bit 17
8	P73/TO3	ROM/RAM	O	C	Ed	—	L	L	ROM/RAM switching control terminal (L:ROM)
9	P80/INT4/TI4	_INTREQ OUT	I/O	C	Eu	E↓&L	Z	—	DSP request input and cont. output (L:Rq & cont.)
10	P81/INT5/TI5	B.DOWN	I	—	Eu	E↑&L	Z	—	Power down detect (H: Detected)
11	P82/TO4		O	C	—	—	L	L	
12	P83/TO5	_REQ	O	C	Eu	—	H	L	MAIN-SUB CPU comm. control output (L: Comm. request from sub)
13	P84/INT6/TI6	_ACK	I	—	Eu	E↓&L	—	—	MAIN-SUB CPU comm. control input (L: Ack. return from main)
14	P85/INT7/TI7	ERR	I	—	—	E↑&L	—	—	DIR control input terminal (LC89055Q)(H: ERR)
15	P86/TO6		I	—	—	Lv	Z	—	(GND)
16	P97/INT0	_CS	I	—	Ed	E↑&L	—	—	DIR control input terminal (LC89055Q), when CH status change L→H
17	P90/TXD0	SI	O	C					MAIN-SUB CPU comm. control terminal (data output)
18	P91/RXD0	SO	I	—					MAIN-SUB CPU comm. control terminal (data input)
19	P92/_CTS0/SCLK0	CLK	I/O	C					MAIN-SUB CPU comm. control terminal (I2C clock in/output)
20	P93/TXD1		O	C	—	—	Z	L	
21	P94/RXD1		O	C	—	—	Z	L	
22	P95/SCLK1		O	C	—	—	Z	L	
23	AM8/_16	←	—	—	—	—	—	—	Fixed to +5V
24	CLK		O	C	Eu	—	—	—	
25	Vcc	←	—	—	—	—	—	—	+5V
26	Vss	I/O1	—	—	—	—	—	—	GND
27	X1	Xin	I	—	—	—	—	—	X'tal connection
28	X2	Xout	O	—	—	—	—	—	X'tal connection
29	_EA	←	—	—	—	—	—	—	Fixed to +5V
30	_RESET	RESET2_	I	—	Eu	Lv	L	—	Reset input (controlled by main CPU)
31	P96/XT1	A/D RESET	O	N	Eu	—	H	H	A/D control terminal (L: Reset)
32	P97/XT2		O	C	Ed	—	L	L	
33	TEST1	←	I	—	—	—	—	—	Connected to TEST2
34	TEST2	←	I	—	—	—	—	—	Connected to TEST1
35	PA0	DINA	O	C	Ed	—	L	L	Digital input switching control output
36	PA1	DINB	O	C	Ed	—	L	L	Digital input switching control output
37	PA2		O	C	—	—	L	L	
38	PA3	DINC	O	C	Ed	—	L	L	Digital input switching control output
39	PA4	DOUTA	O	C	Ed	—	L	L	Digital output switching control output
40	PA5	DOUTB	O	C	Ed	—	L	L	Digital output switching control output
41	PA6	DEEMP	O	C	Ed	—	L	L	DAC de-emphasis filter cont. out terminal (H:ON)
42	PA7/SCOUT	96k-DAC	O	C	—	—	L	L	DAC control terminal (H: Sample frequency 96kHz)
43	ALE		O	C	—	—	L	L	(Address latch enable)
44	Vcc		—	—	—	—	—	—	+5V
45	P00/AD0	(AD0)	I/O	C	—	—	Z	L	(EPROM data in D0 / address out A0)
46	P01/AD1	(AD1))	I/O	C	—	—	Z	L	(EPROM data in D1 / address out A1)
47	P02/AD2	(AD2)	I/O	C	—	—	Z	L	(EPROM data in D2 / address out A2)
48	P03/AD3	(AD3)	I/O	C	—	—	Z	L	(EPROM data in D3 / address out A3)
49	P04/AD4	(AD4)	I/O	C	—	—	Z	L	(EPROM data in D4 / address out A4)
50	P05/AD5	(AD5)	I/O	C	—	—	Z	L	(EPROM data in D5 / address out A5)
51	P06/AD6	(AD6)	I/O	C	—	—	Z	L	(EPROM data in D6 / address out A6)
52	P07/AD7	(AD7)	I/O	C	—	—	Z	L	(EPROM data in D7 / address out A7)
53	P10/AD8/A8	(A8)	O	C	—	—	Z	L	(EPROM address out A8)
54	P11/AD9/A9	(A9)	O	C	—	—	Z	L	(EPROM address out A9)
55	P12/AD10/A10	(A10)	O	C	—	—	Z	L	(EPROM address out A10)
56	P13/AD11/A11	(A11)	O	C	—	—	Z	L	(EPROM address out A11)
57	P14/AD12/A12	(A12)	O	C	—	—	Z	L	(EPROM address out A12)
58	P15/AD13/A13	(A13)	O	C	—	—	Z	L	(EPROM address out A13)
59	P16/AD14/A14	(A14)	O	C	—	—	Z	L	(EPROM address out A14)
60	P17/AD15/A15	(A15)	O	C	—	—	Z	L	(EPROM address out A15)
61	_WDTOUT	←	O	C	—	—	Z	H	Watch dog output
62	Vss	←	—	—	—	—	—	—	GND
63	Vcc	←	—	—	—	—	—	—	+5V
64	P20/A0/A16	(A16)	O	C	—	—	Z	L	(EPROM address out A16)
65	P21/A1/A17	DIR CLK	O	C	—	—	Z	L	DIR control terminal (LC89055Q) control clock output
66	P22/A2/A18	DIR CE	O	C	—	—	Z	L	DIR control terminal (LC89055Q) control chip enable output
67	P23/A3/A19	DIR MOSI	O	C	—	—	Z	L	DIR control terminal (LC89055Q) control data output
68	P24/A4/A20	DIR MOSO	I	—	—	Lv	—	—	DIR control terminal (LC89055Q) control data input
69	P25/A5/A21	FGAIN	O	C	Ed	—	L	L	FRONT ch GAIN switching control output (H: SW=NO)
70	P26/A6/A22	DAC-RESET	O	C	Ed	—	L	H	DAC control terminal (L: Power down mode, ↑(rising edge) Reset)
71	P27/A7/A23	SEL CK	O	C	—	—	Z	L	ADC/DIR data clock switching control terminal (L: ADC)
72	P30/_RD	(_RD)	O	C	—	—	Z	L	(Flash memory control terminal)
73	P31/_WR	(_WR)	O	C	—	—	Z	L	(Flash memory control terminal)
74	P32/_HWR	CSI	I	—	—	Lv	—	—	DIR control input terminal (L: PCM)
75	P33/_WAIT	ERR MUTE_	O	C	Ed	—	L	L	Pop noise preventive mute control output (L: Mute)
76	P34/_BUSRQ		I	—	—	Lv	Z	—	GND
77	P35/_BUSRQ	DIG.(AC3) MUTE	O	C	Ed	—	Z	L	Digital mute control output (L: AC-3 or DTS decode enable)
78	P36/_R/W		I	—	—	Lv	Z	—	GND
79	P37/_RAS	DIR RESET	O	C	—	—	Z	L	DIR control output (LC89055Q) (L: Reset)
80	P40/_CS0/_CAS0		O	C	—	—	Z	L	
81	P41/_CS1/_CAS1		O	C	—	—	Z	L	
82	P42/_CS2/_CAS2	(_CS0)	O	C	—	—	Z	L	(Flash memory control terminal)
83	P60/PG00	DSP. RESET	O	C	—	—	Z	L	DSP reset output terminal (L:Reset)
84	P61/PG01	I/02 SCD OUT	I	C	—	Lv	Z	—	DSP status data input terminal
85	P62/PG02	I/03 DSP. CS	O	—	—	—	Z	L	DSP chip select cont.output (L:Data out)
86	P63/PG03	I/04 DSP. CLK	O	C	—	—	Z	L	DSP data clock output terminal
87	P64/PG10	I/05 SCD IN	O	C	—	—	Z	L	DSP data output terminal
88	P65/PG11	I/06 4527_CE	O	C	—	—	Z	L	AD control terminal (AK4527), Chip enable output
89	P66/PG12	I/07 4527_CLK	O	C	—	—	Z	L	AD control terminal (AK4527), Data clock output
90	P67/PG13	I/08 4527_DIN	O	C	—	—	Z	L	AD control terminal (AK4527), Data output
91	Vss	←	—	—	—	—	—	—	GND
92	P50/AN0	INTTREQ IN	I	—	Eu	Lv	Z	—	
93	P51/AN1		I	—	Eu	Lv	Z	—	
94	P52/AN2	EMP	I	—	—	Lv	—	—	H: EMP on
95	P53/AN3	96K DET	I	—	—	Lv	—	—	96k signal detect input, H: 96k
96	P54/AN4		I	—	Eu	Lv	—	Z	
97	P55/AN5		I	—	Eu	Lv	—	Z	
98	P56/AN6	ACC ON/OFF	I	—	Eu	Lv	—	Z	
99	P57/AN7		I	—	Eu	Lv	—	Z	
100	V REFH	←	—	—	—	—	—	—	AD ref. +5V

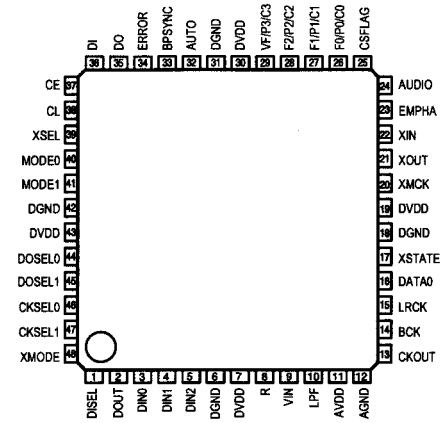
CS493292-CL (AU: IC814)



● CS493292-CL Terminal Funtion

Pin No.	Port Name	Function
1,12,23	VD1,2,3	Digital power supply (+)
2,13,24	DGND1,2,3	Digital GND
3	AUDATA3, XMT958	SPDIF transmitter output, Digital audio output 3
4	$\overline{WR}$, $\overline{DS}$, $\overline{EMWR}$, GPIO10	Host write strobe, Host data strobe, External memory write enable, General purpose in/output 10
5	$\overline{RD}$, R/$\overline{W}$, $\overline{EMOE}$,GPIO11	Host parallel output enable, Host parallel R/$\overline{W}$, External memory write enable, General purpose in/output 11
6	A1,SCDIN	Host address bit 1, SPI serial control data input
7	A0,SCCLK	Host address bit 0, Serial control port clock
8	DATA7, EMAD7, GPIO7	Bidirectional data bus 7, External memory address 7, General purpose in/output 7
9	DATA6, EMAD6, GPIO6	Bidirectional data bus 6, External memory address 6, General purpose in/output 6
10	DATA5, EMAD5, GPIO5	Bidirectional data bus 5, External memory address 5, General purpose in/output 5
11	DATA4, EMAD4, GPIO4	Bidirectional data bus 4, External memory address 4, General purpose in/output 4
14	DATA3, EMAD3, GPIO3	Bidirectional data bus 3, External memory address 3, General purpose in/output 3
15	DATA2, EMAD2, GPIO2	Bidirectional data bus 2, External memory address 2, General purpose in/output 2
16	DATA1, EMAD1, GPIO1	Bidirectional data bus 1, External memory address 1, General purpose in/output 1
17	DATA0, EMAD0, GPIO0	Bidirectional data bus 0, External memory address 0, General purpose in/output 0
18	$\overline{CS}$	Host parallel chip select, Host serial SPI chip select
19	SCDIO, SCDOUT, PSEL,GPIO9	Serial control port data in/output, Parallel port type select, General purpose in/output 9
20	$\overline{INTREQ}$, $\overline{ABOOT}$	Control port interrupt request, Automatic boot enable
21	$\overline{EXTMEM}$, GPIO8	External memory chip select, General purpose in/output 8
22	SDATAN1	PCM audio data input 1
25	SCLKN1, STCCLK2	PCM audio input bit clock
26	LRCLKN1	PCM audio input sample rate clock
27	CMPDAT, SDATAN2	PCM audio data input 2
28	CMPCLK, SCLKN2	PCM audio input bit clock
29	CMPREQ, LRCLKN2	PCM audio input sample rate clock
30	CLKIN	Master clock input
31	CLKSEL	DSP clock select
32	FILT2	PLL filter
33	FILT1	PLL filter
34	VA	Analog power supply (+)
35	AGND	Analog GND
36	$\overline{RESET}$	Master reset input
37	DD	Reserved
38	DC	Reserved
39	AUDATA2	Digital audio output 2
40	AUDATA1	Digital audio output 1
41	AUDATA0	Digital audio output 0
42	LRCLK	Audio output sample rate clock
43	SCLK	Audio output bit clock
44	MCLK	Audio master clock

LC89055W (AU: IC800)

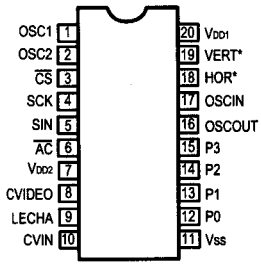


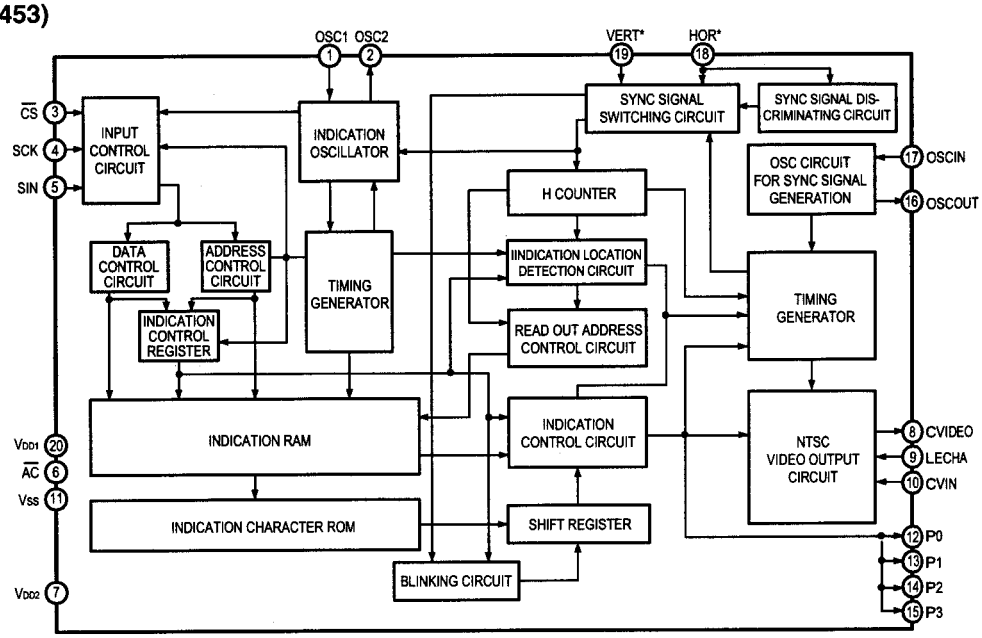
LC89055W Terminal Function

Pin No.	Pin Name	I/O	Function
1	DISEL	I	Data input terminal (select input pin of DIN0, DIN1)
2	DOUT	O	Input bi-phase data through output terminal
3	DIN0	I	Amp built-in coaxial/optical input correspond data input terminal
4	DIN1	I	Amp built-in coaxial/optical input correspond data input terminal
5	DIN2	I	Optical input correspond data input terminal
6	DGND		Digital GND
7	DVDD		Digital power supply
8	R	I	VCO gain control input terminal
9	VIN	I	VCO free-run frequency setting input terminal
10	LPF	O	PLL loop filter setting terminal
11	AVDD		Analog power supply
12	AGND		Analog GND
13	CKOUT	O	Clock output terminal (256fs, 384fs, 512fs, X'tal osc., VCO free-run osc.)
14	BCK	O	64fs clock output terminal
15	LRCK	O	fs clock output terminal (L: Rch, H: Lch, I²S: Reverse)
16	DATA0	O	Data output terminal
17	XSTATE	O	Input data detecting result output terminal
18	DGND		Digital GND
19	DVDD		Digital power supply
20	XMCK	O	X'tal osc. clock output terminal (24.576MHz or 12.288MHz)
21	XOUT	O	X'tal osc. connection output terminal
22	XIN	I	X'tal osc. connection input terminal, external signal input possible (24.576MHz or 12.288MHz)
23	EMPHA	O	Emphasis information output terminal of channel status
24	AUDIO	O	Bit1 output terminal of channel status
25	CSFLAG	O	Top 40bit revise flag output terminal of channel status
26	F0/P0/C0	O	Input fs cal. sig. out / data type out / input word inf. output terminal
27	F1/P1/C1	O	Input fs cal. sig. out / data type out / input word inf. output terminal
28	F2/P2/C2	O	Input fs cal. sig. out / data type out / input word inf. output terminal
29	VF/P3/C3	O	Validity flag out / data type out / input word inf. output terminal
30	DVDD		Digital power supply
31	DGND		Digital GND
32	AUTO	O	Non PCM burst data transfer detect sig. output terminal
33	BPSYNC	O	Non PCM burst data preamble Pa, Pb, Pc, Pd sync sig. output terminal
34	ERROR	O	PLL lock error, data error flag output terminal
35	DO	O	CPU I/F read data output terminal
36	DI	I	CPU I/F write data input terminal
37	CE	I	CPU I/F chip enable input terminal
38	CL	I	CPU I/F clock input terminal
39	XSEL	I	Frequency select input pin of XIN X'tal osc. (24.576MHz or 12.288MHz)
40	MODE0	I	Mode setting input terminal
41	MODE1	I	Mode setting input terminal
42	DGND		Digital GND
43	DVDD		Digital power supply
44	DOSEL0	I	Data output format select input terminal
45	DOSEL1	I	Data output format select input terminal
46	CKSEL0	I	Output clock select input terminal
47	CKSEL1	I	Output clock select input terminal
48	XMODE	I	Reset input terminal

* For latch-up countermeasure, set digital (DVDD) and analog (AVDD) power on/off in the same timing.

M35015-210SP (AU: IC453)

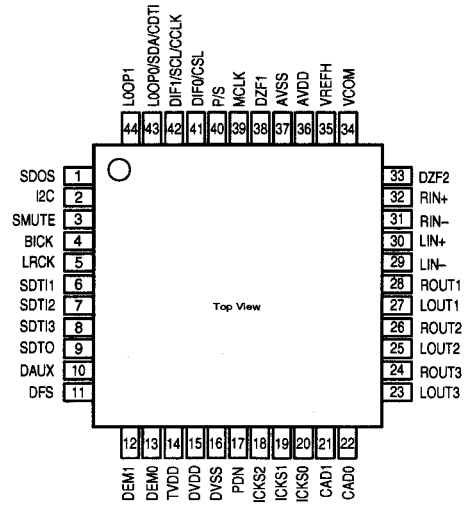




M35015-210SP Terminal Function

Pin No.	Symbol	Name	I/O	Function
1	OSC1	Osc. circuit ext. terminal.	I	External terminal for indication oscillator circuit. Standard OSC. freq. is approx. 7MHz.
2	OSC2		O	With this OSC. freq., decides horizontal indicatin and character width.
3	$\overline{CS}$	Chip select input	I	Chip select terminal and turns to "L" when transfer serial data. Hysteresis input. Pull up resistor is built-in.
4	SCK	Serial clock input	I	Takes in serial data of SIN at SCK rise when CS terminal is in "L". Hysteresis input. Pull up rersist is built-in.
5	SIN	Serial data input	I	Serial input of register for indication control and data, and address for indication data memory. Hysteresis input. Pull up rersistor is built-in.
6	$\overline{AC}$	Auto-clear input	I	Resets internal circuit of IC at "L" mode. Hysteresi input. Pull up resistor is built-in.
7	VDD2	Power supply	—	Power supply terminal of analog system. Connect to +5V.
8	CVIDEO	Combined video output	O	Output terminal of combined video signal. Outputs 2Vp-p combined signal. Character output, etc. Overlap CVIN signal and outputs at superimpose.
9	LECHA	Character level input	I	Input terminal deciding character output level in combined video signal. color of character is white.
10	CVIN	Combined video input	I	Input terminal of external combined video signal. Character output etc. overlap this external combined video signal.
11	Vss	Ground	—	Ground terminal. Connect to GND.
12	P0	Output port p0	O	General output or character background signal BL NK1* output is switchable. Polarity can be selected at ROM mask.
13	P1	Output port P1	O	General output or character background signal CO1* output is switchable. Polarity can be selected at ROM mask.
14	P2	Output port P2	O	General output or character background signal BLNK2* output is switchable. Polarity can be selected at ROM mask.
15	P3	Output port P3	O	General output or character background signal CO2* output is switchable. Polarity can be selected at ROM mask.
16	OSCOUT	Ext. terminal for sync sig. OSC. Circuit	O	Terminal for external use of sync signal OSC. circuit. Use the freq.: 14.32MHz at NTSC system, 17.73MHz at PAL. system, 14.30MHz at MPAL system.
17	OSCIN		I	
18	HOR*	Horizontal sync signal	I	Inputs horizontal sync signal. Hysteresis input.
19	VERT*	Vertical sync signal	—	Input vertical sync signal. Hysteresis input. Polarity can be selected at ROM mask.
20	VDD1	Power supply	I	Power supply terminal of digital system. Connect to +5V.

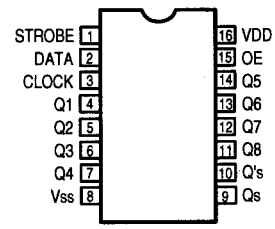
AK4527BVQ (AU:IC602)



AK4527BVQ Terminal Function

Pin No.	Pin Name	I/O	Function
1	SDOS	I	SDTO source select pin, L: Internal ADC output, H: DAUX input
2	I2C	I	Serial control mode select pin, L: 3-core serial, H: I²C bus
3	SMUTE	I	Soft mute pin, H: Soft mute start, L: Release
4	BICK	I	Audio serial data clock pin
5	LRCK	I	Input channel clock pin
6	SDTI1	I	DAC1 audio serial data input pin
7	SDTI2	I	DAC2 audio serial data input pin
8	SDTI3	I	DAC3 audio serial data input pin
9	SDTO	O	Audio serial data output pin
10	DAUX	I	Auxiliary audio serial data input pin
11	DFS	I	Double speed sampling mode pin, L: Normal, H: Double
12	NC	—	No Connect, No internal bonding
13	DZFE	I	Zero input detect enable pin
14	TVDD	—	Power pin for output buffer, 2.7V~5.5V
15	DVDD	—	Digital power pin, 4.5V~5.5V
16	DVss	—	Digital GND pin, 0V
17	PDN	I	Power down & reset pin, L: Powered-down and register initialized, Reset with PDN when switching CAD0-I
18	TST	I	Test pin, connected to DVSS
19	NC	—	No Connect, No internal bonding
20	ADIF	I	Analog Input Format Select pin
21	CAD1	I	Chip address-1 pin
22	CAD0	I	Chip address-0 pin
23	LOUT3	O	DAC3L channel analog out pin
24	ROUT3	O	DAC3R channel analog out pin
25	LOUT2	O	DAC2L channel analog out pin
26	ROUT2	O	DAC2R channel analog out pin
27	LOUT1	O	DAC1L channel analog out pin
28	ROUT1	O	DAC1R channel analog out pin
29	LIN-	I	L-ch analog inverted input pin
30	LIN+	I	L-ch analog non-inverted input pin
31	RIN-	I	R-ch analog inverted input pin
32	RIN+	I	R-ch analog non-inverted input pin
33	DZF2/OVF	O	0 input detect 2 pin/Analog input overflow detect pin
34	VCOM	O	Common V-out pin, AVDD/2, connect large capacitor to avoid noise
35	VREFH	I	Ref. V input pin, AVDD
36	AVDD	—	Analog GND pin, 4.5V~5.5V
37	AVss	—	Analog GND pin, 0V
38	DZF1	O	0 input detect pin, H: Input data of G1 is 8192 times "0" in a raw or RSTN bit "0", L: When P/S= "0"
39	MCLK	I	Master clock input pin
40	P/S	I	Parallel/Serial select pin, L: Serial control
41	DIF0	I	Audio data I/F format 0 pin (parallel control)
	CSN	I	Chip select pin (3-wire serial control), connect to DVDD when I²C bus control
42	DIF1	I	Audio data I/F format 1 pin (parallel control)
	SCL/CCLK	I	Control data clock pin (serial control), I²C="L": CCLK (3-wire serial), I²C="H": SCL (I²C bus)
43	LOOP0	I	Loop back mode 0 pin (parallel control), effects digital loop back ADC to all DAC
	SDA/CDTI	I/O	Control data input pin (serial control), I²C="L": CCTI (3-wire serial), I2C="H" SDA (I²C bus)
44	LOOP1	I	Loop back mode 1 pin, from SDT1 to all DAC

BU4094BCF (CO: IC304,305)



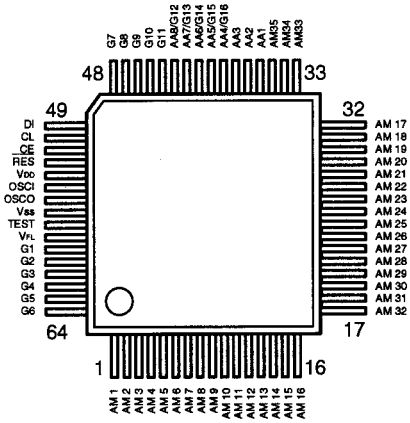
CO: IC304

Port	Symbol	Function
Q1	A	Video input switching
Q2	B	Video input switching
Q3	C	Video input switching
Q4	D	Video output switching
Q5	E	Video output switching
Q6	F	Video output switching
Q7	H	Video output switching
Q8	G	Video output switching

CO: IC305

Port	Symbol	Function
Q1	DIRECT/TONE DEFEAT	DIRECT & TONE DEFEAT relay control (H:DIRECT,TONE DEFEAT)
Q2	S1	Video signal switching control output
Q3	S2	Video signal switching control output
Q4	EXT. IN	Sub woofer channel gain control terminal (L:EXT. IN)
Q5	D	Video output switching
Q6	G	Video output switching
Q7	NC	
Q8	FRONT A+B	Current limiter control terminal (H:Front SP A+B)

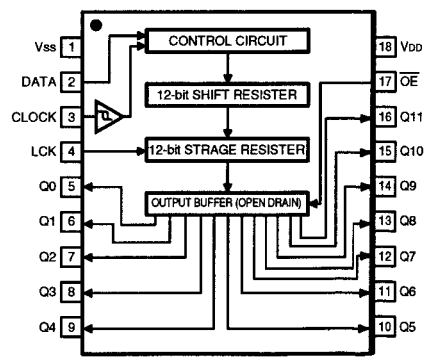
LC75721E (CO: IC101)



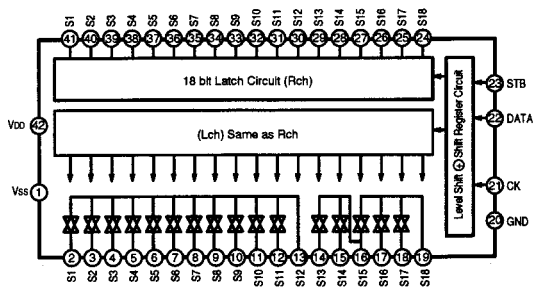
LC75721E Terminal Function

Symbol	Function
VDD	Power terminal +5V
Vss	Power terminal GND
VFL	Power terminal FL drive
DI CL CE	Serial data transfer terminal DI: Data CL: Clock CE: Chip enable
OSCI OSCO	External CR connecting terminal
$\overline{RES}$	System reset terminal
AM1~AM35 AA1~AA3	Anode output terminal
AA4/G16 AA5/G15 AA6/G14 AA7/G13 AA8/G12	Anode/Grid output terminal
G1~G11	Grid output terminal
TEST	LSI test terminal

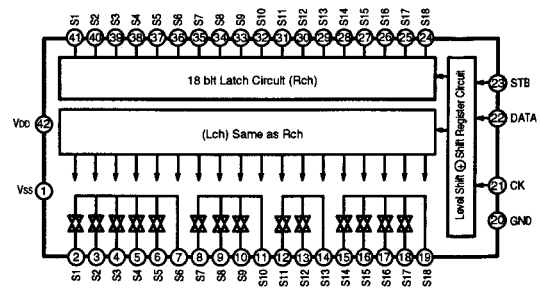
BU2090F (CO: IC103)



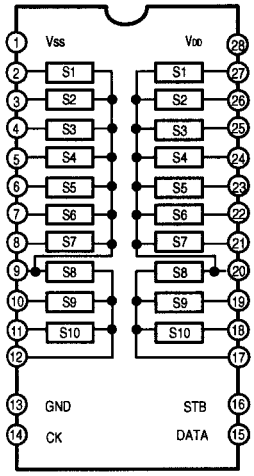
TC9274N-011 (AU: IC107)



TC9274N-017 (EX: IC312)



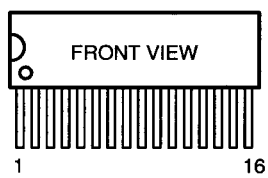
TC9273N-004 (AU: IC108)

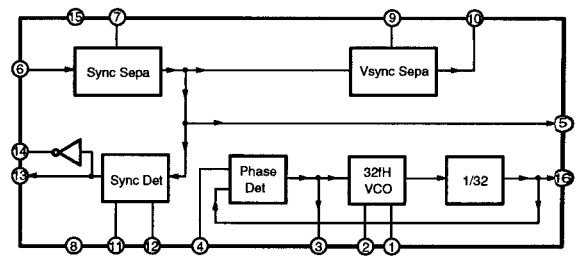


TC9273N Terminal Function

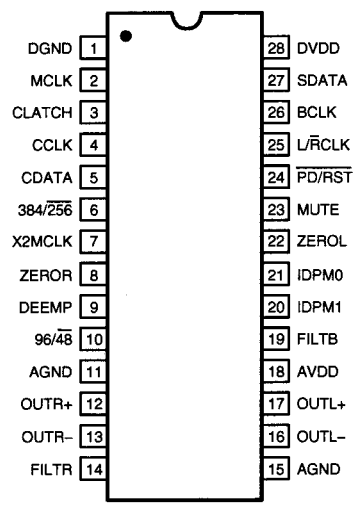
Pin No	Symbol	Name	Function	
1	Vss	+Power Terminal	Dual Power Use:VDD = 8.0~17 V Single Power Use:VDD = 8.0~18V	
13	GND	Digital Ground	GND=0V GND=0V	
28	VDD	+Power Terminal	Vss=-8.0~-17V	
2~12 12~27	S1~S10	I/O Terminal	Input terminal of analog switch.	
14	CK	Clock Input	Clock input for data transfer.	Low level Border Input Terminal
15	DATA	Data Input	Serial input for switch setting.	
16	STB	Strobe Input	Strobe InputStrobe input for data writing.	

NJM2229S (AU: IC452)





AD1854 (AU: IC601)

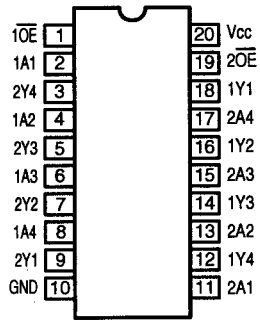


Terminal Function

No.	Name	I/O	Function
1	DGND	I	Digital Ground.
2	MCLK	I	Master Clock Input
3	CLATCH	I	Latch input for control data
4	CCLK	I	Control clock input for control data
5	CDATA	I	Serial control input
6	384/256	I	Selects the master clock mode
7	X2MCLK	I	Selects internal clock doubler (LO) or internal clock=MCLK(HI)
8	ZEROR	O	Right Channel Zero Flag Output
9	DEEMP	I	De-Emphasis
10	96/48	I	Selects 48kHz (LO) or 96kHz Sample Frequency Control
11,15	AGND	I	Analog Ground
12	OUTR+	O	Right Channel Positive line level analog output
13	OUTR-	O	Right Channel Negative line level analog output
14	FILTR	O	Voltage Reference Filter Capacitor Connection
16	OUTL-	O	Left Channel Negative line level analog output
17	OUTL+	O	Left Channel Positive line level analog output
18	AVDD	I	Analog Power supply
19	FILTB	O	Filter Capacitor connection
20	IDPM1	I	Input serial data port mode control one
21	IDPM0	I	Input serial data port mode control zero
22	ZEROL	O	Left Channel Zero Flag output
23	MUTE	I	Mute. Assert HI to mute both stereo analog output
24	PD/RST	I	Power-Down/Reset
25	L/R CLK	I	Left/Right clock input for input data
26	BCLK	I	Bit clock input for input data
27	SDATA	I	Serial input
28	DVDD	I	Digital Power Supply

SN74LV244APW (AU: IC818, 825)

TOP VIEW

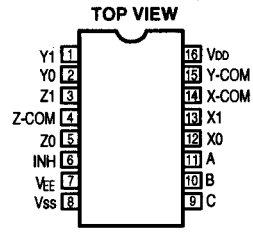


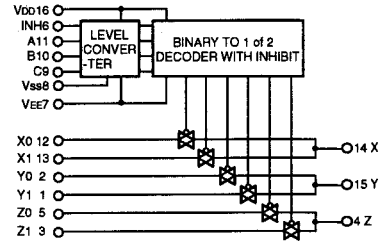
FUNCTION TABLE (each buffer)

INPUT		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

BU4053BCF (AU:IC256)
MM74HC4053SJ (AU: IC451)

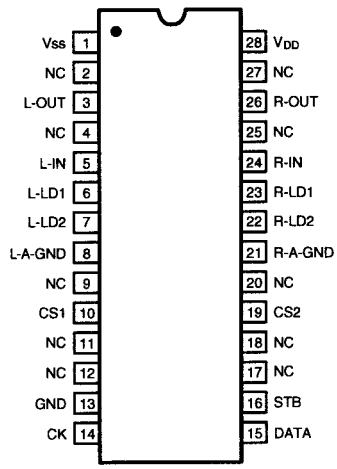
TOP VIEW

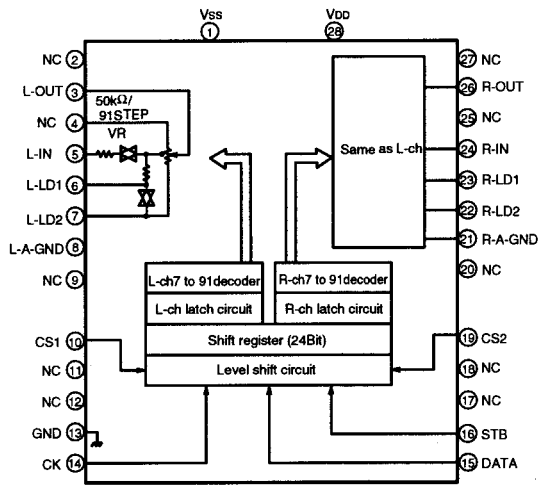




TC9459N
(EX: IC805)

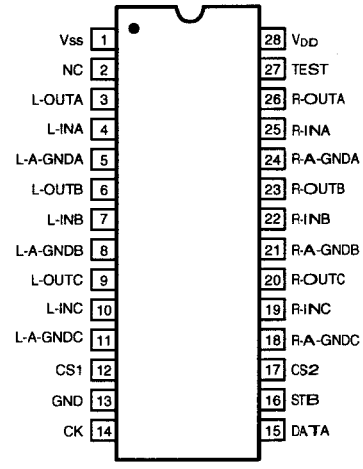
TOP VIEW





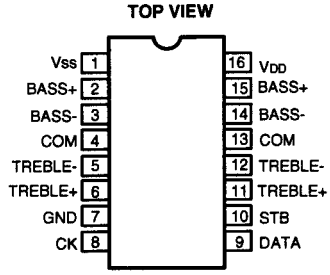
TC9482N
(EX: IC809)

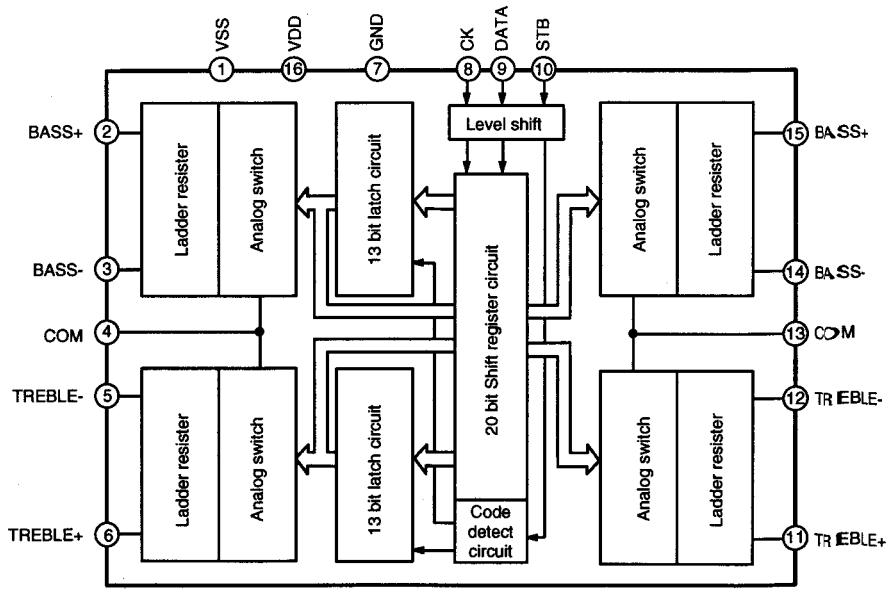
TOP VIEW



TC9184AP (EX: IC102)

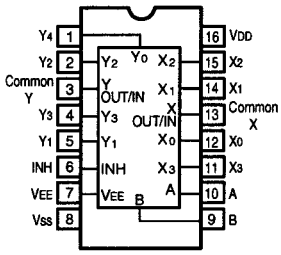
TOP VIEW





BU4052BCF (AU:IC255,509,510)

TOP VIEW



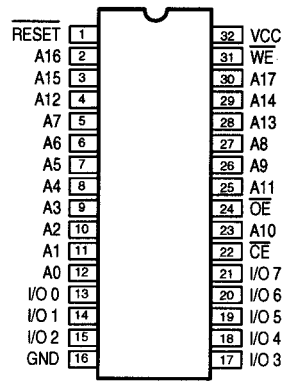
FUNCTION TABLE

INH	A	B	ON SWITCH
L	L	L	X_0 Y_0
L	H	L	X_1 Y_1
L	L	H	X_2 Y_2
L	H	H	X_3 Y_3
H	X	X	NONE

X:Don't Care

AT49LV002T (AU:IC817)

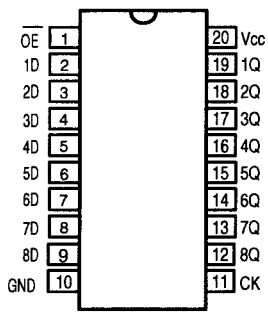
TOP VIEW



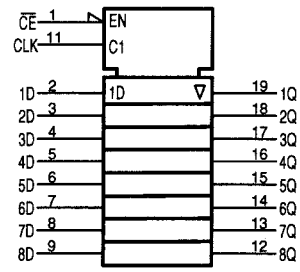
FUNCTION TABLE

Pin Name	Function
A0 - A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RESET}$	RESET
I/O0 -I/O7	Data Inputs/Outputs
DC	Don't Connect

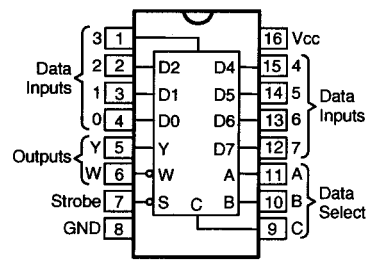
SN74AHC574PW (AU: IC815, 816)



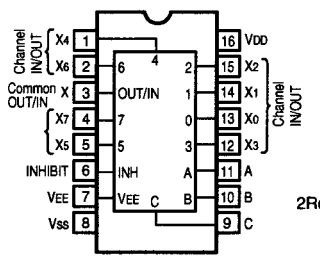
logic symbol



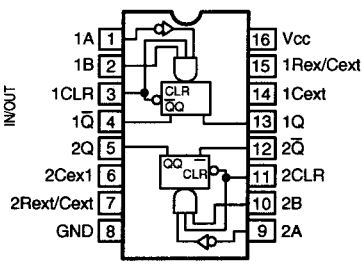
SN74HC151NS (EX:IC505,506)



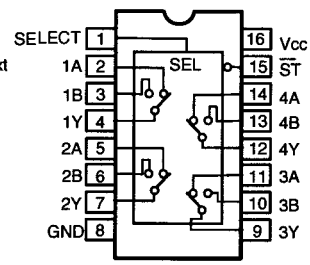
BU4051BCF (AU:IC251,252,504~507)



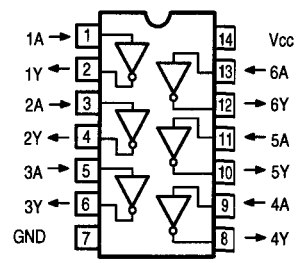
TC74VHC123AF (AU: IC801)



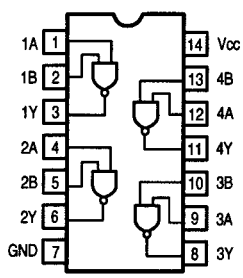
74LVX157 (AU: IC804)



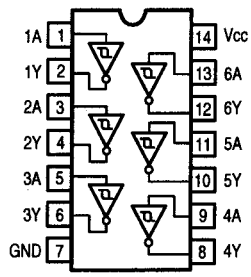
TC74HCU04AF (EX:IC504)



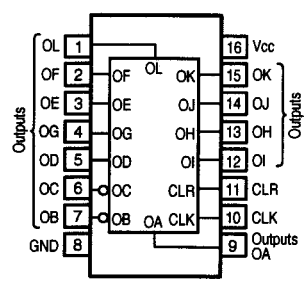
SN74LV00APW (AU: IC807)



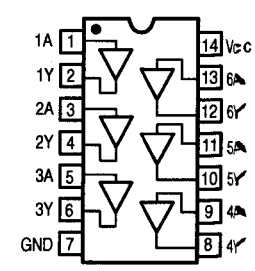
SN74LV14APW (AU: IC809)



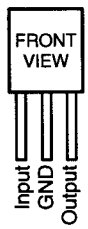
SN74LV4040APW (AU: IC813)



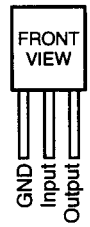
TC74HCT7007AF (AU:IC823)



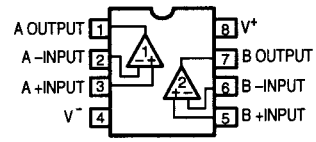
BA033T (AU: IC819)
KIA7805API (RE: IC901, 902, 907)
KIA7806API (PO: IC501)
KIA7812API (RE: IC905)



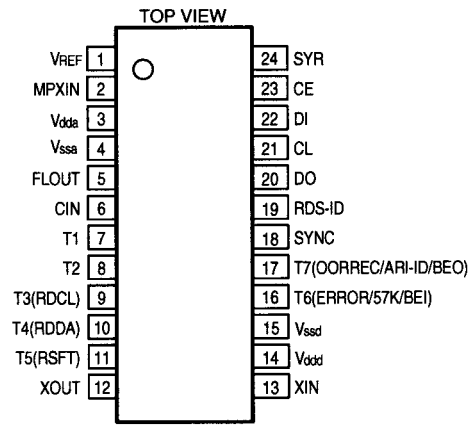
KIA7905PI (RE: IC909)
KIA7912PI (RE: IC906)



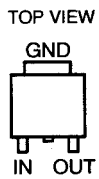
BA15218F (AU: IC112)
BA4510F (AU: IC811, 812)
NJM2068MD (EX: IC103, 301, 302, 308~310, 701, 801~804) (AU: IC109, 701, 721, 741, 761)
TK15420MTL (AU: IC253, 254, 257, 501~503, 508, 511)



LC72720NM (CO: IC105)
Europe Model Only

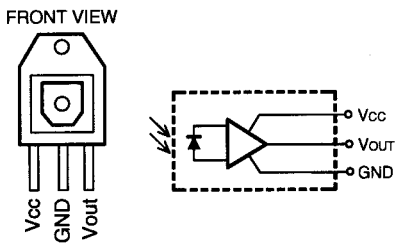


NJM2391DL1 (AU: IC824)

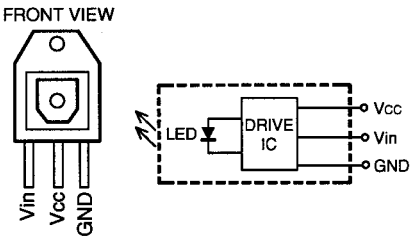


● OPTICAL

INPUT
GP1FA551RZ (EX:IC501~503)

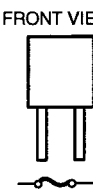


OUTPUT
GP1FA551TZ(EX:IC707)



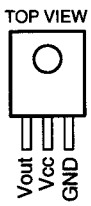
● IC PROTECTOR

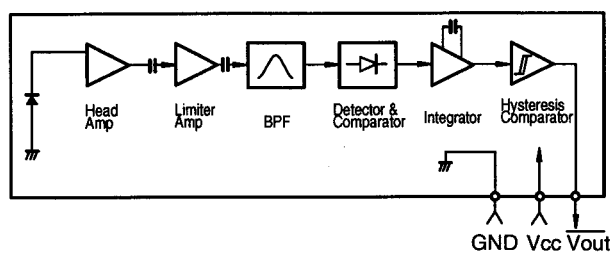
ICP-N15 (PO: IC502)



● OTHERS

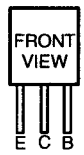
GP1U27X (Remote Control Sensor)
(CO: IC102)



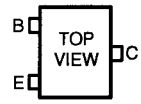


• TRANSISTORS

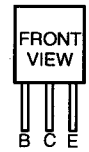
2SA970 (BL)
2SA988 (E/F)
2SA933S (S)
2SA1145 (O/Y)
2SC1740S (S)
2SC2705 (O/Y)
2SC3311A
2SD2144STPU
KTA1266 (GR)
KTC2874B
2SC/KTC3200(BL)



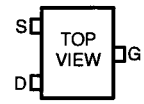
2SA1505Y
2SC2412K (S)
2SD601A
KTC2875B



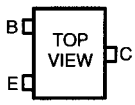
2SB/KTB778 (R/O)



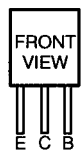
2SK771



DTA114EK
DTA114TK
DTA144EK
DTC114EK
DTC143EK
DTC144EK
DTC323TK

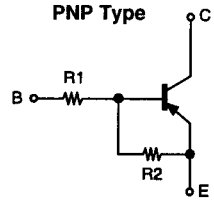


DTC114ES



DTA114TK
DTA114EK
DTA144EK

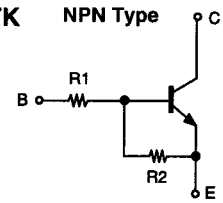
PNP Type



	R1	R2
DTA114EK	10kohm	10kohm
DTA114TK	10kohm	–
DTA144EK	47kohm	47kohm

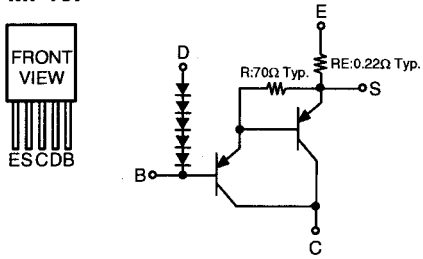
DTC114EK
DTC114ES
DTC143EK
DTC144EK
DTC323TK

NPN Type

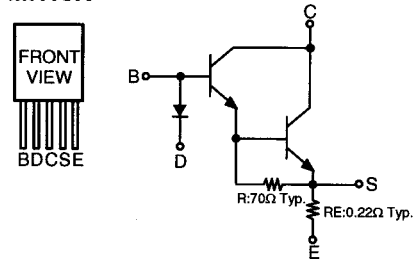


	R1	R2
DTC114EK	10kohm	10kohm
DTC114ES	10kohm	10kohm
DTC143EK	4.7kohm	4.7kohm
DTC144EK	47kohm	47kohm
DTC323TK	2.2kohm	–

MP15P

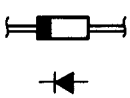


MN15N

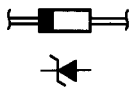


• DIODES (included LED)

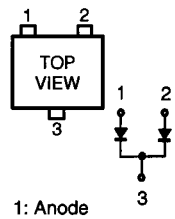
1SR35-400A
1SS270A
RB721Q-40



HZS3C-2
HZS5C-1
HZS6A-1
HZS6A-2
HZS7B-2
HZS9B-1
HZS33-2
MTZJ18A

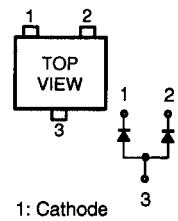


DAN202K



1: Anode
2: Anode
3: Cathode

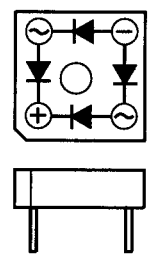
DAP202K



1: Cathode
2: Cathode
3: Anode

S4VB20
S4VB20F

TOP VIEW

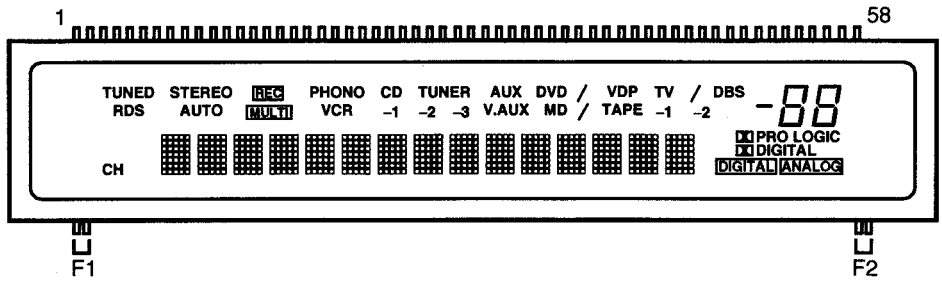


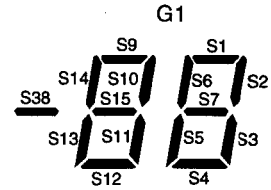
SEL1210S (Red)
SEL1410E (Green)

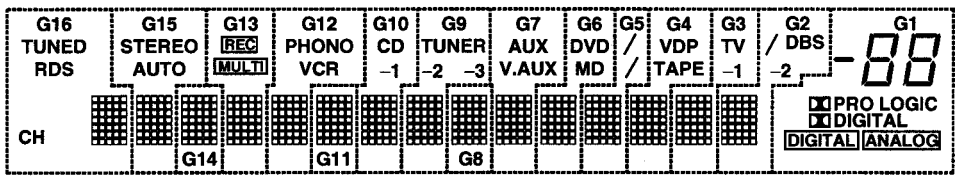
TOP VIEW

● FL DISPLAY

CM1690C (CO: FL101)







G2~G16

S1	S2	S3	S4	S5
S6	S7	S8	S9	S10
S11	S12	S13	S14	S15
S16	S17	S18	S19	S20
S21	S22	S23	S24	S25
S26	S27	S28	S29	S30
S31	S32	S33	S34	S35

Pin Assignment

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
CONNECTION	F1	F1	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18
PIN NO.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
CONNECTION	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32	S33	S34	S35	S36	S37	S38
PIN NO.	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58		
CONNECTION	G16	G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	F2	F2		

F1,F2 : Filament
G1~G16 : Grid
S1~S38 : Anode

Anode & Grid Assignment

	G1	G2~G16		G1	G2~G16		G1	G2~G16		G1	G2~G16
S1	S1	S1	S10	S10	S10	S19	—	S19	S28	—	S28
S2	S2	S2	S11	S11	S11	S20	—	S20	S29	—	S29
S3	S3	S3	S12	S12	S12	S21	—	S21	S30	—	S30
S4	S4	S4	S13	S13	S13	S22	—	S22	S31	—	S31
S5	S5	S5	S14	S14	S14	S23	—	S23	S32	—	S32
S6	S6	S6	S15	S15	S15	S24	—	S24	S33	—	S33
S7	S7	S7	S16	—	S16	S25	—	S25	S34	—	S34
S8		S8	S17	DIGITAL	S17	S26	—	S26	S35	—	S35
S9	S9	S9	S18	PRO LOGIC	S18	S27	—	S27			

	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G15	G16
S36	DIGITAL	/	TV	VDP	/(DVD)	DVD	AUX	—	TUNER	CD	—	PHONO	REC	—	STEREO	TUNED
S37	ANALOG	–2	–1	TAPE	/(MD)	MD	V.AUX	—	–2	–1	—	VCR	MULTI	—	AUTO	RDS
S38	S38	DBS	—	—	—	—	—	—	–3	—	—	—	—	—	—	CH