DENON

For U.S.A. & Canada model

SERVICE MANUAL

Ver. 1

MODEL AVR-5805

AV SURROUND RECEIVER

注　意

サービスをおこなう前に、このサービスマニュアルを必ずお読みください。本機は、火災、感電、けがなどに対する安全性を確保するために、さまざまな配慮をおこなっており、また法的には「電気用品安全法」にもとづき、所定の許可を得て製造されております。
従ってサービスをおこなう際は、これらの安全性が維持されるよう、このサービスマニュアルに記載されている注意事項を必ずお守りください。

● **For purposes of improvement, specifications and design are subject to change without notice.**	● 本機の仕様は性能改良のため、予告なく変更することがあります。 ● 補修用性能部品の保有期間は、製造打切後8年です。
● **Please use this service manual with referring to the operating instructions without fail.**	● 修理の際は、必ず取扱説明書を参照の上、作業を行ってください。
● **Some illustrations using in this service manual are slightly different from the actual set.**	● 本文中に使用しているイラストは、説明の都合上現物と多少異なる場合があります。

DENON, Ltd.

TOKYO JAPAN

X0219-1V.01 DE/CDM 0411

SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Before returning the unit to the customer, make sure you make either (1) a leakage current check or (2) a line to chassis resistance check. If the leakage current exceeds 0.5 milliamps, or if the resistance from chassis to either side of the power cord is less than 460 kohms, the unit is defective.

注　意　サービス、点検時には次のことにご注意願います。

◉注意事項をお守りください！

サービスのとき特に注意を必要とする個所については、キャビネット、部品、シャーシなどにラベルや捺印で、注意事項を表示しています。これらの注意書きおよび取扱説明書などの注意事項を必ずお守りください。

◉感電に注意！

(1)このセットは、交流電圧が印加されていますので、通電時に内部金属部に触れると感電することがあります。従って通電サービス時には、絶縁トランスの使用や手袋の着用、部品交換には、電源プラグを抜くなどして、感電にご注意ください。

(2)内部には、高電圧の部分がありますので、通電時の取扱には、十分ご注意ください。

◉指定部品の使用！

セットの部品は難燃性や耐電圧など安全上の特性を持ったものとなっています。従って交換部品は、使用されていたものと同じ特性の部品を使用してください。特に配線図、部品表に⚠印で指定されている安全上重要な部品は必ず指定のものをご使用ください。

◉部品の取付けや配線の引きまわしは、元どおりに！

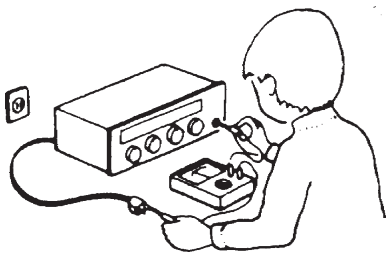
安全上、テープやチューブなどの絶縁材料を使用したり、プリント基板から浮かして取付けた部品があります。また内部配線は引きまわしやクランパーによって発熱部品や高圧部品に接近しないように配慮されていますので、これらは必ず元どおりにしてください。

◉サービス後は安全点検を！

サービスのために取り外したねじ、部品、配線などが元どおりになっているか、またサービスした個所の周辺を劣化させてしまったところがないかなどを点検し、外部金属端子部と、電源プラグの刃の間の絶縁チェックをおこなうなど、安全性が確保されていることを確認してください。

（絶縁チェックの方法）

電源コンセントから電源プラグを抜き、アンテナや、プラグなどを外し、電源スイッチを入れます。500Ｖ絶縁抵抗計を用いて、電源プラグのそれぞれの端子と、外部露出金属部〔アンテナ端子、ヘッドホン端子、マイク端子、入力端子など〕との間で、絶縁抵抗値が1MΩ以上であること、この値以下のときは、セットの点検修理が必要です。



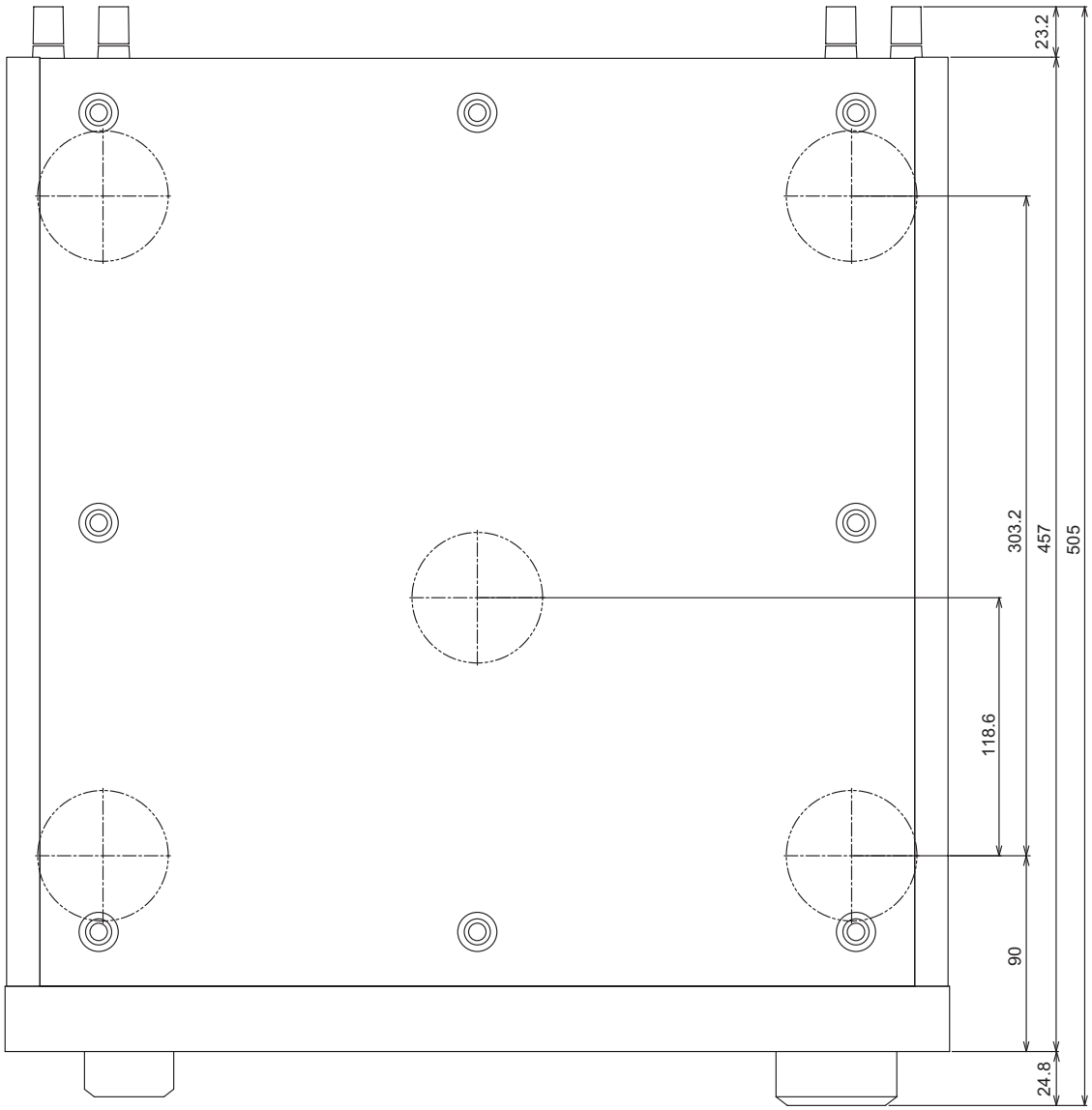
注　意　安全上重要な部品について

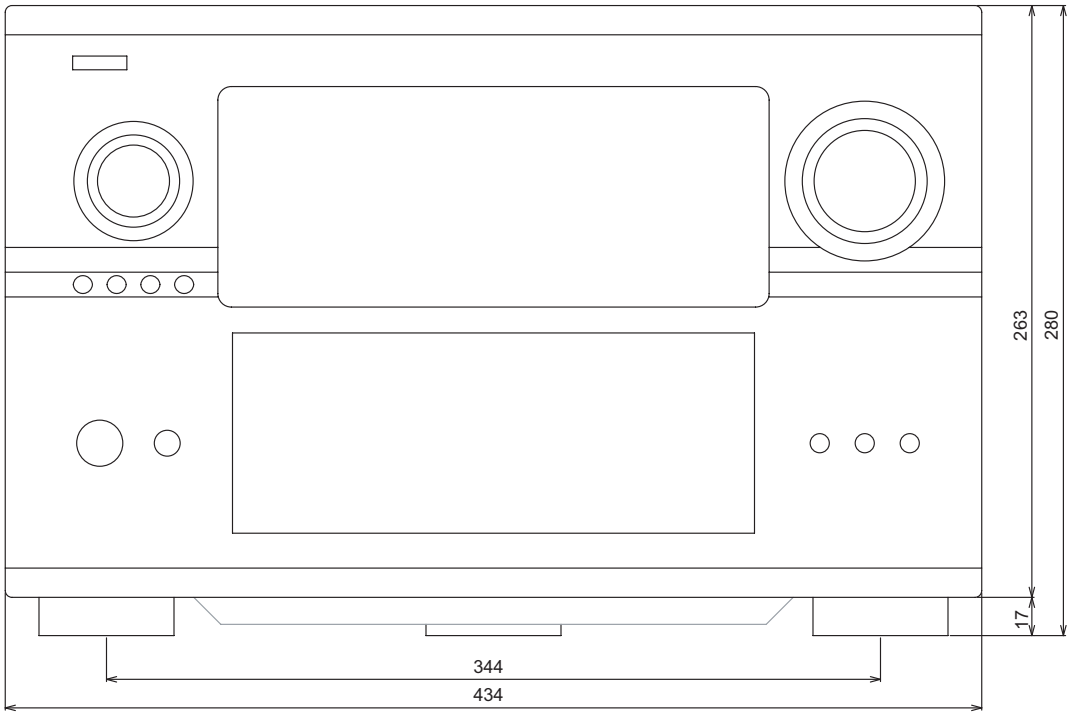
本機に使用している多くの電気部品、および機構部品は安全上、特別な特性を持っています。この特性はほとんどの場合、外観では判別つきにくく、また、もとの部品より高い定格（定格電力、耐圧）を持ったものを使用しても安全性が維持されるとは、限りません。安全上の特性を持った部品は、このサービスマニュアルの配線図、部品表につぎのように表示していますので、必ず指定されている部品番号のものを使用願います。

(1) 配線図… ⚠マークで表示しています。

(2) 部品表… ⚠マークで表示しています。
指定された部品と異なるものを使用した場合には、感電、火災などの危険を生じる恐れがあります。

DIMENSION





WIRE ARRANGEMENT

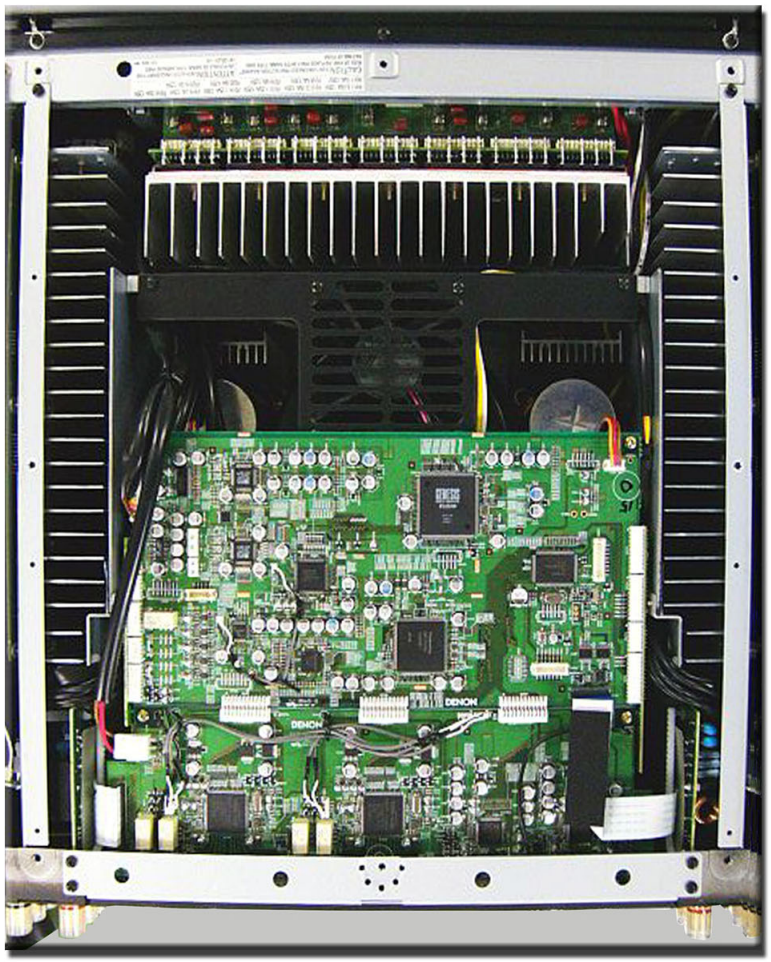
If wire bundles are untied or moved to perform adjustment or parts replacement etc.,be sure to rearrange them neatly as they were originally bundled or placed afterward. Otherwise, incorrect arrangement can be a cause of noise generation.

Wire arrangement viewed from the top

ワイヤー整形図

調整や部品の交換等により、ワイヤー類の結束をはずしたり移動させた場合には、それらの作業が完了した時点でワイヤーの整形をおこなってください。正しく整形されていないとノイズ発生の原因となることがあります。

上面からみたワイヤー整形



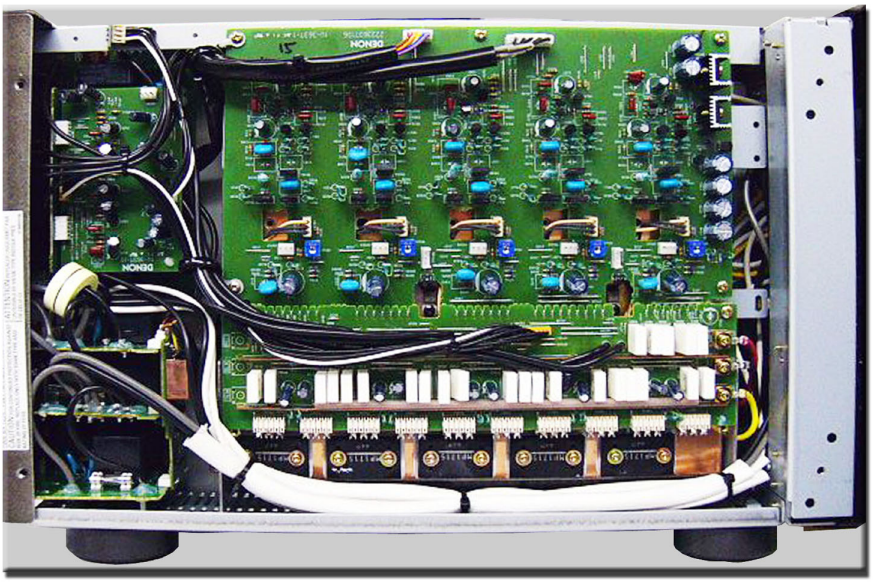
Front Panel side

Back Panel side

Wire arrangement viewed from the side (left)

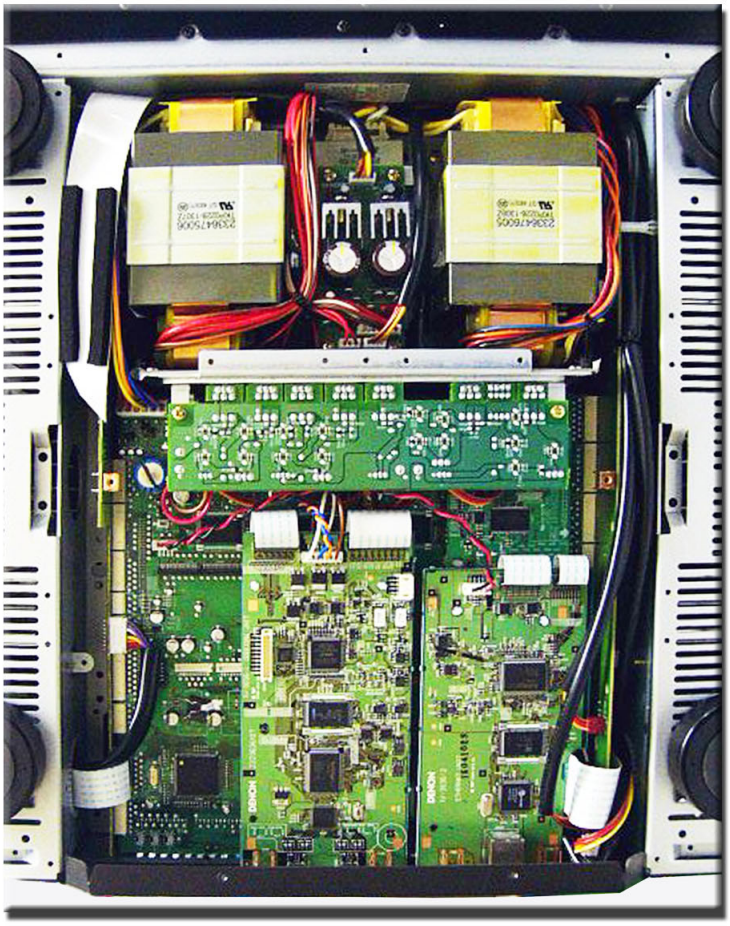
側面（左側）からみたワイヤー整形

Back Panel side



Front Panel side

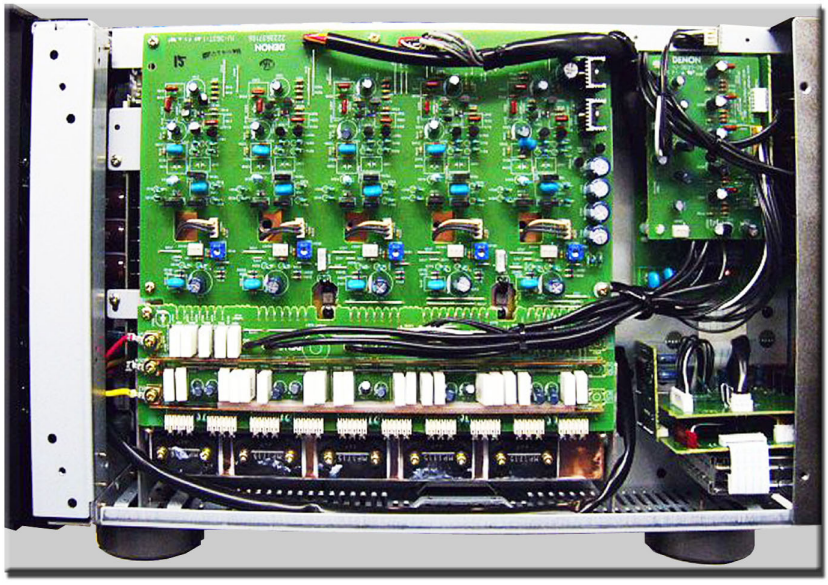
Wire arrangement viewed from the bottom　　下面からみたワイヤー整形



Front Panel side

Back Panel side

Wire arrangement viewed from the side (right)　側面（右側）からみたワイヤー整形

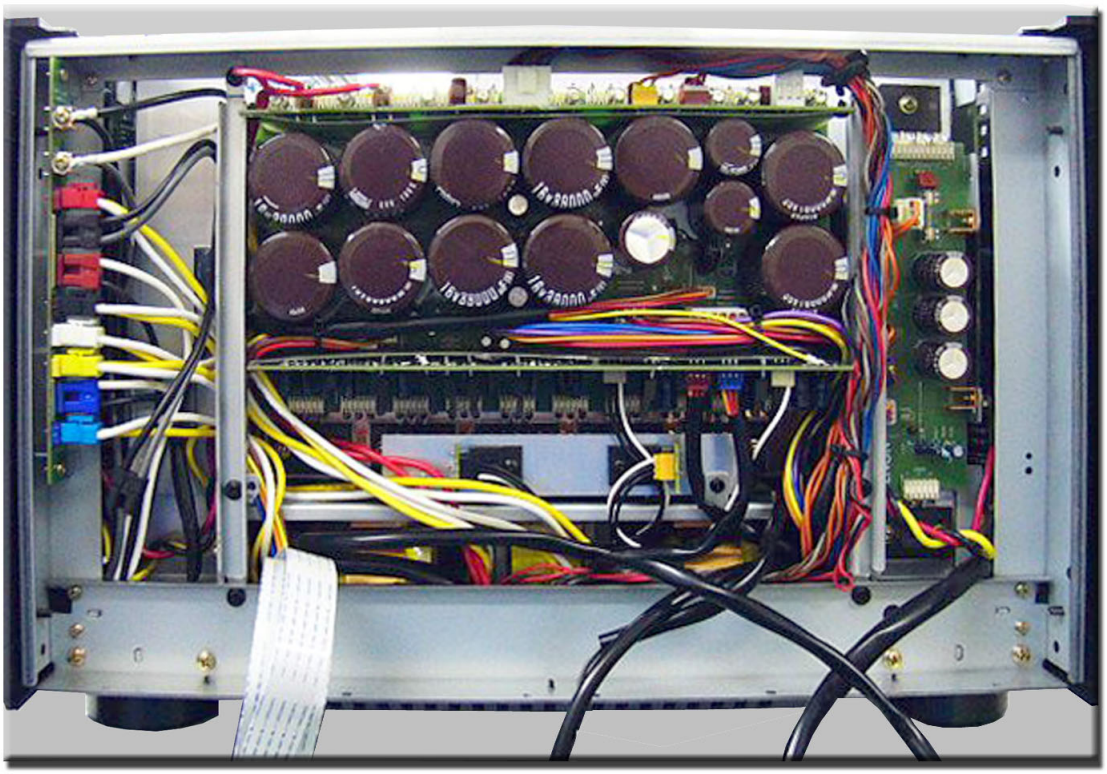


Front Panel side

Back Panel side

Wire arrangement viewed from the Front (without the Front Panel)

正面からみたワイヤー整形（前面パネルをはずした状態）



CAUTION IN SERVICING

Initializing AV SURROUND RECEIVER /AMPLIFIER

AV SURROUND RECEIVER/AMPLIFIER initialization should be performed when the µcom, peripheral parts of µcom, and Digital P.W.B. are replaced.

1. Switch off the unit using the Main unit's power operation switch.
2. Hold the following STANDARD button and HOME THX CINEMA button, and turn the Main unit's power operation switch on.
3. Check that the entire display is flashing with an interval of about 1 second, and release your fingers from the 2 buttons and the microprocessor will be initialized.

Note: ・If step 3 does not work, start over from step 1.
・All user settings will be lost and this factory setting will be recovered when this initialization mode.
So make sure to memorize your setting for restoring after the initialization.

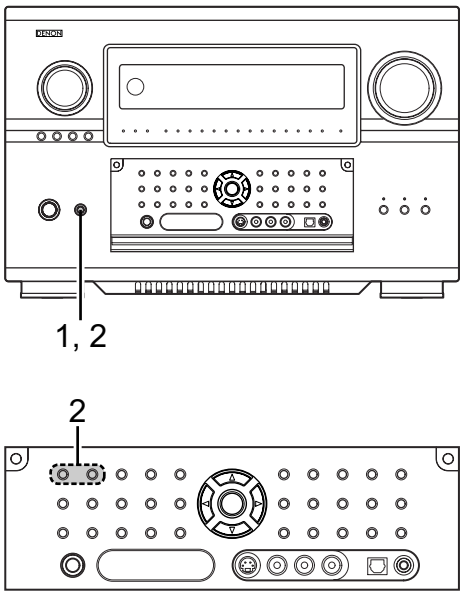
サービス時の注意事項

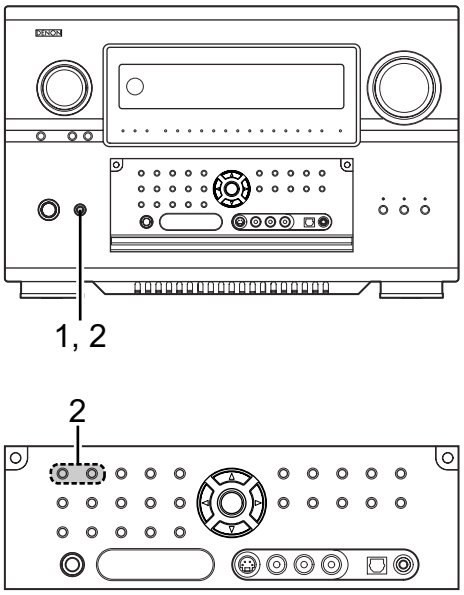
AV サラウンドアンプ / レシーバーの初期化について

マイコンやマイコン周辺部品、Digital 基板等を交換した場合は、AV サラウンドアンプの初期化を行って下さい。

1. 電源スイッチを OFF にします。
2. ホーム THX シネマボタンとスタンダードボタンを同時に押しながら、電源スイッチを ON にします。
3. ディスプレイ表示が約 1 秒間隔で点滅するのを確認後、2 つのボタンから指を離します。
＊マイコンが初期化されます。

注意：・上記 3 の状態にならない場合は、もう一度操作 1 からやり直してください。
・初期化を行うとお客様が設定した内容が工場出荷状態に戻りますので、あらかじめ設定内容を控えておき初期化後再設定してください。



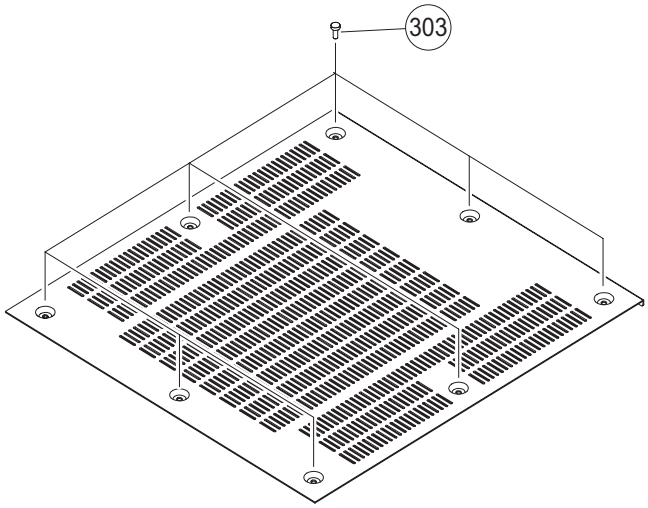


DISASSEMBLY

(Follow the procedure below in reverse order when reassembling.)

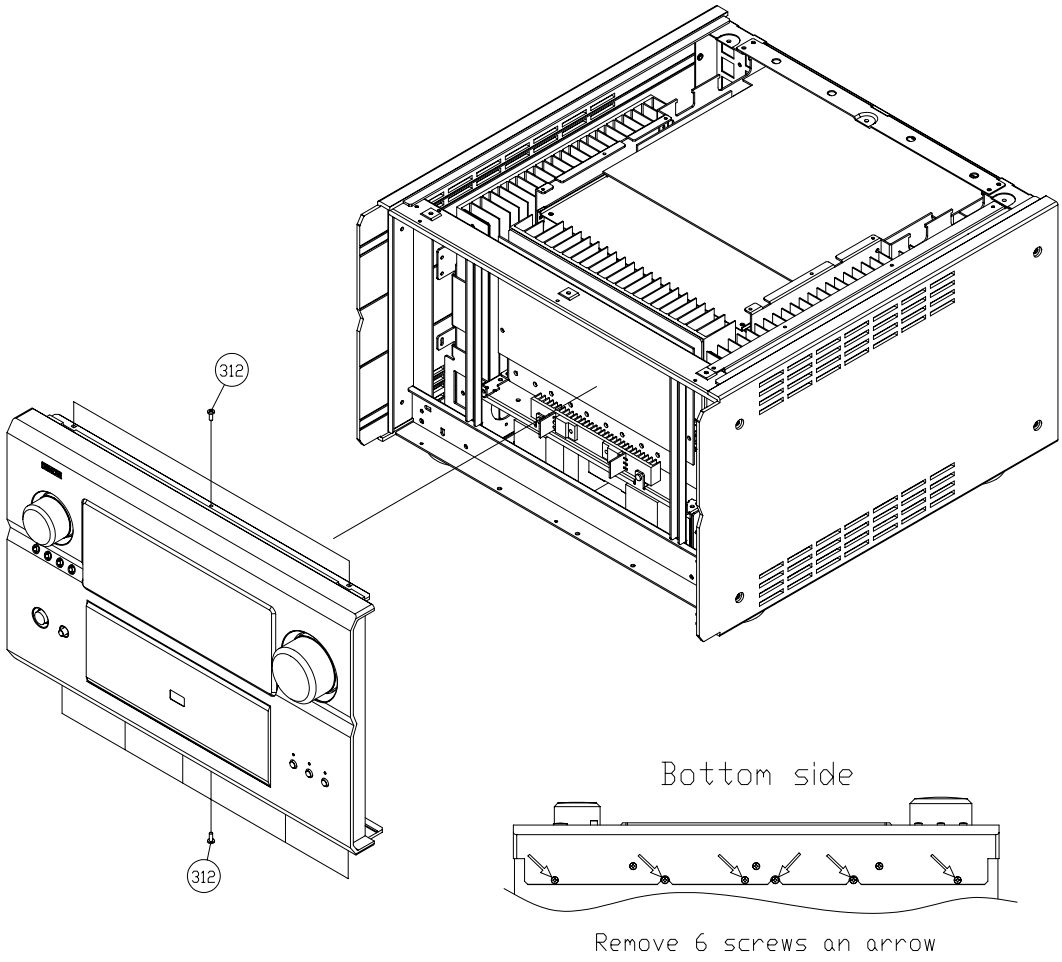
1. Top Cover

(1) Remove 8 screws (303) on the top.



2. Front Panel

(1) Remove 9 screws (312).



各部のはずしかた

（組み立てるときは、逆の順序で行ってください。）

1. Top Cover

(1) ねじ (303) を 8 本はずします。

2. Front Panel

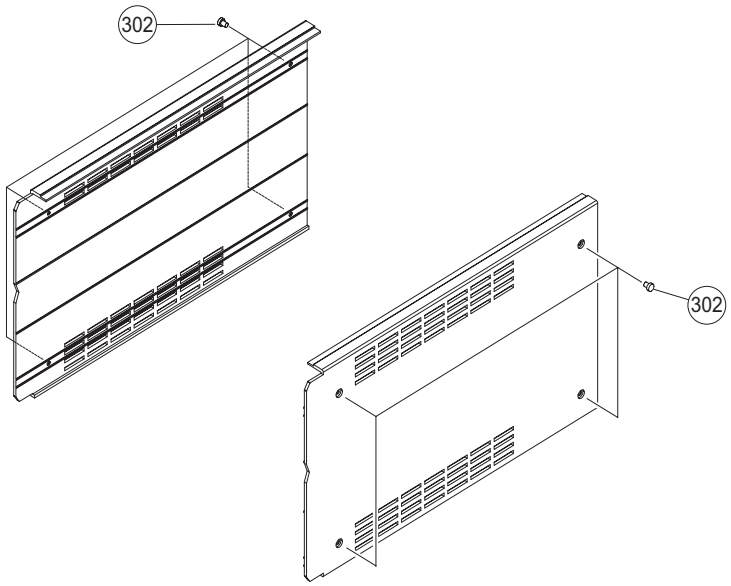
(1) ねじ (312) を 9 本はずします。

3. Side Cover

(1) Remove 8 screws (302).

3. Side Cover

(1) ねじ (302) を各 4 本、計 8 本はずします。



4. Bottom Cover

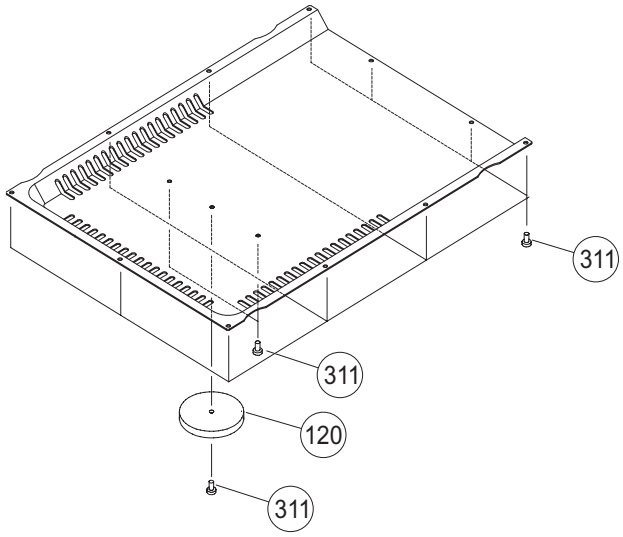
(1) Remove 1 screw (312) fixing the Foot (120).

(2) Remove 13 screws (311).

4. Bottom Cover

(1) Foot (120) を取り付けているねじ (312) をはずします。

(2) ねじ (311) を 13 本はずします。



5. Video unit

(1) Remove 2 screws (311) fixing the Shield Plate (65).

(2) Remove 4 screws (311) fixing the Rear Angle (141).

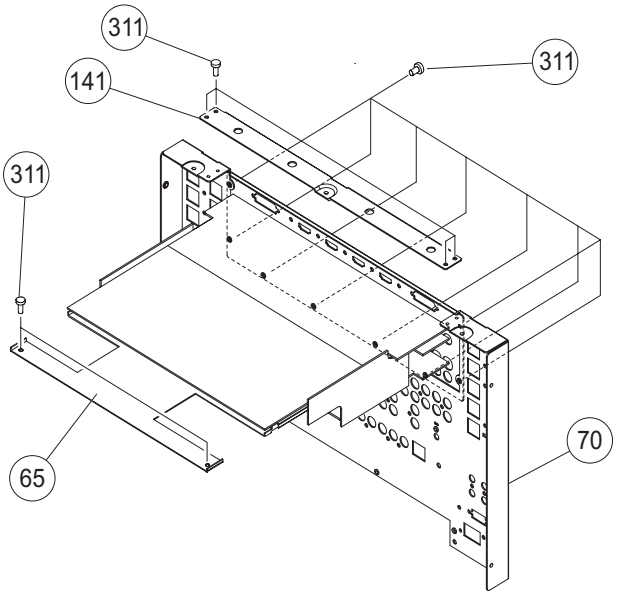
(3) Remove 8 screws (311) fixing the Back Plate (70).

5. Video Unit

(1) Shield Plate (65) を取り付けているねじ(311)を 2 本はずします。

(2) Rear Angle (141) を取り付けているねじ (311) を 4 本はずします。

(3) Back Plate (70) を取り付けているねじ (311) を 8 本はずします。

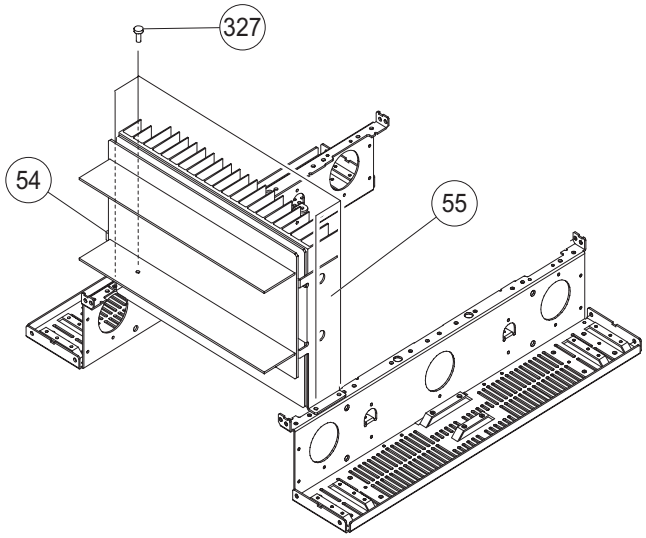


6. Regulator Unit

(1) Remove 4 screws (327) fixing the Radiator Bracket L/R. (L : (54), R : (55))

6. Regulator Unit

(1) Radiator Bracket (L) (54) (R) (55) を取り付けているねじ (327) を 4 本はずします。



7. Power Amp Unit L/R

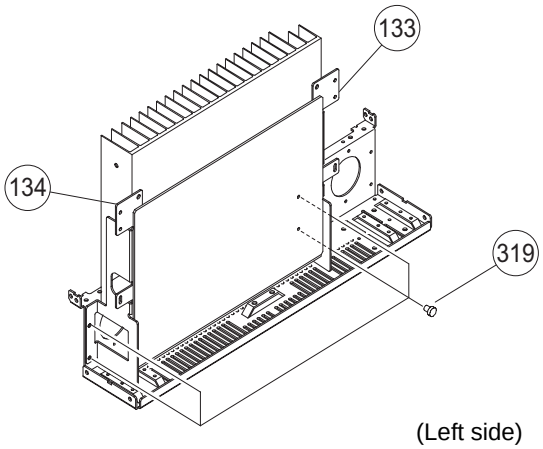
(1) Remove 4 screws (319) fixing the Radiator Bracket L/R. (L : (133), R : (134))

※ Right side is same.

7. Power Amp Unit L/R

(1) Radiator Bracket (L) (133) (R) (134) を取り付けているねじ (319) を 4 本はずします。

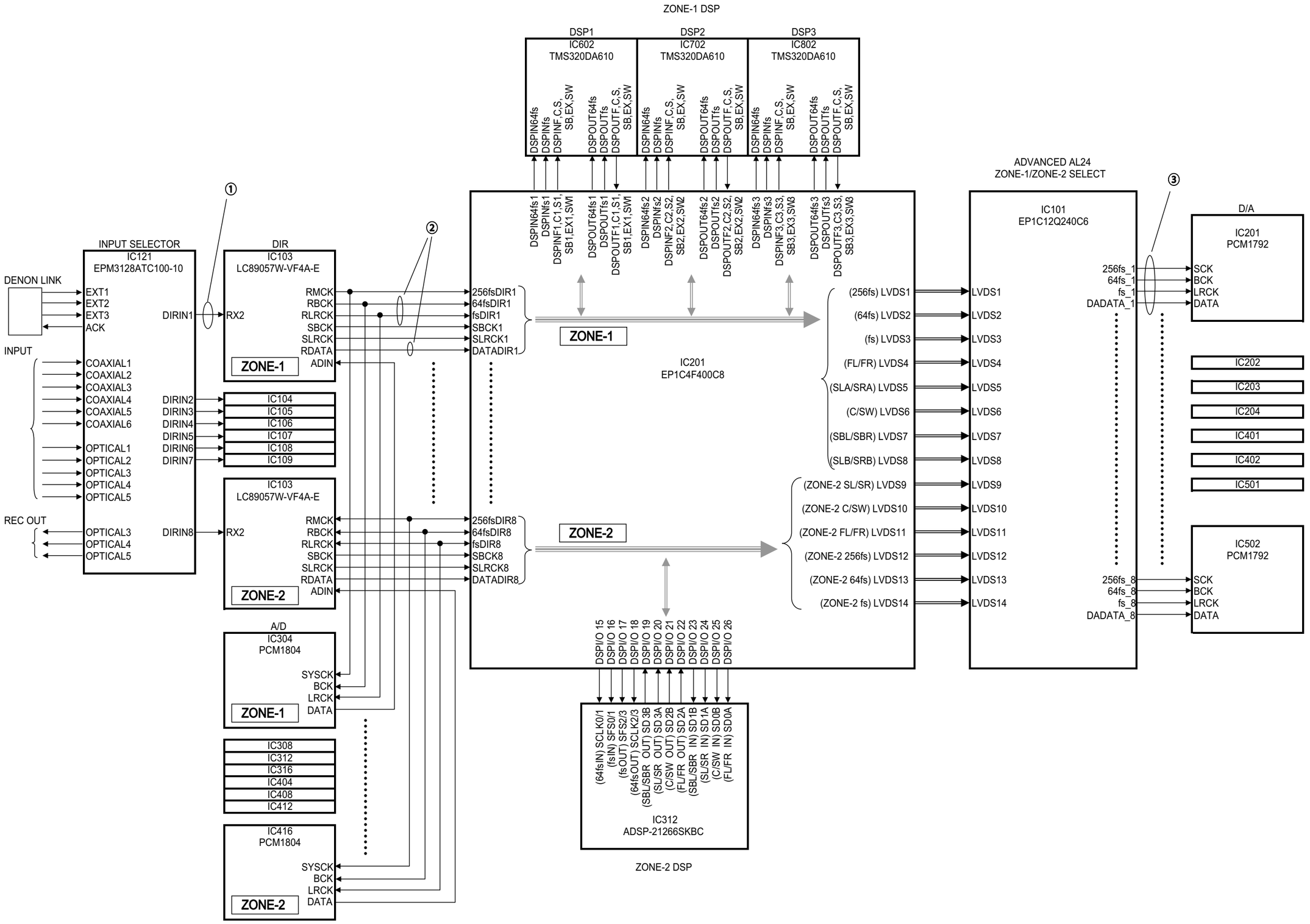
※ (R) 側も同様



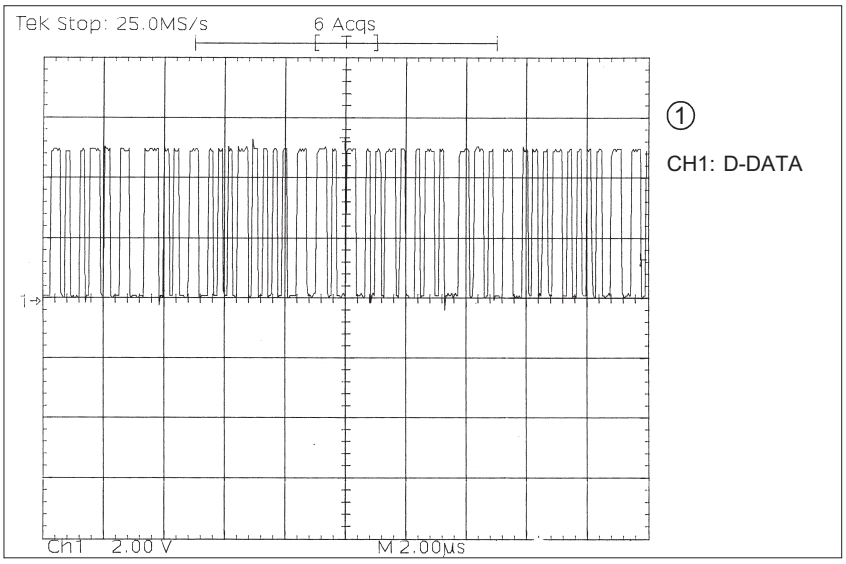
(Left side)

CLOCK FLOW & WAVE FORM IN DIGITAL BLOCK

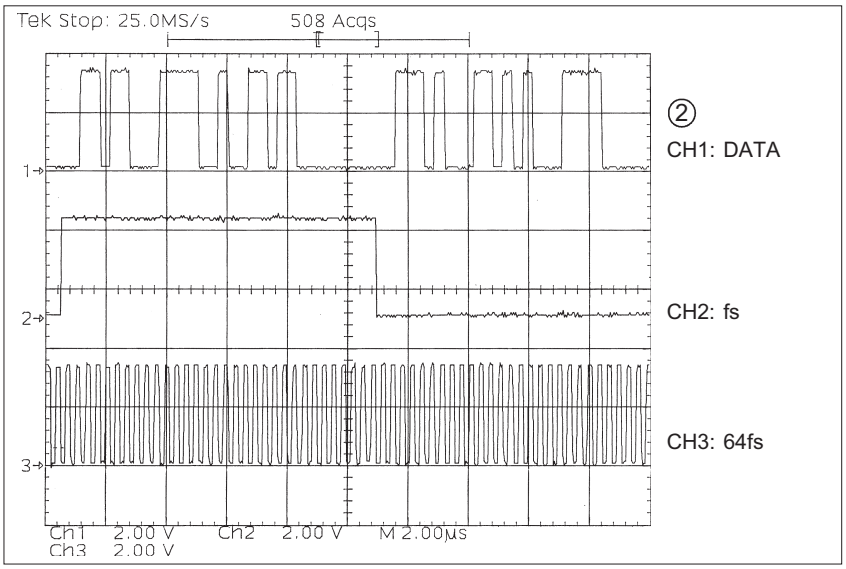
Clock Flow



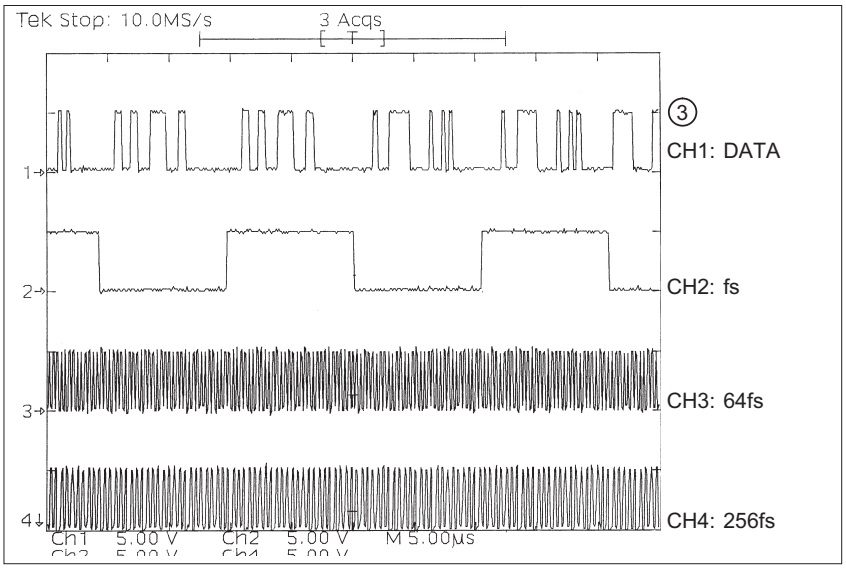
Wave form



①
CH1: D-DATA



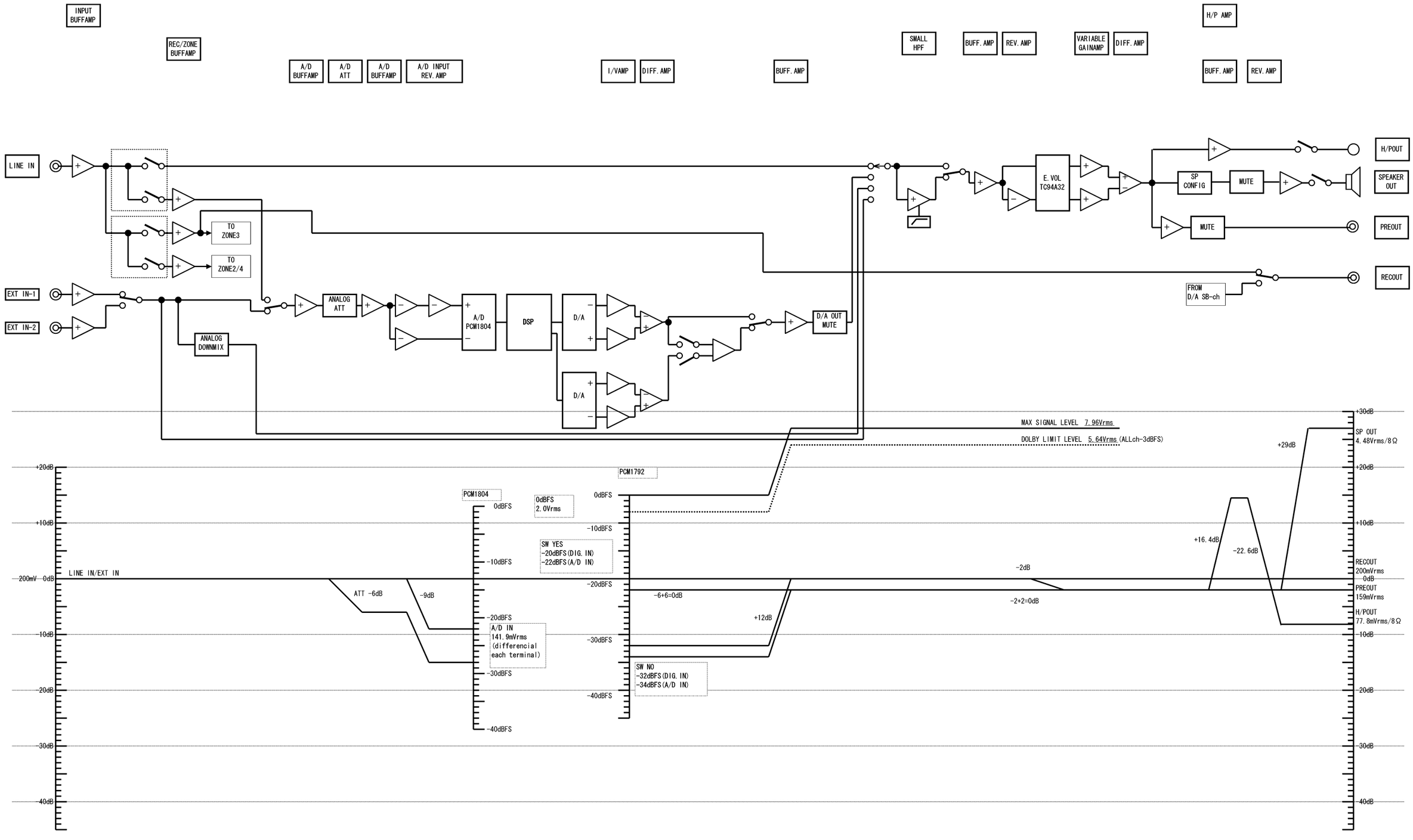
②
CH1: DATA
CH2: fs
CH3: 64fs



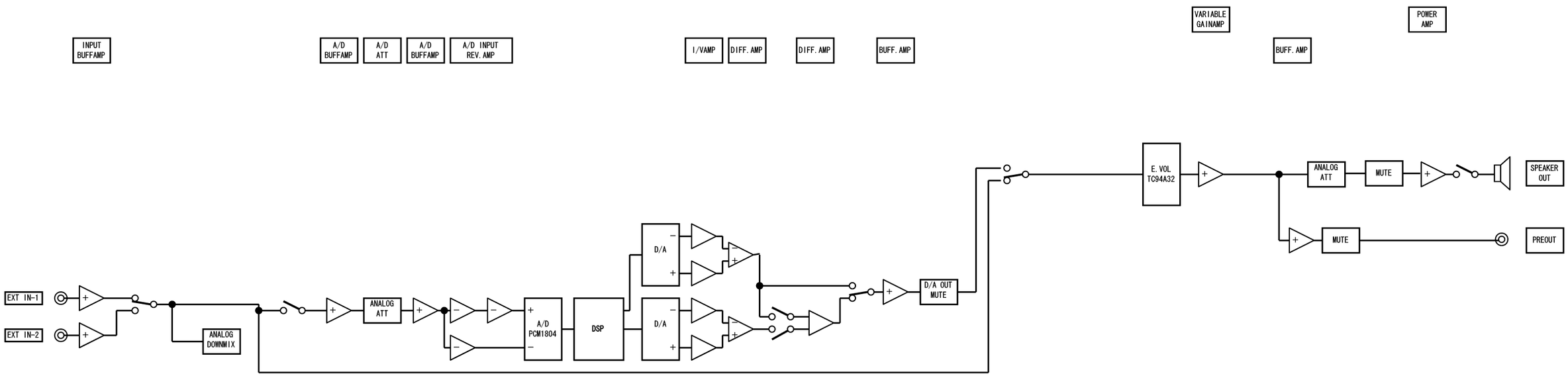
③
CH1: DATA
CH2: fs
CH3: 64fs
CH4: 256fs

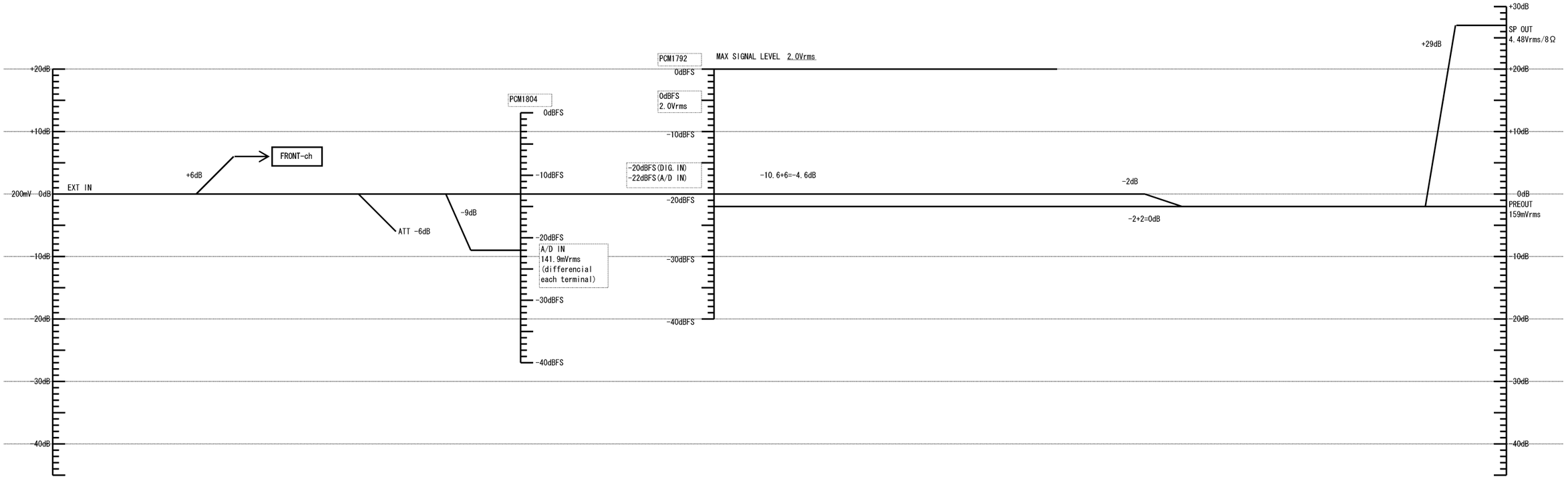
LEVEL DIAGRAMS

FRONT ch

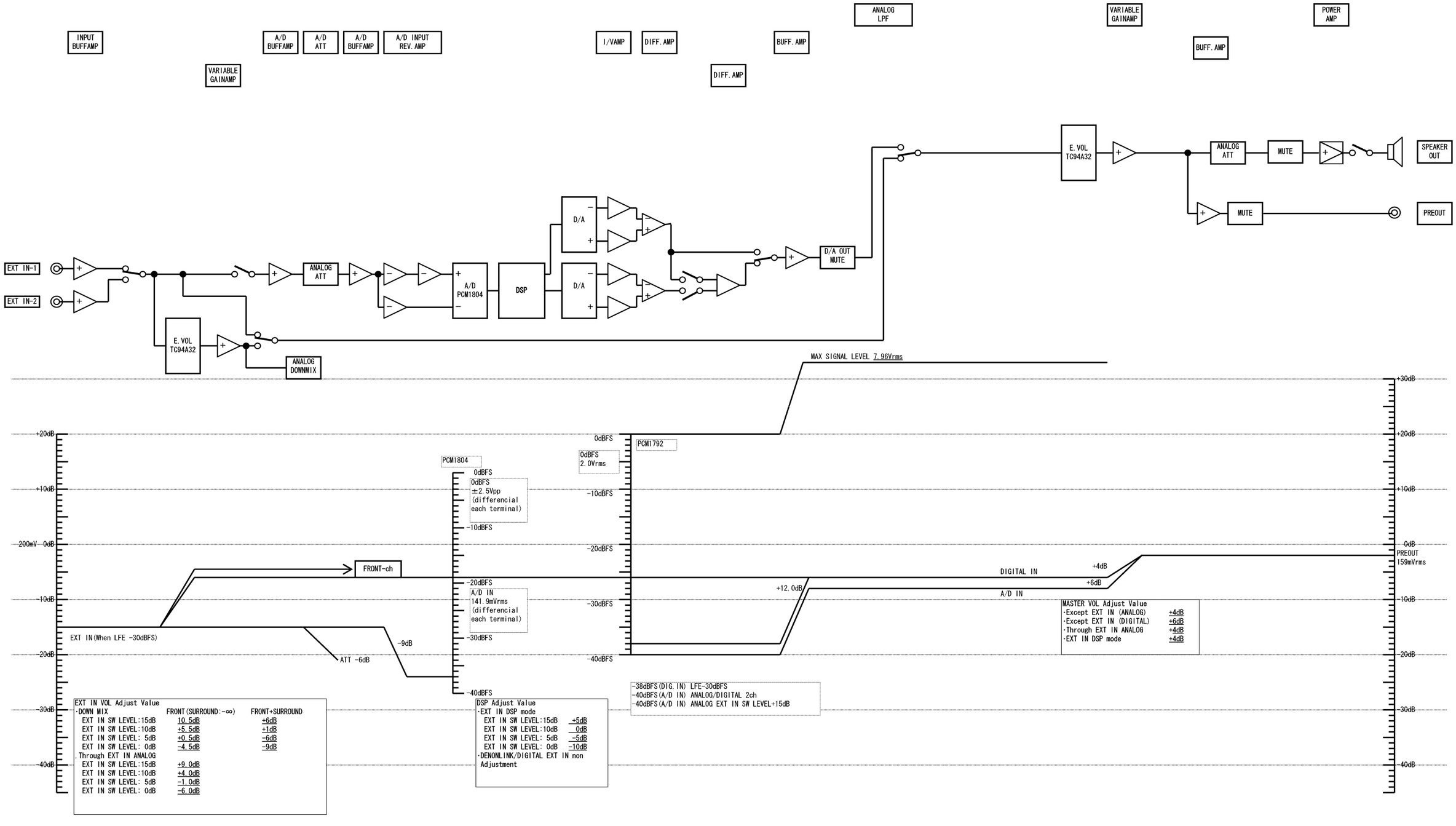


CENTER ch

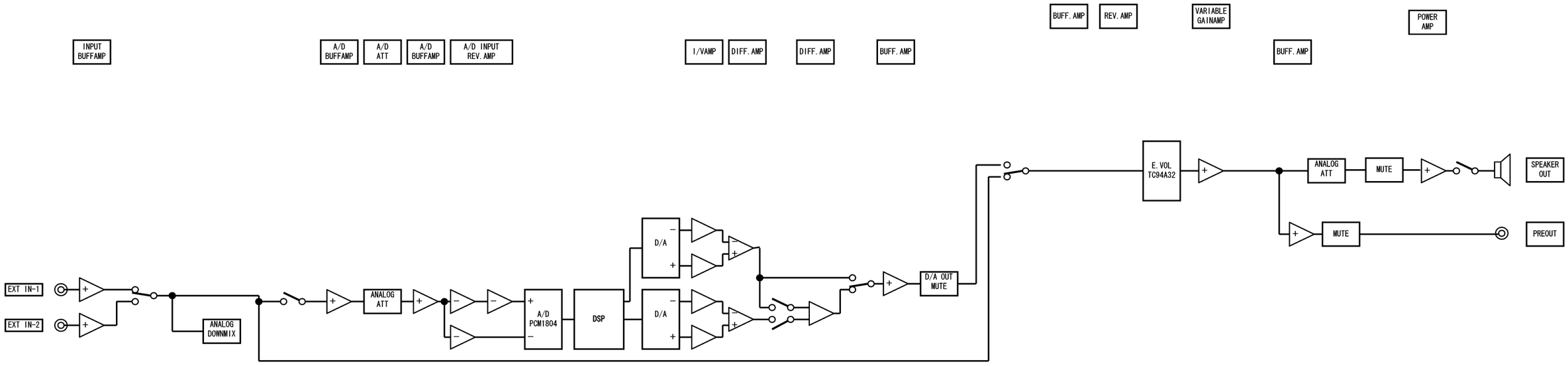

INPUT BUFFAMP
A/D BUFFAMP
A/D ATT
A/D BUFFAMP
A/D INPUT REV. AMP
I/VAMP
DIFF. AMP
DIFF. AMP
BUFF. AMP
VARIABLE GAINAMP
BUFF. AMP
POWER AMP
EXT IN-1
EXT IN-2
ANALOG DOWNMIX
ANALOG ATT
A/D PCM1804
DSP
D/A
D/A
D/A OUT MUTE
E. VOL TC94A32
ANALOG ATT
MUTE
SPEAKER OUT
MUTE
PREOUT


PCM1792
MAX SIGNAL LEVEL 2.0Vrms
PCM1804
FRONT-ch
EXT IN
+6dB
ATT -6dB
-9dB
-20dBFS(DIG. IN)
-22dBFS(A/D IN)
A/D IN
141.9mVrms
(differencial
each terminal)
-10.6+6=-4.6dB
-2dB
-2+2=0dB
+29dB
SP OUT
4.48Vrms/8Ω
PREOUT
159mVrms
+20dB
+10dB
0dB
-10dB
-20dB
-30dB
-40dB
200mV

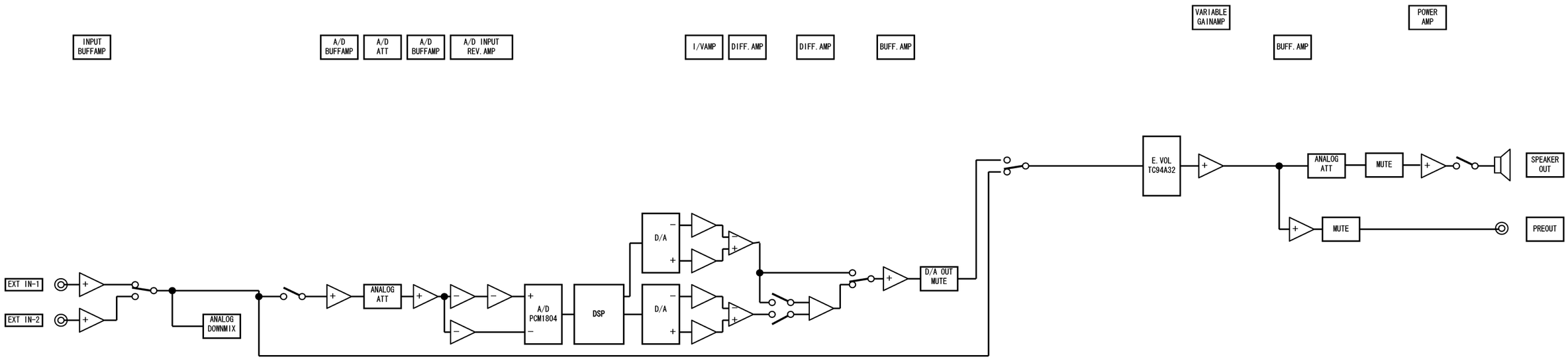
SUBWOOFER ch

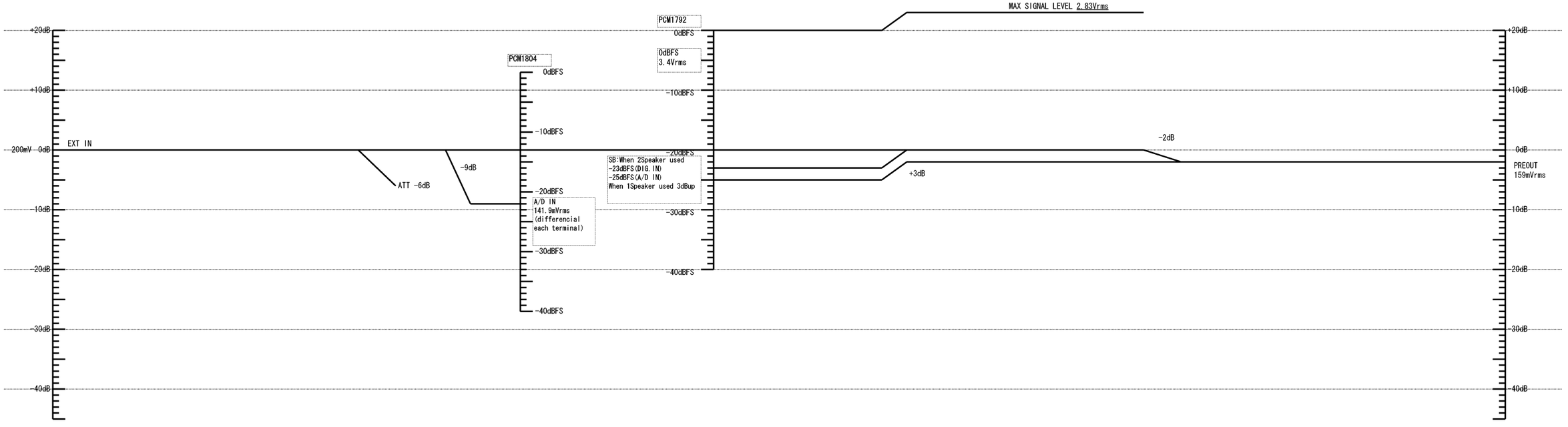


SURROUND ch

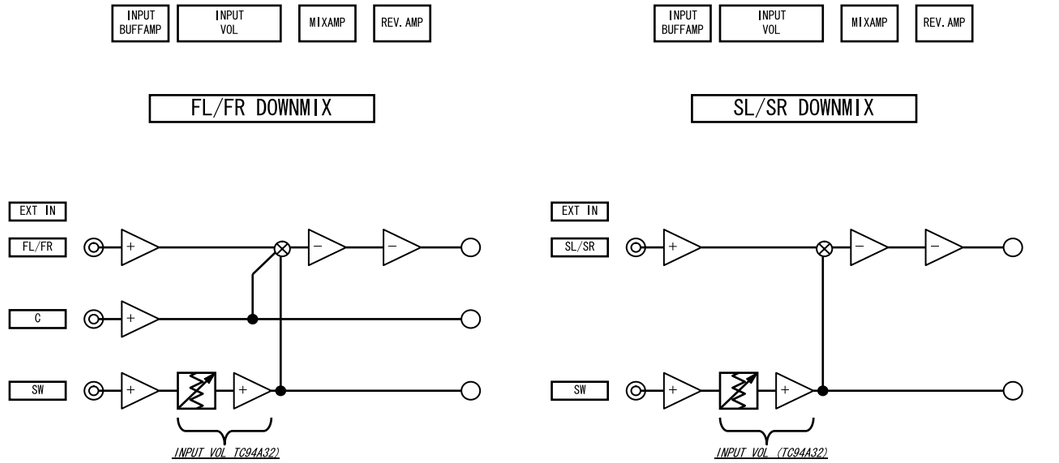

INPUT BUFFAMP
A/D BUFFAMP
A/D ATT
A/D BUFFAMP
A/D INPUT REV. AMP
I/VAMP
DIFF. AMP
DIFF. AMP
BUFF. AMP
BUFF. AMP
REV. AMP
VARIABLE GAINAMP
BUFF. AMP
POWER AMP
EXT IN-1
EXT IN-2
ANALOG DOWNMIX
ANALOG ATT
A/D PCM1804
DSP
D/A
D/A
D/A OUT MUTE
E. VOL TC94A32
ANALOG ATT
MUTE
SPEAKER OUT
MUTE
PREOUT
MAX SIGNAL LEVEL 5.64Vrms
+20dB
+10dB
200mV 0dB
-10dB
-20dB
-30dB
-40dB
EXT IN
ATT -6dB
-9dB
PCM1804
0dBFS
-10dBFS
-20dBFS
-30dBFS
-40dBFS
A/D IN
141.9mVrms
(differencial
each terminal)
PCM1792
0dBFS
0dBFS
3.4Vrms
-10dBFS
-20dBFS
-30dBFS
-40dBFS
Config.1
-23dBFS(DIG.IN)
-25dBFS(A/D IN)
Config.2
-29dBFS(DIG.IN)
-31dBFS(A/D IN)
-10.6+6=-4.6dB
+9dB
+3dB
+9dB
-2dB
-2+2=0dB
+20dB
+10dB
0dB
-10dB
-20dB
-30dB
-40dB
PREOUT
159mVrms

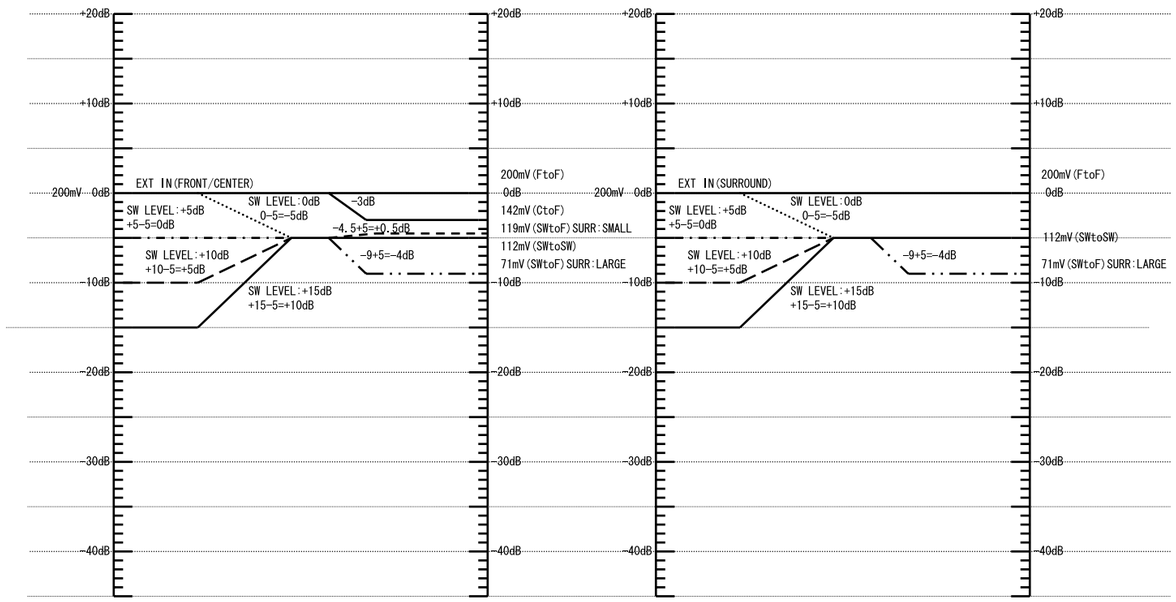
SURROUND BACK ch



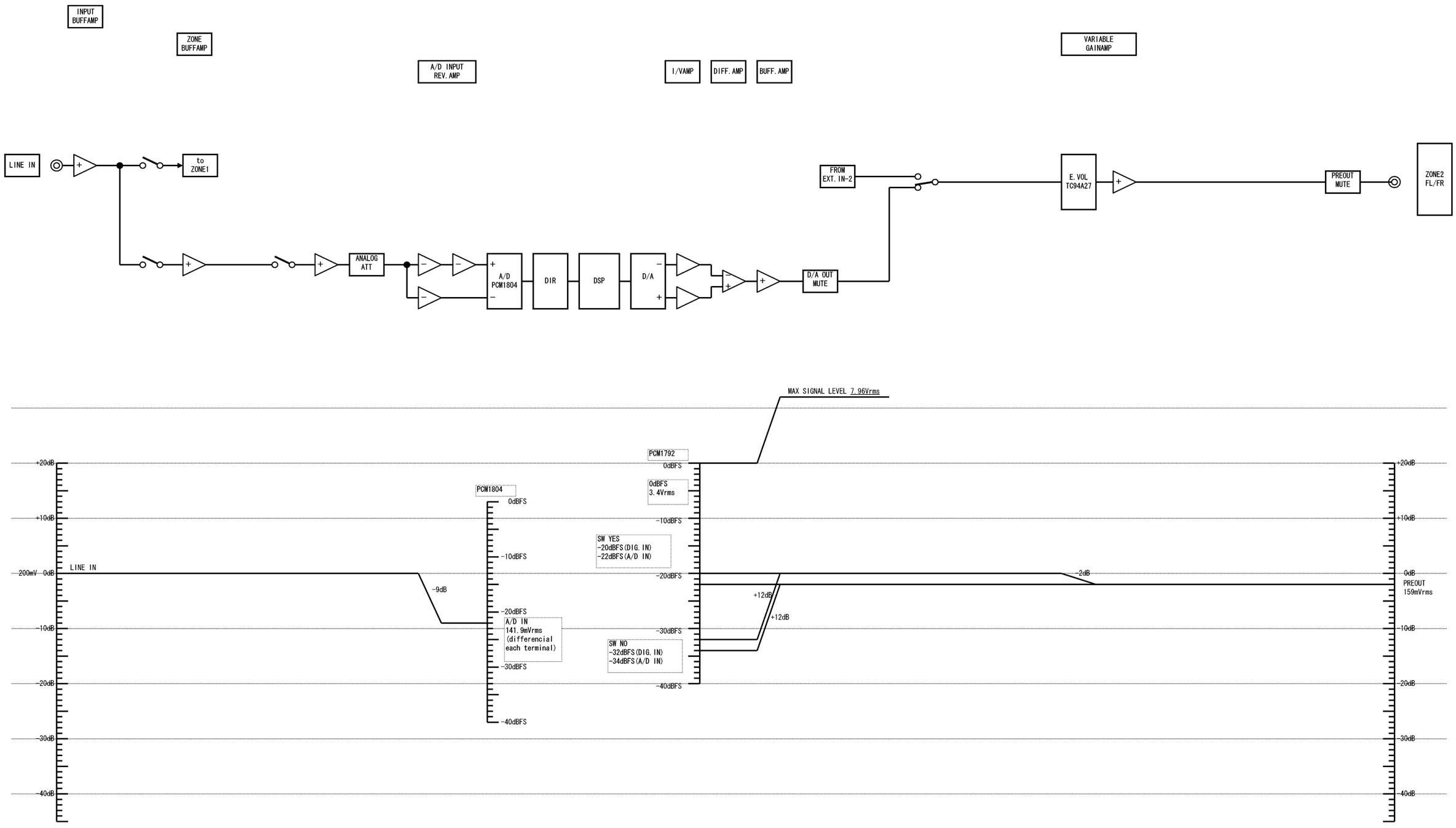


EXT IN ANALOG DOWNMIX

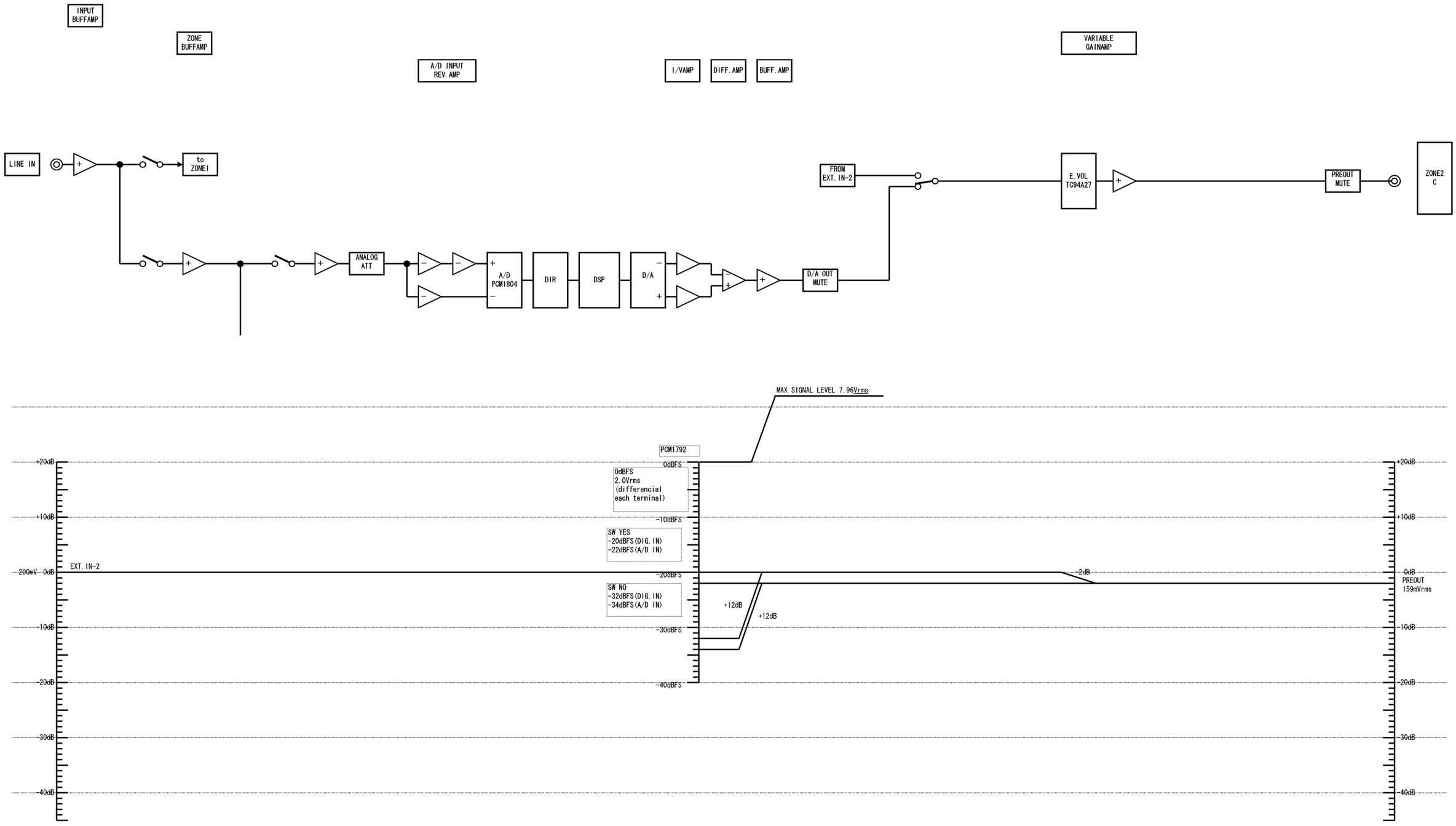




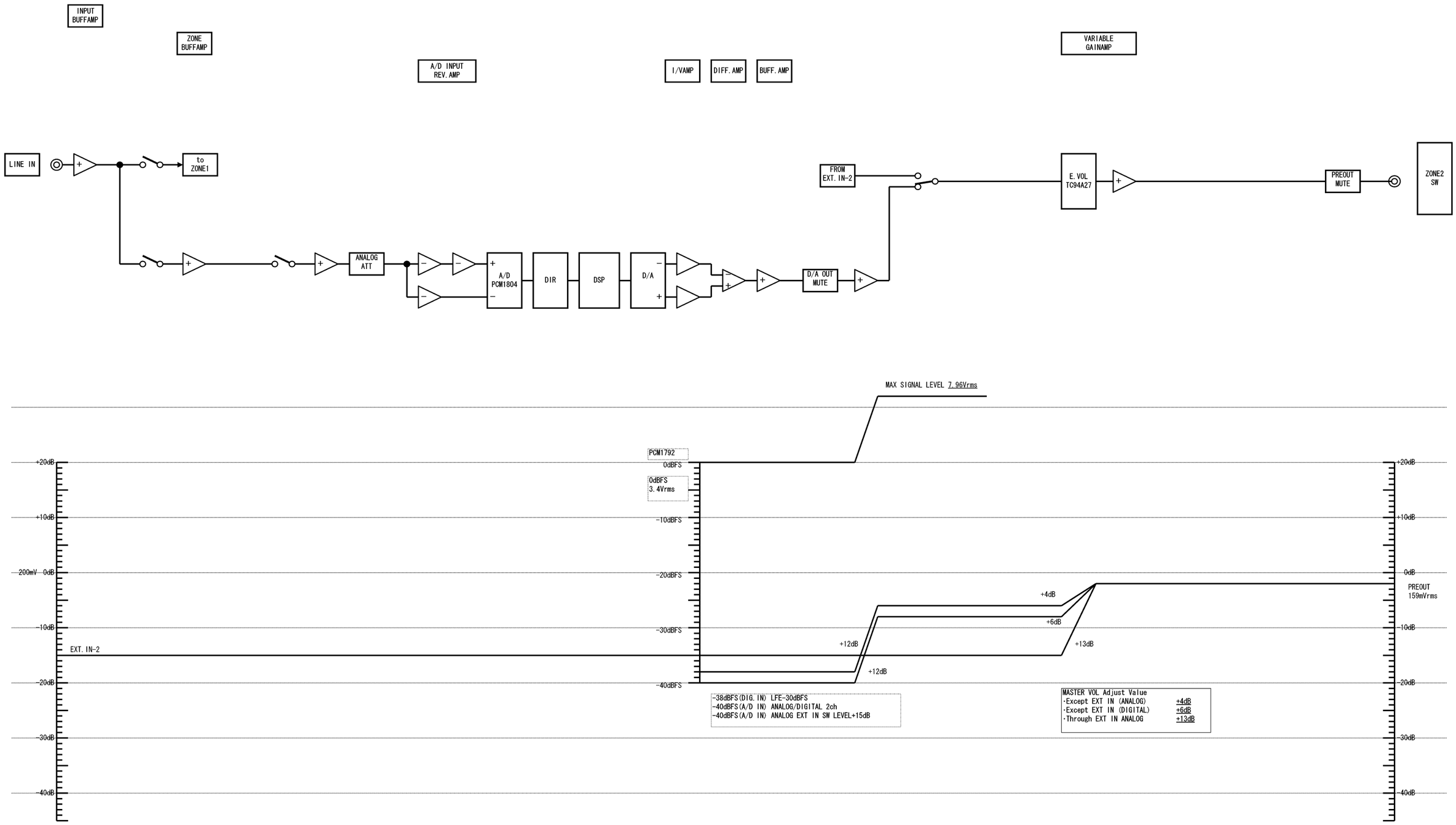
ZONE2 FL/FR ch



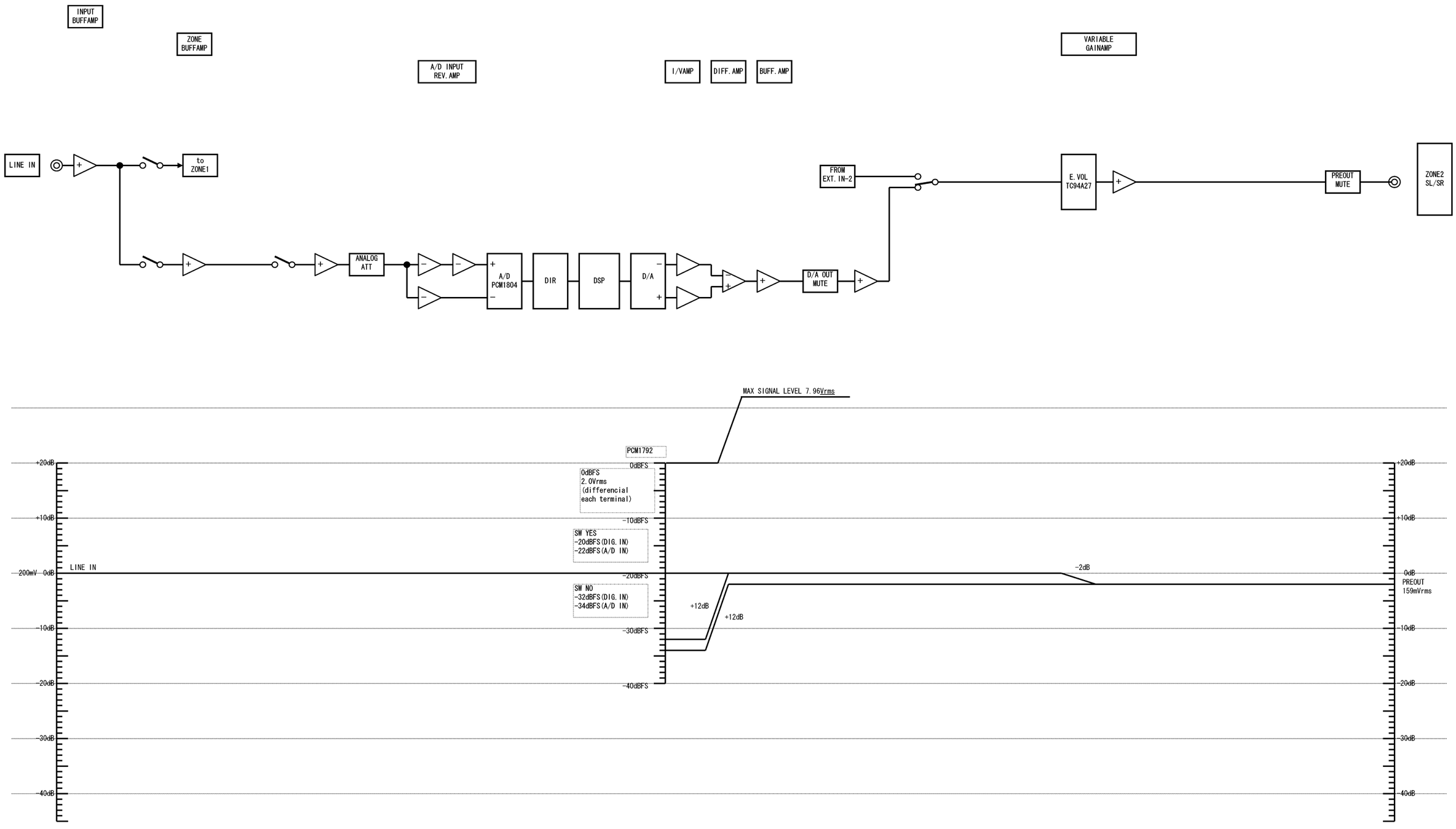
ZONE2 C ch


INPUT BUFFAMP
ZONE BUFFAMP
A/D INPUT REV. AMP
I/VAMP
DIFF. AMP
BUFF. AMP
VARIABLE GAINAMP
LINE IN
to ZONE1
ANALOG ATT
A/D PCM1804
DIR
DSP
D/A
D/A OUT MUTE
FROM EXT. IN-2
E. VOL TC94A27
PREOUT MUTE
ZONE2 C
MAX SIGNAL LEVEL 7.96Vrms
PCM1792
0dBFS
OdBFS
2.0Vrms
(differencial
each terminal)
-10dBFS
SW YES
-20dBFS(DIG. IN)
-22dBFS(A/D IN)
-20dBFS
SW NO
-32dBFS(DIG. IN)
-34dBFS(A/D IN)
-30dBFS
-40dBFS
+12dB
+12dB
-2dB
+20dB
+10dB
200mV 0dB
EXT. IN-2
-10dB
-20dB
-30dB
-40dB
0dB
PREOUT
159mVrms

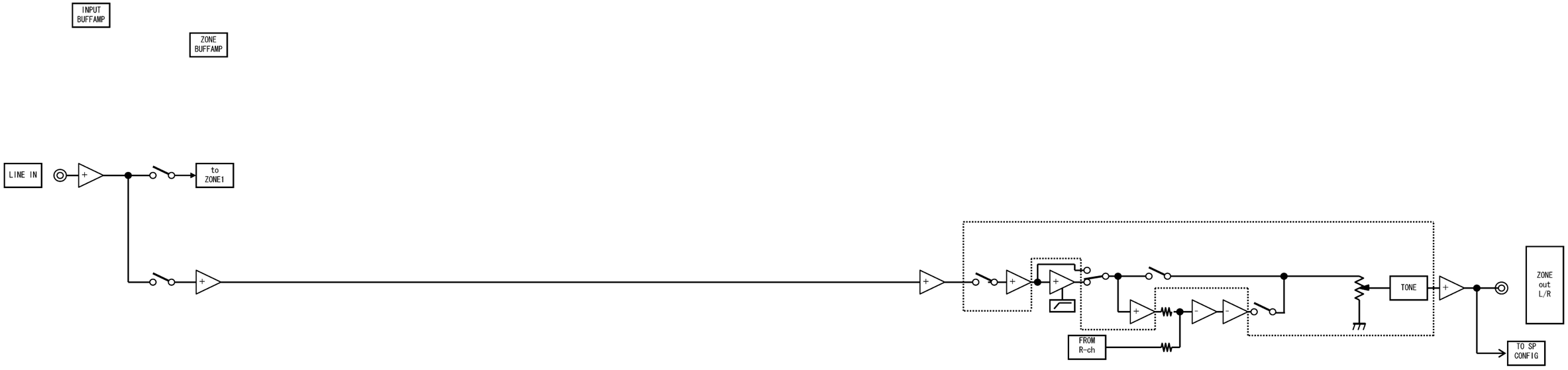
ZONE2 SW ch

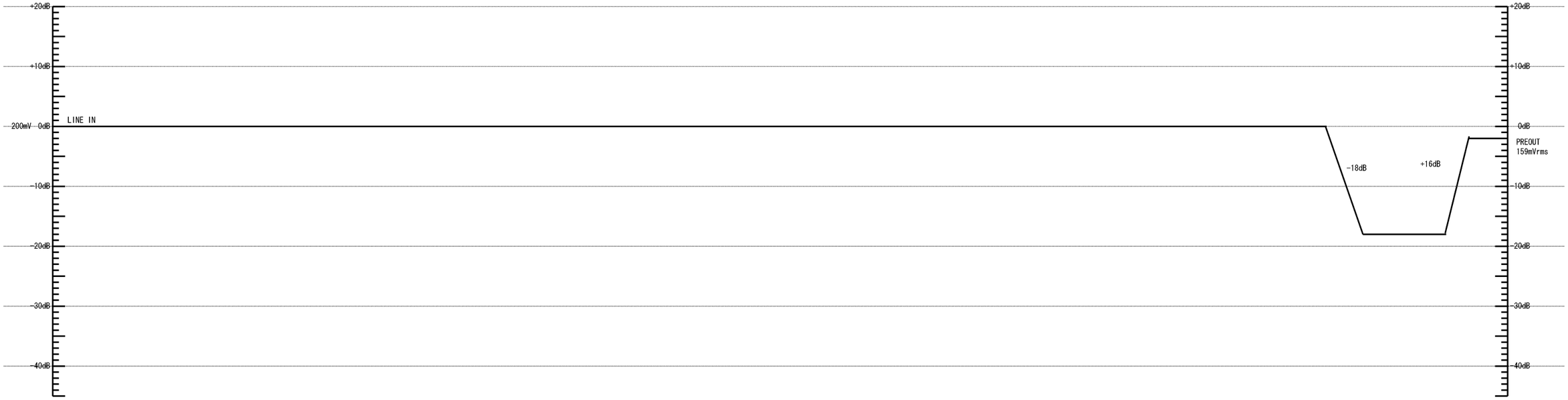

INPUT BUFFAMP
ZONE BUFFAMP
A/D INPUT REV. AMP
I/VAMP
DIFF. AMP
BUFF. AMP
VARIABLE GAINAMP
LINE IN
to ZONE1
ANALOG ATT
A/D PCM1804
DIR
DSP
D/A
D/A OUT MUTE
FROM EXT. IN-2
E. VOL TC94A27
PREOUT MUTE
ZONE2 SW
MAX SIGNAL LEVEL 7.96Vrms
PCM1792
0dBFS
0dBFS 3.4Vrms
-10dBFS
-20dBFS
-30dBFS
-40dBFS
+20dB
+10dB
200mV 0dB
-10dB
-20dB
-30dB
-40dB
EXT. IN-2
+4dB
+6dB
+12dB
+13dB
+12dB
PREOUT 159mVrms
-38dBFS(DIG. IN) LFE-30dBFS
-40dBFS(A/D IN) ANALOG/DIGITAL 2ch
-40dBFS(A/D IN) ANALOG EXT IN SW LEVEL+15dB
MASTER VOL Adjust Value
·Except EXT IN (ANALOG) +4dB
·Except EXT IN (DIGITAL) +6dB
·Through EXT IN ANALOG +13dB

ZONE2 SL/SR ch

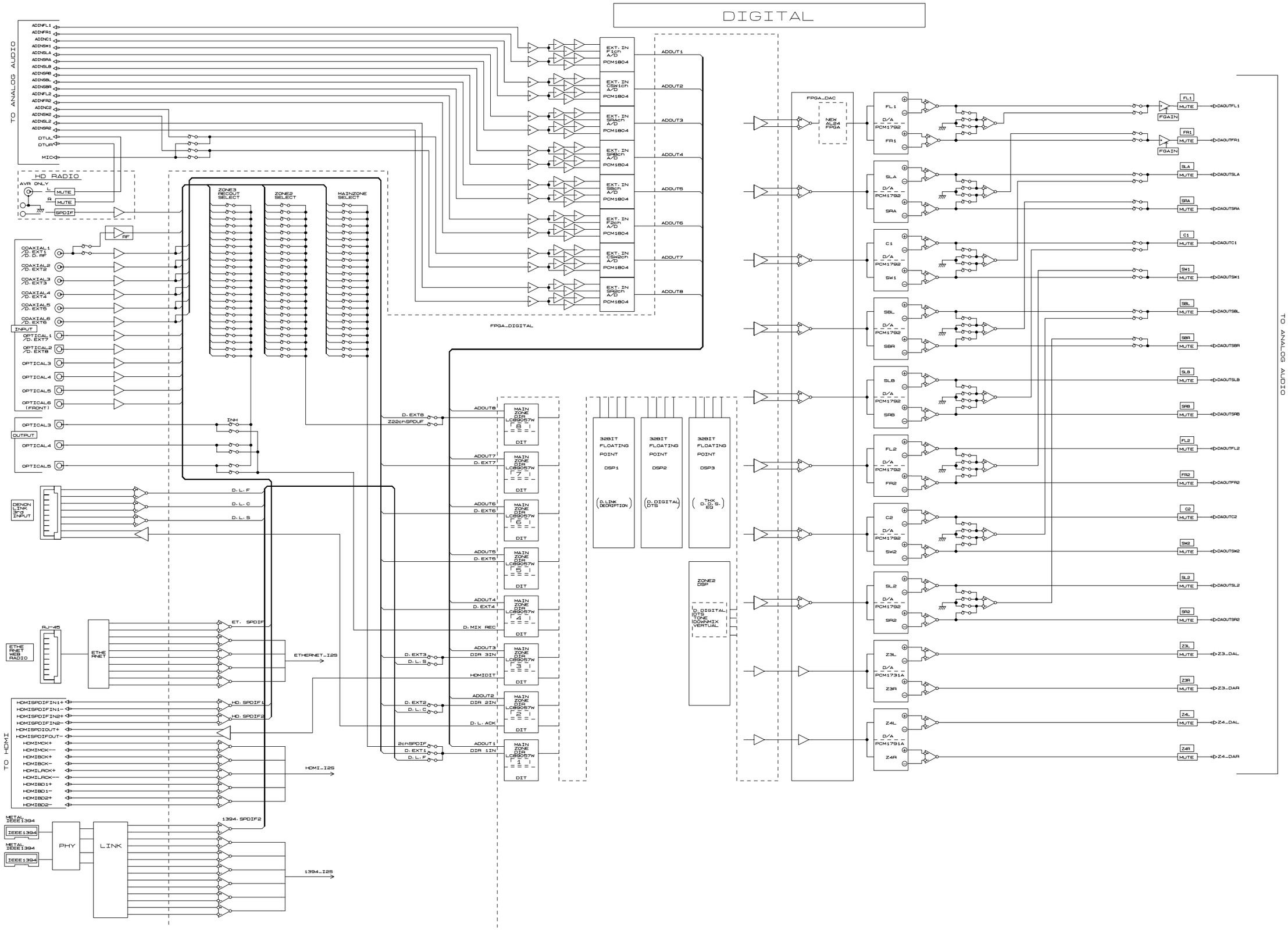


ZONE2/ 3/4 L/R

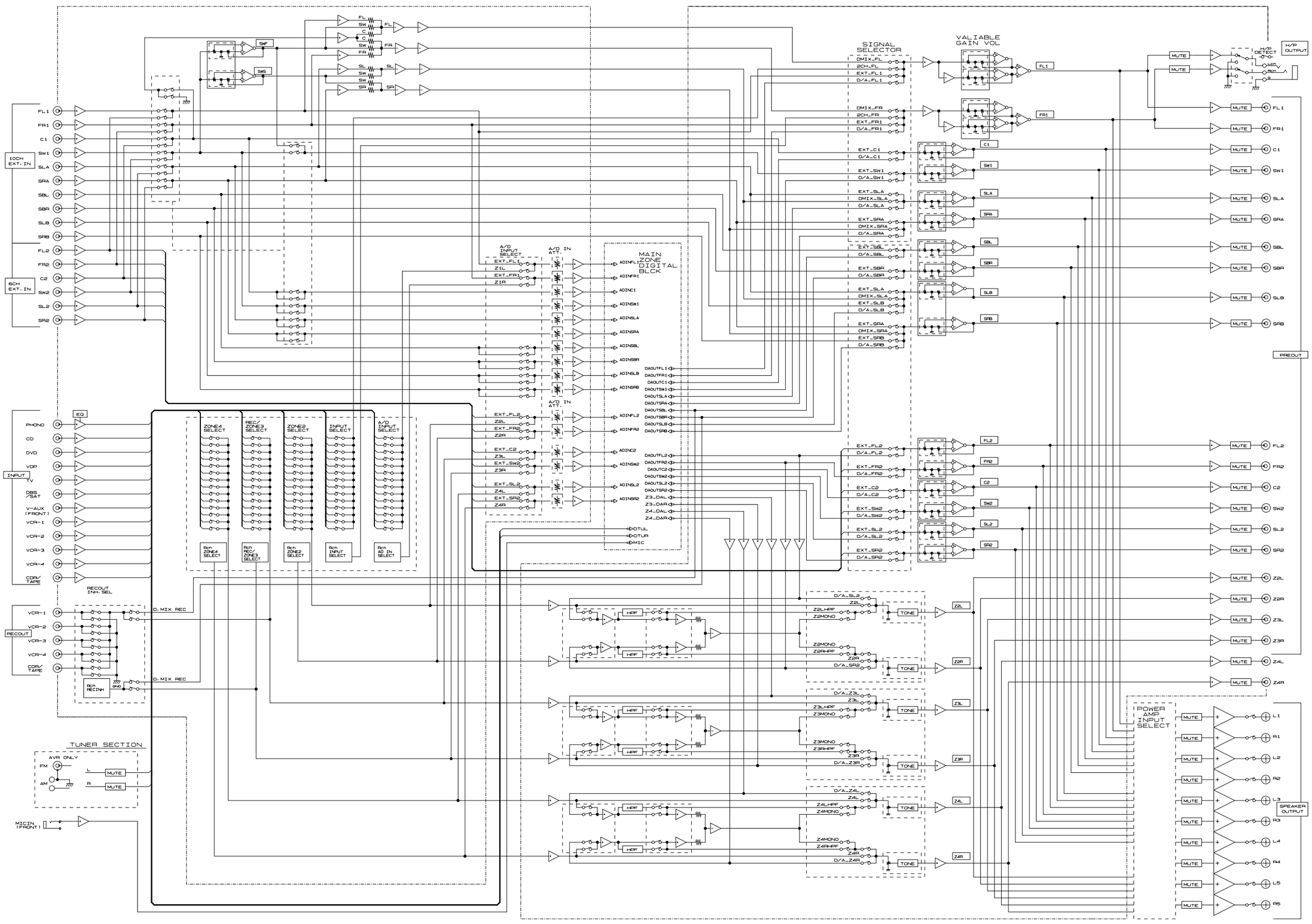

INPUT BUFFAMP
ZONE BUFFAMP
LINE IN
to ZONE1
TONE
ZONE out L/R
FROM R-ch
TO SP CONFIG


+20dB
+10dB
200mV 0dB
-10dB
-20dB
-30dB
-40dB
LINE IN
-18dB
+16dB
PREOUT
159mVrms

BLOCK DIAGRAMS

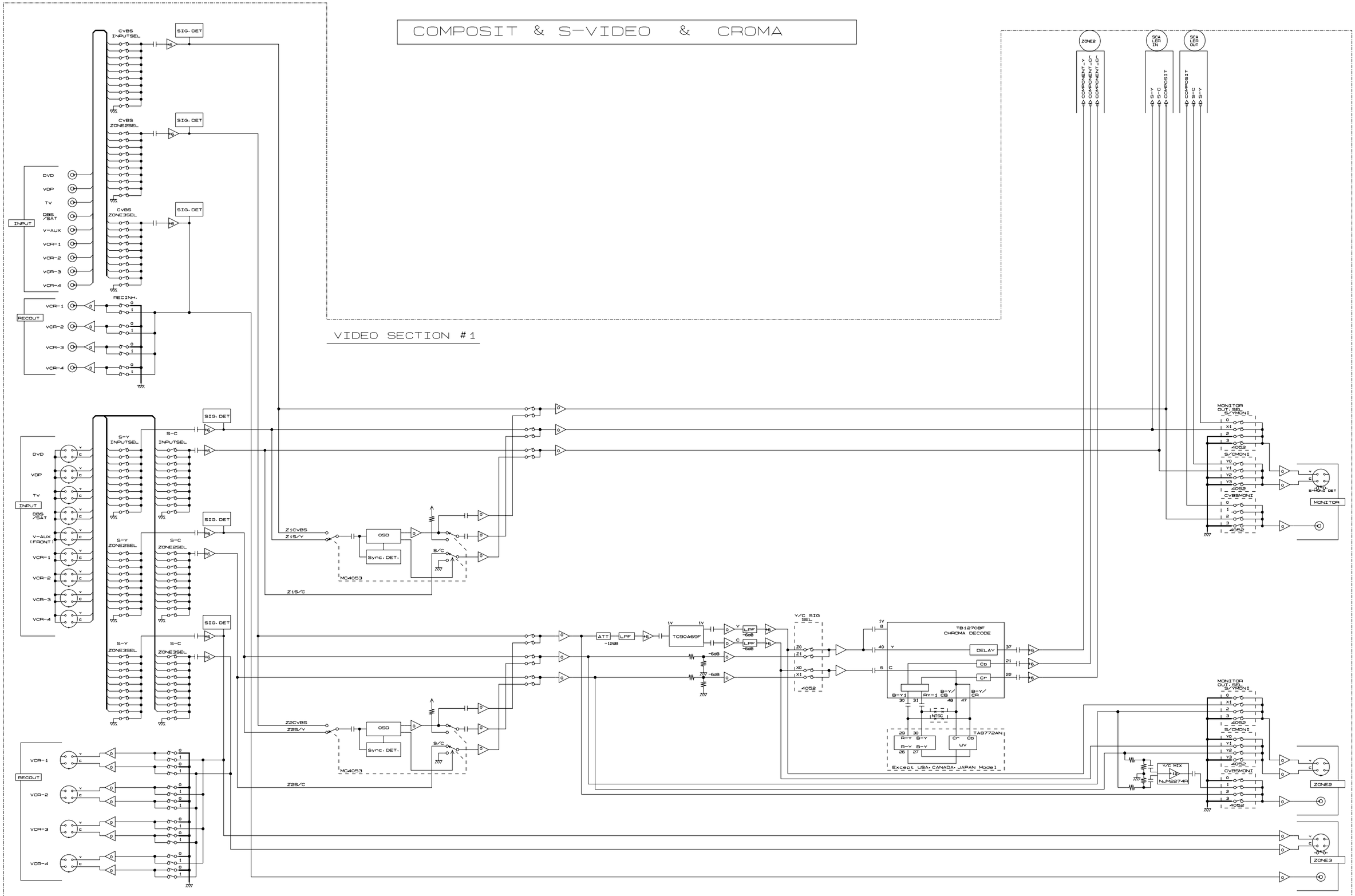


ANALOG AUDIO



COMPOSIT & S-VIDEO & CROMA

VIDEO SECTION #1



COMPONENT VIDEO & HDMI &SCALER

COMPONENT VIDEO SECTION #1

INPUT
VIDEO 1 Y Pb/Cb Pr/Cr
VIDEO 2 Y Pb/Cb Pr/Cr
VIDEO 3 Y Pb/Cb Pr/Cr
VIDEO 4 Y Pb/Cb Pr/Cr
VIDEO 5 Y Pb/Cb Pr/Cr
VIDEO 6 Y Pb/Cb Pr/Cr
ZONE1 COMP. SIG. DET
ZONE2 COMP. SIG. DET
ZONE1SEL
ZONE2SEL
Pb/Cb
Pr/Cr
480i ~ 1080i
MONITOR1 Y Pb/Cb Pr/Cr
MONITOR2 Y Pb/Cb Pr/Cr
ZONE2 Y Pb/Cb Pr/Cr

DIGITAL VIDEO SECTION

E2PROM
HDMI IN1
HDMI IN2
HDMI IN3
DVI IN
HDMI RECEIVER
HDMI&DVI RECEIVER
YUV20/ RGB24
I2S SPDIF
HDMI TRANSMITER
DVI TRANSMITER
HDMI MONITOR
DVI MONITOR
HDMI_DIGITAL_AUDIO

DIGITAL VIDEO SECTION #2

E2PROM
HDMI IN1
HDMI IN2
HDMI IN3
DVI IN
HDMI RECEIVER
HDMI&DVI RECEIVER
YUV20/ RGB24
HDMI TRANSMITER
DVI TRANSMITER
HDMI MONITOR
DVI MONITOR
COMPONENT_Y
COMPONENT_Cb
COMPONENT_Cr
VIDEO ENCODER PIXELWORKS QR ADI
S-Y
S-C
COMP.
YUV20
VIDEO I/P CONVERTOR FLI2310
BUS SWITCHER
I2S SPDIF
HDMI_DIGITAL_AUDIO

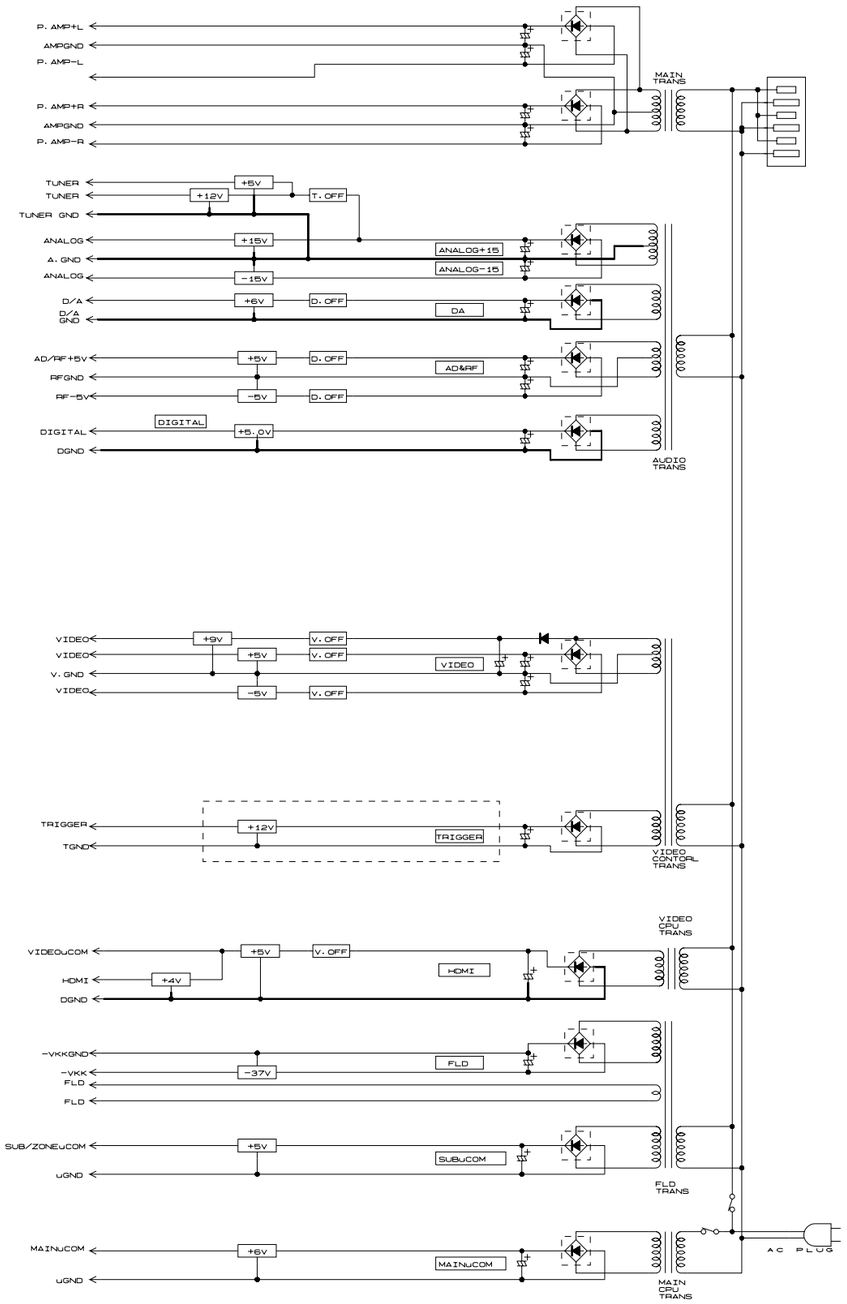
COMPONENT SCALER SECTION

COMPONENT_Y
COMPONENT_Cb
COMPONENT_Cr
VIDEO DECODER MATSUSHITA
S-Y
S-C
COMP.
YUV20
VIDEO I/P CONVERTOR FLI2310
VIDEO ENCODER COMPONENT ADI
Y
Cb
Cr
VIDEO ENCODER S&COMPOSIT ADI
CONP.
SCALER IN
SCALER OUT
ZONE2

GUI SECTION #3

S-Y
S-C
CVBS
VIDEO ENCODER PIXELWORKS QR ADI
ITUR656
GUI
RGB16
RGB TO YUV ENCODER
YUV16
VIDEO DECODER
ANAROG_R
ANAROG_G
ANAROG_B

P. SUPPLY


P. AMP+L
AMPGND
P. AMP-L
P. AMP+R
AMPGND
P. AMP-R
MAIN TRANS
TUNER
TUNER
TUNER GND
+8V
+12V
T. OFF
ANALOG
A. GND
ANALOG
+15V
-15V
ANALOG+15
ANALOG-15
D/A
D/A GND
+6V
D. OFF
DA
AD/RF+8V
RFGND
RF-8V
+5V
-5V
D. OFF
AD&RF
DIGITAL
DGND
DIGITAL
+5.0V
AUDIO TRANS
VIDEO
VIDEO
V. GND
VIDEO
+9V
+5V
-5V
V. OFF
VIDEO
TRIGGER
TGND
+12V
TRIGGER
VIDEO CONTORL TRANS
VIDEO CPU TRANS
VIDEOμCOM
HDMI
DGND
+5V
+4V
V. OFF
HDMI
-VKKGND
-VKK
FLD
FLD
-37V
FLD
SUB/ZONEμCOM
μGND
+5V
SUBμCOM
FLD TRANS
MAINμCOM
μGND
+6V
MAINμCOM
MAIN CPU TRANS
AC PLUG

ADJUSTMENT

AUDIO Section

IDLING CURRENT (1U-3637-1)

Required measurement equipment: DC Voltmeter

1. PREPARATION

(1) Avoid direct blow from an air conditioner or an electric fan, and adjust the unit at normal room temperature 15 °C ~ 30 °C (59 °F ~ 86 °F).

(2) Presetting

- POWER (Power source switch) OFF
- SPEAKER (Speaker terminal) No load
  (Do not connect speaker, dummy resistor, etc.)

2. ADJUSTMENT

(1) Remove side cover and set VR101, VR201, VR301, VR401, VR501 on 1U-3637-1 (Power Unit) at fully counterclockwise (◯).

(2) Connect DC Voltmeter to test points (CN103, CN203, CN303, CN403, CN503 ① ③ pin).

(3) Connect power cord to AC Line, and turn power switch "ON".

(4) Turn power switch "ON" with pressing [GAME] and [SRROUND BACK] buttons in the door of front panel.

(5) Presetting.
MASTER VOLUME : "---" counterclockwise (◯ min.)
MODE : 9CH STEREO
FUNCTION : CD

(6) Allow 2 minutes, and turn VR101 clockwise (◯) to adjust the TEST POINT voltage to 3.5 mV ± 0.2 mV DC.

(7) After 10 minutes from preset, turn VR101 to set the voltage to 4.0 mV ± 0.2 mV DC.

(8) Adjust the Variable Resistors of other channels in the same way.

(9) After 5 minutes from (7), turn VR101 to set the voltage to 4.0 m ± 0.2 mV DC.

(10) Adjust the Variable Resistors of other channels in the same way.

調整

オーディオセクション

アイドリング電流の調整 (1U-3637-1)

調整に必要な測定器： DC Voltmeter

1. 準備

(1) セットをクーラ、扇風機のそばなど風通しの良い場所を避け、通常の使用状態に置きます。セットの周囲温度は 15 ～ 30 ℃、湿度は常湿とします。

(2) プリセット

- 電源スイッチ OFF
- スピーカー端子 無負荷
  (スピーカー・ダミー抵抗器などを接続しない。)

2. 調整

(1) サイドカバーをはずし、1U-3637-1（パワーユニット）の VR101, VR201, VR301, VR401, VR501 を反時計方向 (◯) に回し切った状態にセットします。

(2) テストポイント (CN103, CN203, CN303, CN403, CN503 の① ③ pin) に DC Voltmeter を接続します。

(3) 電源コードを AC ライン（95 ～ 105V の範囲であること）に接続し、電源スイッチを "ON" にします。

(4) フロントパネルのドア内にある「GAME」ボタンと「SURROUND BACK」ボタンを押しながら電源スイッチを "ON" にします。

(5) ON 後、次のようにセットします。

- MASTER VOLUME（音量調節つまみ）→反時計方向 (◯) に回す、最小の状態にする。
- SPEAKER（スピーカー端子）→無負荷（スピーカー、ダミー抵抗器などを接続しない。）

  MODE ： 9CH STEREO
  FUNCTION ： CD

(6) 2 分以内に VR101 を時計方向 (◯) に回しテストポイントの電圧を次のように調整します。

  3.5mV ± 0.2mV DC

(7) 予備調整から 10 分後 VR101 を回し、次のように電圧を設定します。

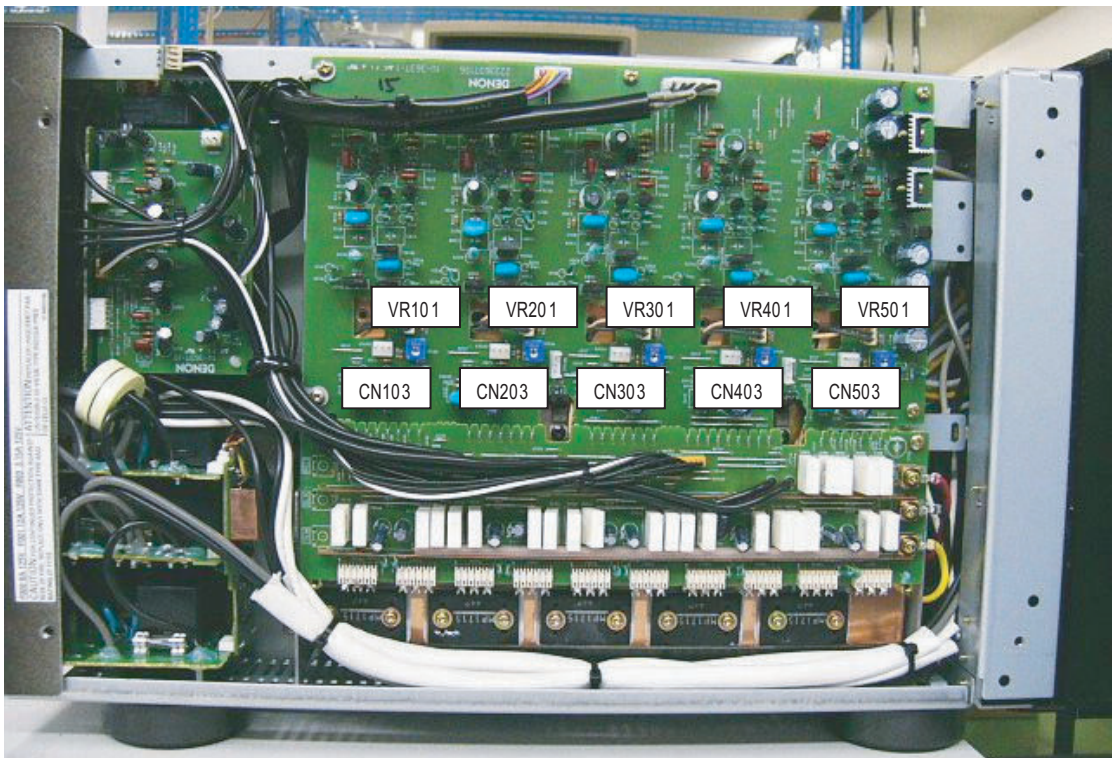
  4.0mV ± 0.2mV DC

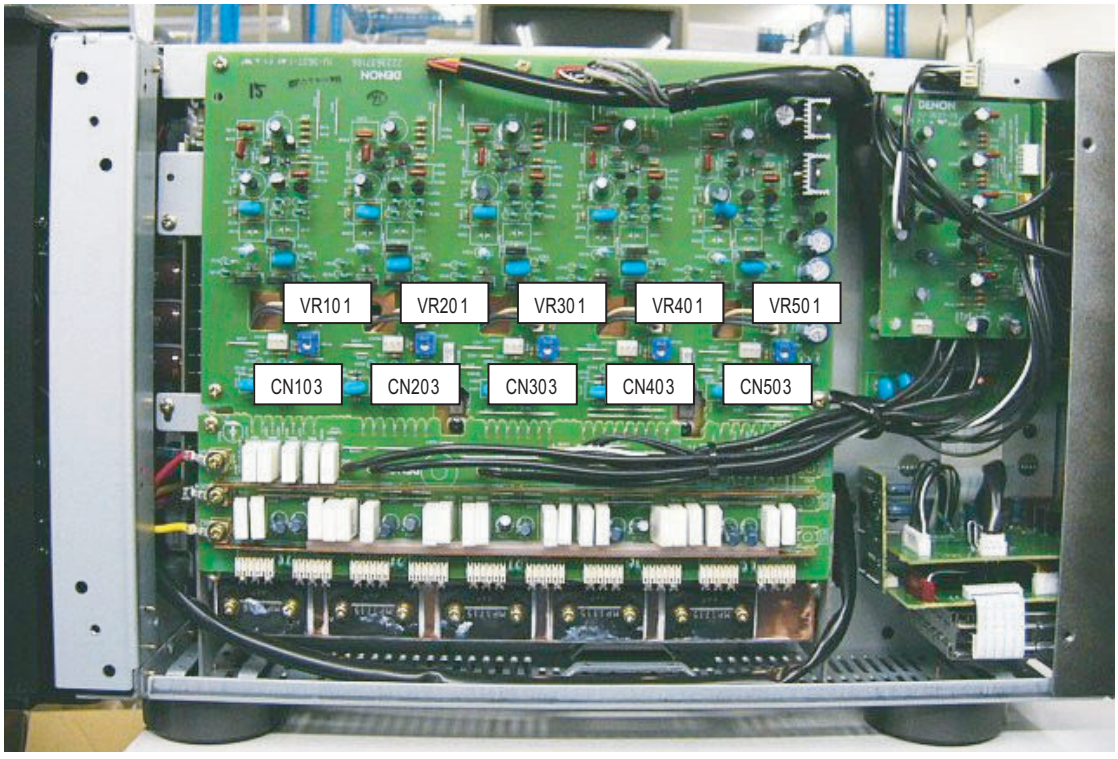
(8) 同じ方法で各チャネルの可変抵抗を調整します。

(9) (7) 項設定から 5 分後 VR101 を回し、次のように電圧を設定します。

  4.0mV ± 0.2mV DC

(10) 同じ方法で各チャネルの可変抵抗を調整します。





Audio Section

VIDEO Section

I. MAIN ZONE

1. SETTING

(1) Connect the oscilloscope to the Y-signal and C-signal of S MONITOR OUT terminal and each terminate at 75 Ohms.

(2) Connect the oscilloscope to the Y-signal, P_B-signal and C_B-signal, P_R-signal and C_R-signal of COMPONENT MONITOR OUT2 terminal and each terminate at 75 Ohms.
※ **Use the 75 Ohms resistance must be 1%**

(3) DVD test disc : DVDT-S01

(4) COMPONENT VIDEO OUT of DVD player is connected to COMPONENT IN-5.

2. BEFORE ADJUSTMENT

2.1. Setting the Oscilloscope as below.

(1) P_B/C_B, P_R/C_R, C
(a) TIME/DIV : 10μs
(b) VOLT/DIV : 100mV
(Use the probe : x10)

(2) Y
(a) TIME/DIV : 10μs
(b) VOLT/DIV : 200mV
(Use the probe : x10)

Power on. Power Supply

USA & Canada	:	120V
Europe	:	230V
Japan	:	100V
China & Korea	:	220V

2.2. Setup the DVD player and confirmation of the stators

(1) Set to "INTERLACED" mode at the COMPONENT OUT.

(2) Confirm the DVD player's out put level is equal as the item 2.4. in following.

2.3. Preparation

(1) Push [POWER] button with pressing [GAME] and [SURROUND BACK] buttons.

(2) Confirm "0.0dB" appearing on the FL display.

(3) Turn the FUNCTION knob to select "VCR-1" input.

(4) Push [VIDEO ON/OFF] button twice to select "VIDEO OFF". (It becomes Adjustment mode.)

(5) Push [OPEN/CLOSE] button of DVD player, then open the Disc Tray.
Set DVD test disc (DVDT-S01) on the Disc Tray, and then push [CLOSE] button.

(6) DVD player FL display appear "STOP", push [PLAY] button to playback DVD.

(7) Push the [DISPLAY] button of remote control of DVD player unit and then appear the ON-Screen Display (GUI) on the monitor TV.

(8) Push the [+10] and [2] button, select Title 12 of DVD.

(9) Push the [ENTER] button, playback Title 12.
(color bar 75%)

ビデオセクション

I. MAIN ZONE

1. セッティング手順

(1) セットの S MONITOR OUT 端子から Y 信号と C 信号をそれぞれオシロスコープ（終端抵抗：75Ω）に接続します。

(2) セットの COMPONENT MONITOR OUT2 の端子（Y, P_B/C_B, P_R/C_R）をそれぞれオシロスコープ（終端抵抗：75Ω）に接続します。
※ **75Ω 抵抗は 1%品を使用する事。**

(3) DVD テストディスク：DVDT-S01 を用意します。

(4) DVD プレーヤーの COMPONENT VIDEO OUT を COMPONENT IN-5 に接続します。

2. 調整のまえに

2.1. オシロスコープを下記に設定

(1) P_B/C_B, P_R/C_R, C
(a) TIME/DIV : 10μs
(b) VOLT/DIV : 100mV
（プローブ x10 使用）

(2) Y
(a) TIME/DIV : 10μs
(b) VOLT/DIV : 200mV
（プローブ x10 使用）

電源電圧 : 100V

2.2. DVD プレーヤの設定と確認

(1) COMPONENT OUT の設定を " インターレース " にします。

(2) DVD プレーヤーの出力が以下 2.4. に合っていることを確認します。

2.3. 準備手順

(1) セットの AC コードをコンセントへ挿入し、「GAME」と「SURROUND BACK」ボタンを押しながらセットの電源を "ON" にします。

(2) FL 表示右上の VOL 表示が "0.0dB" になっていることを確認します。

(3) FUNCTION ノブを回し、入力を "VCR-1" に切り替えます。

(4) 「VIDEO ON/OFF」ボタンを 2 回押し、"VIDEO OFF" にします。（調整モードになります）

(5) DVD プレーヤーの「OPEN/CLOSE」ボタンを押しトレイを開き、トレイ上に DVD テストディスク（DVDT-S01）をセット後、「CLOSE」ボタンを押します。

(6) DVD プレーヤーの表示管上に "STOP" が表示されてから、「PLAY」ボタンを押し、ディスクを再生します。

(7) DVD プレーヤーのリモコンの「DISPLAY」ボタンを押しグラフィカル・ユーザー・インターフェイス (GUI) 画面を出します。

(8) 番号ボタンの「+10」,「2」ボタンを押し、Title 12 を選択します。

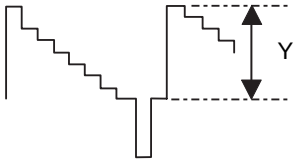
(9) 「ENTER」ボタンを押し、Title 12 を再生します。
（75%カラーバー信号）

2.4. Procedure

(1) Adjust the signal of S MONITOR OUT by the wave of oscilloscope.

(a) Target, Y-signal

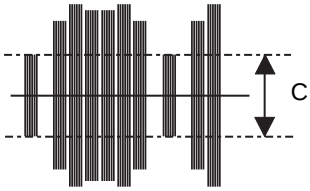
Point : 1U-3645-2 VR802
Adjustment Value : 714 ± 14mV
Waveform



Y-signal of S MONITOR OUT

(b) Target, C-signal

Point : 1U-3645-2 VR803
Adjustment Value : 286 ± 5mV
Waveform

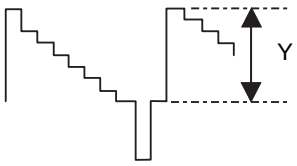


C-signal of S-MONITOR

(2) Adjust the signal of COMPONENT OUT by the wave of oscilloscope.

(a) Target, Y-signal

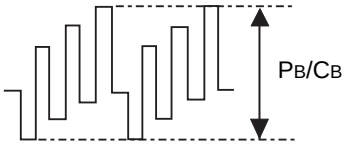
Point : 1U-3645-2 VR702
Adjustment Value : 714 ± 14mV
Waveform



Y-signal COMPONENT OUT

(b) Target, PB/CB-signal

Point : 1U-3645-2 VR703
Adjustment Value : *525 ± 10mV
Waveform



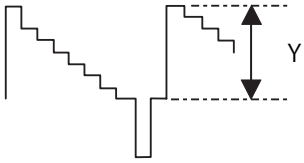
PB/CB-signal COMPONENT OUT

2.4. 手順

(1) セットの S MONITOR OUT の信号レベルをオシロスコープ上の波高値で調整します。

(a) Y 信号レベル

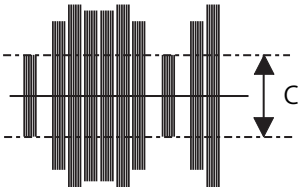
調整個所 : 1U-3645-2 VR802
調整値 : 714 ± 14mV
波形



S MONITOR OUT の Y 信号レベル

(b) C 信号レベル

調整個所 : 1U-3645-2 VR803
調整値 : 286 ± 5mV
波形

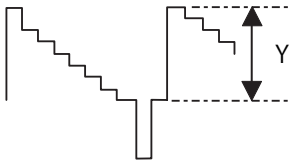


S MONITOR の C 信号レベル

(2) COMPONENT OUT の信号レベルをオシロスコープ上の波高値で調整します。

(a) Y 信号レベル

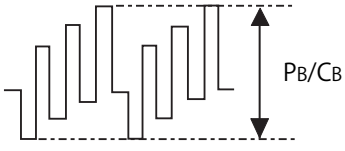
調整個所 : 1U-3645-2 VR702
調整値 : 714 ± 14mV
波形



COMPONENT OUT の Y 信号レベル

(b) PB/CB 信号レベル

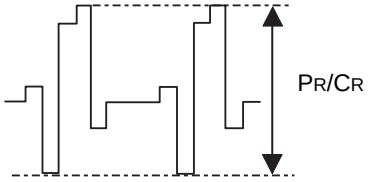
調整個所 : 1U-3645-2 VR703
調整値 : 525 ± 10mV
波形



COMPONENT OUT の PB/CB 信号レベル

(c) Target, PR/CR-signal

Point	:	1U-3645-2 VR704
Adjustment Value	:	*525 ± 10mV
Waveform		

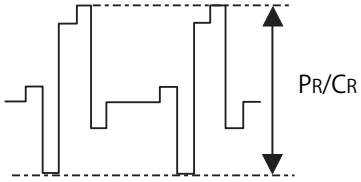


PR/CR-signal COMPONENT OUT

* : 486 ± 10mV for U.S.A. & Canada model

(c) PR/CR 信号レベル

調整個所	:	1U-3645-2 VR704
調整値	:	525 ± 10mV
波形		



COMPONENT OUT の PR/CR 信号レベル

Ⅱ. ZONE2

1. SETTING

(1) Connect the oscilloscope to the Y-signal, P_B-signal and C_B-signal, P_R-signal and C_R-signal of ZONE2 COMPONENT OUT terminal and each terminate at 75 Ohms.
※ **Use the 75 Ohms resistance must be 1%**

(2) DVD test disc : DVDT-S01

(3) S OUT of DVD player is connected to VCR-1 S IN.

2. Before Adjustment

2.1. Setting the Oscilloscope as below.

(1) P_B/C_B, P_R/C_R
(a) TIME/DIV : 10μs
(b) VOLT/DIV : 100mV
(Use the probe : x10)

(2) Y
(a) TIME/DIV : 10μs
(b) VOLT/DIV : 200mV
(Use the probe : x10)

Power on. Power Supply

USA & Canada	:	120V
Europe	:	230V
Japan	:	100V
China & Korea	:	220V

2.2. Setup the DVD player and confirmation of the stators

(1) Set to "INTERLACED" mode at the COMPONENT OUT.

(2) Confirm the DVD player's out put level is equal as the item 2.4. in following.

2.3. Preparation

(1) Push [POWER] button with pressing [GAME] and [SURROUND BACK] buttons.

(2) Confirm "0.0dB" appearing on the FL display.

(3) Turn the FUNCTION knob to select "VCR-1" input.

(4) Push [VIDEO ON/OFF] button twice to select "VIDEO OFF". (It becomes Adjustment mode.)

(5) Push [OPEN/CLOSE] button of DVD player, then open the Disc Tray.
Set DVD test disc (DVDT-S01) on the Disc Tray, and then push [CLOSE] button.

(6) DVD player FL display appear "STOP", push [PLAY] button to playback DVD.

(7) Push the [DISPLAY] button of remote control of DVD player unit and then appear the ON-Screen Display (GUI) on the monitor TV.

(8) Push the [+10] and [2] button, select Title 12 of DVD.

(9) Push the [ENTER] button, playback Title 12.
(color bar 75%)

Ⅱ. ZONE2

1. セッティング手順

(1) セットの ZONE2 COMPONENT OUT の端子（Y, P_B/C_B, P_R/C_R）をそれぞれオシロスコープ（終端抵抗：75Ω）に接続します。
※ **75Ω 抵抗は 1%品を使用する事。**

(2) DVD テストディスク：DVDT-S01 を用意します。

(3) DVD プレーヤーの S OUT を VCR-1 S IN に接続します。

2. 調整のまえに

2.1. オシロスコープを下記に設定

(1) P_B/C_B, P_R/C_R
(a) TIME/DIV : 10μs
(b) VOLT/DIV : 100mV
（プローブ x10 使用）

(2) Y
(a) TIME/DIV : 10μs
(b) VOLT/DIV : 200mV
（プローブ x10 使用）

電源電圧 : 100V

2.2. DVD プレーヤの設定と確認

(1) COMPONENT OUT の設定を " インターレース " にします。

(2) DVD プレーヤーの出力が以下 2.4. に合っていることを確認します。

2.3. 準備手順

(1) セットの AC コードをコンセントへ挿入し、「GAME」と「SURROUND BACK」ボタンを押しながらセットの電源を "ON" にします。

(2) FL 表示右上の VOL 表示が "0.0dB" になっていることを確認します。

(3) FUNCTION ノブを回し、入力を "VCR-1" に切り替えます。

(4) 「VIDEO ON/OFF」ボタンを 2 回押し、"VIDEO OFF" にします。（調整モードになります）

(5) DVD プレーヤーの「OPEN/CLOSE」ボタンを押しトレイを開き、トレイ上に DVD テストディスク（DVDT-S01）をセット後、「CLOSE」ボタンを押します。

(6) DVD プレーヤーの表示管上に "STOP" が表示されてから、「PLAY」ボタンを押し、ディスクを再生します。

(7) DVD プレーヤーのリモコンの「DISPLAY」ボタンを押しグラフィカル・ユーザー・インターフェイス (GUI) 画面を出します。

(8) 番号ボタンの「+10」,「2」ボタンを押し、Title 12 を選択します。

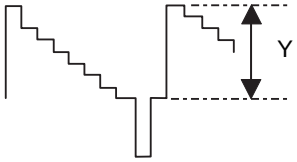
(9) 「ENTER」ボタンを押し、Title 12 を再生します。
（75%カラーバー信号）。

2.4. Procedure

(1) Adjust the signal of COMPONENT OUT by the wave of oscilloscope.

(a) Target, Y-signal

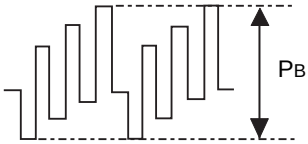
Point : 1U-3646-1 VR601
Adjustment Value : 714 ± 14mV
Waveform



Y-signal COMPONENT OUT

(b) Target, PB/CB-signal

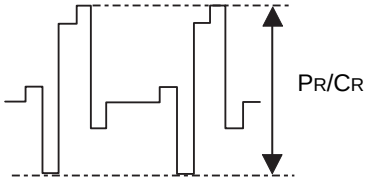
Point : 1U-3646-1 VR602
Adjustment Value : *525 ± 10mV
Waveform



PB/CB-signal COMPONENT OUT

(c) Target, PR/CR-signal

Point : 1U-3646-1 VR603
Adjustment Value : *525 ± 10mV
Waveform



PR/CR-signal COMPONENT OUT

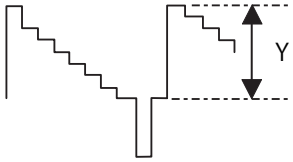
* : 486 ± 10mV for U.S.A. & Canada model

2.4. 手順

(1) COMPONENT OUT の信号レベルをオシロスコープ上の波高値で調整します。

(a) Y 信号レベル

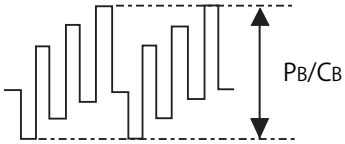
調整個所 : 1U-3646-1 VR601
調整値 : 714 ± 14mV
波形



COMPONENT OUT の Y 信号レベル

(b) PB/CB 信号レベル

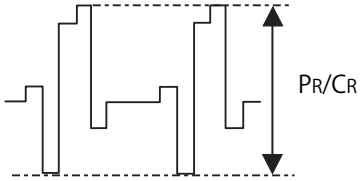
調整個所 : 1U-3646-1 VR602
調整値 : 525 ± 10mV
波形



COMPONENT OUT の PB/CB 信号レベル

(c) PR/CR 信号レベル

調整個所 : 1U-3646-1 VR603
調整値 : 525 ± 10mV
波形



COMPONENT OUT の PR/CR 信号レベル

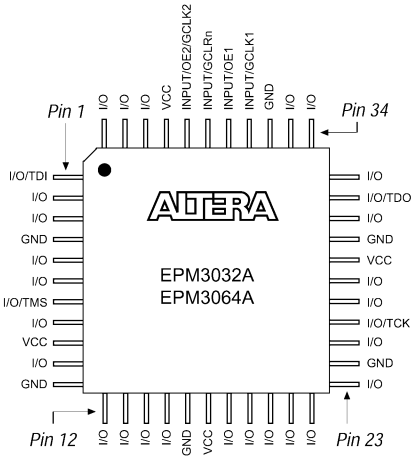
SEMICONDUCTORS

Only major semiconductors are shown, general semiconductors etc. are omitted to list.
主な半導体を記載しています。汎用の半導体は記載を省略しています。

1. IC's

EPM3032ATC44-10 (IC518)　AD P.W.B

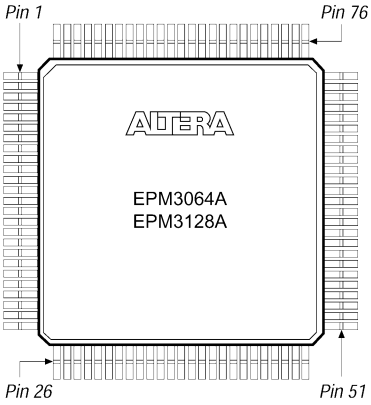
.



EPM3032ATC44-10 Terminal Function

Pin No.	Pin Name	Dir.	I/O Standard	FUNCTION
1	+TDI	input	LVTTL	JTAG DATA INPUT
2	GND*			N.C.
3	GND*			N.C.
4	GND	gnd		GND
5	GND*			N.C.
6	RCHLIMITO	output	LVTTL	Rch LIMITER ON/OFF H:ON,L:OFF
7	+TMS	input	LVTTL	JTAG TMS INPUT
8	L1SIGDET	input	LVTTL	L1ch SIGNAL DETECTION INPUT L:DETECTION
9	VCCIO	power		+3.3V
10	L2SIGDET	input	LVTTL	L2ch SIGNAL DETECTION INPUT
11	GND	gnd		GND
12	L3SIGDET	input	LVTTL	L3ch SIGNAL DETECTION INPUT L:DETECTION
13	L4SIGDET	input	LVTTL	L4ch SIGNAL DETECTION INPUT L:DETECTION
14	L5SIGDET	input	LVTTL	L5ch SIGNAL DETECTION INPUT L:DETECTION
15	L6SIGDET	input	LVTTL	L6ch SIGNAL DETECTION INPUT L:DETECTION
16	GND	gnd		GND
17	VCCINT	power		+3.3V
18	R6SIGDET	input	LVTTL	R6ch SIGNAL DETECTION INPUT L:DETECTION
19	R5SIGDET	input	LVTTL	R5ch SIGNAL DETECTION INPUT L:DETECTION
20	R4SIGDET	input	LVTTL	R4ch SIGNAL DETECTION INPUT L:DETECTION
21	R3SIGDET	input	LVTTL	R3ch SIGNAL DETECTION INPUT L:DETECTION
22	R2SIGDET	input	LVTTL	R2ch SIGNAL DETECTION INPUT L:DETECTION
23	R1SIGDET	input	LVTTL	R1ch SIGNAL DETECTION INPUT L:DETECTION
24	GND	gnd		GND
25	LCHLIMITO	output	LVTTL	Lch LIMITER ON/OFF H:ON,L:OFF
26	+TCK	input	LVTTL	JTAG CLK INPUT
27	ASIGDET	output	LVTTL	SIGNAL DETECTION OUTPUT H:DETECTION
28	GND*			N.C.
29	VCCIO	power		+3.3V
30	GND	gnd		GND
31	GND*			N.C.
32	*TDO	output	LVTTL	JTAG DATA OUTPUT
33	GND*			N.C.
34	GND*			N.C.
35	GND*			N.C.
36	GND	gnd		GND
37	GND+			N.C.
38	GND+			N.C.
39	GND+			N.C.
40	GND+			N.C.
41	VCCINT	power		+3.3V
42	GND*			N.C.
43	GND*			N.C.
44	GND*			N.C.

EPM3064ATC100-10 (IC301) 1394 P.W.B.

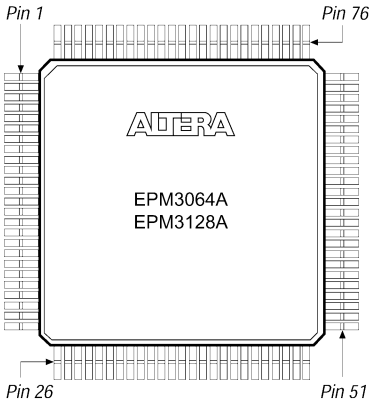


EPM3064ATC100-10 Terminal Function

Pin No.	Pin Name	Dir.	I/O Standard	FUNCTION
1	NC			N.C.
2	NC			N.C.
3	VCCIO	power		+3.3V
4	+TDI	input	LVCMOS	JTAG DATA INPUT
5	NC			N.C.
6	CLKPLD	input	LVCMOS	u-COM CLOCK INPUT
7	NC			N.C.
8	MOSIPLD	input	LVCMOS	u-COM DATA INPUT
9	RSV	input	LVCMOS	RESERVED
10	22MON	input	LVCMOS	
11	GND	gnd		GND
12	VCO44/48ON	output	LVCMOS	VCO 44kHz/48kHz ON/OFF H:OFF,L:ON
13	VCXO48ON	output	LVCMOS	VCXO 48kHz ON/OFF H:OFF,L:ON
14	VCXO44ON	output	LVCMOS	VCXO 44kHz ON/OFF H:OFF,L:ON
15	+TMS	input	LVCMOS	JTAG TMS INPUT
16	CBRC44ON	output	LVCMOS	CBRC 44kHz ON/OFF H:ON,L:OFF
17	CBRC48ON	output	LVCMOS	CBRC 48kHz ON/OFF H:ON,L:OFF
18	VCCIO	power		+3.3V
19	44/48VCO	input	LVCMOS	VCO CLOCK INPUT
20	48VCXO	input	LVCMOS	VCXO 48kHz INPUT (24.576MHz)
21	44VCXO	input	LVCMOS	VCXO 44kHz INPUT (22.5792MHz)
22	NC			N.C.
23	44CBRC	input	LVCMOS	OSC 44kHz INPUT (22.5792MHz)
24	NC			N.C.
25	48CBRC	input	LVCMOS	OSC 48kHz INPUT (24.576MHz)
26	GND	gnd		GND
27	NC			N.C.
28	NC			N.C.
29	INIT	output	LVCMOS	SM5819A INIT H:ON,L:OFF
30	PCLKDET	input	LVCMOS	TSB41AB2 PCLK DETECT
31	PCLKOUT	output	LVCMOS	PLCK OUTPUT
32	PCLKIN	input	LVCMOS	TSB41AB2 PCLK INPUT
33	GND	gnd		GND
34	VCCIO	power		+3.3V
35	ON	output	LVCMOS	SM5819A ON H:ON,L:OFF
36	MUTE	output	LVCMOS	DM1000 MUTE OUTPUT
37	S/PDIF/SRch	output	LVCMOS	S/PDIF / SRch OUTPUT
38	GND	gnd		GND
39	VCCINT	power		+3.3V
40	S/SLch	output	LVCMOS	S / SLch OUTPUT
41	C/Cch	output	LVCMOS	Cch OUTPUT
42	-/FRch	output	LVCMOS	FRch OUTPUT
43	GND	gnd		GND
44	F/FLch	output	LVCMOS	F / FLch OUTPUT
45	fs/SWch	output	LVCMOS	fs / SWch OUTPUT
46	64fs/BCK	output	LVCMOS	64fs OUTPUT
47	256fs	output	LVCMOS	256fs OUTPUT
48	DSBCK	output	LVCMOS	SM5819A DSBCK OUTPUT
49	NC			N.C.
50	NC			N.C.
51	VCCIO	power		+3.3V
52	SEL4FS	output	LVCMOS	SM5819A 4fs MODE SELECT H:ON,L:OFF
53	GND	gnd		GND
54	SEL1FS	output	LVCMOS	SM5819A 1fs MODE SELECT H:ON,L:OFF
55	NC			N.C.
56	POSLR	input	LVCMOS	SM5819A Sch INPUT
57	POFLR	input	LVCMOS	SM5819A Fch INPUT
58	POCSW	input	LVCMOS	SM5819A Cch INPUT
59	GND	gnd		GND
60	PLRCK	input	LVCMOS	SM5819A fs INPUT
61	PBCK	input	LVCMOS	SM5819A 64fs INPUT
62	+TCK	input	LVCMOS	JTAG CLOCK INPUT
63	MCK	output	LVCMOS	SM5819A MCK OUTPUT
64	DSISW	output	LVCMOS	SM5819A SWch OUTPUT
65	GND	gnd		GND
66	VCCIO	power		+3.3V

Pin No.	Pin Name	Dir.	I/O Standard	FUNCTION
67	DSISR	output	LVCMOS	SM5819A SRch OUTPUT
68	DSISL	output	LVCMOS	SM5819A SLch OUTPUT
69	DSIFR	output	LVCMOS	SM5819A FRch OUTPUT
70	NC			N.C.
71	DSIFL	output	LVCMOS	SM5819A FLch OUTPUT
72	NC			N.C.
73	*TDO	output	LVCMOS	JTAG DATA OUTPUT
74	GND	gnd		GND
75	DSICT	output	LVCMOS	SM5819A Cch OUTPUT
76	AV1DATA0	input	LVCMOS	DM1000 FLch INPUT
77	NC			N.C.
78	GND	gnd		GND
79	AV1DATA1	input	LVCMOS	DM1000 FRch INPUT
80	AV1DATA2	input	LVCMOS	DM1000 Cch INPUT
81	AV1DATA3	input	LVCMOS	DM1000 SWch INPUT
82	VCCIO	power		+3.3V
83	AV1DATA4	input	LVCMOS	DM1000 SLch INPUT
84	AV1DATA5	input	LVCMOS	DM1000 SRch INPUT
85	AV1DATA7	input	LVCMOS	DM1000 MUTE INPUT
86	GND	gnd		GND
87	AV1CTRL1	input	LVCMOS	DM1000 256fs INPUT
88	AV1CLK	input	LVCMOS	DM1000 64fs INPUT
89	AV2DATA0	input	LVCMOS	DM1000 IFULL INPUT
90	AV1CTRL0	input	LVCMOS	DM1000 fs INPUT
91	VCCINT	power		+3.3V
92	AV2DATA1	input	LVCMOS	DM1000 IEMPTY INPUT
93	AV2DATA2	input	LVCMOS	DM1000 48/n44 INPUT
94	AV2DATA4	input	LVCMOS	DM1000 VCO Enable INPUT
95	GND	gnd		GND
96	AV2DATA6	input	LVCMOS	DM1000 S/PDIF INPUT
97	RESERVED			RESERVED
98	VCOIN	output	LVCMOS	DM1000 VCOIN OUTPUT
99	RESERVED			RESERVED
100	CSPLD	input	LVCMOS	u-COM CS INPUT

EPM3128ATC100-10 (IC121) AD P.W.B.

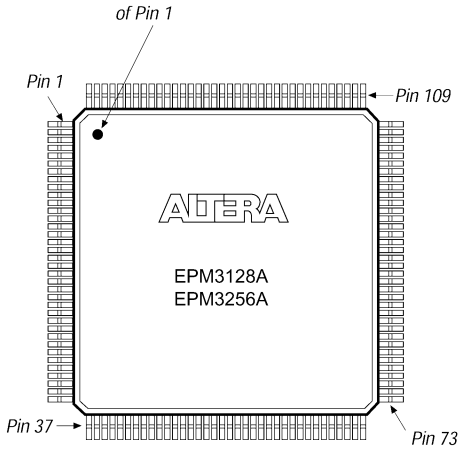


EPM3128ATC100-10 Terminal Function

Pin No.	Pin Name	Dir.	I/O Standard	FUNCTION
1	HDRADIO	input	LVTTL	HDRADIO SPDIF INPUT
2	DINPLDOSI	output	LVTTL	PLD DATA OUTPUT
3	VCCIO	power		+3.3V
4	+TDI	input	LVTTL	JTAG DATA INPUT
5	DINPLDREQ	output	LVTTL	PLD REQUEST OUTPUT
6	ADOVERL1	input	LVTTL	ADC L1ch OVER INPUT
7	ADOVERR1	input	LVTTL	ADC R1ch OVER INPUT
8	ADOVERL2	input	LVTTL	ADC L2ch OVER INPUT
9	ADOVERR2	input	LVTTL	ADC R2ch OVER INPUT
10	ADOVERL3	input	LVTTL	ADC L3ch OVER INPUT
11	GND	gnd		GND
12	ADOVERR3	input	LVTTL	ADC R3ch OVER INPUT
13	ADOVERL4	input	LVTTL	ADC L4ch OVER INPUT
14	ADOVERR4	input	LVTTL	ADC R4ch OVER INPUT
15	+TMS	input	LVTTL	JTAG TMS INPUT
16	ADOVERL5	input	LVTTL	ADC L5ch OVER INPUT
17	ADOVERR5	input	LVTTL	ADC R5ch OVER INPUT
18	VCCIO	power		+3.3V
19	ADOVERL6	input	LVTTL	ADC L6ch OVER INPUT
20	ADOVERR6	input	LVTTL	ADC R6ch OVER INPUT
21	ADOVERL7	input	LVTTL	ADC L7ch OVER INPUT
22	ADOVERR7	input	LVTTL	ADC R7ch OVER INPUT
23	ADOVERL8	input	LVTTL	ADC L8ch OVER INPUT
24	ADOVERR8	input	LVTTL	ADC R8ch OVER INPUT
25	MIC_IN	output	LVTTL	MIC SELECT OUTPUT H:MIC
26	GND	gnd		GND

Pin No.	Pin Name	Dir.	I/O Standard	FUNCTION
27	OSR8-1	output	LVTTL	ADC Z2Fch OSR1 OUTPUT
28	OSR8-0	output	LVTTL	ADC Z2Fch OSR0 OUTPUT
29	OSR7-1	output	LVTTL	ADC Z2Cch OSR1 OUTPUT
30	OSR7-0	output	LVTTL	ADC Z2Cch OSR0 OUTPUT
31	OSR6-1	output	LVTTL	ADC Z2SRch OSR1 OUTPUT
32	OSR6-0	output	LVTTL	ADC Z2SRch OSR0 OUTPUT
33	GND	gnd		GND
34	VCCIO	power		+3.3V
35	OSR1-1	output	LVTTL	ADC Z1ch OSR1 OUTPUT
36	OSR1-0	output	LVTTL	ADC Z1ch OSR0 OUTPUT
37	ADC-RST8	output	LVTTL	Z2Fch ADC RESET OUTPUT
38	GND	gnd		GND
39	VCCINT	power		+3.3V
40	ADC-RST7	output	LVTTL	Z2Cch ADC RESET OUTPUT
41	ADC-RST6	output	LVTTL	Z2SRch ADC RESET OUTPUT
42	ADC-RST1	output	LVTTL	Z1ch ADC RESET OUTPUT
43	GND	gnd		GND
44	GND*			N.C.
45	GND*			N.C.
46	HDSPDIFO	input	LVTTL	HDMI SPDIF INPUT
47	IESPDIFO	input	LVTTL	IEEE1394 SPDIF INPUT
48	SPDIF	output	LVTTL	SPDIF OUTPUT
49	ACKDIT	input	LVTTL	ACK DIT SPDIF INPUT
50	RECDIT	input	LVTTL	REC DIT SPDIF INPUT
51	VCCIO	power		+3.3V
52	DIRIN8	output	LVTTL	DIR8 SPDIF OUTPUT
53	GND	gnd		GND
54	DIRIN7	output	LVTTL	DIR7 SPDIF OUTPUT
55	DIRIN6	output	LVTTL	DIR6 SPDIF OUTPUT
56	DIRIN5	output	LVTTL	DIR5 SPDIF OUTPUT
57	DIRIN4	output	LVTTL	DIR4 SPDIF OUTPUT
58	DIRIN3	output	LVTTL	DIR3 SPDIF OUTPUT
59	GND	gnd		GND
60	DIRIN2	output	LVTTL	DIR2 SPDIF OUTPUT
61	DIRIN1	output	LVTTL	DIR1 SPDIF OUTPUT
62	+TCK	input	LVTTL	JTAG CLOCK INPUT
63	AC3RFDET	input	LVTTL	AC3RF DETECTION INPUT
64	DEMOD_ON	output	LVTTL	DEMODURATION ON
65	GND	gnd		GND
66	VCCIO	power		+3.3V
67	DEMOD_RST	output	LVTTL	DEMODURATION RESET
68	C1RL	output	LVTTL	COAXIAL1 INPUT SELECT
69	DLINK_ON	output	LVTTL	DENON LINK ON/OFF
70	DLINKACK	output	LVTTL	DENON LINK ACK ON/OFF
71	EXT3	input	LVTTL	DENON LINK SPDIF3 INPUT
72	EXT2	input	LVTTL	DENON LINK SPDIF2 INPUT
73	*TDO	output	LVTTL	JTAG DATA OUTPUT
74	GND	gnd		GND
75	EXT1	input	LVTTL	DENON LINK SPDIF1 INPUT
76	DDRF	input	LVTTL	DDRF SPDIF INPUT
77	C1	input	LVTTL	COAXIAL1 SPDIF INPUT
78	GND	gnd		GND
79	C2	input	LVTTL	COAXIAL2 SPDIF INPUT
80	C3	input	LVTTL	COAXIAL3 SPDIF INPUT
81	C4	input	LVTTL	COAXIAL4 SPDIF INPUT
82	VCCIO	power		+3.3V
83	C5	input	LVTTL	COAXIAL5 SPDIF INPUT
84	C6	input	LVTTL	COAXIAL6 SPDIF INPUT
85	O1	input	LVTTL	OPTICAL1 SPDIF INPUT
86	GND	gnd		GND
87	DINPLDCLK	input	LVTTL	PLD CLOCK INPUT
88	DINPLDCS	input	LVTTL	PLD CS INPUT
89	DINPLDISO	input	LVTTL	PLD DATA INPUT
90	GND+			
91	VCCINT	power		+3.3V
92	O2	input	LVTTL	OPTICAL2 SPDIF INPUT
93	O3	input	LVTTL	OPTICAL3 SPDIF INPUT
94	O4	input	LVTTL	OPTICAL4 SPDIF INPUT
95	GND	gnd		GND
96	O5	input	LVTTL	OPTICAL5 SPDIF INPUT
97	O6	input	LVTTL	OPTICAL6 SPDIF INPUT
98	OPT3REC	output	LVTTL	OPTICAL3 REC SPDIF OUTPUT
99	OPT4REC	output	LVTTL	OPTICAL4 REC SPDIF OUTPUT
100	OPT5REC	output	LVTTL	OPTICAL5 REC SPDIF OUTPUT

EPM3128ATC144-10 (IC904) DIGITAL P.W.B.

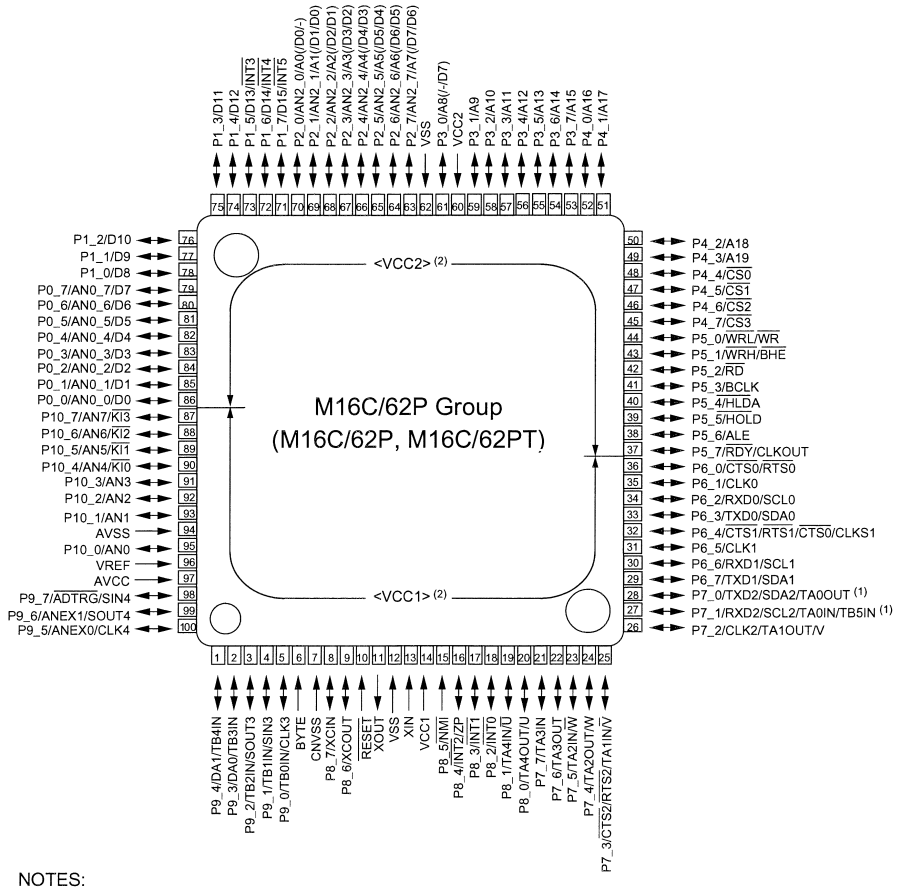


EPM3128ATC144-10 Terminal Function

Pin No.	Pin Name	Dir.	I/O Standard	FUNCTION
1	NC			
2	NC			
3	GND	gnd		
4	+TDI	input	LVTTL	JTAG DATA INPUT
5	DSPISO1	output	LVTTL	DSP1-HOST DATA OUTPUT
6	DSPOSI1	input	LVTTL	DSP1-HOST DATA INTPUT
7	DSPCLK1	output	LVTTL	DSP1-HOST CLOCK OUTTPUT
8	DSPCS1	output	LVTTL	DSP1-HOST CS OUTPUT
9	DSPREADY1	input	LVTTL	DSP1-HOST READY INPUT
10	DSPROMRST1	output	LVTTL	DSP1 ROM RESET OUTPUT
11	DSPRST1	output	LVTTL	DSP1 RESET OUTPUT
12	NC			
13	GND	gnd		
14	DSPISO2	output	LVTTL	DSP2-HOST DATA OUTPUT
15	DSPOSI2	input	LVTTL	DSP2-HOST DATA INTPUT
16	DSPCLK2	output	LVTTL	DSP2-HOST CLOCK OUTTPUT
17	GND	gnd		
18	DSPCS2	output	LVTTL	DSP2-HOST CS OUTPUT
19	NC			
20	+TMS	input	LVTTL	JTAG TMS INPUT
21	DSPREADY2	input	LVTTL	DSP2-HOST READY INPUT
22	DSPROMRST2	output	LVTTL	DSP2 ROM RESET OUTPUT
23	DSPRST2	output	LVTTL	DSP2 RESET OUTPUT
24	VCCIO	power		
25	DSPISO3	output	LVTTL	DSP3-HOST DATA OUTPUT
26	GND	gnd		
27	DSPOSI3	input	LVTTL	DSP3-HOST DATA INPUT
28	DSPCLK3	output	LVTTL	DSP3-HOST CLOCK OUTTPUT
29	DSPCS3	output	LVTTL	DSP3-HOST CS OUTPUT
30	DSPREADY3	input	LVTTL	DSP3-HOST READY INPUT
31	DSPROMRST3	output	LVTTL	DSP3 ROM RESET OUTPUT
32	DSPRST3	output	LVTTL	DSP3 RESET OUTPUT
33	GND	gnd		
34	NC			
35	NC			
36	NC			
37	DIRCLK6	output	LVTTL	DIR6/7 CLOCK OUTPUT
38	DIRDIN6	output	LVTTL	DIR6/7 DATA OUTPUT
39	DIRCE6	output	LVTTL	DIR6/7 CE OUTPUT
40	DIRRST6	output	LVTTL	DIR6/7 RESET OUTPUT
41	DIRCLK8	output	LVTTL	DIR8 CLOCK OUTPUT
42	DIRDIN8	output	LVTTL	DIR8 DATA OUTPUT
43	NC			
44	DIRCE8	output	LVTTL	DIR8 CE OUTPUT
45	DIRRST8	output	LVTTL	DIR8 RESET OUTPUT
46	NC			
47	NC			
48	NC			
49	NC			
50	VCCIO	power		
51	VCCINT	power		
52	GND	gnd		
53	DIR6CPUS	input	LVTTL	DIR6/7 ZONE SELECT H:Z-2/3/4,L:Z1
54	DIR8CPUS	input	LVTTL	DIR8 ZONE SELECT H:Z-2/3/4,L:Z1
55	HOSTRSV2	input	LVTTL	
56	HOSTRSV1	input	LVTTL	
57	GND	gnd		
58	VCCINT	power		
59	GND	gnd		
60	DSPROMRSTS	input	LVTTL	SUB uCOM-DSP ROM RESET INPUT
61	DSPIOPS	input	LVTTL	SUB uCOM-DSP I/O INPUT
62	DSPOSCONS	input	LVTTL	SUB uCOM-DSP OSC ON/OFF INPUT
63	DSPOSI	output	LVTTL	SUB uCOM-DSP DATA OUTPUT
64	GND	gnd		

Pin No.	Pin Name	Dir.	I/O Standard	FUNCTION
65	DSPISO	input	LVTTL	SUB uCOM-DSP DATA INPUT
66	NC			
67	DSPCSS	input	LVTTL	SUB uCOM-DSP CS INPUT
68	DSPA0S	input	LVTTL	SUB uCOM-DSP A0 INPUT
69	DSPA1S	input	LVTTL	SUB uCOM-DSP A1 INPUT
70	DSPA2S	input	LVTTL	SUB uCOM-DSP A2 INPUT
71	DSPREQ1S	output	LVTTL	SUB uCOM-DSP1 REQEST OUTPUT
72	DSPREQ2S	output	LVTTL	SUB uCOM-DSP2 REQEST OUTPUT
73	VCCIO	power		
74	DSPREQ3S	output	LVTTL	SUB uCOM-DSP3 REQEST OUTPUT
75	NC			
76	VCCIO	power		
77	GND	gnd		
78	DSPREQ4S	output	LVTTL	SUB uCOM-DSP4 REQEST OUTPUT
79	DSPREQ5S	output	LVTTL	SUB uCOM-DSP5 REQEST OUTPUT
80	DSPREQ6S	output	LVTTL	SUB uCOM-DSP6 REQEST OUTPUT
81	HOSTRSV4	input	LVTTL	
82	HOSTRSV3	input	LVTTL	
83	DIRRST1	input	LVTTL	DIR1 RESET INPUT
84	DIRCE5	input	LVTTL	DIR5 CE INPUT
85	GND	gnd		
86	DIRDIN1	input	LVTTL	DIR1 DATA INPUT
87	DIRCLK1	input	LVTTL	DIR1 CLOCK INPUT
88	DIRRST8Z	input	LVTTL	ZONE uCOM- DIR8 RESET INPUT
89	+TCK	input	LVTTL	JTAG CLOCK INPUT
90	NC			
91	DIRCE8Z	input	LVTTL	ZONE uCOM- DIR8 CE INPUT
92	DIRDIN8Z	input	LVTTL	ZONE uCOM- DIR8 DATA INPUT
93	DIRCLK8Z	input	LVTTL	ZONE uCOM- DIR8 CLOCK INPUT
94	GND	gnd		
95	VCCIO	power		
96	DSPROMRSTZ	input	LVTTL	ZONE uCOM- DSP ROM RESET INPUT
97	DSPIOPZ	input	LVTTL	ZONE uCOM- DSP I/O INPUT
98	DSPOSCONZ	input	LVTTL	ZONE uCOM- DSP OSC ON/OFF INPUT
99	DSPOZI	output	LVTTL	ZONE uCOM-DSP DATA OUTPUT
100	DSPIZO	input	LVTTL	ZONE uCOM-DSP DATA INPUT
101	DSPCSZ	input	LVTTL	ZONE uCOM-DSP CS INPUT
102	DSPA0Z	input	LVTTL	ZONE uCOM-DSP A0 INPUT
103	NC			
104	*TDO	output	LVTTL	JTAG DATA OUTPUT
105	GND	gnd		
106	DSPA1Z	input	LVTTL	ZONE uCOM-DSP A1 INPUT
107	DSPA2Z	input	LVTTL	ZONE uCOM-DSP A2 INPUT
108	NC			
109	DSPREQ1Z	output	LVTTL	ZONE uCOM-DSP1 REQEST OUTPUT
110	DSPREQ2Z	output	LVTTL	ZONE uCOM-DSP2 REQEST OUTPUT
111	DSPREQ3Z	output	LVTTL	ZONE uCOM-DSP3 REQEST OUTPUT
112	DSPREQ4Z	output	LVTTL	ZONE uCOM-DSP4 REQEST OUTPUT
113	DSPREQ5Z	output	LVTTL	ZONE uCOM-DSP5 REQEST OUTPUT
114	GND	gnd		
115	VCCIO	power		
116	DSPREQ6Z	output	LVTTL	ZONE uCOM-DSP6 REQEST OUTPUT
117	ROMRST4	output	LVTTL	ADI DSP ROM RESET
118	DSPIOPOWER4	output	LVTTL	ADI DSP IO POWER ON/OFF OUTPUT
119	DSPOSCON4	output	LVTTL	ADI DSP OSC ON/OFF OUTPUT
120	NC			
121	NC			
122	NC			
123	VCCINT	power		
124	GND	gnd		
125	DSPCLKS	input	LVTTL	SUB uCOM-DSP CLOCK INPUT
126	DSPRSTZ	input	LVTTL	ZONE uCOM-DSP RESET INPUT
127	DSPRSTS	input	LVTTL	SUB uCOM-DSP RESET INPUT
128	DSPCLKZ	input	LVTTL	ZONE uCOM-DSP CLOCK INPUT
129	GND	gnd		
130	VCCINT	power		
131	DSPCLK4	output	LVTTL	ADI DSP CLOCK OUTPUT
132	DSPIPLDO4	output	LVTTL	ADI DSP DATA OUTPUT
133	DSPOPLDI4	input	LVTTL	ADI DSP DATA INPUT
134	DSPRST4	output	LVTTL	ADI DSP RESET OUTPUT
135	GND	gnd		
136	DSPCS4	output	LVTTL	ADI DSP CS4 OUTPUT
137	DSPCS5	input	LVTTL	ADI DSP CS5 INPUT
138	DSPCS6	output	LVTTL	ADI DSP CS6 OUTPUT
139	DSPCS7	output	LVTTL	ADI DSP CS7 OUTPUT
140	FLAG0	input	LVTTL	ADI DSP FLAG0 INPUT
141	FLAG1	input	LVTTL	ADI DSP FLAG1 INPUT
142	FLAG2	input	LVTTL	ADI DSP FLAG2 INPUT
143	FLAG3	input	LVTTL	ADI DSP FLAG3 INPUT
144	VCCIO	power		

M30620FCPGP (IC302) DIGITAL P.W.B.



NOTES:

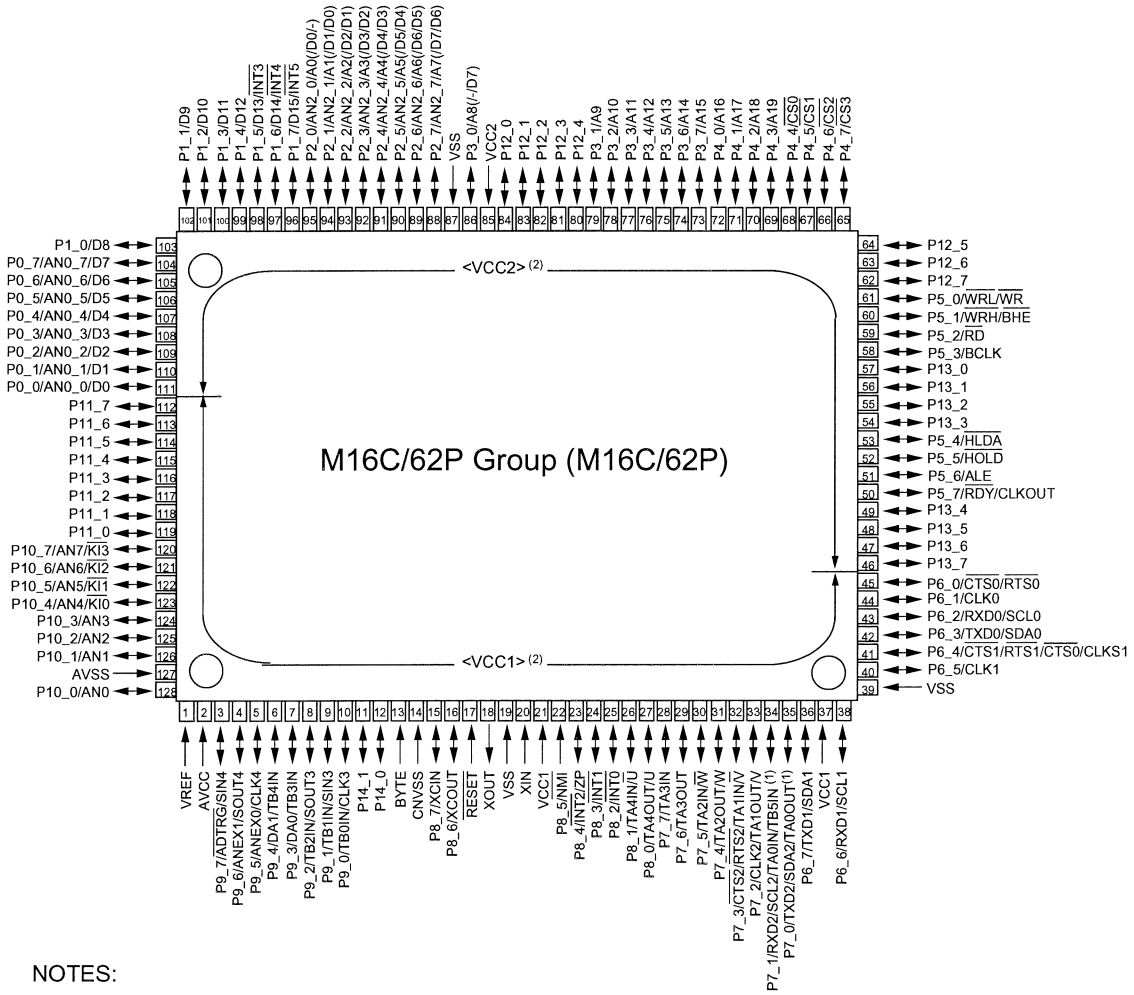
1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/62PT on VCC1 = VCC2.

M30620FCPGP Terminal Function

Pln	Pln Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	FUNCTION
1	P94/TB4	DSP CSZ	O	C	-	-	-	Z	PLD control for DSP chlp select
2	P93/TB3	NC	O	C	-	-	-	Z	Not used
3	P92/SOUT3	NC	O	C	-	-	-	Z	Not used
4	P91/SIN3	NC	O	C	-	-	-	Z	Not used
5	P90/CLK3	NC	O	C	-	-	-	Z	Not used
6	BYTE	BYTE	-	-	-	-	-	-	GND (Ext. data bus blt wldth swltchlng, 16blt: L)
7	CNVCS	CNVSS	-	-	-	-	Ed	-	"SIngle-chlp/MIcro-processor mode swltchlng (Normal slngle-chlp: L, Rewrlte boot program start:H Input set)"
8	P87	NC	O	C	-	-	-	Z	Not used
9	P86	NC	O	C	-	-	-	Z	Not used
10	RESET	ZRESET	I	-	-	-	Eu	L	Reset Input (Reset: L)
11	XOUT	X1	O	-	-	-	-	-	Oscllator connectlon
12	VSS	VSS	-	-	-	-	-	-	GND
13	XIN	X2	I	-	-	-	-	-	Oscllator connectlon
14	VCC	VCC	-	-	-	-	-	-	+5V
15	P85/NMI	_NMI	I	-	-	-	-	-	Not used (Flxed to H)
16	P84/INT2	INT8	I	-	E ↓ &L	-	Eu	Z	DIR8 control pln (LC89057W-E) (※ "Z"set: Operated from SUB μcom)
17	P83/INT1	ACKZIMO	I	-	E ↓ &L	-	Ed	Z	MAIN-ZONE μcom comm. control pln
18	P82/INT0	ZB.DOWN	I	-	Lv	-	Eu	Z	Power down detect (Power down: L)
19	P81	NC	I	-	-	-	-	Z	Not used
20	P80	NC	I	-	-	-	-	Z	Not used
21	P77	NC	I	-	-	-	-	Z	Not used
22	P76	DSPREQ4Z	I	-	-	-	-	Z	PLD control for DSP(use wlth DSP READY)
23	P75	NC	I	-	-	-	-	Z	Not used
24	P74	NC	I	-	-	-	-	Z	Not used
25	P73/CTS2	NC	O	C	-	-	-	Z	Not used
26	P72/CLK2	NC	I	C	-	-	-	Z	Not used
27	P71/RXD2	NC	I	N	-	-	Eu	Z	Not used
28	P70/TXD2	NC	O	N	-	-	Eu	Z	Not used
29	P67/TXD1	TxD.Z	O	C	-	-	Ed	Z	Data transfer output to outslde
30	P66/RXD1	RxD.Z	I	-	Lv	-	Ed	Z	Data recelve Input from outslde
31	P65/CLK1	NC	I	-	-	-	Ed	Z	Not used
32	P64/CTS1	NC	O	C	-	-	-	Z	Not used
33	P63/TXD0	ZOMI	O	C	-	-	Ed	Z	MAIN-ZONE μcom comm. control pln

Pln	Pln Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	FUNCTION
34	P62/RXD0	ZIMO	I	-	-	-	Ed	Z	MAIN-ZONE μcom comm. control pln
35	P61/CLK0	CLKZIMO	I	-	-	-	Ed	Z	MAIN-ZONE μcom comm. control pln
36	P60/CTS0/RTS0	REQZOMI	O	C	-	-	Ed	Z	MAIN-ZONE μcom comm. control pln
37	P57	NC	O	C	-	-	-	Z	Not used
38	P56	NC	O	C	-	-	-	Z	Not used
39	P55/EPM	FRASH EPM	I	-	Lv	-	Eu	Z	Rewrlte boot start: L
40	P54	DIRCLK8Z	O	C	-	-	-	Z	DIR8 control pln (LC89057W-E), control clock output (※ used as DIR for ZONE2)
41	P53	DIR CE8Z	O	C	-	-	-	Z	DIR8 control pln (LC89057W-E), chlp enable output (※ used as DIR for ZONE2)
42	P52	DIR_RST8Z	O	C	-	-	Ed	Z	DIR control output (LC89057W-E) Reset: L (※ used as DIR for ZONE2)
43	P51	DIRDIN8Z	O	C	-	-	Eu	Z	DIR8 control pln (LC89057W-E), control data output (※ used as DIR for ZONE2)
44	P50/CE	FRASH CE	I	-	-	-	Ed	Z	Rewrlte boot program start: H Input set
45	P47	DIRDOUT8	I	-	-	-	Eu	Z	DIR8 control Input pln (LC89057W-E), control data Input (※ "Z"set: Operated from SUB μcom)
46	P46	NC	I	-	-	-	-	Z	Not used
47	P45	NC	O	C	-	-	-	Z	Not used
48	P44	NC	O	C	-	-	-	Z	Not used
49	P43	NC	O	C	-	-	-	Z	Not used
50	P42	NC	O	C	-	-	-	Z	Not used
51	P41	DAPLDSTBZ	O	C	-	-	-	Z	FPGA control for DAC
52	P40	DAPLDCLKZ	O	C	-	-	-	Z	FPGA control for DAC
53	P37	DAPLDDATAZ	O	C	-	-	-	Z	FPGA control for DAC
54	P36	DAMSZ	O	C	-	-	-	Z	FPGA control for DAC
55	P35	DAMDIZ	O	C	-	-	-	Z	FPGA control for DAC
56	P34	DAMCZ	O	C	-	-	-	Z	FPGA control for DAC
57	P33	NC	O	C	-	-	-	Z	Not used
58	P32	NC	O	C	-	-	-	Z	Not used
59	P31	NC	O	C	-	-	-	Z	Not used
60	VCC	VCC	-	-	-	-	-	-	+5V
61	P30	NC	O	C	-	-	-	Z	Not used
62	VSS	VSS	-	-	-	-	-	-	GND
63	P27	NC	O	C	-	-	-	Z	Not used
64	P26	NC	O	C	-	-	-	Z	Not used
65	P25	NC	O	C	-	-	-	Z	Not used
66	P24	NC	O	C	-	-	-	Z	Not used
67	P23	NC	O	C	-	-	-	Z	Not used
68	P22	NC	O	C	-	-	-	Z	Not used
69	P21	NC	O	C	-	-	-	Z	Not used
70	P20	NC	O	C	-	-	-	Z	Not used
71	P17/INT5	NC	I	-	-	-	-	Z	Not used
72	P16/INT4	INT6	I	-	E ↓ &L	-	-	Z	DIR6 control pln (LC89057W-E) (※ "Z"set: Operated from SUB μcom)
73	P15/INT3	INT7	I	-	E ↓ &L	-	-	Z	DIR7 control pln (LC89057W-E) (※ "Z"set: Operated from SUB μcom)
74	P14/D12	MUTEZ2	O	C	-	-	-	Z	Mute control for DAC output (※ "Z"set: Operated from SUB μcom)
75	P13/D11	NC	I	-	-	-	-	Z	Not used
76	P12/D10	NC	I	-	-	-	-	Z	Not used
77	P11/D9	NC	I	-	-	-	-	Z	Not used
78	P10/D8	STBZOPLDI	O	C	-	-	-	Z	MAIN FPGA control pln
79	P07/D7	CLKZOPLDI	O	C	-	-	-	Z	MAIN FPGA control pln
80	P06/D6	ZIPLDO	I	-	-	-	-	Z	MAIN FPGA control pln
81	P05/D5	ZOPLDI	O	C	-	-	-	Z	MAIN FPGA control pln
82	P04/D4	MUTEZ4	O	C	-	-	-	Z	Mute control for DAC output (※ "Z"set: Operated from SUB μcom)
83	P03/D3	MUTEZ3	O	C	-	-	-	Z	Mute control for DAC output (※ "Z"set: Operated from SUB μcom)
84	P02/D2	VPPZ	I	-	-	-	-	Z	Normal: H WrltIng flash ROM for DSP: L
85	P01/D1	DSPA0Z	O	-	-	-	-	Z	PLD control for DSP (3-blt address for target selectIon of RST/CS)
86	P00/D0	DSPA1Z	O	-	-	-	-	Z	PLD control for DSP (3-blt address for target selectIon of RST/CS)
87	P107/AN7	DSPA2Z	O	-	-	-	-	Z	PLD control for DSP (3-blt address for target selectIon of RST/CS)
88	P106/AN6	NC	O	-	-	-	-	Z	Not used
89	P105/AN5	DSPIOPOWERZ	O	C	-	-	-	Z	DSP POWER ON="L" (After 10ms from DIGITAL POWER ON)
90	P104/AN4	NC	O	C	-	-	-	Z	Not used
91	P103/AN3	DSPROMRSTZ	O	C	-	-	-	Z	Not used
92	P102/AN2	DSPRSTZ	O	C	-	-	-	Z	PLD control for DSP reset(Reset: L)
93	P101/AN1	DSPOSCONZ	O	C	-	-	-	Z	ON="H"(After 20ms from DIGITAL POWER ON)
94	AVSS	AVSS	-	-	-	-	-	-	AD GND
95	P100/AN0	DSPBOOT	I	-	-	-	Eu	Z	DSP rewrlte boot program (DSP rewrlte: L Input)
96	VREF	VREF	-	-	-	-	-	-	AD ref. +5V
97	AVCC	AVCC	-	-	-	-	-	-	AD +5V
98	P97/SIN4	DSPOZI	I	-	-	-	-	Z	PLD control pln for DSP
99	P96/SOUT4	DSPIZO	O	C	-	-	-	Z	PLD control pln for DSP
100	P95/CLK4	DSPCLKZ	O	C	-	-	-	Z	PLD control pln for DSP

M30625FGPGP (IC303) DIGITAL P.W.B.



NOTES:

1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/62PT on VCC1 = VCC2.

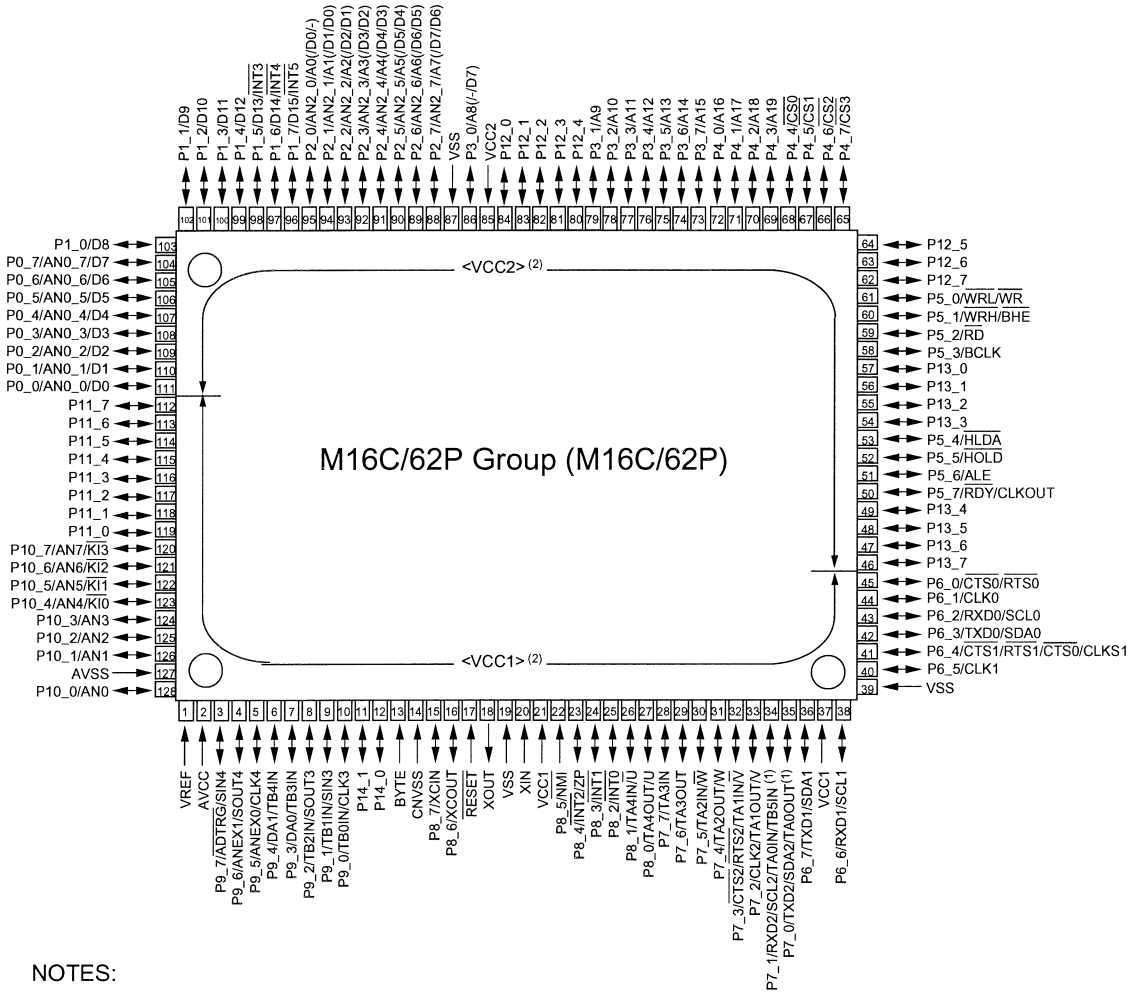
M30625FGPGP Terminal Function

Pin	Pin Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	FUNCTION
1	VREF	VREF	-	-	-	-	-	-	AD ref. +5V
2	AVCC	AVCC	-	-	-	-	-	-	AD +3.3V
3	P97/SIN4	MPLDOSI	I	-	Lv	-	-	Z	MAIN FPGA control pin
4	P96/SOUT4	MPLDISO	O	C	-	-	Ed	Z	MAIN FPGA control pin
5	P95/CLK4	MPLDCLK	O	C	-	-	Ed	Z	MAIN FPGA control pin
6	P94	MPLDSTB	O	C	-	-	Ed	Z	MAIN FPGA control pin
7	P93	DSPOSCONS	O	C	-	-	-	Z	ON="H"(After 20ms from DIGITAL POWER ON)
8	P92/SOUT3	DSPISOS	O	C	-	-	Ed	Z	PLD control pin for DSP
9	P91/SIN3	DSPOSIS	I	-	-	-	Eu	Z	PLD control pin for DSP
10	P90/CLK3	DSPCLKS	O	C	-	-	Ed	Z	PLD control pin for DSP
11	P141	DSPBOOT	I	-	-	-	Eu	Z	"DSP rewrite boot program (DSP rewrite: L input) /(DLINK ID writing mode start: L input set)"
12	P140	NC	I	-	-	-	Eu	Z	Not used
13	BYTE	BYTE	-	-	-	-	-	-	GND (Ext. data bus bit width switching, 16bit: L)
14	CNVCS	CNVSS	-	-	-	-	Ed	-	"Single-chip/Micro-processor mode switching (Normal single-chip: L, Rewrite boot program start:H input set)"
15	P87	DSPIOPOWERS	O	C	-	-	Eu	Z	DSP POWER ON="L" (After 10ms from DIGITAL POWER ON)
16	P86	NC	I	-	-	-	-	Z	Not used
17	RESET	$\overline{\text{SUBRESET}}$	I	-	Lv	-	Eu	L	Reset input (Reset: L)
18	XOUT	X1	O	-	-	-	-	-	Oscillator connection
19	VSS	VSS	-	-	-	-	-	-	GND
20	XIN	X2	I	-	-	-	-	-	Oscillator connection
21	VCC1	VCC1	-	-	-	-	-	-	+3.3V
22	P85/NMI	$\overline{\text{NMI}}$	I	-	-	-	-	-	Not used (Fixed to H)
23	P84/INT2	REQSIIEO	I	-	E ↓ &L	-	-	Z	1394 control pin
24	P83/INT1	ACKSIMO	I	-	E ↓ &L	-	Ed	Z	MAIN-SUB μcom comm. control pin
25	P82/INT0	$\overline{\text{SUBBDOWN}}$	I	-	E ↓ &L		Eu	Z	Power down detect (Power down: L)
26	P81	DIRDOUT1	I	-	-	-	Eu	Z	DIR1 control input pin (LC89057W-E), control data input
27	P80	DIRDIN1	O	C	-	-		Z	DIR1 control pin (LC89057W-E), control data output

Pin	Pin Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	FUNCTION
28	P77	DIRCLK1	O	C	-	-	-	Z	DIR1 control pin (LC89057W-E), control clock output
29	P76	DIRCE1	O	C	-	-	-	Z	DIR1 control pin (LC89057W-E), chip enable output
30	P75	ACKSIIEO	I	-	-	-	Ed	Z	ETHERNET control pin
31	P74	RSTIE	O	C	-	-	Eu	Z	ETHERNET reset output, Reset=" L" (Reset release="H" after 80msec from IEPOWER ON)
32	P73/CTS2	CSIE	O	C	-	-	Eu	Z	ETHERNET control pin
33	P72/CLK2	CLKSOIEI	O	C	-	-	Eu	Z	ETHERNET control pin
34	P71/RXD2	SIIEO	I	N	-	-	Eu	Z	ETHERNET control pin
35	P70/TXD2	SOIEI	O	N	-	-	Eu	Z	ETHERNET control pin
36	P67/TXD1	TXD.S/ (ZISO)	O	C	-	-	-	Z	Data transfer output to outside /(ZONE-SUB μcom comm. control pin)
37	VCC1	VCC1	-	-	-	-	-	Z	+3.3V
38	P66/RXD1	RXD.S/ (ZOSI)	I	-	-	-	-	Z	Data receive input from outside /(ZONE-SUB μcom comm. control pin)
39	VSS	VSS	-	-	-	-	-	Z	GND
40	P65/CLK1	NC	I	-	-	-	Ed	Z	Not used
41	P64/CTS1	NC	O	C	-	-	Ed	Z	Not used
42	P63/TXD0	SOMI	O	C	-	-	-	Z	MAIN-SUB μcom comm. control pin
43	P62/RXD0	SIMO	I	-	-	-	-	Z	MAIN-SUB μcom comm. control pin
44	P61/CLK0	CLKSIMO	I	-	-	-	-	Z	MAIN-SUB μcom comm. control pin
45	P60/CTS0	REQSOMI	O	C	-	-	-	Z	MAIN-SUB μcom comm. control pin
46	P137	DIRDOUT8	I	-	-	-	Eu	Z	DIR8 control input pin (LC89057W-E), control data input (※ "Z"set: operated from ZONE μcom)
47	P136	DIRCE5	O	C	-	-	-	Z	DIR5 control pin (LC89057W-E), chip enable output
48	P135	SUBnCE	O	C	-	-	-	Z	FPGA rewrite control pin
49	P134	SUBTDI	O	-	-	-	-	Z	PLD rewrite control pin(JTAG)
50	P57	SUBTMS	O	-	-	-	-	Z	PLD rewrite control pin(JTAG)
51	P56	SUBTDO	I	-	-	-	-	Z	PLD rewrite control pin(JTAG)
52	P55/EPM	$\overline{\text{FRASH EPM}}$	I	-	Lv	-	Eu	Z	Rewrite boot program start: L
53	P54	SUBTCK	O	C	-	-	-	Z	PLD rewrite control pin(JTAG)
54	P133	SUBDATAOUT	I	-	-	-	-	Z	FPGA rewrite control pin
55	P132	SUBASDI	O	C	-	-	-	Z	FPGA rewrite control pin
56	P131	SUBnCS	O	C	-	-	-	Z	FPGA rewrite control pin
57	P130	SUB n CONFIG	O	C	-	-	-	Z	FPGA rewrite control pin
58	P53	SUBDCLK	O	C	-	-	-	Z	FPGA rewrite control pin
59	P52	SUBCONF_DONE	I	-	-	-	-	Z	FPGA rewrite control pin
60	P51	$\overline{\text{SUBCPUJTAGON}}$	O	C	-	-	-	Z	JTAG (PLD rewrite from SUB-μcom:L) ※ default → D.POWER OFF：H
61	P50/CE	FRASH CE	I	-	-	-	Ed	Z	Rewrite boot program start: H
62	P127	$\overline{\text{FRONTJTAGON}}$	O	C	-	-	-	Z	JTAG (PLD rewrite from FRONT:L) ※ default → D.POWER OFF：H
63	P126	$\overline{\text{FRONTASON}}$	O	C	-	-	-	Z	Active Serial on(FPGA rewrite from FRONT:L) ※ default → D.POWER OFF：H
64	P125	$\overline{\text{SUBCPUASON}}$	O	C	-	-	-	Z	Active Serial on(FPGA rewrite from SUB-μCOM:L) ※ default → D.POWER OFF：H
65	P47	DSPJTAGON	O	C	-	-	-	Z	Fixed to L
66	P46	NC	O	C	-	-	-	Z	Not used
67	P45	OSCON	O	C	-	-	-	Z	Oscillator for DIR CLK(Osc. Stop:L)
68	P44	NC	O	C	-	-	-	Z	Not used
69	P43	NC	O	C	-	-	-	Z	Not used
70	P42	NC	O	C	-	-	-	Z	Not used
71	P41	DIRRST1	O	C	-	-	-	Z	DIR1 ～ 5 control output (LC89057W-E) Reset: L
72	P40	DPOWER	O	C	-	-	Ed	Z	DIGITAL power on/off switching(ON:H)
73	P37	IEPOWER	O	C	-	-	Ed	Z	ETHERNET power control (ON:H)
74	P36	RSV1394	O	C	-	-	-	Z	1394 control pin
75	P35	MOSI1394PLD	O	C	-	-	-	Z	1394 control pin
76	P34	CLK1394PLD	O	C	-	-	-	Z	1394 control pin
77	P33	CS1394PLD	O	C	-	-	-	Z	1394 control pin
78	P32	DINPLDREQ	I	-	-	-	-	Z	PLD control for DIGITAL INPUT
79	P31	DINPLDOSI	I	-	-	-	-	Z	PLD control for DIGITAL INPUT
80	P124	DINPLDISO	O	C	-	-	-	Z	PLD control for DIGITAL INPUT
81	P123	DINPLDCS	O	C	-	-	-	Z	PLD control for DIGITAL INPUT
82	P122	DINPLDCLK	O	C	-	-	-	Z	PLD control for DIGITAL INPUT
83	P121	NC	O	C	-	-	-	Z	Not used
84	P120	NC	O	C	-	-	-	Z	Not used
85	VCC2	VCC2	-	-	-	-	-	-	+3.3V
86	P30	NC	O	C	-	-	-	Z	Not used
87	VSS	VSS	-	-	-	-	-	-	GND
88	P27	NC	O	C	-	-	-	Z	Not used
89	P26	NC	I	-	-	-	Eu	Z	Not used
90	P25	NC	I	-	-	-	Eu	Z	Not used
91	P24	NC	I	-	-	-	Eu	Z	Not used
92	P23	NC	I	-	-	-	Eu	Z	Not used
93	P22	NC	I	-	-	-	Eu	Z	Not used
94	P21	NC	I	-	-	-	Eu	Z	Not used
95	P20	MUTE1	O	C	-	-	-	Z	Mute control for DAC output
96	P17/INT5	1394+12VON	O	C	-	-	Eu	Z	1394 +12V ON:H (TPS67341) ※ same logic as IEPOWER
97	P16/INT4	$\overline{\text{INT1}}$	I	-	E ↓ &L	-	Eu	Z	DIR1 control pin (LC89057W-E)
98	P15/INT3	NC	I	-	-	-	-	Z	Not used
99	P14	NC	I	-	-	-	Eu	Z	Not used
100	P13	NC	I	-	-	-	Eu	Z	Not used
101	P12	DAMDIS	O	C	-	-	-	Z	FPGA control for DAC
102	P11	DAMCS	O	C	-	-	-	Z	FPGA control for DAC

Pin	Pin Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	FUNCTION
103	P10	DAMSS	O	C	-	-	-	Z	FPGA control for DAC
104	P07/AN07	DAPLDDATAS	O	C	-	-	-	Z	FPGA control for DAC
105	P06/AN06	DAPLDCLKS	O	C	-	-	-	Z	FPGA control for DAC
106	P05/AN05	DAPLDSTBS	O	C	-	-	-	Z	FPGA control for DAC
107	P04/AN04	NC	O	C	-	-	-	Z	Not used
108	P03/AN03	INT2	I	-	E ↓ &L	-	Ed	Z	DIR2 control pin (LC89057W-E)
109	P02/AN02	INT3	I	-	E ↓ &L	-	Ed	Z	DIR3 control pin (LC89057W-E)
110	P01/AN01	INT4	I	-	E ↓ &L	-	Ed	Z	DIR4 control pin (LC89057W-E)
111	P00/AN00	INT5	I	-	E ↓ &L	-	Ed	Z	DIR5 control pin (LC89057W-E)
112	P117	INT6	I	-	E ↓ &L	-	Eu	Z	DIR6 control pin (LC89057W-E) (※ "Z"set: Operated from ZONE μcom)
113	P116	INT7	I	-	E ↓ &L	-	Eu	Z	DIR7 control pin (LC89057W-E) (※ "Z"set: Operated from ZONE μcom)
114	P115	INT8	I	-	E ↓ &L	-	Eu	Z	DIR8 control pin (LC89057W-E) (※ "Z"set: Operated from ZONE μcom)
115	P114	NC	I	-	-	-	-	Z	Not used
116	P113	DSPCSS	O	C	-	-	Eu	Z	PLD control for DSP chip select
117	P112	DSPA0S	O	C	-	-	-	Z	PLD control for DSP （3-bit address for target selection of RST/CS)
118	P111	DSPA1S	O	C	-	-	-	Z	PLD control for DSP （3-bit address for target selection of RST/CS)
119	P110	DSPA2S	O	C	-	-	-	Z	PLD control for DSP （3-bit address for target selection of RST/CS)
120	P107/AN7	DSPREQ1S	I	-	-	-	-	Z	PLD control for DSP(use with DSP READY)
121	P106/AN6	DSPREQ2S	I	-	-	-	-	Z	PLD control for DSP(use with DSP READY)
122	P105/AN5	DSPREQ3S	I	-	-	-	-	Z	PLD control for DSP(use with DSP READY)
123	P104/AN4	NC	I	-	-	-	-	Z	Not used
124	P103/AN3	NC	I	-	-	-	-	Z	Not used
125	P102/AN2	NC	I	-	-	-	-	Z	Not used
126	P101/AN1	DSPROMRSTS	O	C	-	-	Ed	Z	PLD control for DSP memory reset（Reset: L)
127	AVSS	AVSS	-	-	-	-	-	-	AD GND
128	P100/AN0	DSPRSTS	O	C	-	-	Ed	Z	PLD control for DSP reset（Reset: L)

M30625FGPGP (IC901) D.VIDEO P.W.B.



NOTES:

1. P7_0 and P7_1 are N channel open-drain output pins.
2. Use the M16C/62PT on VCC1 = VCC2.

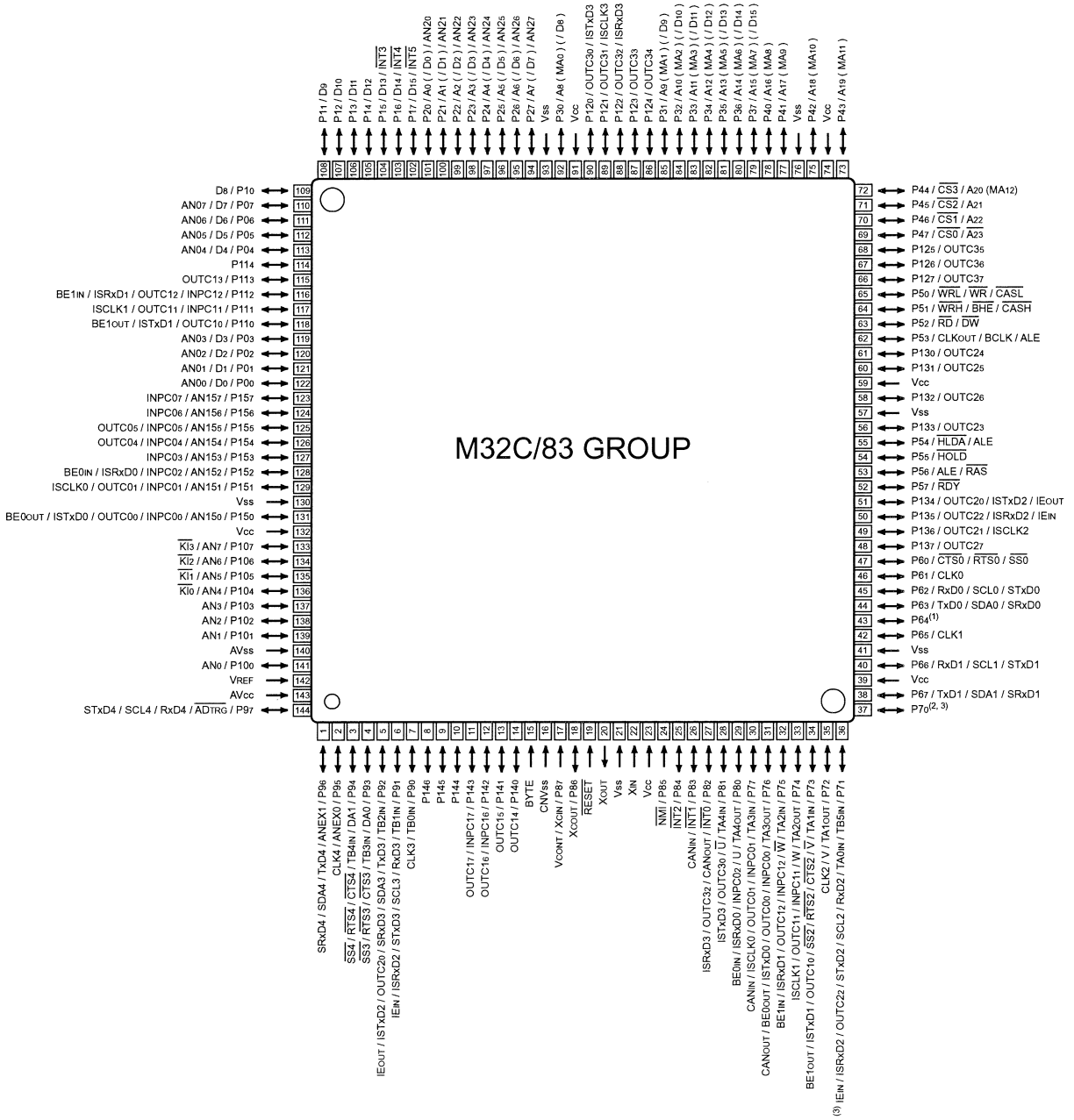
M30625FGPGP Terminal Function

Pin	Pin Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	STBY	stop	FUNCTION
1	VREF	VREF	-	-	-	-	-	-	-	-	AD ref. +5V
2	AVCC	AVCC	-	-	-	-	-	-	-	-	AD +5V
3	P97/SIN4	Z1 OSD STB	O	C	-	-	-	Z	O/L	O/L	OSD control for MAINZONE (M35015)
4	P96/SOUT4	Z1 OSD DATA	O	C	-	-	-	Z	O/L	O/L	OSD control for MAINZONE (M35015)
5	P95/CLK4	Z1 OSD CLK	O	C	-	-	-	Z	O/L	O/L	OSD control for MAINZONE (M35015)
6	P94	NC	O	C	-	-	-	Z	O/L	O/L	Not used
7	P93	NC	O	C	-	-	-	Z	O/L	O/L	Not used
8	P92/SOUT3	NC	O	C	-	-	-	Z	O/L	O/L	Not used
9	P91/SIN3	NC	O	C	-	-	-	Z	O/L	O/L	Not used
10	P90/CLK3	NC	O	C	-	-	-	Z	O/L	O/L	Not used
11	P141	NC	O	C	-	-	-	Z	O/L	O/L	Not used
12	P140	NC	O	C	-	-	-	Z	O/L	O/L	Not used
13	BYTE	BYTE	-	-	-	-	-	-	-	-	GND (Ext. data bus bit width switching, 16bit: L)
14	CNVCS	CNVSS	-	-	-	-	Ed	-	-	-	"Single-chip/Micro-processor mode switching (Normal single-chip: L, Rewrite boot program start:H input set)"
15	P87	TE RST	O	C	-	-	-	Z	O/L	O/L	COMPONENT FORMAT DETECTOR reset (TE8200PF)
16	P86	TC RST	O	C	-	-	-	Z	O/L	O/L	DETECTOR reset for color distinction (TC90101)
17	RESET	_RESET	I	-	Lv	-	Eu	L	I	I	Reset input (Reset: L)
18	XOUT	X1	O	-	-	-	-	-	-	-	Oscillator connection
19	VSS	VSS	-	-	-	-	-	-	-	-	GND
20	XIN	X2	I	-	-	-	-	-	I	I	Oscillator connection
21	VCC1	VCC1	-	-	-	-	-	-	-	-	+ 5 V
22	P85/NMI	_NMI	I	-	-	-	-	-	-	-	Not used (Fixed to H)
23	P84/INT2	INT	I	-	E ↓ &L	-	Ed	Z	I	I	HDMI RX interruption
24	P83/INT1	NC	I	-	E ↑ &L	-	Ed	Z	I	I	Not used
25	P82/INT0	V.B.DOWN	I	-	E ↑ &L	-	Ed	Z	I	I	Power down detect (Power down: L)
26	P81	VSDA	I/O	C	-	-	-	Z	O/L	O/L	VIDEO I2C (Chroma decoder, 3D Y/C) control pin

Pin	Pin Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	STBY	stop	FUNCTION
27	P80	VSCL	I/O	C	-	-	-	Z	O/L	O/L	VIDEO I2C (Chroma decoder, 3D Y/C) control pin
28	P77	NC	O	C	-	-	-	Z	O/L	O/L	Not used
29	P76	VPCKSEL	O	C	-	-	-	Z	O/L	O/L	CLK select for ENCODER(ADV7310)
30	P75	M/T SEL	O	C	-	-	-	Z	O/L	O/L	IC switching control pin (MN673747:H, TC90101:L)
31	P74	VIDEO POWER	O	C	-	-	-	Z	O/L	O/L	MAIN-VIDEO μcom comm. control pin
32	P73/CTS2	REQ VOMI	O	C	-	-		Z	O/L	O/L	MAIN-VIDEO μcom comm. control pin
33	P72/CLK2	CLK VIMO	I	-	Lv	-	Eu	Z	I	O/L	MAIN-VIDEO μcom comm. control pin
34	P71/RXD2	VIMO	I	-	Lv	-	Eu	Z	I	O/L	MAIN-VIDEO μcom comm. control pin
35	P70/TXD2	VOMI	O	N	-	-	(Eu)	Z	O/L	O/L	MAIN-VIDEO μcom comm. control pin
36	P67/TXD1/SDA1	5V SDA/TxD	I/O	C	-	-	-	Z	O/L	O/L	HDMI IC control/Data transfer pin to outside(MAKER BOOT)
37	VCC1	VCC	-	-	-	-	-	-	-	-	+ 5 V
38	P66/RXD1/SCL1	5V SCL/RxD	I/O	C	-	-	-	Z	O/L	O/L	HDMI IC control/Data transfer pin from outside(MAKER BOOT)
39	VSS	VSS	-	-	-	-	-	-	-	-	GND
40	P65/CLK1	Z2 Y/C SEL	O	C	-	-	Ed	Z	O/L	O/L	Chroma decoder selector for ZONE2
41	P64/CTS1	NC	I	-	Lv	-	Eu	Z	I	O/L	Not used
42	P63/TXD0/SDA0	EDIT SDA	I/O	C	-	-	-	Z	O/L	O/L	HDMI/DVI EDIT(E2PROM) control pin
43	P62/RXD0/SCL0	EDIT SCL	I/O	C	-	-	-	Z	O/L	O/L	HDMI/DVI EDIT(E2PROM) control pin
44	P61/CLK0	NC	O	C	-	-	-	Z	O/L	O/L	Not used
45	P60/CTS0	NC	O	C	-	-	-	Z	O/L	O/L	Not used
46	P137	MSDA	I/O	C	-	-	-	Z	O/L	O/L	VIDEO I2C (AN13310) control pin
47	P136	MSCL	I/O	C	-	-	-	Z	O/L	O/L	VIDEO I2C (AN13310) control pin
48	P135	YSEL	O	C	-	-	-	Z	O/L	O/L	COMPONENT Y/S-Video switching control (TC90101) （COMPONENT Y :H, S-Video Y:L）
49	P134	NC	O	C	-	-	-	Z	O/L	O/L	Not used
50	P57	NC	O	C	-	-	-	Z	O/L	O/L	Not used
51	P56	NC	O	C	-	-	-	Z	O/L	O/L	Not used
52	P55/EPM	$\overline{\text{FRASH EPM}}$	I	-	Lv	-	Eu	Z	I	I	Rewrite boot program start: L input set
53	P54	NC	O	C	-	-	-	Z	O/L	O/L	Not used
54	P133	NC	O	C	-	-	-	Z	O/L	O/L	Not used
55	P132	NC	O	C	-	-	-	Z	O/L	O/L	Not used
56	P131	NC	O	C	-	-	-	Z	O/L	O/L	Not used
57	P130	NC	O	C	-	-	-	Z	O/L	O/L	Not used
58	P53	NC	O	C	-	-	-	Z	O/L	O/L	Not used
59	P52	NC	O	C	-	-	-	Z	O/L	O/L	Not used
60	P51	NC	O	C	-	-	-	Z	O/L	O/L	Not used
61	P50/CE	FRASH CE	I	-	-	-	Ed	Z	I	I	Rewrite boot program start: H input set
62	P127	Z1 SMONIDET	I	-	-	-	-	Z	I	O/L	MAINZONE's S-monitor connection detect input (Connected:L)
63	P126	Z1 VSIG DET	I	-	Lv	-	Eu	Z	I	O/L	MAIN ZONE's VIDEO signal detect port （Detected:H)
64	P125	Z2 VSIG DET	I	-	Lv	-	Eu	Z	I	O/L	ZONE2's VIDEO signal detect port （Detected:H)
65	P47	NC	O	C	-	-	-	Z	O/L	O/L	Not used
66	P46	NC	O	C	-	-	-	Z	O/L	O/L	Not used
67	P45	S EXP CLK	O	C	-	-	-	Z	O/L	O/L	CLK output for video switching expander control(BU4094B)
68	P44	S EXP DATA	O	C	-	-	-	Z	O/L	O/L	DATA output for video switching expander control(BU4094B)
69	P43	S EXP STB	O	C	-	-	-	Z	O/L	O/L	STB output for video switching expander control(BU4094B)
70	P42	S EXP OE	O	C	-	-	Ed	Z	O/L	O/L	OE output for video switching expander control(BU4094B)
71	P41	Z2 SYNC DET	I	-	Lv	-	Eu	Z	I	I	Sync. detect input for ZONE2 (H: Ext. synchronized)
72	P40	Z2 OSD RST	O	C	-	-	-	Z	O/L	O/L	OSD control for ZONE2 (M35015)
73	P37	Z2 OSD STB	O	C	-	-	-	Z	O/L	O/L	OSD control for ZONE2 (M35015)
74	P36	Z2 OSD DATA	O	C	-	-	-	Z	O/L	O/L	OSD control for ZONE2 (M35015)
75	P35	Z2 OSD CLK	O	C	-	-	-	Z	O/L	O/L	OSD control for ZONE2 (M35015)
76	P34	NC	O	C	-	-	-	Z	O/L	O/L	Not used
77	P33	NC	O	C	-	-	-	Z	O/L	O/L	Not used
78	P32	NC	O	C	-	-	-	Z	O/L	O/L	Not used
79	P31	Z1 SYNC DET	I	-	Lv	-	Eu	Z	I	I	Sync. detect input for MAINZONE (H: Ext. synchronized)
80	P124	Z1 OSD RST	O	C	-	-	-	Z	O/L	O/L	OSD control for MAINZONE (M35015)
81	P123	NC	O	C	-	-	-	Z	O/L	O/L	Not used
82	P122	NC	O	C	-	-	-	Z	O/L	O/L	Not used
83	P121	C EXP CLK	O	C	-	-	-	Z	O/L	O/L	CLK output for component video switching expander control(BU4094B)
84	P120	C EXP DATA	O	C	-	-	-	Z	O/L	O/L	DATA output for component video switching expander control(BU4094B)
85	VCC2	VCC2	-	-	-	-	-	-	-	-	+ 5 V
86	P30	PAL ENA.	I	-	Lv	-	Eu	Z	I	O/L	PAL DECODE correspondence/ non-correspondence detect (non-correspondence: L)
87	VSS	VSS	-	-	-	-	-	-	-	-	GND
88	P27	C EXP STB	O	C	-	-	-	Z	O/L	O/L	STB output for component video switching expander control(BU4094B)
89	P26	C EXP OE	O	C	-	-	Ed	Z	O/L	O/L	OE output for component video switching expander control(BU4094B)
90	P25	COMP SDET1	I	-	Lv	-	Eu	Z	I	O/L	MAIN ZONE's COMPONENT signal detect input
91	P24	COMP SDET2	I	-	Lv	-	Eu	Z	I	O/L	ZONE2's COMPONENT signal detect input
92	P23	P1HPRMV2	O	C	-	-	-	Z	O/L	O/L	HP(hot-plug) detect input for HDMI IN3 terminal
93	P22	POHPRMV2	O	C	-	-	-	Z	O/L	O/L	HP(hot-plug) detect input for HDMI IN2 terminal
94	P21	P1HPRMV1	O	C	-	-	-	Z	O/L	O/L	HP(hot-plug) detect input for HDMI IN1 terminal
95	P20	P0HPRMV1	O	C	-	-	-	Z	O/L	O/L	HP(hot-plug) detect input for DVI IN terminal
96	P17/INT5	HDMI SENS	I	-	E ↓ &L	-	Ed	Z	I	O/L	HDMI signal detect input
97	P16/INT4	DVI SENS	I	-	E ↓ &L	-	Ed	Z	I	O/L	DVI signal detect input
98	P15/INT3	ACK VIMO	I	-	E ↓ &L	-	Ed	Z	I	O/L	MAIN-VIDEO μcom comm. control pin

Pin	Pin Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	STBY	stop	FUNCTION
99	P14	NC	O	C	-	-	Ed	Z	O/L	O/L	Not used
100	P13	NC	O	C	-	-	Ed	Z	O/L	O/L	Not used
101	P12	DVI T RST	O	C	-	-	-	Z	O/L	O/L	DVI TRANSMITTER reset (Si I9030)
102	P11	HDMI T RST	O	C	-	-	-	Z	O/L	O/L	HDMI TRANSMITTER reset (Si I9030)
103	P10	HDMI CS	O	-	-	-	-	Z	O/L	O/L	HDMI TRANSMITTER chip select (Si I9030)
104	P07/AN07	DVI CS	O	-	-	-	-	Z	O/L	O/L	DVI TRANSMITTER chip select (Si I9030)
105	P06/AN06	AN RST	O	-	-	-	-	Z	O/L	O/L	VIDEO SELECTER_A/D reset (AN13310B)
106	P05/AN05	VD RST	O	-	-	-	-	Z	O/L	O/L	VIDEO DECODER reset (MN67374)
107	P04/AN04	IP RST	O	-	-	-	-	Z	O/L	O/L	IP CONVERTER reset(FLI2310)
108	P03/AN03	IN SEL	O	-	-	-	-	Z	O/L	O/L	VIDEO DECODER input select
109	P02/AN02	VE RST1	O	-	-	-	-	Z	O/L	O/L	VIDEO ENCODER reset (ADV7310)
110	P01/AN01	VE RST2	O	-	-	-	-	Z	O/L	O/L	VIDEO ENCODER reset (ADV7300)
111	P00/AN00	INT1	I	-	-	-	-	Z	I	O/L	HDMI RECEIVER(Si I9031)INT output (DVI IN1/HDMI IN1)
112	P117	INT2	I	-	-	-	-	Z	I	O/L	HDMI RECEIVER(Si I9031)INT output (HDMI IN2/IN3)
113	P116	HDMI R RST	O	C	-	-	-	Z	O/L	O/L	HDMI RECEIVER reset (Si I9031) (HDMI IN2/IN3)
114	P115	DVI R RST	O	C	-	-	-	Z	O/L	O/L	HDMI RECEIVER reset (Si I9031) (DVI IN1/HDMI IN1)
115	P114	SCDT1	I	-	-	-	-	Z	I	O/L	HDMI RECEIVER(Si I9031)SCDT output (DVI IN1/HDMI IN1)
116	P113	SCDT2	I	-	-	-	-	Z	I	O/L	HDMI RECEIVER(Si I9031)SCDT output(HDMI IN2/IN3)
117	P112	WP1	O	C	-	-	-	Z	O/L	O/L	HDMI IN1 EDIT(24LC02) 用 WRITE PROTECT
118	P111	WP2	O	C	-	-	-	Z	O/L	O/L	HDMI IN2 EDIT(24LC02) 用 WRITE PROTECT
119	P110	WP3	O	C	-	-	-	Z	O/L	O/L	HDMI IN3 EDIT(24LC02) 用 WRITE PROTECT
120	P107/AN7	WP4	O	C	-	-	-	Z	O/L	O/L	HDMI IN4 EDIT(24LC02) 用 WRITE PROTECT
121	P106/AN6	SMONIDET2	I	-	-	-	-	Z	I	O/L	ZONE2's S-monitor connection detect input (Connected:L)
122	P105/AN5	Z1 S SIG DET	I	-	-	-	-	Z	I	O/L	MAIN ZONE's S-signal detect input (H: S-signal inputted)
123	P104/AN4	Z2 S SIG DET	I	-	-	-	-	Z	I	O/L	ZONE2's S-signal detect input (H: S-signal inputted)
124	P103/AN3	LINE3	I	-	-	-	-	Z	I	O/L	LINE3 level detection (distinguishes by AD voltage)
125	P102/AN2	LINE2	I	-	-	-	-	Z	I	O/L	LINE2 level detection (distinguishes by AD voltage)
126	P101/AN1	LINE1	I	-	-	-	-	Z	I	O/L	LINE1 level detection (distinguishes by AD voltage)
127	AVSS	AVSS	-	-	-	-	-	-	-	-	AD GND
128	P100/AN0	NC	I	-	Lv	-	Eu	Z	I	O/L	Not used

M30835FJGP (IC409) DIGITAL P.W.B.



NOTES:
1. P64 / $\overline{CTS1}$ / $\overline{RTS1}$ / $\overline{SS1}$ / OUTC21 / ISCLK2
2. P70 / TA0OUT / TxD2 / SDA2 / SRxD2 / OUTC20 / ISTxD2 / IEOUT
3. P70 and P71 are ports for the N-channel open drain output.

M30835FJGP Terminal Function

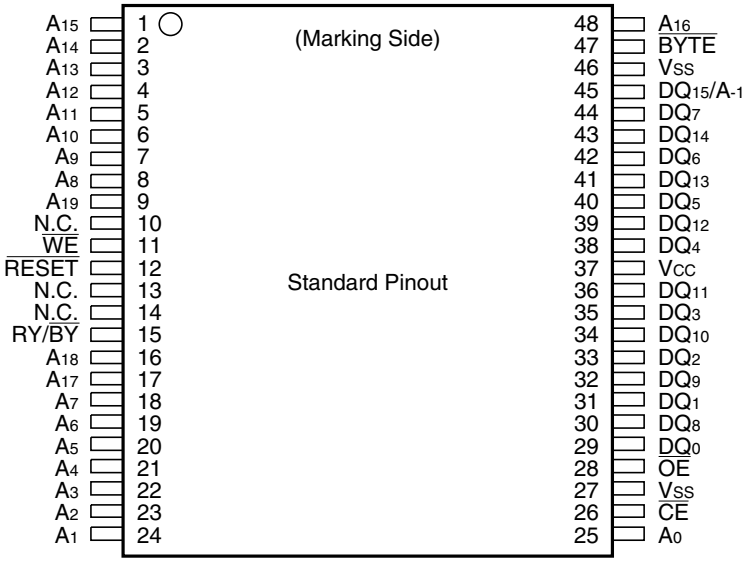
Pin	Pin Name	Symbol	I/O	Type	Det	Op(Int.)	Op(Ext.)	Res	STBY	stop	FUNCTION
1	P96/TXD4	ZIMO	O	C	-	-	-	Z	O/L	O/L	MAIN-ZONE μcom comm. control pin
2	P95/CLK4	CLK ZIMO	O	C	-	-	-	Z	O/L	O/L	MAIN-ZONE μcom comm. control pin
3	P94/$\overline{CTS4}$	REQ ZOMI	I	-	Lv	-	-	Z	I	O/L	MAIN-ZONE μcom comm. control pin
4	P93/$\overline{CTS3}$	NC	O	C	-	-	-	Z	O/L	O/L	Not used
5	P92/TXD3/SDA3	NC	I/O	C	-	-	-	Z	O/L	O/L	Not used
6	P91/RXD3/SCL3	NC	I/O	C	-	-	-	Z	O/L	O/L	Not used
7	P90/CLK3	Z.RST	O	C	-	-		Z	O/L	O/L	ZONE-μcom reset output
8	P146	RSTV	O	C	-	-	-	Z	O/L	O/L	VIDEO-μcom reset output
9	P145	NC	O	C	-	-	-	Z	O/L	O/L	Not used
10	P144	A SIG DET M	I	-	Lv	-	-	Z	I	O/L	AMP current limiter control (When "H" → BINRL(EXP8)is controlled to "H")
11	P143	MUTE POWER	O	C	-	-	-	Z	O/L	O/L	Muting ON:"H" (30msec before POWER ON), OFF:"L"(Same timing as POWER OFF)
12	P142	VCC POWER	O	C	-	-	-	Z	O/L	O/L	ZONE +B control POWER ON=H(After 15ms from POWER ON)
13	P141	SCPU POWER	O	C	-	-	-	Z	O/L	O/L	SUB-μcom power on/off switching(ON：H)
14	P140	232POWER(ETHER)	O	C	-	-	-	Z	O/H	O/L	LOGIC +VCC on/off switching for ETHER control(SAVING OFF/ STANDBY:H)

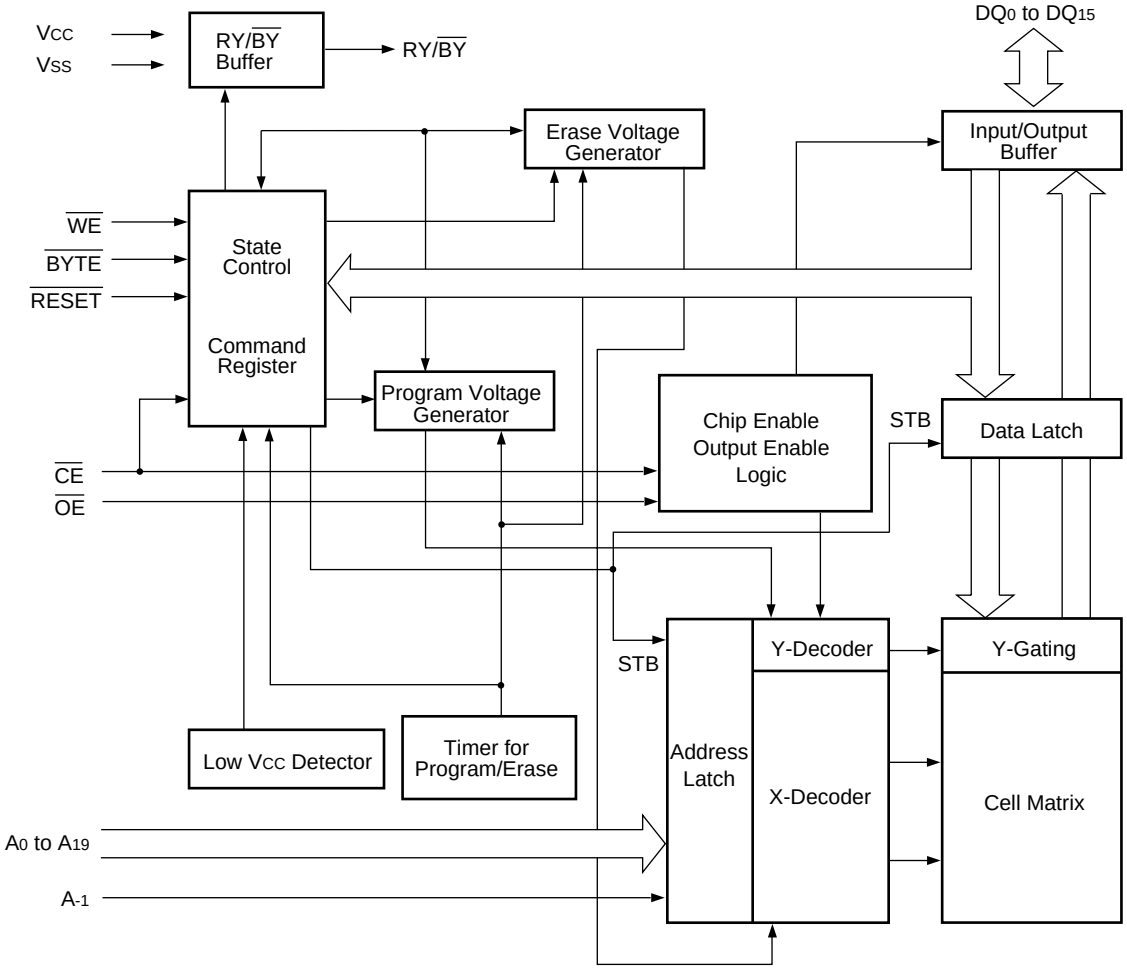
Pin	Pin Name	Symbol	I/O	Type	Det	Op(Int.)	Op(Ext.)	Res	STBY	stop	FUNCTION
15	BYTE	BYTE	-	-	-	-	-	-	-	-	GND(Ext. data bus bit width switching, 16bit:"L")
16	CNVss	CNVSS	I	-	-	-	Ed	-	-	-	"Single-chip/Micro-processor mode switching (Normal single-chip:L, Rewrite boot program start:H input set)"
17	P87/XCIN	POWER	O	C	-	-	-	Z	O/L	O/L	POWER relay control output (H:ON)
18	P86/XCOUT	NC	O	C	-	-	-	Z	O/L	O/L	Not used
19	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	I	-	Lv	-	Eu	L	I	I	Reset input
20	XOUT	X2	O	-	-	-	-	-	-	-	Oscillator connection
21	VSS	VSS	-	-	-	-	-	-	-	-	GND
22	XIN	X1	I	-	-	-	-	-	I	I	Oscillator connection
23	VCC	VCC	-	-	-	-	-	-	-	-	+ 5 V
24	P85/$\overline{\text{NMI}}$	$\overline{\text{NMI}}$	I	-	-	-	-	-	-	-	Not used(Fixed to H)
25	P84/$\overline{\text{INT2}}$	$\overline{\text{B.DOWN}}$	I	-	E ↓ &L	-	Eu	Z	I	I	Power down detect(Power down:L)
26	P83/$\overline{\text{INT1}}$	$\overline{\text{POWER KEY}}$	I	-	E ↓ &L	-	Eu		I	O/L	Interrupt port for WAIT mode cancel
27	P82/$\overline{\text{INT0}}$	REMOCON	I	-	E ↑ &L	-	Ed	Z	I	I	Remote control signal input
28	P81/	REQ VOMI	I	-	Lv	-	-	Z	O/L	O/L	MAIN-VIDEO μcom comm. control pin
29	P80/ISRXD0	SOMI	I	-	Lv	-	-	Z	O/L	O/L	MAIN-SUB μcom comm. control pin
30	P77/ISCLK0	CLK SIMO	O	C	-	-		Z	O/L	O/L	MAIN-SUB μcom comm. control pin
31	P76/ISTXD0	SIMO	O	C	-	-		Z	O/L	O/L	MAIN-SUB μcom comm. control pin
32	P75/ISRXD1	EOMI	I	-	Lv	-	-	Z	O/L	O/L	ETHERNET control pin
33	P74/ISCLK1	CLK EIMO	O	C	-	-		Z	O/L	O/L	ETHERNET control pin
34	P73/$\overline{\text{CTS2}}$/ISTXD1	EIMO	O	C	-	-		Z	O/L	O/L	ETHERNET control pin
35	P72/CLK2	CLK VIMO	O	C	-	-		Z	O/L	O/L	MAIN-VIDEO μcom comm. control pin
36	P71/RXD2/	VOMI	I	-	Lv	-	-	Z	O/L	O/L	MAIN-VIDEO μcom comm. control pin
37	P70/TXD2/	VIMO	O	N	-	-	Eu	Z	O/L	O/L	MAIN-VIDEO μcom comm. control pin
38	P67/TXD1	FRONT TxD	O	C	-	-	-	Z	O/L	O/L	Data transfer pin to outside(MAKER BOOT)
39	VCC	VCC	-	-	-	-	-	-	-	-	+ 5 V
40	P66/RXD1	FRONT RxD	I	-	Lv	-	-	Z	I	O/L	Data transfer pin from outside(MAKER BOOT)
41	VSS	VSS	-	-	-	-	-	-	-	-	GND
42	P65/CLK1	ZVOL DATA4	O	C	-	-	-	Z	O/L	O/L	E-VR control output for ZONE4(BD3811K1)
43	P64/$\overline{\text{CTS1}}$	ZVOL CLK4	O	C	-	-	-	Z	O/L	O/L	E-VR control output for ZONE4(BD3811K1)
44	P63/TXD0	BACK TxD	O	C	-	-	Ed	Z	O/L	O/L	Data transfer pin to outside(AMX)
45	P62/RXD0	BACK RxD	I	-	Lv	-	Ed	Z	I	O/L	Data transfer pin from outside(MAKER BOOT)
46	P61/CLK0	ZVOL DATA3	O	C	-	-	-	Z	O/L	O/L	E-VR control output for ZONE3(BD3811K1)
47	P60/$\overline{\text{CTS0}}$	RDS CE	O	C	-	-	-	Z	O/L	O/L	RDS data output(LC72720)
48	P137	NC	O	C	-	-	-	Z	O/L	O/L	Not used
49	P136/ISCLK2	NC	O	C	-	-	-	Z	O/L	O/L	Not used
50	P135/ISRXD2	NC	I	-	-	-	-	Z	O/L	O/L	Not used
51	P134/ISTXD2	NC	O	C	-	-	-	Z	O/L	O/L	Not used
52	P57	NC	O	C	-	-	-	Z	O/L	O/L	Not used
53	P56	NC	O	C	-	-	-	Z	O/L	O/L	Not used
54	P55/EPM	ZVOL CLK3/$\overline{\text{FRASH EPM}}$	O	C	-	-	-	Z	O/L	O/L	E-VR control output for ZONE3(BD3811K1) /Rewrite boot program start:L input set
55	P54	NC	O	C	-	-	-	Z	O/L	O/L	Not used
56	P133	NC	O	C	-	-	Ed	Z	O/L	O/L	Not used
57	VSS	VSS	-	-	-	-	-	-	-	-	GND
58	P132	ZVOL DATA2	O	C	-	-	-	Z	O/L	O/L	E-VR control output for ZONE2(BD3811K1)
59	VCC	VCC	-	-	-	-	-	-	-	-	+ 5 V
60	P131	ZVOL CLK2	O	C	-	-	-	Z	O/L	O/L	E-VR control output for ZONE2(BD3811K1)
61	P130	E.VOL STB2	O	C	-	-	-	Z	O/L	O/L	E-VR control output for MAIN ZONE(TC94A32FG)
62	P53	F232ET	O	C	-	-	-	Z	O/L	O/L	FRONT232 → ETHERNET pass control pin
63	P52	F232IE	O	C	-	-	-	Z	O/L	O/L	FRONT232 → IEEE1394 pass control pin
64	P51	F232MCPU	O	C	-	-	-	Z	O/L	O/L	FRONT232 → MAIN pass control pin
65	P50/CE	FRASH CE	I	-	-	-	Ed	Z	I	I	Rewrite boot program start:H input set
66	P127	E.VOL STB1	O	C	-	-	-	Z	O/L	O/L	E-VR control output for MAIN ZONE(TC94A32FG)
67	P126	E.VOL DATA	O	C	-	-	-	Z	O/L	O/L	E-VR control output for MAIN ZONE(TC94A32FG)
68	P125	E.VOL CLK	O	C	-	-	-	Z	O/L	O/L	E-VR control output for MAIN ZONE(TC94A32FG)
69	P47/$\overline{\text{CS0}}$/$\overline{\text{A23}}$	MIC DET	I	-	Lv	-	-	Z	O/L	O/L	Microphone detect input(Detected:L)
70	P46/$\overline{\text{CS1}}$/A22	FUNC STB ADIN	O	C	-	-	-	Z	O/L	O/L	STB output for function switching control(A/D IN) (TC9274F-022)
71	P45/$\overline{\text{CS2}}$/A21	FUNC STB EIN	O	C	-	-	-	Z	O/L	O/L	STB output for function switching control (EXT.IN DOWN-MIX)(TC9274F-022)
72	P44/$\overline{\text{CS3}}$/A20	FUC STB INH	O	C	-	-	-	Z	O/L	O/L	STB output for function switching control (REC INH)(TC9274F-022)
73	P43/A19	FUC STB IN	O	C	-	-	-	Z	O/L	O/L	STB output for function switching control (ANALOG SW)(TC94A46FGX2)
74	VCC	VCC	-	-	-	-	-	-	-	-	+ 5 V
75	P42/A18	FUNC STB VSEL2	O	C	-	-	-	Z	O/L	O/L	STB output for function switching control (VOL IN)(TC9274F-022)
76	VSS	VSS	-	-	-	-	-	-	-	-	GND
77	P41/A17	FUNC STB VSEL1	O	C	-	-	-	Z	O/L	O/L	STB output for function switching control (VOL IN)(TC9274F-022)
78	P40/A16	FUC STB AIN	O	C	-	-	-	Z	O/L	O/L	STB output for function switching control (POWER AMP ASSIGN)(TC94A46FG)(TC94A46FG × 4)
79	P37/D15	FUNC DATA	O	C	-	-	-	Z	O/L	O/L	DATA output for function switching control(TC94A46FG/TC9274F)
80	P36/D14	FUNC CLK	O	C	-	-	-	Z	O/L	O/L	CLK output for function switching control(TC94A46FG/TC9274F)
81	P35/D13	AEXP OE	O	C	-	-	-	Z	O/L	O/L	OE output for expander control(BU4094B)
82	P34/D12	AEXP STB	O	C	-	-	-	Z	O/L	O/L	STB output for expander control(BU4095B)
83	P33/A11	AEXP DATA	O	C	-	-	-	Z	O/L	O/L	DATA output for expander control(BU4094B)
84	P32/D10	AEXP CLK	O	C	-	-	-	Z	O/L	O/L	CLK output for expander control(BU4094B)
85	P31/D9	TUNER POWER	O	C	-	-	-	Z	O/L	O/L	TUNER power on/off switching (ON:H)
86	P124	TU STB	O	C	-	-	-	Z	O/L	O/L	PLL control pin(LC72131)

Pin	Pin Name	Symbol	I/O	Type	Det	Op(Int.)	Op(Ext.)	Res	STBY	stop	FUNCTION
87	P123	E2P CS	O	C	-	-	-	Z	O/L	O/L	E2PROM control pin
88	P122/ISRXD3	E2P DO	I	-	Lv	-	-	Z	O/L	O/L	E2PROM control pin
89	P121/ISCLK3	E2P CLK	O	C	-	-	-	Z	O/L	O/L	E2PROM control pin
90	P120/ISTXD3	E2P DI	O	C	-	-	-	Z	O/L	O/L	E2PROM control pin
91	VCC	VCC	-	-	-	-	-	-	-	-	+ 5 V
92	P30/D8	TU/RDS DIN	O	C	-	-	-	Z	O/L	O/L	PLL & RDS control pin (LC72131 & LC72720)
93	VSS	VSS	-	-	-	-	-	-	-	-	GND
94	P27/AN27/D7	TU/RDS CLK	O	C	-	-	-	Z	O/L	O/L	PLL & RDS control pin (LC72131 & LC72720)
95	P26/AN26/D6	TU DOUT	I	-	Lv	-	-	Z	I	O/L	PLL control pin (LC72131)
96	P25/AN25/D5	$\overline{\text{MUTE(T)}}$	O	C	-	-	-	Z	O/L	O/L	TUNER muting control(MUTE:L)
97	P24/AN24/D4	$\overline{\text{STEREO}}$	I	-	Lv	-	Eu	Z	I	O/L	When TUNER FM stereo receive: L
98	P23/AN23/D3	$\overline{\text{TUNED}}$	I	-	Lv	-	Eu	Z	I	O/L	TUNER turned detect (Detected:L)
99	P22/AN22/D2	ACK EIMO	O	C	-	-	-	Z	O/L	O/L	ETHERNET control pin
100	P21/AN21/D1	RDS RESET	O	C	-	-	-	Z	O/L	O/L	RDS reset output(LC72720)
101	P20/AN20/D0	ETHER RST	O	C	-	-	-	Z	O/L	O/L	ETHERNET control pin
102	P17/$\overline{\text{INT5}}$/D15	PROTECTION	I	-	E ↓ &L	-	-		I	I	Protection detect input(Detected:L)
103	P16/$\overline{\text{INT4}}$/D14	REQ EOMI	I	-	E ↓ &L	-	-		I	O/L	ETHERNET control pin
104	P15/$\overline{\text{INT3}}$/D13	REQ SOMI	I	-	E ↓ &L	-	-		I	O/L	MAIN-SUB μcom comm. control pin
105	P14/D12	ACK SIMO	O	C	-	-	-	Z	O/L	O/L	MAIN-SUB μcom comm. control pin
106	P13/D11	RST SUB(RESET2)	O	C	-	-	-	Z	O/L	O/L	SUB-μcom reset output
107	P12/D10	ETHER POWER	O	C	-	-	-	Z	O/L	O/L	ETHERNET POWER ON/OFF switching(ON:H)
108	P11/D9	ACK VIMO	O	C	-	-	-	Z	O/L	O/L	MAIN-VIDEO μcom comm. control pin
109	P10/D8	E.VOL STB SW	O	C	-	-	-	Z	O/L	O/L	E-VR control output for EXT.IN SW(TC94A32FG)
110	P07/AN07/D7	E.VOL STB3	O	C	-	-	-	Z	O/L	O/L	E-VR control output for MAIN ZONE(TC94A32FG)
111	P06/AN06/D6	RDS DATAOUT	I	-	E ↓ &L	-	-		I	O/L	RDS data input(LC72720)
112	P05/AN05/D5	AMPFANIN	I	-	Lv	-	-	Z	O/L	O/L	AMP temperature detect(Detected:L)
113	P04/AN04/D4	FAN ON	O	C	-	-	-	Z	O/L	O/L	FAN control(Operation:H)
114	P114	FAN LOW	O	C	-	-	-	Z	O/L	O/L	FAN control(Low-speed operation:H)
115	P113	TFAN IN	I	-	Lv	-	-	Z	O/L	O/L	TRANS temperature detect(Detected:L)
116	P112/	H/P DET	I	-	-	-	-	Z	O/L	O/L	H/P detect input(Detected:H)
117	P111/	NC	O	C	-	-	-	Z	O/L	O/L	Not used
118	P110/	LED SD	O	C	-	-	-	Z	O/L	O/L	LED driver control pin(M66313FP)
119	P03/AN03/D3	LED OE	O	C	-	-	-	Z	I	I	LED driver control pin(M66313FP) *This port is set as an input during STANDBY.
120	P02/AN02/D2	LED LE	O	C	-	-	-	Z	O/L	O/L	LED driver control pin(M66313FP)
121	P01/AN01/D1	LED CK	O	C	-	-	-	Z	O/L	O/L	LED driver control pin(M66313FP)
122	P00/AN00/D0	REDLED	O	C	-	-	-	Z	O/L	O/L	POWER/STANDBY LED control pin
123	P157/AN157	GRNLED	O	C	-	-	-	Z	O/L	O/L	POWER/STANDBY LED control pin
124	P156/AN156	FL RST	O	C	-	-	-	Z	O/L	O/L	FL tube control pin(LC75721E)
125	P155/AN155	FL CE2	O	C	-	-	-	Z	O/L	O/L	FL tube control pin(LC75721E)
126	P154/AN154	FL CE1	O	C	-	-	-	Z	O/L	O/L	FL tube control pin(LC75721E)
127	P153/AN153	FL DATA	O	C	-	-	-	Z	O/L	O/L	FL tube control pin(LC75721E)
128	P152/AN152/	FL CLK	O	C	-	-	-	Z	O/L	O/L	FL tube control pin(LC75721E)
129	P151/AN151/	VSEL B	I	-	Lv	-	Eu	Z	O/L	O/L	Master VR rotation detect input（Rotary encoder）
130	VSS	VSS	-	-	-	-	-	-	-	-	GND
131	P150/AN150/	VSEL A	I	-	Lv	-	Eu	Z	O/L	O/L	Master VR rotation detect input（Rotary encoder）
132	VCC	VCC	-	-	-	-	-	-	-	-	+ 5 V
133	P107/AN7	ISEL B	I	-	Lv	-	Eu	Z	O/L	O/L	Input selector rotation detect input（Rotary encoder）
134	P106/AN6	ISEL A	I	-	Lv	-	Eu	Z	O/L	O/L	Input selector rotation detect input（Rotary encoder）
135	P105/AN5	KEY4	I	-	Lv	-	Eu	Z	O/L	O/L	Button input4
136	P104/AN4	KEY3	I	-	Lv	-	Eu	Z	O/L	O/L	Button input3
137	P103/AN3	KEY2	I	-	Lv	-	Eu	Z	O/L	O/L	Button input2
138	P102/AN2	KEY1	I	-	Lv	-	Eu	Z	O/L	O/L	Button input1
139	P101/AN1	ACK ZIMO	O	C	-	-	-	Z	O/L	O/L	MAIN-ZONE μcom comm. control pin
140	AVSS	AVSS	-	-	-	-	-	-	-	-	AD GND
141	P100/AN0	MODE	I	-	Lv	-	-	Z	O/L	O/L	Destination switching input
142	VREF	VREF	-	-	-	-	-	-	-	-	AD ref. + 5 V
143	AVCC	AVCC	-	-	-	-	-	-	-	-	AD + 5 V
144	P97/$\overline{\text{ADTRG}}$/RXD4	ZOMI	I	-	Lv	-	Ed	Z	I	O/L	MAIN-ZONE μcom comm. control pin

MBM29LV160BE90TN (IC313) 1394 P.W.B.
MBM29LV160BE90TN (IC605,704,804) DIGITAL P.W.B.

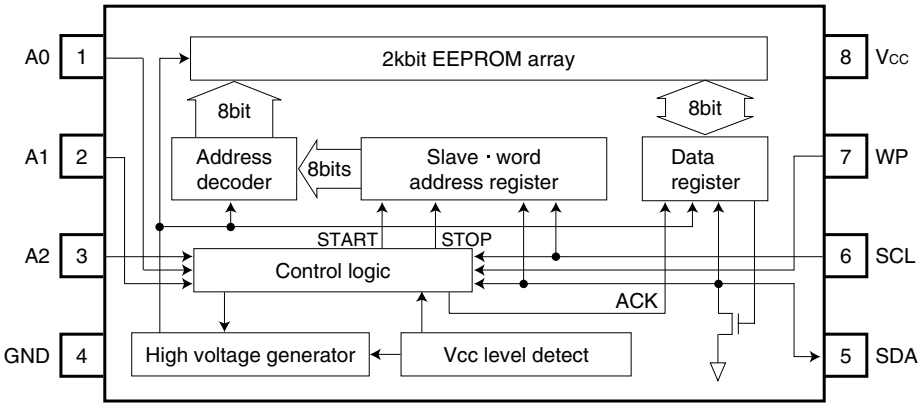
TSOP(I)



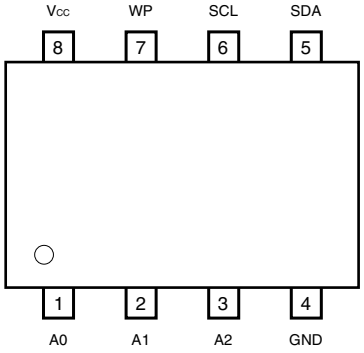


BR24L02F-WE2 (IC101,102,201,202) D,VIDEO P.W.B.

Block diagram



Pin configuration



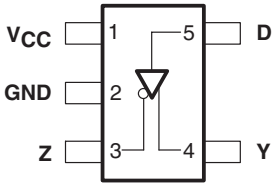
Pin name

Pin name	I / O	Function
Vcc		Power supply
GND		Ground (0V)
A0, A1, A2	IN	Slave address set
SCL	IN	Serial clock input
SDA	IN / OUT	Slave and word address, serial data input, serial data output [1]
WP	IN	Write protect input

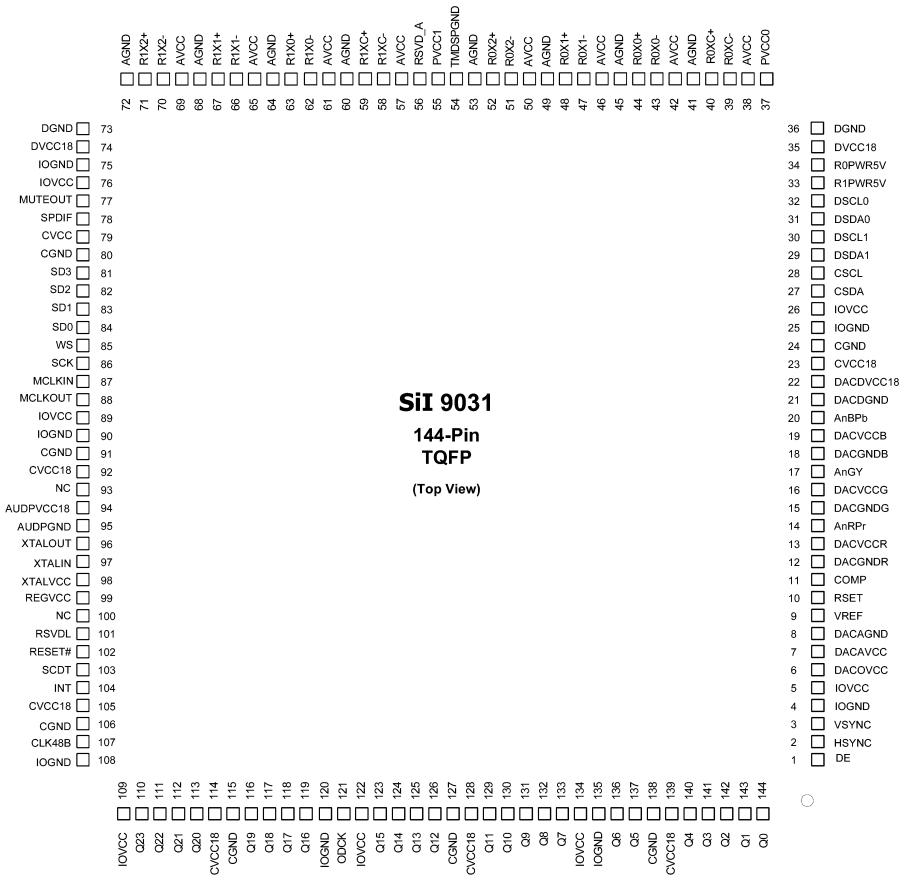
1 An open drain output requires a pull-up resistor.

SN65LVDS1DBVR (IC102) AD P.W.B.
SN65LVDS1DBVR (IC108) D.VIDEO P.W.B.
SN65LVDS1DBVR (IC402) DIGITAL P.W.B

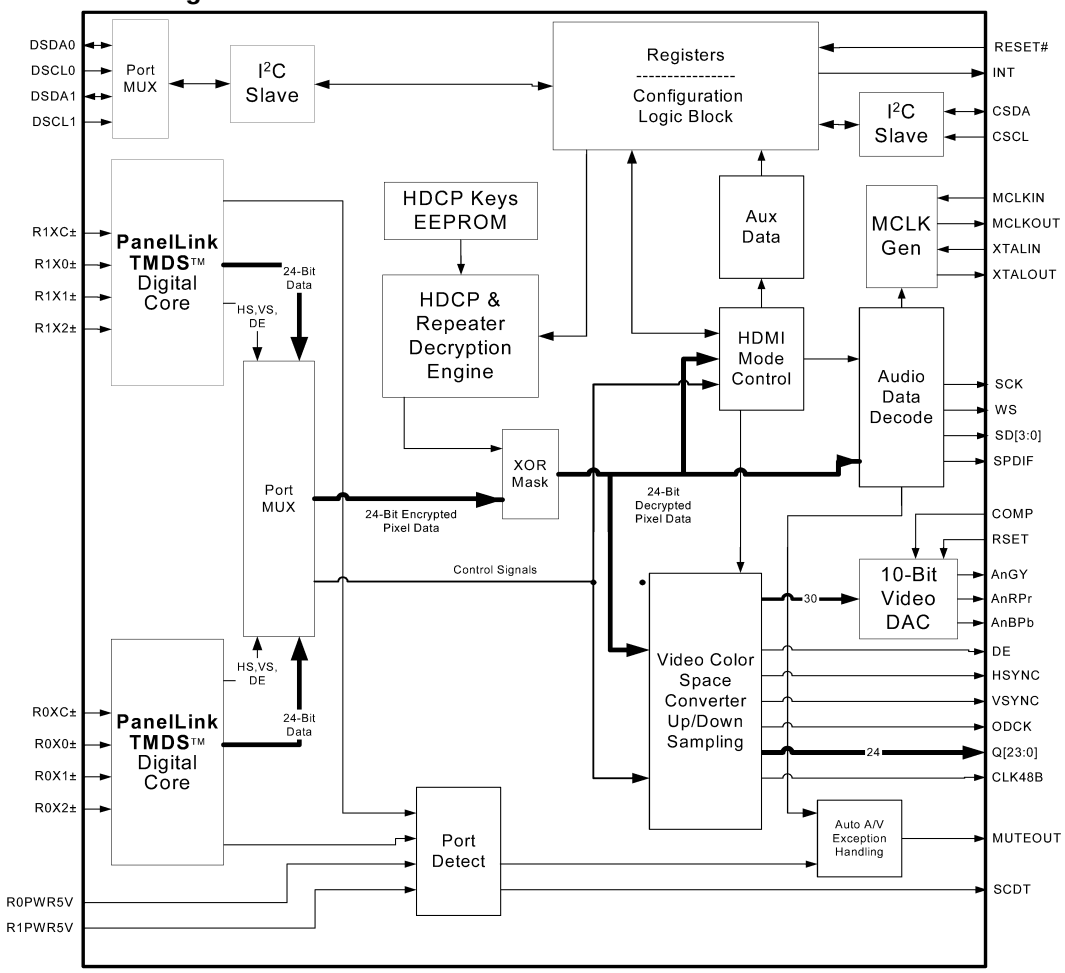
(TOP VIEW)



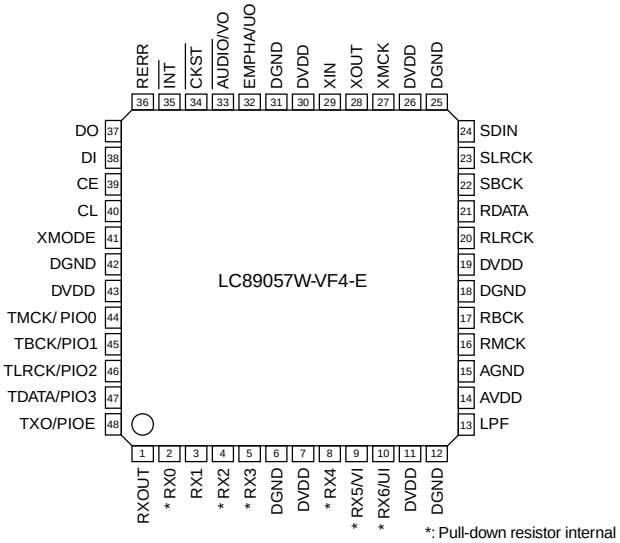
SII9031 (IC103,203) D.VIDEO P.W.B.



Functional Block Diagram



LC89057W-VF4-E (IC103-110) DIGITAL P.W.B.

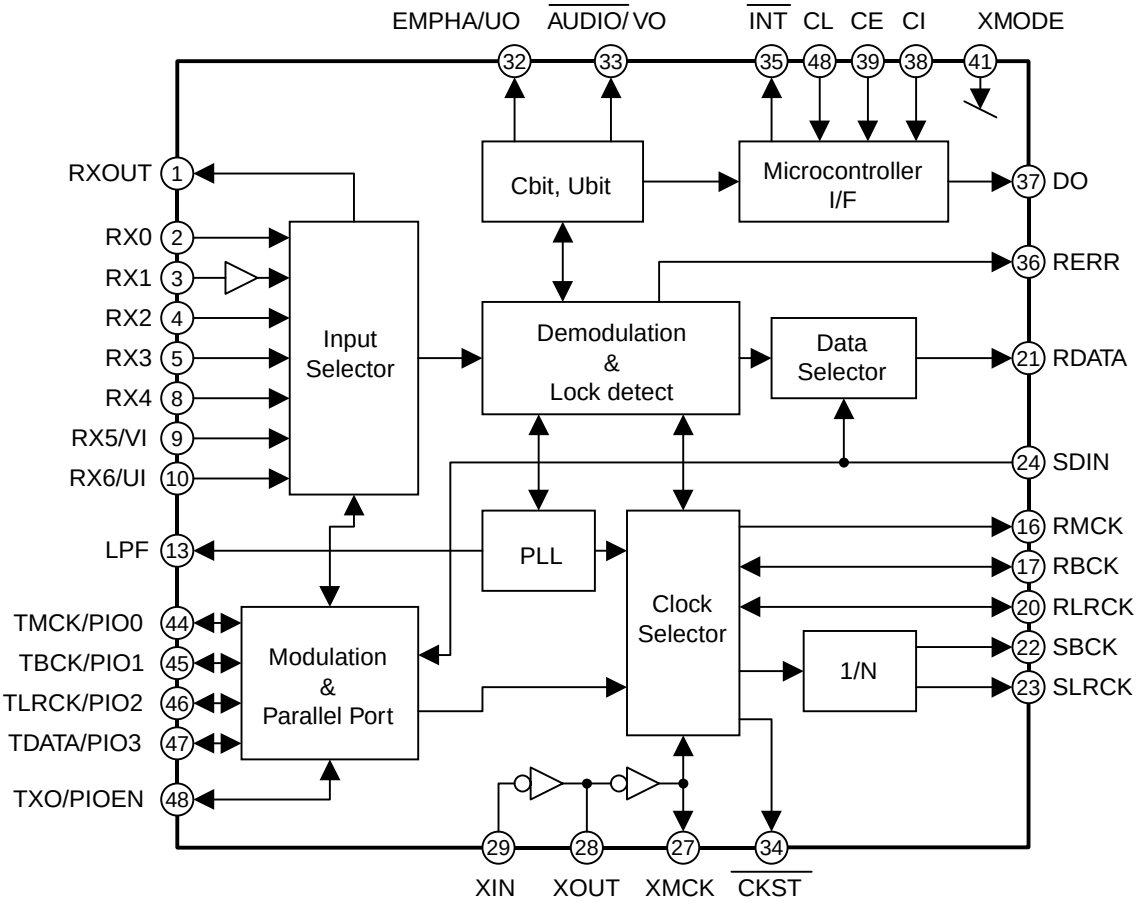


*: Pull-down resistor internal

LC89057W-VF4-E Terminal Function

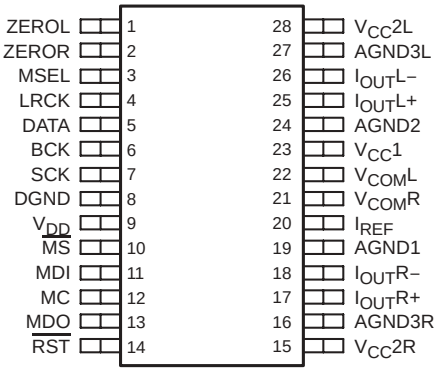
Pin No.	Pin	I/O	Function
1	RXOUT	O	Input bi-phase selection data output pin
2	RX0	I_5	TTL-compatible digital data input pin
3	RX1	I	Coaxial-compatible digital data input pin with built-in amplifier
4	RX2	I_5	TTL-compatible digital data input pin
5	RX3	I_5	TTL-compatible digital data input pin
6	DGND		Digital GND
7	DVDD		Digital power supply
8	RX4	I_5	TTL-compatible digital data input pin
9	RX5/VI	I_5	TTL-compatible digital data || Validity flag input pin for modulation
10	RX6/UI	I_5	TTL-compatible digital data || User data input pin for modulation
11	DVDD		PLL digital power supply
12	DGND		PLL digital GND
13	LPF	O	PLL loop filter connection pin
14	ACDD		PLL analog power supply
15	AGND		PLL analog GND
16	RMCK	O	R system clock output pin (256fs, 512fs, XIN, VCO)
17	RBCK	O/I	R bit clock input/output pin (64fs)
18	DGND		Digital GND
19	DVDD		Digital power supply
20	RLRCK	O/I	R LR clock input/output pin (fs)
21	RDATA	O	Serial audio data input pin
22	SBCK	O	S bit clock output pin (32fs, 64fs, 128fs)
23	SLRCK	O	S LR clock output pin (fs/2, fs, 2fs)
24	SDIN	I_5	Serial audio data input pin
25	DGND		Digital GND
26	DVDD		Digital power supply
27	XMCK	O	Oscillation amplifier output pin
28	XOUT	O	Crystal resonator connection output pin
29	XIN	I	Crystal resonator connection, external supply clock input pin (24.576 MHz or 12.288 MHz)
30	DVDD		Digital power supply
31	DGND		Digital GND
32	EMPHA/UO	I/O	Emphasis information || U data output || Chip address setting pin
33	$\overline{\text{AUDIO}}$/VO	I/O	Non-PCM output || V flag output || Chip address setting pin
34	$\overline{\text{CKST}}$	I/O	Clock switch transition period signal || Demodulation master or slave function switch pin
35	$\overline{\text{INT}}$	I/O	Microcontroller interrupt output || Modulation or general-purpose I/O switch pin
36	RERR	O	PLL clock error, data error flag output
37	DO	O	Microcontroller I/F read data output pin (3-state)
38	DI	I_5	Microcontroller I/F write data input pin
39	CE	I_5	Microcontroller I/F chip enable input pin
40	CL	I_5	Microcontroller I/F clock input pin
41	XMODE	I_5	System reset input pin
42	DGND		Digital GND
43	DVDD		Digital power supply
44	TMCK/PIO0	I/O	Modulation 256fs system clock input || General-purpose I/O input/output pin
45	TMCK/PIO1	I/O	Modulation 64fs bit clock input || General-purpose I/O input/output pin
46	TLRCK/PIO2	I/O	Modulation fs clock input || General-purpose I/O input/output pin
47	TLRCK/PIO3	I/O	Modulation serial audio data input || General-purpose I/O input/output pin
48	TXO/PIOEN	O/I	Modulation data output || General-purpose I/O enable input pin

LC89057W-VF4-E BLOCK DIAGRAM

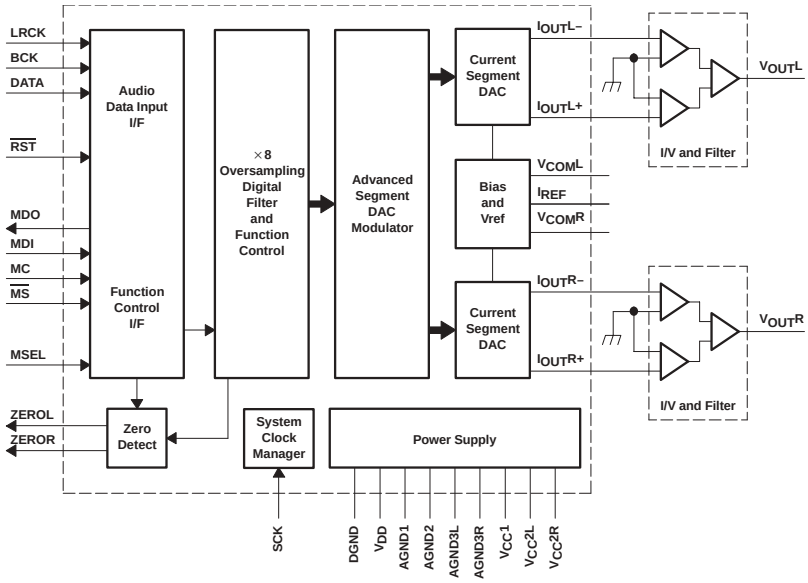


PCM1792DBR (IC201-204,401,402,501,502) DAC P.W.B.

(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM

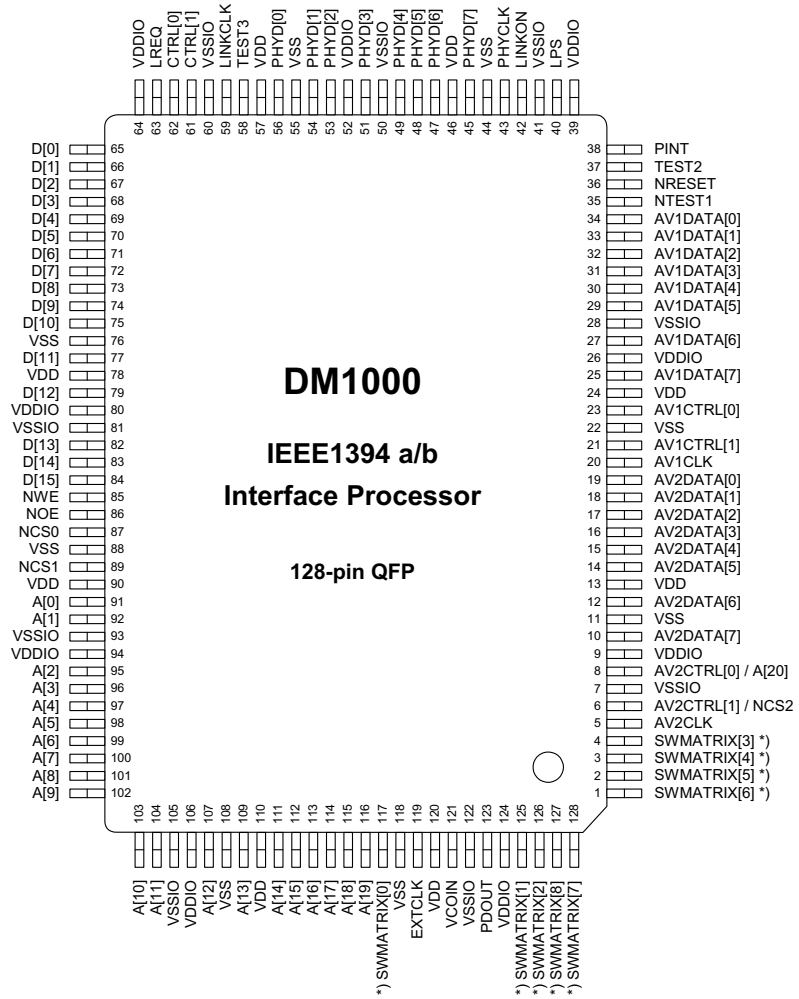


Terminal Functions

TERMINAL NAME	TERMINAL PIN	I/O	DESCRIPTIONS
AGND1	19	–	Analog ground (internal bias)
AGND2	24	–	Analog ground (internal bias)
AGND3L	27	–	Analog ground (L-channel DACFF)
AGND3R	16	–	Analog ground (R-channel DACFF)
BCK	6	I	Bit clock input(1)
DATA	5	I	Serial audio data input for normal operation(1)
DGND	8	–	Digital ground
$I_{OUT}L+$	25	O	L-channel analog current output+
$I_{OUT}L-$	26	O	L-channel analog current output–
$I_{OUT}R+$	17	O	R-channel analog current output+
$I_{OUT}R-$	18	O	R-channel analog current output–
I_{REF}	20	–	Output current reference bias pin
LRCK	4	I	Left and right clock (f_S) input for normal operation(1)
MC	12	I	Mode control clock input(1)
MDI	11	I	Mode control data input(1)
MDO	13	I/O	Mode control readback data output(3)
$\overline{MS}$	10	I/O	Mode control chip-select input(2)
MSEL	3	I	$I^2C/\overline{SPI}$ select(1)
$\overline{RST}$	14	I	Reset(1)
SCK	7	I	System clock input(1)
$V_{CC}1$	23	–	Analog power supply, 5 V
$V_{CC}2L$	28	–	Analog power supply (L-channel DACFF), 5 V
$V_{CC}2R$	15	–	Analog power supply (R-channel DACFF), 5 V
$V_{COM}L$	22	–	L-channel internal bias decoupling pin
$V_{COM}R$	21	–	R-channel internal bias decoupling pin
V_{DD}	9	–	Digital power supply, 3.3 V
ZEROL	1	I/O	Zero flag for L-channel(2)
ZEROR	2	I/O	Zero flag for R-channel(2)

(1) Schmitt-trigger input, 5-V tolerant
(2) Schmitt-trigger input and output. 5-V tolerant input and CMOS output
(3) Schmitt-trigger input and output. 5-V tolerant input. In I^2C mode, this pin becomes an open-drain 3-state output; otherwise, this pin is a CMOS output.

DM1000 (IC201) 1394 P.W.B.

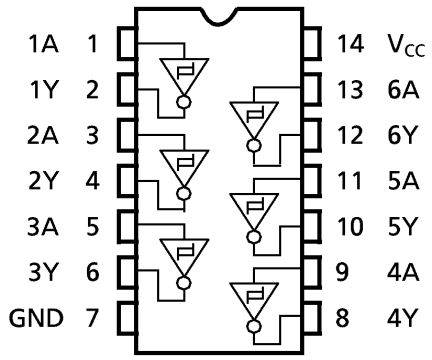


Pin Assignment by Pin Number

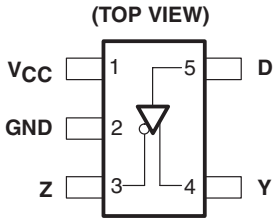
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	SWMATRIX[6] *)	33	AV1DATA[1]	65	D[0]	97	A[4]
2	SWMATRIX[5] *)	34	AV1DATA[7]	66	D[1]	98	A[5]
3	SWMATRIX[4] *)	35	NTEST1	67	D[2]	99	A[6]
4	SWMATRIX[3] *)	36	NRESET	68	D[3]	100	A[7]
5	AV2CLK	37	TEST2	69	D[4]	101	A[8]
6	AV2CTRL[1] / NCS[2]	38	PINT	70	D[5]	102	A[9]
7	VSSIO	39	VDDIO	71	D[6]	103	A[10]
8	AV2CTRL[0] / A[20]	40	LPS	72	D[7]	104	A[11]
9	VDDIO	41	VSSIO	73	D[8]	105	VSSIO
10	AV2DATA[7]	42	LINKON	74	D[9]	106	VDDIO
11	VSS	43	PHYCLK	75	D[10]	107	A[12]
12	AV2DATA[6]	44	VSS	76	VSS	108	VSS
13	VDD	45	PHYD[7]	77	D[11]	109	A[13]
14	AV2DATA[5]	46	VDD	78	VDD	110	VDD
15	AV2DATA[4]	47	PHYD[6]	79	D[12]	111	A[14]
16	AV2DATA[3]	48	PHYD[5]	80	VDDIO	112	A[15]
17	AV2DATA[2]	49	PHYD[4]	81	VSSIO	113	A[16]
18	AV2DATA[1]	50	VSSIO	82	D[13]	114	A[17]
19	AV2DATA[0]	51	PHYD[3]	83	D[14]	115	A[18]
20	AV1CLK	52	VDDIO	84	D[15]	116	A[19]
21	AV1CTRL[1]	53	PHYD[2]	85	NWE	117	SWMATRIX[0] *)
22	VSS	54	PHYD[1]	86	NOE	118	VSS
23	AV1CTRL[0]	55	VSS	87	NCS[0]	119	EXTCLK
24	VDD	56	PHYD[0]	88	VSS	120	VDD
25	AV1DATA[7]	57	VDD	89	NCS[1]	121	VCOIN
26	VDDIO	58	TEST3	90	VDD	122	VSSIO
27	AV1DATA[6]	59	LINKCLK	91	A[0]	123	PDOUT
28	VSSIO	60	VSSIO	92	A[1]	124	VDDIO
29	AV1DATA[5]	61	CTRL[1]	93	VSSIO	125	SWMATRIX[1] *)
30	AV1DATA[4]	62	CTRL[0]	94	VDDIO	126	SWMATRIX[2] *)
31	AV1DATA[3]	63	LREQ	95	A[2]	127	SWMATRIX[8] *)
32	AV1DATA[2]	64	VDDIO	96	A[3]	128	SWMATRIX[7] *)

*) refer to chapter 4 for the Switch-Matrix description

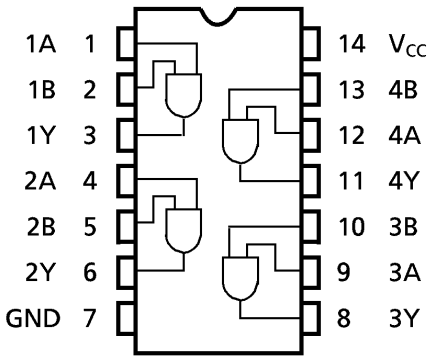
TC74VHC14FT (IC104,114) AD P.W.B.



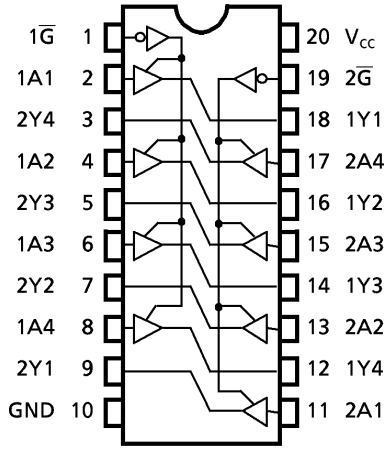
SN65LVDS1DBVR (IC108) D.VIDEO P.W.B.
(IC102) AD P.W.B.
(IC402) DIGITAL P.W.B.



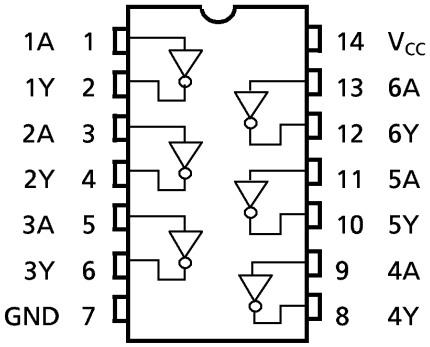
TC74VHC08FT (IC111) DIGITAL P.W.B.
(IC319,321) AD P.W.B.



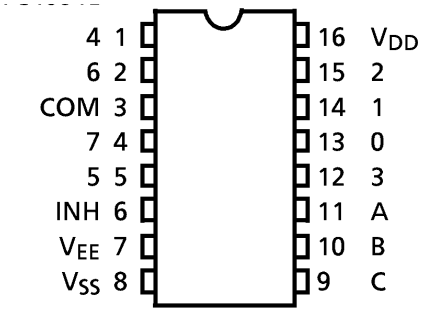
TC74VHC244FT (IC112,304-307,403,406,408,603,906) DIGITAL P.W.B.



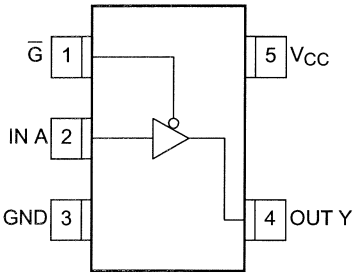
TC74VHC04FT (IC113) DIGITAL P.W.B.



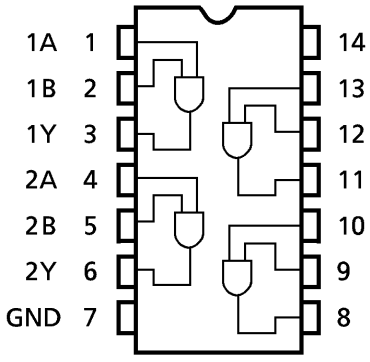
TC4051BFT (IC121-123,125-127,129-131) A.VIDEO P.W.B.
TC4052BFT (IC116-119,810,811) A.VIDEO P.W.B.
TC4051BFT (IC112-115,124,128,132) A.VIDEO P.W.B.



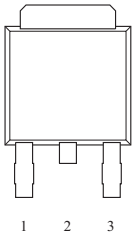
TC7SZ125F (IC308) DIGITAL P.W.B.



TC74VHCT08AFT (IC306) D.VIDEO P.W.B.

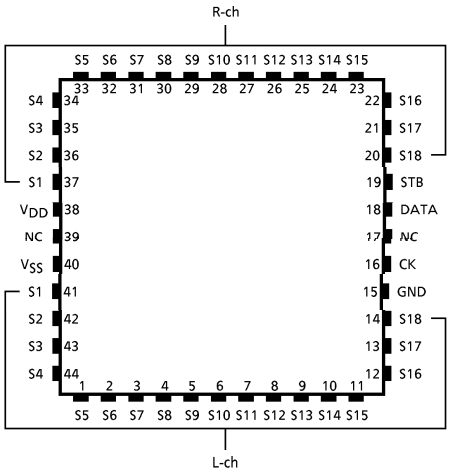


KIA7912F-RTF (IC303,508) DIGITAL P.W.B.

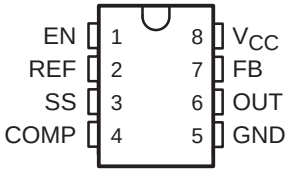


1. GND
2. INPUT
3. OUTPUT

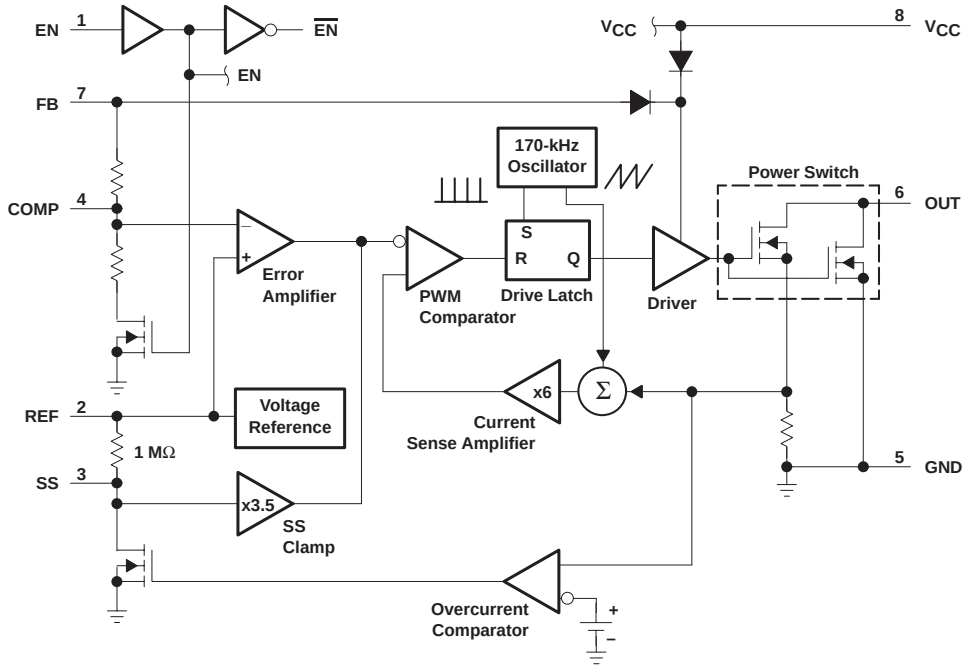
TC9274F-022 (IC120,213,214,401,402) AUDIO P.W.B.



TPS6734IDR (IC301) DIGITAL P.W.B.



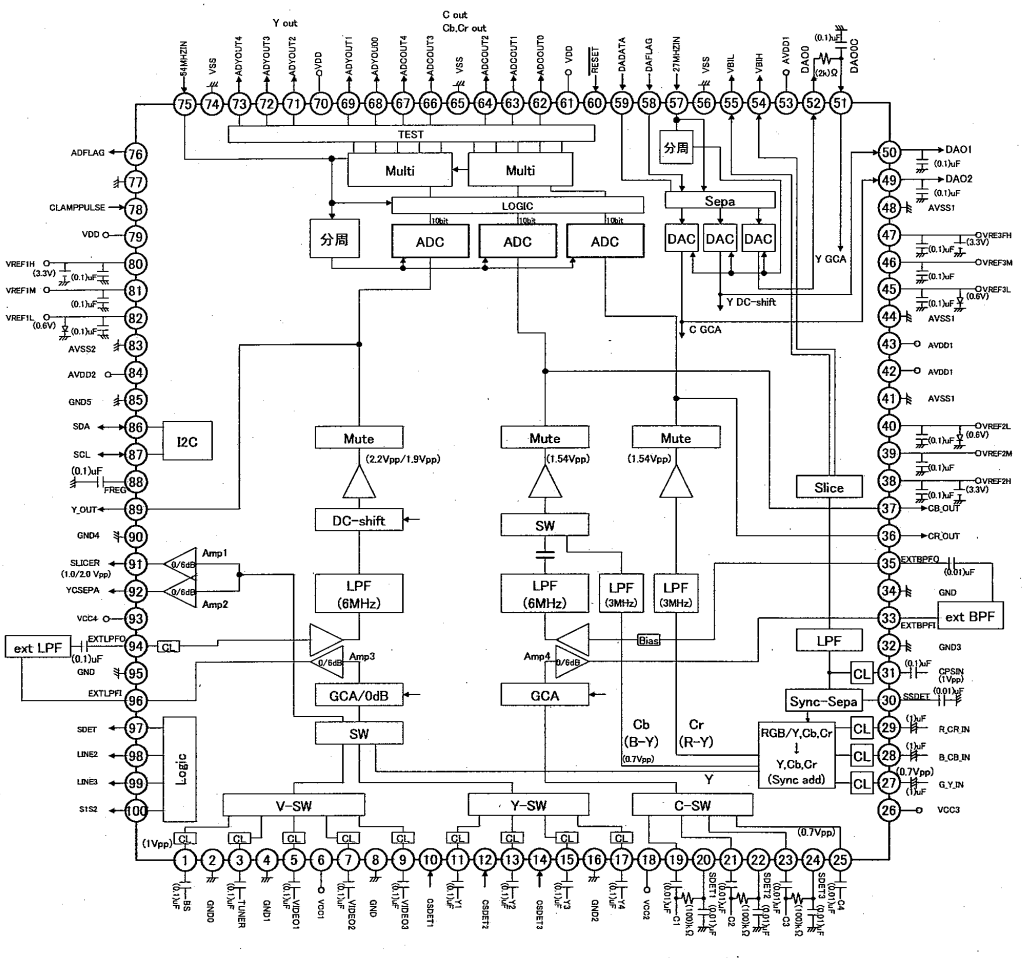
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
EN	1	Enable. EN ≥ 2 V turns on the TPS6734. EN ≤ 0.4 V turns it off and reduces the supply current to 3 μA max.
REF	2	1.22-V reference voltage output. REF can source 100 μA for external loads.
SS	3	Soft Start. A capacitor between SS and GND brings the output voltage up slowly at power-up.
COMP	4	Compensation connection. A 0.001-μF capacitor between COMP and FB stabilizes the feedback loop.
GND	5	Ground
OUT	6	N-channel MOSFET drain connection
FB	7	Feedback voltage. FB is connected to the converter output for the feedback loop.
V_{CC}	8	Supply voltage input

AN13310BA (IC406) D.VIDEO P.W.B.

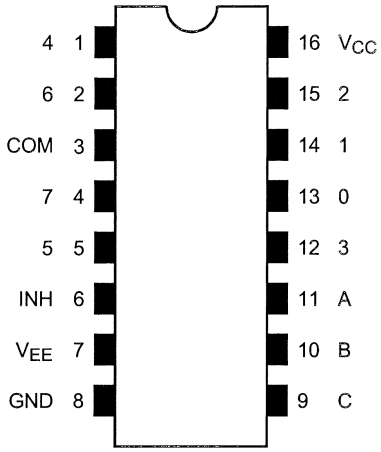


AN13310BA Terminal Function

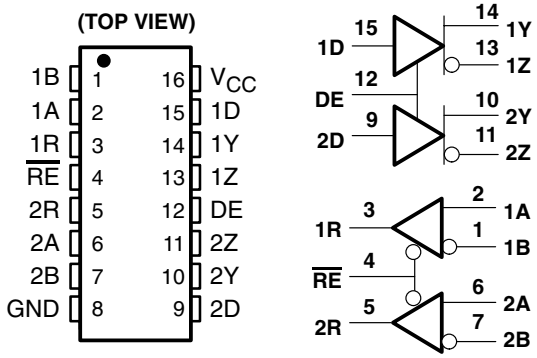
Pin No.	Function	Impedance	Pin No.	Function	Impedance
1	BS input	Emitter Clamp	26	VCC3 (Analog Power supply)	5[V]
2	GND0(Analog ground)	0 [V]	27	RGB Gin/Cy input	Emitter Clamp
3	TUNER input	Emitter Clamp	28	RGB Bin/Cb input	Clamp/38kΩ
4	GND1(Analog ground)	0 [V]	29	RGB Rin/Cr input	Clamp/38kΩ
5	VIDEO1 input	Emitter Clamp	30	Sync Sepa DET	1kΩ
6	VCC1 (Analog Power supply)	5[V]	31	CPS input	Emitter Clamp
7	VIDEO2 input	Emitter Clamp	32	GND3(Analog ground)	0 [V]
8	GND(Analog ground)	0 [V]	33	EXT BPF output	Lo-Z
9	VIDEO3 input	Emitter Clamp	34	GND(Analog ground)	0 [V]
10	CSDET1 input	Pull Up 150kΩ	35	EXT BPF input	50kΩ
11	Y1 input	Emitter Clamp	36	Cr output	Lo-Z
12	CSDET2 input	Pull Up 150kΩ	37	Cb output	Lo-Z
13	Y2 input	Emitter Clamp	38	Cr ADC Referrence High Voltage	3. 3[V]
14	CSDET3 input	Pull Up 150kΩ	39	Cr ADC Referrence Middle Voltage	——
15	Y3 input	Emitter Clamp	40	Cr ADC ReferrenceL ow Voltage	0. 6[V]
16	GND2(Analog ground)	0 [V]	41	AVSS1(Analog ground)	0 [V]
17	Y4 input	Emitter Clamp	42	AVDD1 (Analog Power supply)	3. 3[V]
18	VCC2 (Analog Power supply)	5[V]	43	AVDD1 (Analog Power supply)	3. 3[V]
19	C1 input	46kΩ	44	AVSS1(Analog ground)	0 [V]
20	SDET1 input	150kΩ	45	Cb ADC Referrence Low Voltage	0. 6[V]
21	C2 input	46kΩ	46	Cb ADC Referrence Middle Voltage	——
22	SDET2 input	Hi-Z	47	Cb ADC Referrence High Voltage	3. 3[V]
23	C3 input	46kΩ	48	AVSS1	0 [V]
24	SDET3 input	Hi-Z	49	C GCA Control output	4. 5kΩ
25	C4 input	46kΩ	50	Y DC_Shifter Control output	4. 5kΩ

Pin No.	Function	Impedance	Pin No.	Function	Impedance
51	Y GCA Control input	70kΩ	76	AD Flag output	CMOS out
52	Y GCA Control output	4. 5kΩ	77	VSS(Digital ground)	0 [V]
53	AVDD1 (Analog Power supply)	3. 3[V]	78	Clamp Pulse input	Hi-Z
54	Vertical Blanking Data Insertion(H)	CMOS out	79	VDD (Digital Power supply)	3. 3[V]
55	Vertical Blanking Data Insertion(L)	CMOS out	80	Y ADC Referrence High Voltage	3. 3[V]
56	VSS(Digital ground)	0 [V]	81	Y ADC Referrence Middle Voltage	——
57	27MHz Clock input	Hi-Z	82	Y ADC Referrence Low Voltage	0. 6[V]
58	DA Flag input	Hi-Z	83	AVSS2(Analog ground)	0 [V]
59	DAC Data input	Pull Down 100kΩ	84	AVDD2 (Analog Power supply)	3. 3[V]
60	Reset input(Lo Reset)	Pull Up 100kΩ	85	GND5(Analog ground)	0 [V]
61	VDD (Digital Power supply)	3. 3[V]	86	I2C data control input	Hi-Z
62	ADCOUT0 output	CMOS out	87	I2C clock control input	Hi-Z
63	ADCOUT1 output	CMOS out	88	Referrence Voltage output	Lo-Z
64	ADCOUT2 output	CMOS out	89	Y output	Lo-Z
65	VSS(Digital ground)	0 [V]	90	GND4(Analog ground)	0 [V]
66	ADCOUT3 output	CMOS out	91	SLICER output	Lo-Z
67	ADCOUT4 output	CMOS out	92	YCSEPA output	Lo-Z
68	ADYOUT0 output	CMOS out	93	VCC4 (Analog Power supply)	5[V]
69	ADYOUT1 output	CMOS out	94	EXT LPF input	Emitter Clamp
70	VDD (Digital Power supply)	3. 3[V]	95	GND(Analog ground)	0 [V]
71	ADYOUT2 output	CMOS out	96	EXT LPF output	Lo-Z
72	ADYOUT3 output	CMOS out	97	SDET output	1kΩ
73	ADYOUT4 output	CMOS out	98	LINE2 output	10kΩ
74	VSS(Digital ground)	0 [V]	99	LINE3 output	10kΩ
75	54MHz Clock input	Hi-Z	100	S1S2 output	1kΩ

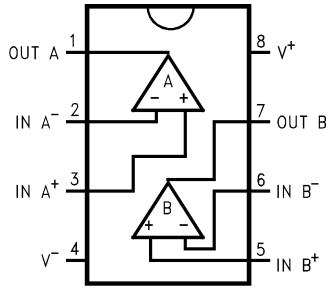
TC74LVX4051FT (IC401,408) 1394 P.W.B.



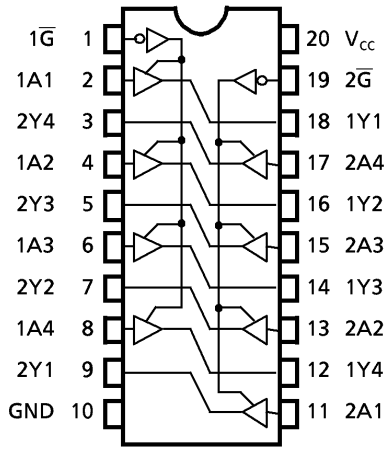
SN65LVDS050PWR (IC401) DIGITAL P.W.B.
(IC908) D.VIDEO P.W.B.



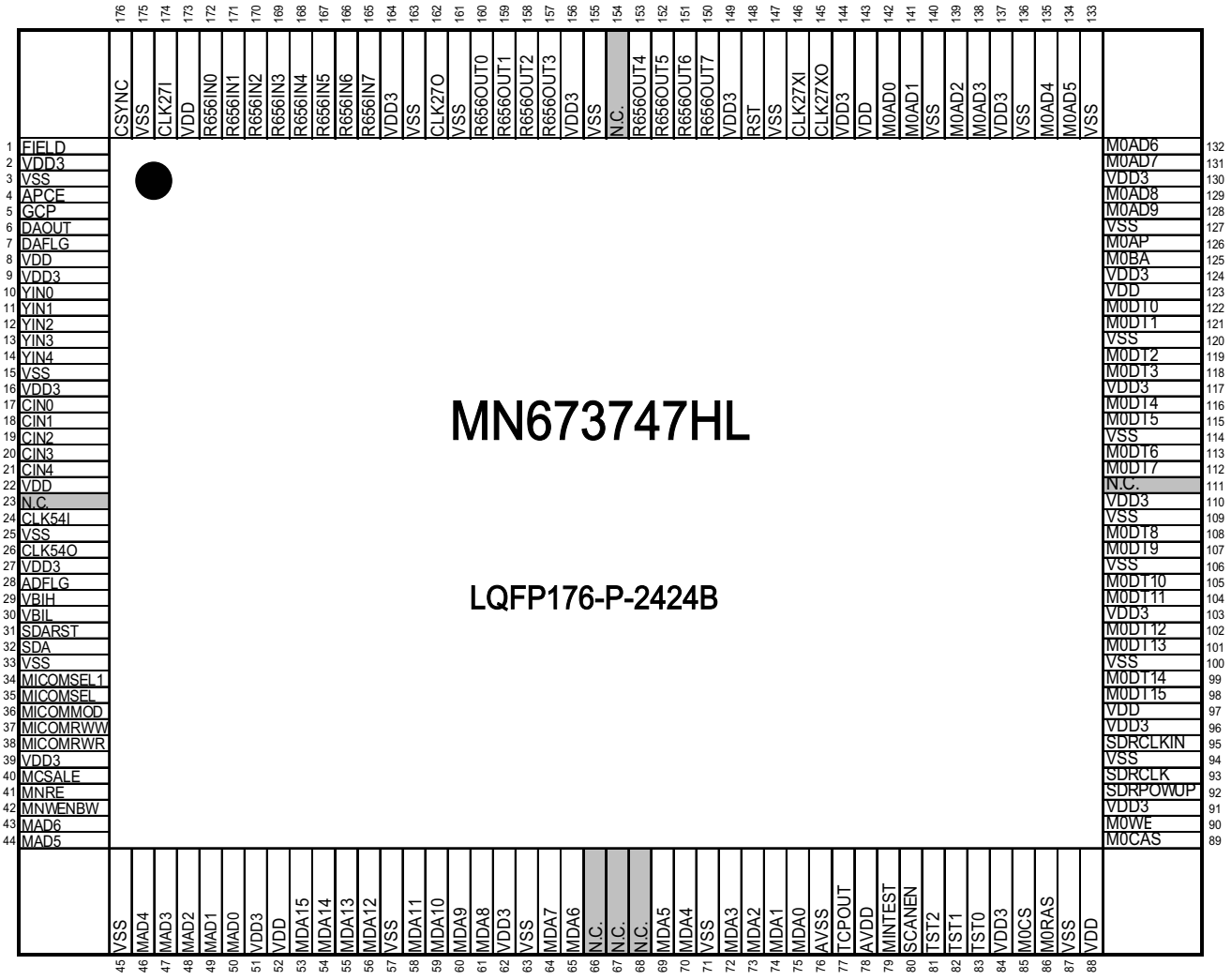
LMC6772AIM (IC403) 1394 P.W.B.



TC74VHCT244AFT (IC405,407) DIGITAL P.W.B.
(IC907) D.VIDEO P.W.B.



MN673747HL (IC410) D.VIDEO P.W.B.



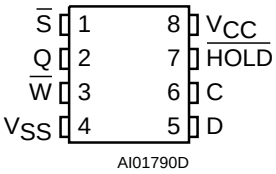
MN673747HL Terminal Function

No.	Symbol	I/O	Function
1	FIELD	O	Field discrimination signal output terminal
2	VDD3	-	3.3V
3	VSS	-	GND
4	APCE	O	Phase error 2fsc output terminal
5	GCP	O	Clamp Plus output (Sync-Tip)
6	DAOUT	O	DAC data output terminal
7	DAFLG	O	DAC select control terminal
8	VDD	-	1.5V
9	VDD3	-	3.3V
10	YIN0	I	Y/CPS ADC input terminal (LSB)
11	YIN1	I	Y/CPS ADC input terminal
12	YIN2	I	Y/CPS ADC input terminal
13	YIN3	I	Y/CPS ADC input terminal
14	YIN4	I	Y/CPS ADC input terminal (MSB)
15	VSS	-	GND
16	VDD3	-	3.3V
17	CIN0	I	C/Cr/Cb ADC input terminal (LSB)
18	CIN1	I	C/Cr/Cb ADC input terminal
19	CIN2	I	C/Cr/Cb ADC input terminal
20	CIN3	I	C/Cr/Cb ADC input terminal
21	CIN4	I	C/Cr/Cb ADC input terminal (MSB)
22	VDD	-	1.5V
23	N.C.	-	Non-Connect
24	CLK54I	I	ADC clock input terminal
25	VSS	-	GND
26	CLK54O	O	ADC clock input terminal
27	VDD3	-	3.3V
28	ADFLG	I	ADC control
29	VBIH	I	VBI Input terminal(Data)
30	VBIL	I	VBI Input terminal (Sync.)

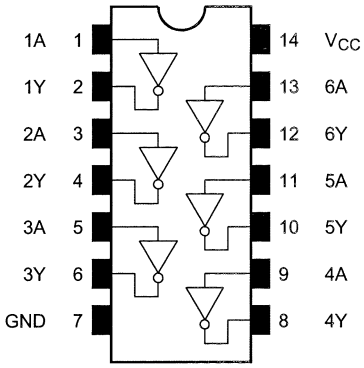
No.	Symbol	I/O	Function
31	SDARST	I	I2C reset signal input terminal(Not used VSS)
32	SDA	I/O	I2C data in/output terminal (Not used VSS)
33	VSS	-	GND
34	MICOMSEL1	I	μcom I/F select input terminal
35	MICOMSEL	I	μcom I/F select input terminal
36	MICOMMOD	I	μcom mode select input terminal
37	MICOMRWW	O	μcom encroachingus(WRITE)synchronous signal output terminal
38	MICOMRWR	O	μcom encroachingus(READ)synchronous signal output terminal
39	VDD3	-	3.3V
40	MCSALE	I	μcom I/F chip select input terminal
41	MNRE	I	μcom I/F read input terminal
42	MNWENBW	I	μcom I/F write input terminal
43	MAD6	I	μcom I/F data/address input terminal (MSB)
44	MAD5	I	μcom I/F data/address input terminal
45	VSS	-	GND
46	MAD4	I	μcom I/F data/address input terminal
47	MAD3	I	μcom I/F data/address input terminal
48	MAD2	I	μcom I/F data/address input terminal
49	MAD1	I	μcom I/F data/address input terminal
50	MAD0	I	μcom I/F data/address input terminal (LSB)
51	VDD3	-	3.3V
52	VDD	-	1.5V
53	MDA15	I/O	μcom I/F data/address in/output terminal(MSB)
54	MDA14	I/O	μcom I/F data/address in/output terminal
55	MDA13	I/O	μcom I/F data/address in/output terminal
56	MDA12	I/O	μcom I/F data/address in/output terminal
57	VSS	-	GND
58	MDA11	I/O	μcom I/F data/address in/output terminal
59	MDA10	I/O	μcom I/F data/address in/output terminal
60	MDA9	I/O	μcom I/F data/address in/output terminal
61	MDA8	I/O	μcom I/F data/address in/output terminal
62	VDD3	-	3.3V
63	VSS	-	GND
64	MDA7	I/O	μcom I/F data/address in/output terminal
65	MDA6	I/O	μcom I/F data/address in/output terminal
66	N.C.	-	Non-Connect
67	N.C.	-	Non-Connect
68	N.C.	-	Non-Connect
69	MDA5	I/O	μcom I/F data/address in/output terminal
70	MDA4	I/O	μcom I/F data/address in/output terminal
71	VSS	-	GND
72	MDA3	I/O	μcom I/F data/address in/output terminal
73	MDA2	I/O	μcom I/F data/address in/output terminal
74	MDA1	I/O	μcom I/F data/address in/output terminal
75	MDA0	I/O	μcom I/F data/address in/output terminal (LSB)
76	AVSS	-	PLL GND
77	TCPOUT	I/O	PLL TEST(OPEN)
78	AVDD	-	3.3V PLL
79	MINTEST	I	Test (OPEN or VSS)
80	SCANEN	I	Test (OPEN or VSS)
81	TST2	I	Test (OPEN or VSS)
82	TST1	I	Test (OPEN or VSS)
83	TST0	I	Test (OPEN or VSS)
84	VDD3	-	3.3V
85	M0CS	O	SDRAM CS output terminal
86	M0RAS	O	SDRAM RAS output terminal
87	VSS	-	GND
88	VDD	-	1.5V
89	M0CAS	O	SDRAM CAS output terminal
90	M0WE	O	SDRAM WE output terminal
91	VDD3	-	3.3V
92	SDRPOWUP	I	Test (OPEN or VSS)
93	SDRCLK	O	SDRAM clock output terminal SDRAM
94	VSS	-	GND
95	SDRCLKIN	I	SDRAM clock input terminal
96	VDD3	-	3.3V
97	VDD	-	1.5V
98	M0DT15	I/O	SDRAM data in/output terminal(MSB)
99	M0DT14	I/O	SDRAM data in/output terminal
100	VSS	-	GND
101	M0DT13	I/O	SDRAM data in/output terminal
102	M0DT12	I/O	SDRAM data in/output terminal
103	VDD3	-	3.3V
104	M0DT11	I/O	SDRAM data in/output terminal
105	M0DT10	I/O	SDRAM data in/output terminal
106	VSS	-	GND
107	M0DT9	I/O	SDRAM data in/output terminal

No.	Symbol	I/O	Function
108	M0DT8	I/O	SDRAM data in/output terminal
109	VSS	-	GND
110	VDD3	-	3.3V
111	N.C.	-	Non-Connect
112	M0DT7	I/O	SDRAM data in/output terminal
113	M0DT6	I/O	SDRAM data in/output terminal
114	VSS	-	GND
115	M0DT5	I/O	SDRAM data in/output terminal
116	M0DT4	I/O	SDRAM data in/output terminal
117	VDD3	-	3.3V
118	M0DT3	I/O	SDRAM data in/output terminal
119	M0DT2	I/O	SDRAM data in/output terminal
120	VSS	-	GND
121	M0DT1	I/O	SDRAM data in/output terminal
122	M0DT0	I/O	SDRAM data in/output terminal (LSB)
123	VDD	-	1.5V
124	VDD3	-	3.3V
125	M0BA	O	SDRAM address output terminal(MSB)
126	M0AP	O	SDRAM address output terminal
127	VSS	-	GND
128	M0AD9	O	SDRAM address output terminal
129	M0AD8	O	SDRAM address output terminal
130	VDD3	-	3.3V
131	M0AD7	O	SDRAM address output terminal
132	M0AD6	O	SDRAM address output terminal
133	VSS	-	GND
134	M0AD5	O	SDRAM address output terminal
135	M0AD4	O	SDRAM address output terminal
136	VSS	-	GND
137	VDD3	-	3.3V
138	M0AD3	O	SDRAM address output terminal
139	M0AD2	O	SDRAM address output terminal
140	VSS	-	GND
141	M0AD1	O	SDRAM address output terminal
142	M0AD0	O	SDRAM address output terminal(LSB)
143	VDD	-	1.5V
144	VDD3	-	3.3V
145	CLK27XO	-	clock 27 MHz output terminal(X'tal)
146	CLK27XI	-	clock 27 MHz input terminal(X'tal)
147	VSS	-	GND
148	RST	I	reset input terminal
149	VDD3	-	3.3V
150	R656OUT7	O	Rec.656 output terminal(MSB)
151	R656OUT6	O	Rec.656 output terminal
152	R656OUT5	O	Rec.656 output terminal
153	R656OUT4	O	Rec.656 output terminal
154	N.C.	-	Non-Connect
155	VSS	-	GND
156	VDD3	-	3.3V
157	R656OUT3	O	Rec.656 output terminal
158	R656OUT2	O	Rec.656 output terminal
159	R656OUT1	O	Rec.656 output terminal
160	R656OUT0	O	Rec.656 output terminal(LSB)
161	VSS	-	GND
162	CLK27O	O	clock 27 MHz output terminal
163	VSS	-	GND
164	VDD3	-	3.3V
165	R656IN7	I	Rec.656 input terminal (MSB) (Not used Open or VSS)
166	R656IN6	I	Rec.656 input terminal (Not used Open or VSS)
167	R656IN5	I	Rec.656 input terminal (Not used Open or VSS)
168	R656IN4	I	Rec.656 input terminal (Not used Open or VSS)
169	R656IN3	I	Rec.656 input terminal (Not used Open or VSS)
170	R656IN2	I	Rec.656 input terminal (Not used Open or VSS)
171	R656IN1	I	Rec.656 input terminal (Not used Open or VSS)
172	R656IN0	I	Rec.656 input terminal (LSB) (Not used Open or VSS)
173	VDD	-	1.5V
174	CLK27I	I	Clock 27 MHz input terminal
175	VSS	-	GND
176	CSYNC	I/O	Composite Sync. in/output terminal

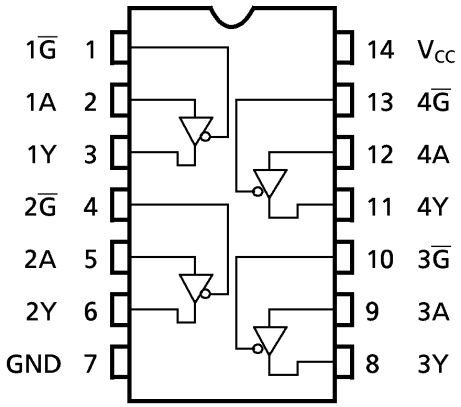
M95128-WMN6T (IC410) DIGITAL P.W.B.



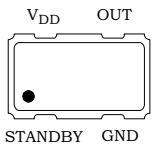
TC74VCX04FT (IC411) D.VIDEO P.W.B.



TC74VHC125FT (IC412,413) DIGITAL P.W.B.

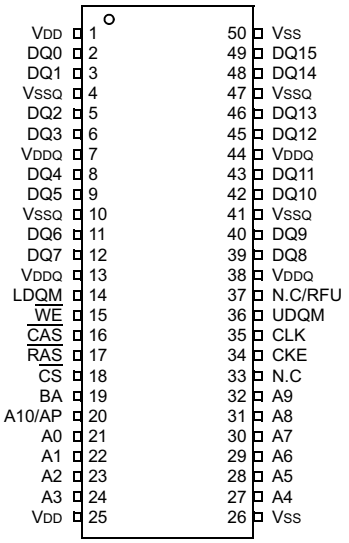


FCXO-03L(27.000MHz) (IC412) D.VIDEO P.W.B.
FCXO-03L(27.5792MHz) (IC420) 1394 P.W.B.



K4S161622H-TC60 (IC413) D.VIDEO P.W.B.

PIN CONFIGURATION (TOP VIEW)

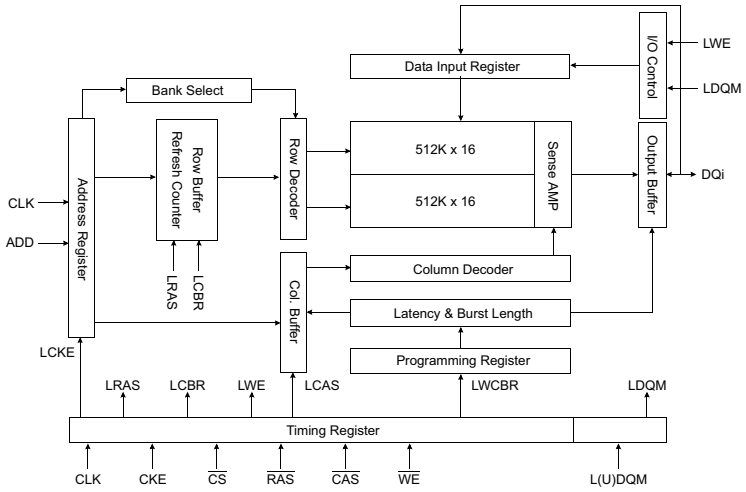


50PIN TSOP (II)
(400mil x 825mil)
(0.8 mm PIN PITCH)

PIN FUNCTION DESCRIPTION

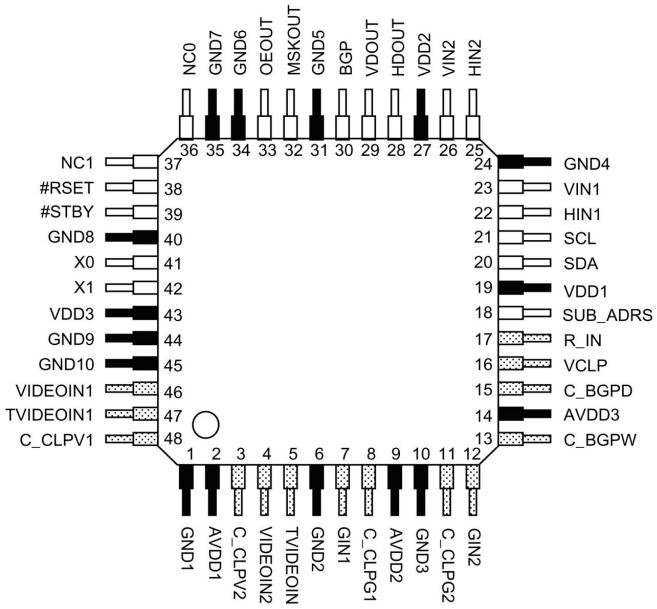
Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{10}/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{10}, column address : CA_0 ~ CA_7
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data Input/Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
$DQ_{0 \sim 15}$	*Data Input/Output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

FUNCTIONAL BLOCK DIAGRAM



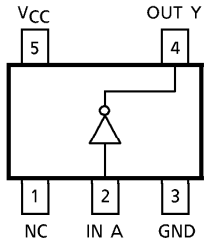
* Samsung Electronics reserves the right to change products or specification without notice.

TE8200PF (IC414) D.VIDEO P.W.B.

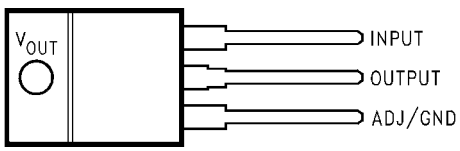


	Analog	
	・ Sync Signal Input	: 4, 5, 7, 12, 46, 47
	・ Voltage References Output	: 16
	・ Clamp Voltage References input	: 3, 8, 11, 48
	・ Resistor Terminal	: 17
	・ Capacitance Terminal	: 13, 15
	VDD, AVDD, GND	
	・ 3.3V Power Supply for Analog	: 2, 9, 14
	・ 3.3V Power Supply for Logic	: 19, 27, 43
	・ Ground	: 1, 6, 10, 24, 31, 34 35, 40, 44, 45
	Logic	
	・ Input Buffer	: 18, 38, 39
	・ Input Buffer 5V Tolerant(schmitt)	: 22, 23, 25, 26
	・ Input Buffer 5V Tolerant	: 21
	・ I/O Buffer (IOL=12mA or Pseudo Open Drain	: 20
	・ OSC Buffer	: 41, 42
	・ Output Buffer (IOL=12mA)	: 28
	・ Output Buffer (IOL=8mA)	: 29, 30, 32, 33
	・ No Connect	: 36, 37

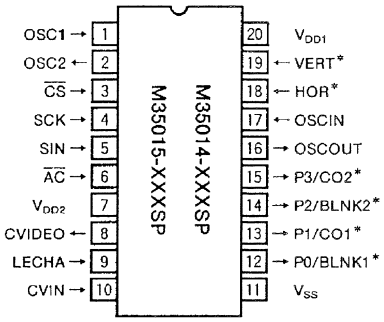
TC7SZU04F (IC423-426,957,958) 1394 P.W.B.



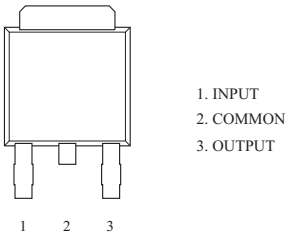
LMS1587CT-ADJ (IC502,503,505,506,508,509) REG2 P.W.B.



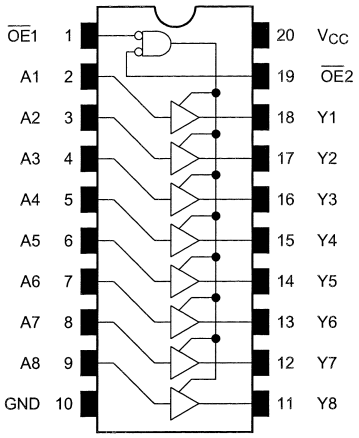
M35014 (IC503)



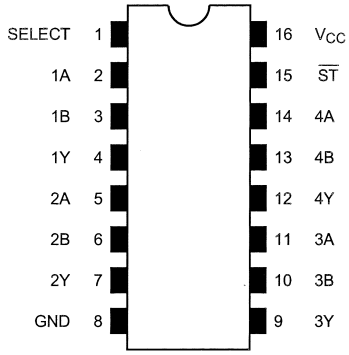
KIA7812AF-RTF (IC101,602)
KIA7812AF-RTF (IC302,504)
KIA7805AF (IC601)



TC74LCX541F (IC614-617) D.VIDEO P.W.B.

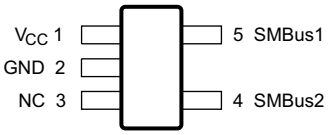


TC74LCX157F (IC704)



LTC1694CS5 (IC902) D.VIDEO P.W.B.

TOP VIEW



V_{CC}(Pin 1): Power Supply Input. V_{CC} can range from 2.7V to 6V and requires a 0.1μF bypass capacitor to GND. Supply current is typically 45μA when the SMBus or I^2C lines are inactive (SCL and SDA are a logic high level).

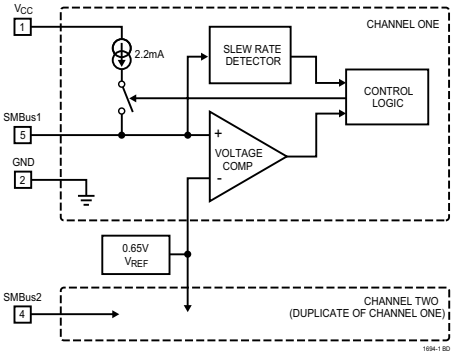
GND (Pin 2):Ground.

NC (Pin 3):No Connection.

SMBus2 (Pin 4):Active Pull-Up for SMBus.

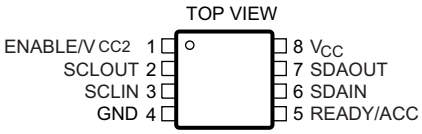
SMBus1 (Pin 5):Active Pull-Up for SMBus.

BLOCK DIAGRAM

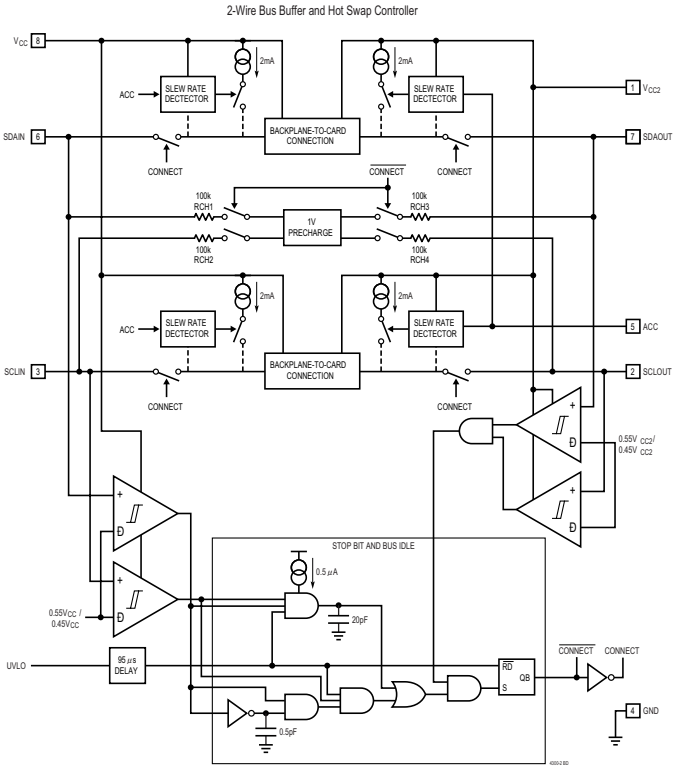


LTC4300-2CMS8 (IC903) D.VIDEO P.W.B.

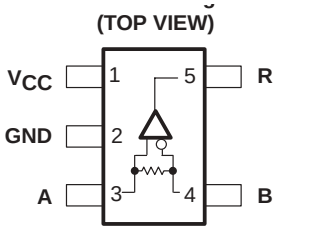
TOP VIEW



BLOCK DIAGRAM



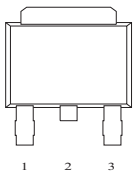
SN65LVDS2DBVR (IC909) D.VIDEO P.W.B.



110-Ω Resistor for LVDT Only

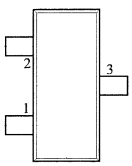
2. TR's

KTC2025D-RTF (TR422) DIGITAL P.W.B.



1. BASE
2. COLLECTOR
3. EMITTER

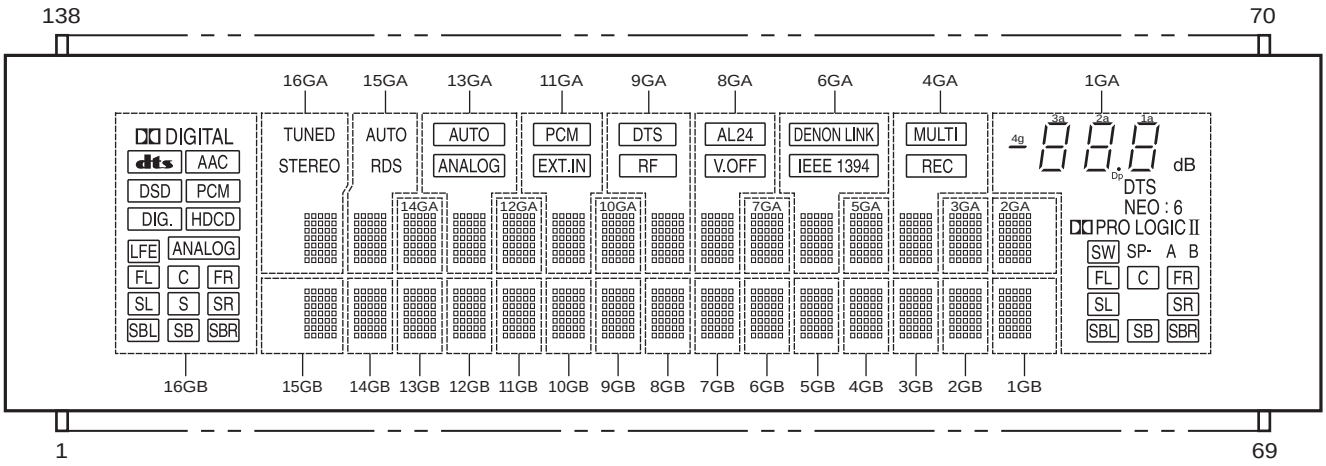
KTC3911S-RTK (TR111,211,311,411,511) AMP(L) P.W.B.
(TR112,212,312,412,512) AMP(R) P.D.F.
(TR513,515-518,520,521) AD P.W.B.

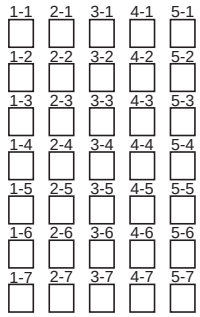


1. EMITTER
2. BASE
3. COLLECTOR

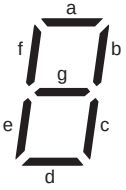
3. FL DISPLAY

FLD(32-BT-10GN) (VI:FL701)





[15GB ~ 1GB, 16GA ~ 2GA]



[1GA]

Pin connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
Connection	F1	F1	F1	F1	NP	NP	NC	P38B	P37B	P36B	P35B	P34B	P33B	P32B	P31B	P30B	P29B	P28B	P27B	P26B	P25B	P24B	P23B	P22B	P21B	P20B	P19B	P18B	P17B	P16B	P15B	P14B	P13B	P12B	P11B	P10B	P9B	P8B	P7B	P6B	P5B	P4B	P3B	P2B	P1B	NC	IC	1GB	2GB	3GB

Pin No.	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
Connection	4GB	5GB	6GB	7GB	8GB	9GB	10GB	11GB	12GB	13GB	14GB	15GB	16GB	NP	NP	F2	F2	F2	F2	F2	F2	F2	F2	NP	NP	IC	P37A	P33A	P35A	P34A	P33A	P32A	P31A	P30A	P29A	P28A	P27A	P26A	P25A	P24A	P23A	P22A	P21A	P20A	P19A	P18A	P17A	P15A

Pin No.	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138
Connection	P14A	P13A	P12A	P11A	P10A	P9A	P8A	P7A	P6A	P5A	P4A	P3A	P2A	P1A	NC	NC	1GA	2GA	3GA	4GA	5GA	6GA	7GA	8GA	9GA	10GA	11GA	12GA	13GA	14GA	15GA	16GA	NP	NP	F1	F1	F1	F1

NOTE 1) F1,F2 : Filament
2) NP : No pin
3) NC : No connection
(NC pin should be electrically open on the PC board)
4) DL : Datum Line
5) 1GA~16GA, 1GB~16GB : Grid
6) IC : Internal connection
(IC pin should be electrically open on the PC board)

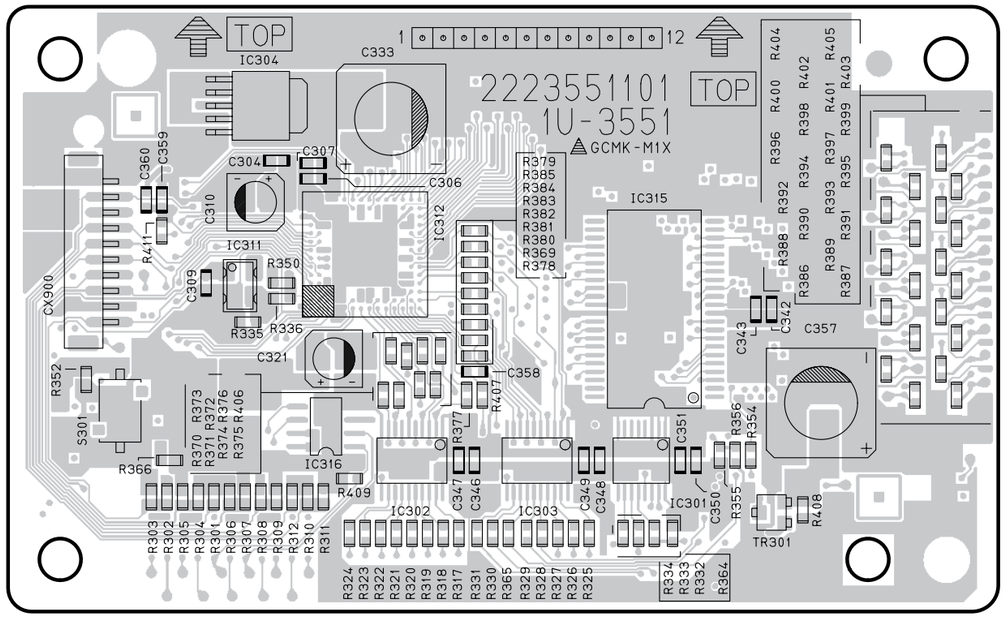
ANODE CONNECTION

	16GA	15GA	14GA	13GA	12GA	11GA	10GA	9GA	8GA	7GA	6GA	5GA	4GA	3GA	2GA	1GA
P1A	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	4g
P2A	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	3a
P3A	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3b
P4A	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	3f
P5A	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	3g
P6A	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	3c
P7A	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	3e
P8A	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3d
P9A	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	2a
P10A	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	2b
P11A	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	2f
P12A	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2g
P13A	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	2c
P14A	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	2e
P15A	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	2d
P16A	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1a
P17A	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	1b
P18A	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	1f
P19A	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	1g
P20A	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	1c
P21A	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1e
P22A	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	1d
P23A	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	Dp
P24A	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	dB
P25A	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	DTS NEO : 6
P26A	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	□□PRO LOGIC II
P27A	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	SW
P28A	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	SP-
P29A	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	A
P30A	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	B
P31A	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	FL
P32A	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	C
P33A	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	FR
P34A	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	SL
P35A	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	SR
P36A	TUNED	AUTO	–	AUTO	–	PCM	–	DTS	AL24	–	DENON LINK	–	MULTI	–	–	SBL
P37A	STEREO	RDS	–	ANALOG	–	EXT.IN	–	RF	V.OFF	–	IEEE 1394	–	REC	–	–	SB
P38A	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SBR

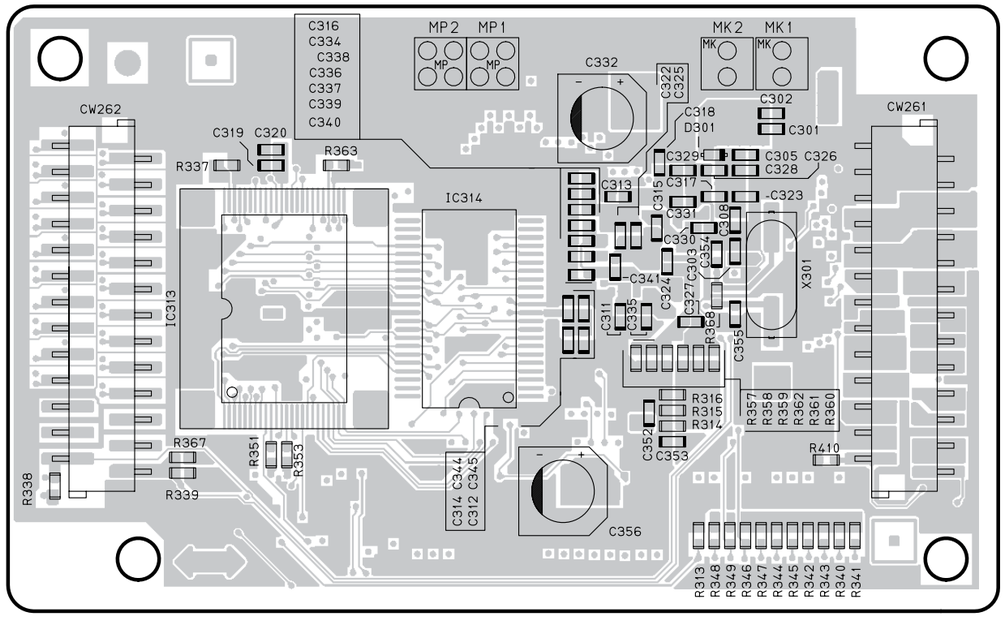
	16GB	15GB	14GB	13GB	12GB	11GB	10GB	9GB	8GB	7GB	6GB	5GB	4GB	3GB	2GB	1GB
P1B	□□ DIGITAL	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1	1-1
P2B	dts	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1	2-1
P3B	AAC	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1	3-1
P4B	DSD	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1	4-1
P5B	PCM	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1	5-1
P6B	DIG.	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2
P7B	HDCD	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2	2-2
P8B	ANALOG	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2	3-2
P9B	LFE	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2	4-2
P10B	FL	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2	5-2
P11B	C	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3	1-3
P12B	FR	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3	2-3
P13B	SL	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3	3-3
P14B	S	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3	4-3
P15B	SR	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3	5-3
P16B	–	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4	1-4
P17B	–	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4	2-4
P18B	–	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4	3-4
P19B	–	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4	4-4
P20B	–	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4	5-4
P21B	–	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5	1-5
P22B	–	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5	2-5
P23B	–	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5	3-5
P24B	–	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5	4-5
P25B	–	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5	5-5
P26B	–	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6	1-6
P27B	–	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6	2-6
P28B	–	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6	3-6
P29B	–	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6
P30B	–	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6
P31B	–	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7	1-7
P32B	–	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7	2-7
P33B	–	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7	3-7
P34B	–	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7	4-7
P35B	–	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7	5-7
P36B	SBL	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
P37B	SB	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
P38B	SBR	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

PRINTED WIRING BOARDS

1U-3551 DSP ADI EX P.W.B. UNIT

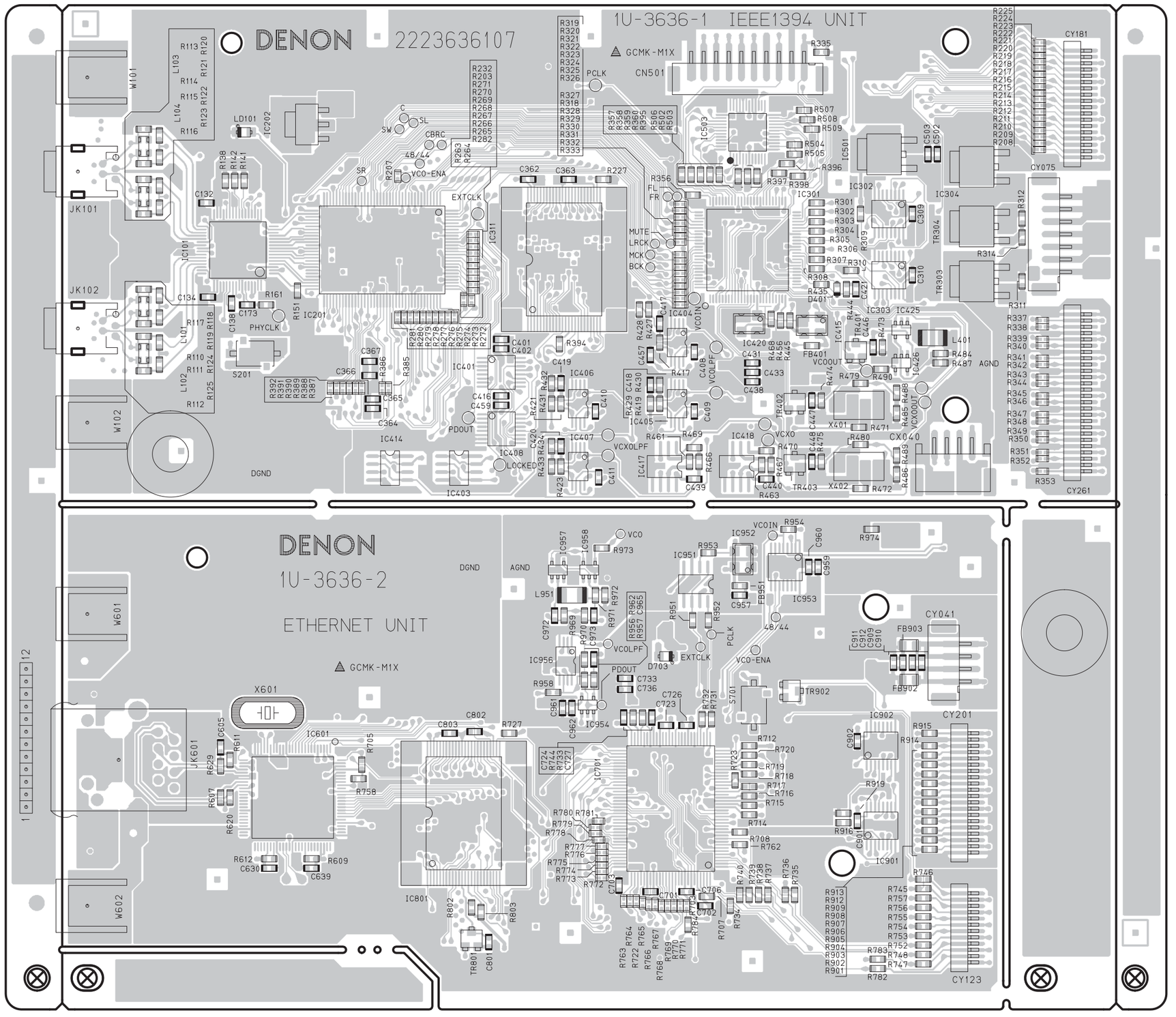


COMPONENT SIDE

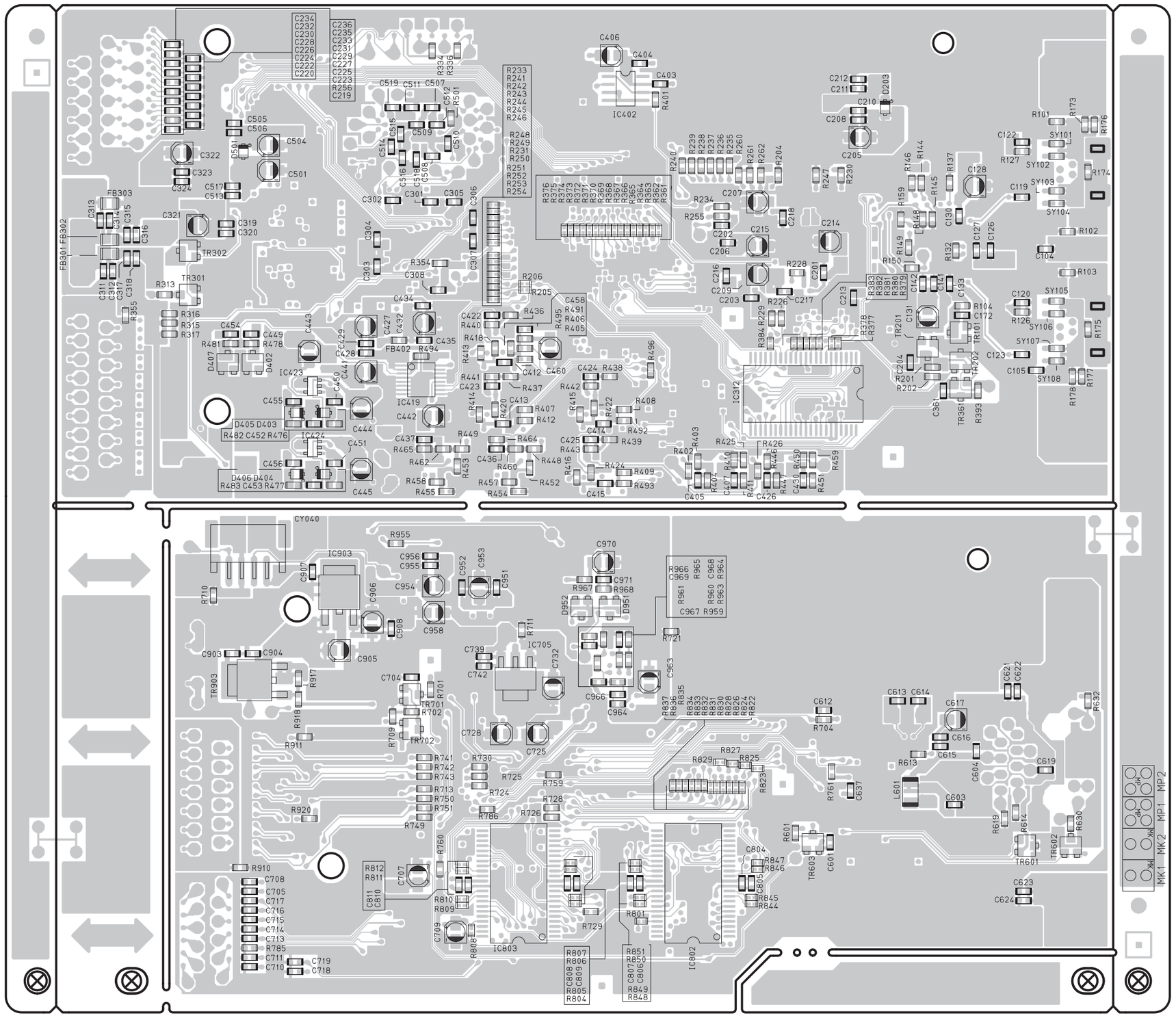


FOIL SIDE

1U-3636 1394 P.W.B. UNIT

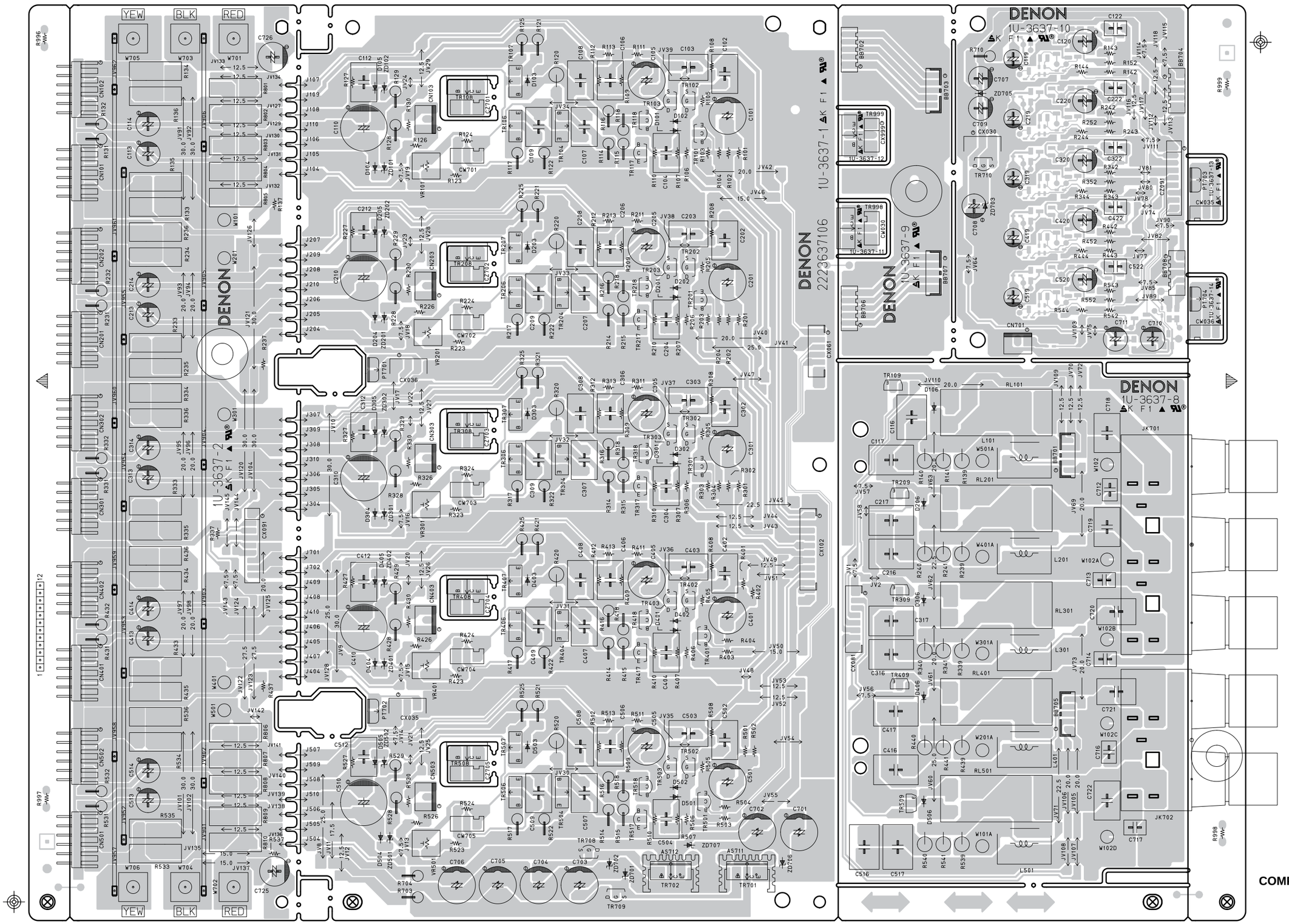


COMPONENT SIDE

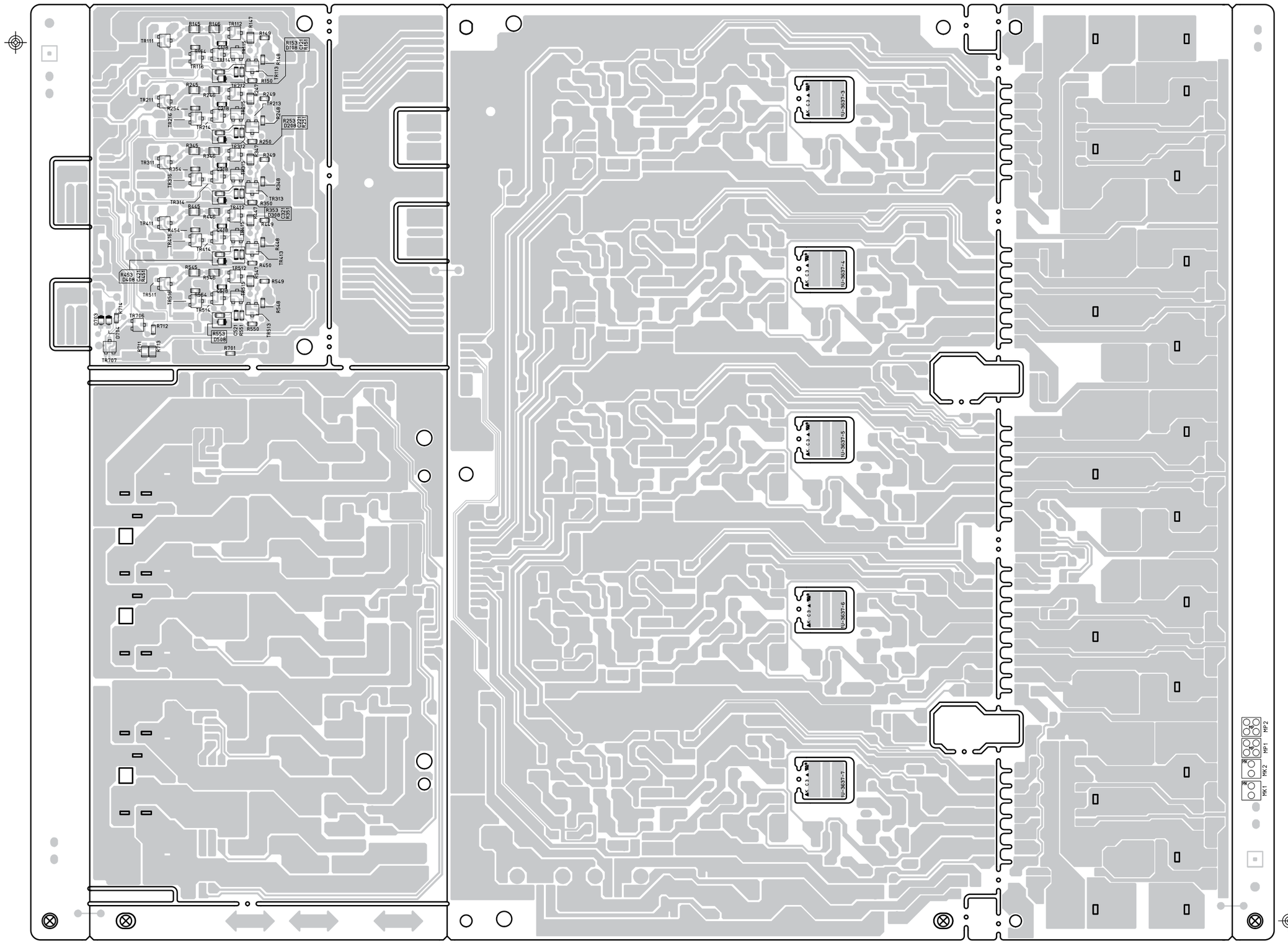


□ FOIL SIDE

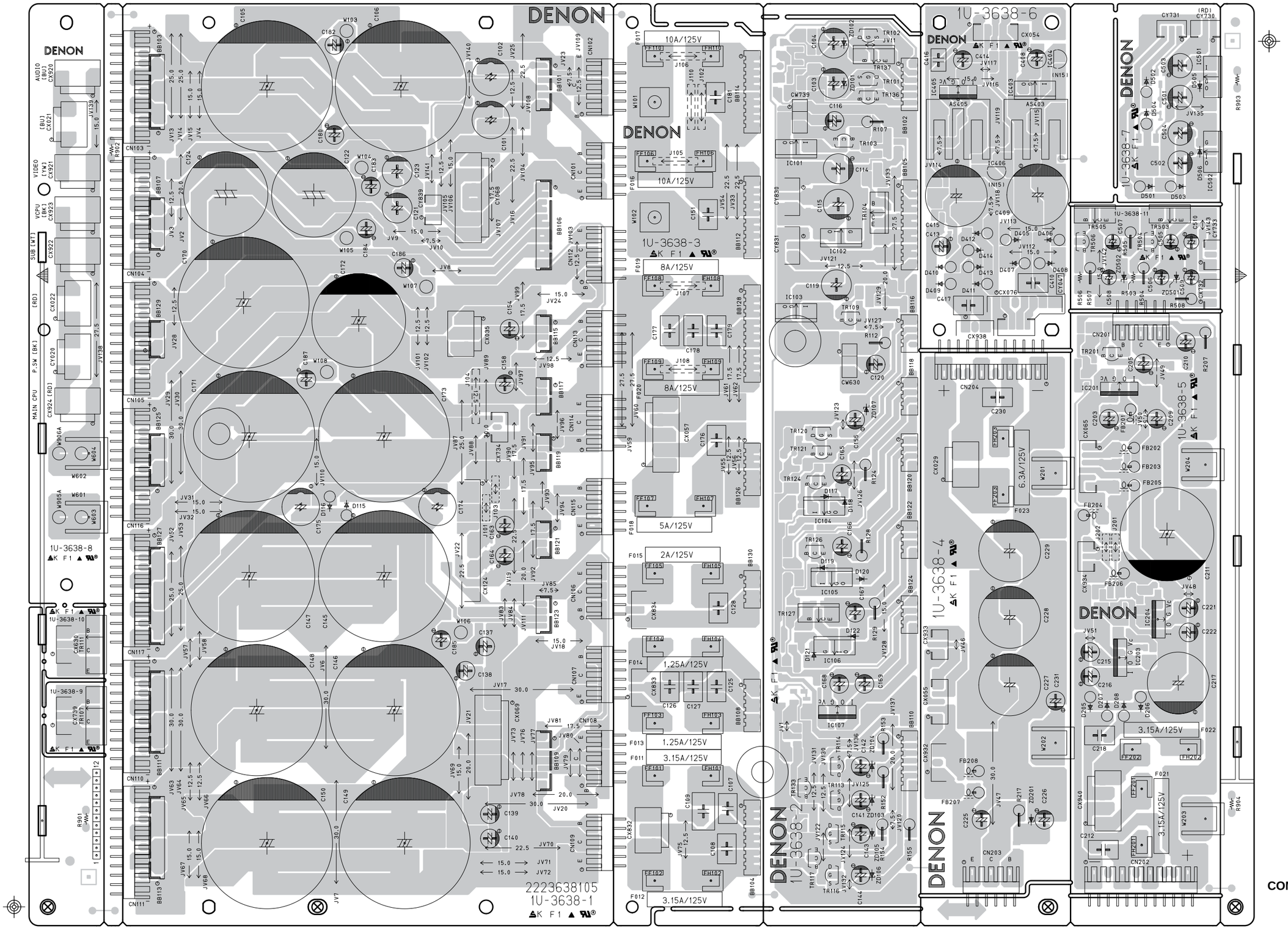
1U-3637 AMP P.W.B. UNIT



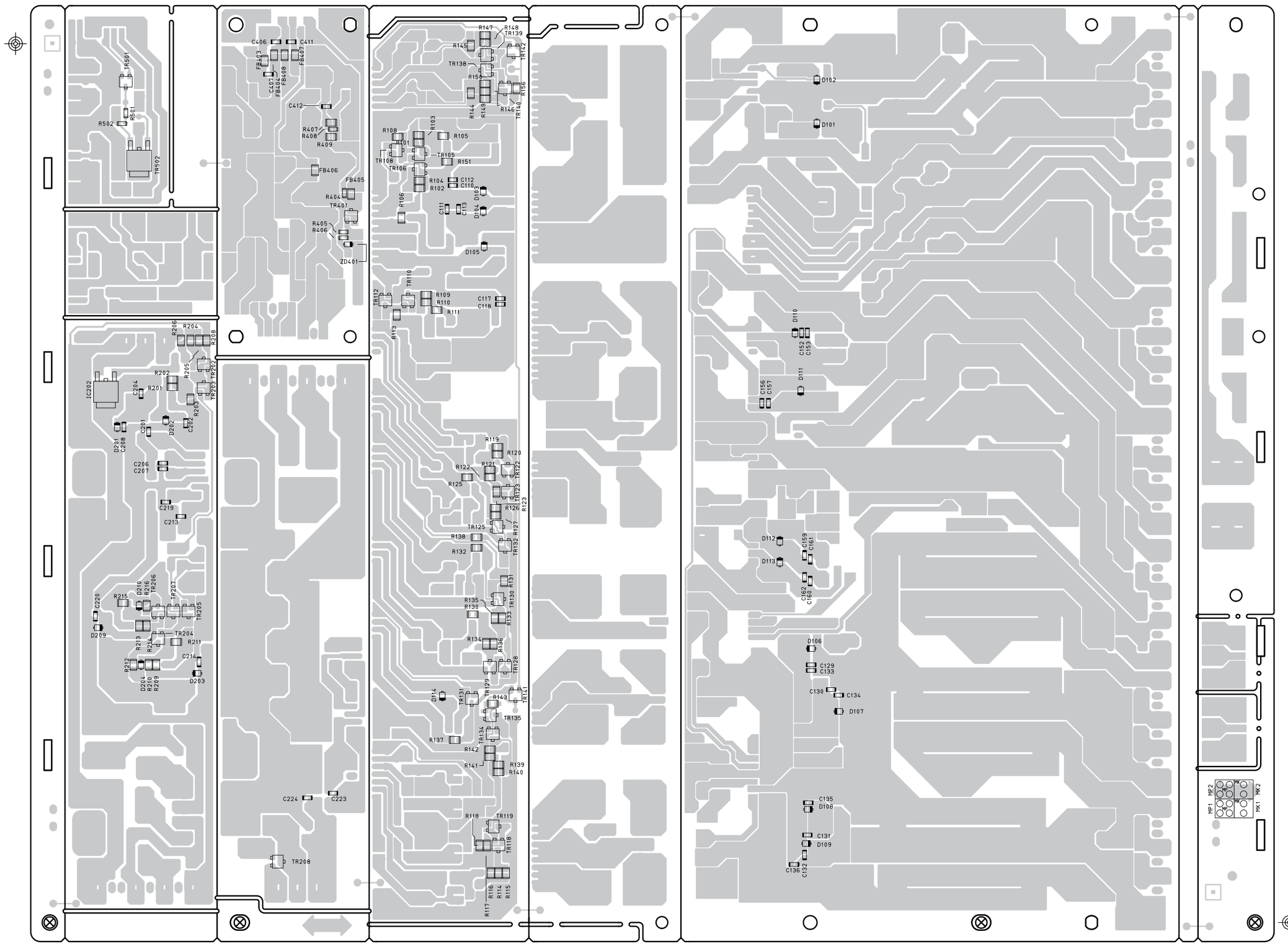
COMPONENT SIDE


R145
R146
TR112
R147
TR111
R149
C115
TR115
R154
TR114
R153
D107
C124
R151
TR116
R150
R148
R113
R245
TR212
R247
R246
R249
TR211
C218
TR215
R213
R254
R248
TR216
R253
D208
C221
R251
TR214
R250
R345
TR312
R347
R346
R349
TR311
C318
TR315
R354
R348
TR316
TR313
TR314
R445
TR412
R447
R358
R353
D308
C321
R355
R446
R449
TR411
C418
TR415
R454
R448
TR416
TR413
TR414
R450
R545
TR512
R547
R546
R549
TR511
C518
TR515
R564
R548
TR516
TR513
TR514
R453
D408
C421
R451
R553
D508
C521
R551
R550
R701
D703
R714
TR706
D704
R712
R711
R719
TR707
IW-3637-3
IW-3637-4
IW-3637-5
IW-3637-6
IW-3637-7
MP2
MP1
MK2
MK1
FOIL SIDE

1U-3638 REG P.W.B. UNIT

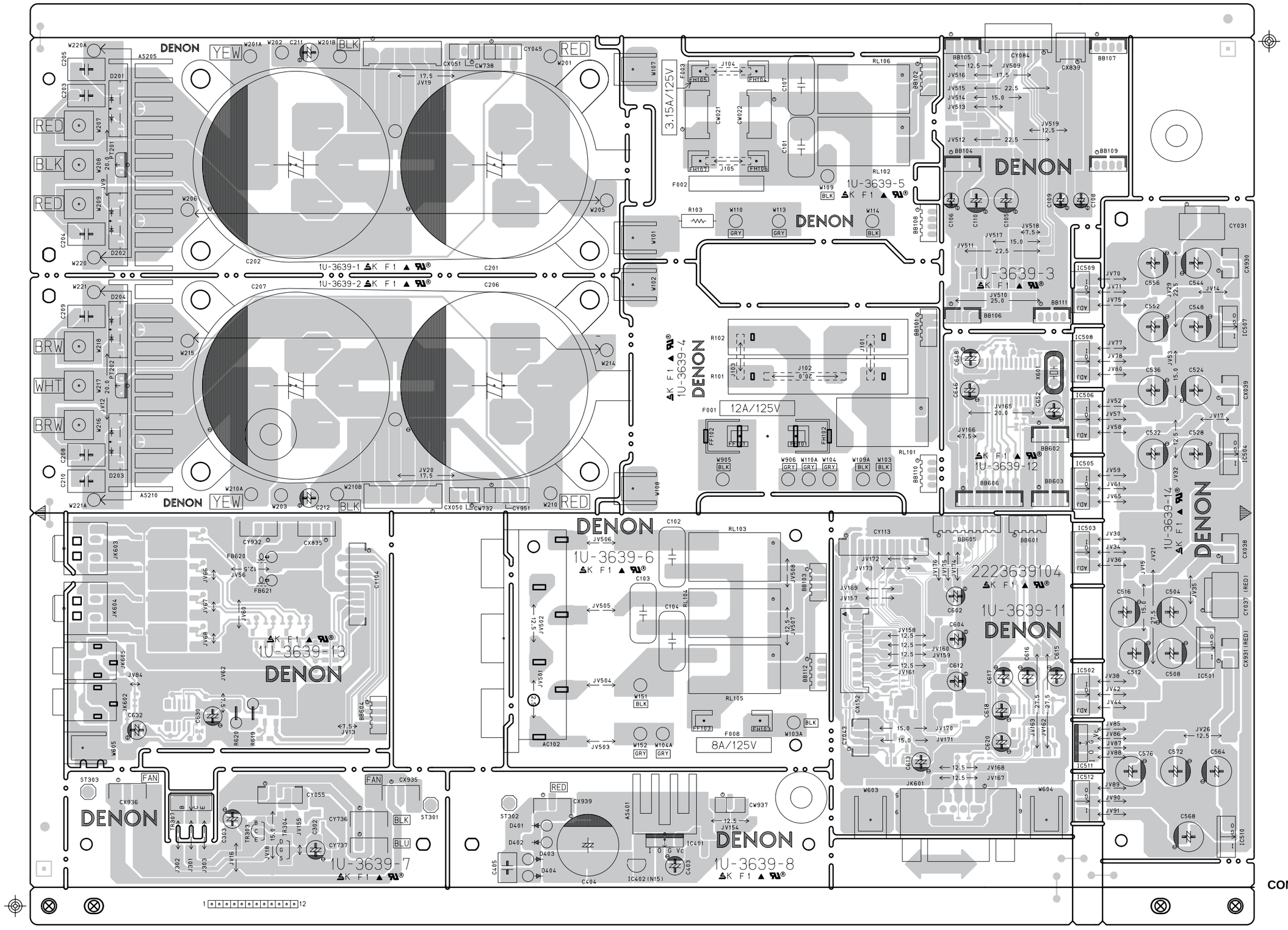


COMPONENT SIDE

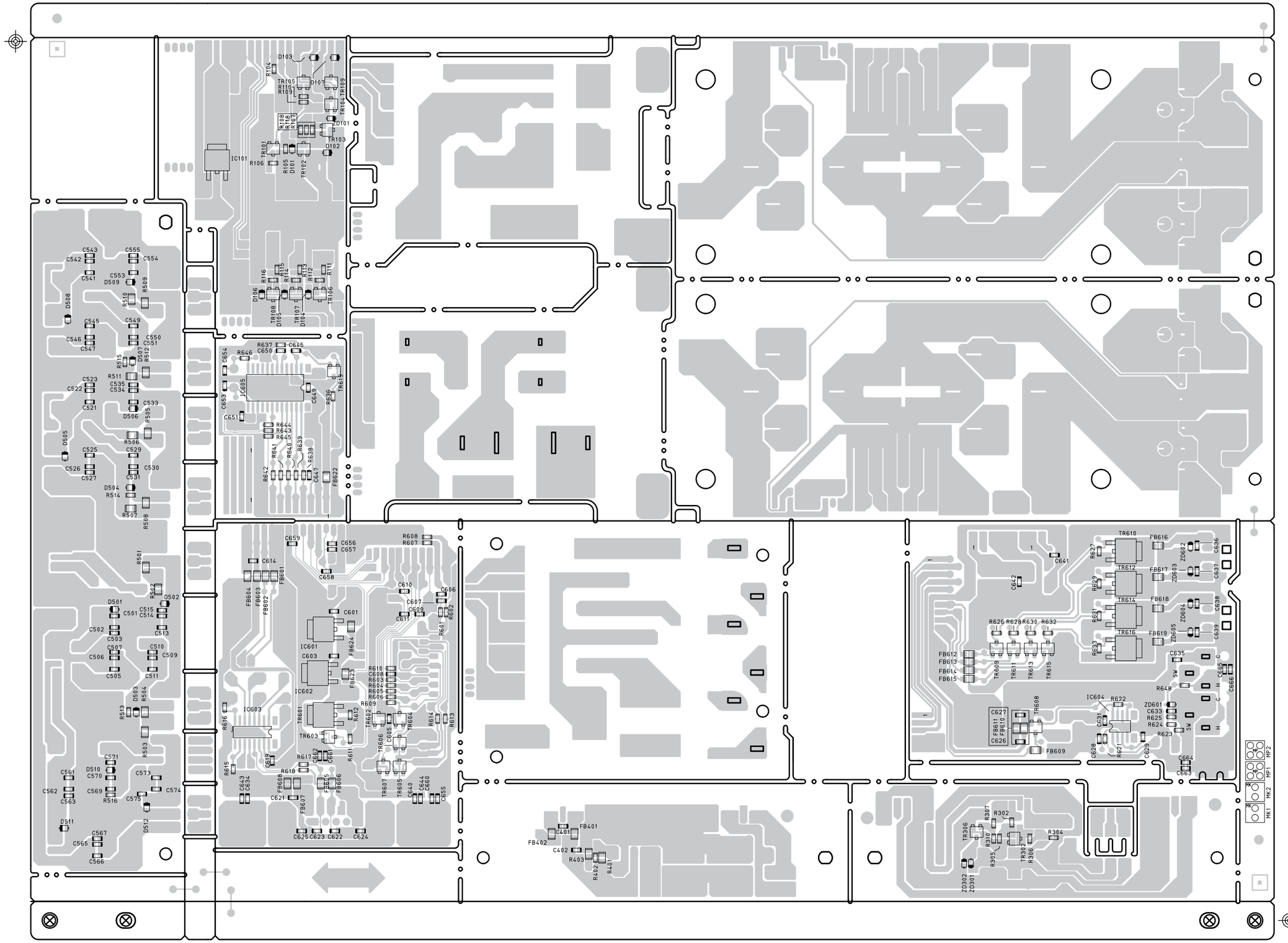

T4501
R501
R502
TR502
C406
C411
FB403
FB407
FB408
C407
FB404
C412
R407
R408
R409
FB406
FB405
R404
TR401
R405
R406
ZD401
R147
R148
TR139
R145
TR142
TR138
R150
R156
R144
R149
R146
TR140
R108
R103
R101
R105
TR105
TR108
R151
TR106
R104
C112
R102
C110
D103
R106
C111
C113
D104
D105
TR110
TR112
R109
C117
R110
C118
R111
R113
R206
R204
R208
R202
R205
TR202
TR203
IC202
C204
R201
R203
C201
D202
C202
D201
C208
C206
C207
C219
C213
C220
R215
D210
R216
TR206
TR207
TR205
D209
TR204
R213
R214
R211
C214
R212
D203
D204
R210
R209
C224
C223
TR208
R119
R120
R122
R121
TR121
TR122
R125
TR123
R123
R126
R127
TR125
TR132
R138
R132
R131
R130
R135
R139
R133
TR133
TR130
R134
R136
TR128
D114
TR131
R129
R143
TR141
TR135
R137
TR134
R142
R141
R139
R140
R118
TR119
TR118
R116
R114
R115
R117
D102
D101
D110
C152
C155
C156
C157
D111
D112
C159
C161
D113
C162
C160
D106
C129
C133
C130
C134
D107
C135
D108
C131
D109
C136
C132
MP2
MK
MK
MP1
MK2
MK1

FOIL SIDE

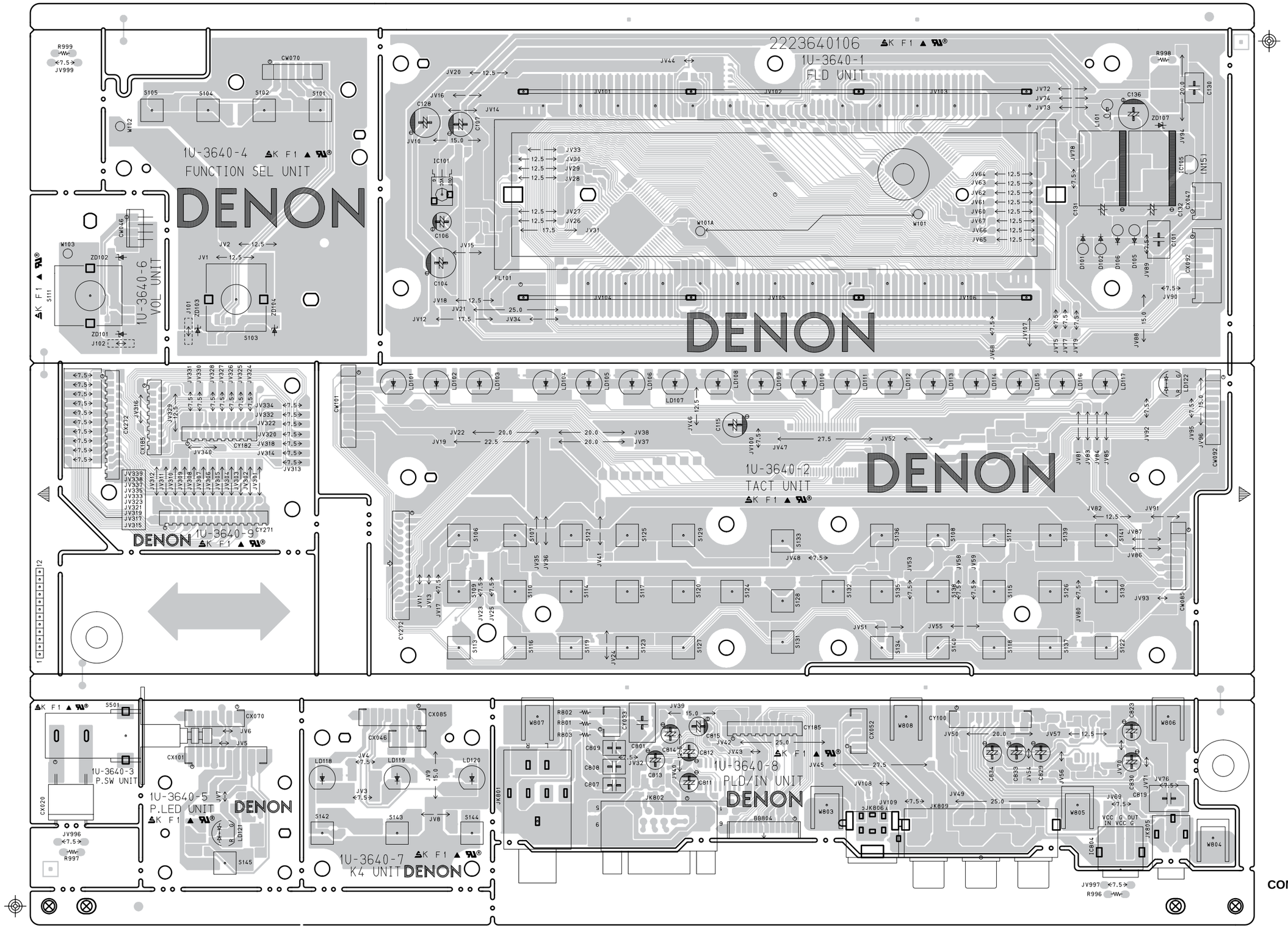
1U-3639 REG2 P.W.B. UNIT



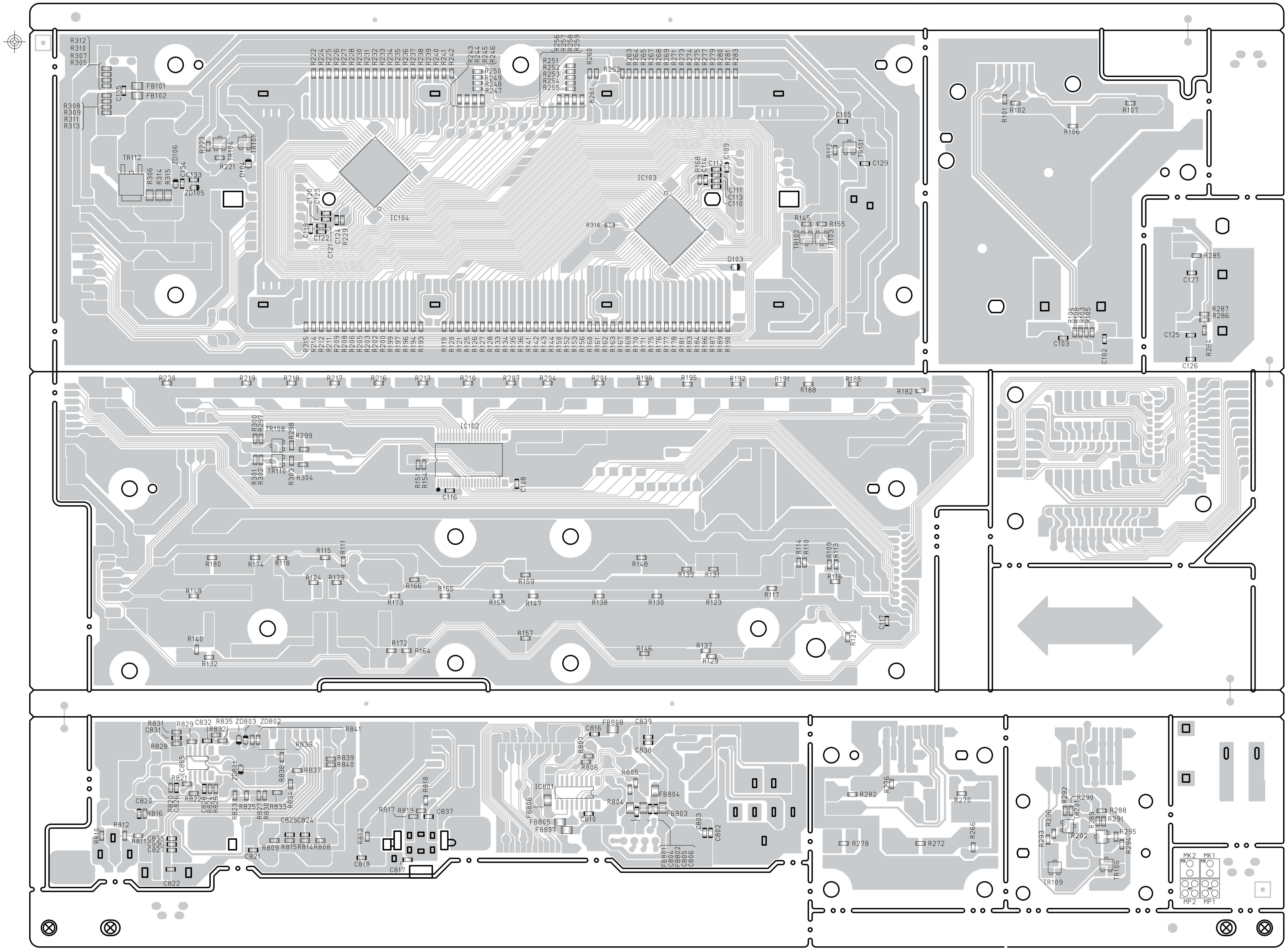
COMPONENT SIDE


FOIL SIDE

1U-3640 FRONT P.W.B. UNIT

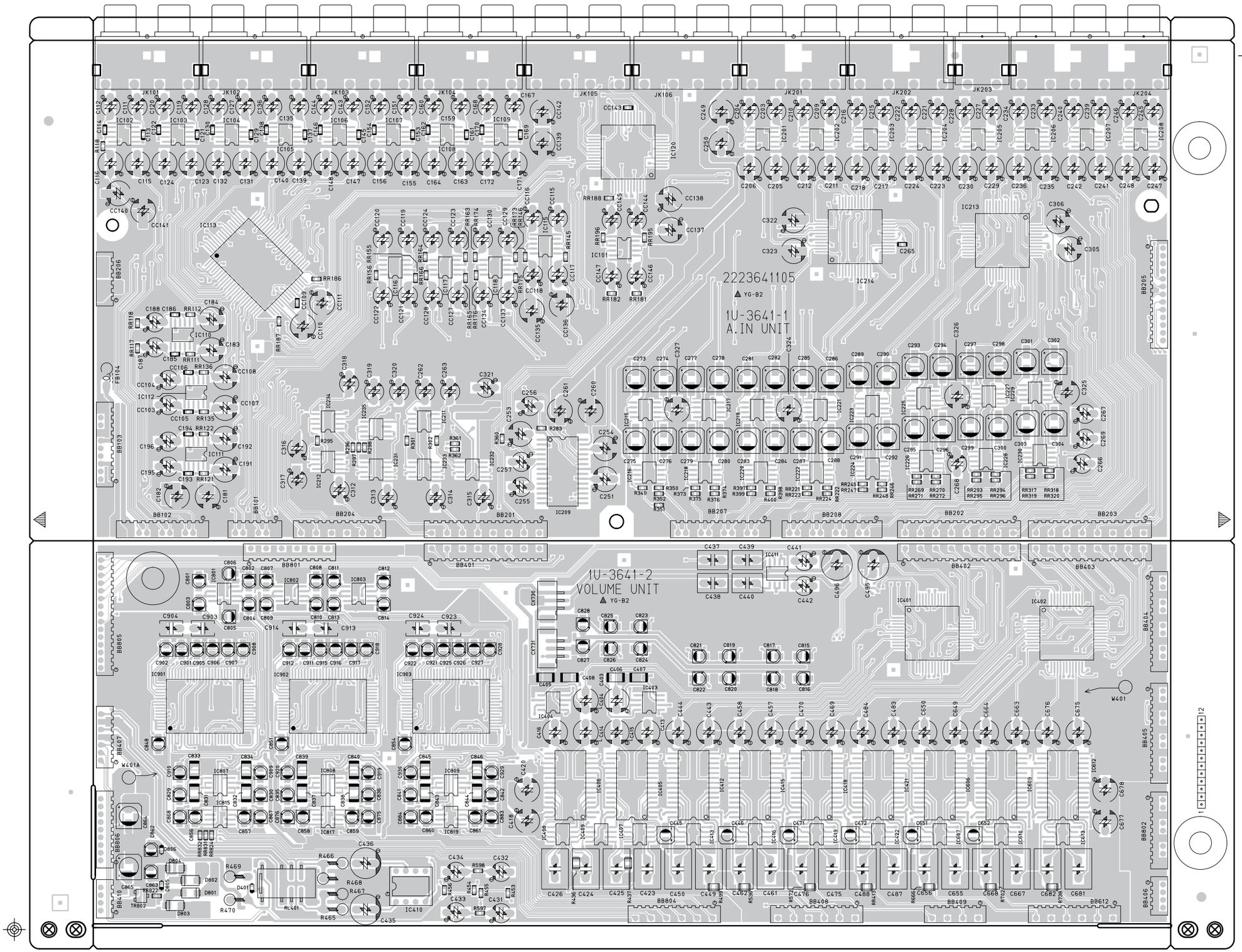


COMPONENT SIDE

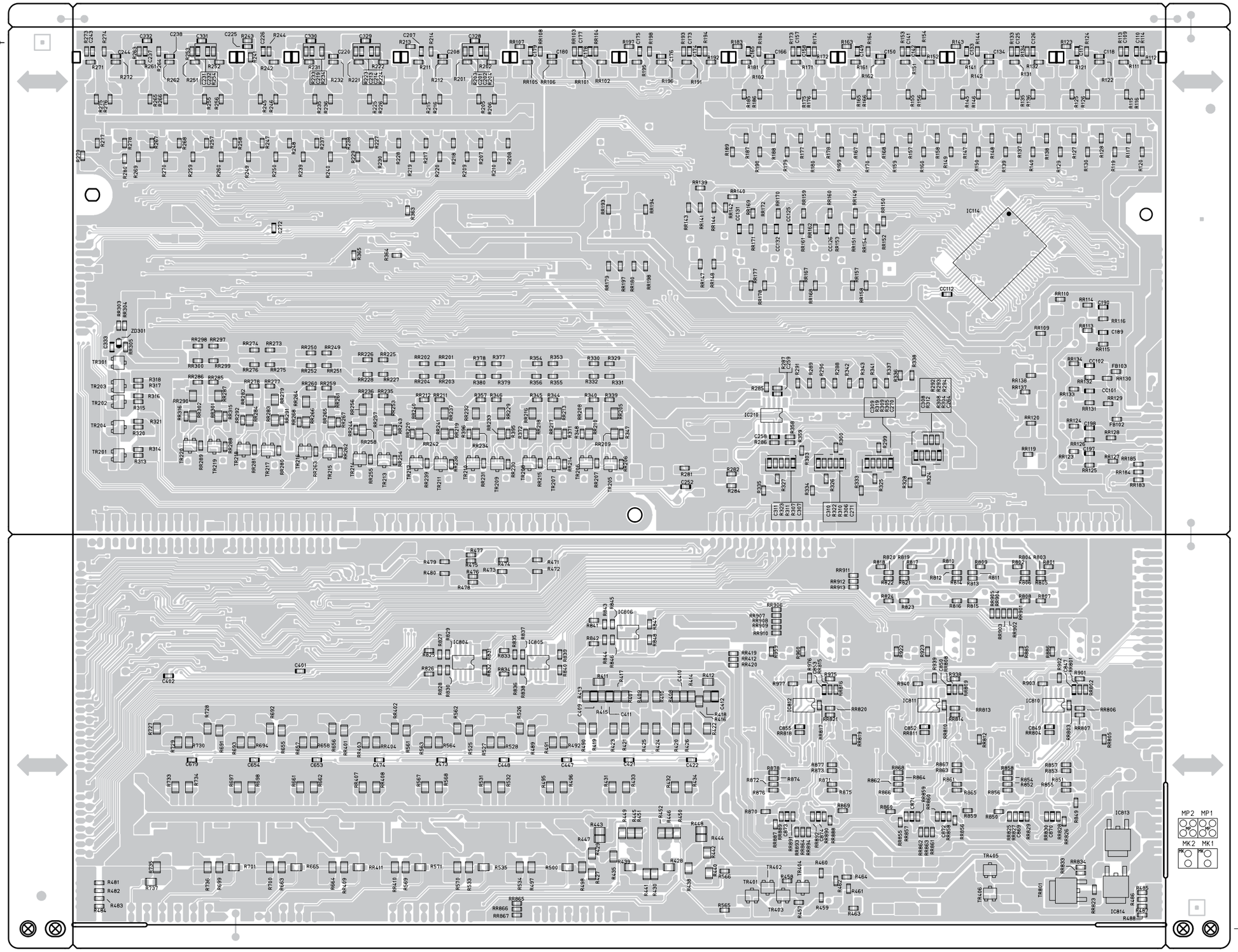


FOIL SIDE

1U-3641 AUDIO P.W.B. UNIT

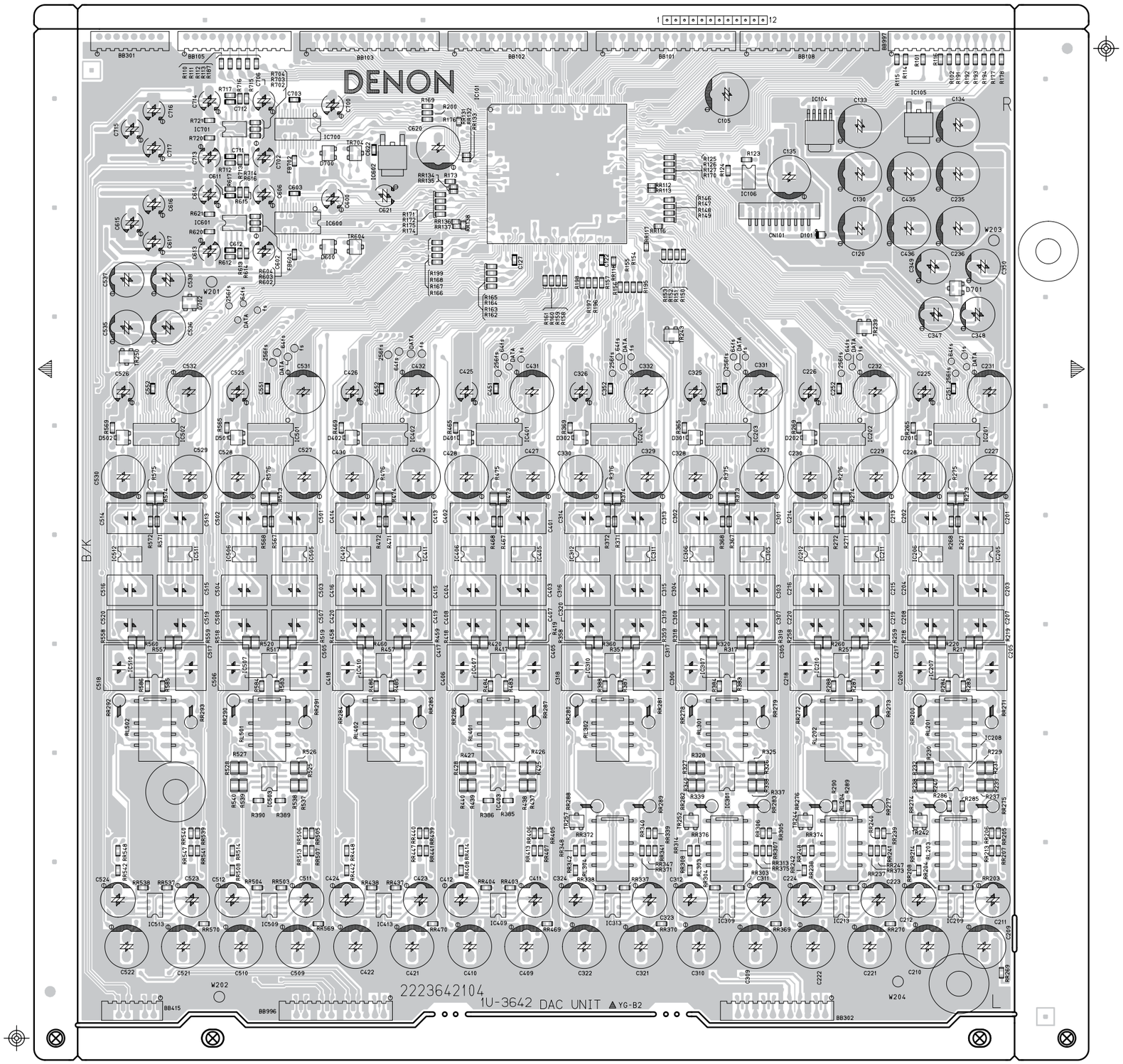


COMPONENT SIDE

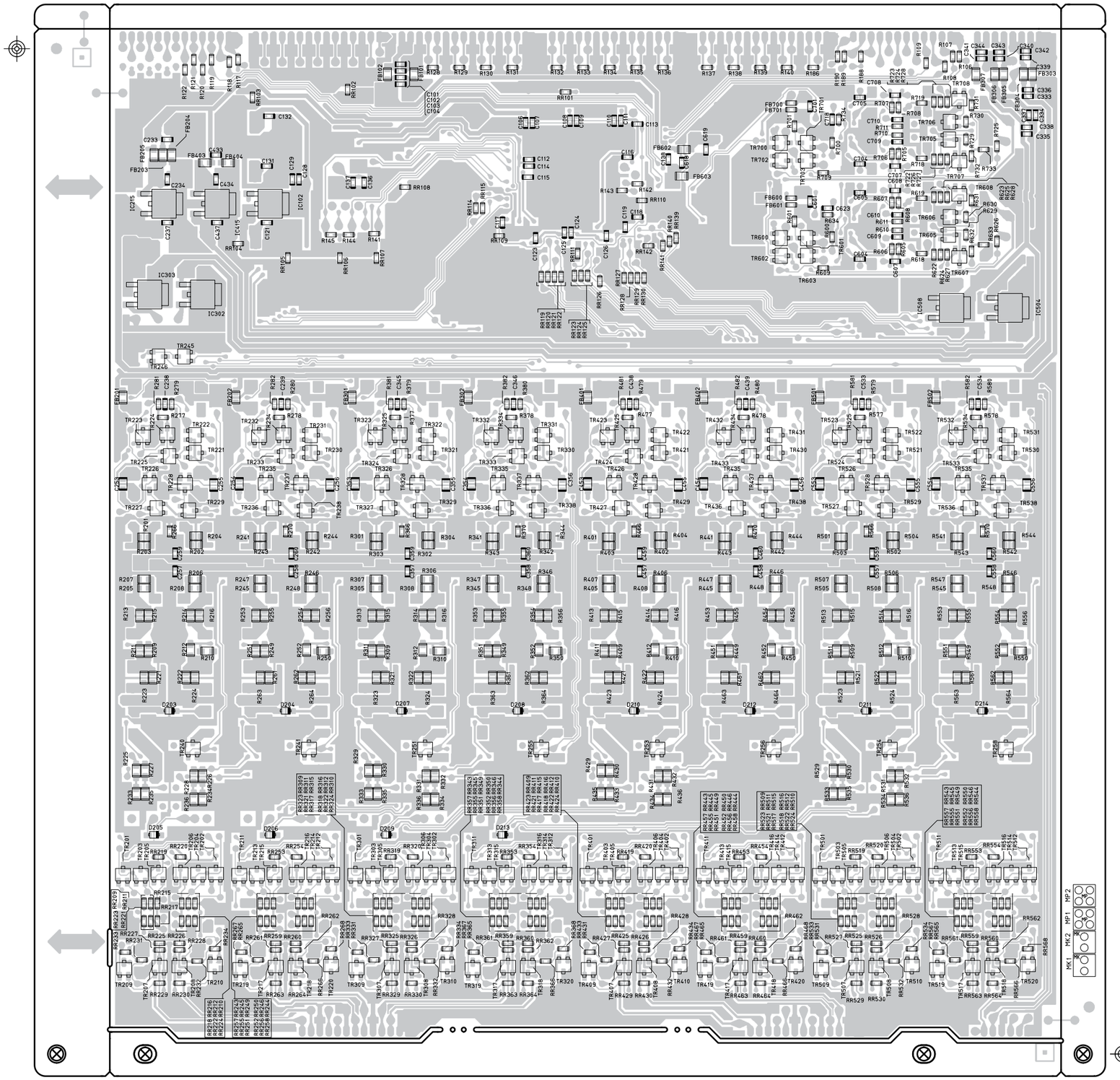


FOIL SIDE

1U-3642 DAC P.W.B. UNIT

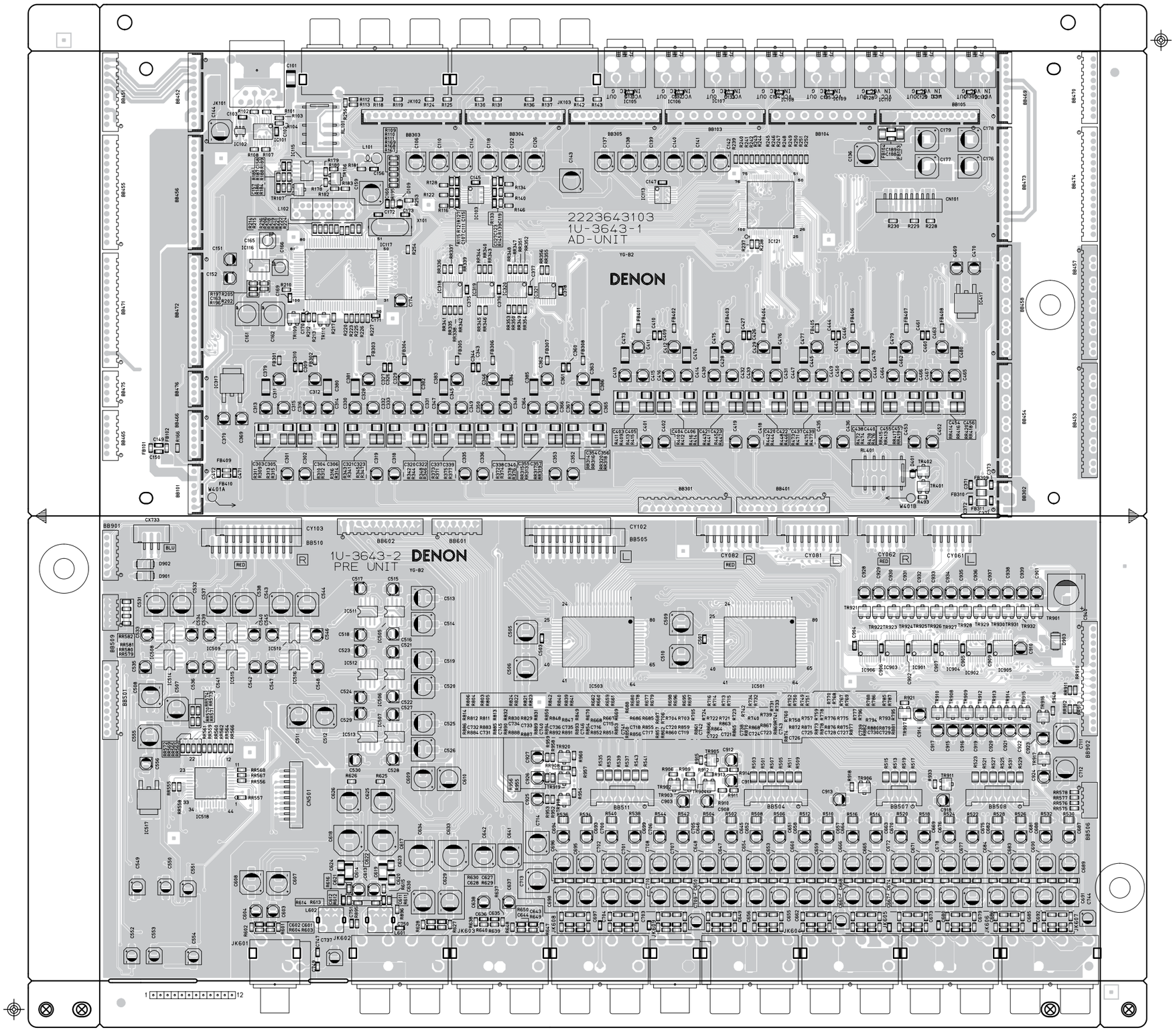


COMPONENT SIDE

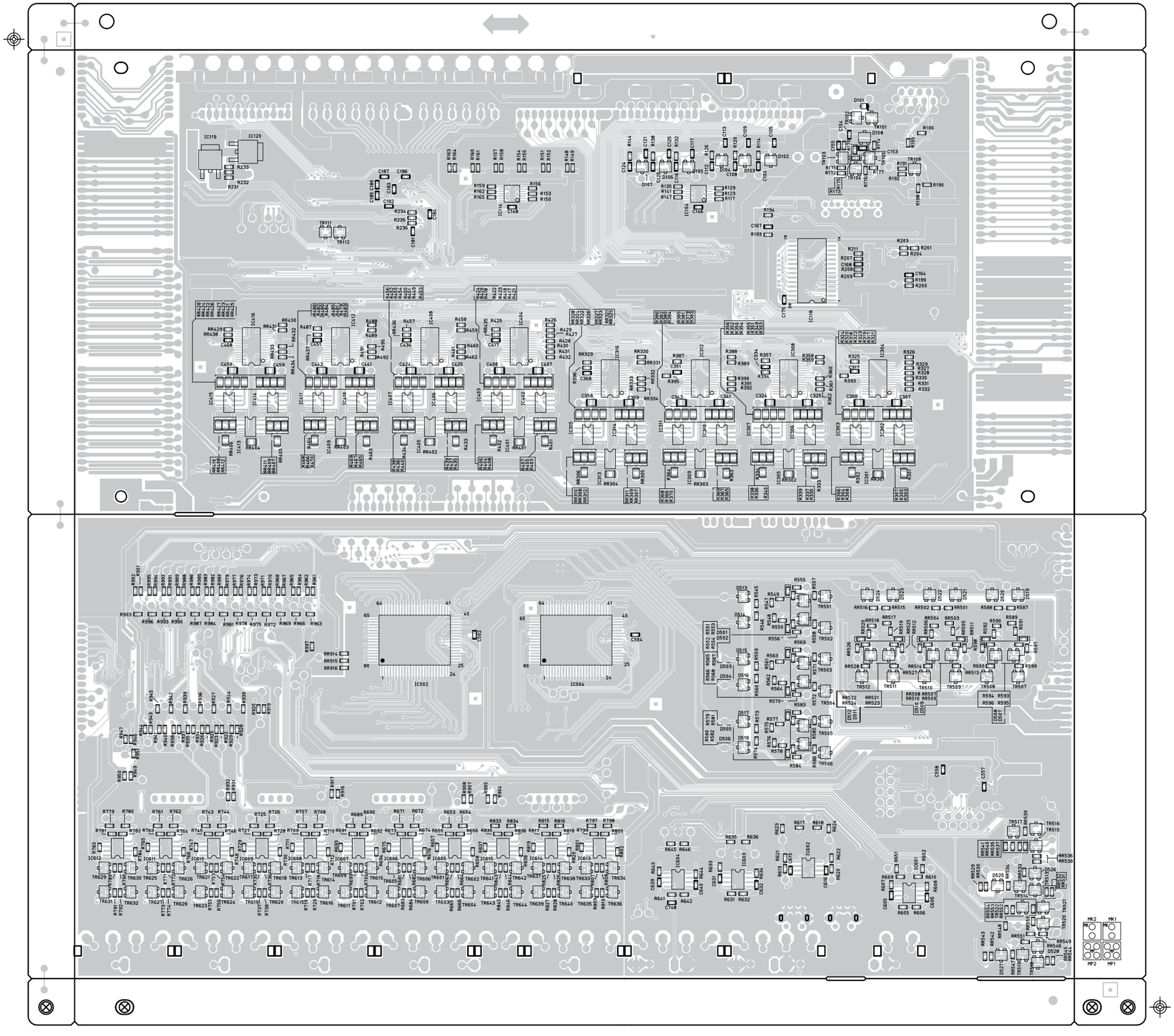


FOIL SIDE

1U-3643 AD P.W.B. UNIT

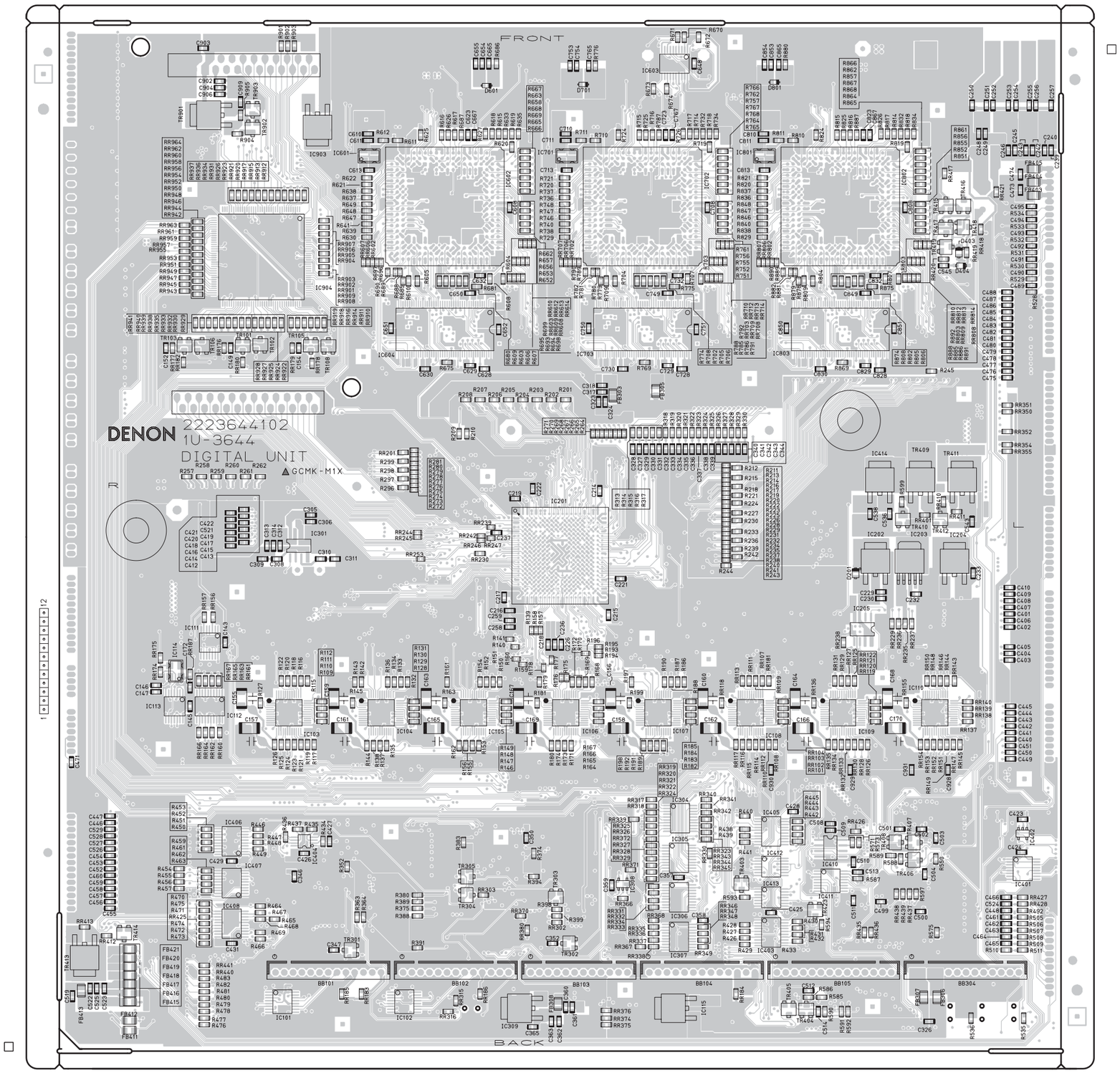


COMPONENT SIDE

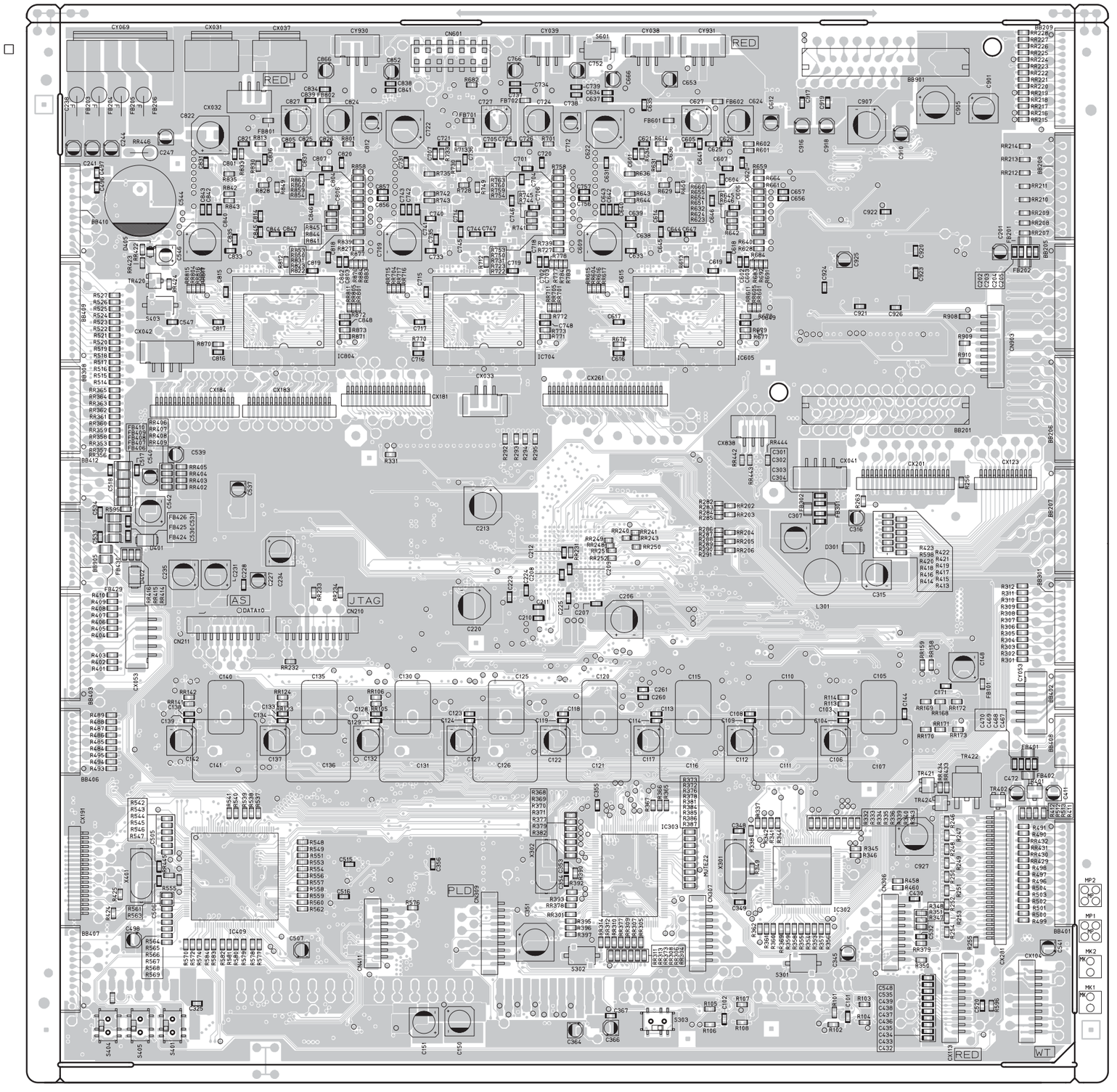


FOIL SIDE

1U-3644 DIGITAL P.W.B. UNIT

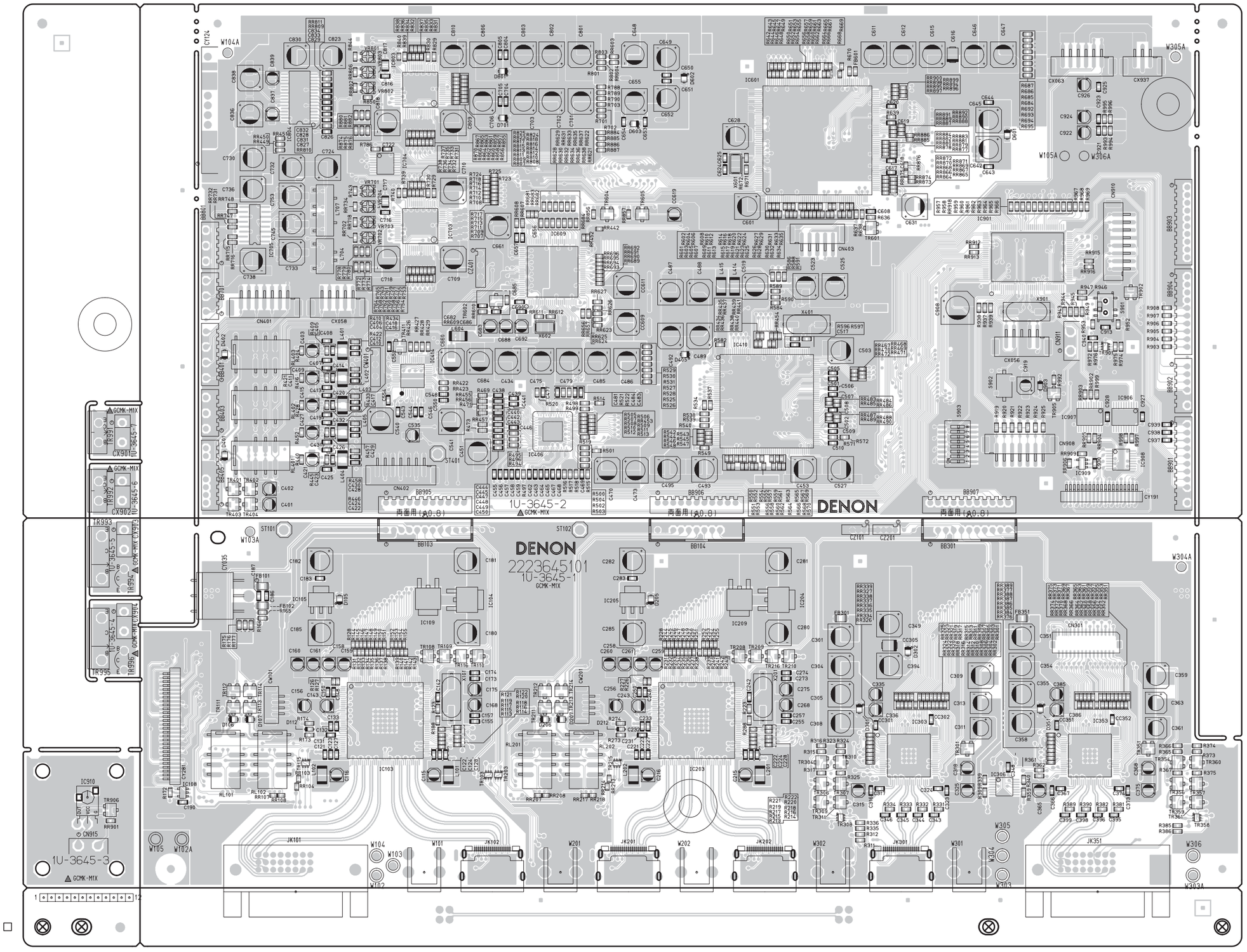


COMPONENT SIDE

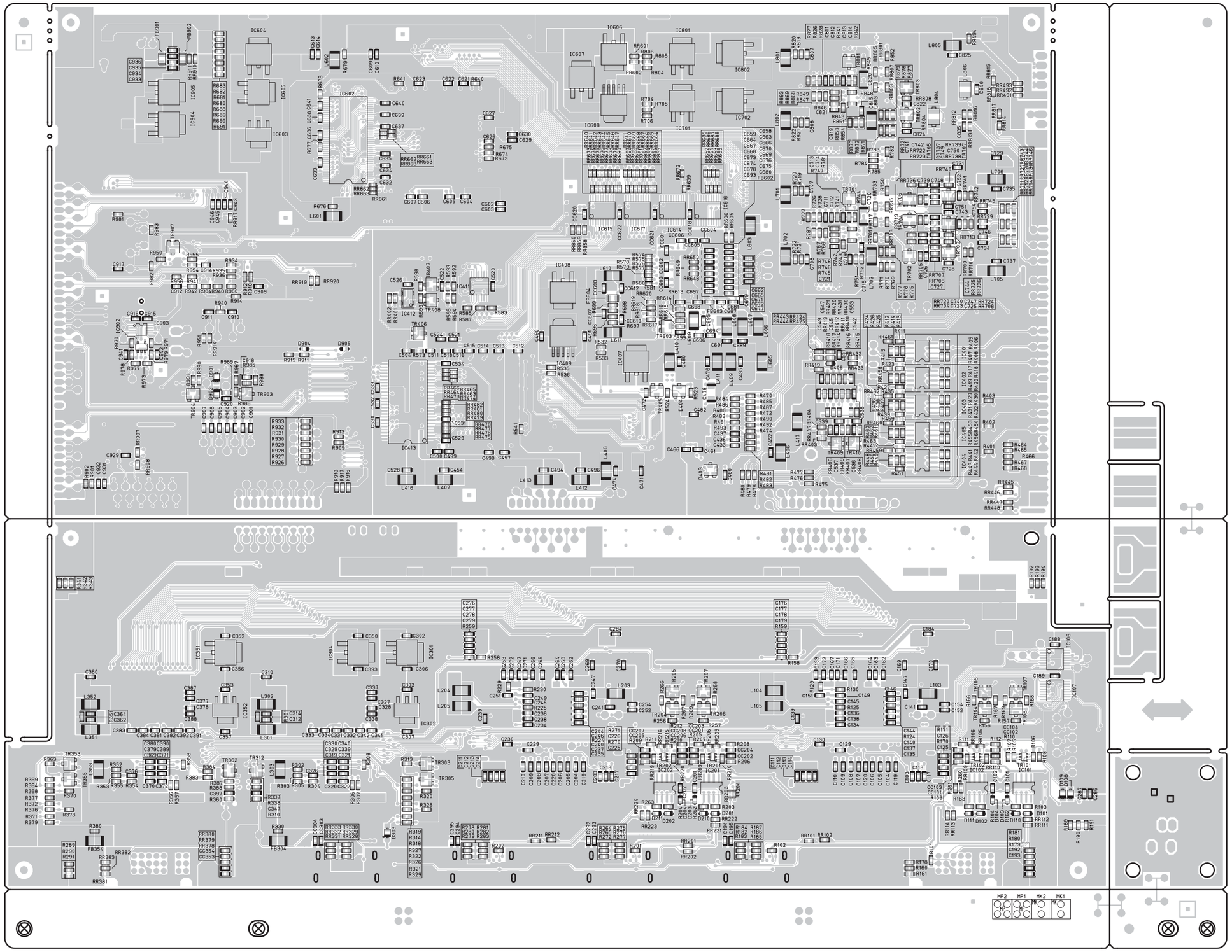


FOIL SIDE

1U-3645 D. VIDEO P.W.B. UNIT

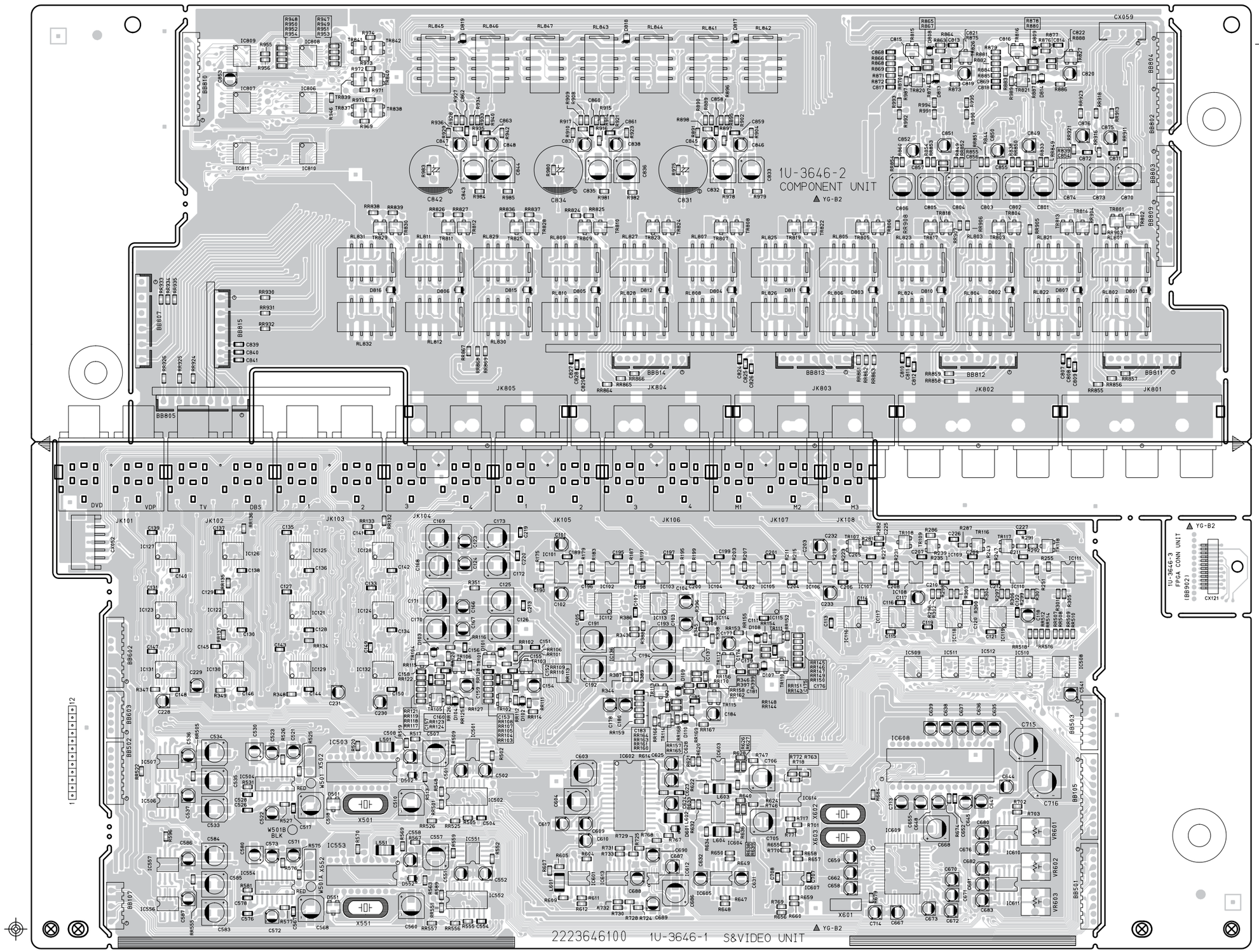


COMPONENT SIDE

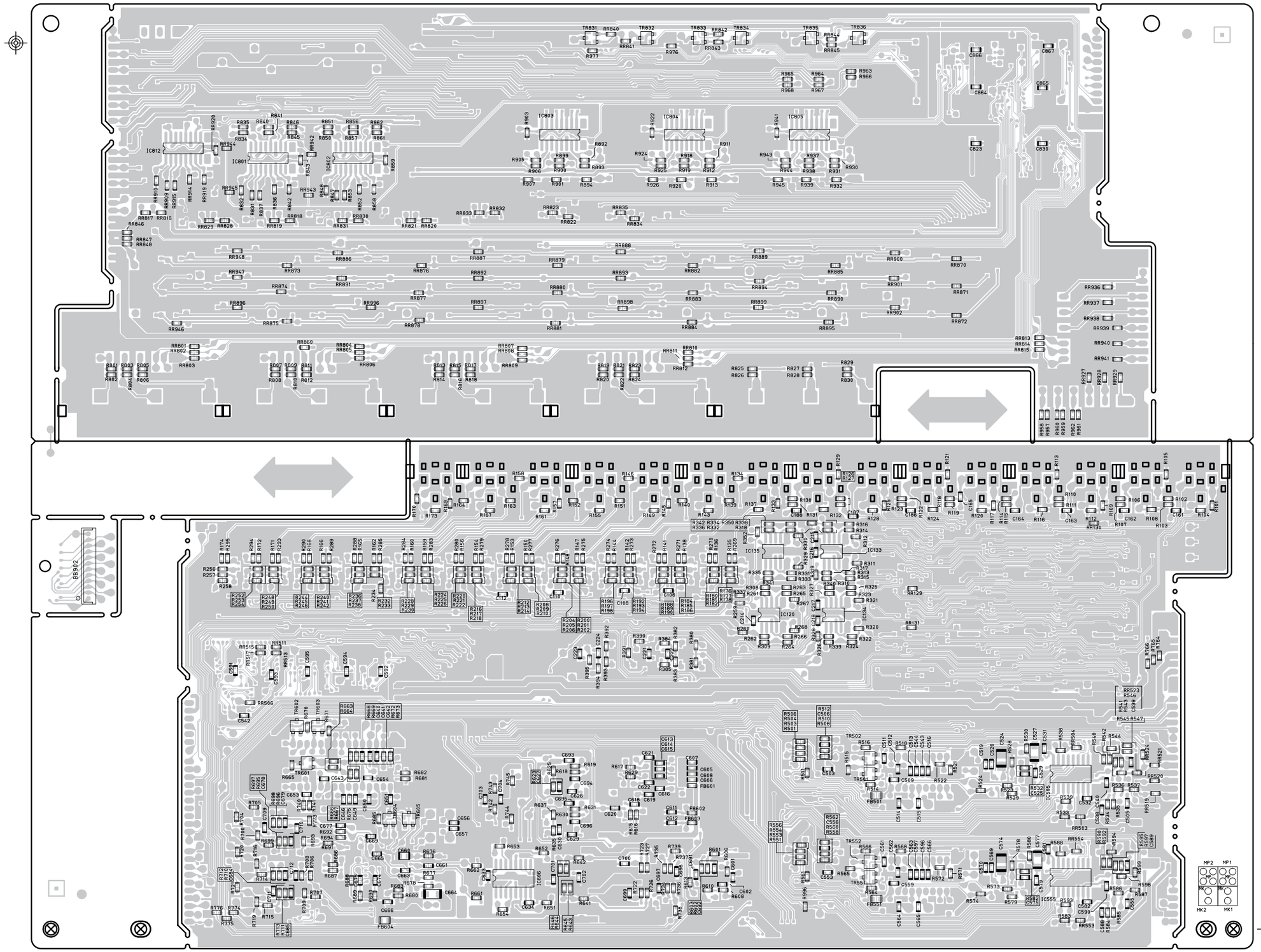


FOIL SIDE

1U-3646 A. VIDEO P.W.B. UNIT

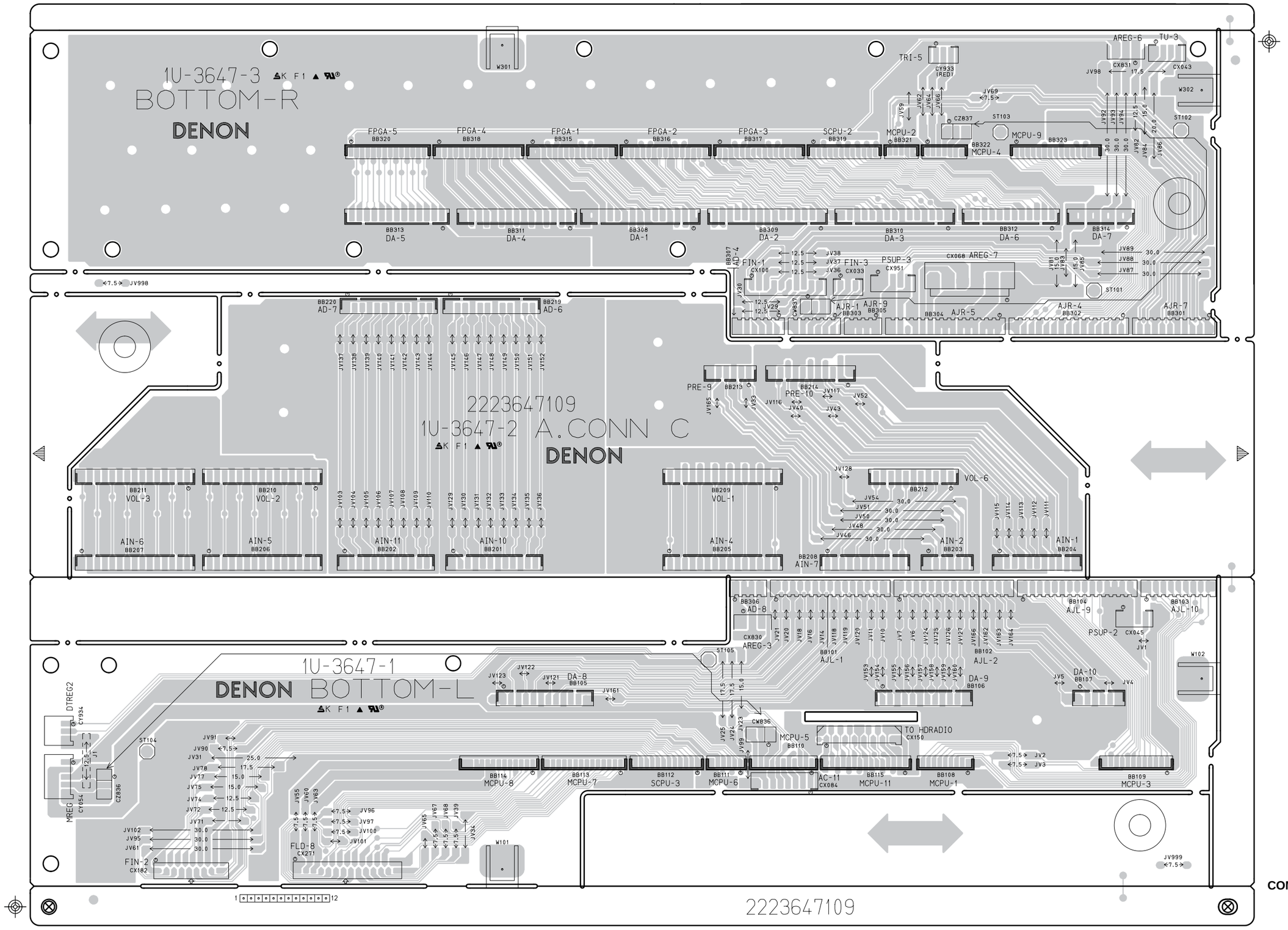


COMPONENT SIDE



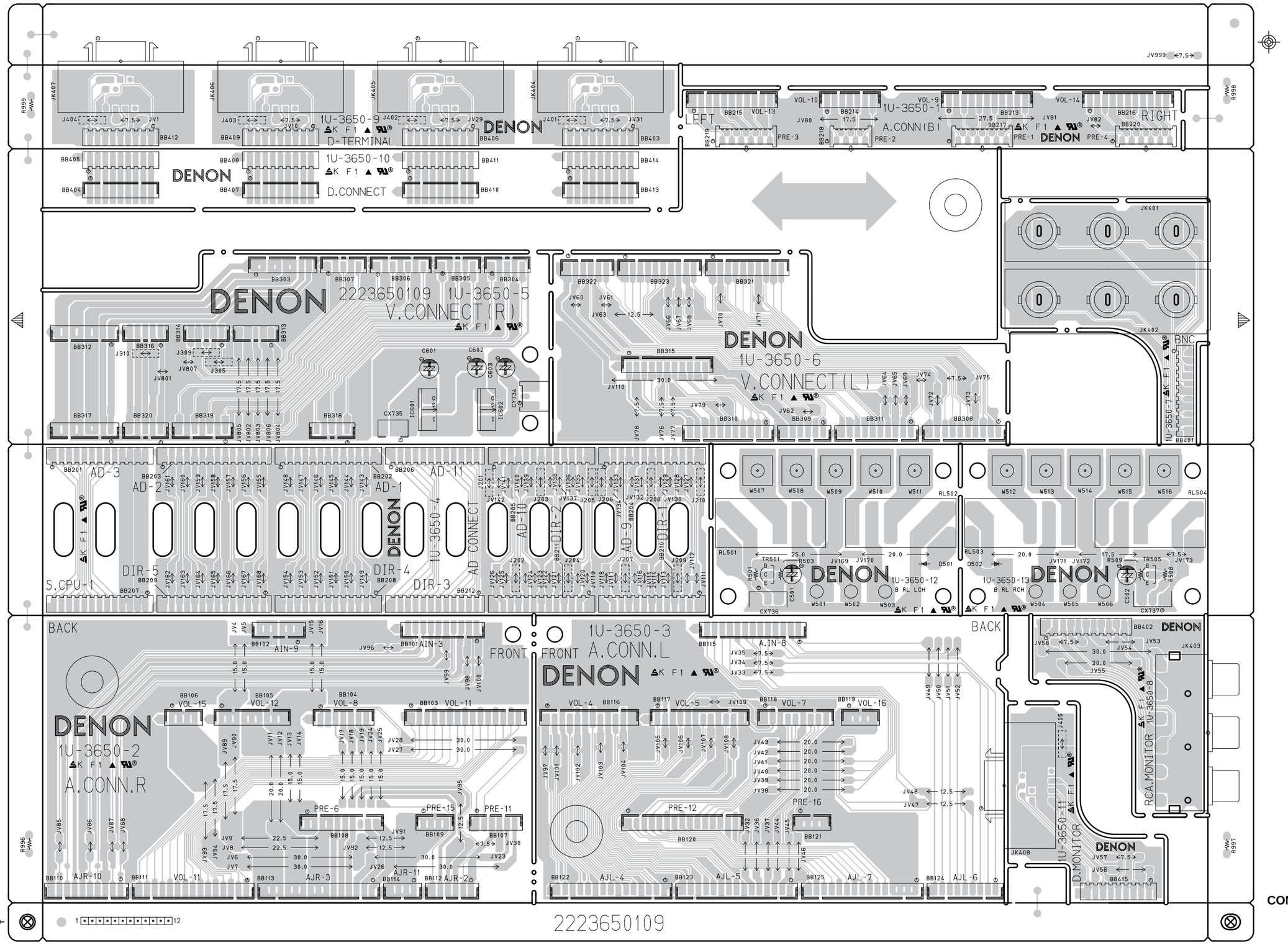
FOIL SIDE

1U-3647 CONNECT-1 P.W.B. UNIT



COMPONENT SIDE

1U-3650 CONNECT-2 P.W.B. UNIT



COMPONENT SIDE