

SERVICE MANUAL

MODEL	JP	E3	E2	EK	E2A	E1C	EUT
AVR-2309CI		✓					
AVR-889		✓					

AV SURROUND RECEIVER

注意

サービスをおこなう前に、このサービスマニュアルを必ずお読みください。本機は、火災、感電、けがなどに対する安全性を確保するために、さまざまな配慮をおこなっており、また法的には「電気用品安全法」にもとづき、所定の許可を得て製造されております。従ってサービスをおこなう際は、これらの安全性が維持されるよう、このサービスマニュアルに記載されている注意事項を必ずお守りください。

• For purposes of improvement, specifications and design are subject to change without notice.

• 本機の仕様は性能改良のため、予告なく変更することがあります。
• 補修用性能部品の保有期間は、製造打切後 8 年です。

• Please use this service manual with referring to the operating instructions without fail.

• 修理の際は、必ず取扱説明書を参照の上、作業を行ってください。

• Some illustrations using in this service manual are slightly different from the actual set.

• 本文中に使用しているイラストは、説明の都合上現物と多少異なる場合があります。

DENON

Denon Brand Company, D&M Holdings Inc.

SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Before returning the unit to the customer, make sure you make either (1) a leakage current check or (2) a line to chassis resistance check. If the leakage current exceeds 0.5 milliamps, or if the resistance from chassis to either side of the power cord is less than 460 kohms, the unit is defective.

CAUTION Please heed the points listed below during servicing and inspection.

⊙ Heed the cautions!

Spots requiring particular attention when servicing, such as the cabinet, parts, chassis, etc., have cautions indicated on labels or seals. Be sure to heed these cautions and the cautions indicated in the handling instructions.

⊙ Caution concerning electric shock!

- (1) An AC voltage is impressed on this set, so touching internal metal parts when the set is energized could cause electric shock. Take care to avoid electric shock, by for example using an isolating transformer and gloves when servicing while the set is energized, unplugging the power cord when replacing parts, etc.
- (2) There are high voltage parts inside. Handle with extra care when the set is energized.

⊙ Caution concerning disassembly and assembly!

Though great care is taken when manufacturing parts from sheet metal, there may in some rare cases be burrs on the edges of parts which could cause injury if fingers are moved across them. Use gloves to protect your hands.

⊙ Only use designated parts!

The set's parts have specific safety properties (fire resistance, voltage resistance, etc.). For replacement parts, be sure to use parts which have the same properties. In particular, for the important safety parts that are marked \triangle on wiring diagrams and parts lists, be sure to use the designated parts.

⊙ Be sure to mount parts and arrange the wires as they were originally!

For safety reasons, some parts use tape, tubes or other insulating materials, and some parts are mounted away from the surface of printed circuit boards. Care is also taken with the positions of the wires inside and clamps are used to keep wires away from heating and high voltage parts, so be sure to set everything back as it was originally.

⊙ Inspect for safety after servicing!

Check that all screws, parts and wires removed or disconnected for servicing have been put back in their original positions, inspect that no parts around the area that has been serviced have been negatively affected, conduct an insulation check on the external metal connectors and between the blades of the power plug, and otherwise check that safety is ensured.

(Insulation check procedure)

Unplug the power cord from the power outlet, disconnect the antenna, plugs, etc., and turn the power switch on. Using a 500V insulation resistance tester, check that the insulation resistance between the terminals of the power plug and the externally exposed metal parts (antenna terminal, headphones terminal, microphone terminal, input terminal, etc.) is $1M\Omega$ or greater. If it is less, the set must be inspected and repaired.

CAUTION Concerning important safety parts

Many of the electric and structural parts used in the set have special safety properties. In most cases these properties are difficult to distinguish by sight, and using replacement parts with higher ratings (rated power and withstand voltage) does not necessarily guarantee that safety performance will be preserved. Parts with safety properties are indicated as shown below on the wiring diagrams and parts lists in this service manual. Be sure to replace them with parts with the designated part number.

- (1) Schematic diagrams ... Indicated by the \triangle mark.
- (2) Parts lists ... Indicated by the \triangle mark.

Using parts other than the designated parts could result in electric shock, fires or other dangerous situations.

注 意 サービス、点検時にはつぎのことにご注意願います。

◎注意事項をお守りください！

サービスのとき特に注意を必要とする個所についてはキャビネット、部品、シャーシなどにラベルや捺印で注意事項を表示しています。これらの注意書きおよび取扱説明書などの注意事項を必ずお守りください。

◎感電に注意！

- (1) このセットは、交流電圧が印加されていますので通電時に内部金属部に触れると感電することがあります。従って通電サービス時には、絶縁トランスの使用や手袋の着用、部品交換には、電源プラグを抜くなどして感電にご注意ください。
- (2) 内部には高電圧の部分がありますので、通電時の取扱には十分ご注意ください。

◎分解、組み立て作業時のご注意！

板金部品の端面の『バリ』は、部品製造時に充分管理をしておりますが、板金端面は鋭利となっている箇所がありますので、部品端面に触れたまま指を動かすとまれに怪我をする場合がありますので十分注意して作業して下さい。手の保護のために手袋を着用して下さい。

◎指定部品の使用！

セットの部品は難燃性や耐電圧など安全上の特性を持ったものとなっています。従って交換部品は、使用されていたものと同じ特性の部品を使用して下さい。特に配線図、部品表に ▲ 印で指定されている安全上重要な部品は必ず指定のものをご使用ください。

◎部品の取付けや配線の引きまわしは、元どおりに！

安全上、テープやチューブなどの絶縁材料を使用したり、プリント基板から浮かして取付けた部品があります。また内部配線は引きまわしやクランパーによって発熱部品や高圧部品に接近しないように配慮されていますので、これらは必ず元どおりにして下さい。

◎サービス後は安全点検を！

サービスのために取り外したねじ、部品、配線などが元どおりになっているか、またサービスした個所の周辺を劣化させてしまったところがないかなどを点検し、外部金属端子部と、電源プラグの刃の間の絶縁チェックをおこなうなど、安全性が確保されていることを確認してください。

(絶縁チェックの方法)

電源コンセントから電源プラグを抜き、アンテナやプラグなどを外し、電源スイッチを入れます。500V 絶縁抵抗計を用いて、電源プラグのそれぞれの端子と外部露出金属部 [アンテナ端子、ヘッドホン端子、マイク端子、入力端子など] との間で、絶縁抵抗値が 1 MΩ 以上であることを確認してください。この値以下のときはセットの点検修理が必要です。

注 意 安全上重要な部品について

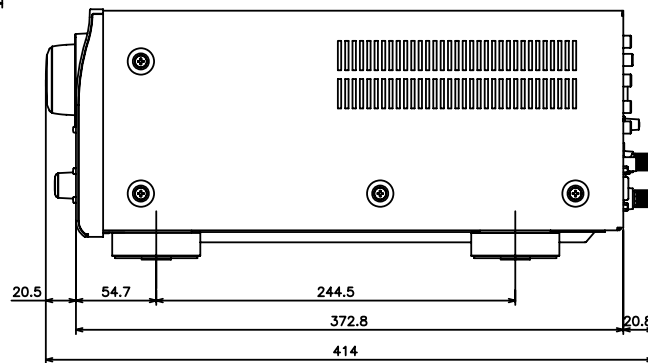
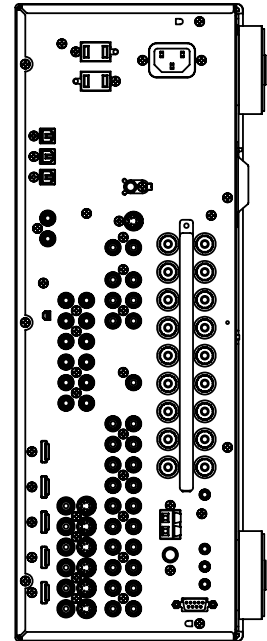
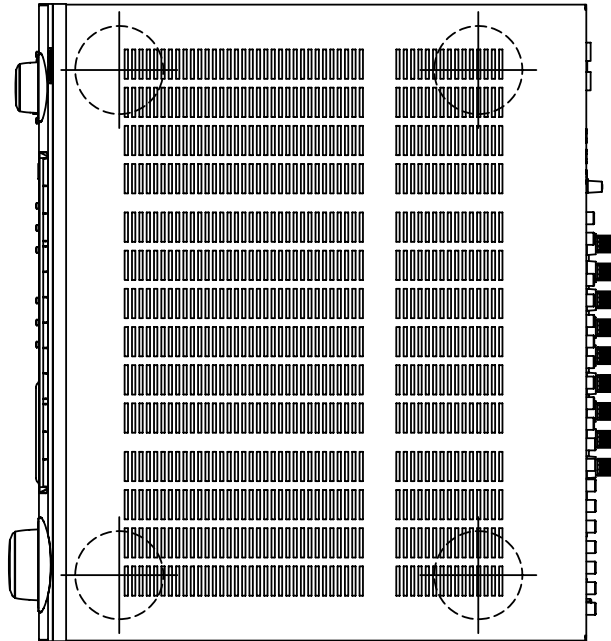
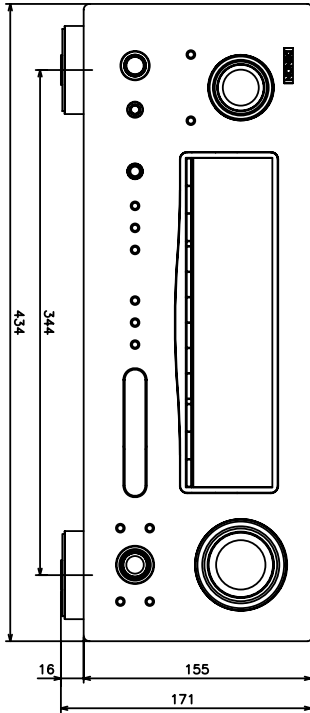
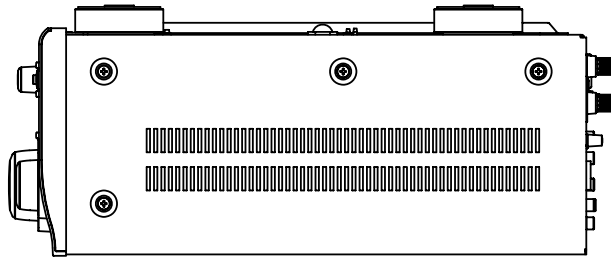
本機に使用している多くの電気部品、および機構部品は安全上、特別な特性を持っています。この特性はほとんどの場合、外観では判別つきにくく、またもとの部品より高い定格（定格電力、耐圧）を持ったものを使用しても安全性が維持されるとは、限りません。安全上の特性を持った部品は、このサービスマニュアルの配線図、部品表につぎのように表示していますので必ず指定されている部品番号のものを使用願います。

- (1) 配線図… ▲ マークで表示しています。
- (2) 部品表… ▲ マークで表示しています。

指定された部品と異なるものを使用した場合には、感電、火災などの危険を生じる恐れがあります。

DIMENSION

AVR-2309CI/AVR-889 model



WIRE ARRANGEMENT

If wire bundles are untied or moved to perform adjustment or parts replacement etc., be sure to rearrange them neatly as they were originally bundled or placed afterward. Otherwise, incorrect arrangement can be a cause of noise generation.

Wire arrangement viewed from the top

ワイヤー整形図

調整や部品の交換等により、ワイヤー類の結束をはずしたり移動させた場合には、それらの作業が完了した時点でワイヤーの整形をおこなってください。正しく整形されてないとノイズ発生の原因となることがあります。

上面からみたワイヤー整形

Back Panel side



Front Panel side

CAUTION IN SERVICING

Initializing AV SURROUND RECEIVER/AMPLIFIER

AV SURROUND RECEIVER/AMPLIFIER initialization should be performed when the μ com, peripheral parts of μ com, and Digital P.W.B. are replaced.

1. Switch off the unit.
2. Hold the following INPUT MODE button and SPEAKERS button, and switch on the unit.
3. Check that the entire display is flashing with an interval of about 1 second, and release your fingers from the 2 buttons and the microprocessor will be initialized.

Note: • If step 3 does not work, start over from step 1.
• All user settings will be lost and this factory setting will be recovered when this initialization mode. So make sure to memorize your setting for restoring after the initialization.

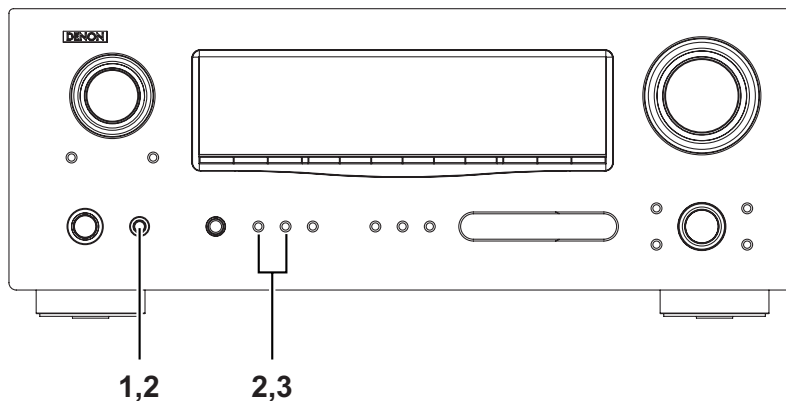
サービス時の注意事項

AV サラウンドレシーバー / アンプの初期化について

マイコンやマイコン周辺部品、Digital 基板等を交換した場合は、AV サラウンドレシーバー / アンプの初期化を行って下さい。

1. ON/OFF ボタンを OFF にします。
2. INPUT MODE ボタンと SPEAKERS ボタンを同時に押しなが、ON/OFF ボタンを押して ON にします。
3. ディスプレイ表示が約 1 秒間隔で点滅するのを確認後、2つのボタンから指を離します。
*マイコンが初期化されます。

注意: • 上記 3 の状態にならない場合は、もう一度操作 1 からやり直してください。
• 初期化を行うとお客様が設定した内容が工場出荷状態に戻りますので、あらかじめ設定内容を控えておき初期化後再設定してください。



About RS-232C communications

RS-232C communications are not possible when "Z4" is displayed on the FL display.

Press and hold in the "STATUS" and "▽" buttons for over 3 seconds with the power turned on to turn the "Z4" display off. RS-232C communications are now enabled.

RS-232C の通信について

FL Display に "Z4" が表示されている場合は、RS-232C の通信ができません。

電源が ON の状態で、"STATUS"、"▽" の 2 つのボタンを 3 秒以上押し続けて、"Z4" を非表示にしてください。RS-232C の通信ができるようになります。

JIG to use for servicing

When you repair the printing board, you can use the following JIG. Please order to Denon Official Service Distributor in your region if necessary.

Extention cable kit

00D SPK- 561 EXTENSION UNIT KIT : 1 Set
00D SPK- 562 TUCP CONN. JOINT KIT : 1 Set

Extention cable for Idling Current

Parts Number for Extension Cables and Quantity of Unit.

Parts Number	Parts Name	Q'ty / unit	Remarks
612050082004D	6P 250mm NH	1	L=250mm 6P NH Cable
612050083007D	8P 250mm NH	1	L=250mm 8P NH Cable

How to use and Adjust Idle Current.

1. The thin and hard plate (ex. Ruler) is fixed with the tape behind the cable.
2. The voltmeter is connected with the other side of the extension cable.
3. Refer to ADJUSTMENT(Idle Current).

サービス時に使用する治具について

基板を修理する際、使用する治具は 下記のとおりです。必要に応じて販社サービスへ注文下さい。

延長ケーブルキット

00D SPK- 561 EXTENSION UNIT KIT : 1 式
00D SPK- 562 TUCP CONN. JOINT KIT : 1 式

アイドル電流用延長ケーブル

延長ケーブルの品番と使用本数

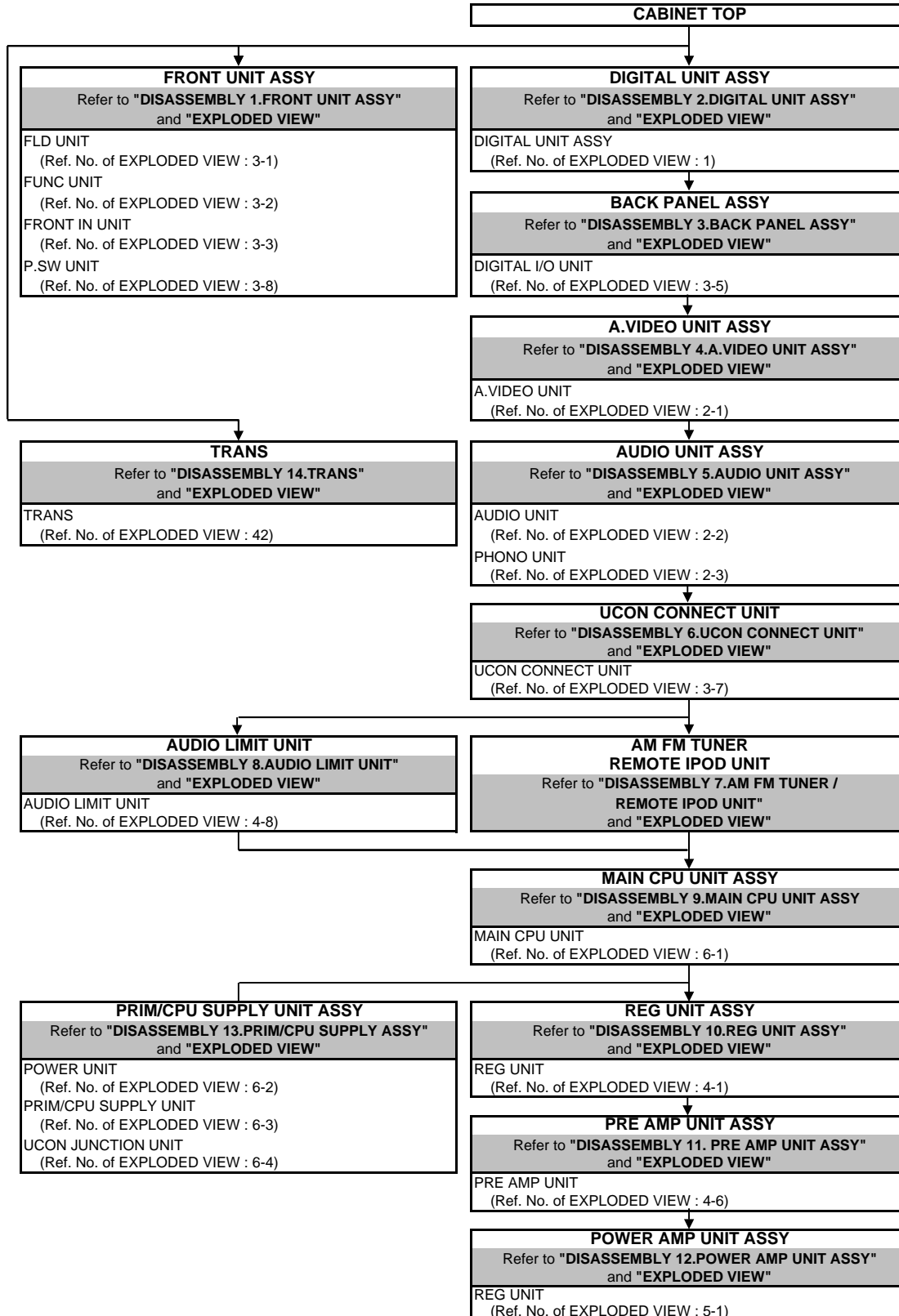
Parts Number	Parts Name	Q'ty / unit	Remarks
612050082004D	6P 250mm NH	1	L=250mm 6P NH Cable
612050083007D	8P 250mm NH	1	L=250mm 8P NH Cable

使用方法と調整方法

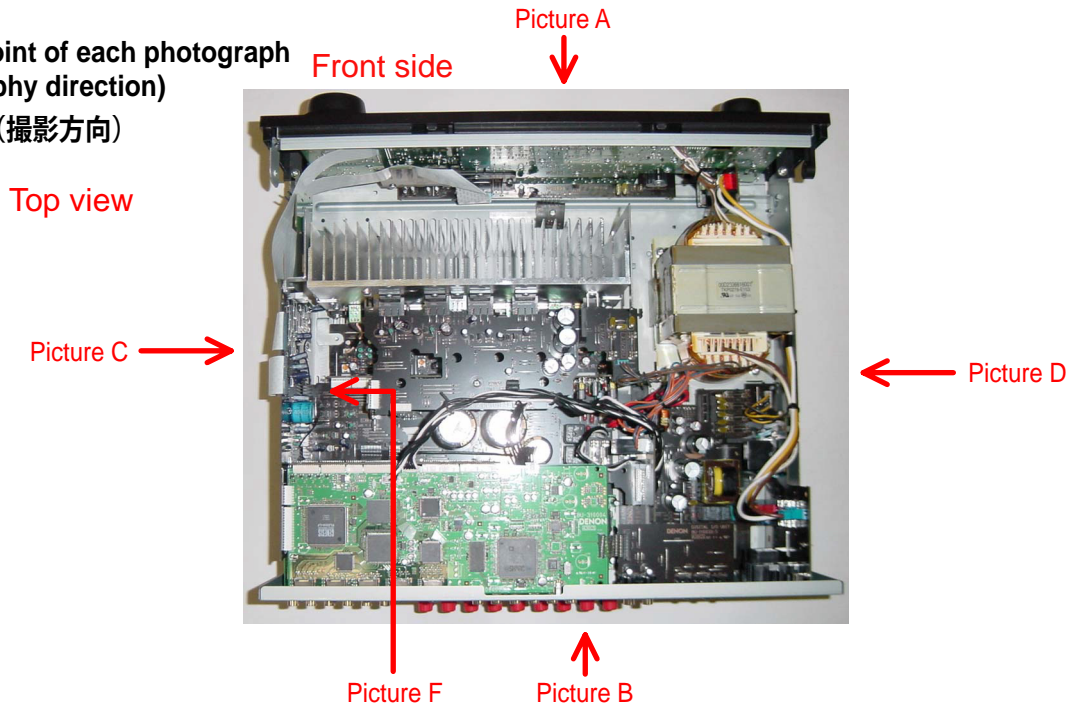
1. ケーブルに沿わせて定規などの硬い板をテープで止めてください。
2. ケーブルのコネクタとは反対側に電圧計を接続します。
3. 調整の項目を参照してアイドル電流を調整します。

DISASSEMBLY

- Disassemble in order of the arrow of the figure of following flow.
下記フロー図の矢印の順番にはずしてください。
- In the case of the re-assembling, assemble it in order of the reverse of the following flow.
再組み立ての場合は、下記のフローの逆の順番に組立ててください
- In the case of the re-assembling, observe "attention of assembling" it.
再組み立ての場合は、「組立のご注意」を遵守してください。



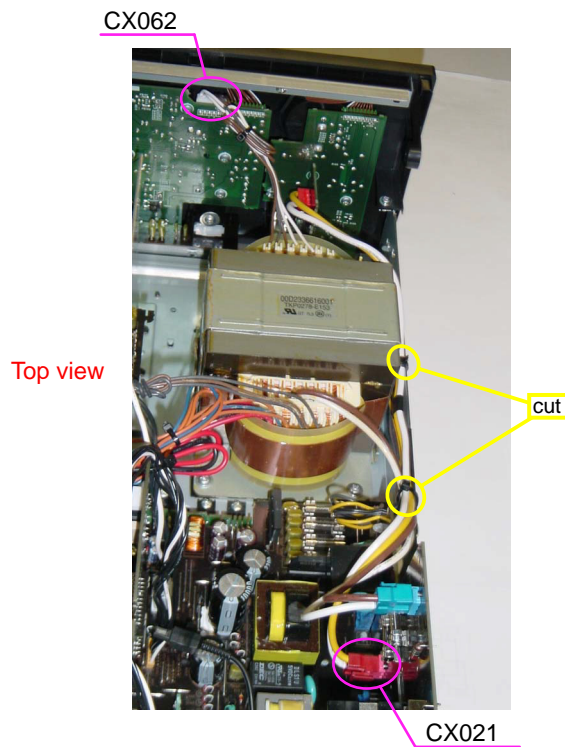
The viewpoint of each photograph
(photography direction)
各図の視点(撮影方向)



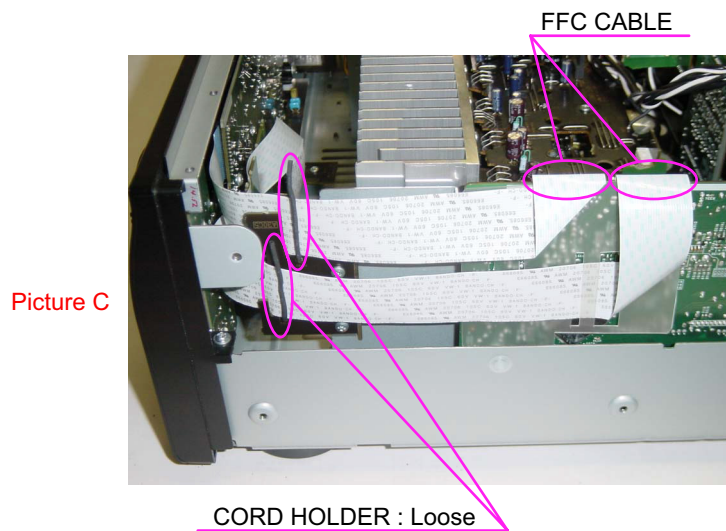
1. FRONT UNIT ASSY

Proceeding (手順) : **TOP COVER SUB ASSY** → **FRONT UNIT ASSY**

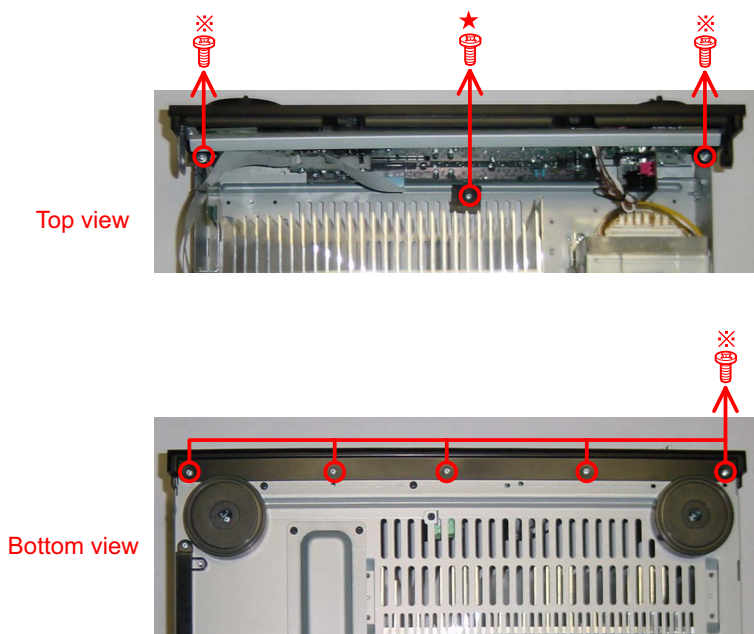
(1) Disconnect the connector wires. (コネクタワイヤーをはずす。)



(2) Disconnect the FFC cable. (FFC ケーブルとねじをはずす。)



(3) Remove the screws. (ねじをはずす。)

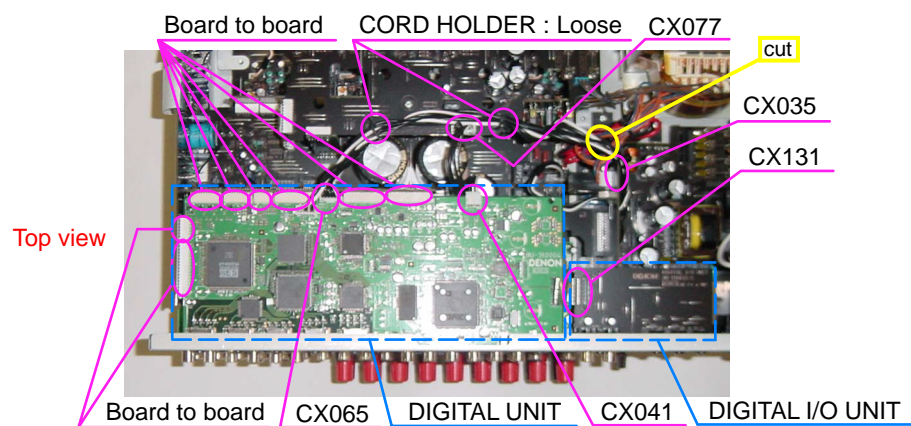


Please refer to "**EXPLODED VIEW**" for the disassembly method of each P.W.B included in FRONT UNIT ASSY.
FRONT UNIT ASSY の各基板のはずしかたは "**EXPLODED VIEW**" を参照してください。

2. DIGITAL UNIT ASSY

Proceeding (手順) : **TOP COVER SUB ASSY** → **DIGITAL UNIT ASSY**

(1) Disconnect the connector wires and boards. (コネクタワイヤーとコネクタボードをはずす。)



(2) Remove the screws. (ねじをはずす。)



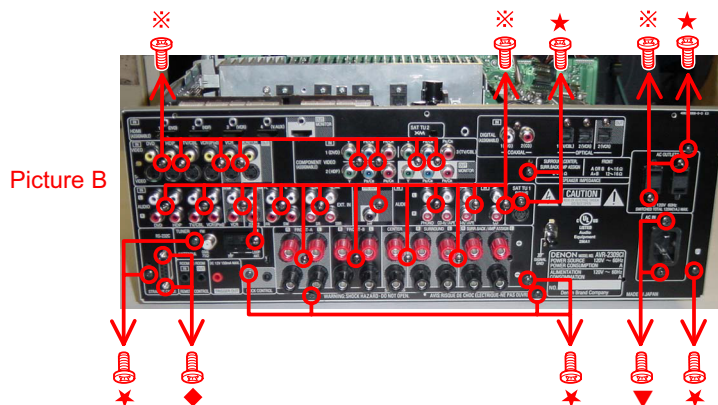
3. BACK PANEL ASSY

Proceeding (手順) : **TOP COVER SUB ASSY** → **DIGITAL UNIT ASSY**
→ **BACK PANEL ASSY**

(1) Remove the screw cover. (screw cover をはずす。)



(2) Remove the screws. (ねじをはずす。)

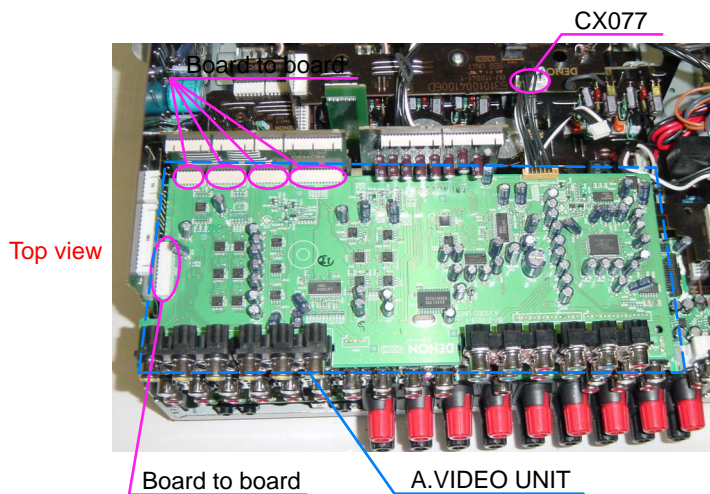


Please refer to "EXPLODED VIEW" for the disassembly method of each P.W.B included in BACK PANEL ASSY.
 BACK PANEL ASSY の各基板のはずしかたは "EXPLODED VIEW" を参照してください。

4. A.VIDEO UNIT ASSY

Proceeding (手順) : TOP COVER SUB ASSY → DIGITAL UNIT ASSY
 → BACK PANEL ASSY → A.VIDEO UNIT ASSY

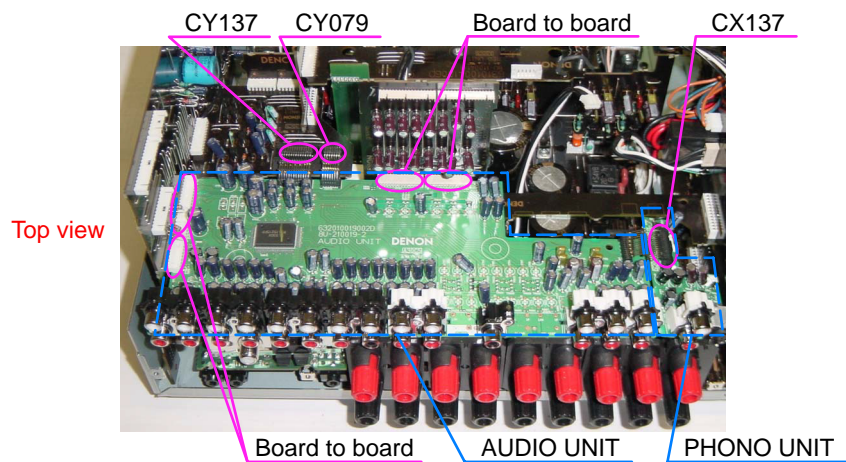
(1) Disconnect the connector wires and boards. (コネクタワイヤーとコネクタボードをはずす。)



5. AUDIO UNIT ASSY

Proceeding (手順) : **TOP COVER SUB ASSY** → **DIGITAL UNIT ASSY**
 → **BACK PANEL ASSY** → **A.VIDEO UNIT ASSY**
 → **AUDIO UNIT ASSY**

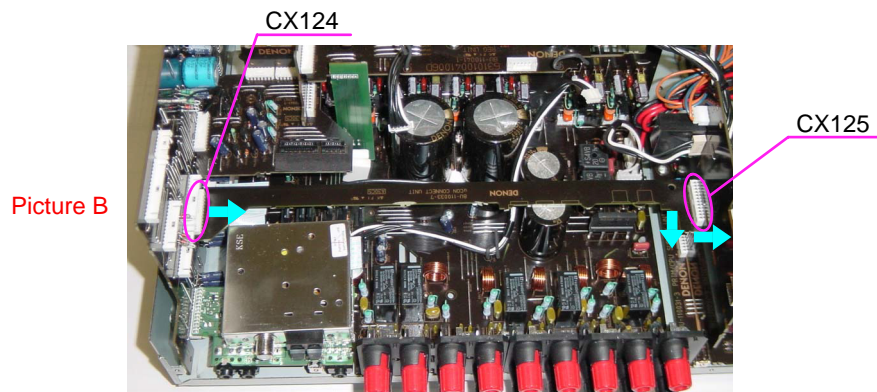
(1) Disconnect the connector wires and boards. (コネクタワイヤーとコネクタボードをはずす。)



6. UCON CONNECT UNIT

Proceeding (手順) : **TOP COVER SUB ASSY** → **DIGITAL UNIT ASSY**
 → **BACK PANEL ASSY** → **A.VIDEO UNIT ASSY**
 → **AUDIO UNIT ASSY** → **UCON CONNECT UNIT**

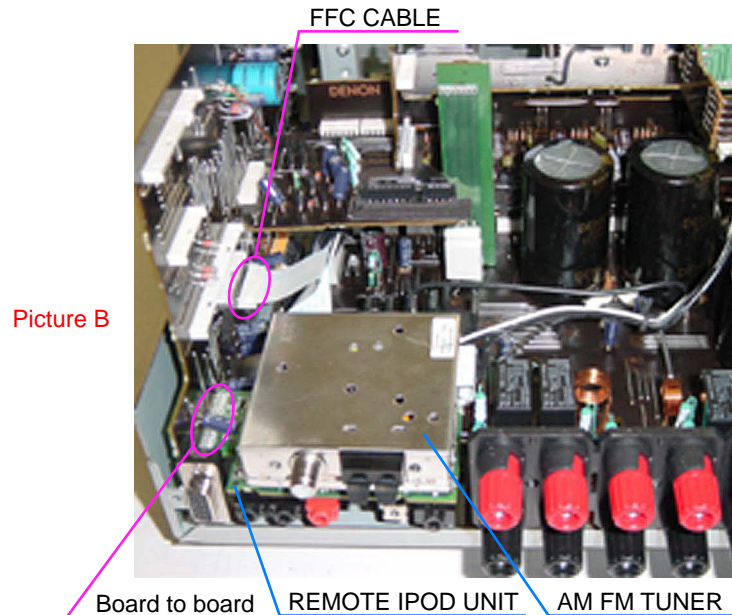
(1) Disconnect the connector board. (コネクタボードをはずす。)



7. AM FM TUNER / REMOTE IPOD UNIT

Proceeding (手順) : **TOP COVER SUB ASSY** → **DIGITAL UNIT ASSY**
→ **BACK PANEL ASSY** → **A.VIDEO UNIT ASSY**
→ **AUDIO UNIT ASSY** → **UCON CONNECT UNIT**
→ **AM FM TUNER / REMOTE IPOD UNIT**

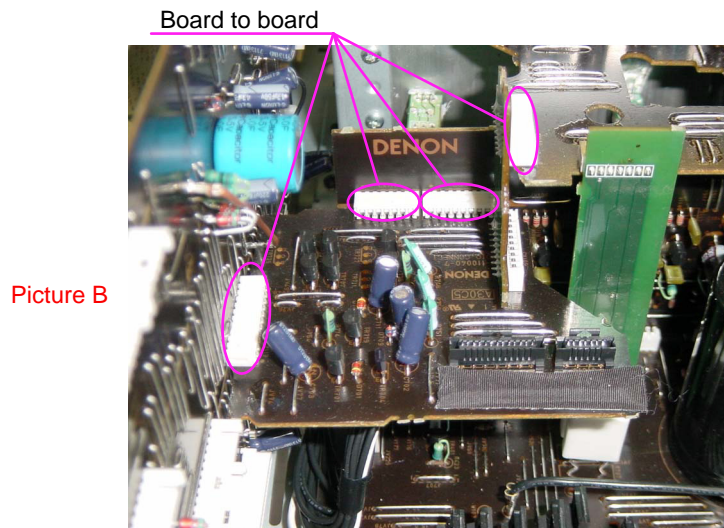
(1) Disconnect the connector wire and connector board. (FFC ケーブルとコネクタボードをはずす。)



8. AUDIO LIMIT UNIT

Proceeding (手順) : **TOP COVER SUB ASSY** → **DIGITAL UNIT ASSY**
→ **BACK PANEL ASSY** → **A.VIDEO UNIT ASSY**
→ **AUDIO UNIT ASSY** → **UCON CONNECT UNIT**
→ **AUDIO LIMIT UNIT**

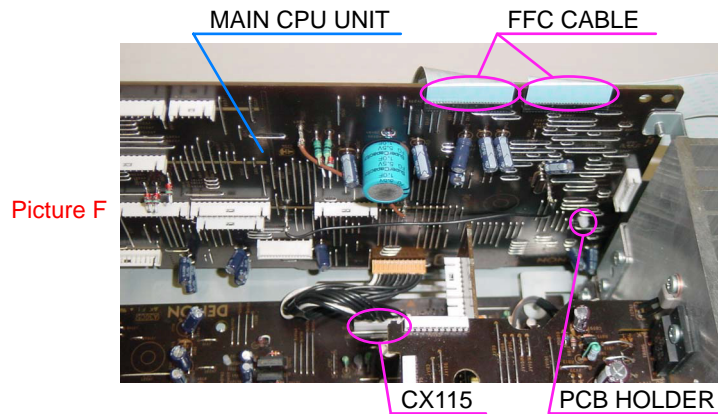
(1) Disconnect the connector boards. (コネクタボードをはずす。)



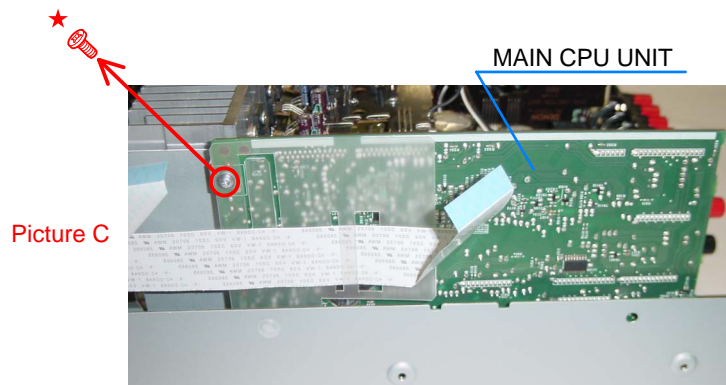
9. MAIN CPU UNIT ASSY

Proceeding (手順) : **TOP COVER SUB ASSY** → **DIGITAL UNIT ASSY**
→ **BACK PANEL ASSY** → **A.VIDEO UNIT ASSY**
→ **AUDIO UNIT ASSY** → **UCON CONNECT UNIT**
→ **AUDIO LIMIT UNIT** → **MAIN CPU UNIT ASSY**

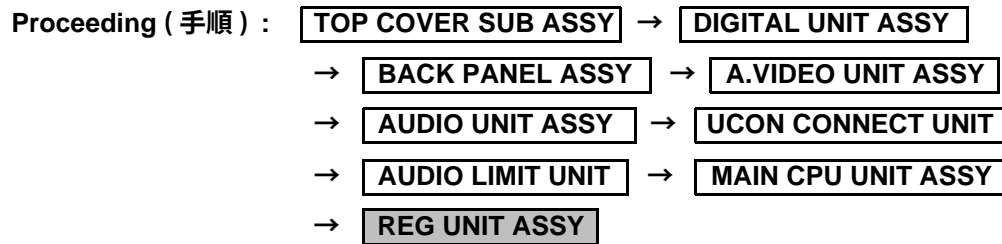
(1) Disconnect the connector wire and FFC cables. (コネクタワイヤーとFFCケーブルをはずす。)



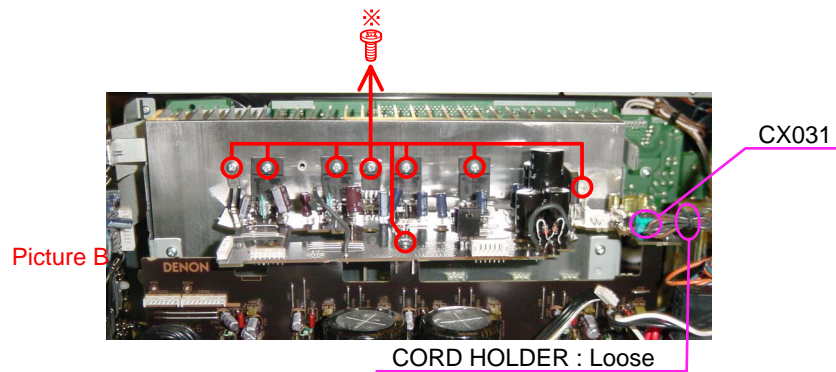
(2) Remove the screw. (ねじをはずす。)



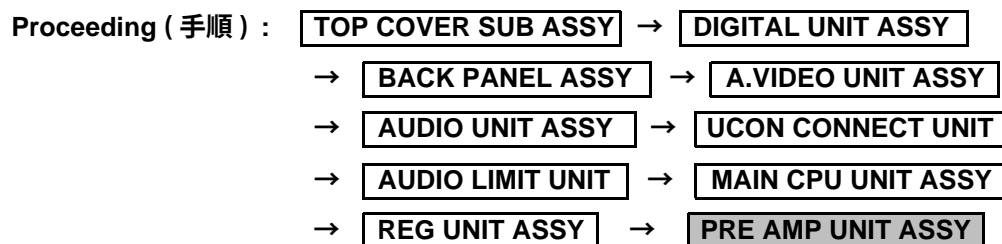
10. REG UNIT ASSY



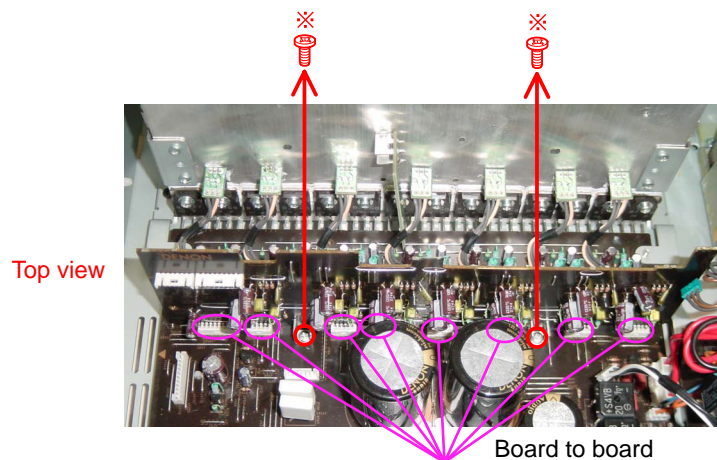
(1) Disconnect the connector wire and remove the screws. (コネクタワイヤーとねじをはずす。)



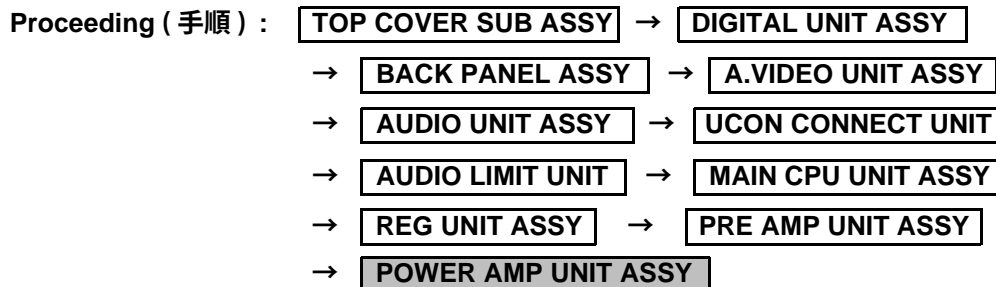
11. PRE AMP UNIT ASSY



(1) Remove the screws and disconnect the connector board. (ねじとコネクタボードをはずす。)



12. POWER AMP UNIT ASSY



Please refer to "EXPLODED VIEW" for the disassembly method of POWER AMP UNIT ASSY.
POWER AMP UNIT ASSY のはずしかたは "EXPLODED VIEW" を参照してください。



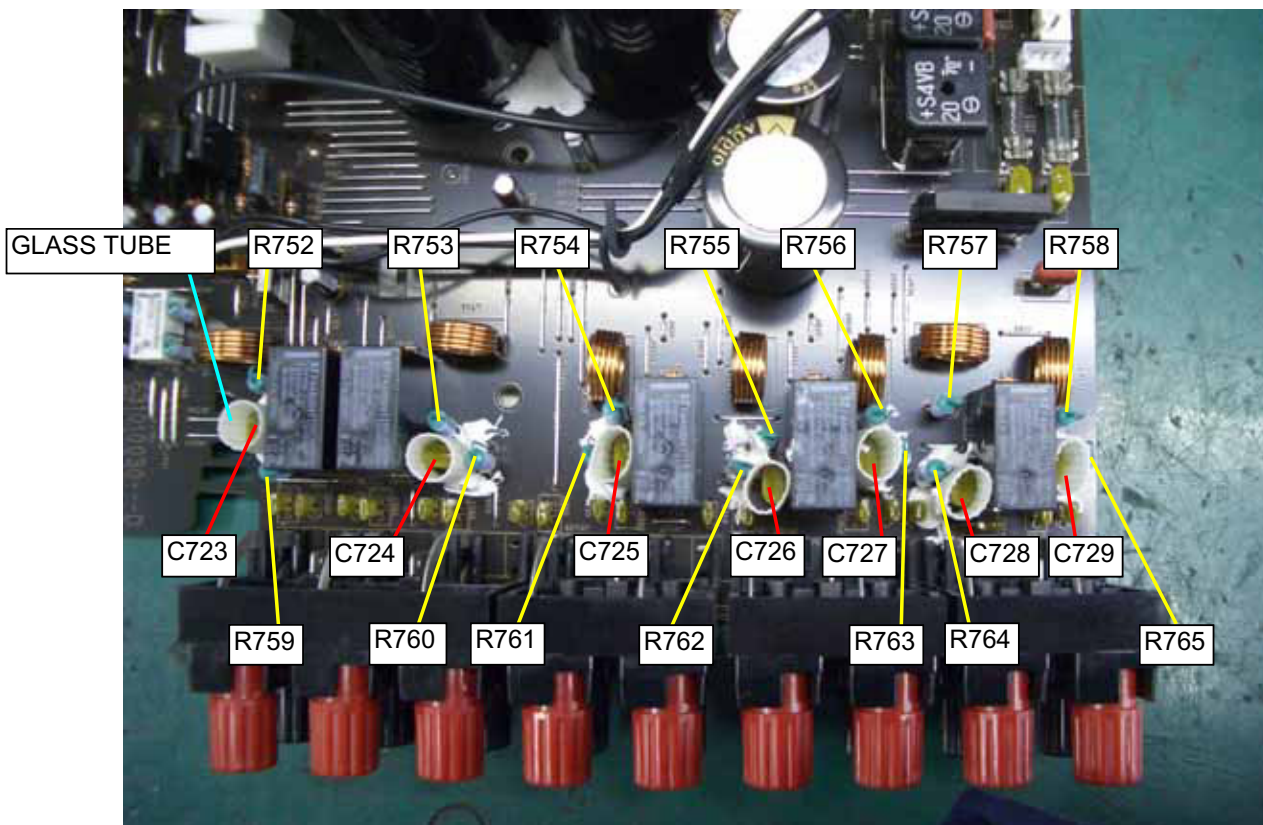
<attention of assemble>

- ※ When repairing, be sure to provide spatial distance between R752 to R765 and C723 to C729.
R752 to R765 become hot when there is a problem.
As a measure to deal with the heat of R752 to R765, attach GLASS TUBE to C723 to C729 for products with serial numbers starting from the ones indicated below.
Do not attach GLASS TUBE to products with earlier serial numbers.
Be particularly careful when repairing products on which no GLASS TUBE are attached.

<組立のご注意>

- ※ 修理の際は、R752～R765 と C723～C729の間には、必ず空間距離を設けてください。
R752～R765 は、異常時に高温になります。
R752～R765 の高温対策として、以下のシリアル番号以降の生産品には、C723～C729に保護用の GLASS TUBE を付けています。
それ以前の生産品には、GLASS TUBE を付けていません。
GLASS TUBE が付いていない生産品の修理時は特に注意してください。

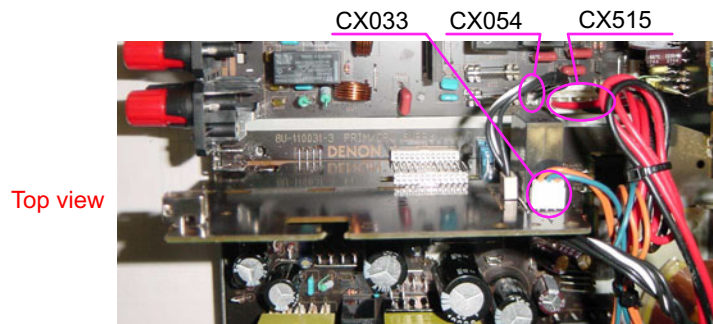
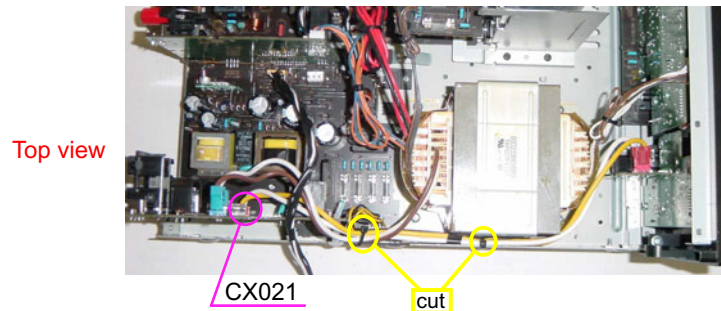
MODEL	SERIAL No.
AVR2309CIBKE3	06041～
AVR889BKE3	03001～



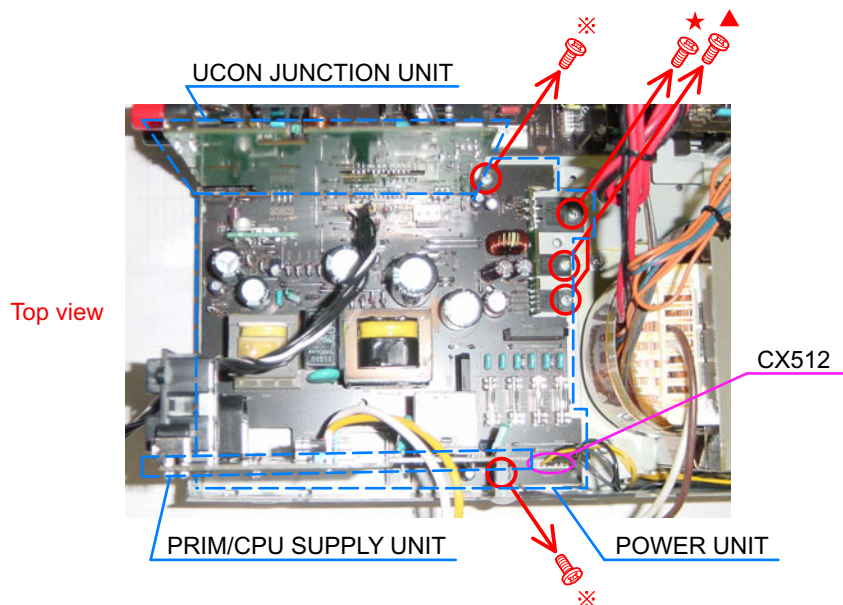
13. PRIM/CPU SUPPLY UNIT UNIT ASSY

- Proceeding (手順) :
- **TOP COVER SUB ASSY** → **DIGITAL UNIT ASSY**
 - **BACK PANEL ASSY** → **A.VIDEO UNIT ASSY**
 - **AUDIO UNIT ASSY** → **UCON CONNECT UNIT**
 - **AUDIO LIMIT UNIT** → **MAIN CPU UNIT ASSY**
 - **PRIM/CPU SUPPLY UNIT ASSY**

(1) Disconnect the connector wires. (コネクタワイヤーをはずす。)



(2) Disconnect the connector wire and remove the screws. (コネクタワイヤーとねじをはずす。)

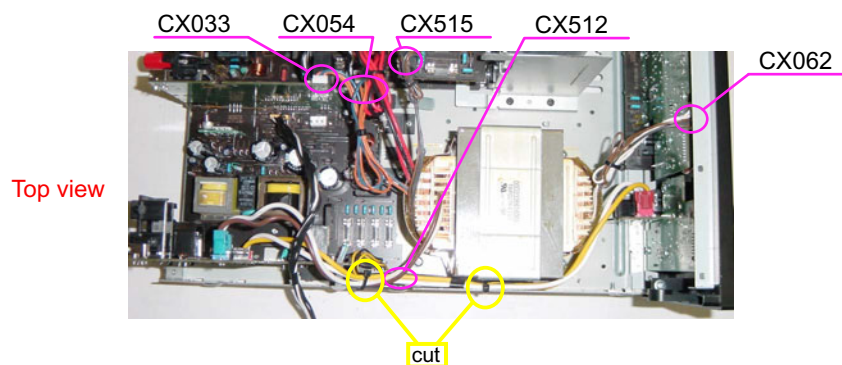


Please refer to "**EXPLODED VIEW**" for the disassembly method of PRIM/CPU SUPPLY UNIT ASSY.
PRIM/CPU SUPPLY UNIT ASSY のはずしかたは "**EXPLODED VIEW**" を参照してください。

14. TRANS

Proceeding (手順) : **TOP COVER SUB ASSY** → **TRANS**

(1) Disconnect the connector wires. (コネクタコードをはずす。)



Please refer to "**EXPLODED VIEW**" for the disassembly method of TRANS.
TRANS のはずしかたは "**EXPLODED VIEW**" を参照してください。

CHECK WITH TEST MODE

μcom/DSP Error Display Mode

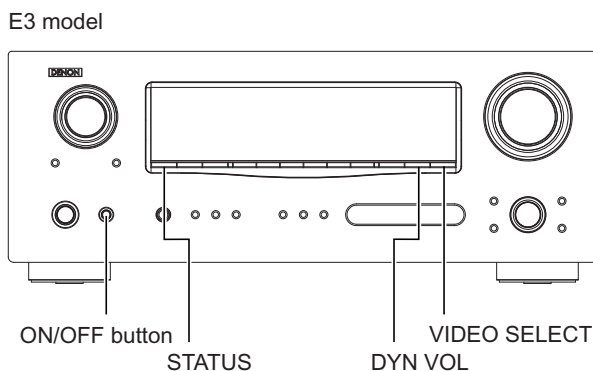
Operation Spec

μcom version display mode:

When the following conditions are satisfied at its starting state, error information is displayed before version information.
Starting method (same as μcom version display):

E3 model

While pressing 2 buttons, "DYN VOL" and "VIDEO SELECT", turn on ON/OFF button.
Then, press "STATUS" button to display the following information on the FL Display.



Display Order

Error information → Destination information → Main-μcom version information → Sub-μcom version information
→ DSP version information

Display

Any one of the following list is displayed, in the priority of ①②③④.



Condition	State	Display
① Sub-μcom NG	No response from Sub-μcom	" □ S U B □ □ E R R O R □ 0 1 □ "
② DIR NG	No response from DIR	" □ D I R □ □ E R R O R □ 0 1 □ "
③ DSP NG	When DSP boot, executing DSP reset makes no change to DSP FLAG 0 port "H".	" □ D S P □ □ E R R O R □ 0 1 □ "
	No change to DSP FLAG 0 port "H" before issuing DSP command.	" □ D S P □ □ E R R O R □ 0 2 □ "
	When DSP data read, executing WRITE="L" makes no change to ACK="H".	" □ D S P □ □ E R R O R □ 0 3 □ "
	When DSP data read, executing REQ="L" makes no change to ACK="L".	" □ D S P □ □ E R R O R □ 0 4 □ "
	When DSP data write, executing WRITE="H" makes no change to ACK="H".	" □ D S P □ □ E R R O R □ 0 5 □ "
	When DSP data write, executing REQ="L" makes no change to ACK="L".	" □ D S P □ □ E R R O R □ 0 6 □ "
	When DSP special code boot, executing DSP reset makes no change to DSP FLAG 0 port "H".	" □ D S P □ □ E R R O R □ 1 1 □ "
	No change to DSP FLAG 0 port "H" before issuing DSP special read command.	" □ D S P □ □ E R R O R □ 1 2 □ "
	No change to DSP FLAG 0 port "H" before DSP version read.	" □ D S P □ □ E R R O R □ 1 3 □ "
④ Both SUB/DSP OK		(No error display, version display only)

テストモードによるチェック方法

マイコン・DSP エラー表示モード

動作仕様

マイコンバージョン表示モード：

起動状態にて下記の条件に該当した場合は、バージョン情報表示の前にエラー情報を表示します。

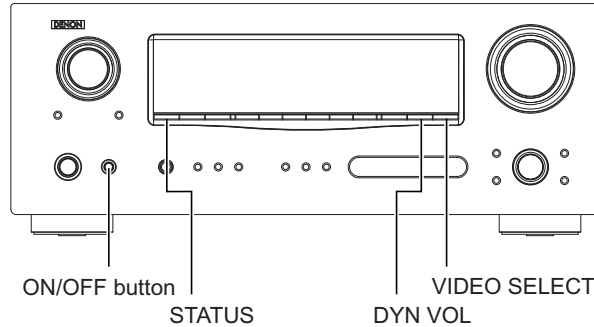
起動方法 (マイコンバージョン表示と同様)：

● E3 モデル

"DYN VOL", "VIDEO SELECT" の 2 つのボタンを押した状態で、ON/OFF ボタンを押して電源を入れます。

その後、"STATUS" ボタンを押すと下表の内容が FL Display に表示されます。

E3 model



表示順序

エラー情報 → 仕向地表示 → メインマイコンバージョン情報 → サブマイコンバージョン情報 → DSP バージョン情報

表示条件

下表のいずれかを表示します。表示の優先順は、①②③④。



条件	状態	表示内容
① SUB マイコンが NG	SUB マイコンからの応答がない	" □ SUB □ □ ERROR □ 0 1 □ "
② DIR が NG	DIR からの応答がない	" □ DIR □ □ ERROR □ 0 1 □ "
③ DSP が NG	DSP コードブート時、DSP リセットを実行しても DSP FLAG 0 ポートが "H" にならない	" □ DSP □ □ ERROR □ 0 1 □ "
	DSP コマンド発行前に、DSP FLAG 0 ポートが "H" にならない	" □ DSP □ □ ERROR □ 0 2 □ "
	DSP データリード時、WRITE="L" としても ACK="H" とならない	" □ DSP □ □ ERROR □ 0 3 □ "
	DSP データリード時、REQ="L" としても ACK="L" とならない	" □ DSP □ □ ERROR □ 0 4 □ "
	DSP データライト時、WRITE="H" としても ACK="H" とならない	" □ DSP □ □ ERROR □ 0 5 □ "
	DSP データライト時、REQ="L" としても ACK="L" とにならない	" □ DSP □ □ ERROR □ 0 6 □ "
	DSP スペシャルコードブート時、DSP リセットを実行しても DSP FLAG 0 ポートが "H" にならない	" □ DSP □ □ ERROR □ 1 1 □ "
	DSP スペシャルリードコマンド発行前に、DSP FLAG 0 ポートが "H" にならない	" □ DSP □ □ ERROR □ 1 2 □ "
	DSP バージョンリード前に、DSP FLAG 0 ポートが "H" にならない	" □ DSP □ □ ERROR □ 1 3 □ "
④ SUB/DSP 共に OK		(表示せずにバージョン表示を行う)

PROCEDURE FOR CHECKING ERRORS

Displaying the protection history

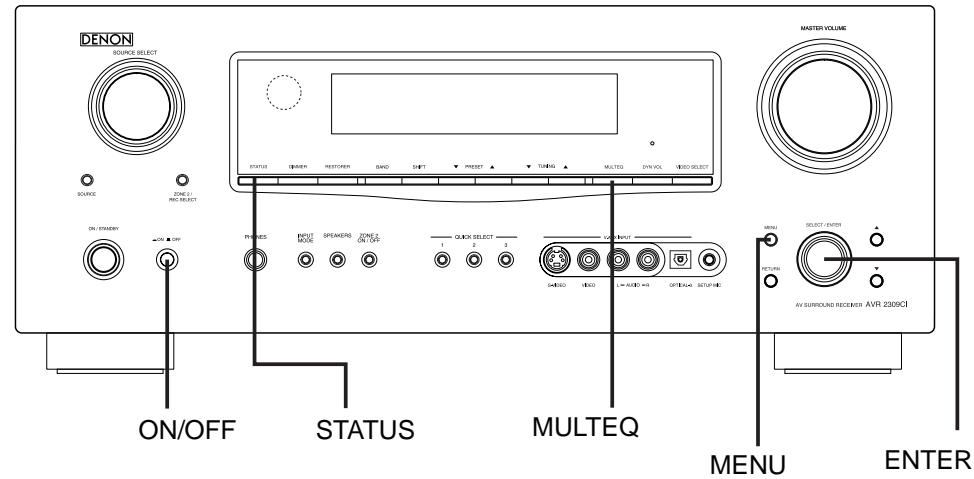
1. Operation specifications

ERROR MODE(displaying the protection history)
When started up, the error information is displayed.

Starting up:

With the "MENU" and "MULTEQ" buttons pressed, press the "ON/OFF" button to turn the power on. The error (protection history display) mode is set.

Now, press the "STATUS" button to turn on the FL display.



2. About the display on the FL display

When the "STATUS" button is pressed after setting the error (protection history display) mode, a history like the one shown below is displayed, depending on the conditions.

(1) Normally (when there has been no protection incident)

Upper	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
Lower	:	N	O	P	R	O	T	E	C	T					

(2) For ASO/DC (when the last protection incident was ASO or DC protection)

Upper	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
Lower	:	A	S	O	/	D	C								

(3) For THERMAL (when the last protection incident was THERMAL protection)

Upper	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
Lower	:	T	H	E	R	M	A	L							

When the "STATUS" button is pressed again after the above protection history is displayed, the normal display reappears.

ERROR 確認方法

PROTECTION 履歴表示

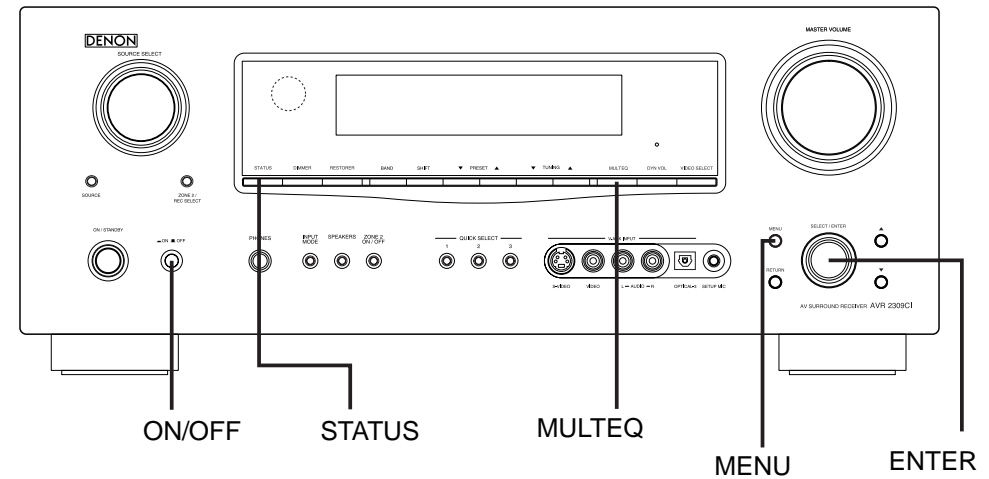
1. 動作仕様

ERROR (PROTECTION 履歴表示) モード：
起動状態にて、ERROR 情報を表示します。

起動方法：

“MENU” と “MULTEQ” の2つのボタンを押した状態で、ON/OFF ボタンを押して電源を入れると、ERROR (PROTECTION 履歴表示) モードとなります。

その後、“STATUS” ボタンを押すと FL Display 表示されます。



2. FL Display 表示に関して

ERROR (PROTECTION 履歴表示) モード “後に、“STATUS” ボタンを押すと、状況によって以下のような履歴を表示します。

(1) 正常時 (今まで PROTECTION が発生していない場合)

上段	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
下段	:	N	O	P	R	O	T	E	C	T					

(2) ASO/DC 時 (最後の PROTECTION が ASO または DC PROTECTION の場合)

上段	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
下段	:	A	S	O	/	D	C								

(3) THERMAL 時 (最後の PROTECTION が THERMAL PROTECTION の場合)

上段	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
下段	:	T	H	E	R	M	A	L							

上記の PROTECTION 履歴表示後に、再度 “STATUS” ボタンを押すと、定常表示となります。

3. Clearing the protection history

There are two ways to clear the protection history, as described below.

- (1) Start up the error (protection display) mode, display the error, then press and hold in the "ENTER" button for 3 seconds.

Upper	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
Lower	:	T	H	E	R	M	A	L							

↓ Press and hold in the "ENTER" button for 3 seconds

Upper	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
Lower					C	L	E	A	R						

↓ The above is displayed and the protection history is cleared.

Upper	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
Lower	:	N	O		P	R	O	T	E	C	T				

- (2) Initialize.

※ If you want to save a backup, use the method in 3.(1) above.

Warning indication by the STANDBY LED

If the power is turned off when a protection incident has been detected, the STANDBY LED (red) flashes as follows as warning according to the conditions in which the protection incident occurred.

- (1) ASO/DC PROTECTION : Flashes in cycles of 0.5 seconds (0.25 seconds lit, 0.25 seconds off)
- (2) THERMAL PROTECTION : Flashes in cycles of 2 seconds (1 second lit, 1 second off)

3. PROTECTION 履歴のクリア方法

PROTECTION 履歴をクリアするには、下記2通りの方法があります。

- (1) ERROR(PROTECTION 表示) モードを起動して ERROR を表示状態にして、“ENTER” ボタンを3秒間長押しする。

上段	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
下段	:	T	H	E	R	M	A	L							

↓ ENTER ボタンを3秒間長押しする。

上段	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
下段					C	L	E	A	R						

↓ 上記が表示され、PROTECTION 履歴がクリアされます。

上段	P	R	O	T	E	C	T		H	I	S	T	O	R	Y
下段	:	N	O		P	R	O	T	E	C	T				

- (2). イニシャライズを行う。

※バックアップを保持したい場合は、3.(1)の方法で行なってください。

STANDBY LED による警告表示

PROTECTION を検出した状態で POWER OFF した場合、PROTECTION の発生状況によって、STANDBY LED(赤色)が下記のように点滅し、警告表示します。

- (1) ASO/DC PROTECTION : 0.5 秒周期の点滅 (0.25 秒点灯 / 0.25 秒消灯)
- (2) THERMAL PROTECTION : 2 秒周期の点滅 (1 秒点灯 / 1 秒消灯)

ADJUSTMENT

Audio Section

Idling Current (8U-110030-1)

Required measurement equipment: DC Voltmeter

Preparation

- (1) Avoid direct blow from an air conditioner or an electric fan, and adjust the unit at normal room temperature 15°C ~ 30°C (59°F ~ 86°F).
- (2) Presetting
POWER (Power source switch) OFF
SPEAKER (Speaker terminal) No
load
(Do not connect speaker, dummy resistor, etc.)

Adjustment

- (1) Remove top cover and set VR401, VR402, VR403, VR404, VR405, VR406, VR407, on 8U-110030-1 (Power Amp Unit) at fully counterclockwise (⊖).
- (2) Connect DC Voltmeter to test points (FRONT-Lch: CX063 ③ ④ pin, FRONT-Rch: CX063 ① ② pin, CENTER ch: CX063 ⑤ ⑥ pin, SURROUND-Lch: TP102 ③ ④ pin, SURROUND-Rch: CX082 ① ② pin, SURROUND BACK-Lch: CX082 ⑦ ⑧ pin, SURROUND BACK-Rch: CX082 ⑤ ⑥ pin).
- (3) Connect power cord to AC Line, and turn power switch "ON".
- (4) Presetting.
MASTER VOLUME : "----" counterclockwise (⊖ min.)
MODE : 7CH STEREO
FUNCTION : CD
- (5) Allow 2 minutes, and turn VR401 clockwise (⊕) to adjust the TEST POINT voltage to 2 mV ± 0.3 mV DC.
- (6) After 10 minutes from preset, turn VR401 to set the voltage to 2 mV ± 0.3 mV DC.
- (7) Adjust the Variable Resistors of other channels in the same way.
- (8) After 5 minutes from (6), turn VR401 to set the voltage to 2 mV ± 0.3 mV DC.
- (9) Adjust the Variable Resistors of other channels in the same way.

調整

オーディオセクション

アイドリング電流の調整 (8U-110030-1)

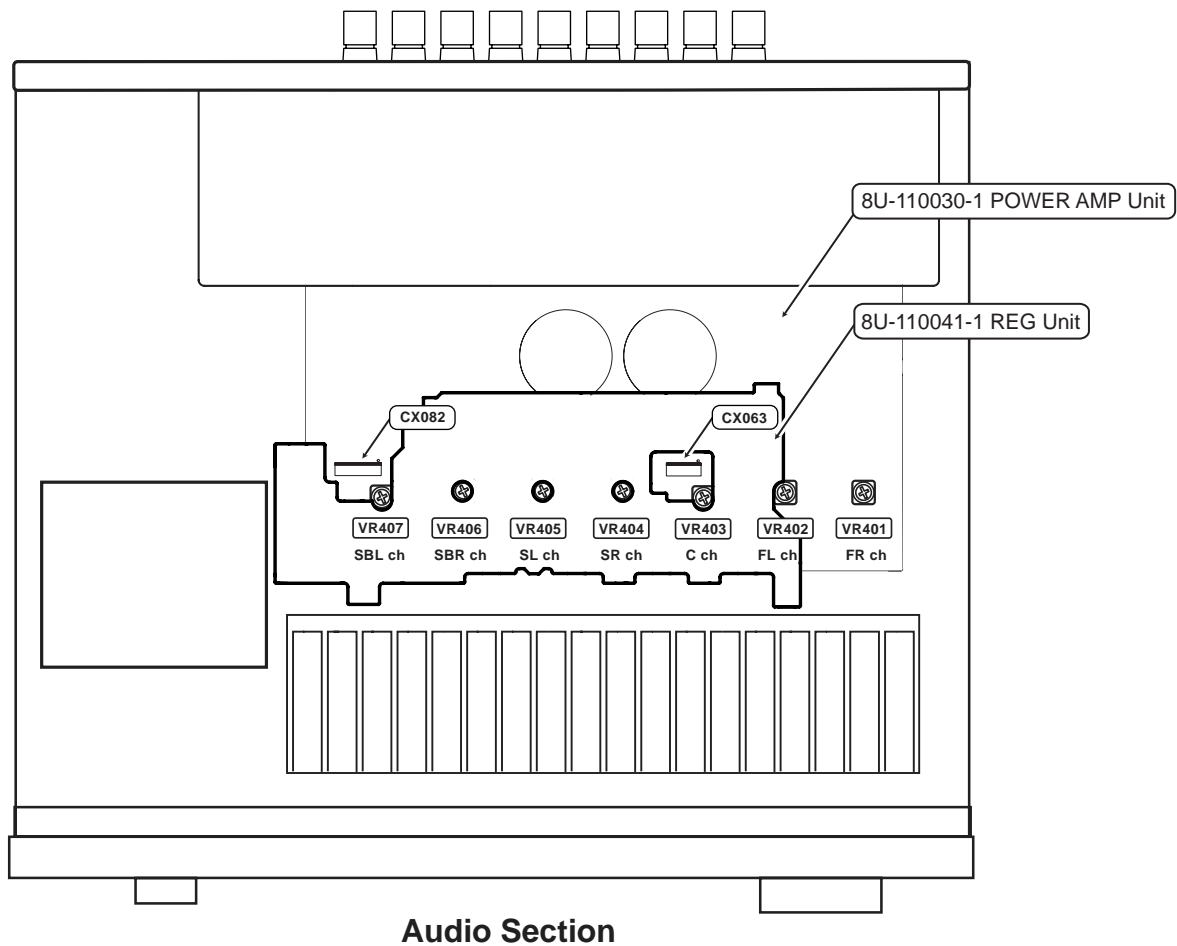
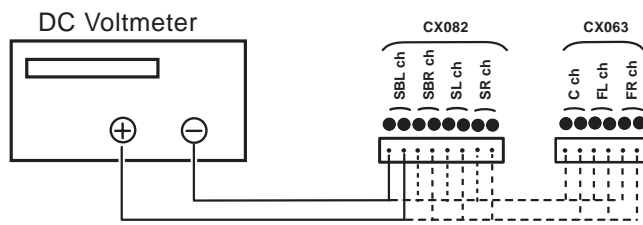
調整に必要な測定器：DC Voltmeter

準備

- (1) セットをクーラ、扇風機のそばなど風通しの良い場所を避け、通常の使用状態に置きます。セットの周囲温度は 15 ~ 30 °C、湿度は常湿とします。
- (2) プリセット
電源スイッチ OFF
スピーカ端子 無負荷
(スピーカ・ダミー抵抗器などを接続しない。)

調整

- (1) 上カバーをはずし、8U-110030-1 (パワーアンプユニット) の VR401、VR402、VR403、VR404、VR405、VR406、VR407 を反時計方向 (⊖) に回し切った状態にセットします。
- (2) テストポイント (FRONT-Lch: CX063 ③ ④ pin、FRONT-Rch: CX063 ① ② pin、CENTER ch: CX063 ⑤ ⑥ pin、SURROUND-Lch: CX082 ③ ④ pin、SURROUND-Rch: CX082 ① ② pin、SURROUND BACK-Lch: CX082 ⑦ ⑧ pin、SURROUND BACK-Rch: CX082 ⑤ ⑥ pin) に DC Voltmeter を接続します。
- (3) 電源コードを AC 電源に接続し、電源スイッチを "ON" にします。
- (4) ON 後、次のようにセットします。
MASTER VOLUME (音量調節つまみ) → 反時計方向 (⊖) に回す、最小の状態にします。
SPEAKER (スピーカ端子) → 無負荷 (スピーカ、ダミー抵抗器などを接続しない。)
MODE : 7CH STEREO
FUNCTION : CD
- (5) 2 分以内に VR401 を時計方向 (⊕) に回しテストポイントの電圧を次のように調整します。
2 mV ± 0.3 mV DC
- (6) 予備調整から 10 分後に VR401 を回し、次のように電圧を設定します。
2 mV ± 0.3 mV DC
- (7) 同じ方法で各チャンネルの可変抵抗を調整します。
- (8) (6) 項設定から 5 分後 VR401 を回し、次のように電圧を設定します。
2 mV ± 0.3 mV DC
- (9) 同じ方法で各チャンネルの可変抵抗を調整します。



Audio Section

The adjustment volume and connection terminal of 8U-110030-1 (POWER AMP Unit)P.W.B. under 8U-110041-1 (REG Unit)P.W.B..

Insert an adjustment driver / connection terminal from an adjustment aperture of 8U-110041-1 (REG Unit)P.W.B..

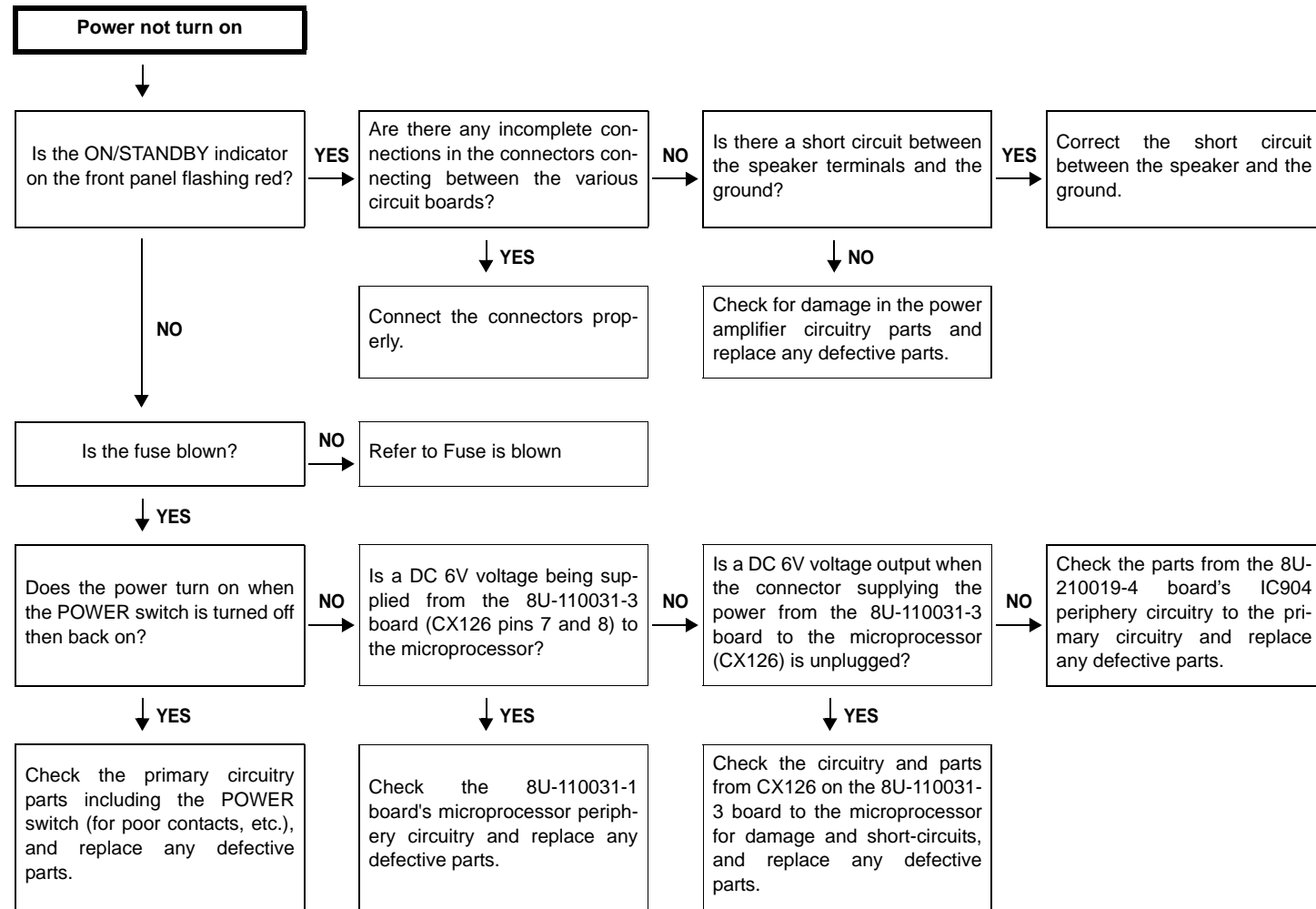
8U-110030-1(POWER AMP Unit) 基板の調整ボリュームと接続端子は 8U-110041-1(REG Unit) 基板の下にあります。

8U-110041-1(REG Unit) 基板の調整孔から調整ドライバー / 接続端子を挿入してください。

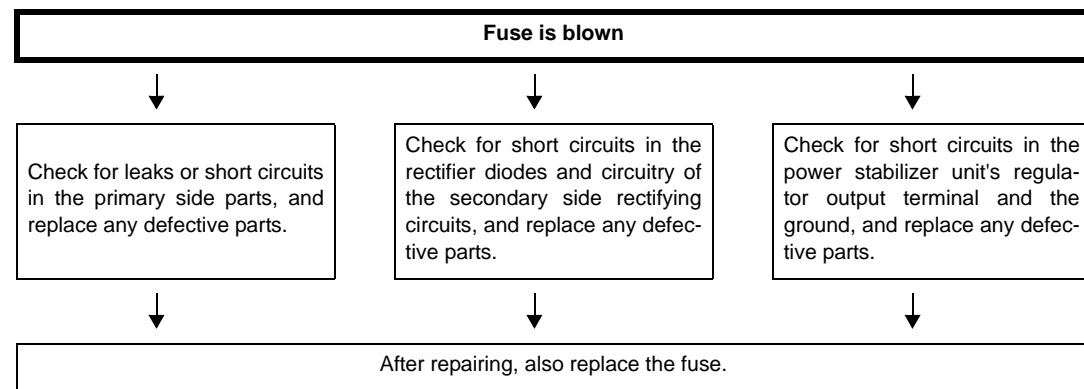
TROUBLE SHOOTING

1. POWER

1.1. Power not turn on



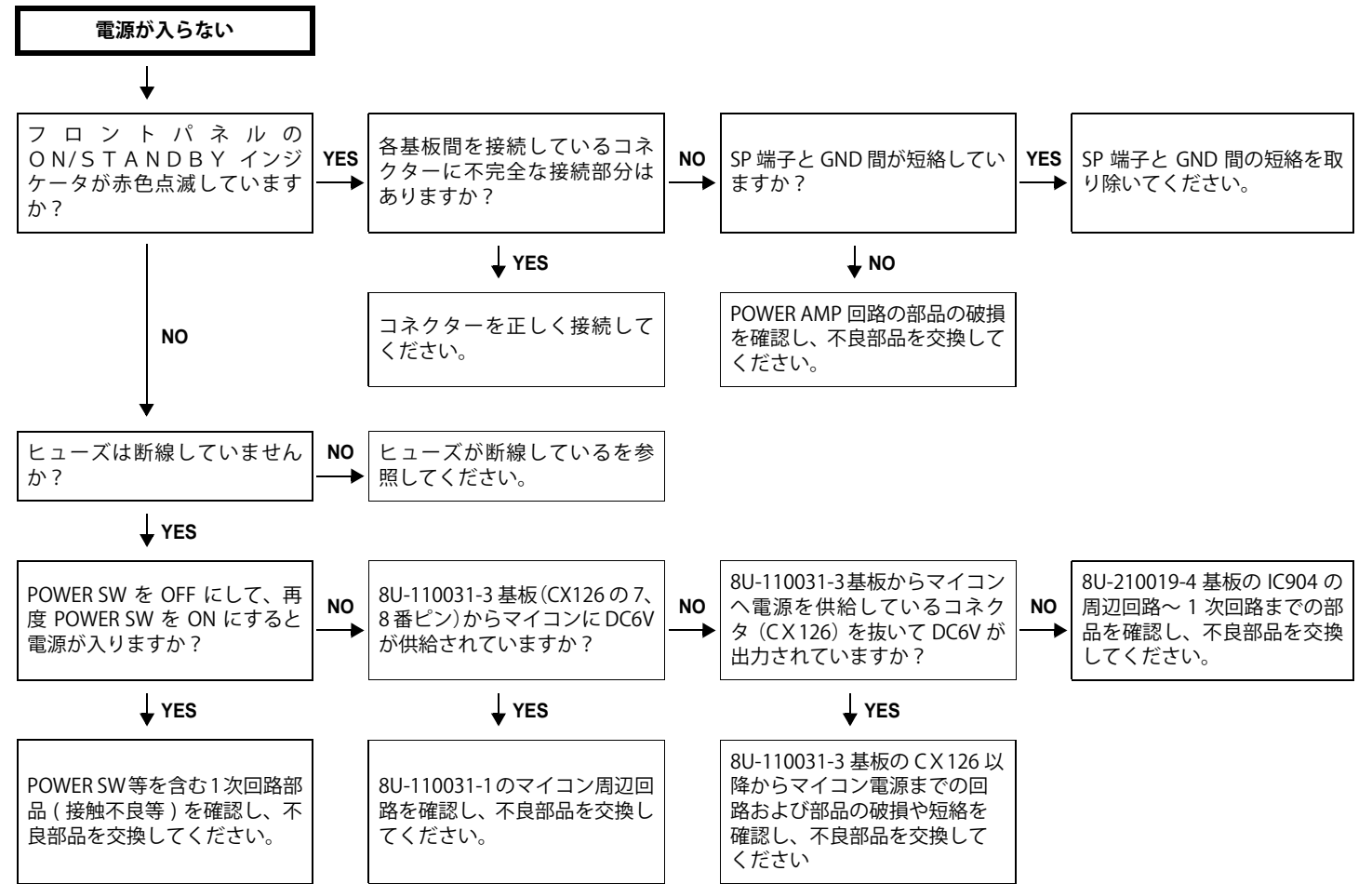
1.2. Fuse is blown



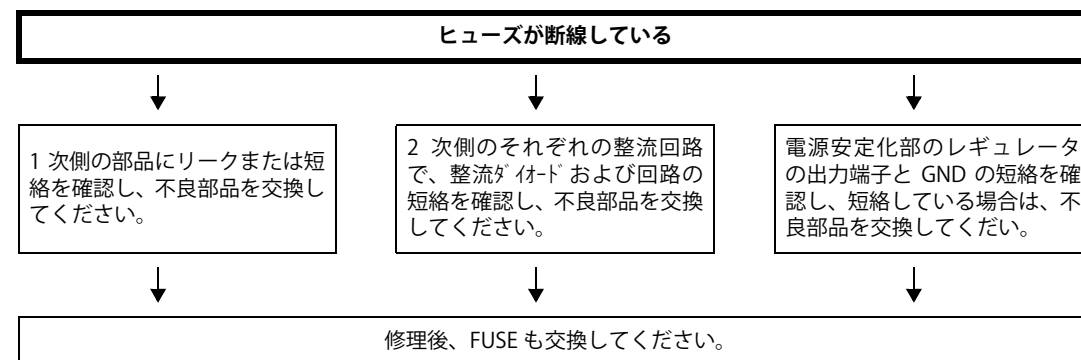
トラブルシューティング

1. 電源

1.1. 電源が入らない

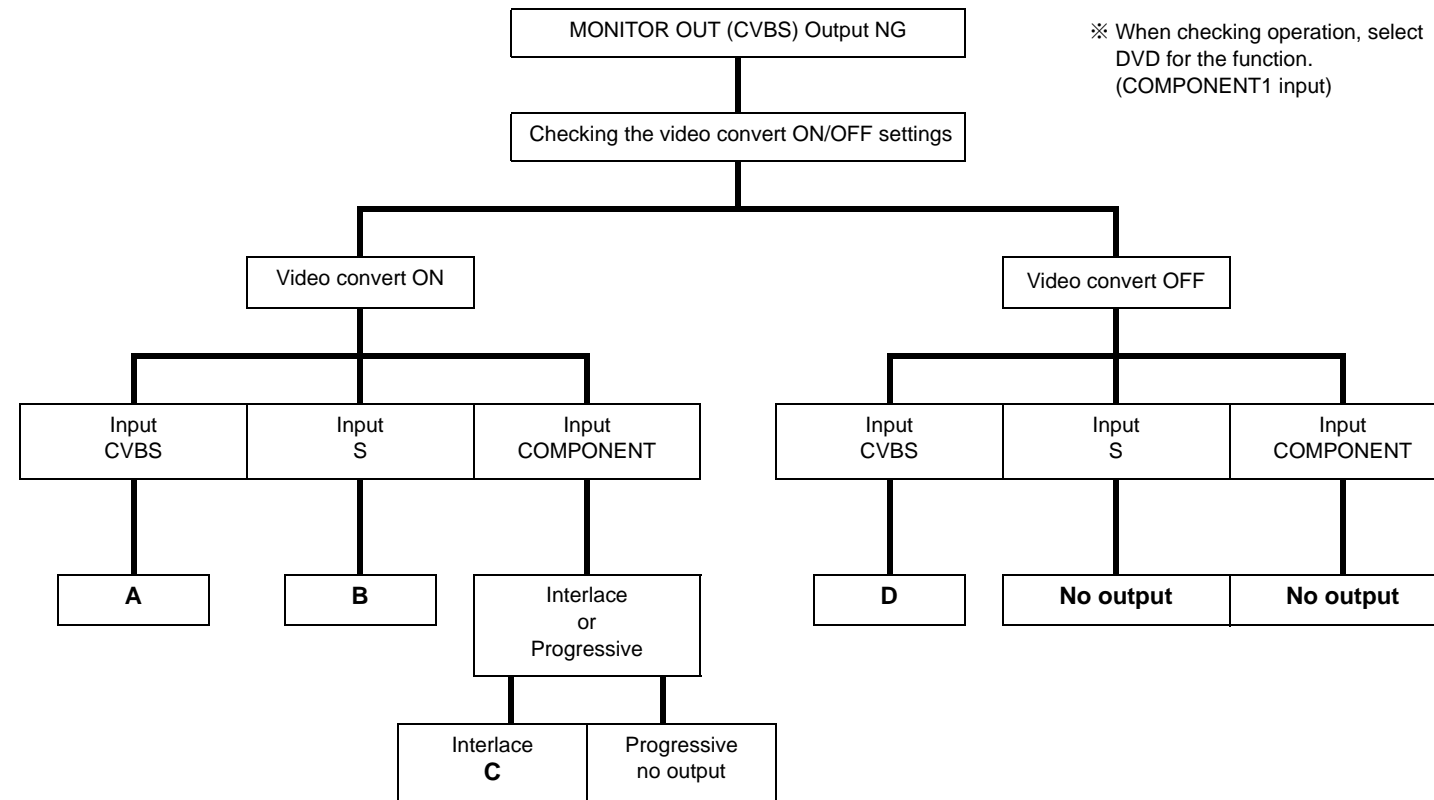


1.2. ヒューズが断線している



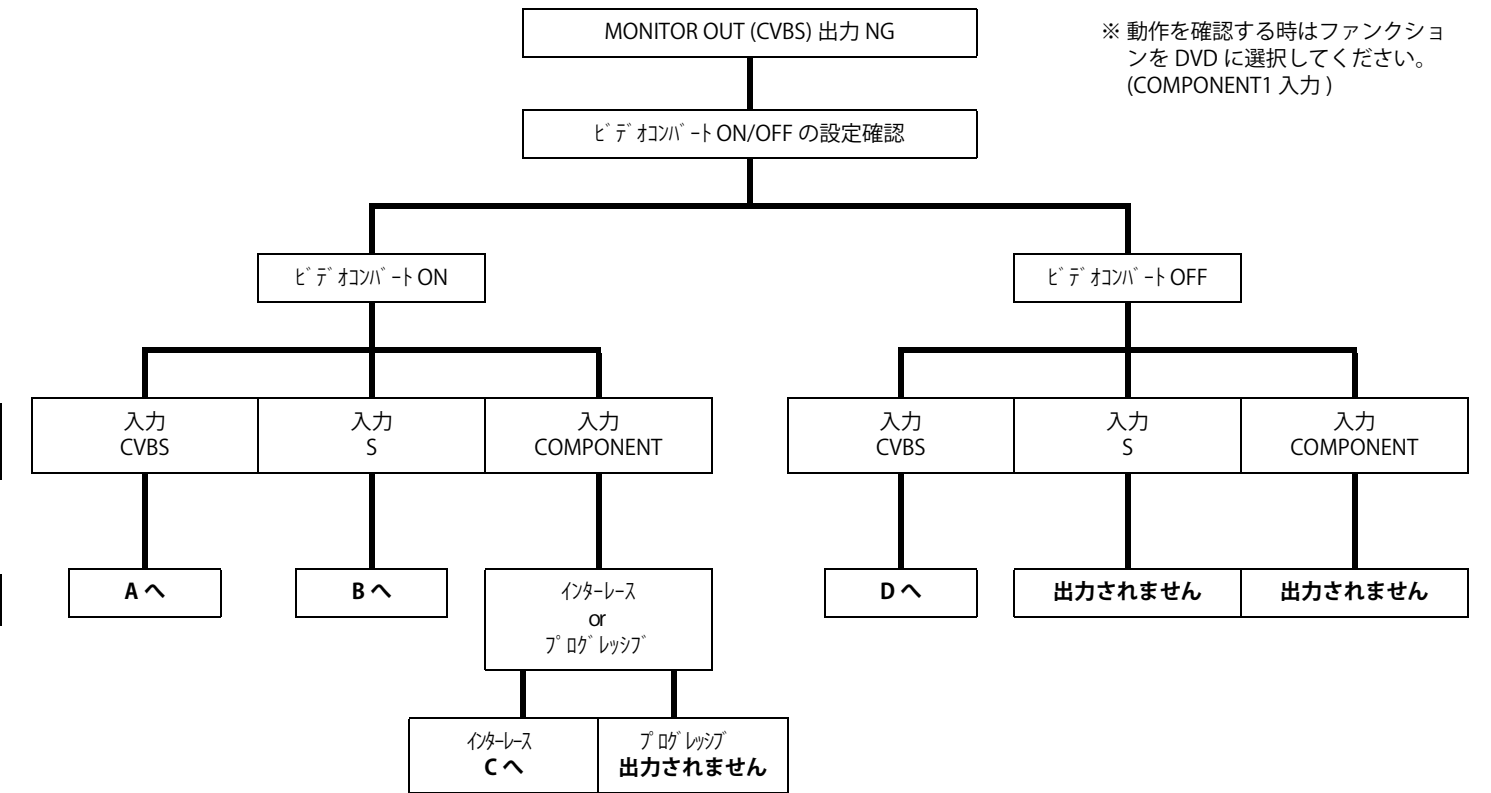
2. Analog video

2.1. MONITOR OUT (CVBS) Output NG

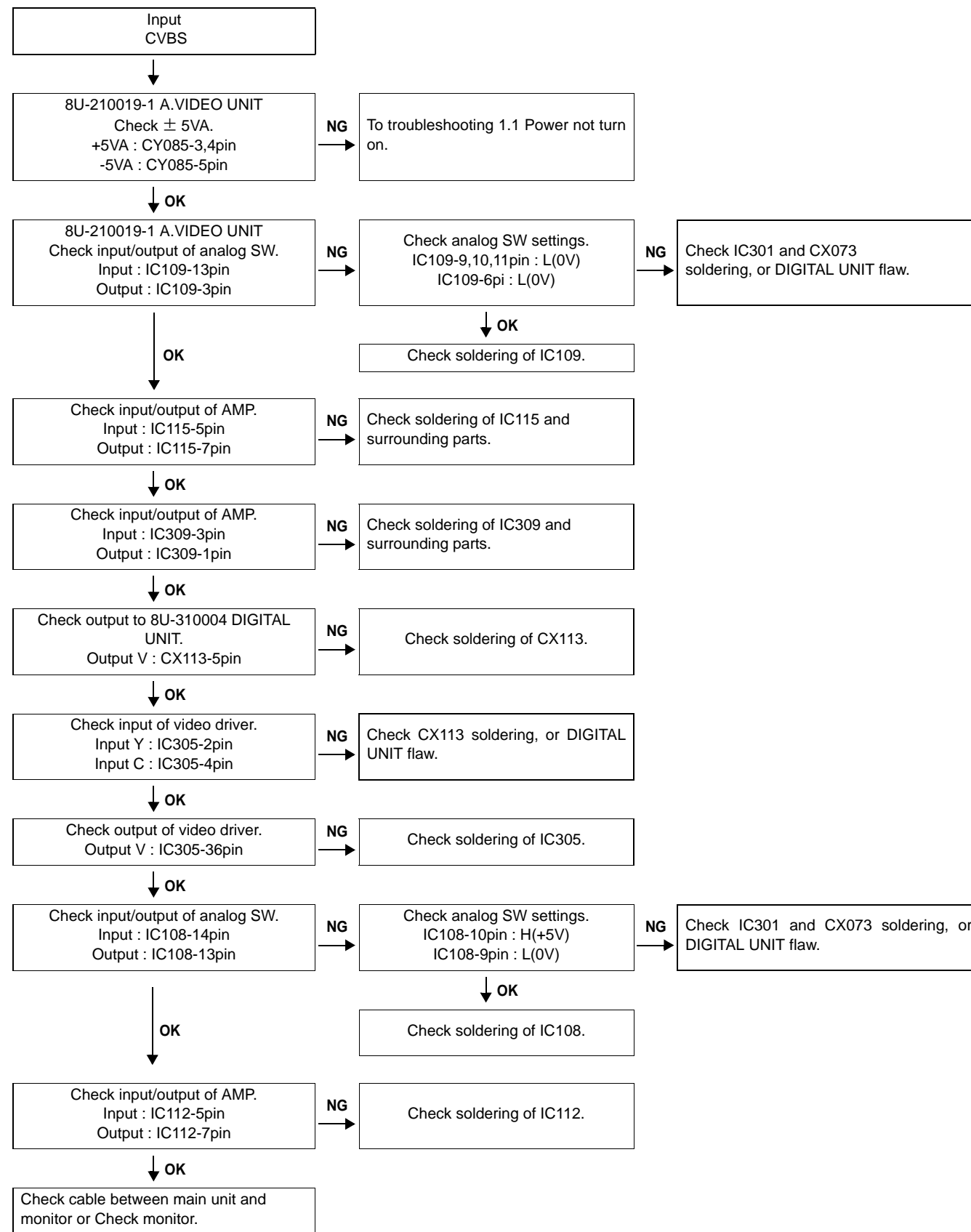


2. アナログビデオ

2.1. MONITOR OUT (CVBS) 出力 NG

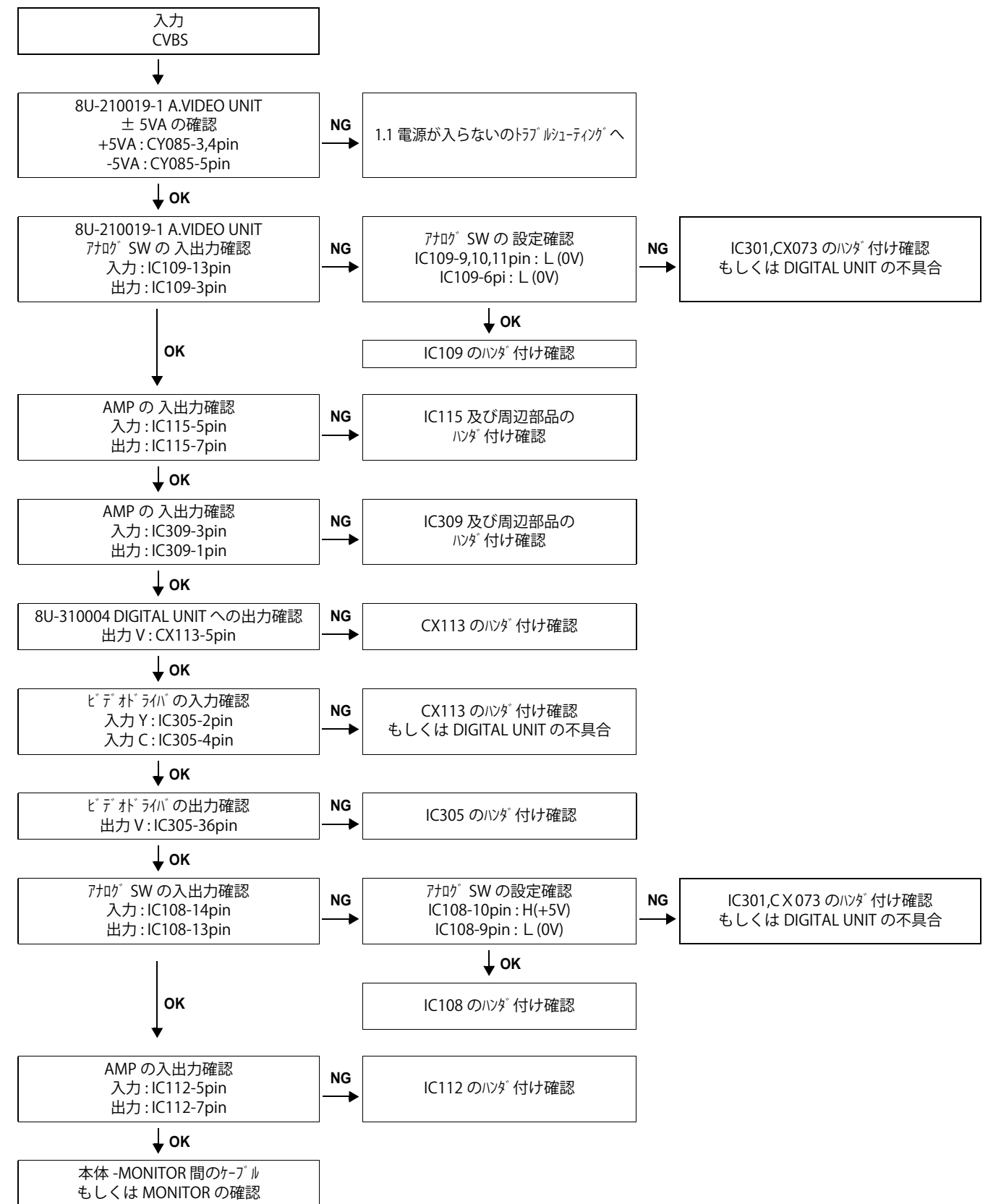


A



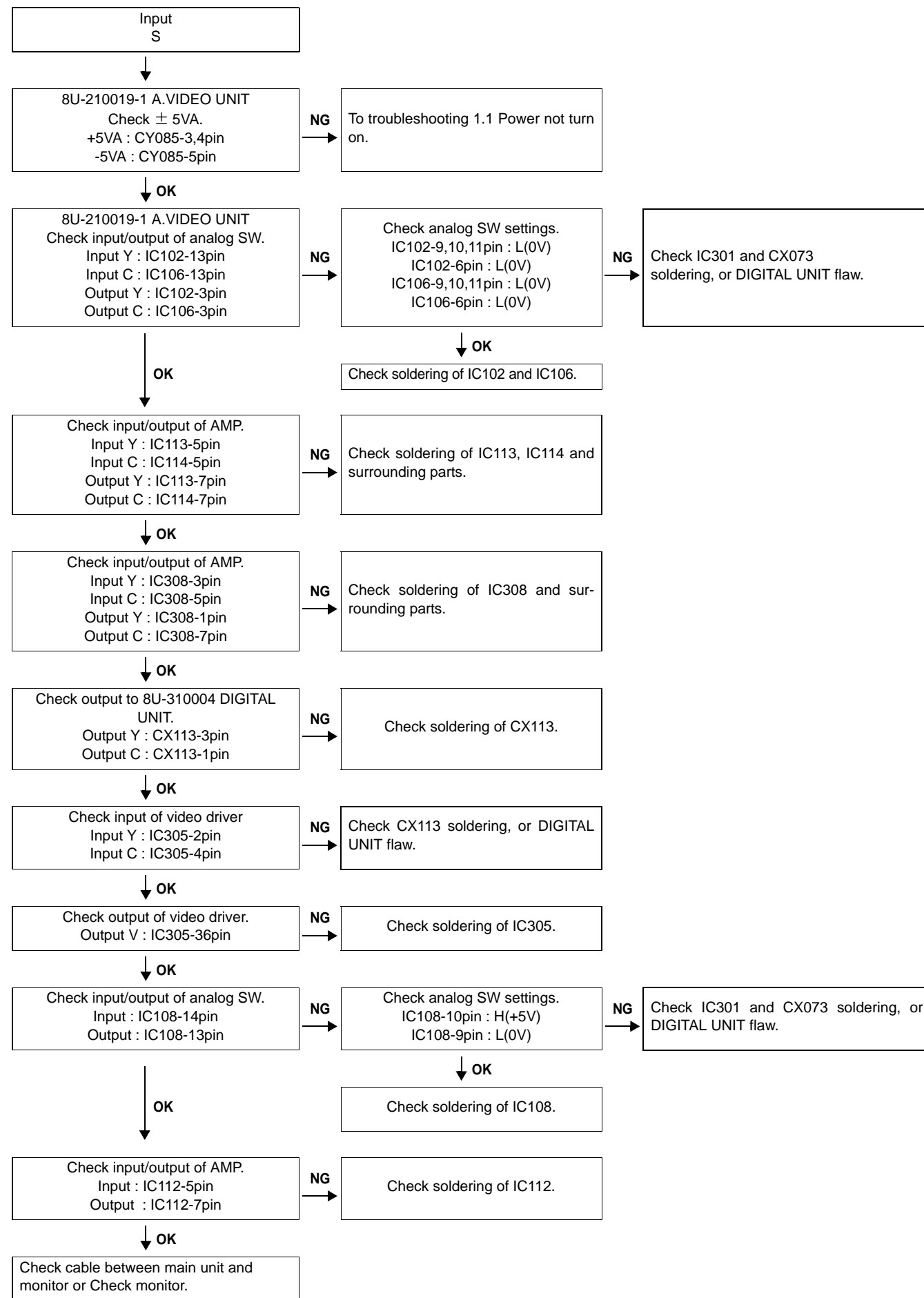
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

A



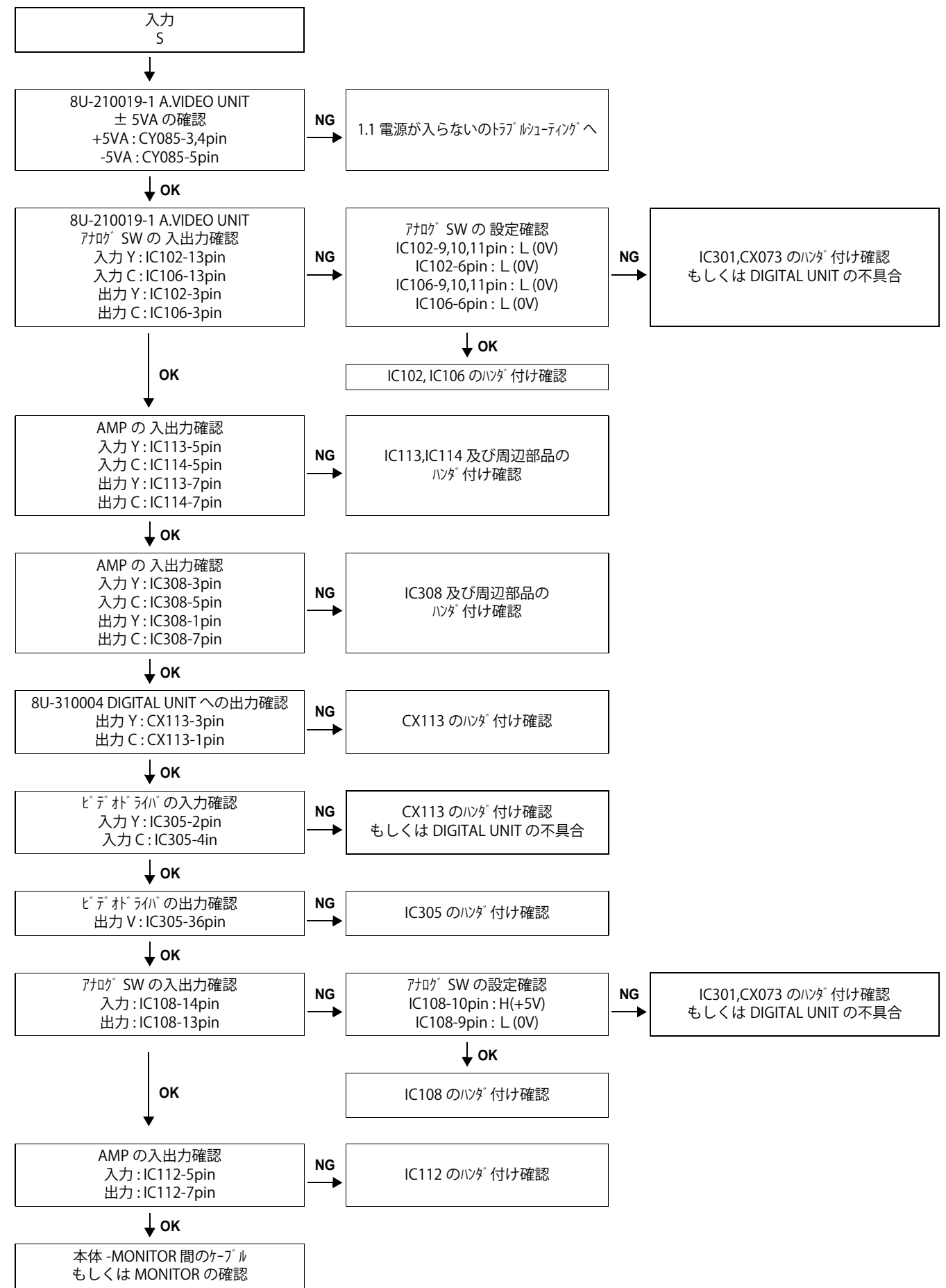
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

B



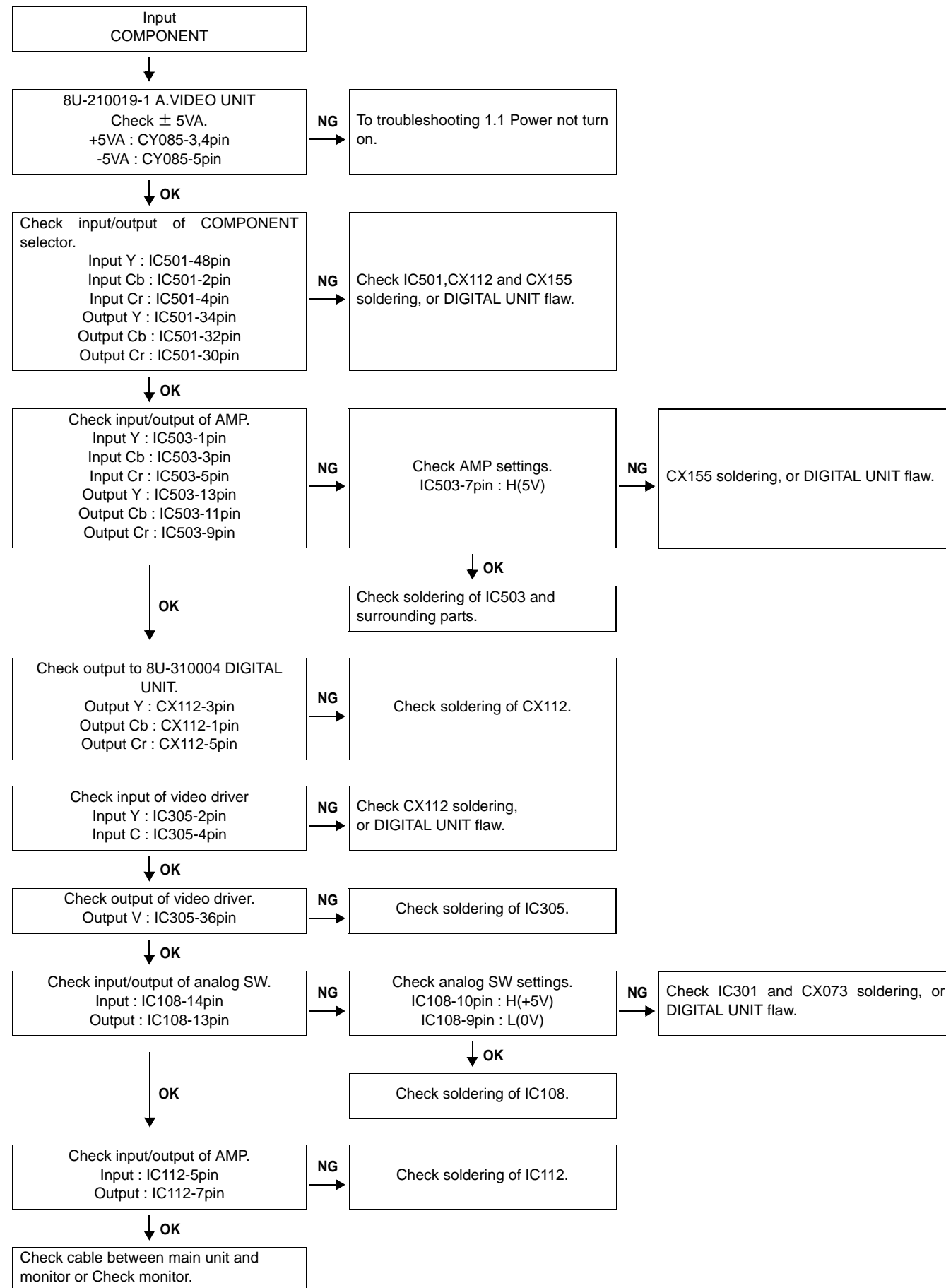
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

B



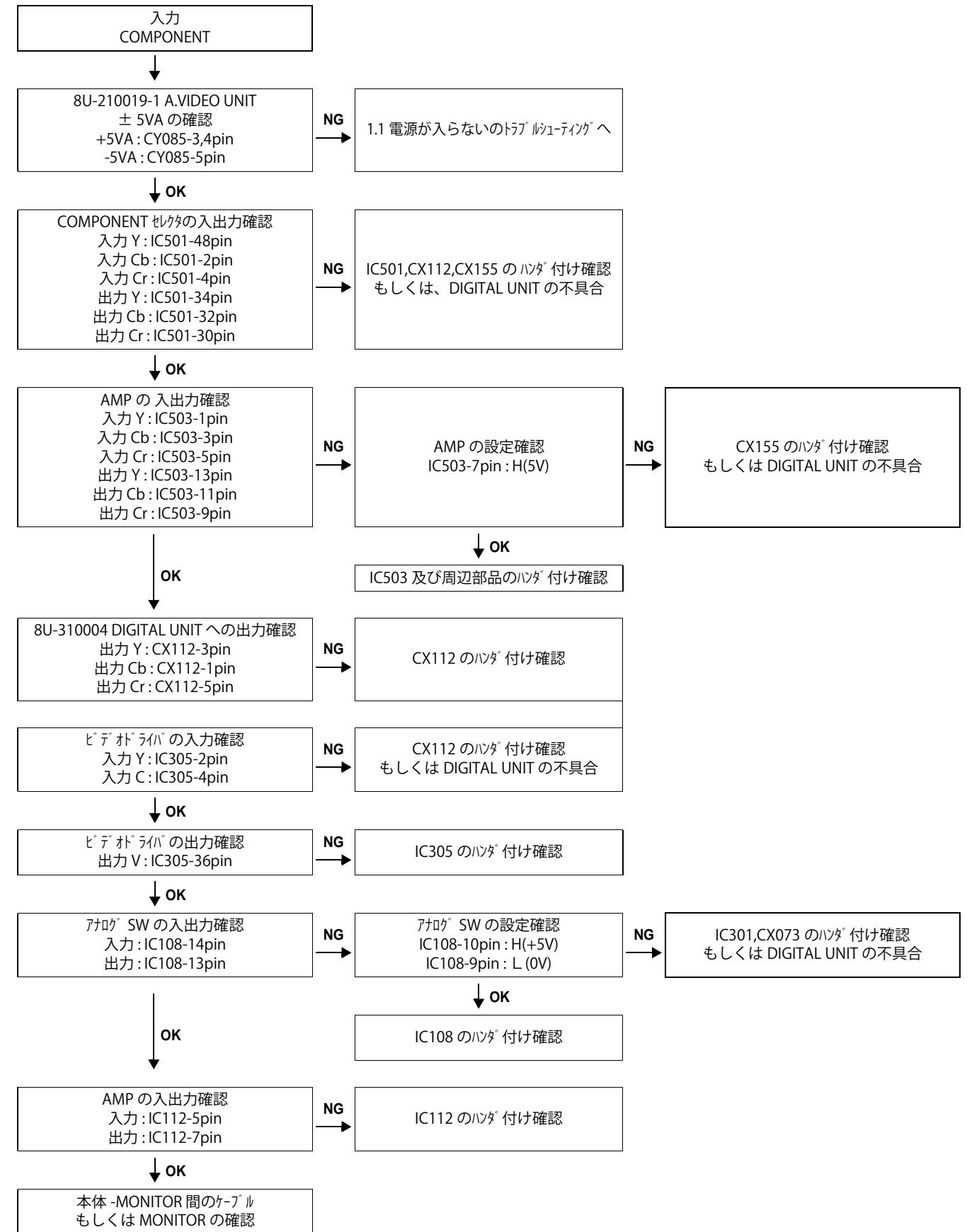
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

C



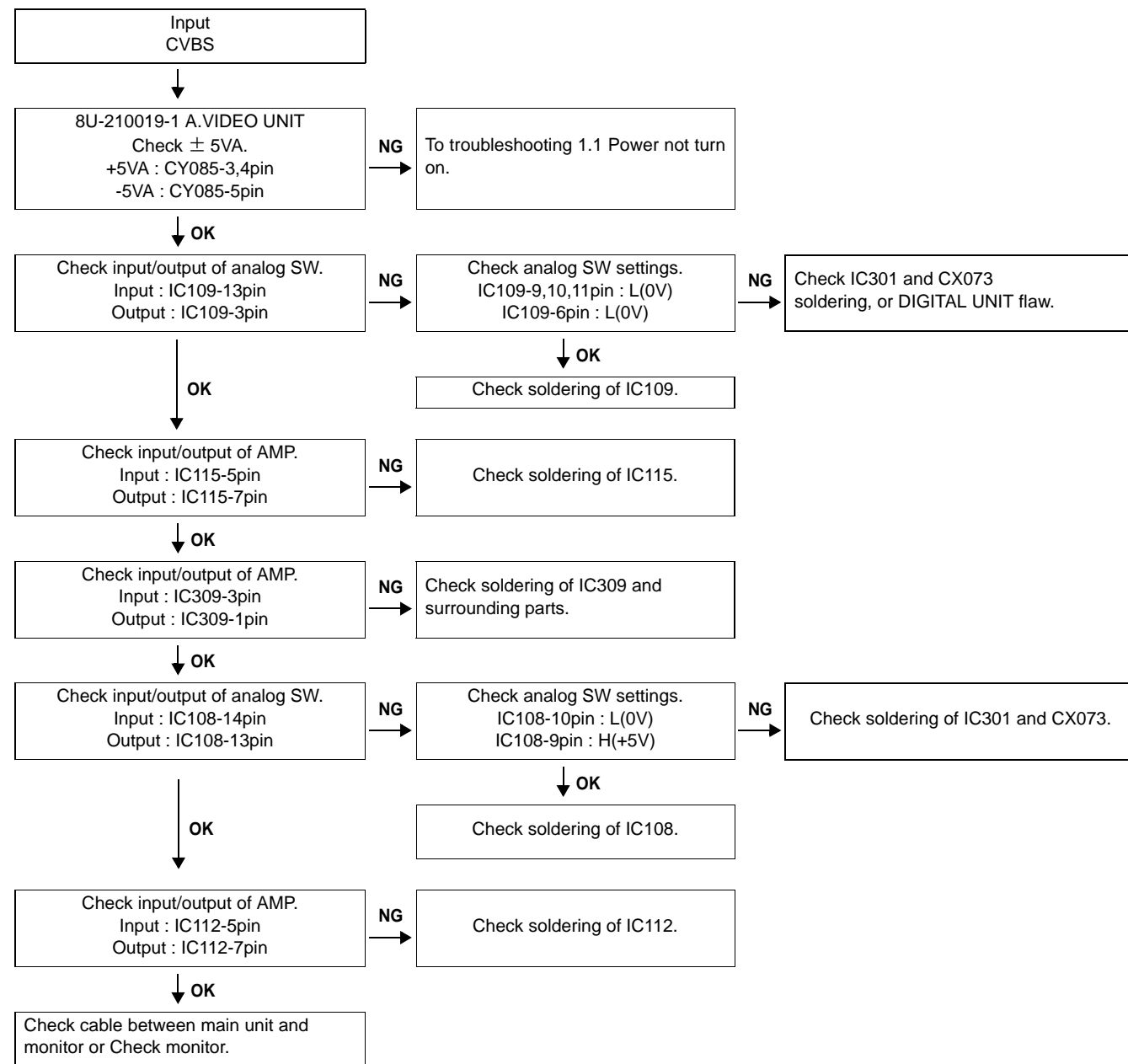
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

C



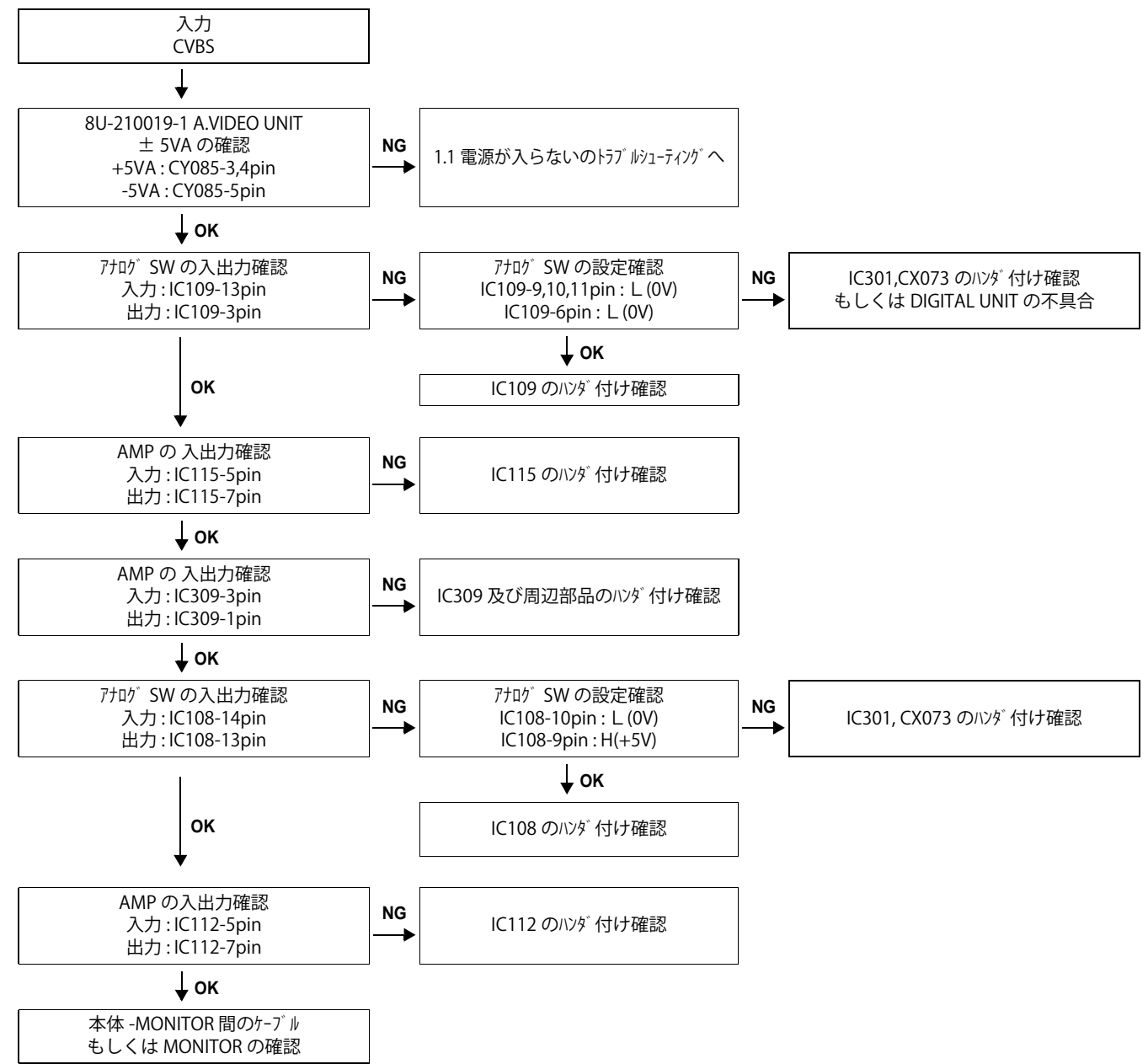
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

D



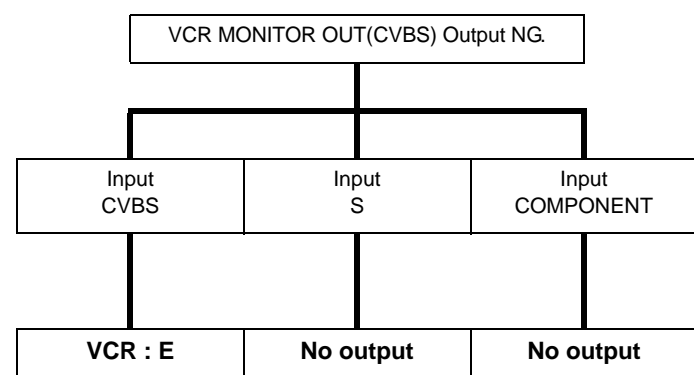
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

D



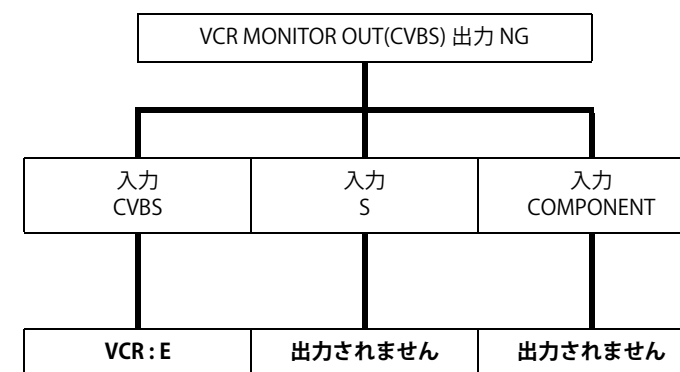
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

2.2. VCR MONITOR OUT(CVBS) Output NG



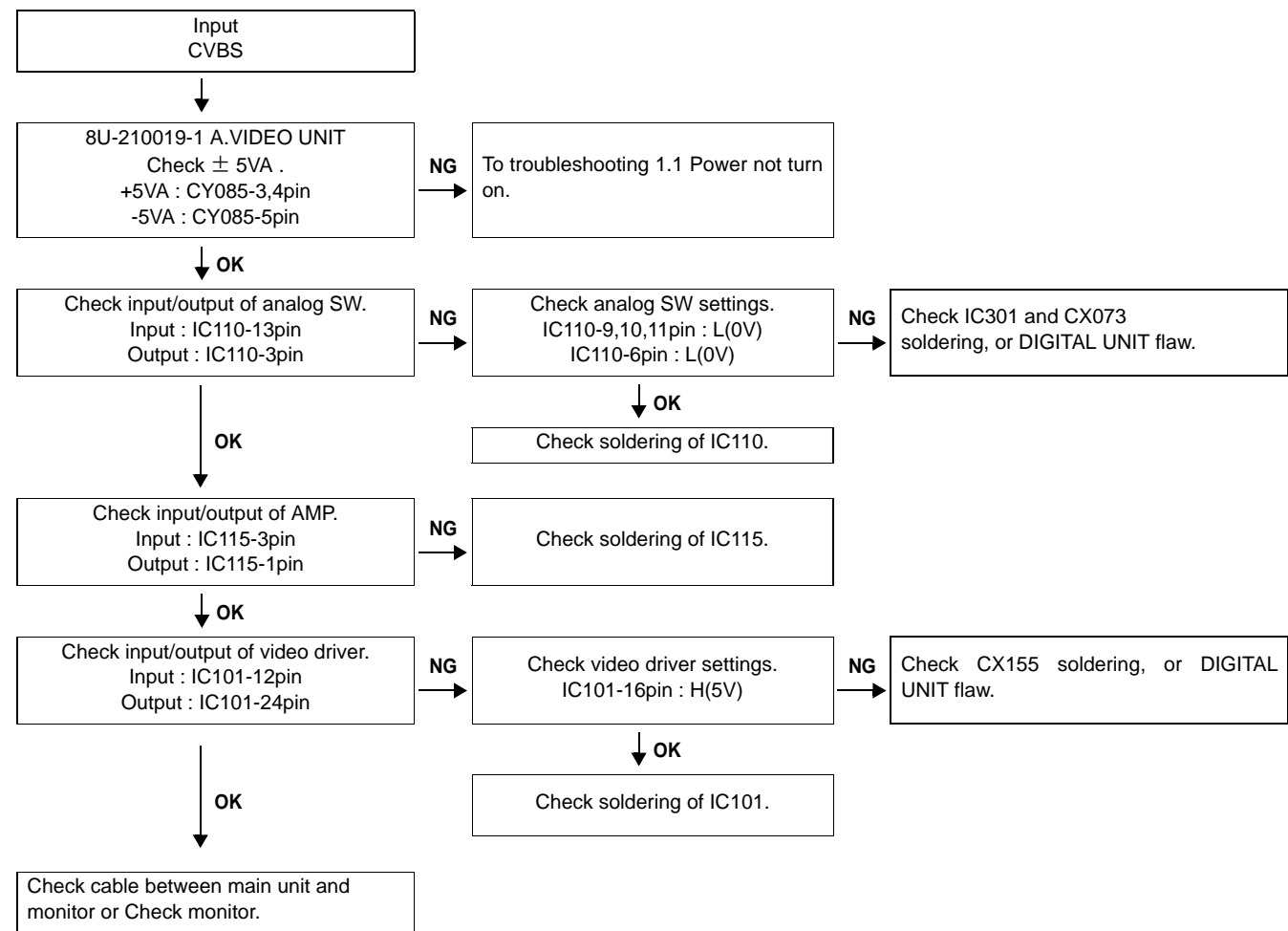
※ When checking operation, select DVD for the function.

2.2. VCR MONITOR OUT(CVBS) 出力 NG



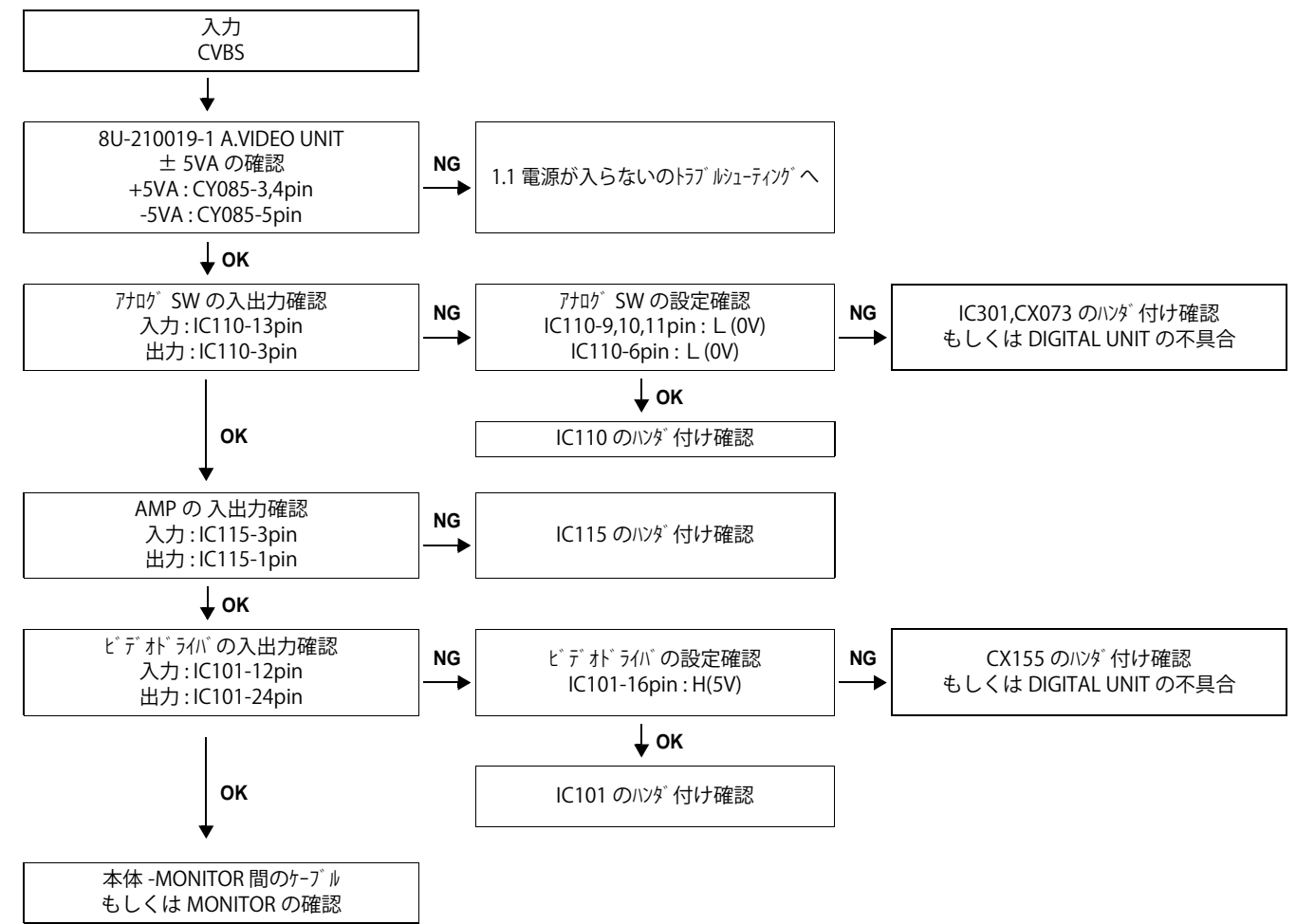
※ 動作を確認する時はファンクションを DVD に選択してください。

E



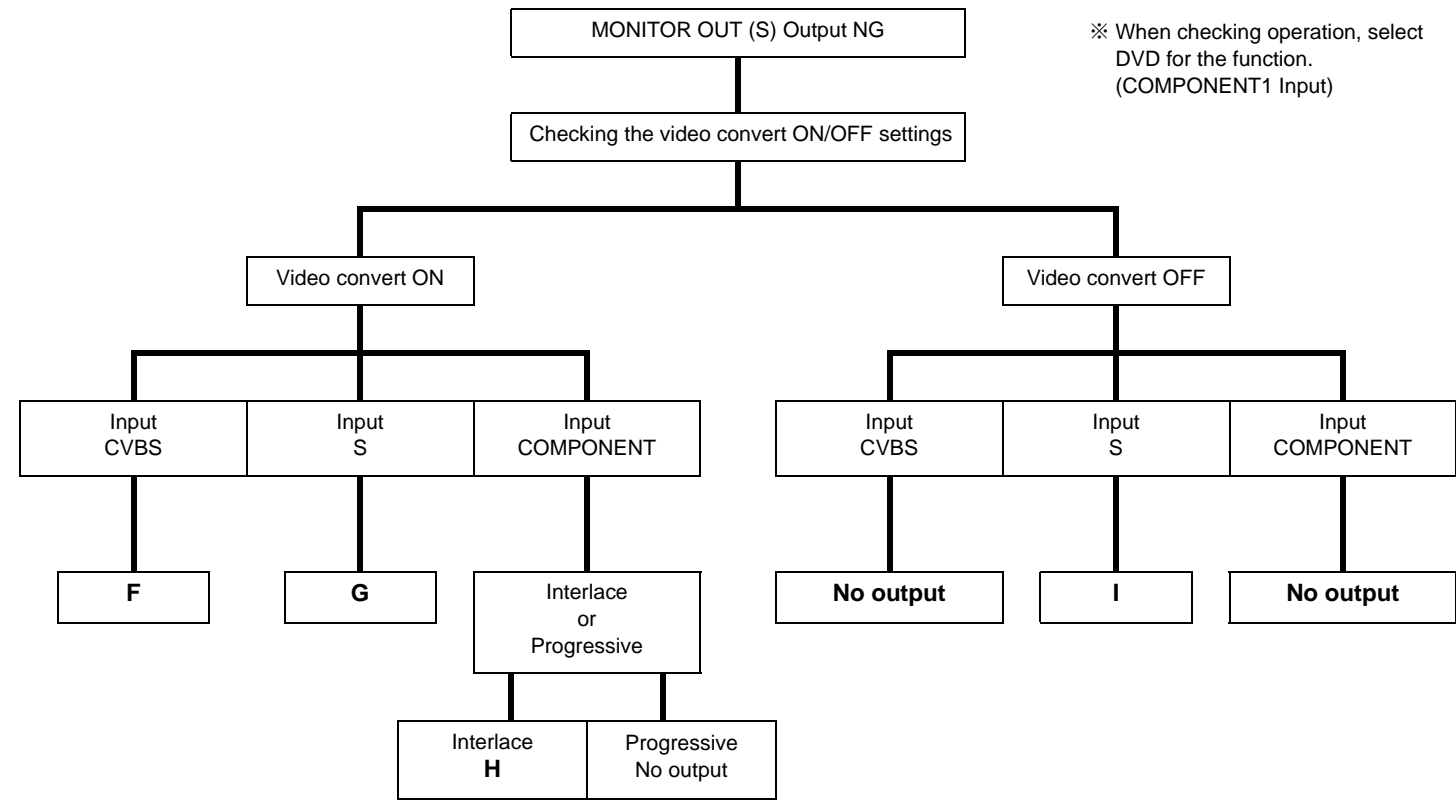
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

E

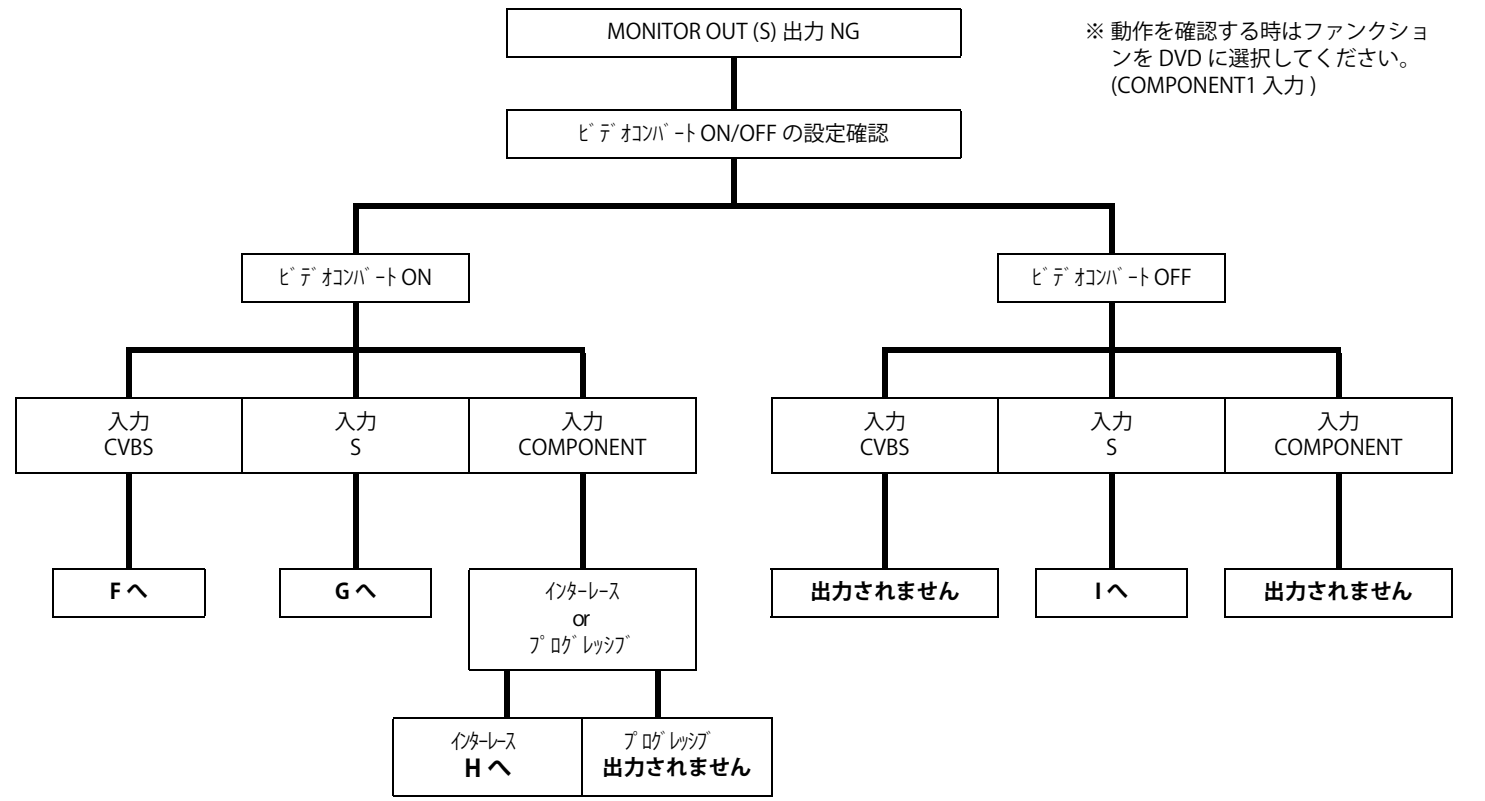


※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

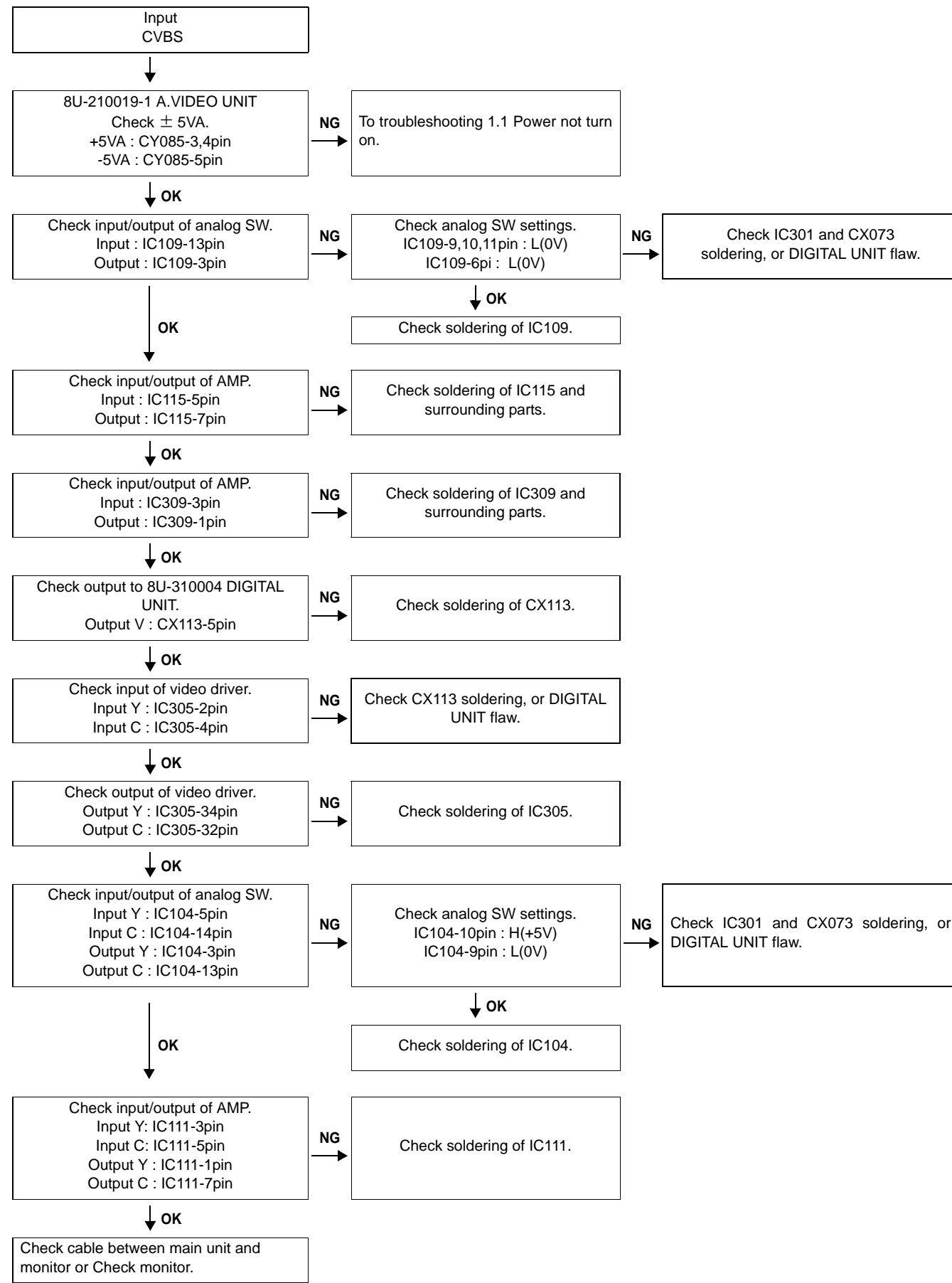
2.3. MONITOR OUT (S) Output NG



2.3. MONITOR OUT (S) 出力 NG

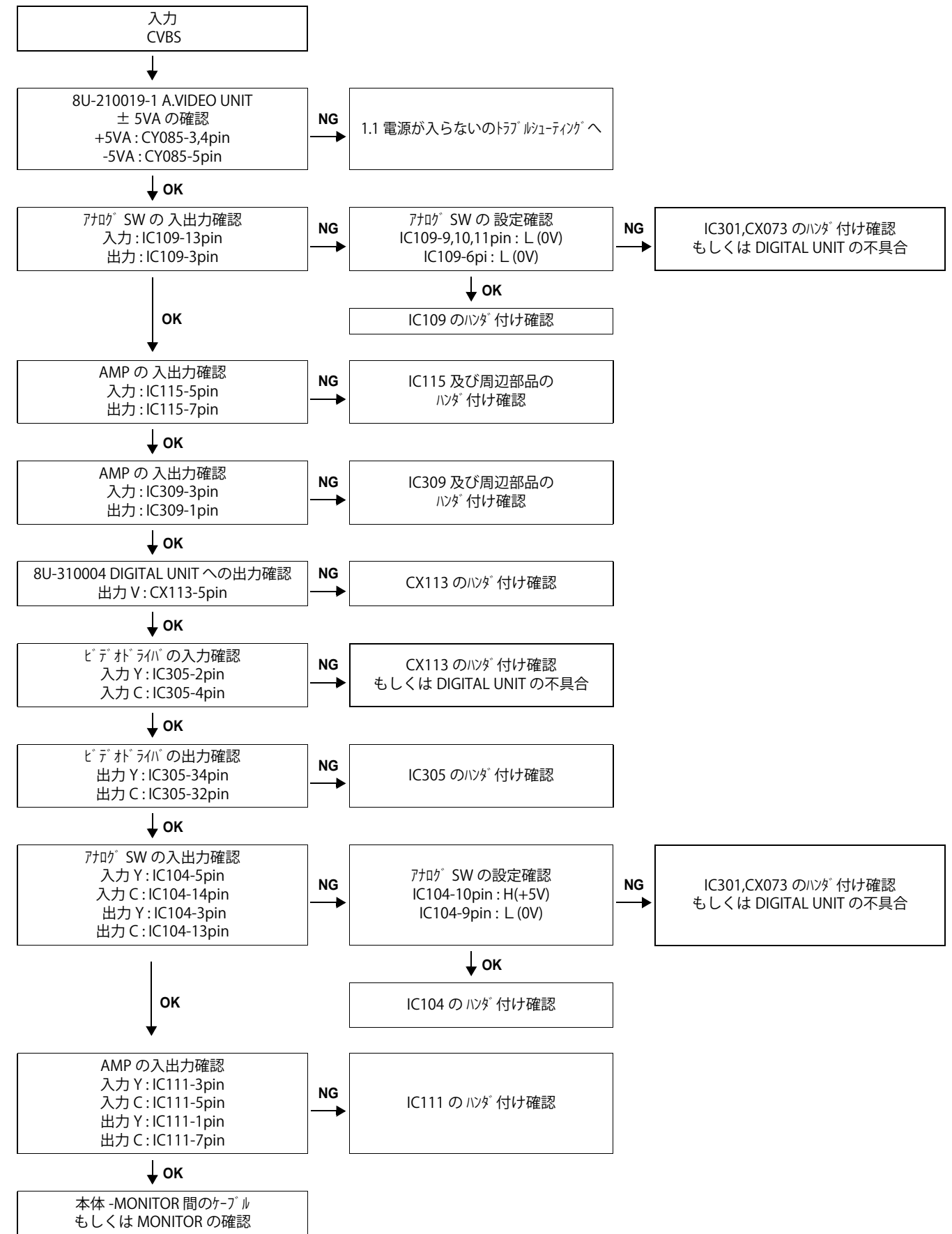


F



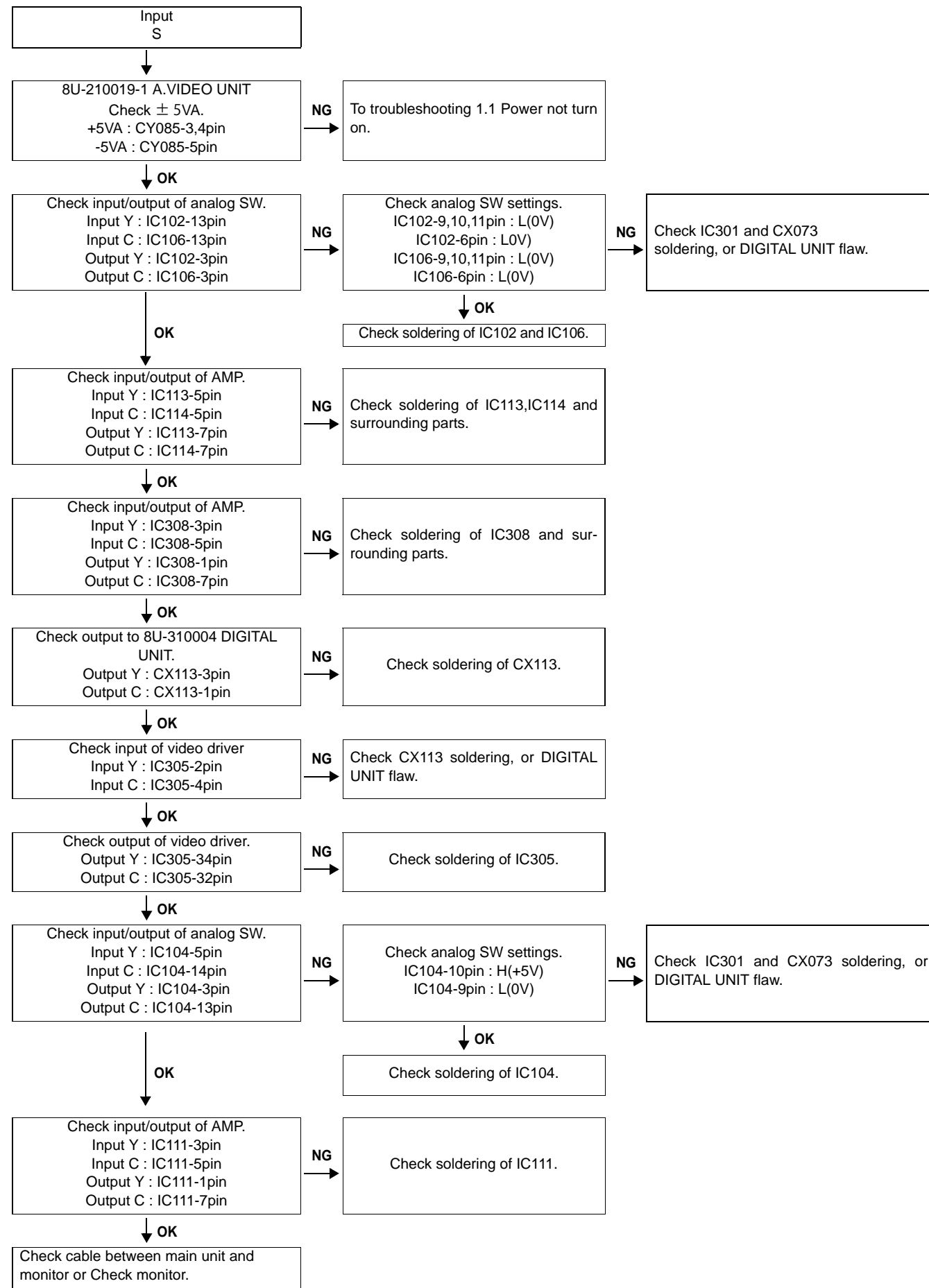
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

F



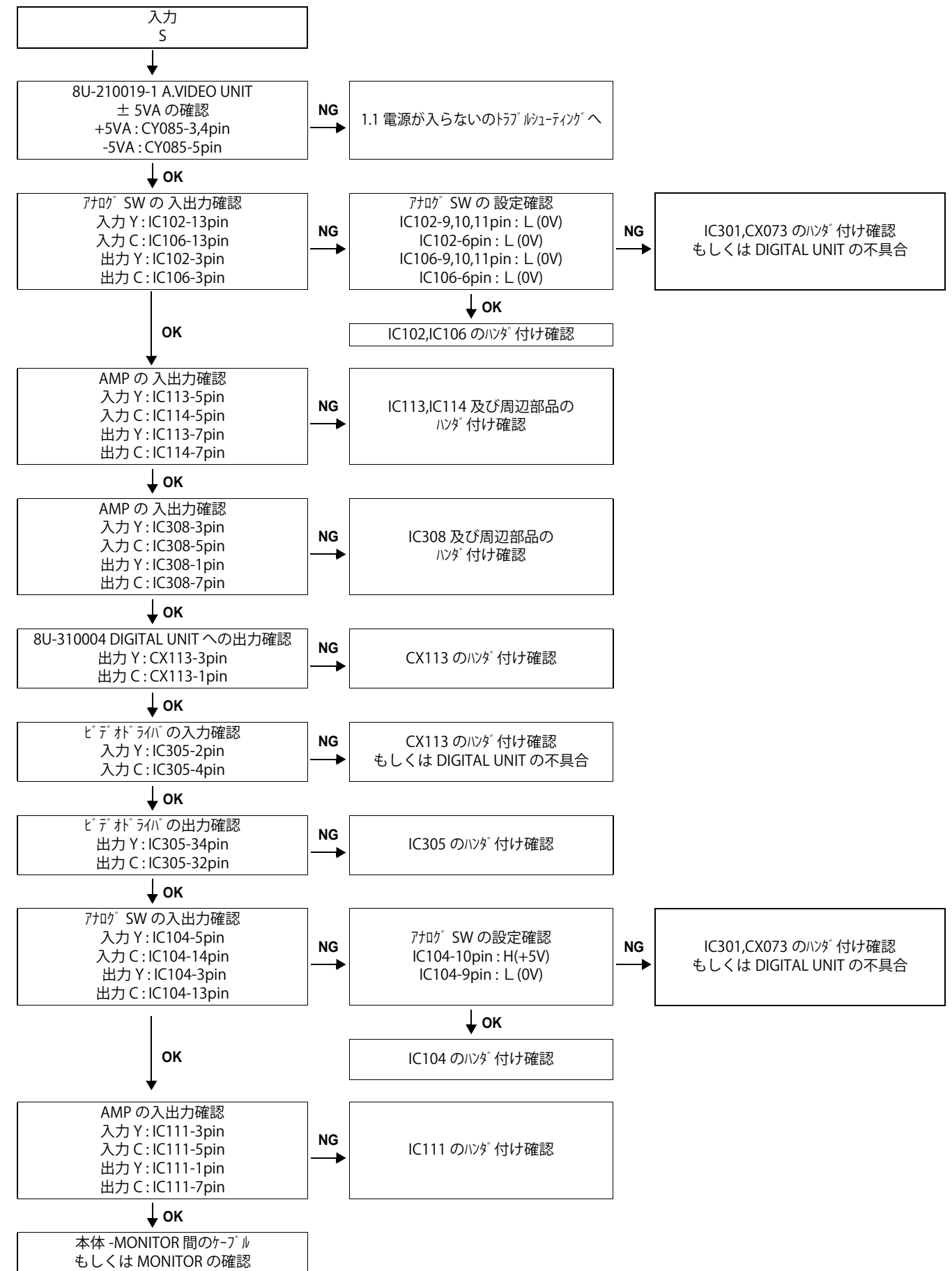
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

G



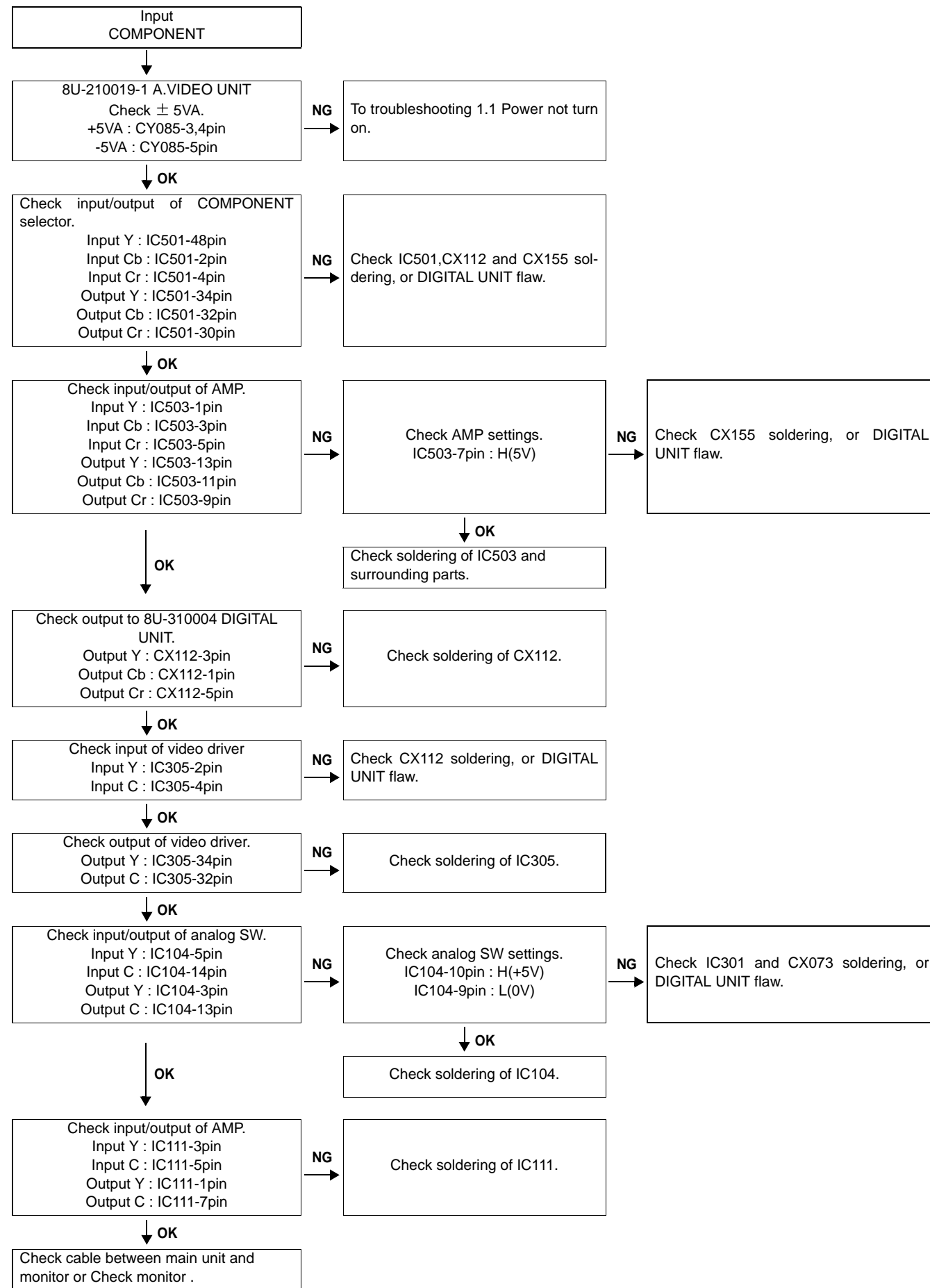
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

G



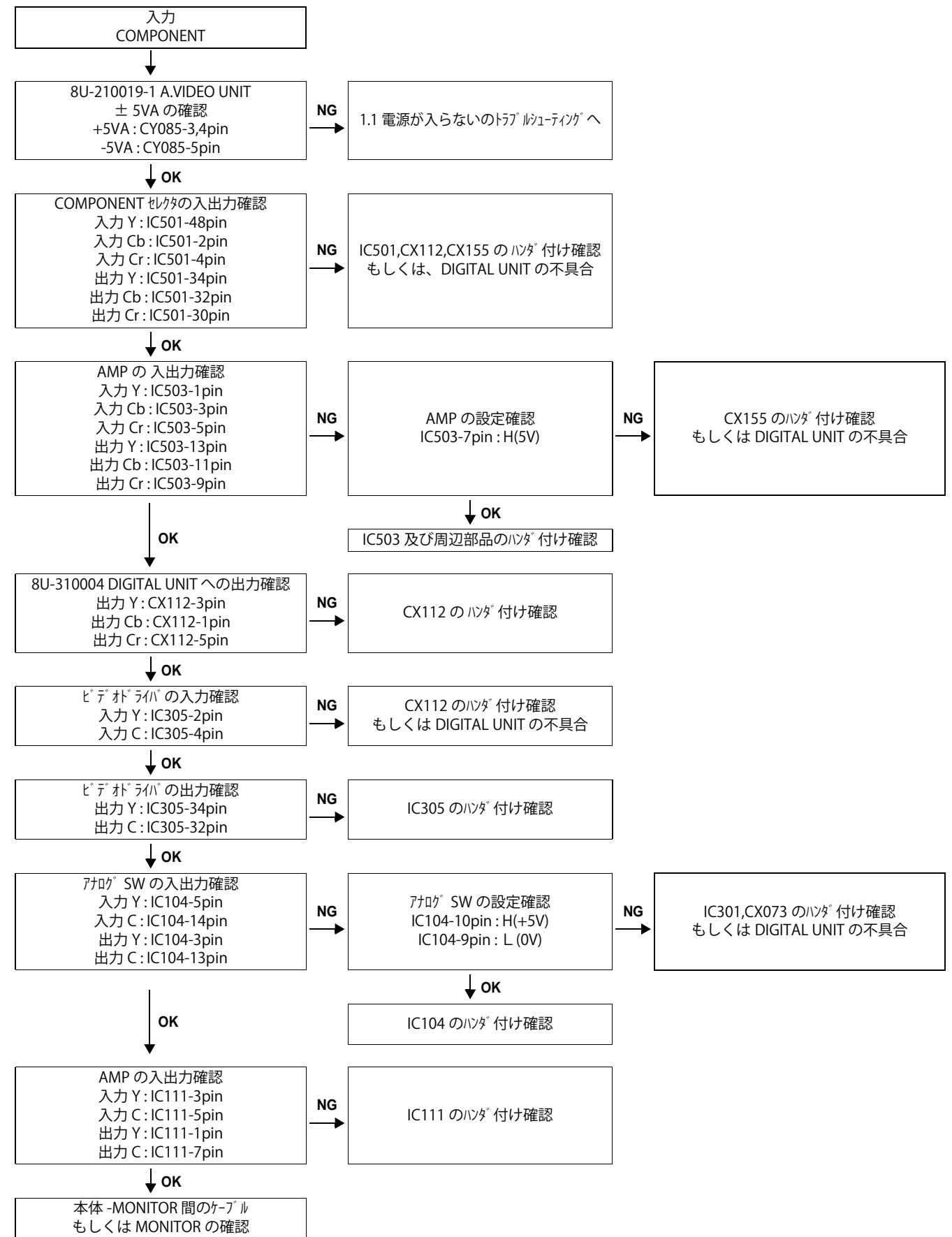
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

H



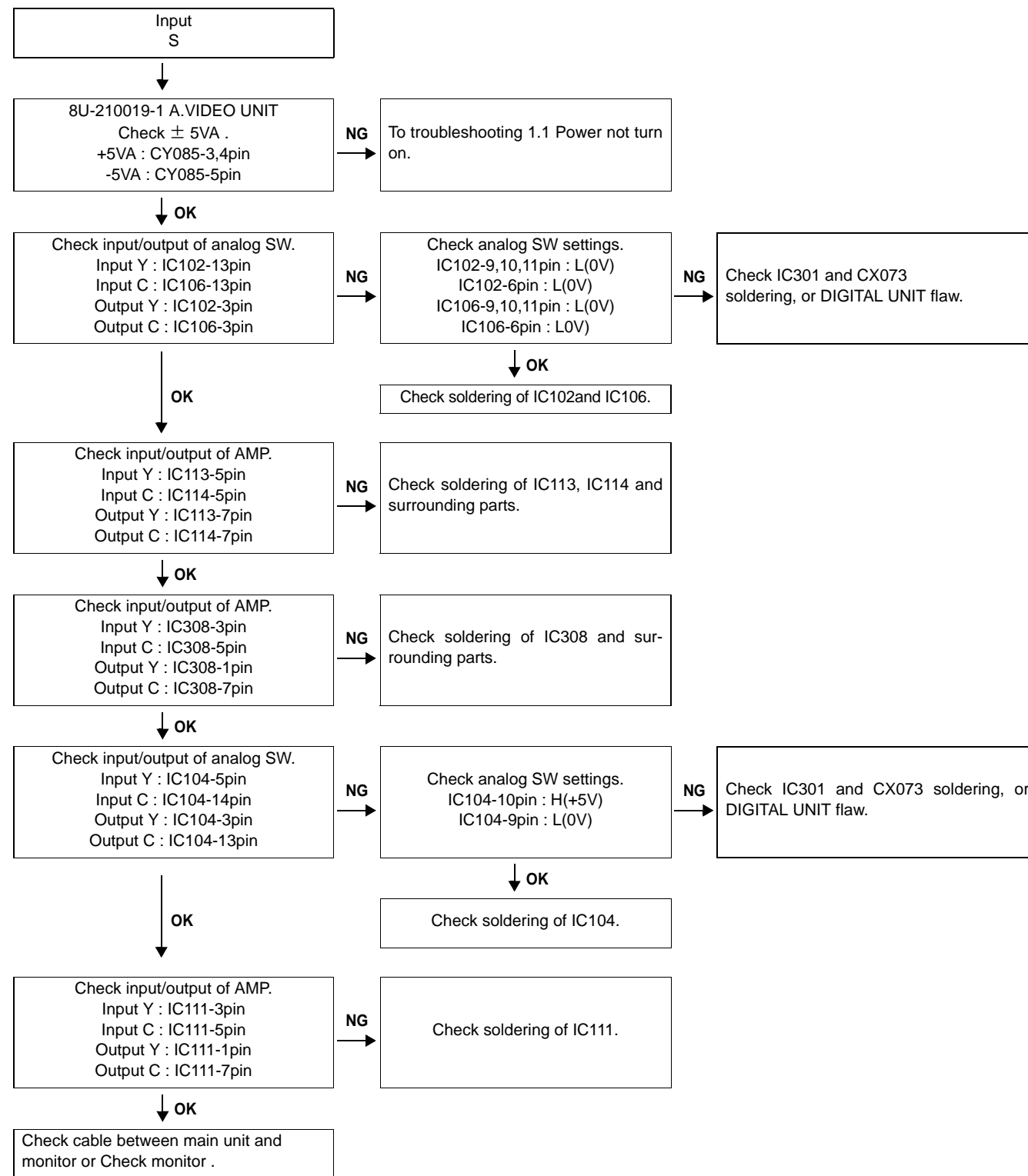
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

H



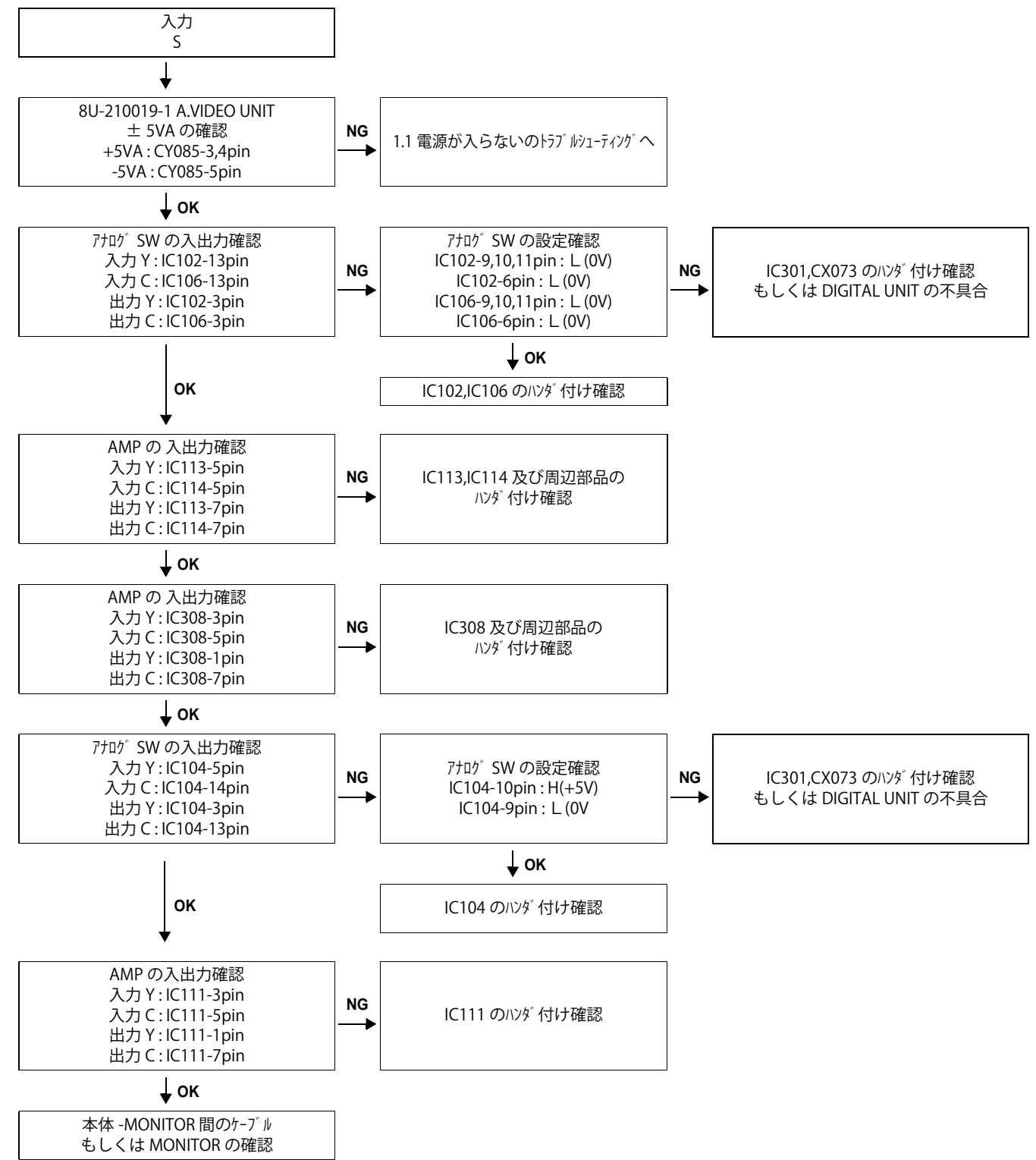
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

I



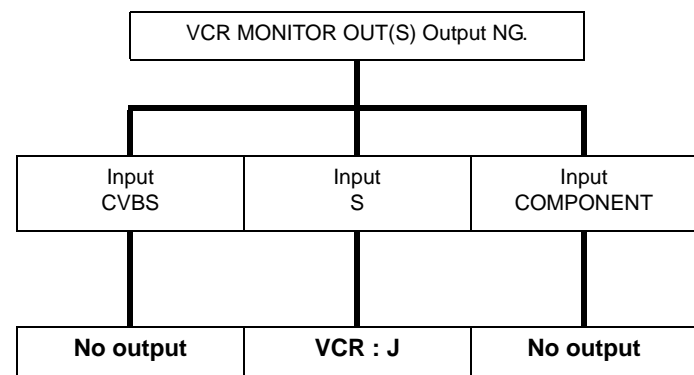
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

I



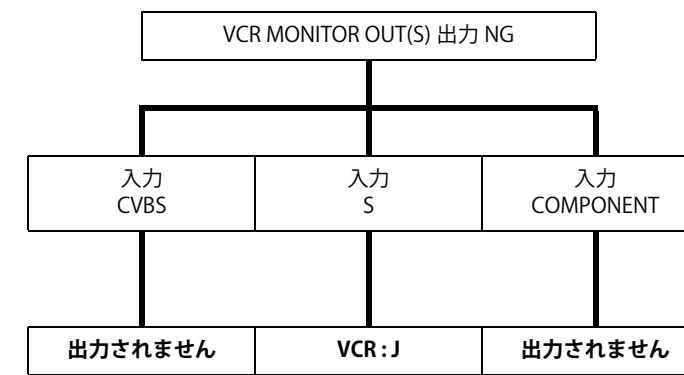
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

2.4. VCR MONITOR OUT(S) Output NG



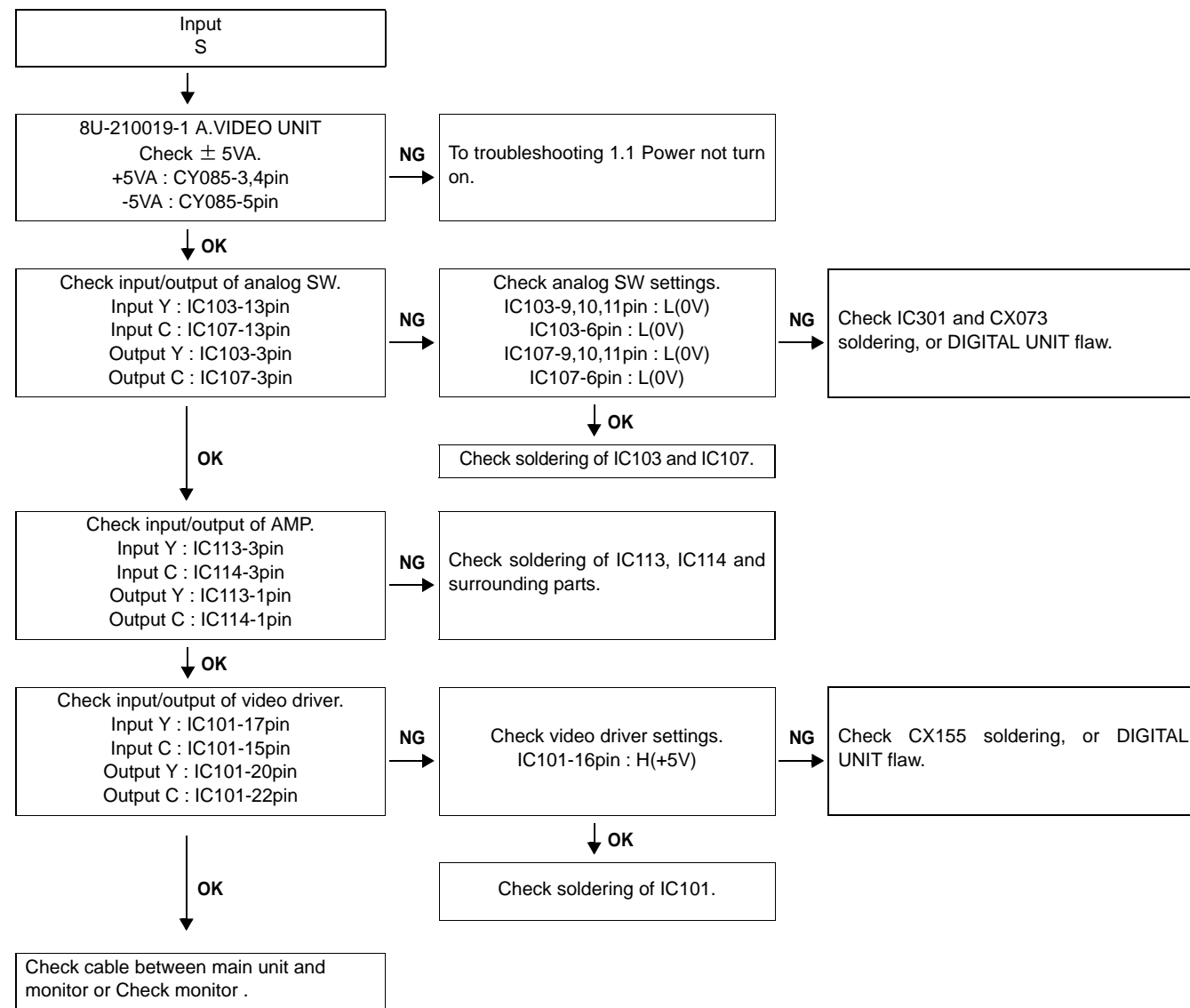
※ When checking operation, select DVD for the function.

2.4. VCR MONITOR OUT(S) 出力 NG



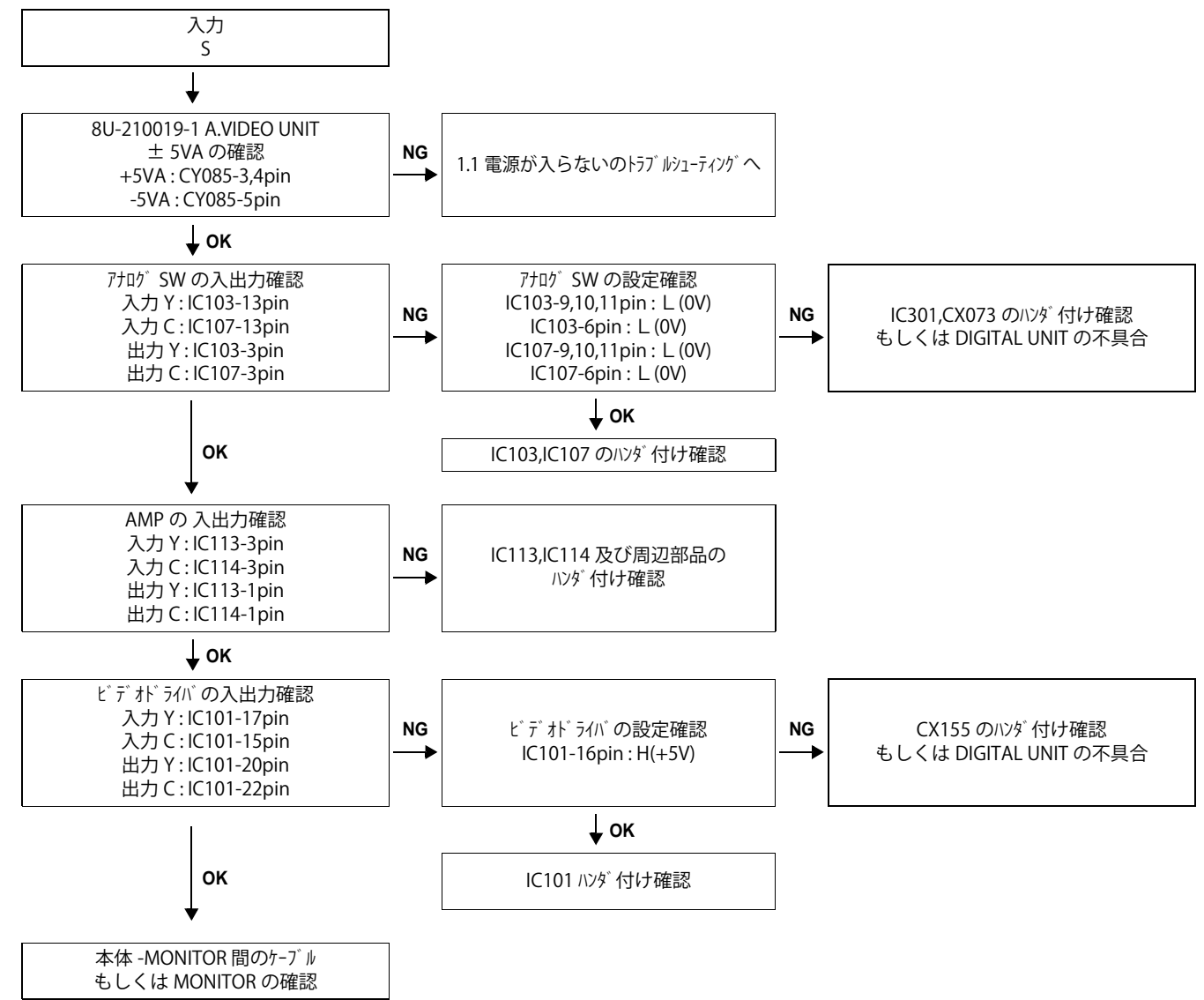
※ 動作を確認する時はファンクションを DVD に選択してください。

J



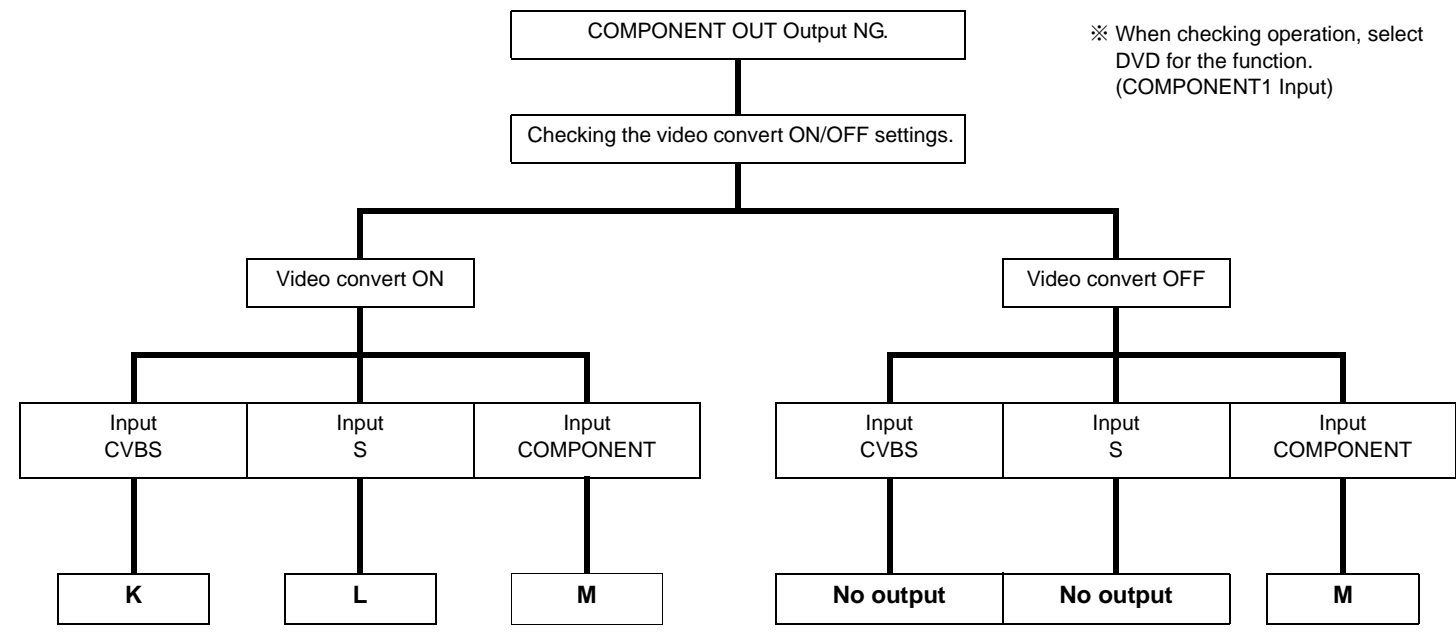
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

J

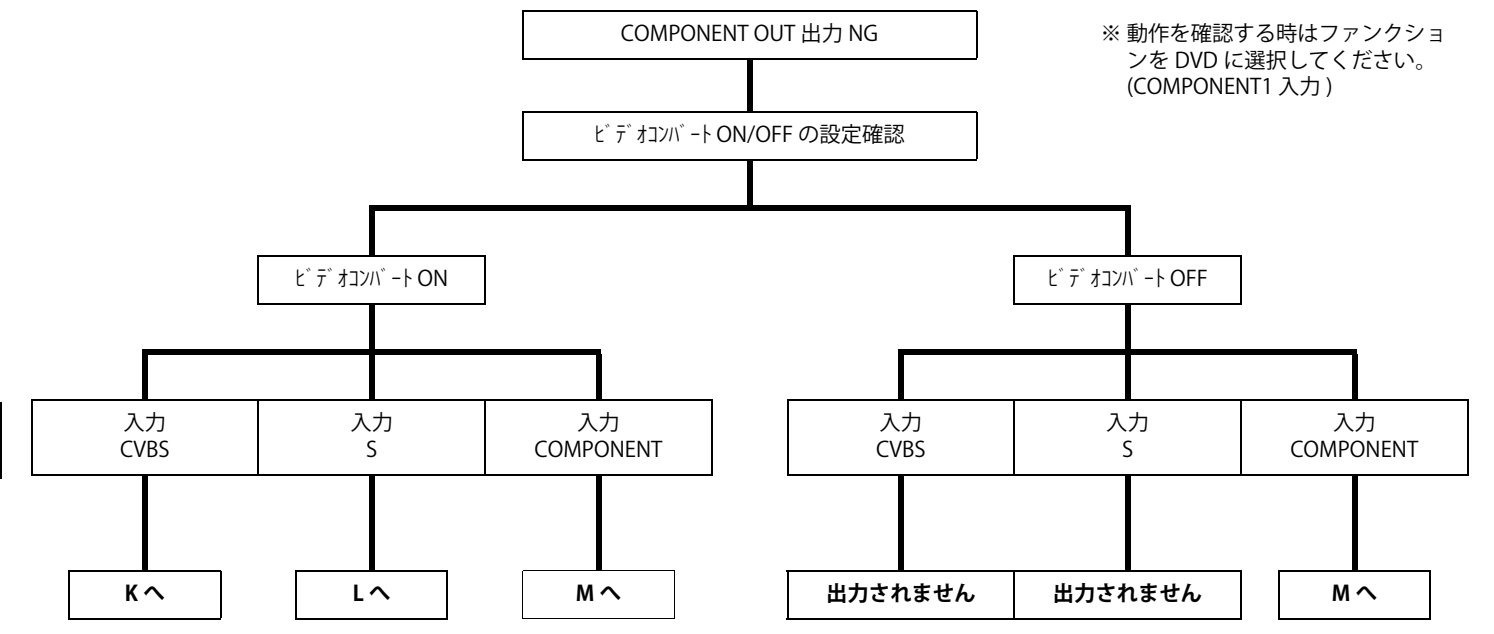


※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

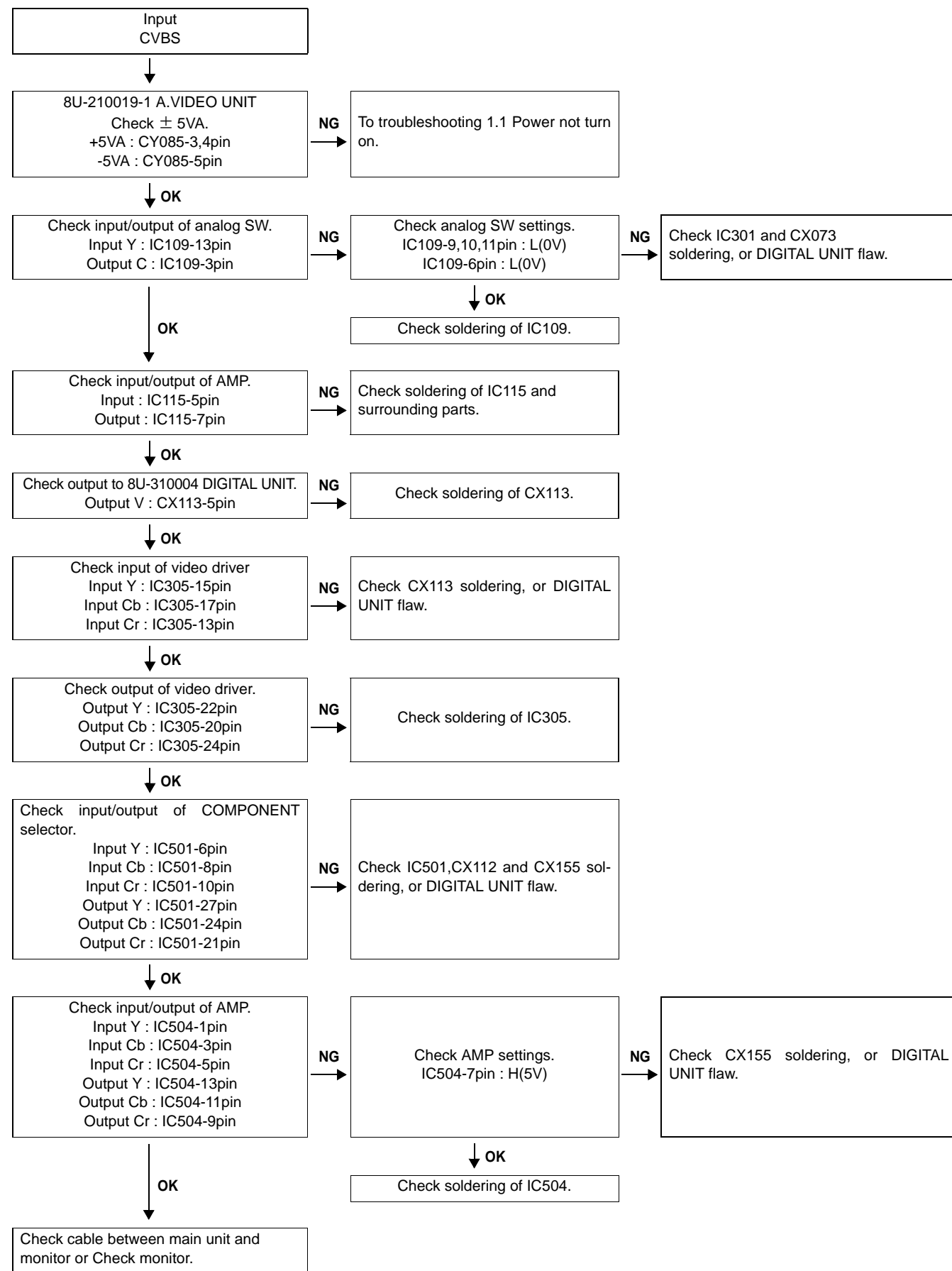
2.5. COMPONENT OUT Output NG



2.5. COMPONENT OUT 出力 NG

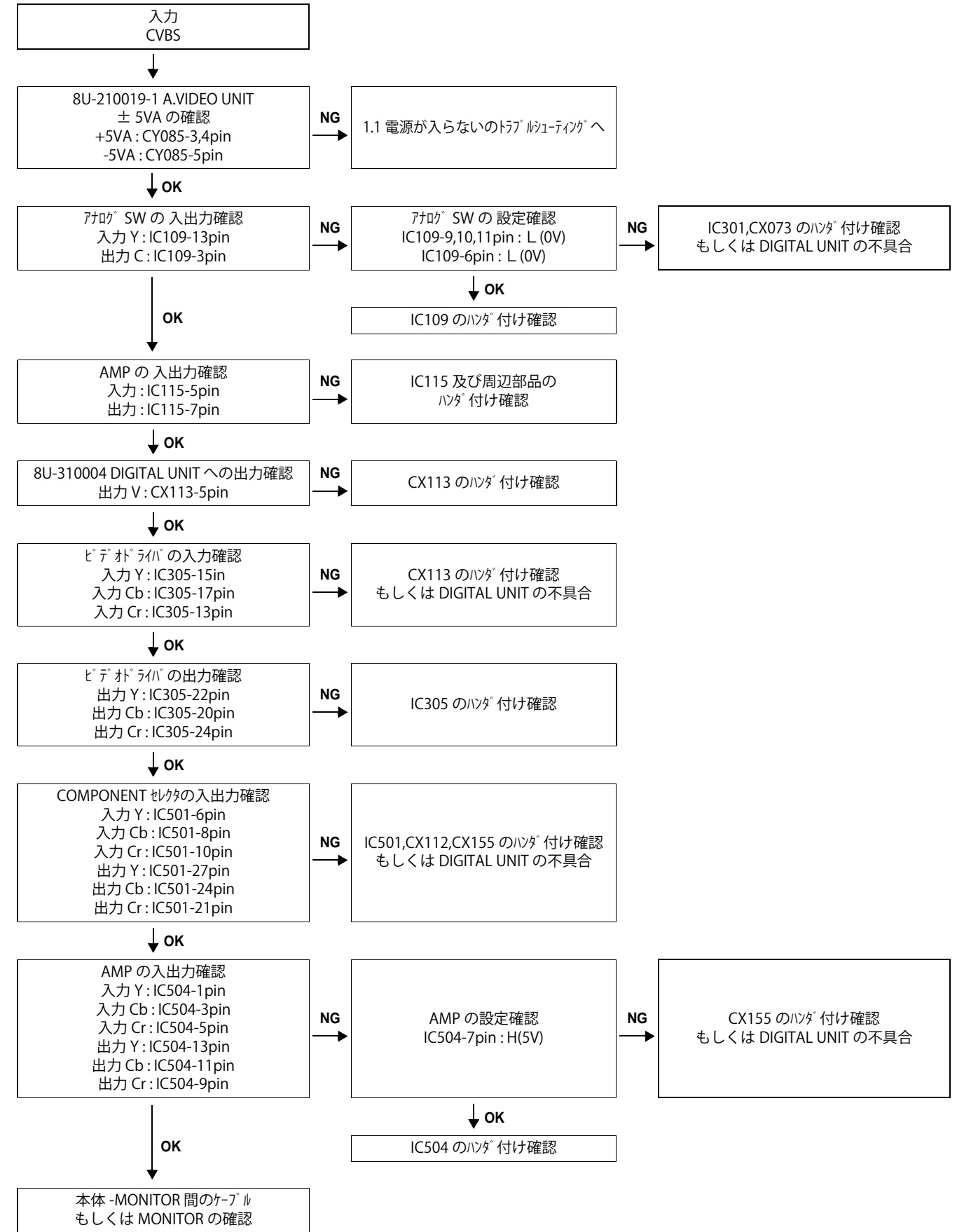


K



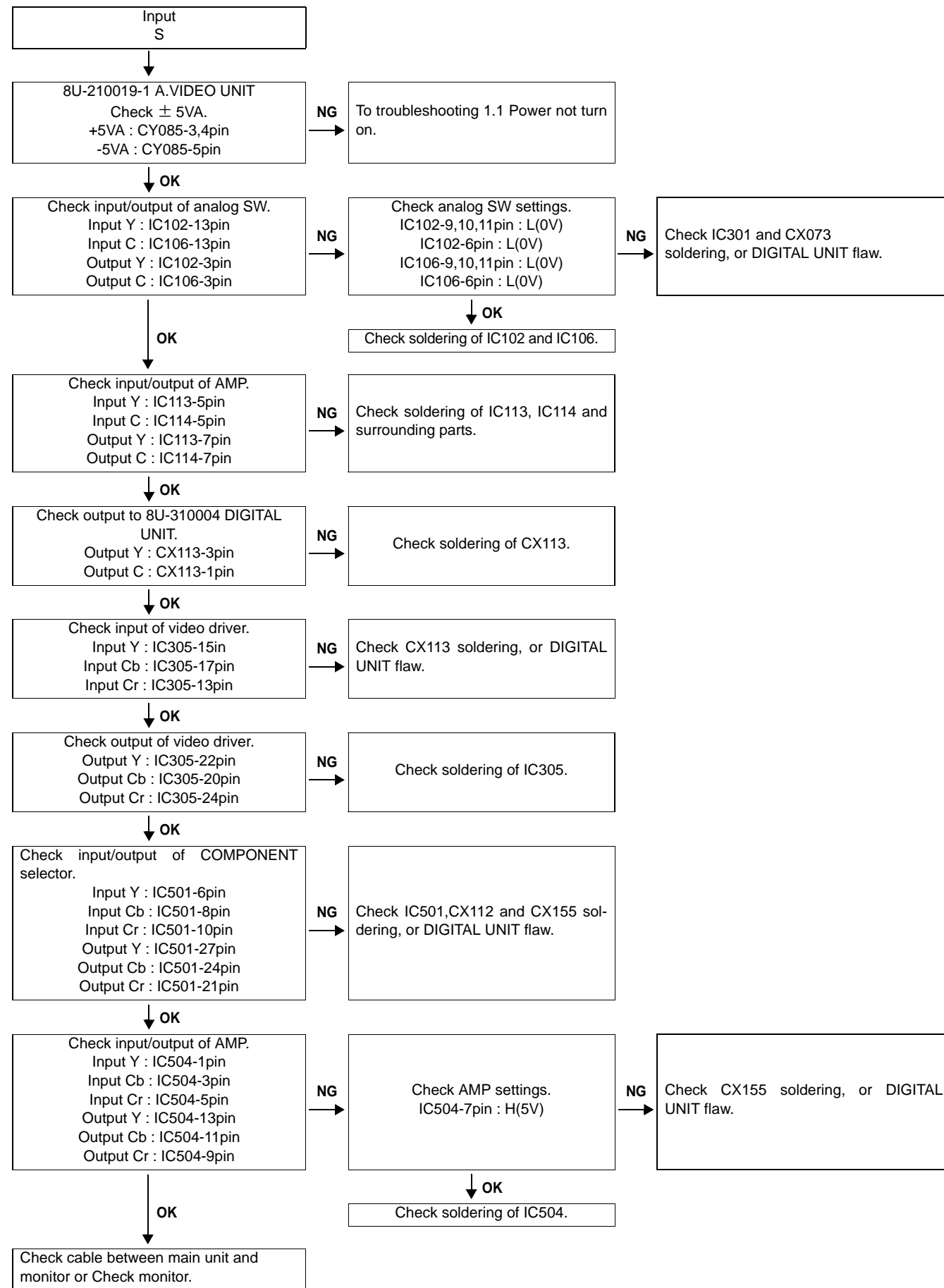
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

K



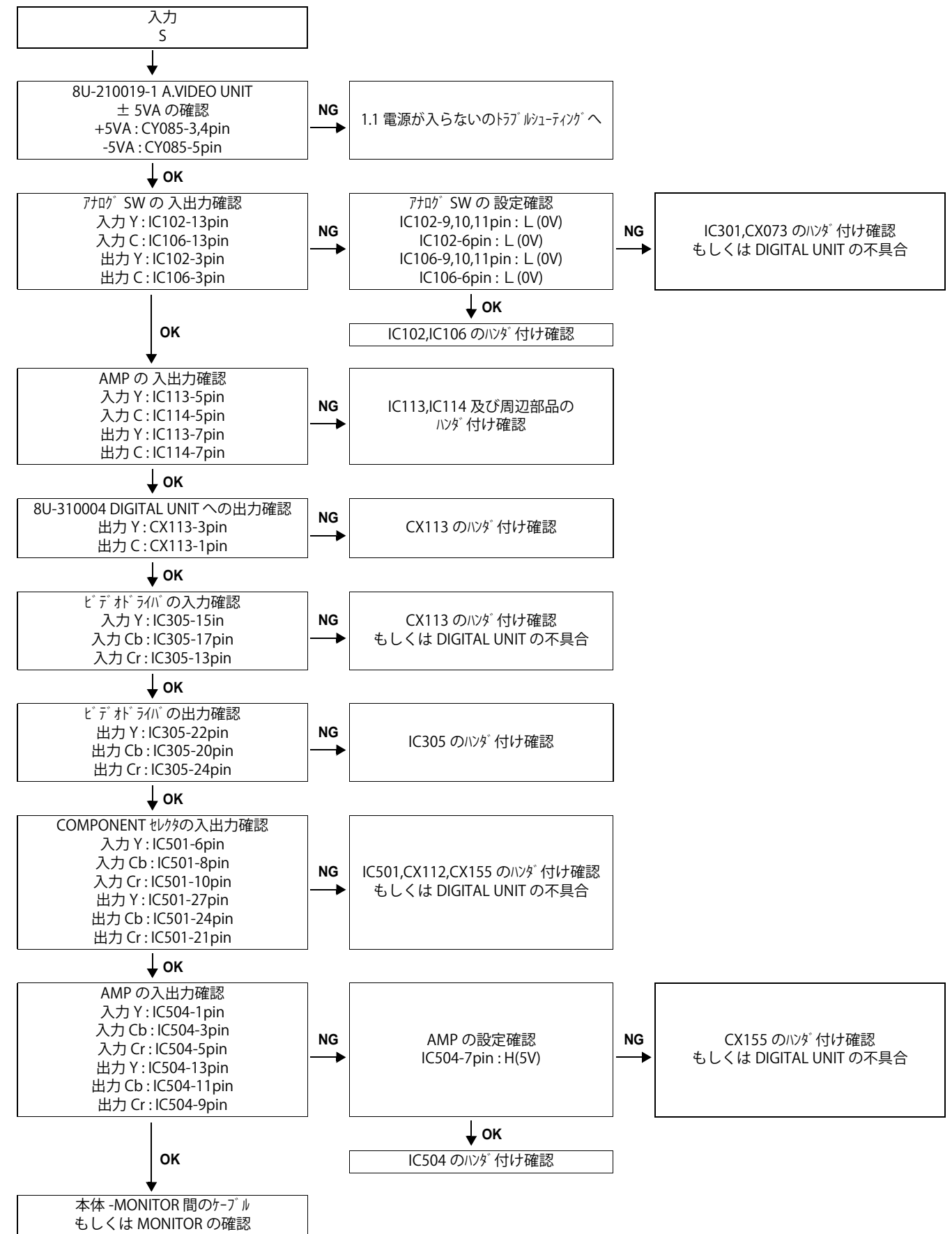
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

L



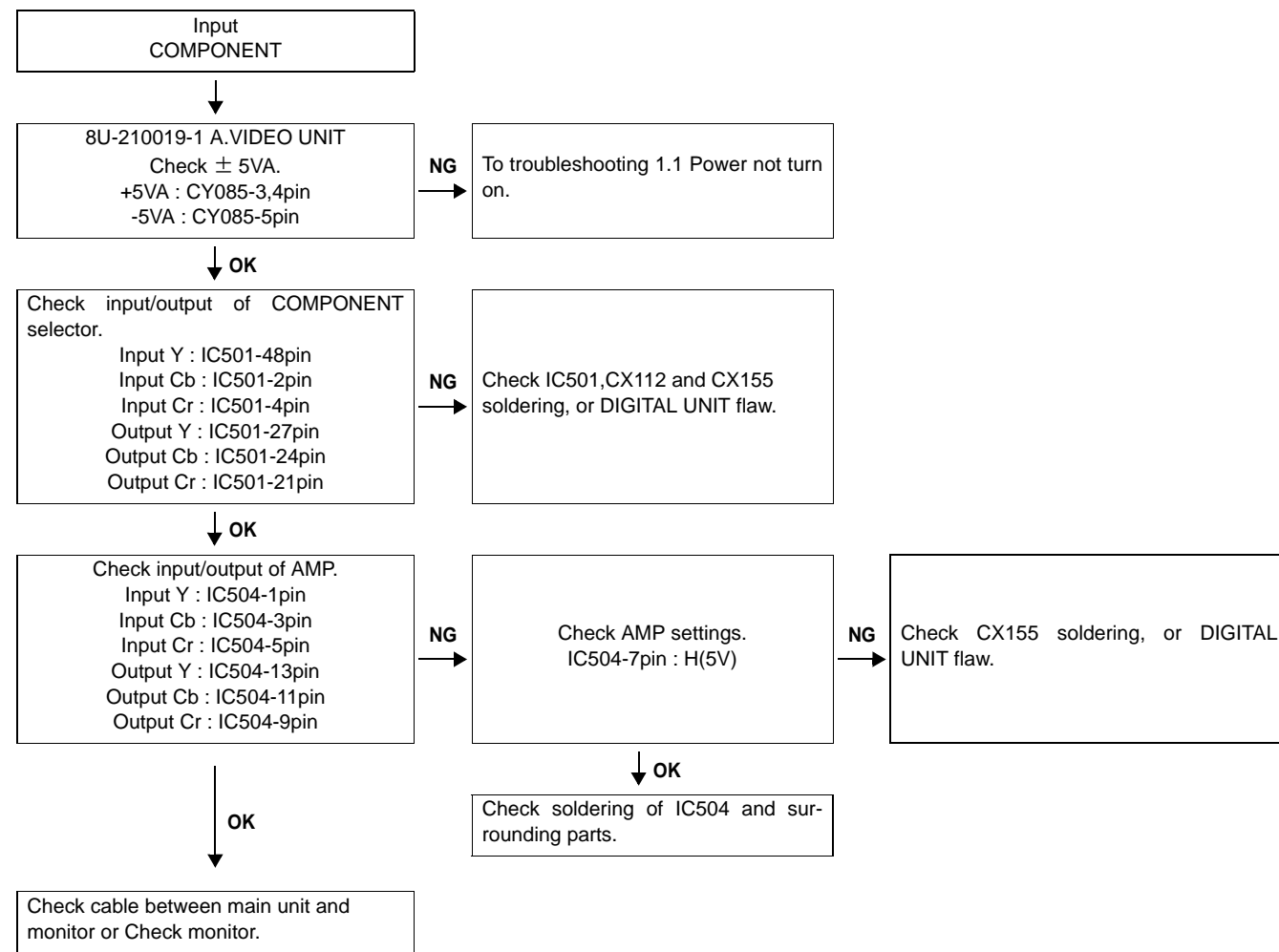
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

L



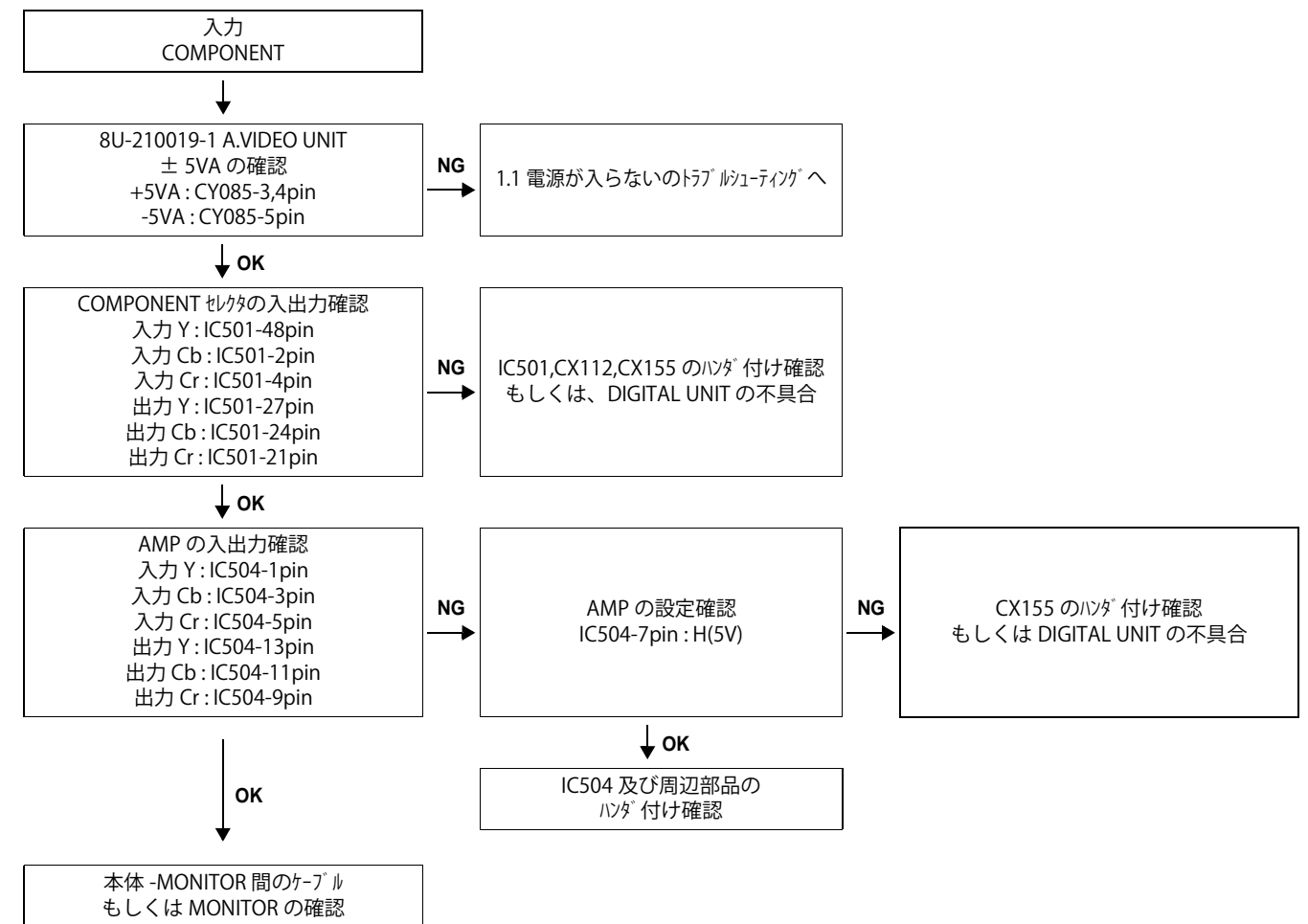
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

M



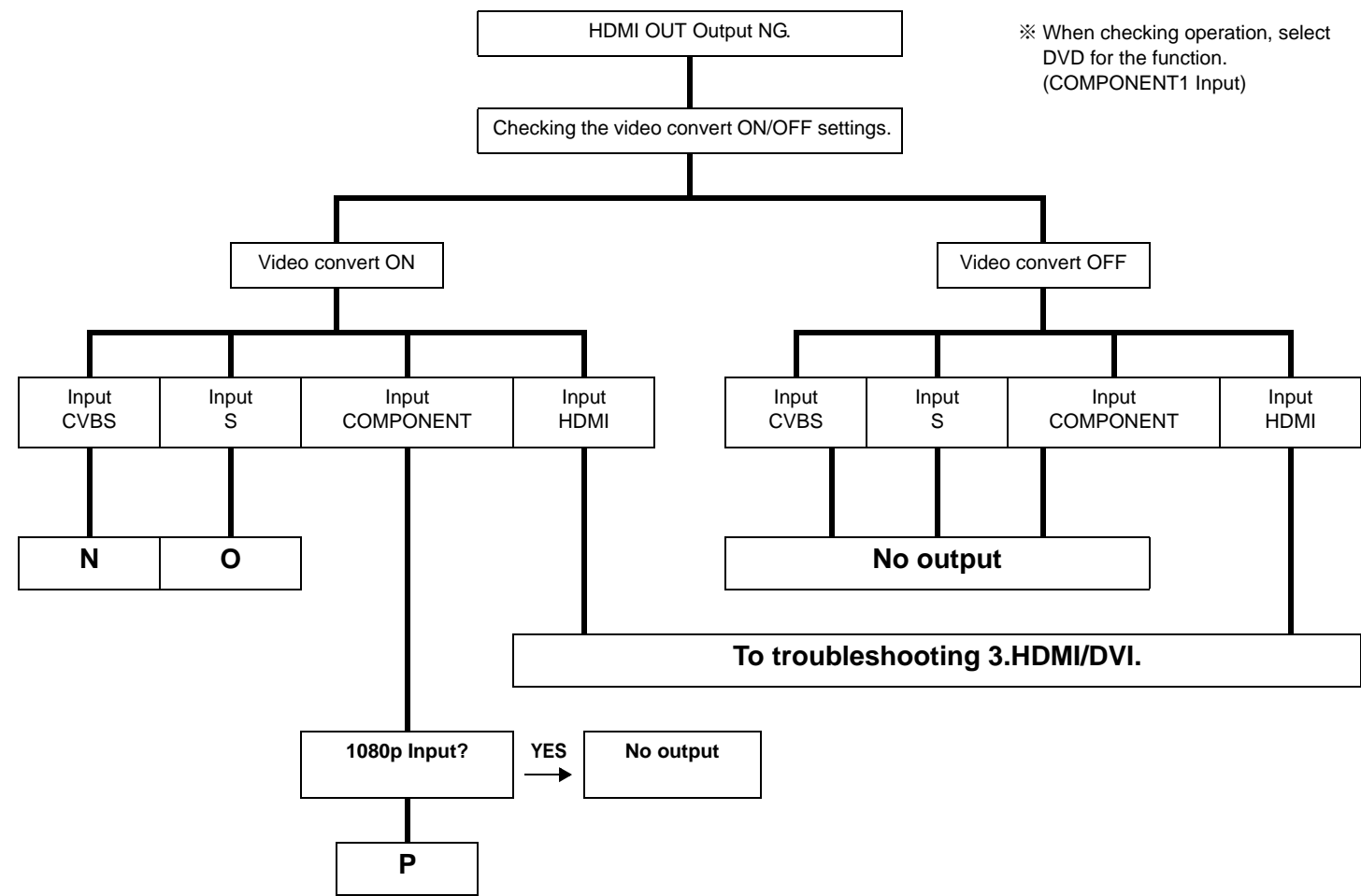
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

M

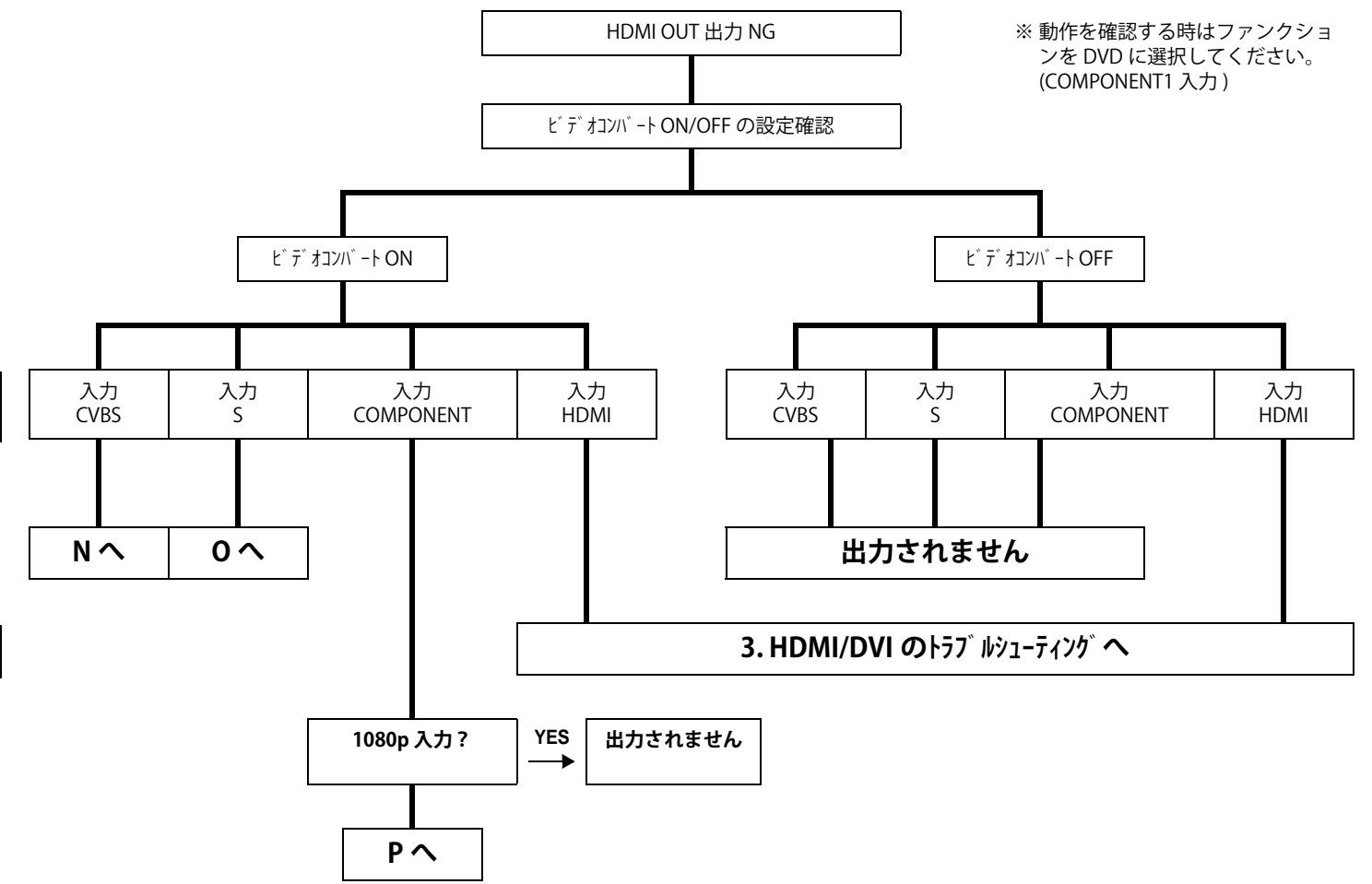


※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

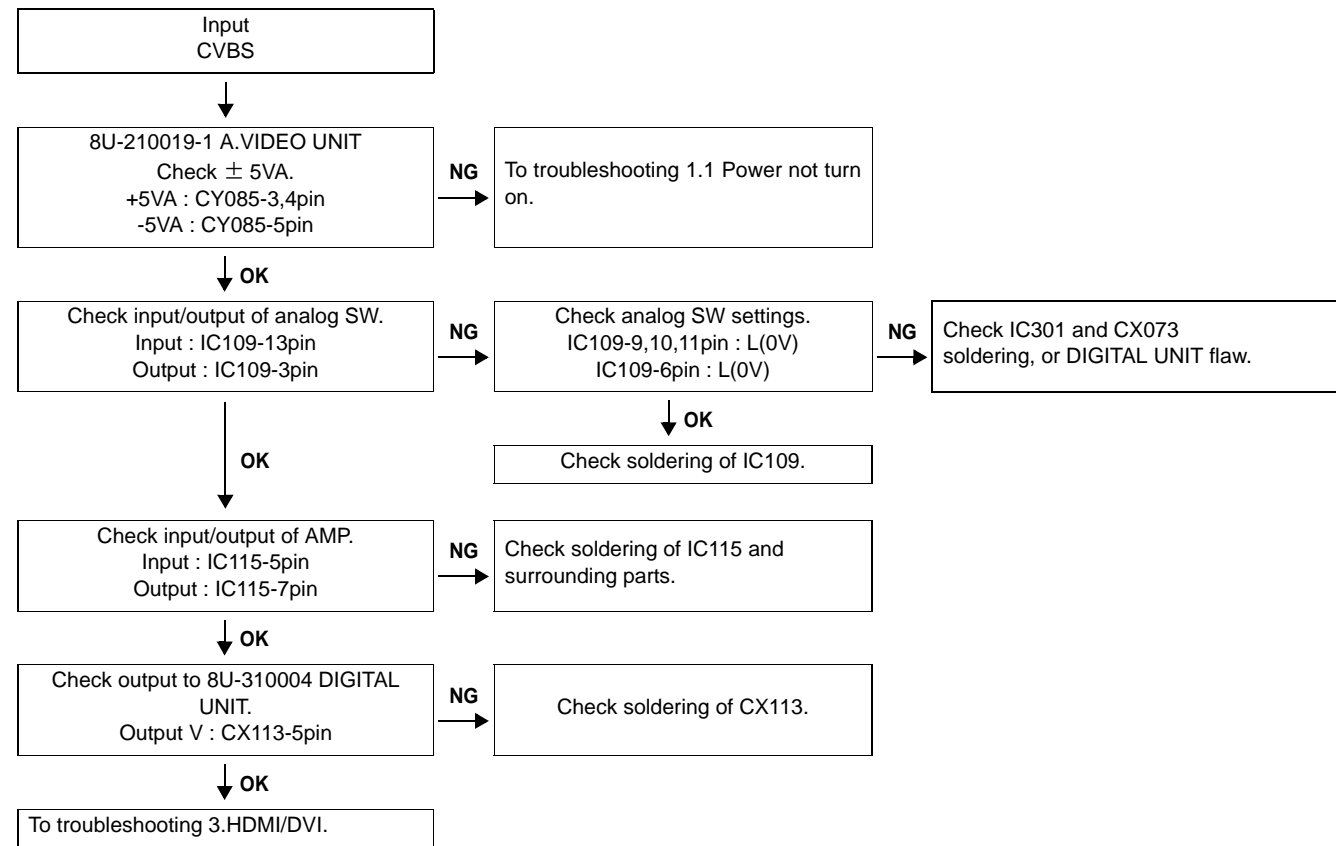
2.6. HDMI OUT Output NG



2.6. HDMI OUT 出力 NG

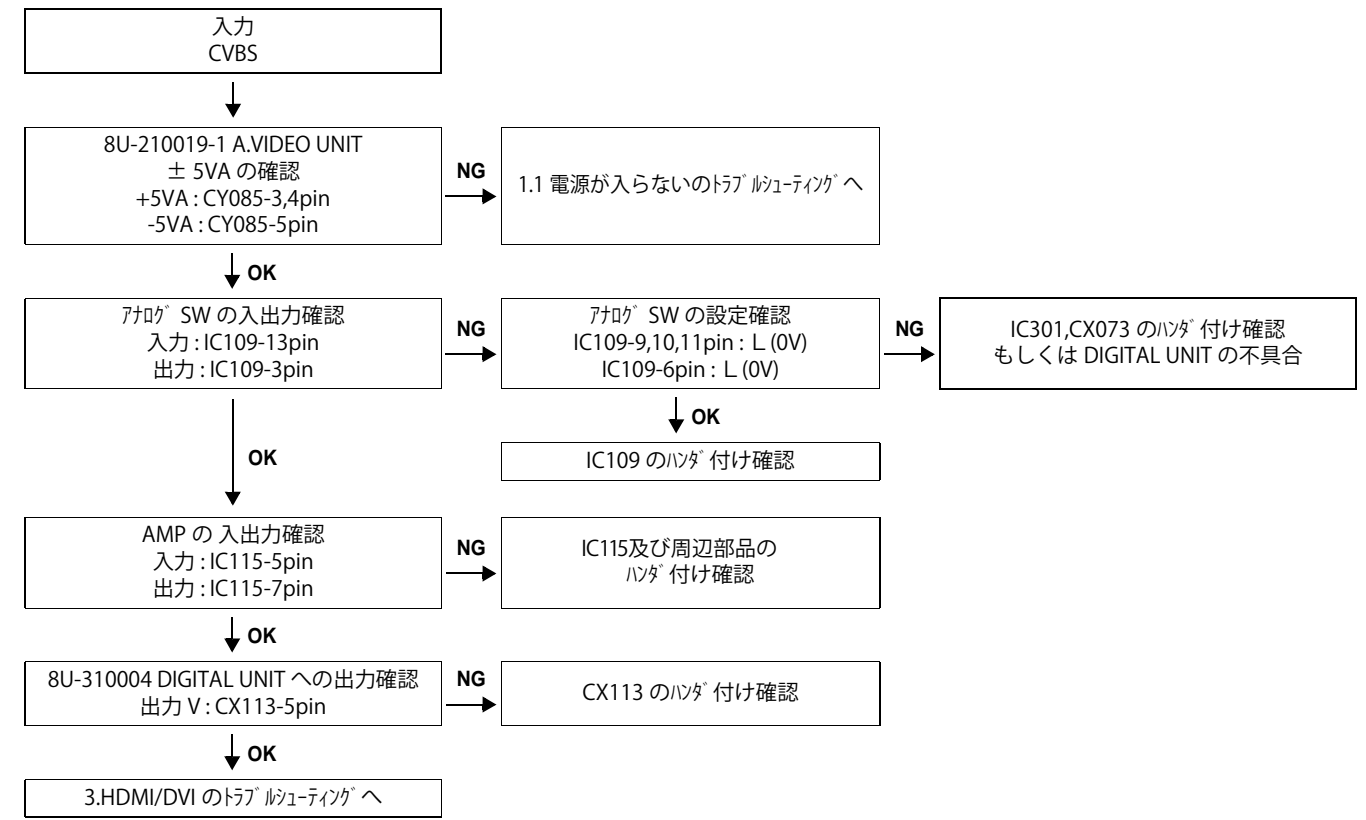


N



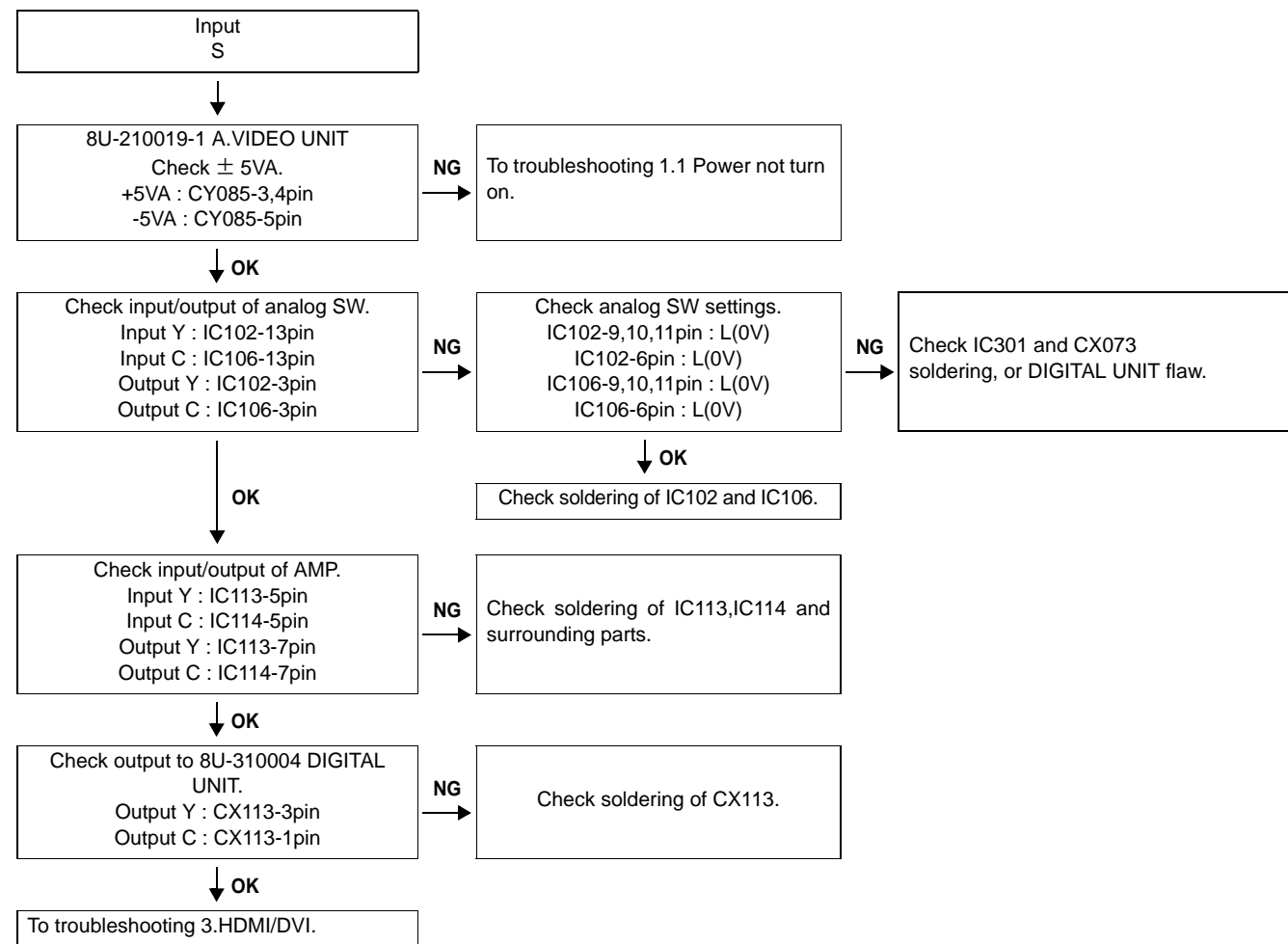
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

N



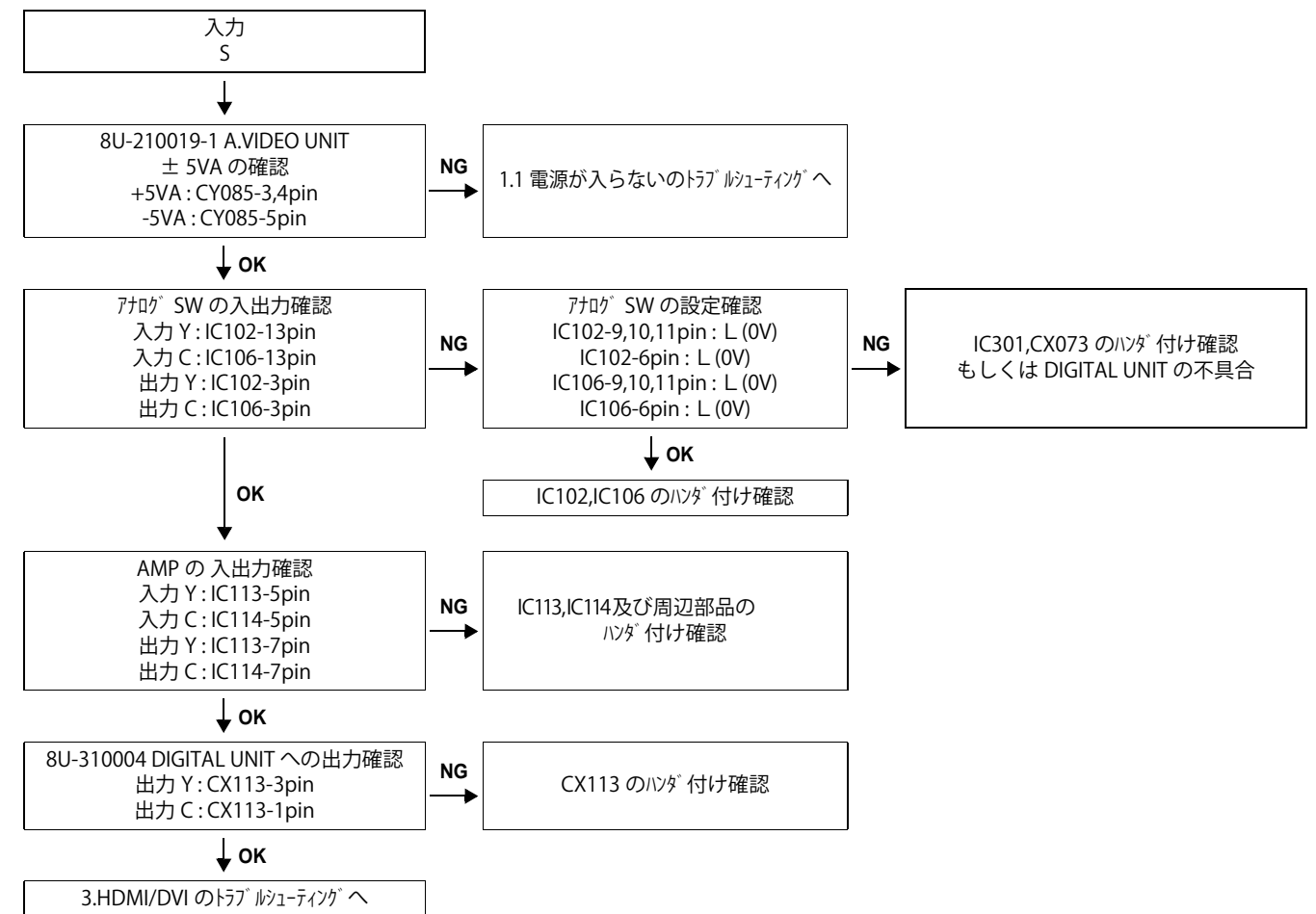
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

0



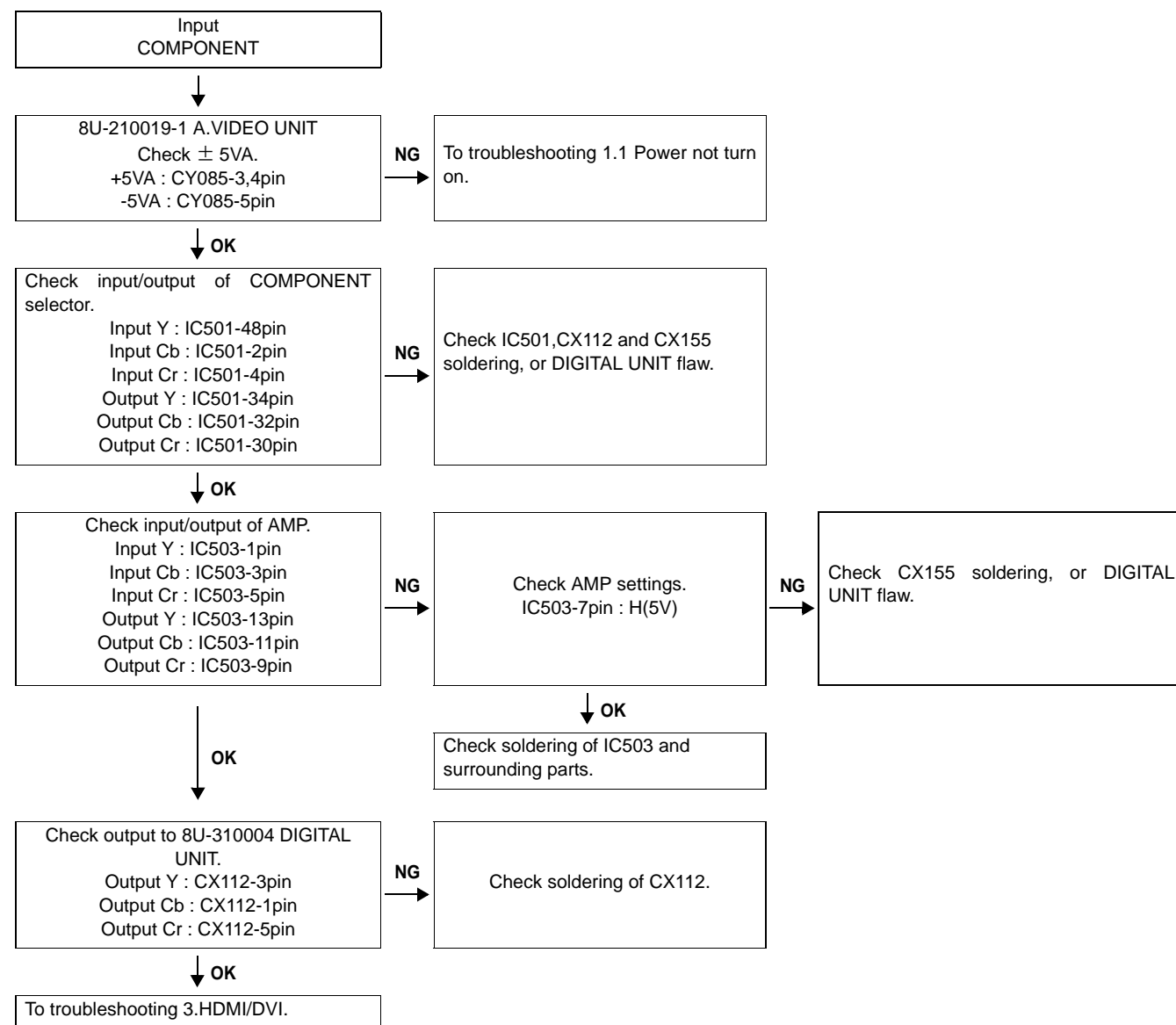
※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

0



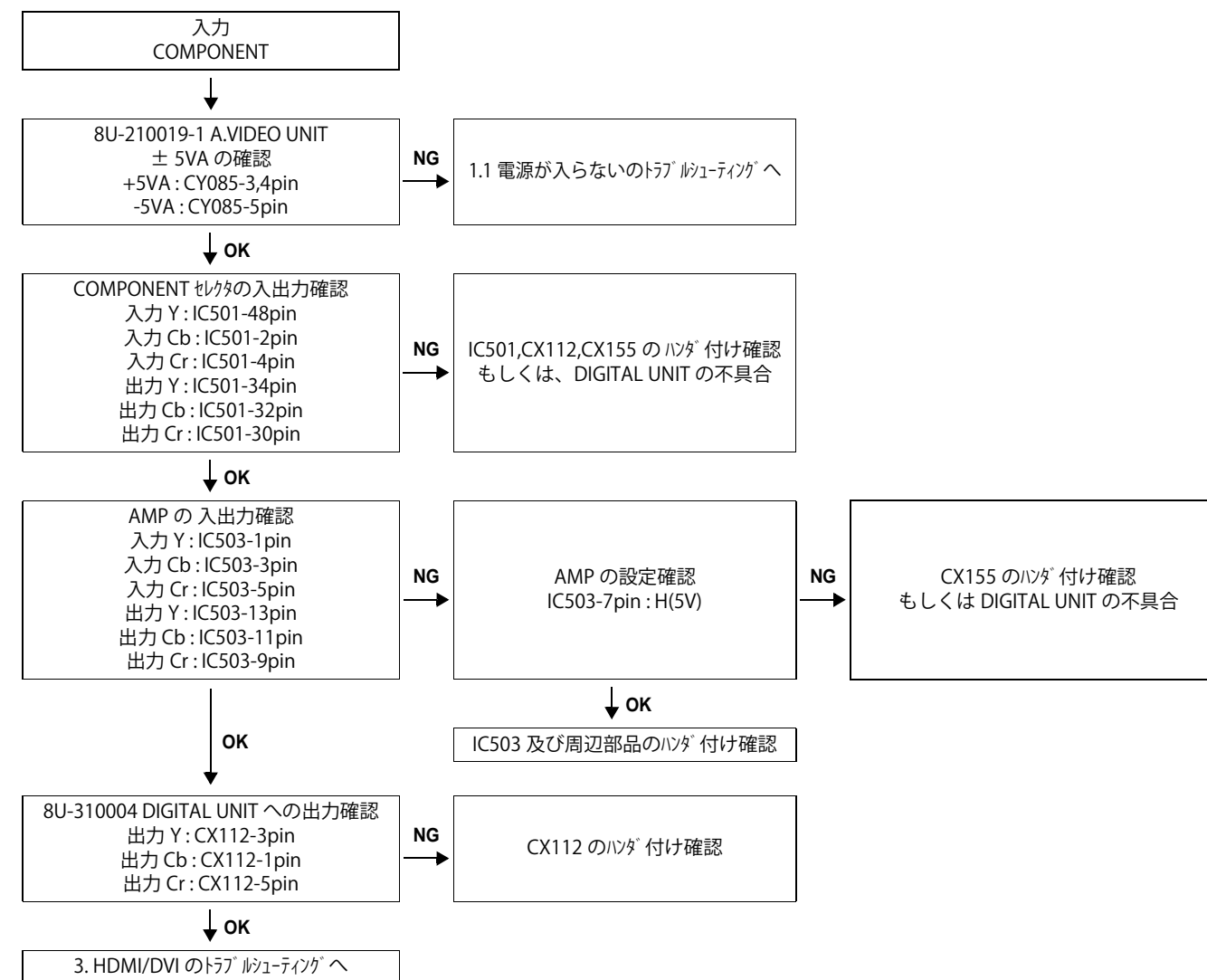
※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

P



※ Unless specified, 8U-210019-1 A.VIDEO UNIT part.

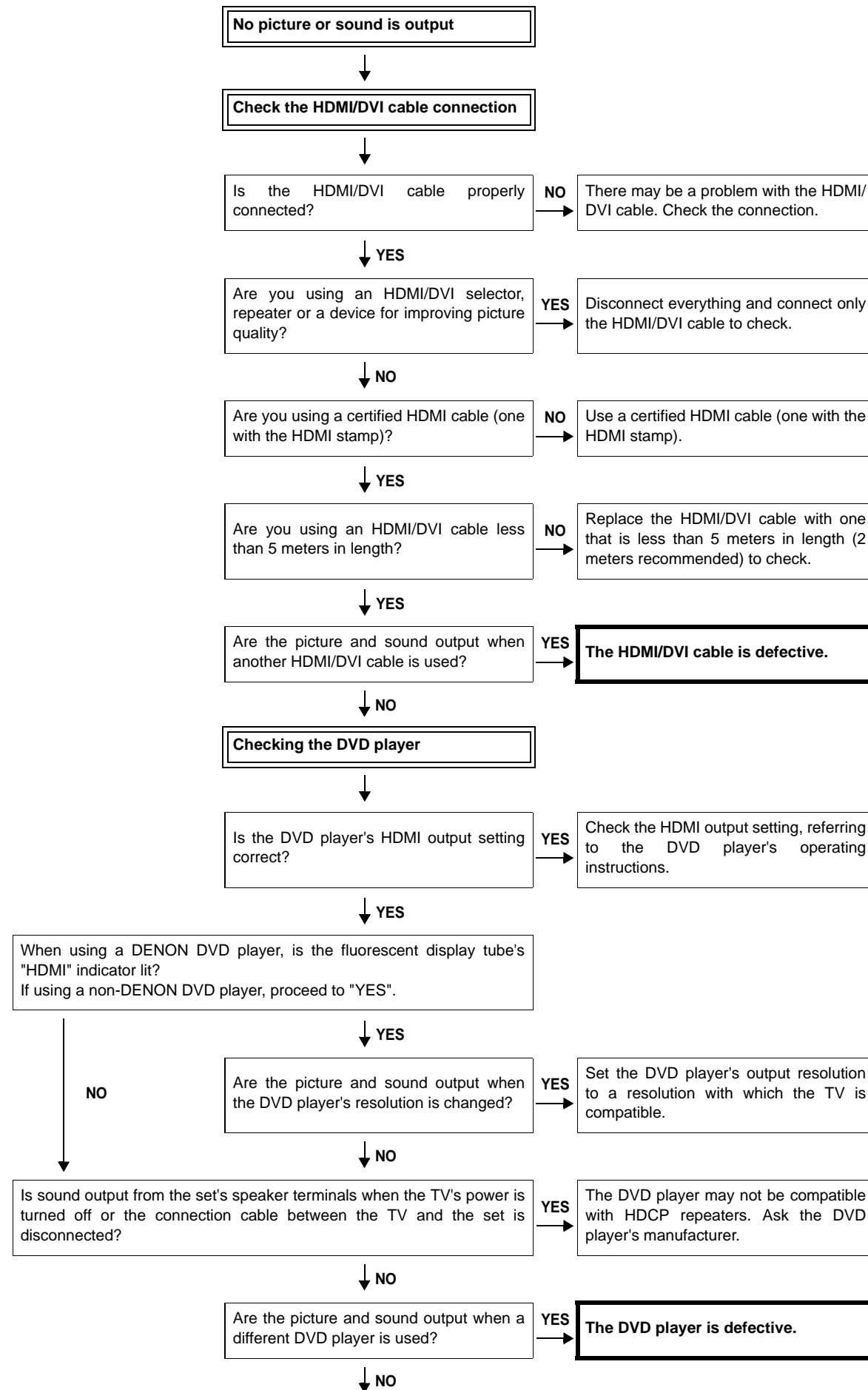
P



※ 特に記載がない場合は 8U-210019-1 A.VIDEO UNIT の部品です。

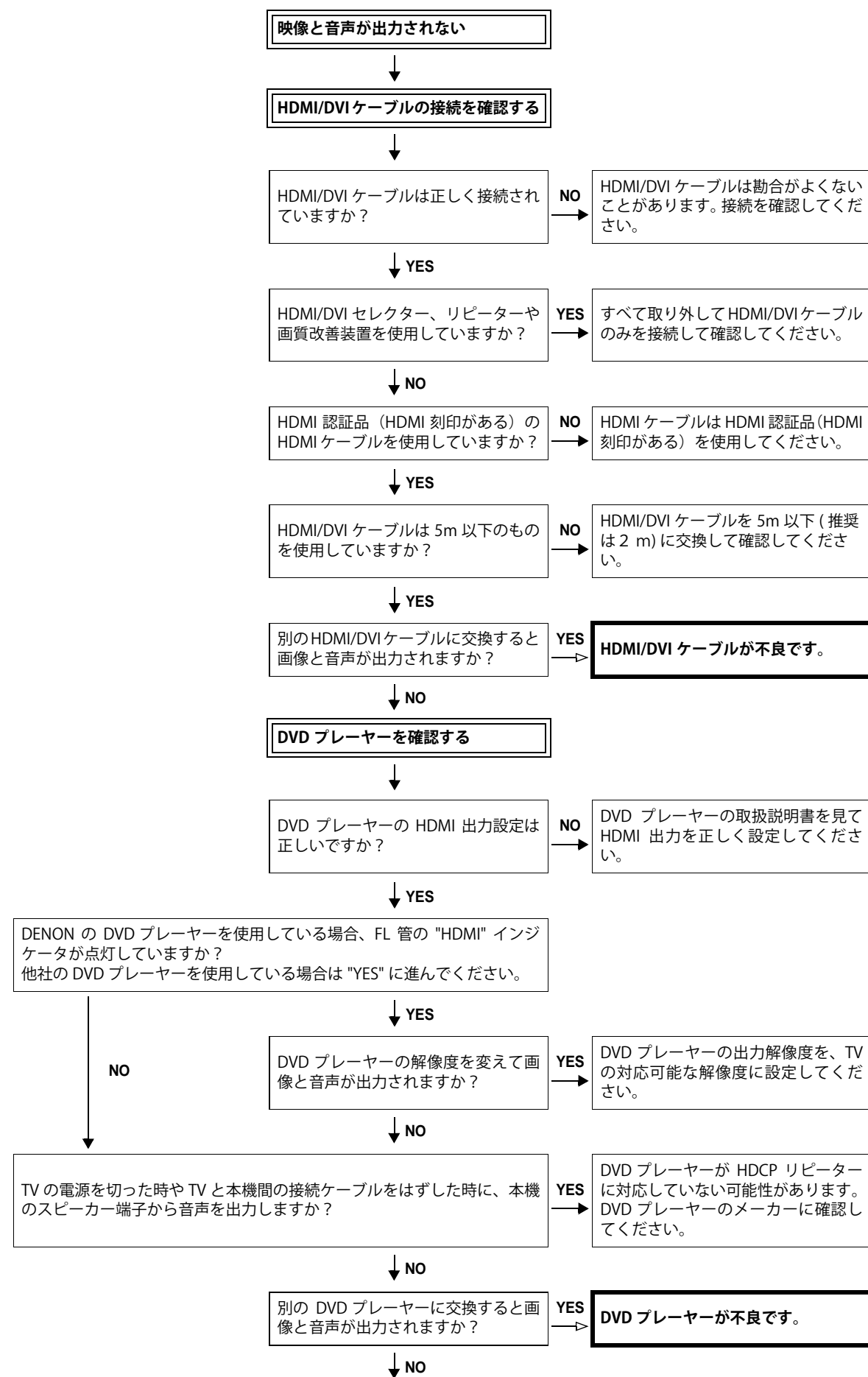
3. HDMI/DVI

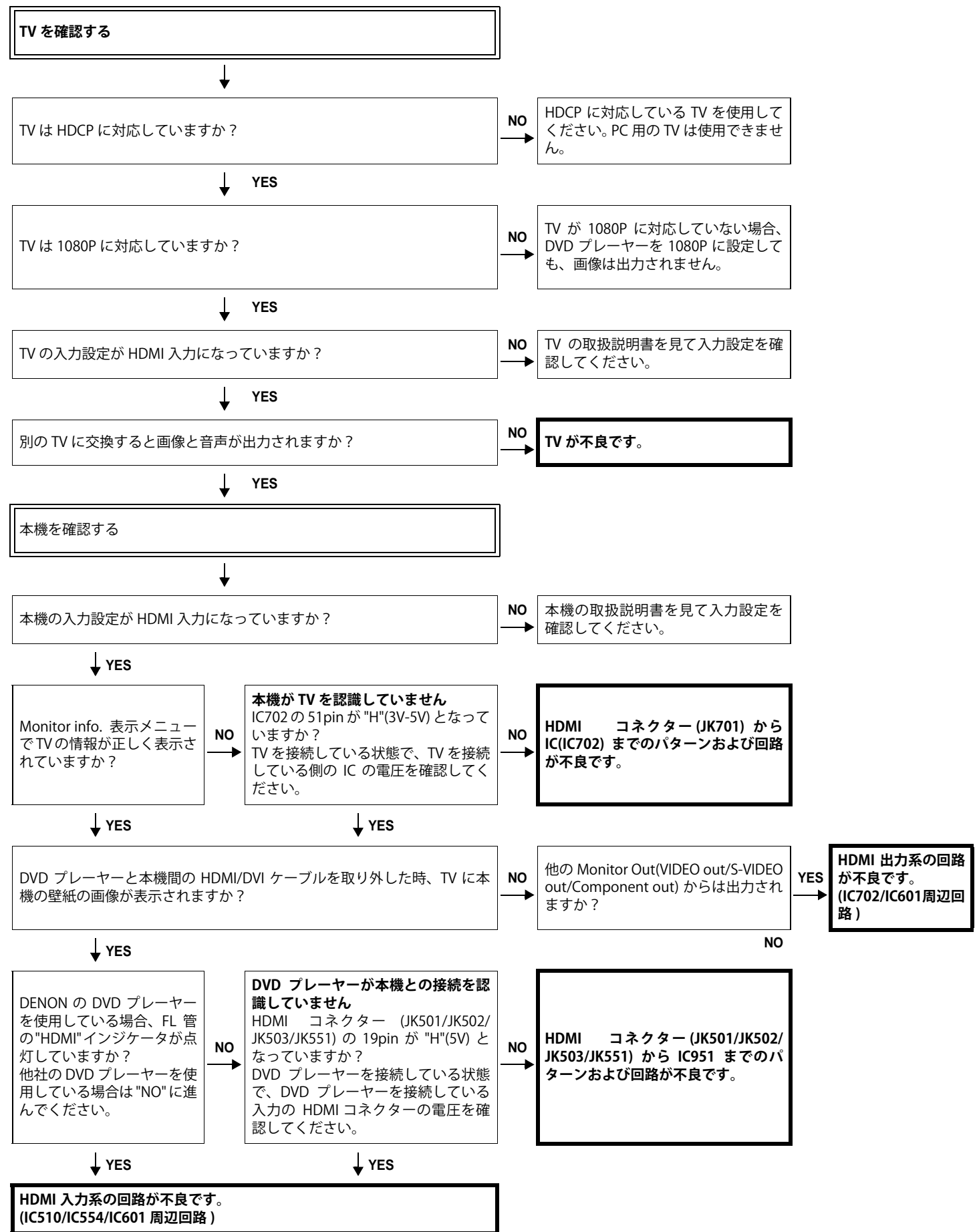
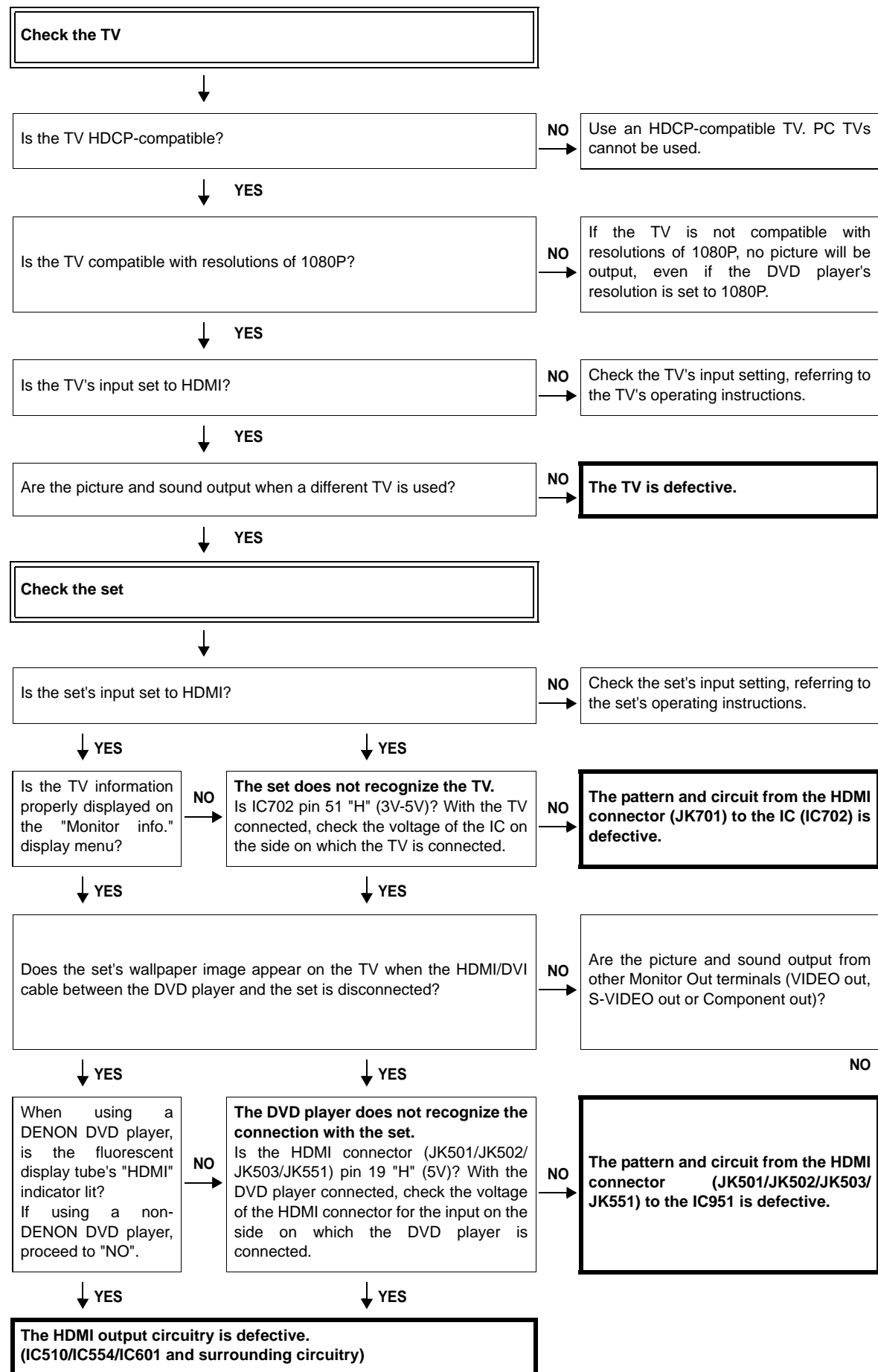
3.1. No picture or sound is output



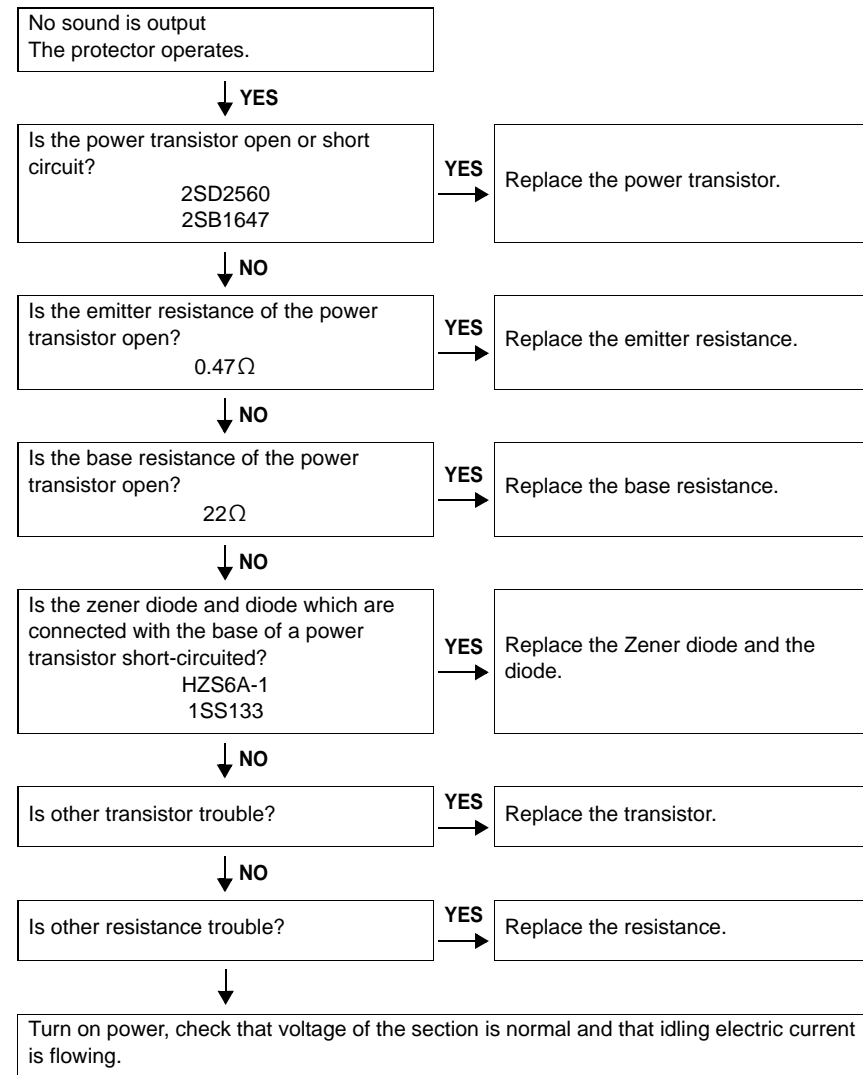
3. HDMI/DVI

3.1. 映像と音声出力されない

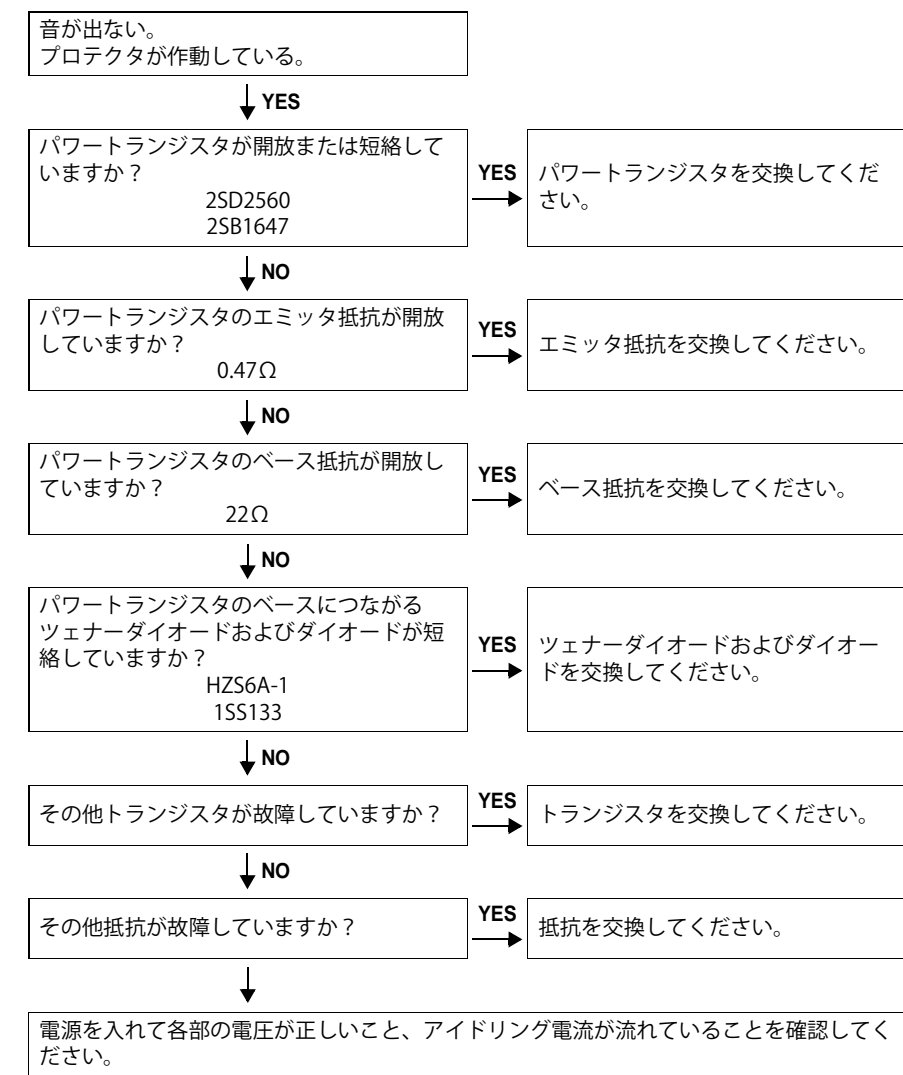




4. Power AMP (8U-110030,8U-110041)

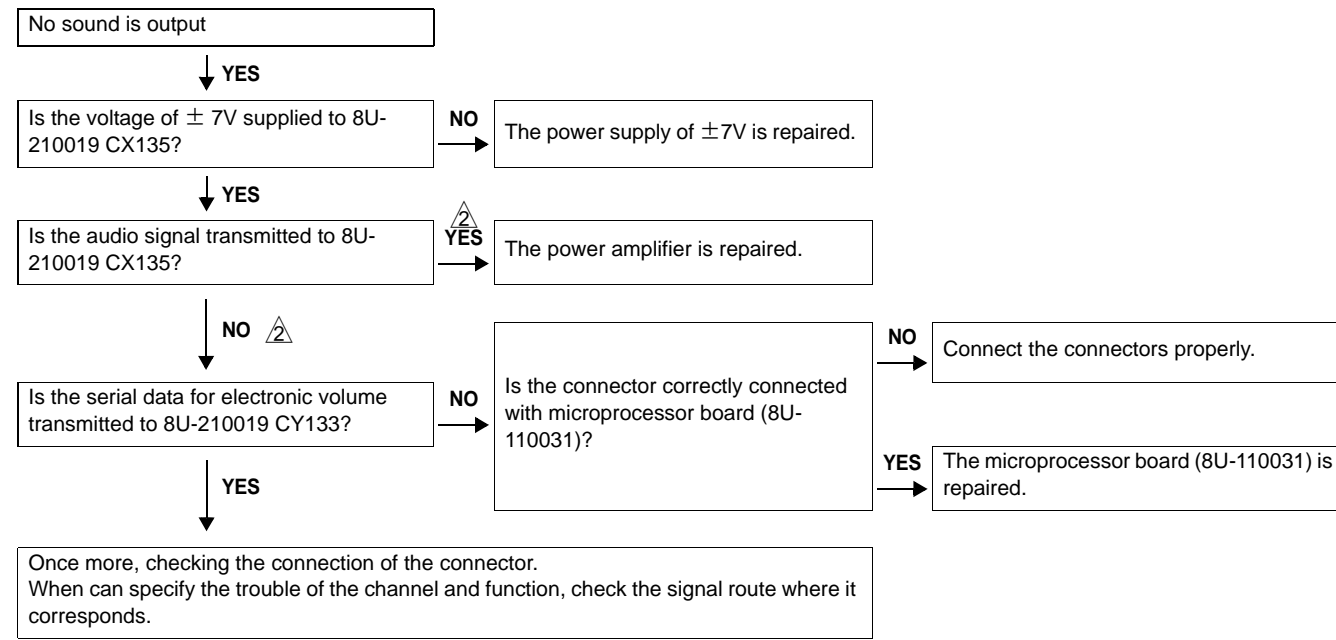


4. パワーアンプ (8U-110030,8U-110041)



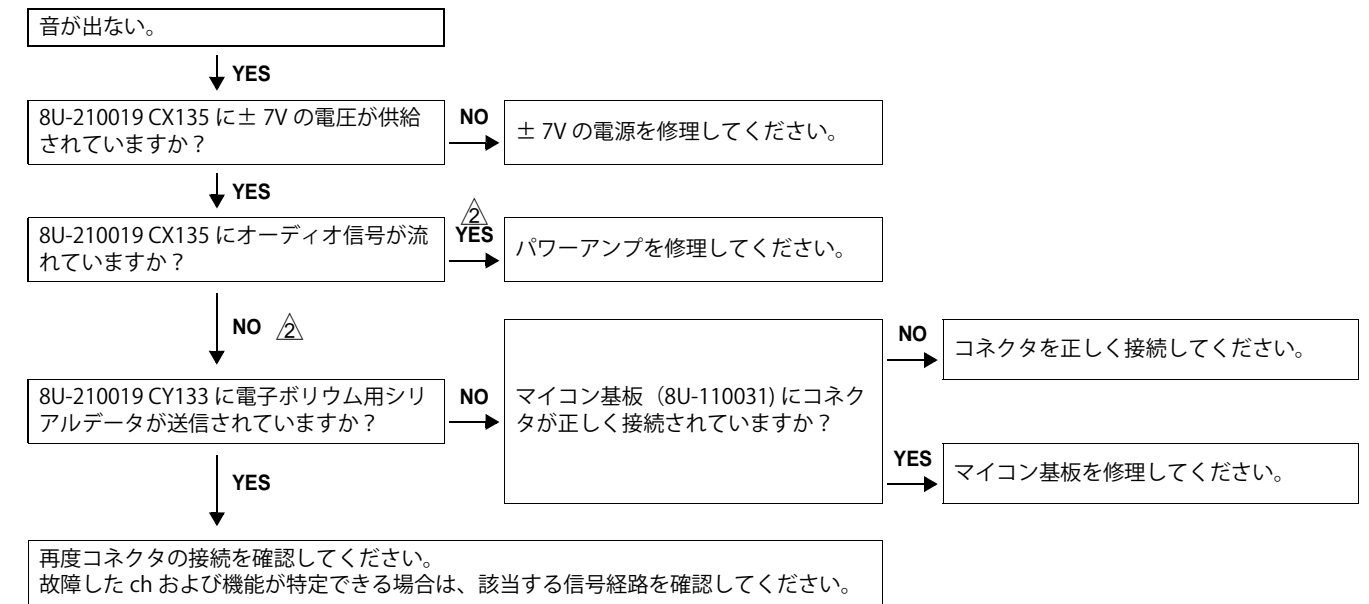
5. Analog audio

5.1. 8U-210019

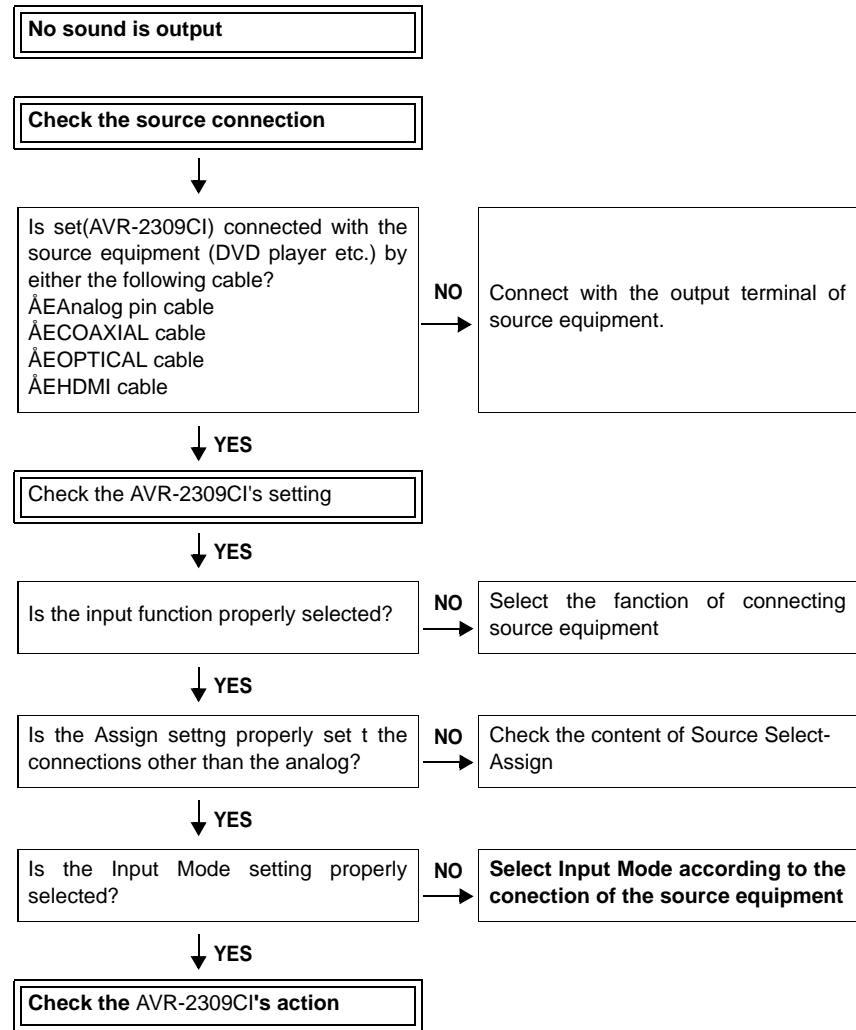


5. アナログオーディオ

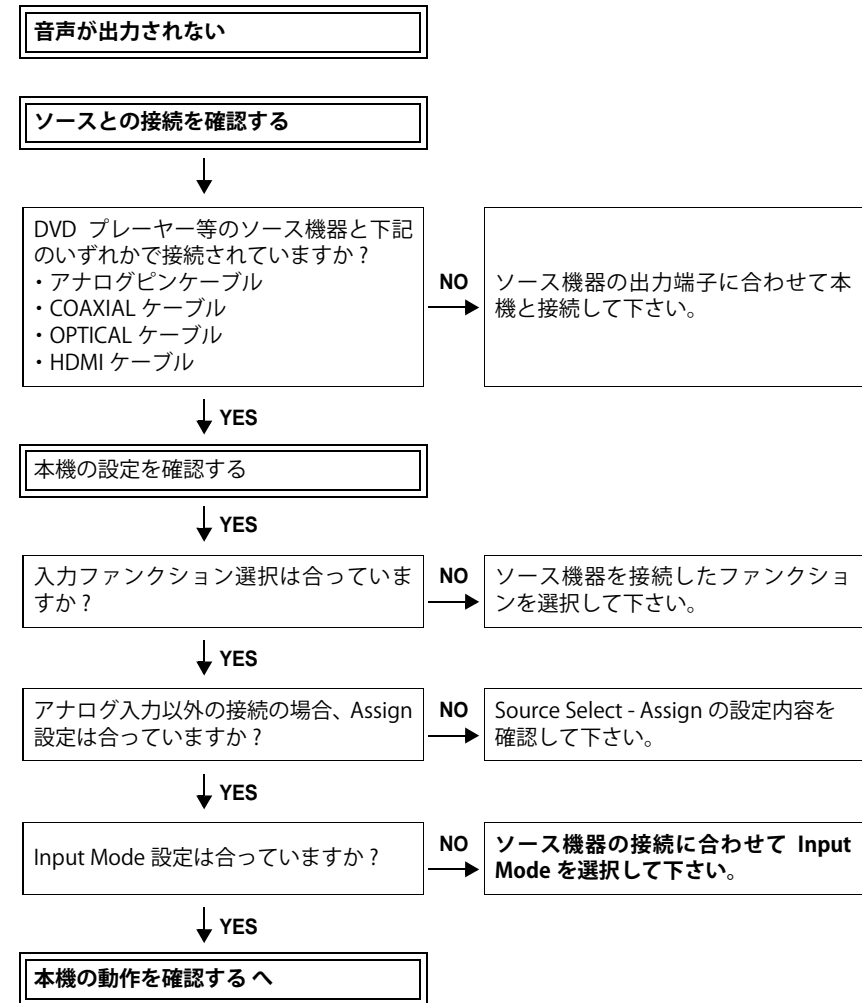
5.1. 8U-210019

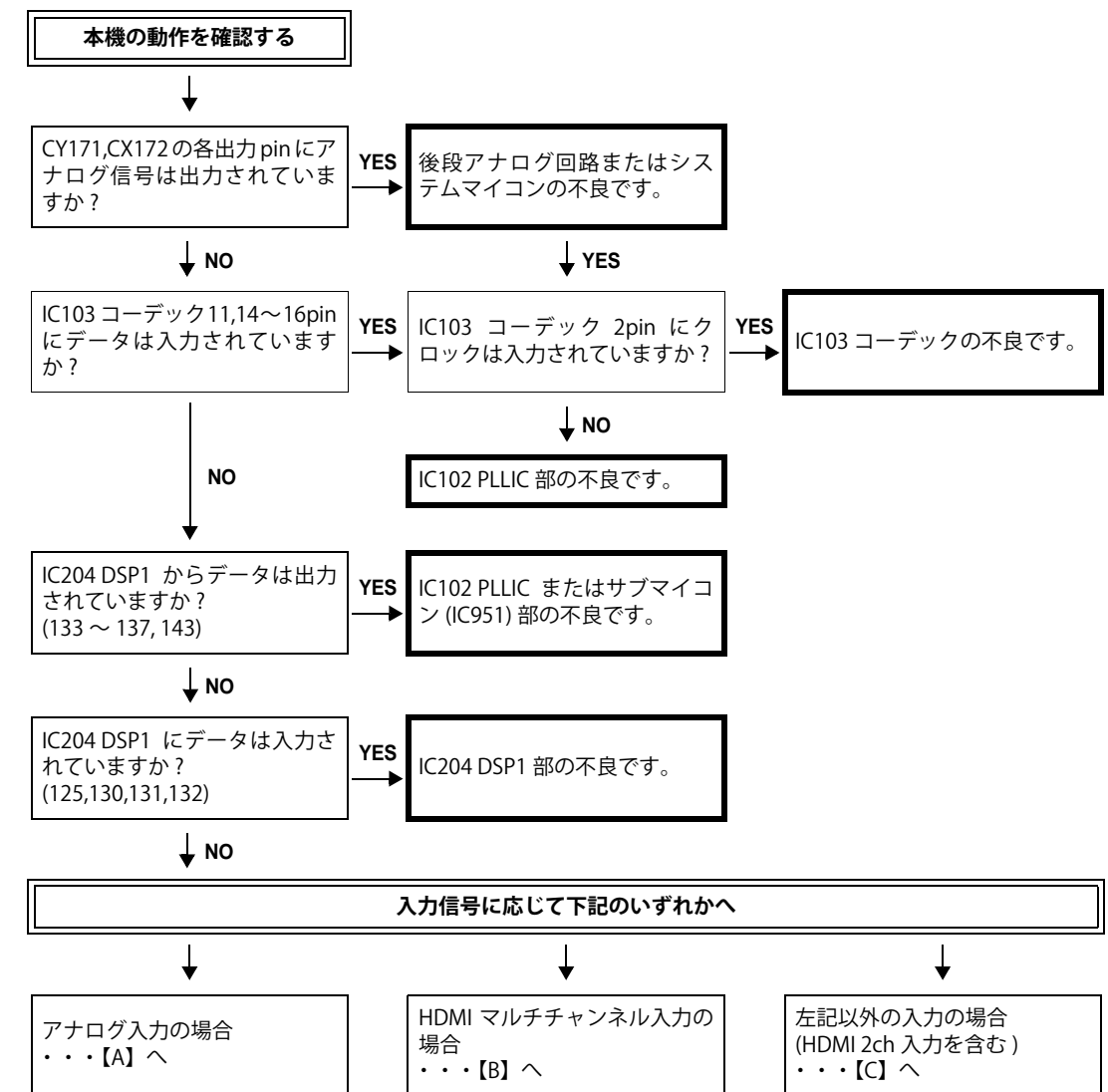
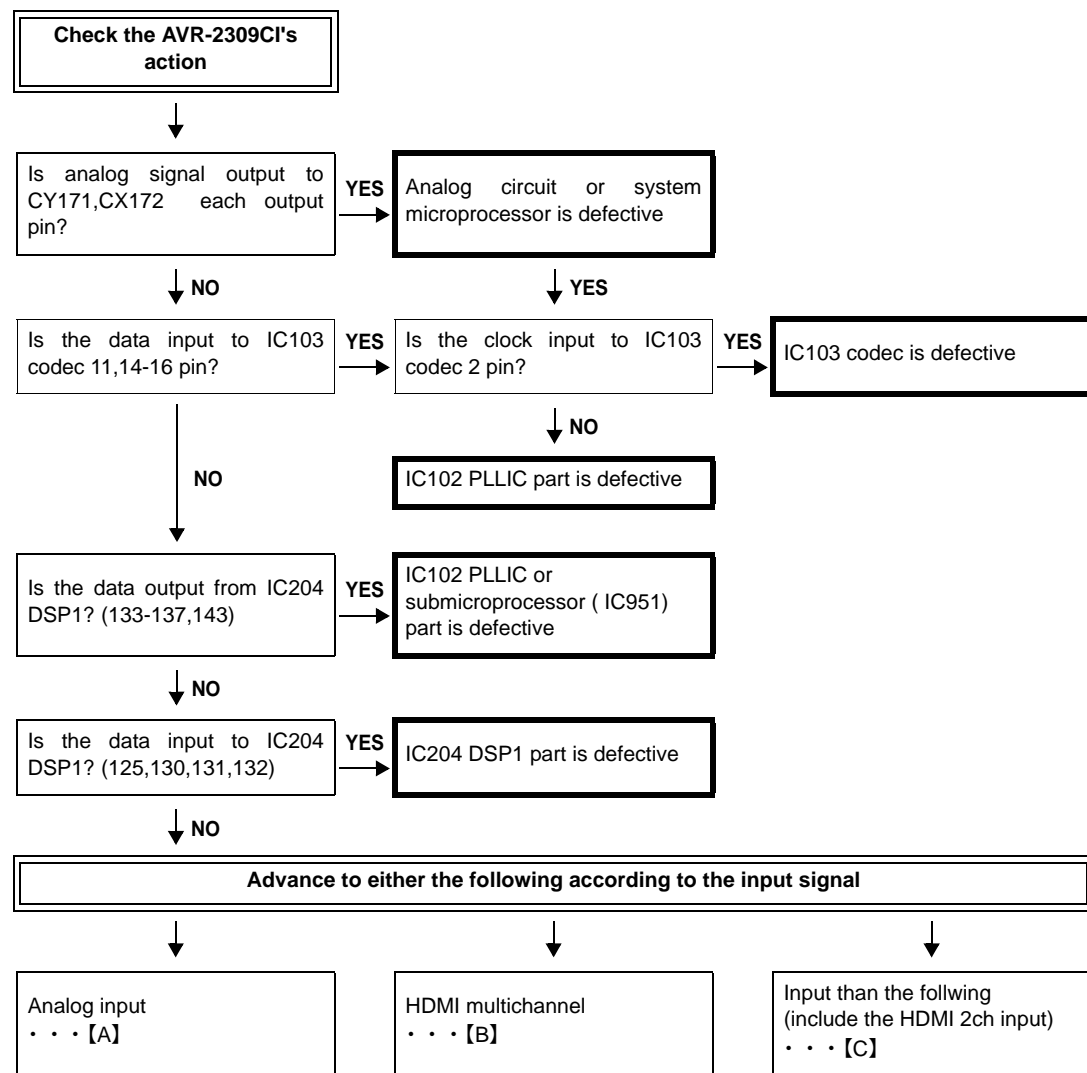


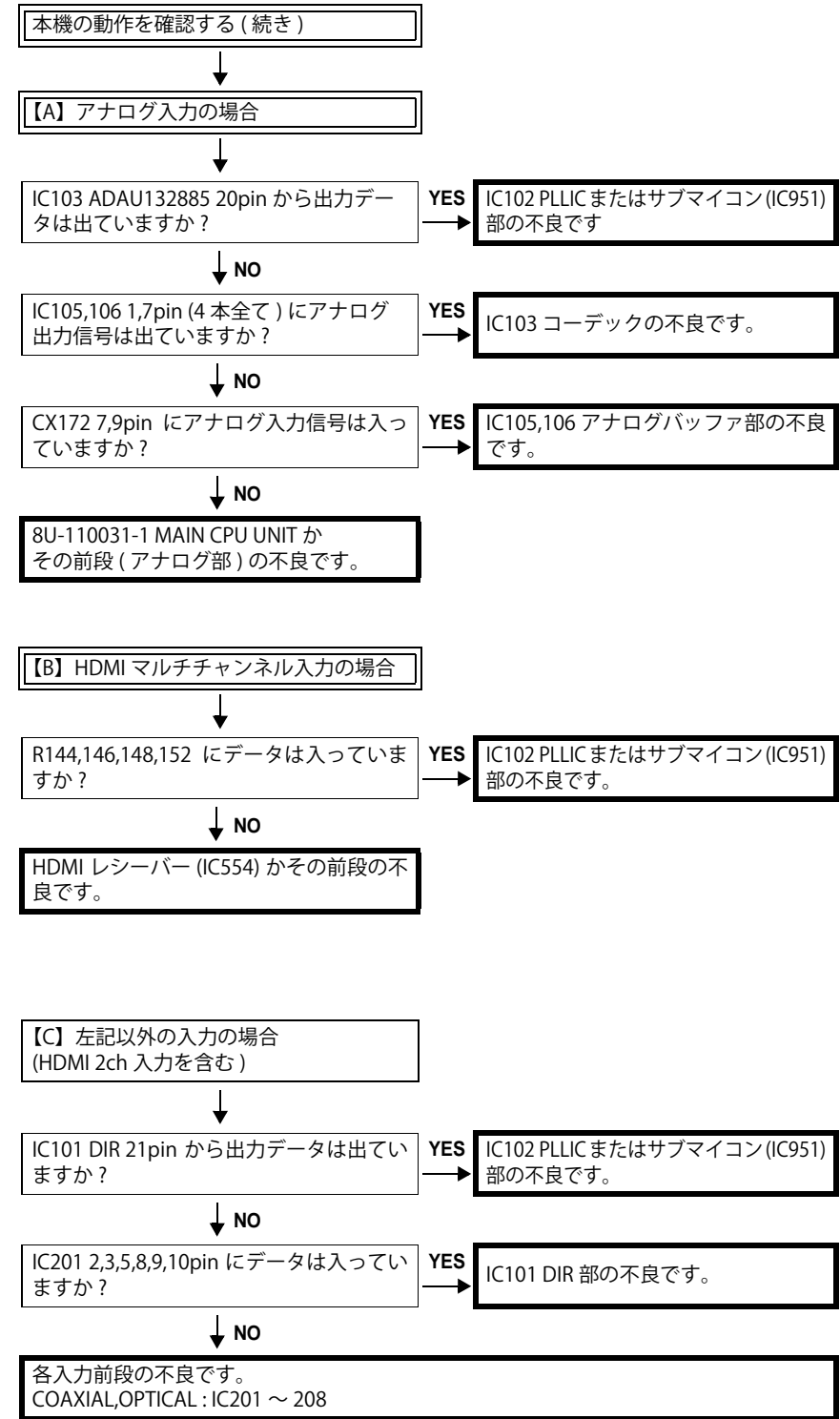
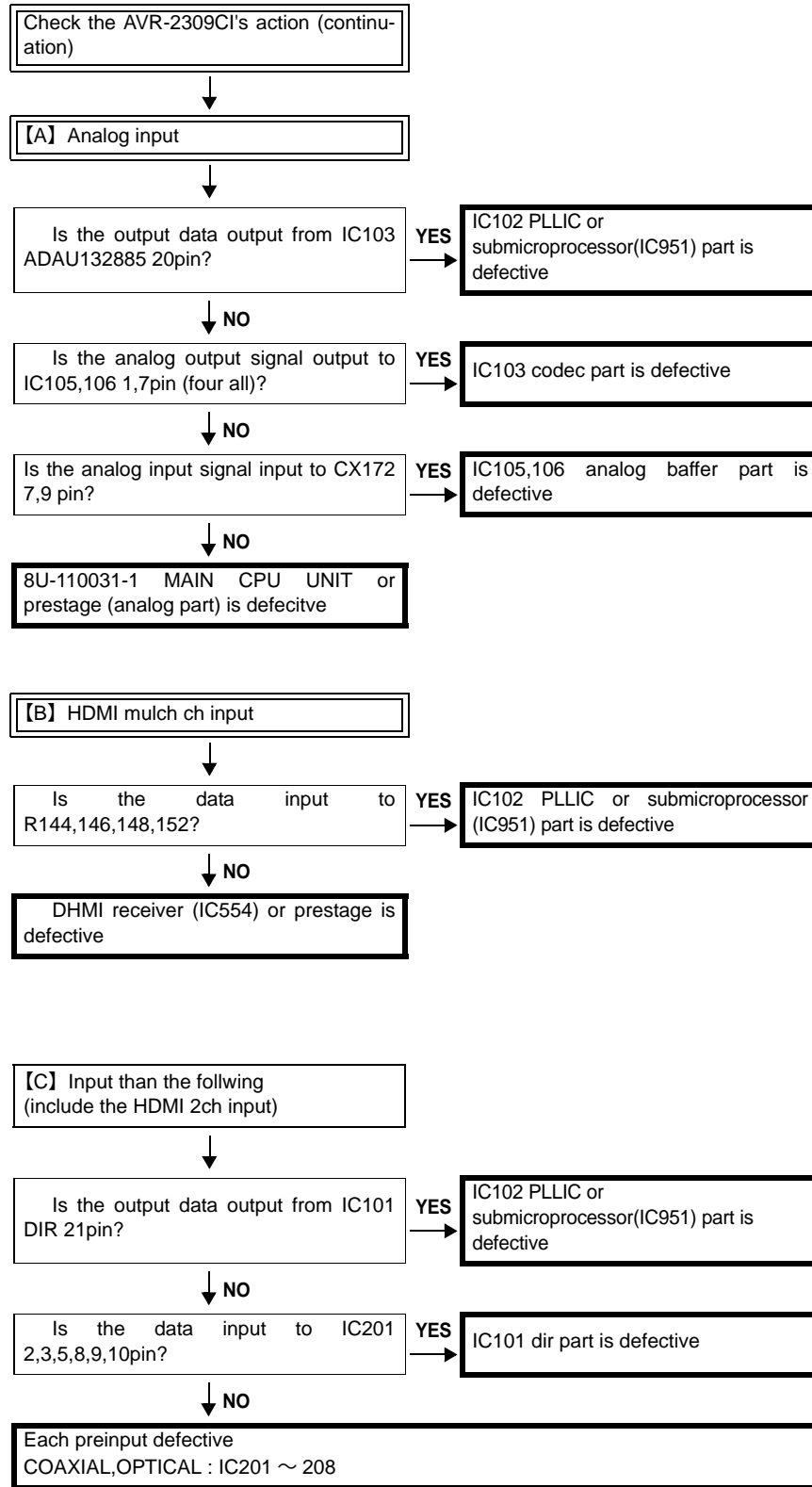
6. Digital Audio



6. デジタルオーディオ

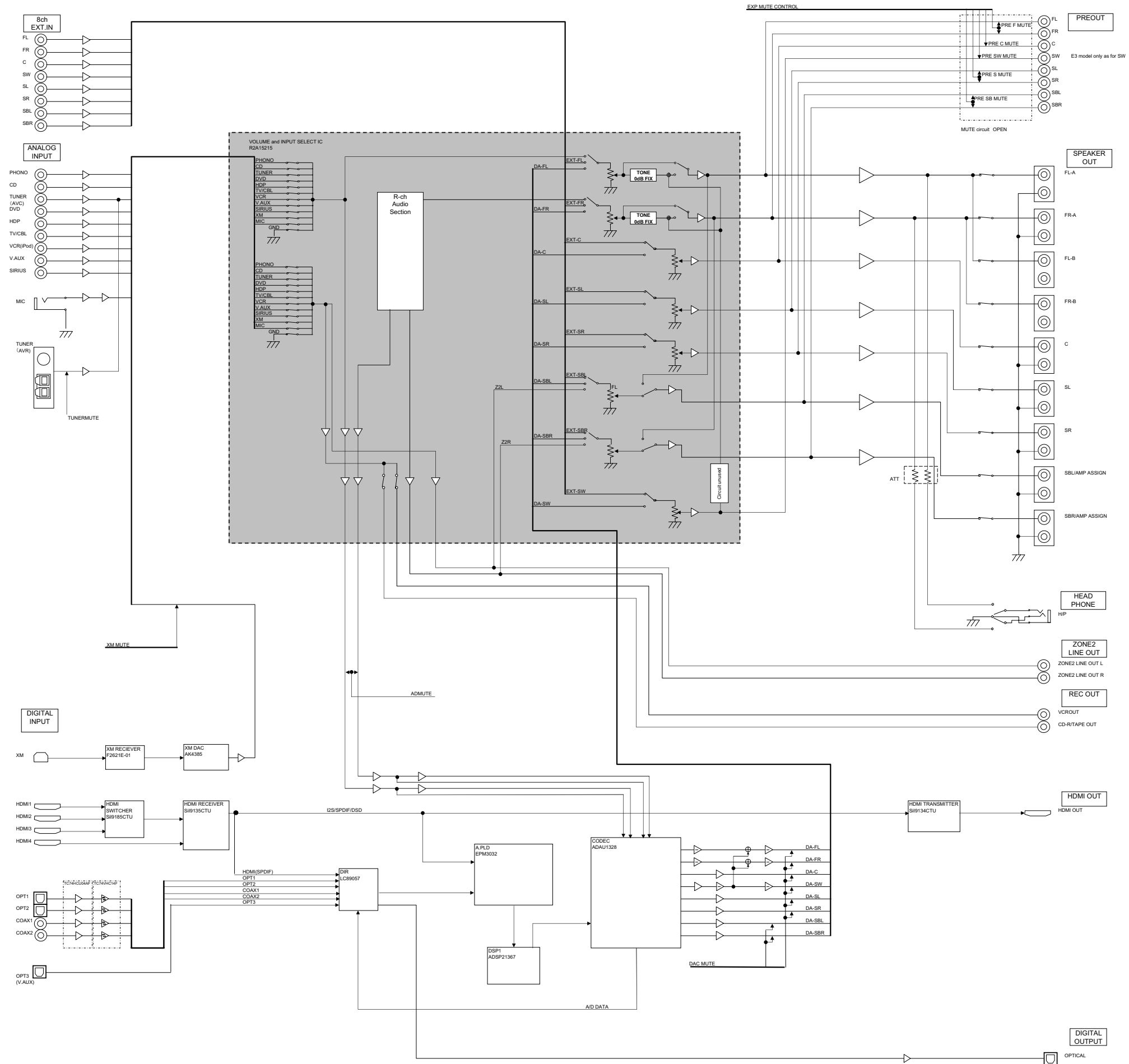






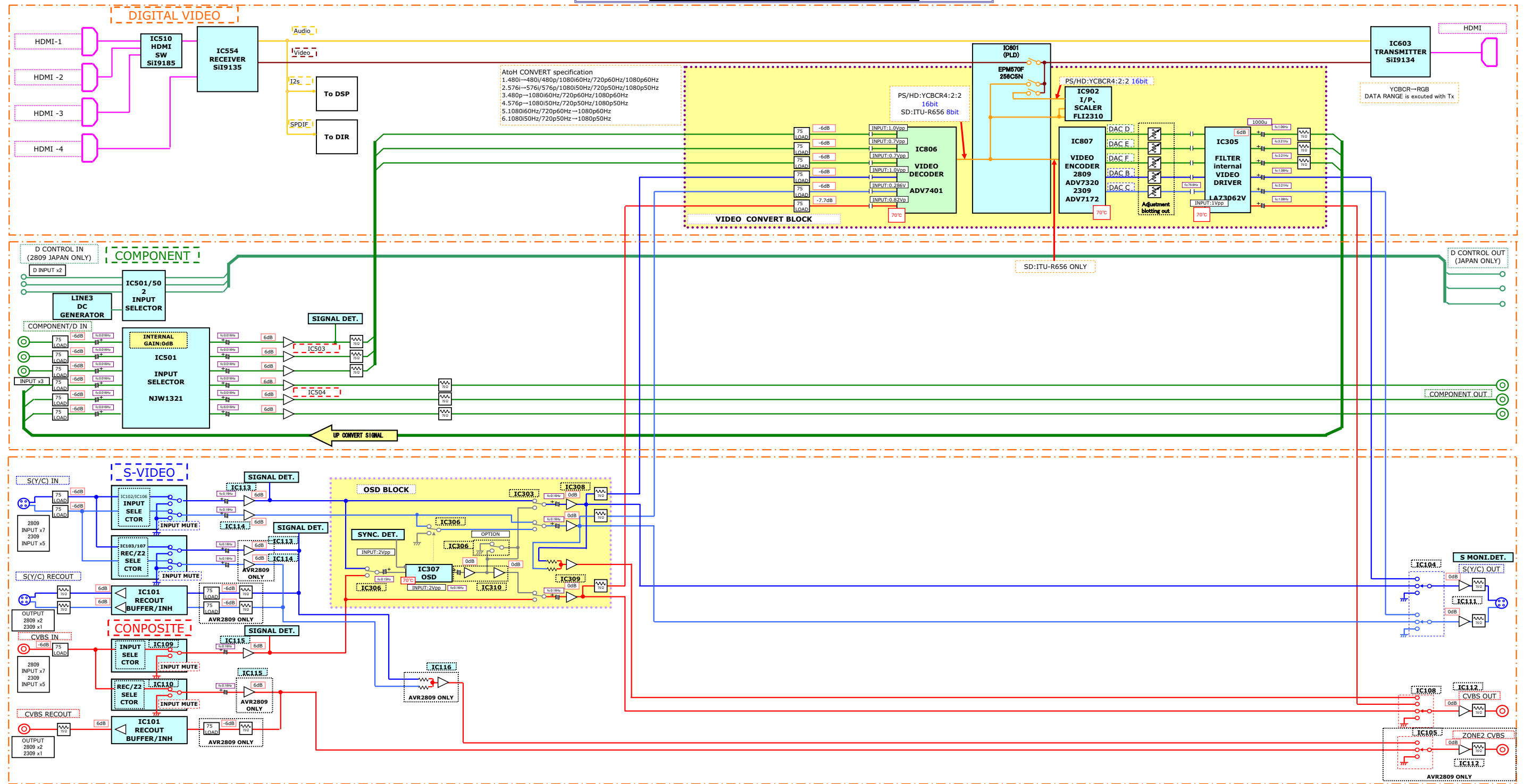
BLOCK DIAGRAMS (1/2)

AUDIO BLOCK DIAGRAM



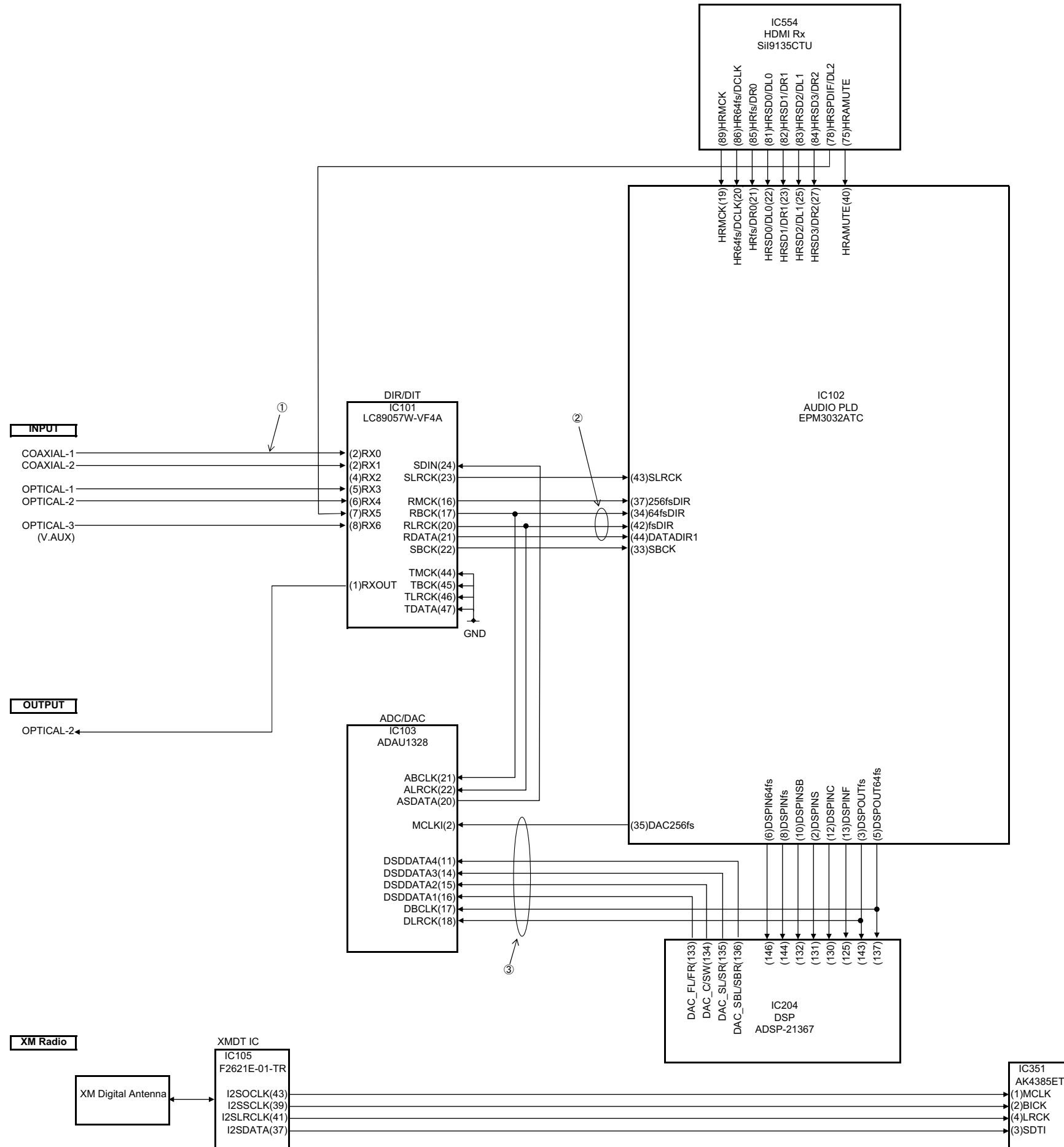
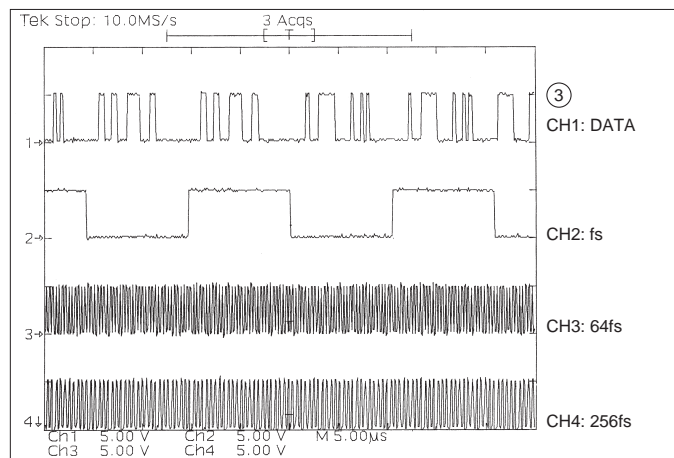
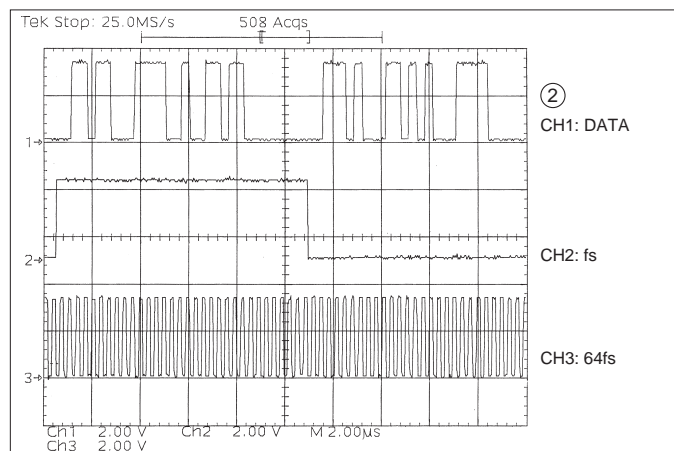
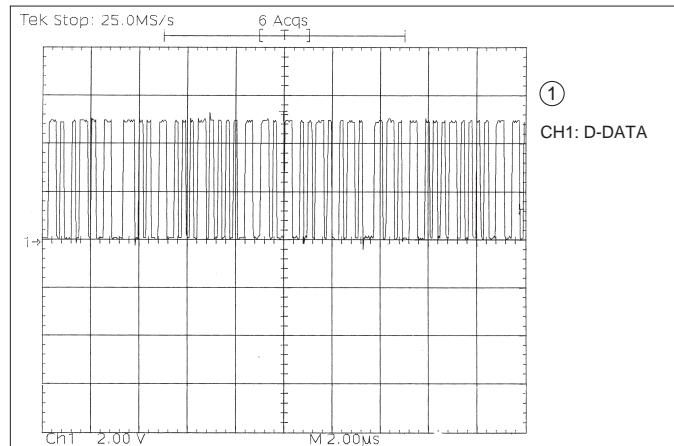
BLOCK DIAGRAMS (2/2) VIDEO BLOCK DIAGRAM

AVR-2809/2309 VIDEO BLOCK DIAGRAM



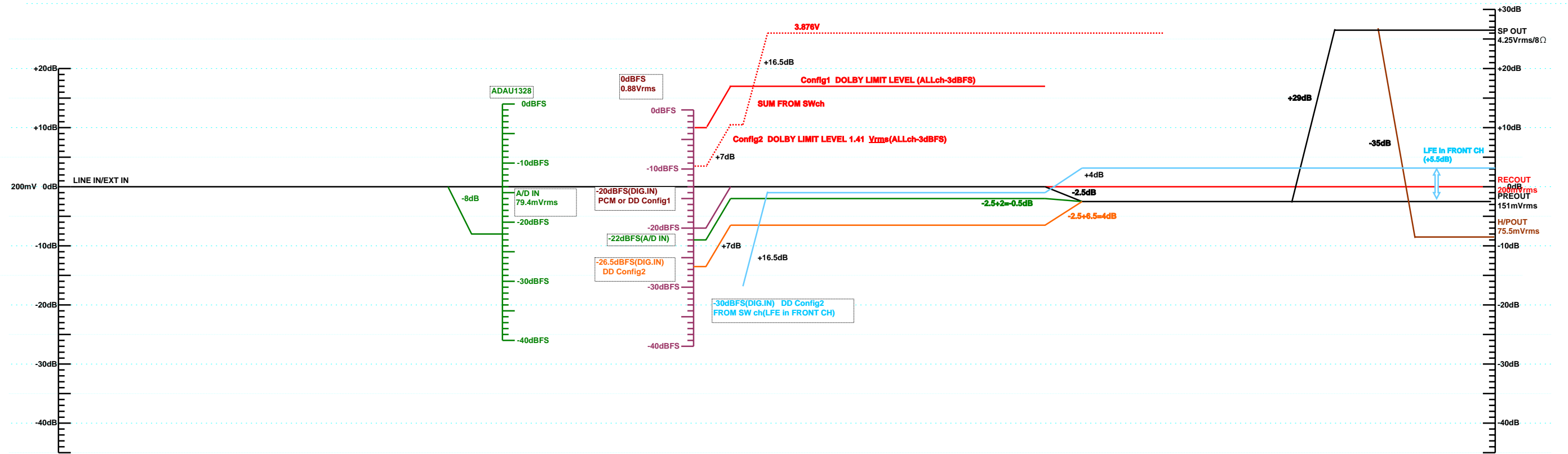
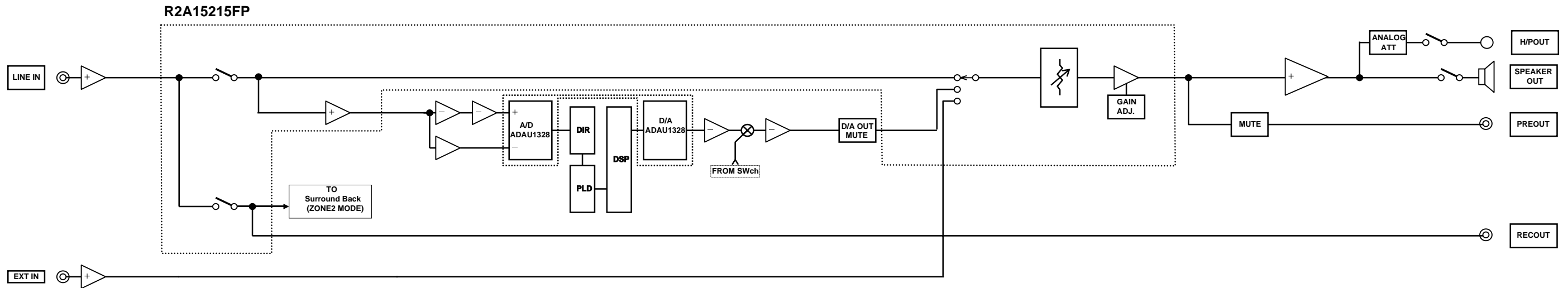
CLOCK FLOW & WAVE FORM IN DIGITAL BLOCK

Wave form

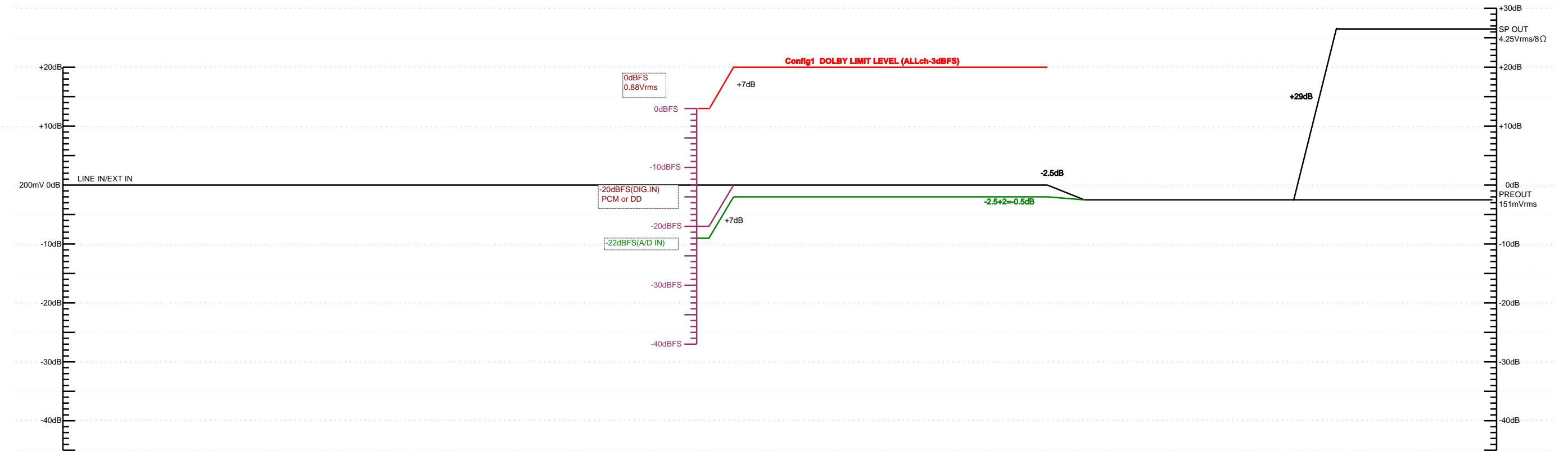
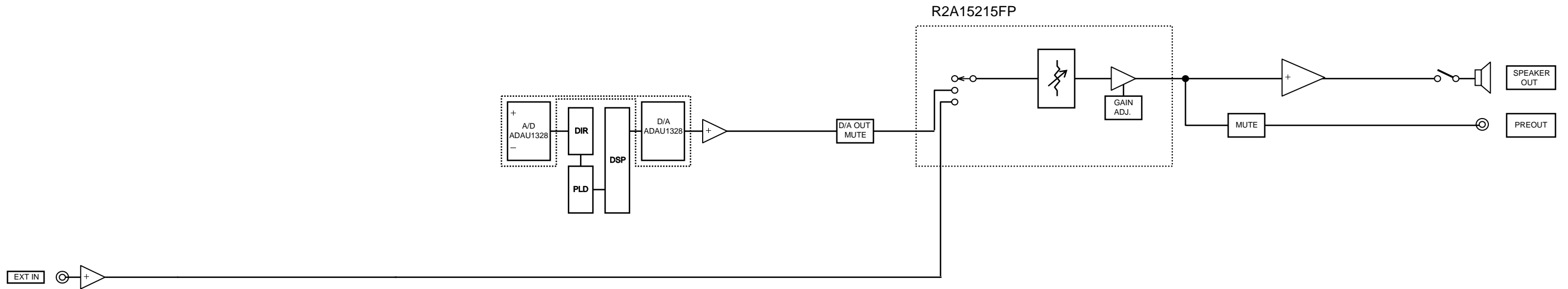


LEVEL DIAGRAMS (1/5)

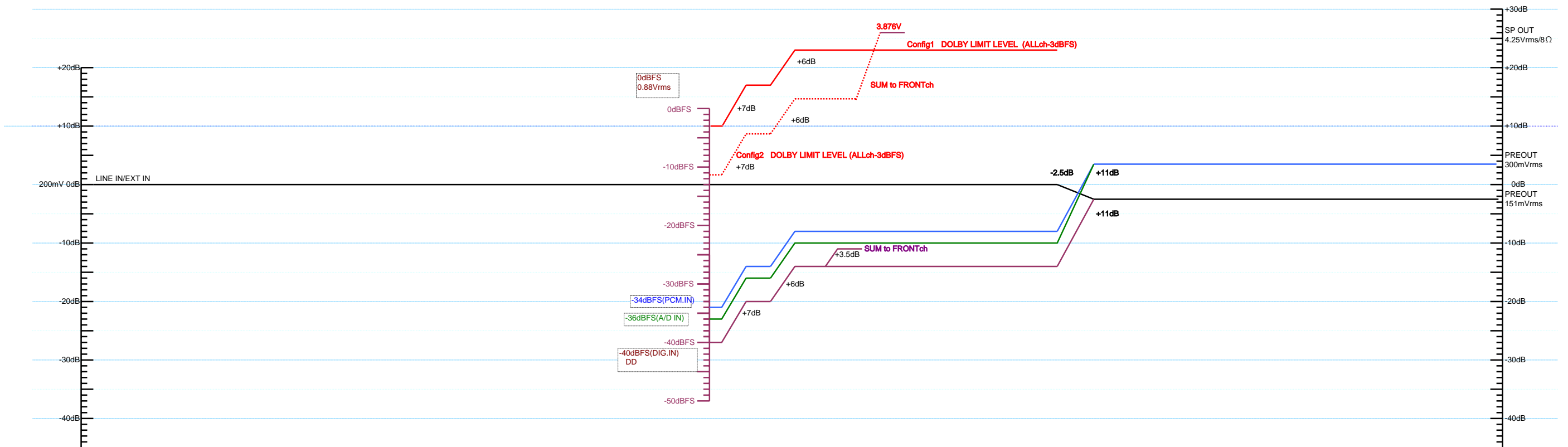
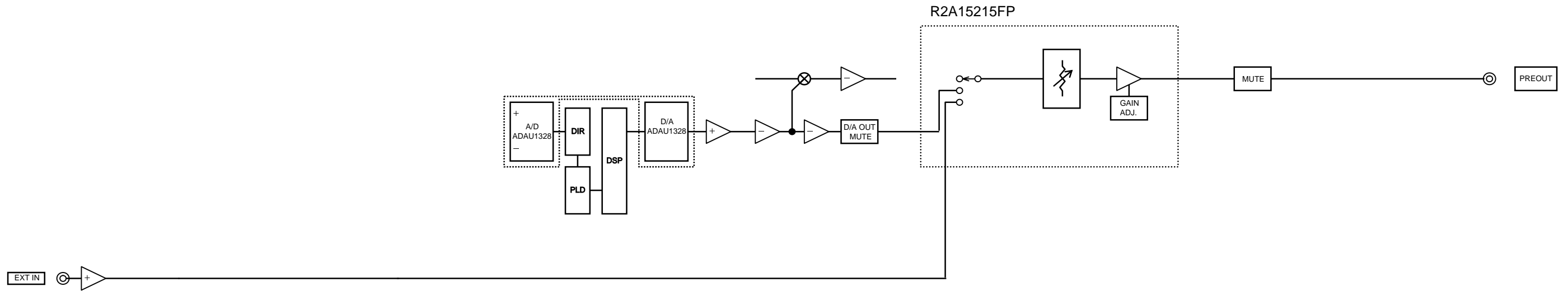
AVR-2309
LEVEL DIAGRAM
FRONT ch



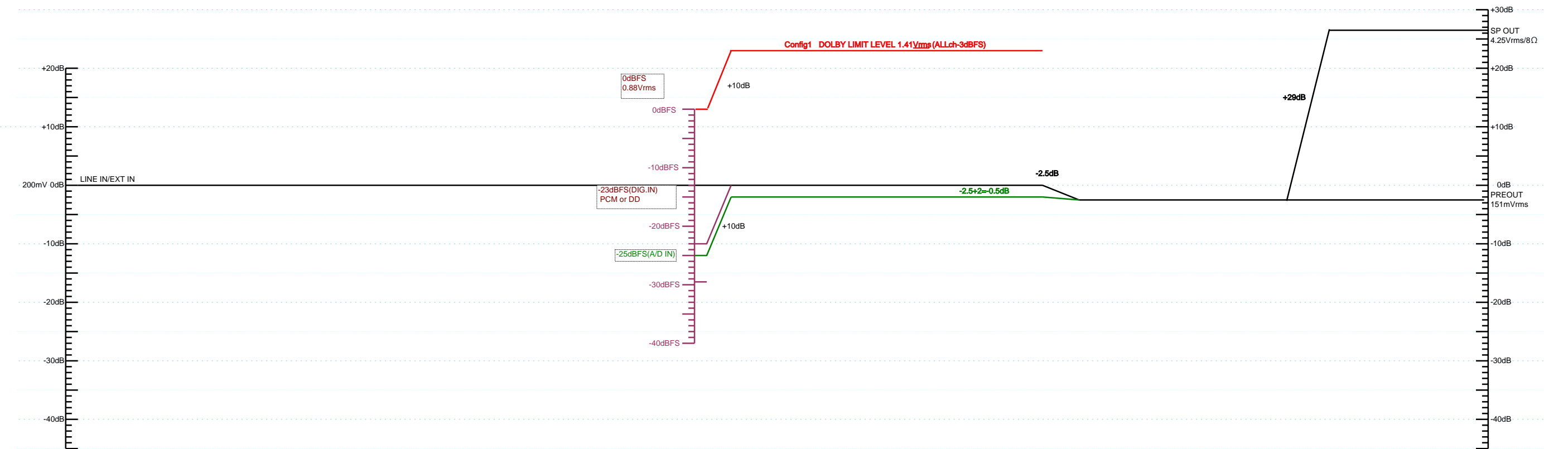
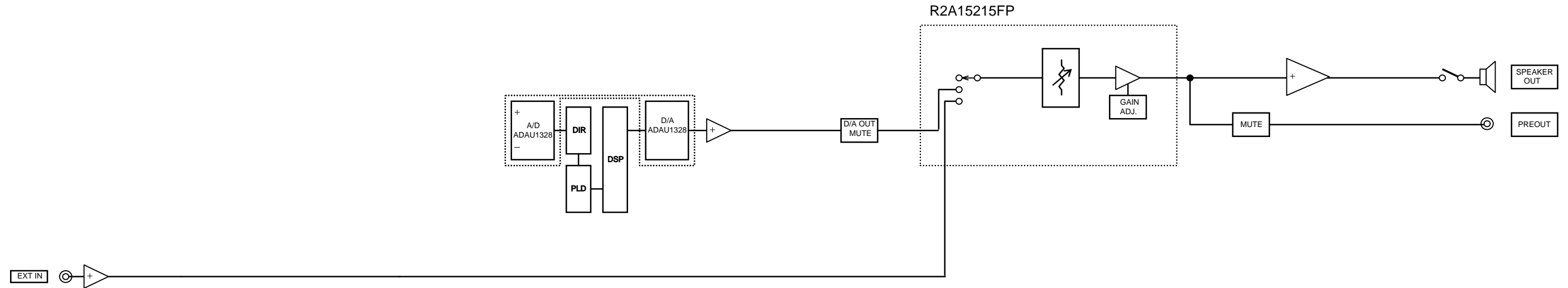
AVR-2309
LEVEL DIAGRAM
CENTER ch



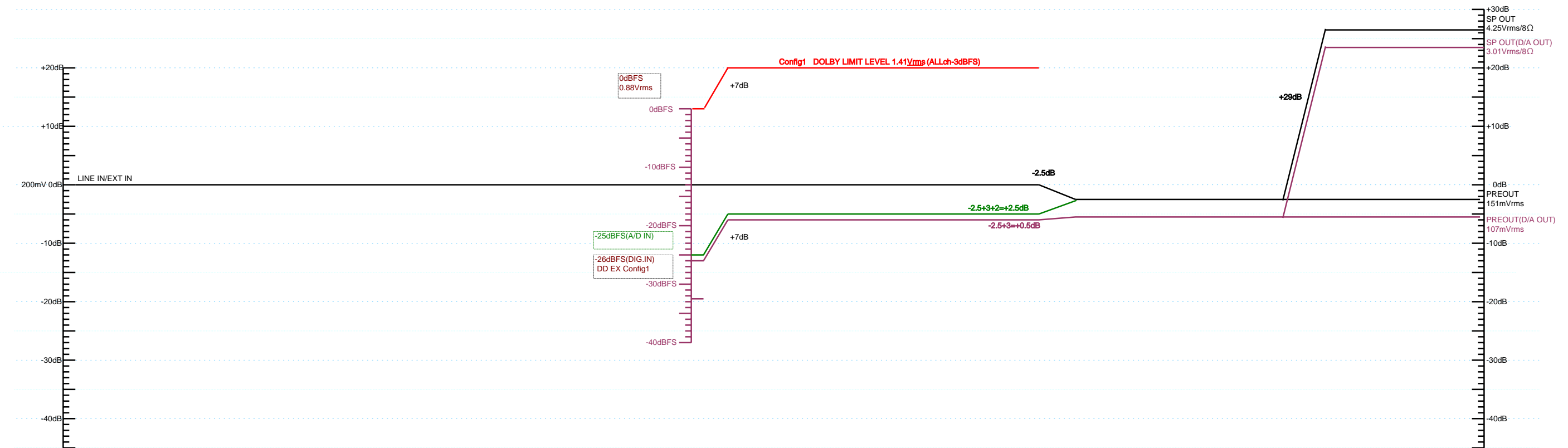
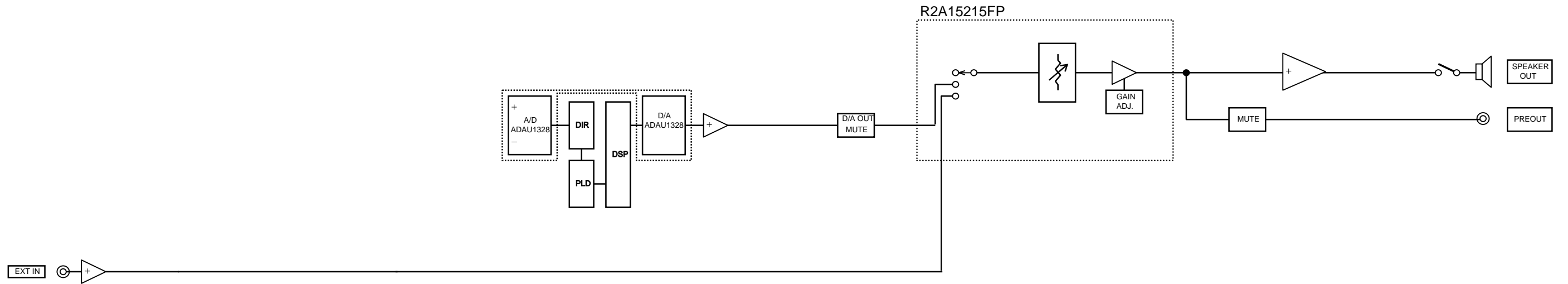
AVR-2309
LEVEL DIAGRAM
SUBWOOFER ch



AVR-2309
LEVEL DIAGRAM
SURROUND ch



AVR-2309
LEVEL DIAGRAM
SURR.BACK ch



SEMICONDUCTORS

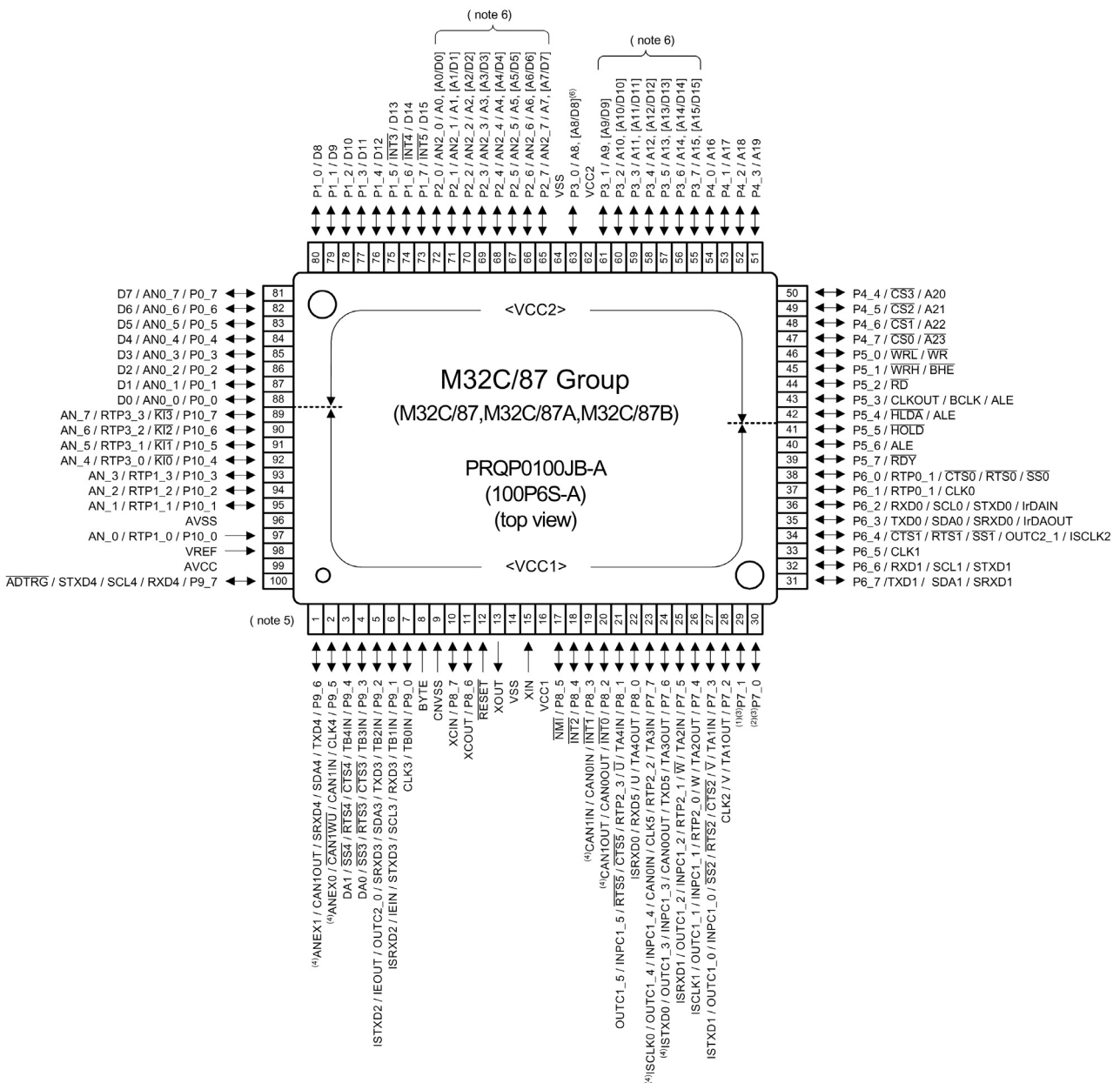
Only major semiconductors are shown, general semiconductors etc. are omitted to list.
 The semiconductor which described a detailed drawing in a schematic diagram are omitted to list.
 主な半導体を記載しています。汎用の半導体は記載を省略しています。
 回路図の中に詳細図がある半導体は記載を省略しています。

1. IC's

Note : Abbreviation ahead of IC No. indicates the name of P.W.B., etc.
 注) : IC No. の前の記号は、基板の名称を表します。

- | | |
|-------------------------|------------------------|
| DI : DIGITAL P.W.B. | FR : FRONT P.W.B. |
| AV : AUDIO VIDEO P.W.B. | MC : MAIN CPU P.W.B. |
| PA : POWER AMP P.W.B. | PR : POWER REG. P.W.B. |

M30879FLBFP (MC: IC105)



NOTES:

1. P7_1 / TA0IN / TB5IN / RTP0_3 / RXD2 / SCL2 / STXD2 / INPC1_7 / OUTC1_7 / OUTC2_2 / ISRXD2 / IEIN
2. P7_0 / TA0OUT / RTP0_2 / TXD2 / SDA2 / SRXD2 / INPC1_6 / OUTC1_6 / OUTC2_0 / ISTXD2 / IEOUT
3. P7_0 and P7_1 are N-channel open drain output ports.
4. The CAN pins cannot be used in M32C/87B. Only CAN0 pins can be used in M32C/87A.
5. Refer to **Package Dimensions** for the pin1 position on the package.
6. Pin names in brackets [] represent a single functional signal. They should not be considered as two separate functional signals.

M30879FLBFP Terminal Function

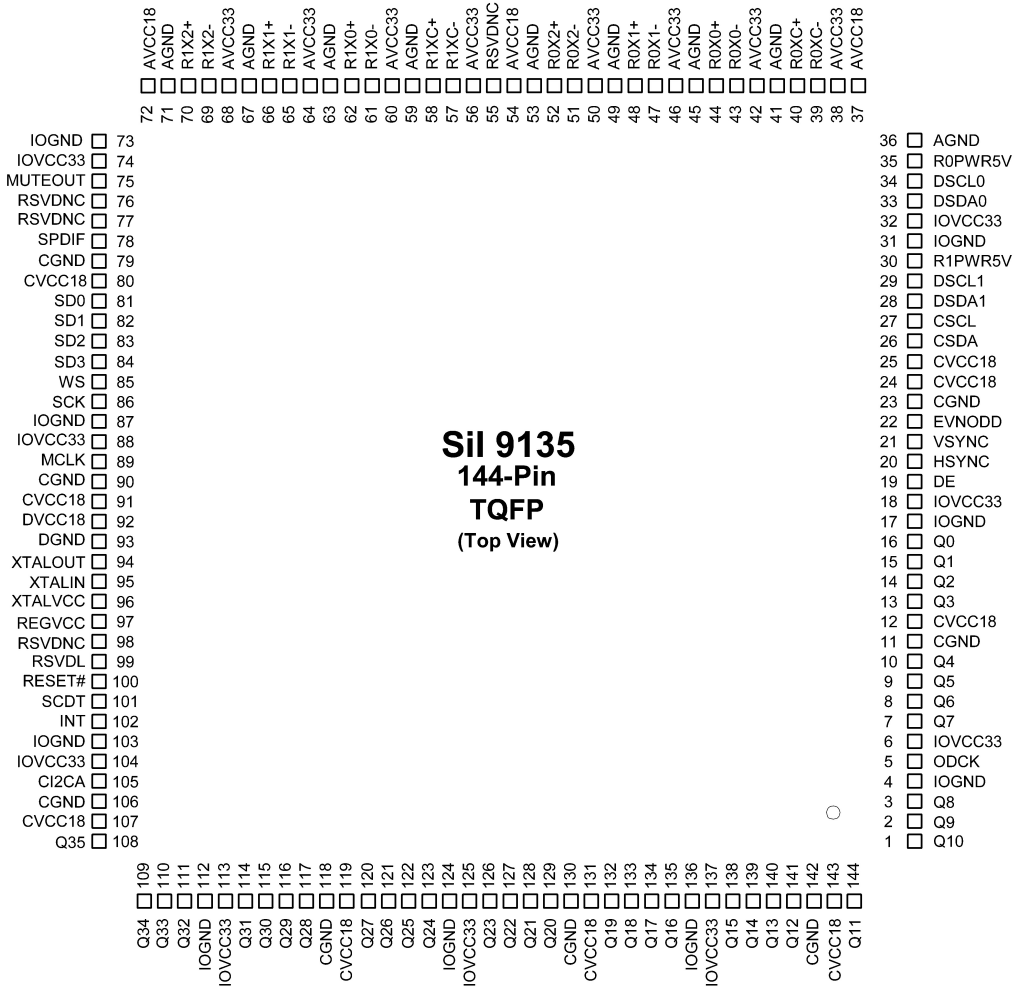
Pin	Pin Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	Stby	Stop	Function
1	P96/TXD4	SIRIUS TXD	O	C	-	-	-	Z	O/L	O/L	SIRIUS control pin
2	P95/CLK4	MICDET	I	-	Lv	-	Eu	Z	O/L	O/L	Microphone detect input (Detected : H)
3	P94/TB4	H/PDET	I	-	Lv	-	Eu	Z	O/L	O/L	HEADPHONE detect input (Detected : H)
4	P93/TB3	FL_DATA	O	C	-	-	-	Z	O/L	O/L	FLD DRIVER control pin
5	P92/SOUT3	MOSI	O	C	-	-	Ed	Z	O/L	O/L	MAIN-SUB μ com comm. control pin
6	P91/SIN3	SOMIm	I	-	Lv	-	-	Z	I	O/L	MAIN-SUB μ com comm. control pin
7	P90/CLK3	CLKMO	O	C	-	-	Ed	Z	O/L	O/L	MAIN-SUB μ com comm. control pin
8	BYTE	BYTE	I	-	-	-	-	-	-	-	MAIN-SUB μ com comm. control pin
9	CNVCS	CNVSS	I	-	-	-	Ed	Z	I	I	UP GRADE PIN
10	P87	FL_RST	O	C	-	-	-	Z	O/L	O/L	FLD DRIVER Reset control pin
11	P86	GRNLED	O	C	-	-	-	Z	O/L	O/L	STBYLED GREEN control pin
12	RESET	RESET	I	-	Lv	-	Eu	L	I	I	u-COM RESET SIGNAL INPUT
13	XOUT	XOUT	O	-	-	-	-	-	O/L	O/L	OSILATOR CONNECTION
14	VSS	VSS	-	-	-	-	-	-	-	-	GND
15	XIN	XIN	I	-	-	-	-	-	I	I	OSILATOR CONNECTION
16	VCC	VCC	-	-	-	-	-	-	-	-	POWER 5V
17	P85/NMI	NMI	I	-	-	-	-	-	-	-	5V
18	P84/INT2	PROTECTION	I	-	E ↓ &L	-	Eu	Z	I	I	PROTECTION SIGNAL INPUT
19	P83/INT1	POWERKEY	I	-	Lv	-	Eu	Z	I	I	MAIN POWER relay control output
20	P82/INT0	REMOTEDET	I	-	Lv	-	Ed	Z	O/L	O/L	ROOM TO ROOM Signal detect pin (Detected : H)
21	P81	ISELB	I	-	-	-	Eu	Z	O/L	O/L	Input selector rotation detect input (Rotary encoder)
22	P80	VSELA	I	-	-	-	Eu	Z	O/L	O/L	Master Volume rotation detect input (Rotary encoder)
23	P77	SSELA	I	-	-	-	Eu	Z	O/L	O/L	Selector rotation detect input (Rotary encoder)
24	P76	-	O	C	-	-	-	Z	O/L	O/L	Not used
25	P75	HD AUDIO LED	O	C	-	-	-	Z	O/L	O/L	HD AUDIO LED control
26	P74	SSELB	I	-	-	-	Eu	Z	O/L	O/L	Selector rotation detect input (Rotary encoder)
27	P73/CTS2	VOLDATA	O	C	-	-	-	Z	O/L	O/L	Volume control pin
28	P72/CLK2	VOLCLK	O	C	-	-	-	Z	O/L	O/L	Volume control pin
29	P71/RXD2	RXDMIXO	I	-	-	-	Ed	Z	I	O/L	XM RADIO control pin
30	P70/TXD2	TXDMOXMI	O	N	-	-	Eu	Z	O/L	O/L	XM RADIO control pin
31	P67/TXD1	MO232CI	O	C	-	-	-	Z	O/L	O/L	RS232C SIGNAL OUTPUT
32	P66/RXD1	MI232CO	I	-	-	-	Ed	Z	I	O/L	RS232C SIGNAL INPUT
33	P65/CLK1	EXPCLK	O	C	-	-	-	Z	O/L	O/L	Extended IC control pin
34	P64/CTS1	EXPDATA	O	C	-	-	-	Z	O/L	O/L	Extended IC control pin
35	P63/TXD0	MOIPO	O	C	-	-	-	Z	O/L	O/L	iPod control pin
36	P62/RXD0	MIIPO	I	-	-	-	Ed	Z	I	O/L	iPod control pin
37	P61/CLK0	VSELB	I	-	-	-	Eu	Z	O/L	O/L	Master Volume rotation detect input (Rotary encoder)
38	P60/CTS0	ISELA	I	-	-	-	Eu	Z	O/L	O/L	Input selector rotation detect input (Rotary encoder)
39	P57	REDLED	O	C	-	-	-	Z	O/H	O/L	STBY LED RED CONTROL
40	P56	FL_CE1	O	C	-	-	-	Z	O/L	O/L	FLD DRIVER control pin
41	P55/EPM	FRASH CE/FL_CLK	O	C	-	-	-	Z	O/L	O/L	Rewrite boot program start : L input set /FLD DRIVER control pin
42	P54	M232CPOWER	O	C	-	-	Ed	Z	O/L	O/L	RS232C POWER control pin (STANDBY:H)
43	P53	DYN GRN LED	O	C	-	-	-	Z	O/L	O/L	DYNAMIC VOLUME LED GREEN control
44	P52	DYN RED LED	O	C	-	-	-	Z	O/L	O/L	DYNAMIC VOLUME LED RED control
45	P51	TRIGGER1	O	C	-	-	-	Z	O/L	O/L	TRIGGER OUT 1 control pin
46	P50/CE	FRASH CE	O	C	-	-	-	Z	O/L	O/L	Rewrite boot program start : H input set
47	P47	RDSOUT	I	-	-	-	Eu	Z	O/L	O/L	RDS DETECT IN control pin
48	P46	TURDSCLK(CKTU)	O	C	-	-	-	Z	O/L	O/L	TUNER/RDS CLOCK OUT
49	P45	TURSDATA(DATATU)	O	C	-	-	-	Z	O/L	O/L	TUNER/RDS DATA OUT control pin
50	P44	RDSCE	O	C	-	-	-	Z	O/L	O/L	RDS Chip enable
51	P43	RDSRST	O	C	-	-	-	Z	O/L	O/L	RDS reset output
52	P42	THERMAL	I	-	-	-	Ed	Z	O/L	O/L	Temperature detect
53	P41	EXPOE	O	C	-	-	-	Z	O/L	O/L	Extended IC control pin
54	P40	EXPSTB	O	C	-	-	-	Z	O/L	O/L	Extended IC control pin
55	P37	TUDOUT(DATAOUT)	I	-	Lv	-	Ed	Z	O/L	O/L	TUNING DATA INPUT control pin
56	P36	TUSTB	O	C	-	-	-	Z	O/L	O/L	TUNER STB OUT
57	P35	STEREO	I	-	Lv	-	Eu	Z	O/L	O/L	When TUNER FM stereo receive : L
58	P34	TUNED	I	-	Lv	-	Eu	Z	O/L	O/L	TUNER turned detect (Detected : L)
59	P33	IPDET	I	-	Lv	-	Eu	Z	O/L	O/L	MINI JACK connected detection pin for DOCK connection (H:DETECTIVE)

Pin	Pin Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	Stby	Stop	Function
60	P32	REMOTEPOWER	O	C	-	-	-	Z	O/L	O/L	REMOTE POWER control pin (ON : H)
61	P31	232C CONTROL	O	C	-	-	Ed	Z	O/L	O/L	232C control pin (MAIN : L / SUB : H)
62	VCC	VCC	-	-	-	-	-	-	-	-	+5V
63	P30	VOLPROTECT	I	-	E ↑ &H	-	Eu	Z	O/L	O/L	Voltage detection control pin
64	VSS	VSS	-	-	-	-	-	-	-	-	GND
65	P27	PRE POWER	O	C	-	-	-	Z	O/L	O/L	PRE POWER control pin (H : ON)
66	P26	SCPUPOWER	O	C	-	-	-	Z	O/L	O/L	SUB CPU POWER ON/OFF switcing (H : ON)
67	P25	XMPOWER	O	C	-	-	-	Z	O/L	O/L	XM RADIO POWER control pin
68	P24	POWER	O	C	-	-	Ed	Z	O/L	O/L	MAIN POWER relay control output (ON : H)
69	P23	CPU/EPOWER	O	C	-	-	Ed	Z	O/L	O/L	MAIN CPU POWER control pin (POWER ON : H)
70	P22	LIMIT	O	C	-	-	-	Z	O/L	O/L	LIMIT control
71	P21	-	O	C	-	-	-	Z	O/L	O/L	Not used
72	P20	-	O	C	-	-	-	Z	O/L	O/L	Not used
73	P17/INT5	REMOCOM	I	-	E ↑ &H	-	Ed	Z	I	I	Remote control signal input
74	P16/INT4	REQSOMIm	I	-	E ↓ &L	-	Ed	Z	I	O/L	MAIN-SUB Épcom comm. control pin
75	P15/INT3	B.DOWN	I	-	E ↓ &L	-	Eu	Z	I	I	Power down detect (Power down : L)
76	P14/D12	RST SUB	O	C	-	-	-	Z	O/L	O/L	SUB µcom Reset control pin
77	P13/D11	LIMITDET	I	-	Lv	-	Eu	Z	O/L	O/L	Signal detect input (Detected : H)
78	P12/D10	-	O	C	-	-	Ed	-	O/L	O/L	Not used
79	P11/D9	-	O	C	-	-	-	-	O/L	O/L	Not used
80	P10/D8	VOLMUTE	O	C	-	-	-	Z	O/L	O/L	VOLUME MUTE control pin
81	P07/D7	MUTEPOWER	O	C	-	-	-	Z	O/L	O/L	For MUTE +B control pin
82	P06/D6	SYNCDDET	I	-	Lv	-	Ed	Z	O/L	O/L	Sync. detect input for MAIN(H: Ext. synchronized)
83	P05/D5	OSDMUTE	O	C	-	-	-	Z	O/L	O/L	OSD control pin
84	P04/D4	-	O	C	-	-	-	Z	O/L	O/L	Not used
85	P03/D3	OSDRST	O	C	-	-	-	Z	O/L	O/L	OSD control pin
86	P02/D2	OSDSTR	O	C	-	-	-	Z	O/L	O/L	OSD control pin
87	P01/D1	OSDCLK	O	C	-	-	-	Z	O/L	O/L	OSD control pin
88	P00/D0	OSDDATA	O	C	-	-	-	Z	O/L	O/L	OSD control pin
89	P103/AN3	KEY1	I	-	Lv	-	Eu	Z	O/L	O/L	KEY1 SIGNAL INPUT
90	P102/AN2	KEY2	I	-	Lv	-	Eu	Z	O/L	O/L	KEY2 SIGNAL INPUT
91	P101/AN1	KEY3	I	-	Lv	-	Eu	Z	O/L	O/L	KEY3 SIGNAL INPUT
92	P104/AN4	ACKSUB	O	C	-	-	Ed	Z	O/L	O/L	MAIN-SUB µcom comm. control pin
93	P107/AN7	XMOLINKACTIVE	I	-	-	-	Ed	Z	O/L	O/L	XM RADIO control pin
94	P106/AN6	XMOANTREV	I	-	E ↓ &L	-	Ed	Z	O/L	O/L	XM RADIO control pin
95	P105/AN5	XMIRESET	O	C	-	-	Eu	Z	O/L	O/L	XM RADIO RESET control pin
96	AVSS	AVSS	-	-	-	-	-	-	-	-	GND
97	P100/AN0	SET_OPTION	I	-	Lv	-	-	Z	O/L	O/L	SET OPTION SELECT
98	VREF	VREF	-	-	-	-	-	-	-	-	VREF
99	AVCC	AVCC	-	-	-	-	-	-	-	-	POWER 5V
100	P97/RXD4	SIRIUS RXD	I	-	-	-	Ed	Z	O/L	O/L	SIRIUS control pin

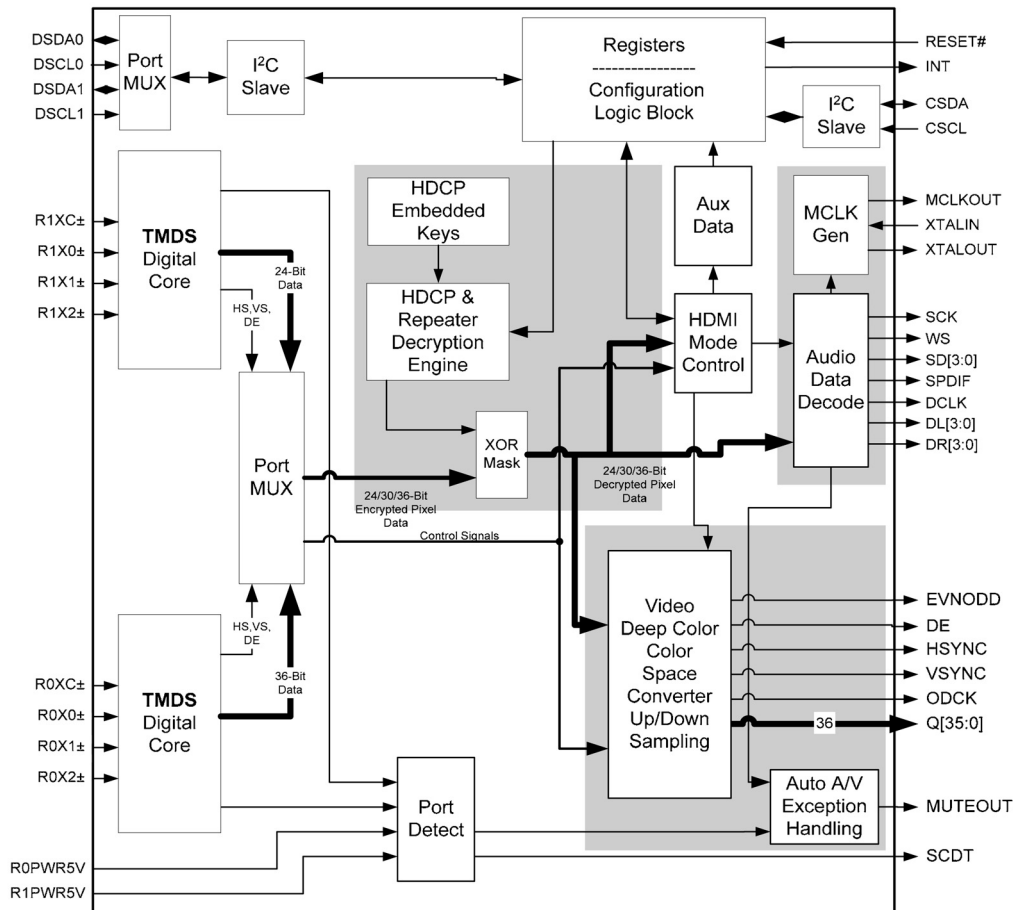
Note: Pin No. : Terminal number of microcomputer.
Port Name : The name entered in the data sheet of microcomputer.
Symbol : Symbolized interface function.
I/O : Input or out of part.
Type : Composition of port in case of output port.
Op : Pull up/Pull down selection information.
Det : Indicates judging state of input port. Level detection is "LV"; Edge detection is "Ed"; Detection by both shifting is "E&L";
Res : State at reset.
STBY : State of port when STANDBY mode.
Stop : State of port when Stop mode.

"I" = Input port
"O" = Output port
"C" = CMOS output
"N" = NMOS open drain output
"P" = PMOS open drain output
"Lu" = Inner microcomputer pull up
"Ld" = Inner microcomputer pull down
"Eu" = External microcomputer pull up
"Ed" = External microcomputer pull down
"H" = Outputs High Level at reset
"L" = Outputs Low Level at reset
"Z" = Becomes High impedance mode at reset
"O/L" = Output port and "L"
"I" = Input port
"O/L" = Output port and "L"
"I" = Input port

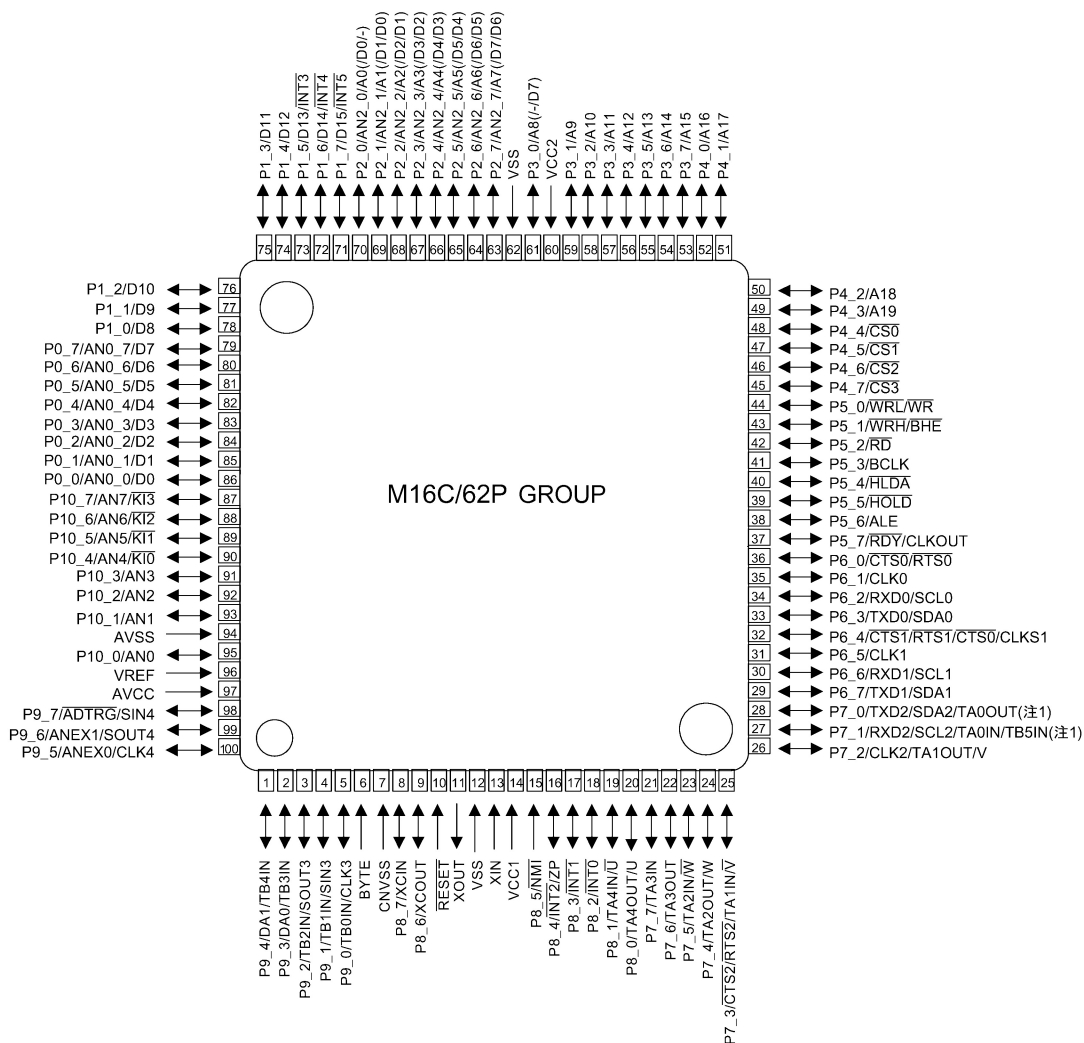
Sil9135CTU (DI : IC554)



Functional Block Diagram



M3062LFGPGP (DI: IC951)



M3062LFGPGP Terminal Function

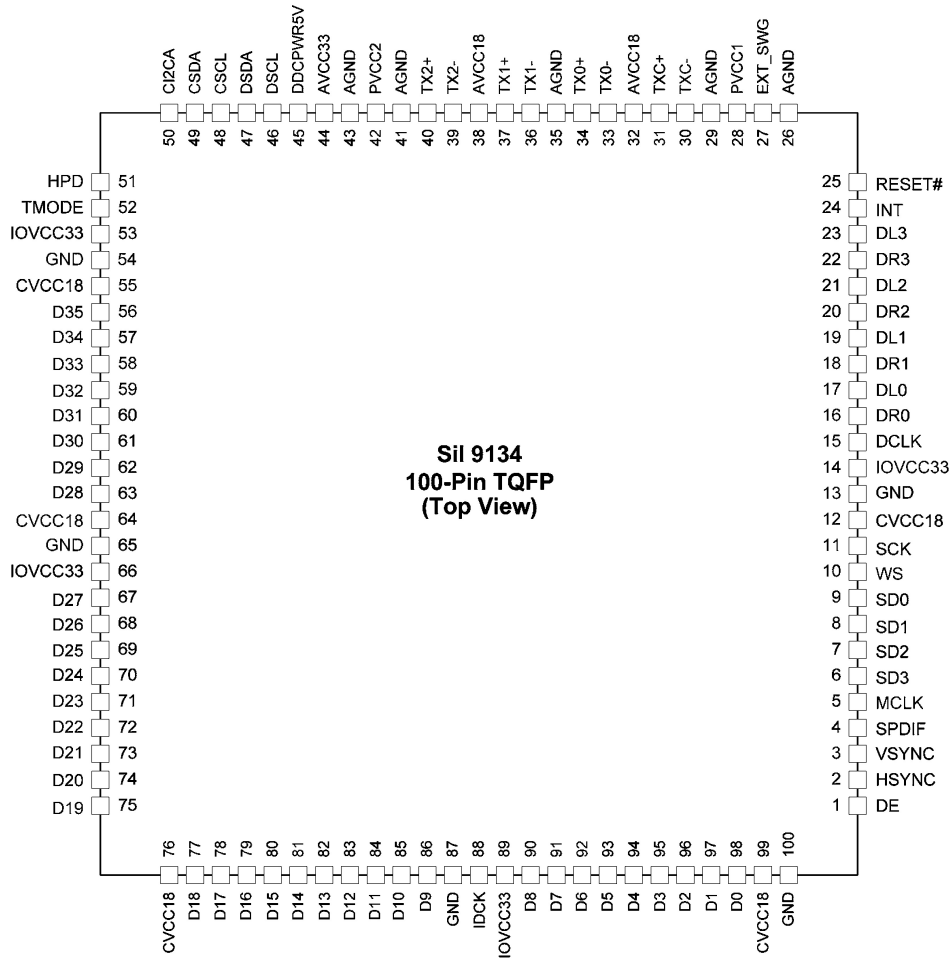
Pin	Pin Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	Function
1	P94/TB4	VPLD DATA	O	C	-	-	-	Z	VIDEO PLD control pin
2	P93/TB3	DIR CE	O	C	-	-	-	Z	DIR control pin(LC89057W-VF4A)
3	P92/SOUT3	DIR DIN	O	C	-	-	-	Z	DIR control pin(LC89057W-VF4A)
4	P91/SIN3	DIR DOUT	I	-	Lv	-	Eu	Z	DIR control pin(LC89057W-VF4A)
5	P90/CLK3	DIR CLK	O	C	-	-	-	Z	DIR control pin(LC89057W-VF4A)
6	BYTE	BYTE	-	-	-	-	-	-	GND(Ext. data bus bit width switching, 16bit:L)
7	CNVCS	CNVSS	-	-	-	-	-	-	Single-chip/Micro-processor mode switching(Normal single-chip:L, Rewrite boot program start:H input set)
8	P87	VERST	O	C	-	-	Eu	Z	Reset for VIDEO ENCODER(ADV7172)
9	P86	VDRST	O	C	-	-	Eu	Z	Reset for VIDEO DECODER(ADV7401)
10	RESET	SUBRESET	I	-	Lv	-	Eu	L	Reset input
11	XOUT	X1	O	-	-	-	-	-	Oscillator connection
12	VSS	VSS	-	-	-	-	-	-	GND
13	XIN	X2	I	-	-	-	-	-	Oscillator connection
14	VCC	VCC	-	-	-	-	-	-	+3.3V
15	P85/NMI	NMI	I	-	-	-	-	-	Not used(Fixed to H)
16	P84/INT2	CEC_IN	I	-	E ↓ &L	-	Eu	Z	CEC-D signal input pin
17	P83/INT1	ACKSIMO	I	-	E ↓ &L	-	Ed	Z	MAIN-SUB μcom comm. control input pin("L" return from MAIN μcom)
18	P82/INT0	SUB BDOWN	I	-	E ↓ &L	-	Eu	Z	Power down detect(Power down:L)
19	P81	IP RST	O	C	-	-	-	Z	IP CONV(FLI2310) reset
20	P80	-	I	-	-	-	Ed	Z	Not used
21	P77	SICODECO	I	-	-	-	-	Z	CODEC (ADAU1328) control pin
22	P76	CPU_MUTE/TMS	O	C	-	-	-	Z	MAIN PLD DAC MUTE control pin/PLD rewrite control(JTAG)
23	P75	APLDSEL1/TDI	O	C	-	-	-	Z	MAIN PLD control pin/PLD rewrite control(JTAG)

Pin	Pin Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	Function
24	P74	MTCK	O	C	-	-	-	Z	PLD rewrite control(JTAG)
25	P73/CTS2	VIDEO_POWER	O	C	-	-	-	Z	VIDEO Power ON/OFF switching(H:ON)
26	P72/CLK2	DAC_POWER	O	C	-	-	Ed	Z	DIGITAL Power ON/OFF switching(H:ON)
27	P71/RXD2	VSCL	I/O	N	-	-	Eu	Z	VIDEO I2C- IP CONV(FLI2310)/V_ENCODER(ADV7172)/V_DECODER(ADV7401)/COMPONENT SELECT IC(NJW1321FP1) control IC
28	P70/TXD2	VSDA	I/O	N	-	-	Eu	Z	VIDEO I2C- IP CONV(FLI2310)/V_ENCODER(ADV7172)/V_DECODER(ADV7401)/COMPONENT SELECT IC(NJW1321FP1) control IC
29	P67/TXD1	TXD	O	C	-	-	Eu	Z	Data transmission output to outside
30	P66/RXD1	RXD	I	-	Lv	-	Eu	Z	Data transmission input from outside
31	P65/CLK1	SW SUM	O	C	-	-	Ed	Z	Additional instructions to Front of an SW signal(H:ON)
32	P64/CTS1	HDMIPOWER	O	C	-	-	-	Z	HDMI POWER control pin(H:ON)
33	P63/TXD0	SOMI	O	C	-	-	-	Z	MAIN-SUB μ com comm. control pin
34	P62/RXD0	SIMO	I	-	-	-	Ed	Z	MAIN-SUB μ com comm. control pin
35	P61/CLK0	CLKSIMO	I	-	-	-	Ed	Z	MAIN-SUB μ com comm. control pin
36	P60/CTS0	REQSOMI	O	C	-	-	Ed	Z	MAIN-SUB μ com comm. control pin
37	P57	1TMDSSWRST	O	C	-	-	-	Z	Sil9185 Reset pin
38	P56	HDP2	O	C	-	-	-	Z	HD DET control pin
39	P55/EPM	ADPDOWN/AUTH	I	C	-	-	Ed	Z	Rewrite boot program start : L input set
40	P54	CEC_OUT	O	C	-	-	-	Z	CEC-D signal output pin
41	P53	MONIDIS	O	C	-	-	-	Z	COMPONENT MONITOR OUT output control pin
42	P52	VCR2INH (CDR)	O	C	-	-	-	Z	Not used
43	P51	VCR1INH (VCR)	O	C	-	-	-	Z	VCR1OUT output INH control (L:MUTE)
44	P50/CE	WP4/(AVMUTE)	O/I	-	-	-	Eu	Z	Write Protect control / Rewrite boot program start : H input set
45	P47	HS_INT	I	-	E \downarrow & L	-	Eu	Z	HDMI IN SEL(Sil9185) INT output
46	P46	DSPPWR	O	C	-	-	Ed	Z	H:DSP Power ON
47	P45	HDP1	O	C	-	-	Ed	Z	HP DET control pin
48	P44	P.SAVE	O	-	-	-	Ed	Z	COMPONENT CONVERT output control pin
49	P43	HRINT	I	C	E \downarrow & L	-	-	Z	HDMI RECEIVER(Sil9031)INT output
50	P42	HSCL/EDID SCL	I/O	C	-	-	Eu	Z	VIDEO I2C/HDMI EDIT(E2PROM) control pin
51	P41	HSDA/EDID SDA	I/O	C	-	-	Eu	Z	VIDEO I2C/HDMI EDIT(E2PROM) control pin
52	P40	Z1SMONIA	O	C	-	-	-	Z	Z1 SMONITOR select
53	P37	HDMIR_RST	O	C	-	-	Eu	Z	Reset for HDMI RECEIVER(Sil9135)
54	P36	1HTRST	O	C	-	-	Eu	Z	Reset for HDMI TRANSMITTER1
55	P35	Z1SMONIB	O	C	-	-	Ed	Z	Z1 SMONITOR select
56	P34	1HTINT	I	-	Lv	-	-	Z	HDMI OUT signal detect input(HDMI TRANS1 Sil9134)
57	P33	PAL/NTSC	O	-	-	-	Ed	Z	Not used
58	P32	SOCODECI	O	C	-	-	-	Z	CODEC (ADAU1328) control pin
59	P31	CLKCODEC	O	C	-	-	-	Z	CODEC (ADAU1328) control pin
60	VCC	VCC	-	-	-	-	-	-	+3.3V
61	P30	CECODEC	O	C	-	-	-	Z	CODEC (ADAU1328) control pin
62	VSS	VSS	-	-	-	-	-	-	GND
63	P27	CODECRST	O	C	-	-	-	Z	CODEC (ADAU1328) control pin
64	P26	XMDACRST	O	C	-	-	-	Z	XMDAC control pin (AK4385)
65	P25	XMDACCS	O	C	-	-	-	Z	XMDAC control pin (AK4385)
66	P24	XMDACMC	O	C	-	-	-	Z	XMDAC control pin (AK4385)
67	P23	XMDACMDI	O	C	-	-	-	Z	XMDAC control pin (AK4385)
68	P22	VEXPSTB	O	C	-	-	-	Z	Terminal output for VIDEO expander control(BU4094BCFV)
69	P21	VEXPOE	O	C	-	-	Ed	Z	Terminal output for VIDEO expander control(BU4094BCFV)
70	P20	VEXPCLK	O	C	-	-	-	Z	CLK output for VIDEO expander control(BU4094BCFV)
71	P17/INT5	VEXPDIN	O	C	-	-	-	Z	DATA output for VIDEO expander control(BU4094BCFV)
72	P16/INT4	COMPSDET	I	-	Lv	-	Eu	Z	COMPONENT IN signal detect input
73	P15/INT3	Z1VSIG.DET	I	-	Lv	-	Eu	Z	VIDEO IN signal detect input (Signal inputted : H)
74	P14/D12	Z1SMONIDET	I	-	-	-	Eu	Z	S MONITOR connection existence detection input (connected:L)
75	P13/D11	Z1SSIGDET	I	-	-	-	Eu	Z	S signal detect input (signal inputted:H)
76	P12/D10	SYNCDet	I	-	Lv	-	-	Z	SyncDet pin
77	P11/D9	CPUCONT	O	C	-	-	-	-	A.PLD Control Bit
78	P10/D8	D.POWER	O	C	-	-	Ed	Z	Digital Power ON/OFF control pin
79	P07/D7	PLDWRITE	O	C	-	-	-	Z	PLD JTAGLINE ON/OFF control
80	P06/D6	VPLDCE/TDO	O/I	-	-	-	Ed	Z	VIDEO PLD control pin/PLD rewrite control (JTAG)
81	P05/D5	HDP3	O	C	-	-	-	Z	HP DET control pin
82	P04/D4	HDP4	O	C	-	-	-	Z	HP DET control pin
83	P03/D3	INT1	I	-	Lv	-	Eu	Z	DIR1 control pin
84	P02/D2	INT2	O	C	-	-	-	Z	Not used
85	P01/D1	DIRRST2	O	C	-	-	-	Z	Not used
86	P00/D0	DIRRST1	O	C	-	-	-	Z	DIR1 control pin

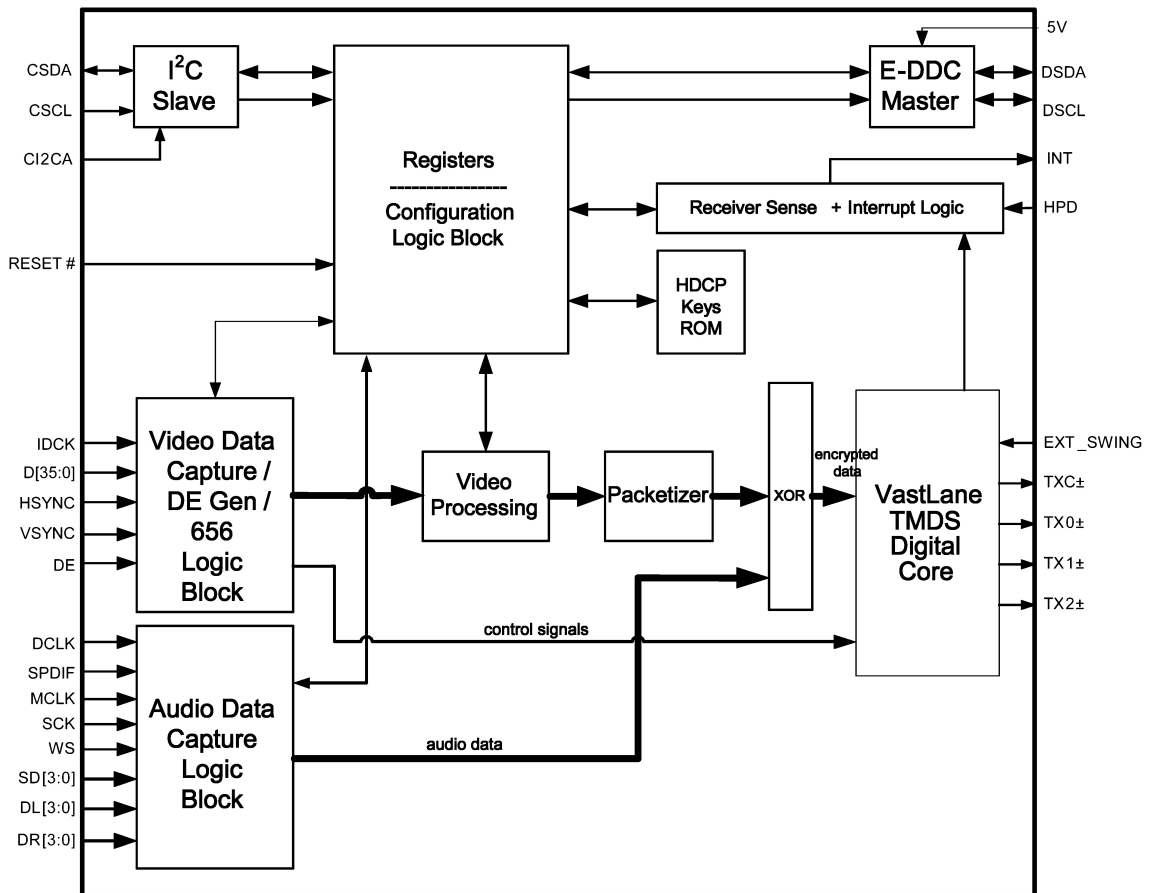
Pin	Pin Name	Symbol	I/O	Type	Det	Op (Int.)	Op (Ext.)	Res	Function
87	P107/AN7	DSPRST	O	C	-	-	-	Z	DSP (ADSP-21367) reset output pin (reset:L)
88	P106/AN6	-	O	C	-	-	-	Z	Not used
89	P105/AN5	DSPROMRST	O	C	-	-	Ed	Z	DSP memory reset(reset:L)
90	P104/AN4	-	O	C	-	-	-	Z	Not used
91	P103/AN3	DSPFLAG0	I	-	Lv	-	Ed	Z	DSP control pin (ADSP-21367)
92	P102/AN2	DSPICS	O	C	-	-	Eu	Z	DSP control pin (ADSP-21367)
93	P101/AN1	DSP FLAG1	I	-	-	-	-	Z	Not used
94	AVSS	AVSS	-	-	-	-	-	-	AD GND
95	P100/AN0	VPLDCLK	O	-	-	-	-	Z	VIDEO PLD control pin
96	VREF	VREF	-	-	-	-	-	-	AD ref. +3.3V
97	AVCC	AVCC	-	-	-	-	-	-	AD +3.3V
98	P97/SIN4	DSPMISO	I	-	Lv	-	Eu	Z	DSP control pin (ADSP-21367)
99	P96/SOUT4	DSPMOSI	O	C	-	-	Eu	Z	DSP control pin (ADSP-21367)
100	P95/CLK4	DSPICLK	O	C	-	-	Eu	Z	DSP control pin (ADSP-21367)

Note: Pin No. : Terminal number of microcomputer.
Port Name : The name entered in the data sheet of microcomputer.
Symbol : Symbolized interface function.
I/O : Input or out of part.
 "i" = Input port
 "o" = Output port
Type : Composition of port in case of output port.
 "C" = CMOS output
 "N" = NMOS open drain output
 "P" = PMOS open drain output
Op : Pull up/Pull down selection information.
 "lu" = Inner microcomputer pull up
 "ld" = Inner microcomputer pull down
 "eu" = External microcomputer pull up
 "ed" = External microcomputer pull down
Det : Indicates judging state of input port. Level detection is "LV"; Edge detection is "Ed"; Detection by both shifting is "E&L";
Serial data detection is "S" (Serial data output is also "S").
Res : State at reset.
 "H" = Outputs High Level at reset
 "L" = Outputs Low Level at reset
 "Z" = Becomes High impedance mode at reset
STBY : State of port when STANDBY mode.
 "O/L" = Output port and "L"
 "i" = Input port
Stop : State of port when Stop mode.
 "O/L" = Output port and "L"
 "i" = Input port

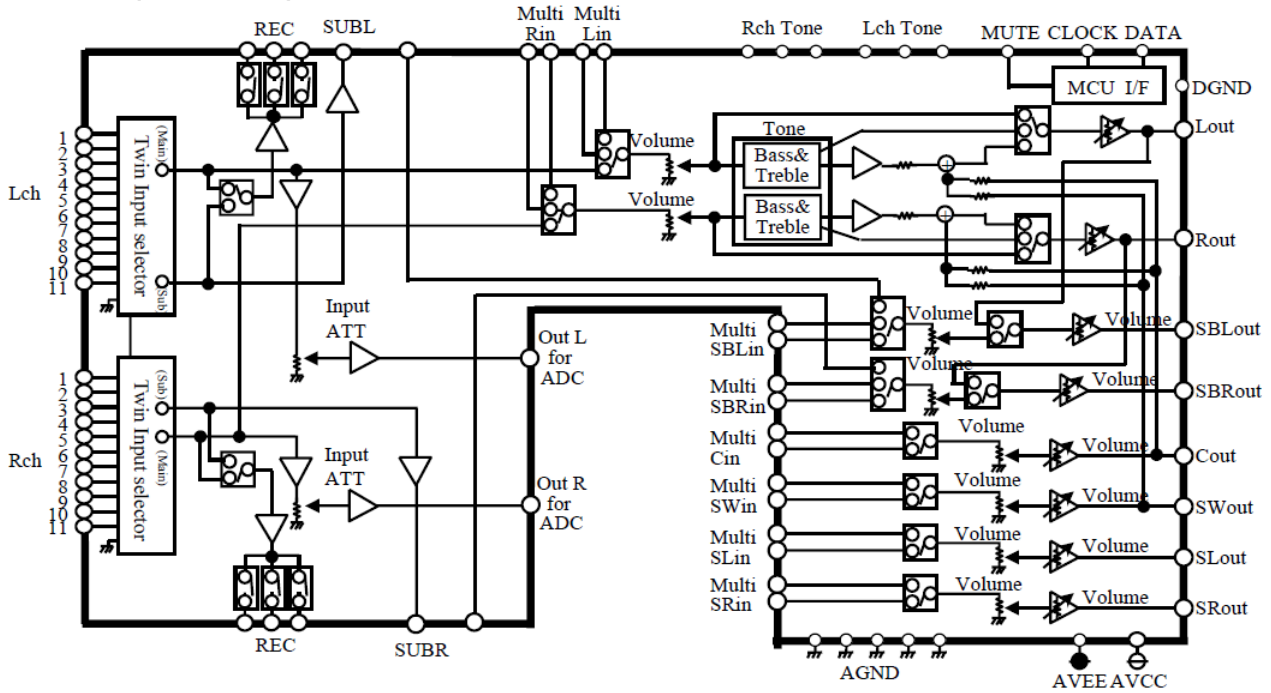
SiI9134CTU (DI : IC702)



Functional Block Diagram

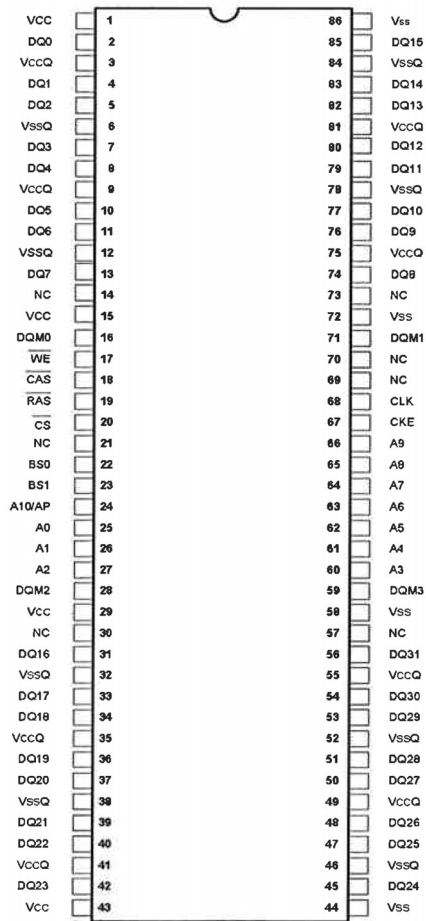


R2A15215 (AV : IC612)

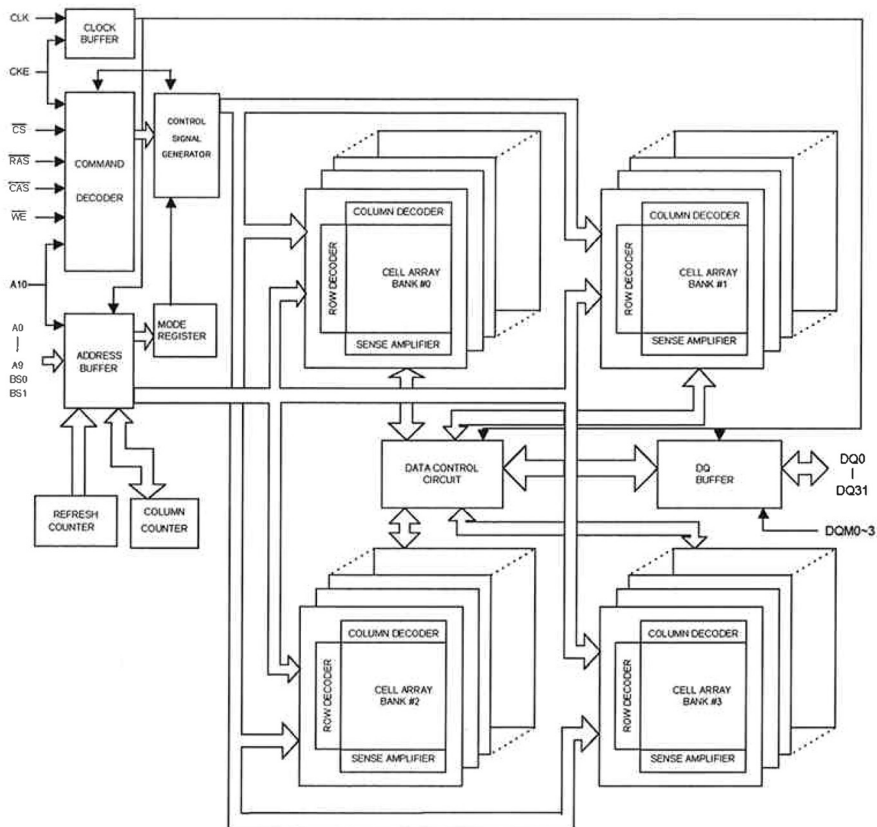


PIN No.	Name	Function
23,21, 17,15, 11,9, 5,3	FR0UT,FL0UT, CO0UT,SW0UT, SR0UT, SLOUT, SBROUT,SBLOUT	Output pin of FL/FR/C/SW/SL/SR/SBL/SBR channel
24,20, 18,14, 12,8, 6,2	FRC,FLC, CC,SWC, SRC,SLC, SBRC,SBLC	Connects capacitor for reducing click noise of L/R/C/SW/SL/SR/SBL/SBR channel volume
4,7,10,16, 19,22,56	AGND	Analog ground of internal circuit
28,34	TREL, TRER	Frequency characteristic setting pin of L/R channel tone control (Treble)
26,27, 32,33	BASSL1,BASSL2 BASSR1,BASSR2	Frequency characteristic setting pin of L/R channel tone control (Bass)
30	AVCC	Positive power supply to internal circuit
43,42, 41,40, 39,38, 37,36, 93,94, 95,96, 97,98, 99,100	FRIN2, FLIN2, SRN2,SLIN2, SWIN2,CIN2, SBRIN2,SBLIN2 FLIN1, FRIN1, CIN1,SWIN1, SLIN1,SRIN1, SBLIN1,SBRIN1	Input pin of L/R/C/SW/SL/SR/SBL/SBR channel (Multi IN 1/2)
48	DGND	Digital ground of internal circuit
49	DATA	Input pin of control data
50	CLOCK	Input pin of control clock
52	AVEE	Negative power supply to internal circuit
59,61,63, 65,67,69, 71,73,79	INL1,INL2, INL3, INL4,INL5,INL6, INL7,INL8,INL9	Input pin of L/R channel (Input Selector)
58,60,62, 64,66,68, 70,72,78	INR1,INR2, INR3, INR4,INR5,INR6, INR7,INR8,INR9	Input pin of L/R channel (Input Selector)
51	MUTE	Outside Mute Control PIN
44,45	SBRCIN,SBLCIN	Input pin for SBL/SBR channel Volume
46,47	SUBL,SUBR	Output pin for L/R channel SUB Output
54,55	ADCL, ADCR	Output pin for L/R channel ADC
90,91	RECR3,RECL3	Output pin for L/R channel REC Output
75,76, 81,82, 83,84, 85,86	INRA/RECR1,INLA/RECL1, INRB/RECR2,INLB/RECL2, INR10/RECR4,INL10/RECL4, INR11/RECR5,INL11/RECL5	Input pin of L/R channel (Input Selector)/ Output pin for L/R channel REC Output
1,13,25,29,31, 35,53, 57,74,77,80, 87,88,89,92	N.C.	No Connected PIN

W9864G2GH-6 (DI : IC203)



Functional Block Diagram

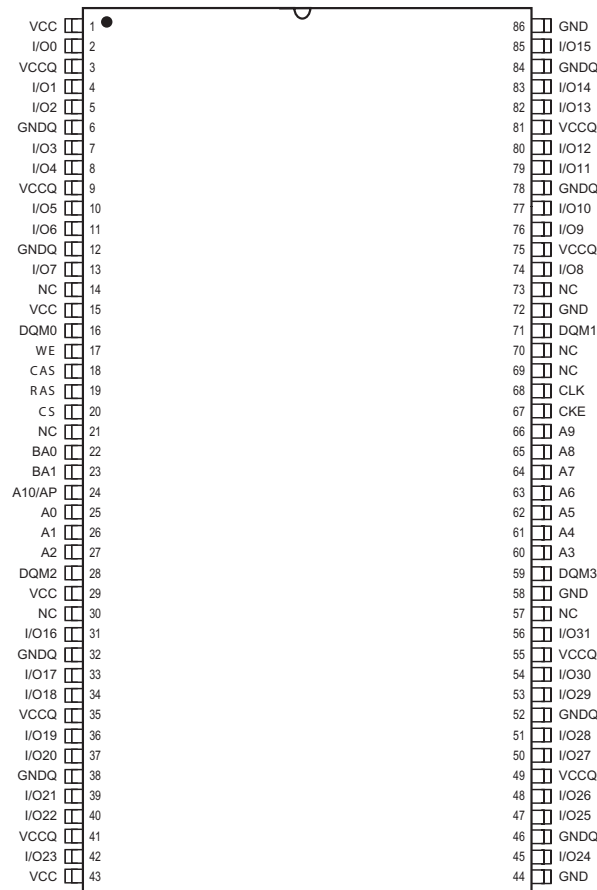


NOTE:
The cell array configuration is 2048 * 256 * 32

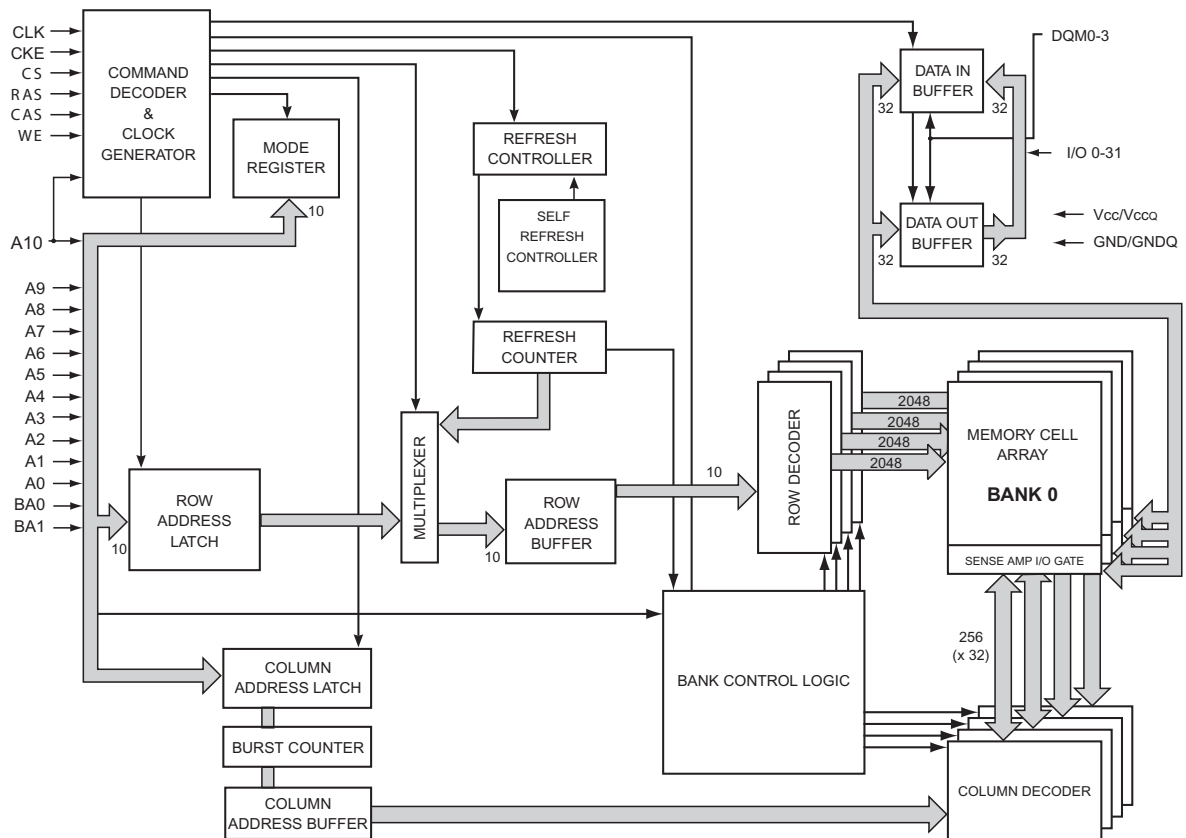
Pin Function

PIN NUMBER	PIN NAME	FUNCTION	DESCRIPTION
24, 25, 26, 27, 60, 61, 62, 63, 64, 65, 66	A0–A10	Address	Multiplexed pins for row and column address. Row address: A0–A10. Column address: A0–A7. A10 is sampled during a precharge command to determine if all banks are to be precharged or bank selected by BS0, BS1.
22, 23	BS0, BS1	Bank Select	Select bank to activate during row address latch time, or bank to read/write during address latch time.
2, 4, 5, 7, 8, 10, 11, 13, 31, 33, 34, 36, 37, 39, 40, 42, 45, 47, 48, 50, 51, 53, 54, 56, 74, 76, 77, 79, 80, 82, 83, 85	DQ0– DQ31	Data Input/ Output	Multiplexed pins for data output and input.
20	$\overline{\text{CS}}$	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
19	$\overline{\text{RAS}}$	Row Address Strobe	Command input. When sampled at the rising edge of the clock $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ define the operation to be executed.
18	$\overline{\text{CAS}}$	Column Address Strobe	Referred to $\overline{\text{RAS}}$
17	$\overline{\text{WE}}$	Write Enable	Referred to $\overline{\text{RAS}}$
16, 28, 59, 71	DQM0– DQM3	Input/Output Mask	The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.
68	CLK	Clock Inputs	System clock used to sample inputs on the rising edge of clock.
67	CKE	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.
1, 15, 29, 43	Vcc	Power	Power for input buffers and logic circuit inside DRAM.
44, 58, 72, 86	Vss	Ground	Ground for input buffers and logic circuit inside DRAM.
3, 9, 35, 41, 49, 55, 75, 81	Vccq	Power for I/O Buffer	Separated power from VCC, to improve DQ noise immunity.
6, 12, 32, 38, 46, 52, 78, 84	Vssq	Ground for I/O Buffer	Separated ground from VSS, to improve DQ noise immunity.
14, 21, 30, 57, 69, 70, 73	NC	No Connection	No connection. (The NC pin must connect to ground or floating.)

IS42S32200E (DI : IC903)



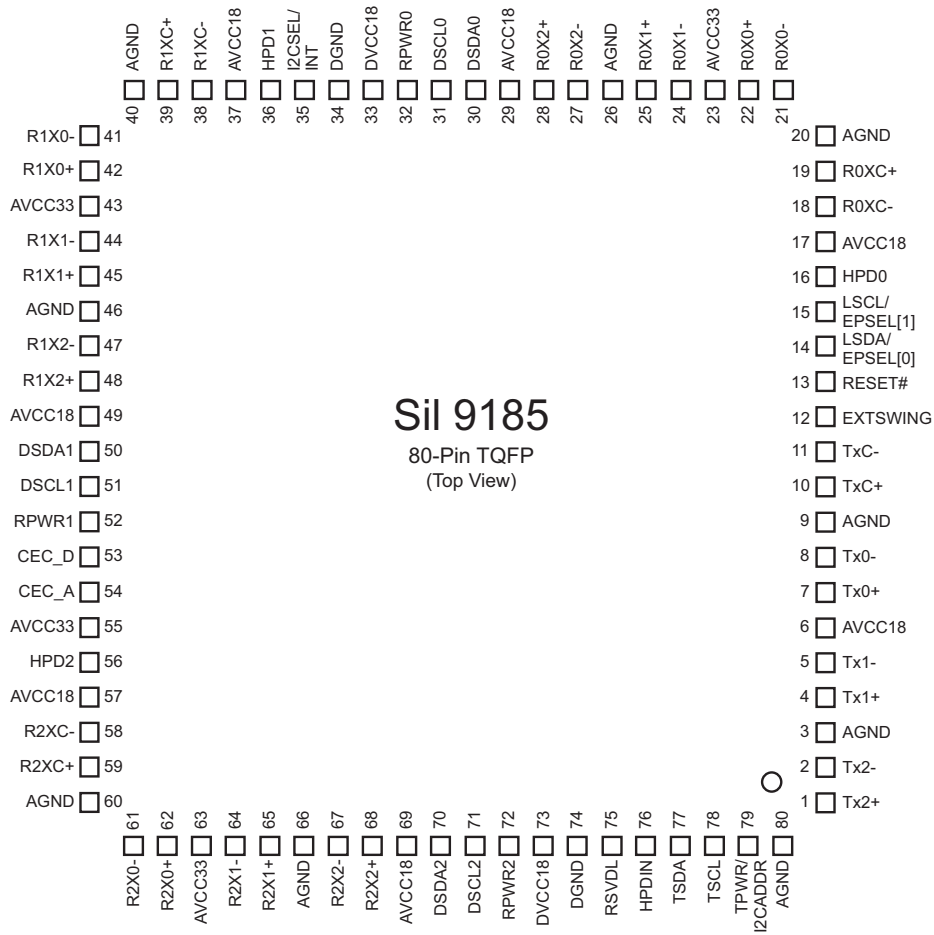
Functional Block Diagram



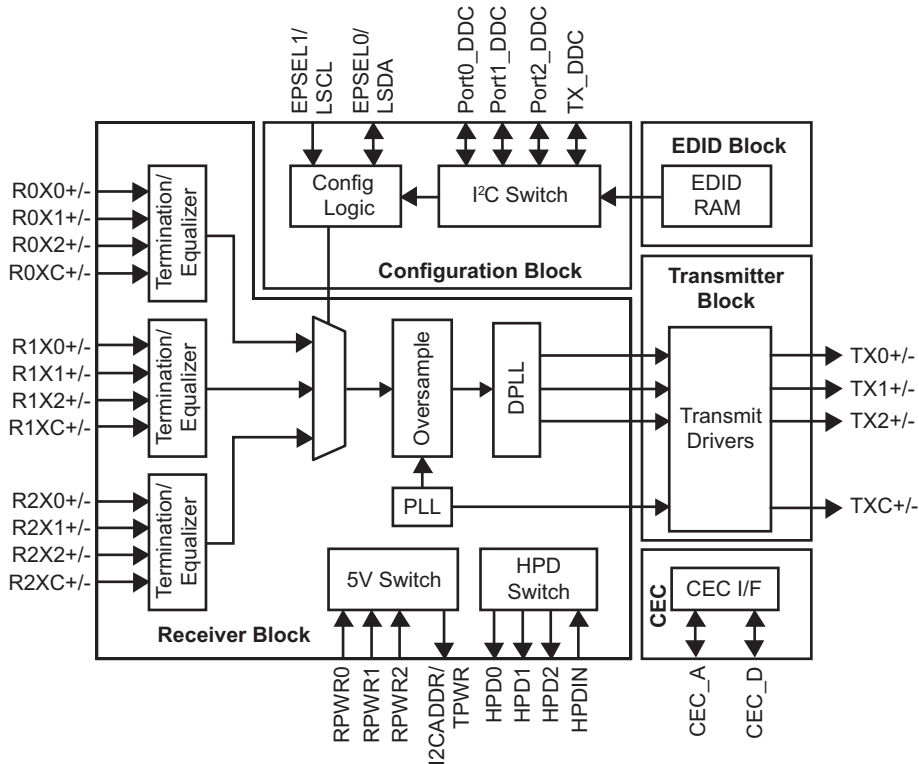
Pin Function

Symbol	Pin No.	Type	Function (In Detail)
A0-A10	25 to 27 60 to 66 24	Input Pin	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (A0-A7 with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
BA0, BA1	22,23	Input Pin	Bank Select Address: BA0 and BA1 defines which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
CAS	18	Input Pin	CAS, in conjunction with the RAS and WE, forms the device command. See the "Command Truth Table" for details on device commands.
CKE	67	Input Pin	The CKE input determines whether the CLK input is enabled. The next rising edge of the CLK signal will be valid when is CKE HIGH and invalid when LOW. When CKE is LOW, the device will be in either power-down mode, clock suspend mode, or self refresh mode. CKE is an asynchronous input.
CLK	68	Input Pin	CLK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
CS	20	Input Pin	The CS input determines whether command input is enabled within the device. Command input is enabled when CS is LOW, and disabled with CS is HIGH. The device remains in the previous state when CS is HIGH.
I/O0 to I/O31	2, 4, 5, 7, 8, 10,11,13 74,76,77,79,80,82,83,85 45,47,48,50,51,53,54,56 31,33,34,36,37,39,40,42	I/O Pin	I/O0 to I/O15 are I/O pins. I/O through these pins can be controlled in byte units using the DQM0-DQM3 pins
DQM0 DQM3	16,28,59,71	Input Pin	DQMx control the lower and upper bytes of the I/O buffers. In read mode, the output buffers are placed in a High-Z state. During a WRITE cycle the input data is masked. When DQMx is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. I/O0 through I/O7 are controlled by DQM0. I/O8 through I/O15 are controlled by DQM1. I/O16 through I/O23 are controlled by DQM2. I/O24 through I/O31 are controlled by DQM3.
RAS	19	Input Pin	RAS, in conjunction with CAS and WE, forms the device command. See the "Command Truth Table" item for details on device commands.
WE	17	Input Pin	WE, in conjunction with RAS and CAS, forms the device command. See the "Command Truth Table" item for details on device commands.
Vccq	3,9,35,41,49,55,25,81	Supply Pin	Vccq is the output buffer power supply.
Vcc	1,15,29,43	Supply Pin	Vcc is the device internal power supply.
GNDq	6,12,32,38,46,52,78,84	Supply Pin	GNDq is the output buffer ground.
GND	44,58,72,86	Supply Pin	GND is the device internal ground.

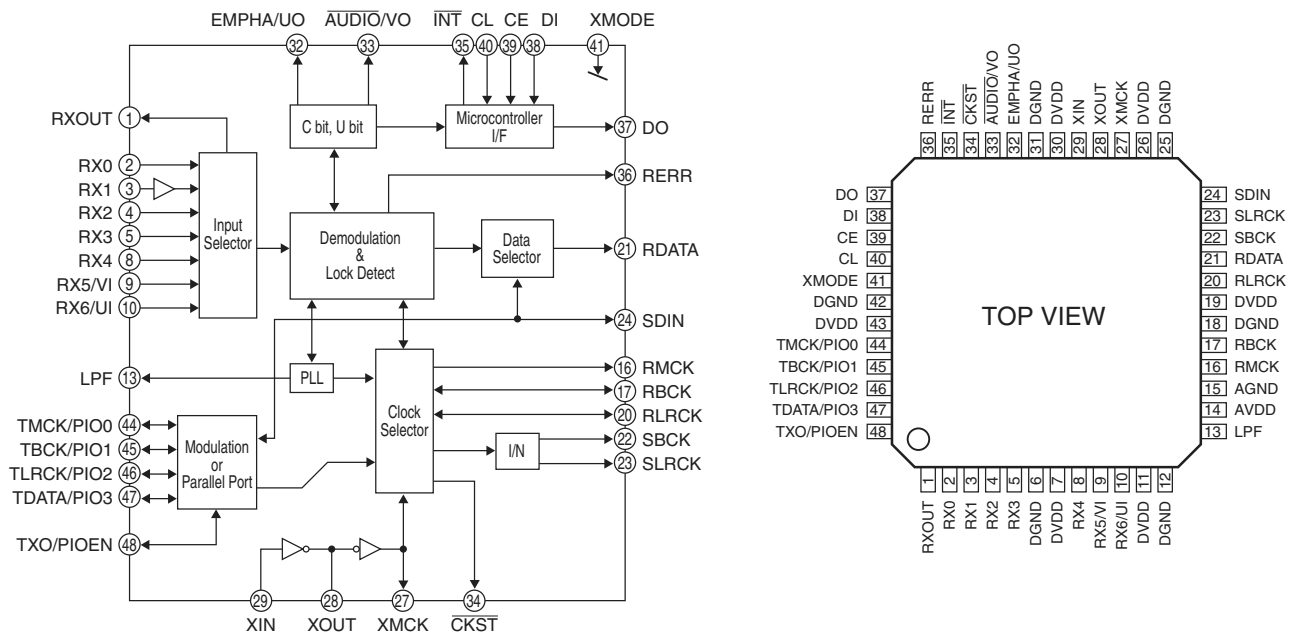
SiI9185CTU (DI : IC510)



Functional Block Diagram



LC89057W-VF4A (DI : IC101)



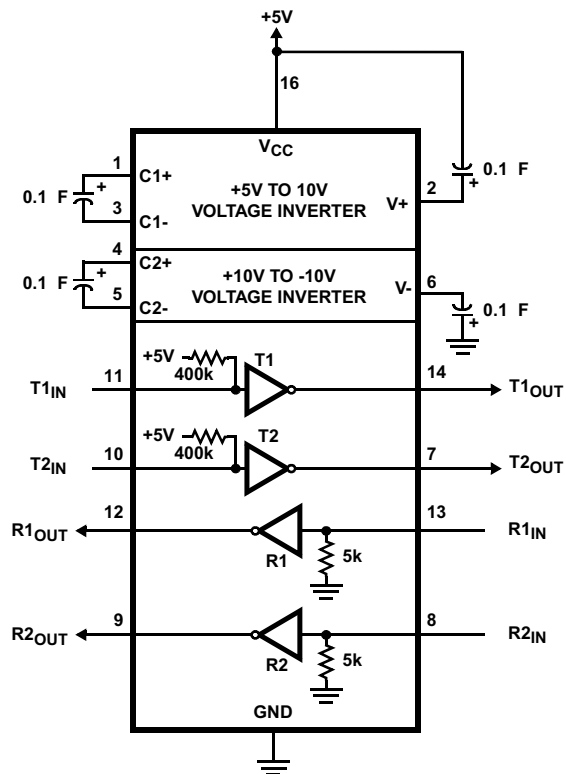
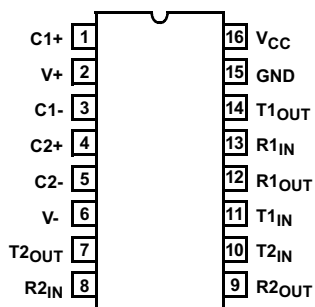
LC89057W Terminal Function

Pin No.	Pin Name	I/O	Function
1	RXOUT	O	Input bi-phase select data output terminal
2	RX0	I	TTL compatible digital data input terminal
3	RX1	I	Coaxial compatible amp built-in digital data input terminal
4	RX2	I	TTL compatible digital data input terminal
5	RX3	I	TTL compatible digital data input terminal
6	DGND	„	Digital GND
7	DVDD	„	Digital power
8	RX4	I	TTL compatible digital data input terminal
9	RX5/VI	I	TTL compatible digital data/Validity flag input terminal for modulation
10	RX6/UI	I	TTL compatible digital data/User data input terminal for modulation
11	DVDD	„	Digital power for PLL
12	DGND	„	Digital GND for PLL
13	LPF	O	PLL loop filter connecting terminal
14	AVDD	„	Analog power for PLL
15	AGND	„	Analog GND for PLL
16	RMCK	O	RMCK clock output terminal (256fs, 512fs, XIN, VCO)
17	RBCK	O/I	RBCK clock in/output terminal (64fs)
18	DGND	„	Digital GND
19	DVDD	„	Digital power
20	RLRCK	O/I	RLRCK clock in/output terminal (fs)
21	RDATA	O	Serial audio data output terminal
22	SBCK	O	SBCK clock output terminal (32fs, 64fs, 128fs)
23	SLRCK	O	SLRCK clock output terminal (fs/2, fs, 2fs)
24	SDIN	I	Serial audio data input terminal
25	DGND	„	Digital GND
26	DVDD	„	Digital power
27	XMCK	O	Osc. amp output terminal

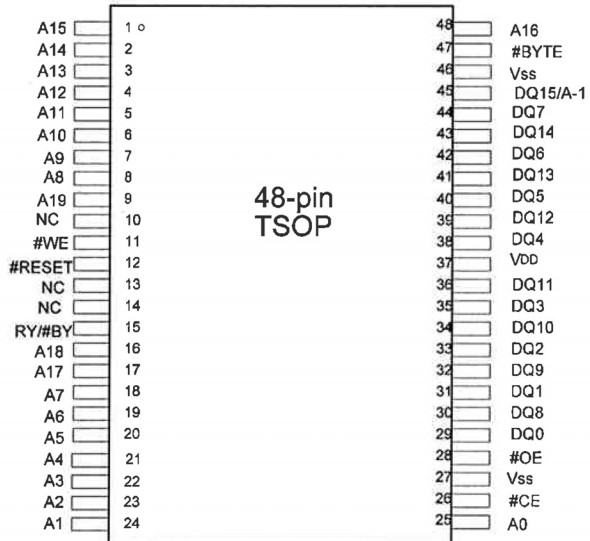
Pin No.	Pin Name	I/O	Function
28	XOUT	O	X tal osc. connecting output terminal
29	XIN	I	X tal osc. connection, external clock input terminal (24.576MHz or 12.288MHz)
30	DVDD	„	Digital power
31	DGND	„	Digital GND
32	EMPHA/UO	I/O	Emphasis information/U-data output/Chip address setting terminal
33	AUDIO/VO	I/O	Non-PCM detect/V-flag output/ Chip address setting terminal
34	CKST	I/O	Clock switch transition period output/Demodulation master or slave function switching terminal
35	INT	I/O	Interrupt output for \sim com (Interrupt factor selectable)/Modulation or general I/O switching terminal
36	RERR	O	PLL lock error, data error flag output
37	DO	O	μ com I/F, read out data output terminal (3-state)
38	DI	I	μ com I/F, write data input terminal
39	CE	I	μ com I/F, chip enable input terminal
40	CL	I	μ com I/F, clock input terminal
41	XMODE	I	System reset input terminal
42	DGND	„	Digital GND
43	DVDD	„	Digital power
44	TMCK/PIO0	I/O	256fs system clock input for modulation/General I/O in/output terminal
45	TBCK/PIO1	I/O	64fs bit clock input for modulation/General I/O in/output terminal
46	TLRCK/PIO2	I/O	fs clock input for modulation/General I/O in/output terminal
47	TDATA/PIO3	I/O	Serial audio data input for modulation/General I/O in/output terminal
48	TXO/PIOEN	O/I	Modulation data output/ General I/O enable input terminal

* For latch-up countermeasure, perform each power supply ON/OFF in the same timing.

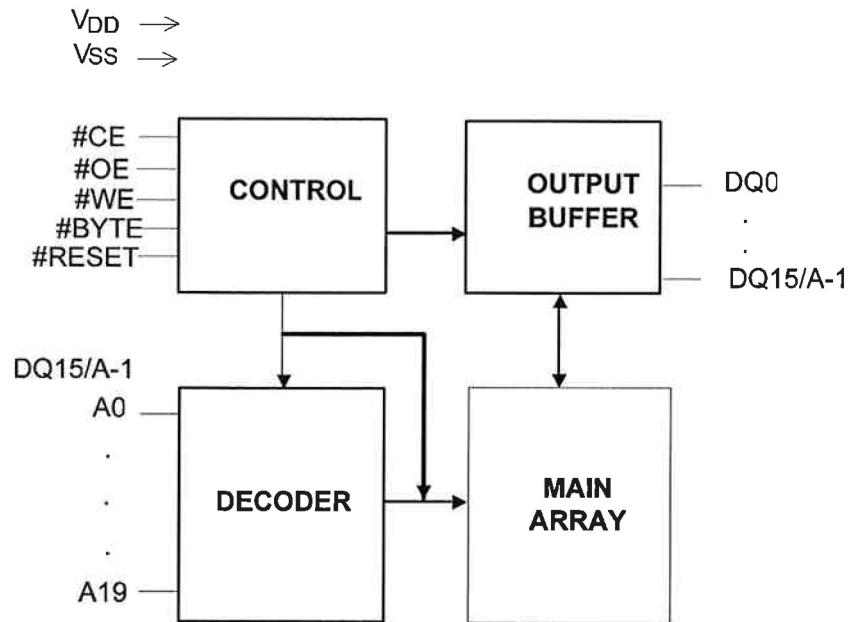
HIN202EIBNZ-T (MC:IC104)



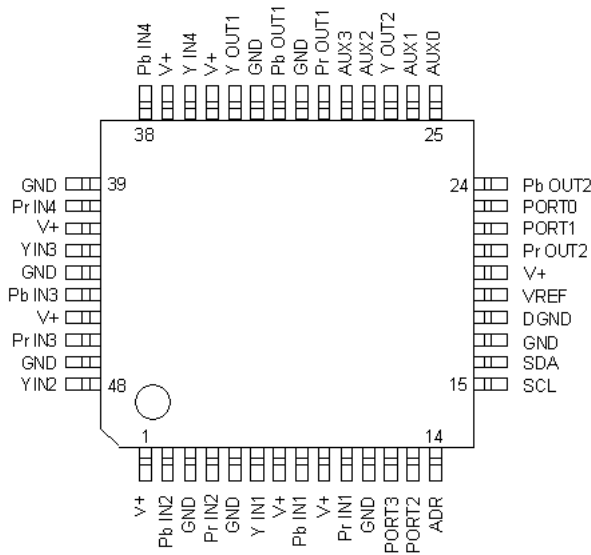
W19B160BBT7H (DI : IC205)



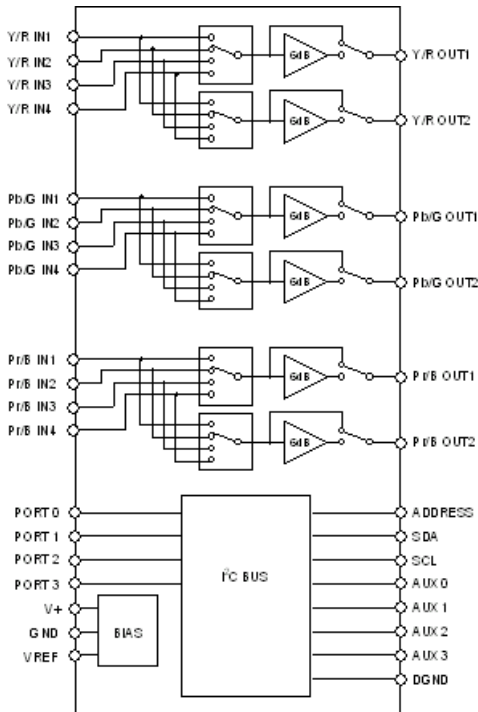
Functional Block Diagram



NJW1321FP1 (AV : IC501)



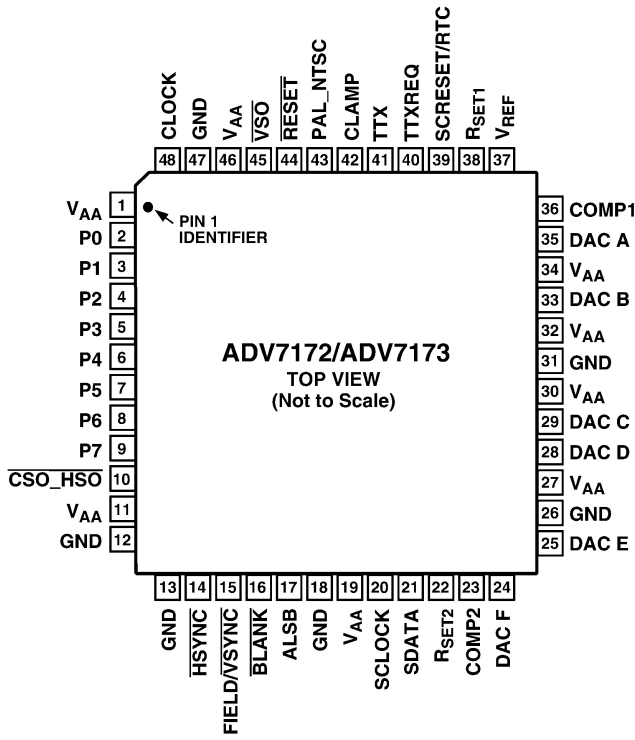
1. V+	13. PORT2	25. AUX0	37. V+
2. Pb IN2	14. ADR	26. AUX1	38. Pb IN4
3. GND	15. SCL	27. Y OUT2	39. GND
4. Pr IN2	16. SDA	28. AUX2	40. Pr IN4
5. GND	17. GND	29. AUX3	41. V+
6. Y IN1	18. DGND	30. Pr OUT1	42. Y IN3
7. V+	19. VREG	31. GND	43. GND
8. Pb IN1	20. V+	32. Pb OUT1	44. Pb IN3
9. V+	21. Pr OUT2	33. GND	45. V+
10. Pr IN1	22. PORT1	34. Y OUT1	46. Pr IN3
11. GND	23. PORT 0	35. V+	47. GND
12. PORT3	24. Pb OUT2	36. Y IN4	48. Y IN2



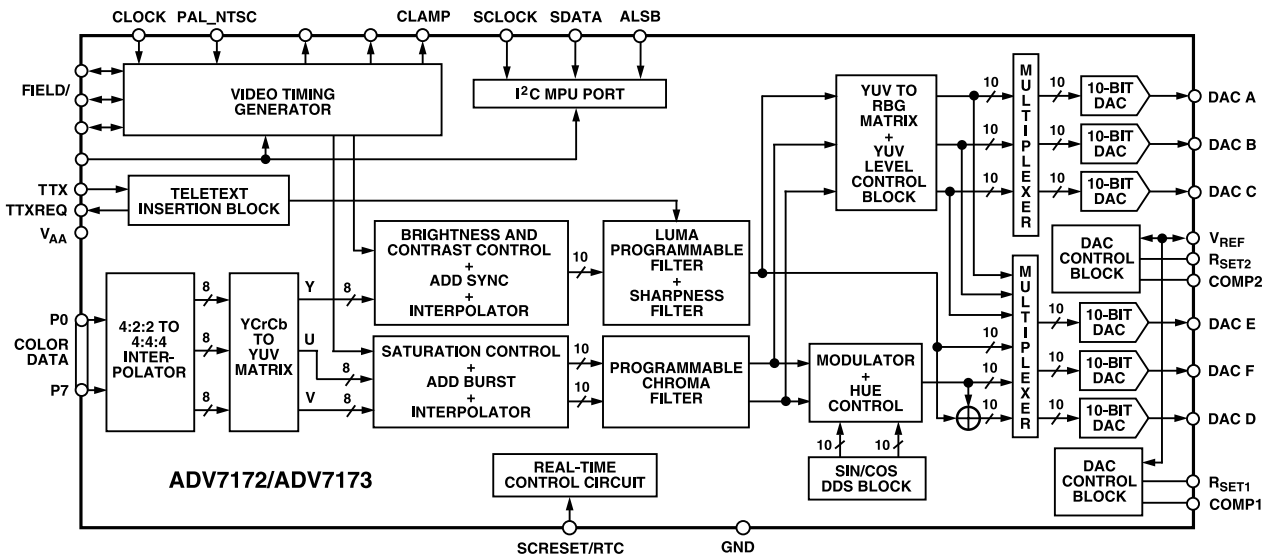
Control Pin Sub VSCL (27pin) VSDA (28pin)

Pin Name	AUX0		AUX1		AUX2		AUX3		
Signal Name	OSD V/Y		Z1OSDV		Z1OSDY		-		
	Output	D7	D6	D5	D4	D3	D2	D1	D0
DATA2	L setup	0	0	0	0	0	0	0	0
	H setup	1	1	1	1	1	1	1	1
Function	Superimpose Signal select L : S H : CVBS	MAIN ZONE CVBS signal channel select L : Through channel select H : OSD channel select		MAIN ZONE S signal channel select L : Through channel select H : OSD channel select		Not used			

ADV7172 (DI : IC805)



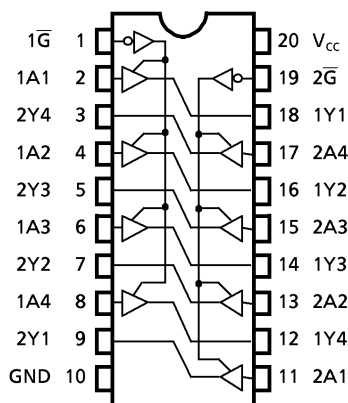
BLOCK DIAGRAM

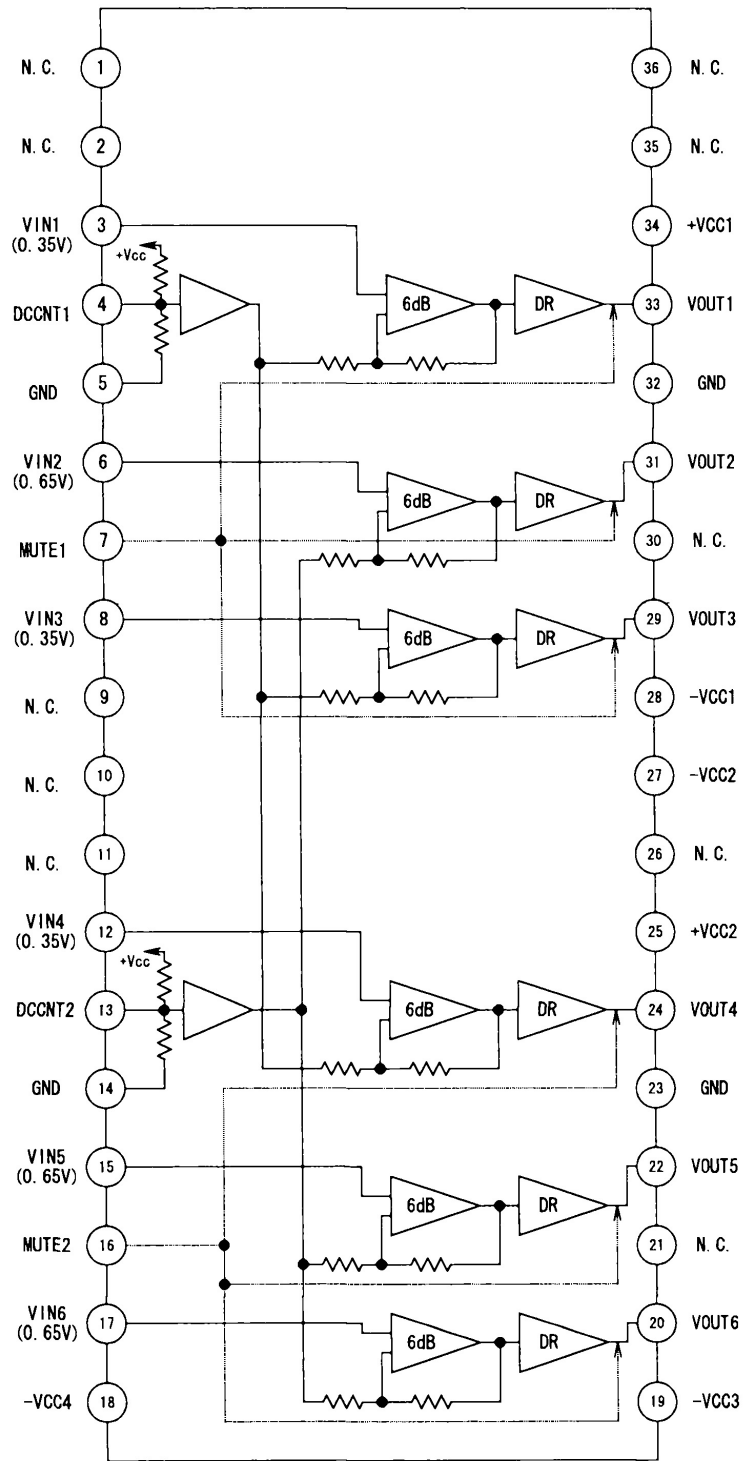


PIN FUNCTION DESCRIPTION

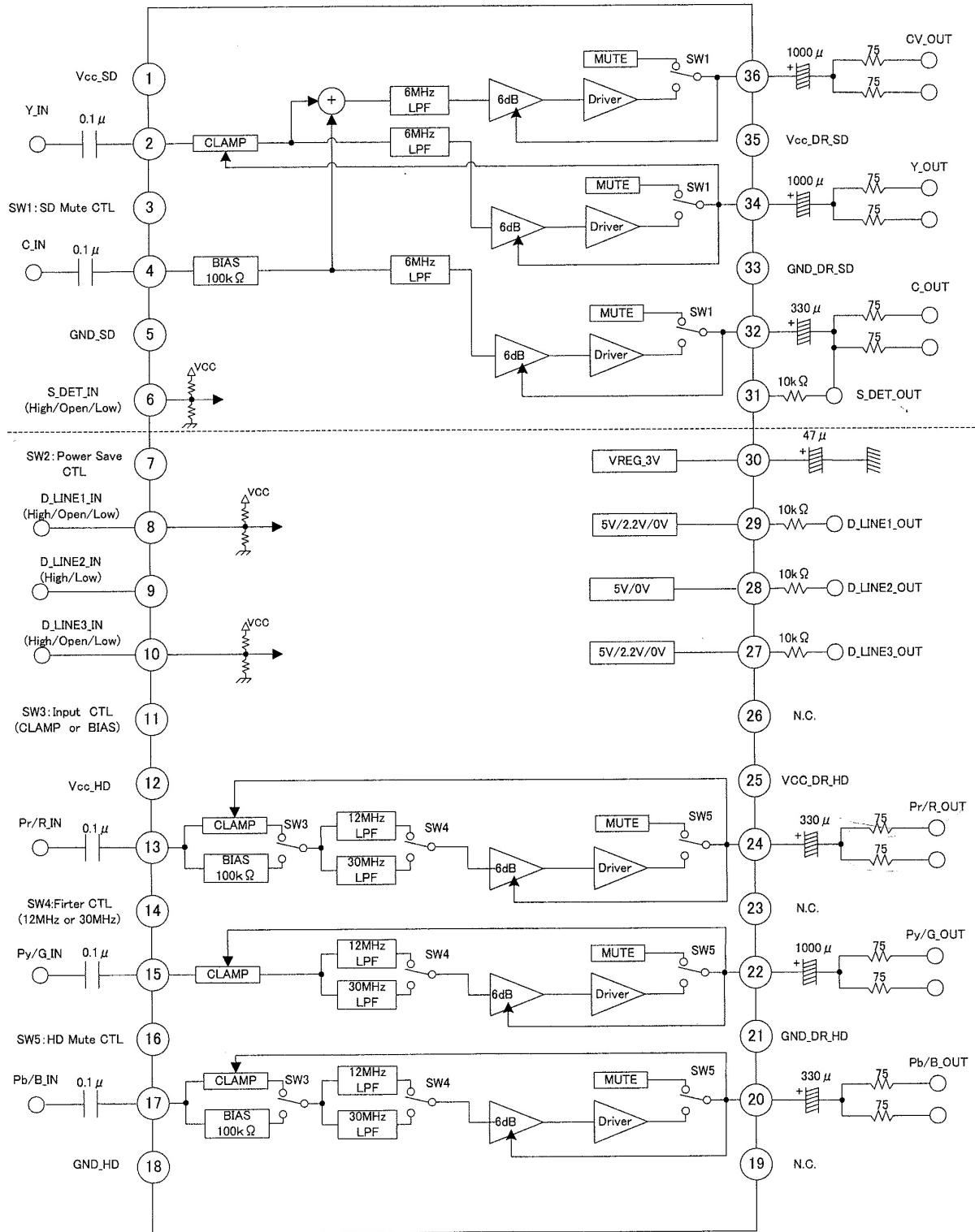
Mnemonic	Input/Output	Function
P7–P0	I	8-Bit 4:2:2 Multiplexed YCrCb Pixel Port (P7–P0) P0 represents the LSB.
CLOCK	I	TTL Clock Input. Requires a stable 27 MHz reference clock for standard operation. Alternatively, a 24.5454 MHz (NTSC) or 29.5 MHz (PAL) can be used for square pixel operation.
$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1 and 2) Control Signal. This pin may be configured to output (Master Mode) or as an input and accept (Slave Mode) Sync signals.
$\overline{\text{FIELD}}/\overline{\text{VSYNC}}$	I/O	Dual Function $\overline{\text{FIELD}}$ (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin may be configured to output (Master Mode) or as an input (Slave Mode) and accept these control signals.
$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is Logic Level “0.” This signal is optional.
SCRESET/RTC	I	This pin can be configured as an input by setting MR42 and MR41 of Mode Register 4. It can be configured as a subcarrier reset pin, in which case a low-to-high transition on this pin will reset the subcarrier phase to Field 0. Alternatively it may be configured as a Real-Time Control (RTC) Input.
V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
R_{SET1}	I	A 150 Ω resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals from DACs A, B, and C (the “large” DACs).
R_{SET2}	I	A 600 Ω resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals from DACs D, E, and F (the “small” DACs).
COMP1	O	Compensation Pin for DACs A, B, and C. Connect a 0.1 μF Capacitor from COMP to V_{AA} . For Optimum Dynamic Performance in Low Power Mode, the value of the COMP1 capacitor can be lowered to as low as 2.2 nF.
COMP2	O	Compensation Pin for DACs D, E, and F. Connect a 0.1 μF Capacitor from COMP to V_{AA} .
DAC A	O	GREEN/Composite/Y Analog Output. This DAC is capable of providing 34.66 mA output.
DAC B	O	BLUE/S-Video Y/U Analog Output. This DAC is capable of providing 34.66 mA output.
DAC C	O	RED/S-Video C/V Analog Output. This DAC is capable of providing 34.66 mA output.
DAC D	O	GREEN/Composite/Y Analog Output. This DAC is capable of providing 8.66 mA output.
DAC E	O	BLUE/S-Video Y/U Analog Output. This DAC is capable of providing 8.66 mA output.
DAC F	O	RED/S-Video C/V Analog Output. This DAC is capable of providing 8.66 mA output.
SCLOCK	I	MPU Port Serial Interface Clock Input.
SDATA	I/O	MPU Port Serial Data Input/Output.
CLAMP	O	TTL Output Signal to external circuitry to enable clamping of all video signals.
$\overline{\text{PAL_NTSC}}$	I	Input signal to select PAL or NTSC mode of operation, pin set to Logic “1” selects PAL.
$\overline{\text{VSO}}$	O	$\overline{\text{VSO}}$ TTL Output Sync Signal.
$\overline{\text{CSO_HSO}}$	O	Dual Function $\overline{\text{CSO}}$ or $\overline{\text{HSO}}$ TTL Output Sync Signal.
ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address.
$\overline{\text{RESET}}$	I	The input resets the on-chip timing generator and sets the ADV7172/ADV7173 into default mode. This is NTSC operation, Timing Slave Mode 0, DACs A, B, and C powered OFF, DACs D, E, and F powered ON, Composite and S-Video out.
TTX	I	Teletext Data Input Pin.
TTXREQ	O	Teletext Data Request output signal used to control teletext data transfer.
V_{AA}	P	Power Supply (3 V to 5 V).
GND	G	Ground Pin.

TC74VHC244FT (DI : IC112)

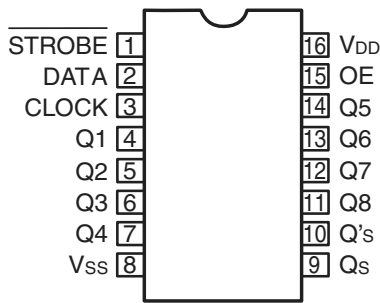




LA73062V (AV : IC305)



BU409413CFV-E2 (AV: IC301)
TC4094BF (MC: IC106,107)



BU4094BCFV-E2 Terminal Function

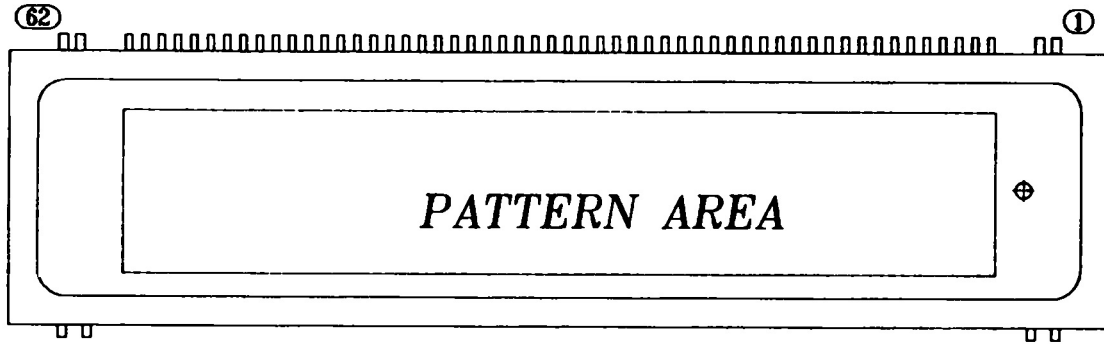
Device	Pin Name	Symbol	Function
AV : IC301	EXP1	INA	MAIN ZONE VIDEO(V/S) input switching
	EXP2	INB	MAIN ZONE VIDEO(V/S) input switching
	EXP3	INC	MAIN ZONE VIDEO(V/S) input switching
	EXP4	Z2A	ZONE2 VIDEO(V/S) input switching
	EXP5	Z2B	MAIN ZONE VIDEO(V/S) input switching
	EXP6	Z2C	MAIN ZONE VIDEO(V/S) input switching
	EXP7	Z1MONIA	MAIN ZONE VMONITOR output switching
	EXP8	Z1MONIB	MAIN ZONE VMONITOR output switching

TC4094BF Terminal Function

Device	Pin Name	Symbol	Function
MC : IC106	EXP1	T.MUTE	TUNER MUTE CONTROL L:MUTE
	EXP2	PREFMUTE	PREOUT FRONT MUTE CONTROL L:MUTE
	EXP3	PRECMUTE	PREOUT CENTER MUTE CONTROL L:MUTE
	EXP4	PRESWMUTE	PREOUT SUBWOOFER MUTE CONTROL L:MUTE
	EXP5	PRESMUTE	PREOUT SURROUND MUTE CONTROL L:MUTE
	EXP6	PRESBMUTE	PREOUT SURROUND BACK MUTE CONTROL L:MUTE
	EXP7	PREZ2MUTE	ZONE2 PREOUT MUTE CONTROL L:MUTE
	EXP8	A/DMUTE	ADIN MUTE CONTROL L:MUTE
MC : IC107	EXP9	HPRLY	HEAD PHONE RELAY CONTROL H:HEAD PHONE ON
	EXP10	FRL	FRONT A SPEAKER RELAY CONTROL H:Front A Speaker ON
	EXP11	CRL	CENTER SPEAKER RELAY CONTROL H:Center Speaker ON
	EXP12	NC	-
	EXP13	SRL	SURROUND SPEAKER RELAY CONTROL H:Surround Speaker ON
	EXP14	SBRL	SURROUND BACK SPEAKER RELAY CONTROL H:Surround Back Speaker ON
	EXP15	FBRL	FRONT B SPEAKER RELAY CONTROL H:Front B Speaker ON
	EXP16	SIRIUS RESET	SIRIUS reset control

2. FL DISPLAY

FLD (HCA-19MM02T) (FR: FL101)



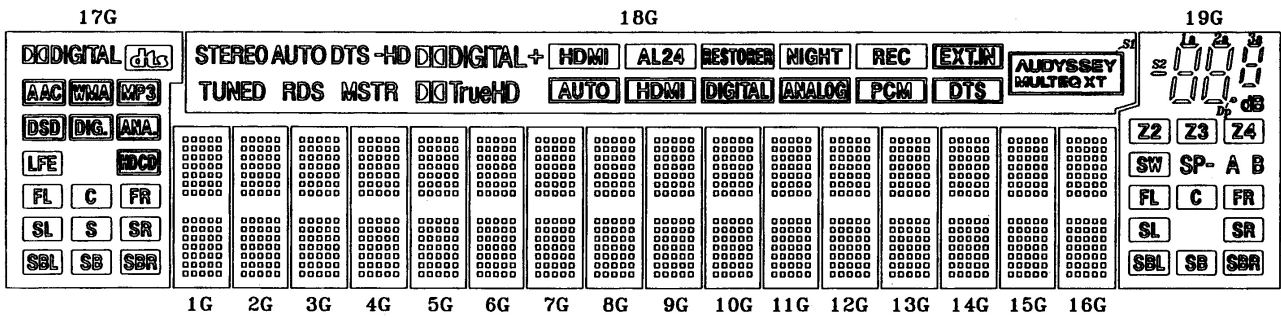
PIN CONNECTION

PIN NO.	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41~5	4	3	2	1
CONNECTION	F2	F2	NP	NP	VDISP	L-GND	D-GND	VDD	OSCO	RESET	CS	CP	DA	DO	TEST	Q _{19G}	Q _{18G}	Q _{17G}	17G	18G	19G	NX	NP	NP	F1	F1

Notes

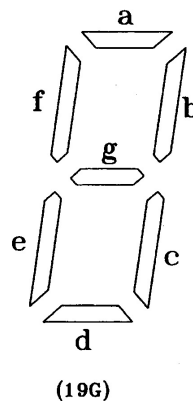
- 1) Fn : Filament pin
- 2) nG : Grid pin
- 3) NX : No Extended pin
- 4) NP : No pin

GRID ASSIGNMENT



(1G~16G)

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25
26	27	28	29	30
31	32	33	34	35
36	37	38	39	40
41	42	43	44	45
46	47	48	49	50
51	52	53	54	55
56	57	58	59	60
61	62	63	64	65
66	67	68	69	70



ANODE CONNECTION

	COM1~COM16 1G~16G	COM17 17G	COM18 18G	COM19 19G
SEGB 1	1		XT	S2
SEGB 2	2		MULTIBO	1a
SEGB 3	3		AUDYSSBY	1b
SEGB 4	4		S1	1f
SEGB 5	5		DTS	1g
SEGB 6	6		EXTAN	1c
SEGB 7	7		PCM	1e
SEGB 8	8		REC	1d
SEGB 9	9	dts	ANALOG	2a
SEGB 10	10	DIGITAL	NIGHT	2b
SEGB 11	11		DIGITAL	2f
SEGB 12	12		RESTORE	2g
SEGB 13	13		HDMI	2c
SEGB 14	14		AL24	2e
SEGB 15	15		AUTO	2d
SEGB 16	16		HDMI	3a
SEGB 17	17	MP3	+	3b
SEGB 18	18	DMA	DIGITALHD	3f
SEGB 19	19	AAC	DIGITAL	3g
SEGB 20	20		MSTR	3c
SEGB 21	21		HD	3e
SEGB 22	22		DTS	3d
SEGB 23	23		RDS	Dp
SEGB 24	24	ARA	AUTO	dB
SEGB 25	25	DIG.	TUNED	Z2
SEGB 26	26	DSD	STEREO	Z3
SEGB 27	27			Z4
SEGB 28	28			
SEGB 29	29			
SEGB 30	30			
SEGB 31	31			
SEGB 32	32			
SEGB 33	33	DCB		
SEGB 34	34	LFE		
SEGB 35	35			

	COM1~COM16 1G~16G	COM17 17G	COM18 18G	COM19 19G
SEGA 1	36			
SEGA 2	37			
SEGA 3	38			SW
SEGA 4	39			SP-
SEGA 5	40			A
SEGA 6	41			B
SEGA 7	42			FL
SEGA 8	43	FR		C
SEGA 9	44	C		FR
SEGA 10	45	FL		SL
SEGA 11	46			SR
SEGA 12	47			SBL
SEGA 13	48			SB
SEGA 14	49			SBR
SEGA 15	50			
SEGA 16	51	SR		
SEGA 17	52	S		
SEGA 18	53	SL		
SEGA 19	54			
SEGA 20	55			
SEGA 21	56			
SEGA 22	57			
SEGA 23	58			
SEGA 24	59	SBR		
SEGA 25	60	SB		
SEGA 26	61	SBL		
SEGA 27	62			
SEGA 28	63			
SEGA 29	64			
SEGA 30	65			
SEGA 31	66			
SEGA 32	67			
SEGA 33	68			
SEGA 34	69			
SEGA 35	70			

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