H3000 Ultra-Harmonizer(R)
SERVICE MANUAL

Eventide
the next step

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INTRODUCTION

The purpose of this service manual is to provide technical information on the H3000 Ultra-Harmonizer. It is meant as a starting point in trouble shooting any problems encountered with the H3000 in the field and to provide some insight into its capabilities. Some familiarity with its operation is necessary so refer to the H3000 Instruction Manual for help with basics.

The H3000 is a software-based, digital audio, signal processor which uses electronically balanced, stereo inputs and outputs to produce a variety of audio effects. These range from simple time delay to pitch shifting. In addition to its audio capabilities the H3000 includes a sophisticated MIDI implementation which allows it to communicate with other MIDI devices.

SIGNAL PROCESSING ARCHITECTURE

The H3000 is a general purpose, software based signal processing device. This allows a quicker design cycle and flexible signal processing algorithms. The primary goal is a stereo pitch shifter, so the architecture is based on the computational needs of pitch shifting.

In addition to raw computing power the H3000 is a flexible, software based design, the signal processors are RAM based, so that their programs are downloaded by the host microprocessor. Also, the host easily changes signal processing parameters while the signal processing programs are executing. Finally, the signal processors address a large block of memory in order to implement long audio delay lines.

A Shared Resource Multi-Processor

The signal processing elements (for convenience called "PELs") share most of the available resources, including the data converters, the interface to the host processor and, especially, the large block of memory for delay lines.

The architecture is built around a single "global" bus. Attached to this bus are all of the PELs, the delay memory, the A/D and D/A converters, and the host interface. The bus is active only when data is to be transferred between devices on the bus. Each processor has its own local memory, allowing the bus to remain free during non-I/O processing.

The PELs

The PELs are centered around the Texas Instruments TMS32010 DSP processor which use external RAM for program memory. Its simple external I/O port design allows it to interface to the global bus relatively easily. Each PEL consists of a TMS32010 along with 2 K words of 16 bit external "program" memory. Each processor also contains 144 words of internal "data" memory. Also, mapped into the program memory space of each processor is a unique "boot" ROM for each of the PELs.

The processors run at 18.3 MHz, yielding an instruction time of 218 nanoseconds. At the sample rate of 44.1 kHz this gives exactly 104 single-cycle instructions per sample period for each of the PELs. In the TMS32010, most instructions operate in a single cycle, with the exception of branch instructions, subroutine calls and I/O instructions.

The processors are connected to the global bus through bidirectional data buffers. They are only attached to the bus during the execution of an I/O (IN or OUT in TMS32010 code) instruction.

Global Bus Addressing

The addressing of the global bus is tied very closely to the I/O port structure of the TMS32010. Like the TMS320, the global bus has 8 read ports and 8 write ports, each mapped to the various peripheral devices on the bus. The PELs gain access to the global bus by using the I/O instructions "IN" and "OUT". Since the IN and OUT instructions are 2 cycle instructions, all bus accesses require at least two instruction cycles.

The small number of port addresses severely limit the number of peripheral devices allowed on the bus. This is overcome by expanding one of the sixteen bit write ports into sixteen 12-bit ports. It is done by decoding the upper four data bits and using those bits to address the additional registers. The additional address space allows for a number of "flag" type registers, interrupt control registers, and two frequency synthesizer control registers.

The Host

The host processor is the nerve center of the H3000, controlling all aspects of the machine. An 8-bit microprocessor, the 6809, is the host. Given input from the front panel and the MIDI control port, the host controls the signal processors. This includes loading executable code into each of the PELs, calculating and setting all signal processing parameters, and controlling analog input and output levels. As great as the responsibilities of the host are, they are not very computationally intensive.

The host has access to the global bus, but in a more limited way than the PELs. The slower 6809 is limited to one bus access per sample period, about once every 22 microseconds. With this method, complex bus arbitration is unnecessary, while an adequate data rate to the PELs can be sustained.

The Host Interface

In interfacing with the PELs, the host has two main functions. First, before anything can happen, the host must load executable code into the program memory of the PELs. Once the PELs are up and running, the host must then control various parameters of the signal processing algorithm. The host transfers data to the PELs with two sixteen bit registers, the Host Address Register and the Host Data Register. These registers form a unidirectional bridge from the 6809 to the global bus. The 6809 can write to the host registers, while the PELs can read from them. In addition to the host registers, the host has control of the PEL reset and of the sample clock input to the PELs, the BIO input. These are both used to control the PELs during the program loading process.

The Host Address Register is used in two different ways, depending on whether program code is to be transferred or parameters are to be changed. When code is to be loaded into the PELs, the upper 4 bits of the address register determine which PEL the data is destined for. The lower 12 bits specify the destination address in the PEL's program memory. When parameters are transferred to a PEL, the address refers to the internal data memory of the PEL. The upper 8 bits of the Host Data Register then determine the destination PEL.

In both cases, the PELs must execute code to read the host interface. In the case of loading programs into PELs, this code is located in the boot ROMs and is executed after the host resets the PELs. For parameter changes, the code must be inserted into the program loops of each of the signal processing programs.

Mailboxes

For inter-PEL communication, there are three sixteen bit registers called "Mailboxes". The mailboxes enable one processor to "deliver" a message, to be picked up at a later time by another processor, or, by the host. They are the primary communications link between the processors. Typically, the messages exchanged represent audio signals traveling from PEL to PEL.

The mailboxes are attached to the global bus and can be accessed every processor cycle. This enables many messages to be passed between processors during the course of one sample period. Mailboxes are also used to transfer data from the PELs to the host processor. This is the only data path from the PELs to the Host.

Delay Memory

The delay memory is a 64 K word block of memory that is used to create audio delay lines. 64 k by 4-bit dynamic RAMs are used for this. The delay memory cycle time is once every two processor cycles. Since the TMS32010 has only a 4 K word external address space (and this is limited to program memory only), special hardware is used to address the delay memory.

The delay memory is accessed through two separate ports on the global bus. One, the Delay Address Register, is a sixteen bit register that controls the address of the next delay memory cycle. The other, the Delay Data Register, is used to read or write data to the delay memory. Thus, reading from or writing to the delay memory requires two global bus accesses, the first to specify the address and the second to actually read or write the data.

In order to ease the I/O trouble of delay accesses, the Delay Address Register is equipped with a set of counters. Each time a read is completed from the delay memory, the address register is incremented, allowing successive locations to be read more efficiently.

Analog Input and Output

The audio input is provided by a two channel, 16-bit analog to digital converter, sampling at a rate of 44.1 kHz. The two channels of data, multiplexed in time, are available at the same address on the global bus. The right channel's data is available during the first half of the sample period and the left channel's data is available during the other.

The audio data is re-converted to analog by two 16-bit digital to analog converters. The left and right D/A converters each have their own address on the global bus. The converters can be set to run at the input sample rate of 44.1 kHz (synchronous), or at a variable sample rate (asynchronous). The variable sample rate is provided in order to allow pitch shifting without the need for digital decimation/interpolation filters.

The variable output sample rate is provided by a pair of frequency synthesizers. A 40 MHz clock is divided down to provide an output sample rate that can vary from 22 kHz to 88 kHz. The control inputs to the frequency synthesizers are available on the global bus, and thus can be controlled by the PELs or by the host processor. On each new output clock cycle, the frequency synthesizers set status bits to indicate that data is needed for the D/A converters. These bits can be read and tested by the PELs.

The Status Port

The status port is sort of the catch-all location in the bus design. A read of the status port returns the values of a number of one-bit flags in the system. Some are general purpose bits, intended for handshaking and triggering events. Others are special purpose, including the Odd/Even Sync bit (explained under synchronization), and the frequency

synthesizer status bits. Writes to the status register are channeled to various registers, depending upon the value in the upper 4 bits of the data word. The possible destinations include the bit registers mentioned above, the frequency synthesizer control words, and interrupt lines for both the host processor and the PELs.

Bus Allocation

Global bus cycle allocation is based around the input sample period. Each 22 microsecond sample period is evenly divided into 104 time slots, each slot corresponding to an available bus cycle. One bus cycle per sample period is reserved for the host processor, leaving 103 cycles available for the PELs. Also, the delay memory is unavailable for 4 time slots per sample period, due to the refresh needs of its dynamic RAM.

Bus contention will result if any two PELs access the global bus simultaneously, and is to be avoided. There is an exception to this rule, though. Two or more processors can access the bus simultaneously *if* they are reading from the same device. This is particularly useful for reading data from the A/D converters and for reading from the host interface registers.

Synchronization

The bus design makes processor synchronization a crucial issue. Synchronization in this architecture takes place on several levels.

The first and lowest level of synchronization is PEL sync, the synchronization of the internal states of the TMS32010 processors. The TMS32010 has four possible internal states. In order for multiple processors to access the same bus, these states must be synchronized. As with the host interface, the TMS32010 has no convenient way of doing this. To circumvent this problem a circuit which compares the output clock of the TMS32010 with a reference clock is used. If the two clocks are out of phase, this circuit eliminates one input clock period to the TMS32010. Clock periods are dropped until the two clocks are in phase. By applying this circuit to all of the PELs, synchronization between the processors is automatically maintained.

The highest level of synchronization is sample period sync. Since bus cycle allocation is based on the sample period, each processor must know where it is in relation to the sample clock. The TMS32010 has an input pin, BIO, specifically for this purpose. The BIO pin is a one bit input which can be used as a branch condition by the processor. In order to synchronize with the start of a sample period, the processor simply waits for the state of the BIO pin to change.

There is one final level of synchronization. Since the BIO input to the PELs is sampled only every other instruction, there is a one cycle uncertainty in synchronization. To eliminate this uncertainty, a middle level of synchronization, ODD/EVEN sync is provided. One of the bits in the status port gives an indication of whether the processor is on an odd

numbered cycle, or an even cycle. In combination with the BIO input, this is sufficient to allow the processor to align exactly with the start of a sample period.

H3000 SPECIFICATIONS

Inputs	Stereo, true differential balanced
Outputs	Stereo, differential, transformerless
Dynamic Range	Greater than 92dB "A weighted
Distortion	.01 % (.007 % typical) @ 1 kHz. 1 dB below clipping in "pitch change" mode, 0 shift, levels all at 0 dB
Sampling Characteristics	Full 16 bit resolution at 44.1 kHz sampling rate
Frequency Response	5 Hz to 20 kHz +/-1 dB, +/-.5dB typical
Delay	Up to 1.5 seconds
Pitch Variation	1 octave up, 2 octaves down
Power Requirements	75 watts, 110 volts to 130 volts, or 200 to 240 volts, AC 50/60 Hz
Size	Inches - (3.5h x 19w x 13.5d) centimeters - (8.9h x 48w x 34.3d)
Weight	13 lbs. net 18 lbs. shipping weight

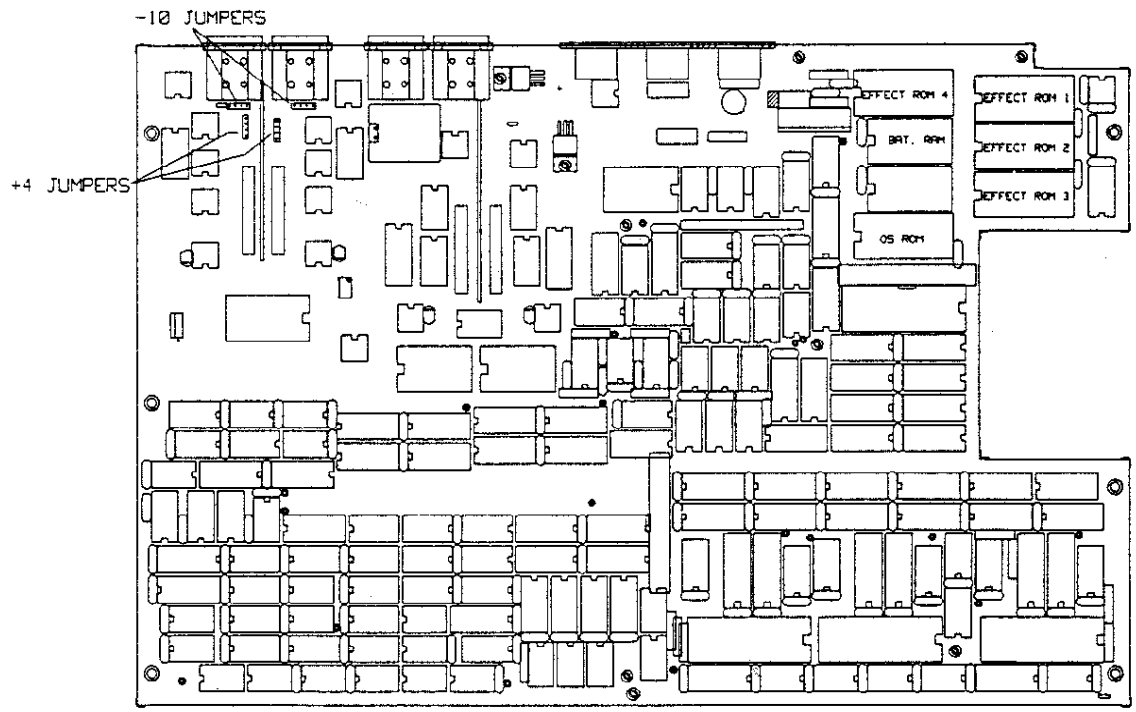
OPTIMUM PERFORMANCE FROM THE ULTRA-HARMONIZER

To obtain the best performance from the H3000, certain operating principles should be applied. Use the "hottest" input levels possible without clipping. A digital gain device is used in the input section which allows front panel control of levels. This device works best when it is "turned all the way up" in other words when it attenuates least. At the factory it is set for pro levels of +4 dBm, and internal jumpers 1 through 4 should be in the "+4 position" (see diagram on next page) so that the gain control devices will hardly attenuate. If consumer -10dBm levels are used, the jumpers should be moved accordingly so that your unit can operate at its optimum, high levels.

For best signal to noise ratio, always set the input level control so that the top bar of the level indicators flashes from time to time. If this results in output levels that are too "hot", reduce the output levels, not the input!

CHANGING INPUT LEVELS

The input levels of the H3000 can be changed to accept either +4dBm or -10dBm nominal operating levels. They are set to pro audio, +4dBm at the factory. To change this remove the top cover of the unit and pull the small jumper blocks from the +4 pins and put them on the -10 pins.



H3000 MAINPC

SERVICING THE H3000

This manual is intended to be used as a reference for the qualified technician responsible for repairing, maintaining and updating professional audio equipment. Printed circuit boards and integrated circuit chips are unfortunately often victims of abuse from well intended soldering irons. Heat and static electricity are too often responsible for electronic troubles. Extreme care should be used when working within the H3000. Refer repairs to a qualified service person whenever possible.

CONFIRMING A PROBLEM

Typical of most good trouble shooting techniques is being able to confirm and identify a problem and its symptoms before effecting any solutions. With a device as complex as the H3000 there are many occasions when operator error, wiring mistakes or faulty installation account for what was thought to be a device breakdown. The H3000 Owner's manual is the best place to start.

A thorough under-standing of the operator's manual will avert many operator error conditions. If the device is passing processed audio signals, displaying correct information on the front panel and reacting to the buttons and knob in most cases the H3000 is working properly.

A good understanding of differentially balanced inputs and outputs will take care of most wiring mistakes.

Faulty installations can be anything from bad audio connections, low ac line voltage or improper ventilation. The H3000 will get very hot if the top and bottom vent slots are blocked by other devices or the unit is in a sealed road case. Overheating in this way will have the effect of "crashing" the audio in time or "locking up" the front panel.

Some words about "crashing" the audio are certainly in order here. The entire unit relies on the two main address and data busses. If any component of the system fails (meaning any digital chip) the entire system could crash or at the very least the audio could be turned to noise and distortion. When the program running is a basic delay or a non-shifted Harmonizer and the audio output is not any facsimile of the input the audio has most likely "crashed". This is effectively random noise generated by such things as bus contention, wrong timing or no timing at all. Don't be overly concerned with the quality or level of this noise. It will change with different programs.

NECESSARY EQUIPMENT

Following is a list of essential test equipment for trouble-shooting an H3000. Much more sophisticated gear can be helpful but these will do in most cases.

100 MHz, dual trace oscilloscope

Audio oscillator/analyzer test set (Amber model 3501 or equivalent)

100 MHz frequency counter

WHERE TO START

Once a problem has been confirmed with the H3000 there is one basic question to be answered..."Should I tackle this myself or send it back to Eventide?" Doing the hardware modifications and changing software is not difficult. Trouble-shooting the digital electronics can be a bit tough. Remember that Eventide has all the parts, equipment and information necessary to repair the H3000 quickly.

SELFTEST

Perhaps the single, most useful tool in trouble-shooting the H3000 is the diagnostic SELFTEST EPROM available from Eventide. The SELFTEST routines are performed by inserting this EPROM into an EFFECT ROM slot and running the tests. It automatically tests and logs errors for the digital circuitry. Externally looping audio outputs to audio inputs and MIDI OUT to MIDI IN allows the unit to check its own audio specs (over time) and its MIDI section. There are also exercises for very specific hardware areas that together with an oscilloscope can greatly aid in trouble-shooting. For more information contact an Eventide dealer or Eventide directly.

DIGITAL TROUBLE-SHOOTING PROCEDURES

Here is a general procedure to follow if a problem is confirmed and suspected to be digital in nature. Use the schematics and circuit descriptions for better understanding.

1) Check all power supply voltages.
   U1 = +5 volts (4.85 is acceptable)
   U17 = +15 volts
   U18 = -15 volts
   U20 = +5 volts
   U21 = -5 volts
   U19 = -5 volts

2) Check Central Timing Circuits. Measure the CLK1S signal for 44.1 kHz and waveform stability.

3) If there is no audio output from the H3000 check the A to D converter (U15) for output data at pin 27.

4) Check the RIGHT OUTPUT SAMPLE RATE and LEFT OUTPUT SAMPLE RATE signals in the Interface to Converters section. These are both test points.

5) If the unit seems to do nothing at all (locked-up display, no audio) check the RESET circuit for a high voltage level at power-up.

6) Check the Brain signals.
   Interrupts
   Brain address lines
   Brain data lines
   BRAIN R/W
   CLKE and CLKQ

7) Check Global Data bus lines. They will not look like textbook perfect square waves. They should not be held to any strange levels.

8) Check PEL sync (described in Central Timing Circuit description) and PEL signals.

ANALOG TROUBLE-SHOOTING PROCEDURES

The analog section of the H3000 is fairly simple. Here is a basic procedure to follow if an analog problem is suspected.

1) Load program #102: DUAL SHIFT.
   Set pitch shift to 1.00 on both channels.
   Set delay parameters both to zero.

2) Input a +4 dBm, 1 kHz sine wave to the H3000.
   Set the input and output levels on the H3000 to 0dB.

3) At this point normal signal tracing steps can be used. Keep in mind that the left channel is almost a mirror image of the right. This makes comparisons very easy.

TROUBLE-SHOOTING GUIDE

The following chart outlines some general procedures for trouble-shooting the H3000 based on trouble reports received at the factory. It is not meant to be the only guide used for repair, rely on and develop a common sense approach to the device and its symptoms.

SYMPTOM	POSSIBLE PROBLEMS
Nothing happens upon turn-on. No display or no clicks or no hum.	No AC line voltage getting to unit. Blown fuse (1 amp, slo-blo). Voltage selector switch on back in wrong position. 8 pin MOLEX power connector inside unit unplugged. Front panel ribbon connector loose.
No display action upon turn-on. Only a dim backlight.	Voltage selector switch on back in wrong position. **Q...**Does the Bypass Switch operate? **Yes...**Press function then adjust contrast with the knob. Check the Front Panel board. **No...**Check the +5 volt regulator (U1). Press in socketted IC's to make sure they are seated fully. Push Tape Speed Controller board fully on. Check Front Panel board.
Blows fuses immediately.	Voltage selector switch on back in wrong position. Check CR1 rectifier on chassis for short circuit. Check insulator pad under CR1 (rectifier) and U1 (+5 volt regulator) Check all power supplies.
Audio crashes after warm-up.	Do all modifications. Check Central Timing Circuits. Check PEL synchronization (refer to Central Timing description). Reset operating system.
No audio at all.	**Q...**Does audio pass when H3000 is bypassed (LED off)? Is input bargraph lighting?

No audio at all cont.	**No...**Check external wiring. **No...**Check external signal flow and balanced line connections. **Simplify the hookup as much as possible.** Try a high output mic directly into the H3000 and headphones plugged into the output to eliminate most variables. **Yes...**Check output level settings. **Yes...**They should all be at 0dB. Try different programs making sure they are not using triggered softkeys (e.g. Dual Shift). **Q...**Are both channels bad? **Yes...**Check A to D data output. If okay, try virginizing. Do all modifications (sync. problem). If still bad use digital trouble-shooting procedure.
One audio channel bad.	Check effect program running. Many are mono in, stereo out which use the left channel input and shut off the right. Reverse input cables. Check audio when bypassed. Check D to A converter (PCM53).
No response to MIDI input.	Check MIDI enables on H3000. Use MIDI Mon. function to see data coming into the H3000. This is detailed in the instruction manual. Check U68 (opto isolator).
Won't load programs. Displays >>SEQ<< message when load key is pressed.	MIDI transmit functions need to be disabled for program loading to resume normally. Read instruction manual sections on MIDI.
Won't save presets. Saving locks up front panel.	**Q...**Is memory full? It will display "Not enough room to save preset..." if full. **Yes...**Delete unwanted presets. **No...**Reset operating system.

H3000 ALIGNMENT PROCEDURE

There are only four adjustments available on the H300C P.C.B. These are in the A to D converter section. There is a DC bias adjust pot and a distortion adjust pot for each channel. Adjustments should never be necessary under normal operating conditions. If, however, a critical component in the A to D fails and is replaced, both channels should be checked and adjusted as needed. Alignment is best done using a distortion analyzer and an oscilloscope. The procedure is as follows:

1) Connect an audio oscillator to the channel 1 input of the H3000. Use a 1 kHz sine wave of approximately 4 dBm.

2) Load the DUAL SHIFT program (#102) and set the left and right pitch shift parameters to 0 cents. Set left and right delays to 0 ms. Set all input and output levels to 0 dB.

3) Let the unit warm up to operating temperature (at least 20 minutes).

4) Connect the H3000 output to the distortion analyzer input. Connect the analyzer's monitor output to the oscilloscope input. An external trigger from the oscillator will be helpful.

5) The H3000 should have an output of approximately +20 dBm. Make certain that the +4 dBm jumpers are in place. If the jumpers are set for -10 dBm the output will be clipping from too much gain.

6) Increase the input level to the H3000 and observe the clipping point on the scope. The top and bottom should clip at the same time, that is, symmetrically.

7) Set the distortion analyzer for distortion with the scale near 1%. Monitor the distortion residual (the T.H.D. and noise output from the analyzer) on the scope. There should be large spikes when the H3000 is clipping. The residual will show a positive spike for positive clipping and a negative spike for negative clipping. Vary the input level with the oscillator to observe the clipping action.

8) Turn the DC bias adjust pot of the appropriate channel until both distortion spikes (positive and negative) appear simultaneously as input level is adjusted above and below clipping.

9) When symmetrical clipping is reached turn the input level down to just below clipping and adjust that channels distortion pot for less than .01% distortion. Generally the H3000 will deliver .007%. Distortion analyzer filters may be necessary. 400 Hz highpass and 30 kHz lowpass filters are typical.

10) Repeat this procedure for the second channel.

11) If a gross adjustment of either pot is needed recheck both DC bias and distortion as there can be some interaction.

RESETTING THE OPERATING SYSTEM

This procedure is used when installing a "B conversion kit" but has other uses. It essentially clears many of the H3000's internal software registers. It can also clear all of the user memory, so beware. In S versions it will clear all user memory. In the H3000-B the operating system can be cleared without loosing the user presets. The procedure is as follows:

A. Depress and hold the FUNCTION key while you switch on the power to the unit.

B. Release the Function key.

C. When the H3000 displays "REMOVE ALL PRESETS?", press the "NO" softkey (the third softkey from the left).

D. When the H3000 displays "RESET THE OPERATING SYSTEM?", press the "YES" softkey (the second softkey from the left).

E. The H3000 will automatically load program number 100 "DIATONIC SHIFT" and display the program parameters.

NOTE: On rare occasions, after step B, the upper line of the H3000 display will flash, and then the display will black out. This does not necessarily indicate a malfunction. If this happens, continue with steps C and D, by pressing the third softkey from the left, and then the second softkey from the left. The H3000 should then display the parameters for the DIATONIC SHIFT program as indicated in step E.

NOTE 2: It is also possible that after changing from S software to B software without clearing the memory that strange results will be displayed on the H3000 front panel. These could be in the form of wrong characters in program names or too many characters where they don't belong. The solution to this is, unfortunately removing the user presets by pressing "YES" during the "REMOVE ALL PRESETS?" display.

TECHNICAL MODIFICATIONS

The H3000 has undergone a few technical improvements since its first shipment date. The changes are not drastic and can usually be done in less than an hour. They do not change how the device operates from the user's point of view. They do increase the unit's durability under extreme heat conditions and immunity to random timing problems. All of these changes have been implemented at EVENTIDE on current production models. However, any unit in the field may need one or more of these modifications.

1. These pertain to the MIDI thru port. To insure maximum drive capability of the MIDI thru signal these parts should be in place. They are located at the rear of the PCB by the MIDI input connector.

R156 should be 220 ohms, 1/4 watt
R158 should be 2.2k ohms, 1/4 watt
R159 should be 150 ohms, 1/4 watt
U68 should be 6N137 opto-isolator

These will greatly increase the number of MIDI units that can be chained from the In to Thru jacks.

2. This change relates to audio breakdown at extremely high temperatures. Only a very few units will need this, though it is advisable to check. The TMS32010 processors used are either TMS32010, TMS32010-16 or TMS320C10-14. The 32010 and 32010-16 are of the NMOS variety and require a faster clock rise time. The TMS320C10-14 is a CMOS device. The IC that drives their clock input is a NOR gate.

If U110, U120 and U130 are TMS32010 or TMS32010-16
then:
U117, U127 and U137 must be 74**ALS**02

If U110, U120 and U130 are TMS320C10-14
then:
U117, 127 and 137 must be 74**LS**02

3. These changes help to stabilize the "sync" of the three TMS32010 processors. The three processors must all operate perfectly in step with each other, one missed or lagging clock cycle can completely destroy the audio at the output. The two resistors are located near the right, front of the unit and the IC's are at the left side, near the middle.

R174 should be 1k ohm, 1/4 watt
R175 should be 470 ohms, 1/4 watt
U100 and U101 should be 74**ALS**163

The IC's can be socketted if so desired.

4. To correct some rare, occasional audio problems and self-test errors in the frequency synthesizer test the timing at U208 (74F08) is changed slightly by this modification. Add a capacitor to the bottom of the PCB.

Add a 56pF capacitor between pins 6 and 7 of U203.

The capacitor is at the AND gate's output to ground.

5. Certain external MIDI devices rely on other units to provide power through the MIDI lines themselves. The H3000 will not work with these unless pin 2 of the MIDI OUT and MIDI THRU jacks are connected to ground at the chassis.

Construct a 4 inch jumper wire with solder lugs on both ends. Use a #4 bolt, nut and lock washer to connect the wire to the empty hole on the PC board to the right of the MIDI OUT connector. Make sure that the washer is on the bottom of the PC board (for continuity). Attach the other end to the ground bolt on the chassis near the AC line filter.

SOFTWARE REVISIONS

The H3000 currently uses six Operating System versions for the three different models (H3000-S, H3000-B and H3000-SE). The following is a list of the EPROM configurations that are possible.

H3000-S

Version 1.53	BIGROM VER 1.53	512 K
	SMALLROM VER 1.53	256 K
Optional	SELFTEST VER 1.53	256 K
Version 2.16	SROM1 OPERATING SYSTEM	512 K
	SROM2 ALGORITHMS	256 K
	SROM3 MORE ALGORITHMS	256 K
	SROM4 FACTORY PRESETS	256 K
Optional	ROM5 SELFTEST VER 2.16	512 K*

H3000-B

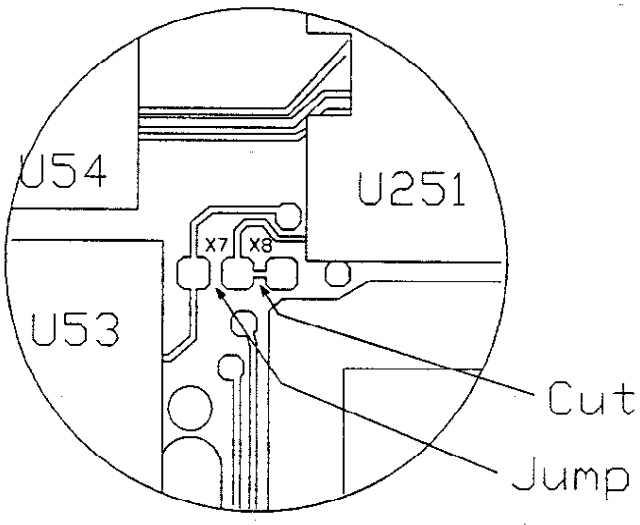
Version 2.11	ROM1 OPERATING SYSTEM	512 K
	ROM2 APPLICATIONS	512 K
	ROM3 MORE APPLICATIONS	512 K
Optional	ROM4 STUDIO PRESETS VER 2.13	512 K
Version 2.13	ROM1 OPERATING SYSTEM VER 2.13	512 K
	ROM2 APPLICATIONS VER 2.11	512 K
	ROM3 MORE APPLICATIONS VER 2.11	512 K
Optional	ROM4 STUDIO PRESETS VER 2.13	512 K
	ROM5 SELFTEST VER 2.14 or 2.16	512 K

Version 2.16	BROM1 OPERATING SYSTEM VER 2.16	512 K
	BROM2 ALGORITHMS VER 2.16	512 K
	BROM3 MORE ALGORITHMS VER 2.16	512 K
Optional	ROM4 STUDIO PRESETS VER 2.13	512 K
	ROM5 SELFTEST VER 2.14 or 2.16	512 K

H3000-SE

Version 2.16	SEROM1 OPERATING SYSTEM VER 2.16	512 K
	SEROM2 ALGORITHMS VER 2.16	1 M
	SEROM3 FACTORY PRESETS VER 2.16	1 M
Optional	ROM4 SVAIROM VER 2.16	512 K
	ROM5 SELFTEST VER 2.14 or 2.16	512 K

***Note...** In order to use the 512 K SELFTEST in this version the X7 jumper must be in place and the X8 jumper must be removed. Remove the solder bridge at X8 or cut the small trace, then put a solder bridge in place at X7. Also remove SROM2, SROM3 and SROM4 while the SELFTEST is installed. Reverse this procedure to remove SELFTEST for normal operation. In general 256 K EPROMs and 512 K EPROMs cannot be mixed in the four EFFECT ROM slots. However, 1 M and 512 K EPROMs can.



BLOCK DIAGRAM DESCRIPTION

To quickly and generally describe the way the H3000 accomplishes the processing it does, refer to the block diagram. There are 15 blocks that we'll cover. A more detailed explanation of the circuitry follows. In each block is a schematic name (a word, followed by SH). That is where to find the circuitry of that block.

The POWER SUPPLY, RESET block supplies the H3000 with regulated +5 volts for the digital circuits and various regulated and unregulated voltages for the analog electronics. The system reset line when applied, starts the microprocessors fetching and executing. This is the first event that needs to take place to get the system up and running.

Now let's get analog signals into the H3000. Audio inputs are fed to the 16 bit A to D section. This is where the two input channels are scaled, filtered and converted to a 16 bit, serial data stream. The crystal oscillator that drives the converter also serves as the main clock for the entire H3000. Fader control is simply digital control of the input and output levels.

The digital audio line is routed to the CONVERTER INTERFACE block. This is where the serial data from the A to D is converted to 16 bit parallel (two channels) data. Once converted it is sent to the Global Bus. The Global Bus is the main data communications bus in the H3000.

The CLOCKS block is where the main timing signals for all the digital circuits are derived. The input clock is 36.69 MHz. This clock comes from the A to D section mentioned earlier. The block contains many divider circuits as well as a PAL (Programmable Array Logic) which creates all necessary timing.

The BRAIN PROCESSOR block is considered the host microprocessor. It controls the front panel, loads programs, handles the MIDI interface and many other functions. This block also contains the program EPROMs and the non-volatile, RAM for storing user presets. It is truly the "brain" of the system.

The BRAIN INTERFACE is where the complex task of host communication takes place. It primarily allows the brain to read from and write to the Global Data Bus mentioned earlier. The brain controls most everything from the Global Bus.

PROCESSING ELEMENTS 1, 2 AND 3 are the digital signal processors in the H3000. These PELs create the audio effects that we hear from the unit. They are three identical

sections which all control different aspects of the audio signal depending upon the program running. The PELs get audio data from the Global Data Bus and manipulate it according to the information that the brain sends them. This info is in the form of parameters and DSP programs that the PELs get primarily from the brain. The processor in each PEL is a TMS32010. The TMS is a gigantic number cruncher that operates very fast. The H3000 uses three of them.

The GLOBAL CONTROL block is where specific operations are controlled. Operations such as reading from the A to D, writing to the D to A and writing and reading the delay address are accomplished here. It is really an expanded address decoding circuit. GLOBAL CONTROL also contains three 16 bit temporary registers called MAILBOXES which are used to move data between the PELs and to the brain.

The BULK MEMORY block is where the Dynamic RAM for implementing audio delay lines is located and controlled. The DRAM address information comes from the Global Bus and is multiplexed into the DRAM array. There is also a dynamic RAM refresh circuit and data input/output registers which transfer audio data to and from the Global Bus.

Two special purpose elements called Frequency synthesizers are contained in the FREQUENCY SYNTHS block. These circuits are used to manipulate the output sample rate in order to achieve pitch shift effects. Again, data from the Global Bus is used to set up a series of high speed counters. These counters provide the desired output sample rate.

The FRONT PANEL block is the user interface of the H3000. This consists of all the switches, the knob, the keypad and the 40 character by 2 line LCD display located on the front panel PC board. The Brain Data Bus controls these functions directly.

The BRAIN PERIPHERALS block contains the MIDI interface, fader data bus and decoders, and some brain I/O ports called Bit Latches. The MIDI interface consists of a UART, an opto isolator and some open-collector inverting line drivers. Standard MIDI In, Out and Thru are provided. The fader interface controls the digital attenuator circuits in the input and output section. The fader data bus carries all the level information for input, output, mix and feedback MDACs. An MDAC is a Multiplying D to A converter. These are used as digital attenuators and digital mixers.

The DIGITAL TO ANALOG block is where the results of all this data crunching are heard. Two channels of D to A conversion take place here. The 16 bit numbers are finally converted back to analog signals, are again filtered and scaled then, electronically balanced and sent to the output XLRs.

POWER SUPPLY AND RESET

The H3000's main power supply provides multiple voltages from one transformer. A dual primary transformer is used to enable operation from either 110 volt or 220 volt AC lines. Frequencies of 60 or 50 Hertz are acceptable. Switch S1 connects the two primaries in parallel for 110 volt lines and in series for 220 volt lines. The 30 VAC secondary is full wave rectified by a 1 Amp bridge (AC1 mounted on the PCB) then filtered by C170 and C171 which are mounted on the underside of the PCB. The bipolar +18 volts and -18 volts, unregulated, is sent to the analog input section regulators that will be described later. R165 drops the -18 volts to -10 for use in the A to D converter.

The 14VAC secondary provides the +5 volt power for all of the digital circuits. The center tapped secondary is rectified by CR1 which is a Schottky Bridge, mounted on the chassis. The middle pin of the rectifier is attached to its metal case so the case must be properly isolated from the chassis with an insulator pad. Otherwise the +7 volts will short to the case and most likely short out one of the diodes in the Schottky bridge. This +7 volts is filtered by four capacitors mounted under the PCB (C161, 162, 163, 164). U1 is the +5 volt regulator. R163 and R164 set up a voltage divider which trims the +5 volts via a reference pin. The case is mounted on the back of the H3000, inside of the heatsink. The regulator case is at +5 volts, which is why it is covered with a plastic cap. A little heat on the cap (from a heat gun) will help to snap the cap on in the event it must be removed. The regulator is totally isolated from the chassis by a pad and the mounting socket.

The RESET generator is the circuit which starts the H3000's digital circuits operating properly. C155 creates a long time constant when AC is applied. The delay is long enough for the +5 volt supply to stabilize, then U261 pulls the RESET line high. This reset is applied to the brain, which begins fetching instructions from memory.

ANALOG INPUT

The H3000 uses a single 16 bit multiplexed A to D and two D to A's to achieve 2 channel operation. The input (A/D) sampling rate is fixed at 44.1 kHz, (the same as that used in CD's), but the output sample rate is variable, making the converter section "asynchronous". The input, output, mix, and feedback levels are all digitally controllable. The following is a semi-detailed circuit description for channel A. Channel B is identical in operation. On the PCB channel B is usually the mirror image of channel A.

INPUT SECTION (A to D)

Female XLR connector J5 receives the input in differential form, couples it through caps C1, C6 and tie down resistors (R1 thru R7) into the buffer amps (U1A & U1B). Caps C2 and C7 suppress RF noise pickup. U2A performs Common Mode Rejection (hum rejection) and amplification, providing a choice of two different operating levels (-10dBm or

+4dBm) which is selected by jumpers Jmp1 and Jmp2 (with jumpers installed, +4 is selected). The output goes to the MDAC (U3) which allows 48 dB of precise digital gain control (from 0 to -48 dB attenuation).

A frequency preemphasis network (U4A, R14, R15, R16 & C12) sends a 9V p-p full scale signal to the 9th order input filter (U5) and to the "mix" buffer amp (U4). It is a "peak detected", preemphasized, version of this "mix" signal which is monitored by the bargraph on the front panel. This prevents the user from clipping emphasized high frequencies. Incidently, the 9th order Murata anti-aliasing filters need a low impedance source (and a high impedance load).

After the lowpass filtering, the signal is mixed at U6A with any feedback signal sent via R67 from the output DAC section. A gross offset is added by R21, R22, R23, C18, and CR1. Diode CR9 provides temperature compensated reference for biasing. A unique "auto-offset" circuit has been employed whereby the "tacit" offset is digitally controlled to sit in a preselected "quiet spot". A magnitude comparator (U178) compares the current 16 bit sample value to a jumper selected offset value and sends a "0" or a "1" to an integrator (U16A) whose filtered output is mixed with the "gross" offset from the diode biasing circuit. The ratio of resistors keeps the auto-offset from affecting high level signals.

The CX20018 A/D converter is a "dual slope integration" device. Basically, U47B drives the sample-and-hold cap (C27) thru transistor Q1. The held sample is "integrated down" in two different stages of resolution by U7A and U7B. The signal in the S/H amp is held while a current from the A/D is turned on, discharging the held voltage at a precise rate until internal comparators have their thresholds exceeded. At the same time the discharging current is turned on, a high speed counter starts and continues counting until the low order comparators flip (or a maximum count of 32,148 is reached). When the counter stops, it contains the converted value.

In a little more detail, U7A holds the acquired sampled values and does the first nine bits of coarse integration. A zener reference set by R72, R71, CR5, provides the integration current for both channels. The output of U7A splits to the second integrator stage, and to the converter (thru R26) for high order comparison. After the high order comparator "flips", the second integration stage, U7B, amplifies and biases the remainder of the held sample such that feedback diode CR3 clips the lower portion of the waveform, sending an amplified view of the remaining sample to the converter thru R30. The remaining sampled value is thus "zoomed in on" for integration until the low order internal comparator finally flips, accounting for the last seven bits of resolution. A high resolution offset adjustment (R27, R28, R29, R31, C25) must be used in the second integration stage to properly align the internal, low bit comparator. This is the only channel distortion adjustment required. C23 and C24 shunt high frequency digital trash to ground before entering the converter.

MASTER CLOCK GENERATOR

The CX20018 requires a fair amount of external circuitry including a crystal oscillator circuit, which provides the master system clock. The crystal tank circuit is made up of Y1, L1, C48, and C49 (in a series configuration). R83 and CR14 provide a .6V reference to pin 23 of the CX20018 converter which internally selects a divide by two for the 73.382 MHz master clock. The resulting 36.691 MHz clock appears as a .5V p-p swing at pin 22. This is biased up, amplified and buffered by C60, R74, 75, 76, and Q3. Spaces are provided for C93 and C53 to tune or quell harmonics, but these are generally not used. C63 bypasses Q3. The A/D converter clock rate of 73.382 MHz is used to achieve the necessary resolution and to provide 44.1 kHz by the following divisions: $XTAL/2/13/2^7 = 44.1$ kHz.

There are five different required voltages which are supplied by regulators U60 through U64. Surrounding caps are simply power supply bypass. The voltages are all noted on schematics.

INTERFACE TO CONVERTERS

AUTO OFFSET CORRECTION

The auto offset correction circuit is used to provide a more stable noise floor in the H3000. U178 is a magnitude comparator which compares a preset 4 bit number (permanently selected by the 4 jumpers on PCB grid) to the 4 least significant bits of audio data. The result of the compare is an output at pin 5 of U178 (74LS85) then sent to the 13 input NAND gate of U179. When bits AD4 through AD14 are inactive (no input signal) the results of the compare and AD15, which is the most significant bit, will control the output signal of U179. The output of U218 is sent to the A to D converter section which demultiplexes the two channels then, integrates them to produce a slight DC offset to add to the input of the A to D which helps to keep things more stable.

INPUT SIGNAL

This section converts the serial data from the A to D into parallel data and transfers it to the global data bus. CLK10 is passed through U203, inverted by U202, then again inverted by U218 to provide some timing delay, but no effective change in logic. Pin 6 of U218 is then sent to the AND gate in U203 with the much faster CLK5 signal. The output at pin 8 is a series of 16 pulses while pin 10 is high, then low while pin 10 is low. This signal is inverted and sent to the A to D as BCLK which internally controls data transmission in the SONY chip. This signal also clocks the 16 bit shift register formed by U180 and U181. Here the first burst of 16 clocks convert one channel to parallel then the second burst converts the other. This parallel data is then put on the global data bus through latches U182 and U183. At this point the PELs can begin manipulating data to create the wide range of audio effects in the H3000.

RIGHT, LEFT OUTPUT

The eight HC374 latches, U184 through U191, are responsible for sending processed audio data to the D to A converters. The processed data is available at various times on the global data bus. It is latched into a first set of 16 bit latches (U184, U185, U188 and U189) by the WRITE RIGHT DAC and WRITE LEFT DAC signals. Then the OUTPUT SAMPLE RATE (right or left) signals latch the data through U186, U187, U190 and U191 to the D to A converters. The 16 bit data busses LDAC and RDAC are connected directly to the Burr Brown D to A converters.

OUTPUT SAMPLE RATE SELECT

The H3000's output sample rate is variable in order to accommodate the difficulties found in pitch shifting. U195 controls where the sample rate is derived from. This 4-line-to-1-line decoder is controlled by the FREQ SELECT A and B inputs from the brain peripherals section. Both decoders are always enabled. The I0 inputs are used for all non-pitch shifting programs such as reverbs and filters. I1 is selected when both Y outputs are to use the same RIGHT CLOCK signal. This is done in programs where both output sample rates are the same (e.g. Stereo Shift). I2 is selected when the two output signals are being pitch shifted to different intervals (Dual Shift, Diatonic). Here RIGHT CLOCK and LEFT CLOCK are sent to the Y outputs of U195. There is one special case...Timesqueeze. This program uses the I2 condition for the audio output sample rate, then a wire jumper is put in place at pin 12 of U195 so that LEFT CLOCK FSYN is sent to the Timesqueeze PCB. I3 is selected for use with an external clock, but has not been implemented.

Two Dual, Monostable Multivibrators are used to condition the output sample rates. U193 and U194 are used to stretch the pulses to more exact widths. R151 and C151 create a time constant for accurately latching data into the DAC through U191 and U190 on the right side. R150 and C150 do the same thing only are set to different values for use in the output deglitch circuitry. These are timed to remove unwanted switching noises found at the DAC outputs. U192 is used as a NAND-Gate Flip Flop in order that the PELs can monitor the status of the output sample rate. The PELs do this by watching the RIGHT FSYN STAT and LEFT FSYN STAT signals.

CENTRAL TIMING CIRCUITS

CLOCK GENERATOR

The main timing signals for the H3000's digital operation are derived with these circuits. On the lower, left of the page is the master clock output (MCLK OUT). This is the crystal oscillator, divided by two, from the A to D section. 40 MHz is only an approximation (it was based on a 48kHz sample rate, which was not used). The real frequency is 36.69

MHz. For purposes of discussion, 40MHz is good enough. U200 buffers and inverts the analog-type signal (now called CLK1). U201 divides CLK1 by two to derive CLK2 (20MHz). CLK2 is routed to the clock inputs of U100, U101 and U102. This set of programmable, synchronous dividers (synchronous means that all the outputs change at the same time) derive ten other clock signals. U100 is set as a divide by two circuit. Thus, CLK3 is 10MHz, CLK4 is 5MHZ, CLK5 is 2.5MHz and CLK6 is 1.25MHz. This chip effectively divides the CLK2 (20MHz) signal by 16 (1.25MHz). U101 is not as simple. It is set up as a divide by 13 circuit. Consult a data book for more specific operational details. These outputs are not symmetrical square waves. U102 is set up to divide by 16 with two outputs unused. CLK1S is the input sample rate which is in reality 44.1 kHz. There is a test point labelled 1S for checking this. CLK2S is 44.1 KHz divided by 2 or 22.05 KHz. Remember that CLK2 through 10 were only approximations of the actual frequencies but that CLK1S and 2S are exact values.

PULSE GENERATORS

All of the main timing signals are fed to U103 and U104 to create many important signals for the system. U103 is a factory programmed PAL (**P**rogrammable **A**rray **L**ogic) chip. The outputs of this chip are sent to U104, an octal latch, which deglitches them and maintains synchronous transitions. These outputs go to many places in the H3000. Don't be fooled by pin 16 of U104, when left unconnected it "floats" between logic states.

CLK4 is sent through U129 to provide enough drive for the BRAINCLK signal which goes everywhere on the board. Most notably to the BRAIN microprocessor U50, a 68A09. CLK6 and an inverted version of CLK5 (NOTE: logical inversion is denoted on the schematics by *) is sent to NOR gate U222 then latched through U139 to create the signal BRAIN SYNC. This signal keeps the BRAIN in synchronization with the PELs (the TMS32010 processors). All of the processors must stay "in sync" for the entire system to work.

PEL SYNCHRONIZATION

Keeping the 3 TMS32010's in sync is done by U129, U139, and U200. This is a most critical section of the H3000. It is most susceptible to over heating, cold starting, component tolerances and clock rise times. The three PELs (**P**rocessing **EL**ements are described later) must operate on the same clock cycle. If one, for example runs a bit slower than the others it will corrupt the audio data that is being processed by the three. This will most likely result in "GARBAGE AUDIO". To keep the three in step a correction circuit is used. Each TMS32010 has a clock input (approximately 18.6 MHz) and a divided by four clock output (pin 6). This 4.65 MHz signal is then compared to the main timing CLK4 signal, which is the same frequency, by an Exclusive OR gate in U129. If this were a perfect world the two clock signals being compared would be exactly the same and the output of the EXOR gate would remain low. Needless to say the 2 signals will most likely slide in and out of sync with time, temperature and component tolerances. When this happens a short high pulse will be seen at the XOR output. This difference signal may look a bit strange on an oscilloscope. The pulse may appear to have very slow rise and fall slopes and not reach

+5 volts. Don't despair, this is normal. When the difference signal is long enough to throw the processor out of sync with the rest it is latched high by a delayed CLK2 signal (U200 provides the delay) and is sent to the NOR gate driving the CLKIN pin of that TMS32010. The high at that NOR gate's input effectively disables the output of the gate (CLKIN of the TMS32010) long enough for the CLKOUT signal to re-sync with CLK4. This process drops one CLKIN cycle to the TMS32010. A few of these correction operations during one input sample period could cause a sync failure..."GARBAGE AUDIO".

BRAIN PROCESSOR

The H3000's "brain" is a 68A09 microprocessor (U50 on the schematic). How this processor operates is beyond the scope of this manual. For detailed information consult a Motorola, 8 Bit Microprocessors data book.

PROCESSOR

The 68A09 must have a RESET signal before it will begin fetching instructions. When power is applied to the unit the RESET line is held low momentarily then goes high. This action starts the system running. BRAINCLK is the 68A09's oscillator (see the Central Timing Circuits) which runs at about 4.5 MHz. The BRAIN SYNC signal is what keeps the 68A09 synchronous with the PELs. This signal indicates the beginning of an input sample period. NMI, IRQ and FIRQ are all interrupt request lines to the 68A09. Various parts of the H3000 can generate an interrupt to the 68A09. For example; if a byte of MIDI data is received and needs to be interpreted by the brain, the IRQ line will go low (generated by U66, the UART on the Brain Peripherals schematic) and the brain will do what is necessary with the MIDI data. NMI and FIRQ work in a similar fashion, but communicate from other sections of the H3000. CLKE and CLKQ are timing clocks generated by the 68A09. They are both 1.14 MHz, but the two are out of phase. The brain also generates the BRAIN R/W signal to indicate whether it is reading from the data bus or writing to the data bus. The 68A09 uses a standard 8 bit data bus and a 16 bit address bus.

SYSTEM ROM

U53 is a 512 K EPROM. It contains the operating system for the brain. The operating system is the set of instructions that makes the H3000 tick. The address lines A0 thru A13 are derived from the brain address bus, and the address lines A14, A15 and A16 are derived from the EXPANSION ENABLE multiplexor, U52. The OE* pin of the EPROM is tied to the BRAIN R/W because the EPROM is only read from by the BRAIN. The CE* pin (pin 22) is controlled by the ADDRESS DECODE PAL, U56.

The four EPROMs, U250, U251, U252 and U253 all hold programs for the TMS32010 processors (PELs). These are the application EPROMs. In the H3000-S version there is one

256 K EPROM called "SMALLROM". In the H3000-B there are as many as four 512 K EPROMs called ROM1, ROM2, etc. These EPROMs are interchangeable within the four sockets provided. There is a difference when installing 256 K or 512 K chips. Jumpers X7 and X8 are pads on the main board used for configuring the EPROM addressing. A 256 K EPROM needs only A15 in addition to the brain addressing, therefore A16 and A17 are held at +5 volts by the jumpers X8 and X6. With 512 K EPROMs, X8 is cut from +5 volts and connected to X7 (pin 4 of U52) to enable A16. A17 remains for future EPROM expansion. When jumpering X7 to X8 a cut on the PC board must be made between X8 and +5 volts.

OE* of the application EPROMs is tied to the BRAIN R/W line through U217 just as the operating system is. CE* of each of these four chips comes from U254 which multiplexes the Brain Page bus.

ADDRESS DECODE

U56 is a Programmable Array Logic device. It is factory programmed to enable a system of extended addressing for the brain processor. This PAL enables the brain to address the extra bit (A16) in the 512 K EPROMs and can be expanded to address 1 M EPROMs with another cut and jumper on the PCB. The PAL is essentially a chip with many logic gates on it that can be configured by the user. It provides 6 output signals in the H3000 (pins 12, 14, 15, 16, 17 and 19). The rest are inputs. IO ENABLE is a signal which controls brain peripherals. BRAIN PAGE ENABLE is the control line for extending the addressing of the 68A09. Pin 16 enables the operating system EPROM. Pin 15 enables the 8 K Static RAM (U54) which is used by the brain to store data temporarily. Pin 14 selects the Non Volatile RAM (U55) which is used to store user presets which are maintained when power is off. The 8K NVRAM has a battery built in with a life expectancy of 10 years.

EXPANSION ENABLE

U52 is a quad, 2 line to 1 line Data Selector which provides the expanded address lines previously discussed. It is selected by the conditions of BA14 and BA15 which are NORed through U217.

BRAIN PAGE LATCH

U51 is a quad latch which latches the 8 brain data bits at the appropriate time to create 8 Brain Page bits. The Brain Page bits are then used to control the extended addressing of the brain. The Brain Page Latch is clocked by the signal PAGE LATCH from the Brain Peripheral Circuitry schematic.

TIMEKEEPER INTERRUPT

This flip flop (U213) is used to generate the NMI signal to the brain. NMI is used by the software to keep track of time and sample the action of the front panel wheel. When CLK1KS has a rising edge a low is generated at pin 5. This is an interrupt to the brain. The software can then reset the flip flop by sending a low to NMIRESET (pin 4).

PROCESSING ELEMENTS

It is this section that takes audio input data and manipulates it to produce all of the H3000's effects. There are 3 PELs. All are identical except for the pair of factory programmed ROMs (S288s) that are labelled "PROMSL1A" and "PROMSL1B" for PEL #1 and "PROMSL2A" and "PROMSL2B" for PEL #2, etc. These PROMs determine which PEL circuit is #1, #2 and #3. Otherwise all is the same. PEL #1 will be explained here but all of the information applies to the other two.

PROCESSOR

It is beyond the scope of this manual to describe how a TMS32010 processor operates. For more information consult a Texas Instruments data book. The chip is designed as a high speed signal processor. It is able to perform mathematical functions very fast. X2 is the input clock signal. This runs at 18.35 MHz. U117 performs the clock correct function that was explained in the Central Timing Circuits description. Pin 6 is the CLKOUT line that goes to the Central Timing schematic. The RESET TO PELS signal is similar to the Brain reset line, however, it is reset any time a new instruction is loaded into the PEL from the Brain (via the application ROMs). The INT* line is a little used interrupt to the processor. SAMPLE CLOCK is the 44.1 KHz input sampling frequency. WE*, DEN* and MEN* are all outputs from the processor which are activated by different software instructions. The TMS32010 has a 16 bit data bus (PD0 through PD15) and a 12 bit address bus (PA0 through PA11). It isn't a big address bus but, remember it was designed for speed.

PROGRAM MEMORY

U111 and U112 make up the PEL's program memory area. This is the area that contains the signal processing instruction set for the PEL. They are 2K by 8 bit RAMs. WE* is an write enable from the TMS320. CE2* is a chip enable which is taken from the MEN* of the TMS. CE1* is the inverted version of PA11 (PEL ADDRESS #11).

LOADING PROGRAM

U113 and U114 are called BOOT ROMs. They are factory programmed and contain a short routine for the TMS320 which is executed upon receiving a RESET TO PELS signal. It loads an address and data from the Brain then checks to see if the information was for

PEL #1 (itself). If it is then, the TMS320 loads another set. This is done until all three PELs are loaded with signal processing programs.

IO STROBE

U117 and U128 decode various signals within the PEL to create the PEL ACCESS SIGNAL. When this signal is low the PEL is allowed to write addresses to the Global Address bus and data to the Global Data bus. U118 is an octal, tri-state buffer which connects the PEL Address bus to the Global Address bus. U115 and U116 are octal, tri-state transceivers (which means they can write to and read from the Global bus) which communicate data to the bus. The PEL ENABLE signal must be low in order for the PEL to access the bus.

BRAIN PERIPHERAL CIRCUITRY

This section of the H3000 handles the Brain decoding for functions such as display interfacing, Fader Bus control and special purpose Brain I/O operations. The MIDI Interface is also on this schematic.

MIDI INTERFACE

The **M**usical **I**nstrument **D**igital **I**nterface consists of a UART (U66), an opto isolator (U68), some open collector inverters (U69) and a 74LS163 (U67) to derive the BAUD rate.

MIDI is a serial data communications protocol which is clearly defined and adhered to by manufacturers. The hardware is also essentially standard. U67 is used to divide the 4.58 MHz, BRAIN CLK signal by 9. Pin 11 of U67 is 509 KHz. This signal is then sent to the UART, U66, which divides this frequency by 16 to get approximately 31.25 KHz. 31.25 KHz (+ or - 5%) is the specified BAUD rate for MIDI communications.

The UART 68A50 (**U**niversal **A**synchronous **R**eceiver **T**ransmitter, U66) is responsible for taking MIDI serial data in, converting it to parallel data and then sending it to the Brain, via the Brain Data bus, to be interpreted. It also handles taking MIDI data from the bus, converting it to serial form and sending it out to the MIDI output jack to be processed by external devices. Pins 3 and 4 are the 500 KHz input clock for U66. This is used for both transmitting and receiving data. Pin 2 is the receive data input (RxD) which comes from the output of U68, the opto isolator. Pin 3 is the transmit data output (TxD) which is sent through two inverter stages before going to the output jack. BRAIN CLKE (pin 14) is used to keep the UART in sync with the Brain. The 68A50 was designed for the 68A09 microprocessor that is the Brain. The Brain software controls the 3 chip select lines CS0, CS1 and CS2* and the register select line, RS. IRQ (pin 7) is generated (goes low) any time a byte of MIDI data is received. This interrupts the Brain so that the Brain can process the data. The data outputs of the UART are connected directly to the Brain Data bus.

The MIDI output is derived from the open collector inverters in U69. Pin 10 of U69 is connected internally to the collector of a transistor. Therefore, if nothing is connected to the MIDI OUT jack, no current will flow through R155. When no current flows the collector inside pin 10 remains open (stays at +5 volts) no matter what pin 11 does. With a proper load across the outputs (pins 4 and 5 of the MIDI OUT jack) pin 10 will go to ground and current will flow through R154, through the external devices circuitry and through R155 to ground. This forms the specified 5 mA current loop. MIDI IN is handled by U68. This is a 6N137 opto isolator. Pins 4 and 5 of the MIDI IN jack form the external current loop along with limiting resistor R159 and the LED between pins 2 and 3 of the opto isolator. D24 is used for protection only. Pin 6 of the opto isolator connects directly to the UART to provide it with serial data of the proper voltage level (the signal is pulled up by R158). R217, pins 9 and 10 form an invertor which drives another open collector inverter in U69. U69, pin 8 sends a copy of MIDI input data back to the MIDI THRU jack in order that devices can be chained together.

BRAIN IO DECODE

U60, U61 and U62 are circuits that decode the Brain Address bus to control certain functions. U60 is a 74LS138 (3-line-to-1-of-8-line decoder), and it creates the following signals:

EXPANSION IO ENABLE...Used to enable Timesqueeze option.

ENABLE for U62...Enables U62 for expanded decoding.

FASTHAND...Notifies the Brain that the PELs have completed some task.

DISPLAY STROBE...Enables the LCD to receive data from the Brain.

ENABLE for U61...Enable U61 for expanded decoding.

CLK to FADER INTERFACE...Latches data into the Fader Data Buffer.

BRAIN PORT ENABLE...Accessed when the Brain writes to the Global bus.

U61 is used for various read operations for the Brain. They are:

READ SWITCH ENABLES...Enables front panel switch information to be placed on the BD bus.

READ STATUS QUICK...Enables the Brain to quickly read the STATUS BITS at U80.

PAGE LATCH...Clocks Brain data into the Brain Page Latch.

READ PEL LOW...Enables data transfer from the PELs to the Brain via the Global Data bus. Controls the low byte.

READ PEL HIGH...High byte control for above.

U62 also decodes addresses, but it is a 74LS259. This 8 bit, addressable latch uses only BD0 and sends it to the output address set up by BA0, BA1 and BA2. The control lines generated are:

RELAY DRIVE...Controls the Bypass Relay.

PEL RESET...Controls the resetting of all the PELs.

BIOZ ENABLE...Enables the BIOZ sample clock in the PELs.

FREQ SELECT A...Used to select the output sample rate source.

FREQ SELECT B...Used to select the output sample rate source.

FADER STROBE ADDRESS HOLD...Used as a write strobe to U65 to enable an MDAC to receive data.

NMI RESET...Resets the interrupt flag called NMI.

FADER INTERFACE

The fader interface controls all of the digital attenuators in the Audio Input and Audio Output sections. U63 and U65 select which attenuator is to receive Fader Data, U64 then sends an 8 bit number to the MDACs via the MDAC bus.

U63 latches 5 Brain Address bits and the R/W line when U215, pin 12 goes high. BA0, BA1 and BA2 are sent to U65 to be multiplexed for control of 6 different MDACs in the Analog section:

R FB *CS...Right Feedback, Chip Select

L OUT LVL *CS...Left Output Level, Chip Select

L FB *CS...Left Feedback, Chip Select

R LVL IN *CS...Right Input Level, Chip Select

R OUT LVL *CS...Right Output Level, Chip Select

L LVL IN *CS...Left Input Level, Chip Select

U63, pin 7 is used to control the A/B inputs of the Dual MDACs U41 and U32. The other two lines from U63 (pins 10 and 15) are sent to the LCD as DISPLAY ADDRESS and DISPLAY READ/WRITE signals as well as enables for U65. U65 is finally enabled by the FADER STROBE ADDRESS HOLD line. When that line goes low, the current MDAC to be updated is selected. U64 at that point in time has already been latched with the Fader Data to be written into the MDAC.

BYPASS RELAY

Q20 is the transistor that drives the Bypass Relay found on the Audio Output schematic. The RELAY DRIVE signal biases R161 and the base of the transistor. The relay coil is connected between the two points labelled RELAY. D20 is used for surge protection and R160 limits the current from the +10 volt, unregulated supply.

FRONT PANEL

The front panel PCB contains all of the electronics for the user interface. The display, switches, wheel and contrast are controlled and monitored by the front panel data bus (FPD) which is actually directly connected to the Brain Data bus.

LCD DISPLAY

U1 is the 40 character by 2 line, liquid crystal display that provides the user with visual information necessary to operate the H3000. It contains on-board decoder/drivers which translate the 8 bit Brain information into readable characters at correct positions on the display. The character set available contains a wide assortment of numbers, letters and symbols. The display is accessed by the three signals DISPLAY R/W, DISPLAY ENABLE and DISPLAY ADDRESS. The FPD bus contains the code and location information for the display's on-board decoders.

The LCD is backlit by a matrix of LEDs mounted behind the crystal. +5 volts is applied to R23 which drops it by .65 volts for the LEDs which in effect controls the light intensity.

LCD contrast is the control of the viewing angle that the user sees. The signal ANGLE ENABLE clocks the latch U3 which takes 6 FPD bits and latches them to the outputs when the contrast is changed by the user. These values are then presented to weighting resistors R4 through R9 which form a crude D to A converter. The sum of these DC voltages is then applied to the VO pin of the display.

SOFT KNOB

The Soft Knob is the wheel on the front panel that allows the user to enter data into the H3000. The wheel itself is only a mechanical wheel that has a disc mounted to the back which interrupts the light inside of the dual photo-interrupter. A dual interrupter is used to enable clockwise and counter clockwise motion to be detected by the Brain. VOA and VOB are the outputs which are fed to U5 and put on the FPD bus when SWITCH ENABLE A goes low.

SWITCH READ ENABLE

U5 provides switch closure information to the FPD bus. This 74LS244 is a tri-state line driver. When SWITCH ENABLE A goes low, the information from the switch matrix is put on the bus. The switch matrix consists of the keypad, the lit bypass switch, and the 8 unlit switches. U4 is a hex "D" flip-flop that sends FPD signals to the matrix. It is clocked by the SWITCH ENABLE B pulse. These 6 signals are sent to the open collector, hex invertor U4. Unless there is a switch closure the outputs of these gates remain high because they are being pulled up by the resistors in R17. Closing any of the switches will generate a data byte to the Brain to indicate which one it was. The Bypass switch operates independently of the matrix. It also has an LED which is driven by the signal BYPASS LAMP and current limited by R2.

KEYPAD

The H3000's keypad is an arrangement of 16 switches. Pin 1 of the pad is common to the left, vertical row; pin 2 is common to the second vertical row and so on with pins 3 and 4. Pin 5 is common to the top horizontal row; pin 6 is common to the second horizontal row and so on with pins 7 and 8. Therefore, pushing the top left switch (1) will make pin 1 continuous with pin 5 and so on.

LEVEL DISPLAY

U6 and U7 control the LED bargraph levels for the left and right audio input signals. The LM3915's are bargraph drivers. The RIGHT DISPLAY and LEFT DISPLAY signals are DC voltages generated in the analog output section. An external reference is set up by the two resistors R11 and R12 for the left channel and R13 and R14 for the right channel. The LM3915 then outputs the appropriate signals to the LEDs. These output voltages are in the range of +3 volts.

GLOBAL CONTROL CIRCUITRY

The Global Control Circuitry controls the Global Data bus and decodes many of the devices that use its information.

MAILBOXES

The six 74HC374 octal latches (U95 through U98) are grouped in three pairs. They are best thought of as one 16 bit RAM. Notice that their D inputs and Q outputs are all tied together on the Global Data bus. The latches are written to by a low transition on their clock line. That stores the data into the latch while the Global Data bus goes on doing other things. When the latches are enabled by their OE* line, they will put their data back onto the bus.

These Mailboxes are used to transfer 16 bit data from PEL to PEL and from the Brain to the PELs as well as from the PELs to the Brain. They are clocked by the outputs of U92 which is an address decoder for the Global Address bus. The Mailboxes are enabled in the same way by U91.

COMMON IO DECODE

U91, U92 and U93 are the address decoders for the Global Address bus. U93 decodes the addresses for read operations. The 3- line-to-1-of-8-line decoder uses the GA0, GA1 and GA2 lines as the inputs then GR/W, GR/W* and PEL ENABLE are used to enable the output. Here is a summary of the decoded operations.

READ ADC...Enables A to D converter data onto the bus.

READ BRAIN DATA...Sends Brain data to the Global bus.

READ BRAIN ADDRESS...Puts Brain Address and PEL select information onto the bus.

READ DELAY...Sends delayed audio data from the DRAMs to the bus.

READ STATUS...Enables the status registers (U81 and U82) data onto the bus

READ MAILBOXES...These three enable the outputs of the mailboxes.

U92 performs the write decodes in the same manner. It uses the GR/W*, WRITE STROBE and PEL ENABLE signals for its enables.

WRITE DELAY ADDRESS...Loads an address into the DRAMs

WRITE RIGHT DAC...Clocks audio data from the bus to the right D to A converter.

WRITE LEFT DAC...Clocks data to the left D to A converter.

WRITE DELAY...Writes audio data into the DRAMs.

WRITE MAILBOXES...These three lines clock data into the mailboxes.

To extend the addressing capabilities of the Global Address bus U93 is added using three Global Data lines as inputs and the WRITE STROBE and a buffered, decoded line from U92. These form additional write functions.

PEL FIRQ...This is an interrupt from the PELs to the Brain.

RESET FASTHAND...This resets the FASTHAND signal to the Brain.

WRITE FLAGS...This enables the Status Bit latches.

WRITE FSYN...This loads data to the frequency synthesizers.

WRITE DELAY PAGE...this enables extended DRAM to be added.

PEL EXPANSION CONNECTOR

J14 is a connector which contains signals for future expansion of the H3000 hardware.

BULK MEMORY

This section is where the Dynamic RAM array is located and controlled. The DRAM is used to implement an audio delay of up to 1.5 seconds in the H3000. Audio samples are stored in the 64 K word array for playback at some other time.

MEMORY ADDRESS REGISTER/COUNTER

The DRAMs have a multiplexed address scheme. Only 8 address lines are able to address more than 64,000 memory locations per internal array (these DRAMs have 4 arrays hence 64 K by 4). Therefore, a rather complex multiplexing circuit is needed.

The PELs are responsible for calculating the addresses for the DRAMs. The address is put on the Global Data bus as a 16 bit word. When WRITE DELAY ADDRESS goes low, the word is written into the D inputs of the counters (U140, U141, U142 and U143) and appears at their Q outputs. This number is then sent to the 2 to 1 multiplexors (U146 and U147). The SEL line of the 74LS257 chips chooses the first 8 bits and on the falling edge of the RAS signal DAB0 through DAB7 is loaded into the DRAMs as the Row Address. RAS is slightly delayed by U208 and this changes the SEL line in order to load the Column Address into the DRAMs. When the DAB bus has changed the CAS signal loads the second 8 bit word. At that point WE* for the DRAMs writes or reads data to or from the chips using the DO bus. The addresses can be decremented by only a clock pulse from U203, pin 3.

DELAY MEMORY

U150, U151, U152 and U153 are used as a 16 bit memory array. Each chip is responsible for 4 bits of data. The I/O lines of the DRAMs handle data input and output. The 8 bit, DAB bus is common to all four DRAMs as are all of the control signals. OE* is the output enable line, WE* is the read (when high), write (when low) line. RAS* is the row address strobe line and CAS* is the column address strobe line.

REFRESH

Dynamic RAMs will not hold their data forever. Each bit is stored on a capacitor which will discharge if not periodically refreshed. The DRAMs handle most of the refreshing internally but every row must be accessed every 4 ms in order to keep the contents valid. U144 and U145 take on the task of addressing rows to keep them refreshed.

Clk1S is inverted by U202 and sent to the clock input of U144, a 74HC4040B 12 stage, binary counter. Pins 2 through 9 are buffered by U145, a tri-state line driver. When REFRESH SELECT goes low U144's outputs are enabled. The count from U144 then becomes a row address which is sent to the DRAMs. Data is not written to or read from the Global Data bus during this operation. The row is strictly addressed to enable the DRAMs to be refreshed continually.

DELAY INPUT/OUTPUT REGISTER

U154 and U155 are the interface between the Global Data bus and the DRAMs. These two latches are used to input data from the bus. When OE* goes low, the 16 bit, audio data word is written into the DRAMs. The latches are clocked by the WRITE DELAY line (writes a word into the DRAMs).

U156 and U157 are the output latches for the delay memory. They operate the same way as the input but, are clocked by the RAS signal. The data word is written from the

delay memory to the Global Data bus when the READ DELAY line goes low (OE* of the latches).

DELAY TIMING

Proper timing for the DRAMs is achieved by U208 and U205. The Main Timing circuits create RAS* and CAS* which are then processed with SMALL ENABLE and REFRESH SELECT to control the multiplexing of the DRAM addresses.

WRITE HANDLING

CLK5 and ALT STROBE are both inverted and sent to the inputs of U204. Pin 6 of U204 is the "clear" input of the set/clear, flip-flop that is formed by the two gates of U204. WRITE DELAY is used as the "set" input. With both inputs low the output (pin 8 of U204) will remain in its last state. A high at the "set" input drives the output high. After "set" goes low again a high at "clear" will drive the output low. This is used as the data input for U206. The ALT STROBE* signal clocks this latch. Pin 9 of U206 is the WE* control pin for the DRAMs. Pin 8 of U206 controls the loading of the DRAMs from the Global Data bus by enabling U155 and U154.

FREQUENCY SYNTHESIZERS

The H3000 uses two frequency synthesizers to generate higher or lower output sample rates in order to pitch shift. One is also used for the Tape Speed Controller circuit. A description of the Left Frequency Synthesizer follows. The right is identical.**UPDATE**

NUMBER LATCH

U160 and U161 form the 12 bit FD bus which is used to latch preset numbers to the following circuits. The WRITE FSYN signal clocks the data into the latches. U160 pin 5 is used to choose which synthesizer is being written to. U222 inverts the signal for the right synth.

FD0 through FD11 are sent to U162 and U163. These 74LS174 latches are clocked by the pulse from U169 which is derived from the selection bit (pin 5 of U160). Now these 12 bits are used as inputs to three presettable, synchronous counters (U164, U165 and U166). the DA, DB, DC and DD inputs are used internally by the counters as the number to count down to zero from. CLK1 (36.68 MHz) from the Central Timing Circuits is used as the count clock. This is inverted by U200 for the left circuit and delayed by U203 for the right.

The counting begins with U164. U164 has two enable pins which are both enabled. When this counter gets to zero the RCO (Ripple Carry Output) goes high to enable U165 to begin counting. When U165 counts to zero the RCO pin goes high to enable U166 which counts to zero like the others and outputs a high on RCO which sends the output of U175

low when pin 11 goes high. U175 (pin 8) drives the data input of U176 which clocks the output, LEFT CLOCK, to the Interface To Converters section to produce an output sample rate which must be very steady for good audio quality. U175, pin 8 also provides an LD (load) pulse back to the counters to start the process over again.

UPDATE CIRCUITRY

The LD signal is sent to the U167 flip-flop and is then latched into U168 by ALT STROBE. U169 (pin 11) resets the U167 flip-flop and is gated by pin 9 to allow an update clock for U162 and U164 to occur at a time when the FD bus is stable.

BRAIN INTERFACE

This circuitry allows the brain to control the signal processing (PELs) in the H3000. It is the "glue logic" section.

READ GLOBAL

U70 and U71 allow the brain (U50, the 68A09) to read data from the Global Data bus. The two 74HC374 chips form a 16 bit register which is latched by the output of U215. This is the clock signal to the latches. It will latch data upon a high to low transition which is dependent upon the proper conditions of the signals WRITE STROBE (U260 pin 4), BRAINTIME (U216 pin 4) and GR/W (Global Read Write, U79 pin 15). The READ PEL LOW and READ PEL HIGH signals enable the data transfer from the Global bus to the Brain Data bus. Since the 68A09 has only an 8 bit data bus it must read the 16 bit Global bus one byte at a time. The READ PEL LOW signal reads the low byte (GD0 to GD7) and READ PEL HIGH reads the high byte (GD8 to GD15).

WRITE GLOBAL

This section performs the more difficult task of the Brain writing to the Global Data bus. Again, since the Brain has only an 8 bit data bus, it must write to the 16 bit Global bus in two steps. First, U72 latches the MSB to a register called MD. MD0 to MD7 are simply what will be GD8 to GD15. MD data is sent to U74 while the Brain sends the LSB to U73. The WRITE STROBE signal then enables both U73 and U74 according to the conditions of GR/W and BRAINTIME through U215. The clock signal for U72 is derived from U212. Its output is always enabled. The clock signal for U73 and U74 is controlled by the NAND logic of U212, using BA0, BRAIN STROBE and BRAIN PORT ENABLE.

INPUT ADDRESS, INPUT DATA

U75 and U76 are used to latch addresses to the PELs and to select which PEL the information goes to. U77 and U78 latch data into the selected PEL at the selected address. All of this information pertains to PEL instructions and parameter data. BA1 through BA12 are inputs to the latch; note that the TMS32010's have only 12 address lines. BP0 through BP3 are used to select a particular PEL to receive the information. The BRAIN STROBE signal (through U212) clocks the first address and PEL select data into U75 and U76, then the READ BRAIN ADDRESS signal enables them to the Global Address bus. Next, U72 latches the MSB onto the MD bus to U78 and the Brain sends the LSB to U77. The next BRAIN STROBE signal latches the data into both U77 and U78. Then the READ BRAIN DATA signal enables the data to the Global Data bus for the PELs.

GLOBAL ADDRESS

The Global Address bus consists of only three addresses which are used to control PEL functions also. U79 also latches the BRAIN R/W signal at appropriate times to create the GR/W signal. BA1, BA2 and BA3 (BA0 and BA4 are not used) are latched when the BRAIN STROBE signal, through U212, pin 6 clocks the latch. They are then enabled by BRAINTIME through U216. BRAINTIME is low while the Brain is allowed to access the Global Data bus and high while the PELs are accessing it. It is high most of the time.

STATUS FLAGS

U80 through U83 form the Status Registers, which are used for a variety of monitoring tasks in the Brain and the PELs. Status registers are one bit memories that are used to communicate between different sections of the H3000. For example, the FIRQ line at the bottom, left of the page is a flip-flop that can be set by the PELs to interrupt the Brain. When the Brain has processed the interrupt it will reset the flip-flop by pulsing the RESET PELIRQ line. U83 works in the same manner but, it is an 8 bit, addressable latch. It takes a single data bit in (in this case GD0) and sends it to the address of the three bits A0, A1 and A2, which in this case are GD10, GD11 and GD12. Now U83 can send this information to the output when WRITE FLAGS goes low. These output bits are then put on the Global Data bus through U82 to be read by the PELs. All of these bits are used in different manners by the software. A brief explanation of them follows.

U83, Q1 through Q6 are general purpose registers which the software defines and uses.

U83, Q0 is an interrupt from the PELs to the Brain.

U83, Q7 is an interrupt from the Brain to the PELs.

CLK5* is a sample sync bit. It tells the PEL which input sample is being processed, right or left.

LEFT FSYN STAT is a bit which indicates that the Left DAC has been written to.

RIGHT FSYN STAT is the same but, for the Right DAC.

DATA STAT is a bit to indicate to the Brain that the PELs have received data from U78 and U79.

ADDRESS STAT is a bit that indicates to the Brain that the PELs have received address and select information.

FASTHAND notifies the Brain that the PELs have completed some task. It is a fast way for them to communicate.

FIRQ is an interrupt from the PELs to the Brain.

RESET TO PELS is a reset for the PELs which the Brain controls in order to load instructions into the PELs.

BIOZ ENABLE is a line that locks the PELs to the sample frequency.

OUTPUT SECTION

After the A to D converter and the following signal processing, the serial data is converted to parallel data for the Burr Brown PCM53 DAC (U25). The MSB must be inverted to get 2's compliment numbers. This inverts the digital data in the process. Phase is reinverted by the following circuitry. The DAC outputs a 20V p-p stepped analog signal. A deglitcher is employed (U26A & U27) to remove junk produced during the DAC's settling time. C95 and R92 alleviate charge ejection and other transient effects that cause circuit noise and distortion. After this, U27A attenuates the signal to 9V p-p and provides the low impedance for the Murata output filter (U28).

After the 9th order lowpass filter, the signal is AC coupled by C102, C103 and applied to the SinX/X compensating circuit (U29A, R96, R97, R98, and C104 & C105) which provides a gentle boost in the high frequencies. The output of this is split and dealt to two, multiplying DACS for gain control. One MDAC (U31) sends this preemphasized, processed signal back to the A/D for "feedback" control. The other MDAC (U32) is dual which is used in a novel summing circuit which adds the processed signal and a "mix" signal from the preemphasized A/D. This "mix" signal is also peak detected for the front panel bargraph drivers by U29. The mixed output at U29, pin 7, is finally deemphasized (R101, R102, R108, C113) and fed to the output drivers U33A and U33B. R105 and R109 provide output short circuit protection, and oscillation suppression along with R106, R111, C114 and C115. The 4PDT bypass relay, K1, switches the differential output between the input and the DAC output section. The output of the H3000 appears as a processed, but noninverted signal at the output connector J6.

J5
J6
J7
J8
K1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U25
SOCKET
U26
U27
U28
U29
U31
U32
U33
SOCKET
U34
U35
SOCKET
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R70
R79
R53
R22
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Q3
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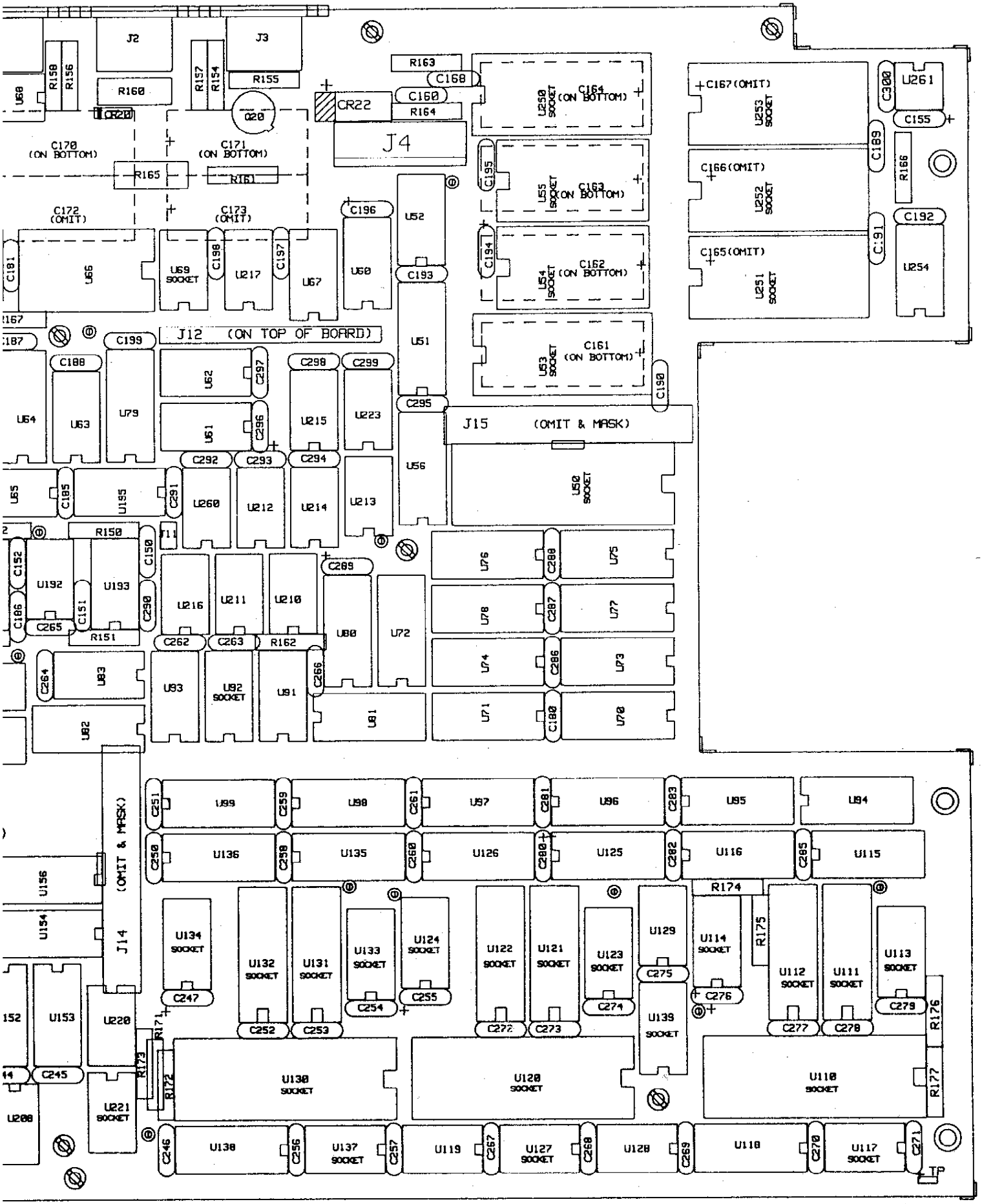

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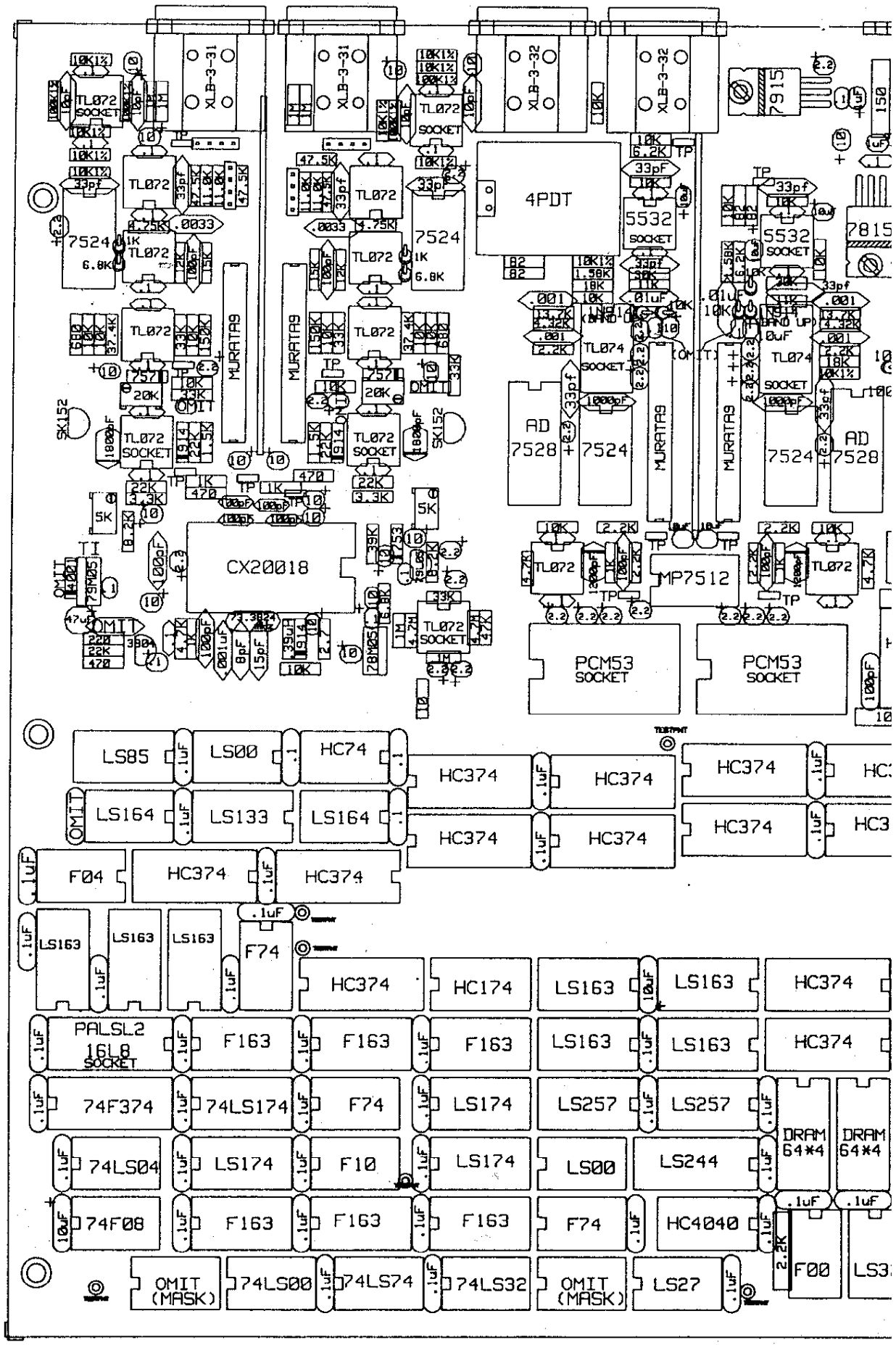
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XLR-3-32
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7528
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5532
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CX20018
MP7512
PCM53
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LS85
LS00
HC74
LS164
LS133
HC374
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LS163
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PALSL2
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F163
74F374
74LS174
LS174
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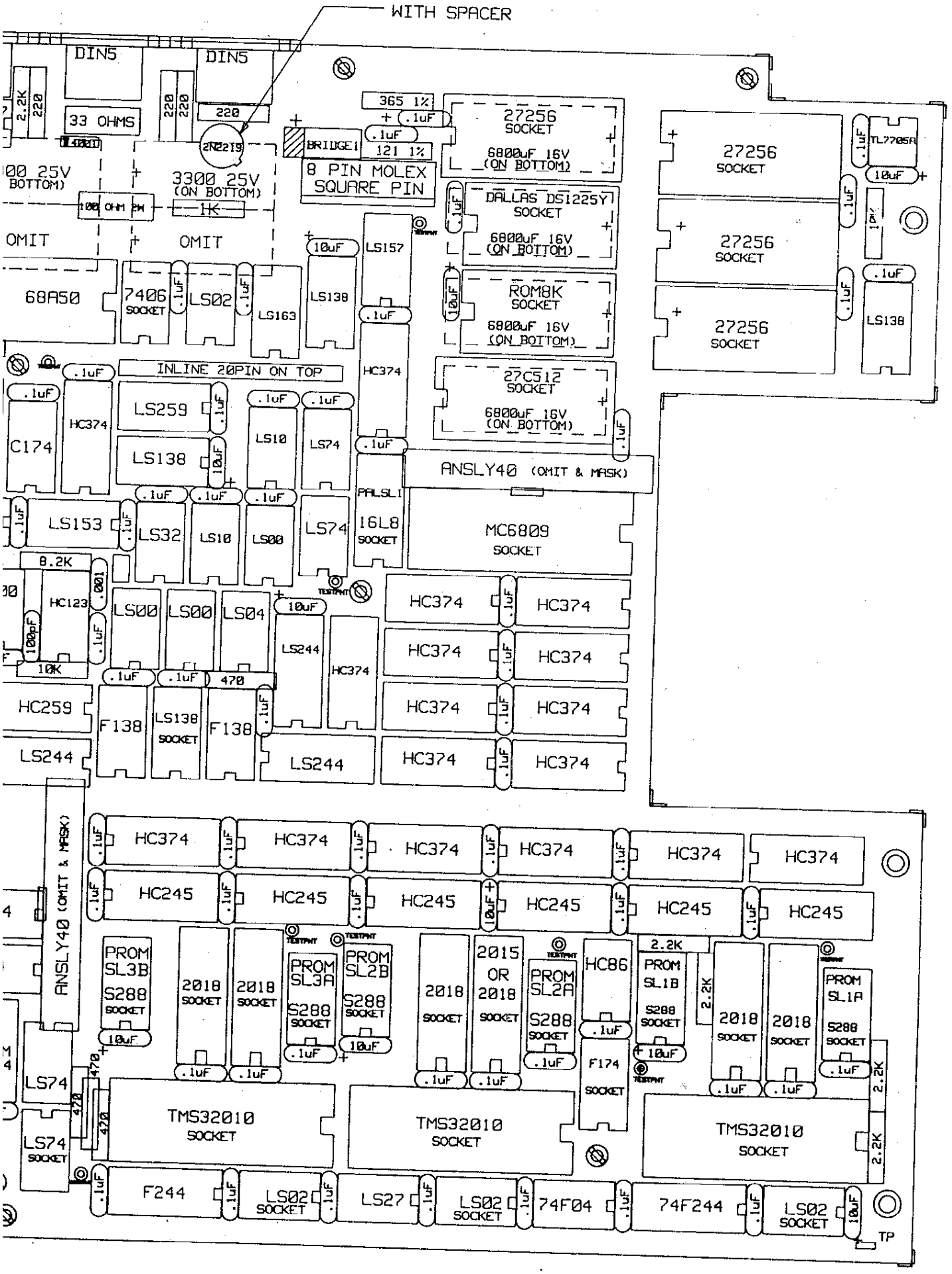
HC174



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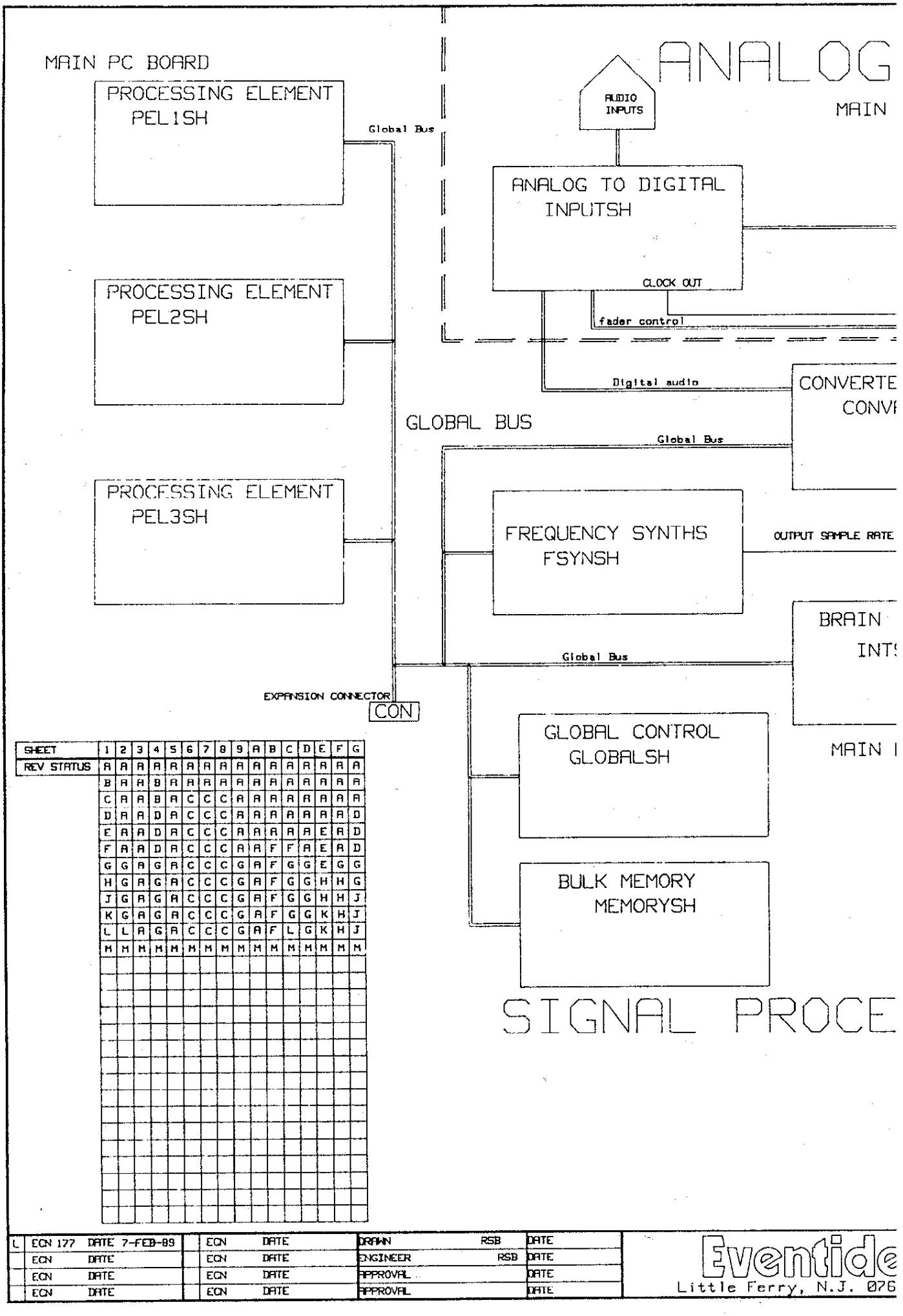

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	C	A	A	B	A	C	C	C	A	A	A	A	A	A	A	A
	D	A	A	D	A	C	C	C	A	A	A	A	A	A	A	D
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	J	G	A	G	A	C	C	C	G	A	F	G	G	H	H	J
	K	G	A	G	A	C	C	C	G	A	F	G	G	K	H	J
	L	L	A	G	A	C	C	C	G	A	F	L	G	K	H	J
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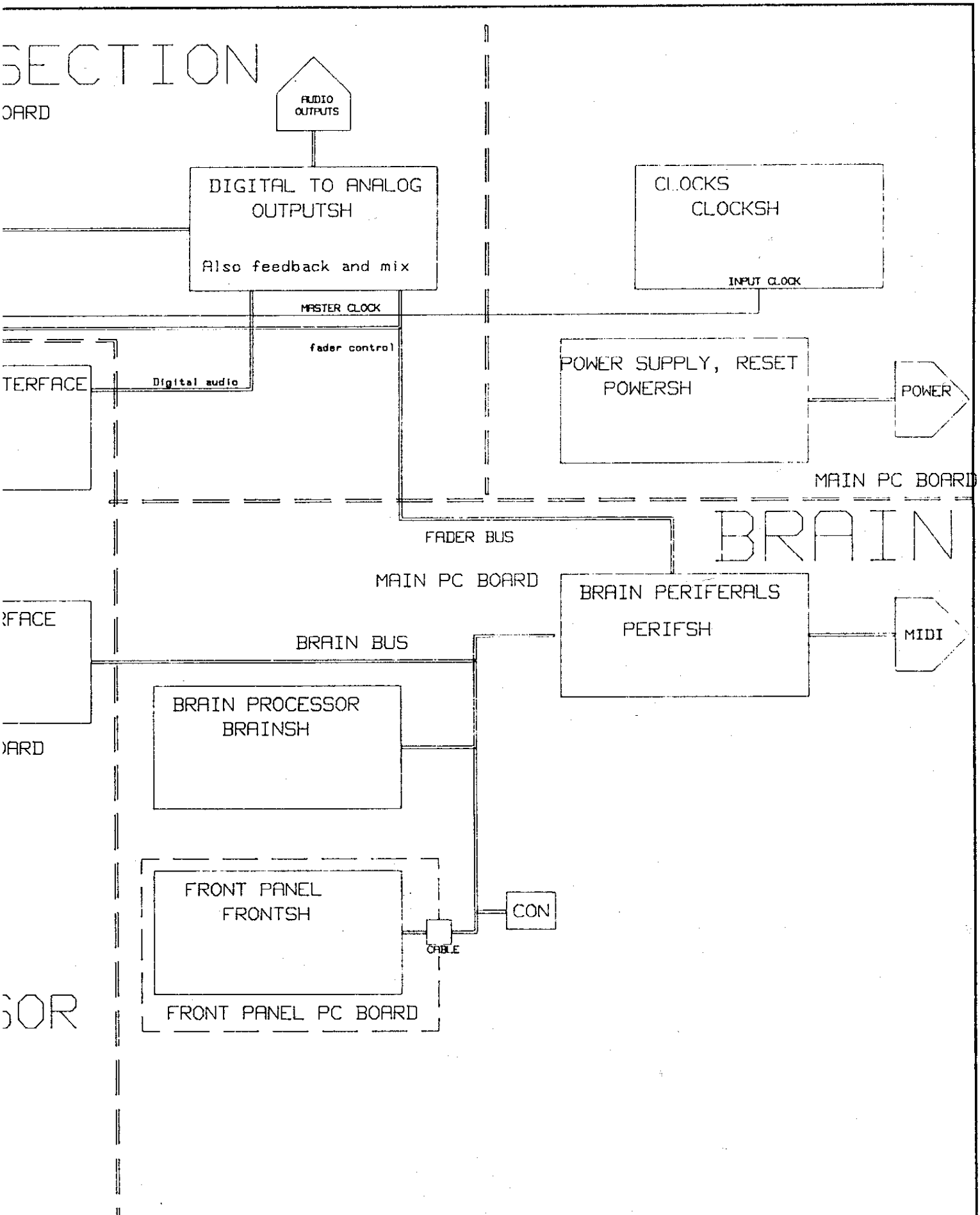
Little Ferry, N.J. 076



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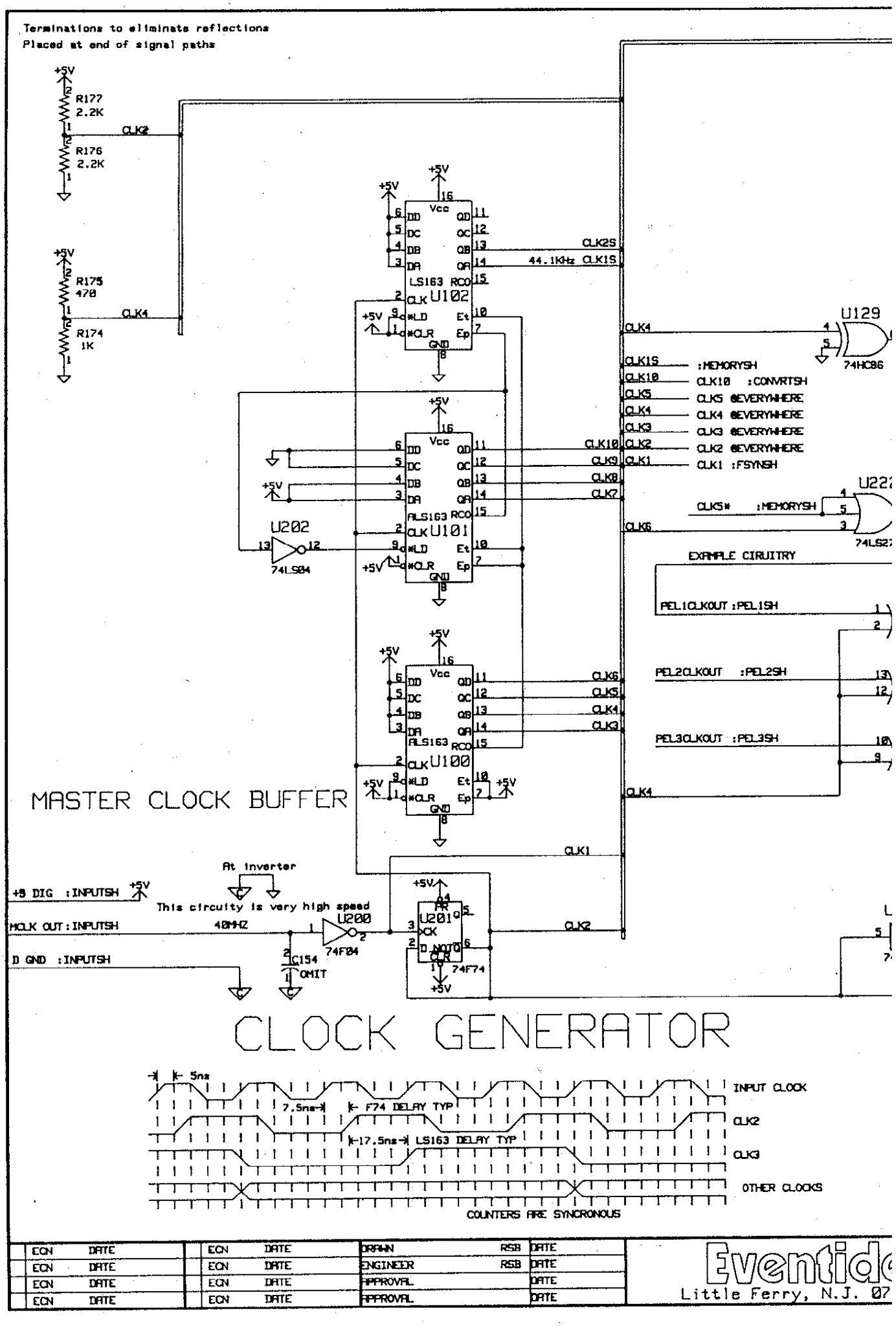
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Placed at end of signal paths
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R176 2.2K
R175 470
R174 1K
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CLK4
+5V
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U100
U202
74LS04
LS163
ALS163
Vcc
GND
*LD
*CLR
CLK2S
44.1KHz CLK1S
CLK10
CLK9
CLK8
CLK7
CLK6
CLK5
CLK4
CLK3
CLK1
U129
74HC86
CLK1S :MEMORYSH
CLK10 :CONVRTSH
CLK5 @EVERYWHERE
CLK4 @EVERYWHERE
CLK3 @EVERYWHERE
CLK2 @EVERYWHERE
CLK1 :FSYNSH
CLK5* :MEMORYSH
EXAMPLE CIRUITRY
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PEL2CLKOUT :PEL2SH
PEL3CLKOUT :PEL3SH
MASTER CLOCK BUFFER
At inverter
+5 DIG :INPUTSH
This circuitry is very high speed
MCLK OUT :INPUTSH
40MHZ
D GND :INPUTSH
U200
74F04
U201
74F74
C154
OMIT
CLOCK GENERATOR
5ns
7.5ns
F74 DELAY TYP
17.5ns
LS163 DELAY TYP
INPUT CLOCK
CLK2
CLK3
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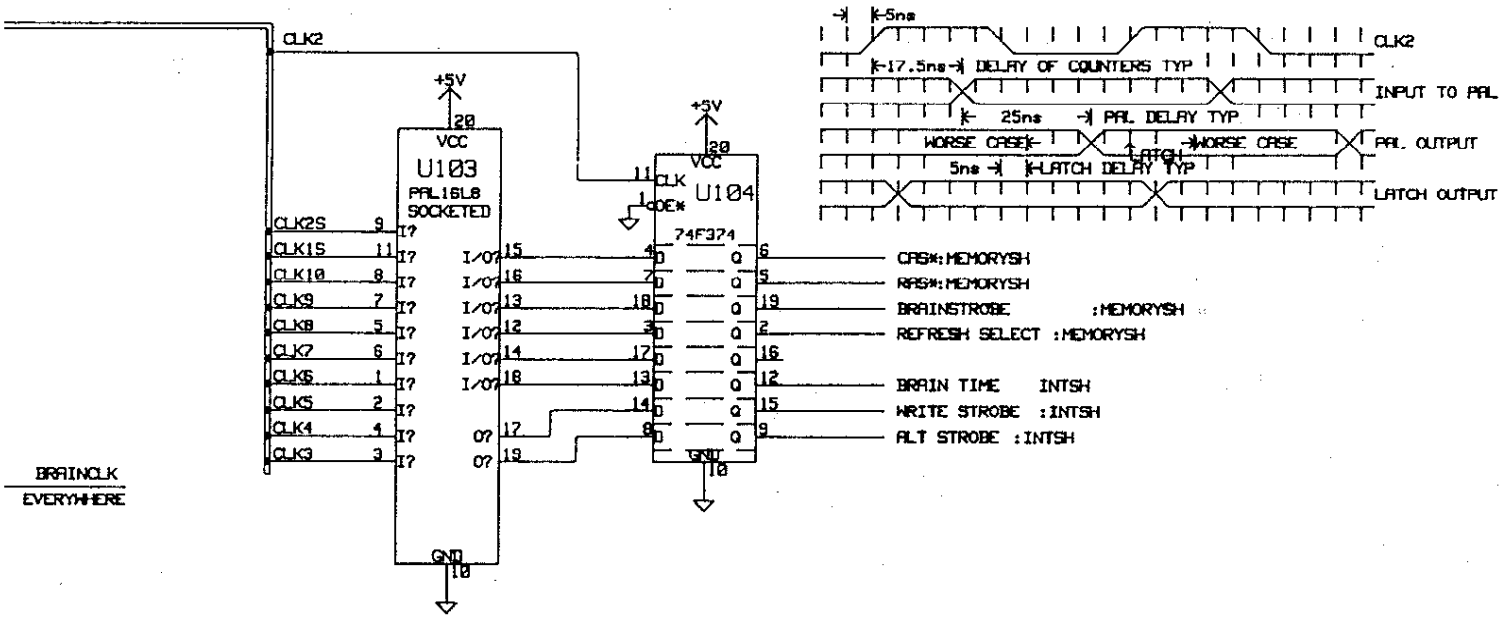

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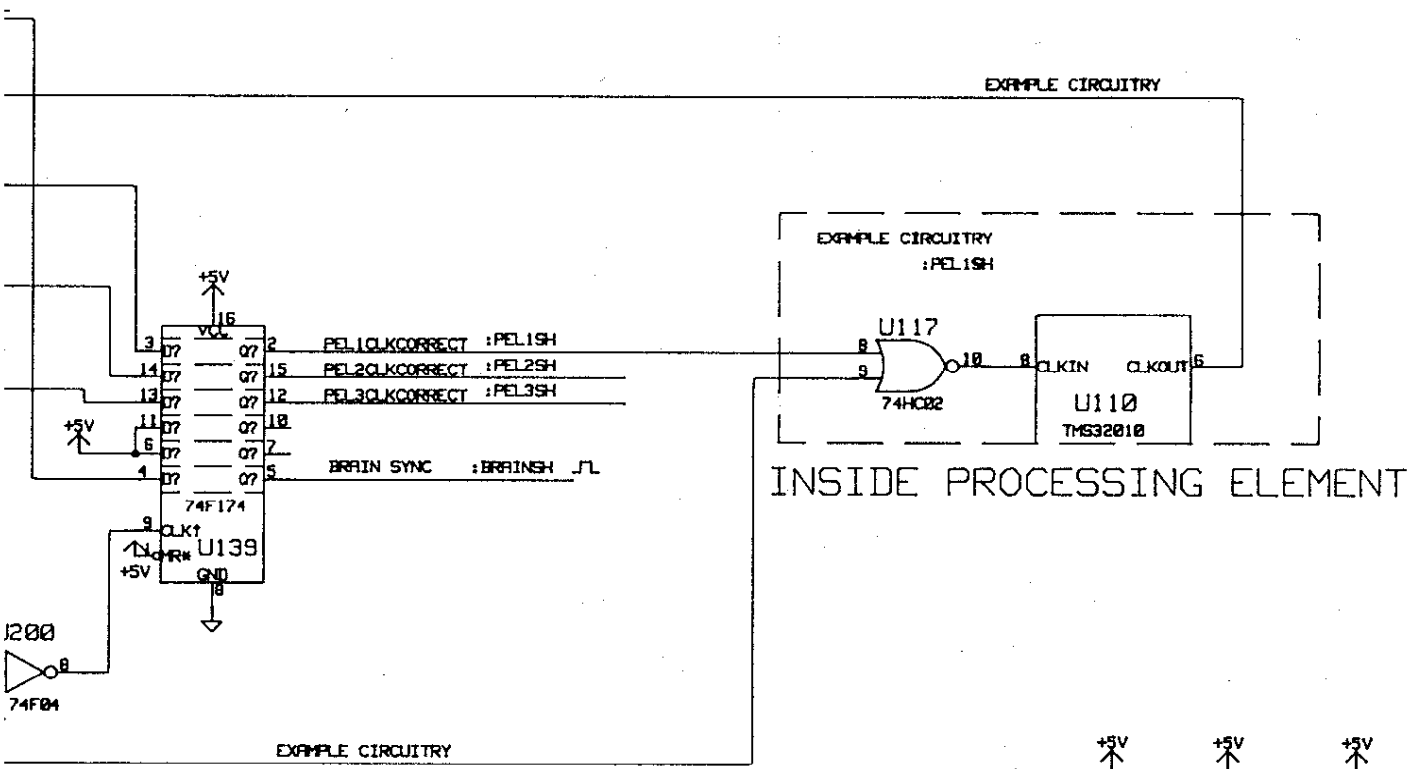
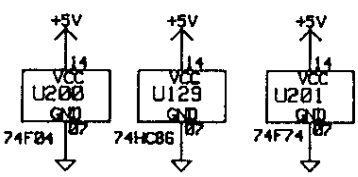
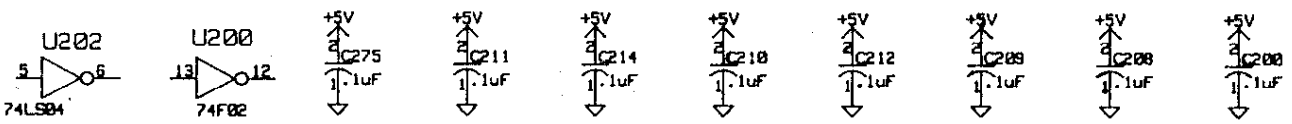
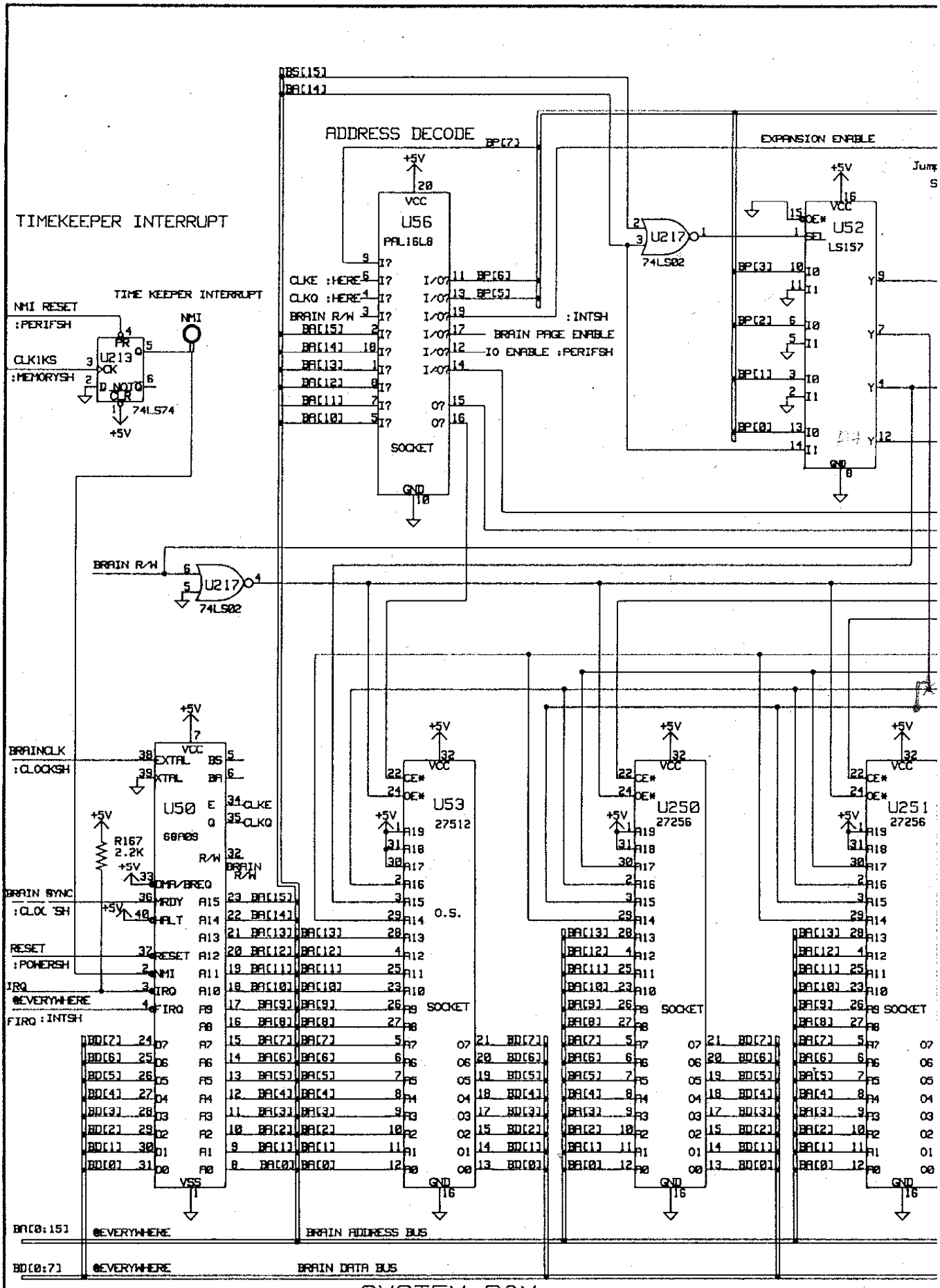


L SYNCHRONIZATION





FILENAME 10722RM	DESCRIPTION CENTRAL TIMING CIRCUITS (CLOCKSH)		DWG. No. 132072
DATE 07/19/89	DRAWING NAME H3000 SCHEMATIC	SHEET 2 OF 16	REV M

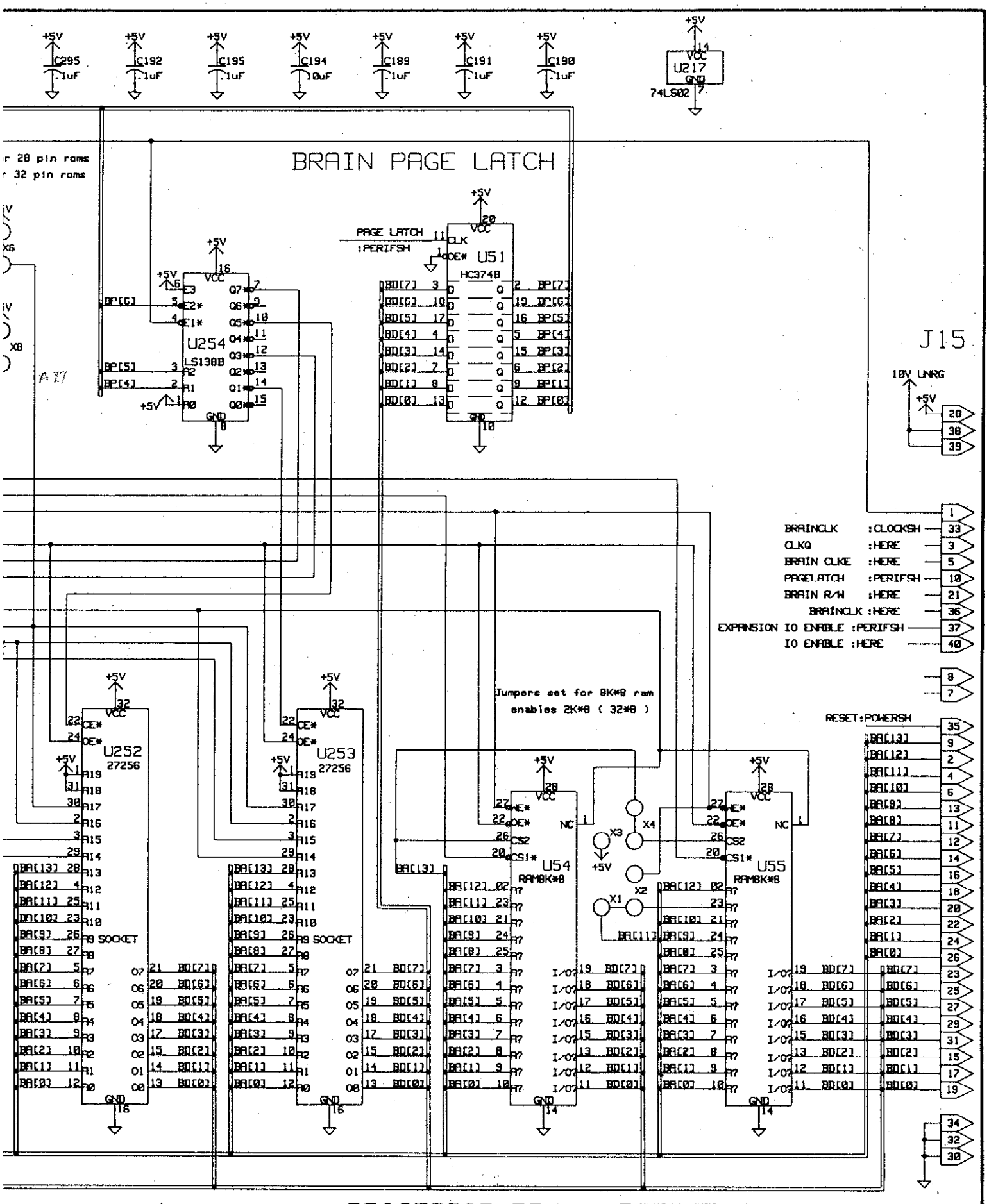


PROCESSOR SYSTEM ROM

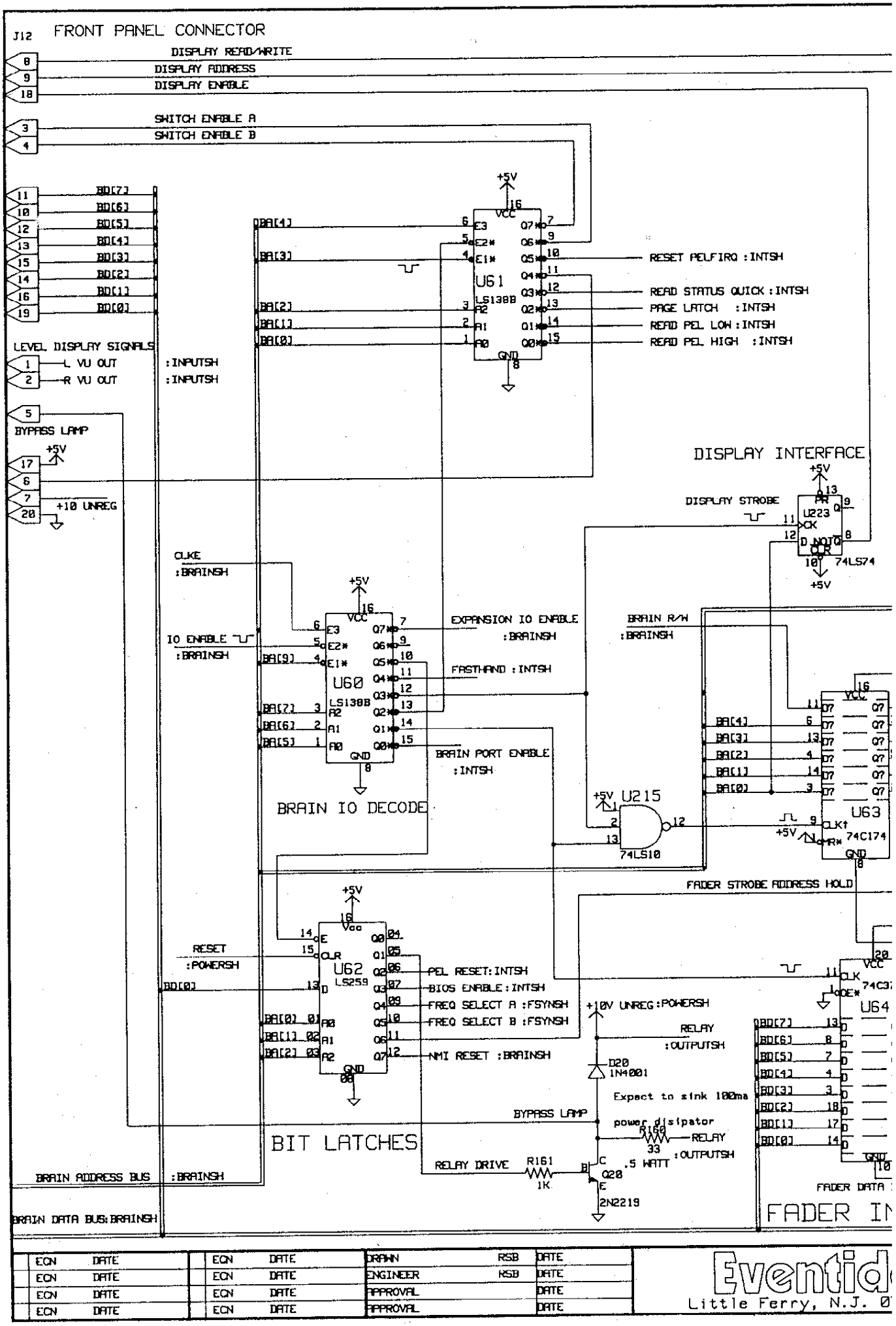
A0-A5 = 512K

	ECN	DATE		ECN	DATE	DRAWN RSB	DATE
	ECN	DATE		ECN	DATE	ENGINEER RSB	DATE
	ECN	DATE		ECN	DATE	APPROVAL	DATE
	ECN	DATE		ECN	DATE	APPROVAL	DATE

Eventide
Little Ferry, N.J. 0

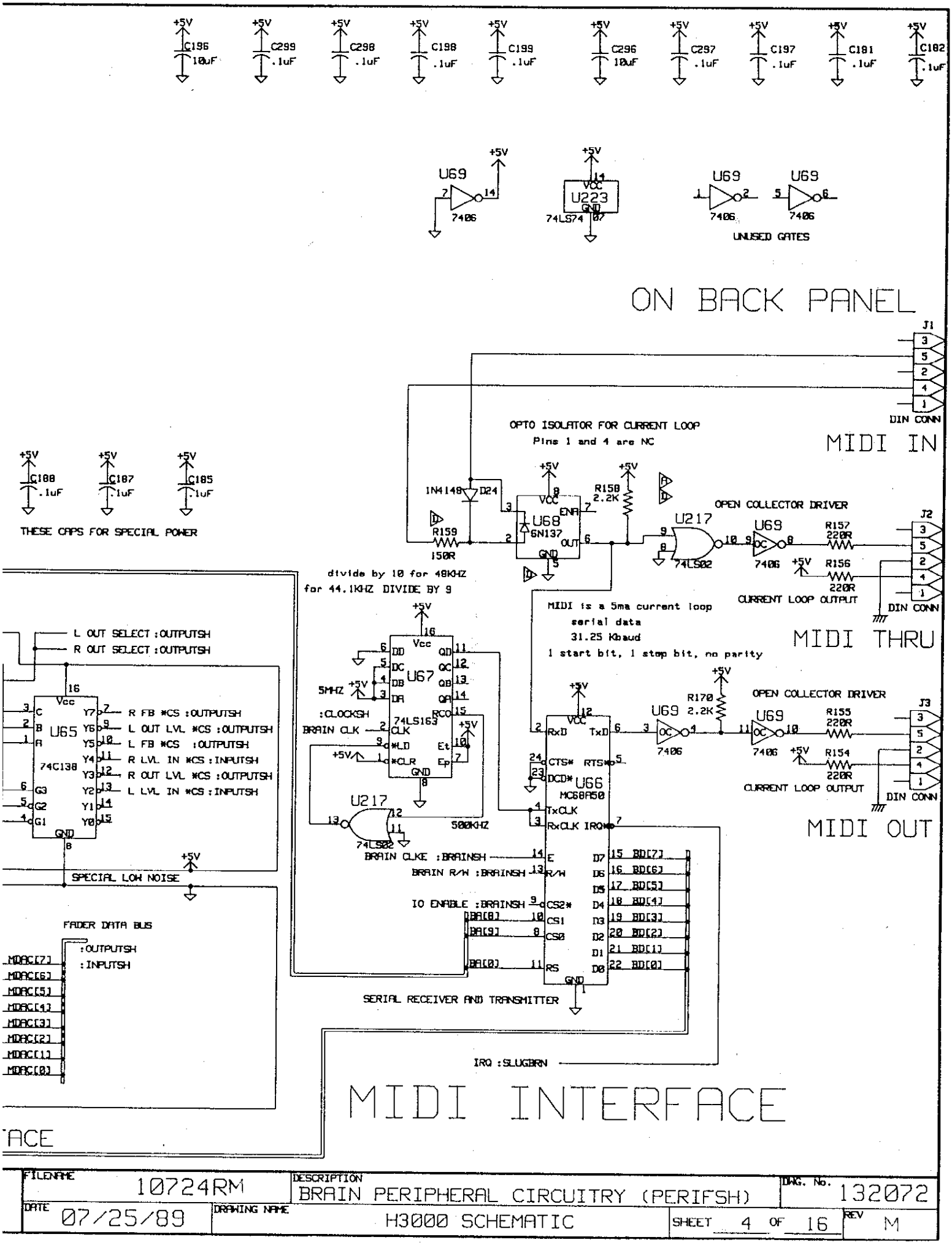


FILENAME 10723RM	DESCRIPTION BRAIN PROCESSOR (BRAINSH)		DWG. No. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 3 OF 16	REV M

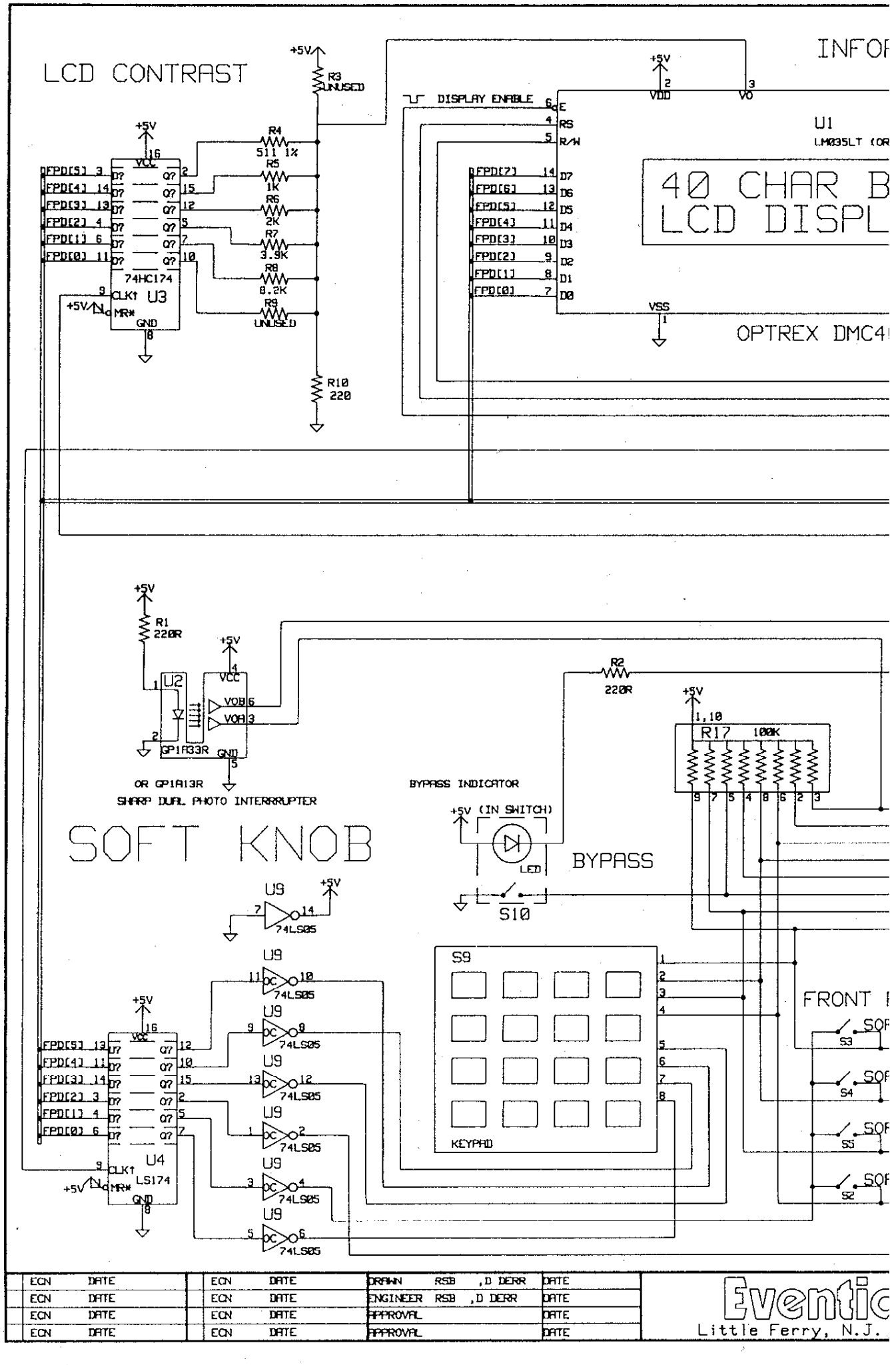


	ECN	DATE		ECN	DATE	DRAWN	RSB	DATE
	ECN	DATE		ECN	DATE	ENGINEER	RSB	DATE
	ECN	DATE		ECN	DATE	APPROVAL		DATE
	ECN	DATE		ECN	DATE	APPROVAL		DATE

Eventid
Little Ferry, N.J. 0

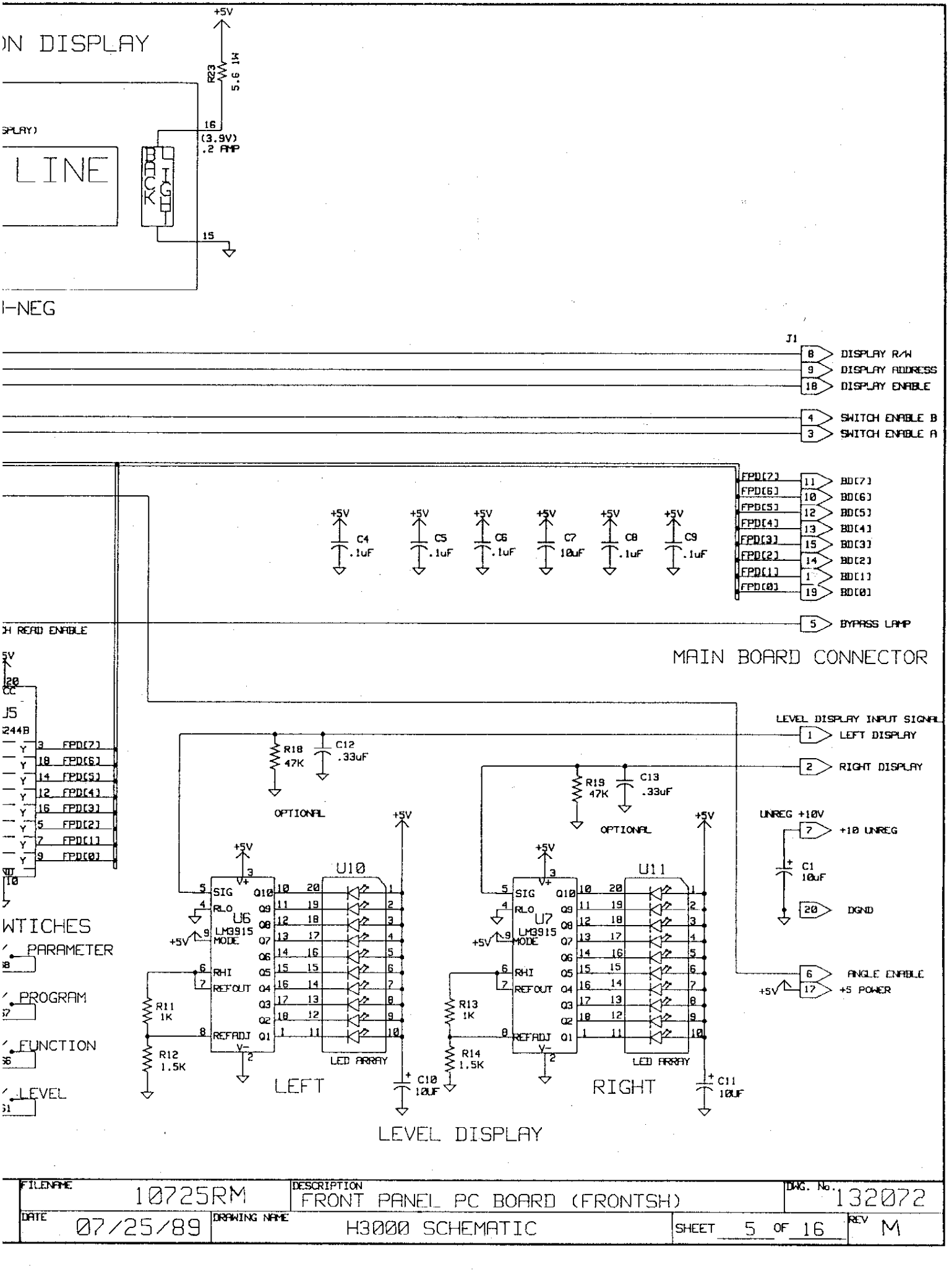


FILENAME 10724RM	DESCRIPTION BRAIN PERIPHERAL CIRCUITRY (PERIFSH)		DWG. No. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 4 OF 16	REV M

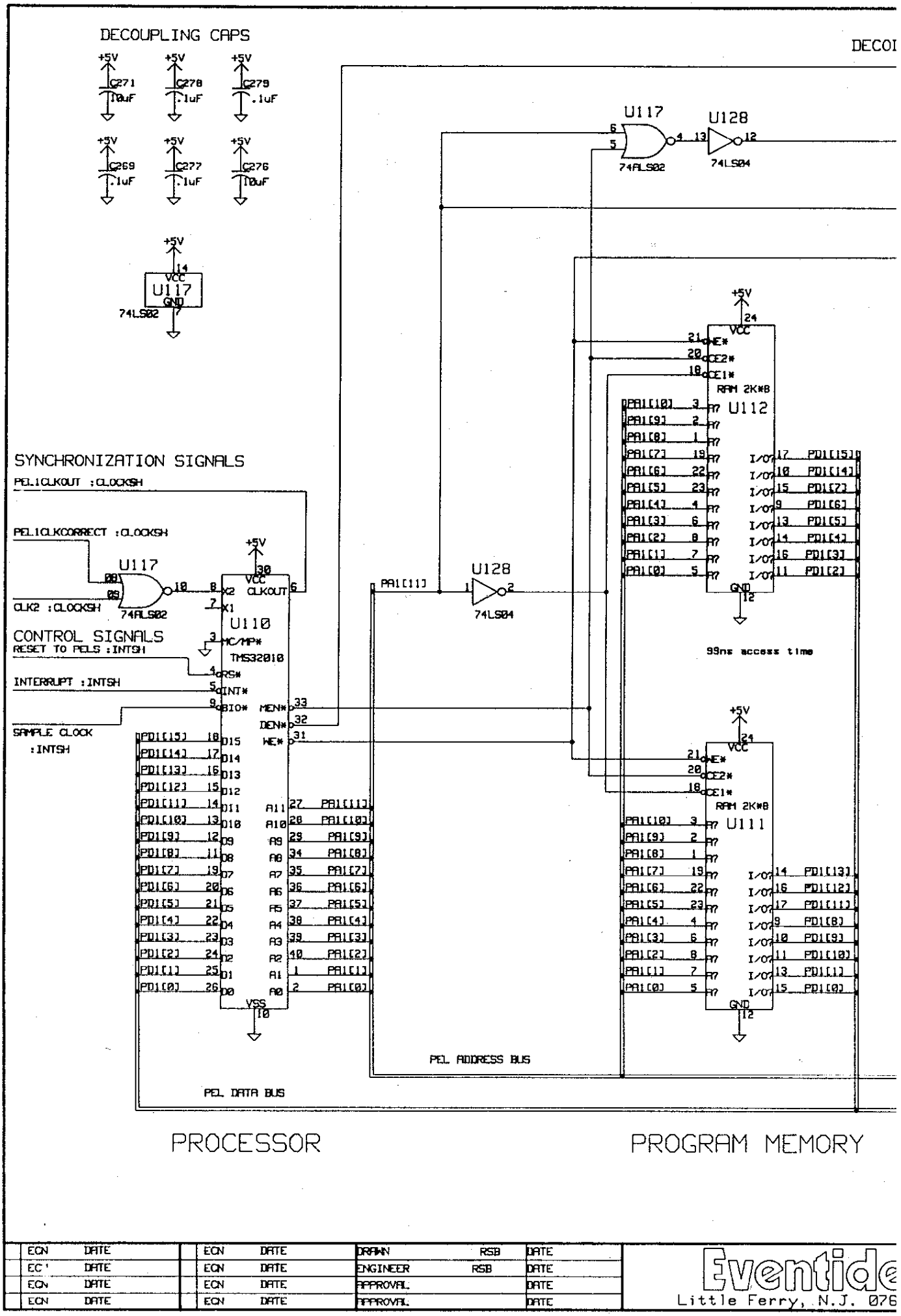


ECN	DATE	ECN	DATE	DRAWN RSB ,D DERR	DATE
ECN	DATE	ECN	DATE	ENGINEER RSB ,D DERR	DATE
ECN	DATE	ECN	DATE	APPROVAL	DATE
ECN	DATE	ECN	DATE	APPROVAL	DATE

Eventic
Little Ferry, N.J.

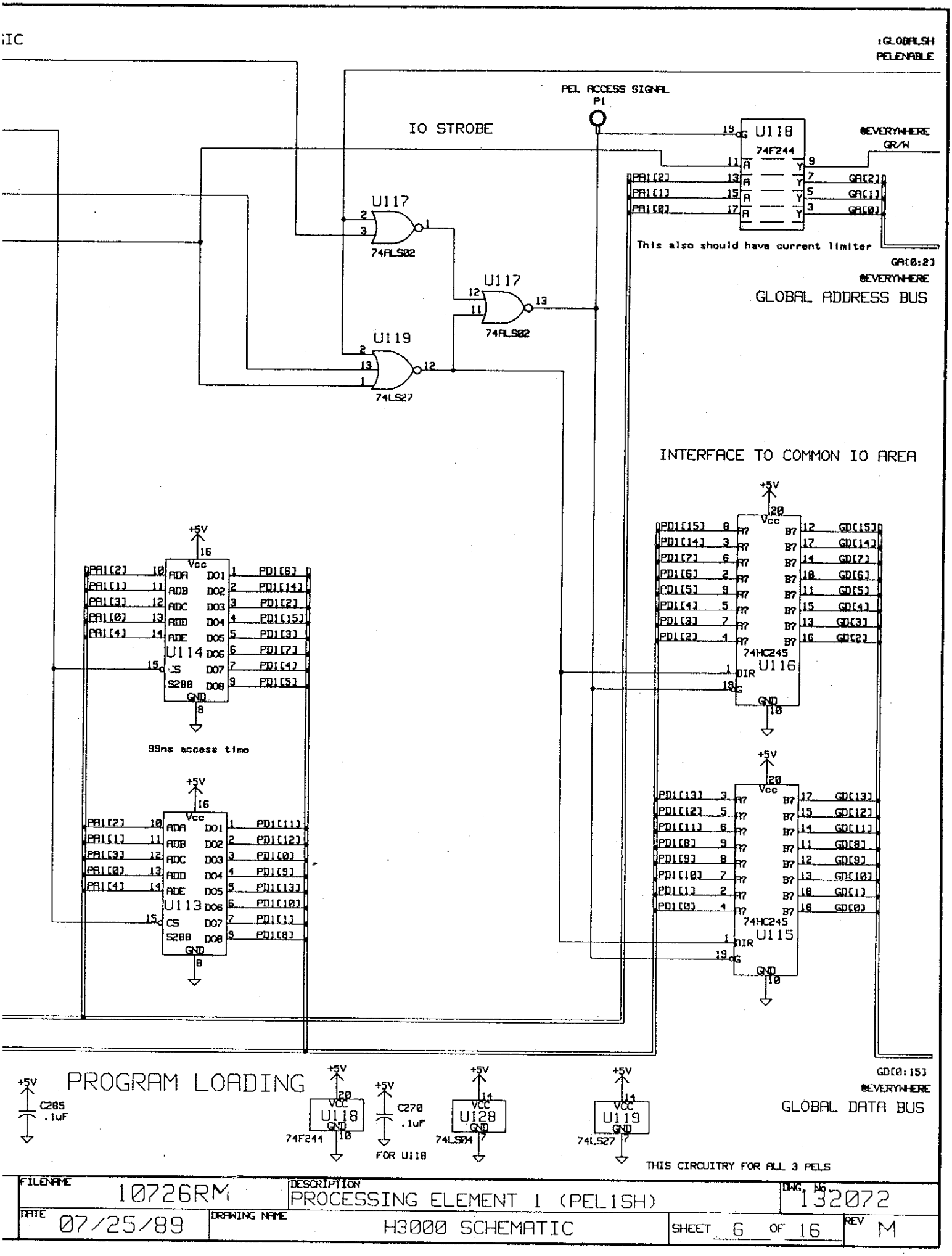


FILENAME 10725RM	DESCRIPTION FRONT PANEL PC BOARD (FRONTSH)		DWG. No. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 5 OF 16	REV M

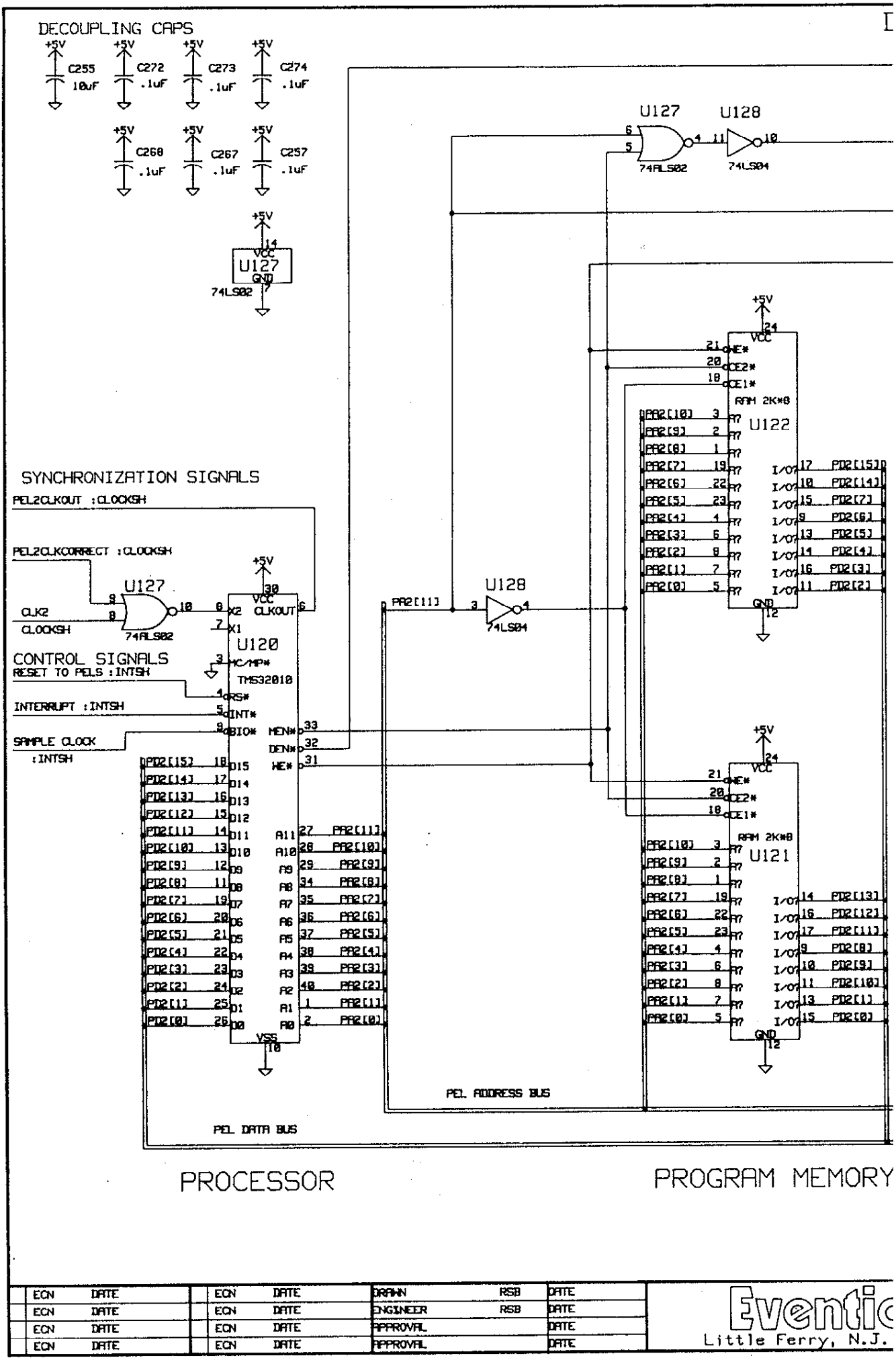


	ECN	DATE		ECN	DATE	DRAWN	RSB	DATE
	ECN	DATE		ECN	DATE	ENGINEER	RSB	DATE
	ECN	DATE		ECN	DATE	APPROVAL		DATE
	ECN	DATE		ECN	DATE	APPROVAL		DATE

Eventide
Little Ferry, N.J. 076

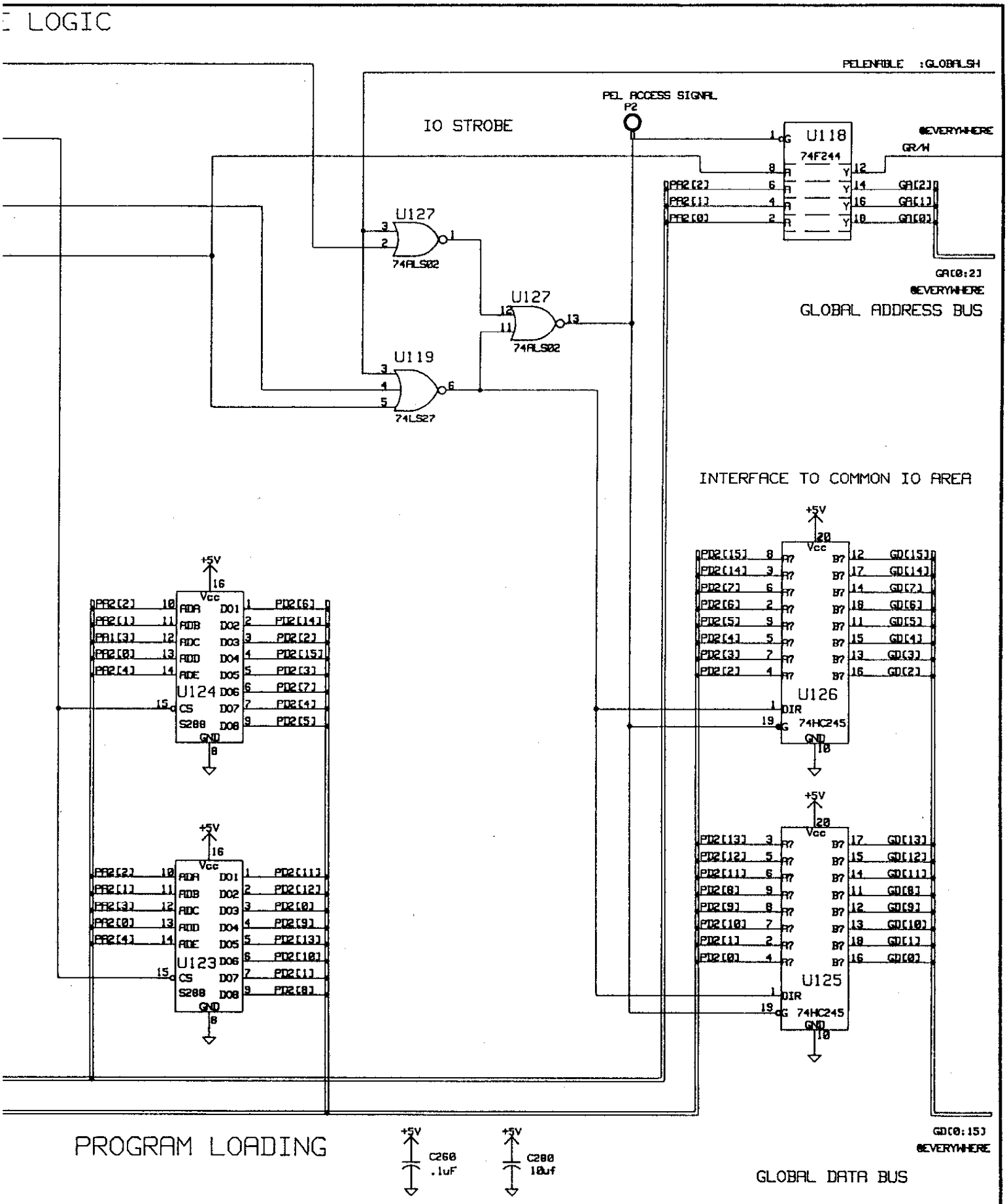


FILENAME 10726RM	DESCRIPTION PROCESSING ELEMENT 1 (PELISH)		DWG. No. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 6 OF 16	REV M

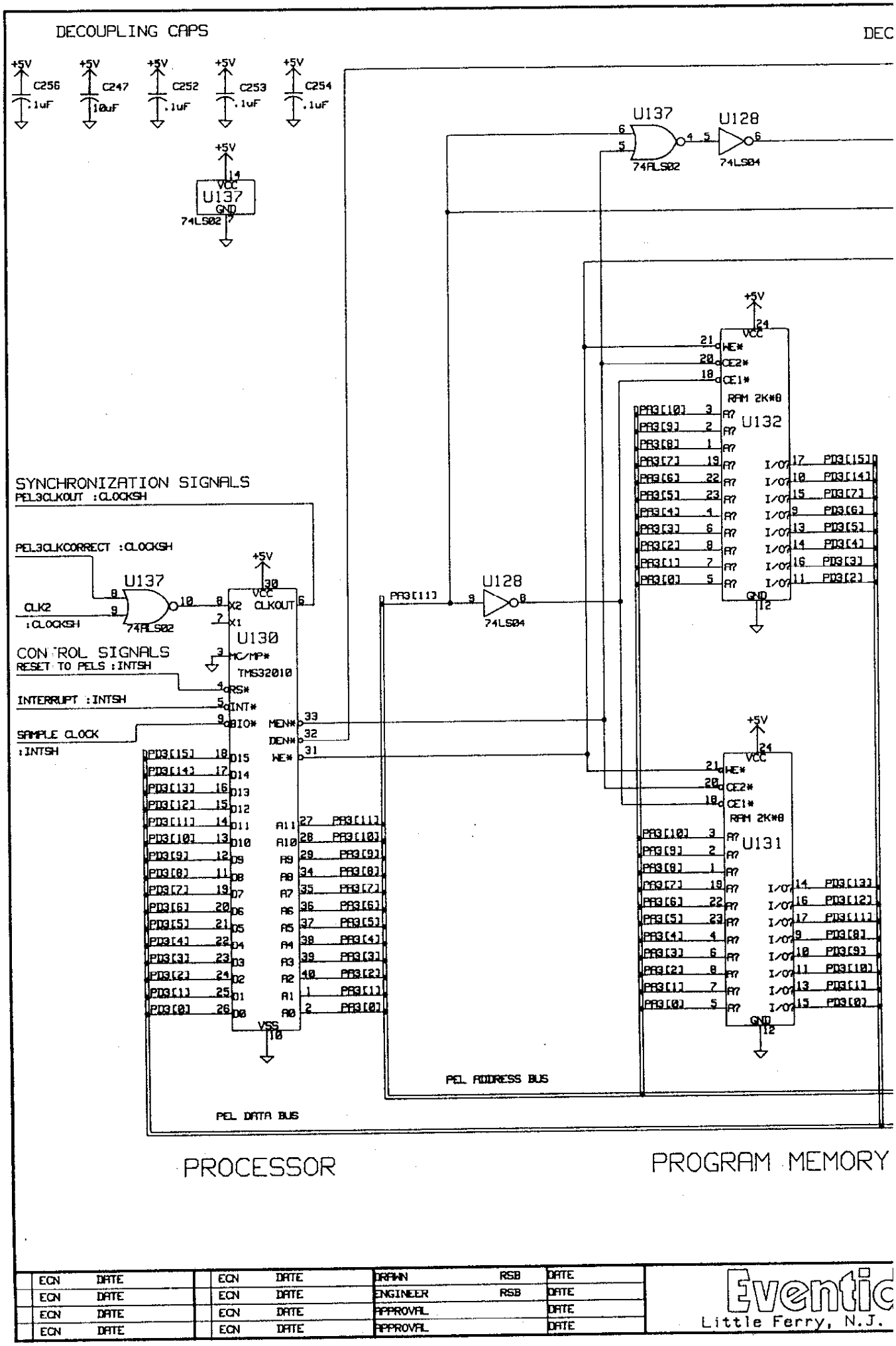


ECN	DATE	ECN	DATE	DRAWN	RSB	DATE
ECN	DATE	ECN	DATE	ENGINEER	RSB	DATE
ECN	DATE	ECN	DATE	APPROVAL		DATE
ECN	DATE	ECN	DATE	APPROVAL		DATE

Eventic
Little Ferry, N.J.

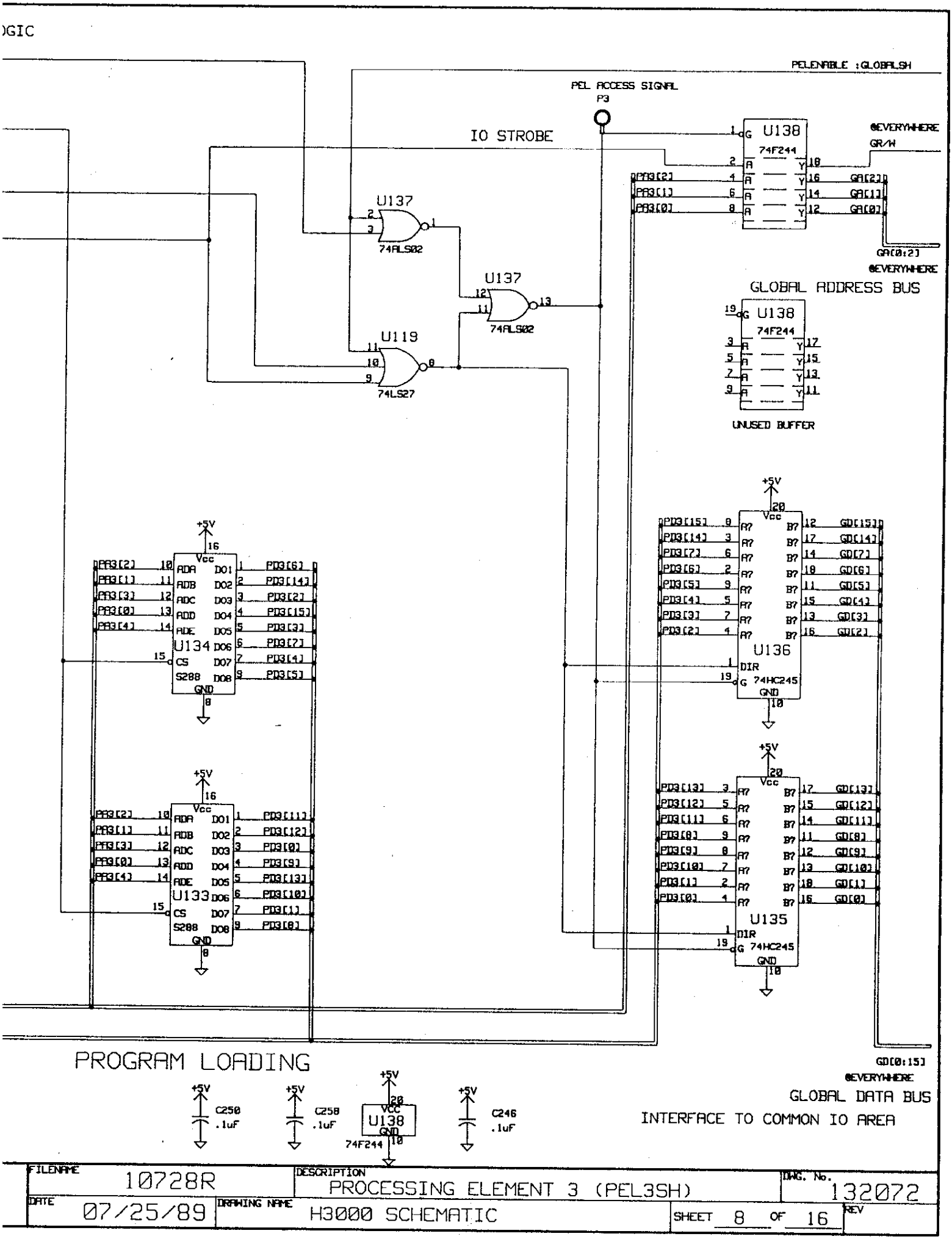


FILENAME 10727RM	DESCRIPTION PROCESSING ELEMENT 2 (PEL2SH)		DWG. NO. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 7 OF 16	REV M

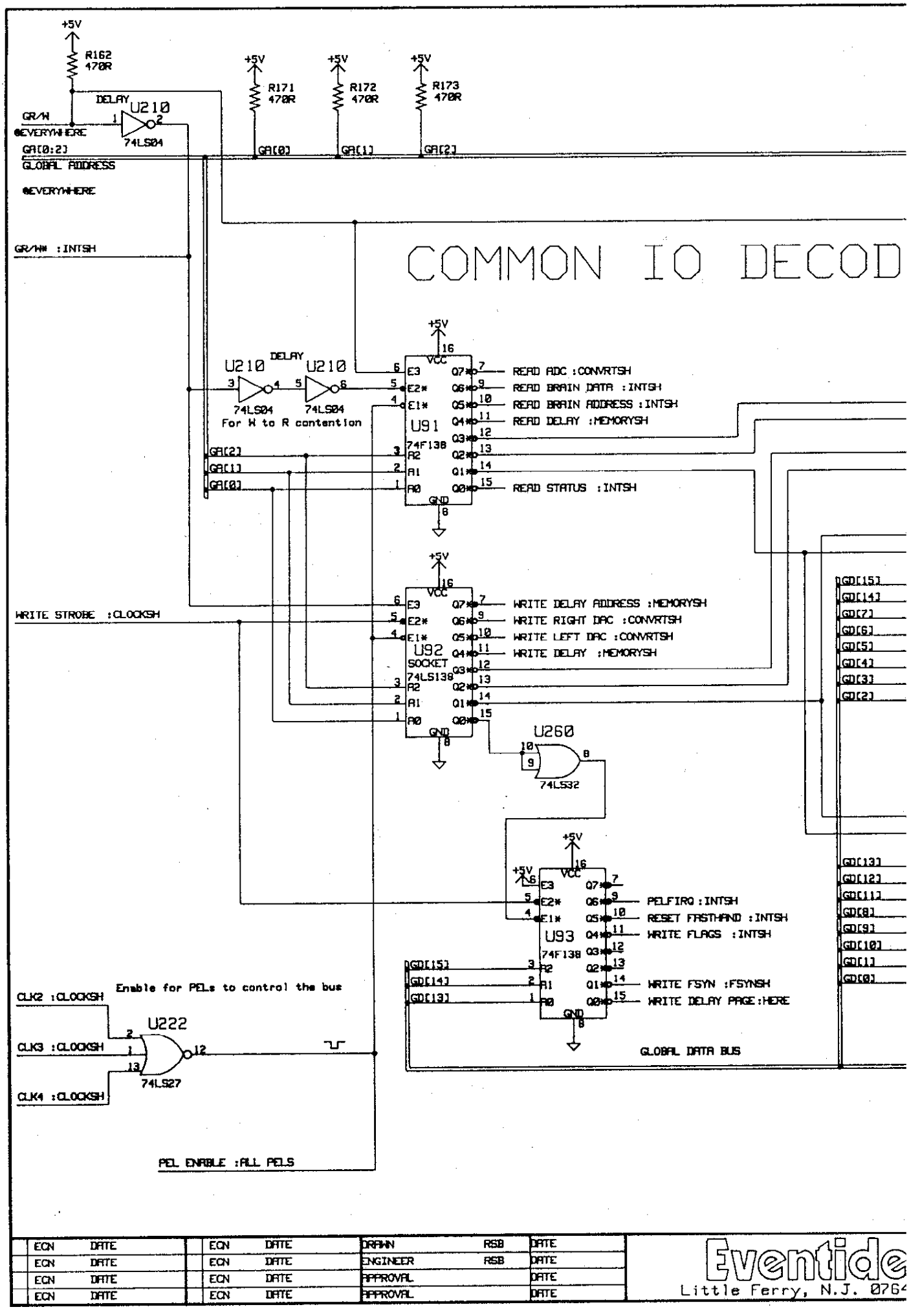


ECN	DATE	ECN	DATE	DRAWN	RSB	DATE
ECN	DATE	ECN	DATE	ENGINEER	RSB	DATE
ECN	DATE	ECN	DATE	APPROVAL		DATE
ECN	DATE	ECN	DATE	APPROVAL		DATE

Eventic
Little Ferry, N.J.

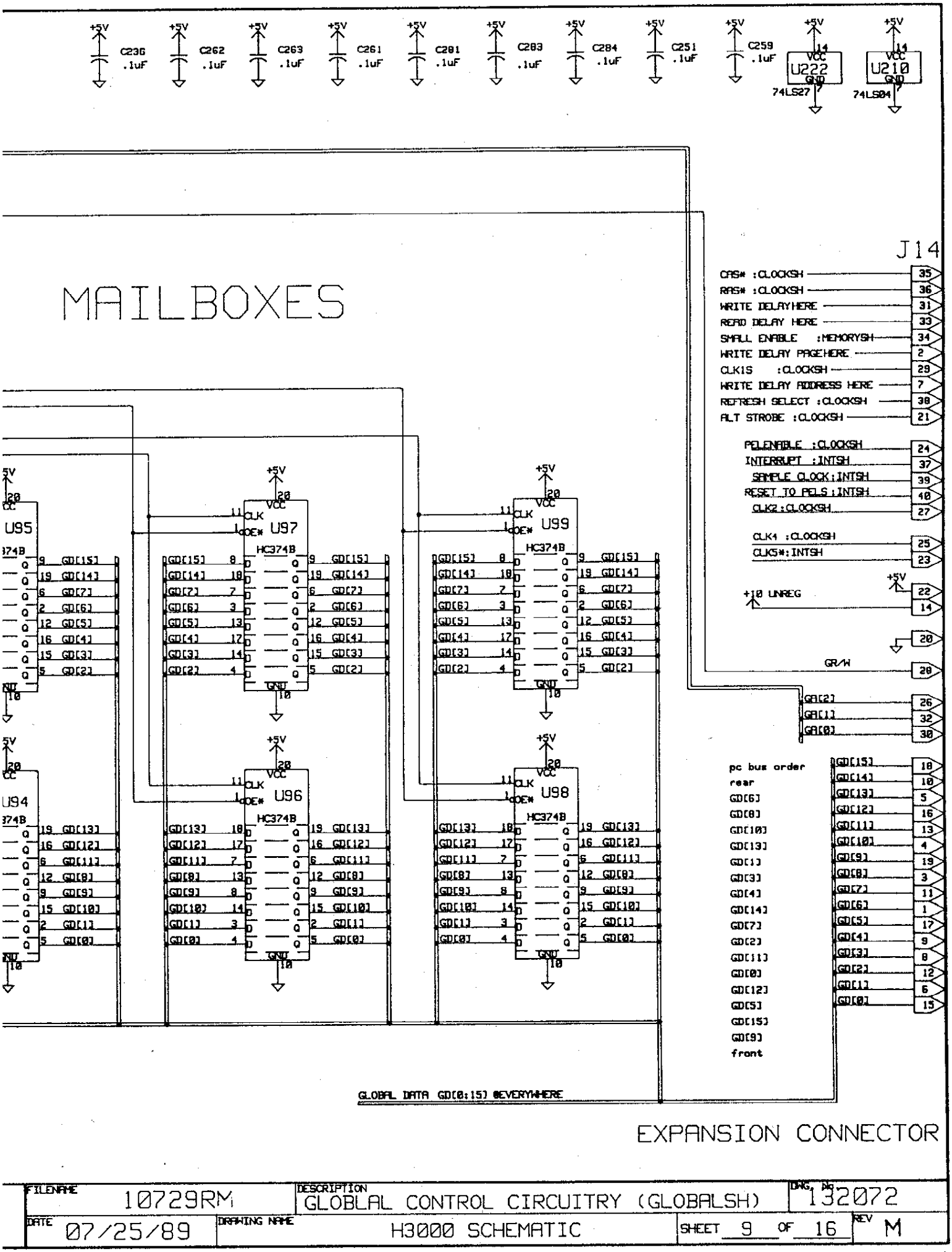


FILENAME 10728R	DESCRIPTION PROCESSING ELEMENT 3 (PEL3SH)		DWG. No. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 8 OF 16	REV

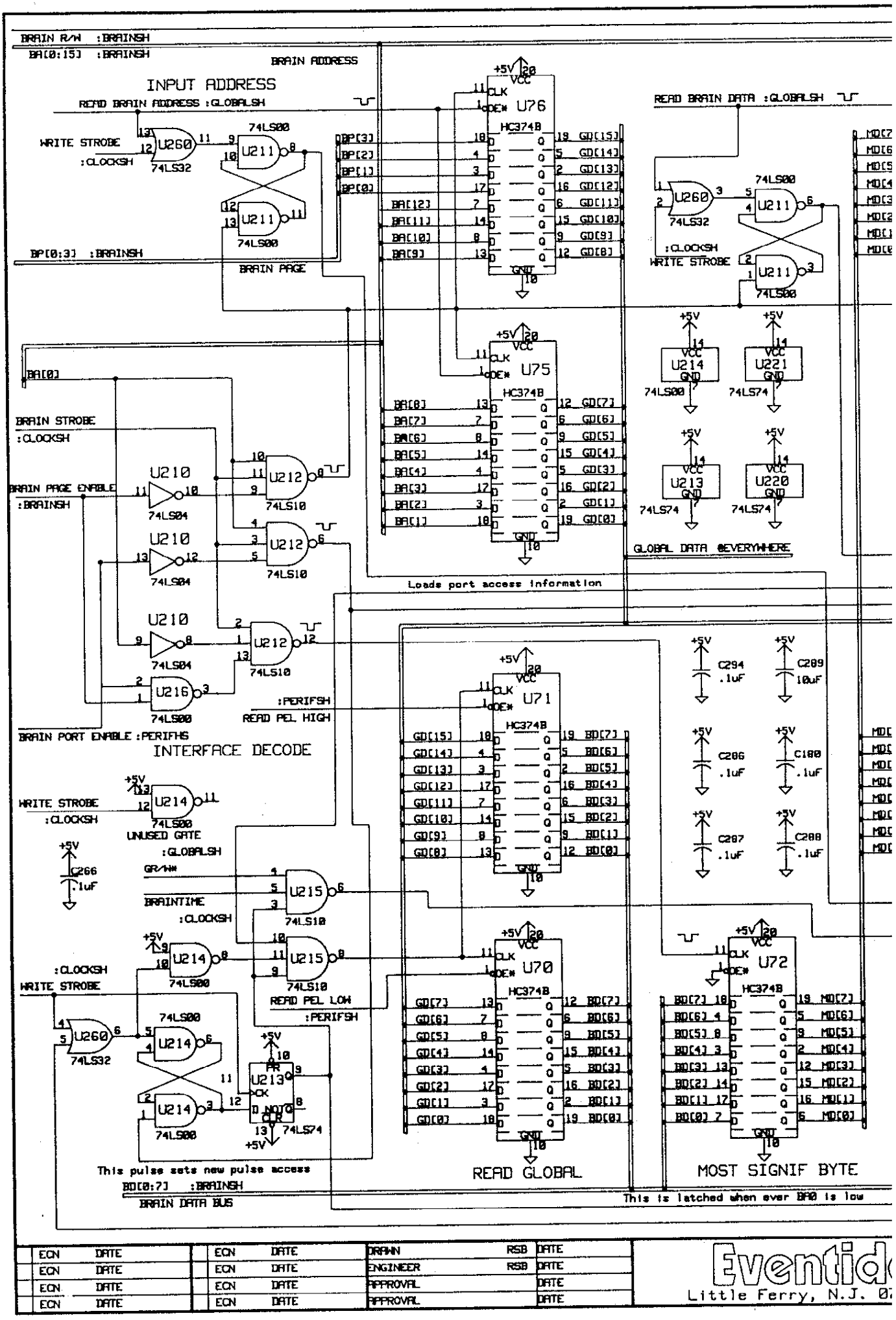


ECN	DATE	ECN	DATE	DRAWN	RSB	DATE
ECN	DATE	ECN	DATE	ENGINEER	RSB	DATE
ECN	DATE	ECN	DATE	APPROVAL		DATE
ECN	DATE	ECN	DATE	APPROVAL		DATE

Eventide
Little Ferry, N.J. 076

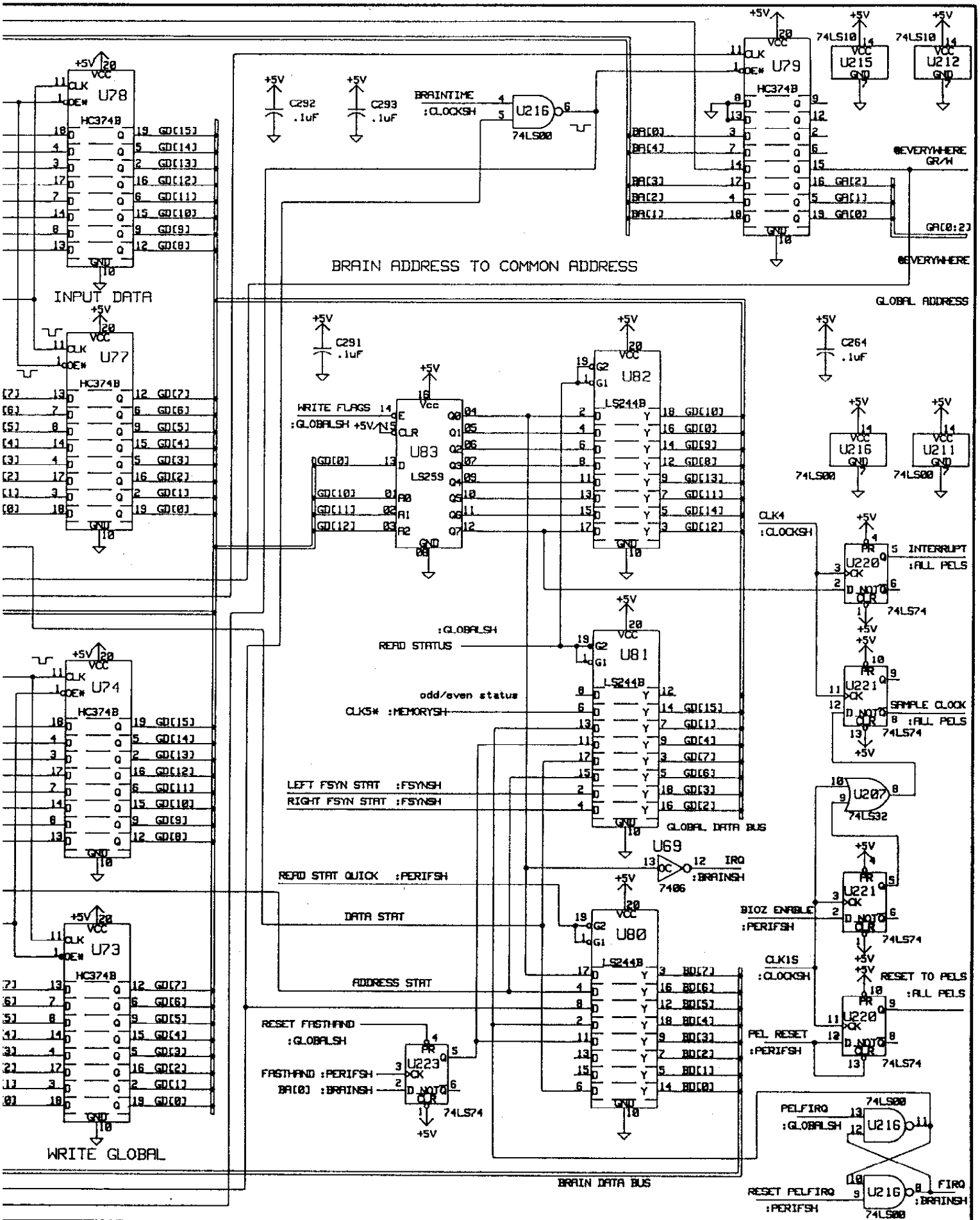


FILENAME 10729RM	DESCRIPTION GLOBLAL CONTROL CIRCUITRY (GLOBALSH)		DWG. NO. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 9 OF 16	REV M

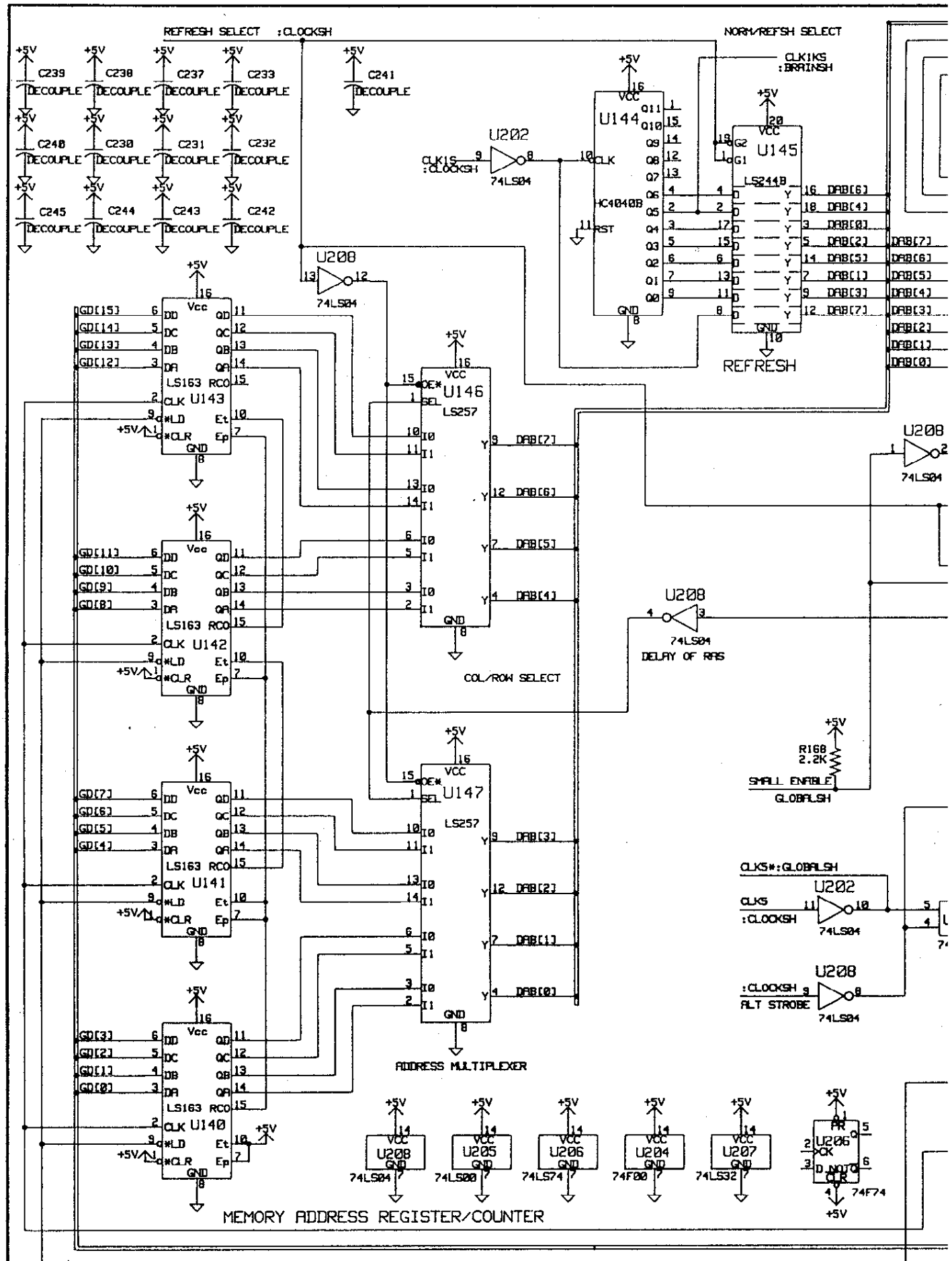


	ECN	DATE		ECN	DATE	DRAWN	RSB	DATE
	ECN	DATE		ECN	DATE	ENGINEER	RSB	DATE
	ECN	DATE		ECN	DATE	APPROVAL		DATE
	ECN	DATE		ECN	DATE	APPROVAL		DATE

Eventide
Little Ferry, N.J. 07

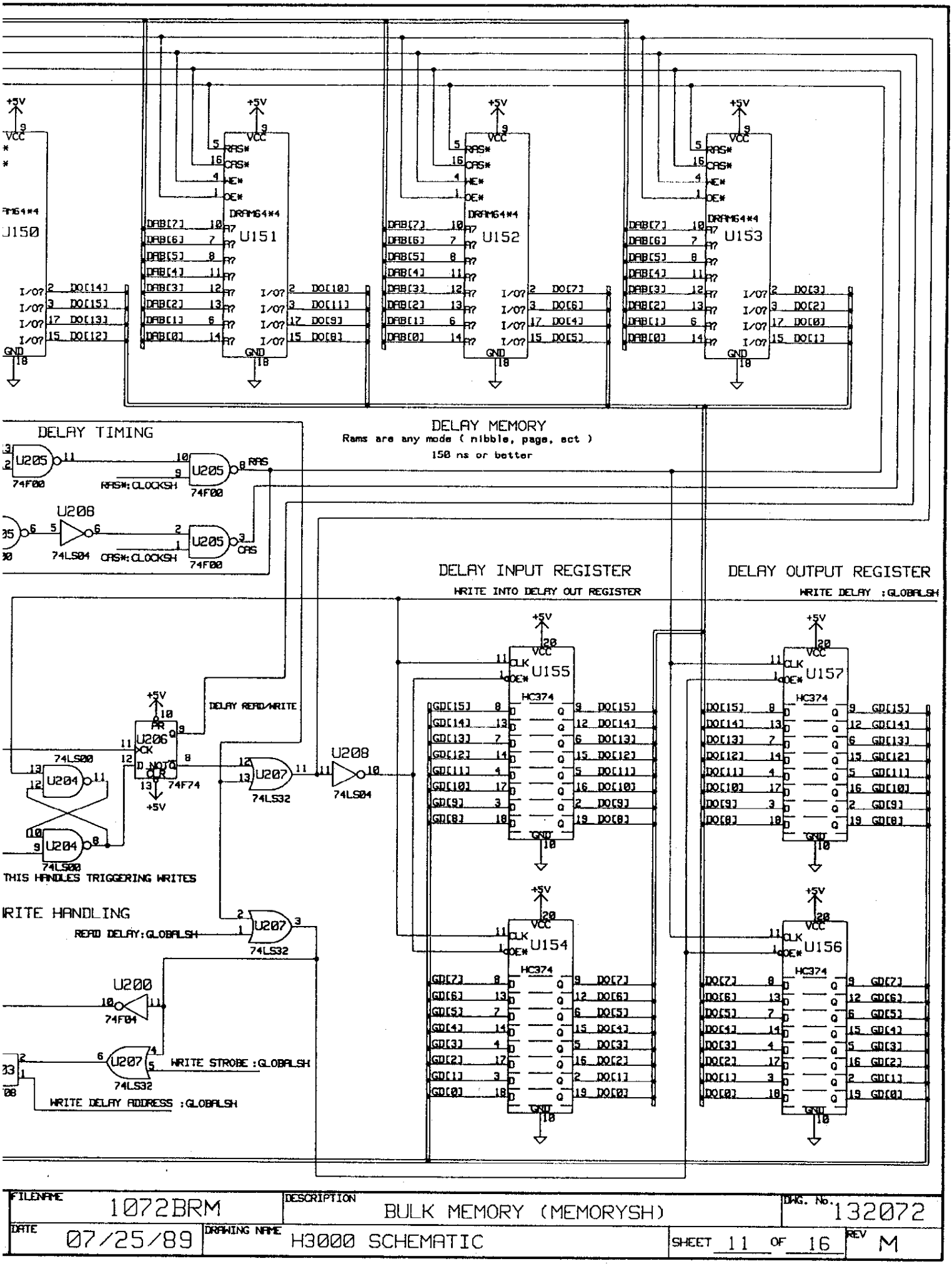


FILENAME 1072ARM	DESCRIPTION BRAIN INTERFACE (INTSH)		DWG. No. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 10 OF 16	REV M

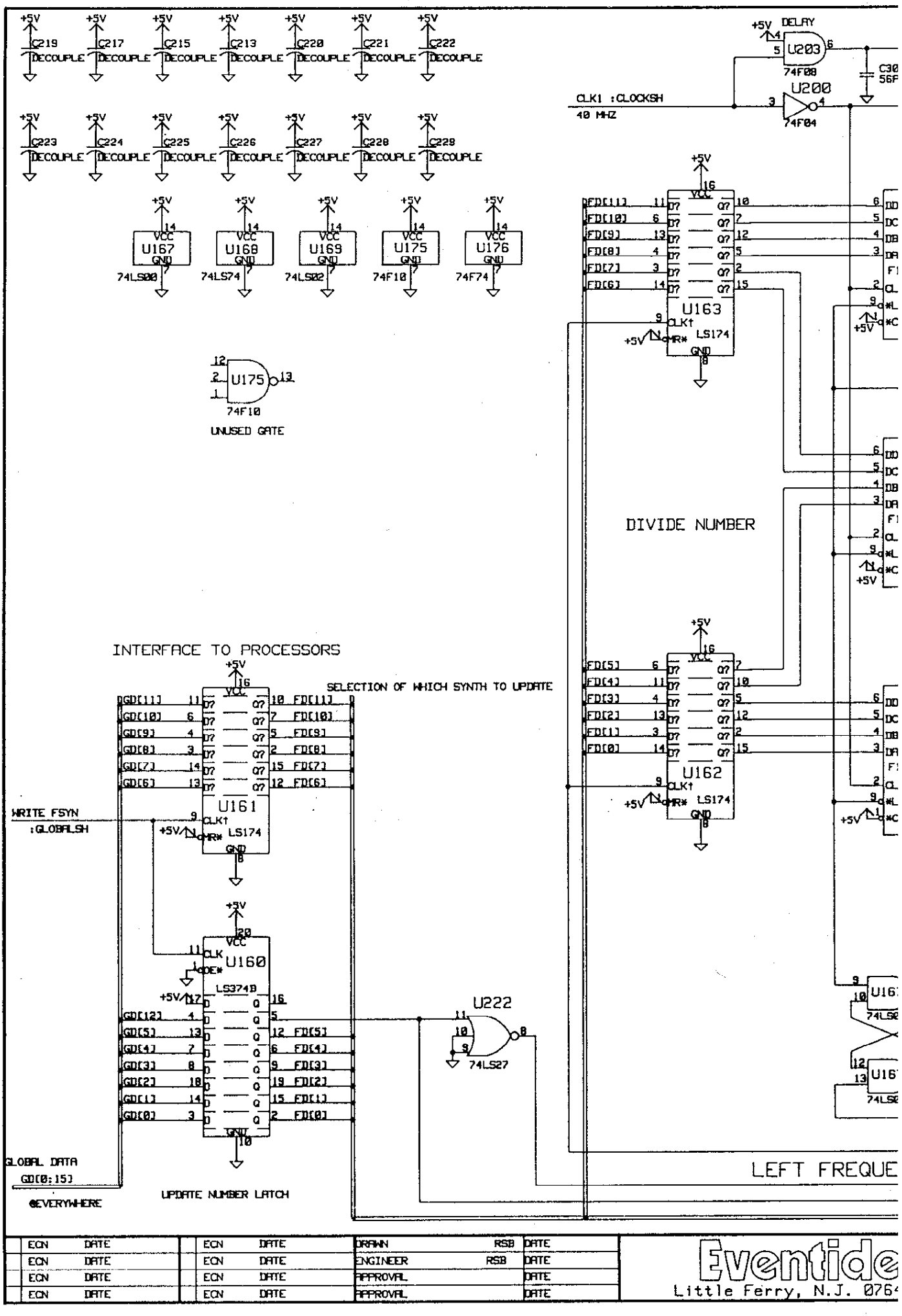


ECN	DATE	ECN	DATE	DRAWN	RSB	DATE
ECN	DATE	ECN	DATE	ENGINEER	RSB	DATE
ECN	DATE	ECN	DATE	APPROVAL		DATE
ECN	DATE	ECN	DATE	APPROVAL		DATE

Eventide
Little Ferry, N.J. 07643

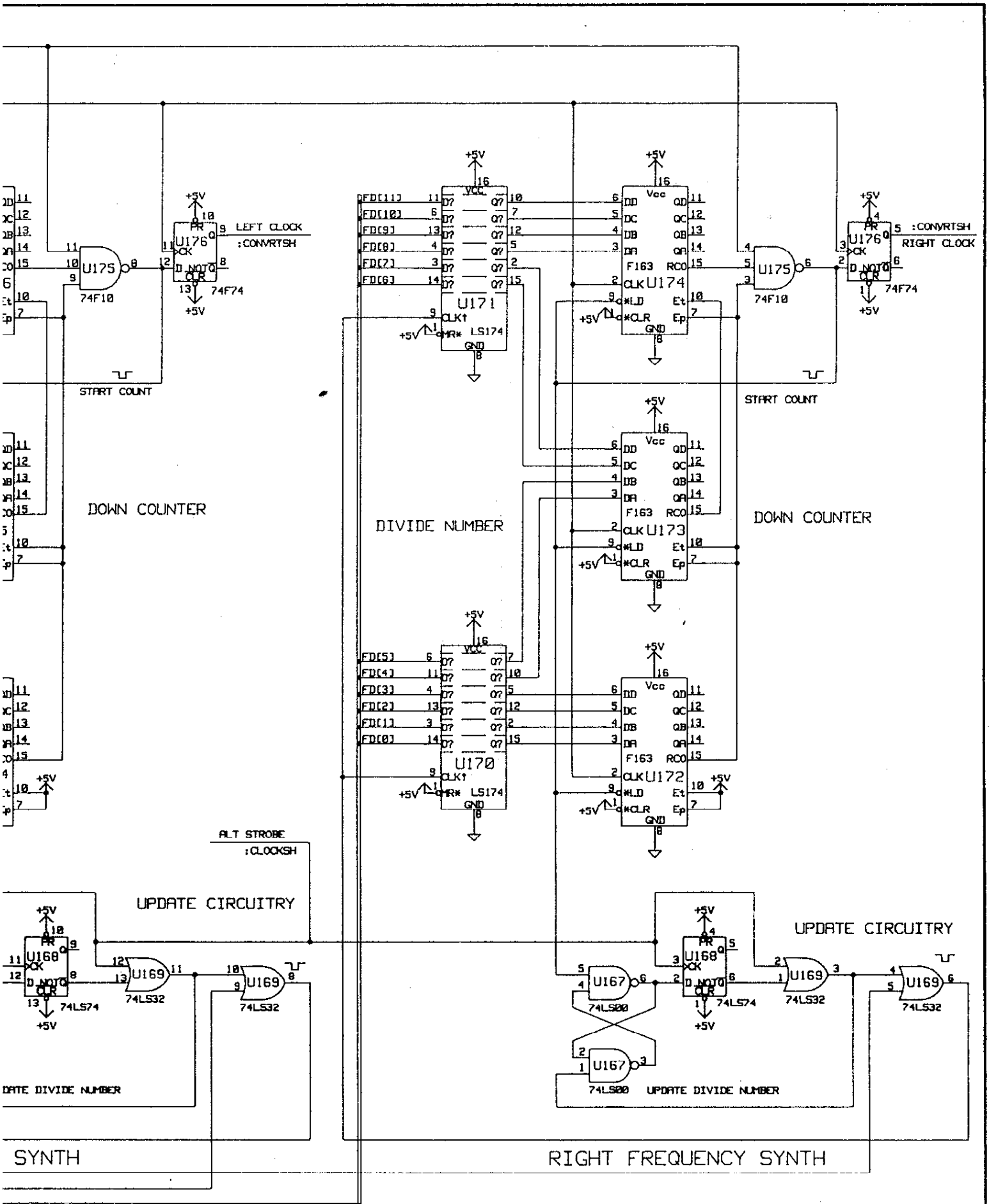


FILENAME 1072BRM	DESCRIPTION BULK MEMORY (MEMORYSH)		DWG. No. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 11 OF 16	REV M

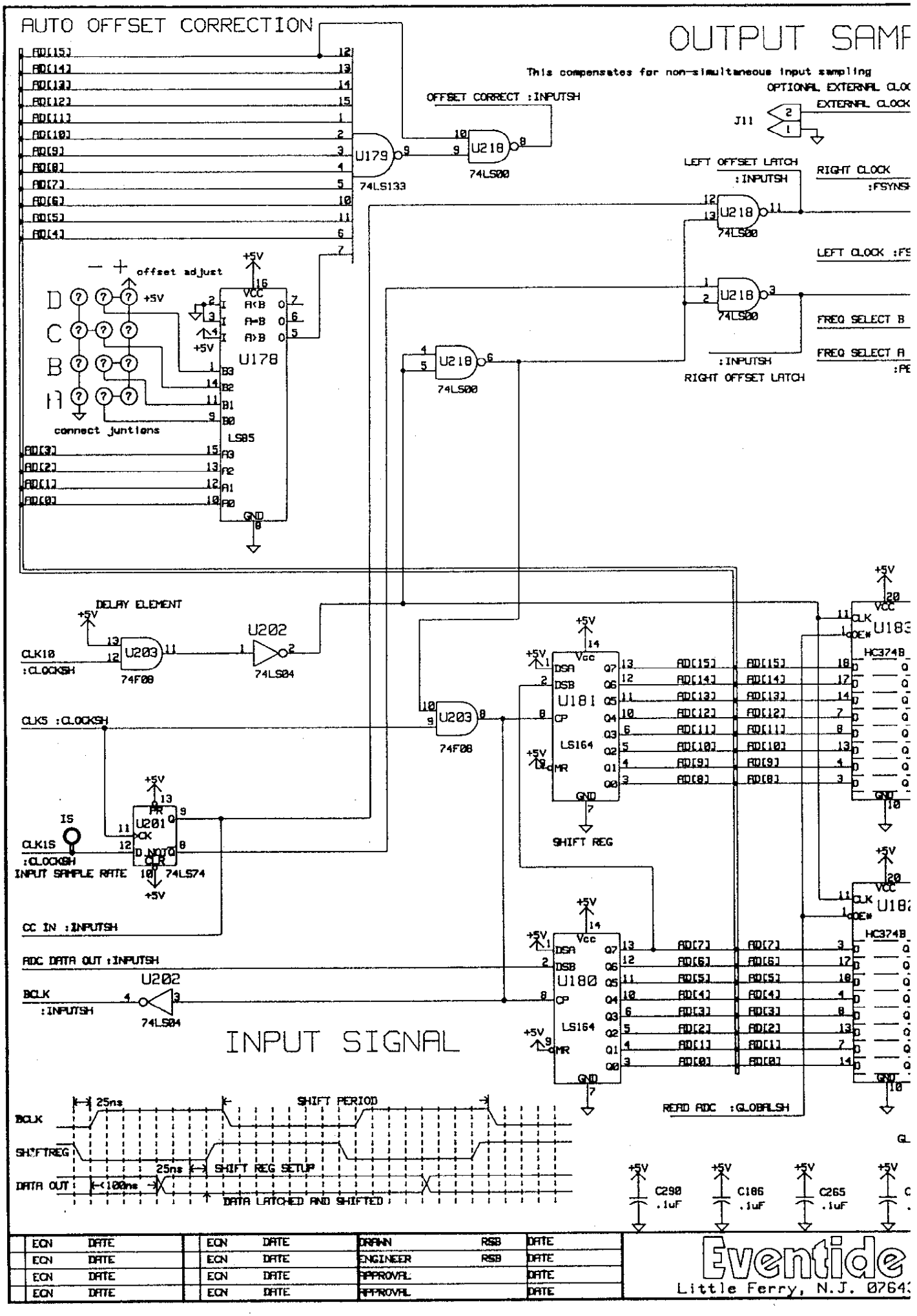


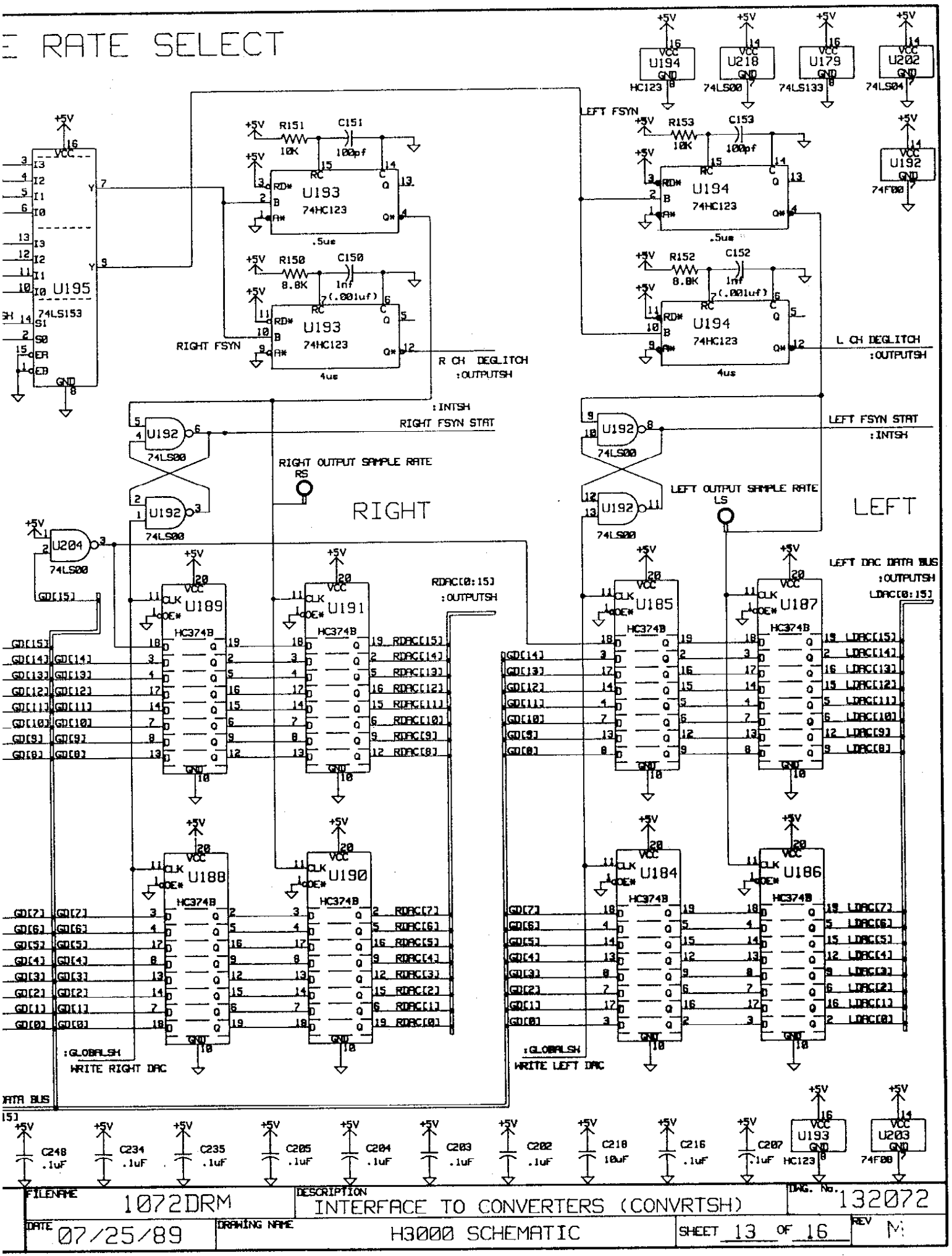
	ECN	DATE		ECN	DATE	DRAWN RSB	DATE
	ECN	DATE		ECN	DATE	ENGINEER RSB	DATE
	ECN	DATE		ECN	DATE	APPROVAL	DATE
	ECN	DATE		ECN	DATE	APPROVAL	DATE

Eventide
Little Ferry, N.J. 076

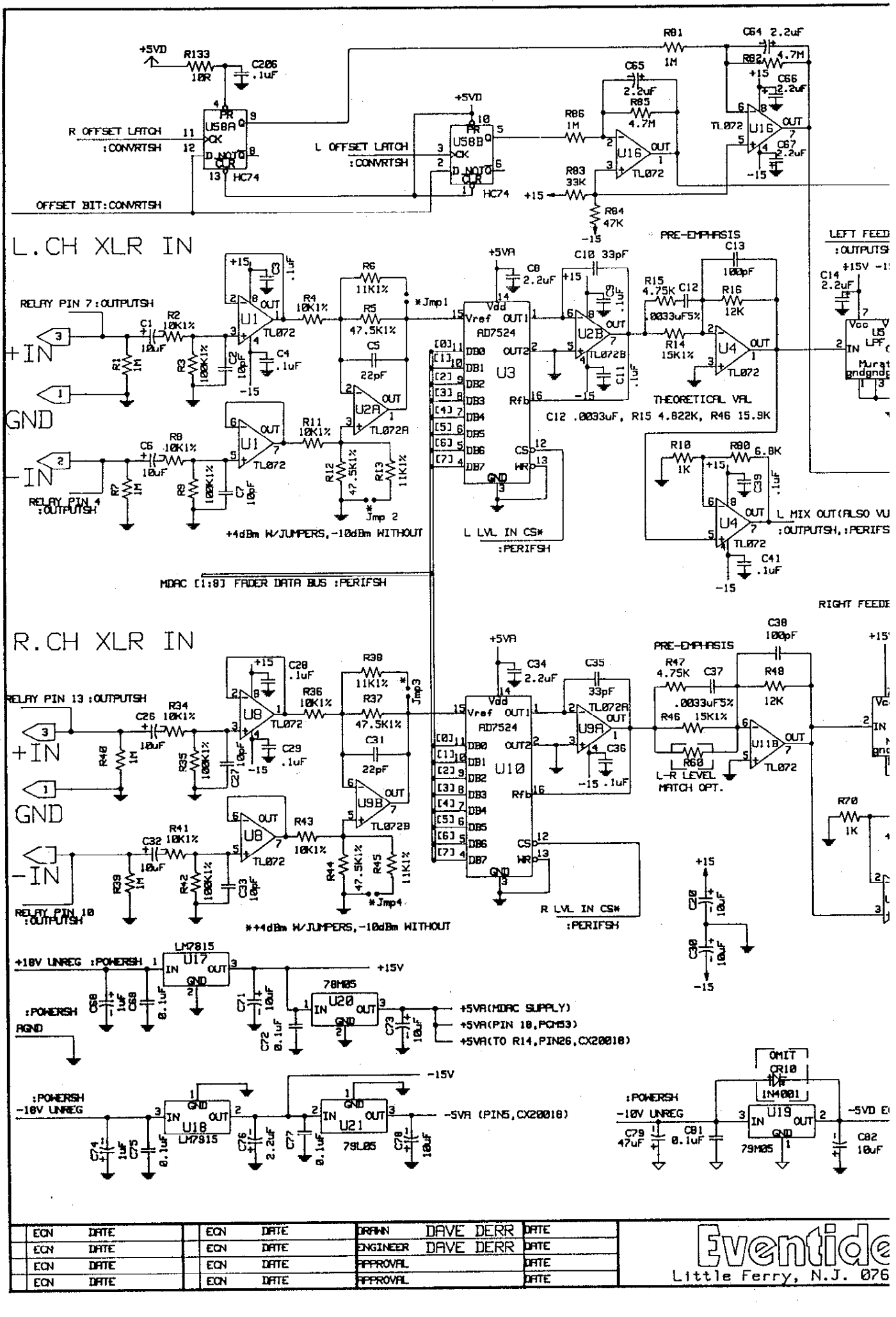


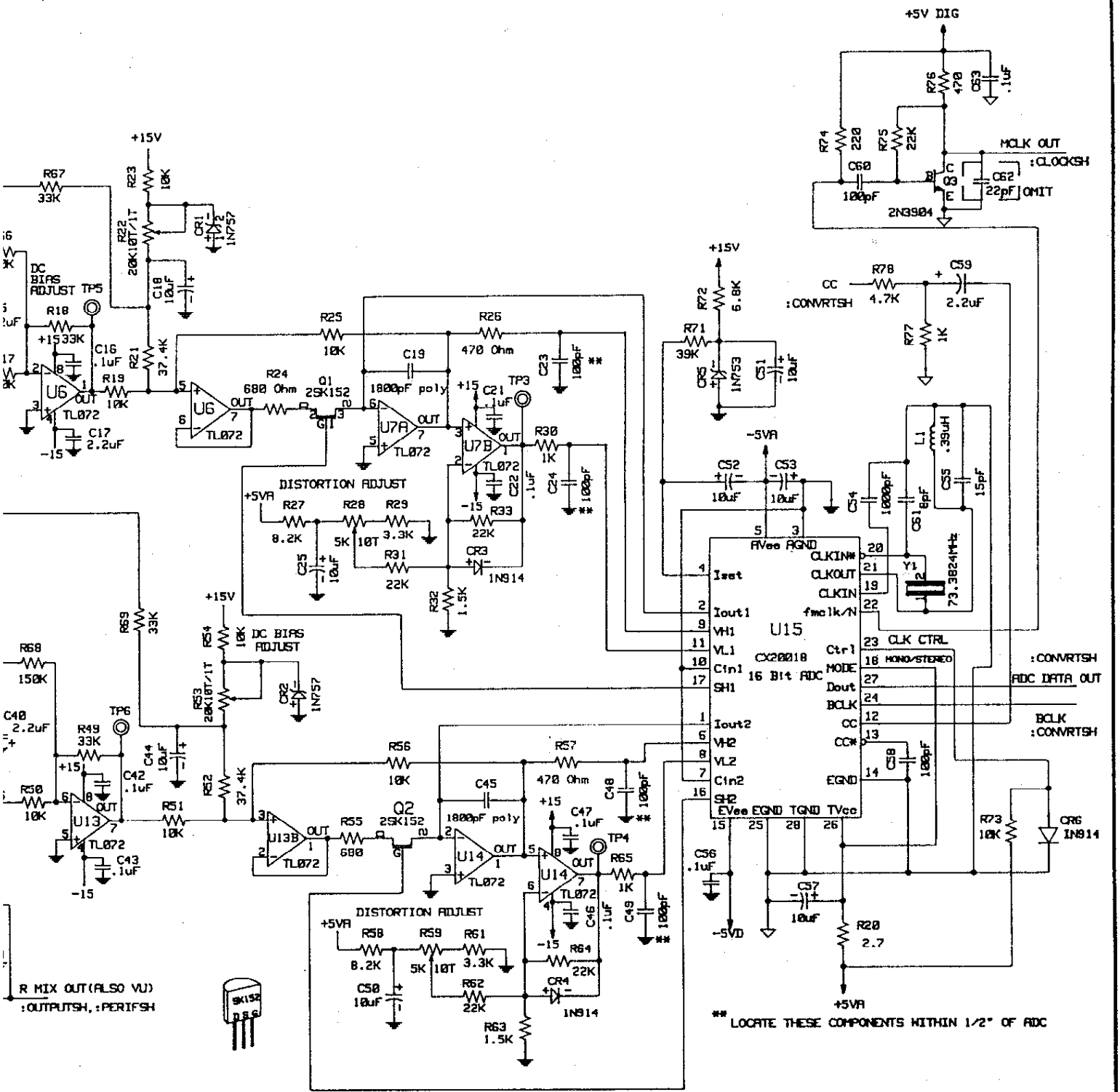
FILENAME 1072CRM	DESCRIPTION FREQUENCY SYNTHESIZERS		DWG. No. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 12 OF 16	REV M


AUTO OFFSET CORRECTION
OUTPUT SAMP
This compensates for non-simultaneous input sampling
OFFSET CORRECT :INPUTSH
OPTIONAL EXTERNAL CLOC
EXTERNAL CLOCK
J11
LEFT OFFSET LATCH
:INPUTSH
RIGHT CLOCK
:FSYNS
LEFT CLOCK :FS
FREQ SELECT B
FREQ SELECT A
:PE
RIGHT OFFSET LATCH
offset adjust
connect juntions
+5V
U178
LS85
U179
74LS133
U218
74LS00
DELAY ELEMENT
U202
74LS04
U203
74F08
CLK10
:CLOCKSH
CLK5 :CLOCKSH
U201
74LS74
CLK1S
INPUT SAMPLE RATE
CC IN :INPUTSH
ADC DATA OUT :INPUTSH
BCLK
:INPUTSH
U181
U180
LS164
SHIFT REG
HC374B
READ ADC :GLOBALSH
INPUT SIGNAL
25ns
SHIFT PERIOD
SHIFTREG
25ns
SHIFT REG SETUP
DATA OUT
100ns
DATA LATCHED AND SHIFTED
C290
.1uF
C186
.1uF
C265
.1uF
ECN
DATE
DRAWN
RSB
ENGINEER
APPROVAL
Eventide
Little Ferry, N.J. 0764



FILENAME 1072DRM	DESCRIPTION INTERFACE TO CONVERTERS (CONVRTSH)		DWG. No. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 13 OF 16	REV M


L.CH XLR IN
R.CH XLR IN
+5VD
R133
10R
C206
.1uF
R OFFSET LATCH :CONVRTSH
L OFFSET LATCH :CONVRTSH
OFFSET BIT:CONVRTSH
U58A
U58B
HC74
R81
1M
C64 2.2uF
R82
4.7M
C65
2.2uF
R85
4.7M
C66
2.2uF
R86
1M
R83
33K
R84
47K
C67
2.2uF
TL072
U16
+15
-15
PRE-EMPHASIS
C13
100pF
R15
4.75K
C12
.0033uF5%
R16
12K
R14
15K1%
C14
2.2uF
LEFT FEED
:OUTPUTSH
RELAY PIN 7 :OUTPUTSH
RELAY PIN 4 :OUTPUTSH
+IN
-IN
GND
R1
1M
R2
10K1%
C1
10uF
R3
100K1%
C2
10pF
C4
.1uF
R4
10K1%
R5
47.5K1%
R6
11K1%
*Jmp1
C5
22pF
R7
1M
R8
10K1%
C6
10uF
R9
100K1%
C7
10pF
R11
10K1%
R12
47.5K1%
R13
11K1%
*Jmp 2
U1
U2A
U2B
TL072
TL072A
TL072B
+4dBm W/JUMPERS,-10dBm WITHOUT
+5VA
C8
2.2uF
C10 33pF
C11
.1uF
U3
AD7524
Vdd
Vref
OUT1
OUT2
Rfb
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
CS
WR
GND
L LVL IN CS*
:PERIFSH
MDAC [1:8] FADER DATA BUS :PERIFSH
THEORETICAL VAL
C12 .0033uF, R15 4.822K, R46 15.9K
R10
1K
R80
6.8K
C39
.1uF
U4
L MIX OUT(ALSO VU
:OUTPUTSH,:PERIFS
C41
.1uF
RIGHT FEEDE
RELAY PIN 13 :OUTPUTSH
RELAY PIN 10 :OUTPUTSH
R34
10K1%
R35
100K1%
R36
10K1%
R37
47.5K1%
R38
11K1%
*Jmp3
C26
10uF
C27
10pF
C28
.1uF
C29
.1uF
C31
22pF
R39
1M
R40
1M
R41
10K1%
R42
100K1%
R43
10K1%
R44
47.5K1%
R45
11K1%
*Jmp4
C32
10uF
C33
10pF
U8
U9A
U9B
U10
U11B
TL072
TL072A
TL072B
**+4dBm W/JUMPERS,-10dBm WITHOUT
C34
2.2uF
C35
33pF
C36
.1uF
R47
4.75K
C37
.0033uF5%
R48
12K
R46
15K1%
R60
L-R LEVEL MATCH OPT.
C38
100pF
R70
1K
R LVL IN CS*
:PERIFSH
C28
10uF
C30
10uF
+18V UNREG :POWERSH
:POWERSH
AGND
LM7815
U17
78M05
U20
C68
1uF
C69
0.1uF
C71
10uF
C72
0.1uF
C73
10uF
+15V
+5VA(MDAC SUPPLY)
+5VA(PIN 18,PCM53)
+5VA(TO R14,PIN26,CX20018)
-15V
-18V UNREG
U18
LM7915
U21
79L05
C74
1uF
C75
0.1uF
C76
2.2uF
C77
0.1uF
C78
10uF
-5VA (PIN5,CX20018)
OMIT
CR10
1N4001
U19
79M05
C79
47uF
C81
0.1uF
C82
10uF
-5VD E
ECN
DATE
DRAWN
DAVE DERR
ENGINEER
DAVE DERR
APPROVAL
Eventide
Little Ferry, N.J. 076



NOTES:

PRE-EMPHASIS EQUATIONS

$$R14 = \frac{ZL*ZH*(1-M)}{M*ZL-ZH}$$

M = HIGH FREQ GAIN
M = FL(low)/FH(high) FOR 10dB, M=.316
SELECT RC (R15,C12) FOR DESIRED SHELVING FREQUENCY (IN THIS CASE 10kHz)
ZL = R15+(1/(2*PI*FL*C12))
ZH = R15+(1/(2*PI*FH*C12))
FOR VALUES SHOWN FL=20Hz,FH=20kHz

PARTS IN OUTLINE BOXES ARE OPTIONAL

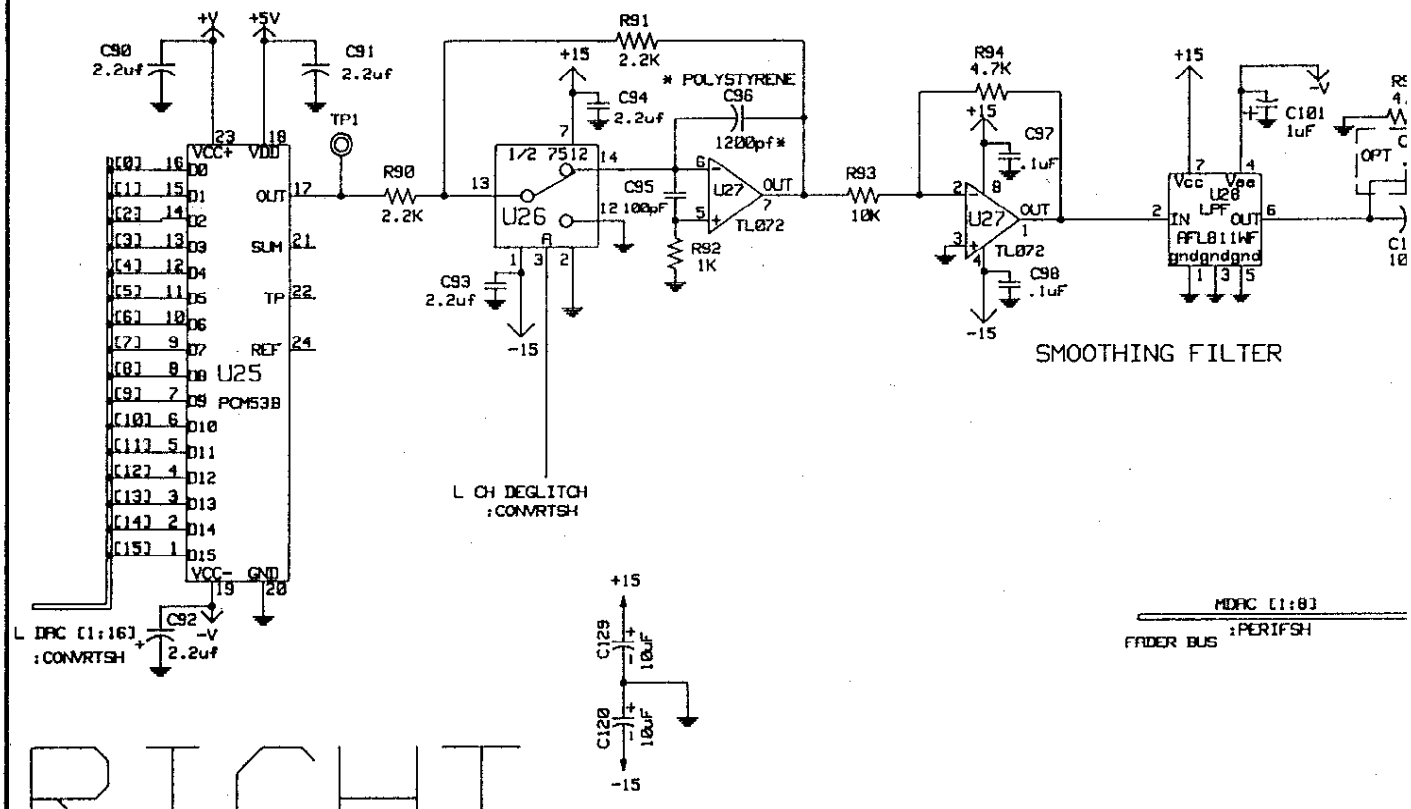
LAST DESIGNATOR

U	64
C	72
R	91
CR	14
L	1
X	1
Q	3

FILENAME: 1072ERM	DESCRIPTION: AUDIO INPUT SECTION (INPUTSH)		DWG. No. 132072
DATE: 07/25/89	DRAWING NAME: H3000 SCHEMATIC	SHEET 14 OF 16	REV M

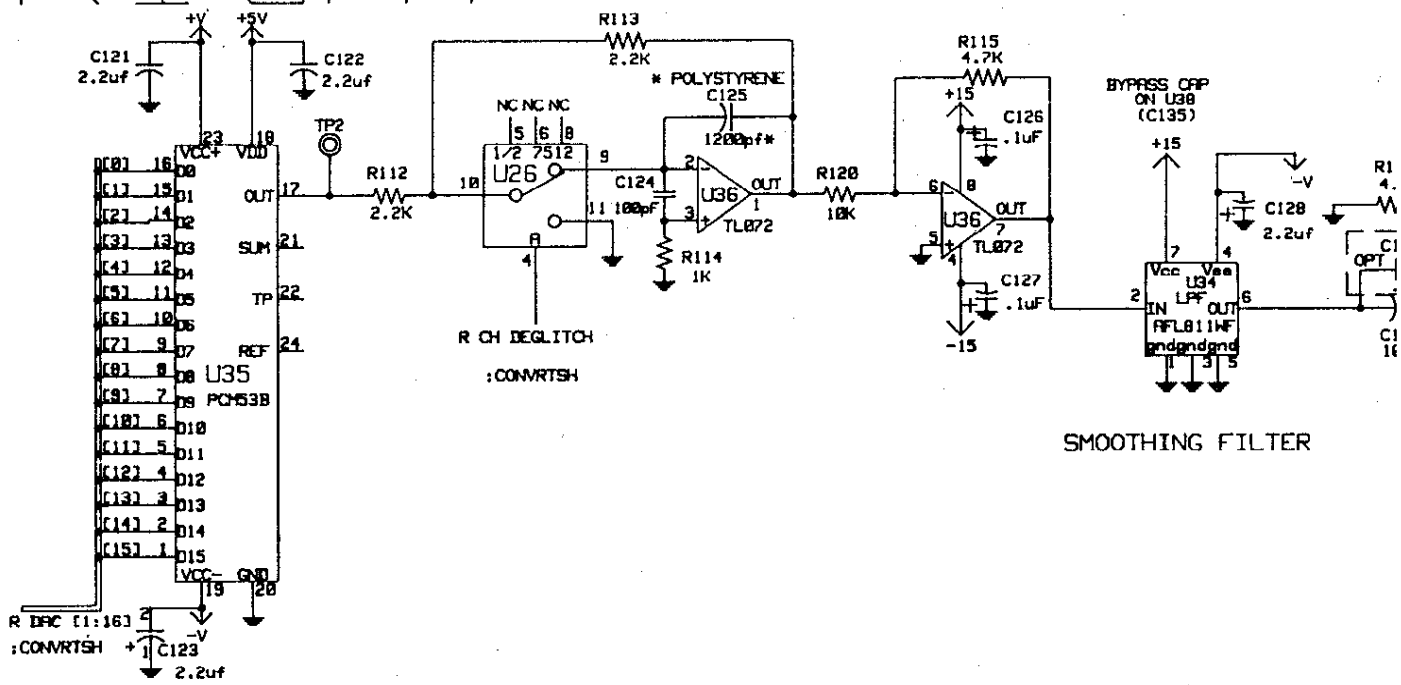
LEFT

SAMPLE HOLD



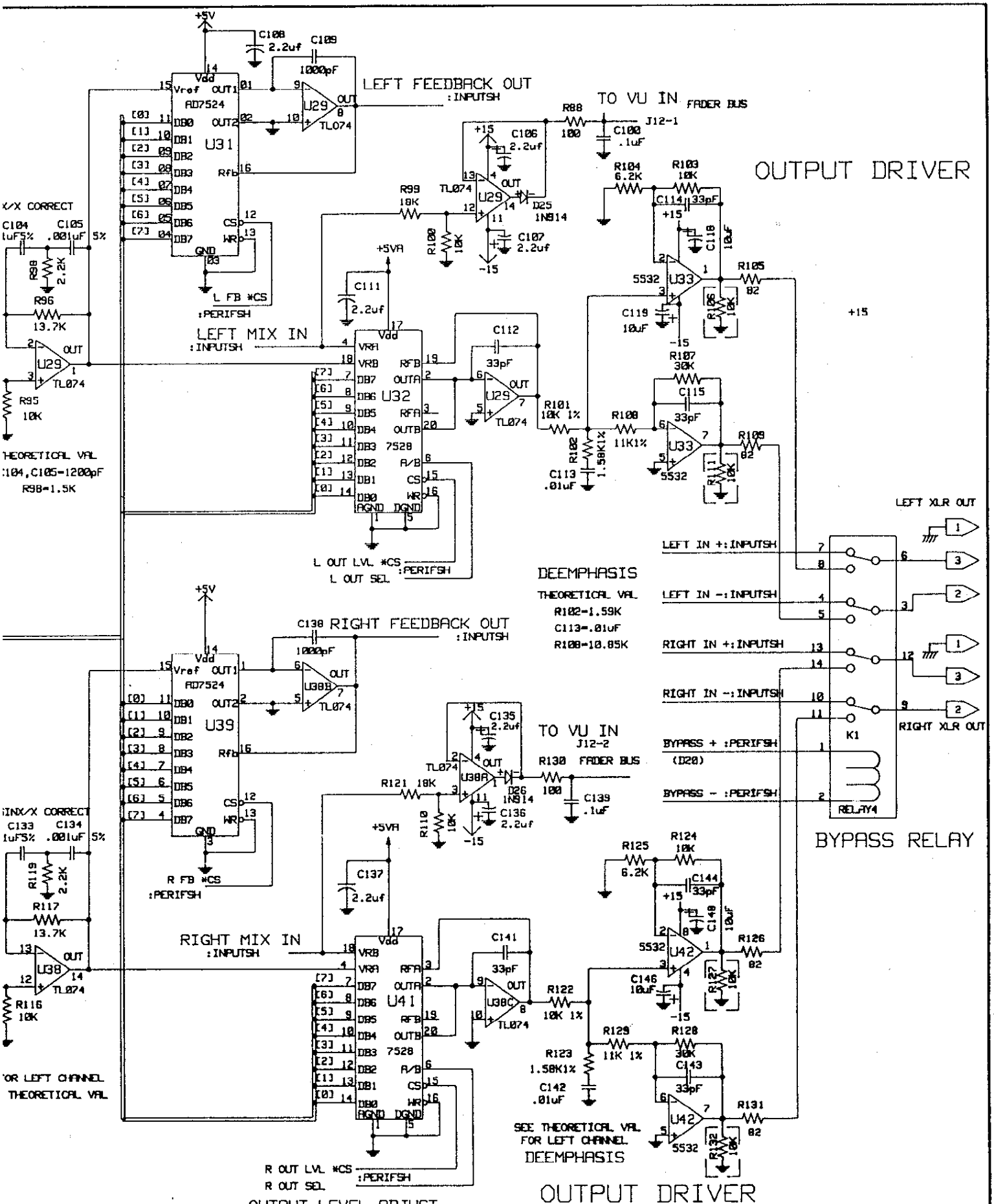
RIGHT

SAMPLE HOLD

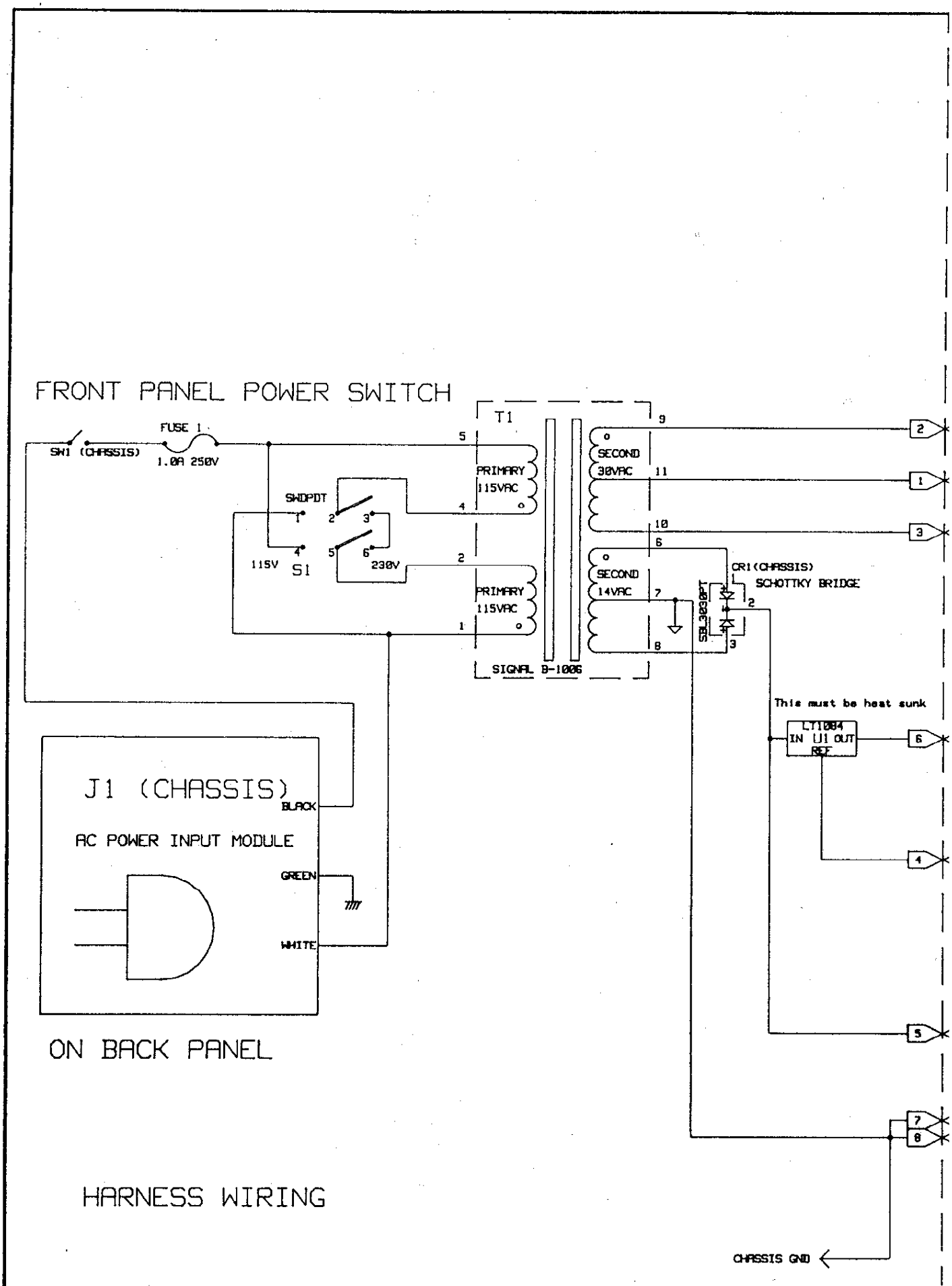


ECN	DATE	ECN	DATE	DRAWN DAVE DERR	DATE
ECN	DATE	ECN	DATE	ENGINEER DAVE DERR	DATE
ECN	DATE	ECN	DATE	APPROVAL	DATE
ECN	DATE	ECN	DATE	APPROVAL	DATE

Eventide
Little Ferry, N.J. 0764

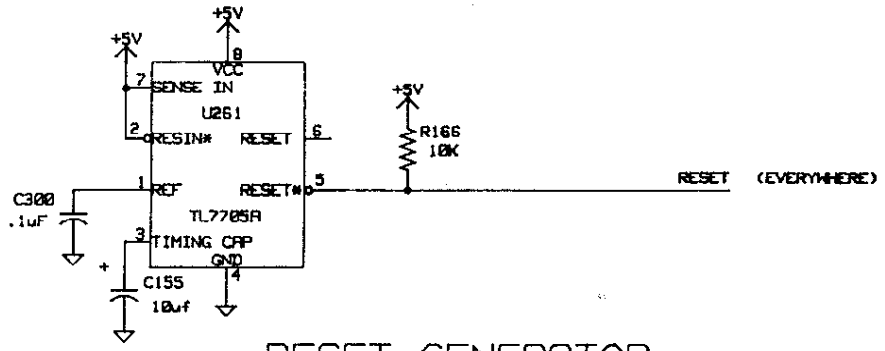


FILENAME	DESCRIPTION	DWG. No.
1072FRM	DAC OUTPUT SECTION (OUTPUTSH)	132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 15 OF 16 — REV M

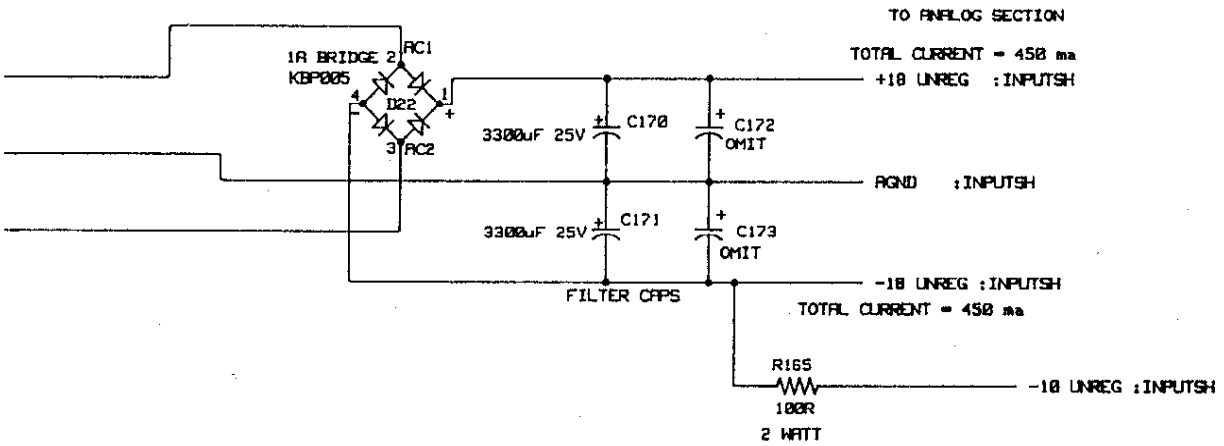


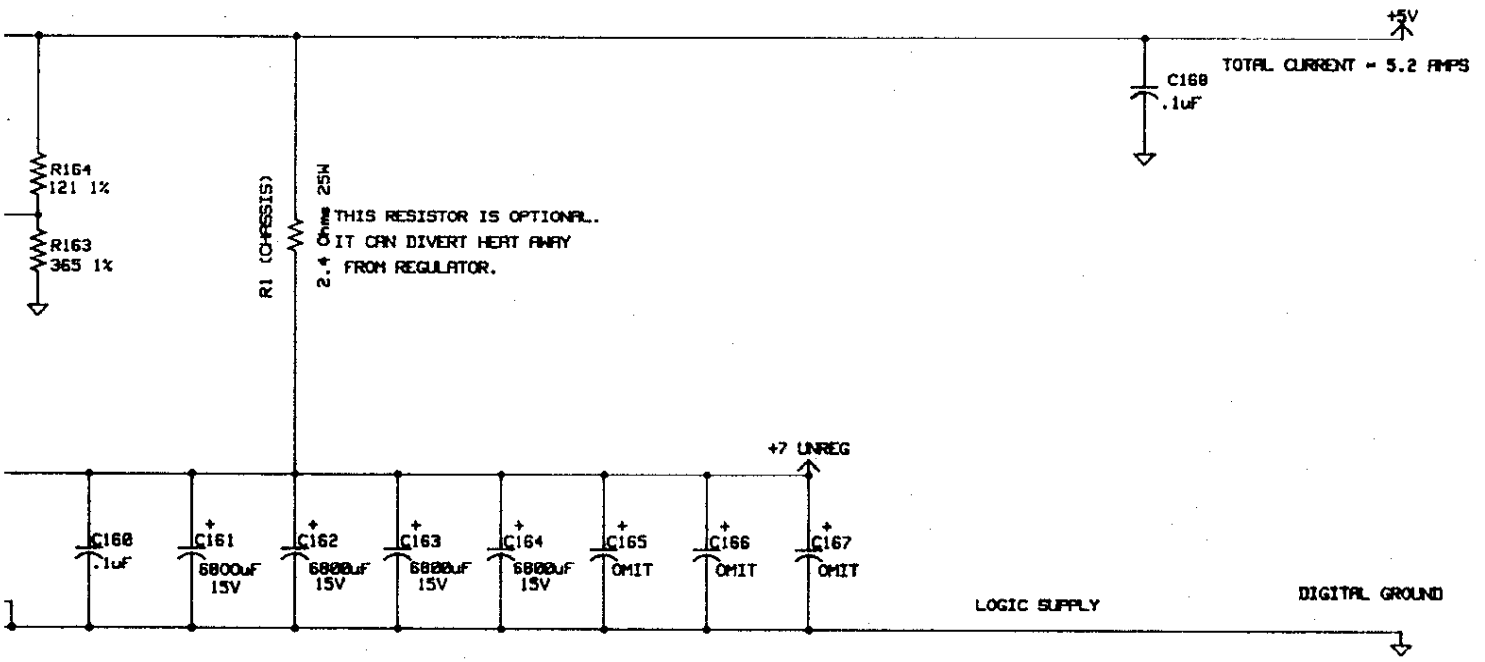
ECN	DATE	ECN	DATE	DRAWN	DATE
ECN	DATE	ECN	DATE	ENGINEER	DATE
ECN	DATE	ECN	DATE	APPROVAL	DATE
ECN	DATE	ECN	DATE	APPROVAL	DATE

Eventide
Little Ferry, N.J. 07643



RESET GENERATOR





POWER SUPPLY

FILENAME 1072GRM	DESCRIPTION POWER SUPPLY AND RESET (POWERSH)		DWG. No. 132072
DATE 07/25/89	DRAWING NAME H3000 SCHEMATIC	SHEET 16 OF 16	REV V1