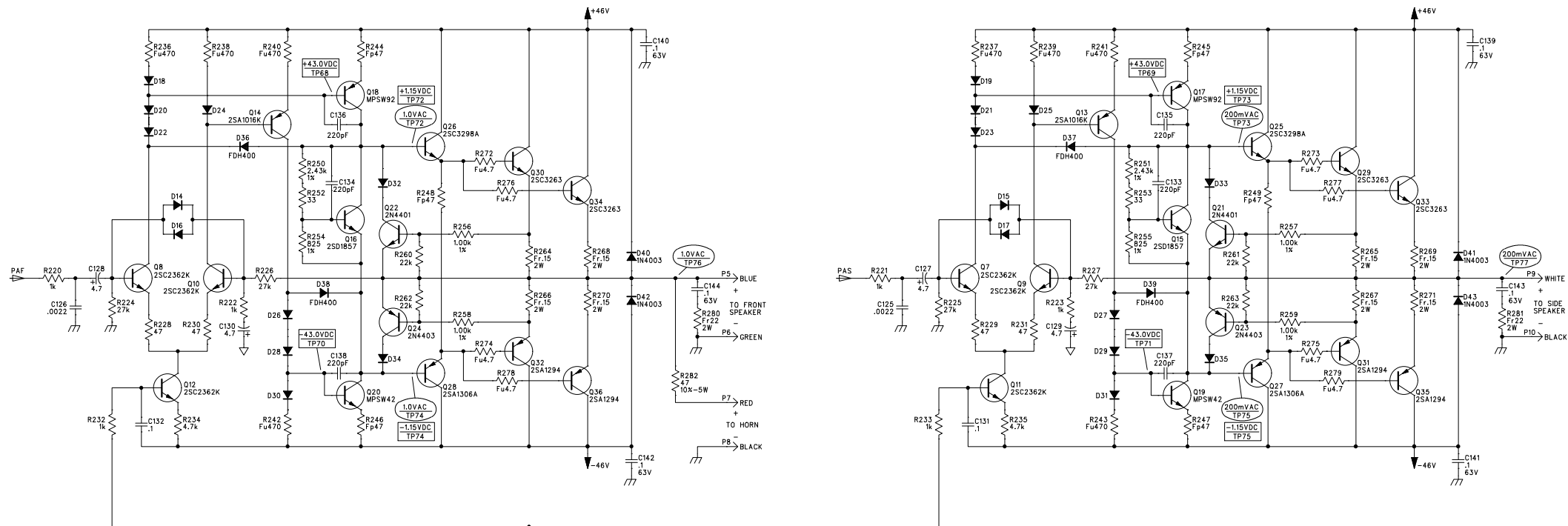
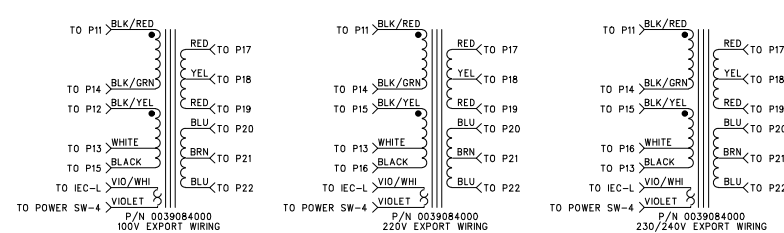
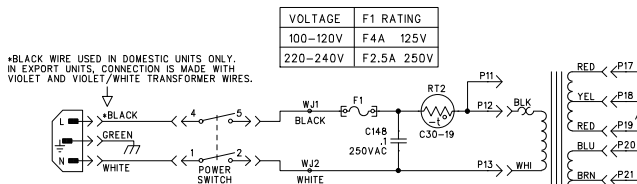
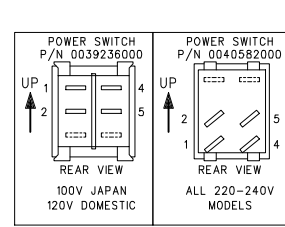
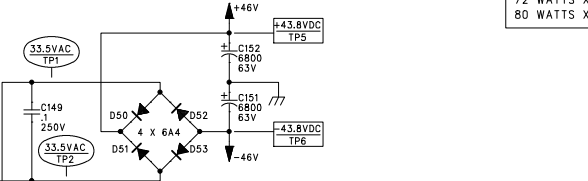
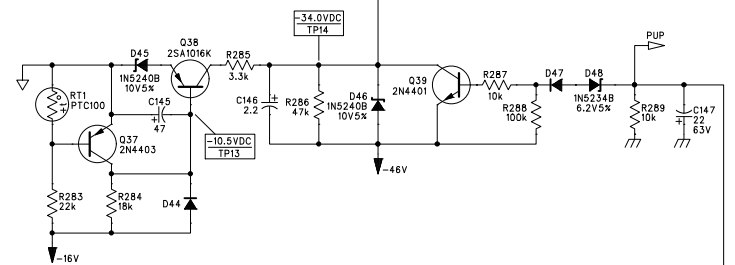


REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
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OUTPUT POWER TEST:
 UNIT AT RATED LINE VOLTAGE.
 8 OHM RESISTIVE LOADS CONNECTED TO P5/P6 AND P9/P10.
 ALL CONTROLS FULLY COUNTER-CLOCKWISE EXCEPT MASTER VOLUME (R193) SET FULLY CLOCKWISE.
 SFX DISABLE SWITCH (S6) OUT.
 CONNECT 1kHz SINEWAVE TO RING OF LEFT INSERT JACK (J9). (INSERT PLUG FULLY, THEN BACK OUT ONE CLICK.)
 ADJUST SIGNAL LEVEL TO VERIFY THE FOLLOWING AT P5/P6:
 76 WATTS AT 0.1% T.H.D.
 84 WATTS AT 1.0% T.H.D.
 93 WATTS AT 5.0% T.H.D.
 SFX DISABLE SWITCH (S6) IN.
 ADJUST SIGNAL FREQUENCY FOR EQUAL POWER AT BOTH LOADS (APPROX. 4.2kHz).
 ADJUST LEVEL TO VERIFY THE FOLLOWING AT P5/P6 AND P9/P10:
 62 WATTS X 2 = 124 WATTS AT 0.1% T.H.D.
 72 WATTS X 2 = 144 WATTS AT 1.0% T.H.D.
 80 WATTS X 2 = 160 WATTS AT 5.0% T.H.D.



- TESTPOINT VALUES FOR TP55-56 AND TP65 MAY VARY GREATLY WITH SPECIFIC EXCITATION FREQUENCY, AND ARE DEPENDENT UPON DSP SOFTWARE REVISION.
- ADDITIONAL CONDITION FOR TP65: TEMPORARILY SET MIC/LINE FX LEVEL (R162) TO 10 (FULL CLOCKWISE) TO OBSERVE SIGNAL AT TP65.
- FOR TESTPOINTS TP41-51 AND TP54-77, CONNECT 1kHz, 25mV SINEWAVE SIGNAL TO LINE INPUT (J6). FOR TESTPOINTS TP57-77, SET MIC/LINE FX LEVEL (R162) TO 1 (FULL COUNTER-CLOCKWISE).
- FOR TESTPOINTS TP39-40, CONNECT 1kHz, 100mV SINEWAVE SIGNAL TO AUX IN (J4), L AND R.
- ADDITIONAL CONDITIONS FOR TP27-38: CHANGE SIGNAL FREQUENCY TO 6.3 kHz. SET STRONG DYNAMICS (R26) TO 10 (FULL CLOCKWISE).
- FOR TESTPOINTS TP23-38 AND TP52-53, CONNECT 1kHz, 25mV SINEWAVE SIGNAL TO INSTRUMENT INPUT (J1).
- TESTPOINTS TP1-22 READ WITH NO INPUT SIGNAL. FOR TP16-20, CONNECT FOOTSWITCH ASSEMBLY 0059871000 TO FOOTSWITCH JACK (J11).
- ALL TESTPOINT VOLTAGES READ TO GROUND WITH A 50MΩ WITH UNIT AT RATED LINE VOLTAGE; P1, P2 AND P4 CONNECTED TO P11, P12 AND P14 RESPECTIVELY; AND P3 CONNECTED TO uDSP PCA 0059873000.
- CONTROLS SET TO 5-1/2 (50% ROTATION) EXCEPT STRING DYNAMICS (R26) AND FEEDBACK NOTCHES (R56 R113) SET TO 1 (FULL COUNTER-CLOCKWISE). SET SFX DISABLE SWITCH (S6) IN. SELECT FIRST DELAY (MOST COUNTER-CLOCKWISE DELAY SELECTION) FOR ENCODERS S2 AND S4. NO FOOTSWITCH.
- LAST REFERENCES: C197, CS2, D74, F3, J11, P22, P14, Q42, R315, RT2, S6, TP77, U26, WJ2. (WJ3 NOT USED).
- THIS SCHEMATIC IS FOR PCB FABRICATION P/N 0059871000 AND PCB ASSEMBLY P/N 0059878000.
- ALL POLARIZED CAPACITORS IN uF, 20% 50V MINIMUM.
- ALL UNPOLARIZED CAPACITORS IN uF, 10% OR BETTER; 50V MINIMUM. (POWER SUPPLY BYPASS CAPACITORS ARE 20%).
- ALL DIODES ARE IN4448.
- ALL RESTORERS IN OHMS, 5% 1/4W.

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Fender MUSICAL INSTRUMENTS
 Corona, CA U.S.A.

CHECKED BY: _____ TITLE: SERVICE DIAGRAM, COMBINED (schematic)
 DATE: _____ ACUSTASONIC SFX 2
 (POWER AMP & POWER SUPPLY)

APPROVED BY: _____
 DATE: _____

DRAWN: B. DESI ENGR: B. DESI
 DATABASE FILE: Z9425.SCH

SIZE: DRAWING NUMBER: 0059876000
 RELEASE DATE: 22-APR-03 SHEET: 2 OF 3

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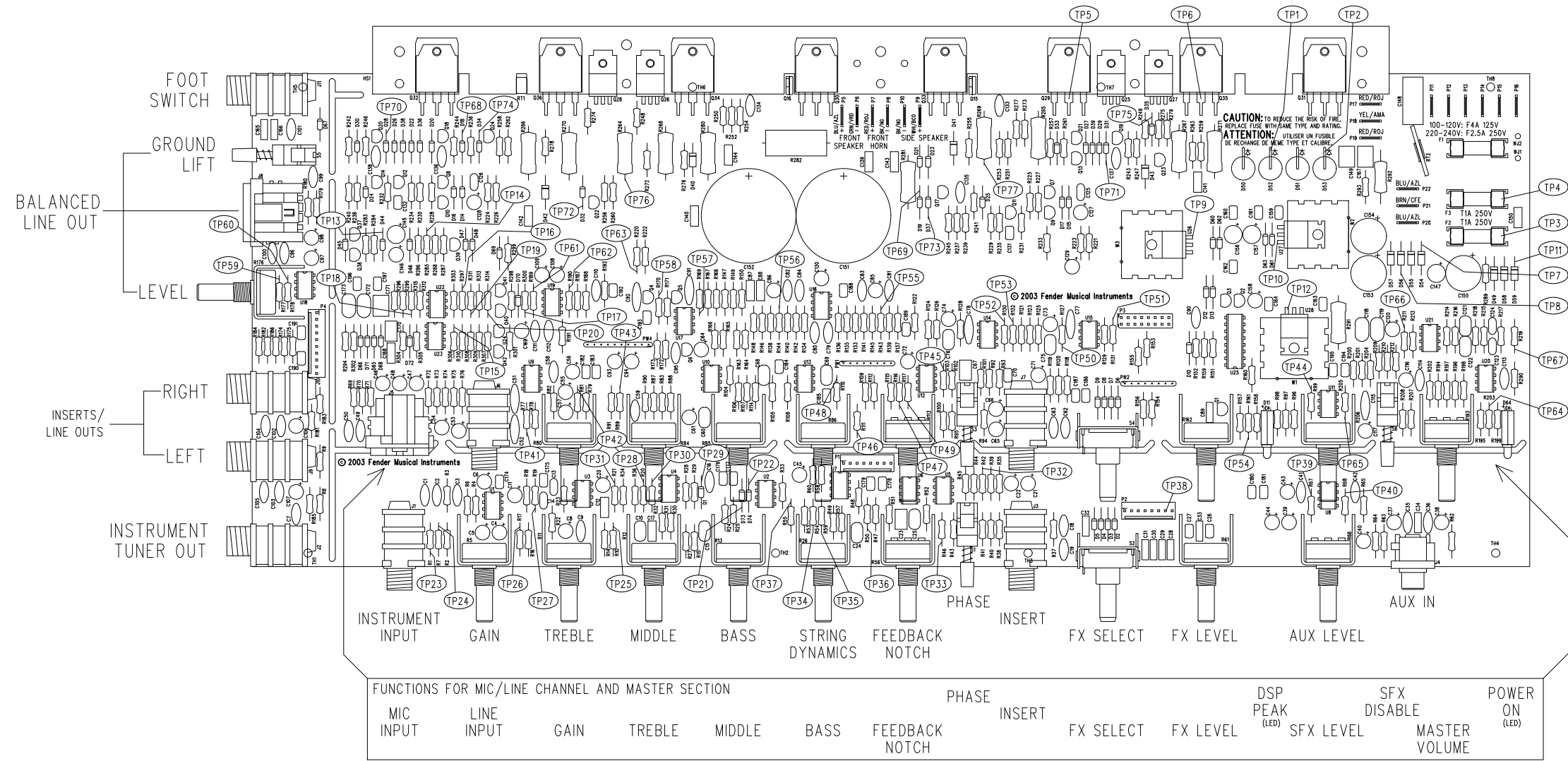
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FUNCTIONS FOR MIC/LINE CHANNEL AND MASTER SECTION

MIC INPUT LINE INPUT GAIN TREBLE MIDDLE BASS FEEDBACK NOTCH

PHASE INSERT FX SELECT FX LEVEL DSP PEAK (LED) SFX LEVEL SFX DISABLE MASTER VOLUME POWER ON (LED)

FILM/DWG: SERVICE DIAGRAM
 DATABASE: Z542P.PCB DATE: 22-APR-03

2. DSP PCB ASSEMBLY P/N 0059873000 MUST BE CONNECTED TO P3 FOR SIGNAL TO APPEAR AT TP55 AND TP56.
 1. SEE SHEETS 1 AND 2 FOR PRIMARY WIRING, TEST CONDITIONS AND TP VALUES.
 NOTES: (UNLESS OTHERWISE NOTED)

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CHECKED BY: _____	TITLE: SERVICE DIAGRAM, COMBINED (PCB assy)		
DATE: _____	ACOUSTASONIC SFX 2		
APPROVED BY: _____	MAIN		
DATE: _____	SIZE: D	DRAWING NUMBER: 0059876000	REV: A
DRAWN: B. DESI	ENGR: B. DESI	RELEASE DATE: 22-APR-03	SHEET 3 OF 3
DATABASE FILE: Z542P.PCB			

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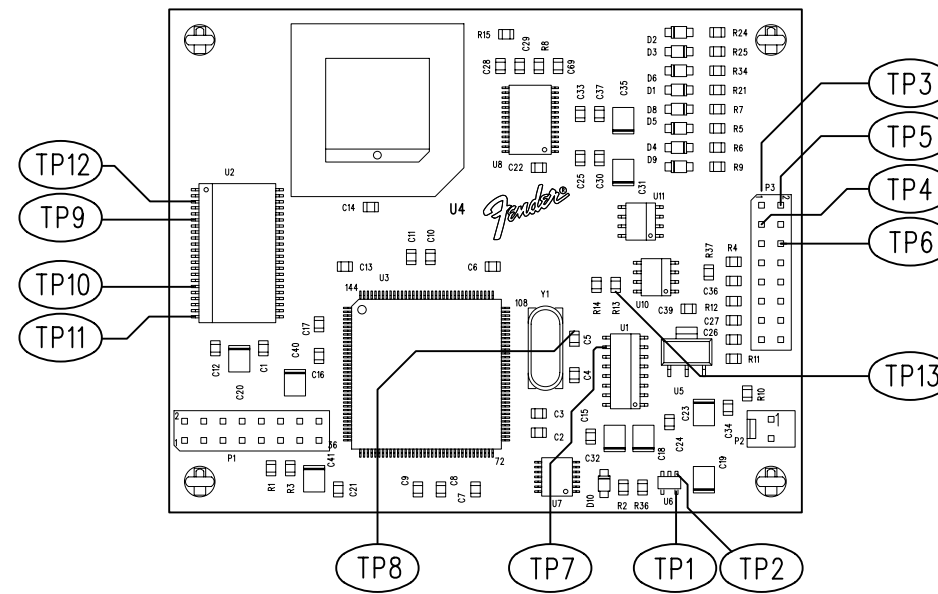
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REVISIONS


REV.	DESCRIPTION	DATE	APPROVED
A	PR480	30-NOV-01	J T L
B	EC 2743	07-MAR-02	J T L
C	EC 2789	10-JUN-02	J C S
D	PR542	25-APR-03	R J D



FILM/DWG: SERVICE DIAGRAM
 DATABASE: Z481P.PCB DATE: 25-APR-03

1. SEE SHEET 1 FOR TEST CONDITIONS AND TEST POINT VALUES.

NOTES: (UNLESS OTHERWISE NOTED)

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CHECKED BY: _____ DATE: _____		TITLE: SERVICE DIAGRAM, COMBINED (PCB assy) uDSP SERIES	
APPROVED BY: _____ DATE: _____		SIZE B	DRAWING NUMBER 0057283000
DRAWN: J. Jimenez	ENGR: J. Lamb	REV. D	
DATABASE FILE: Z481P.PCB		RELEASE DATE: 30-NOV-01	SHEET 2 OF 2