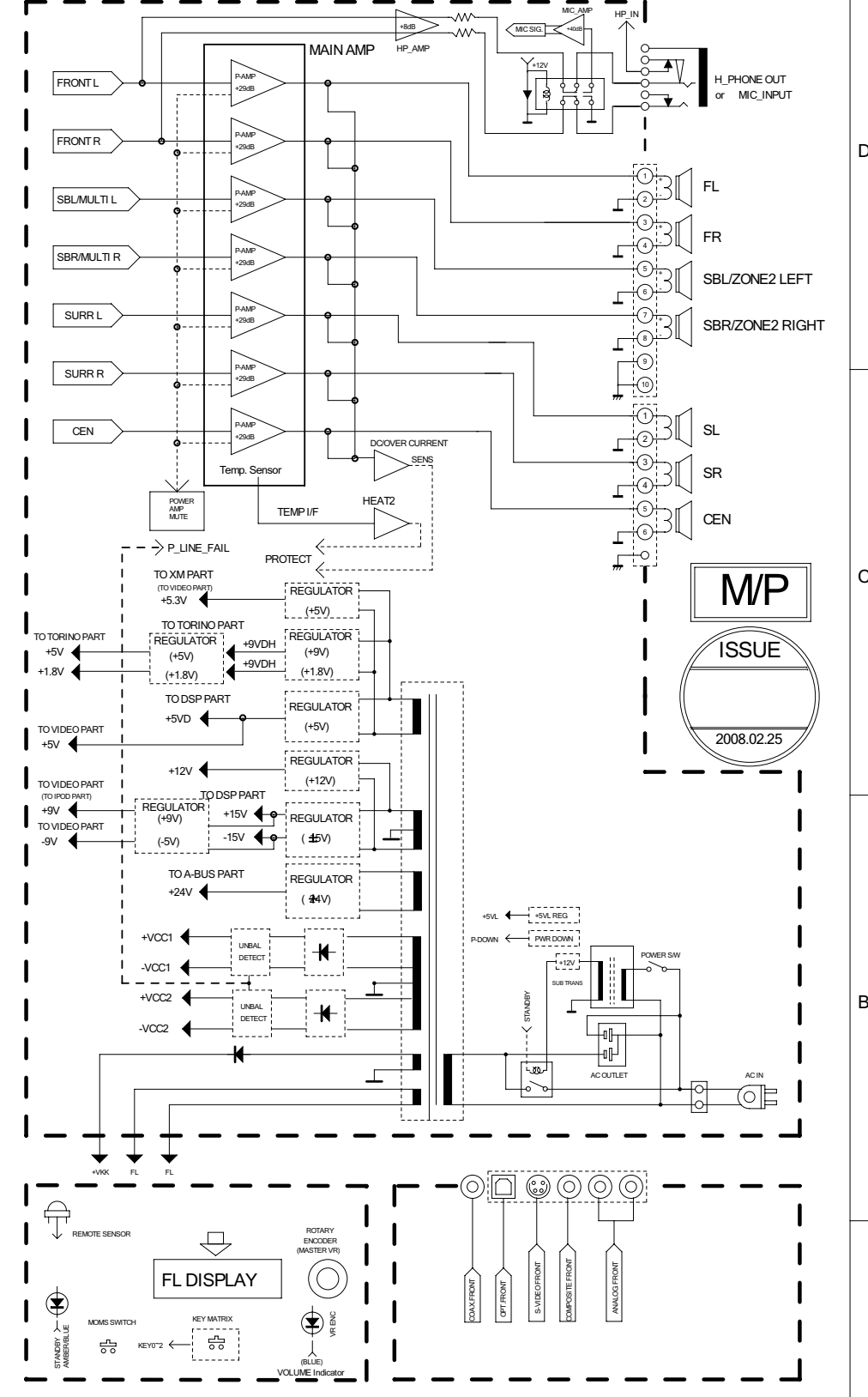
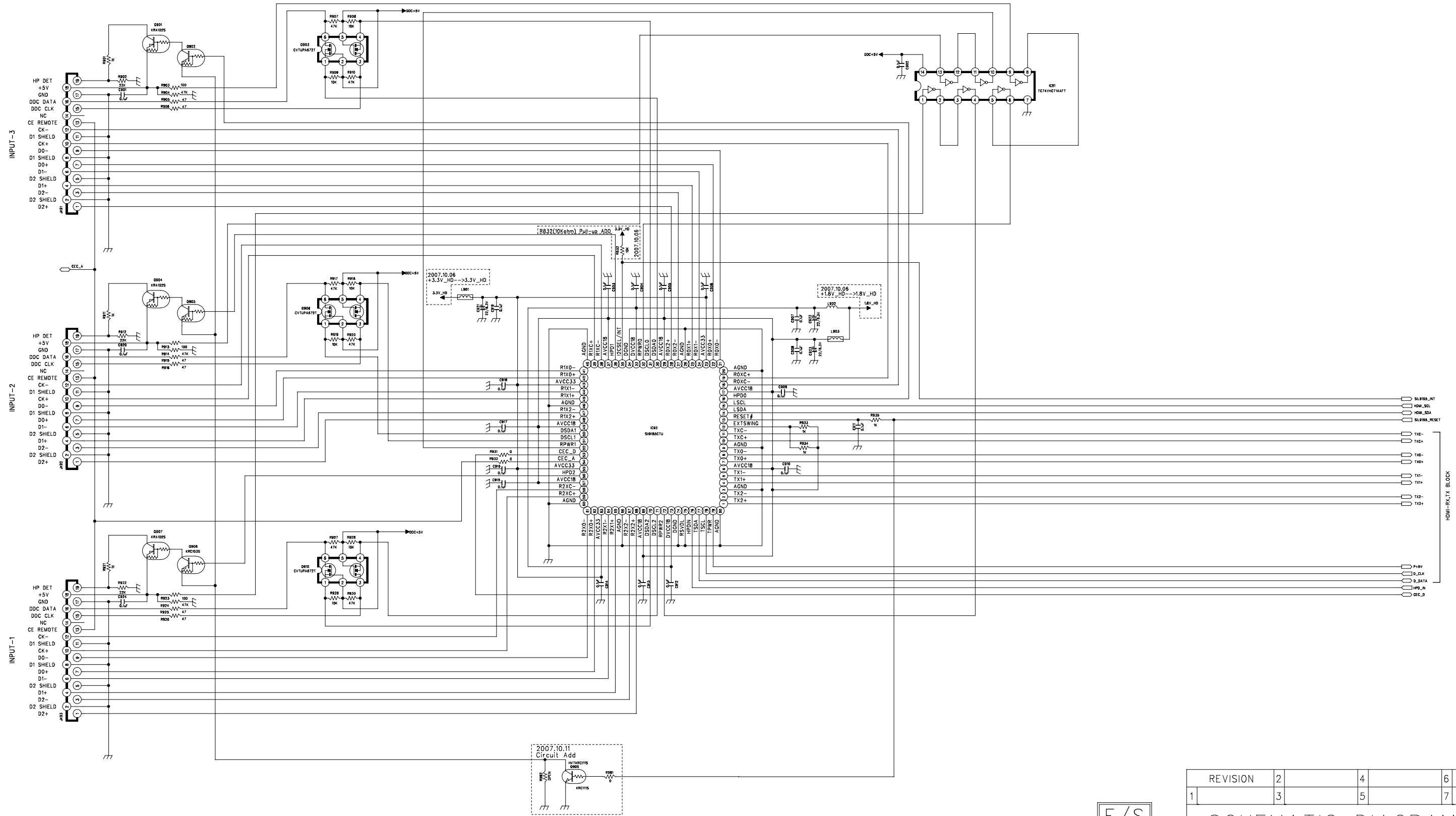


### AVR254/255/354/355 BLOCK DIAGRAM

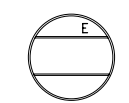


REVISION	2	4	6	
1	3	5	7	
<b>SCHEMATIC DIAGRAM</b>				SHEET
MODEL	AVR254/255/354/355			1/1
DESIGN	CHECK	APPROVE	DRAWING NO	
S.H.Yang	W.Y.Yang	G.S.Wey	BLOCK DIAGRAM	
08.02.25	08.02.25	08.02.25	2024BLDZ	

CUP12035Z

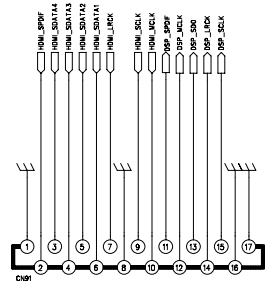
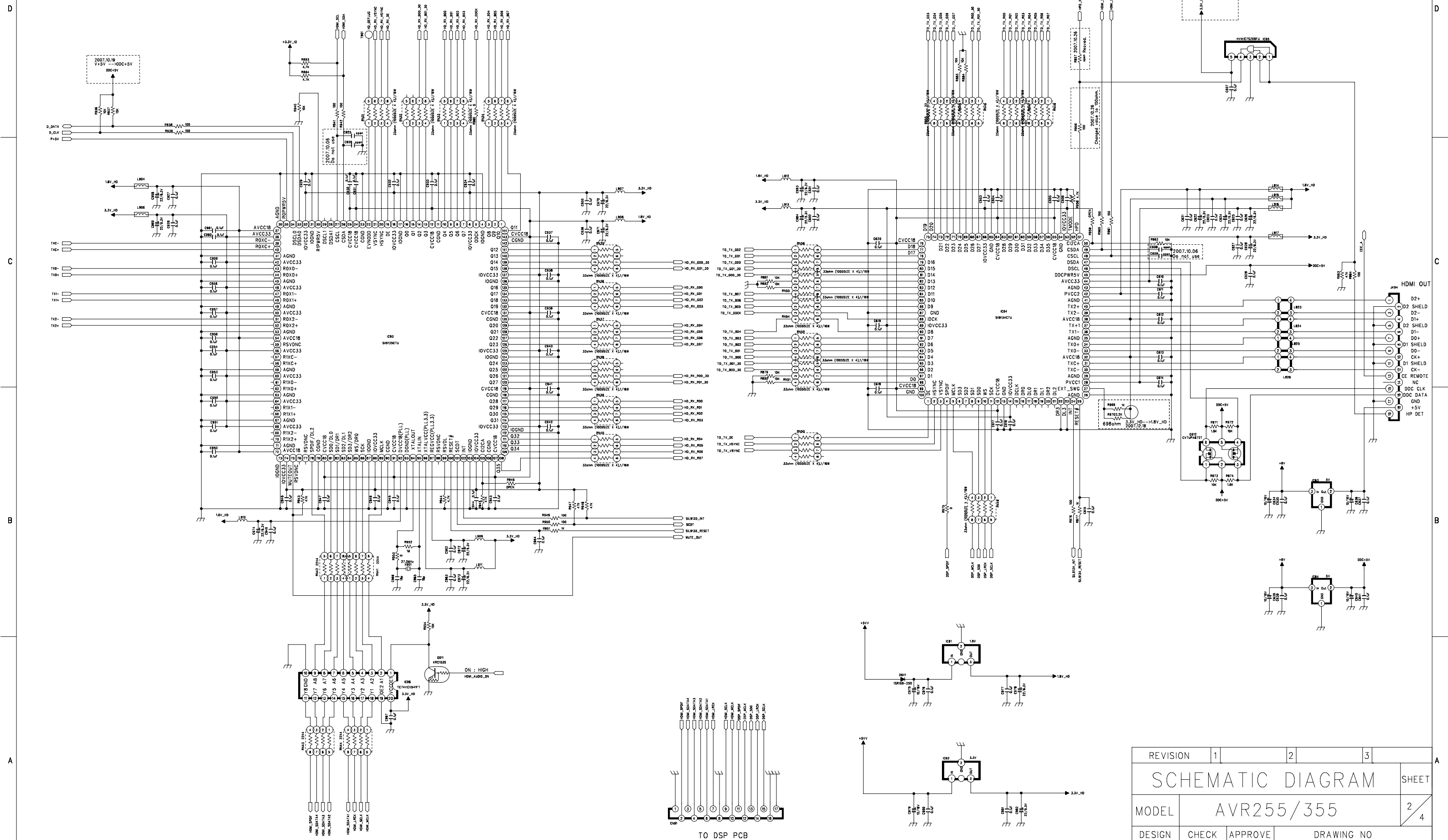


E/S



REVISION	2	4	6
1	3	5	7
SCHEMATIC DIAGRAM			SHEET
MODEL	AVR255/355		1/4
DESIGN	CHECK	APPROVE	DRAWING NO
M.S KIM	W.Y YANG	G.S WEY	2035SCEZ
07.14.07	07.14.07	07.14.07	(HDMI-INPUT)

CUP12035Z



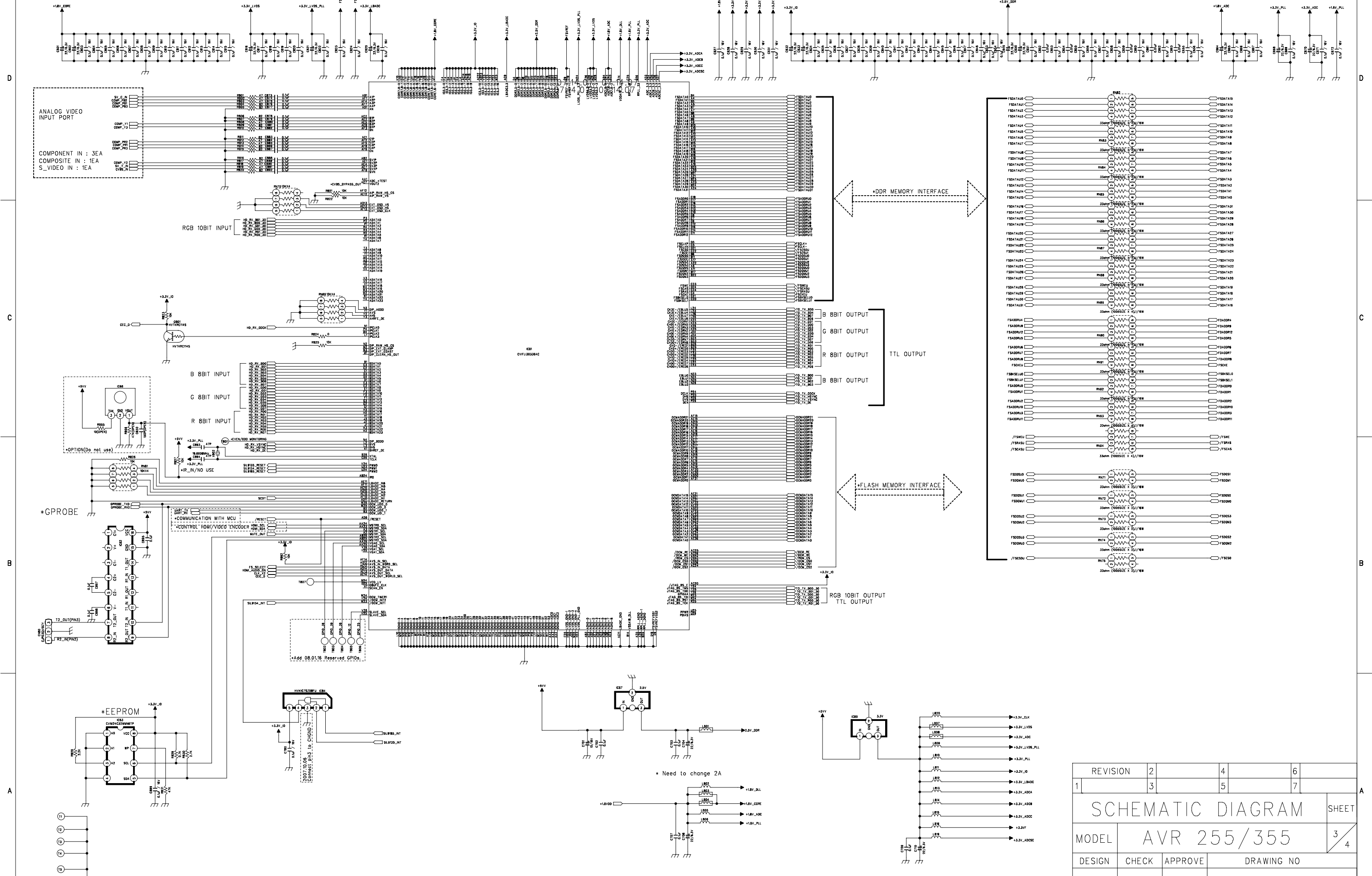
TO DSP PCB

REVISION	1	2	3
SCHEMATIC DIAGRAM			SHEET
MODEL	AVR255/355		2/4
DESIGN	CHECK	APPROVE	DRAWING NO
M.S KIM	W.Y YANG	G.S WEY	2035SCEZ
07.14.07	07.14.07	07.14.07	(HDMI-RX,TX)

AVR254

harman/kardon

CUP12035Z



REVISION	2	4	6
	3	5	7
SCHEMATIC DIAGRAM			
MODEL	AVR 255/355		
DESIGN	CHECK	APPROVE	DRAWING NO
M.S KIM	W.Y YANG	G.S WEY	2035SCEZ (TORINO)
07.14.07	07.14.07	07.14.07	

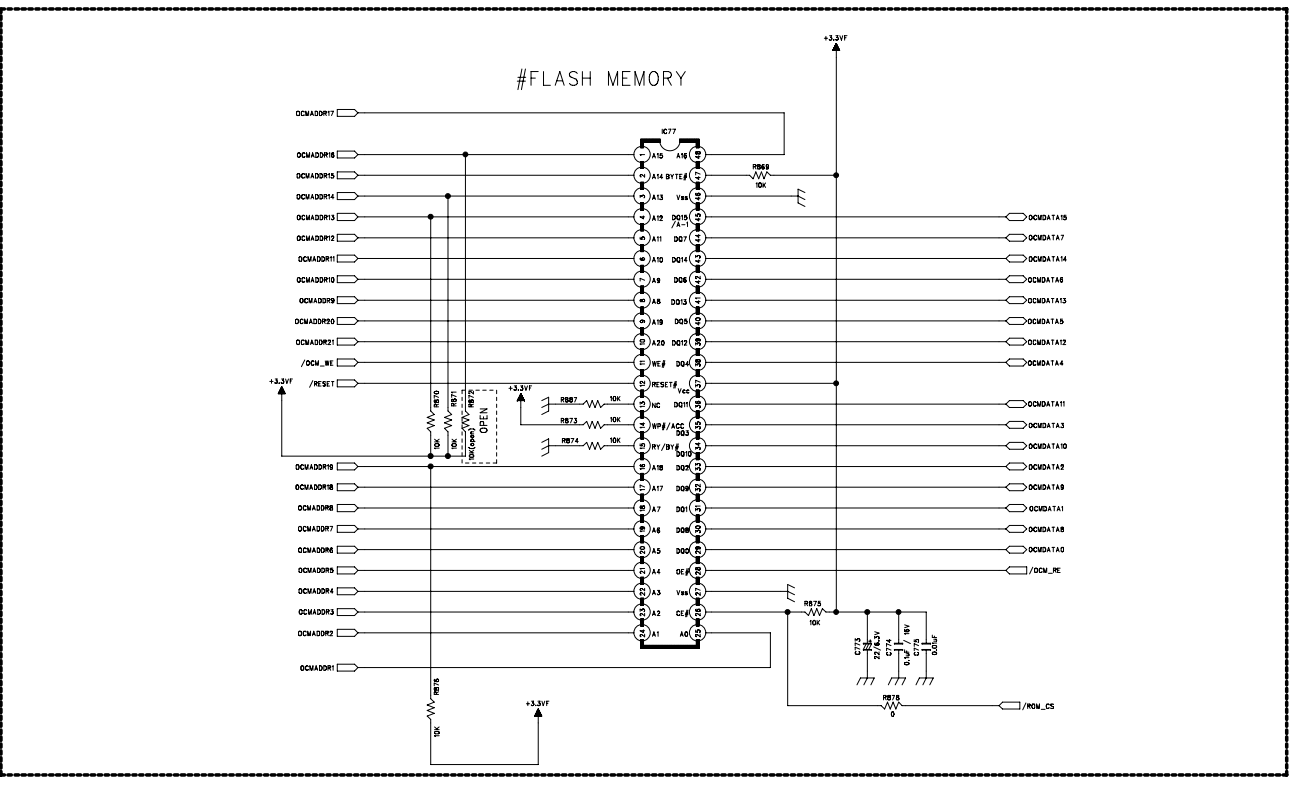
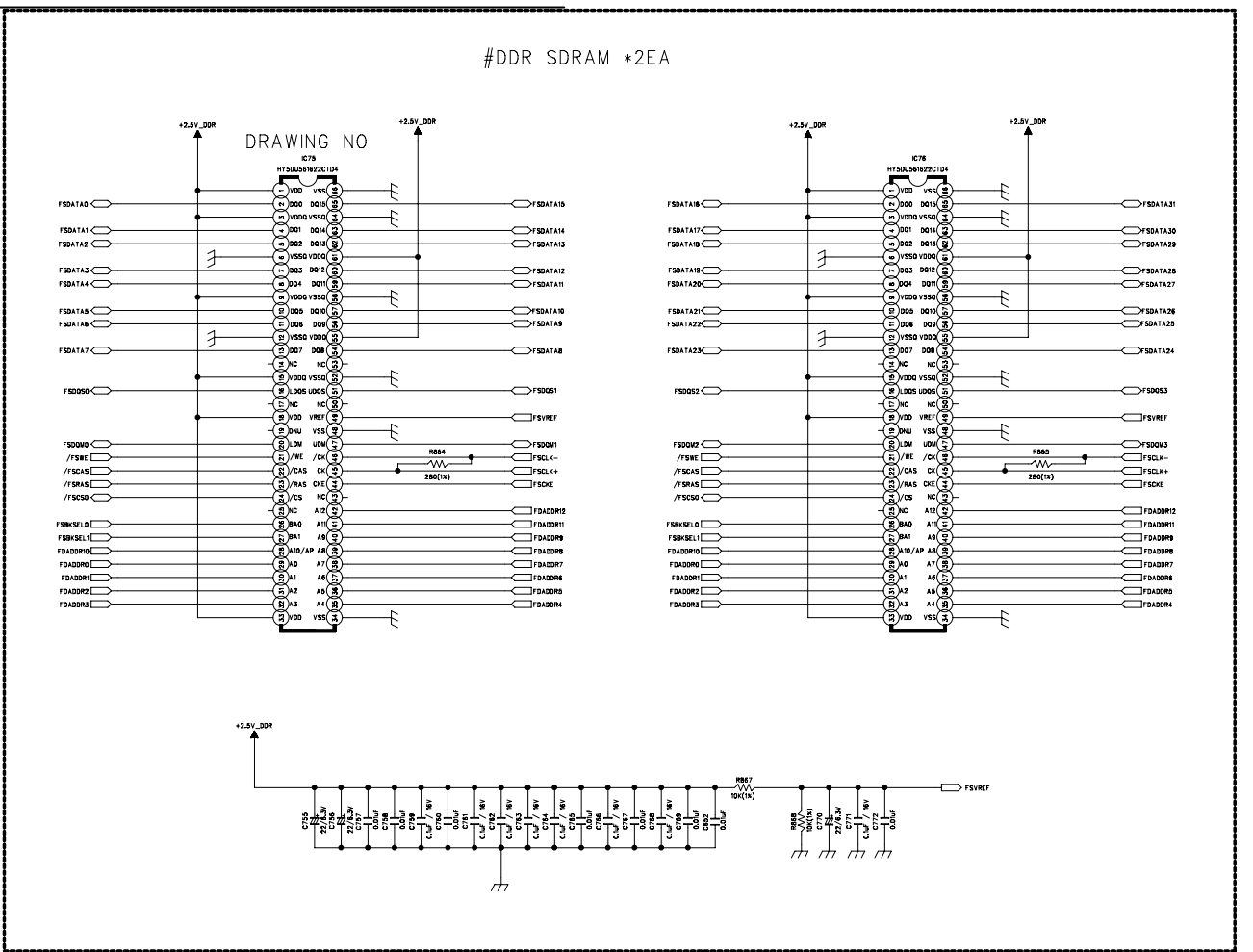
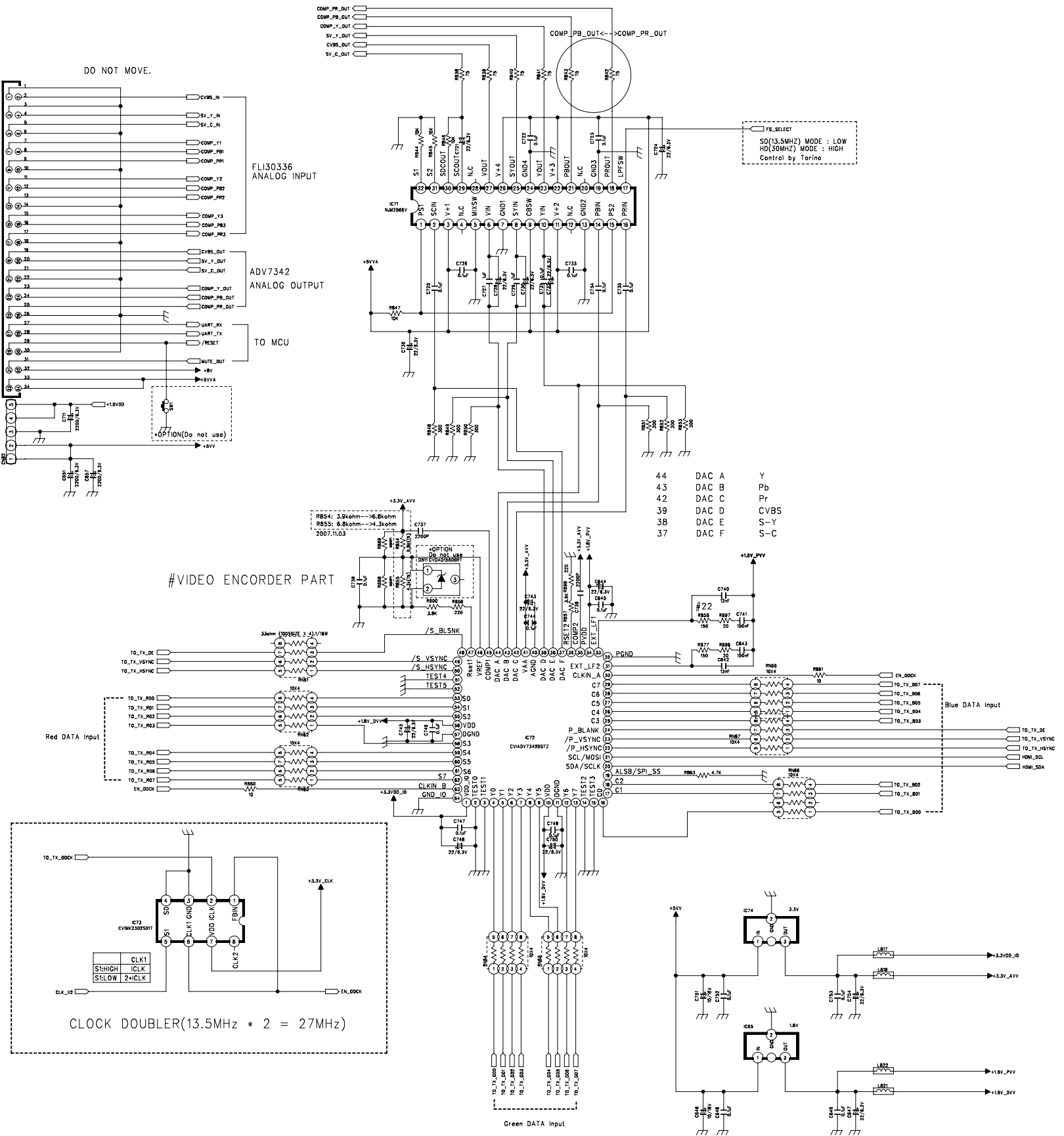
AVR254

CUP12035Z

harman/kardon

#DDR SDRAM \*2EA

#FLASH MEMORY

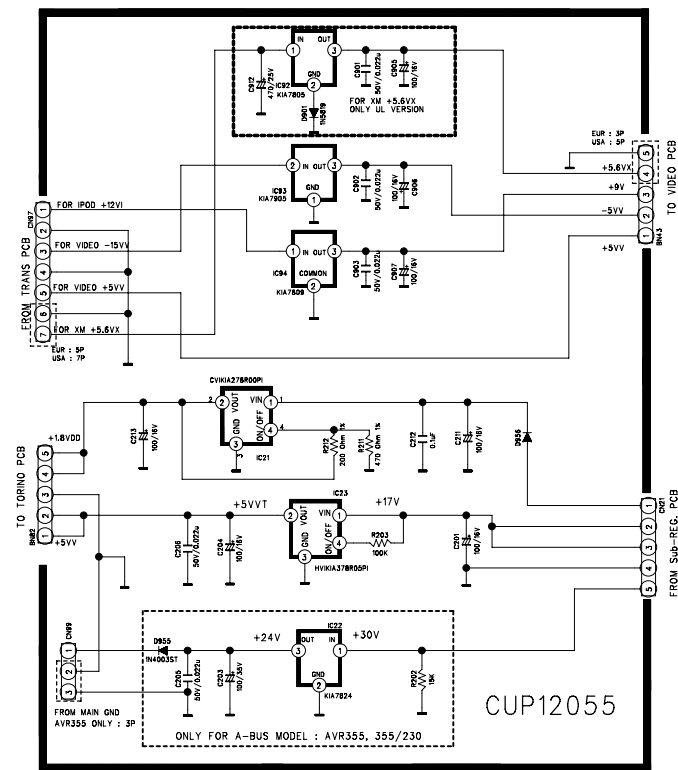


Legend for DAC outputs:

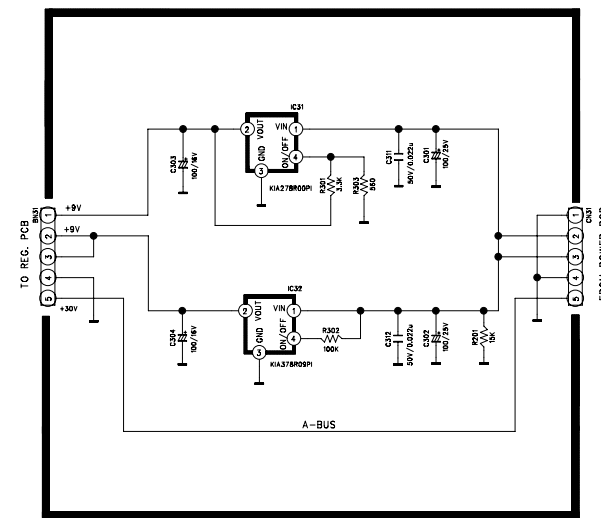
44	DAC A	Y
43	DAC B	Pb
42	DAC C	Pr
39	DAC D	CVBS
38	DAC E	S-Y
37	DAC F	S-C

REVISION	2	4	6
	3	5	7
SCHEMATIC DIAGRAM			
MODEL	AVR255/355		
DESIGN	CHECK	APPROVE	DRAWING NO
M.S KIM	W.Y YANG	G.S WEY	2035SCEZ
07.14.07	07.14.07	07.14.07	(ADV7342+MEM.)

< REGULATOR PCB >



< Sub-REGULATOR PCB >



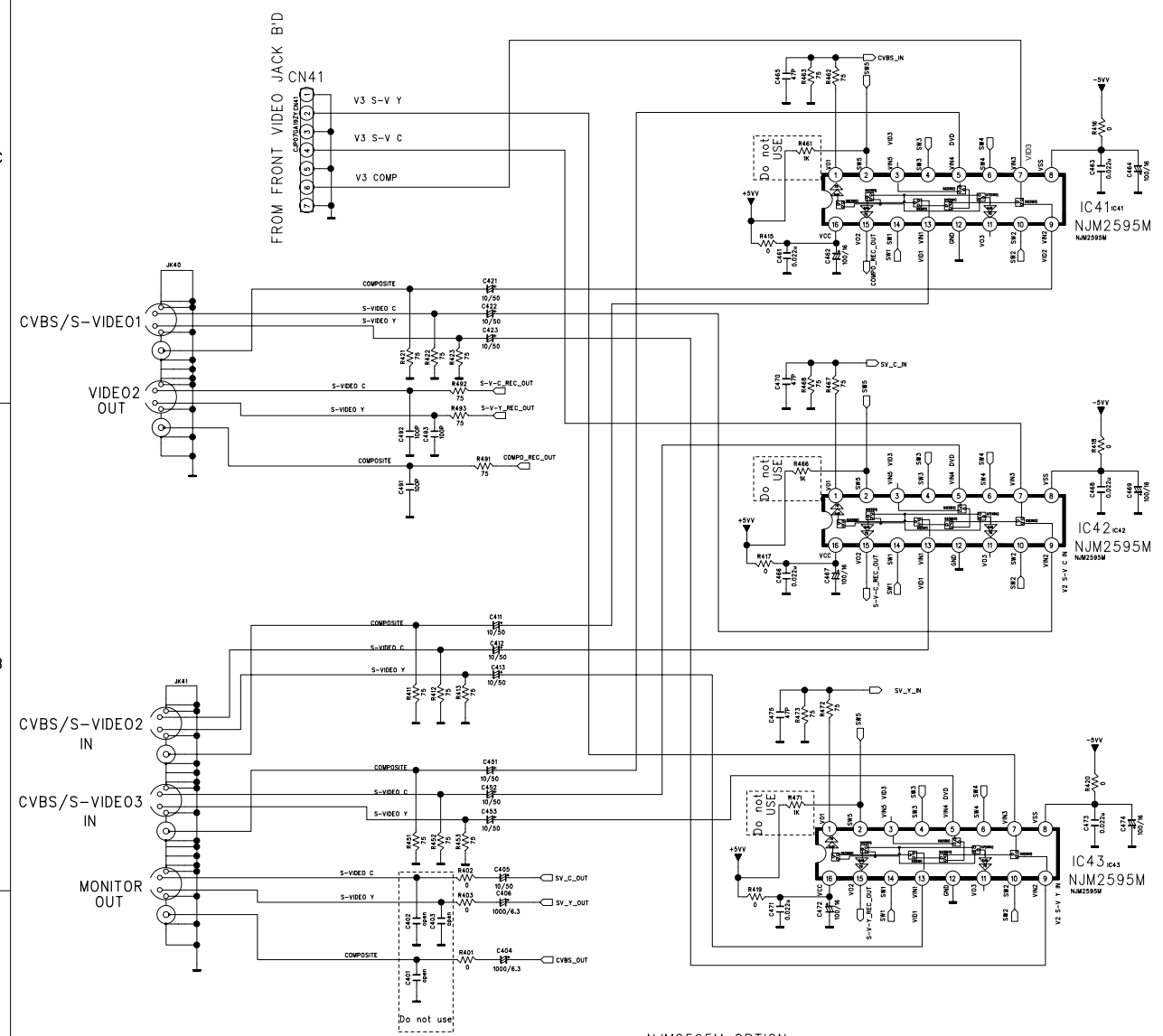
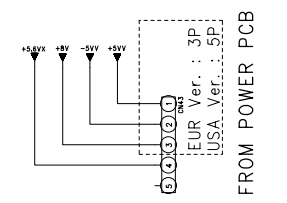
LPP

J. SUE

REVISION	2	4	6
1	3	5	7
SCHEMATIC DIAGRAM			
SHEET			
MODEL	AVR 254/255/354/355		
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.B	Y.Y.W	K.S.W	CUP12055Z
08.01.19			(REGULATOR)

AVR254 harman/kardon

CUP12032Z



• DEFINITION OF I2C REGISTER ( NJW1321 )

I2C BUS FORMAT

SENT	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB
(S)M(T)	(S)LA	(S)A(DD)M(T)	(D)A(DD)M(T)	(D)A(DD)M(T)	(D)A(DD)M(T)	(D)A(DD)M(T)	(D)A(DD)M(T)	(D)A(DD)M(T)

SLAVE ADDRESS

MSB	Slave Address(M/T)						MSB	Hex
1	0	0	0	0	0	0	ADR(M/T)	R/N(NT) R/W(M/T)

CONTROL REGISTER TABLE

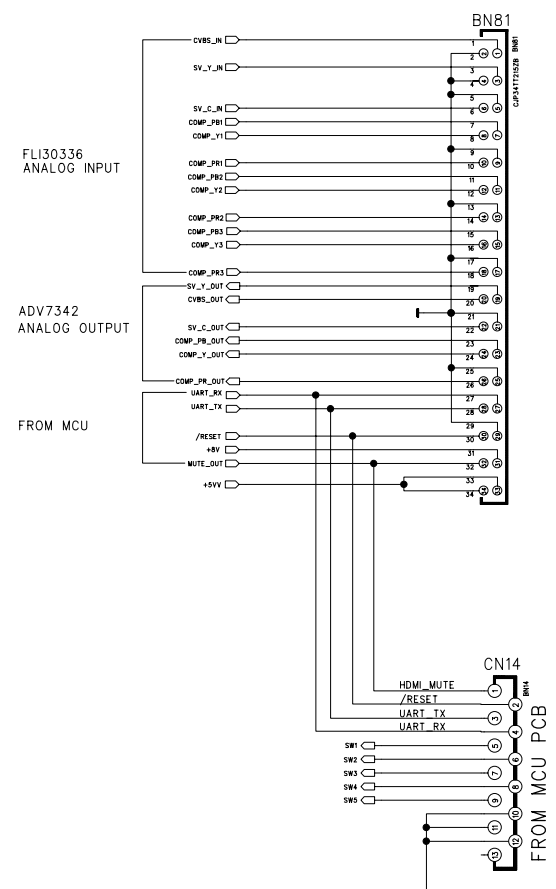
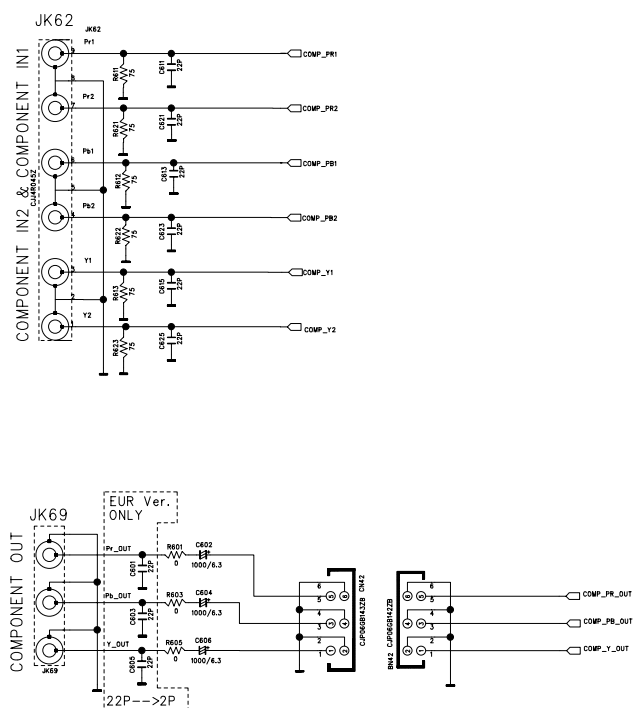
<WRITE MODE>

NO.	D7	D6	D5	D4	D3	D2	D1	D0
DATA 1	PS1	PS2	OUT1	OUT2	OUT2	OUT2	OUT2	OUT2
DATA 2	AUX0	AUX1	AUX2	AUX2	AUX2	AUX2	AUX2	AUX2

<READ MODE>

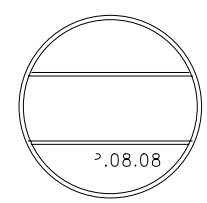
NO.	D7	D6	D5	D4	D3	D2	D1	D0
DATA	PORT0	PORT1	PORT2	PORT2	PORT2	PORT2	PORT2	PORT2

Legend: S: Starting Term, A: Acknowledge Bit, P: Ending Term, R/NOT R: Set the Write Mode or Read Mode, ADR: Set the Slave Address by "ADR" termOut, R/NOT R = 0: WRITE MODE, ADR = 0/1: ADR=0 Hex(40), ADR=1 Hex(40), R/NOT R = 0: READ MODE, ADR = 0/1: ADR=0 Hex(50), ADR=1 Hex(50), OUT: OUTPUT, AUX: AUXILIARY (CONTROL SIGNAL OUTPUT), PORT: INPUT



\*NJM2595M OPTION  
==>V\_MUTE "LOW" ACTIVE

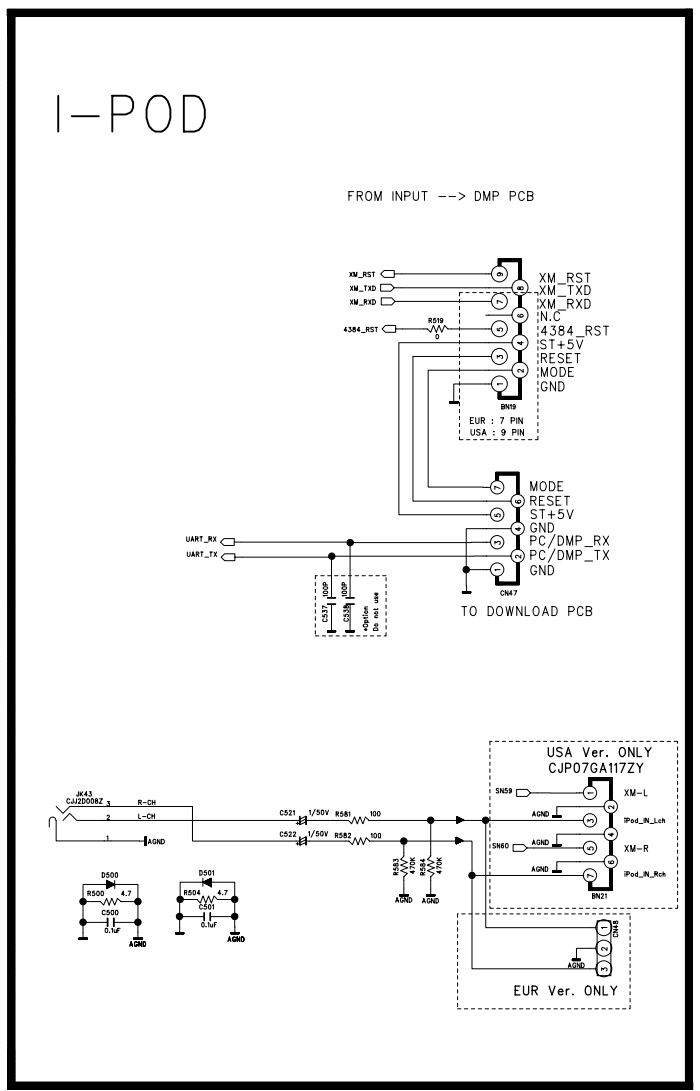
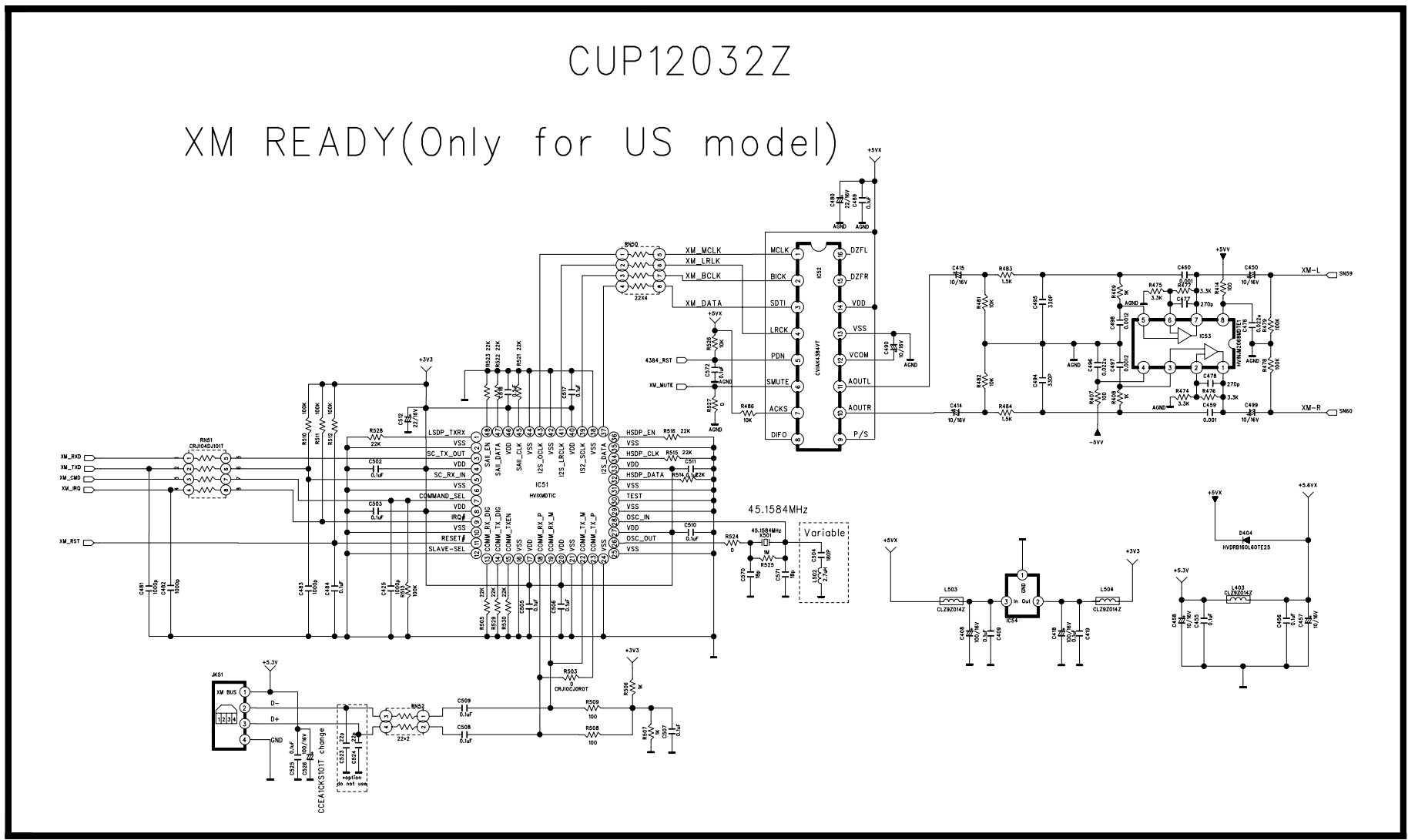
FUNC.	SW1	SW2	SW3	SW4	SW5
CVBS/S-V1	H	L	L	L	H
CVBS/S-V2	L	H	L	L	H
CVBS/S-V3	H	L	L	H	H
FRONT CVBS/S-V	H	H	L	L	H
IPOD	H	L	H	H	H



REVISION	2	4	6	
1	3	5	7	
SCHEMATIC DIAGRAM				SHEET
MODEL	AVR254 /255			1/2
DESIGN	CHECK	APPROVE	DRAWING NO	
M.S.K	W.Y.Y	K.S.W	2032SCEZ	
06.08.23	06.	06.	(VIDEO)	

AVR254

harman/kardon



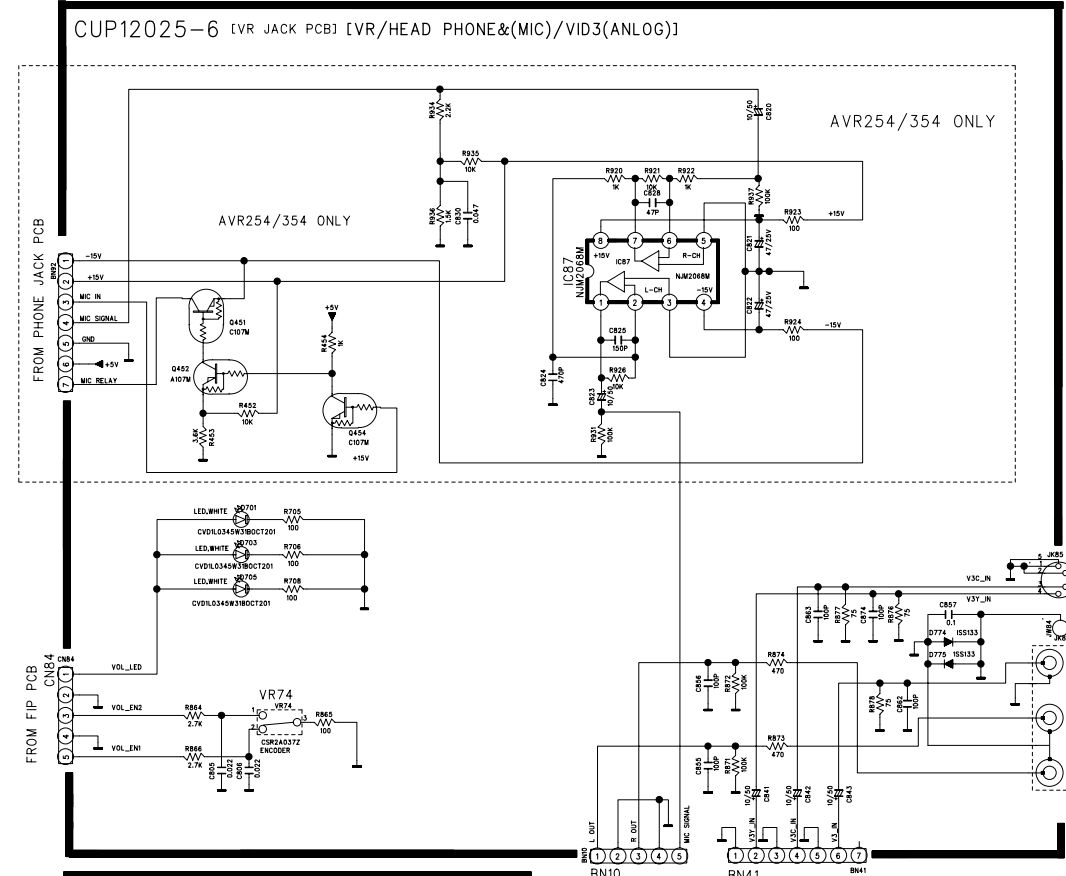
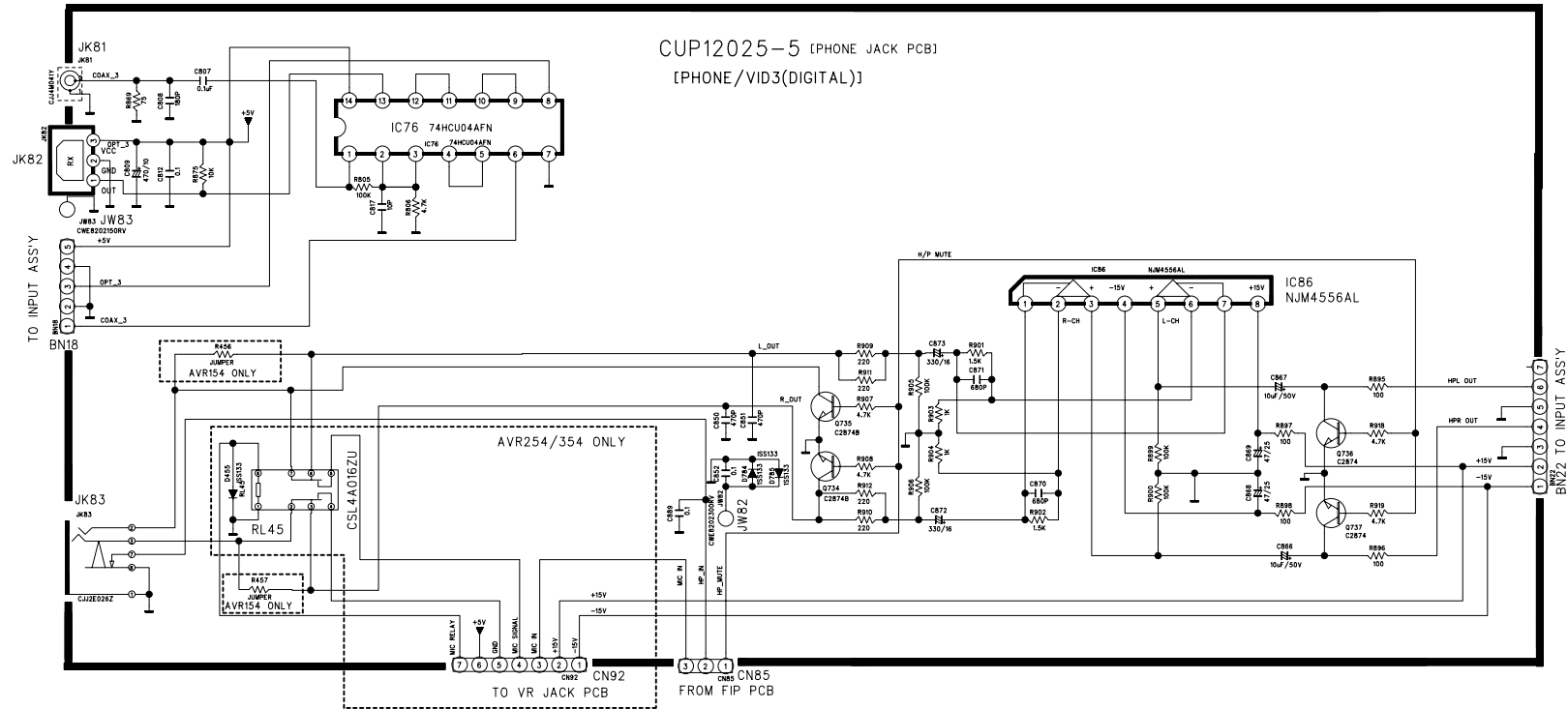
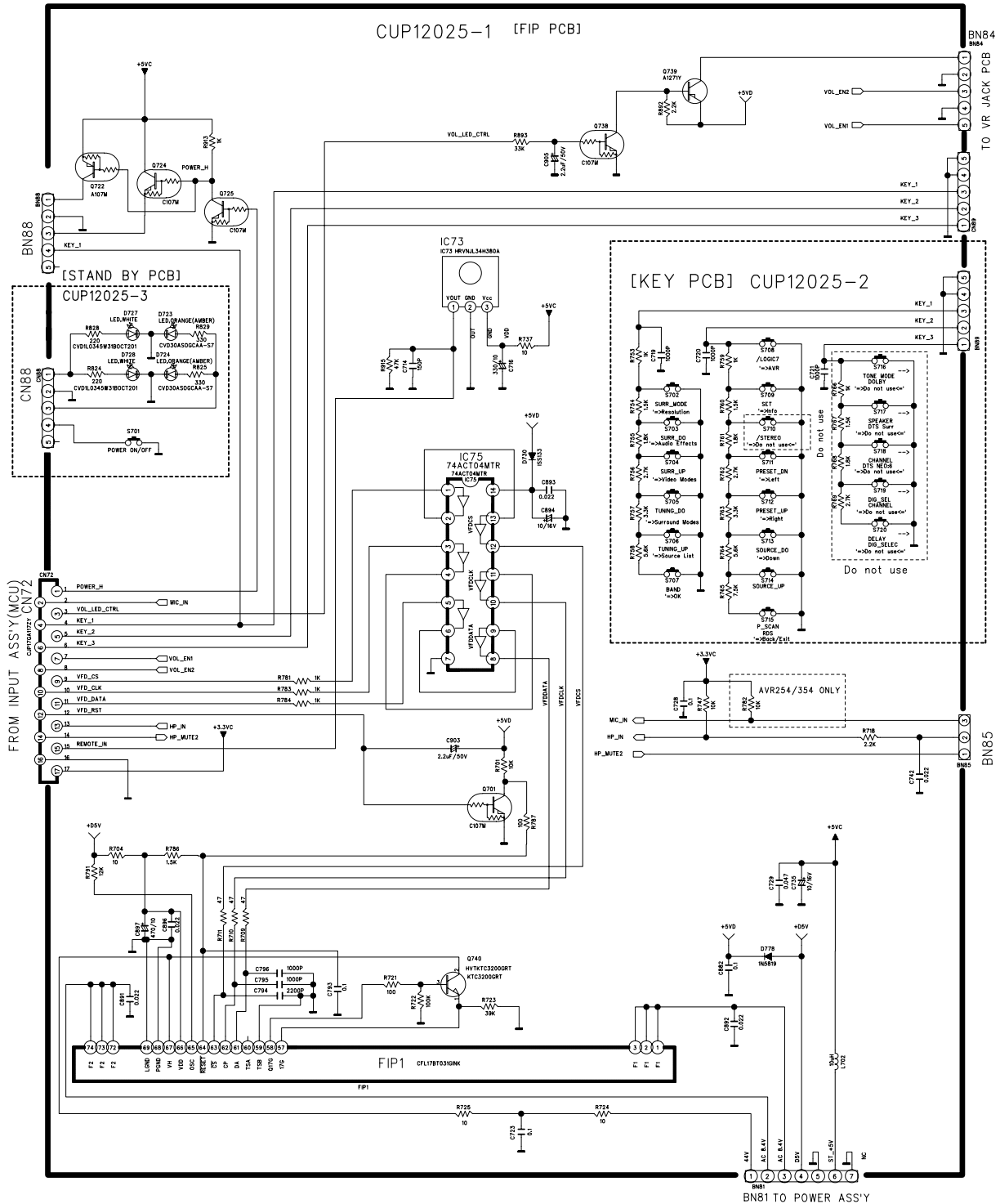
REVISION	2	4	6
1	3	5	7
SCHEMATIC DIAGRAM			SHEET
MODEL	AVR254 / 255		1 / 4
DESIGN	CHECK	APPROVE	DRAWING NO
M.S.K	W.Y.Y	K.S.W	2032SCEZ
05.00.00	05.00.00	05.00.00	(AMP)



AVR254

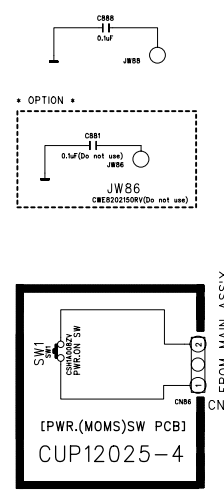
harman/kardon

CUP12025Z

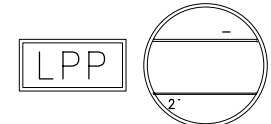


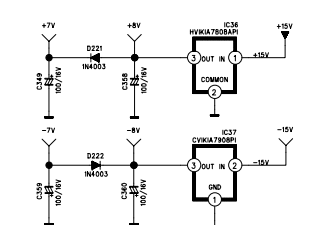
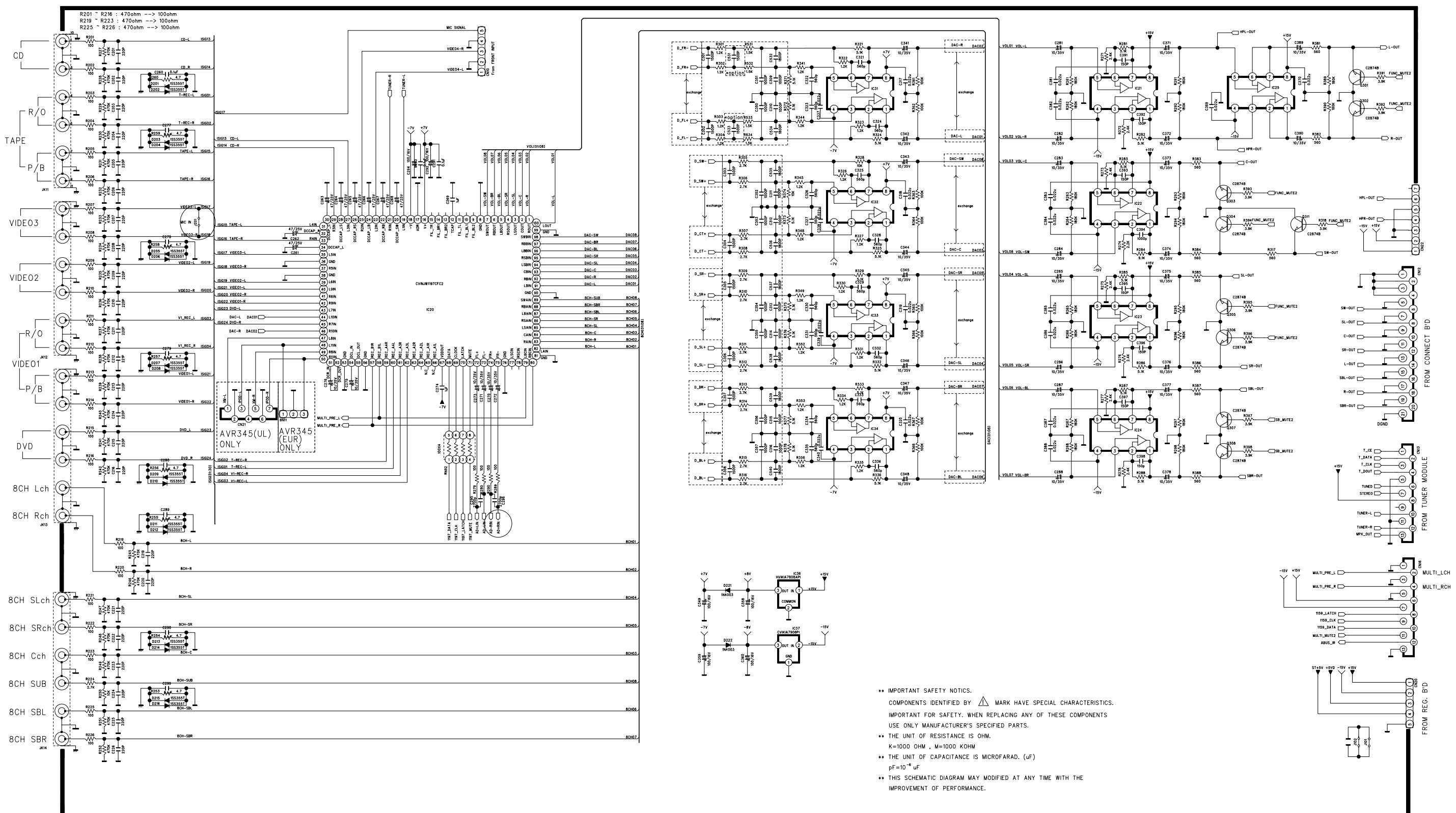
CUP12025-8 [BLACKET JACK PCB FOR CARD CABLE]

CUP12025-9 [BLACKET JACK PCB FOR PHONE JACK]



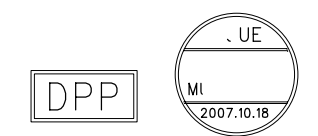
REVISION	2	4	6
1	3	5	7
SCHEMATIC DIAGRAM			
SHEET			
MODEL	AVR154/254/354		
DESIGN	CHECK	APPROVE	DRAWING NO
S.H.YANG	W.Y.YANG	G.S.WEY	2025SCDZ
07.12.07	07.12.07	07.12.07	(FRONT)





•• IMPORTANT SAFETY NOTICES.  
 COMPONENTS IDENTIFIED BY  $\Delta$  MARK HAVE SPECIAL CHARACTERISTICS.  
 IMPORTANT FOR SAFETY, WHEN REPLACING ANY OF THESE COMPONENTS  
 USE ONLY MANUFACTURER'S SPECIFIED PARTS.  
 •• THE UNIT OF RESISTANCE IS OHM.  
 K=1000 OHM , M=1000 KOHM  
 •• THE UNIT OF CAPACITANCE IS MICROFARAD. ( $\mu$ F)  
 $\mu$ F=10<sup>-6</sup> F  
 •• THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WITH THE  
 IMPROVEMENT OF PERFORMANCE.

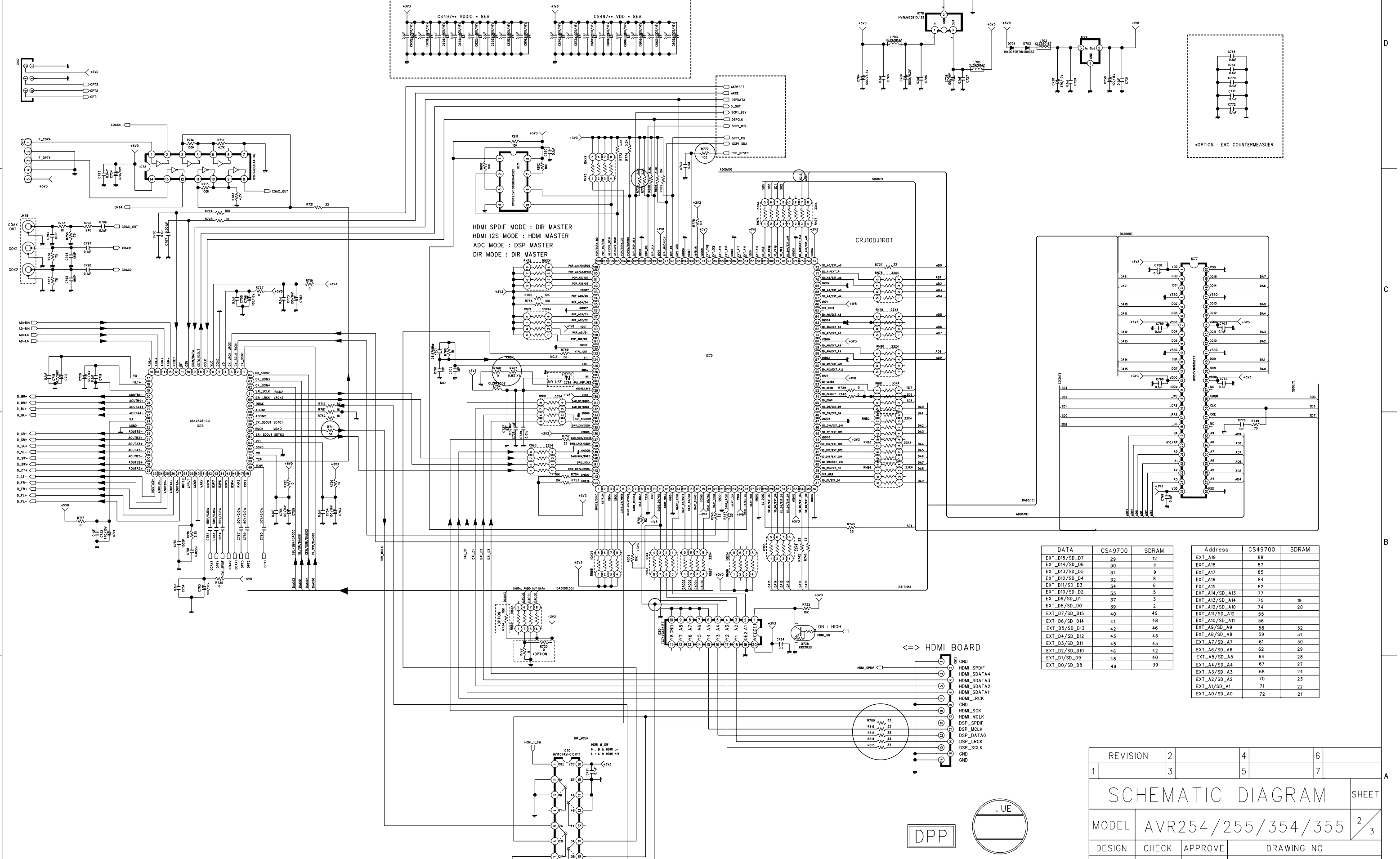
REVISION	2	4	6
1	3	5	7
SCHEMATIC DIAGRAM			
MODEL	AVR254/255/354/355		
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2029SCLZ
07.10.18			(INPUT)



AVR254

harman/kardon

CUP12029



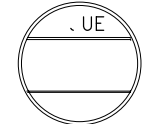
HDMI SPDIF MODE : DIR MASTER  
 HDMI I2S MODE : HDMI MASTER  
 ADC MODE : DSP MASTER  
 DIR MODE : DIR MASTER

DATA	CS49700	SDRAM
EXT_D15/SD_D7	29	12
EXT_D14/SD_D6	30	11
EXT_D13/SD_D5	31	9
EXT_D12/SD_D4	32	8
EXT_D11/SD_D3	34	6
EXT_D10/SD_D2	35	5
EXT_D9/SD_D1	37	3
EXT_D8/SD_D0	39	2
EXT_D7/SD_D15	40	49
EXT_D6/SD_D14	41	48
EXT_D5/SD_D13	42	46
EXT_D4/SD_D12	43	45
EXT_D3/SD_D11	45	43
EXT_D2/SD_D10	46	42
EXT_D1/SD_D9	48	40
EXT_D0/SD_D8	49	39

Address	CS49700	SDRAM
EXT_A19	89	
EXT_A18	87	
EXT_A17	85	
EXT_A16	84	
EXT_A15	82	
EXT_A14/SD_A13	77	
EXT_A13/SD_A14	75	19
EXT_A12/SD_A10	74	20
EXT_A11/SD_A12	55	
EXT_A10/SD_A11	56	
EXT_A9/SD_A9	58	32
EXT_A8/SD_A8	59	31
EXT_A7/SD_A7	62	30
EXT_A6/SD_A6	64	28
EXT_A5/SD_A5	64	28
EXT_A4/SD_A4	67	27
EXT_A3/SD_A3	68	24
EXT_A2/SD_A2	70	23
EXT_A1/SD_A1	71	22
EXT_A0/SD_A0	72	21

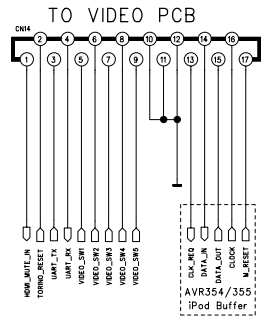
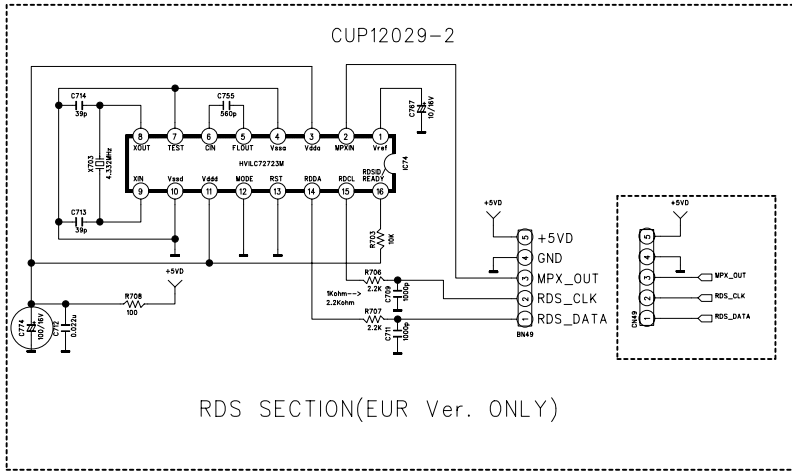
REVISION	2	4	6
	3	5	7
SCHEMATIC DIAGRAM			
MODEL	AVR254/255/354/355		SHEET 2/3
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2029SCLZ
07.10.18			(DSP)

DPP

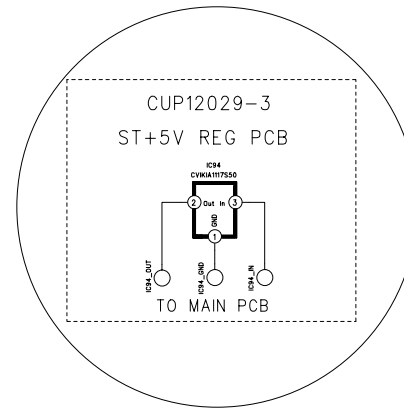


AVR254

harman/kardon

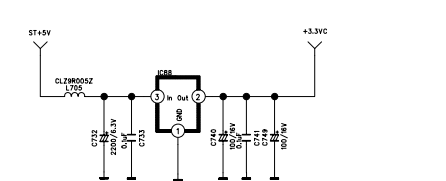
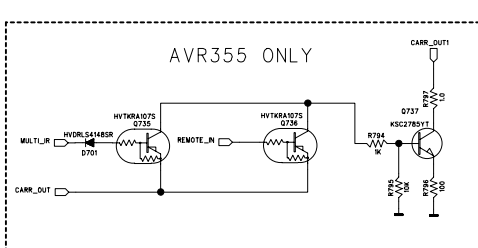
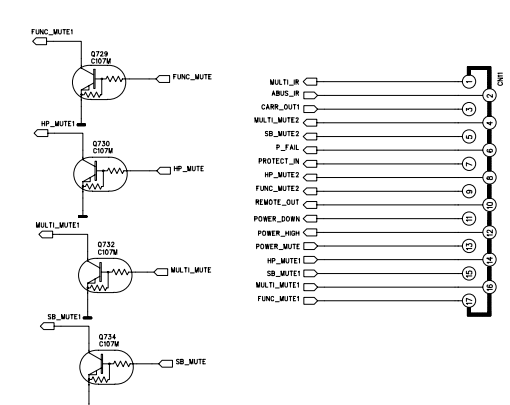
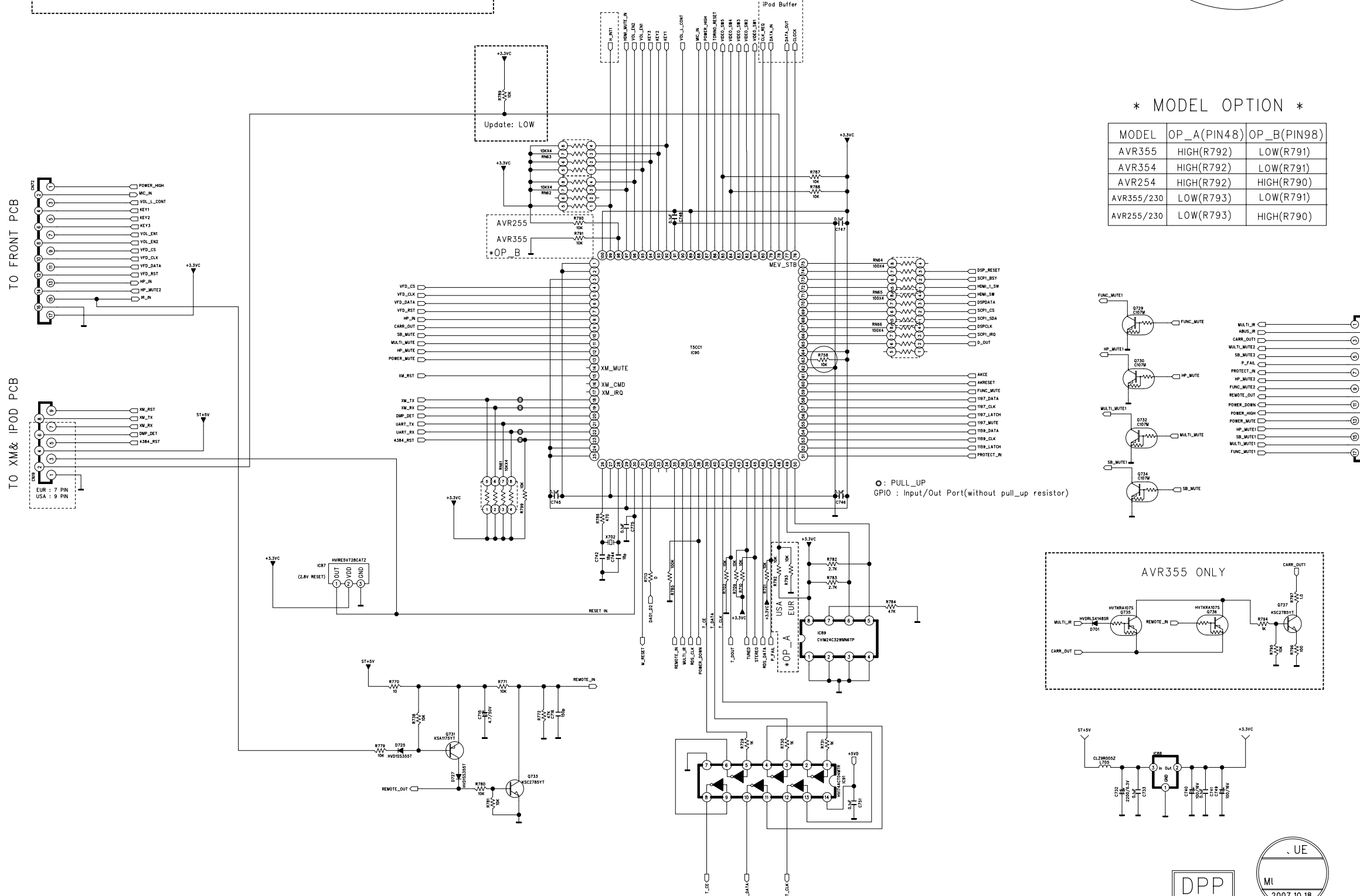


U-COM	AVR255	AVR355	AVR155
PIN 97	HDMI_MUTE_IN	HDMI_MUTE_IN	N.A
PIN 86	TORINO_RESET	TORINO_RESET	N.C
PIN 21	UART_TX(TORINO&PC)	UART_TX(TORINO&PC)	UART_TX(PC)
PIN 22	UART_RX(TORINO&PC)	UART_RX(TORINO&PC)	UART_RX(PC)
PIN 81	VIDEO_SW1	VIDEO_SW1	N.A
PIN 82	VIDEO_SW2	VIDEO_SW2	OSD_CS1
PIN 83	VIDEO_SW3	VIDEO_SW3	OSD_CLK
PIN 84	VIDEO_SW4	VIDEO_SW4	OSD_DA
PIN 85	VIDEO_SW5	VIDEO_SW5	OSD_M
PIN 80	CLOCK		HDMI_MUX_SDA
PIN 79	DATA_OUT		HDMI_MUX_SCLK
PIN 77	DATA_IN		OSD_H
PIN 76	CLK-REQ		

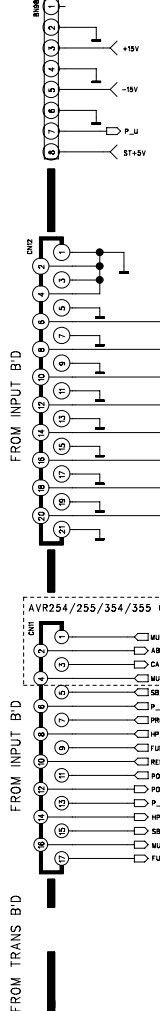
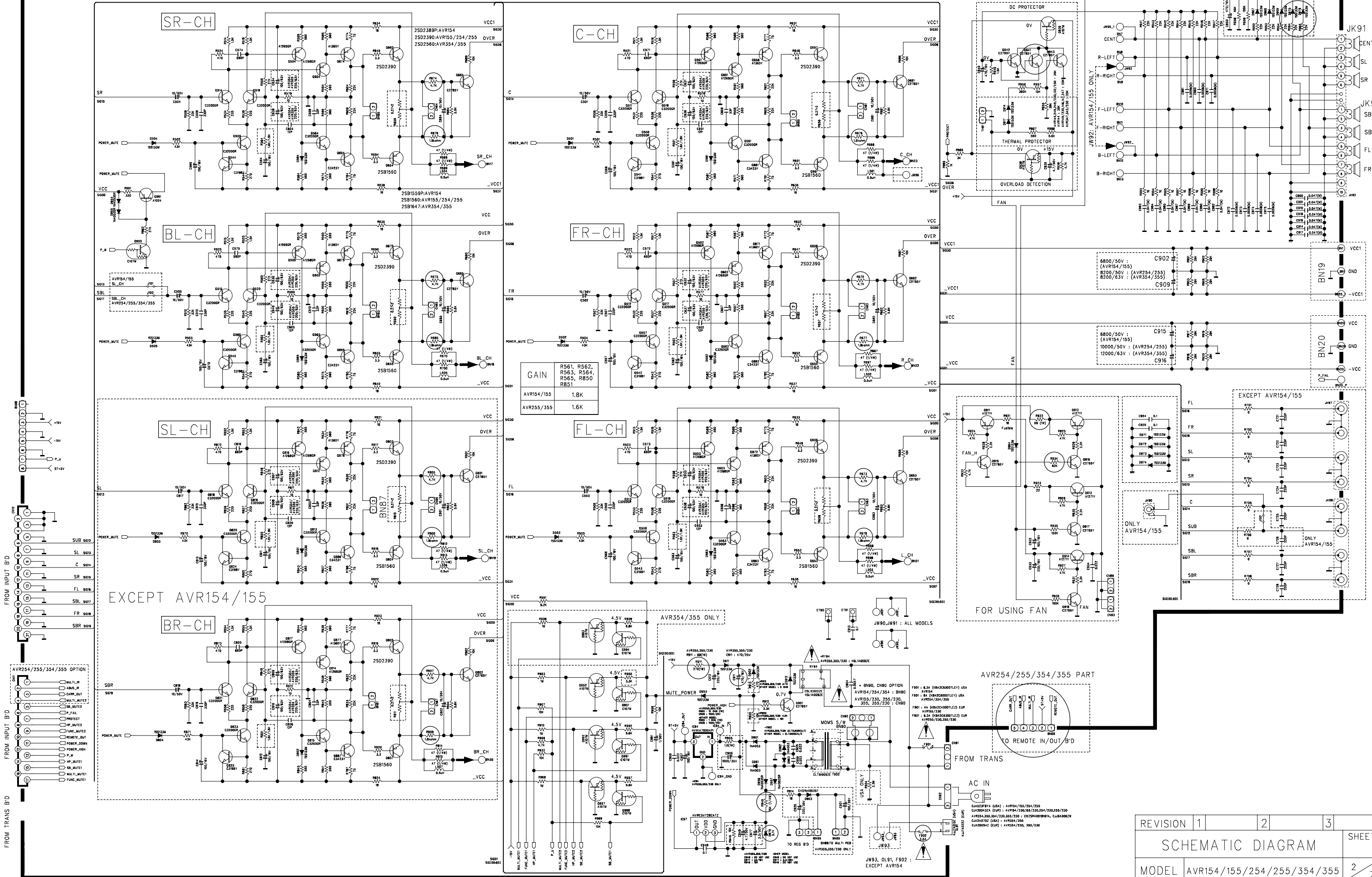


\* MODEL OPTION \*

MODEL	OP_A(PIN48)	OP_B(PIN98)
AVR355	HIGH(R792)	LOW(R791)
AVR354	HIGH(R792)	LOW(R791)
AVR254	HIGH(R792)	HIGH(R790)
AVR355/230	LOW(R793)	LOW(R791)
AVR255/230	LOW(R793)	HIGH(R790)



REVISION	2	4	6
	3	5	7
SCHEMATIC DIAGRAM			
MODEL	AVR254/255/354/355		SHEET 3/3
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2029SCLZ
07.10.18			(CPU)



EXCEPT AVR154/155

AVR354/355 ONLY

FOR USING FAN

ONLY AVR154/155

EXCEPT AVR154/155

ONLY AVR154/155

AVR254/255/354/355 PART

TO REMOTE IN/OUT B/D

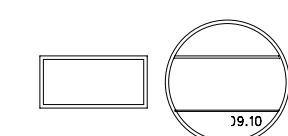
FROM TRANS

AC IN

TO REG B/D

EXCEPT AVR154

•• IMPORTANT SAFETY NOTICE.  
 IMPORTANT FOR SAFETY WHEN REPLACING ANY OF THESE COMPONENTS  
 USE ONLY MANUFACTURE'S SPECIFIED PARTS.  
 •• THE UNIT OF RESISTANCE IS OHM.  
 K=1000 OHM, M=1000 KOHM,  
 •• THE UNIT OF CAPACITANCE IS MICROFARAD (UF)  
 pF = 10<sup>-6</sup> UF  
 •• THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WITH THE  
 IMPROVEMENT OF PERFORMANCE

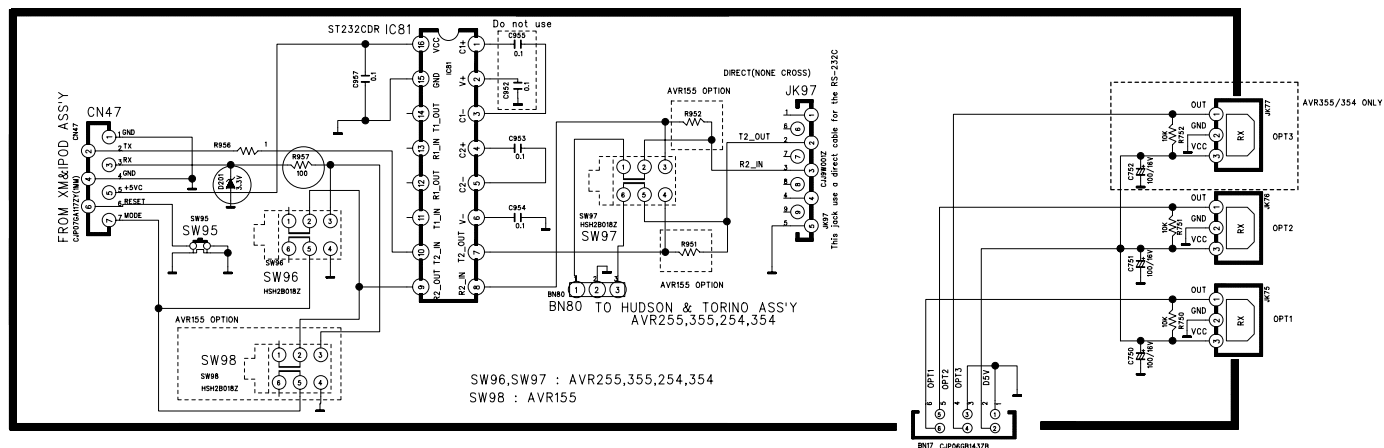


REVISION	1	2	3	SHEET
SCHEMATIC DIAGRAM				2
MODEL	AVR154/155/254/255/354/355			7
DESIGN	CHECK	APPROVE	DRAWING NO	
C.B.LEE	W.Y.YANG	G.S.WEY	2026SCLZ	
07.08.23				(MAIN)

### AVR254

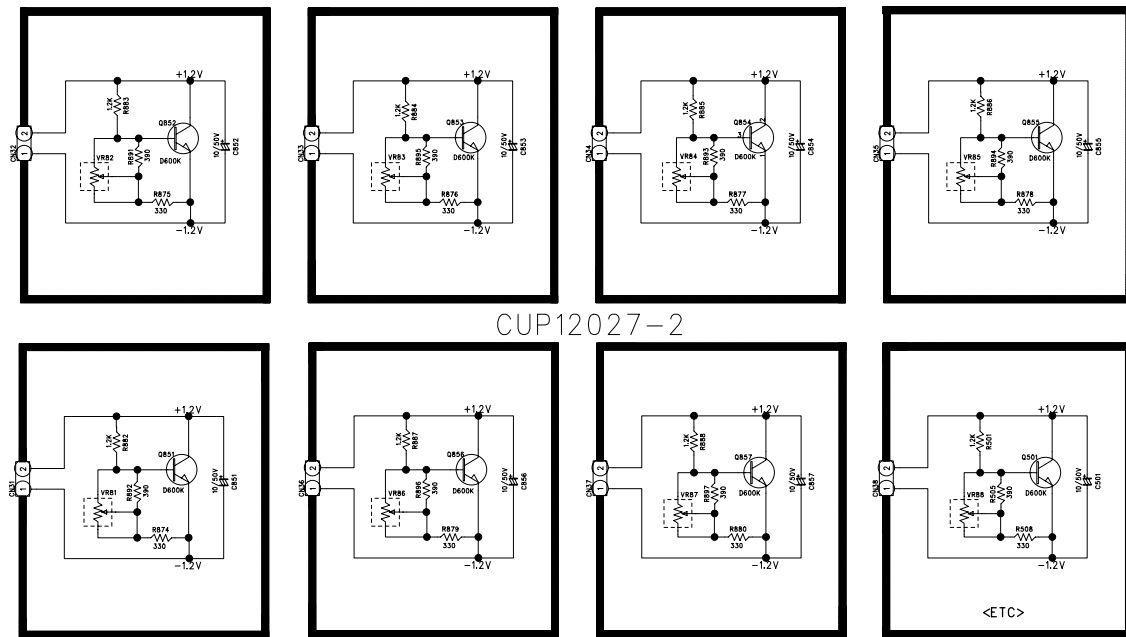
harman/kardon

#### CUP12027-1



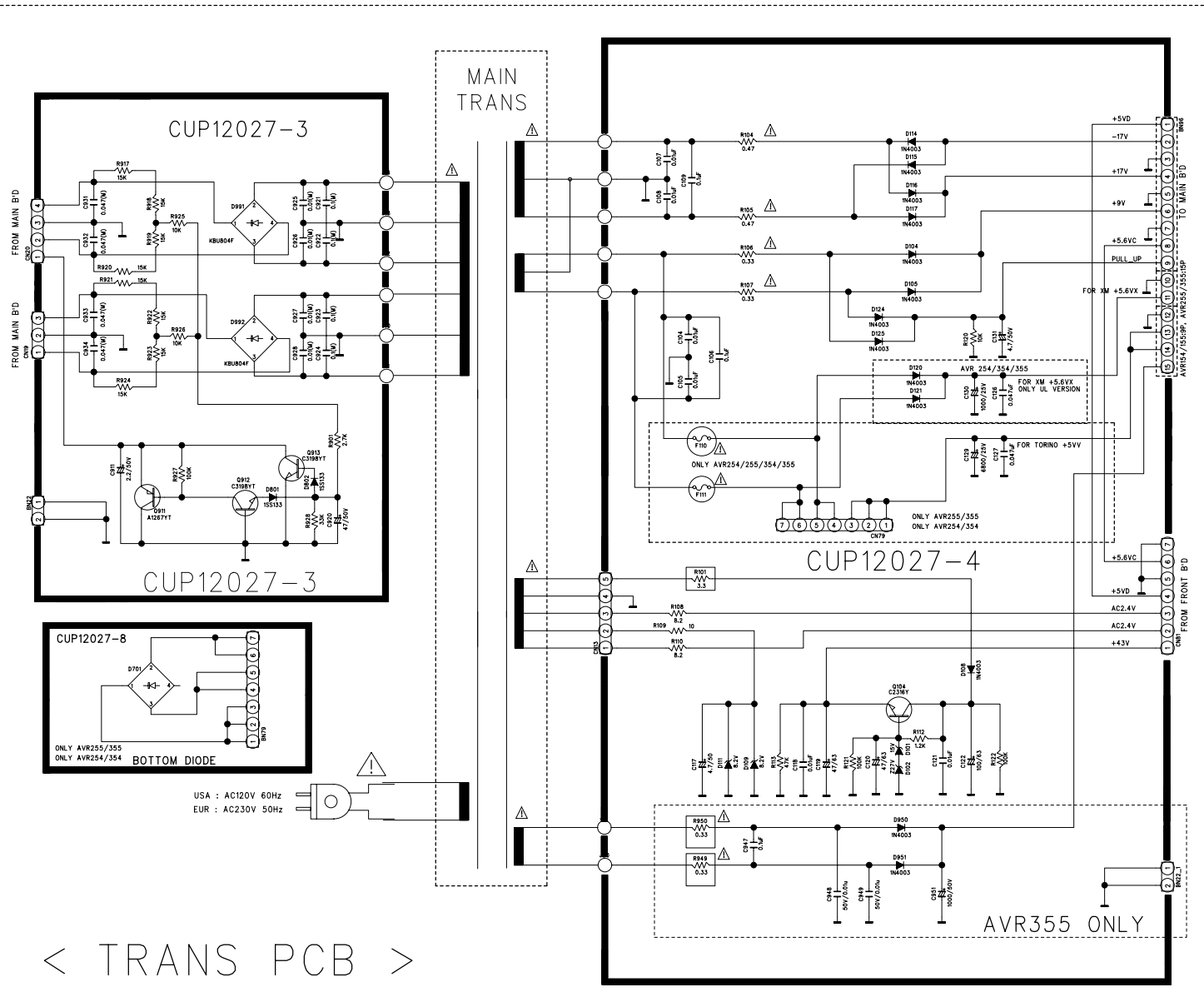
#### < OPTICAL IN & RS-232 PCB >

#### < BIAS T.R PCB >

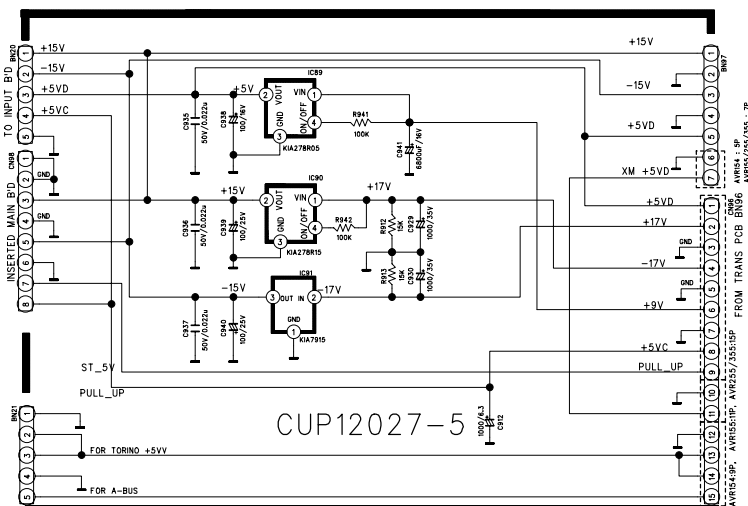


#### CUP12027-2

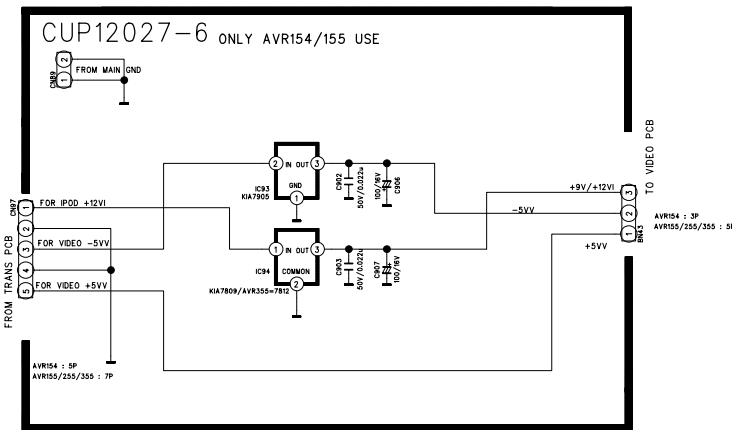
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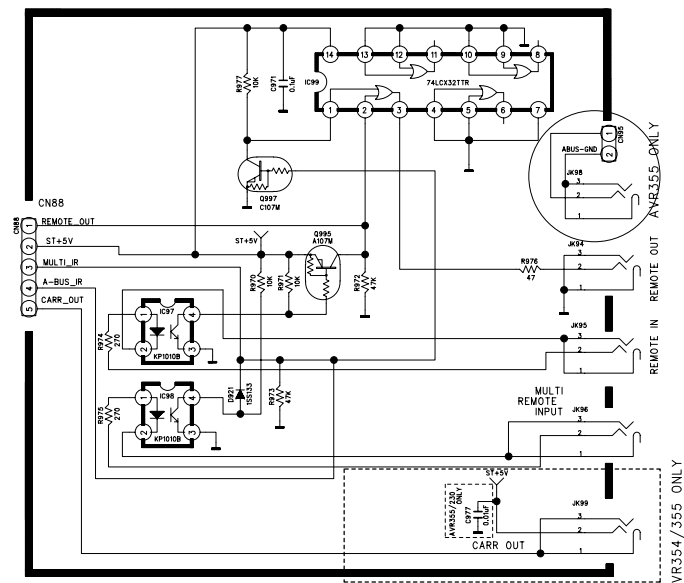
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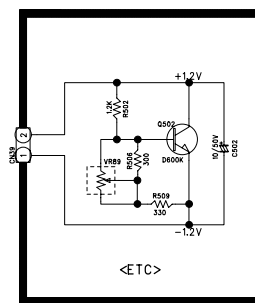
#### CUP12027-5



#### < REGULATOR PCB >



#### AVR254/255/354/355 ONLY CUP12027-7 < REMOTE IN/OUT PCB >



M P

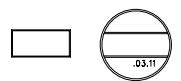
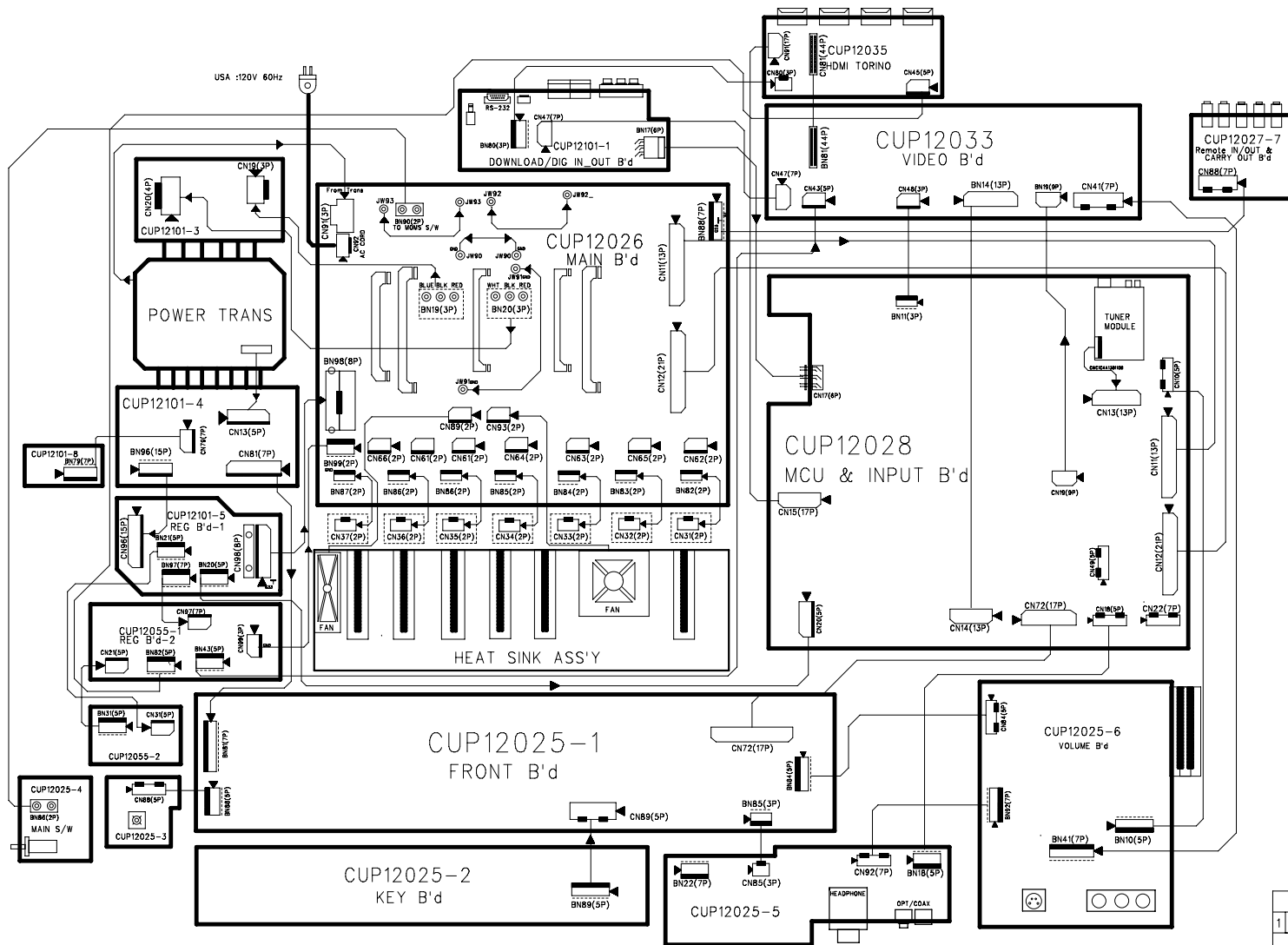
SUE  
2008.01.27

REVISION	2	4	6
1	3	5	7
SCHEMATIC DIAGRAM			
MODEL	AVR x54/x55		
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.B	Y.Y.W	K.S.W	CUP12027Z
08.01.22			(POWER)

AVR254

harman/kardon

# AVR254 WIRING DIAGRAM



REVISION	2	4	6
1	3	5	7
SCHEMATIC DIAGRAM			
MODEL	AVR254		
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.B	W.Y.Y	K.S.W	WIRING DIAGRAM
08.03.11	08.03.11	08.03.11	1190SCDZ