Zentel

A3S56D30FTP
A3S56D40FTP

256M Double Data Rate Synchronous DRAM

PIN FUNCTION

SYMBOL	TYPE	DESCRIPTION
CLK, /CLK	Input	Clock: CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK. Output (read) data is referenced to the crossings of CLK and /CLK (both directions of crossing).
CKE	Input	Clock Enable: CKE controls Power Down and Self Refresh. Taking CKE LOW provides Precharge Power Down or Self Refresh (all banks idle), or Active Power Down (row active in any bank). Taking CKE HIGH provides Power Down exit or Self Refresh exit. After Self Refresh is started, CKE becomes asynchronous input. Power Down and Self Refresh is maintained as long as CKE is LOW.
/CS	Input	Chip Select: When /CS is HIGH, any command means No Operation.
/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
A0-12	Input	A0-12 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-12. The Column Address is specified by A0-9(x8) and A0-8(x16). A10 is also used to indicate precharge option. When A10 is HIGH at a Read / Write command, an Auto Precharge is performed. When A10 is HIGH at a Precharge command, all banks are precharged.
BA0,1	Input	Bank Address: BA0,1 specifies one of four banks to which a command is applied. BA0,1 must be set with Active, Precharge, Read, Write commands.
DQ0-7 (x8), DQ0-15 (x16),	Input / Output	Data Input/Output: Data bus
DQS (x8) UDQS, LDQS (x16)	Input / Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS correspond to the data on DQ8-DQ15
DM (x8) UDM, LDM (x16)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-DQ7; UDM corresponds to the data on DQ8-DQ15.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
VddQ, VssQ	Power Supply	VddQ and VssQ are supplied to DQ, DQS buffers.
VREF	Input	SSTL_2 reference voltage.

12-Bit, 170 MHz Video and Graphics Digitizer with 3D Comb Filter Decoder and Quad HDMI 1.4 Fast Switching Receiver

PRELIMINARY

ADV7844

FEATURES

Quad HDMI 1.4 Fast Switching Receiver
170 MHz Video and Graphics Digitizer
3D Comb Filter Video Decoder
SCART Fast Blank Support
Adaptive HDMI Equaliser
Integrated CEC Controller
HDMI Repeater Support
Advanced VBI data slicer

Video and Graphics Digitizer
- **Four 170 MHz, 12-bit ADCs,**
- **12-channel analog input mux**
- **525i-/625i-component analog input**
- **525p-/625p-component progressive scan support**
- **720p-/1080i-/1080p-component HDTV support**
- **Low refresh rates (24/25/30 Hz) support for 720p/1080p**
- **Digitizes RGB graphics up to 1600 × 1200 at 60 Hz (UXGA)**

3D Video Decoder
- **NTSC/PAL/SECAM color standards support**
- **NTSC/PAL 2D/3D motion detecting comb filter**
- **Advanced time-base correction (TBC) with frame synchronization**
- **Interlaced-to-progressive conversion for 525i and 625i**
- **IF compensation filters**
- **Vertical peaking and horizontal peaking filters**
- **Robust synchronization extraction for poor video source**

4:1 HDMI 1.4 225 MHz Receiver
- ***Fast-Switching* of HDMI ports**
- **2:2 HEAC muxing support**
  - **2 HEAC channel support**
  - **2 Ethernet Interfaces for HEC Support**
  - **SPDIF interface for ARC support.**
- **3D Video format support including frame packing 1080p 24Hz, 720p 50 Hz, 720p 60Hz**
- **Full colorimetry support including sYCC601, Adobe RGB, Adobe YCC 601**
- **36-/30-bit Deep Color and 24-bit color support**
- **HDCP 1.3 support with internal HDCP Keys**
- **+5V Detect and Hot plug assert for each HDMI port**
- **Full HDMI Audio Support including HBR, DSD, DST**
- **Advanced Audio mute feature**
- **Flexible digital audio output interfaces**
- **Supports up to 5 SPDIF outputs,**
- **Supports up to 4 I2S outputs**

General
- **Highly flexible 36-bit pixel output interface**
- **Internal EDID RAM for HDMI and graphics**
- **Dual STDI (standard identification) function support**
- **Any-to-any, 3 × 3 color space conversion (CSC) matrix**
- **2 programmable interrupt request output pins**
- **Simultaneous analog processing and HDMI monitoring**

APPLICATIONS

Advanced TVs
- **PDP HDTVs**
- **LCD TVs (HDTV ready)**
- **LCD/DLP® rear projection HDTVs**
- **CRT HDTVs**
- **LCoS™ HDTVs**

AVR video receivers
LCD/DLP front projectors
HDTV STBs with PVR
Projectors

FUNCTIONAL BLOCK DIAGRAM

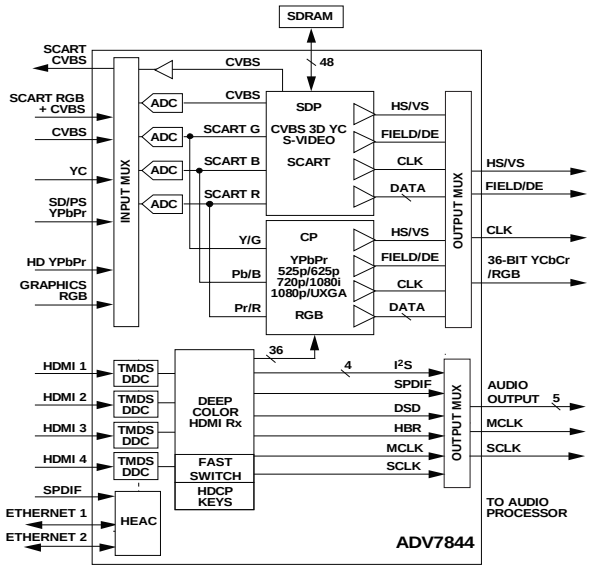


Figure 1.

Advantiv® Advanced Television Solutions by Analog Devices | NSV® Precision Video by Analog Devices

ADV7844

PRELIMINARY

DETAILED FUNCTIONAL BLOCK DIAGRAM

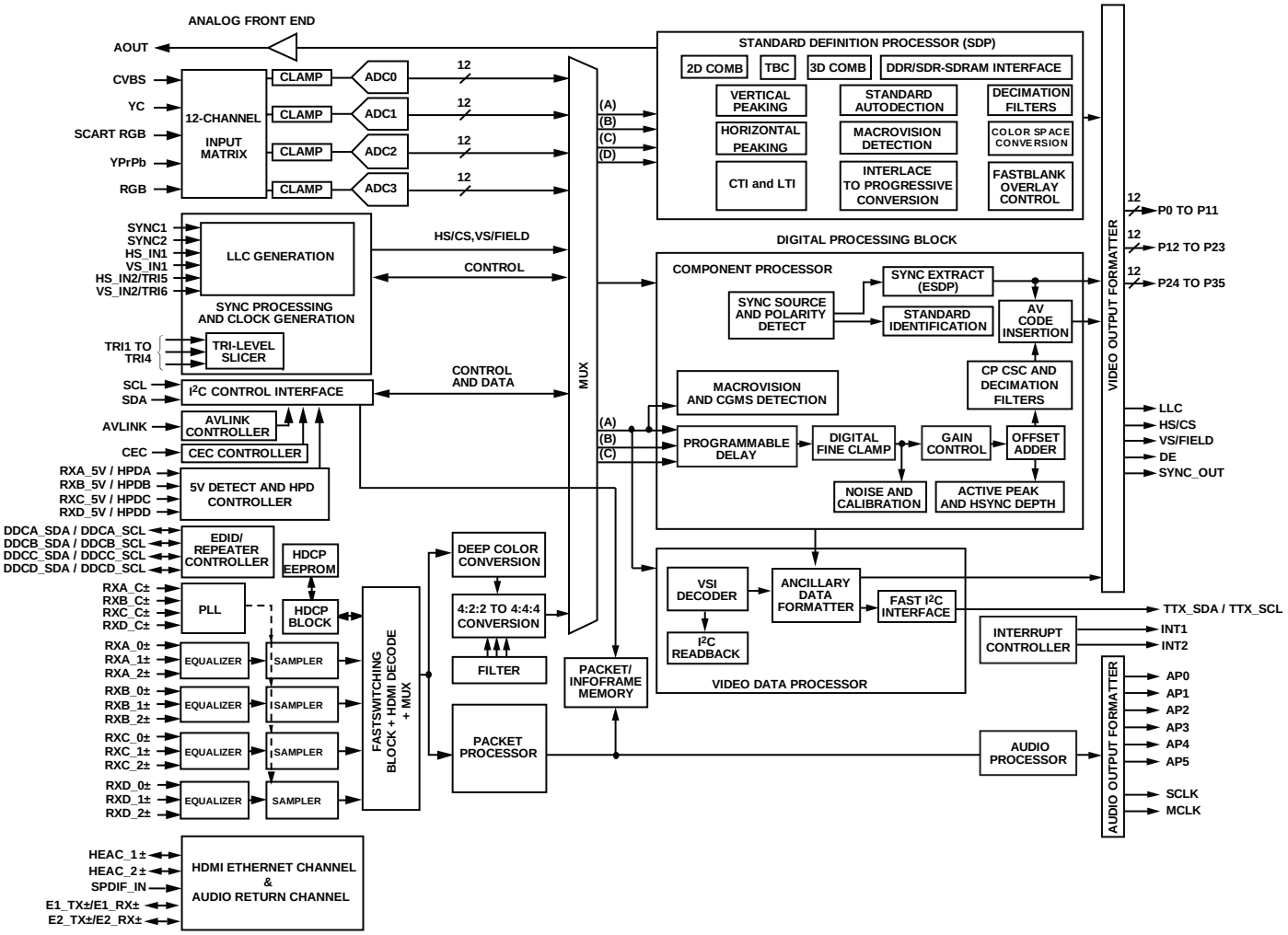


Figure 2. Detailed Functional Block Diagram

ADV7844

PRELIMINARY

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	VS/FIELD	E2_TX+	E2_RX+	TVDD	RXD_2-	RXD_1-	RXD_0-	RXD_C-	HEAC_2-	TVDD	RXC_2-	RXC_1-	RXC_0-	RXC_C-	NC	TVDD	RXB_2-	RXB_1-	RXB_0-	RXB_C-	HEAC_1-	GND	A
B	HS/CS	FIELD/DE	E2_TX-	E2_RX-	TVDD	RXD_2+	RXD_1+	RXD_0+	RXD_C+	HEAC_2+	TVDD	RXC_2+	RXC_1+	RXC_0+	RXC_C+	NC	TVDD	RXB_2+	RXB_1+	RXB_0+	RXB_C+	HEAC_1+	GND	B
C	P0	P1	E1_TX+	E1_RX+	TVDD	PWRDN1	PWRDN2	HPA_D	RXD_5V	RXC_5V	TVDD	GND	GND	GND	GND	GND	GND	TVDD	TVDD	TVDD	TVDD	TVDD	TVDD	C
D	P2	P3	E1_TX-	E1_RX-	TVDD	SYNC_OUT	CEC	HPA_C	RXB_5V	HPA_B	TVDD	RXA_5V	HPA_A	DDCD_SDA	DDCD_SCL	DDCC_SDA	DDCC_SCL	RTERM	DDCB_SDA	DDCB_SCL	TVDD	RXA_2+	RXA_2-	D
E	DVDDIO	DVDDIO	GND	GND																DDCA_SDA	CVDD	RXA_1+	RXA_1-	E
F	P5	P4	EP_MISO	EP_MOSI																DDCA_SCL	CVDD	RXA_0+	RXA_0-	F
G	P7	P6	EP_CS	EP_SCK			GND	GND	GND	GND	TEST1	TEST2	GND	GND	CVDD	CVDD	CVDD			VGA_SCL	CVDD	RXA_C+	RXA_C-	G
H	P9	P8	TTX_SDA	TTX_SCL			GND	GND	GND	GND	GND	GND	GND	GND	CVDD	CVDD	CVDD			VGA_SDA	CVDD	NC	NC	H
J	P11	P10	MCLK	AP0			GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			PVDD	TEST3	GND	GND	J
K	P13	P12	AP5	SCLK			VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			PVDD	GND	XTALN	XTALP	K
L	DVDDIO	DVDDIO	GND	GND			VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND	GND	GND	GND	L
M	P15	P14	AP4	AP3			VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND	GND	REFN	REFP	M
N	P17	P16	AP2	AP1			VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			AVDD	AVDD	AVDD	AVDD	N
P	P18	P19	SCL	SDA			VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			AVDD	AVDD	AIN11	AIN12	P
R	P20	P21	TEST4	INT1			VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			HS_IN2/TRI7	VS_IN2/TRI8	SYNC4	AIN10	R
T	P22	P23	TEST5	INT2			VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			GND	GND	GND	GND	T
U	DVDDIO	DVDDIO	DVDDIO	DVDDIO			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	GND	GND	GND			TRI4	TRI3	AIN9	AIN8	U
V	LLC	P24	RESET	AVLINK																TRI1	TRI2	SYNC3	AIN7	V
W	P25	P26	NC	SPDIF_IN																AVDD	AVDD	AVDD	AVDD	W
Y	P27	P28	GND	GND	GND	VDD_SDRAM	SDRAM_A11	SDRAM_A6	SDRAM_A2	SDRAM_CS	SDRAM_LDQS	GND	SDRAM_DQ6	SDRAM_DQ2	SDRAM_DQ15	SDRAM_DQ11	SDRAM_CKE	VDD_SDRAM	GND	AOUT	NC	AIN5	AIN6	Y
AA	P29	P30	GND	GND	GND	VDD_SDRAM	SDRAM_A9	SDRAM_A5	SDRAM_A1	SDRAM_RAS	SDRAM_DQ7	GND	SDRAM_DQ5	SDRAM_DQ1	SDRAM_DQ12	SDRAM_DQ8	SDRAM_CK	VDD_SDRAM	GND	NC	NC	SYNC2	AIN4	AA
AB	P31	P32	P34	NC	GND	DVDDIO	SDRAM_A8	SDRAM_A4	SDRAM_A0	SDRAM_BA1	SDRAM_CAS	VDD_SDRAM	SDRAM_DQ4	SDRAM_DQ0	SDRAM_DQ13	SDRAM_DQ9	SDRAM_CKN	VDD_SDRAM	GND	SYNC1	HS_IN1/TRI5	VS_IN1/TRI6	GND	AB
AC	GND	P33	P35	NC	GND	DVDDIO	SDRAM_A7	SDRAM_A3	SDRAM_A10	SDRAM_BA0	SDRAM_WE	VDD_SDRAM	SDRAM_DQ3	SDRAM_VREF	SDRAM_DQ14	SDRAM_DQ10	SDRAM_UDQS	VDD_SDRAM	GND	AIN1	AIN2	AIN3	GND	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Figure 7. Pin Configuration

Table 6. Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	GND	Ground	Ground
A2	VS/FIELD	Digital video output	VS is a vertical synchronization output signal. FIELD is a field synchronization output signal in all interlaced video modes. VS or FIELD can be configured for this pin.
A3	E2_TX+	Digital output	Digital Output Channel 2 True of Ethernet Interface
A4	E2_RX+	Digital input	Digital Input Channel 2 True of Ethernet Interface
A5	TVDD	Power	Terminator Supply Voltage (3.3 V).
A6	RXD_2-	HDMI input	Digital Input Channel 2 Complement of Port D in the HDMI Interface.
A7	RXD_1-	HDMI input	Digital Input Channel 1 Complement of Port D in the HDMI Interface.
A8	RXD_0-	HDMI input	Digital Input Channel 0 Complement of Port D in the HDMI Interface.
A9	RXD_C-	HDMI input	Digital Input Clock Complement of Port D in the HDMI Interface.
A10	HEAC_2-	HDMI input/output	HDMI Ethernet and Audio Return Channel (HEAC) Complement Channel 2 in HDMI Interface
A11	TVDD	Power	Terminator Supply Voltage (3.3 V).
A12	RXC_2-	HDMI input	Digital Input Channel 2 Complement of Port C in the HDMI Interface.
A13	RXC_1-	HDMI input	Digital Input Channel 1 Complement of Port C in the HDMI Interface.
A14	RXC_0-	HDMI input	Digital Input Channel 0 Complement of Port C in the HDMI Interface.
A15	RXC_C-	HDMI input	Digital Input Clock Complement of Port C in the HDMI Interface.
A16	NC	No connect	No Connect.
A17	TVDD	Power	Terminator Supply Voltage (3.3 V).
A18	RXB_2-	HDMI input	Digital Input Channel 2 Complement of Port B in the HDMI Interface.
A19	RXB_1-	HDMI input	Digital Input Channel 1 Complement of Port B in the HDMI Interface.
A20	RXB_0-	HDMI input	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
A21	RXB_C-	HDMI input	Digital Input Clock Complement of Port B in the HDMI Interface.
A22	HEAC_1-	HDMI input/output	HDMI Ethernet and Audio Return Channel (HEAC) Complement Channel 1 in HDMI Interface
A23	GND	Ground	Ground
B1	HS/CS	Digital video output	HS is a horizontal synchronization output signal. CS (composite synchronization) signal is a single signal containing both horizontal and vertical synchronization pulses.
B2	FIELD/DE	Miscellaneous digital	DE (data enable) is a signal that indicates active pixel data. FIELD is a field synchronization output signal in all interlaced video modes. DE or FIELD can be configured for this pin.
B3	E2_TX-	Digital output	Digital Output Channel 2 Complimentary of Ethernet Interface
B4	E2_RX-	Digital input	Digital Input Channel 2 Complimentary of Ethernet Interface
B5	TVDD	Power	Terminator Supply Voltage (3.3 V).
B6	RXD_2+	HDMI input	Digital Input Channel 2 True of Port D in the HDMI Interface.
B7	RXD_1+	HDMI input	Digital Input Channel 1 True of Port D in the HDMI Interface.
B8	RXD_0+	HDMI input	Digital Input Channel 0 True of Port D in the HDMI Interface.
B9	RXD_C+	HDMI input	Digital Input Clock True of Port D in the HDMI Interface.
B10	HEAC_2+	HDMI input/output	HDMI Ethernet and Audio Return Channel (HEAC) True Channel 2 in HDMI Interface
B11	TVDD	Power	Terminator Supply Voltage (3.3 V).
B12	RXC_2+	HDMI input	Digital Input Channel 2 True Of Port C in the HDMI Interface.
B13	RXC_1+	HDMI input	Digital Input Channel 1 True Of Port C in the HDMI Interface.
B14	RXC_0+	HDMI input	Digital Input Channel 0 True Of Port C in the HDMI Interface.
B15	RXC_C+	HDMI input	Digital Input Clock True Of Port C in the HDMI Interface.
B16	NC	No Connect	No Connect.
B17	TVDD	Power	Terminator Supply Voltage (3.3 V).
B18	RXB_2+	HDMI input	Digital Input Channel 2 True of Port B in the HDMI Interface.
B19	RXB_1+	HDMI input	Digital Input Channel 1 True of Port B in the HDMI Interface.
B20	RXB_0+	HDMI input	Digital Input Channel 0 True of Port B in the HDMI Interface.
B21	RXB_C+	HDMI input	Digital Input Clock True of Port B in the HDMI Interface.

ADV7844

PRELIMINARY

Pin No.	Mnemonic	Type	Description
B22	HEAC_1+	HDMI input/output	HDMI Ethernet and Audio Return Channel (HEAC) True Channel 1 in HDMI Interface
B23	GND	Ground	Ground
C1	P0	Digital video output	Video Pixel Output Port.
C2	P1	Digital video output	Video Pixel Output Port.
C3	E1_TX+	Digital output	Digital Output Channel 1 True of Ethernet Interface
C4	E1_RX+	Digital input	Digital Input Channel 1 True of Ethernet Interface
C5	TVDD	Power	Terminator Supply Voltage (3.3 V).
C6	$\overline{\text{PWRDN1}}$	Miscellaneous digital	Controls the Power-Up of the ADV7844. Should be connected to a digital 3.3 V I/O supply to power up the ADV7844.
C7	$\overline{\text{PWRDN2}}$	Test pin	This pin should be connected to the ground.
C8	HPA_D	Miscellaneous digital	Hot Plug Assert signal output for HDMI port D.
C9	RXD_5V	HDMI input	5 V Detect Pin for Port D in the HDMI Interface.
C10	RXC_5V	HDMI input	5 V Detect Pin for Port C in the HDMI Interface.
C11	TVDD	Power	Terminator Supply Voltage (3.3 V).
C12	GND	Ground	Ground
C13	GND	Ground	Ground
C14	GND	Ground	Ground
C15	GND	Ground	Ground
C16	GND	Ground	Ground
C17	GND	Ground	Ground
C18	TVDD	Power	Terminator Supply Voltage (3.3 V).
C19	TVDD	Power	Terminator Supply Voltage (3.3 V).
C20	TVDD	Power	Terminator Supply Voltage (3.3 V).
C21	TVDD	Power	Terminator Supply Voltage (3.3 V).
C22	TVDD	Power	Terminator Supply Voltage (3.3 V).
C23	TVDD	Power	Terminator Supply Voltage (3.3 V).
D1	P2	Digital video output	Video Pixel Output Port.
D2	P3	Digital video output	Video Pixel Output Port.
D3	E1_TX-	Digital output	Digital Output Channel 1 Complimentary of Ethernet Interface
D4	E1_RX-	Digital input	Digital Input Channel 1 Complimentary of Ethernet Interface
D5	TVDD	Power	Terminator Supply Voltage (3.3 V).
D6	SYNC_OUT	Miscellaneous digital	Sliced synchronization output.
D7	CEC	Digital input/output	Consumer Electronic Control Channel.
D8	HPA_C	Miscellaneous digital	Hot Plug Assert signal output for HDMI port C.
D9	RXB_5V	HDMI input	5 V Detect Pin for Port B in the HDMI Interface.
D10	HPA_B	Miscellaneous digital	Hot Plug Assert signal output for HDMI port B.
D11	TVDD	Power	Terminator Supply Voltage (3.3 V).
D12	RXA_5V	HDMI input	5 V Detect Pin for Port A in the HDMI Interface.
D13	HPA_A	Miscellaneous digital	Hot Plug Assert signal output for HDMI port A.
D14	DDCD_SDA	HDMI input	HDCP Slave Serial Data Port D. DDCD_SDA is a 3.3 V input that is 5 V tolerant.
D15	DDCD_SCL	HDMI input	HDCP Slave Serial Clock Port D. DDCD_SCL is a 3.3 V input that is 5 V tolerant.
D16	DDCC_SDA	HDMI input	HDCP Slave Serial Data Port C. DDCC_SDA is a 3.3 V input that is 5 V tolerant.
D17	DDCC_SCL	HDMI input	HDCP Slave Serial Clock Port C. DDCC_SCL is a 3.3 V input that is 5 V tolerant.
D18	RTERM	Miscellaneous	Sets Internal Termination Resistance. A 500 Ω resistor between this pin and

Pin No.	Mnemonic	Type	Description
		analog	GND should be used.
D19	DDCB_SDA	HDMI input	HDCP Slave Serial Data Port B. DDCB_SDA is a 3.3 V input that is 5 V tolerant.
D20	DDCB_SCL	HDMI input	HDCP Slave Serial Clock Port B. DDCB_SCL is a 3.3 V input that is 5 V tolerant.
D21	TVDD	Power	Terminator Supply Voltage (3.3 V).
D22	RXA_2+	HDMI input	Digital Input Channel 2 True of Port A in the HDMI Interface.
D23	RXA_2-	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
E1	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
E2	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
E3	GND	Ground	Ground
E4	GND	Ground	Ground
E20	DDCA_SDA	HDMI input	HDCP Slave Serial Data Port A. DDCA_SDA is a 3.3 V input that is 5 V tolerant.
E21	CVDD	Power	Comparator Supply Voltage (1.8 V).
E22	RXA_1+	HDMI input	Digital Input Channel 1 True of Port A in the HDMI Interface.
E23	RXA_1-	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
F1	P5	Digital video output	Video Pixel Output Port.
F2	P4	Digital video output	Video Pixel Output Port.
F3	EP_MISO	Digital output	SPI Master In/Slave Out for External EDID Interface.
F4	EP_MOSI	Digital input	SPI Master Out/Slave In for External EDID Interface.
F20	DDCA_SCL	HDMI input	HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant.
F21	CVDD	Power	Comparator Supply Voltage (1.8 V).
F22	RXA_0+	HDMI input	Digital Input Channel 0 True of Port A in the HDMI Interface.
F23	RXA_0-	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
G1	P7	Digital video output	Video Pixel Output Port.
G2	P6	Digital video output	Video Pixel Output Port.
G3	$\overline{\text{EP\_CS}}$	Digital output	SPI Chip Select for External EDID Interface.
G4	EP_SCK	Digital output	SPI Clock for External EDID Interface.
G7	GND	Ground	Ground
G8	GND	Ground	Ground
G9	GND	Ground	Ground
G10	GND	Ground	Ground
G11	TEST1	Test	Do Not Connect.
G12	TEST2	Test	Do Not Connect.
G13	GND	Ground	Ground
G14	GND	Ground	Ground
G15	CVDD	Power	Comparator Supply Voltage (1.8 V).
G16	CVDD	Power	Comparator Supply Voltage (1.8 V).
G17	CVDD	Power	Comparator Supply Voltage (1.8 V).
G20	VGA_SCL	Miscellaneous digital	DDC Port Serial Clock Input for VGA
G21	CVDD	Power	Comparator Supply Voltage (1.8 V).
G22	RXA_C+	HDMI input	Digital Input Clock True of Port A in the HDMI Interface.
G23	RXA_C-	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
H1	P9	Digital video output	Video Pixel Output Port.
H2	P8	Digital video output	Video Pixel Output Port.
H3	TTX_SDA	Miscellaneous digital	I2C Port Serial Data Input/Output Pin. SDA is the data line for the teletext port.
H4	TTX_SCL	Miscellaneous digital	I2C Port Serial Clock Input. SCL is the clock line for the teletext port.

ADV7844

PRELIMINARY

Pin No.	Mnemonic	Type	Description
H7	GND	Ground	Ground
H8	GND	Ground	Ground
H9	GND	Ground	Ground
H10	GND	Ground	Ground
H11	GND	Ground	Ground
H12	GND	Ground	Ground
H13	GND	Ground	Ground
H14	GND	Ground	Ground
H15	CVDD	Power	Comparator Supply Voltage (1.8 V).
H16	CVDD	Power	Comparator Supply Voltage (1.8 V).
H17	CVDD	Power	Comparator Supply Voltage (1.8 V).
H20	VGA_SDA	Miscellaneous digital	DDC Port Data Clock Input for VGA
H21	CVDD	Power	Comparator Supply Voltage (1.8 V).
H22	NC	No Connect	No Connect
H23	NC	No Connect	No Connect
J1	P11	Digital video output	Video Pixel Output Port.
J2	P10	Digital video output	Video Pixel Output Port.
J3	MCLK	Miscellaneous	Audio Master Clock Output.
J4	AP0	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD), Direct Stream Transfer (DST) or I2S.
J7	GND	Ground	Ground
J8	GND	Ground	Ground
J9	GND	Ground	Ground
J10	GND	Ground	Ground
J11	GND	Ground	Ground
J12	GND	Ground	Ground
J13	GND	Ground	Ground
J14	GND	Ground	Ground
J15	GND	Ground	Ground
J16	GND	Ground	Ground
J17	GND	Ground	Ground
J20	PVDD	Power	PLL Supply Voltage (1.8 V).
J21	TEST3	Test	Do Not Connect.
J22	GND	Ground	Ground
J23	GND	Ground	Ground
K1	P13	Digital video output	Video Pixel Output Port.
K2	P12	Digital video output	Video Pixel Output Port.
K3	AP5	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD), Direct Stream Transfer (DST) or I2S.
K4	SCLK	Miscellaneous digital	Audio Serial Clock Output.
K7	VDD	Power	Digital Core Supply Voltage (1.8 V).
K8	GND	Ground	Ground
K9	GND	Ground	Ground
K10	GND	Ground	Ground
K11	GND	Ground	Ground
K12	GND	Ground	Ground

Pin No.	Mnemonic	Type	Description
K13	GND	Ground	Ground
K14	GND	Ground	Ground
K15	GND	Ground	Ground
K16	GND	Ground	Ground
K17	GND	Ground	Ground
K20	PVDD	Power	PLL Supply Voltage (1.8 V).
K21	GND	Ground	Ground
K22	XTALN	Miscellaneous analog	Input Pin for 28.63636 MHz Crystal.
K23	XTALP	Miscellaneous analog	Crystal Input. Input pin for 28.63636 MHz Crystal or an External 1.8 V, 28.63636 MHz Clock Oscillator Source to Clock the ADV7844.
L1	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
L2	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
L3	GND	Ground	Ground
L4	GND	Ground	Ground
L7	VDD	Power	Digital Core Supply Voltage (1.8 V).
L8	GND	Ground	Ground
L9	GND	Ground	Ground
L10	GND	Ground	Ground
L11	GND	Ground	Ground
L12	GND	Ground	Ground
L13	GND	Ground	Ground
L14	GND	Ground	Ground
L15	GND	Ground	Ground
L16	GND	Ground	Ground
L17	GND	Ground	Ground
L20	GND	Ground	Ground
L21	GND	Ground	Ground
L22	GND	Ground	Ground
L23	GND	Ground	Ground
M1	P15	Digital video output	Video Pixel Output Port.
M2	P14	Digital video output	Video Pixel Output Port.
M3	AP4	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD), Direct Stream Transfer (DST) or I2S.
M4	AP3	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD), Direct Stream Transfer (DST) or I2S.
M7	VDD	Power	Digital Core Supply Voltage (1.8 V).
M8	GND	Ground	Ground
M9	GND	Ground	Ground
M10	GND	Ground	Ground
M11	GND	Ground	Ground
M12	GND	Ground	Ground
M13	GND	Ground	Ground
M14	GND	Ground	Ground
M15	GND	Ground	Ground
M16	GND	Ground	Ground
M17	GND	Ground	Ground
M20	GND	Ground	Ground
M21	GND	Ground	Ground
M22	REFN	Miscellaneous	Internal Voltage Reference Output.

ADV7844

PRELIMINARY

Pin No.	Mnemonic	Type	Description
		analog	
M23	REFP	Miscellaneous analog	Internal Voltage Reference Output.
N1	P17	Digital video output	Video Pixel Output Port.
N2	P16	Digital video output	Video Pixel Output Port.
N3	AP2	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD), Direct Stream Transfer (DST) or I2S.
N4	AP1	Miscellaneous	Audio Output Pin. Pins AP0-AP5 can be configured to output SPDIF Digital Audio Output (SPDIF), High Bit Rate (HBR), Direct Stream Digital (DSD), Direct Stream Transfer (DST) or I2S.
N7	VDD	Power	Digital Core Supply Voltage (1.8 V).
N8	GND	Ground	Ground
N9	GND	Ground	Ground
N10	GND	Ground	Ground
N11	GND	Ground	Ground
N12	GND	Ground	Ground
N13	GND	Ground	Ground
N14	GND	Ground	Ground
N15	GND	Ground	Ground
N16	GND	Ground	Ground
N17	GND	Ground	Ground
N20	AVDD	Power	Analog Supply Voltage (1.8 V).
N21	AVDD	Power	Analog Supply Voltage (1.8 V).
N22	AVDD	Power	Analog Supply Voltage (1.8 V).
N23	AVDD	Power	Analog Supply Voltage (1.8 V).
P1	P18	Digital video output	Video Pixel Output Port.
P2	P19	Digital video output	Video Pixel Output Port.
P3	SCL	Miscellaneous digital	I^2C Port Serial Clock Input. SCL is the clock line for the control port.
P4	SDA	Miscellaneous digital	I^2C Port Serial Data Input/Output Pin. SDA is the data line for the control port.
P7	VDD	Power	Digital Core Supply Voltage (1.8 V).
P8	GND	Ground	Ground
P9	GND	Ground	Ground
P10	GND	Ground	Ground
P11	GND	Ground	Ground
P12	GND	Ground	Ground
P13	GND	Ground	Ground
P14	GND	Ground	Ground
P15	GND	Ground	Ground
P16	GND	Ground	Ground
P17	GND	Ground	Ground
P20	AVDD	Power	Analog Supply Voltage (1.8 V).
P21	AVDD	Power	Analog Supply Voltage (1.8 V).
P22	AIN11	Analog video input	Analog Video Input Channel.
P23	AIN12	Analog video input	Analog Video Input Channel.
R1	P20	Digital video output	Video Pixel Output Port.
R2	P21	Digital video output	Video Pixel Output Port.
R3	TEST4	Test	Do Not Connect.

Pin No.	Mnemonic	Type	Description
R4	INT1	Miscellaneous digital	Interrupt. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
R7	VDD	Power	Digital Core Supply Voltage (1.8 V).
R8	GND	Ground	Ground
R9	GND	Ground	Ground
R10	GND	Ground	Ground
R11	GND	Ground	Ground
R12	GND	Ground	Ground
R13	GND	Ground	Ground
R14	GND	Ground	Ground
R15	GND	Ground	Ground
R16	GND	Ground	Ground
R17	GND	Ground	Ground
R20	HS_IN2/TRI7	Miscellaneous analog	HS on Graphics Port 2. The HS input signal is used for 5-wire timing mode. This pin can also be used as a trilevel/bilevel input on the SCART or D-terminal connector. Result available via I^2C.
R21	VS_IN2/TRI8	Miscellaneous analog	VS on Graphics Port 2. The VS input signal is used for 5-wire timing mode. This pin can also be used as a trilevel/bilevel input on the SCART or D-terminal connector. Result available via I^2C.
R22	SYNC4	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
R23	AIN10	Analog video input	Analog Video Input Channel.
T1	P22	Digital video output	Video Pixel Output Port.
T2	P23	Digital video output	Video Pixel Output Port.
T3	TEST5	Test	Do Not Connect.
T4	INT2	Miscellaneous digital	Interrupt. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
T7	VDD	Power	Digital Core Supply Voltage (1.8 V).
T8	GND	Ground	Ground
T9	GND	Ground	Ground
T10	GND	Ground	Ground
T11	GND	Ground	Ground
T12	GND	Ground	Ground
T13	GND	Ground	Ground
T14	GND	Ground	Ground
T15	GND	Ground	Ground
T16	GND	Ground	Ground
T17	GND	Ground	Ground
T20	GND	Ground	Ground
T21	GND	Ground	Ground
T22	GND	Ground	Ground
T23	GND	Ground	Ground
U1	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
U2	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
U3	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
U4	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
U7	VDD	Power	Digital Core Supply Voltage (1.8 V).
U8	VDD	Power	Digital Core Supply Voltage (1.8 V).
U9	VDD	Power	Digital Core Supply Voltage (1.8 V).
U10	VDD	Power	Digital Core Supply Voltage (1.8 V).

ADV7844

PRELIMINARY

Pin No.	Mnemonic	Type	Description
U11	VDD	Power	Digital Core Supply Voltage (1.8 V).
U12	VDD	Power	Digital Core Supply Voltage (1.8 V).
U13	VDD	Power	Digital Core Supply Voltage (1.8 V).
U14	VDD	Power	Digital Core Supply Voltage (1.8 V).
U15	GND	Ground	Ground
U16	GND	Ground	Ground
U17	GND	Ground	Ground
U20	TRI4	Miscellaneous analog	Trilevel/Bilevel Input on the SCART or D-Terminal Connector. Result available via I2C.
U21	TRI3	Miscellaneous analog	Trilevel/Bilevel Input on the SCART or D-Terminal Connector. Result available via I2C.
U22	AIN9	Analog video input	Analog Video Input Channel.
U23	AIN8	Analog video input	Analog Video Input Channel.
V1	LLC	Digital video output	Line-Locked Output Clock for the Pixel Data (Range is 13.5 MHz to 170 MHz).
V2	P24	Digital video output	Video Pixel Output Port.
V3	$\overline{\text{RESET}}$	Miscellaneous digital	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7844 circuitry.
V4	AVLINK	Digital input/output	Digital SCART Control Channel.
V20	TRI1	Miscellaneous analog	Trilevel/Bilevel Input on the SCART or D-Terminal Connector. Result available via I2C.
V21	TRI2	Miscellaneous analog	Trilevel/Bilevel Input on the SCART or D-Terminal Connector. Result available via I2C.
V22	SYNC3	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
V23	AIN7	Analog video input	Analog Video Input Channel.
W1	P25	Digital video output	Video Pixel Output Port.
W2	P26	Digital video output	Video Pixel Output Port.
W3	NC	No connect	No Connect.
W4	SPDIF_IN	Miscellaneous digital	Audio Clock Input Pin for SPDIF
W20	AVDD	Power	Analog Supply Voltage (1.8 V).
W21	AVDD	Power	Analog Supply Voltage (1.8 V).
W22	AVDD	Power	Analog Supply Voltage (1.8 V).
W23	AVDD	Power	Analog Supply Voltage (1.8 V).
Y1	P27	Digital video output	Video Pixel Output Port.
Y2	P28	Digital video output	Video Pixel Output Port.
Y3	GND	Ground	Ground
Y4	GND	Ground	Ground
Y5	GND	Ground	Ground
Y6	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
Y7	SDRAM_A11	SDRAM interface	Address Output. Interface to external RAM address lines.
Y8	SDRAM_A6	SDRAM interface	Address Output. Interface to external RAM address lines.
Y9	SDRAM_A2	SDRAM interface	Address Output. Interface to external RAM address lines.
Y10	$\overline{\text{SDRAM\_CS}}$	SDRAM interface	Chip Select. $\overline{\text{SDRAM\_CS}}$ enables and disables the command decoder on the RAM. One of four command signals to the external SDRAM.
Y11	SDRAM_LDQS	SDRAM interface	Lower Data Strobe Pin. Data strobe pins are used for the RAM interface. This is an output with read data and an input with write data. It is edge aligned with write data and centered in read data. SDRAM_ LDQS corresponds to the data on SDRAM_DQ0 to SDRAM_
Y12	GND	Ground	Ground

Pin No.	Mnemonic	Type	Description
Y13	SDRAM_DQ6	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
Y14	SDRAM_DQ2	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
Y15	SDRAM_DQ15	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
Y16	SDRAM_DQ11	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
Y17	SDRAM_CKE	SDRAM interface	Clock Enable. This pin acts as an enable to the clock signals of the external RAM.
Y18	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
Y19	GND	Ground	Ground
Y20	AOUT	Analog monitor output	Analog Monitor Output.
Y21	NC	No connect	No Connect.
Y22	AIN5	Analog video input	Analog Video Input Channel.
Y23	AIN6	Analog video input	Analog Video Input Channel.
AA1	P29	Digital video output	Video Pixel Output Port.
AA2	P30	Digital video output	Video Pixel Output Port.
AA3	GND	Ground	Ground
AA4	GND	Ground	Ground
AA5	GND	Ground	Ground
AA6	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AA7	SDRAM_A9	SDRAM interface	Address Output. Interface to external RAM address lines.
AA8	SDRAM_A5	SDRAM interface	Address Output. Interface to external RAM address lines.
AA9	SDRAM_A1	SDRAM interface	Address Output. Interface to external RAM address lines.
AA10	$\overline{\text{SDRAM\_RAS}}$	SDRAM interface	Row Address Select Command Signal. One of four command signals to the external SDRAM.
AA11	SDRAM_DQ7	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AA12	GND	Ground	Ground
AA13	SDRAM_DQ5	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AA14	SDRAM_DQ1	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AA15	SDRAM_DQ12	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AA16	SDRAM_DQ8	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AA17	SDRAM_CK	SDRAM interface	Differential Clock Output. All address and control output signals to the RAM should be sampled on the positive edge of SDRAM_CK and on the negative edge of $\overline{\text{SDRAM\_CK}}$.
AA18	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AA19	GND	Ground	Ground
AA20	NC	No connect	No Connect.
AA21	NC	No connect	No Connect.
AA22	SYNC2	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
AA23	AIN4	Analog video input	Analog Video Input Channel.
AB1	P31	Digital video output	Video Pixel Output Port.
AB2	P32	Digital video output	Video Pixel Output Port.
AB3	P34	Digital video output	Video Pixel Output Port.
AB4	NC	No connect	No Connect.
AB5	GND	Ground	Ground
AB6	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
AB7	SDRAM_A8	SDRAM interface	Address Output. Interface to external RAM address lines.
AB8	SDRAM_A4	SDRAM interface	Address Output. Interface to external RAM address lines.

Pin No.	Mnemonic	Type	Description
AB9	SDRAM_A0	SDRAM interface	Address Output. Interface to external RAM address lines.
AB10	SDRAM_BA1	SDRAM interface	Bank Address Output. Interface to external RAM bank address lines.
AB11	SDRAM_CAS	SDRAM interface	Column Address Select Command Signal. One of four command signals to the external SDRAM.
AB12	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AB13	SDRAM_DQ4	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AB14	SDRAM_DQ0	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AB15	SDRAM_DQ13	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AB16	SDRAM_DQ9	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AB17	SDRAM_CK	SDRAM interface	Differential Clock Output. All address and control output signals to the RAM should be sampled on the positive edge of SDRAM_CK and on the negative edge of SDRAM_CK.
AB18	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AB19	GND	Ground	Ground
AB20	SYNC1	Miscellaneous analog	This is a synchronization on green or luma input (SOG/SOY) used in embedded synchronization mode. User configurable.
AB21	HS_IN1/TRI5	Miscellaneous analog	HS on Graphics Port 1. The HS input signal is used for 5-wire timing mode. HS_IN1/TRI5 is a 3.3 V input that is 5 V tolerant.
AB22	VS_IN1/TRI6	Miscellaneous analog	Vertical Synchronization Input Signal. Used for 5-wire timing mode.
AB23	GND	Ground	Ground
AC1	GND	Ground	Ground
AC2	P33	Digital video output	Video Pixel Output Port.
AC3	P35	Digital video output	Video Pixel Output Port.
AC4	NC	No connect	No Connect.
AC5	GND	Ground	Ground
AC6	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
AC7	SDRAM_A7	SDRAM interface	Address Output. Interface to external RAM address lines.
AC8	SDRAM_A3	SDRAM interface	Address Output. Interface to external RAM address lines.
AC9	SDRAM_A10	SDRAM interface	Address Output. Interface to external RAM address lines.
AC10	SDRAM_BA0	SDRAM interface	Bank Address Output. Interface to external RAM bank address lines.
AC11	SDRAM_WE	SDRAM interface	Write Enable Output Command Signal. One of four command signals to the external SDRAM.
AC12	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AC13	SDRAM_DQ3	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AC14	SDRAM_VREF	SDRAM interface	1.25 V Reference for DDR SDRAM Interface or 1.65 V for SDR.
AC15	SDRAM_DQ14	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AC16	SDRAM_DQ10	SDRAM interface	Data Bus. Interface to external RAM 16-bit data bus.
AC17	SDRAM_UDQS	SDRAM interface	Upper Data Strobe Pin. Data strobe pins for the RAM interface. This is an output with read data and an input with write data. It is edge aligned with write data and centered in read data. UDQS corresponds to the data on DQ8 to DQ16.
AC18	VDD_SDRAM	Power	External Memory Interface Digital Input/Output Supply (DDR 2.5 V or SDR 3.3 V).
AC19	GND	Ground	Ground
AC20	AIN1	Analog video input	Analog Video Input Channel.
AC21	AIN2	Analog video input	Analog Video Input Channel.
AC22	AIN3	Analog video input	Analog Video Input Channel.
AC23	GND	Ground	Ground

HDMI 1.4 Mux with Xpressview Fast Switching

ADI Confidential

ADV3014

FEATURES

4-input, 1-output HDMI mux
HDMI 1.4a support: 3D TV formats, content type bits, CEC 1.4-compatible
Xpressview fast switching on all HDMI input ports
High-bandwidth digital content protection (HDCP 1.4a)
HDCP repeater support
225 MHz HDMI Rx and Tx support 36-/30-/24-bit Deep Color
Ultralow jitter digital PLL (100% deskew)
Quad HDMI Rx input
- **Adaptive equalizer for cable lengths up to 30 meters**
- **Internal extended display identification data (EDID) RAM**
- **EDID replication (512 bytes per port)**
- **EDID with HDMI cable 5 V power support**
- **5 V detect inputs**
- **Hot plug assertion control pins**

Single HDMI Tx output: EDID data extraction and hot plug detect (HPD) input
HDMI 1.4a audio pass-through support
- **I²S, DSD, and HBR, including Dolby TrueHD and DTS-HD master audio**

General
- **Interrupt controller with 3 interrupt outputs**
- **Software libraries, driver, and application available**
- **2-layer PCB design supported**
- **144-lead, 20 mm × 20 mm LQFP package**

APPLICATIONS

Port expansion for Analog Devices HDMI decoders
Audio video receivers (AVRs)
Home theater in a box (HTiB)
Sound bar with HDMI repeater support
Flat panel TVs
Other repeater applications

GENERAL DESCRIPTION

The ADV3014 is a high performance, four-input, one-output, High-Definition Multimedia Interface (HDMI™) switch that integrates HDMI 1.4a receiver and transmitter functions onto one chip. It supports all HDCP repeater functions through fully tested Analog Devices, Inc., repeater software libraries and drivers. The ADV3014 incorporates Xpressview™ fast switching on all

FUNCTIONAL BLOCK DIAGRAM

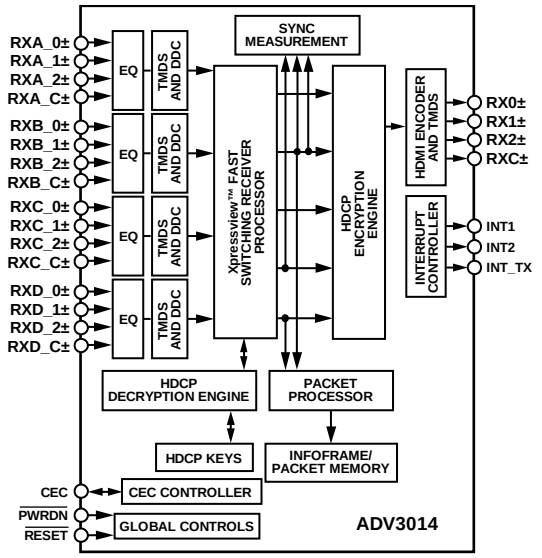


Figure 1.

input HDMI ports. Using the Analog Devices hardware-based HDCP engine that minimizes software overhead, Xpressview technology allows fast switching between any HDMI input ports in less than 1 second.

The ADV3014 supports all mandatory HDMI 1.4a 3D TV formats in addition to all HD TV formats up to 1080p 36-bit Deep Color. The ADV3014 also features an integrated HDMI 1.4 CEC controller, which supports capability discovery and control (CDC).

The HDMI receiver supports programmable/adaptive equalization that ensures robust operation of the interface at cable lengths of up to 30 meters.

The ADV3014 offers integrated control of hot plug circuits, sensing of 5 V input signals and on-board EDID controls with EDID replication and power-down mode EDID.

The ADV3014 supports pass-through of all HDMI 1.4a audio formats including I²S, DSD, and HBR formats such as Dolby® TrueHD and DTS-HD® master audio.

Fabricated in an advanced CMOS process, the ADV3014 is provided in a space-saving, 144-lead, 20 mm × 20 mm LQFP surface-mount, Pb-free package. It is specified over the 0°C to 70°C temperature range.

Advantiv® Advanced Television Solutions by Analog Devices | NSV® Precision Video by Analog Devices

DETAILED FUNCTIONAL BLOCK DIAGRAM

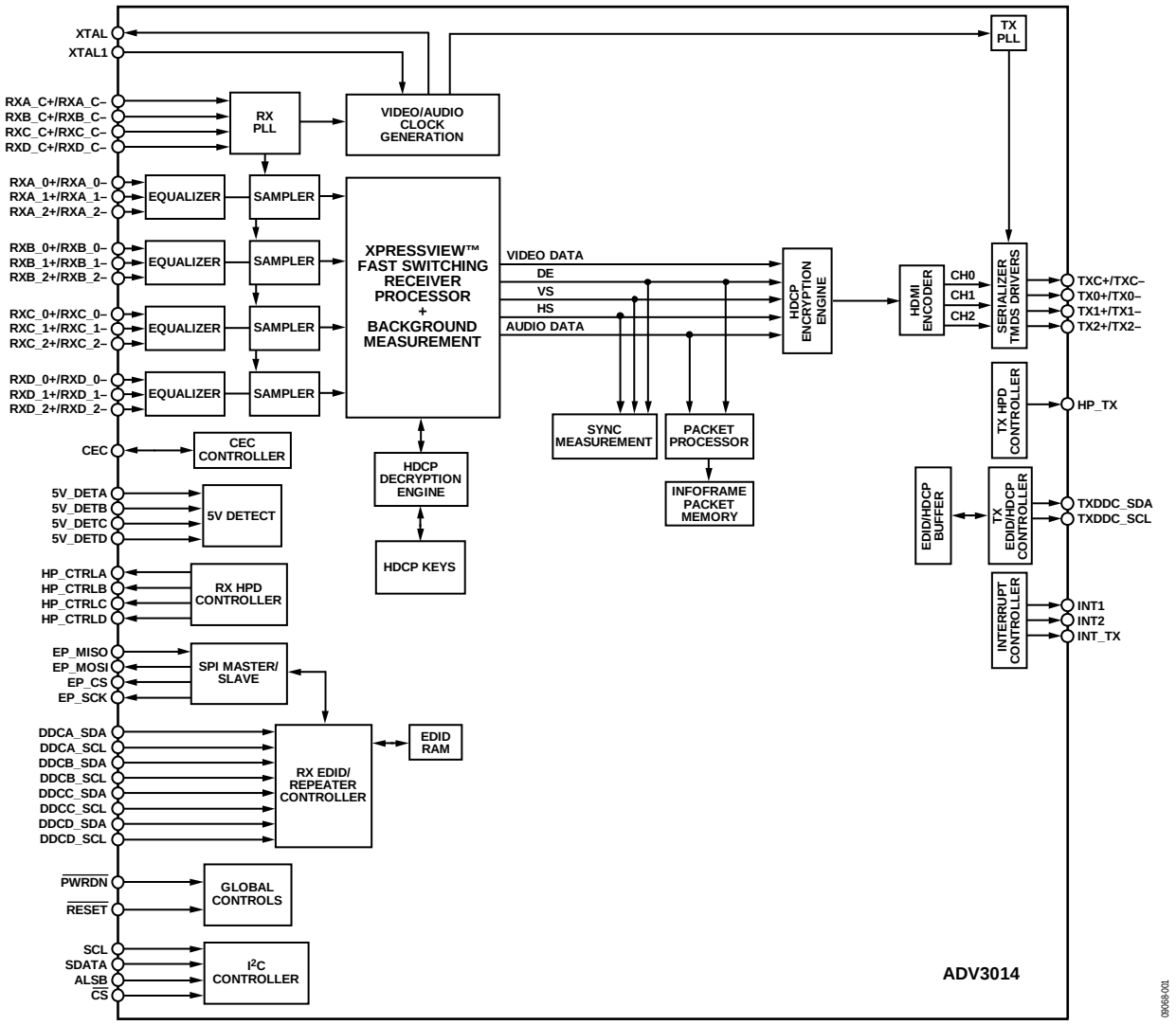


Figure 2. Detailed Functional Block Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

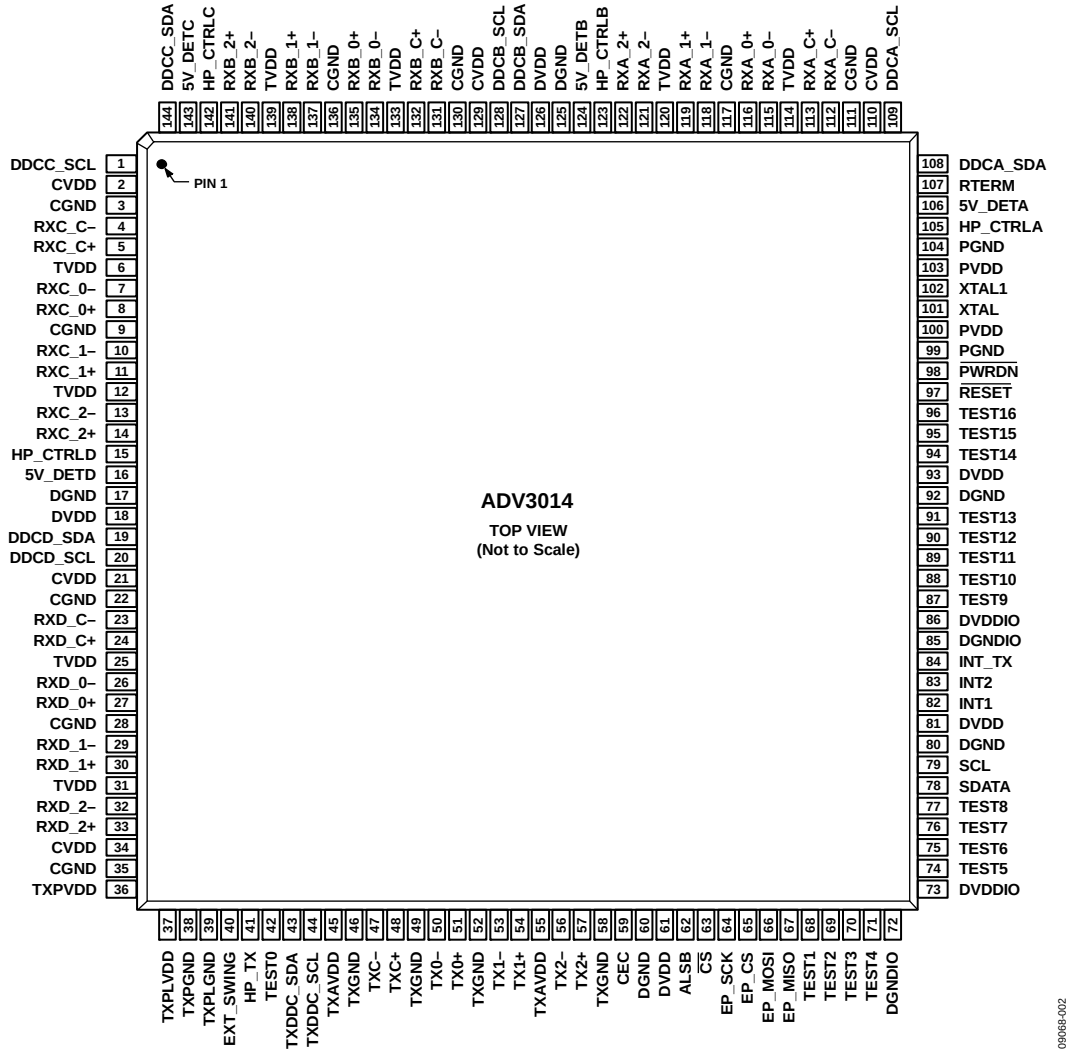


Figure 4. Pin Configuration

Table 5: Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	DDCC_SCL	Digital input	HDCP Slave Serial Clock Port C. DDCC_SCL is a 3.3 V input that is 5 V tolerant.
2	CVDD	Power	Receiver Comparator Supply Voltage (1.8 V).
3	CGND	Ground	TVDD and CVDD Ground.
4	RXC_C–	HDMI input	Digital Input Clock Complement of Port C in the HDMI Interface.
5	RXC_C+	HDMI input	Digital Input Clock True of Port C in the HDMI Interface.
6	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
7	RXC_0–	HDMI input	Digital Input Channel 0 Complement of Port C in the HDMI Interface.
8	RXC_0+	HDMI input	Digital Input Channel 0 True of Port C in the HDMI Interface.
9	CGND	Ground	TVDD and CVDD Ground.
10	RXC_1–	HDMI input	Digital Input Channel 1 Complement of Port C in the HDMI Interface.
11	RXC_1+	HDMI input	Digital Input Channel 1 True of Port C in the HDMI Interface.
12	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
13	RXC_2–	HDMI input	Digital Input Channel 2 Complement of Port C in the HDMI Interface.

ADI Confidential **ADV3014**

Pin No.	Mnemonic	Type	Description
14	RXC_2+	HDMI input	Digital Input Channel 2 True of Port C in the HDMI Interface.
15	HP_CTRLD	Digital output	Hot Plug Control Output for Port D. This pin is 5 V tolerant.
16	5V_DETD	HDMI input	5 V Detect Pin for Port D in the HDMI Interface. This pin is 5 V tolerant.
17	DGND	Ground	DVDD Ground.
18	DVDD	Power	Digital Supply Voltage (1.8 V).
19	DDCD_SDA	Digital I/O	HDCP Slave Serial Data Port D. DDCD_SDA is a 3.3 V input that is 5 V tolerant.
20	DDCD_SCL	Digital Input	HDCP Slave Serial Clock Port D. DDCD_SCL is a 3.3 V input that is 5 V tolerant.
21	CVDD	Power	Comparator Supply Voltage (1.8 V).
22	CGND	Ground	TVDD and CVDD Ground.
23	RXD_C−	HDMI input	Digital Input Clock Complement of Port D in the HDMI Interface.
24	RXD_C+	HDMI input	Digital Input Clock True of Port D in the HDMI Interface.
25	TVDD	Power	Terminator Supply Voltage (3.3 V).
26	RXD_0-	HDMI input	Digital Input Channel 0 Complement of Port D in the HDMI Interface.
27	RXD_0+	HDMI input	Digital Input Channel 0 True of Port D in the HDMI Interface.
28	CGND	Ground	TVDD and CVDD Ground.
29	RXD_1−	HDMI input	Digital Input Channel 1 Complement of Port D in the HDMI Interface.
30	RXD_1+	HDMI input	Digital Input Channel 1 True of Port D in the HDMI Interface.
31	TVDD	Power	Terminator Supply Voltage (3.3 V).
32	RXD_2−	HDMI input	Digital Input Channel 2 Complement of Port D in the HDMI Interface.
33	RXD_2+	HDMI input	Digital Input Channel 2 True of Port D in the HDMI Interface.
34	CVDD	Power	Comparator Supply Voltage (1.8 V).
35	CGND	Ground	TVDD and CVDD Ground.
36	TXPVDD	Power	1.8 V PLL Power Supply. These pins provide power to the digital portion of the clock PLL. The designer should provide quiet, noise-free power to these pins.
37	TXPLVDD	Power	1.8 V power supply
38	TXPGND	Ground	TXPVDD Ground.
39	TXPLGND	Ground	TXPLVDD Ground
40	EXT_SWING	Analog input	Sets Internal Reference Currents. Place an 887Ω resistor (1% tolerance) between this pin and ground.
41	HP_TX	Analog input	Hot Plug Detect Signal. This pin indicates to the interface whether the receiver is connected. This pin is 5 V tolerant.
42	TEST0	Test pin	Connect to ground.
43	TXDDC_SDA	Digital I/O	Serial Port Data I/O to Receiver. This pin serves as the master to the DDC bus. This pin is 5 V tolerant.
44	TXDDC_SCL	Digital output	Serial Port Data Clock to Receiver. This pin serves as the master clock for the DDC bus. This pin is 5 V tolerant.
45	TXAVDD	Power	1.8 V Power Supply for TMDS Outputs.
46	TXGND	Ground	TXAVDD Ground.
47	TXC−	HDMI output	Differential Clock Output. Differential clock output at the TMDS clock rate; supports TMDS logic level.
48	TXC+	HDMI output	Differential Clock Output. Differential clock output at the TMDS clock rate; supports TMDS logic level.
49	TXGND	Ground	TXAVDD Ground.
50	TX0−	HDMI output	Differential Output Channel 0 Complement. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.
51	TX0+	HDMI output	Differential Output Channel 0 True. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.
52	TXGND	Ground	TXAVDD Ground.
53	TX1−	HDMI output	Differential Output Channel 1 Complement. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.
54	TX1+	HDMI output	Differential Output Channel 1 True. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.
55	TXAVDD	Power	1.8 V Power Supply for TMDS Outputs.
56	TX2−	HDMI output	Differential Output Channel 2 Complement. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.

ADV3014

ADI Confidential

Pin No.	Mnemonic	Type	Description
57	TX2+	HDMI output	Differential Output Channel 2 True. Differential output of the red data at 10× the pixel clock rate; supports TMDS logic level.
58	TXGND	Ground	TXAVDD Ground.
59	CEC	Digital I/O	Consumer Electronics Control Channel. This pin is 5 V tolerant.
60	DGND	Ground	DVDD Ground.
61	DVDD	Power	Digital Supply Voltage (1.8 V).
62	ALSB	Digital input	This pin is used to set the I^2C address of the Rx IO and the Tx main maps.
63	$\overline{CS}$	Digital input	Chip Select Pin. This pin must be set low or left floating for the chip to process I2C messages that are destined for the ADV3014. The ADV3014 ignores I2C messages that it receives if this pin is high.
64	EP_SCK	Digital output	SPI Clock Interface for the EDID.
65	EP_CS	Digital output	SPI Chip Selected Interface for the EDID.
66	EP_MOSI	Digital output	SPI Master Out/Slave In for the EDID.
67	EP_MISO	Digital input	SPI Master In/Slave Out for the EDID.
68	TEST1	Test pin	Connect to ground.
69	TEST2	Test pin	Connect to ground.
70	TEST3	Test pin	Connect to ground.
71	TEST4	Test pin	Connect to ground.
72	DGNDIO	Ground	DVDDIO Ground.
73	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
74	TEST5	Test pin	Connect to ground.
75	TEST6	Test pin	Connect to ground.
76	TEST7	Test pin	Connect to ground.
77	TEST8	Test pin	Connect to ground.
78	SDATA	Digital I/O	I^2C Port Serial Data Input/Output Pin. SDATA is the data line for the control port.
79	SCL	Digital input	I^2C Port Serial Clock Input. SCL is the clock line for the control port.
80	DGND	Ground	DVDD Ground.
81	DVDD	Power	Digital Supply Voltage (1.8 V).
82	INT1	Digital output	Interrupt Pin. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
83	INT2	Digital output	Interrupt Pin. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user control.
84	INT_TX	Digital output	Interrupt; Open Drain. A 2 kΩ pull-up resistor to the microcontroller I/O supply is recommended.
85	DGNDIO	Ground	DVDDIO Ground.
86	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
87	TEST9	Test pin	Leave floating.
88	TEST10	Test pin	Leave floating.
89	TEST11	Test pin	Leave floating.
90	TEST12	Test pin	Leave floating.
91	TEST13	Test pin	Leave floating.
92	DGND	Ground	DVDD Ground.
93	DVDD	Power	Digital Supply Voltage (1.8 V).
94	TEST14	Test pin	Leave floating.
95	TEST15	Test pin	Leave floating.
96	TEST16	Test pin	Leave floating.
97	$\overline{RESET}$	Digital input	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV3014 circuitry.
98	$\overline{PWRDN}$	Digital input	Active-Low Power-Down Pin. If used, this pin should be pulled high to power up the ADV3014. This pin can also be used as an in-system power detect where an internal EDID can be powered from a 5 V signal of the HDMI port when it is connected to active equipment. This pin is 5 V tolerant.
99	PGND	Ground	PVDD Ground.
100	PVDD	Power	PLL Supply Voltage (1.8 V).
101	XTAL	Miscellaneous analog	Input Pin for 28.63636 MHz Crystal or an External 1.8 V 28.63636 MHz Clock Oscillator Source to Clock the ADV3014.

ADI Confidential **ADV3014**

Pin No.	Mnemonic	Type	Description
102	XTAL1	Miscellaneous analog	Crystal Output Pin. This pin should be left floating if a clock oscillator is used.
103	PVDD	Power	PLL Supply Voltage (1.8 V).
104	PGND	Ground	PVDD Ground.
105	HP_CTRLA	Digital output	Hot Plug Control Output for Port A. This pin is 5 V tolerant.
106	5V_DETA	Digital input	5 V Detect Pin for Port A in the HDMI Interface. This pin is 5 V tolerant.
107	RTERM	Miscellaneous analog	This pin sets the internal termination resistance. A 500 Ω resistor between this pin and ground should be used.
108	DDCA_SDA	Digital I/O	HDCP Slave Serial Data Port A. DDCA_SDA is a 3.3 V input/output that is 5 V tolerant.
109	DDCA_SCL	Digital input	HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant.
110	CVDD	Power	Receiver Comparator Supply Voltage (1.8 V).
111	CGND	Ground	TVDD and CVDD Ground.
112	RXA_C−	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
113	RXA_C+	HDMI input	Digital Input Clock True of Port A in the HDMI Interface.
114	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
115	RXA_0−	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
116	RXA_0+	HDMI input	Digital Input Channel 0 True of Port A in the HDMI Interface.
117	CGND	Ground	TVDD and CVDD Ground.
118	RXA_1−	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
119	RXA_1+	HDMI input	Digital Input Channel 1 True of Port A in the HDMI Interface.
120	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
121	RXA_2−	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
122	RXA_2+	HDMI input	Digital Input Channel 2 True of Port A in the HDMI Interface.
123	HP_CTRLB	Digital output	Hot Plug Control Output for Port B. This pin is 5 V tolerant.
124	5V_DETB	Digital input	5 V Detect Pin for Port B in the HDMI Interface. This pin is 5 V tolerant.
125	DGND	Ground	DVDD Ground.
126	DVDD	Power	Digital Supply Voltage (1.8 V).
127	DDCB_SDA	Digital I/O	HDCP Slave Serial Data Port B. DDCB_SDA is a 3.3 V input/output that is 5 V tolerant.
128	DDCB_SCL	Digital input	HDCP Slave Serial Clock Port B. DDCB_SCL is a 3.3 V input that is 5 V tolerant.
129	CVDD	Power	Receiver Comparator Supply Voltage (1.8 V).
130	CGND	Ground	TVDD and CVDD Ground.
131	RXB_C−	HDMI input	Digital Input Clock Complement of Port B in the HDMI Interface.
132	RXB_C+	HDMI input	Digital Input Clock True of Port B in the HDMI Interface.
133	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
134	RXB_0−	HDMI input	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
135	RXB_0+	HDMI input	Digital Input Channel 0 True of Port B in the HDMI Interface.
136	CGND	Ground	TVDD and CVDD Ground.
137	RXB_1−	HDMI input	Digital Input Channel 1 Complement of Port B in the HDMI Interface.
138	RXB_1+	HDMI input	Digital Input Channel 1 True of Port B in the HDMI Interface.
139	TVDD	Power	Receiver Terminator Supply Voltage (3.3 V).
140	RXB_2−	HDMI input	Digital Input Channel 2 Complement of Port B in the HDMI Interface.
141	RXB_2+	HDMI input	Digital Input Channel 2 True of Port B in the HDMI Interface.
142	HP_CTRLC	Digital output	Hot Plug Control Output for Port C. This pin is 5 V tolerant.
143	5V_DETC	Digital input	5 V Detect Pin for Port C in the HDMI Interface. This pin is 5 V tolerant.
144	DDCC_SDA	Digital I/O	HDCP Slave Serial Data Port C. DDCC_SDA is a 3.3 V input/output that is 5 V tolerant.

KEC

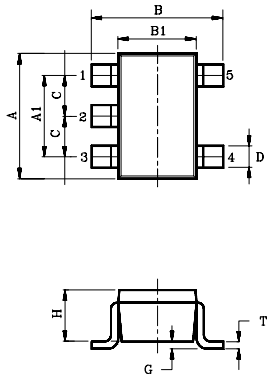
SEMICONDUCTOR
TECHNICAL DATA

KIC7SZ08FU
SILICON MONOLITHIC CMOS
DIGITAL INTEGRATED CIRCUIT

2 INPUT AND GATE

FEATURES

- High Output Drive : ±24mA (Typ.)
  @V_{CC}=3V
- Super High Speed Operation : t_{PD}=2.7ns(Typ.)
  @V_{CC}=5V, 50pF
- Operation Voltage Range : $V_{CC(opr)}$=1.8~5.5V.
- Supply Voltage Data Retention : V_{CC}=1.5~5.5V.
- 5V Tolerant Function



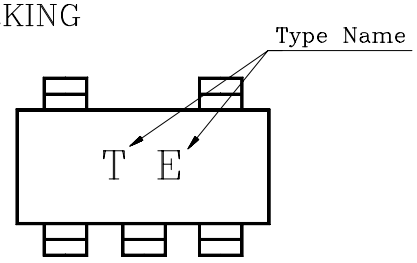
DIM	MILLIMETERS
A	2.00±0.20
A1	1.3±0.1
B	2.1±0.1
B1	1.25±0.1
C	0.65
D	0.2+0.10/−0.05
G	0~0.1
H	0.9±0.1
T	0.15+0.1/−0.05

USV

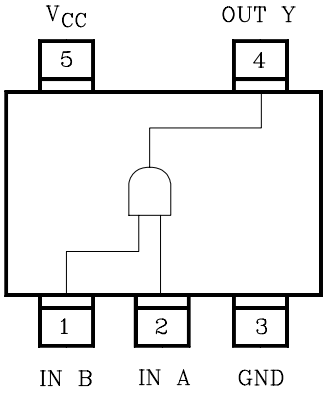
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~6	V
DC Input Voltage	V_{IN}	-0.5~6	V
DC Output Voltage	V_{OUT}	-0.5~6	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	200	mW
Storage Temperature	T_{stg}	-65~150	℃
Lead Temperature (10s)	T_L	260	℃

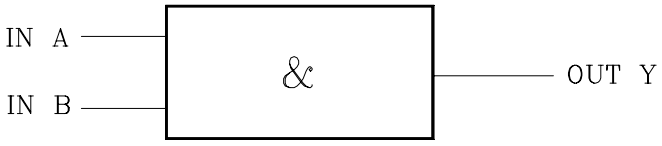
MARKING



PIN CONNECTION(TOP VIEW)



LOGIC DIAGRAM



CMOS 32-Bit Microcontrollers

TMP92CD28FG / TMP92CD28DFG

1. Outline and Device Characteristics

The TMP92CD28 is a high-speed advanced 32-bit Microcontroller developed for controlling equipment which processes mass data.

The TMP92CD28 has a high-performance CPU (900/H1 CPU) and various built-in I/Os.

The TMP92CD28FG and TMP92CD28DFG are housed in a 100-pin flat package.

Device characteristics are as follows:

(1) CPU: 32-bit CPU (900/H1 CPU)
- Compatible with 900/L1 instruction code
- 16 Mbytes of linear address space
- General-purpose register and register banks
- Micro DMA: 8 channels (250 ns/4 bytes at f_{SYS} = 20 MHz, best case)

(2) Minimum instruction execution time: 50 ns (at f_{SYS} = 20 MHz)

(3) Internal memory
- Internal RAM: 32-Kbytes
- Internal ROM: 512-Kbytes

(4) External memory expansion
- Expandable up to 16 Mbytes (Shared program/data area)
- Can simultaneously support 8- or 16-bit width external data bus
  ···Dynamic data bus sizing
- Separate bus system

(5) Memory controller
- Chip select output: 3 channels

(6) 8-bit timers: 6 channels

(7) 16-bit timers: 2 channels

(8) General-purpose serial interface: 2 channels
- UART/synchronous mode: 2 channels (channel 0 , and 1)
- IrDA ver.1.0 (115 kbps) mode selectable: 2 channels (channel 0 and 1)

(9) Serial bus interface: 2 channels
- I^2C bus mode
- Clock synchronous mode (only channel 1)

(10) SPI controller : 1 channel
- Supported up to SPI mode of SD card and MMC card
- Built-in FIFO buffer of 32 bytes to each Input/Output

(11) High Speed serial interface : 1 channel
- Built-in FIFO buffer of 32 bytes to each Input/Output

(12) USB Host Controller : 1chanel
- Universal Serial Bus Specification Rev2.0
- Open HCI for USB Release 1.0a
- 12Mbps – Full speed support. (Isochronous Transfer is not supported.)

(13) Watchdog timer

(14) Timer for real-time clock (RTC)

(15) Key-on wake up (only for HALT release):4 channels

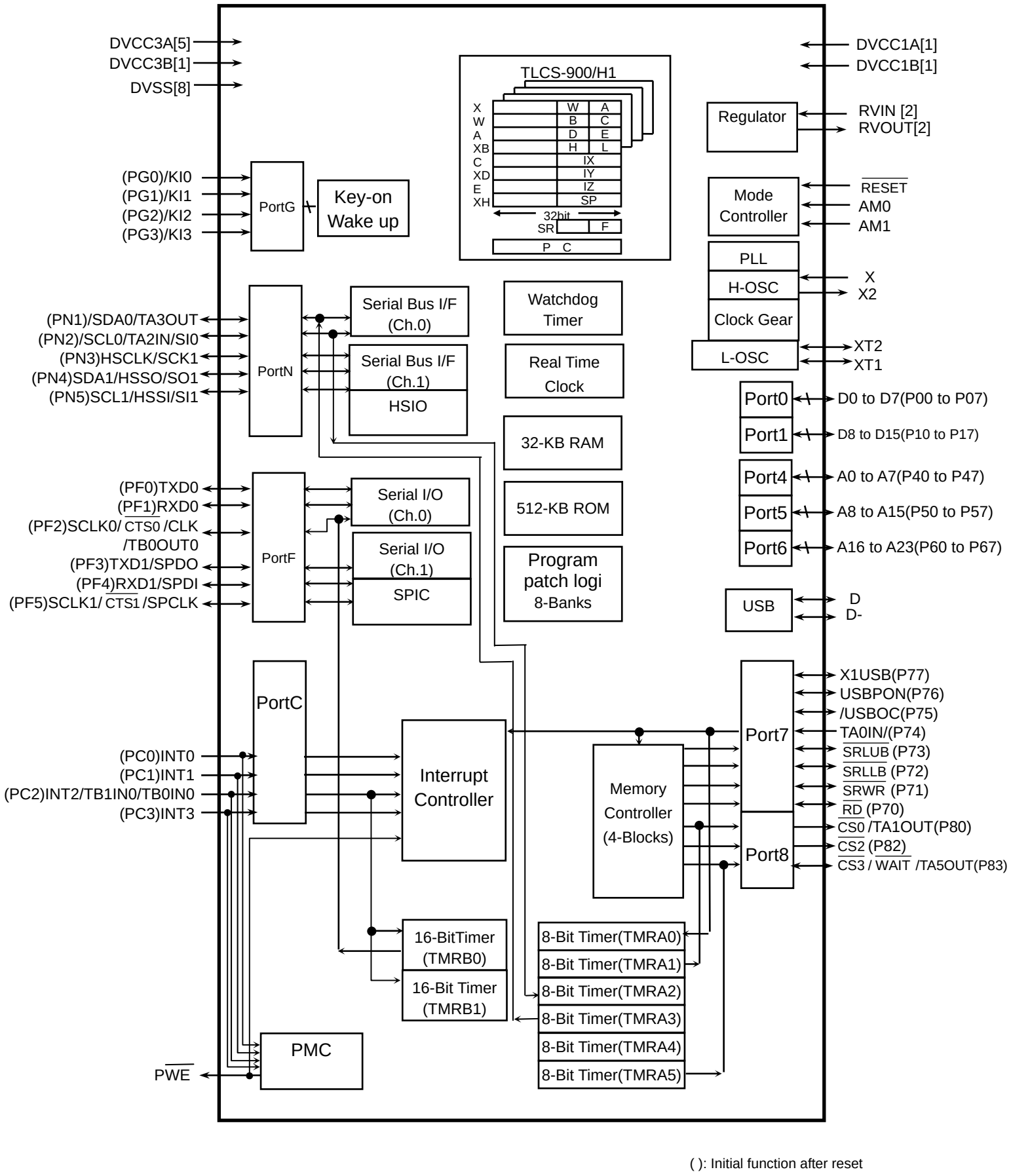
(16) Program patch logic: 8 banks

(17) Interrupts: 47interrupts
- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 34 internal interrupts: Seven selectable priority levels
- 4 external interrupts (INT0 to INT3): Seven selectable priority levels
  (INT0 to INT3 selectable edge or level interrupt)

(18) Input/output ports: 70pins

(19) Standby function
- Three HALT modes: IDLE2 (Programmable), IDLE1, STOP
- Power cut mode (Built-in power supply management circuits (PMC) for leak current provision.)

(20) Clock controller
- Built-in two blocks of clock doubler (PLL). PLL supplies 48 MHz for USB and 36 MHz for CPU from 9MHz
- Clock gear function: Select high-frequency clock fc to fc/16
- Special timer for CLOCK (fs = 32.768 kHz)



( ): Initial function after reset

Figure 1.1 TMP92CD28 Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins for the TMP92CD28, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP92CD28FG.

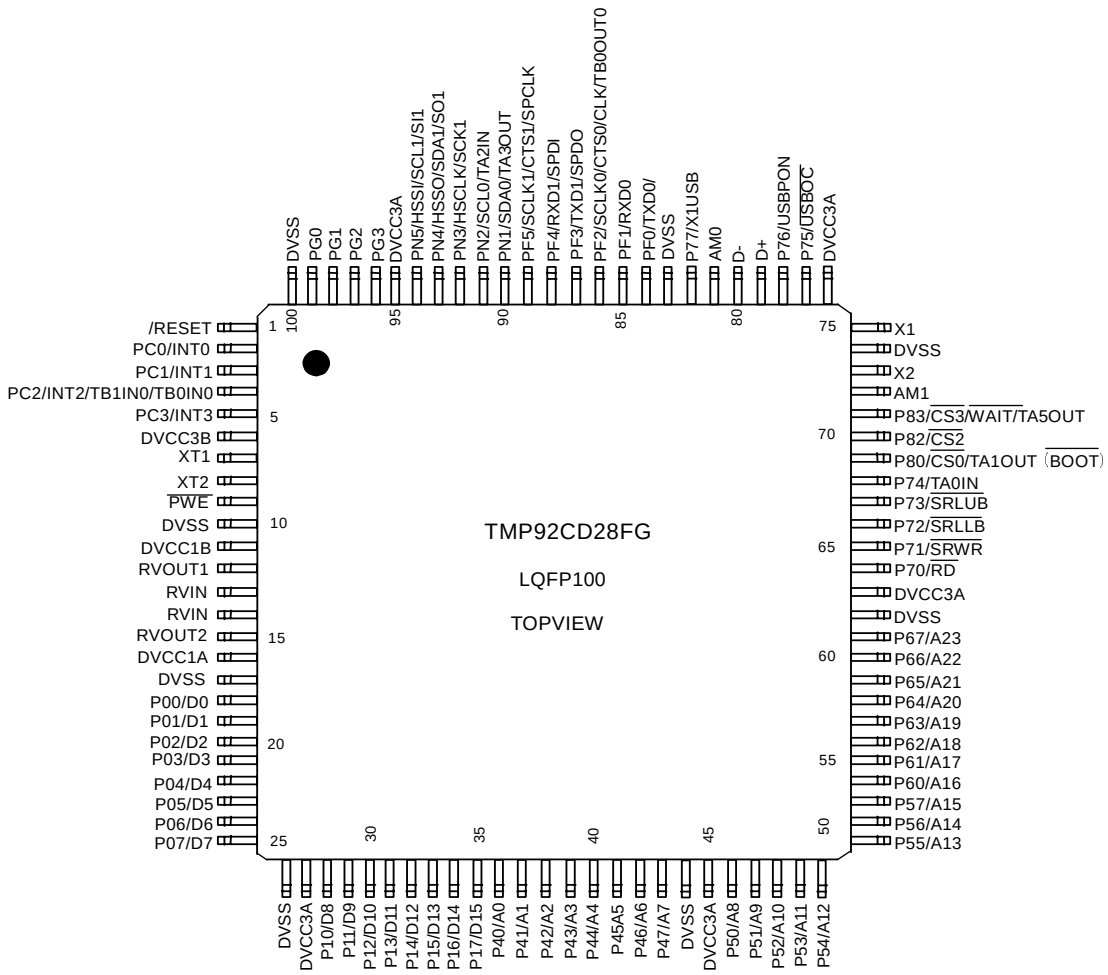


Figure 2.1.1 Pin Assignment Diagram (100-pin LQFP)

Figure 2.1.2 shows the pin assignment of the TMP92CD28DFG.

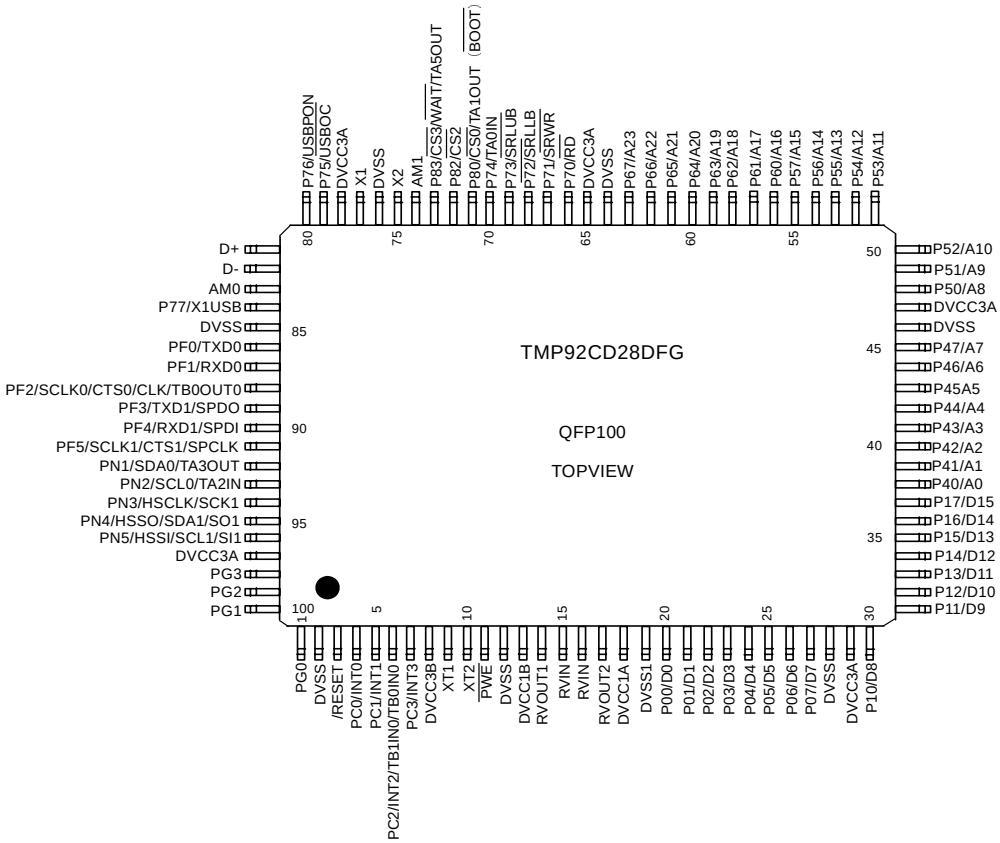


Figure 2.1.2 Pin Assignment Diagram (100-pin QFP)

2.2 Pin Names and Functions

The following table shows the names and functions of the input/output pins

Table 2.2.1 Pin Names and Functions (1/3)

Pin name	Number of Pin	I/O	Function
P00 to P07 D0 to D7	8	I/O I/O	Port 0: I/O port Input or output specifiable in units of bits Data: Data bus 0 to 7
P10 to P17 D8 to D15	8	I/O I/O	Port 1: I/O port Input or output specifiable in units of bits Data: Data bus 8 to 15
P40 to P47 A0 to A7	8	I/O Output	Port 4: I/O port Input or output specifiable in units of bits Address: Address bus 0 to 7
P50 to P57 A8 to A15	8	I/O Output	Port 5: I/O port Input or output specifiable in units of bits Address: Address bus 8 to 15
P60 to P67 A16 to A23	8	I/O Output	Port 6: I/O port Input or output specifiable in units of bits Address: Address bus 16 to 23
P70 $\overline{RD}$	1	I/O Output	Port 70: I/O port (Schmitt input, with pull-up register) Read: Outputs strobe signal for read external memory.
P71 $\overline{SRWR}$	1	I/O Output	Port 71: I/O port (Schmitt input, with pull-up register) Write enable for SRAM: Strobe signal for wiritng data.
P72 $\overline{SRLLB}$	1	I/O Output	Port 72: I/O port (Schmitt input, with pull-up register) Data enable for SRAM on pins D0 to D7
P73 $\overline{SRLUB}$	1	I/O Output	Port 73: I/O port (Schmitt input, with pull-up register) Data enable for SRAM on pins D8 to D15
P74 TA0IN	1	Input Input	Port 74: Input port (Schmitt input) 8-bit timer 0 input: Input pin of 8-bit timer TMRA0
P75 USBOC	1	I/O Input	Port 75: I/O port (Schmitt input) USBOC Input
P76 USBPON	1	I/O Output	Port 76: I/O port (Schmitt input) USBPON Output
P77 X1USB	1	I/O Input	Port 77: I/O port 48MHz Clock Input for USB Host Controller
P80 $\overline{CS0}$ TA1OUT ($\overline{BOOT}$ Note)	1	Output Output Output Input	Port 80: Output port Chip select 0: Outputs “Low” when address is within specified address area 8-bit timer 1 Output: Output pin of 8-bit timer TMRA0 or TMRA1 This pin sets single boot mode (only during reset). (Note) The function of TMP92FD28
P82 $\overline{CS2}$	1	Output Output	Port 82: Output port Chip select 2: Outputs “Low” when address is within specified address area
P83 $\overline{CS3}$ TA5OUT $\overline{WAIT}$	1	I/O Output Output Input	Port 83: I/O port Chip select 3: Outputs “Low” when address is within specified address area 8-bit timer 5 Output: Output pin of 8-bit timer TMRA4 or TMRA5 Wait: Signal used to request CPU bus wait
PC0 INT0	1	Input Input	Port C0: Input port (Schmitt input) Interrupt request pin0 : Interrupt request pin with programmable level/rising/falling edge
PC1 INT1	1	Input Input	Port C1: Input port (Schmitt input) Interrupt request pin 1 : Interrupt request pin with programmable level/rising/falling edge
PC2 INT2 TB0IN0 TB1IN0	1	Input Input Input Input	Port C2: Input port (Schmitt input) Interrupt request pin 2 : Interrupt request pin with programmable level/rising/falling edge 16-bit timer 0 input 0: Input of count/capture trigger in 16-bit timer TMRB0 16-bit timer 1 input 0: Input of count/capture trigger in 16-bit timer TMRB1
PC3 INT3	1	Input Input	Port C3: Input port (Schmitt input) Interrupt request pin 3 : Interrupt request pin with programmable level/rising/falling edge

Table 2.2.2 Pin Names and Functions (2/3)

Pin name	Number of Pin	I/O	Function
PF0	1	I/O	Port F0: I/O port (Schmitt input)
TXD0		Output	Serial 0 send data: Open drain output programmable
PF1	1	I/O	Port F1: I/O port (Schmitt input)
RXD0		Input	Serial 0 receive data
PF2	1	I/O	Port F2: I/O port (Schmitt input)
SCLK0		I/O	Serial 0 clock I/O
$\overline{\text{CTS0}}$		Input	Serial 0 data send enable (Clear to send)
CLK		Output	Clock: System Clock output
TB0OUT0		Output	16-bit timer 0 output 0: Output pin of 16-bit timer TMRB0
PF3	1	I/O	Port F3: I/O port (Schmitt input)
TXD1		Output	Serial 1 send data: Open drain output programmable
SPDO		Output	SPI Data output
PF4	1	I/O	Port F4: I/O port (Schmitt input)
RXD1		Input	Serial 1 receive data
SPDI		Input	SPI Data input
PF5	1	I/O	Port F5: I/O port (Schmitt input)
SCLK1		I/O	Serial 1 clock I/O
$\overline{\text{CTS1}}$		Input	Serial 1 data send enable (Clear to send)
SPCLK		Output	SPI Clock output
PG0 to PG3	4	Input	Port G: Input port (Schmitt input)
KI0 to KI3			Key input 0 to 7: Pin used of key-on wakeup 0 to 7

Table 2.2.3 Pin Names and Functions (3/3)

Pin name	Number of Pin	I/O	Function
PN1 SDA0 TA3OUT	1	I/O I/O Output	Port N1: I/O port (Schmitt input, Open drain output) Serial bus interface 0 send/receive data at I^2C mode 8-bit timer 3 Output: Output pin of 8-bit timer TMRA2 or TMRA3
PN2 SCL0 TA2IN	1	I/O I/O Input	Port N2: I/O port (Schmitt input, Open drain output) Serial bus interface 0 clock I/O data at I^2C mode 8-bit timer 2 input: Input pin of 8-bit timer TMRA2
PN3 SCK1 HSCLK	1	I/O I/O Output	Port N3: I/O port (Schmitt input) Serial bus interface 1 clock I/O data at SIO mode HSIO Clock output
PN4 SO1 SDA1 HSSO	1	I/O Output I/O Output	Port N4: I/O port (Schmitt input, Open drain output) Serial bus interface 1 send data at SIO mode Serial bus interface 1 send/receive data at I^2C mode HSIO Data output
PN5 SI1 SCL1 HSSI	1	I/O Input I/O Input	Port N5: I/O port (Schmitt input, Open drain output) Serial bus interface 1 receive data at SIO mode Serial bus interface 1 clock I/O data at I^2C mode HSIO Data input
AM0, AM1	2	Input	Operation mode: Fixed to AM1 = “1” and AM0 = “1”
X1 / X2	2	I/O	High-frequency oscillator connection I/O pins
XT1/XT2	2	I/O	Low-frequency oscillator circuit connection pin.
$\overline{\text{RESET}}$	1	Input	Reset: Intializes TMP92CD28 (Schmitt input, with pull-up register)
$\overline{\text{PWE}}$	1	Output	External power supply control output: Pin to control ON/OFF of external power supply. In stand-by mode, outputs “L” level. In other than stand-by mode, outputs “H” level.
D+, D-	2	I/O	Data pin connected to USB. In case USB is not used, connect both pins to pull-up(DVCC3A) or pull-down resistor for protect current flows it.
RVIN	2	Input	Power supply pin for Internal Regulator
RVOUT1, RVOUT2	2	Output	1.5V output from Internal Regulator (Only Mask ROM Version)
DVCC3A	5	–	Power supply pin for peripheral I/O-A (Connect all DVCC3A pins to power supply pin.)
DVCC3B	1	–	Power supply pin for peripheral I/O-B (Connect all DVCC3B pins to power supply pin.)
DVCC1A	1	–	Power supply pin for internal logic-A.
DVCC1B	1	–	Power supply pin for internal logic-B.
DVSS	8	–	GND pins (0 V) (All DVSS pins shold be connected with GND(0V))

KSZ8851SNL/SNLI

Single-Port Ethernet Controller with SPI Interface

Rev. 2.0

General Description

The KSZ8851SNL is a single-chip Fast Ethernet controller consisting of a 10/100 physical layer transceiver (PHY), a MAC, and a Serial Peripheral Interface (SPI). The KSZ8851SNL is designed to enable an Ethernet network connectivity with any host micro-controller equipped with SPI interface. The KSZ8851SNL offers the most cost-effective solution for adding high-throughput Ethernet link to traditional embedded systems with SPI interface.

The KSZ8851SNL is a single chip, mixed analog/digital device offering Wake-on-LAN technology for effectively addressing Fast Ethernet applications. It consists of a Fast Ethernet MAC controller, SPI interface and incorporates a unique dynamic memory pointer with 4-byte buffer boundary and a fully utilizable 18KB for both TX (allocated 6KB) and RX (allocated 12KB) directions in host buffer interface.

The KSZ8851SNL is designed to be fully compliant with the appropriate IEEE 802.3 standards. An industrial temperature-grade version of the KSZ8851SNL, the KSZ8851SNLI is also available (see “Ordering Information” section).

LinkMD®

Physical signal transmission and reception are enhanced through the use of analog circuitry, making the design more efficient and allowing for lower-power consumption. The KSZ8851SNL is designed using a low-power CMOS process that features a single 3.3V power supply with options for 1.8V, 2.5V or 3.3V VDD I/O. The device includes an extensive feature set that offers management information base (MIB) counters and a fast SPI interface with clock speed up to 40MHz.

The KSZ8851SNL includes unique cable diagnostics feature called LinkMD®. This feature determines the length of the cabling plant and also ascertains if there is an open or short condition in the cable. Accompanying software enables the cable length and cable conditions to be conveniently displayed. In addition, the KSZ8851SNL supports Hewlett Packard (HP) Auto-MDIX thereby eliminating the need to differentiate between straight or crossover cables in applications.

Functional Diagram

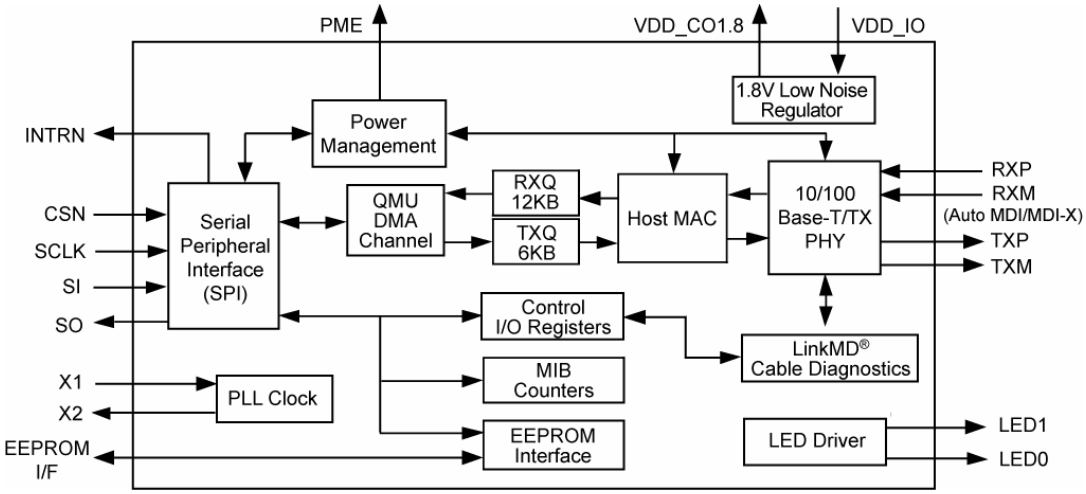


Figure 1. KSZ8851SNL/SNLI Functional Diagram

Features

- Integrated MAC and PHY Ethernet Controller fully compliant with IEEE 802.3/802.3u standards
- SPI Interface with clock speeds up to 40MHz for high throughput applications
- Supports 10BASE-T/100BASE-TX
- Supports IEEE 802.3x full-duplex flow control and half-duplex backpressure collision flow control
- Supports RXQ and TXQ FIFO DMA for fast data read and write transfers
- Supports IP Header (IPv4)/TCP/UDP/ICMP checksum generation and checking
- Supports IPv6 TCP/UDP/ICMP checksum generation and checking
- Automatic 32-bit CRC generation and checking
- Supports simple command and data phases in SPI cycle for RXQ/TXQ FIFO and registers read/write
- Supports multiple data frames for TXQ FIFO and RXQ FIFO without additional command phase
- Supports flexible Byte (8-bit), Word (16-bit) and Double word (32-bit) read/write access to internal registers
- Larger internal memory with 12K Bytes for RX FIFO and 6K Bytes for TX FIFO. Programmable low, high and overrun watermark for flow control in RX FIFO
- Efficient architecture design with configurable host interrupt schemes to minimize host CPU overhead and utilization
- Powerful and flexible address filtering scheme
- Optional to use external serial EEPROM configuration for MAC address
- Single 25MHz reference clock for both PHY and MAC
- HBM ESD Rating 6kV

Power Modes, Power Supplies, and Packaging

- Single 3.3V power supply with options for 1.8V, 2.5V and 3.3V VDD I/O
- Built-in integrated 3.3V or 2.5V to 1.8V low noise regulator (LDO) for core and analog blocks
- Enhanced power management feature with energy detect mode and soft power-down mode to ensure low-power dissipation during device idle periods
- Comprehensive LED indicator support for link, activity and 10/100 speed (2 LEDs)
  – User programmable
- Low-power CMOS design
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Available in 32-pin (5mm x 5mm) MLF® package

Additional Features

In addition to offering all of the features of a Layer 2 controller, the KSZ8851SNL offers:

- Supports to add two-byte before frame header in order for IP frame content with double word boundary
- Micrel LinkMD® cable diagnostic capabilities to determine cable length, diagnose faulty cables, and determine distance to fault
- Wake-on-LAN functionality
  – Incorporates Magic Packet™, wake-up frame, network link state, and detection of energy signal technology
- HP Auto MDI-X™ crossover with disable/enable option
- Ability to transmit and receive frames up to 2000 bytes

Network Features

- 10BASE-T and 100BASE-TX physical layer support
- Auto-negotiation: 10/100 Mbps full and half duplex
- Adaptive equalizer
- Baseline wander correction

Applications

- Video/Audio Distribution Systems
- Voice over IP (VoIP) and Analog Telephone Adapters (ATA)
- Building Automation
- Home Base Control with Ethernet Connection
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security, Motion Control and Surveillance Cameras

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet
- Embedded Systems

Pin Configuration

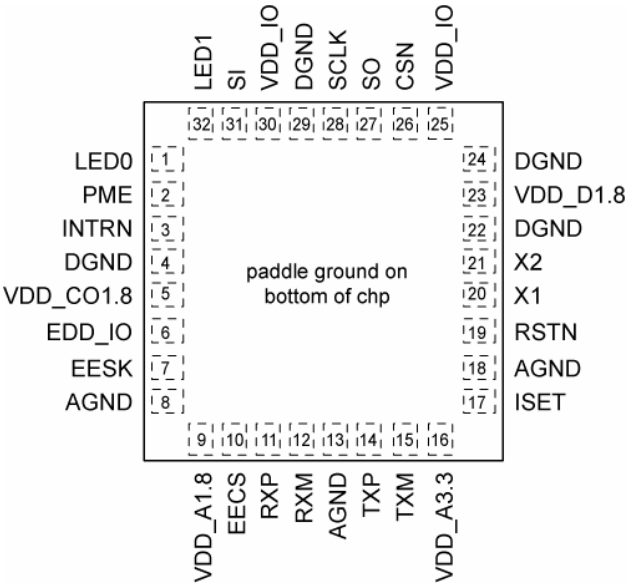


Figure 2. 32-Pin (5mm x 5mm) MLF®

Pin Description

Pin Number	Pin Name	Type	Pin Function
1	LED0	Opu	Programmable LED output to indicate PHY activity/status. LED is ON when output is LOW; LED is OFF when output is HIGH. LED indicators[1] defined as follows: Chip Global Control Register: CGCR bit [9] / 0 (Default) / 1 LED1 (pin 32) / 100BT / ACT LED0 (pin 1) / LINK/ACT / LINK Link (up) = LED On; Activity = LED Blink; Link/Act = LED On/Blink; Speed = LED On (100BASE-T); LED Off (10BASE-T)
2	PME	Opu	Power Management Event (default active low) It is asserted (low or high depends on polarity set in PMECR register) when one of the wake-on-LAN events is detected by KSZ8851SNL. The KSZ8851SNL is requesting the system to wake up from low power mode.
3	INTRN	Opu	Interrupt Not An active low signal to host CPU to indicate an interrupt status bit is set. This pin needs an external 4.7K pull-up resistor.
4	DGND	Gnd	Digital IO ground.
5	VDD_CO1.8	P	1.8V regulator output . This 1.8V output pin provides power to pins 9 (VDD_A1.8) and 23 (VDD_D1.8) for core VDD supply. If VDD_IO is set for 1.8V then this pin should be left floating, pins 9 (VDDA_1.8) and 23 (VDD_D1.8) will be sourced by the external 1.8V supply that is tied to pins 25 and 30 (VDD_IO) with appropriate filtering.
6	EED_IO	Ipd/O	In/Out Data from/to external EEPROM Config Mode: The pull-up/pull-down value is latched as with/without EEPROM during power-up / reset. See “Strapping Options” section for details.
7	EESK	Opd	EEPROM Serial Clock A 4μs (OBCR[1:0]=11 on-chip bus speed @ 25MHz) or 800ns (OBCR[1:0]=00 on-chip bus speed @ 125 MHz) serial output clock to load configuration data from the serial EEPROM.
8	AGND	Gnd	Analog ground.
9	VDD_A1.8	P	1.8V analog power supply from VDD_CO1.8 (pin 5) with appropriate filtering. If VDD_IO is 1.8V, this pin must be supplied power from the same source as pins 25 and 30 (VDD_IO) with appropriate filtering.
10	EECS	Opd	EEPROM Chip Select This signal is used to select an external EEPROM device.
11	RXP	I/O	Physical receive (MDI) or transmit (MDIX) signal (+ differential).
12	RXM	I/O	Physical receive (MDI) or transmit (MDIX) signal (– differential).
13	AGND	Gnd	Analog ground.
14	TXP	I/O	Physical transmit (MDI) or receive (MDIX) signal (+ differential).
15	TXM	I/O	Physical transmit (MDI) or receive (MDIX) signal (– differential).
16	VDD_A3.3	P	3.3V analog V_{DD} input power supply with well decoupling capacitors.
17	ISET	O	Set physical transmits output current. Pull-down this pin with a 3.01K 1% resistor to ground.
18	AGND	Gnd	Analog ground.
19	RSTN	Ipu	Reset Not.

Pin Number	Pin Name	Type	Pin Function
			Hardware reset pin (active Low). This reset input must be held low for a minimum of 10ms after stable supply voltage 3.3V.
20	X1	I	25MHz crystal or oscillator clock connection. Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock requirement is +/- 50ppm for either crystal or oscillator.
21	X2	O	
22	DGND	Gnd	Digital IO ground
23	VDD_D1.8	P	1.8V digital power supply from VDD_CO1.8 (pin 5) with appropriate filtering. If VDD_IO is 1.8V, this pin must be supplied power from the same source as pins 25 and 30 (VDD_IO) with appropriate filtering.
24	DGND	Gnd	Digital IO ground
25	VDD_IO	P	3.3V, 2.5V or 1.8V digital V_{DD} input power supply for IO with well decoupling capacitors.
26	CSN	Ipu	SPI slave mode: Chip Select Not Active low input pin for SPI interface.
27	SO	O	SPI slave mode: Serial data out for SPI interface. This SO is tri-stated output when CSN is negated and this pin must have external 4.7K pull-up to keep the SO line high while the driver is tri-stated.
28	SCLK	I	SPI slave mode: Serial clock input for SPI interface. This clock speed can run up to 40MHz.
29	DGND	Gnd	Digital IO ground
30	VDD_IO	P	3.3V, 2.5V or 1.8V digital V_{DD} input power supply for IO with well decoupling capacitors.
31	SI	Ipd	SPI slave mode: Serial data in for SPI interface.
32	LED1	Opu	Programmable LED1 output to indicate PHY activity/status (see LED0 description at pin1)

Legend:

P = Power supply Gnd = Ground

I/O = Bi-directional I = Input O = Output.

Ipd = Input with internal pull-down (58K +/-30%).

Ipu = Input with internal pull-up (58K +/-30%).

Opd = Output with internal pull-down (58K +/-30%).

Opu = Output with internal pull-up (58K +/-30%).

Ipu/O = Input with internal pull-up (58K +/-30%) during power-up/reset; output pin otherwise.

Ipd/O = Input with internal pull-down (58K +/-30%) during power-up/reset; output pin otherwise.

Strapping Options

Pin Number	Pin Name	Type	Pin Function
6	EED_IO	Ipd/O	EEPROM select: Pull-up = EEPROM present Floating (NC) or Pull-down = EEPROM not present (default) During power-up / reset, this pin value is latched into register CCR, bit 9

Note: Ipd/O = Input with internal pull-down (58K +/-30%) during power-up/reset; output pin otherwise.
Pin strap-ins are latched during power-up or reset.

TOSHIBA TC74HCU04AP/AF/AFN

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HCU04AP, TC74HCU04AF, TC74HCU04AFN

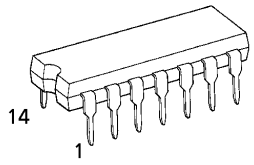
HEX INVERTER

(Note) The JEDEC SOP (FN) is not available in Japan.

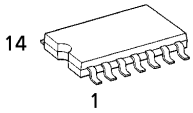
The TC74HCU04A is a high speed CMOS INVERTER fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Since the internal circit is composed of a single stage inverter, it can be used in analog applications such as crystal oscllators.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

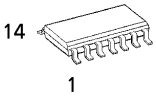
- High Speed ····· t_{pd} = 4ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 1μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIH}$ = 10% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ·· V_{CC}(opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS04



P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)

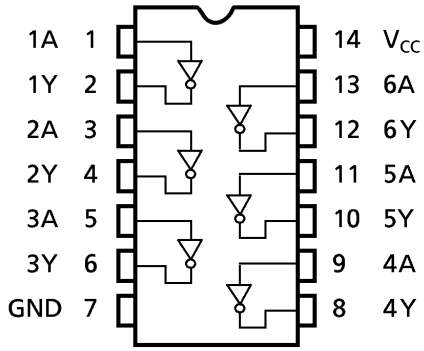


F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)



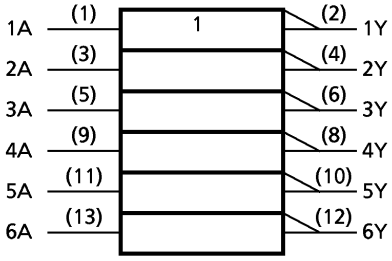
FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

961001EBA2

32-bit RISC Microcontroller – TX03 Series

TMPM333FDFG
TMPM333FYFG
TMPM333FWFG

1. Overview and Features

The TX03 series is a 32-bit RISC microcontroller series with an ARM Cortex™-M3 microcontroller core.

Features of the TMPM333FDFG/FYFG/FWFG are as follows:

1.1 Features

(1) ARM Cortex-M3 microcontroller core

1) Improved code efficiency has been realized through the use of Thumb®-2 instruction
- New 16-bit Thumb instructions for improved program flow
- New 32-bit Thumb instructions for improved performance
- Auto-switching between 32-bit instruction and 16-bit instruction is executed by compiler.

2) Both high performance and low power consumption have been achieved.

-High performance
- A 32-bit multiplication (32×32=32 bit) can be executed with one clock.
- Division takes between 2 and 12 cycles depending on dividend and devisor

-Low power consumption
- Optimized design using a low power consumption library
- Standby function that stops the operation of the microcontroller core

3) High-speed interrupt response suitable for real-time control
- An interruptible long instruction.
- Stack push automatically handled by hardware.

(2) On Chip program memory and data memory

Product name	On chip Flash ROM	On chip RAM
TMPM333FDFG	512Kbyte	32Kbyte
TMPM333FYFG	256Kbyte	16Kbyte
TMPM333FWFG	128Kbyte	8Kbyte

(3) 16-bit timer : 10 channels
- 16-bit interval timer mode
- 16-bit event counter mode
- 16-bit PPG output
- Input capture function

(4) Real time clock (RTC) : 1 channel
- Clock (hour, minute and second)
- Calendar (Month, week, date and leap year)
- Time correction + or − 30 seconds (by software)
- Alarm (Alarm output)
- Alarm interrupt

(5) Watchdog timer : 1 channel
- 26 cycles of binary counter
- Watchdog timer out

(6) General-purpose serial interface : 3 channels
- Either UART mode or synchronous mode can be selected (4byte FIFO equipped)

(7) Serial bus interface : 3 channels
- Either I^2C bus mode or synchronous mode can be selected.

(8) 10-bit A/D converter : 12 channels
- Start by an internal or external timer trigger
- Fixed channel/scan mode
- Single/repeat mode
- AD monitoring 2ch
- Conversion speed 1.15usec(@fsys = 40MHz)

(9) Interrupt source
- Internal: 38 factors…The order of precedence can be set over 7 levels (except the watchdog timer interrupt).
- External: 8 factors…The order of precedence can be set over 7 levels.

(10) Input/ output ports
- 79 pins

(11) Standby mode

- Standby modes :IDLE, SLOW, SLEEP, STOP
- Sub clock operation(32.768kHz) :SLOW, SLEEP

(12) Clock generator

- On-chip PLL (quadrupled)
- Clock gear function: The high-speed clock can be divided into 1/1, 1/2, 1/4 or 1/8.

(13) Endian

- Little endian

(14) Maximum operating frequency

- 40MHz

(15) Operating voltage range

- 2.7V~3.6V (with on-chip regulator)

(16) Temperature range

- -20~85 degrees (except during Flash writing/ erasing)
- 0~70 degrees (during Flash writing/ erasing)

(17) Package

- LQFP100-P-1414-0.5H (14mm × 14mm, 0.5mm pitch)

1.2 Block Diagram

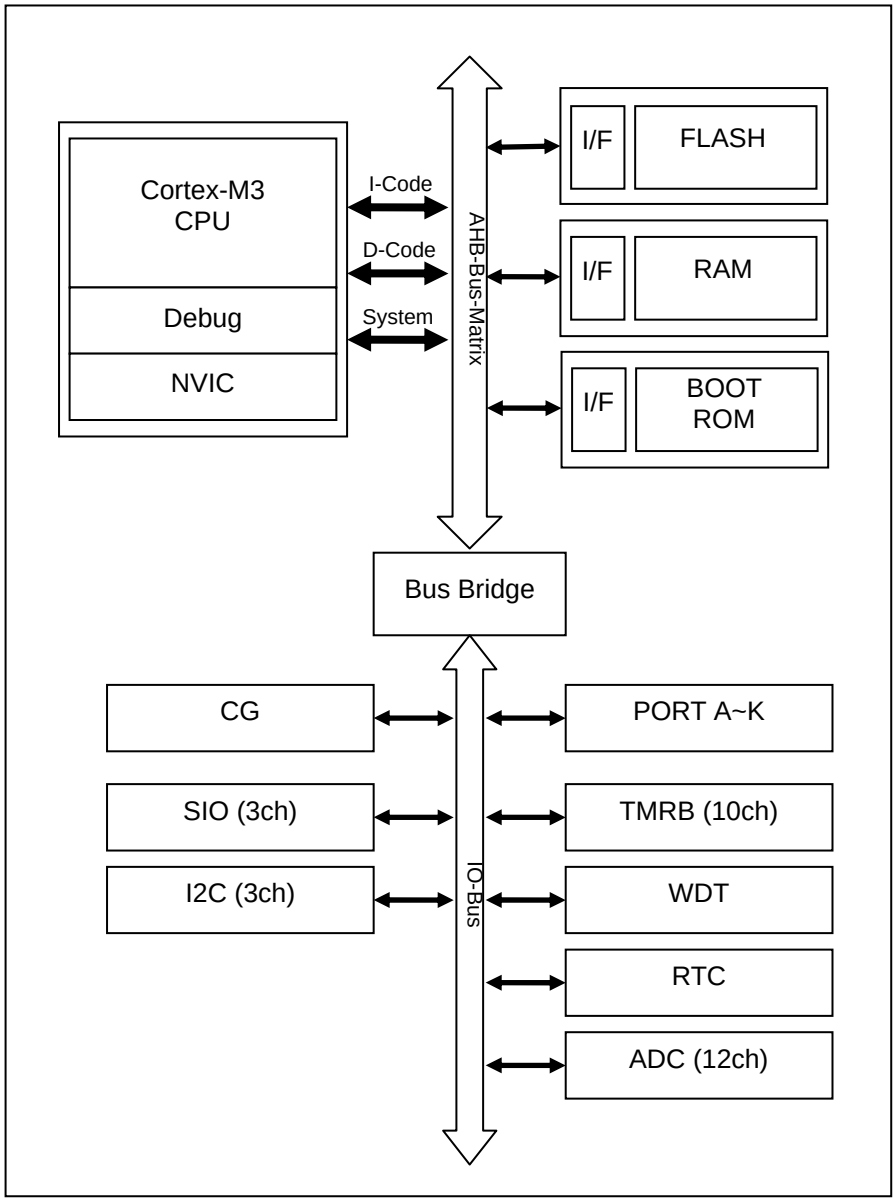


Fig. 1-1 TMPM333 FDFG/FYFG/FWFG Block Diagram

2 Pin Layout and Pin Functions

This chapter describes the pin layout, pin names and pin functions of TMPM333FDFG/ TMPM333FYFG/ TMPM333FWFG.

2.1 Pin Layout (Top view)

Fig.2-1 shows the pin layout of TMPM333FDFG/TMPM333FYFG/TMPM333FWF.

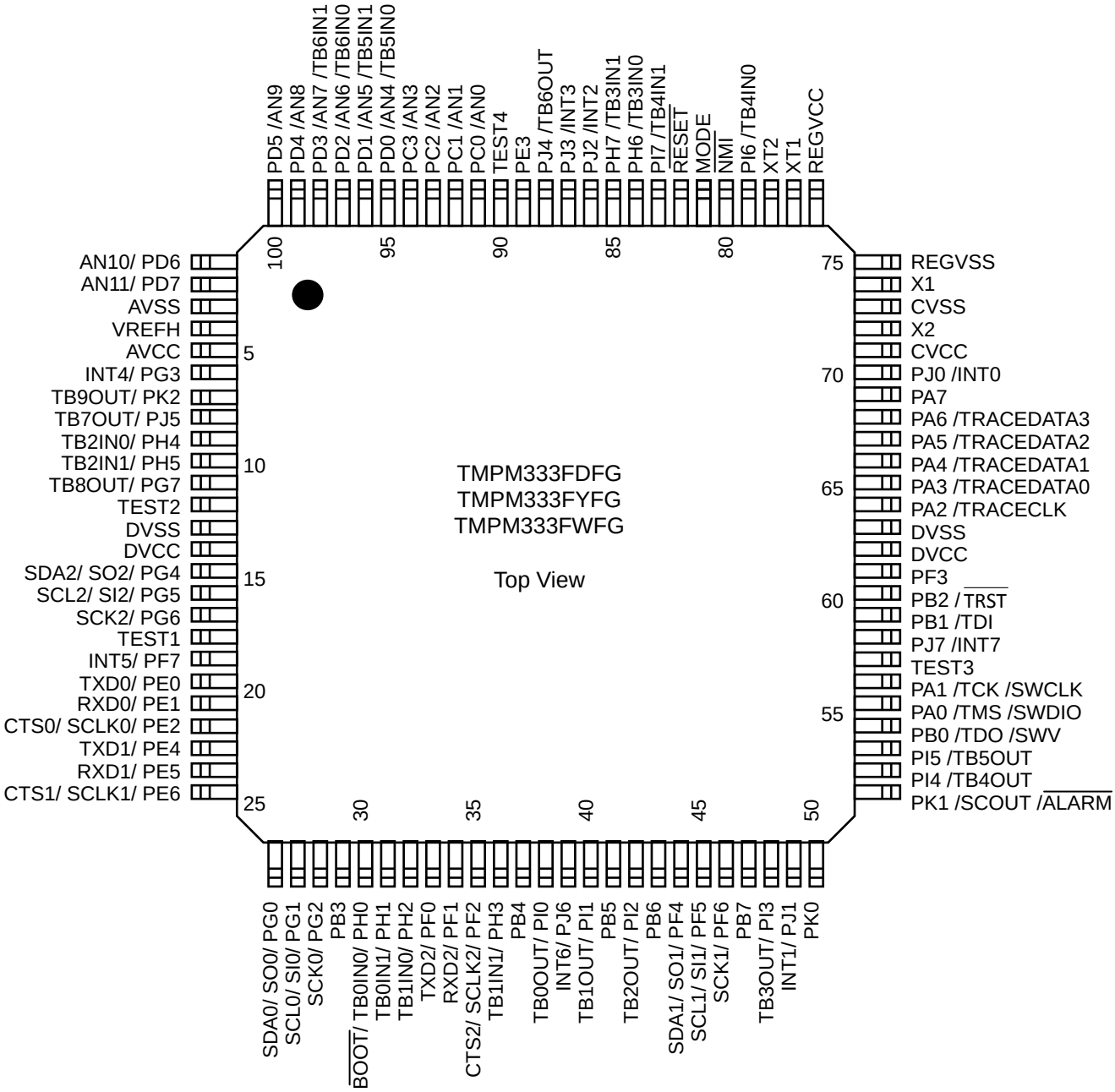


Fig.2-1 Pin Layout (LQFP100)

Table2-1 Pin Numbers and Names (1/2)

Pin No.	Pin name	Pin No.	Pin name
1	PD6, AN10	26	PG0, SO0, SDA0
2	PD7, AN11	27	PG1, SI0, SCL0
3	AVSS	28	PG2, SCK0
4	VREFH	29	PB3
5	AVCC	30	PH0, TB0IN0, $\overline{\text{BOOT}}$
6	PG3, INT4	31	PH1, TB0IN1
7	PK2, TB9OUT	32	PH2, TB1IN0
8	PJ5, TB7OUT	33	PF0, TXD2
9	PH4, TB2IN0	34	PF1, RXD2
10	PH5, TB2IN1	35	PF2, SCLK2, CTS2
11	PG7, TB8OUT	36	PH3, TB1IN1
12	TEST2	37	PB4
13	DVSS	38	PI0, TB0OUT
14	DVCC	39	PJ6, INT6
15	PG4, SO2, SDA2	40	PI1, TB1OUT
16	PG5, SI2, SCL2	41	PB5
17	PG6, SCK2	42	PI2, TB2OUT
18	TEST1	43	PB6
19	PF7, INT5	44	PF4, SO1, SDA1
20	PE0, TXD0	45	PF5, SI1, SCL1
21	PE1, RXD0	46	PF6, SCK1
22	PE2, SCLK0, CTS0	47	PB7
23	PE4, TXD1	48	PI3, TB3OUT
24	PE5, RXD1	49	PJ1, INT1
25	PE6, SCLK1, CTS1	50	PK0,

2 **Pin Layout and Pin Functions**

Table2-1 Pin Numbers and Names (2/2)

Pin No.	Pin name	Pin No.	Pin name
51	PK1, SCOUT, $\overline{\text{ALARM}}$	76	REGVCC
52	PI4, TB4OUT	77	XT1
53	PI5, TB5OUT	78	XT2
54	PB0, TDO, SWV	79	PI6, TB4IN0
55	PA0, TMS, SWDIO	80	$\overline{\text{NMI}}$
56	PA1, TCK, SWCLK	81	MODE
57	TEST3	82	$\overline{\text{RESET}}$
58	PJ7, INT7	83	PI7, TB4IN1
59	PB1, TDI	84	PH6, TB3IN0
60	PB2, $\overline{\text{TRST}}$	85	PH7, TB3IN1
61	PF3	86	PJ2, INT2
62	DVCC	87	PJ3, INT3
63	DVSS	88	PJ4, TB6OUT
64	PA2, TRACECLK	89	PE3
65	PA3, TRACEDATA0	90	TEST4
66	PA4, TRACEDATA1	91	PC0, AN0
67	PA5, TRACEDATA2	92	PC1, AN1
68	PA6, TRACEDATA3	93	PC2, AN2
69	PA7	94	PC3, AN3
70	PJ0, INT0	95	PD0, AN4, TB5IN0
71	CVCC	96	PD1, AN5, TB5IN1
72	X2	97	PD2, AN6, TB6IN0
73	CVSS	98	PD3, AN7, TB6IN1
74	X1	99	PD4, AN8
75	REGVSS	100	PD5, AN9

2.2 Pin names and Functions

Table2-2 and Table2-3 sort the input and output pins of the TMPM333FDFG/ TMPM333FYFG/ TMPM333FWFG by pin or port. Each table includes alternate pin names and functions for multi-function pins.

2.2.1 Sorted by Pin

Table2-2 Pin Names and Functions Sorted by Pin (1/5)

Type	# of Pins	Pin Name	Input/ Output	Function	Programmable Pull up/ Pull down	Schmitt trigger	Programmable Open Drain Output
Function	1	PD6 AN10	I I	Input port Analog input	Pull up	-	-
	2	PD7 AN11	I I	Input port Analog input	Pull up	-	-
PS	3	AVSS	I	A/D converter: GND pin (0V) Tie AVSS to power supply even if the A/D converter is not used.	-	-	-
	4	VREFH	I	Supplying the A/D converter with a reference power supply. Tie VREFH to power supply even if the A/D converter is not used.	-	-	-
	5	AVCC	I	Supplying the A/D converter with a power supply. Tie AVCC to power supply even if the A/D converter is not used.	-	-	-
Function	6	PG3 INT4	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
	7	PK2 TB9OUT	I/O O	I/O port Timer B output	Pull up	-	-
	8	PJ5 TB7OUT	I/O I	I/O port Timer B output	Pull up	-	-
	9	PH4 TB2IN0	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	10	PH5 TB2IN1	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	11	PG7 TB8OUT	I/O O	I/O port Timer B output	Pull up	-	○
Test	12	TEST2	-	TEST pin: Not connected.	-	-	-
PS	13	DVSS	-	GND pin	-	-	-
	14	DVCC	-	Power supply pin	-	-	-
Function	15	PG4 SDA2/ SO2	I/O I/O O	I/O port If the serial bus interface operates -in the I2C mode : data pin -in the SIO mode: data pin	Pull up	○	○
	16	PG5 SCL2/ SI2	I/O I/O I	I/O port If the serial bus interface operates -in the I2C mode : clock pin -in the SIO mode: data pin	Pull up	○	○
	17	PG6 SCK2	I/O I/O	I/O port Inputting and outputting a clock if the serial bus interface operates in the SIO mode.	Pull up	○	○
Test	18	TEST1	-	TEST pin: Not connected.	-	-	-
Function	19	PF7 INT5	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○

2 **Pin Layout and Pin Functions**

Table2-2 Pin Names and Functions Sorted by Pin (2/5)

Type	# of Pins	Pin Name	Input/ Output	Function	Programmable Pull-up/ Pull down	Schmitt trigger	Programmable Open Drain Output
Function	20	PE0 TXD0	I/O O	I/O port Sending serial data	Pull up	-	○
	21	PE1 RXD0	I/O I	I/O port Receiving serial data	Pull up	○	○
	22	PE2 SCLK0 CTS0	I/O I I	I/O port Serial clock input/ output Handshake input pin	Pull up	○	○
	23	PE4 TXD1	I/O O	I/O port Sending serial data	Pull up	-	○
	24	PE5 RXD1	I/O I	I/O port Receiving serial data	Pull up	○	○
	25	PE6 SCLK1 CTS1	I/O I I	I/O port Serial clock input/ output Handshake input pin	Pull up	○	○
	26	PG0 SDA0/ SO0	I/O I/O O	I/O port If the serial bus interface operates -in the I2C mode : data pin -in the SIO mode: data pin	Pull up	○	○
	27	PG1 SCL0/ SI0	I/O I/O I	I/O port If the serial bus interface operates -in the I2C mode : clock pin -in the SIO mode: data pin	Pull up	○	○
	28	PG2 SCK0	I/O I/O	I/O port Inputting and outputting a clock if the serial bus interface operates in the SIO mode.	Pull up	○	○
	29	PB3	I/O	I/O port	Pull up	-	-
Function/ Control	30	PH0 TB0IN0 $\overline{\text{BOOT}}$	I/O I I	I/O port Inputting the timer B capture trigger Setting a single boot mode: This pin goes into single boot mode by sampling "L" at the rise of a reset signal.	Pull up	○	-
Function	31	PH1 TB0IN1	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	32	PH2 TB1IN0	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	33	PF0 TXD2	I/O O	I/O port Sending serial data	Pull up	-	○
	34	PF1 RXD2	I/O I	I/O port Receiving serial data	Pull up	○	○
	35	PF2 SCLK2 CTS2	I/O I I	I/O port Serial clock input/ output Handshake input pin	Pull up	○	○
	36	PH3 TB1IN1	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	37	PB4	I/O	I/O port	Pull up	-	-
	38	PI0 TB0OUT	I/O O	I/O port Timer B output	Pull up	-	-
	39	PJ6 INT6	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○

Table2-2 Pin Names and Functions Sorted by Pin (3/5)

Type	# of Pins	Pin Name	Input/ Output	Function	Programmable Pull-up/ Pull down	Schmitt trigger	Programmable Open Drain Output
Function	40	PI1 TB1OUT	I/O O	I/O port Timer B output	Pull up	-	-
	41	PB5	I/O	I/O port	Pull up	-	-
	42	PI2 TB2OUT	I/O O	I/O port Timer B output	Pull up	-	-
	43	PB6	I/O	I/O port	Pull up	-	-
	44	PF4 SDA1/ SO1	I/O I/O O	I/O port If the serial bus interface operates -in the I2C mode : data pin -in the SIO mode: data pin	Pull up	○	○
	45	PF5 SCL1/ SI1	I/O I/O I	I/O port If the serial bus interface operates -in the I2C mode : clock pin -in the SIO mode: data pin	Pull up	○	○
	46	PF6 SCK1	I/O I/O	I/O port Inputting and outputting a clock if the serial bus interface operates in the SIO mode.	Pull up	○	○
	47	PB7	I/O	I/O port	Pull up	-	-
	48	PI3 TB3OUT	I/O O	I/O port Timer B output	Pull up	-	-
	49	PJ1 INT1	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
	50	PK0	I/O	I/O port	-	○	● (Note 4)
	51	PK1 SCOUT $\overline{\text{ALARM}}$	I/O O O	I/O port System clock output Alarm output	Pull up	-	-
	52	PI4 TB4OUT	I/O O	I/O port Timer B output	Pull up	-	-
	53	PI5 TB5OUT	I/O O	I/O port Timer B output	Pull up	-	-
Function/ Debug	54	PB0 TDO/SWV	I/O O	I/O port Debug pin	Pull up	-	-
	55	PA0 TMS/SWDIO	I/O I/O	I/O port Debug pin	Pull up	○	-
	56	PA1 TCK/ SWCLK	I/O I	I/O port Debug pin	Pull up	-	-
Test	57	TEST3	-	TEST pin: Not connected.	-	-	-
Function	58	PJ7 INT7	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
Function/ Debug	59	PB1 TDI	I/O I	I/O port Debug pin	Pull up	-	-
	60	PB2 $\overline{\text{TRST}}$	I/O I	I/O port Debug pin	Pull up	○	-
Function	61	PF3	I/O	I/O port	Pull up	○	○
PS	62	DVCC	-	Power supply pin	-	-	-
	63	DVSS	-	GND pin	-	-	-

2 **Pin Layout and Pin Functions**

Table2-2 Pin Names and Functions Sorted by Pin (4/5)

Type	# of Pins	Pin Name	Input/ Output	Function	Programmable Pull-up/ Pull down	Schmitt trigger	Programmable Open Drain Output
Function/ Debug	64	PA2 TRACECLK	I/O O	I/O port Debug pin	Pull up	-	-
	65	PA3 TRACEDATA0	I/O O	I/O port Debug pin	Pull up	-	-
	66	PA4 TRACEDATA1	I/O O	I/O port Debug pin	Pull up	-	-
	67	PA5 TRACEDATA2	I/O O	I/O port Debug pin	Pull up	-	-
	68	PA6 TRACEDATA3	I/O O	I/O port Debug pin	Pull up	-	-
Function	69	PA7	I/O	I/O port	Pull up		
	70	PJ0 INT0	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
PS	71	CVCC	-	Power supply pin	-	-	-
Clock	72	X2	O	Connected to a high-speed oscillator.	-	-	-
PS	73	CVSS	-	GND pin	-	-	-
Clock	74	X1	I	Connected to a high-speed oscillator.	-	○	-
PS	75	REGVSS	-	GND pin	-	-	-
	76	REGVCC	-	Power supply pin	-	-	-
Clock	77	XT1	I	Connected to a low-speed oscillator.	-	○	-
	78	XT2	O	Connected to a low-speed oscillator.	-	-	-
Function	79	PI6 TB4IN0	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	80	$\overline{\text{NMI}}$	I	Non-maskable interrupt	-	○ w/ noise filter	-
Control	81	MODE	I	Mode pin: Tied to GND pin	-	○	-
Function	82	$\overline{\text{RESET}}$	I	Reset input pin	Tied to Pull up	○ w/ noise filter	-
	83	PI7 TB4IN0	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	84	PH6 TB3IN0	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	85	PH7 TB3IN1	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	86	PJ2 INT2	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
	87	PJ3 INT3	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
	88	PJ4 TB6OUT	I/O O	I/O port Timer B output	Pull up	-	-
	89	PE3	I/O	I/O port	Pull up	○	○
Test	90	TEST4	-	TEST pin: Not connected.	-	-	-

Table2-2 Pin Names and Functions Sorted by Pin (5/5)

Type	# of Pins	Pin Name	Input/ Output	Function	Programmable Pull-up/ Pull down	Schmitt trigger	Programmable Open Drain Output
Function	91	PC0 AN0	I I	Input port Analog input	Pull up	-	-
	92	PC1 AN1	I I	Input port Analog input	Pull up	-	-
	93	PC2 AN2	I I	Input port Analog input	Pull up	-	-
	94	PC3 AN3	I I	Input port Analog input	Pull up	-	-
	95	PD0 AN4 TB5IN0	I I I	Input port Analog input Inputting the timer B capture trigger	Pull up	-	-
	96	PD1 AN5 TB5IN1	I I I	Input port Analog input Inputting the timer B capture trigger	Pull up	-	-
	97	PD2 AN6 TB6IN0	I I I	Input port Analog input Inputting the timer B capture trigger	Pull up	-	-
	98	PD3 AN7 TB6IN1	I I I	Input port Analog input Inputting the timer B capture trigger of	Pull up	-	-
	99	PD4 AN8	I I	Input port Analog input	Pull up	-	-
	100	PD5 AN9	I I	Input port Analog input	Pull up	-	-

(Note 1) TEST1 through 4 must be left unconnected.
(Note 2) Be sure to tie MODE to GND.
(Note 3) Tie VREFH/ AVCC to power supply and AVSS to GND even if the A/D converter is not used.
(Note 4) Nch open drain port.
(Note 5) The noise elimination width of the noise filter is approximately 30 ns under typical conditions.

TOSHIBA TC74VHC153F/FN/FT/FK

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC153F,TC74VHC153FN,TC74VHC153FT,TC74VHC153FK

Dual 4-Channel Multiplexer

The TC74VHC153 is an advanced high speed CMOS DUAL 4-CHANNEL MULTIPLEXERs fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Each of these data (1C0-1C3, 2C0-2C3) is selected by the two address inputs A and B.

Separate strobe inputs ($1\overline{G}$, $2\overline{G}$) are provided for each of the two four-line sections.

The strobe input ($\overline{G}$) can be used to inhibit the data output; the output is fixed in low level while the strobe input is held high.

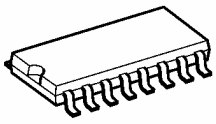
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High speed: t_{pd} = 5.0 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2 to 5.5 V
- Pin and function compatible with 74ALS153

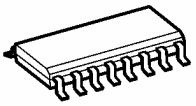
Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74VHC153F



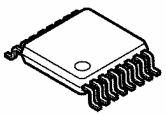
SOP16-P-300-1.27A

TC74VHC153FN



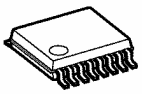
SOL16-P-150-1.27

TC74VHC153FT



TSSOP16-P-0044-0.65A

TC74VHC153FK



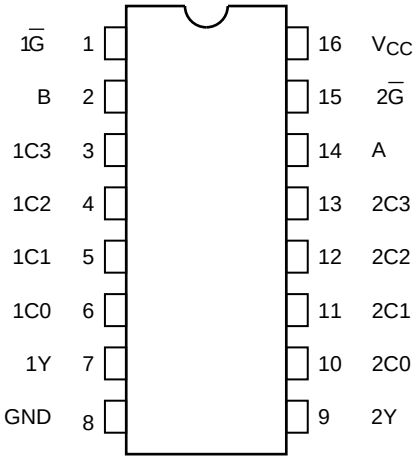
VSSOP16-P-0030-0.50

Weight

SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)
TSSOP16-P-0044-0.65A	: 0.06 g (typ.)
VSSOP16-P-0030-0.50	: 0.02 g (typ.)

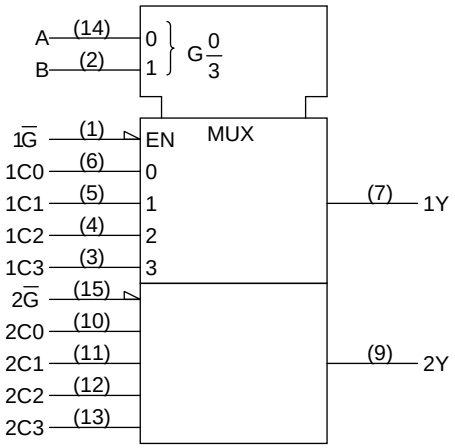
TOSHIBA TC74VHC153F/FN/FT/FK

Pin Assignment



(top view)

IEC Logic Symbol

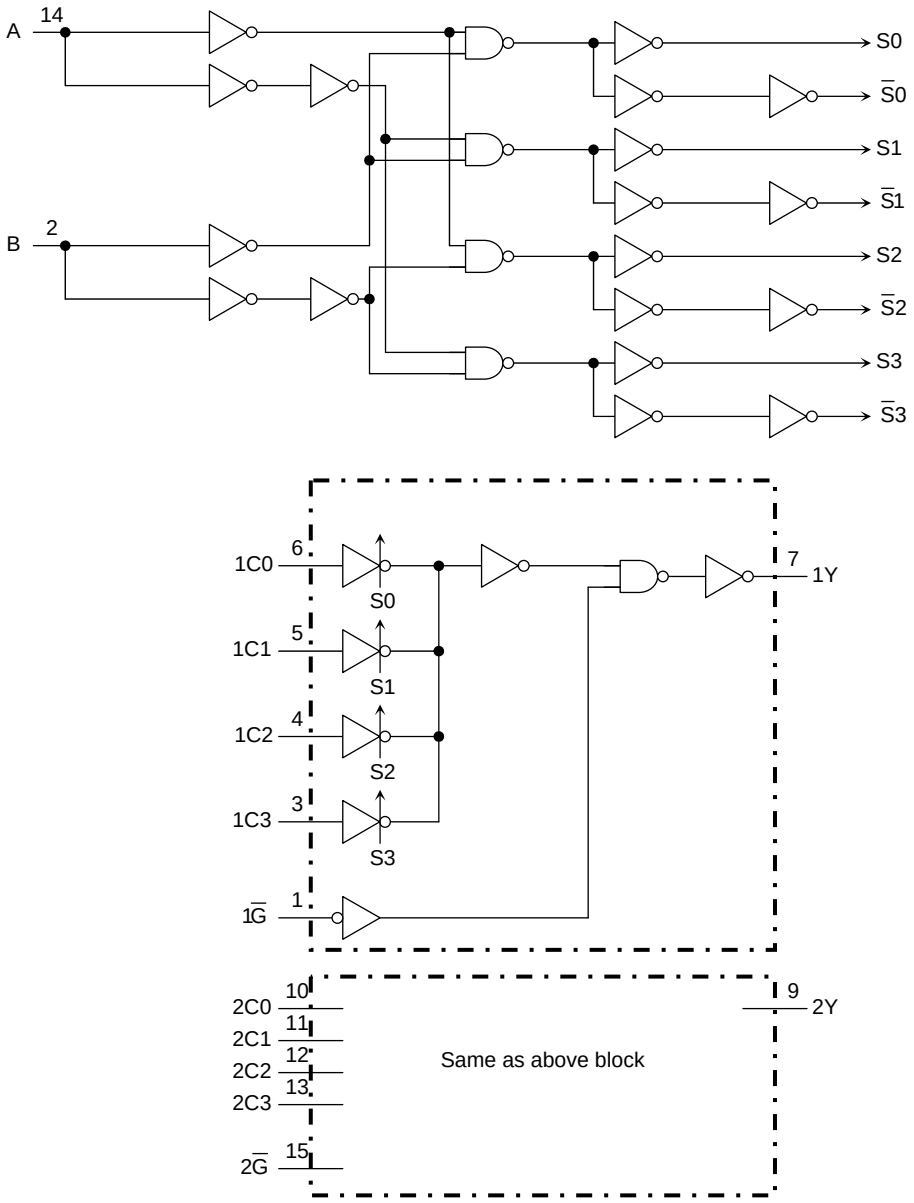


Truth Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

X: Don't care

System Diagram



CS49DV8C Data Sheet

FEATURES

- 32-bit Post-Processor Audio DSP supports Multichannel Dolby® Volume
- Programmable through DSP Composer™
- CS49DV8, supports up to 7.1 Channels of Dolby Volume processing at 48 kHz, 44.1 kHz or 32 kHz.
  - Input Configurable for all input/output digital audio types (I^2S, LJ/RJ, and TDM)
  - 32-bit data path delivers uncompromised dynamic range
  - 192 kHz capable integrated S/PDIF transmitter
  - DAO can operate in master or slave mode (SCLK & LRCLK)
- Integrated Clock Manager/PLL
  - Capable of operating from a wide variety of external crystals or external oscillators
- Input Fs Auto Detection, Reporting and Handling
- Sample rate conversion.
- Master & Slave Host Boot Capability via Serial Interface
- SPI interface capable of running up to 25 MHz during run time
- 1.8V Core and a 3.3V I/O that is tolerant to 5V input

32-bit Dual Audio DSP Engine featuring Multichannel Dolby® Volume

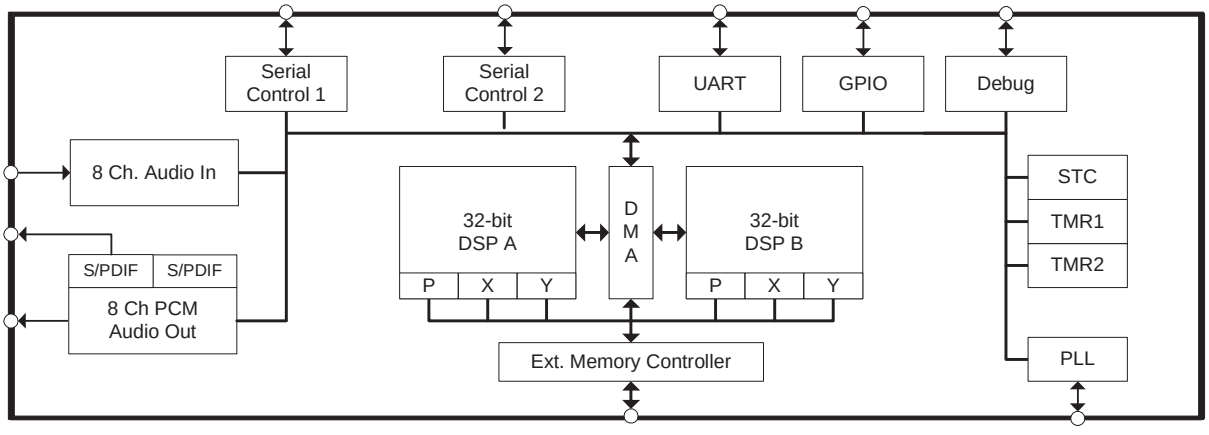
The new CS49DV8C is the fastest time-to-market, mass-production ready Multichannel Dolby Volume solution available. The target applications for the CS49DV8C DSP are:

- Soundbars
- DTVs with Integrated Soundbars
- HDTV Stands/Furniture with Integrated Soundbars
- Automotive Head Units
- Automotive Outboard Amplifiers
- Blu-ray Disc® & DVD Receivers / HTiBs

All of these applications and many more that use volume control and are subject to playback from sources that do not have consistent volume levels will benefit from the CS49DV8C Dolby Volume solution.

Ordering Information

See page 27 for ordering information.



Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

8. Device Pin-Out Diagram

8.1 128-Pin LQFP Pin-Out Diagram

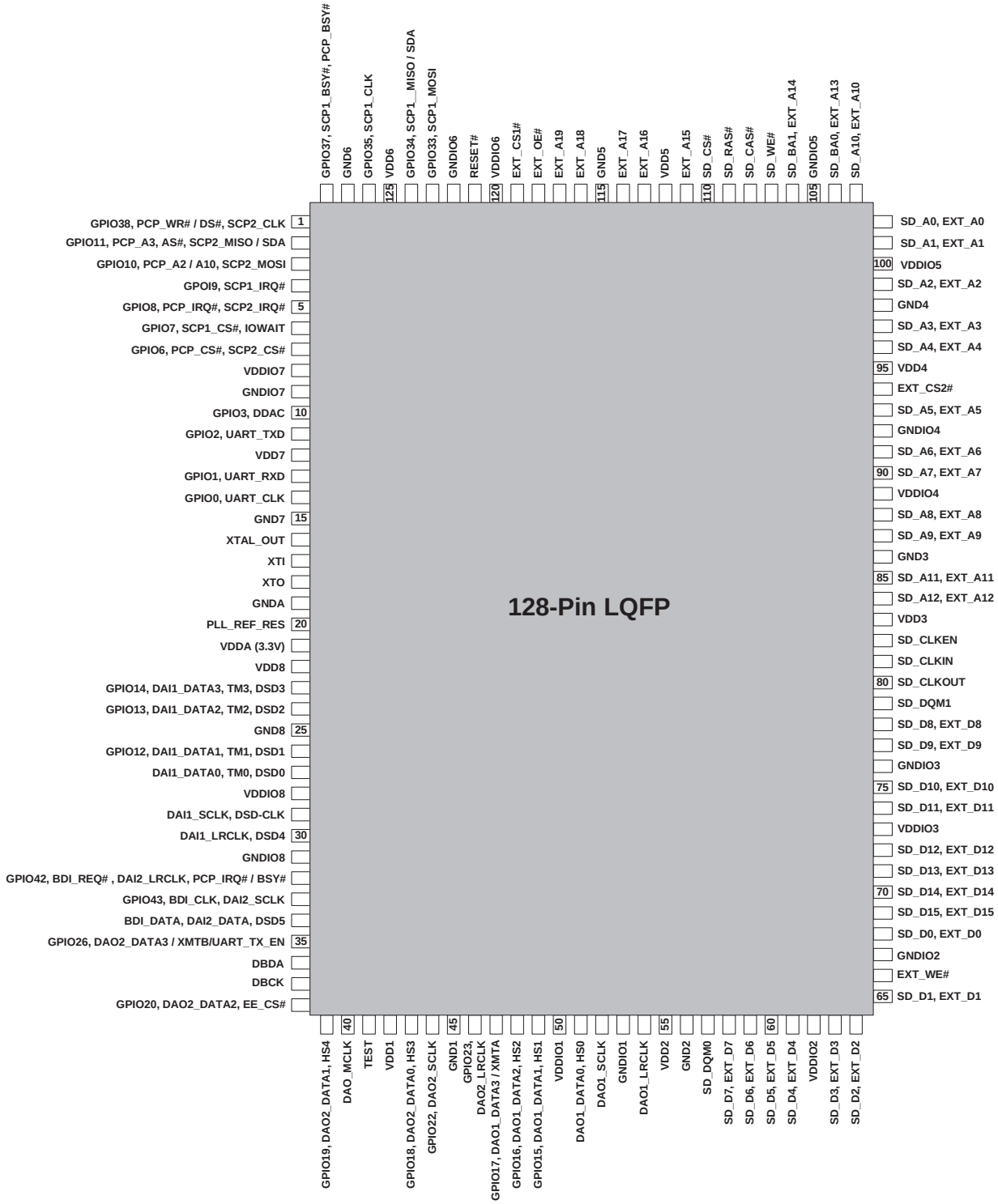


Figure 15. 128-Pin LQFP Pin-Out

TOSHIBA TC74HC151AP/AF/AFN

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC151AP,TC74HC151AF,TC74HC151AFN

8-Channel Multiplexer

Note: xxxFN (JEDEC SOP) is not available in Japan.

The TC74HC151A is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

One of eight date input signals (D0-D7) is selected by decoding of the three-bit address input (A, B, C). The selected data appears on two outputs: non-inverting (Y) and inverting (W).

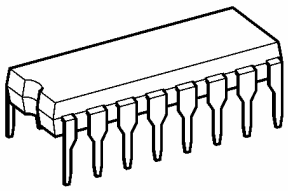
The strobe input provides two output conditions; a low level on the strobe input transfers the selected data to the outputs. A high level on the strobe input sets the Y output low and the W output high without regard to the data or select input conditions.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

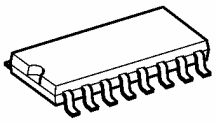
- High speed: t_{pd} = 15 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS151

TC74HC151AP



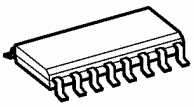
DIP16-P-300-2.54A

TC74HC151AF



SOP16-P-300-1.27A

TC74HC151AFN

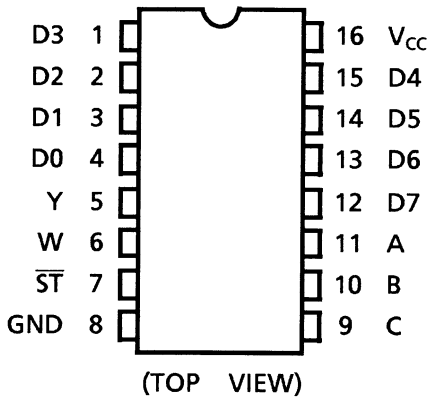


SOL16-P-150-1.27

Weight

DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)
SOL16-P-150-1.27	: 0.13 g (typ.)

Pin Assignment



Technical Note

Sound Processors for Home Theater Systems

2ch Electronic Volume

BD3812F

No.10081EAT03

●Description

BD3812F is an electronic volume having volume, gain amplifier functions necessary for applications in AV receivers, home theatre systems, min-component systems and so forth. Having a chip select terminal, it can be controlled until 4 chips with common bus line.

●Features

1) Residual noise : 1.2μVrms {dynamic range : 131dB (IHF-A)}
2) 2ch independent volume (0 to -103dB, MUTE 1dB/step)
3) 8ch at maximum available in combination of any of BD3811K1, BD3813KS, BD3814FV, BD3815KS (6ch volume) in common bus line
4) It can be controlled until 4 chips with common bus line at the same time
5) Maximum output voltage : 4.2Vrms (Vcc=7, VEE=-7V, RL=10kΩ)
6) 2-line serial control (for both 3.3V and 5V)
7) Built-in Output gain amplifier for adjustment of output signal voltage (0, 6 to 18dB, 2dB/step)
8) Output mute controllable by serial data and external control terminal

●Applications

AV receivers, home theater systems, mini-component systems, etc.

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Powewr supply voltage	VCC	7.5 *1	V
	VEE	-7.5	
Input signal voltage	VIN	VCC+0.3 to VEE-0.3	V
Power dissipation	Pd	450 *2	mW
Operating temperature range	Topr	−20 to +75	℃
Storage temperature range	Tastg	−55 to +125	℃

*1 Even in the specified range of Power Supply Voltage, applying voltage only to the VCC side may cause an excessive current to give a permanent damage to the IC.
When starting up power supplies, VEE and VCC should be powered on simultaneously or VEE first; then followed by VCC.

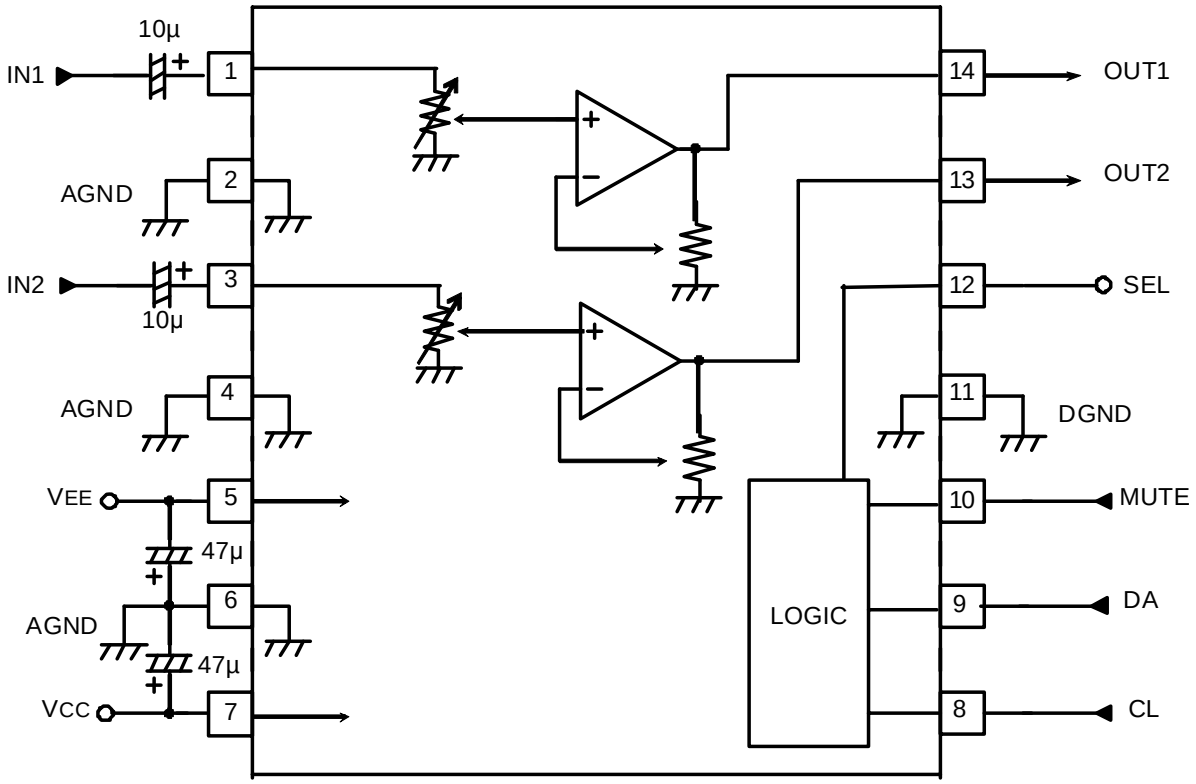
*2 Over Ta=25°C, reduce at the rate of 4.5mW/°C. When installed on the standard board (size: 70x70x1.6mm).

●Operating conditions

It must function normally at Ta=25°C.

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Operating source voltage	VCC	5	7	7.3	V
	VEE	-7.3	-7	-5	

●Application circuit BD3812F



UNIT
RESISTOR :Ω
CAPACITOR : F

Fig.2

●Reference data

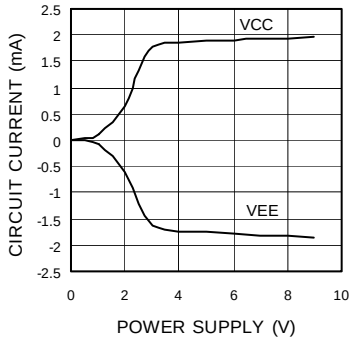


Fig.3 Circuit current - Power supply

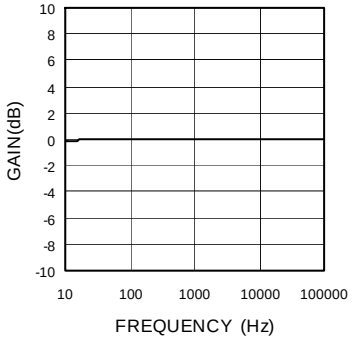


Fig.4 Voltage gain - Frequency

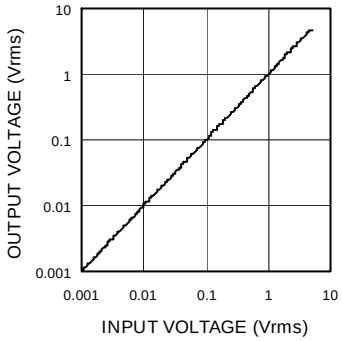


Fig.5 Output voltage - Input voltage

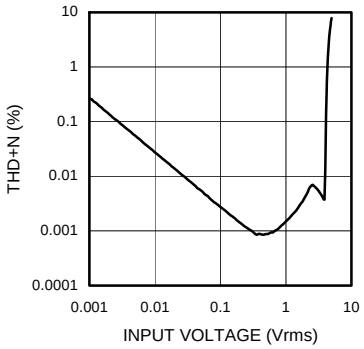


Fig.6 THD+N - Input voltage

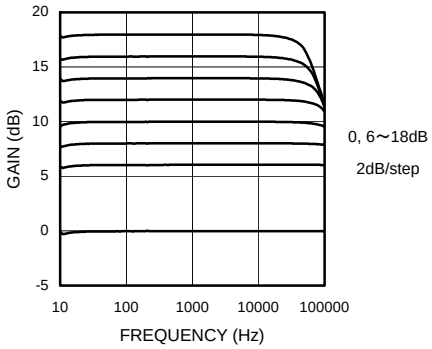


Fig.7 Output gain - Frequency

32-bit RISC Microcontroller – TX03 Series

T5CN5

1. Overview and Features

The TX03 series is a 32-bit RISC microcontroller series with an ARM Cortex™-M3 microcontroller core.

Features of the T5CN5 is as follows:

1.1 Features

(1) ARM Cortex-M3 microcontroller core

1) Improved code efficiency has been realized through the use of Thumb2 instruction

- New 16-bit Thumb instructions for improved program flow
- New 32-bit Thumb instructions for improved performance
- Auto-switching between 32-bit instruction and 16-bit instruction is executed by compiler.

2) Both high performance and low power consumption have been achieved.

-High performance

- A 32-bit multiplication (32×32=32 bit) can be executed with one clock.
- Division takes between 2 and 12 cycles depending on dividend and devisor

-Low power consumption

- Optimized design using a low power consumption library
- Standby function that stops the operation of the microcontroller core

3) High-speed interrupt response suitable for real-time control

- An interruptible long instruction.
- Stack push automatically handled by hardware.

(2) On Chip program memory and data memory

Product name	On chip Flash ROM	On chip RAM
T5CN5	512Kbyte	32Kbyte

(3) 16-bit timer : 10 channels
- 16-bit interval timer mode
- 16-bit event counter mode
- 16-bit PPG output
- Input capture function

(4) Real time clock (RTC) : 1 channel
- Clock (hour, minute and second)
- Calendar (Month, week, date and leap year)
- Time correction + or − 30 seconds (by software)
- Alarm (Alarm output)
- Alarm interrupt

(5) Watchdog timer : 1 channel
- 26 cycles of binary counter
- Watchdog timer out

(6) General-purpose serial interface : 3 channels
- Either UART mode or synchronous mode can be selected (4byte FIFO equipped)

(7) Serial bus interface : 3 channels
- Either I^2C bus mode or synchronous mode can be selected.

(8) CEC : 1 channel
- Transmission and reception per 1 byte.

(9) Remote control signal preprocessor : 2 channels
- Can receive up to 72bit data at a time

(10) 10-bit A/D converter : 12 channels
- Start by an internal or external timer trigger
- Fixed channel/scan mode
- Single/repeat mode
- AD monitoring 2ch
- Conversion speed 1.15usec(@fsys = 40MHz)

(11) Interrupt source
- Internal: 42 factors…The order of precedence can be set over 7 levels (except the watchdog timer interrupt).
- External: 8 factors…The order of precedence can be set over 7 levels.

(12) Input/ output ports
- 79 pins

(13) Standby mode

- Standby modes :IDLE, SLOW, SLEEP, STOP
- Sub clock operation(32.768kHz) :SLOW, SLEEP

(14) Clock generator

- On-chip PLL (quadrupled)
- Clock gear function: The high-speed clock can be divided into 1/1, 1/2, 1/4 or 1/8.

(15) Endian

- Little endian

(16) Maximum operating frequency

- 40MHz

(17) Operating voltage range

- 2.7V~3.6V (with on-chip regulator)

(18) Temperature range

- -20~85 degrees (except during Flash writing/ erasing)
- 0~70 degrees (during Flash writing/ erasing)

(19) Package

- LQFP100-P-1414-0.5H (14mm × 14mm, 0.5mm pitch)

1.2 Block Diagram

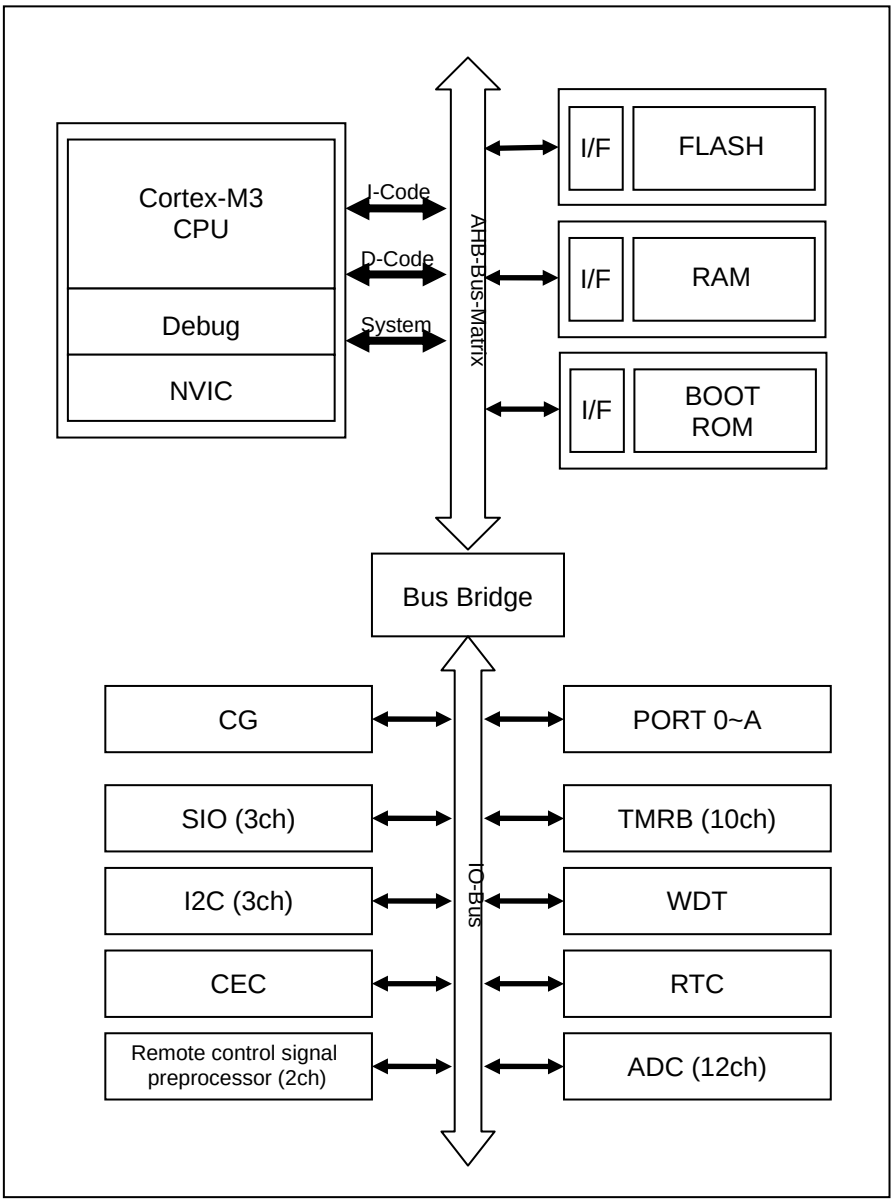


Fig. 1.1 T5CN5 Block Diagram

2. Pin Layout and Pin Functions

This chapter describes the pin layout, pin names and pin functions of T5CN5.

2.1 Pin Layout (Top view)

Fig. 2-1 shows the pin layout of T5CN5.

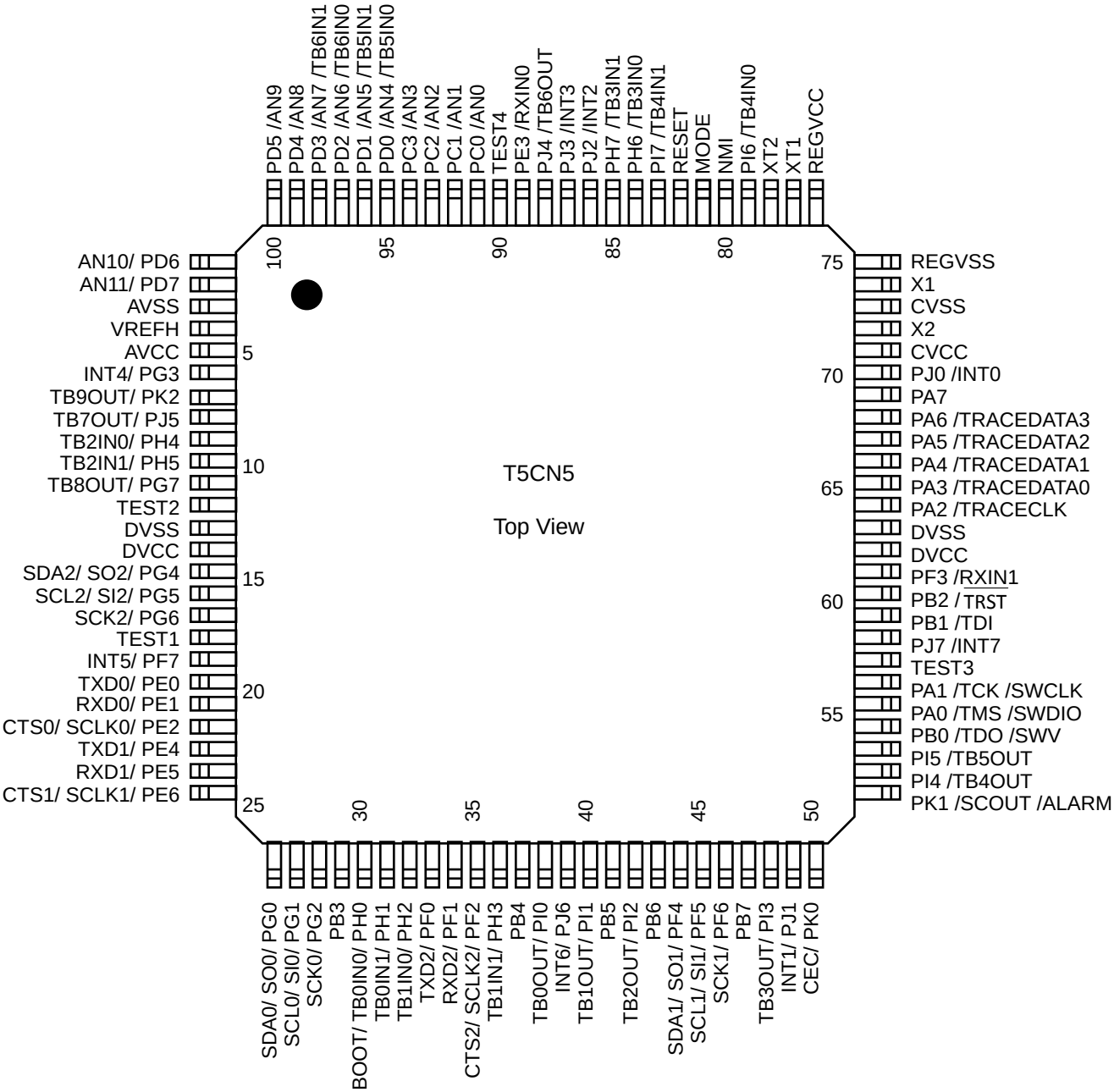


Fig. 2.1 Pin Layout (LQFP100)

Table 2.1 Pin Numbers and Names (1/2)

Pin No.	Pin name	Pin No.	Pin name
1	PD6, AN10	26	PG0, SO0, SDA0
2	PD7, AN11	27	PG1, SI0, SCL0
3	AVSS	28	PG2, SCK0
4	VREFH	29	PB3
5	AVCC	30	PH0, TB0IN0, $\overline{\text{BOOT}}$
6	PG3, INT4	31	PH1, TB0IN1
7	PK2, TB9OUT	32	PH2, TB1IN0
8	PJ5, TB7OUT	33	PF0, TXD2
9	PH4, TB2IN0	34	PF1, RXD2
10	PH5, TB2IN1	35	PF2, SCLK2, CTS2
11	PG7, TB8OUT	36	PH3, TB1IN1
12	TEST2	37	PB4
13	DVSS	38	PI0, TB0OUT
14	DVCC	39	PJ6, INT6
15	PG4, SO2, SDA2	40	PI1, TB1OUT
16	PG5, SI2, SCL2	41	PB5
17	PG6, SCK2	42	PI2, TB2OUT
18	TEST1	43	PB6
19	PF7, INT5	44	PF4, SO1, SDA1
20	PE0, TXD0	45	PF5, SI1, SCL1
21	PE1, RXD0	46	PF6, SCK1
22	PE2, SCLK0, CTS0	47	PB7
23	PE4, TXD1	48	PI3, TB3OUT
24	PE5, RXD1	49	PJ1, INT1
25	PE6, SCLK1, CTS1	50	PK0, CEC

Table 2.1 Pin Numbers and Names (2/2)

Pin No.	Pin name	Pin No.	Pin name
51	PK1, SCOUT, $\overline{\text{ALARM}}$	76	REGVCC
52	PI4, TB4OUT	77	XT1
53	PI5, TB5OUT	78	XT2
54	PB0, TDO, SWV	79	PI6, TB4IN0
55	PA0, TMS, SWDIO	80	$\overline{\text{NMI}}$
56	PA1, TCK, SWCLK	81	MODE
57	TEST3	82	$\overline{\text{RESET}}$
58	PJ7, INT7	83	PI7, TB4IN1
59	PB1, TDI	84	PH6, TB3IN0
60	PB2, $\overline{\text{TRST}}$	85	PH7, TB3IN1
61	PF3, RXIN1	86	PJ2, INT2
62	DVCC	87	PJ3, INT3
63	DVSS	88	PJ4, TB6OUT
64	PA2, TRACECLK	89	PE3, RXIN0
65	PA3, TRACEDATA0	90	TEST4
66	PA4, TRACEDATA1	91	PC0, AN0
67	PA5, TRACEDATA2	92	PC1, AN1
68	PA6, TRACEDATA3	93	PC2, AN2
69	PA7	94	PC3, AN3
70	PJ0, INT0	95	PD0, AN4, TB5IN0
71	CVCC	96	PD1, AN5, TB5IN1
72	X2	97	PD2, AN6, TB6IN0
73	CVSS	98	PD3, AN7, TB6IN1
74	X1	99	PD4, AN8
75	REGVSS	100	PD5, AN9

2.2 Pin names and Functions

Table 2.2 and Table 2.3 sort the input and output pins of the T5CN5 by pin or port. Each table includes alternate pin names and functions for multi-function pins.

3.1.1 Sorted by Pin

Table 2.2 Pin Names and Functions Sorted by Pin (1/5)

Type	# of Pins	Pin Name	Input/ Output	Function	Programmable Pull up/ Pull down	Schmitt trigger	Programmable Open Drain Output
Function	1	PD6 AN10	I I	Input port Analog input	Pull up	-	-
	2	PD7 AN11	I I	Input port Analog input	Pull up	-	-
PS	3	AVSS	I	A/D converter: GND pin (0V) Tie AVSS to power supply even if the A/D converter is not used.	-	-	-
	4	VREFH	I	Supplying the A/D converter with a reference power supply. Tie VREFH to power supply even if the A/D converter is not used.	-	-	-
	5	AVCC	I	Supplying the A/D converter with a power supply. Tie AVCC to power supply even if the A/D converter is not used.	-	-	-
Function	6	PG3 INT4	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
	7	PK2 TB9OUT	I/O O	I/O port Timer B output	Pull up	-	-
	8	PJ5 TB7OUT	I/O I	I/O port Timer B output	Pull up	-	-
	9	PH4 TB2IN0	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	10	PH5 TB2IN1	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	11	PG7 TB8OUT	I/O O	I/O port Timer B output	Pull up	-	○
Test	12	TEST2	-	TEST pin: Not connected.	-	-	-
PS	13	DVSS	-	GND pin	-	-	-
	14	DVCC	-	Power supply pin	-	-	-
Function	15	PG4 SDA2/ SO2	I/O I/O O	I/O port If the serial bus interface operates -in the I2C mode : data pin -in the SIO mode: data pin	Pull up	○	○
	16	PG5 SCL2/ SI2	I/O I/O I	I/O port If the serial bus interface operates -in the I2C mode : clock pin -in the SIO mode: data pin	Pull up	○	○
	17	PG6 SCK2	I/O I/O	I/O port Inputting and outputting a clock if the serial bus interface operates in the SIO mode.	Pull up	○	○
Test	18	TEST1	-	TEST pin: Not connected.	-	-	-
Function	19	PF7 INT5	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○

Table 2.2 Pin Names and Functions Sorted by Pin (2/5)

Type	# of Pins	Pin Name	Input/ Output	Function	Programmable Pull-up/ Pull down	Schmitt trigger	Programmable Open Drain Output
Function	20	PE0 TXD0	I/O O	I/O port Sending serial data	Pull up	-	○
	21	PE1 RXD0	I/O I	I/O port Receiving serial data	Pull up	○	○
	22	PE2 SCLK0 CTS0	I/O I I	I/O port Serial clock input/ output Handshake input pin	Pull up	○	○
	23	PE4 TXD1	I/O O	I/O port Sending serial data	Pull up	-	○
	24	PE5 RXD1	I/O I	I/O port Receiving serial data	Pull up	○	○
	25	PE6 SCLK1 CTS1	I/O I I	I/O port Serial clock input/ output Handshake input pin	Pull up	○	○
	26	PG0 SDA0/ SO0	I/O I/O O	I/O port If the serial bus interface operates -in the I2C mode : data pin -in the SIO mode: data pin	Pull up	○	○
	27	PG1 SCL0/ SI0	I/O I/O I	I/O port If the serial bus interface operates -in the I2C mode : clock pin -in the SIO mode: data pin	Pull up	○	○
	28	PG2 SCK0	I/O I/O	I/O port Inputting and outputting a clock if the serial bus interface operates in the SIO mode.	Pull up	○	○
	29	PB3	I/O	I/O port	Pull up	-	-
Function/ Control	30	PH0 TB0IN0 $\overline{\text{BOOT}}$	I/O I I	I/O port Inputting the timer B capture trigger Setting a single boot mode: This pin goes into single boot mode by sampling "L" at the rise of a reset signal.	Pull up	○	-
Function	31	PH1 TB0IN1	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	32	PH2 TB1IN0	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	33	PF0 TXD2	I/O O	I/O port Sending serial data	Pull up	-	○
	34	PF1 RXD2	I/O I	I/O port Receiving serial data	Pull up	○	○
	35	PF2 SCLK2 CTS2	I/O I I	I/O port Serial clock input/ output Handshake input pin	Pull up	○	○
	36	PH3 TB1IN1	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	37	PB4	I/O	I/O port	Pull up	-	-
	38	PI0 TB0OUT	I/O O	I/O port Timer B output	Pull up	-	-
	39	PJ6 INT6	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○

Table 2.2 Pin Names and Functions Sorted by Pin (3/5)

Type	# of Pins	Pin Name	Input/ Output	Function	Programmable Pull-up/ Pull down	Schmitt trigger	Programmable Open Drain Output
Function	40	PI1 TB1OUT	I/O O	I/O port Timer B output	Pull up	-	-
	41	PB5	I/O	I/O port	Pull up	-	-
	42	PI2 TB2OUT	I/O O	I/O port Timer B output	Pull up	-	-
	43	PB6	I/O	I/O port	Pull up	-	-
	44	PF4 SDA1/ SO1	I/O I/O O	I/O port If the serial bus interface operates -in the I2C mode : data pin -in the SIO mode: data pin	Pull up	○	○
	45	PF5 SCL1/ SI1	I/O I/O I	I/O port If the serial bus interface operates -in the I2C mode : clock pin -in the SIO mode: data pin	Pull up	○	○
	46	PF6 SCK1	I/O I/O	I/O port Inputting and outputting a clock if the serial bus interface operates in the SIO mode.	Pull up	○	○
	47	PB7	I/O	I/O port	Pull up	-	-
	48	PI3 TB3OUT	I/O O	I/O port Timer B output	Pull up	-	-
	49	PJ1 INT1	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
	50	PK0 CEC	I/O I/O	I/O port CEC pin	-	○	● (Note 4)
	51	PK1 SCOUT $\overline{\text{ALARM}}$	I/O O O	I/O port System clock output Alarm output	Pull up	-	-
	52	PI4 TB4OUT	I/O O	I/O port Timer B output	Pull up	-	-
	53	PI5 TB5OUT	I/O O	I/O port Timer B output	Pull up	-	-
Function/ Debug	54	PB0 TDO/SWV	I/O O	I/O port Debug pin	Pull up	-	-
	55	PA0 TMS/SWDIO	I/O I/O	I/O port Debug pin	Pull up	○	-
	56	PA1 TCK/ SWCLK	I/O I	I/O port Debug pin	Pull up	-	-
Test	57	TEST3	-	TEST pin: Not connected.	-	-	-
Function	58	PJ7 INT7	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
Function/ Debug	59	PB1 TDI	I/O I	I/O port Debug pin	Pull up	-	-
	60	PB2 $\overline{\text{TRST}}$	I/O I	I/O port Debug pin	Pull up	○	-
Function	61	PF3 RXIN1	I/O I	I/O port Inputting signal to remote controller	Pull up	○	○
PS	62	DVCC	-	Power supply pin	-	-	-
	63	DVSS	-	GND pin	-	-	-

Table 2.2 Pin Names and Functions Sorted by Pin (4/5)

Type	# of Pins	Pin Name	Input/ Output	Function	Programmable Pull-up/ Pull down	Schmitt trigger	Programmable Open Drain Output
Function/ Debug	64	PA2 TRACECLK	I/O O	I/O port Debug pin	Pull up	-	-
	65	PA3 TRACEDATA0	I/O O	I/O port Debug pin	Pull up	-	-
	66	PA4 TRACEDATA1	I/O O	I/O port Debug pin	Pull up	-	-
	67	PA5 TRACEDATA2	I/O O	I/O port Debug pin	Pull up	-	-
	68	PA6 TRACEDATA3	I/O O	I/O port Debug pin	Pull up	-	-
Function	69	PA7	I/O	I/O port	Pull up		
	70	PJ0 INT0	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
PS	71	CVCC	-	Power supply pin	-	-	-
Clock	72	X2	O	Connected to a high-speed oscillator.	-	-	-
PS	73	CVSS	-	GND pin	-	-	-
Clock	74	X1	I	Connected to a high-speed oscillator.	-	○	-
PS	75	REGVSS	-	GND pin	-	-	-
	76	REGVCC	-	Power supply pin	-	-	-
Clock	77	XT1	I	Connected to a low-speed oscillator.	-	○	-
	78	XT2	O	Connected to a low-speed oscillator.	-	-	-
Function	79	PI6 TB4IN0	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	80	$\overline{\text{NMI}}$	I	Non-maskable interrupt	-	○ w/ noise filter	-
Control	81	MODE	I	Mode pin: Tied to GND pin	-	○	-
Function	82	$\overline{\text{RESET}}$	I	Reset input pin	Tied to Pull up	○ w/ noise filter	-
	83	PI7 TB4IN0	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	84	PH6 TB3IN0	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	85	PH7 TB3IN1	I/O I	I/O port Inputting the timer B capture trigger	Pull up	○	-
	86	PJ2 INT2	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
	87	PJ3 INT3	I/O I	I/O port Interrupt request pin	Pull up	○ w/ noise filter	○
	88	PJ4 TB6OUT	I/O O	I/O port Timer B output	Pull up	-	-
	89	PE3 RXIN0	I/O I	I/O port Inputting signal to remote controller	Pull up	○	○
Test	90	TEST4	-	TEST pin: Not connected.	-	-	-

Table 2.2 Pin Names and Functions Sorted by Pin (5/5)

Type	# of Pins	Pin Name	Input/ Output	Function	Programmable Pull-up/ Pull down	Schmitt trigger	Programmable Open Drain Output
Function	91	PC0 AN0	I I	Input port Analog input	Pull up	-	-
	92	PC1 AN1	I I	Input port Analog input	Pull up	-	-
	93	PC2 AN2	I I	Input port Analog input	Pull up	-	-
	94	PC3 AN3	I I	Input port Analog input	Pull up	-	-
	95	PD0 AN4 TB5IN0	I I I	Input port Analog input Inputting the timer B capture trigger	Pull up	-	-
	96	PD1 AN5 TB5IN1	I I I	Input port Analog input Inputting the timer B capture trigger	Pull up	-	-
	97	PD2 AN6 TB6IN0	I I I	Input port Analog input Inputting the timer B capture trigger	Pull up	-	-
	98	PD3 AN7 TB6IN1	I I I	Input port Analog input Inputting the timer B capture trigger of	Pull up	-	-
	99	PD4 AN8	I I	Input port Analog input	Pull up	-	-
	100	PD5 AN9	I I	Input port Analog input	Pull up	-	-

(Note 1) TEST1 through 4 must be left unconnected.
(Note 2) Be sure to tie MODE to GND.
(Note 3) Tie VREFH/ AVCC to power supply and AVSS to GND even if the A/D converter is not used.
(Note 4) Nch open drain port.

2.3 Pin Names and Power Supply Pins

Table 2.4 Pin Names and Power Supplies

Pin name	Power supply
PA	DVCC
PB	DVCC
PC	AVCC
PD	AVCC
PE	DVCC
PF	DVCC
PG	DVCC
PH	DVCC
PI	DVCC
PJ	DVCC
PK	DVCC
X1, X2	CVCC
XT1, XT2	DVCC
$\overline{\text{RESET}}$	DVCC
$\overline{\text{NMI}}$	DVCC
MODE	DVCC

2.4 Pin Numbers and Power Supply Pins

Table 2.5 Pin Numbers and Power Supplies

Power supply	Pin number	Voltage range
DVCC	14, 62	2.7V~3.6V
AVCC	5	
REGVCC	76	
CVCC	71	

ESMT M12L16161A

SDRAM 512K x 16Bit x 2Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 32ms refresh period (2K cycle)

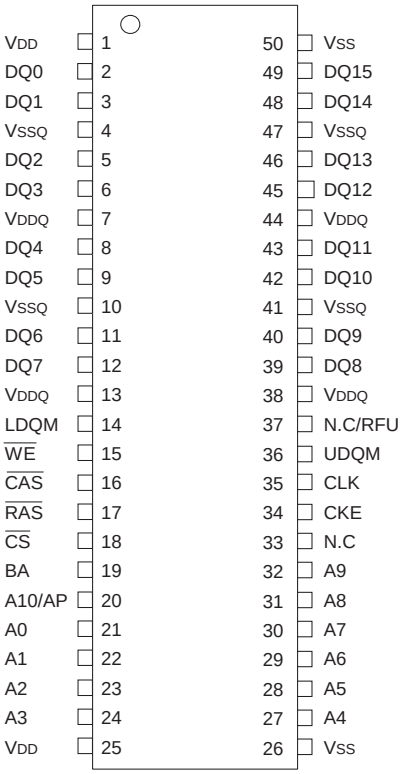
GENERAL DESCRIPTION

The M12L16161A is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 524,288 words by 16 bits, fabricated with high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

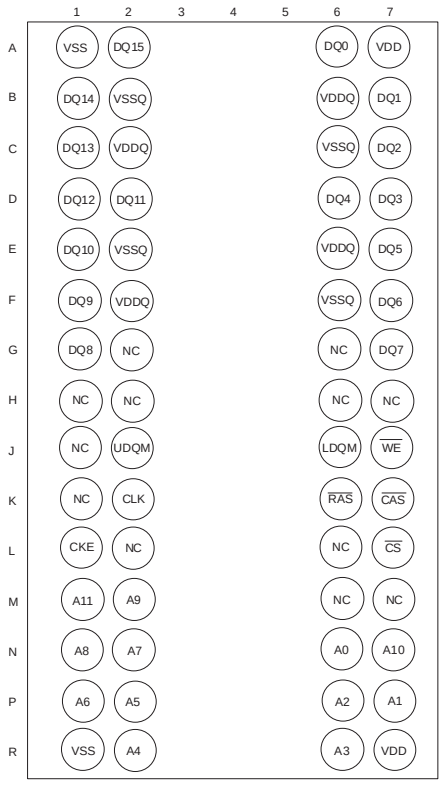
ORDERING INFORMATION

Part NO.	MAX Freq.	PACKAGE	COMMENTS
M12L16161A-5TG	200MHz	TSOP(II)	Pb-free
M12L16161A-7TG	143MHz	TSOP(II)	Pb-free
M12L16161A-7BG	143MHz	VFBGA	Pb-free

PIN CONFIGURATION (TOP VIEW)

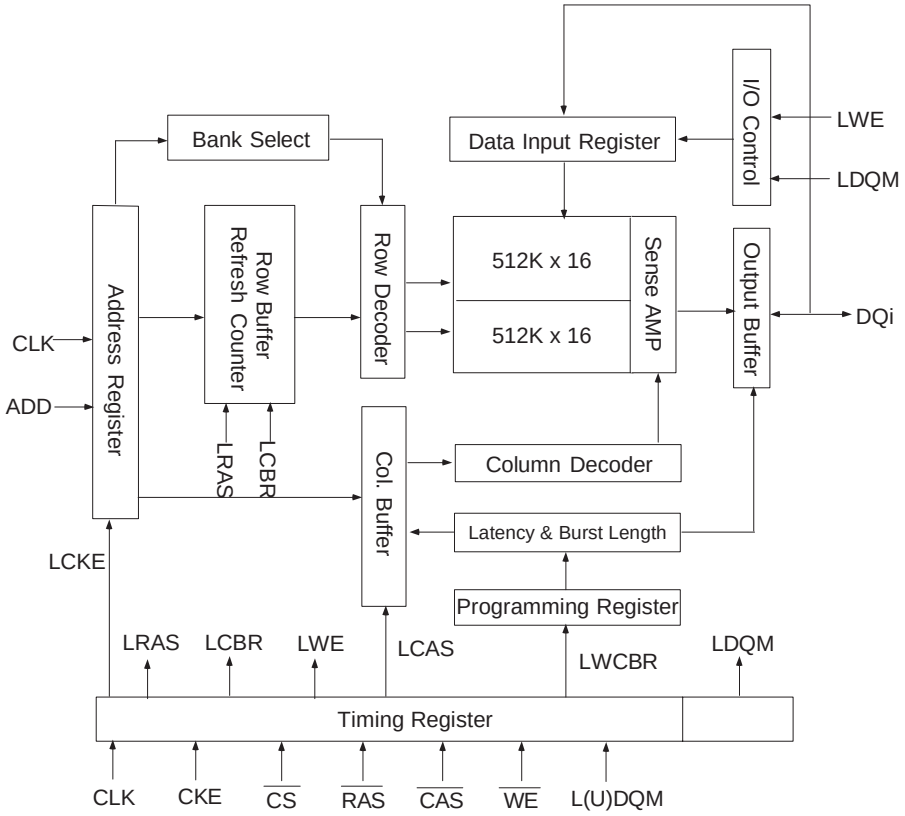


50PIN TSOP(II)
(400mil x 825mil)
(0.8 mm PIN PITCH)



60 Ball VFBGA
(6.4x10.1mm)
(0.65mm ball pitch)

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM.
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA7
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data Input / Output Mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when L(U)DQM active.

M24128
M24C64 M24C32

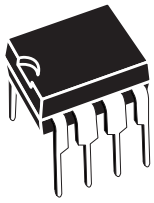
128 Kbit, 64 Kbit and 32 Kbit serial I²C bus EEPROM

Features

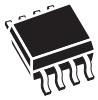
- Two-wire I²C serial interface supports 400 kHz protocol
- Single supply voltages (see *Table 1* for root part numbers):
  - 2.5 V to 5.5 V
  - 1.8 V to 5.5 V
  - 1.7 V to 5.5 V
- Write Control input
- Byte and Page Write
- Random and Sequential Read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection
- More than 1 Million write cycles
- More than 40-year data retention
- Packages
  - ECOPACK® (RoHS compliant)

Table 1. Device summary

Reference	Part number	Supply voltage
M24128	M24128-BW	2.5 V to 5.5V
	M24128-BR	1.8 V to 5.5V
	M24128-BF	1.7 V to 5.5V
M24C64	M24C64-W	2.5 V to 5.5V
	M24C64-R	1.8 V to 5.5V
	M24C64-F	1.7 V to 5.5V
M24C32	M24C32-W	2.5 V to 5.5V
	M24C32-R	1.8 V to 5.5V
	M24C32-F	1.7 V to 5.5V



PDIP8 (BN)



SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

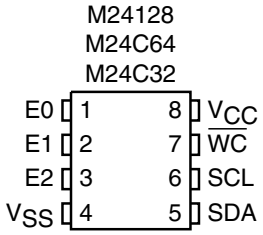
UFDFPN8 (MB)
2 × 3 mm (MLP)

WLCSP (CS)

Table 2. Signal names

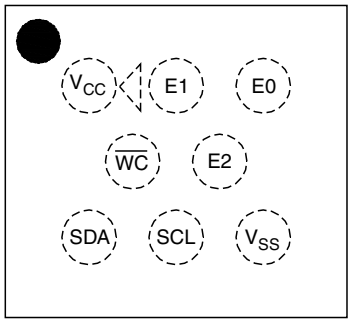
Signal name	Function	Direction
E0, E1, E2	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
WC	Write Control	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. DIP, SO, TSSOP and UFDFPN connections



1. See *Package mechanical data* section for package dimensions, and how to identify pin-1.

Figure 3. M24128 WLCSP connections (top view, marking side, with balls on the underside)



Minilogic Device Corporation ML61

ML61 Series Positive Voltage Detector

❖ *Application*

- *Memory Battery Back-up Circuits*
- *Microprocessor Reset Circuitry*
- *Power Failure Detection*
- *Power-on Reset Circuit*
- *System Battery Life and Charge Voltage Monitor*

❖ *Features*

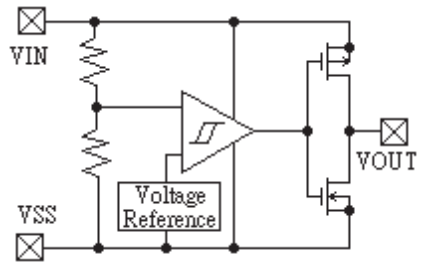
- CMOS Low Power Consumption : Typical 1.0uA at Vin=2.0V
- Selectable Detect Voltage : 1.1V to 6.0V in 0.1V increments
- Highly Accurate : Detect Voltage 1.1V to 1.9V ±3%
  Detect Voltage 2.0V to 6.0V ±2%
- Operating Voltage : 0.8V to 10.0V
- Package Available : SOT23 (150mW), SOT89 (500mW) & TO92 (300mW)

❖ *General Description*

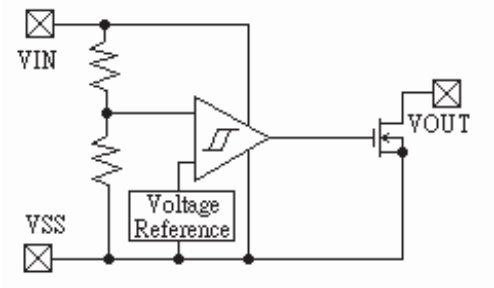
The ML61 is a group of high-precision and low-power voltage detectors.
The ML61 consists of a highly-accurate and low-power reference voltage source, a comparator, a hysteresis circuit, and an output driver. Detect voltage is very accurate and stable with N-channel open drain and CMOS, are available.

❖ *Block Diagram*

(1) CMOS Output

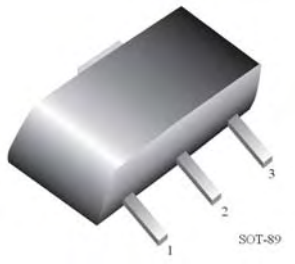


(2) N-Channel Open Drain Output



❖

SOT-89



❖ *Pin Configuration*

Pin Number	*Pin Name*	*Description*
1	*VOUT*	*Supply Voltage Output*
2	*VIN*	*Supply Voltage Input*
3	*VSS*	*Ground*

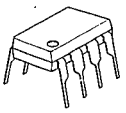
JRC **NJM2068**

LOW-NOISE DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2068 is a high performance, low noise dual operational amplifier. This amplifier features popular pin-out, superior noise performance, and superior total harmonic distortion. This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product and slew rate which far exceeds that of the 4558 type amplifier. The specially designed low noise input transistors allow the NJM2068 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifier.

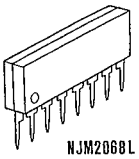
■ PACKAGE OUTLINE



NJM2068D

NJM2068M

NJM2068V



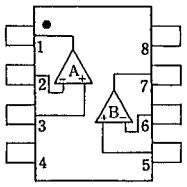
NJM2068L

■ FEATURES

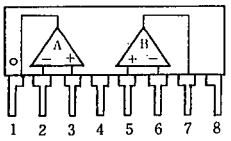
- Operating Voltage (±4V～±18V)
- Low Total Harmonic Distortion (0.001% typ.)
- Low Noise Voltage (FLAT+JISA, 0.56 μV typ.)
- High Slew Rate (6V/μs typ.)
- Unity Gain Bandwidth (27MHz @f=10kHz)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

4

■ PIN CONFIGURATION



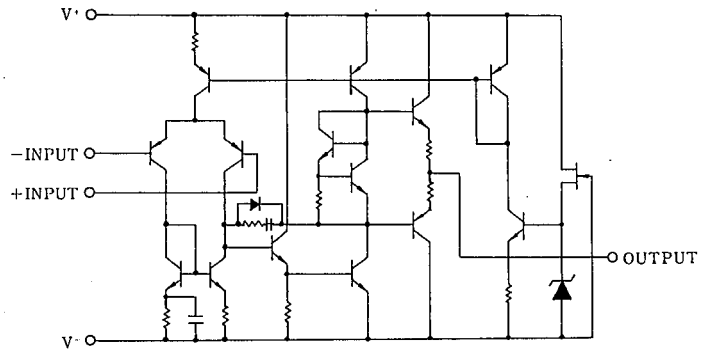
NJM2068D
NJM2068M
NJM2068V



NJM2068L

PIN FUNCITON
1. A OUTPUT
2. A−INPUT
3. A+INPUT
4. V⁻
5. B+INPUT
6. B−INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



JRC

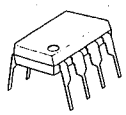
NJM2115

DUAL OPERATIONAL AMPLIFIER

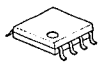
■ GENERAL DESCRIPTION

NJM 2115 is a low operating Voltage (±1.0 V min.) and low saturation output voltage (±2.0 V p-p at supply voltage ±2.5V) operational amplifier. It is applicable to HANDY TYPE CD, RADIO CASSETE CD, and PORTABLE DAT, that are digital audio apparatus which require the 5V single supply operation and high output voltage. The NJM2115 is improved version of the NJM2100 about BIAS-CIRCUIT. So, NJM2115 is low saturation compared to the NJM2100 under the condition of low supply voltage (< ±2.5V). The NJM2115 is stable about the oscillation compared to the NJM2100 under the condition of $V^+/V^- > 2.5V$.

■ PACKAGE OUTLINE

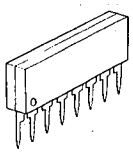


NJM2115D



NJM2115M

NJM2115V

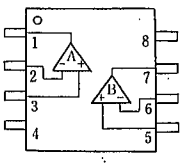


NJM2115L

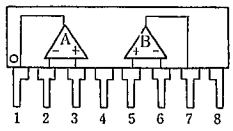
■ FEATURES

- Operating Voltage (±1V ~ ±7V)
- Low Saturation Output Voltage ($\pm 2.0V_{P\text{-}P}$ @ $V^+ = \pm 2.5V$)
- Slew Rate (4V/μs typ.)
- Unity Gain Bandwidth (12MHz typ.)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

■ PIN CONFIGURATION



NJM2115D
NJM2115M
NJM2115V

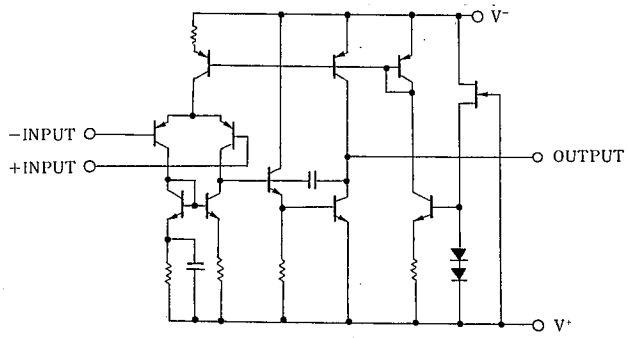


NJM2115L

PIN FUNCTION

1. A OUTPUT
2. A −INPUT
3. A +INPUT
4. V^-
5. B +INPUT
6. B −INPUT
7. B OUTPUT
8. V^+

■ EQUIVALENT CIRCUIT (1/2 Shown)



JRC

NJM4556A

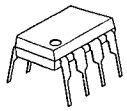
DUAL HIGH CURRENT OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM4556A integrated circuit is a high-gain, high output current dual operational amplifier capable of driving ±70mA into 150 Ω loads (±10.5V output voltage), and operating low supply voltage (V^+/V^-=±2V~).

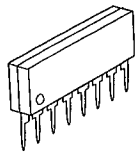
The NJM4556A combines many of the fetures of the popular NJM4558 as well as having the capability of driving 150Ω loads. In addition, the wide band-width, low noise, high slew rate and low distortion of the NJM4556A make it ideal for many audio, telecommunications and instrumentation applications.

■ PACKAGE OUTLINE

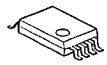


NJM4556AD

NJM4556AM



NJM4556AL

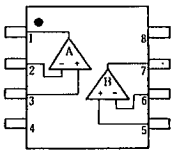


NJM4556AV

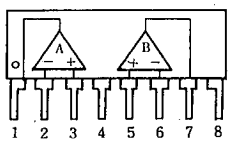
■ FEATURES

- Operating Voltage (±2V~±18V)
- High Output Current (Io=70mA)
- Slew Rate (3V/μs typ.)
- Gain Band Width Product (8MHz typ.)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

■ PIN CONFIGURATION



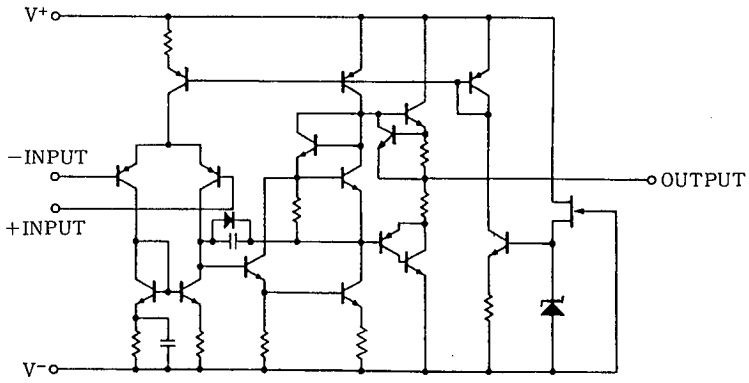
NJM4556AD
NJM4556AM
NJM4556AV



NJM4556AL

PIN FUNCTION
1. A OUTPUT
2. A−INPUT
3. A+INPUT
4. V⁻
5. B+INPUT
6. B−INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



JRC **NJU7223**

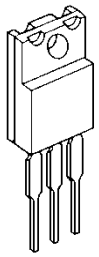
500mA Low Dropout Voltage Regulator

■ GENERAL DESCRIPTION

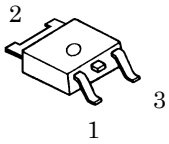
The NJU7223 series is a high precision output voltage, low drop output, low current consumption and high output current 3-terminal positive voltage regulator with a over current protection and a thermal shutdown.

Low dropout voltage is realized at high current output.

■ PACKAGE OUTLINE



NJM7223F



NJU7223DL1

1.V_{OUT}
2.V_{IN}
3.GND

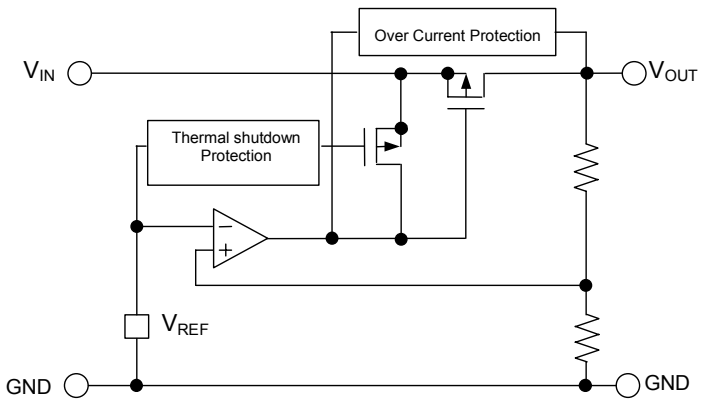
■ FEATURES

- ●High Precision Output Voltage ±2%
- ●High Output Current Io(max.)=500mA
- ●Low Current Consumption 30μA
- ●Low Dropout Voltage ΔV_{IO}=0.4V typ. (Io=0.5A,Vo=5V)
- ●Internal Over Current Protection
- ●Internal Thermal Shutdown Protection
- ●Package Outline TO-220F, TO-252
- ●C-MOS Technology

■ OUTPUT VOLTAGE LINE-UP

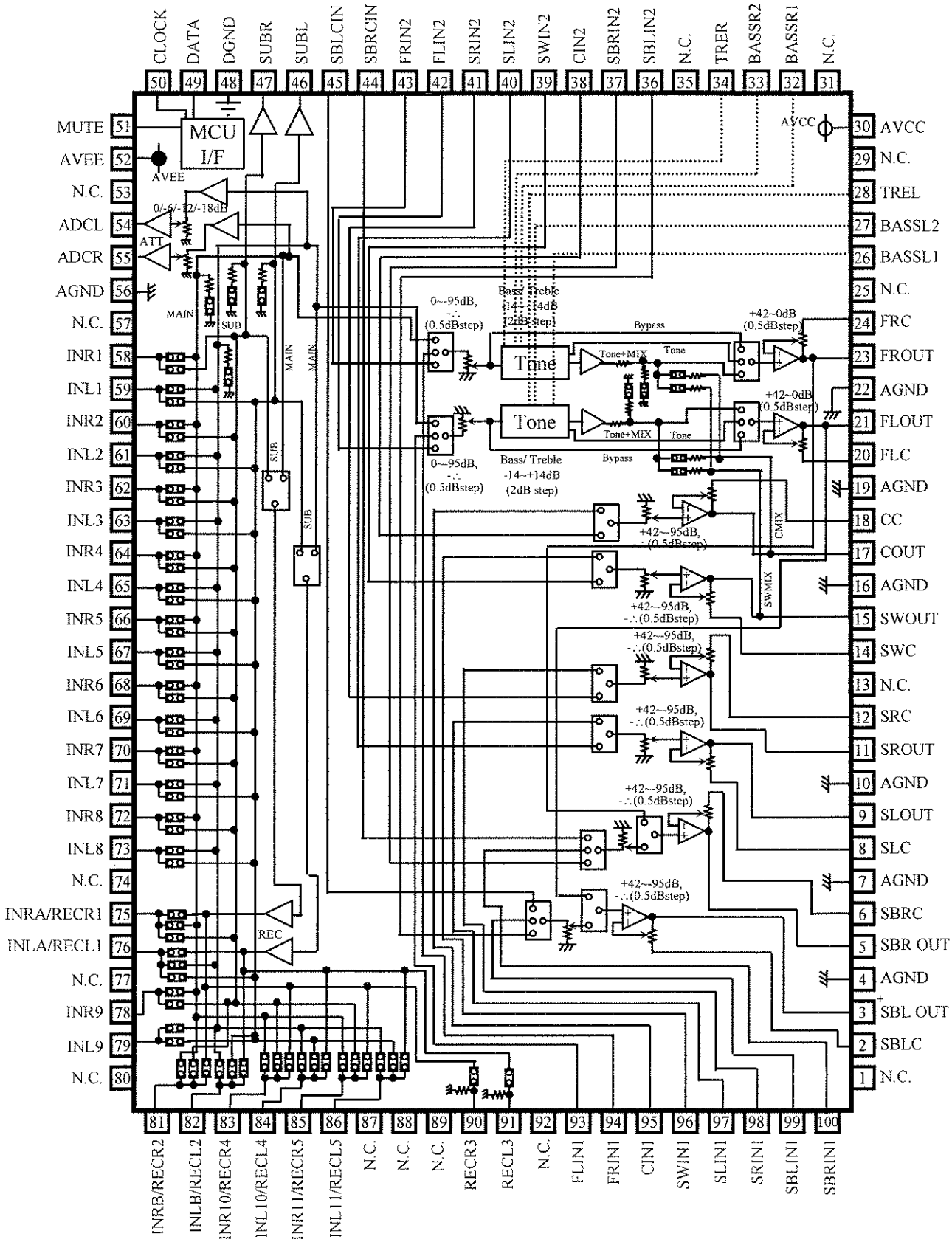
V_{OUT}	TO-220F	TO-252
+1.8V	NJU7223F18	NJU7223DL1-18
+2.5V	NJU7223F25	NJU7223DL1-25
+3.0V	NJU7223F30	NJU7223DL1-30
+3.3V	NJU7223F33	NJU7223DL1-33
+5.0V	NJU7223F50	NJU7223DL1-50

■ EQUIVALENT CIRCUIT



C.S	Integrated Circuit (R2A15218FP)

Fig 1. BLOCKDIAGRAM AND PIN CONFIGURATION(TOP VIEW)



C.S	Integrated Circuit (R2A15218FP)

Fig 2. PIN DESCRIPTION

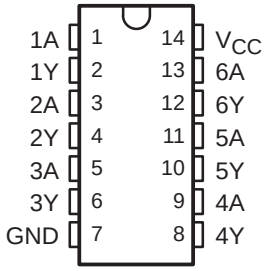
PIN No.	Name	Function
23,21, 17,15, 11,9, 5,3	FROUT,FLOUT, COUT,SWOUT, SROUT, SLOUT, SBROUT,SBLOUT	Output pin of FL/FR/C/SW/SL/SR/SBL/SBR channel
24,20, 18,14, 12,8, 6,2	FRC,FLC, CC,SWC, SRC,SLC, SBRC,SBLC	Connects capacitor for reducing click noise of L/R/C/SW/SL/SR/SBL/SBR channel volume
4,7,10,16, 19,22,56	AGND	Analog ground of internal circuit
28,34	TREL, TRER	Frequency characteristic setting pin of L/R channel tone control (Treble)
26,27, 32,33	BASSL1,BASSL2 BASSR1,BASSR2	Frequency characteristic setting pin of L/R channel tone control (Bass)
30	AVCC	Positive power supply to internal circuit
43,42, 41,40, 39,38, 37,36	FRIN2, FLIN2, SRN2,SLIN2, SWIN2,CIN2, SBRIN2,SBLIN2	Input pin of L/R/C/SW/SL/SR/SBL/SBR channel (Multi IN 1/2)
93,94, 95,96, 97,98, 99,100	FLIN1, FRIN1, CIN1,SWIN1, SLIN1,SRIN1, SBLIN1,SBRIN1	
48	DGND	Digital ground of internal circuit
49	DATA	Input pin of control data
50	CLOCK	Input pin of control clock
52	AVEE	Negative power supply to internal circuit
59,61,63, 65,67,69, 71,73,79	INL1,INL2, INL3, INL4,INL5,INL6, INL7,INL8,INL9	Input pin of L/R channel (Input Selector)
58,60,62, 64,66,68, 70,72,78	INR1,INR2, INR3, INR4,INR5,INR6, INR7,INR8,INR9	
51	MUTE	Outside Mute Control PIN
44,45	SBRCIN,SBLCIN	Input pin for SBL/SBR channel Volume
46,47	SUBL,SUBR	Output pin for L/R channel SUB Output
54,55	ADCL, ADCR	Output pin for L/R channel ADC
90,91	RECR3,RECL3	Output pin for L/R channel REC Output
75,76, 81,82, 83,84, 85,86	INRA/RECR1,INLA/RECL1, INRB/RECR2,INLB/RECL2, INR10/RECR4,INL10/RECL4, INR11/RECR5,INL11/RECL5	Input pin of L/R channel (Input Selector)/ Output pin for L/R channel REC Output
1,13,25,29,31, 35,53, 57,74,77,80, 87,88,89,92	N.C.	No Connected PIN

SN54ACT04, SN74ACT04
HEX INVERTERS

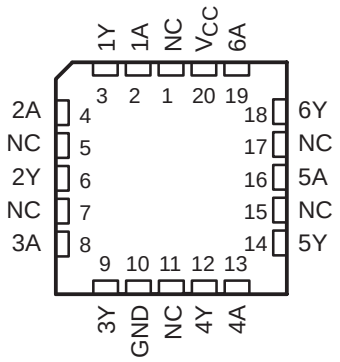
SCAS518C − JULY 1995 − REVISED OCTOBER 2003

- **4.5-V to 5.5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 8.5 ns at 5 V**
- **Inputs Are TTL-Voltage Compatible**

SN54ACT04 . . . J OR W PACKAGE
SN74ACT04 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54ACT04 . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The ‘ACT04 devices contain six independent inverters. The devices perform the Boolean function $Y = \overline{A}$.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube	SN74ACT04N	SN74ACT0N
	SOIC − D	Tube	SN74ACT04D	ACT04
		Tape and reel	SN74ACT04DR	
	SOP − NS	Tape and reel	SN74ACT04NSR	ACT04
	SSOP − DB	Tape and reel	SN74ACT04DBR	AD04
	TSSOP − PW	Tube	SN74ACT04PW	AD04
		Tape and reel	SN74ACT04PWR	
−55°C to 125°C	CDIP − J	Tube	SNJ54ACT04J	SNJ54ACT04J
	CFP − W	Tube	SNJ54ACT04W	SNJ54ACT04W
	LCCC − FK	Tube	SNJ54ACT04FK	SNJ54ACT04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

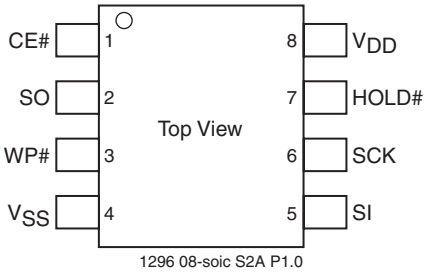
FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

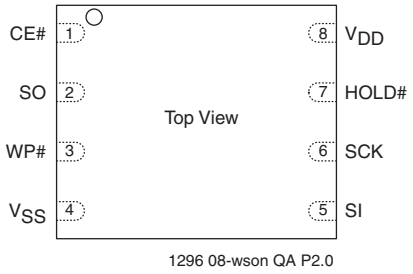
8 Mbit SPI Serial Flash
SST25VF080B

Data Sheet

PIN DESCRIPTION



8-LEAD SOIC



8-CONTACT WSON

FIGURE 1: PIN ASSIGNMENTS

TABLE 1: PIN DESCRIPTION

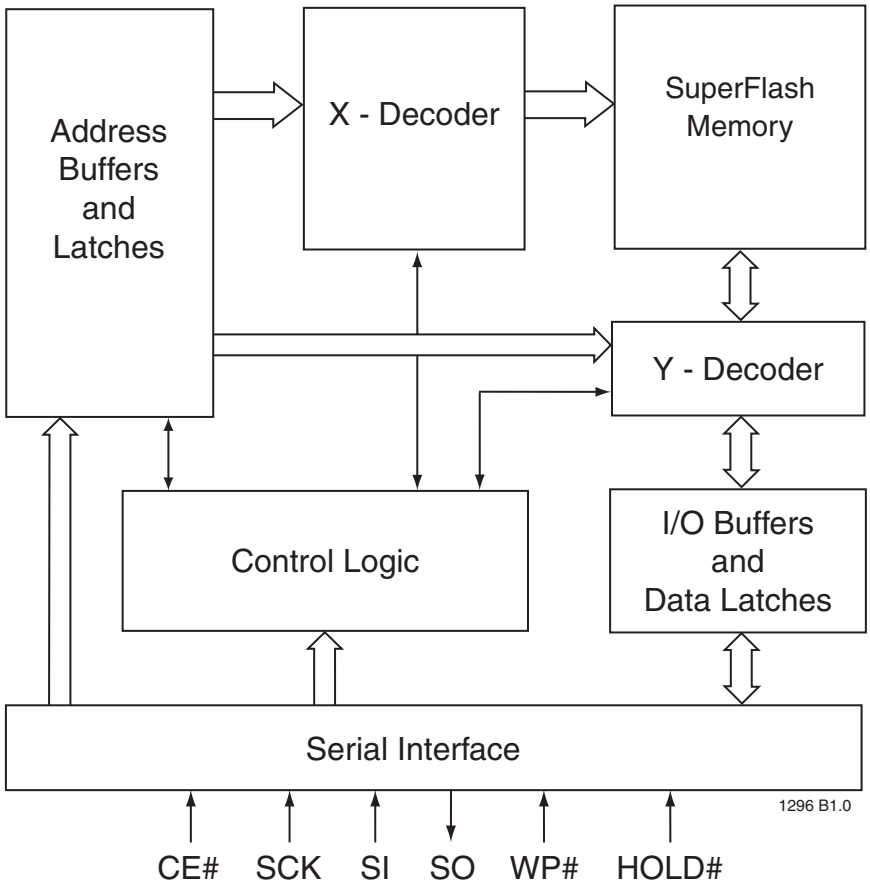
Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. Outputs Flash busy status during AAI Programming when reconfigured as RY/BY# pin. See “Hardware End-of-Write Detection” on page 12 for details.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence.
WP#	Write Protect	The Write Protect (WP#) pin is used to enable/disable BPL bit in the status register.
HOLD#	Hold	To temporarily stop serial communication with SPI flash memory without resetting the device.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V for SST25VF080B
V_{SS}	Ground	

T1.0 1296

8 Mbit SPI Serial Flash
SST25VF080B

Data Sheet

FUNCTIONAL BLOCK DIAGRAM



TOSHIBA TC74VCX541FT/FK/FTG

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VCX541FT, TC74VCX541FK, TC74VCX541FTG

Low-Voltage Octal Bus Buffer with 3.6 V Tolerant Inputs and Outputs

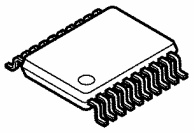
The TC74VCX541 is a high performance CMOS octal bus buffer which is guaranteed to operate from 1.2-V to 3.6-V. Designed for use in 1.5V, 1.8 V, 2.5 V or 3.3 V systems, it achieves high speed operation while maintaing the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

The device is a non-inverting 3-state buffer having two active-low output enables. When either $\overline{OE}1$ or $\overline{OE}2$ are high, the terminal outputs are in the high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

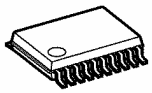
All inputs are equipped with protection circuits against static discharge.

TC74VCX541FT



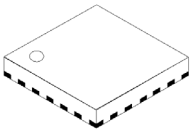
TSSOP20-P-0044-0.65A

TC74VCX541FK



VSSOP20-P-0030-0.50

TC74VCX541FTG



VQON20-0404-0.50

Weight

TSSOP20-P-0044-0.65A : 0.08 g (typ.)
VSSOP20-P-0030-0.50 : 0.03 g (typ.)
VQON20-P-0404-0.50 : 0.0145g (typ.)

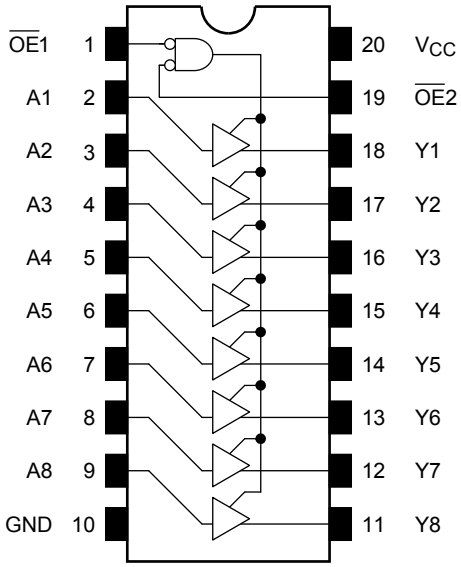
Features (Note 1)

- Low voltage operation: V_{CC} = 1.2~3.6 V
- High speed operation: t_{pd} = 3.5 ns (max) (V_{CC} = 3.0~3.6 V)
  t_{pd} = 4.2 ns (max) (V_{CC} = 2.3~2.7 V)
  t_{pd} = 8.4 ns (max) (V_{CC} = 1.65~1.95 V)
  t_{pd} = 16.8 ns (max) (V_{CC} = 1.4~1.6 V)
  t_{pd} = 42.0 ns (max) (V_{CC} = 1.2 V)
- 3.6 V tolerant inputs and outputs.
- Output current: I_{OH}/I_{OL} = ±24 mA (min) (V_{CC} = 3.0 V)
  I_{OH}/I_{OL} = ±18 mA (min) (V_{CC} = 2.3 V)
  I_{OH}/I_{OL} = ±6 mA (min) (V_{CC} = 1.65 V)
  I_{OH}/I_{OL} = ±2 mA (min) (V_{CC} = 1.4 V)
- Latch-up performance: −300 mA
- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Package: TSSOP
  VSSOP (US)
  VQON
- Power down protection is provided on all inputs and outputs.

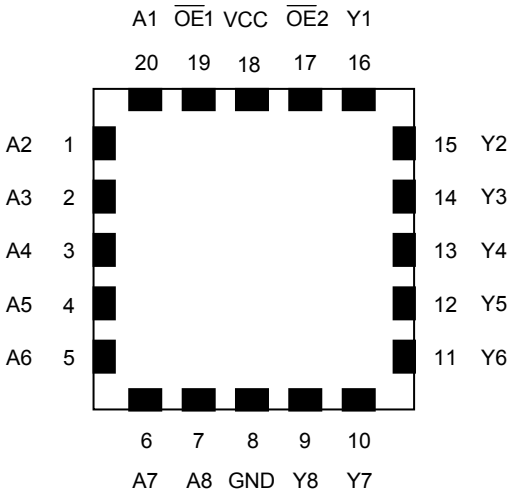
Note 1: When mounting VQON package, the type of recommended flux is RA or RMA.

Pin Assignment (top view)

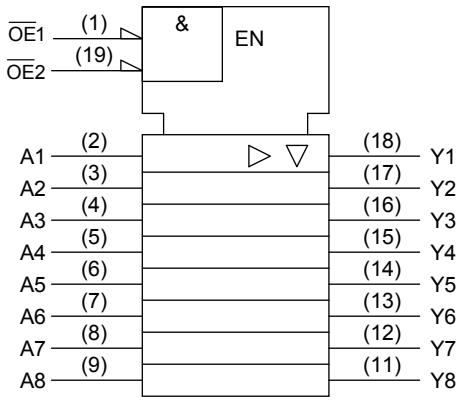
FT(TSSOP20-P-0044-0.65)
FK(VSSOP20-P-0030-0.50)



FTG(VQON20-P-0404-0.50)



IEC Logic Level



Truth Table

Inputs			Outputs
$\overline{OE}1$	$\overline{OE}2$	A_n	
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

X: Don't care

Z: High impedance

TOSHIBA TC74VHC157F/FN/FT

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC157F, TC74VHC157FN, TC74VHC157FT

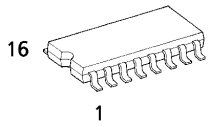
QUAD 2 - CHANNEL MULTIPLEXER

The TC74VHC157 is an advanced high speed CMOS QUAD 2 - CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
It consists of four 2 - input digital multiplexers with common select and strobe inputs.
When the $\overline{STROBE}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level.
The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.
An Input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

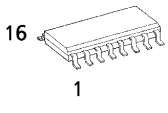
FEATURES :

- High Speed ····· t_{pd} = 4.1ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr) = 2V ~ 5.5V
- Low Noise ····· V_{OLP} = 0.8V (Max.)
- Pin and Function Compatible with 74ALS157

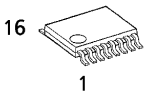
(Note) The JEDEC SOP (FN) is not available in Japan.



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

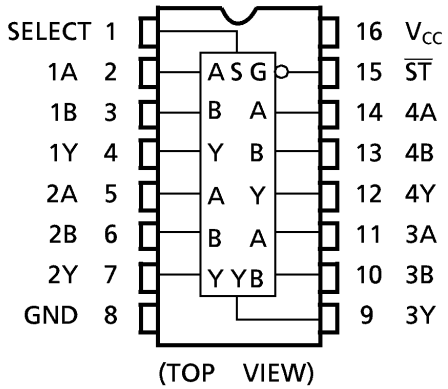


FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)



FT (TSSOP16-P-0044-0.65)
Weight : 0.06g (Typ.)

PIN ASSIGNMENT



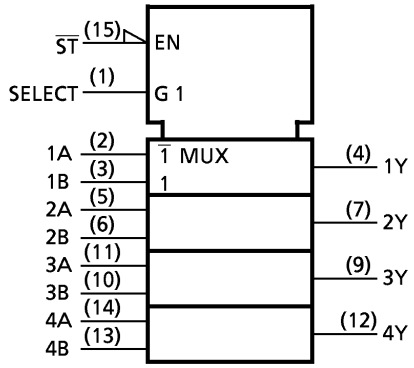
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUT
$\overline{ST}$	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X : Don't Care

IEC LOGIC SYMBOL

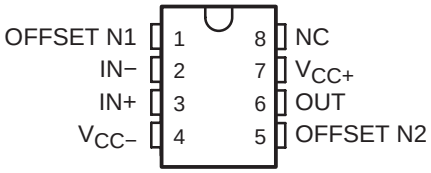


980910EBA2

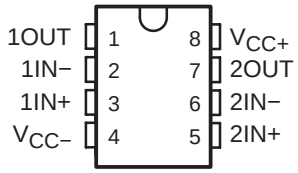
TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080J − SEPTEMBER 1978 − REVISED MARCH 2005

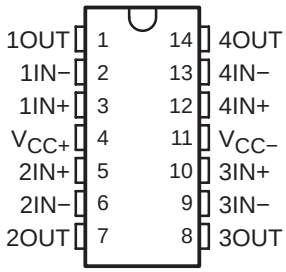
TL071, TL071A, TL071B
D, P, OR PS PACKAGE
(TOP VIEW)



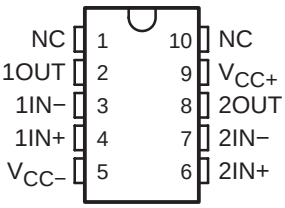
TL072, TL072A, TL072B
D, JG, P, PS, OR PW PACKAGE
(TOP VIEW)



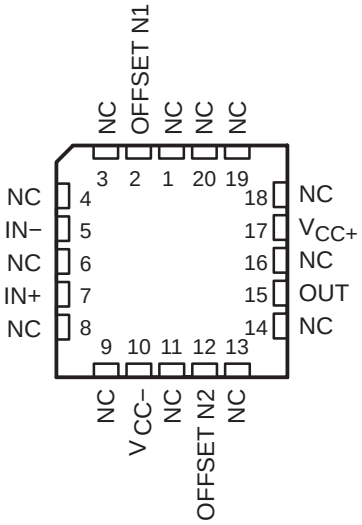
TL074A, TL074B
D, J, N, NS, OR PW PACKAGE
TL074 . . . D, J, N, NS, PW,
OR W PACKAGE
(TOP VIEW)



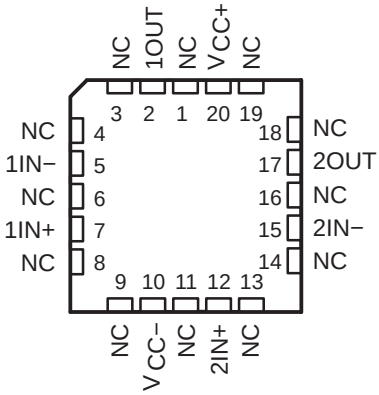
TL072
U PACKAGE
(TOP VIEW)



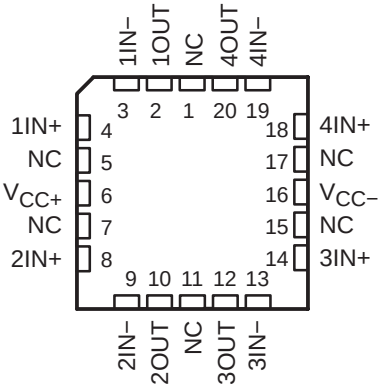
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)



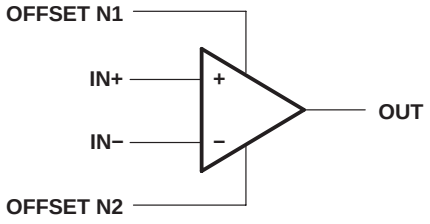
TL074
FK PACKAGE
(TOP VIEW)



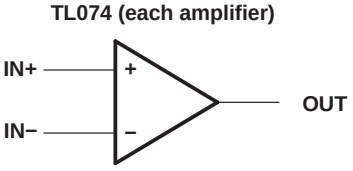
NC − No internal connection

symbols

TL071



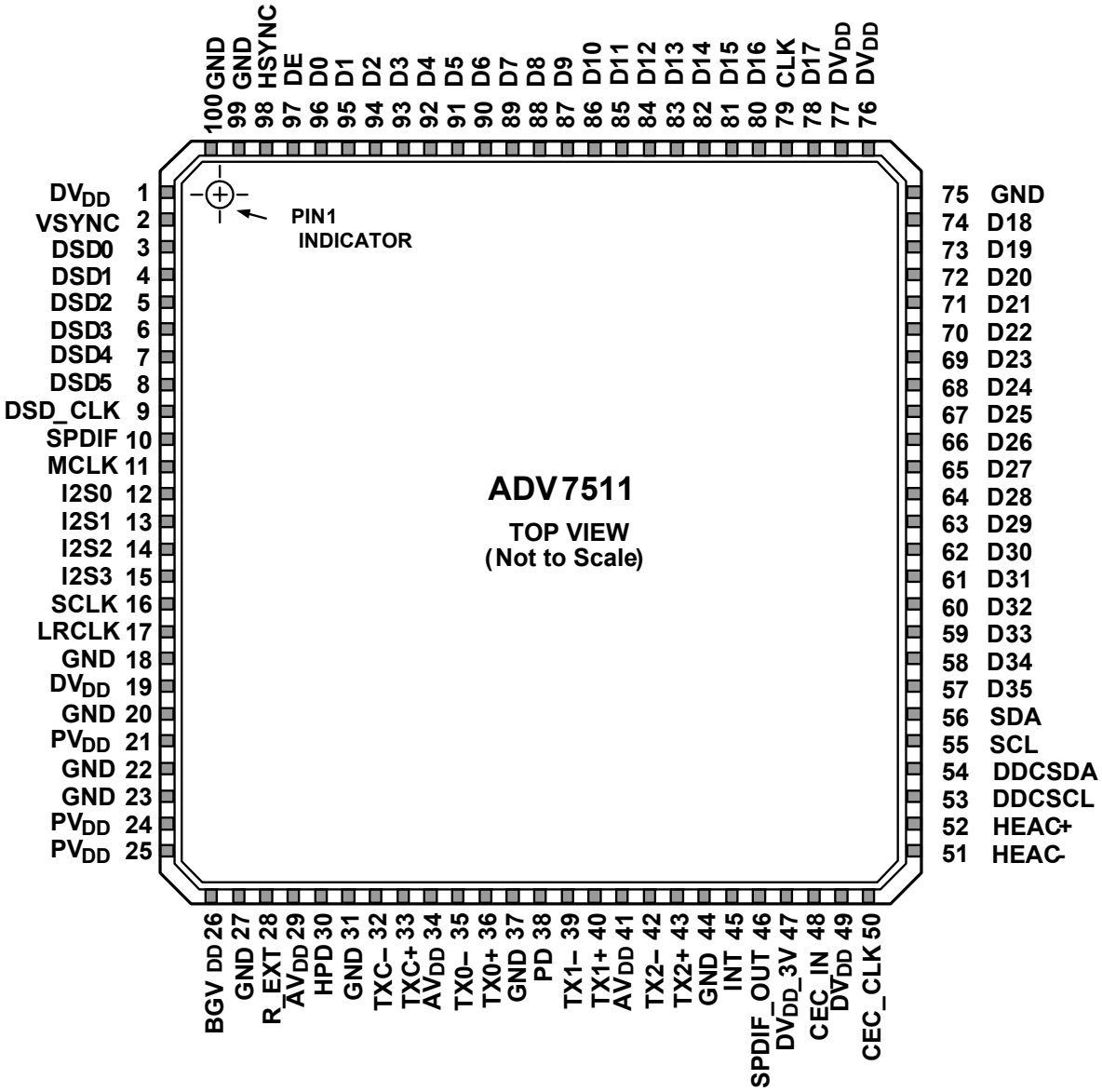
TL072 (each amplifier)
TL074 (each amplifier)



SECTION 5: PIN AND PACKAGE INFORMATION

This section shows the pinout of the ADV7511 100-lead LQFP package. This section also contains a brief description of the different pins as well as the mechanical drawings

Figure 6 100-lead LQFP configuration (top view - not to scale)



ADV7511 ADI Confidential

Rev. PrB

Table 3 Complete Pinout List ADV7511

Pin No.	Mnemonic	Type[1]	Description
57-74, 78, 80-96	D[35:0]	I	Video Data Input. Digital input in RGB or YCbCr format. Supports typical CMOS logic levels from1.8V up to 3.3V. See ►Figure 2 for timing details.
79	CLK	I	Video Clock Input. Supports typical CMOS logic levels from 1.8V up to 3.3V.
97	DE	I	Data Enable signal input for Digital Video. Supports typical CMOS logic levels from 1.8V up to 3.3V.
98	HSYNC	I	Horizontal Sync Input. Supports typical CMOS logic levels from 1.8V up to 3.3V.
2	VSYNC	I	Vertical Sync Input. Supports typical CMOS logic levels from 1.8V up to 3.3V.
28	R_EXT	I	Sets internal reference currents. Place 887 Ω resistor (1% tolerance) between this pin and ground.
51	HEAC-	I	HEAC- is one of a pair of differential lines for the ARC (Audio Return Channel)
52	HEAC+	I	HEAC+ is one of a pair of differential lines for the ARC (Audio Return Channel)
30	HPD	I	Hot Plug Detect signal input. This indicates to the interface whether the sink is connected. 1.8V to 5.0 V CMOS logic level.
10	S/PDIF	I	S/PDIF (Sony/Philips Digital Interface) Audio Input. This pin is typically used as the audio input from a Sony/Philips digital interface. Supports typical CMOS logic levels from 1.8V up to 3.3V. See ► Figure 4 for timing details.
46	S/PDIF_OUT	O	S/PDIF Audio Output from ARC receiver.
11	MCLK	I	Audio Reference Clock input. 128 × N × f_S with N = 1, 2, 3, or 4. Set to 128 × sampling frequency (f_S), 256 × f_S, 384 × f_S, or 512 × f_S. Supports typical CMOS logic levels from 1.8V up to 3.3V.
15-12	I^2S[3:0]	I	I^2S Audio Data Inputs. These represent the eight channels of audio (two per input) available through I^2S. Supports typical CMOS logic levels from 1.8V up to 3.3V. See **Figure** 3 for timing details.
16	SCLK	I	I^2S Audio Clock input. Supports typical CMOS logic levels from 1.8V up to 3.3V.
17	LRCLK	I	Left/Right Channel signal input. Supports typical CMOS logic levels from1.8V up to 3.3V.
8-3	DSD[5:0]	I	DSD audio data inputs. See ▶ Figure 5 for timing details.
9	DSD_CLK	I	DSD Clock input. This is a 2.8224MHz clock for the DSD audio inputs.
38	PD/AD	I	Power-Down Control and I^2C Address Selection. The I^2C address and the PD polarity are set by the PD/AD pin state when the supplies are applied to the ADV7511. Supports typical CMOS logic levels from 1.8V up to 3.3V.
32, 33	TxC−/TxC+	O	Differential TMDS Clock Output. Differential clock output at pixel clock rate; TMDS logic level.
42, 43	Tx2−/Tx2+	O	Differential TMDS Output Channel 2. Differential output of the red data at 10× the pixel clock rate; TMDS logic level.
39, 40	Tx1−/Tx1+	O	Differential TMDS Output Channel 1. Differential output of the green data at 10× the pixel clock rate; TMDS logic level.
35, 36	Tx0−/Tx0+	O	Differential TMDS Output Channel 0. Differential output of the blue data at 10× the pixel clock rate; TMDS logic level.
45	INT	O	Interrupt signal output. CMOS logic level. A 2 kΩ pull-up resistor (10%) to interrupt the microcontroller IO supply is recommended.
29, 34, 41	AVDD	P	1.8V Power Supply for TMDS Outputs.
1, 19, 49, 76, 77	DVDD	P	1.8V Power Supply for Digital and I/O Power Supply. These pins supply power to the digital logic and I/Os. They should be filtered and as quiet as possible.
24, 25	PVDD	P	1.8V PLL Power Supply. These pins provide power to the digital portion of the clock PLL. The designer should provide quiet, noise-free power to these pins.
21	PLVDD	P	1.8V PLL Power Supply. The most sensitive portion of the ADV7511 is the clock generation circuitry. These pins provide power to the analog portion of the clock PLL (VCO). The designer should provide quiet, noise-free power to these pins.
26	BGVDD	P	Band Gap Vdd.

47	MVDD	P	3.3V Power Supply.
18, 20, 22, 23, 27, 31, 37, 44, 46, 51, 75, 99, 100	GND	P	Ground. The ground return for all circuitry on-chip. It is recommended that the ADV7511 be assembled on a single, solid ground plane with careful attention given to ground current paths.
56	SDA	C	Serial Port Data I/O. This pin serves as the serial port data I/O slave for register access. Supports CMOS logic levels from 1.8V to 3.3V.
55	SCL	C	Serial Port Data Clock input. This pin serves as the serial port data clock slave for register access. Supports CMOS logic levels from 1.8V to 3.3V.
54	DDCSDA	C	Serial Port Data I/O to Sink. This pin serves as the master to the DDC bus. Tolerant of 5 V CMOS logic levels.
53	DDCSCL	C	Serial Port Data Clock to Sink. This pin serves as the master clock for the DDC bus. Tolerant of 5 V CMOS logic levels.
50	CEC_CLK	I	CEC clock. From 1MHz to 100Mhz. Supports CMOS logic levels from 1.8V to 5V.
48	CEC_IO	I/O	CEC data signal. Supports CMOS logic levels from 1.8V to 5V.

1. I = input, O = output, P = power supply, C = control

Advanced Analog Circuits

Data Sheet

DUAL LOW NOISE OPERATIONAL AMPLIFIERS AZ4580

Pin Configuration

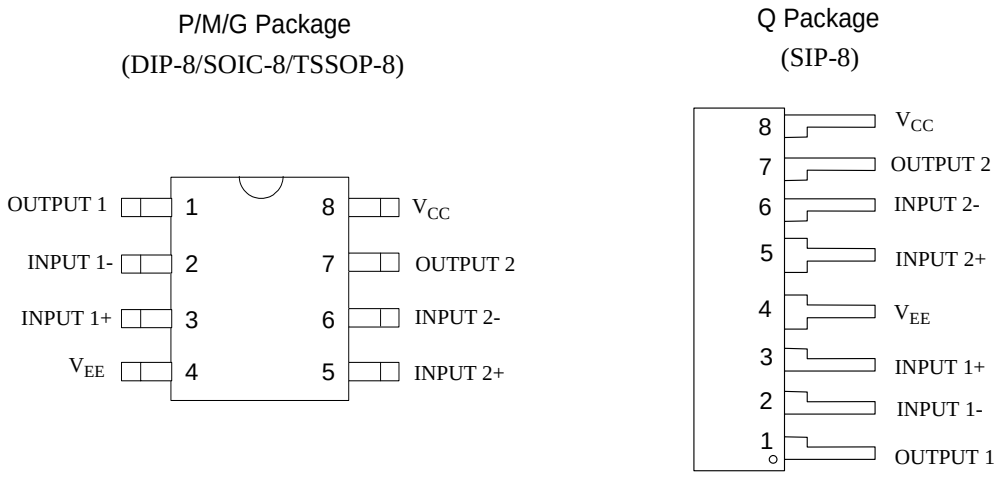


Figure 2. Pin Configuration of AZ4580 (Top View)

Pin Description

Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	OUTPUT 1	2	INPUT 1-	3	INPUT 1+	4	V_{EE}
5	INPUT 2+	6	INPUT 2-	7	OUTPUT 2	8	V_{CC}

CIRRUS LOGIC
Leading the Digital Entertainment Revolution™

CS42528

114 dB, 192 kHz 8-Ch Codec with S/PDIF Receiver

Features

- Eight 24-bit D/A, two 24-bit A/D Converters
- 114 dB DAC / 114 dB ADC Dynamic Range
- -100 dB THD+N
- System Sampling Rates up to 192 kHz
- S/PDIF Receiver Compatible with EIAJ CP1201 and IEC-60958
- Recovered S/PDIF Clock or System Clock Selection
- 8:2 S/PDIF Input MUX
- ADC High-pass Filter for DC Offset Calibration
- Expandable ADC Channels and One-line Mode Support
- Digital Output Volume Control with Soft Ramp
- Digital +/-15dB Input Gain Adjust for ADC
- Differential Analog Architecture
- Supports logic levels between 5 V and 1.8 V.

General Description

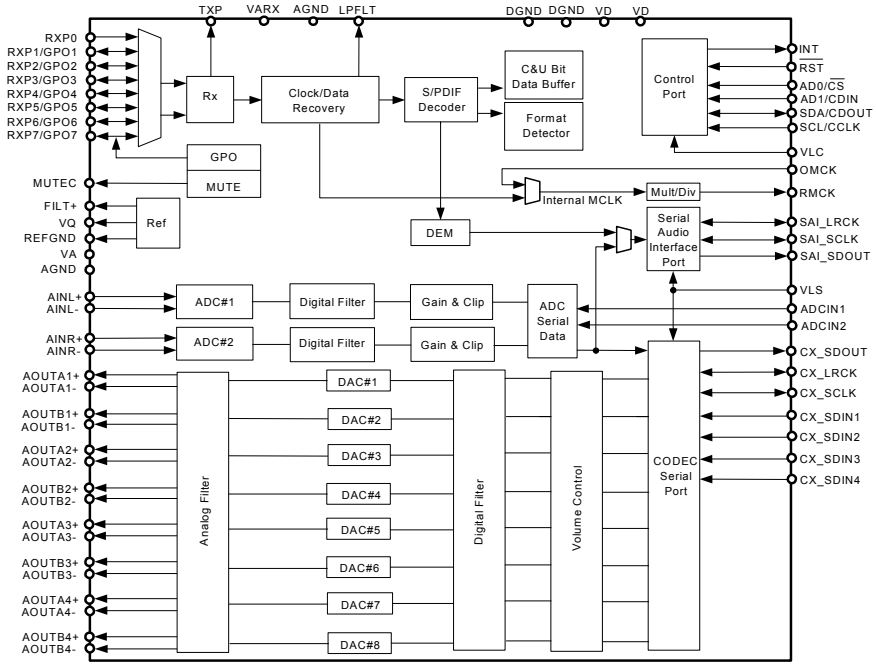
The CS42528 codec provides two analog-to-digital and eight digital-to-analog delta-sigma converters, as well as an integrated S/PDIF receiver, in a 64-pin LQFP package.

The CS42528 integrated S/PDIF receiver supports up to eight inputs, clock recovery circuitry and format auto-detection. The internal stereo ADC is capable of independent channel gain control for single-ended or differential analog inputs. All eight channels of DAC provide digital volume control and differential analog outputs. The general purpose outputs may be driven high or low, or mapped to a variety of DAC mute controls or ADC overflow indicators.

The CS42528 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, digital speaker and automotive audio systems.

ORDERING INFORMATION

CS42528-CQZ	-10° to 70° C	64-pin LQFP	Lead Free
CS42528-DQZ	-40° to 85° C	64-pin LQFP	Lead Free
CDB42528	Evaluation Board		



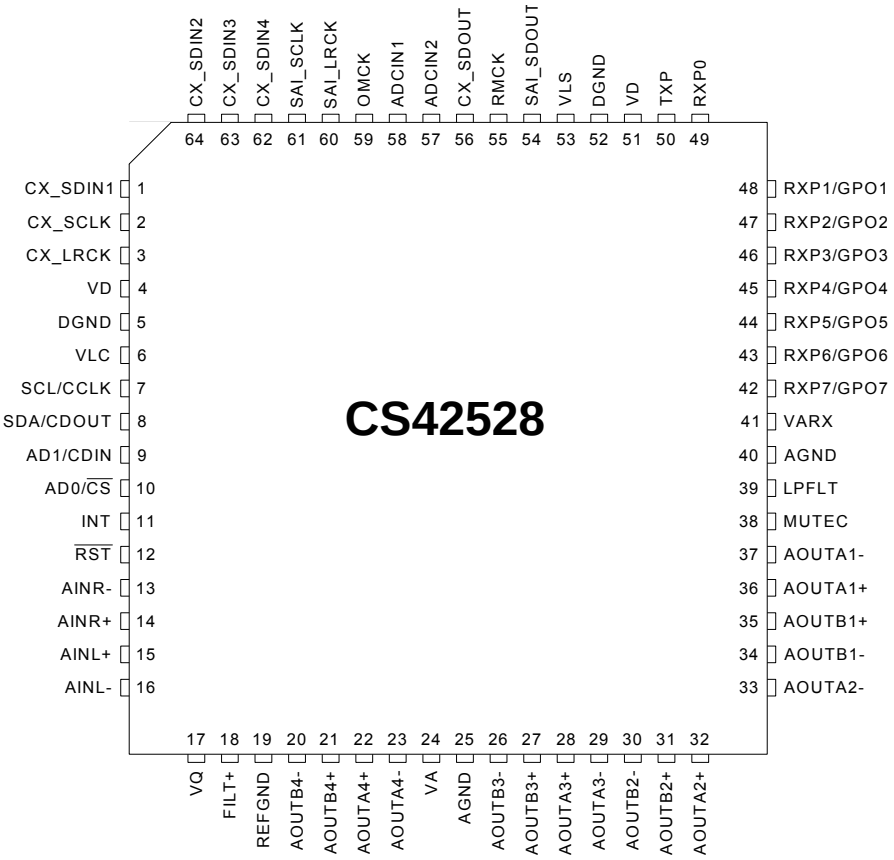
Preliminary Product Information

Cirrus Logic, Inc.
http://www.cirrus.com

CIRRUS LOGIC

CS42528

2. PIN DESCRIPTIONS



Pin Name	#	Pin Description
CX_SDIN1 **CX_SDIN2** **CX_SDIN3** **CX_SDIN4**	1 64 63 62	**Codec Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
CX_SCLK	2	**CODEC Serial Clock** *(Input/Output)* - Serial clock for the CODEC serial audio interface.
CX_LRCK	3	**CODEC Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the CODEC serial audio data line.
VD	4 51	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	5 52	**Digital Ground** (*Input*) - Ground reference. Should be connected to digital ground.
VLC	6	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port.
SCL/CCLK	7	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I^2C mode as shown in the Typical Connection Diagram.
SDA/CDOUT	8	**Serial Control Data** (*Input/Output*) **-** SDA is a data I/O line in I^2C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDOUT is the output data line for the control port interface in SPI mode.
AD1/CDIN	9	**Address Bit 1 (I^2C)/Serial Control Data (SPI)** (*Input*) - AD1 is a chip address pin in I^2C mode; CDIN is the input data line for the control port interface in SPI mode.

AD0/$\overline{CS}$	10	**Address Bit 0 (I^2C)/Control Port Chip Select (SPI)** *(Input)* **-** AD0 is a chip address pin in I^2C mode; $\overline{CS}$ is the chip select signal in SPI mode.
INT	11	**Interrupt** *(Output)* - The CS42528 will generate an interrupt condition as per the Interrupt Mask register. See “Interrupts” on page 40 for more details.
$\overline{RST}$	12	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
AINR- **AINR+**	13 14	**Differential Right Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
AINL+ **AINL-**	15 16	**Differential Left Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins.
VQ	17	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
REFGND	19	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
AOUTA1 +,- **AOUTB1 +,-** **AOUTA2 +,-** **AOUTB2 +,-** **AOUTA3 +,-** **AOUTB3 +,-** **AOUTA4 +,-** **AOUTB4 +,-**	36,37 35,34 32,33 31,30 28,29 27,26 22,23 21,20	**Differential Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
VA **VARX**	24 41	**Analog Power** (*Input*) - Positive power supply for the analog section.
AGND	25 40	**Analog Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MUTEC	38	**Mute Control** (*Output*) - The Mute Control pin outputs high impedance following an initial power-on condition or whenever the PDN bit is set to a ‘1’, forcing the codec into power-down mode. The signal will remain in a high impedance state as long as the part is in power-down mode. The Mute Control pin goes to the selected “active” state during reset, muting, or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
LPFLT	39	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and ground.
RXP7/GPO7 **RXP6/GPO6** **RXP5/GPO5** **RXP4/GPO4** **RXP3/GPO3** **RXP2/GPO2** **RXP1/GPO1**	42 43 44 45 46 47 48	**S/PDIF Receiver Input/ General Purpose Output** (*Input/Output*) - Receiver inputs for S/PDIF encoded data. The CS42528 has an internal 8:2 multiplexer to select the active receiver port, according to the Receiver Mode Control 2 register. These pins can also be configured as general purpose output pins, ADC Overflow indicators or Mute Control outputs according to the RXP/General Purpose Pin Control registers.
RXP0	49	**S/PDIF Receiver Input** (*Input*) - Dedicated receiver input for S/PDIF encoded data.
TXP	50	**S/PDIF Transmitter Output** (*Output*) - S/PDIF encoded data output, mapped directly from one of the receiver inputs as indicated by the Receiver Mode Control 2 register.
VLS	53	**Serial Port Interface Power** (*Input*) - Determines the required signal level for the serial port interfaces.
SAI_SDOUT	54	**Serial Audio Interface Serial Data Output** (*Output*) - Output for two’s complement serial audio PCM data from the S/PDIF incoming stream. This pin can also be configured to transmit the output of the internal and external ADCs.
RMCK	55	**Recovered Master Clock** (*Output*) - Recovered master clock output from the External Clock Reference (OMCK, pin 59) or the PLL which is locked to the incoming S/PDIF stream or CX_LRCK.

CX_SDOUT	56	**CODEC Serial Data Output** (*Output*) - Output for two's complement serial audio data from the internal and external ADCs.
ADCIN1 **ADCIN2**	58 57	**External ADC Serial Input** (*Input*) - The CS42528 provides for up to two external stereo analog to digital converter inputs to provide a maximum of six channels on one serial data output line when the CS42528 is placed in One Line mode.
OMCK	59	**External Reference Clock** (*Input*) - External clock reference that must be within the ranges specified in the register "OMCK Frequency (OMCK Freqx)" on page 54.
SAI_LRCK	60	**Serial Audio Interface Left/Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SAI_SCLK	61	**Serial Audio Interface Serial Clock** *(Input/Output)* - Serial clock for the Serial Audio Interface.

CIRRUS LOGIC

CS4970x4 Data Sheet

FEATURES

- Multi-standard 32-bit High Definition Audio Decoding plus Post-Processing
- Supports high-definition audio formats including:
  - Dolby Digital® Plus
  - Dolby® TrueHD
  - DTS-HD® High Resolution Audio
  - DTS-HD® Master Audio
  - DTS Express™
- Additional Applications Library
  - Dolby Digital® EX, Dolby® Pro Logic® IIz, Dolby Headphone 2®, Dolby® Virtual Speaker 2®, Audistry®
  - DTS-ES 96/24™ Discrete 7.1, DTS-ES™ Discrete 7.1, DTS-ES™ Matrix 6.1, DTS Neo:6®, DTS Neural Surround™
  - DSD®
  - MPEG-2 AAC™ LC 5.1
  - SRS® CS2®, SRS TruVolume™, SRS® TruSurround HD4™, WOW HD™,
  - THX® Ultra2™, THX® ReEQ™
  - Thomson MP3 Surround
  - Audyssey 2EQ™ Module
- Cirrus Logic's Applications Library
  - Cirrus Original Multi-Channel Surround 2 (COMS2), Cirrus Band Xpander™, Cirrus Virtualization Technology, Cirrus Intelligent Room Calibration 2 (IRC2)
  - Crossbar Mixer, Signal Generator
  - Advanced Post-Processors including: 7.1 Bass Manager, Tone Control, 11- Band Parametric EQ, Delay, 2:1/4:1 Decimator, 1:2/1:4 Upsampler

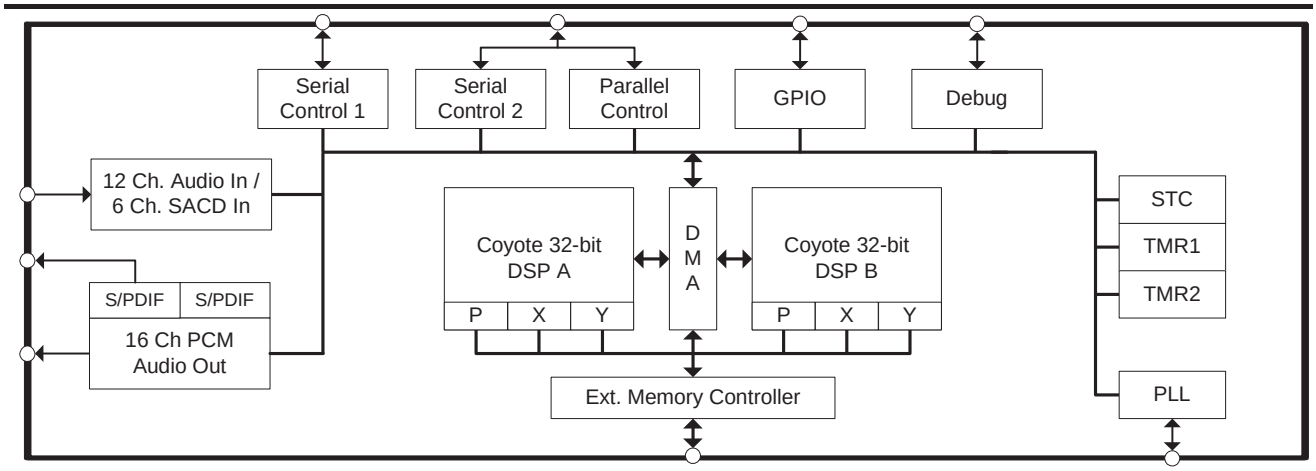
High Definition Audio Decoder DSP Family with Dual 32-bit DSP Engine Technology

- Up to 12 Channels of 32-bit Serial Audio Input
- Customer Software Security Keys
- 16 Ch x 32-bit PCM Out with Dual 192 kHz SPDIF Tx
- Two SPI™/I²C™ ports
- One Parallel Port (144-pin LQFP package only)
- Large On-chip X, Y, and Program RAM & ROM
- SDRAM and Serial Flash Memory Support

The CS4970x4 DSP family is an enhanced version of the CS4953x DSP family with higher overall performance. In addition to all the mainstream audio processing codes in on-chip ROM that the CS4953x DSP offers, the CS4970x4 device family also supports the decoding of major high-definition audio formats. Additionally, the CS4970x4, a dual-core device, performs the high-definition audio decoding on the first core, leaving the second core available for audio post-processing and audio enhancement. The CS4970x4 device supports the most demanding audio post processing requirements. It provides an easy upgrade path to systems currently using the CS495xx or CS4953x device with minor hardware and software changes.

Ordering Information

See page 28 for ordering information.



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

8. Device Pin-Out Diagram

8.1 128-Pin LQFP Pin-Out Diagram

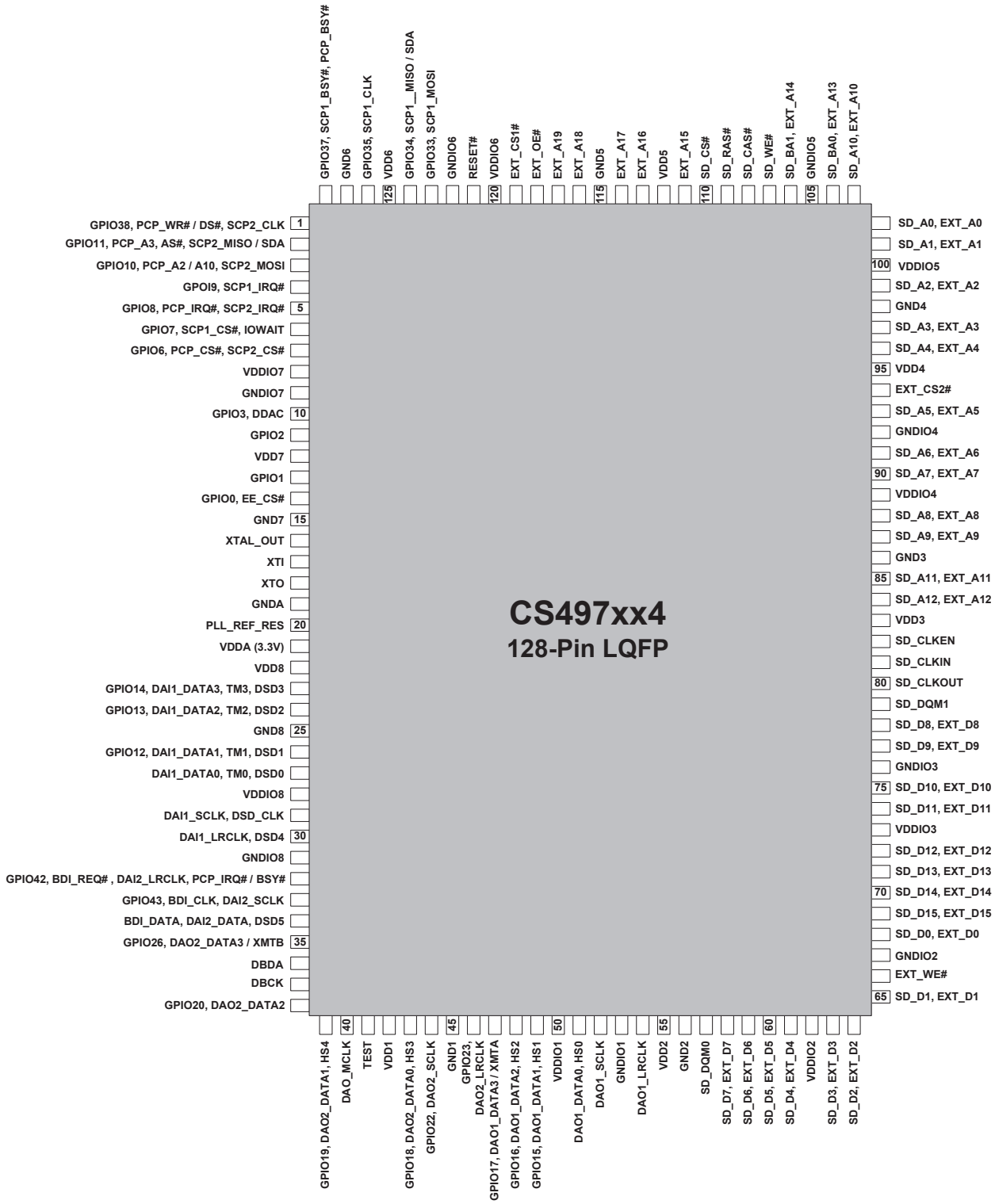


Figure 19. 128-Pin LQFP Pin-Out Diagram

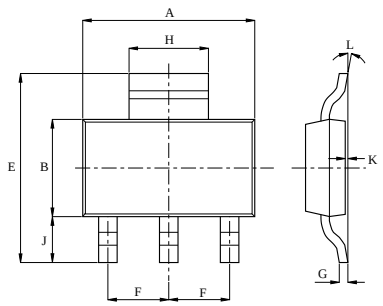
KEC

SEMICONDUCTOR
TECHNICAL DATA

KIA1117BS/BF00~ KIA1117BS/BF50
BIPOLAR LINEAR INTEGRATED CIRCUIT

LOW DROP FIXED AND ADJUSTABLE POSITIVE VOLTAGE REGULATOR

The KIA1117BS/BF × × Series are a Low Drop Voltage Regulator able to provide up to 1A of output current, available even in adjustable version (Vref=1.25V)



DIM	MILLIMETERS
A	6.5±0.2
B	3.5±0.2
C	1.8 MAX
D	0.7+0.15/-0.1
E	7±0.3
F	2.3 TYP
G	0.26+0.09/-0.02
H	3.0+0.15/-0.1
J	1.75±0.25
K	0.1 MAX
L	10° MAX

1. GND (Adj.)
2. OUTPUT
3. INPUT

Heat Sink is common to ② (Output)

SOT-223

FEATURES

· Low Dropout Voltage : 1.1V/Typ. (Iout=1.0A)
· Very Low Quiescent Current : 2.5㎃/Typ.
· Output Current up to 1A
· Fixed Output Voltage of 1.2V, 1.5V, 1.8V, 2.5V, 2.85V, 3.3V, 5.0V
· Adjustable Version Availability : Vref=1.25V
· Internal Current and Thermal Limit
· A Minimum of 10㎌ for stability
· Suitable for MLCC, Tantalum and Low ESR Electrolytic Capacitors
· ESR Range for stability : 1mΩ~200Ω
· Available in ±2%(at 25℃)
· High Ripple Rejection : 80dB/Typ
· Temperature Range : -40℃~150℃

LINE UP

ITEM	OUTPUT VOLTAGE (V)	PACKAGE
KIA1117BS/BF00	Adjustable (1.25~8V)	S : SOT-223 F : DPAK
KIA1117BS/BF12	1.2	
KIA1117BS/BF15	1.5	
KIA1117BS/BF18	1.8	
KIA1117BS/BF25	2.5	
KIA1117BS/BF28	2.85	
KIA1117BS/BF33	3.3	
KIA1117BS/BF50	5.0	

MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage		V_{IN}	10	V
Output Current		I_{OUT}	1.0	A
Power Dissipation 1 (No Heatsink)	S (Note)	P_{D1}	1.0	W
	F		1.3	
Power Dissipation 2 (Infinite Heatsink)	S	P_{D2}	8.3	W
	F		13	
Maximum Junction Temperature		$T_{j(max)}$	150	℃
Operating Junction Temperature		T_{opr}	-40~150	℃
Storage Temperature		T_{stg}	-55~150	℃

Note) Package Mounted on FR-4 PCB 36 ×18 ×1.5㎜

cm^2

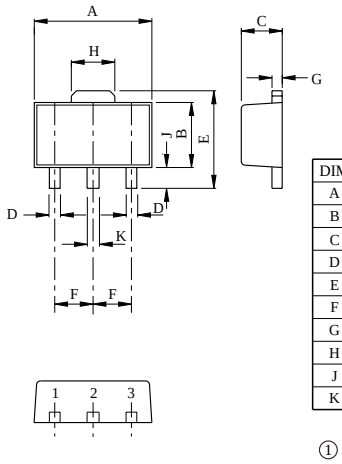
KEC

SEMICONDUCTOR
TECHNICAL DATA

KIC3201S/T-12 ~ KIC3201S/T-60
CMOS Linear Integrated Circuit

Large Current Positive Voltage Regulator

The KIC3201S/T series are highly precise, low power consumption, positive voltage regulators manufactured using CMOS and laser trimming technologies. The series provides large currents with a significantly small dropout voltage. The KIC3201S/T consists of a driver transistor, a precision reference voltage and an error amplifier. Output voltage is selectable in 0.05V steps between a voltage of 1.2V and 6.0V.



DIM	MILLIMETERS
A	4.70 MAX
B	2.50±0.20
C	1.70 MAX
D	0.45+0.15/-0.10
E	4.25 MAX
F	1.50±0.10
G	0.40 TYP
H	1.75 MAX
J	0.75 MIN
K	0.5+0.10/-0.05

① GND
② V_{IN}
③ V_{OUT}

• Heat Sink is common to ② (V_{IN})

SOT-89

Features

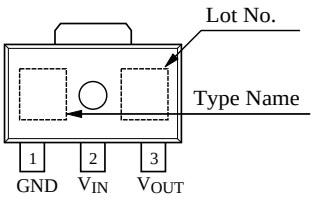
· Maximum Output Current : 400mA
· Dropout Voltage : 150mV @100mA, 300mV @200mA for V_{OUT}=3.0V
· Maximum Operating Voltage : 10V
· Output Voltage Range :
1.2V ~ 6.0V (selectable in 0.05V steps)
· Highly Accurate : ±2%
· Low Power Consumption : Typ. 8.0uA
· Operational Temperature Range : -40℃ ~ 85℃
· Low ESR Capacitor : Ceramic compatible or Tantalum

Applications

· Battery Powered Equipment
· Reference Voltage Sources
· Digital Cameras, Camcoders
· Palmtop Computers
· Portable Audio Video Equipment

Pin Configuration

KIC3201S-XX



SOT-89
(TOP VIEW)

No.	Symbol	Description
1	GND	Ground
2	V_{IN}	Power input
3	V_{OUT}	Output

• Heat Sink is common to ② (V_{IN})

KEC

SEMICONDUCTOR
TECHNICAL DATA

KTC812T
EPITAXIAL PLANAR NPN TRANSISTOR

FOR MUTING AND SWITCHING APPLICATION.

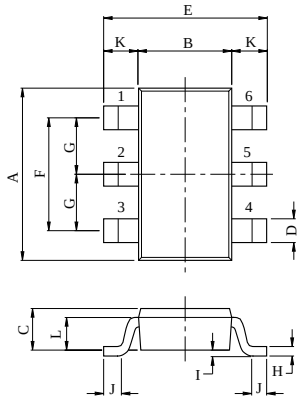
FEATURES

· High Emitter-Base Voltage : V_{EBO}=25V(Min.)

· High Reverse h_{FE}

: Reverse h_{FE}=150(Typ.) (V_{CE}=-2V, I_C=-4mA)

· Low on Resistance : R_{ON}=1Ω(Typ.), (I_B=5mA)



DIM	MILLIMETERS
A	2.9±0.2
B	1.6+0.2/-0.1
C	0.70±0.05
D	0.4±0.1
E	2.8+0.2/-0.3
F	1.9±0.2
G	0.95
H	0.16±0.05
I	0.00-0.10
J	0.25+0.25/-0.15
K	0.60
L	0.55

1. Q_1 EMITTER
2. Q_1 BASE
3. Q_2 COLLECTOR
4. Q_2 EMITTER
5. Q_2 BASE
6. Q_1 COLLECTOR

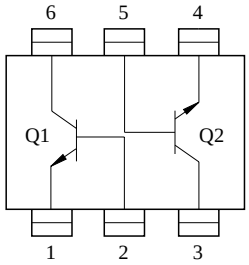
TS6

MAXIMUM RATING (Ta=25℃)

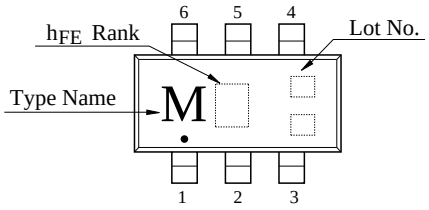
CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	20	V
Emitter-Base Voltage	V_{EBO}	25	V
Collector Current	I_C	300	mA
Base Current	I_B	60	mA
Collector Power Dissipation	P_C *	0.9	mW
Junction Temperature	T_j	150	℃
Storage Temperature Range	T_{stg}	-55 ~150	℃

* Package mounted on a ceramic board (600㎟×0.8㎜)

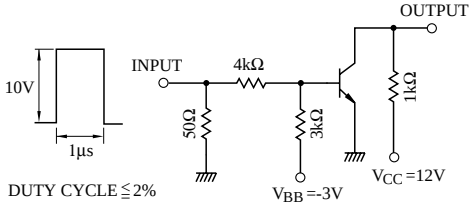
EQUIVALENT CIRCUIT (TOP VIEW)



Marking



ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current		I_{CBO}	V_{CB}=50V, I_E=0	-	-	0.1	μA
Emitter Cut-off Current		I_{EBO}	V_{EB}=25V, I_C=0	-	-	0.1	μA
DC Current Gain		h_{FE}	V_{CE}=2V, I_C=4mA	350	-	1200	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	I_C=30mA, I_B=3mA	-	0.042	0.3	V
Base-Emitter Voltage		V_{BE}	V_{CE}=2V, I_C=4mA	-	0.61	-	V
Transition Frequency		f_T	V_{CE}=6V, I_C=4mA	-	30	-	MHz
Collector Output Capacitance		C_{ob}	V_{CB}=10V, I_E=0, f=1MHz	-	4.8	7	pF
Switching Time	Turn-on Time	t_{on}		-	160	-	nS
	Storage Time	t_{stg}		-	500	-	
	Fall Time	t_f		-	130	-	

Note : h_{FE} Classification B: 350 ~1200

JRC

NJU7751/54

LOW DROPOUT VOLTAGE REGULATOR

■ GENERAL DISCRIPTION

NJU7751/54 is a low dropout voltage regulator with ON/OFF control and Output shunt switch.

Advanced CMOS technology achieves high ripple rejection and ultra low quiescent current.

It is suitable for reset small micro controller and other logic chips.

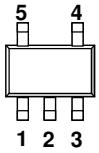
■ PACKAGE OUTLINE

NJU7751/54F

■ FEATURES

- Ultra Low quiescent Current Iq=20μA typ.(I_O=0mA)
- Output capacitor with 1.0uF ceramic capacitor
- Output Current I_O(max.)=100mA
- High Precision Output V_O±1.0%
- Low Dropout Voltage 0.15V typ. (I_O=60mA, V_O=3V)
- With ON/OFF Control (Active High)
- With Output Shunt Switch
- Internal Short Circuit Current Limit
- CMOS Technology
- Package Outline SOT-23-5

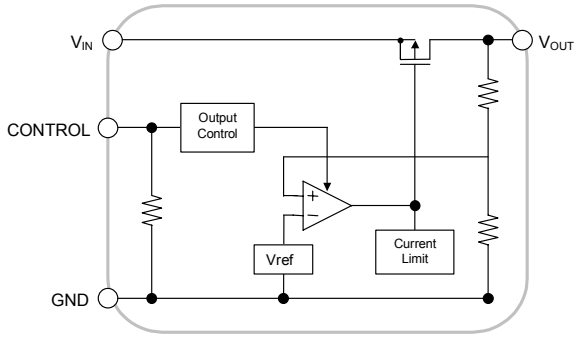
■ PIN CONFIGURATION



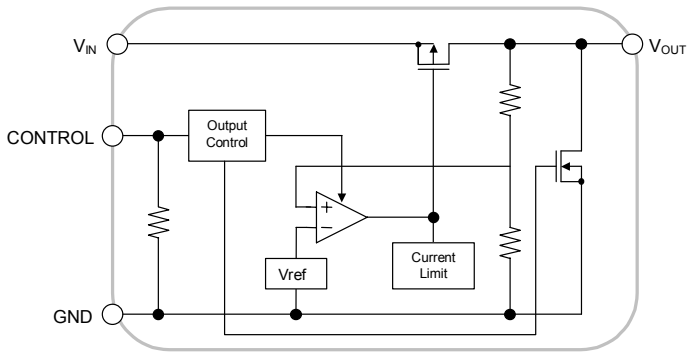
NJU7751/54F

PIN FUNCTION
1.CONTROL
2.GND
3.N.C.
4.V_{OUT}
5.V_{IN}

■ EQUIVALENT CIRCUIT



NJU7751



NJU7754

■ OUTPUT VOLTAGE RANK LIST

DEVICE NAME	V_{OUT}
NJU775*F21	2.1V
NJU775*F25	2.5V
NJU775*F03	3.0V
NJU775*F33	3.3V
NJU775*F05	5.0V

KEC

SEMICONDUCTOR TECHNICAL DATA

KIA278R05PI~KIA278R15PI

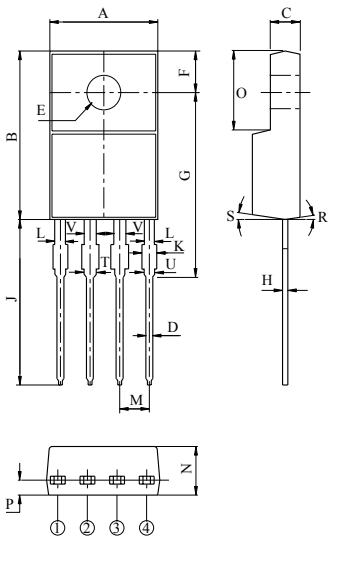
BIPOLAR LINEAR INTEGRATED CIRCUIT

4 TERMINAL 2A OUTPUT LOW DROP VOLTAGE REGULATOR

The KIA278R×× Series are Low Drop Voltage Regulator suitable for various electronic equipments.
It provides constant voltage power source with TO-220 4 terminal lead full molded PKG. The Regulator has multi function such as over current protection, overheat protection and ON/OFF control.

FEATURES

- 2.0A Output Low Drop Voltage Regulator.
- Built in ON/OFF Control Terminal.
- Built in Over Current Protection, Over Heat Protection Function.



DIM	MILLIMETERS
A	10.00±0.20
B	15.00±0.20
C	2.70±0.20
D	0.60±0.10
E	Φ3.20±0.20
F	3.50±0.10
G	15.70±0.20
H	0.40±0.10
J	14.3+0.2/-0.1
K	1.45±0.10
L	1.00±0.10
M	2.54
N	4.50±0.20
O	7.5± 0.1
P	1.50±0.10
R	5 °
S	8 °
T	1.30±0.1
U	3-1.00±0.1
V	1.30±0.1

① DC INPUT (V_{IN})
② DC OUTPUT (V_O)
③ GND
④ ON/OFF CONTROL

TO-220IS-4

LINE UP

ITEM	OUTPUT VOLTAGE (Typ.)	UNIT
KIA278R05PI	5	V
KIA278R06PI	6	
KIA278R08PI	8	
KIA278R09PI	9	
KIA278R10PI	10	
KIA278R12PI	12	
* KIA278R15PI	15	

* Note) * : Under Development.

MAXIMUM RATING (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT	Remark
Input Voltage	V_{IN}	35	V	-
ON/OFF Control Voltage	V_C	35	V	-
Output Current	I_O	2	A	-
Power Dissipation 1	P_{d1}	1.5	W	No heatsink
Power Dissipation 2	P_{d2}	15	W	with heatsink
Junction Temperature	T_j	125	℃	-
Operating Temperature	T_{opr}	-20～80	℃	-
Storage Temperature	T_{stg}	-30～125	℃	-
Soldering Temperature (10sec)	T_{sol}	260	℃	-

KEC

SEMICONDUCTOR
TECHNICAL DATA

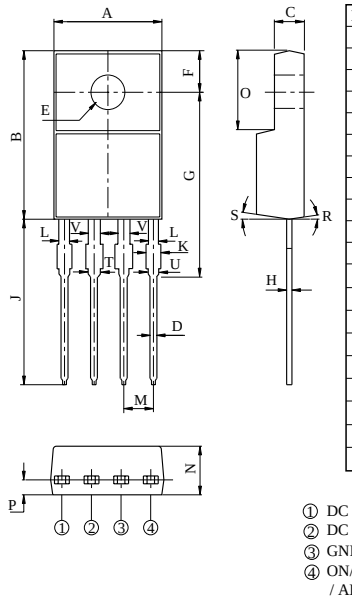
KIA78R000F/PI~ KIA78R050F/PI
BIPOLAR LINEAR INTEGRATED CIRCUIT

4 ,5 TERMINAL LOW DROP VOLTAGE REGULATOR
[Low Quiescent Current-Type]

The KIA78R × × ×F/PI Series are Low Dropout Voltage Regulator suitable for various electronic equipments.
The Regulator has multi function such as over current protection, overheat protection.

FEATURES

· 1.0A Output Low Drop Voltage Regulator.
· Built in ON/OFF Control Terminal. (Active High)
· Built in Over Current Protection, Over Heat Protection Function.
· Low Quiescent Current (Output OFF mode) : 0.5㎂(Typ.)
· Low Standby Current : 800㎂(Typ.)



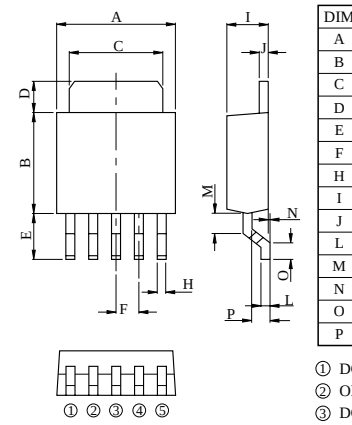
DIM	MILLIMETERS
A	10.00±0.20
B	15.00±0.20
C	2.70±0.20
D	0.60±0.10
E	Φ3.20±0.20
F	3.50±0.10
G	15.70±0.20
H	0.40±0.10
J	14.3+0.2/-0.1
K	1.45±0.10
L	1.00±0.10
M	2.54
N	4.50±0.20
O	7.5±0.1
P	1.50±0.10
R	5°
S	8°
T	1.30±0.1
U	3-1.00±0.1
V	1.30±0.1

① DC INPUT (V_{IN})
② DC OUTPUT (V_O)
③ GND
④ ON/OFF CONTROL (V_C) / ADJUSTABLE

TO-220IS-4

LINE UP

ITEM	OUTPUT VOLTAGE (V)	PACKAGE
KIA78R000F/PI	Adjustable (1.25~15V)	F : DPAK-5 PI : TO-220IS-4
KIA78R015F/PI	1.5	
KIA78R018F/PI	1.8	
KIA78R020F/PI	2.0	
KIA78R025F/PI	2.5	
KIA78R030F/PI	3.0	
KIA78R033F/PI	3.3	
KIA78R050F/PI	5.0	



DIM	MILLIMETERS
A	6.6±0.2
B	6.1±0.2
C	5.0±0.2
D	1.10±0.2
E	2.70±0.2
F	1.27±0.1
H	0.5+0.2/-0.1
I	2.30±0.2
J	0.5±0.1
L	0.50±0.1
M	0.8±0.2
N	0 ~0.25
O	0.7MIN
P	1.00±0.1

① DC INPUT (V_{IN})
② ON/OFF CONTROL (V_C)
③ DC OUTPUT (V_O)
④ N.C / ADJUSTABLE
⑤ GND

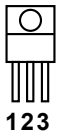
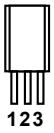
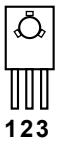
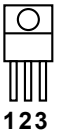
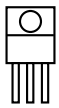
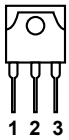
Heat Sink is common to ⑤(GND)

DPAK-5

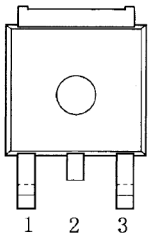
MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage		V_{IN}	16	V
ON/OFF Control Voltage		V_C	16	V
Output Current		I_{OUT}	1	A
Power Dissipation 1 (No heatsink)	F	P_{D1}	1.3	W
	PI		1.5	
Power Dissipation 2 (Without heatsink)	F	P_{D2}	13	W
	PI		15	
Junction Temperature		T_j	150	℃
Operating Temperature		T_{opr}	-20～80	℃
Storage Temperature		T_{stg}	-30～150	℃
Soldering Temperature		T_{sol}	260	℃

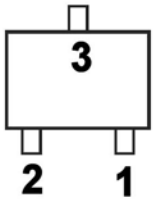
TRANSISTOR, REGULATOR IC BLOCK DIAGRAM

TO-92M  123 1. Emitter 2. Collector 3. Base KTC2874B KSC2785Y KRA107M KRC107M KRA104MT KRC104M KTA1267 KTC 1027	TO-92  123 1. Emitter 2. Collector 3. Base KTD1302T KTA1268GR KTC3200GR KTC3198Y KTA1271Y KSA1175YT KTC 3199 KTA1266YT 2SC2240BL KRC102M	TO-220  123 1. GND 2. INPUT 3. OUTPUT MCNJM7905 MC7915C NJM7908 L7905 KIA 7908 L7915 KIA 7905 KIA7915	TO-92L  123 1. Emitter 2. Collector 3. Base KTA1024Y KSC2316Y
TO-126  123 1. Emitter 2. Collector 3. Base KTD600KG KTA 1360 KTC 3423	TO-92  123 1. Emitter 2. Base 3. Collector KSA733CYT	TO-220  123 1. INPUT 2. GND 3. OUTPUT KIA 7809 KIA7815 MC7815C MC7805C MC7809 L7805 NJM7824 L7815 L7812 KIA 7808 L7808 KIA7812	TO-3P  1 2 3 1. Base 2. Collector 3. Emitter 2SB1560 2SC3423O 2SD2390 2SB1559 2SA1360 2SD2389 2SB1647 2SD2560

NJM2391DL1-25 NJM2391DL1-33
LOW DROPOUT VOLTAGE REGULATOR



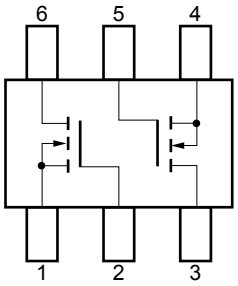
PIN FUNCTION
1. IN
2. GND
3. OUT



1) Emitter
2) Base
3) Collector

KRA 107S
KRC102S
KRA102S
KRC103S
KRC107S
KRC111S
KRC1114S

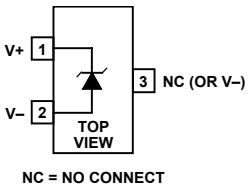
N-CHANNEL MOS FET ARRAY
μPA672T



1. Source 1 (S1)
2. Gate 1 (G1)
3. Drain 2 (D2)
4. Source 2 (S2)
5. Gate 2 (G2)
6. Drain 1 (D1)

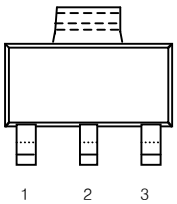
Marking: MA

PIN CONFIGURATION
SOT-23 Package
AD1580



NC = NO CONNECT

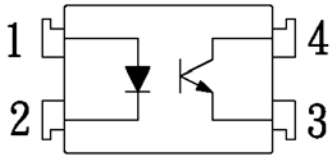
SOT–223 PKG (FRONT VIEW)



LM1117
REGULATOR

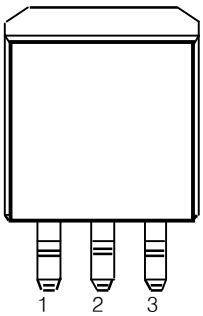
PIN FUNCTION
1. Adj/Gnd
2. Vout
3. Vin

KP1010 photocoupler



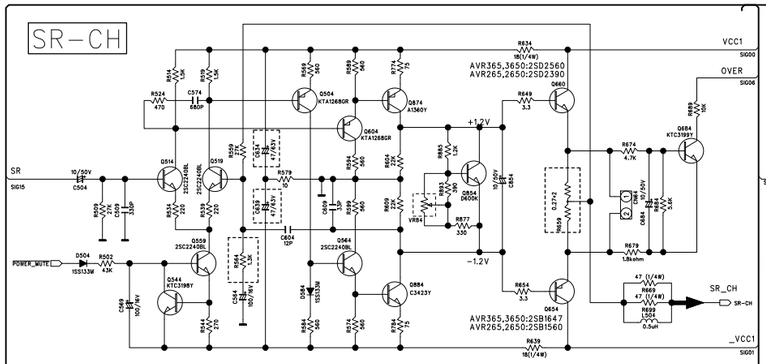
1. Anode
2. Cathode
3. Emitter
4. Collector

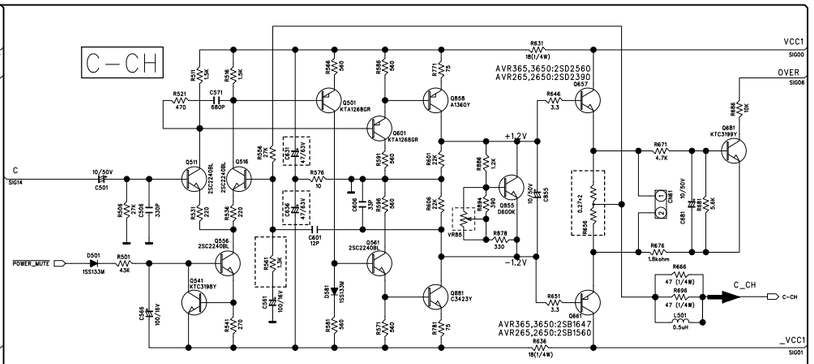
TO–263 (D2 PKG, FRONT VIEW)

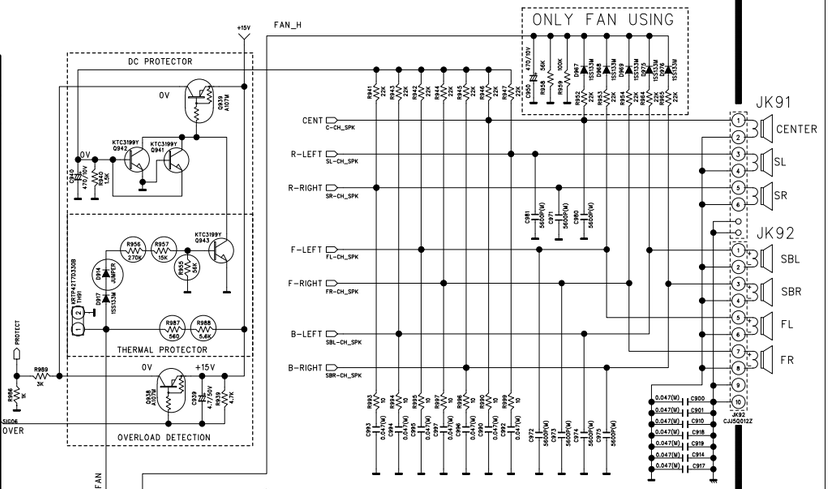


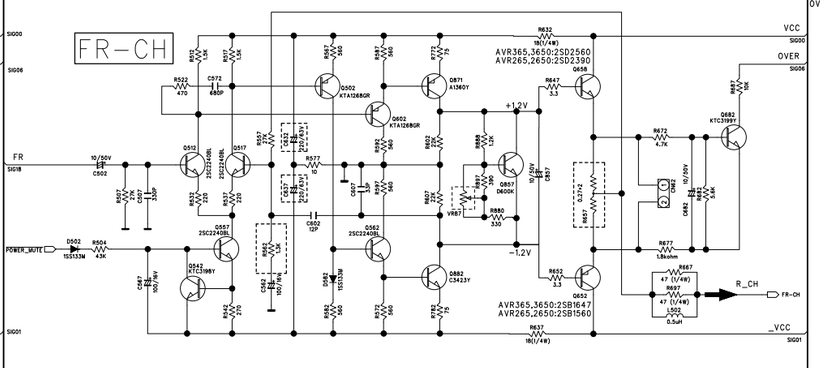
PIN FUNCTION
1. Adj/Gnd
2. Vout
3. Vin

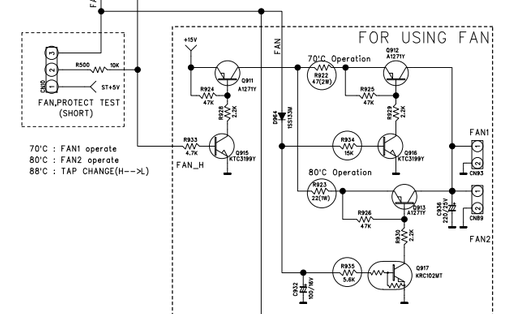
AVR265/365 AMP Schematic Diagram

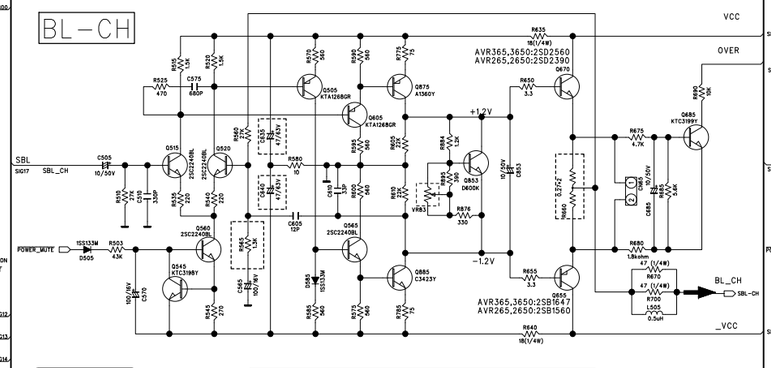


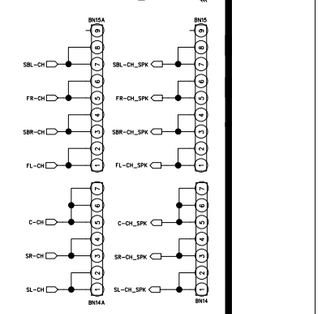


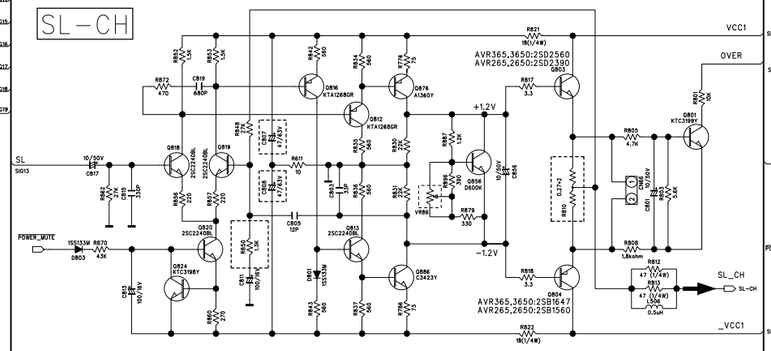


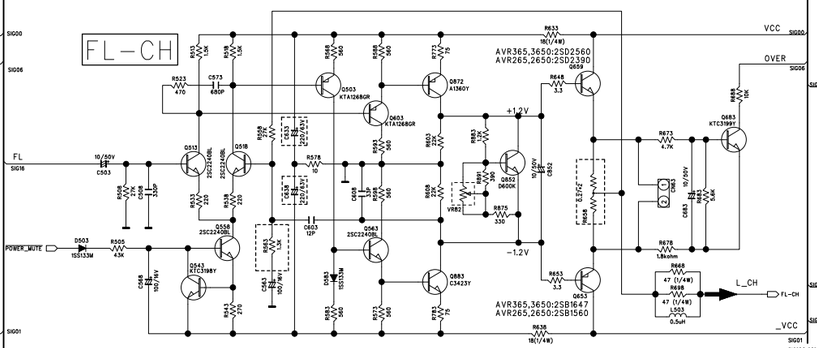


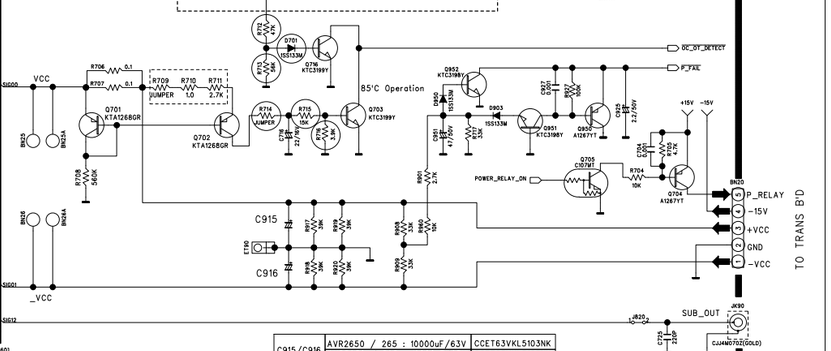


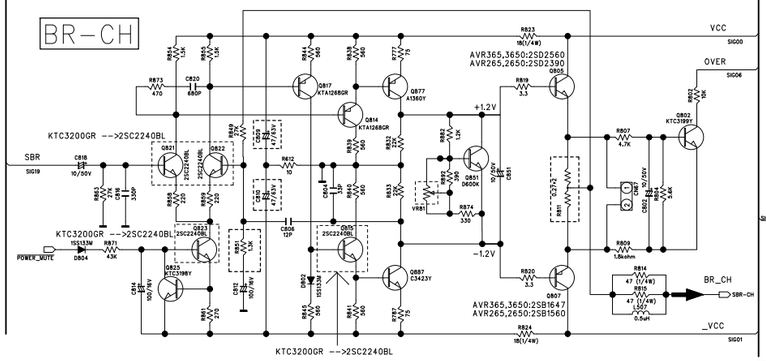








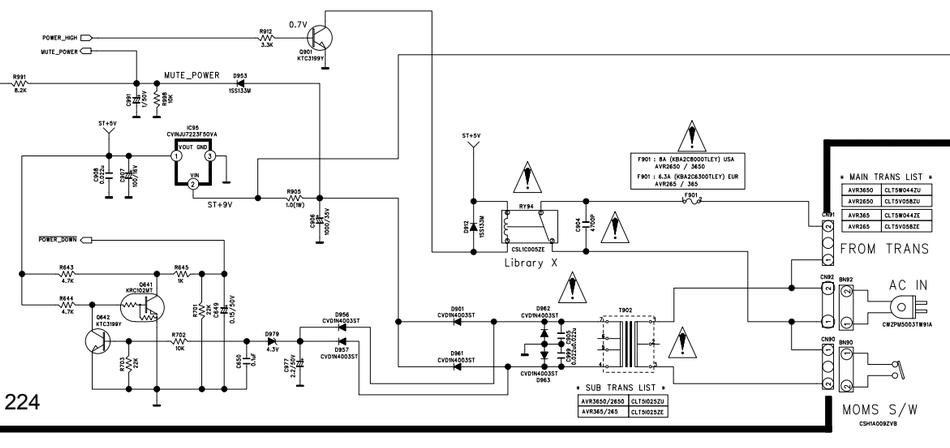




GAIN	R561, R562, R563, R564, R565, R850, R851
AVR265/2650	1.3K
AVR365/3650	1.3K

JW90,JW91 : ALL MODELS

C915/C916		
AVR2650 / 265 : 10000uF/63V	CCET63VKL5103NK
AVR3650 / 365 : 12000uF/63V	CCET63VKL5123NK



AVR 2650

harman/kardon

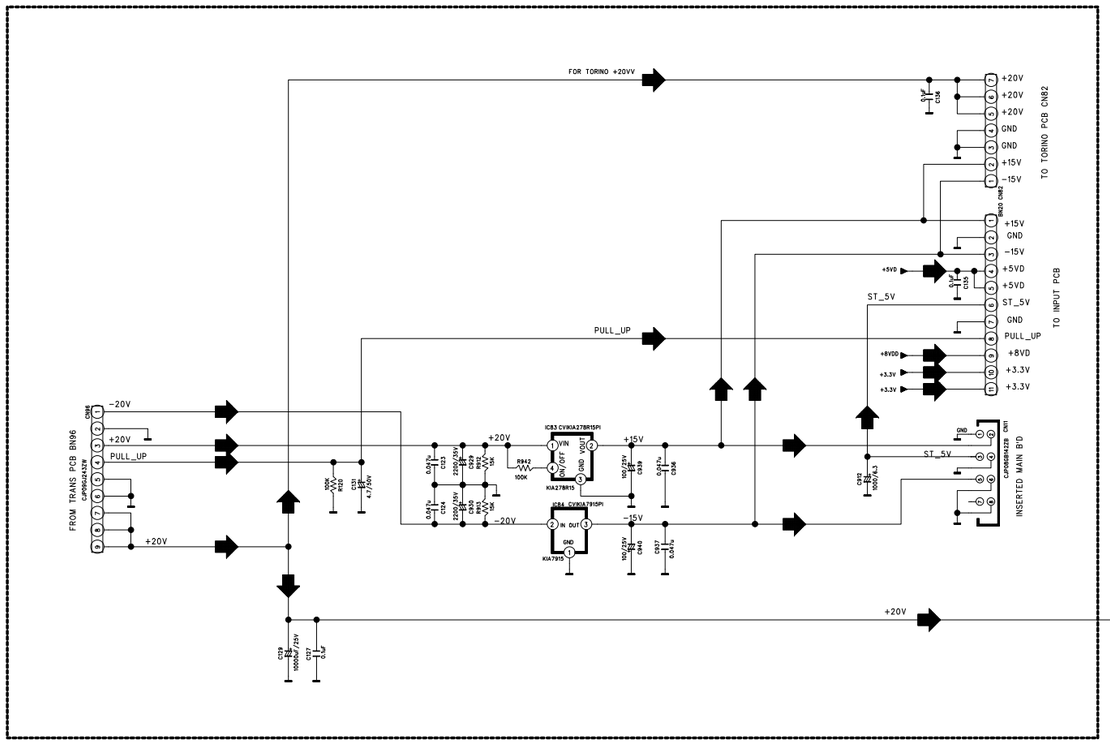
- ** IMPORTANT SAFETY NOTICE.
  INPORTANT FOR SAFETY WHEN REPLACING ANY OF THESE COMPONENTS USE ONLY MANUFACTURE'S SPECIFIED PARTS.
- ** THE UNIT OF RESISTANCE IS OHM.
  K=1000 OHM, M=1000 KOHM.
- ** THE UNIT OF CAPACITANCE IS MICROFARAD (uF)
  pF = 10 ^ uF
- ** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WIHE THE IMPROVEMENT OF PERFORMANCE

ISSUE 2011.05.17

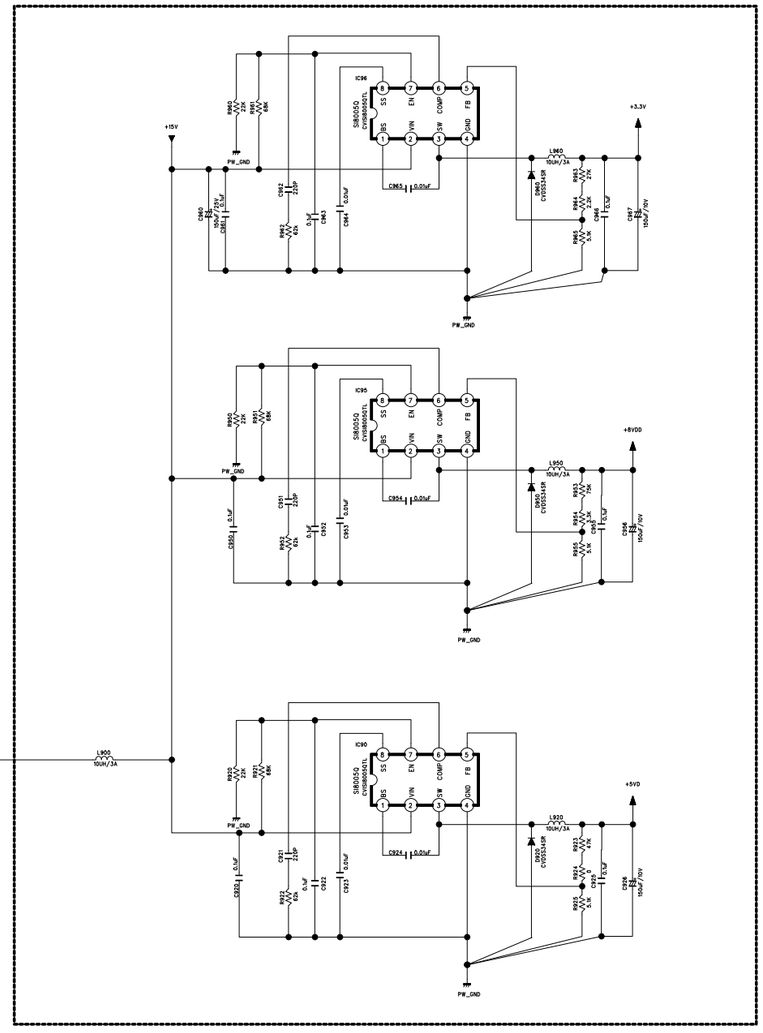
MP

REVISION	1	2	3	SHEET
SCHEMATIC DIAGRAM				
MODEL	AVR CORE			2 / 7
DESIGN	CHECK	APPROVE	DRAWING NO	
W.J.JUNG	W.Y.YANG	H.S.SEOL	12364SCMZ (AMP)	1/1
2011.05.17	2011.05.17	2011.05.17		

< Analog Regulator Part >



< DC-DC Regulator Part >

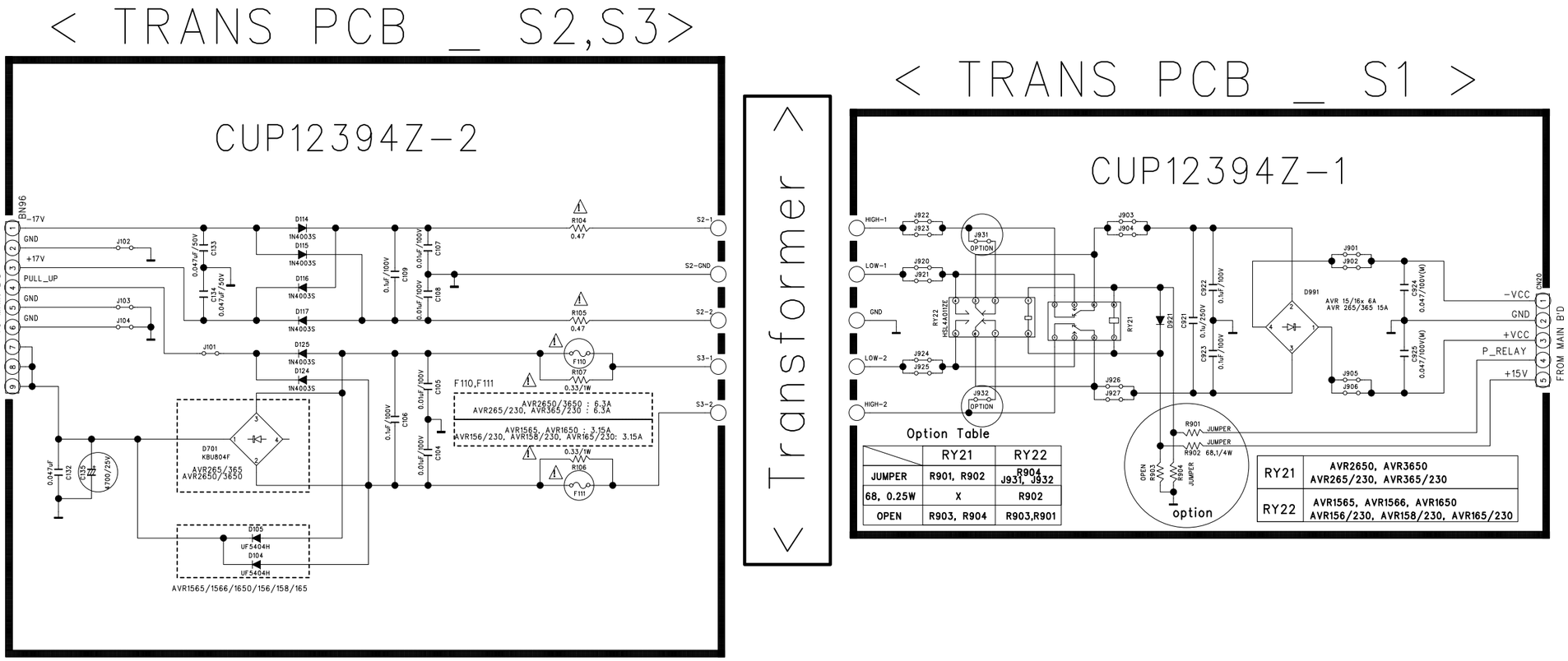


MP

ISSUE
2011.05.17

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR 2650/3650		1/1
DESIGN	CHECK	APPROVE	DRAWING NO
K.B.C	Y.Y.W	K.S.W	CUP12365Z (REG& DC-DC)
2011.05.17	2011.05.17	2011.05.17	1/1



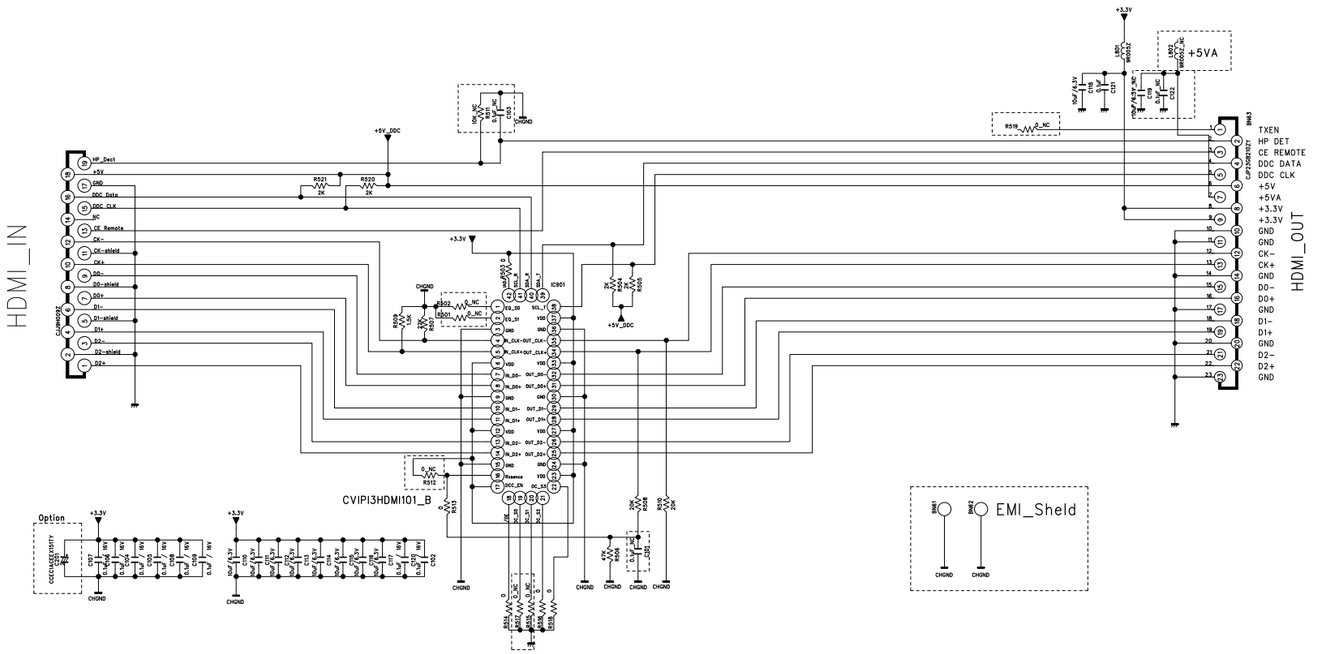
MP

ISSUE
2011.05.17

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM SHEET

MODEL	AVR 165/265/365	1/3
DESIGN	CHECK	APPROVE	DRAWING NO
K.B.C	K.M.S	Y.K.Y	CUP12394Z (POWER) 1/1
11.05.17	11.05.17	11.05.17	



**IMPORTANT SAFETY NOTICE.
COMPONENTS IDENTIFIED BY▲ MARK HAVE SPECIAL CHARACTERISTICS.
IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS.
USE ONLY MANUFACTUREY'S SPECIFIED PARTS.
**THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM
**THE UNIT OF CAPACITANCE IS MICROFARAD (uF)
pF=10^6 uF
**THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WITH THE
IMPROVEMENT OF PERFORMANCE

ISSUE
1
2010.05.17

MP

REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR356x_Front HDMI		1 / 1
DESIGN	CHECK	APPROVE	DRAWING NO
S. KIM	W.Y.YANG	G.S.WEY	HDMI
11.05.17	11.05.17	11.05.17	1 / 1

ZONE2 OUT

AV

SAT

BD

VCR

PVR

CD

iPod & SIRIUS OPT.

R2A15218FP
(8CH E.VOLUME
11 INPUT SELECTOR)

IC101

TO MAIN B'D

WIF10.3

ADC INPUT

TUNER MODULE

8CH DIRECT INPUT B'D

FROM POWER B'D

ZONE2 VOLUME

IC131
CVIBD3812F

** IMPORTANT SAFETY NOTICS.
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS.
IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS
USE ONLY MANUFACTURER'S SPECIFIED PARTS.
** THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM , M=1000 KOHM
** THE UNIT OF CAPACITANCE IS MICROFARAD. (uF)
pF=10^{-6} uF
** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WITH THE
IMPROVEMENT OF PERFORMANCE.

M/P

ISSUE
2011.05.17

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM — SHEET 1/4

MODEL: AVR CORE

DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2327SCMZ (INPUT) 1/1
11.05.17	11.05.17	11.05.17	

AVR 2650

harman/kardon

CUP12327*

*VHC151 OPTION

SELECT INPUT		A	B	C
OPT1 AV	D0	L	L	L
OPT2 SAT	D1	H	L	L
	D2	L	H	L
AUX F_OPT	D3	H	H	L
HDMI_SPDIF	D4	L	L	H
ARC_SPDIF	D5	H	L	H
VENICE_SPDIF	D6	L	H	H
VHC153	D7	H	H	H

*VHC153 OPTION

SELECT INPUT		A	B	G
VCR	COAX2	C3	H	H	L
BD	COAX1	C2	L	H	L
CD	COAX4	C1	H	L	L
PVR	COAX3	C0	L	L	L

HDMI SPDIF MODE : DIR MASTER
HDMI I2S MODE : HDMI MASTER
ADC MODE : DSP MASTER
DIR MODE : DIR MASTER

Do not use

*OPTION : EMC COUNTERMEASUER

<=> HDMI BOARD

HDMI_SPDIF	M1	GND
ARC_SPDIF	M2	HDMI_SPDIF
	M3	ARC_SPDIF
	M4	HDMI_SDATA0
	M5	HDMI_SDATA1
	M6	HDMI_SDATA2
	M7	HDMI_SDATA3
	M8	HDMI_LRCK
	M9	GND
	M10	HDMI_SCK
	M11	HDMI_MCLK
	M12	DSP_SPDIF
	M13	DSP_MCLK
	M14	DSP_DATA0
	M15	DSP_LRCK
	M16	DSP_SCLK
	M17	GND

M/P

ISSUE 2011.05.17

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 2/4

MODEL	AVR CORE	
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2327SCMZ (DSP) 1/1
11.05.17	11.05.17	11.05.17	

CUP12327*

AVR 2650

harman/kardon

FROM HDMI PCB

TO RS232 PCB

FOR SIRIUS

FROM FRONT PCB

IC151 T5CN5

FOR DEBUG

IC155

IC152 CVIW24C32WN6TP

IC104 M333FWFG

IC156 CWIC3201G-33

IC158

PULL_UP

GPIO : Input/Out Port(without pull_up resistor)

REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM — SHEET 3/4

MODEL	AVR CORE	
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2327SCMZ (CPU)
11.05.17	11.05.17	11.05.17	1/1

M/P

ISSUE 2011.05.17

VENICE 6.2 MODULE

to VENICE 6.2

1	DAB+1.2V
2	DAB+3.3V
3	GND
4	GND
9	VENICE_RX
10	VENICE_TX
11	USB_DM
12	USB_DP
13	GND
14	USB_VBUS
15	USB_VBUS_FAULT
16	USB_VBUS_DRIVE
26	SPI_CS
27	SPI_MISO
28	SPI_MOSI
29	SPI_SCLK
30	GND
32	SPDIF_OUT
33	ETHERNET_INT
39	GND
48	GND
61	AGND
62	AGND

CJP64GA2212B

CN62

Don't Use

Q801 A1075

IC1 CVISN74LVC1G125DBVR

IC161 CVWSZ8851SALTR

L803 CLZ9R001Z

L804 CLZ9R001Z

L805 CLZ9R001Z

L715 CLZ9R001Z

JK52

DAB/ETHERNET POWER PARTS

L802 CLZ9R001Z

IC167 78R000F

L806 CLZ9R001Z

L807 CLZ9R001Z

IC165 3.3V

IC166 3.3V

Do not use

IC164 CVWL6XC283PR (2.6V RESET)

IC162 CVITMP92FD28FG

FOR UPDATE(through USB)

USB SELECT	SEL	OE
VENICE_D+/-	L	L
BOLERO_D+/-	H	L

IC168 CVISL54220IUZ-T

JK51

IC166

L601 60

L602 60

Q102 A1075

D103 MVTKR4107S

Q104 C1075

Q105 A1075

Q106 C1075

Q107 C1075

D105 MVTKR4107S

FOR UPDATE(Bolero)

Update: LOW

REVISION							
1		2		3		4	
5		6		7			

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR CORE		4 / 4
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2327SCMZ (VENICE_USB) 1 / 1
11.05.17	11.05.17	11.05.17	

M/P

ISSUE 2011.05.17

CUP12328Z

AVR 2650

harman/kardon

ADV3014 Decoupling Capacitor

ADV7844 Worst Measured Currents

1.8V Total : 904.33mA

3.3V Total : 240.3mA

#12: Added Pull-down 500 ohm

R857 : Front HDMI don`t used

IC901

CVIADV3014BSTZ

M/P

232

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR CORE		1 / 4
DESIGN	CHECK	APPROVE	DRAWING NO
S.K	W.Y.YANG	G.S.WEY	HDMI INPUT
11.05.17	11.05.17	11.05.17	1 / 1

ISSUE 11.05.17

CUP12328Z

11.05.17

ADV7844 Worst Measured Currents

1.8V Total : 1340mA(20%: 1608mA
2.5V Total : 100mA(20%: 120mA)
3.3V Total : 450mA(20%: 540mA)

ADV7844

HDMI Processor & ADC & Decoder

SD to I/P Converter

In case of PCM	
I2S0	FL/FR
I2S1	SUB/CEN
I2S2	SL/SR
I2S3	SBL/SBR

I2S HDMI RX to DSP

M/P

ISSUE
ANAM
MULTI. LAB
11.05.17

AVR 2650

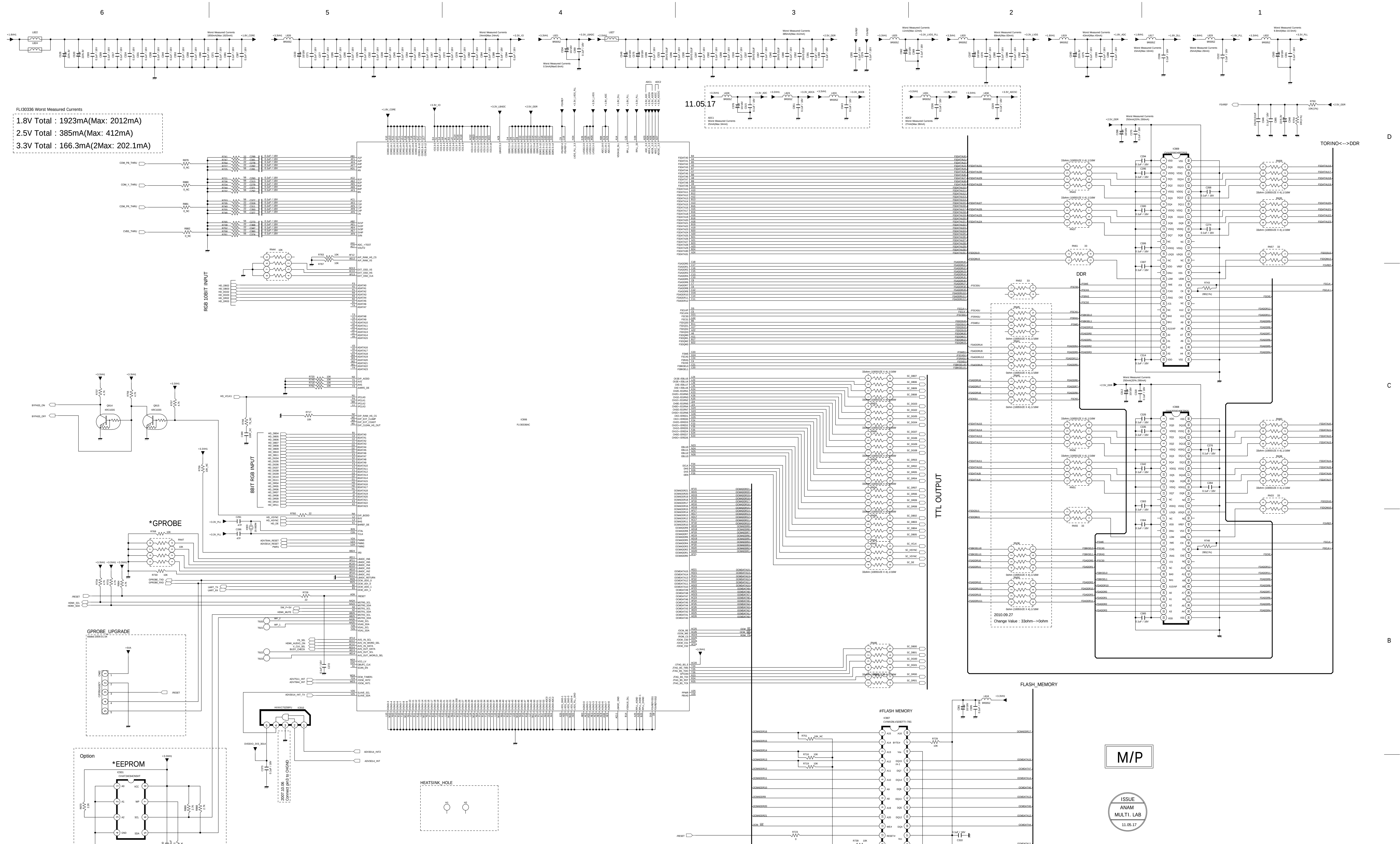
harman/kardon

REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM — SHEET

MODEL: AVR CORE — 1 / 4

DESIGN	CHECK	APPROVE	DRAWING NO
S.K	W.Y.YANG	G.S.WEY	HDMI RX & Decoder 1 1
11.05.17	11.05.17	11.05.17	



AVR 2650

harman/kardon

CUP12328Z

234

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR CORE		1 / 4
DESIGN	CHECK	APPROVE	DRAWING NO
S.K	W.Y.YANG	G.S.WEY	SCALER
11.05.17	11.05.17	11.05.17	1 / 1

CUP12328Z

11.05.17

HDMI By Pass Mode Interface

INPUT			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Scaling Mode Interface

Analog Video Option

AVR 2650

harman/kardon

M/P

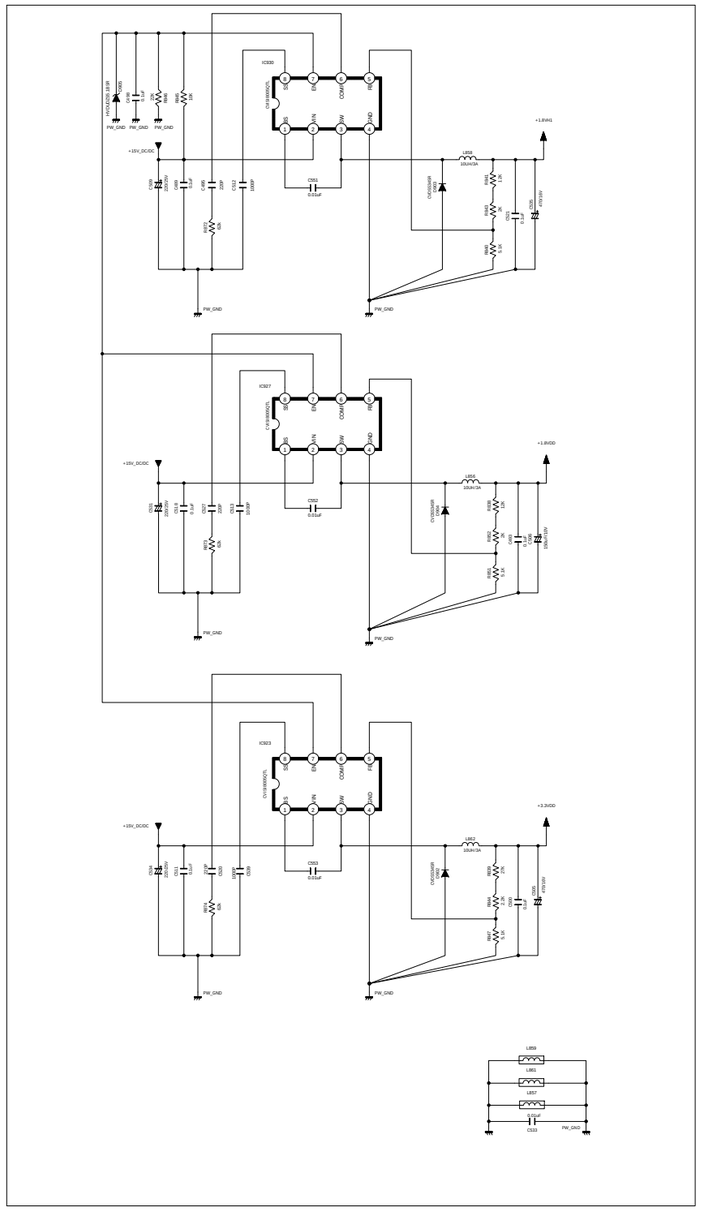
REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM — SHEET

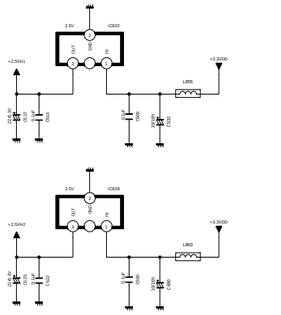
MODEL	AVR CORE		1 / 4
DESIGN	CHECK	APPROVE	DRAWING NO
S.K	W.Y.YANG	G.S.WEY	HDMI TX & Encoder 1 / 1
11.05.17	11.05.17	11.05.17	

ISSUE
ANAM
MULTI. LAB
11.05.17

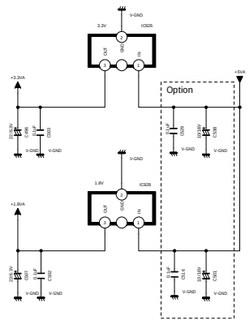
DC/DC REGUALTOR



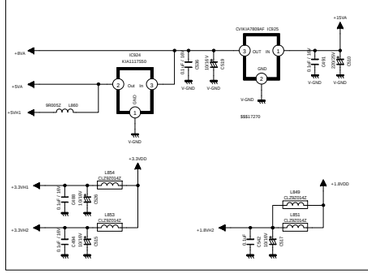
DDRMEM_REG_ 2.5V



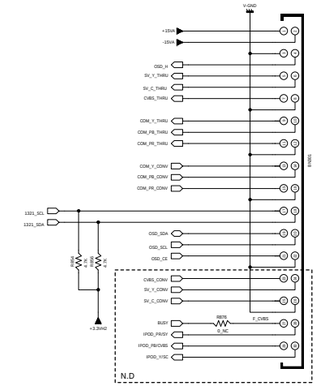
ADC_REG_ 1.8/3.3V



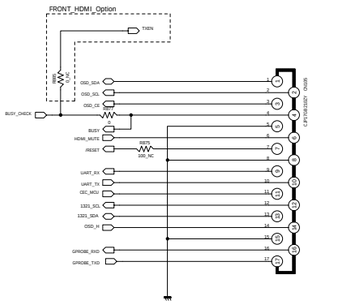
SCALER&Analog_REG



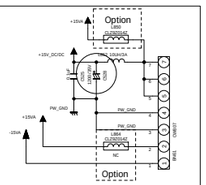
TO VIDEO



TO INPUT



TO POWER



M/P

ISSUE
ANAM
MULTI. LAB
11.05.17

REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR CORE		1 / 4
DESIGN	CHECK	APPROVE	DRAWING NO
S.K	W.Y.YANG	G.S.WEY	POWER&CONNECTOR 1 / 1
11.05.17	11.05.17	11.05.17	

CUP12357Z

CUP12357-1 FIP PCB

CN73

CUP12357-2
[STAND BY PCB]

BN73

FROM INPUT ASS'Y(CPU)

CN72

BASIC MODEL DON'T USE THIS CIRCUIT

R937,R938 ARE USED FOR BASIC MODEL

TO VR JACK PCB

BN74

CN74

FROM FIP PCB

CUP12357-3 [VOLUME PCB]

* OPTION *

* ESD *

JW17

JW18

OPTIONS ARE USED FOR BASIC MODEL & 265/2650

R122 IS USED FOR AVR165/365

REMOCON SENSOR

SN74ACT04DR (HEX INVERTER)

FIP1 CFL1625D19GNK FOR AVR165/BASIC MODEL

FIP2 CFL1628D01GNK FOR AVR265/365

Source_up (AVR1650 & BASIC)
Source List (AVR2650/3650)
Source_down
Up
Surr_Sel_up
Down
Surr_Sel_down
OK
Surr_Mode
Right(=>)
Tuning_up
Left(<=)
Tuning_down
Back/Exit

Right (=>) (AVR1650 & BASIC MODEL)
Surround Modes (AVR2650/3650)
Set
Video Modes
Left (<=)
Audio Effects
Digital
Resolution
Channel
Info
Tone Mode
AVR

FROM MAIN TRANSFORMER

BN71

BN71 --> CN71 CHANGE

TO HEAD PHONE JACK PCB

FROM FIP PCB

ANGLE

STRAIGHT

CN61

BN61

CUP12357-6 USB JACK PCB

USE AVR2650/3650

JK53

BN53

CUP12357-4 HEAD PHONE JACK PCB

JK63

CUP12357-5 USB & INPUT(ANALOG) JACK PCB

USE AVR1650 / 165 & BASIC MODEL

JK51

BN51

JK52

BN52

TO INPUT PCB ASS'Y(INPUT)

AVR 2650

harman/kardon

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 1/7

MODEL	AVRX65 SERIES	
DESIGN	CHECK	APPROVED	DRAWING NO
J.I.H	K.M.S	Y.Y.W	2357SCMZ (FRONT) 1/1
11.05.17	11.05.17	11.05.17	

MP

ISSUE 2011.05.17

VIDEO MUX PART

* DEFINITION OF I2C REGISTER (NJW1321)

I2C BUS FORMAT

MSB S(1BIT)	LSB	MSB	LSB	MSB	LSB		
SLAVE ADDRESS(8BIT)	A(1BIT)	DATA(8BIT)	A(1BIT)	DATA(8BIT)	A(1BIT)	P(1BIT)	

SLAVE ADDRESS

MSB			Slave Address(6BIT)			MSB	Hex
1	0	0	0	0	0	ADR(1BIT) R/NOT W(1BIT)	-

CONTROL REGISTER TABLE

<WRITE MODE>

NO.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
DATA 1	PS1	PS2		OUT1			OUT2	
DATA 2	Aux0		AUX1			Aux2		AUX3

<READ MODE>

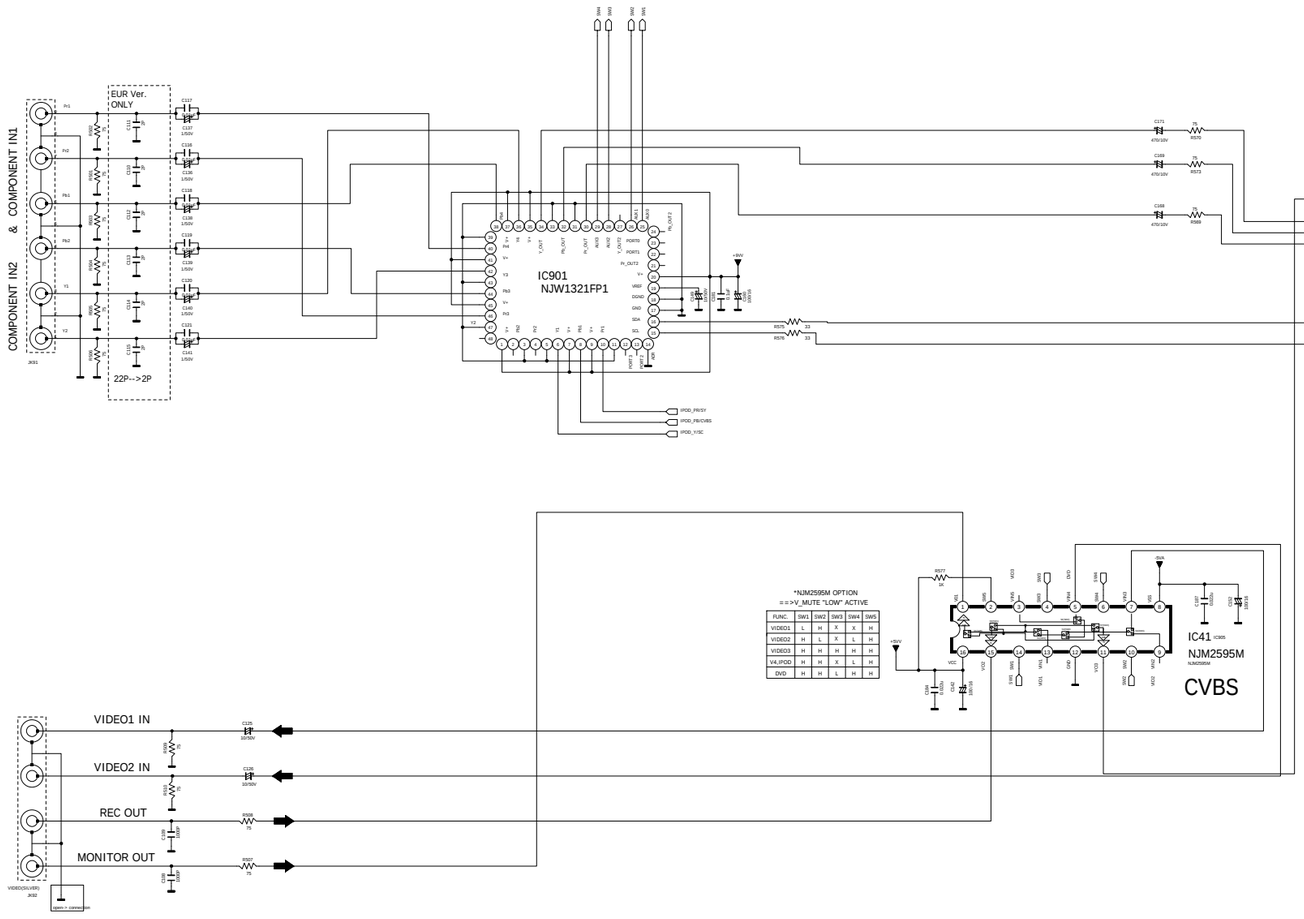
NO.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
DATA	PORT0		PORT1			PORT2		PORT3

S : Starting Term
A : Acknowledge Bit
P : Ending Term

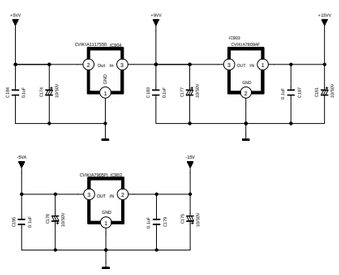
R/NOT W : Set the Write Mode or Read Mode.
ADR : Set the Slave Address by " ADR" terminal.
R/NOT W = 0 : WRITE MODE, ADR = 0/1 ; ADR=0 Hex 84(h), ADR=1 Hex 86(h)
R/NOT W = 0 : READ MODE, ADR = 0/1 ; ADR=0 Hex 85(h), ADR=1 Hex 87(H)

PS : POWER SAVE
=> PS = 1 ; POWER SAVE ON (MUTE), PS = 0 ; POWER SAVE OFF (OUT ON)
OUT : OUTPUT
AUX : AUXILIARY (CONTROL SIGNAL OUTPUT)

PORT : INPUT



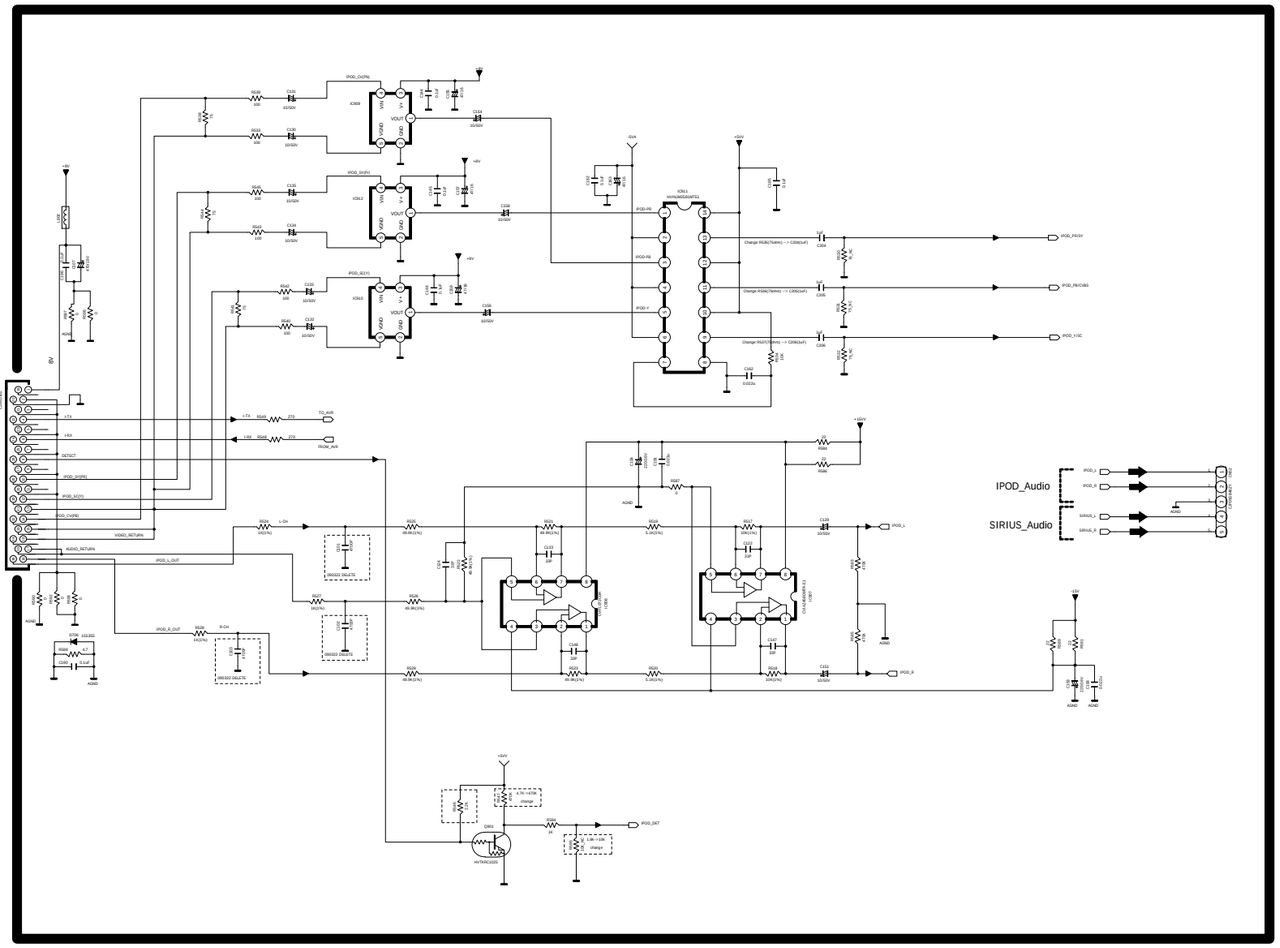
FUNC.	SW1	SW2	SW3	SW4	SW5
VIDEO1	L	H	X	X	H
VIDEO2	H	L	X	L	H
VIDEO3	H	H	H	H	H
V4_IPOD	H	H	X	L	H
DVD	H	H	L	H	H



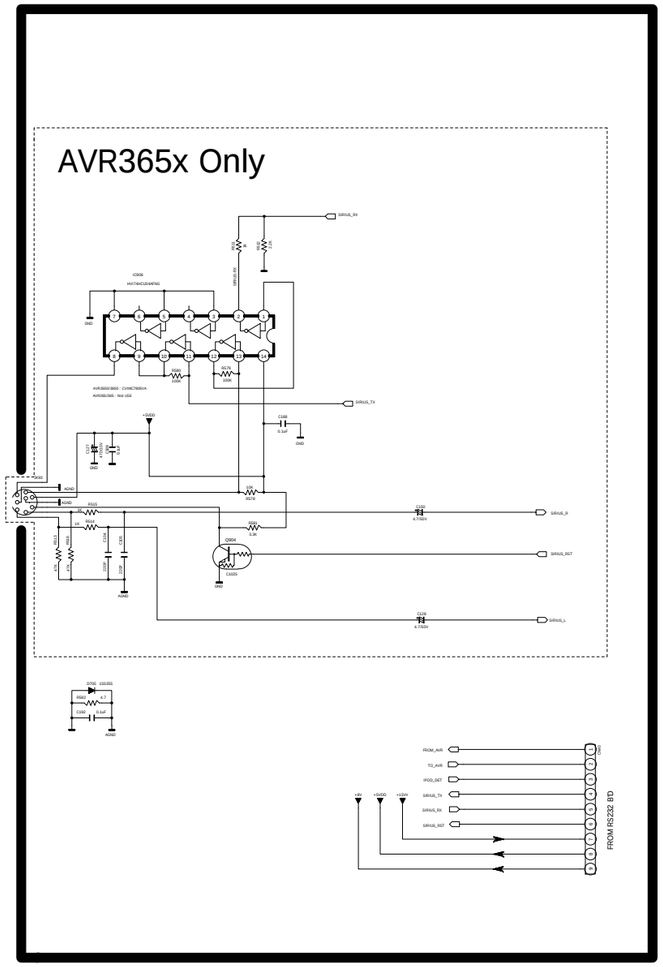
REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM				SHEET
MODEL	AVR CORE			1 / 3
DESIGN	CHECK	APPROVE	DRAWING NO	
S.K	W.Y.YANG	G.S.WEY	12361SEMZ (VIDEO)	1 / 1
11.05.17	11.05.17	11.05.17		

I-POD PART



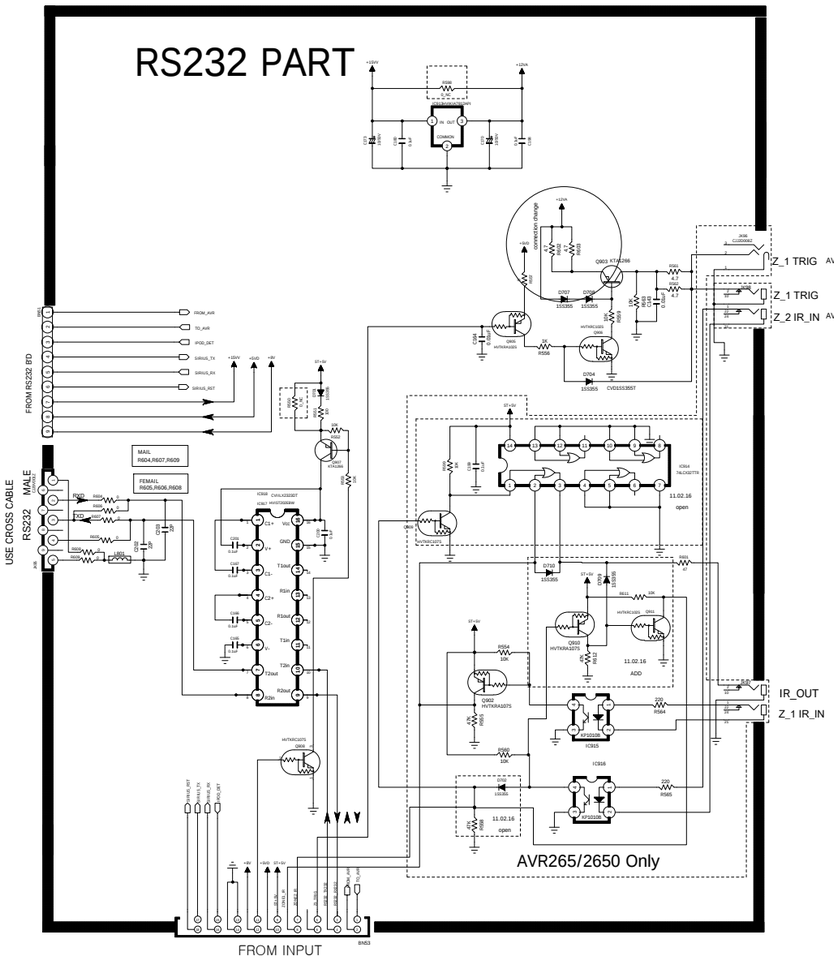
SIRIUS PART



REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM			SHEET
MODEL	ARV CORE		2 / 3
DESIGN	CHECK	APPROVE	DRAWING NO
S.K	W.Y.YANG	G.S.WEY	12361SEMZ
11.05.17	11.05.17	11.05.17	(IPOD&SIRIUS) 1 / 1

(IPOD&SIRIUS)



REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM			SHEET
MODEL	ARV CORE		3 / 3
DESIGN	CHECK	APPROVE	DRAWING NO
S.K	W.Y.YANG	G.S.WEY	12361SEMZ (RS232) 1 / 1
11.05.17	11.05.17	11.05.17	

AVR 2650

harman/kardon

POWER1

P_FAIL

CN20

5P WIRE

S1

MAIN TRANS

5P WIRE

POWER2

D15V

P_UP

-20

+20

BN96

HDMI

CN61

+15V/DC15V

-15V

CN105

CN104

BN301

30P

CN301

VIDEO

+9V +8V

+5V

-5V

+15

-15

IPOD SIRIUS

BN52

CN20

DC15V

+15V

-15V

17 P C/C

17 P C/C

WF105

WF104

BN52

AUDIO

5P WIRE

9P WIRE

DATA

+15V

IPOD SIRIUS

ST5V

+5VD

+15V

RS232

BN20

CN71

18P

BN71

+3.3V

+3.3V

+15V

-15V

+5V

ST5V

P-U

CN20

+12V?

7P WIRE

13P WIRE

MUTE PO

WF103

WF101

CN51

+5V

USB5V

9P WIRE

27P C/C

P-FAIL

S1

AC

BN20

CN91

TRANS

CN1

R904 삭제

AMP

ST5V

-15V

+15V

+5VD

31 P C/C

5P WIRE

BN53

AVR265 USB

11P WIRE

BN14

BN15

FAN

CN93

CN89

CN10

CN90

MOMS

CN92

FAN TEST

AC CORD

7P WIRE

9P WIRE

BN14-1

BN15-1

DCDC

+5V

+3.3_1

+3.3_2

DC15V

8P

CN12

CN96

CN82

+15V

-15V

DC15V

BN20

+15V

ST5V

CN11

8P

CN11

H/P

BN61

6P

CN61

S/T PCB

CN73

6P

BN73

CN71

AC45V VFD AC

FRONT

CN72

BN74

5P WIRE

V/R PCB

CN74

5P WIRE

241

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM — SHEET 1 1

MODEL	AR CORE	
DESIGN	CHECK	APPROVE
K.M.S	L.J.H	Y.W.Y
11.05.17	11.05.17	11.05.17

DRAWING NO: Wiring 1 1