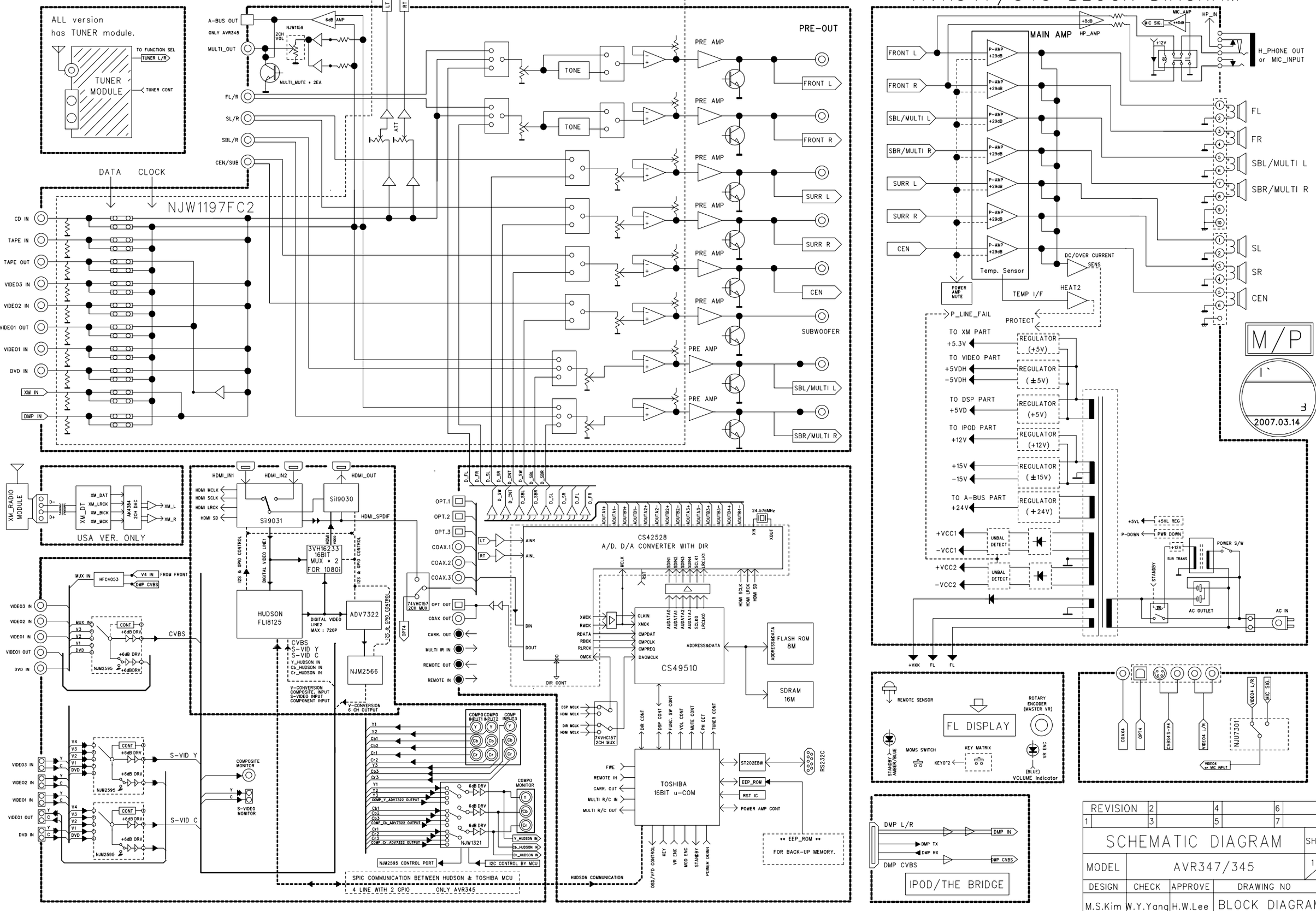
AVR347/345 BLOCK DIAGRAM



M/P

1`

3

2007.03.14

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 1/1

MODEL	AVR347/345	
DESIGN	CHECK	APPROVE	DRAWING NO
M.S.Kim	W.Y.Yang	H.W.Lee	BLOCK DIAGRAM 1190BCDZ 1/1
07.03.14	07.03.14	07.03.14	

CUP11911X

SR-CH

C-CH

BL-CH

FR-CH

SL-CH

FL-CH

BR-CH

EXCEPT AVR145/144/132/146/147

GAIN	R561, R562, R563, R564, R565, R850 R851
AVR145/132/144 AVR146/147	1.8K
AVR245/345 AVR247/347	1.6K

2SD2389P:AVR132/144 /AVR146
2SD2390:AVR145/245 /AVR147/247
2SD2560:AVR345/347
2SB1559P:AVR132/144/146
2SB1560:AVR145/245/AVR147/247
2SB1647:AVR345/347

AVR132/144 OPTION

DC PROTECTOR
THERMAL PROTECTOR
OVERLOAD DETECTION
FOR USING FAN

ONLY FAN USING

JK91 CENTER SL SR
JK92 FL FR SBL SBR
JW92: AVR145/144/132/146/147 ONLY

EXCEPT AVR145/132/144 AVR146/147
ONLY AVR145/132 AVR144/146/147
ONLY AVR146/147 AVR145/132/144

C902 6800/50V (AVR145/132/144/146/147) 8200/50V(AVR245/247) 8200/63V(AVR345/347) C909
C915 6800/50V(AVR145) (AVR145/132/144/146/147) 10000/50V(AVR245/247) 12000/63V(AVR345/347) C916

BN19 VCC GND -VCC
BN20 VCC GND -VCC P_FAIL

AVR345/347 ONLY

JW90,JW91 : ALL MODELS

AVR245/345/247/347 PART
TO REMOTE IN/OUT B'D
FROM TRANS
AC IN
C903 DEL
TO REG B'D
JW93 : AVR145/245/345
JW93 : AVR147/247/347

AVR245/345/247/347 OPTION

FROM INPUT B'D
FROM TRANS B'D

** IMPORTNAT SAFETY NOTICE.
IMPORTANT FOR SAFETY WHEN REPLACING ANY OF THESE COMPONENTS USE ONLY MANUFACTURE'S SPECIFIED PARTS.
** THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM.
** THE UNIT OF CAPACITANCE IS MICROFARAD (uF)
pF = 10^-6 uF
** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WIHE THE IMPROVEMENT OF PERFORMANCE

REVISION	1	2	3	
SCHEMATIC DIAGRAM				SHEET
MODEL	AVR145/245/345/132/144 AVR146/147/247/347			2/7
DESIGN	CHECK	APPROVE	DRAWING NO	
C.B.L	W.Y.Y	H.W.L	1911SCMX (MAIN)	1/1
07.03.14	07.03.14	07.03.14		

TI. LAB 2007.03.14

CUP11915Z

bottom layer is possible.

The patterns of box should be designed as same length.

There are not these parts

impedance layout

PGB0010603 x 8

*option (Do not use these parts)

ISSUE
ANAM
MULTI LAB
2006.02.08

TENTATIVE

* TRANSISTOR *

(KRA102S) : R1, R2 => 10K OHM
(KRA103S) : R1, R2 => 22K OHM
(KRA104S) : R1, R2 => 47K OHM

CRJ104DJ220T

CCEA1CH100T

CLZ9R009Z

M/P

MULTI
2007.03.14

**IMPORTANT SAFETY NOTICE.
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS.
IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS.
USE ONLY MANUFACTUREYS SPECIFIED PARTS.

**THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM

**THE UNIT OF CAPACITANCE IS MICROFARAD (uF)
pF=10-6 uF

**THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME
WITH THE IMPROVEMENT OF PERFORMANCE

REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR345/247/347		6/6
DESIGN	CHECK	APPROVE	DRAWING NO
W.Y.Y	W.Y.Y	H.W.L	1915SCMZ
07.03.14	07.03.14	07.03.14	1/2

CUP11915Z

DO NOT MOVE.

FLI8125 ANALOG INPUT

ADV7322 ANALOG OUTPUT

TO MCU & JANUS

FLI8125BC #8

Blue DATA

Green DATA

Red DATA

Do not USE

SD(13.5MHZ) MODE : LOW
HD(30MHZ) MODE : HIGH
Control by HUDSON

HIGH : OUTPUT ON , LOW : MUTE
THIS PORT IS USED TO MUTE AMALOG OUTPUT OF HDMI TO MEET COPY-PROTECT COMPLIANT.

*Option
Do not Mount.

ADD Connection

Red DATA Input

Green DATA Input

Blue DATA Input

#5: TACT SW WILL BE ADDED BY MANAUL.

*option
Don't use

FROM DOWNLOAD B'd

HDMI CONTROL GPIO

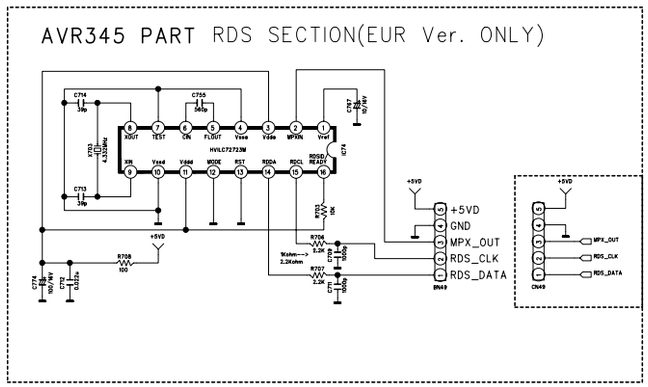
_TI. LAB
2007.01.29

REVISION	2		4		6	
1		3		5		7

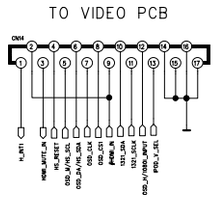
SCHEMATIC DIAGRAM			SHEET
MODEL	AVR345/247/347		6/6
DESIGN	CHECK	APPROVE	DRAWING NO
W.Y.Y	W.Y.Y	H.W.L	1915SCMZ (HUDSON) 2/2
07.03.14	07.03.14	07.03.14	

CUP11913Z

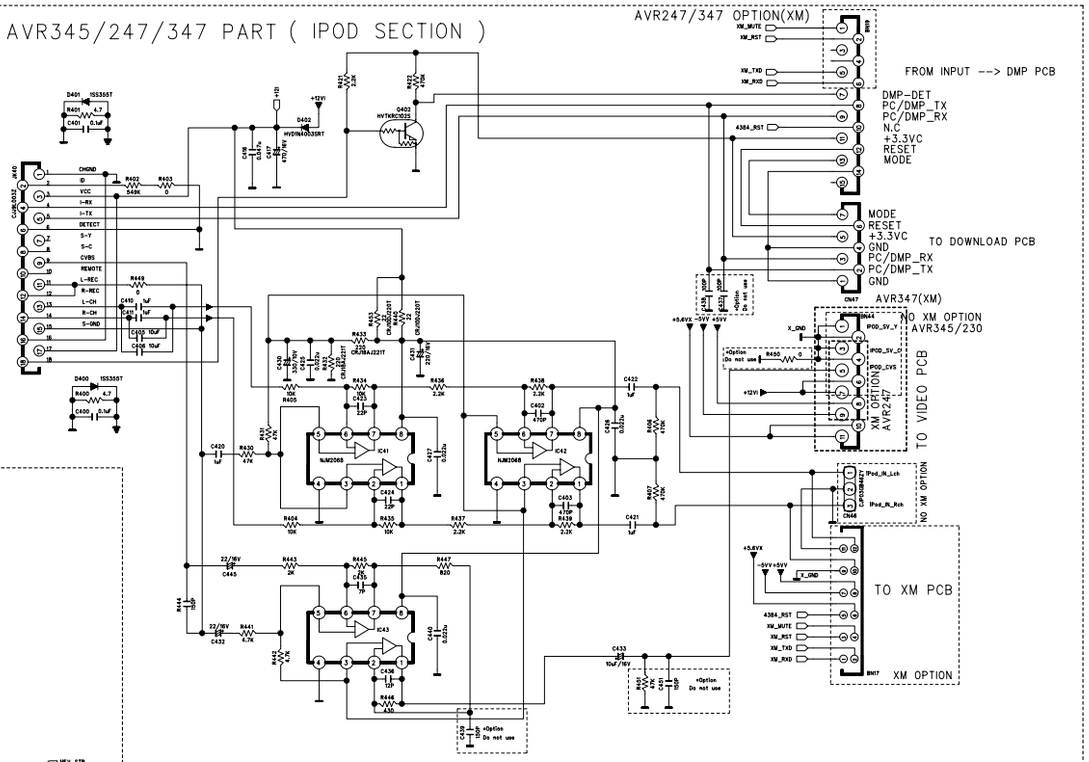
AVR345 PART RDS SECTION(EUR Ver. ONLY)

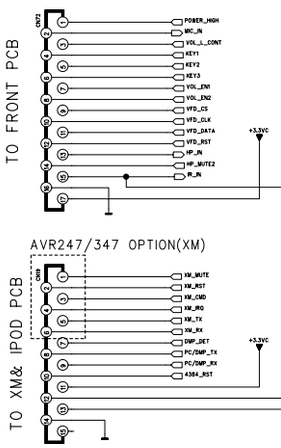


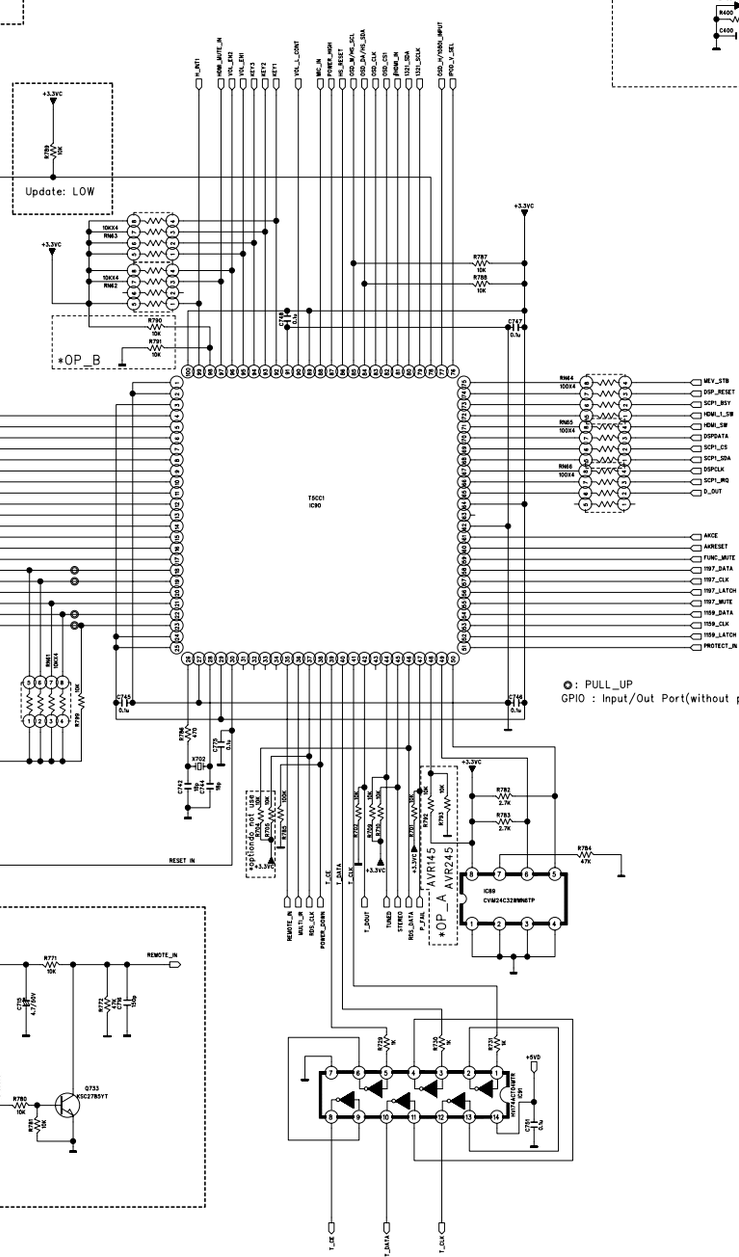
TO VIDEO PCB



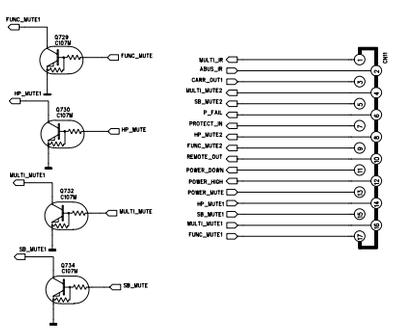
AVR345/247/347 PART (IPOD SECTION)



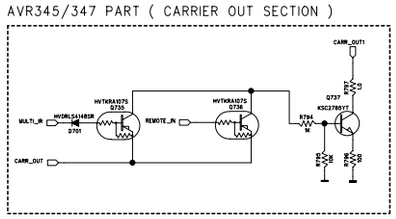


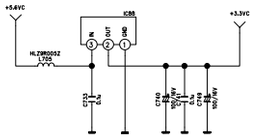


○: PULL_UP
GPIO : Input/Out Port(without pull_up resistor)



AVR345/247/347 PART (CARRIER OUT SECTION)





AVR345/247/347 PART

MODEL OPTION TABLE

MODEL	OP_A(PIN48)	OP_B(PIN98)	OP_C(PIN52)
AVR145, 147	HIGH(R792)	LOW(R791)	LOW(R712)
AVR245	LOW(R793)	LOW(R791)	LOW(R712)
NONE	OPEN	LOW(R791)	NOT OPTION
AVR132	LOW(R793)	HIGH(R790)	LOW(R712)
AVR144, 146	HIGH(R792)	HIGH(R790)	LOW(R712)
AVR145/230	HIGH(R792)	LOW(R791)	HIGH(R711)
AVR245/230	LOW(R793)	LOW(R791)	HIGH(R711)
AVR347	HIGH(R792)	LOW(R791)	NOT OPTION
AVR247	LOW(R793)	LOW(R791)	NOT OPTION
AVR345/230	HIGH(R792)	HIGH(R790)	NOT OPTION

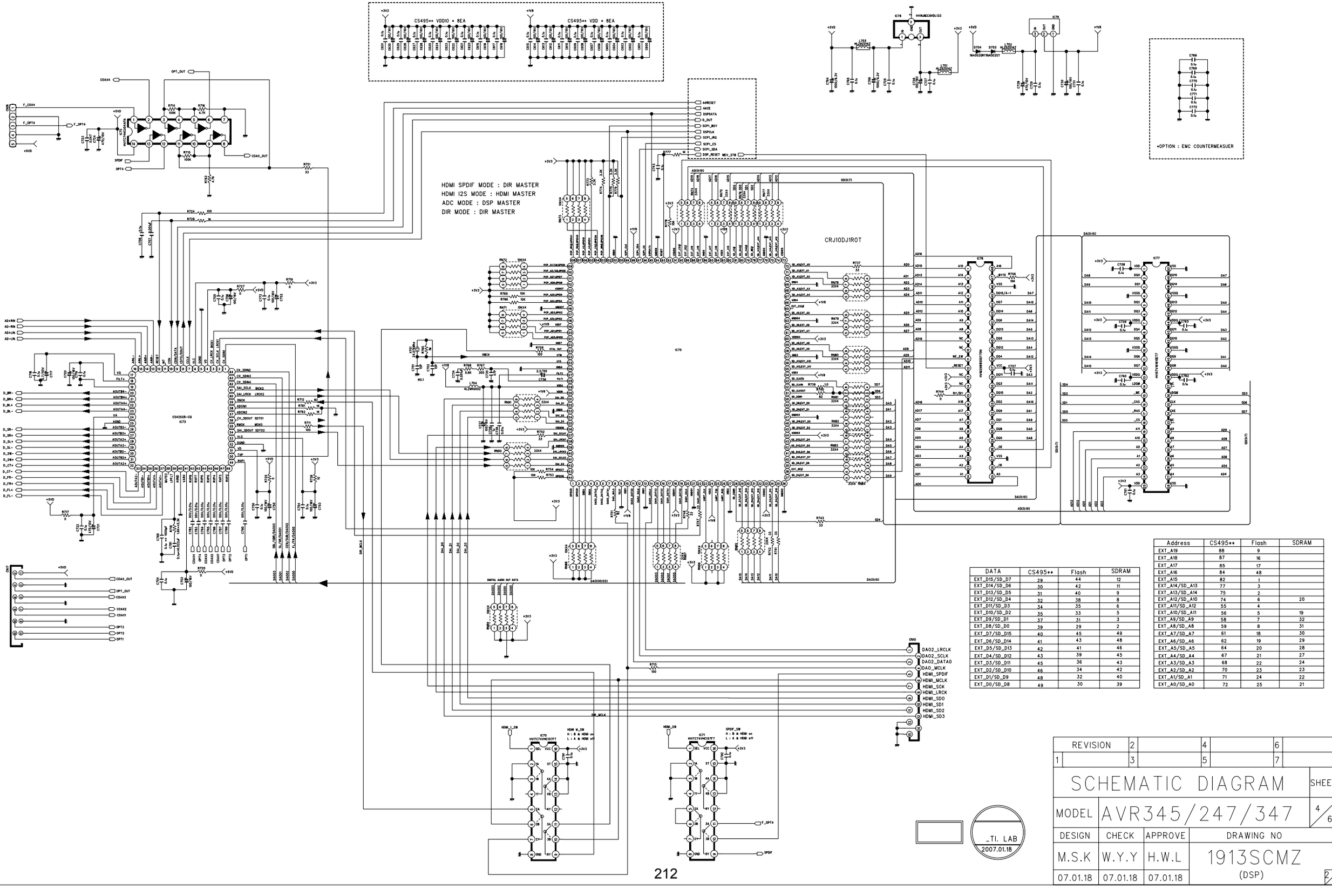
_TI. LAB
2007.01.18

REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM — SHEET 4/6

MODEL	AVR345/247/347	
DESIGN	CHECK	APPROVE	DRAWING NO
M.S.K	W.Y.Y	H.W.L	1913SCMZ (CPU) 3/4
07.01.18	07.01.18	07.01.18	

CUP11913Z



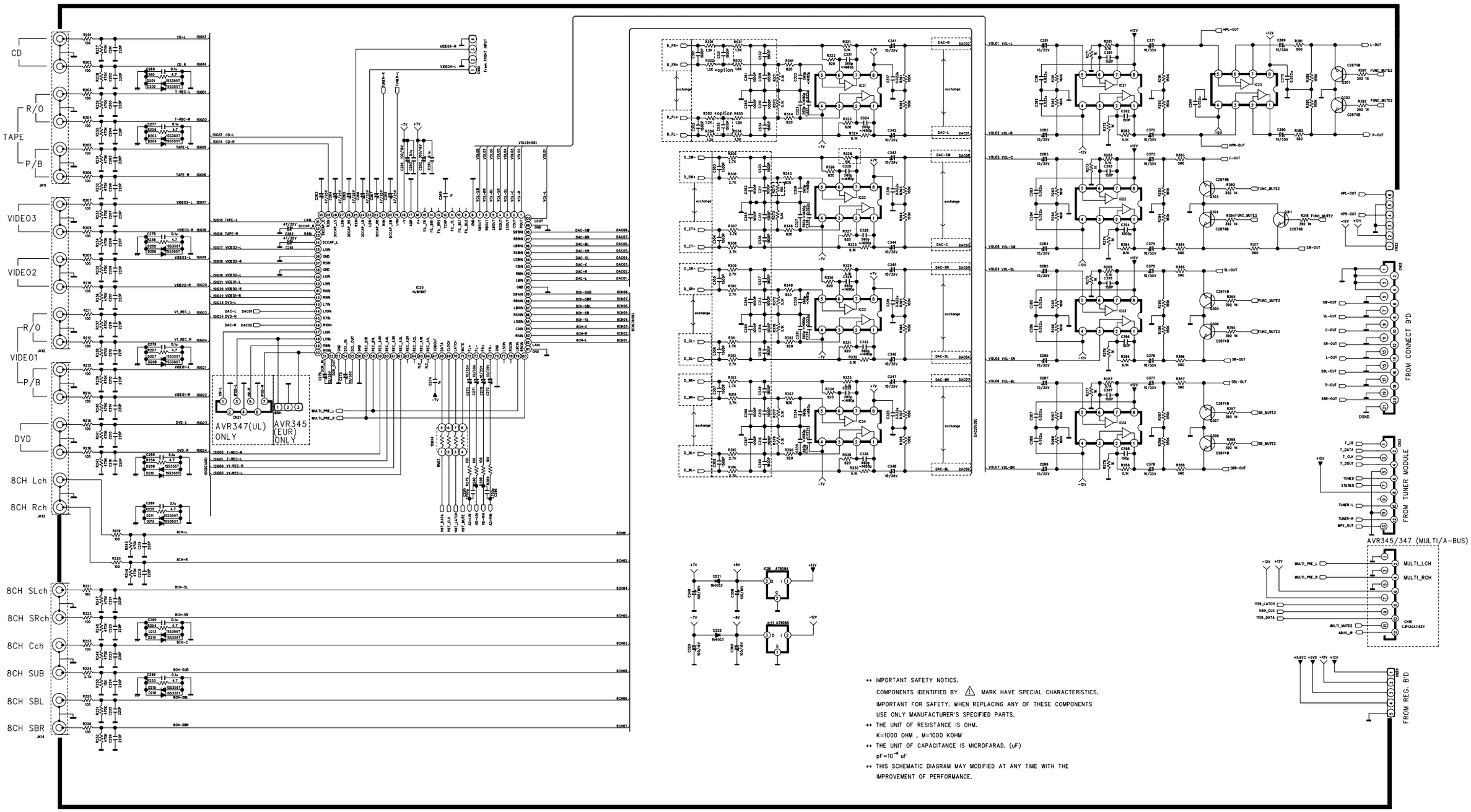
DATA	CS495**	Flash	SDRAM
EXT_D15/SD_D7	29	44	12
EXT_D14/SD_D6	30	42	11
EXT_D13/SD_D5	31	40	9
EXT_D12/SD_D4	32	38	8
EXT_D11/SD_D3	34	35	6
EXT_D10/SD_D2	35	33	5
EXT_D9/SD_D1	37	31	3
EXT_D8/SD_D0	39	29	2
EXT_D7/SD_D15	40	45	49
EXT_D6/SD_D14	41	43	48
EXT_D5/SD_D13	42	41	46
EXT_D4/SD_D12	43	39	45
EXT_D3/SD_D11	45	36	43
EXT_D2/SD_D10	46	34	42
EXT_D1/SD_D9	48	32	40
EXT_D0/SD_D8	49	30	39

Address	CS495**	Flash	SDRAM
EXT_A19	88	9	
EXT_A18	87	16	
EXT_A17	85	17	
EXT_A16	84	48	
EXT_A15	82	1	
EXT_A14/SD_A13	77	3	
EXT_A13/SD_A14	75	2	
EXT_A12/SD_A10	74	6	20
EXT_A11/SD_A12	55	4	
EXT_A10/SD_A11	56	5	19
EXT_A9/SD_A9	58	7	32
EXT_A8/SD_A8	59	8	31
EXT_A7/SD_A7	61	18	30
EXT_A6/SD_A6	62	19	29
EXT_A5/SD_A5	64	20	28
EXT_A4/SD_A4	67	21	27
EXT_A3/SD_A3	68	22	24
EXT_A2/SD_A2	70	23	23
EXT_A1/SD_A1	71	24	22
EXT_A0/SD_A0	72	25	21

REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR345/247/347		4/6
DESIGN	CHECK	APPROVE	DRAWING NO
M.S.K	W.Y.Y	H.W.L	1913SCMZ (DSP) 2/4
07.01.18	07.01.18	07.01.18	

CUP11913Z



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K=1000 OHM , M=1000 KOHM
** THE UNIT OF CAPACITANCE IS MICROFARAD. (uF)
pF=10^{-6} uF
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IMPROVEMENT OF PERFORMANCE.

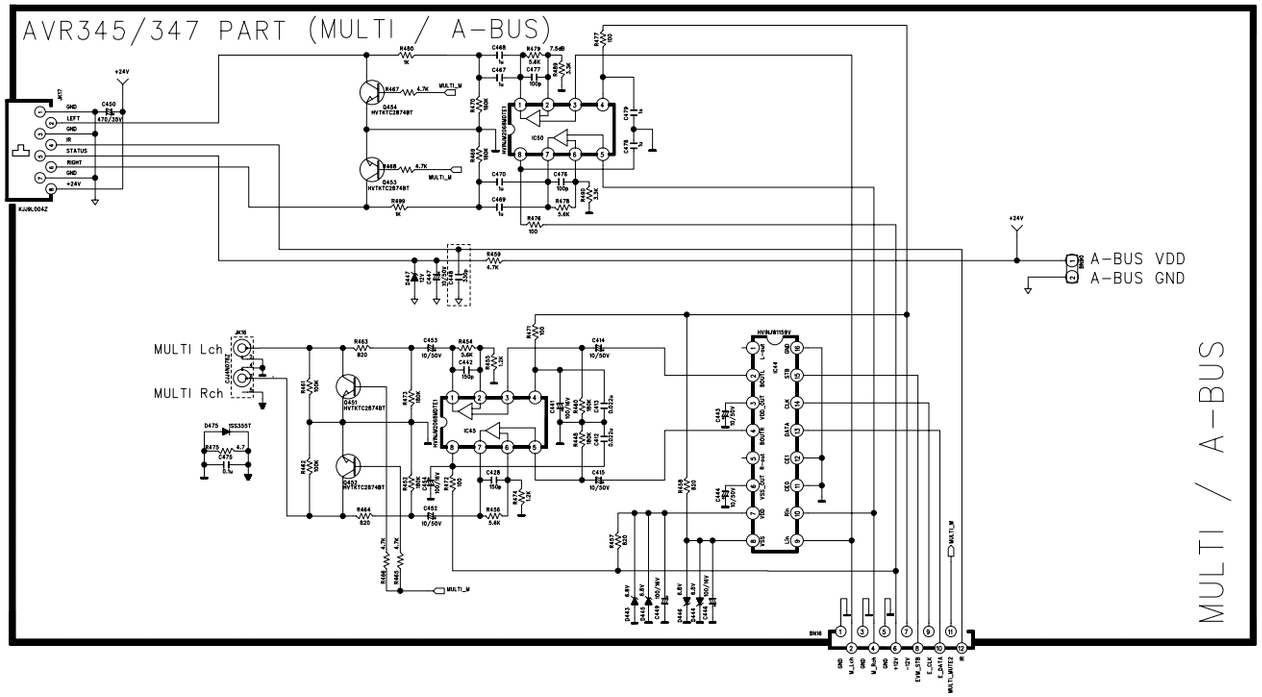
REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM — SHEET 4/6

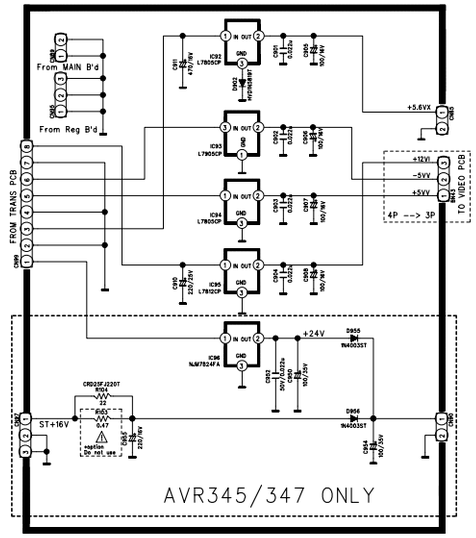
MODEL	AVR345/247/347		
DESIGN	CHECK	APPROVE	DRAWING NO
M.S.K	W.Y.Y	H.W.L	1913SCMZ (INPUT) 1/4
07.01.18	07.01.18	07.01.18	

CUP11913Z

AVR345/347 PART (MULTI / A-BUS)



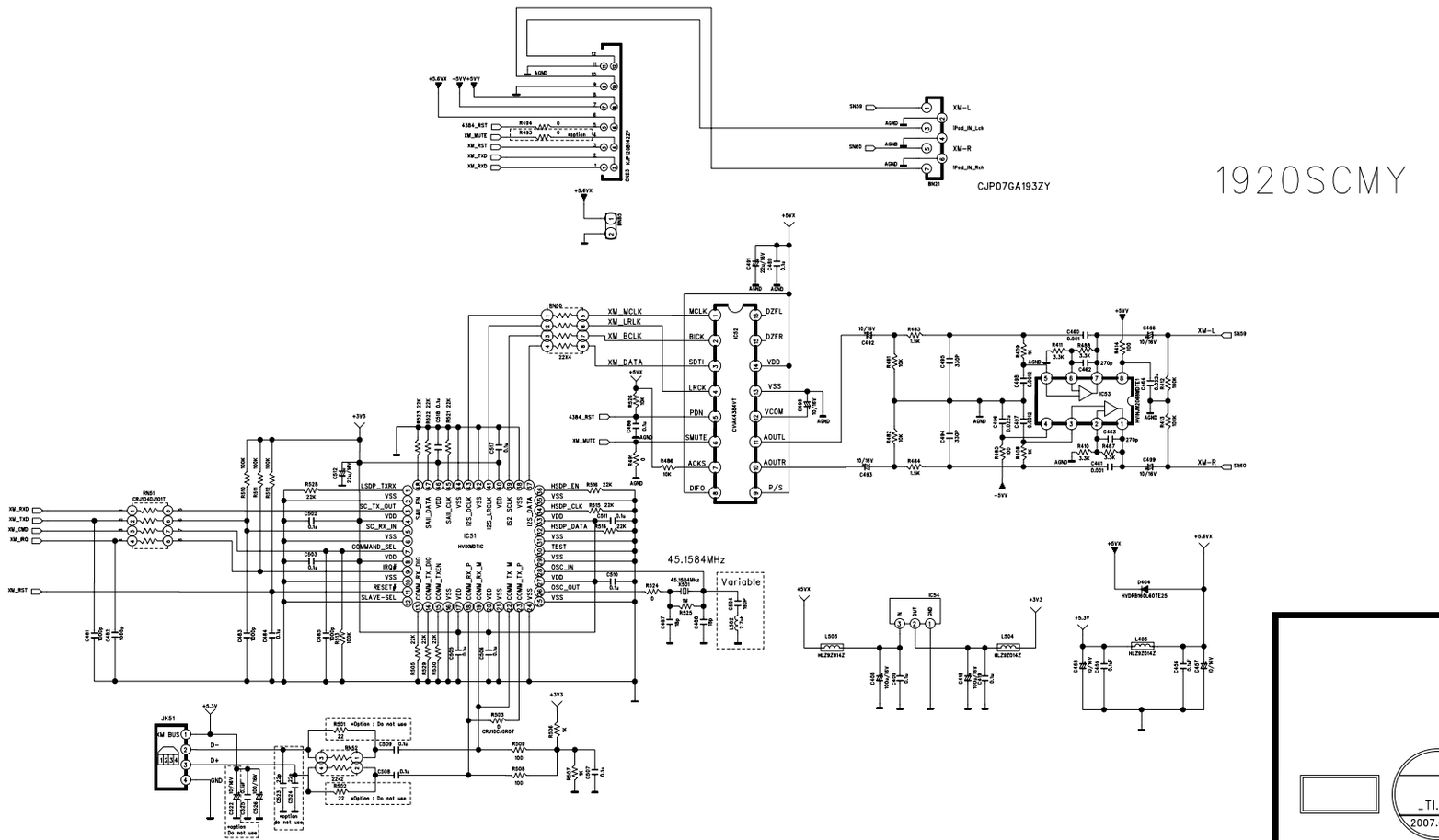
AVR345/347 PART (REGULATOR SECTION)



AVR247/347 PART (XM SECTION USA Ver. ONLY)

1920SCMY

CJP07GA193ZY



REVISION	2	4	6
1	3	5	7

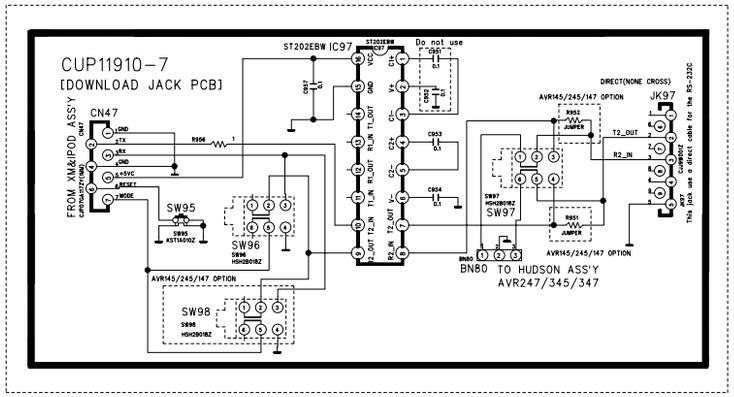
SCHEMATIC DIAGRAM — SHEET 4/6

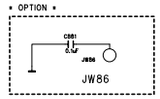
MODEL	AVR345/247/347		
DESIGN	CHECK	APPROVE	DRAWING NO
M.S.K	W.Y.Y	.H.W.L	1913SCMZ (MULTI) 4/4
07.01.18	07.01.18	07.01.18	

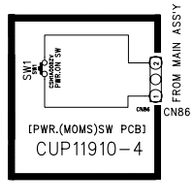
_TI. LAB 2007.01.18

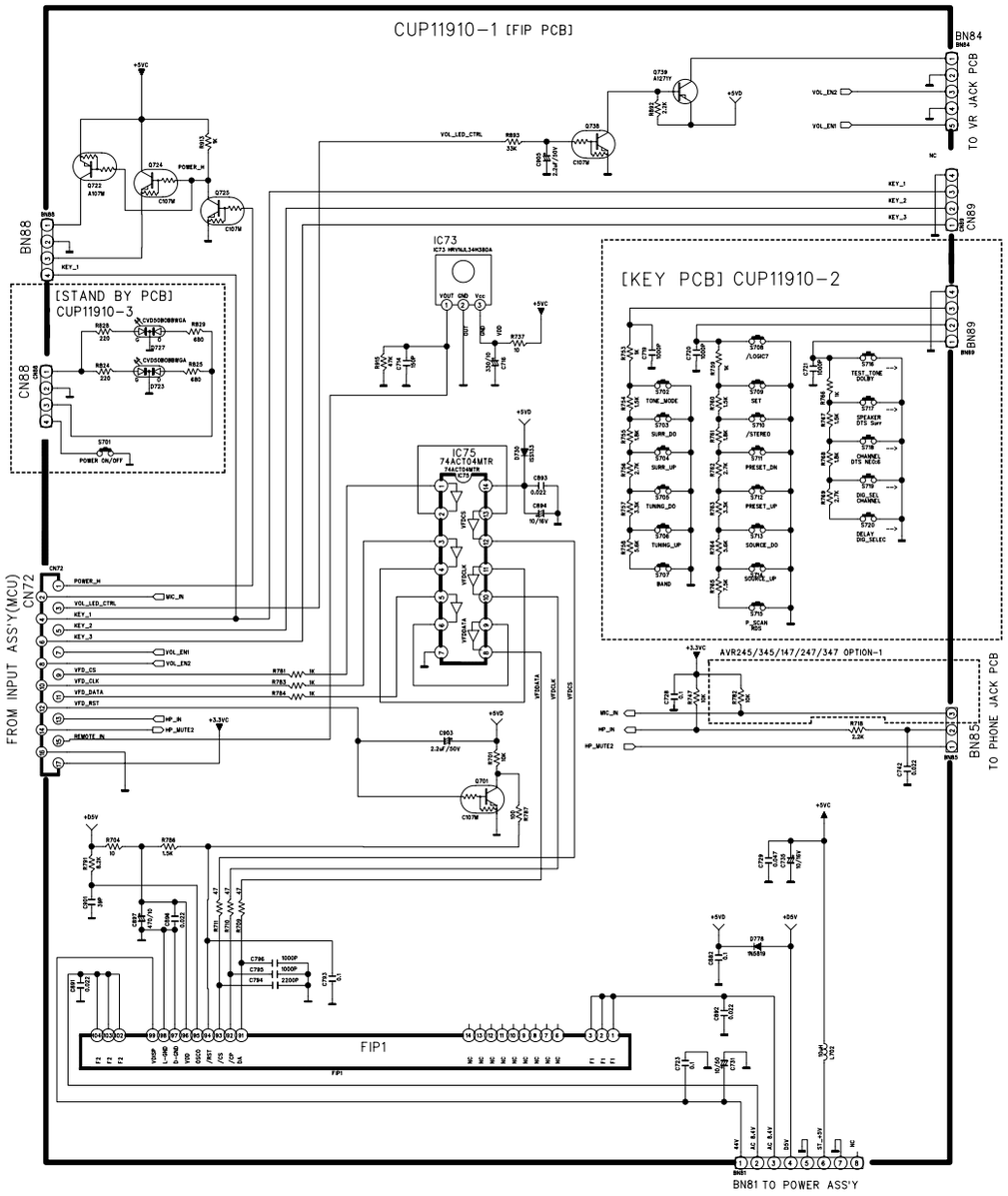
CUP11910X

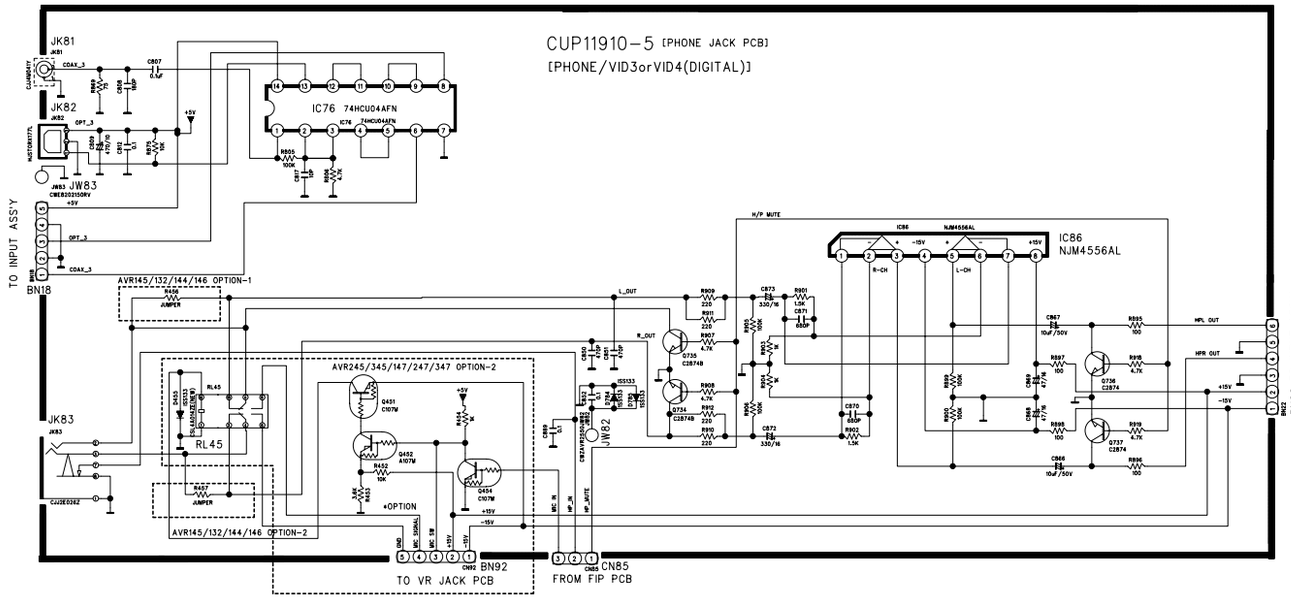
AVR145/245/345/147/247/347 PART

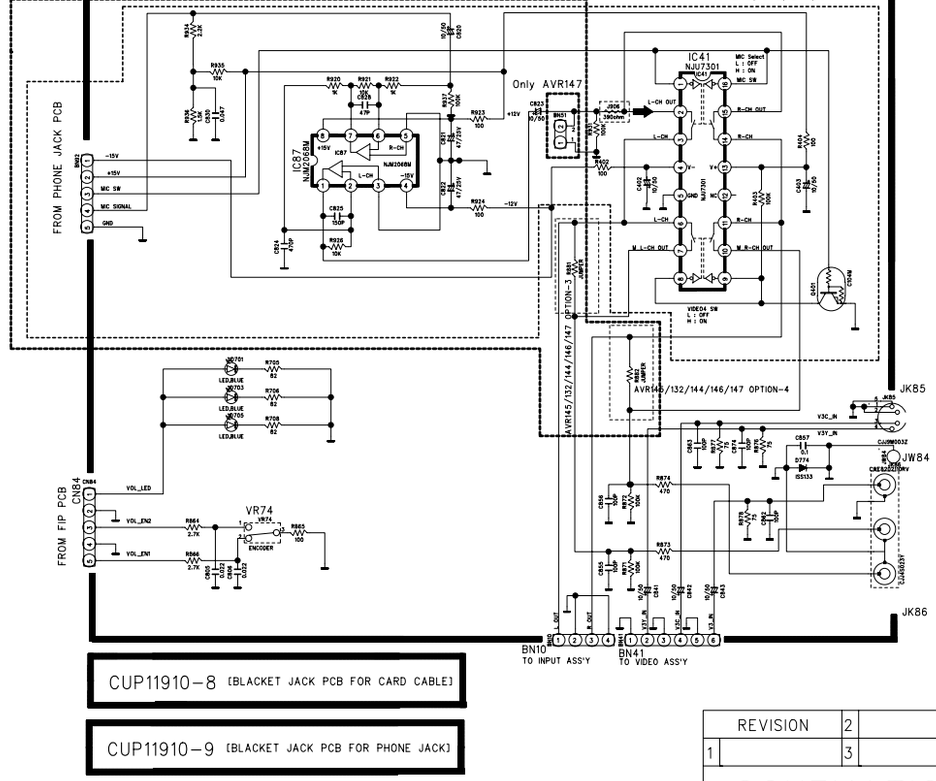












CUP11910-8 [BLACKET JACK PCB FOR CARD CABLE]

CUP11910-9 [BLACKET JACK PCB FOR PHONE JACK]

REVISION	2	4	6
1	3	5	7

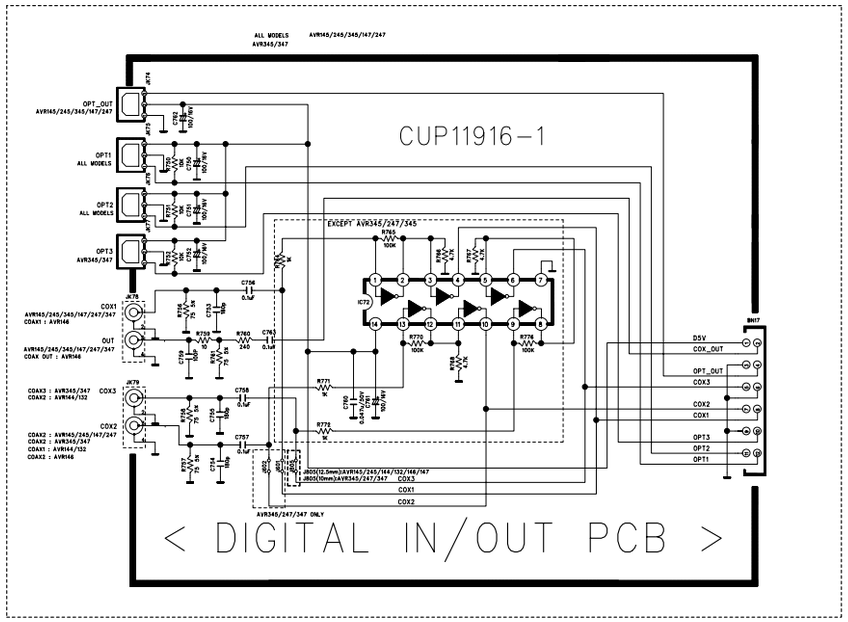
SCHEMATIC DIAGRAM — SHEET 1/7

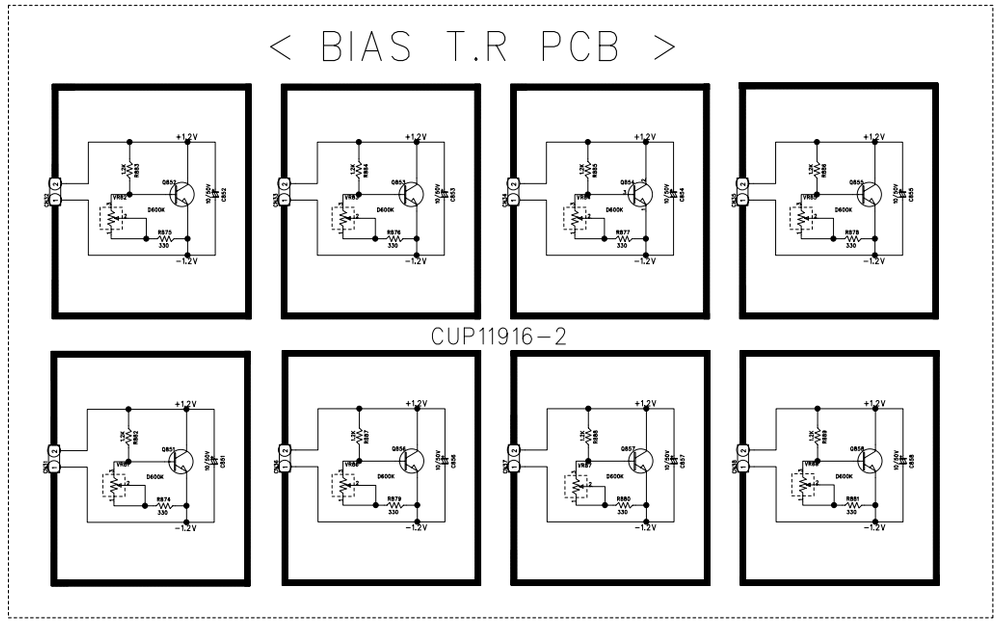
MODEL	AVR145/245/345/132/144 AVR146/147/247/347	
DESIGN	CHECK	APPROVE	DRAWING NO
S.H.Y	W.Y.Y	H.Y.L	1910SCMX (FRONT) 1/1
07.01.18	07.01.18	07.01.18	

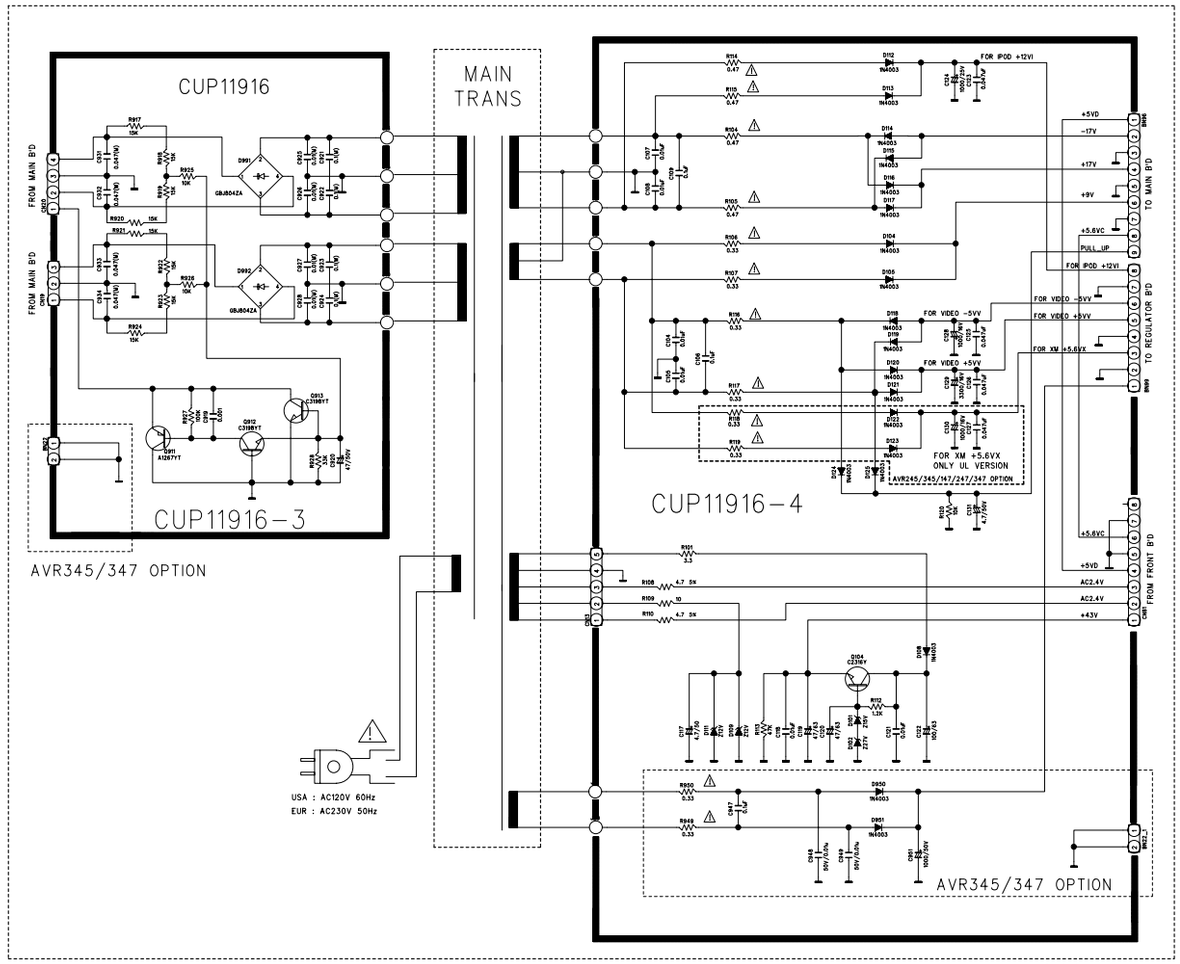
M/P

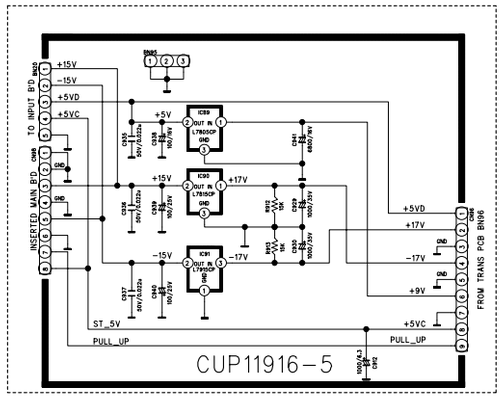
MI 2007.01.18

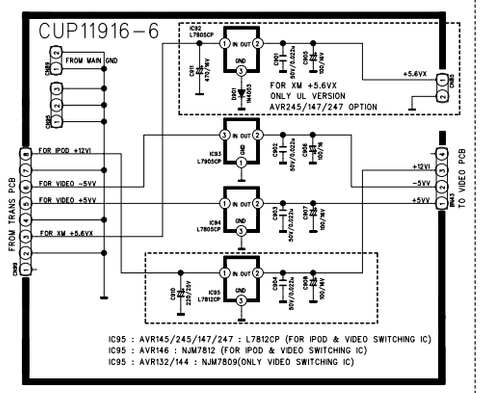
CUP11911X

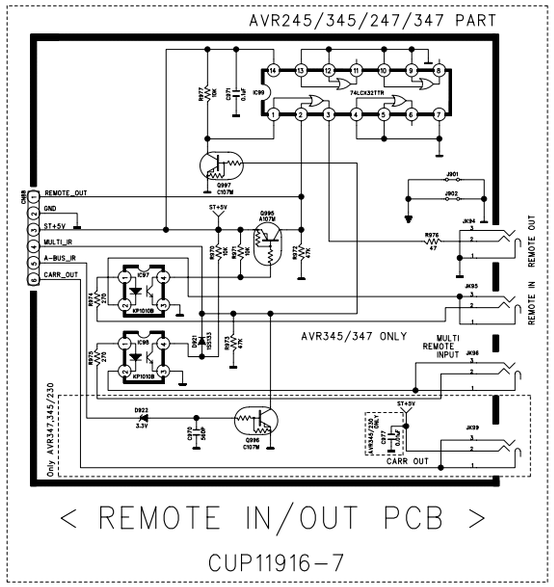












18

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR145/245/345/132/144 AVR146/147/247/347		3/7
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.L	W.Y.Y	H.W.L	1916SCMX (POWER)
07.01.18	07.01.18	07.01.18	1/1

CUP11918Z

FROM VIDEO4 JACK B'D

CN41

V4 S-V Y

V4 S-V C

V4 COMP

AVR347 (XM)

CN42 NO XM OPTION AVR345/230

IPOD Y

IPOD C

IPOD COMP

FROM IPOD

XM OPTION AVR247

+12V1

+5VV

-5VV

+5.6VX

IC48 HCF4053M013TR

JK40

VIDEO3

COMPOSITE

S-VIDEO C

S-VIDEO Y

IC41 NJM2595M

JK40-2

VIDEO2

JK40-1

VIDEO1 OUT

COMPO_REC_OUT

S-V-C_REC_OUT

S-V-Y_REC_OUT

JK41

VIDEO1 IN

JK41-2

DVD

JK41-1

MONITOR OUT

MON_VID_OUT

MON_C_OUT

MON_Y_OUT

IC42 NJM2595M

IC43 NJM2595M

*NJM2595M OPTION
==>V_MUTE "LOW" ACTIVE

FUNC.	SW1	SW2	SW3	SW4	SW5
VDEO1	L	H	X	X	H
VDEO2	H	L	X	L	H
VDEO3	H	H	H	H	H
V4_IPOD	H	H	X	L	H
DVD	H	H	L	H	H

IC62 MC7809C

* DEFINITION OF I2C REGISTER (NJW1321)

I2C BUS FORMAT

S(1BIT)	SLAVE ADDRESS(8BIT)	A(1BIT)	DATA(8BIT)	A(1BIT)	DATA(8BIT)	A(1BIT)	P(1BIT)

S : Starting Term
A : Acknowledge Bit
P : Ending Term

SLAVE ADDRESS

MSB							LSB	MSB	Hex
1	0	0	0	0	0	ADR(1BIT)	R/NOT W(1BIT)		--

R/NOT W : Set the Write Mode or Read Mode.
ADR : Set the Slave Address by " ADR" terminal.
R/NOT W = 0 : WRITE MODE, ADR = 0/1 ; ADR=0 Hex(94(h)), ADR=1 Hex(96(h)
R/NOT W = 0 : READ MODE, ADR = 0/1 ; ADR=0 Hex(95(h)), ADR=1 Hex(97(h)

CONTROL REGISTER TABLE

<WRITE MODE>

NO.	BIT D7	D6	D5	D4	D3	D2	D1	D0
DATA 1	PS1	PS2	OUT1				OUT2	
DATA 2	AUX0		AUX1		AUX2		AUX3	

PS : POWER SAVE
=> PS = 1 ; POWER SAVE ON (MUTE), PS = 0 ; POWER SAVE OFF (OUT ON)
OUT : OUTPUT
AUX : AUXILIARY (CONTROL SIGNAL OUTPUT)

<READ MODE>

NO.	BIT D7	D6	D5	D4	D3	D2	D1	D0
DATA	PORT0		PORT1		PORT2		PORT3	

PORT : INPUT

JK62

COMPONENT IN2 & COMPONENT IN1

IC61 NJW1321

JK69

COMPONENT IN3 & COMPONENT OUT

FROM POWER PCB

CN14

FROM MCU PCB

BN81

TO FLI8125 ANALOG OUTPUT

FROM ADV7322 ANALOG INPUT

BN15

DAO2_LRCLK
DAO2_SCLK
DAO2_DATA0
DAO_MCLK
HDMI_SPDIF
HDMI_MCLK
HDMI_SCK
HDMI_LRCK
HDMI_SDO
HDMI_SD1
HDMI_SD2
HDMI_SD3
GND

* AVR345 =NO.4

REVISION	2		4		6	
1	3		5		7	

SCHEMATIC DIAGRAM — SHEET 5/6

MODEL	AVR345/247/347		
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.L	W.Y.Y.	H.W.L	1918SCMZ (VIDEO) 1/1
07.01.29	07.01.29	07.01.29	

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