harman/kardon Service Manual

AVR 347/230
AVR 350/230

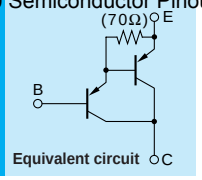
7 x 55W 7.1 CHANNEL A/V RECEIVERS

CONTENTS

THIS MANUAL CONTAINS SEMICONDUCTOR PINOUTS ONLY.
Main Service Manual in separate file

harman/kardon, Inc.
250 Crossways Park Dr.
Woodbury, New York, 11797

Darlington 2SB1647



Silicon PNP Epitaxial Planar Transistor (Complement to type 2SD2560)

Application : Audio, Series Regulator and General Purpose

Absolute maximum ratings (Ta=25°C)

Symbol	2SB1647	Unit
V_{CBO}	–150	V
V_{CEO}	–150	V
V_{EBO}	–5	V
I_C	–15	A
I_B	–1	A
P_C	130(Tc=25°C)	W
Tj	150	°C
Tstg	–55 to +150	°C

Electrical Characteristics (Ta=25°C)

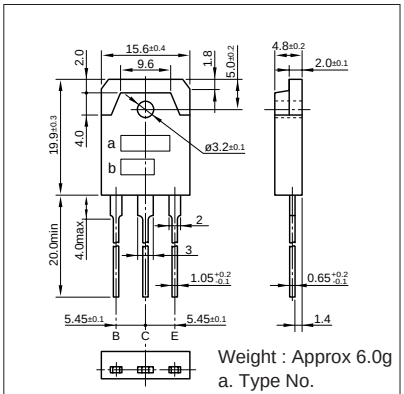
Symbol	Conditions	2SB1647	Unit
I_{CBO}	V_{CB}=–150V	–100max	μA
I_{EBO}	V_{EB}=–5V	–100max	μA
$V_{(BR)CEO}$	I_C=–30mA	–150min	V
h_{FE}	V_{CE}=–4V, I_C=–10A	5000min*	
$V_{CE(sat)}$	I_C=–10A, I_B=–10mA	–2.5max	V
$V_{BE(sat)}$	I_C=–10A, I_B=–10mA	–3.0max	V
f_T	V_{CE}=–12V, I_E=2A	45typ	MHz
C_{OB}	V_{CB}=–10V, f=1MHz	320typ	pF

*h_{FE} Rank O(5000 to 12000), P(6500 to 20000), Y(15000 to 30000)

Typical Switching Characteristics (Common Emitter)

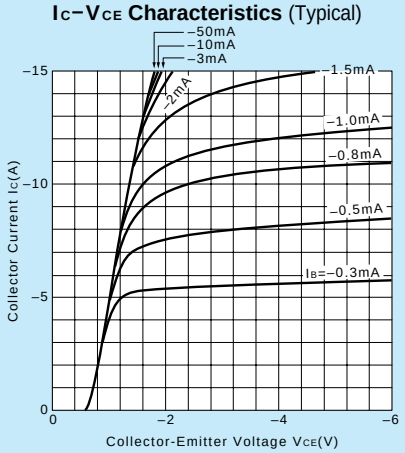
V_{CC} (V)	R_L (Ω)	I_C (A)	V_{BB1} (V)	V_{BB2} (V)	I_{B1} (mA)	I_{B2} (mA)	ton (μs)	tstg (μs)	tf (μs)
–40	4	10	–10	5	–10	10	0.7typ	1.6typ	1.1typ

External Dimensions MT-100(TO3P)

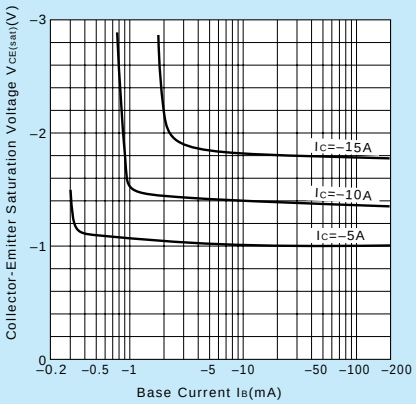


Weight : Approx 6.0g
a. Type No.
b. Lot No.

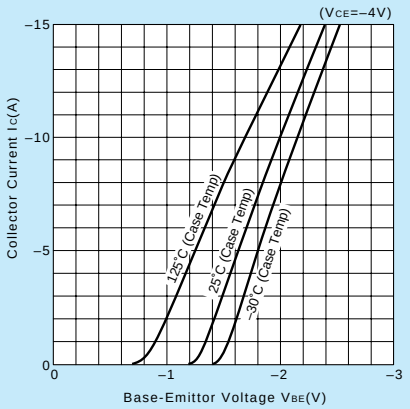
I_C–V_{CE} Characteristics (Typical)



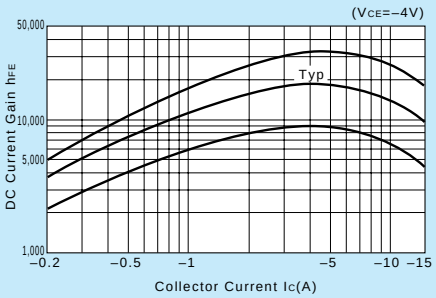
$V_{CE(sat)}$–I_B Characteristics (Typical)



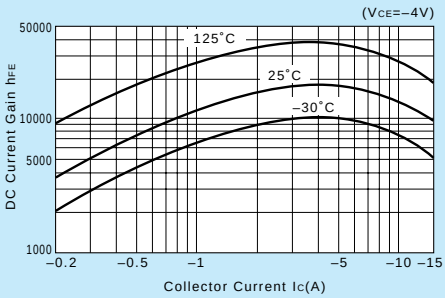
I_C–V_{BE} Temperature Characteristics (Typical)



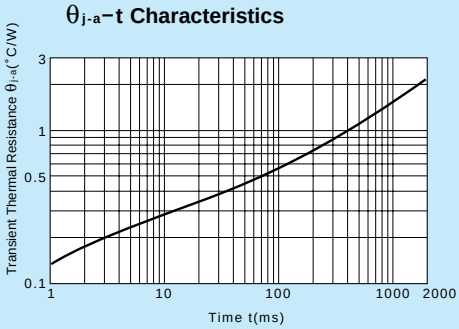
h_{FE}–I_C Characteristics (Typical)



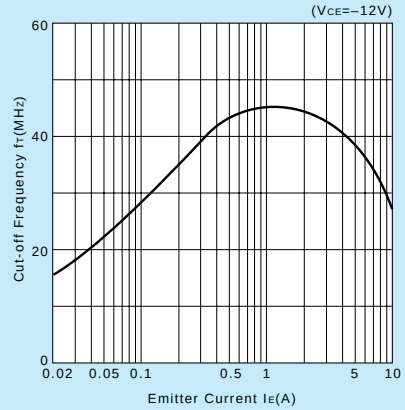
h_{FE}–I_C Temperature Characteristics (Typical)



$\theta_{j\text{-}a}$–t Characteristics

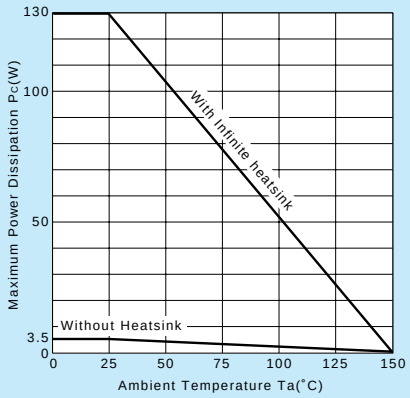


f_T–I_E Characteristics (Typical)



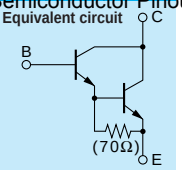
Safe Operating Area (Single Pulse)

Pc–Ta Derating



Darlington 2SD2560

Equivalent circuit



Silicon NPN Triple Diffused Planar Transistor (Complement to type 2SB1647)

Application : Audio, Series Regulator and General Purpose

Absolute maximum ratings (Ta=25°C)

Symbol	2SD2560	Unit
V_{CBO}	150	V
V_{CEO}	150	V
V_{EBO}	5	V
I_C	15	A
I_B	1	A
P_C	130(Tc=25°C)	W
Tj	150	°C
Tstg	–55to+150	°C

Electrical Characteristics (Ta=25°C)

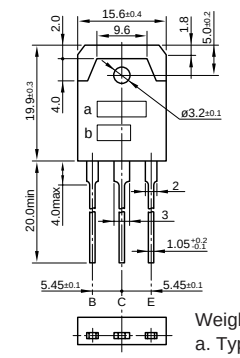
Symbol	Conditions	2SD2560	Unit
I_{CBO}	V_{CB}=150V	100max	μA
I_{EBO}	V_{EB}=5V	100max	μA
$V_{(BR)CEO}$	I_C=30mA	150min	V
h_{FE}	V_{CE}=4V, I_C=10A	5000min*	
$V_{CE(sat)}$	I_C=10A, I_B=10mA	2.5max	V
$V_{BE(sat)}$	I_C=10A, I_B=10mA	3.0max	V
f_T	V_{CE}=12V, I_E=–2A	70typ	MHz
C_{OB}	V_{CB}=10V, f=1MHz	120typ	pF

*h_{FE} Rank O(5000to12000), P(6500to20000), Y(15000to30000)

Typical Switching Characteristics (Common Emitter)

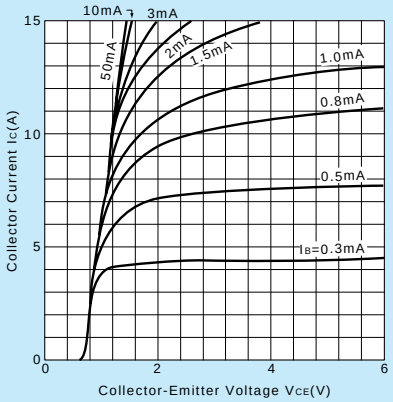
V_{CC} (V)	R_L (Ω)	I_C (A)	V_{BB1} (V)	V_{BB2} (V)	I_{B1} (mA)	I_{B2} (mA)	ton (μs)	tstg (μs)	tf (μs)
40	4	10	10	–5	10	–10	0.8typ	4.0typ	1.2typ

External Dimensions MT-100(TO3P)

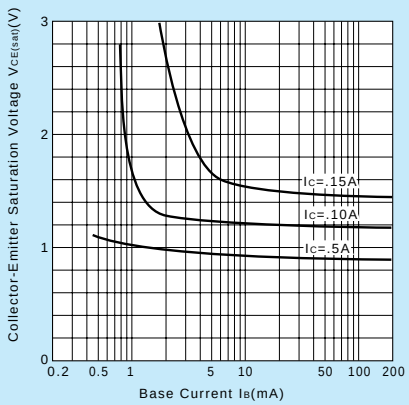


Weight : Approx 6.0g
a. Type No.
b. Lot No.

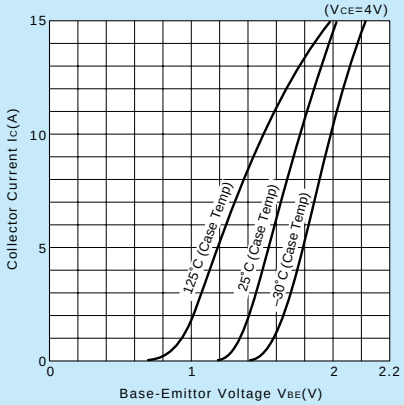
I_C–V_{CE} Characteristics (Typical)



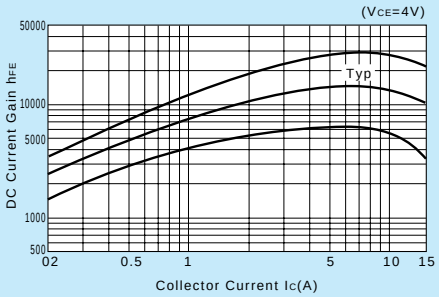
$V_{CE(sat)}$–I_B Characteristics (Typical)



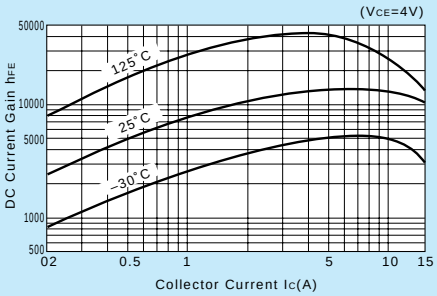
I_C–V_{BE} Temperature Characteristics (Typical)



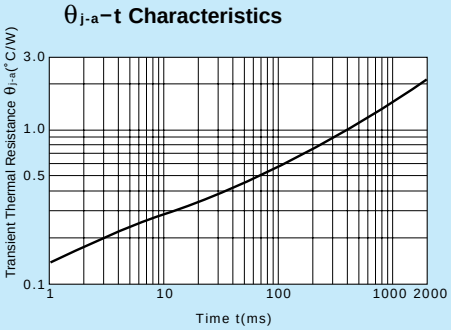
h_{FE}–I_C Characteristics (Typical)



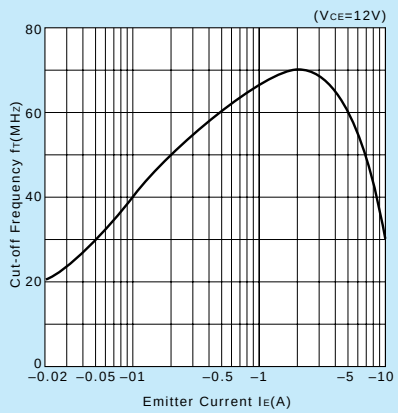
h_{FE}–I_C Temperature Characteristics (Typical)



$\theta_{j\text{-}a}$–t Characteristics

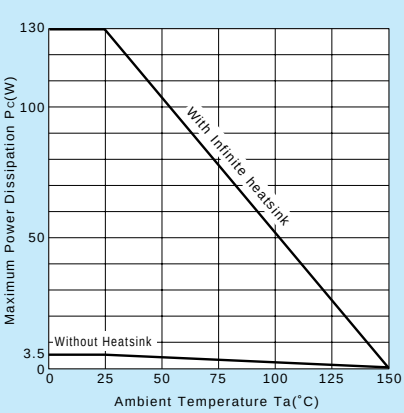


f_T–I_E Characteristics (Typical)



Safe Operating Area (Single Pulse)

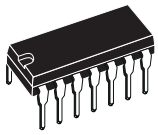
Pc–Ta Derating



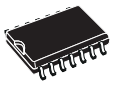
74ACT04

HEX INVERTER

- HIGH SPEED: t_{PD} = 5.0ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION: I_{CC} = 2µA(MAX.) at T_A=25°C
- COMPATIBLE WITH TTL OUTPUTS V_{IH} = 2V (MIN.), V_{IL} = 0.8V (MAX.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 24mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 04
- IMPROVED LATCH-UP IMMUNITY



DIP



SOP

TSSOP

ORDER CODES

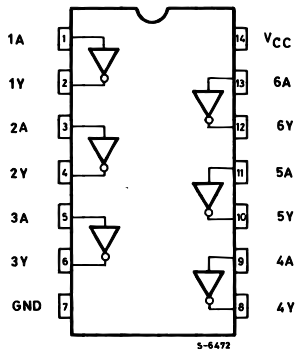
PACKAGE	TUBE	T & R
DIP	74ACT04B	
SOP	74ACT04M	74ACT04MTR
TSSOP		74ACT04TTR

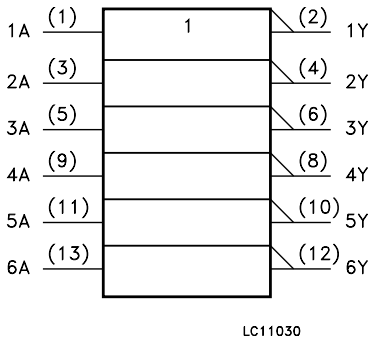
DESCRIPTION

The 74ACT04 is an advanced high-speed CMOS HEX INVERTER fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.
The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS

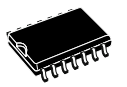




74LCX32

LOW VOLTAGE CMOS QUAD 2-INPUT OR GATE WITH 5V TOLERANT INPUTS

- 5V TOLERANT INPUTS
- HIGH SPEED:
  t_{PD} = 5.2ns (MAX.) at V_{CC} = 3V
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24mA (MIN) at V_{CC} = 3V
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2.0V to 3.6V (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 32
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:
  HBM > 2000V (MIL STD 883 method 3015);
  MM > 200V



SOP

TSSOP

Table 1: Order Codes

PACKAGE	T & R
SOP	74LCX32MTR
TSSOP	74LCX32TTR

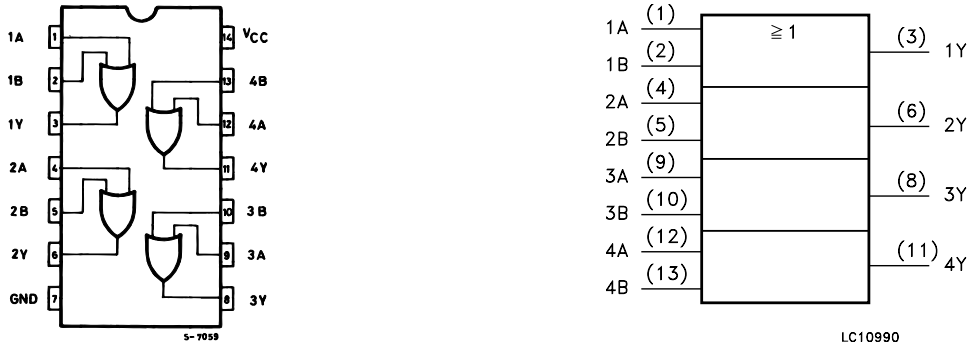
DESCRIPTION

The 74LCX32 is a low voltage CMOS QUAD 2-INPUT OR GATE fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for inputs.

It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols



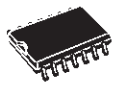
Rev. 6

September 2004

74LCX74

LOW VOLTAGE CMOS DUAL D-TYPE FLIP FLOP WITH 5V TOLERANT INPUTS

- 5V TOLERANT INPUTS
- HIGH SPEED :
  f_{MAX} = 150 MHz (MAX.) at V_{CC} = 3V
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24mA (MIN) at V_{CC} = 3V
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2.0V to 3.6V (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 74
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:
  HBM > 2000V (MIL STD 883 method 3015);
  MM > 200V



SOP

TSSOP

ORDER CODES

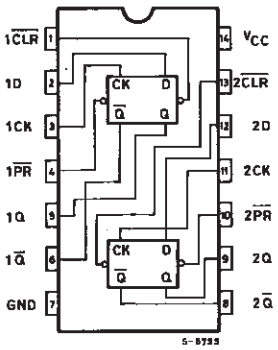
PACKAGE	TUBE	T & R
SOP	74LCX74M	74LCX74MTR
TSSOP		74LCX74TTR

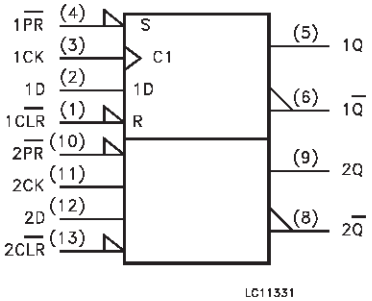
DESCRIPTION

The 74LCX74 is a low voltage CMOS DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for inputs.

A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of the clock pulse.
$\overline{CLR}$ and $\overline{PR}$ are independent of the clock and accomplished by a low setting on the appropriate input.
It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS

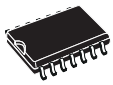




74VHC08

QUAD 2-INPUT AND GATE

- HIGH SPEED: t_{PD} = 4.3 ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION: I_{CC} = 2 µA (MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 8mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC}(OPR) = 2V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 08
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: V_{OLP} = 0.8V (MAX.)



SOP

TSSOP

ORDER CODES

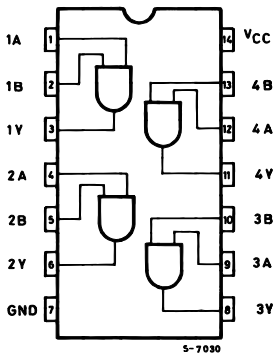
PACKAGE	TUBE	T & R
SOP	74VHC08M	74VHC08MTR
TSSOP		74VHC08TTR

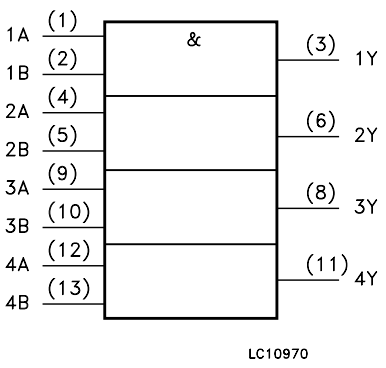
DESCRIPTION

The 74VHC08 is an advanced high-speed CMOS QUAD 2-INPUT AND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.
The internal circuit is composed of 2 stages including buffer output, which provides high noise immunity and stable output.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





June 2001

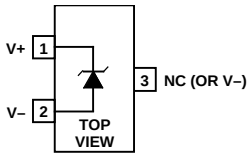
ANALOG DEVICES

1.2 V Micropower, Precision Shunt Voltage Reference

AD1580

FEATURES
Wide Operating Range: 50 μA–10 mA
Initial Accuracy: ±0.1% max
Temperature Drift: ±50 ppm/°C max
Output Impedance: 0.5 Ω max
Wideband Noise (10 Hz–10 kHz): 20 μV rms
Operating Temperature Range: –40°C to +85°C
High ESD Rating
4 kV Human Body Model
400 V Machine Model
Compact, Surface-Mount, SOT-23 Package

PIN CONFIGURATION
SOT-23 Package



NC = NO CONNECT

GENERAL DESCRIPTION

The AD1580 is a low cost, two-terminal (shunt), precision bandgap reference. It provides an accurate 1.225 V output for input currents between 50 μA and 10 mA.

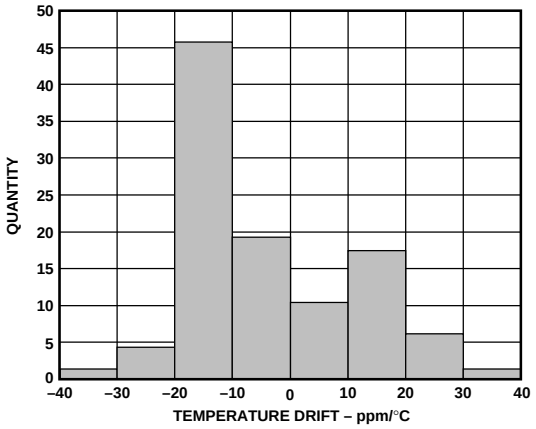
The AD1580's superior accuracy and stability is made possible by the precise matching and thermal tracking of on-chip components. Proprietary curvature correction design techniques have been used to minimize the nonlinearities in the voltage output temperature characteristics. The AD1580 is stable with any value of capacitive load.

The low minimum operating current makes the AD1580 ideal for use in battery powered 3 V or 5 V systems. However, the wide operating current range means that the AD1580 is extremely versatile and suitable for use in a wide variety of high current applications.

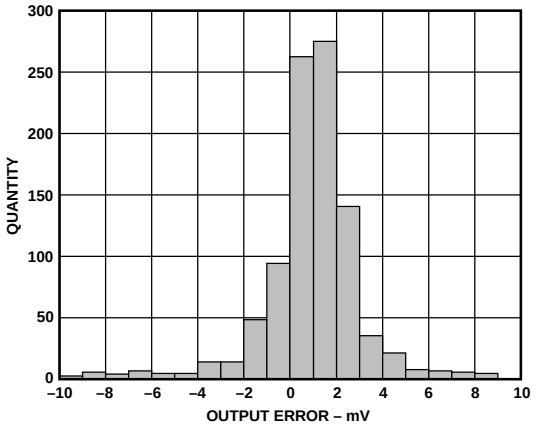
The AD1580 is available in two grades, A and B, both of which are provided in an SOT-23 package, the smallest surface mount package available on the market. Both grades are specified over the industrial temperature range of –40°C to +85°C.

TARGET APPLICATIONS

1. Portable, Battery-Powered Equipment:
   Cellular Phones, Notebook Computers, PDAs, GPS and DMM.
2. Computer Workstations
   Suitable for use with a wide range of video RAMDACs.
3. Smart Industrial Transmitters
4. PCMCIA Cards.
5. Automotive.
6. 3 V/5 V 8–12-Bit Data Converters.



Reverse Voltage Temperature Drift Distribution



Reverse Voltage Error Distribution

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

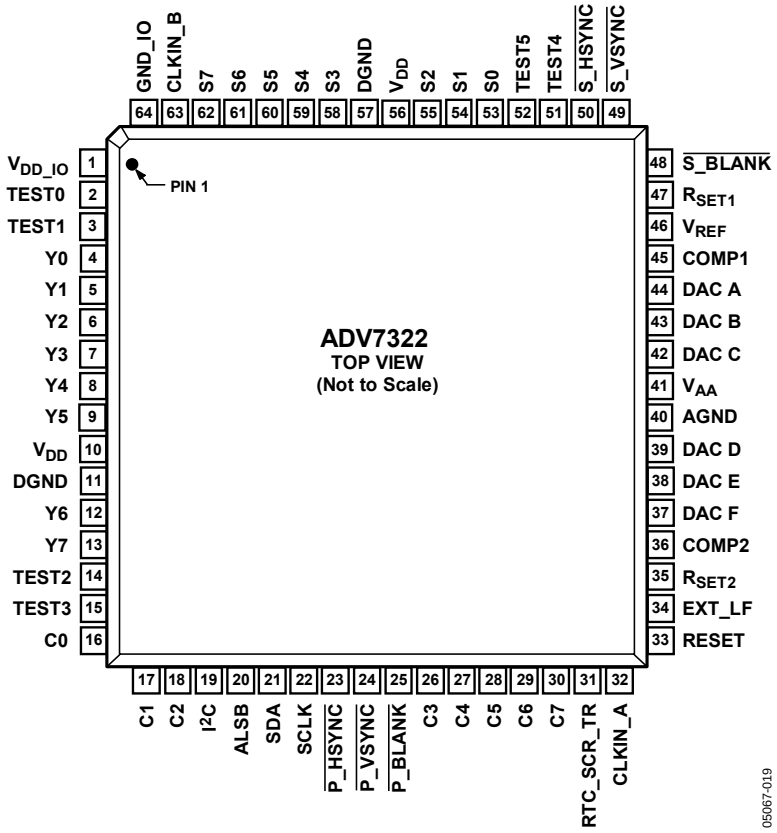


Figure 19. Pin Configuration

Table 6. Pin Function Descriptions

Mnemonic	Input/Output	Function
DGND	G	Digital Ground.
AGND	G	Analog Ground.
CLKIN_A	I	Pixel Clock Input for HD (74.25 MHz Only, PS Only (27 MHz), SD Only (27 MHz).
CLKIN_B	I	Pixel Clock Input. Requires a 27 MHz reference clock for progressive scan mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV mode. This clock is only used in dual modes.
COMP1, COMP2	O	Compensation Pin for DACs. Connect 0.1 µF capacitor from COMP pin to V_{AA}.
DAC A	O	CVBS/Green/Y/Y Analog Output.
DAC B	O	Chroma/Blue/U/Pb Analog Output.
DAC C	O	Luma/Red/V/Pr Analog Output.
DAC D	O	In SD Only Mode: CVBS/Green/Y Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Y/Green [HD] Analog Output.
DAC E	O	In SD Only Mode: Luma/Blue/U Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Pr/Red Analog Output.
DAC F	O	In SD Only Mode: Chroma/Red/V Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Pb/Blue [HD] Analog Output.
$\overline{\text{P\_HSYNC}}$	I	Video Horizontal Sync Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
$\overline{\text{P\_VSYNC}}$	I	Video Vertical Sync Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
$\overline{\text{P\_BLANK}}$	I	Video Blanking Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
$\overline{\text{S\_BLANK}}$	I/O	Video Blanking Control Signal for SD Only.
$\overline{\text{S\_HSYNC}}$	I/O	Video Horizontal Sync Control Signal for SD Only.
$\overline{\text{S\_VSYNC}}$	I/O	Video Vertical Sync Control Signal for SD Only.
Y7 to Y0	I	SD or Progressive Scan/HDTV Input Port for Y Data. Input port for interleaved progressive scan data. The LSB is set up on Pin Y0.
C7 to C0	I	Progressive Scan/HDTV Input Port 4:4:4 Input Mode. This port is used for the Cb [Blue/U] data. The LSB is set up on Pin C0.
S7 to S0	I	SD or Progressive Scan/HDTV Input Port for Cr [Red/V] data in 4:4:4 input mode. LSB is set up on Pin S0.
$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7322 into default register setting. $\overline{\text{RESET}}$ is an active low signal.
R_{SET1}, R_{SET2}	I	A 3040 Ω resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs.
SCLK	I	I^2C Port Serial Interface Clock Input.
SDA	I/O	I^2C Port Serial Data Input/Output.
ALSB	I	TTL Address Input. This signal sets up the LSB of the I^2C address. When this pin is tied low, the I^2C filter is activated, which reduces noise on the I^2C interface.
V_{DD_IO}	P	Power Supply for Digital Inputs and Outputs.
V_{DD}	P	Digital Power Supply.
V_{AA}	P	Analog Power Supply.
V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
EXT_LF	I	External Loop Filter for the Internal PLL.
RTC_SCR_TR	I	Multifunctional Input. Real time control (RTC) input, timing reset input, subcarrier reset input.
I^2C	I	This input pin must be tied high (V_{DD_IO}) for the ADV7322 to interface over the I^2C port.
GND_IO		Digital Input/Output Ground.
TEST0 to TEST5	I	Not used. Tie to DGND

Features

- **Low-voltage and Standard-voltage Operation**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)**
- **Two-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **100 kHz (1.8V) and 400 kHz (2.7V, 5V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **8-byte Page (1K, 2K), 16-byte Page (4K, 8K, 16K) Write Modes**
- **Partial Page Writes Allowed**
- **Self-timed Write Cycle (5 ms max)**
- **High-reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **Automotive Grade and Lead-free/Halogen-free Devices Available**
- **8-lead PDIP, 8-lead JEDEC SOIC, 8-lead MAP, 5-lead SOT23, 8-lead TSSOP and 8-ball dBGA2 Packages**
- **Die Sales: Wafer Form, Waffle Pack and Bumped Wafers**

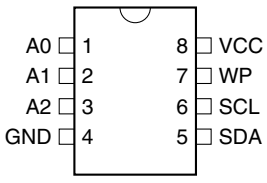
Description

The AT24C01A/02/04/08A/16A provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24C01A/02/04/08A/16A is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead MAP, 5-lead SOT23 (AT24C01A/AT24C02/AT24C04), 8-lead TSSOP, and 8-ball dBGA2 packages and is accessed via a Two-wire serial interface. In addition, the entire family is available in 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

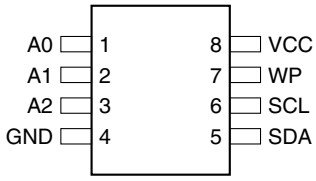
Table 1. Pin Configuration

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect
GND	Ground
VCC	Power Supply

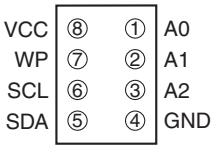
8-lead TSSOP



8-lead SOIC

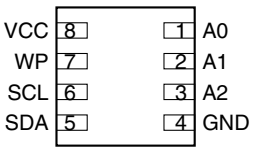


8-ball dBGA2



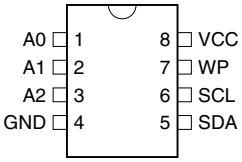
Bottom View

8-lead MAP

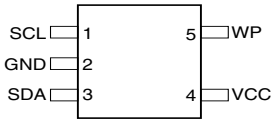


Bottom View

8-lead PDIP



5-lead SOT23



Two-wire Serial EEPROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

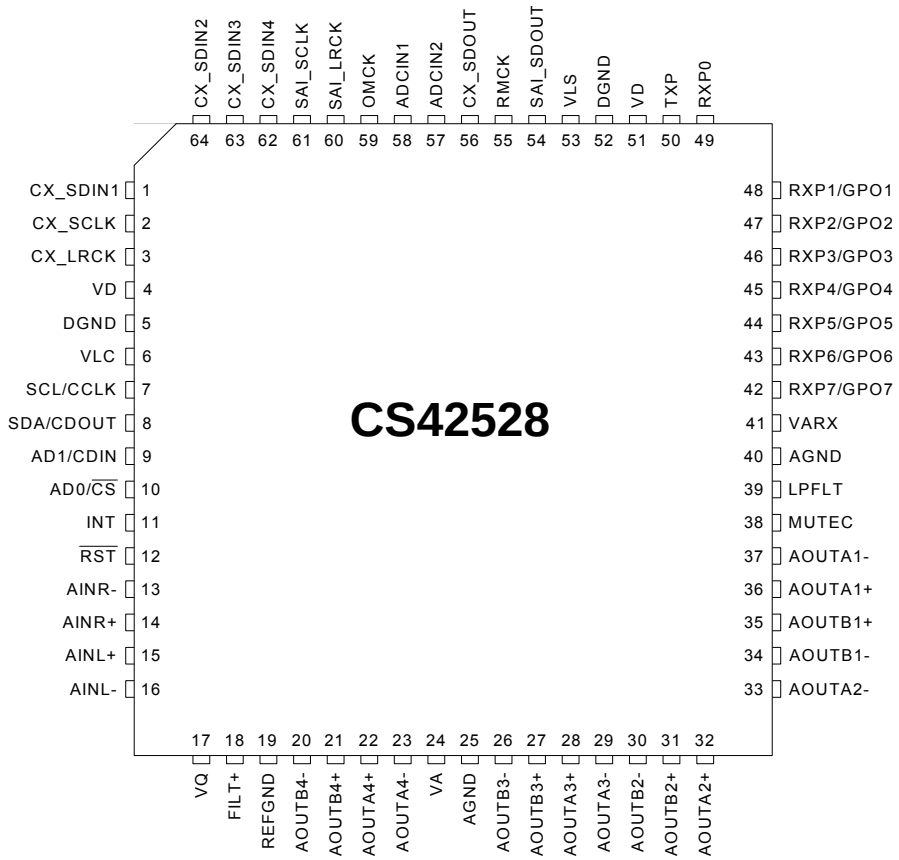
8K (1024 x 8)

16K (2048 x 8)

AT24C01A
AT24C02
AT24C04
AT24C08A
AT24C16A

0180V–SEEPR–8/05

2. PIN DESCRIPTIONS

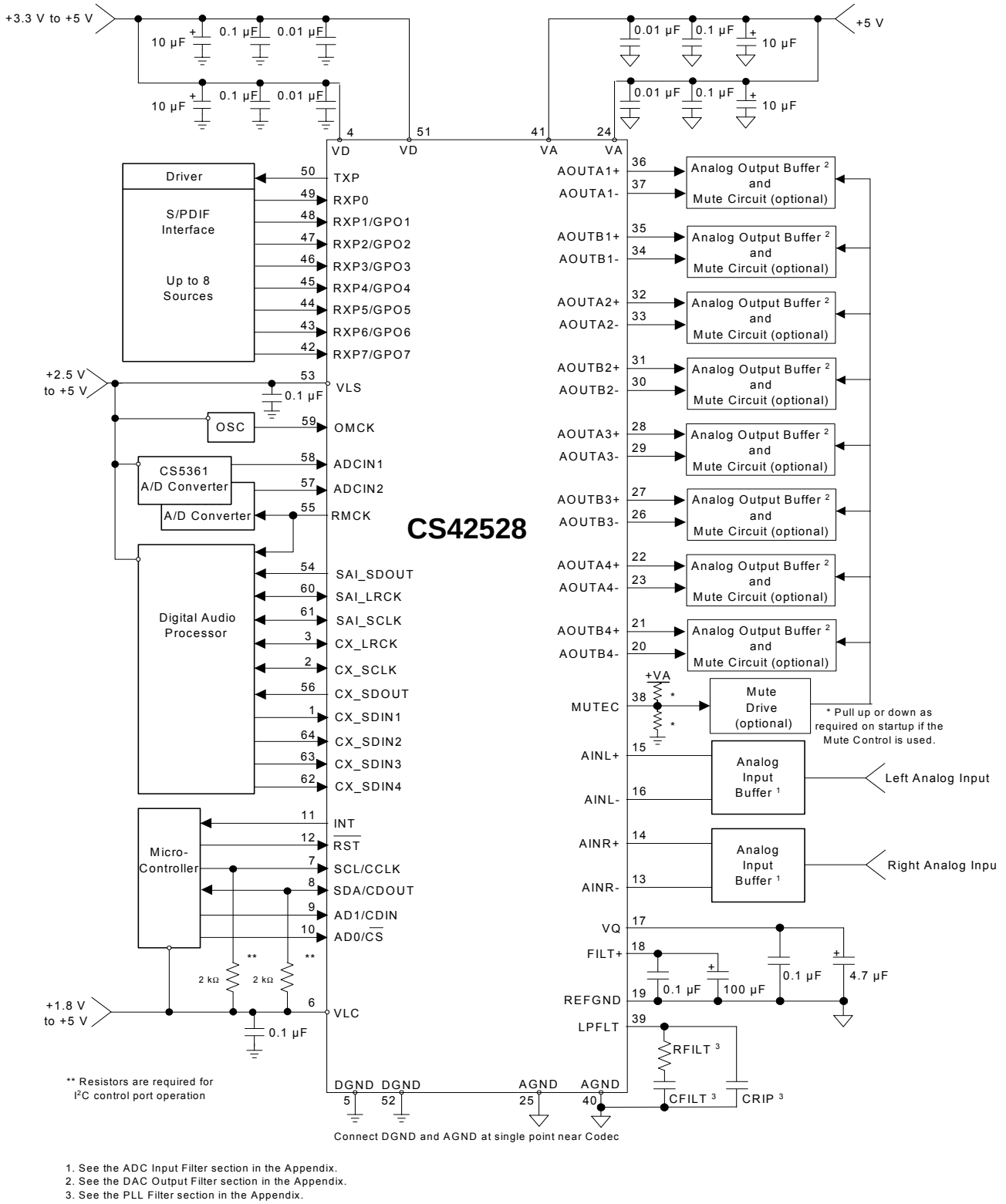


Pin Name	#	Pin Description
CX_SDIN1 **CX_SDIN2** **CX_SDIN3** **CX_SDIN4**	1 64 63 62	**Codec Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
CX_SCLK	2	**CODEC Serial Clock** *(Input/Output)* - Serial clock for the CODEC serial audio interface.
CX_LRCK	3	**CODEC Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the CODEC serial audio data line.
VD	4 51	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	5 52	**Digital Ground** (*Input*) - Ground reference. Should be connected to digital ground.
VLC	6	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port.
SCL/CCLK	7	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I^2C mode as shown in the Typical Connection Diagram.
SDA/CDOUT	8	**Serial Control Data** (*Input/Output*) **-** SDA is a data I/O line in I^2C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDOUT is the output data line for the control port interface in SPI mode.
AD1/CDIN	9	**Address Bit 1 (I^2C)/Serial Control Data (SPI)** (*Input*) - AD1 is a chip address pin in I^2C mode; CDIN is the input data line for the control port interface in SPI mode.

	10	**Address Bit 0 (I^2C)/Control Port Chip Select (SPI)** *(Input)* **-** AD0 is a chip address pin in I^2C mode; $\overline{CS}$ is the chip select signal in SPI mode.
INT	11	**Interrupt** *(Output)* - The CS42528 will generate an interrupt condition as per the Interrupt Mask register. See “Interrupts” on page 40 for more details.
RST	12	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
AINR- **AINR+**	13 14	**Differential Right Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
AINL+ **AINL-**	15 16	**Differential Left Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins.
VQ	17	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
REFGND	19	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
AOUTA1 +,- **AOUTB1 +,-** **AOUTA2 +,-** **AOUTB2 +,-** **AOUTA3 +,-** **AOUTB3 +,-** **AOUTA4 +,-** **AOUTB4 +,-**	36,37 35,34 32,33 31,30 28,29 27,26 22,23 21,20	**Differential Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
VA **VARX**	24 41	**Analog Power** (*Input*) - Positive power supply for the analog section.
AGND	25 40	**Analog Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MUTEC	38	**Mute Control** (*Output*) - The Mute Control pin outputs high impedance following an initial power-on condition or whenever the PDN bit is set to a ‘1’, forcing the codec into power-down mode. The signal will remain in a high impedance state as long as the part is in power-down mode. The Mute Control pin goes to the selected “active” state during reset, muting, or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
LPFLT	39	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and ground.
RXP7/GPO7 **RXP6/GPO6** **RXP5/GPO5** **RXP4/GPO4** **RXP3/GPO3** **RXP2/GPO2** **RXP1/GPO1**	42 43 44 45 46 47 48	**S/PDIF Receiver Input/ General Purpose Output** (*Input/Output*) - Receiver inputs for S/PDIF encoded data. The CS42528 has an internal 8:2 multiplexer to select the active receiver port, according to the Receiver Mode Control 2 register. These pins can also be configured as general purpose output pins, ADC Overflow indicators or Mute Control outputs according to the RXP/General Purpose Pin Control registers.
RXP0	49	**S/PDIF Receiver Input** (*Input*) - Dedicated receiver input for S/PDIF encoded data.
TXP	50	**S/PDIF Transmitter Output** (*Output*) - S/PDIF encoded data output, mapped directly from one of the receiver inputs as indicated by the Receiver Mode Control 2 register.
VLS	53	**Serial Port Interface Power** (*Input*) - Determines the required signal level for the serial port interfaces.
SAI_SDOUT	54	**Serial Audio Interface Serial Data Output** (*Output*) - Output for two’s complement serial audio PCM data from the S/PDIF incoming stream. This pin can also be configured to transmit the output of the internal and external ADCs.
RMCK	55	**Recovered Master Clock** (*Output*) - Recovered master clock output from the External Clock Reference (OMCK, pin 59) or the PLL which is locked to the incoming S/PDIF stream or CX_LRCK.

CX_SDOUT	56	**CODEC Serial Data Output** (*Output*) - Output for two's complement serial audio data from the internal and external ADCs.
ADCIN1 **ADCIN2**	58 57	**External ADC Serial Input** (*Input*) - The CS42528 provides for up to two external stereo analog to digital converter inputs to provide a maximum of six channels on one serial data output line when the CS42528 is placed in One Line mode.
OMCK	59	**External Reference Clock** (*Input*) - External clock reference that must be within the ranges specified in the register "OMCK Frequency (OMCK Freqx)" on page 54.
SAI_LRCK	60	**Serial Audio Interface Left/Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SAI_SCLK	61	**Serial Audio Interface Serial Clock** *(Input/Output)* - Serial clock for the Serial Audio Interface.

3. TYPICAL CONNECTION DIAGRAM



1. See the ADC Input Filter section in the Appendix.
2. See the DAC Output Filter section in the Appendix.
3. See the PLL Filter section in the Appendix.

Figure 5. Typical Connection Diagram

7. Package Pinout, 144-Pin QFP/LQFP

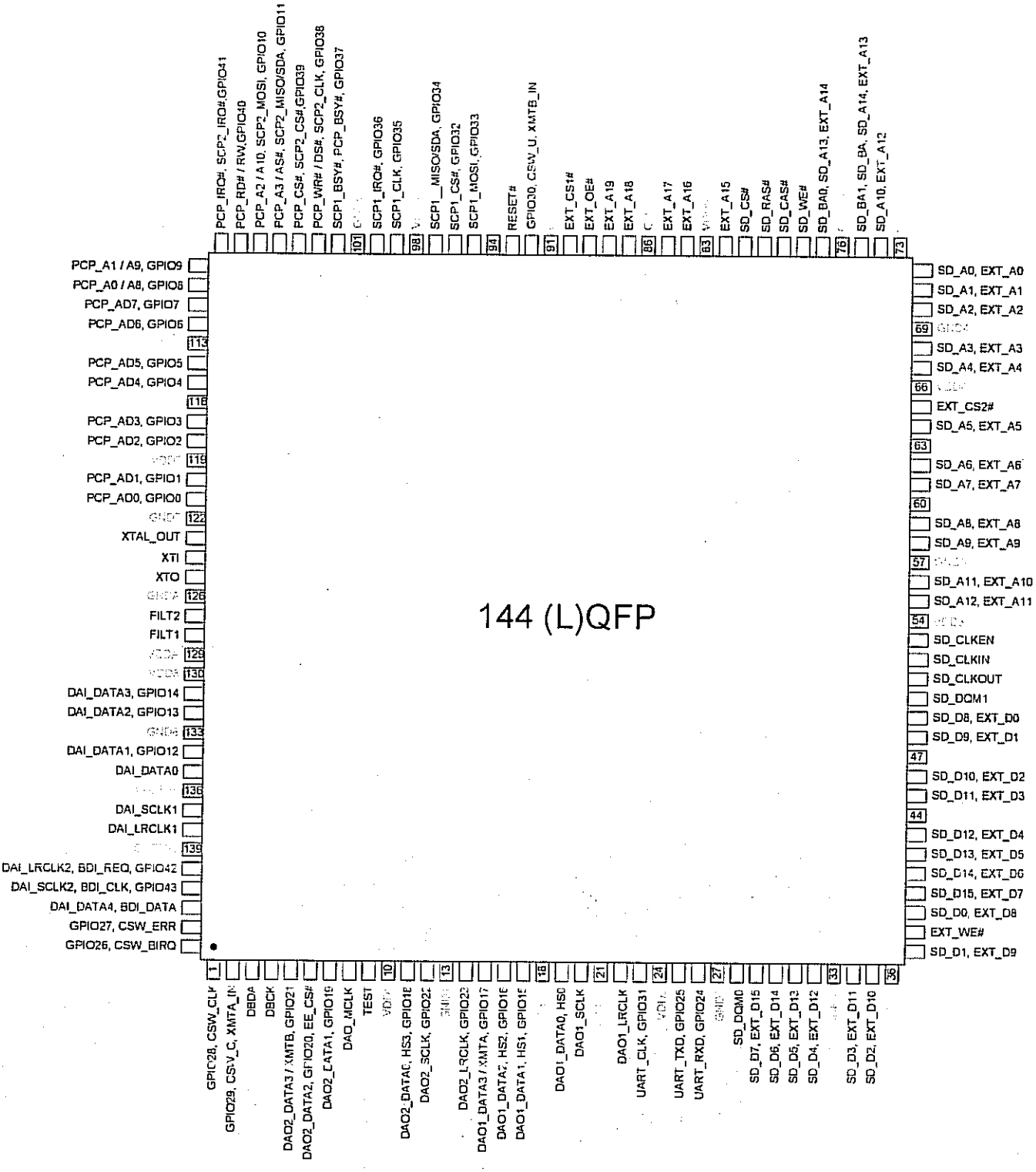
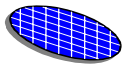


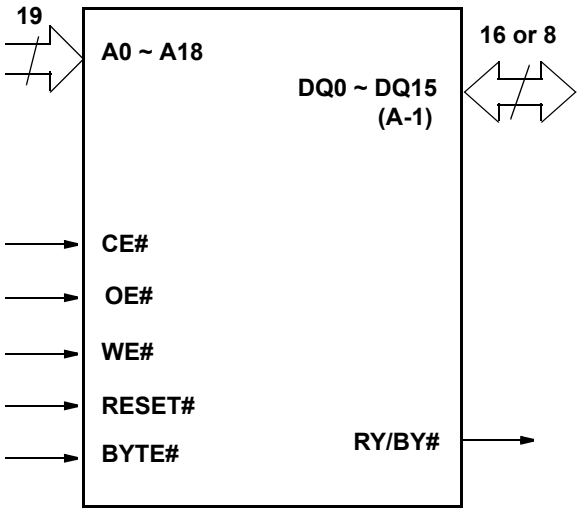
Figure 23. 144-Pin (L)QFP Package Pinout



PIN DESCRIPTION

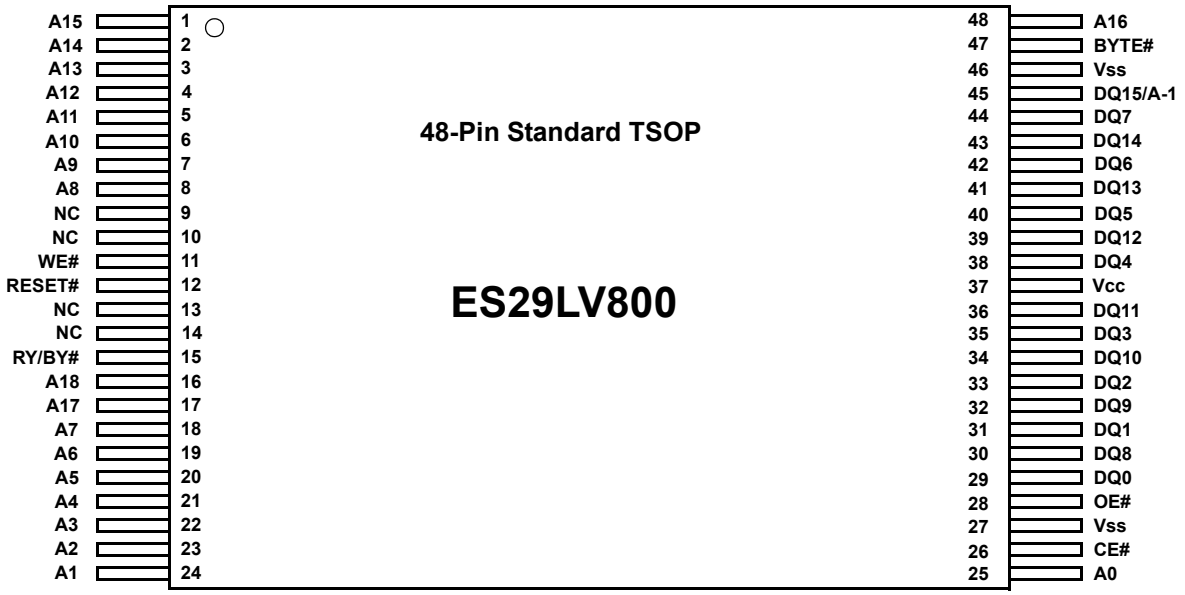
Pin	Description
A0-A18	19 Addresses
DQ0-DQ14	15 Data Inputs/Outputs
DQ15/A-1	DQ15 (Data Input/Output, Word Mode) A-1 (LSB Address Input, Byte Mode)
CE#	Chip Enable
OE#	Output Enable
WE#	Write Enable
RESET#	Hardware Reset Pin, Active Low
BYTE#	Selects 8-bit or 16-bit mode
RY/BY#	Ready/Busy Output
Vcc	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
Vss	Device Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL



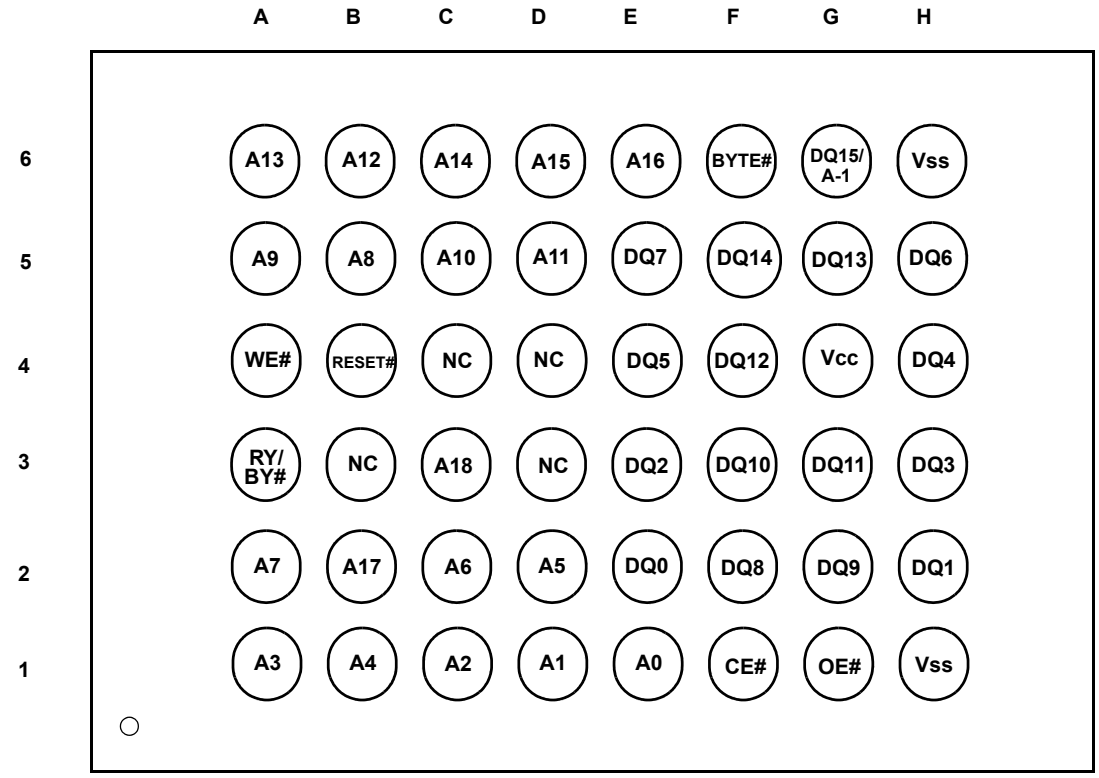
Excel Semiconductor inc.

CONNECTION DIAGRAM



48-Ball FBGA (6 x 8 mm)

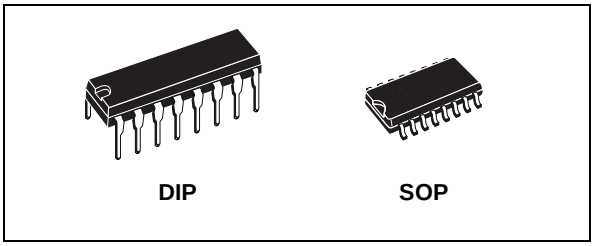
(Top View, Balls Facing Down)



HCF4053B

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

- LOW "ON" RESISTANCE : 125Ω (Typ.) OVER 15V p.p SIGNAL-INPUT RANGE FOR V_{DD} - V_{EE} = 15V
- HIGH "OFF" RESISTANCE : CHANNEL LEAKAGE ± 100pA (Typ.) at V_{DD} - V_{EE} = 18V
- BINARY ADDRESS DECODING ON CHIP
- HIGH DEGREE OF LINEARITY : < 0.5% DISTORTION TYP. at f_{IS} = 1KHz, V_{IS} = 5 V_{pp}, V_{DD} - V_{SS} ≥ 10V, RL = 10KΩ
- VERY LOW QUIESCENT POWER DISSIPATION UNDER ALL DIGITAL CONTROL INPUT AND SUPPLY CONDITIONS : 0.2 μW (Typ.) at V_{DD} - V_{SS} = V_{DD} - V_{EE} =10V
- MATCHED SWITCH CHARACTERISTICS : R_{ON} = 5Ω (Typ.) FOR V_{DD} - V_{EE} = 15V
- WIDE RANGE OF DIGITAL AND ANALOG SIGNAL LEVELS : DIGITAL 3 to 20, ANALOG TO 20V p.p.
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



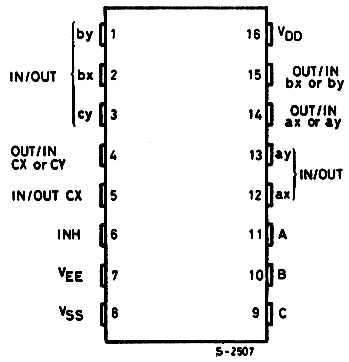
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4053BEY	
SOP	HCF4053BM1	HCF4053M013TR

DESCRIPTION

The HCF4053B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
The HCF4053B analog multiplexer/demultiplexer is a digitally controlled analog switch having low ON impedance and very low OFF leakage current. This multiplexer circuit dissipate extremely low quiescent power over the full V_{DD} - V_{SS} and V_{DD} - V_{EE} supply voltage range, independent of the logic state of the control signals.
When a logic "1" is present at the inhibit input terminal all channel are off. This device is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single pole double-throw configuration.

PIN CONNECTION



October 2002

ANODE CONNECTION

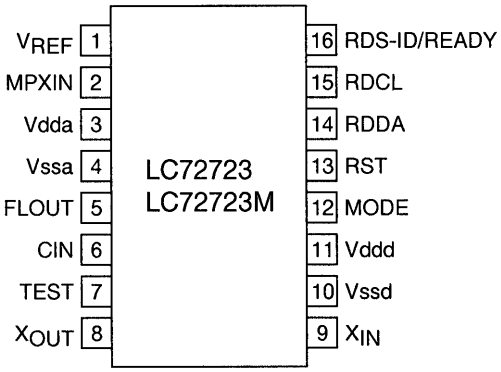
	COM1	COM2	COM3	~	COM16	COM17	COM18
	1G	2G	3G	~	16G	17G	18G
SEGB 1	☐(DIGITAL EX)	☐(LOGIC 7)	1	1	1	B1	☐(VID 1)
SEGB 2			2	2	2	B2	VID 1
SEGB 3			3	3	3	L	☐(DVD 12)
SEGB 4			4	4	4	B3	DVD
SEGB 5			5	5	5	B4	1
SEGB 6	DIGITAL	LOGIC 7	6	6	6	B5	2
SEGB 7			7	7	7	C	☐(VID 2)
SEGB 8			8	8	8	B6	VID 2
SEGB 9			9	9	9	B7	☐(CD)
SEGB10			10	10	10	B8	CD
SEGB11	EX	☐(VMAx)	11	11	11	R	☐(VID 3)
SEGB12			12	12	12	B9	VID 3
SEGB13			13	13	13	B10	☐(FM AM)
SEGB14			14	14	14	LFE	FM
SEGB15			15	15	15	B11	AM
SEGB16	☐(PRO LOGIC)	VMAx	16	16	16	B12	☐(VID 4)
SEGB17			17	17	17	SL	VID 4
SEGB18			18	18	18	B13	☐(TAPE)
SEGB19			19	19	19		TAPE
SEGB20			20	20	20	B14	☐(VID 5)
SEGB21	PRO LOGIC	☐(DSP)	21	21	21	B15	VID 5
SEGB22			22	22	22	SR	☐(6.8CH)
SEGB23			23	23	23	B16	6
SEGB24			24	24	24	B17	8
SEGB25			25	25	25	B18	CH
SEGB26	II	DSP	26	26	26	SBL	
SEGB27			27	27	27	B19	
SEGB28			28	28	28	—	
SEGB29			29	29	29	B20	
SEGB30			30	30	30	B21	
SEGB31	☐(3 STEREO)	☐(5.7CH.)	31	31	31	SBR	
SEGB32			32	32	32	B22	
SEGB33			33	33	33		
SEGB34			34	34	34		
SEGB35			35	35	35		

	COM1	COM2	COM3	~	COM16	COM17	COM18
	1G	2G	3G	~	16G	17G	18G
SEGA 1		5	36	36	36		
SEGA 2			37	37	37		
SEGA 3			38	38	38		
SEGA 4			39	39	39		
SEGA 5			40	40	40		
SEGA 6	3	7	41	41	41		
SEGA 7			42	42	42		
SEGA 8			43	43	43		
SEGA 9			44	44	44		
SEGA 10			45	45	45		
SEGA 11	STEREO	CH. STEREO	46	46	46		
SEGA 12			47	47	47		
SEGA 13			48	48	48		
SEGA 14			49	49	49		
SEGA 15			50	50	50		
SEGA 16	☐(HEADPHONE)	☐(SURR.OFF)	51	51	51		
SEGA 17			52	52	52		
SEGA 18			53	53	53		
SEGA 19			54	54	54		
SEGA 20			55	55	55		
SEGA 21	HEADPHONE	SURR. OFF	56	56	56		
SEGA 22			57	57	57		
SEGA 23			58	58	58		
SEGA 24			59	59	59		
SEGA 25			60	60	60		
SEGA 26	☐(DTS,ES)		61	61	61		
SEGA 27			62	62	62		
SEGA 28			63	63	63		
SEGA 29			64	64	64		
SEGA 30			65	65	65		
SEGA 31			66	66	66		
SEGA 32			67	67	67		
SEGA 33			68	68	68		
SEGA 34			69	69	69		
SEGA 35			70	70	70		

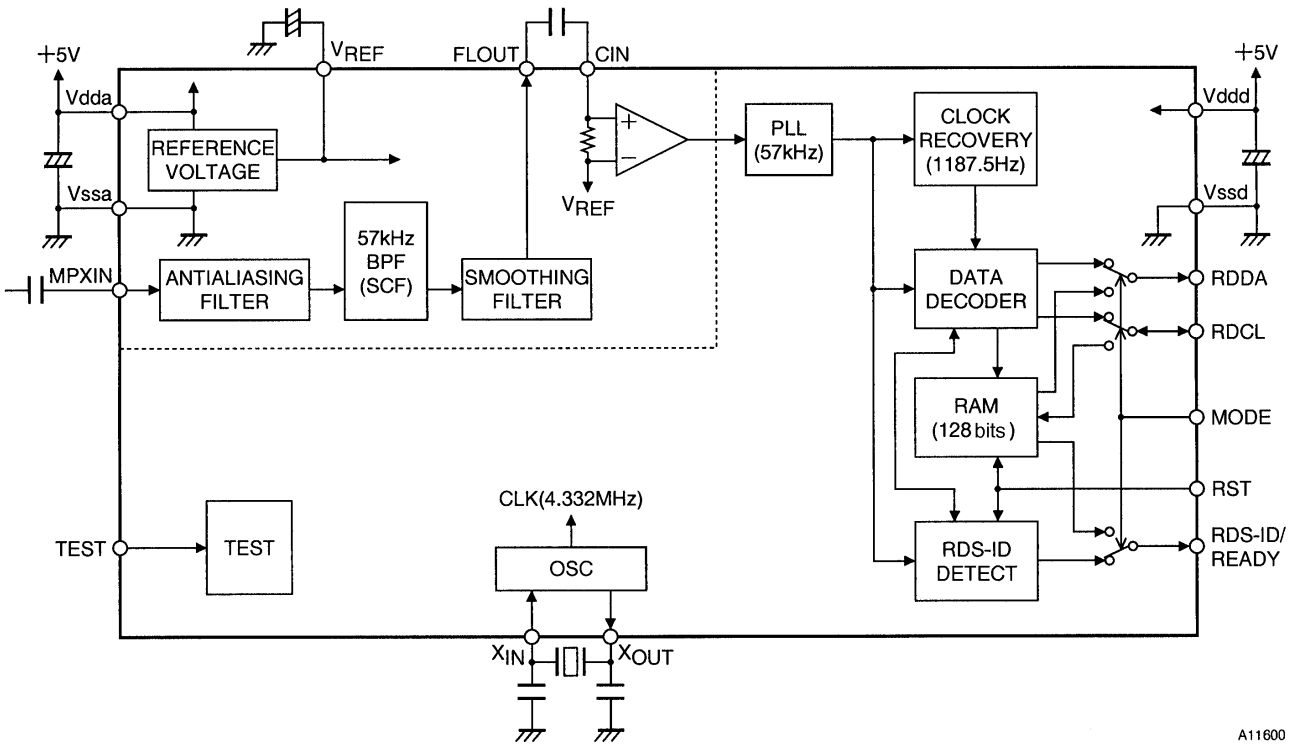
MODEL : HCA-18LM03
ANODE CONNECTION
Rev.(1) 20-Jan-2005

LC72723, LC72723M

Pin Assignment (DIP16/MFP16)

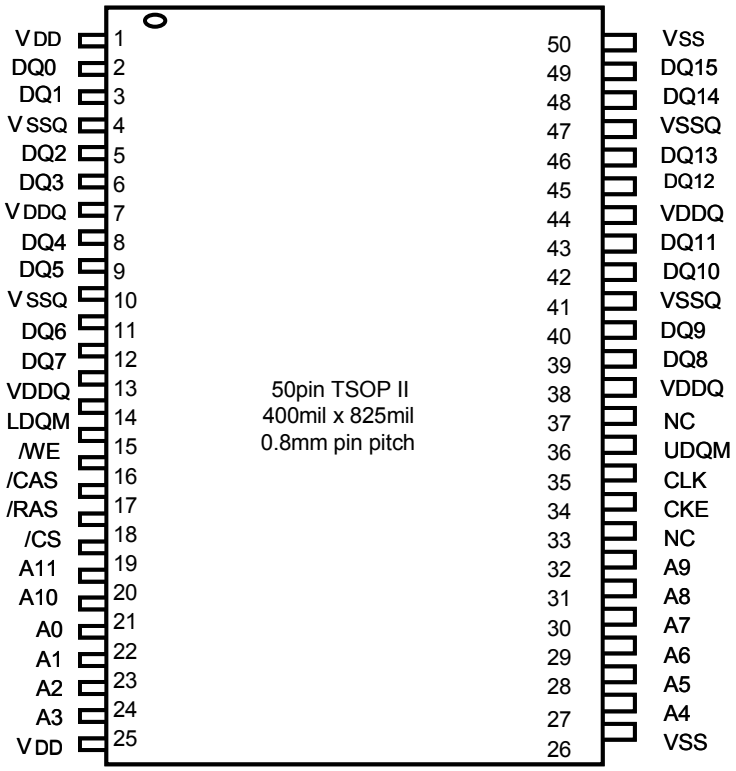


Block Diagram



hynix

PIN CONFIGURATION



PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are referenced to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh.
$\overline{CS}$	Chip Select	Command input enable or mask except CLK, CKE and DQM
BA	Bank Address	Select either one of banks during both $\overline{RAS}$ and $\overline{CAS}$ activity.
A0 ~ A10	Address	Row Address : RA0 ~ RA10, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation. Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	DQM control output buffer in read mode and mask input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuit and input buffer
VDDQ/VSSQ	Data Output Power/Ground	Power supply for DQ
NC	No Connection	No connection

KEC

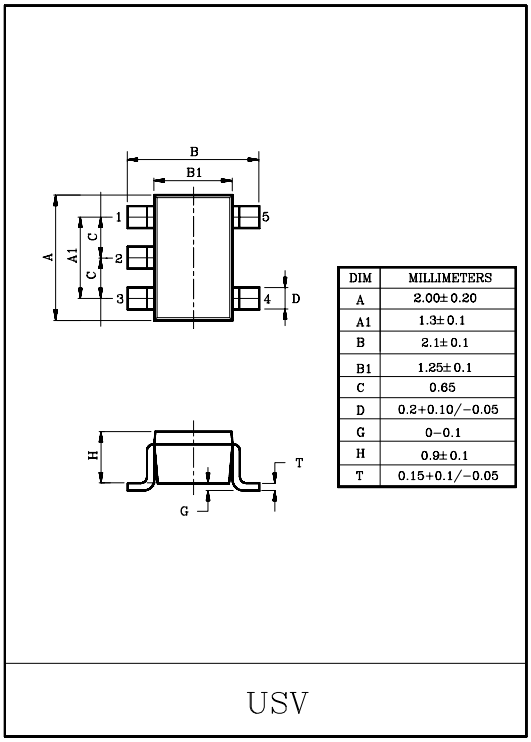
SEMICONDUCTOR
TECHNICAL DATA

KIC7SZ08FU
SILICON MONOLITHIC CMOS
DIGITAL INTEGRATED CIRCUIT

2 INPUT AND GATE

FEATURES

- High Output Drive : ±24mA (Typ.)
  @V_{CC}=3V
- Super High Speed Operation : t_{PD}=2.7ns(Typ.)
  @V_{CC}=5V, 50pF
- Operation Voltage Range : $V_{CC(opr)}$=1.8~5.5V.
- Supply Voltage Data Retention : V_{CC}=1.5~5.5V.
- 5V Tolerant Function



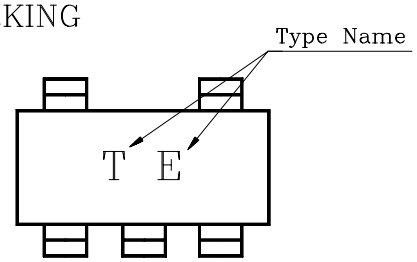
DIM	MILLIMETERS
A	2.00± 0.20
A1	1.3± 0.1
B	2.1± 0.1
B1	1.25± 0.1
C	0.65
D	0.2+0.10/−0.05
G	0~0.1
H	0.9± 0.1
T	0.15+0.1/−0.05

USV

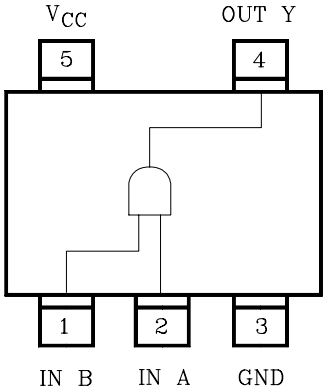
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~6	V
DC Input Voltage	V_{IN}	-0.5~6	V
DC Output Voltage	V_{OUT}	-0.5~6	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	200	mW
Storage Temperature	T_{stg}	-65~150	℃
Lead Temperature (10s)	T_L	260	℃

MARKING



PIN CONNECTION(TOP VIEW)



cosmo

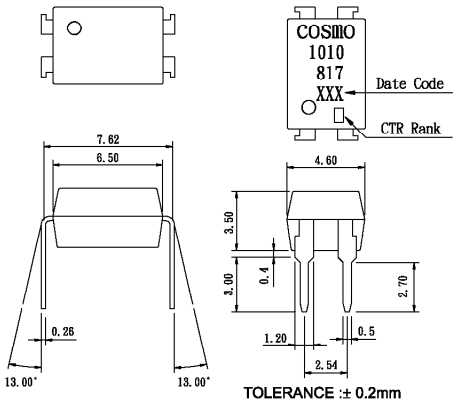
High Reliability Photo Coupler K1010

UL 1577 (File No.E169586) VDE 0884 / 0860 / 0805 (File No.101347)

Features

1. Current transfer ratio
   (CTR:MIN.50% at IF=5mA Vce=5V)
2. High isolation voltage between input and output
   (Viso:5000Vrms).
3. Compact dual-in-line package.
4. Available package : DIP/ SMD/ H.

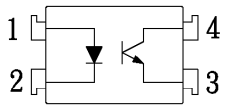
Outside Dimension : Unit (mm)



Applications

1. Registers, copiers, automatic vending machines.
2. System appliances, measuring instruments.
3. Computer terminals, programmable controllers.
4. Communications, telephone, etc.
5. Electric home appliances, such as oil fan heaters, Microwave oven, Washer, Refrigerator, Air conditioner, etc.
6. Medical instruments, physical and chemical equipment.
7. Signal transmission between circuits of different potentials and impedances.
8. Facsimile equipment, Audio, Video.
9. Switching power supply, Laser beam printer.

Schematic : Top View



1. Anode
2. Cathode
3. Emitter
4. Collector

Absolute Maximum Ratings

(Ta=25°C)

	Parameter	Symbol	Rating	Unit
Input	Forward current	IF	50	mA
	Peak forward current	IFM	1	A
	Reverse voltage	VR	6	V
	Power dissipation	PD	70	mW
Output	Collector-emitter voltage	VCEO	60	V
	Emitter-collector voltage	VECO	6	V
	Collector current	IC	50	mA
	Collector power dissipation	PC	150	mW
	Total power dissipation	Ptot	200	mW
	Isolation voltage 1 minute	Viso	5000	Vrms
	Operating temperature	Topr	-30 to +100	°C
	Storage temperature	Tstg	-55 to +125	°C
	Soldering temperature 10 second	Tsol	260	°C

Electro-optical Characteristics

(Ta=25°C)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input	Forward voltage	VF	IF =20mA	—	1.2	1.4	V
	Peak forward voltage	VFM	IFM =0.5A	—	—	3.0	V
	Reverse current	IR	VR =4V	—	—	10	uA
	Terminal capacitance	Ct	V=0, f=1kHz	—	30	—	pF
Output	Collector dark current	ICEO	VCE =20V	—	—	0.1	uA
Transfer charac-teristics	Current transfer ratio	CTR	IF=5mA, VCE =5V	50	—	600	%
	Collector-emitter saturation voltage	VCE(sat)	IF=20mA, IC=1mA	—	0.1	0.2	V
	Isolation resistance	Riso	DC500V	$5X10^{10}$	10^{11}	—	ohm
	Floating capacitance	Cf	V=0, f=1MHz	—	0.6	1.0	pF
	Cut-off frequency	fc	VCC=5V, IC=2mA, RL=100ohm	—	80	—	kHz
	Response time(Rise)	tr	VCE=2V, IC=2mA, RL=100ohm	—	4	18	us
	Response time(Fall)	tf		—	3	18	us

KEC KOREA ELECTRONICS CO.,LTD.

SEMICONDUCTOR TECHNICAL DATA

KTD600K

EPITAXIAL PLANAR NPN TRANSISTOR

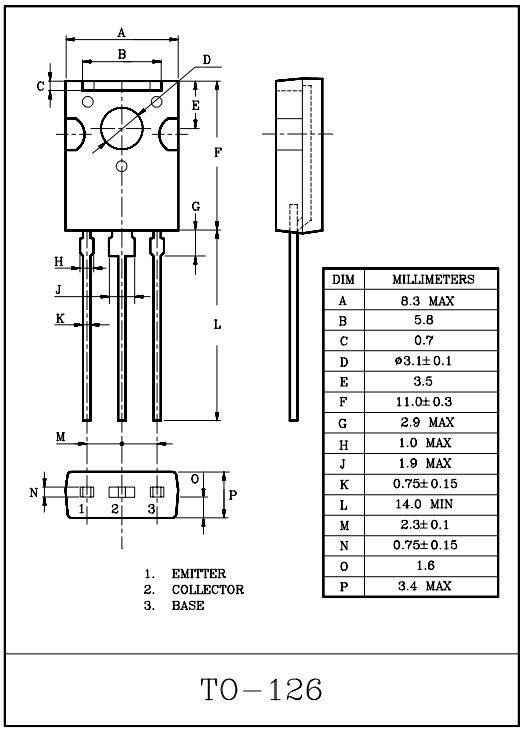
LOW FREQUENCY POWER AMP,
MEDIUM SPEED SWITCHING APPLICATIONS

FEATURES

- High breakdown voltage V_{CEO} 120V, high current 1A.
- Low saturation voltage and good linearity of h_{FE}.

MAXIMUM RATINGS (Ta=25℃)

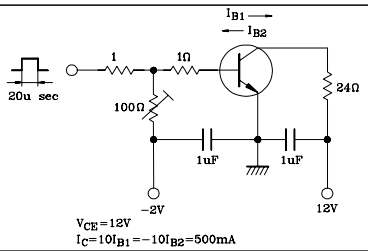
CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector-Base Voltage		V_{CBO}	120	V
Collector-Emitter Voltage		V_{CEO}	120	V
Emitter-Base Voltage		V_{EBO}	5	V
Collector Current		I_C	1	A
		I_{CP}	2	
Collector Power Dissipation	Ta=25℃	P_C	1.5	W
	Tc=25℃		8	
Junction Temperature		T_j	150	℃
Storage Temperature Range		T_{stg}	-55~150	℃



DIM	MILLIMETERS
A	8.3 MAX
B	5.8
C	0.7
D	ø3.1±0.1
E	3.5
F	11.0±0.3
G	2.9 MAX
H	1.0 MAX
J	1.9 MAX
K	0.75±0.15
L	14.0 MIN
M	2.3±0.1
N	0.75±0.15
O	1.6
P	3.4 MAX

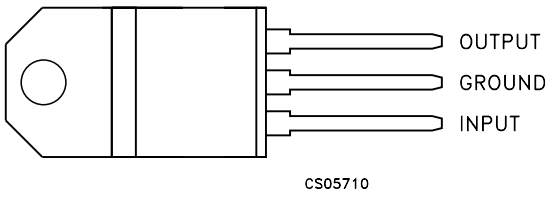
TO-126

ELECTRICAL CHARACTERISTICS (Ta=25℃)

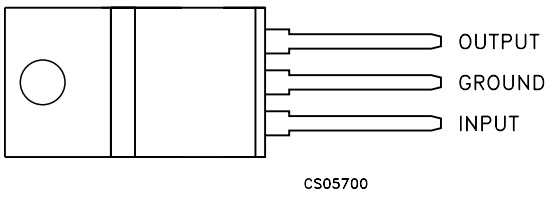
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut of Current		I_{CBO}	V_{CB}=50V, I_E=0	-	-	1	μA
Emitter Cut of Current		I_{EBO}	V_{EB}=4V, I_C=0	-	-	1	μA
Collector-Base Breakdown Voltage		$V_{(BR)CBO}$	I_C=10μA	120	-	-	V
Collector-Emitter Breakdown Voltage		$V_{(BR)CEO}$	I_C=1mA	120	-	-	V
Emitter-Base Breakdown Voltage		$V_{(BR)EBO}$	I_E=10μA	5	-	-	V
DC Current Gain		h_{FE}(1)Note	V_{CE}=5V, I_C=50mA	100	-	320	
		h_{FE}(2)	V_{CE}=5V, I_C=500mA	20	-	-	
Gain Bandwidth Product		f_T	V_{CE}=10V, I_C=50mA	-	130	-	MHz
Output Capacitance		C_{ob}	V_{CB}=10V, f=1MHz	-	20	-	pF
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	I_C=500mA, I_B=50mA	-	0.15	0.4	V
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	I_C=500mA, I_B=50mA	-	0.85	1.2	V
Switching Time	Turn-on Time	t_{on}		-	100	-	nS
	Turn-off Time	t_{off}		-	500	-	
	Storage Time	t_{stg}		-	700	-	

(Note) : h_{FE}(1) Classification Y:100~200, GR:160~320

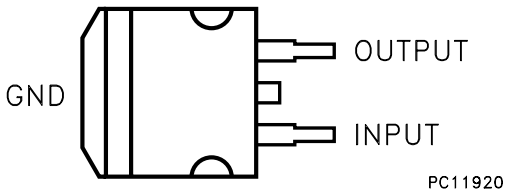
Figure 3: Connection Diagram (top view)



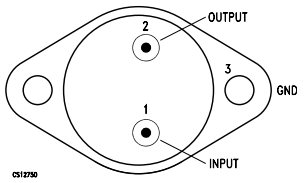
TO-220 (Any Type)



TO-220FP/TO-220FM



D^2PAK (Any Type)



TO-3

Table 3: Order Codes

TYPE	TO-220 (A Type)	TO-220 (C Type)	TO-220 (E Type)	D^2PAK (A Type) (*)	D^2PAK (C Type) (T & R)	TO-220FP	TO-220FM	TO-3
L7805								L7805T
L7805C	L7805CV	L7805C-V	L7805CV1	L7805CD2T	L7805C-D2TR	L7805CP	L7805CF	L7805CT
L7852C	L7852CV			L7852CD2T		L7852CP	L7852CF	L7852CT
L7806								L7806T
L7806C	L7806CV	L7806C-V		L7806CD2T		L7806CP	L7806CF	L7806CT
L7808								L7808T
L7808C	L7808CV	L7808C-V		L7808CD2T		L7808CP	L7808CF	L7808CT
L7885C	L7885CV			L7885CD2T		L7885CP	L7885CF	L7885CT
L7809C	L7809CV	L7809C-V		L7809CD2T		L7809CP	L7809CF	L7809CT
L7810C	L7810CV			L7810CD2T		L7810CP		
L7812								L7812T
L7812C	L7812CV	L7812C-V		L7812CD2T		L7812CP	L7812CF	L7812CT
L7815								L7815T
L7815C	L7815CV	L7815C-V		L7815CD2T		L7815CP	L7815CF	L7815CT
L7818								L7818T
L7818C	L7818CV			L7818CD2T		L7818CP	L7818CF	L7818CT
L7820								L7820T
L7820C	L7820CV			L7820CD2T		L7820CP	L7820CF	L7820CT
L7824								L7824T
L7824C	L7824CV			L7824CD2T		L7824CP	L7824CF	L7824CT

(*) Available in Tape & Reel with the suffix "-TR".

L7900

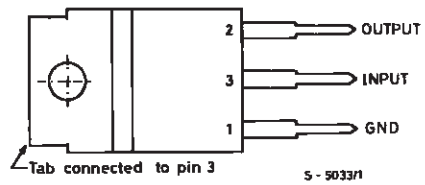
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (for V_O = 5 to 18V) (for V_O = 20, 24V)	-35 -40	V V
I_o	Output Current	Internally limited	
P_{tot}	Power Dissipation	Internally limited	
T_{op}	Operating Junction Temperature Range	0 to 150	°C
T_{stg}	Storage Temperature Range	- 65 to 150	°C

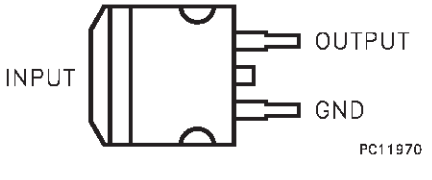
THERMAL DATA

Symbol	Parameter		D^2PAK	TO-220	ISOWATT220	TO-3	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	3	3	4	4	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	50	60	35	°C/W

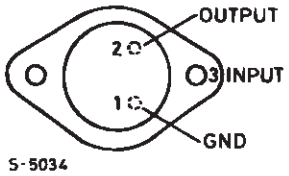
CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)



TO-220 & ISOWATT220



D^2PAK

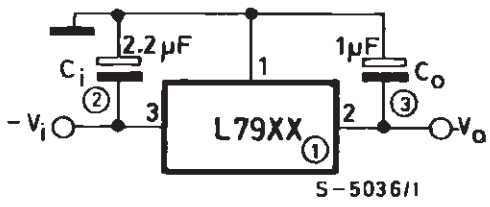


TO-3

Type	TO-220	D^2PAK (*)	ISOWATT220	TO-3	Output Voltage
L7905C	L7905CV	L7905CD2T	L7905CP	L7905CT	-5V
L7952C	L7952CV	L7952CD2T		L7952CT	-5.2V
L7906C	L7906CV	L7906CD2T	L7906CP	L7906CT	-6V
L7908C	L7908CV	L7908CD2T	L7908CP	L7908CT	-8V
L7912C	L7912CV	L7912CD2T	L7912CP	L7912CT	-12V
L7915C	L7915CV	L7915CD2T	L7915CP	L7915CT	-15V
L7918C	L7918CV	L7918CD2T	L7918CP	L7918CT	-18V
L7920C	L7920CV	L7920CD2T	L7920CP	L7920CT	-20V
L7922C	L7922CV	L7922CD2T		L7922CT	-22V
L7924C	L7924CV	L7924CD2T	L7924CP	L7924CT	-24V

(*) AVAILABLE IN TAPE AND REEL WITH "-TR" SUFFIX

APPLICATION CIRCUIT

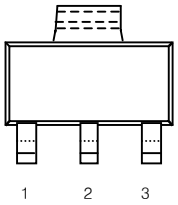


1A LOWDROP OUT VOLTAGE REGULATOR (ADJUSTABLE & FIXED) LM1117

FEATURES

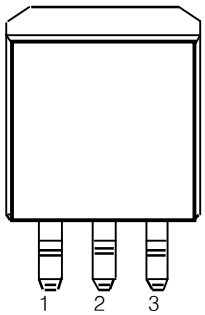
- Output Current up to 1 A
- Low Dropout Voltage (700mV at 1A Output Current)
- Three Terminal Adjustable or Fixed 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V
- 2.85V Device for SCSI-II Active Terminator
- 0.04% Line Regulaion, 0.1% Load Regulation
- Very Low Quiescent Current
- Internal Current andTerminal Limit
- Logic-Controlled Electronics Shutdown
- Surface Mount Package SOT-223 & TO-263 (D2-Pack)
- 100% Thermal Limit Burn-In

SOT-223 PKG (FRONT VIEW)



PIN FUNCTION
1. Adj/Gnd
2. Vout
3. Vin

TO-263 (D2 PKG, FRONT VIEW)



PIN FUNCTION
1. Adj/Gnd
2. Vout
3. Vin

APPLICATION

- Active SCSI Terminators
- Portable/Plan Top/Notebook Computers
- High Efficiency Linear Regulators
- SMPS Post Regulators
- Mother B/D Clock Supplies
- Disk Drives
- Battery Chargers

ORDERING INFORMATION

Device (Marking)	Package
LM1117S	SOT-223
LM1117S-XX	
LM1117T	TO-263 (D2)
LM1117T-XX	

(X=Output Voltage=1.5V, 1.8V, 2.5V, 2.85V, '3.0V, 3.3V, 5.0V, Adjustable=AD)

DESCRIPTION

The LM1117 is a low power positive-voltage regulator designed to meet 1A output current and comply with SCSI-II specifications with a fixed output voltage of 2.85V. This device is an excellent choice for use in battery-powered applications, as active terminators for the SCSI bus, and portable computers.
The LM1117 features very low quiescent current and very low dropout voltage of 700mV at a full load and lower as output current decreases. LM1117 is available as an adjustable or fixed 1.5V, 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, and 5.0V output voltages.
The LM1117 is offered in a 3-pin surface mount package SOT-223 & TO-263. The output capacitor of 10μF or larger is needed for output stability of LM1117 as required by most of the other regulator circuits.

ABSOLUTE MAXIMUM RATINGS

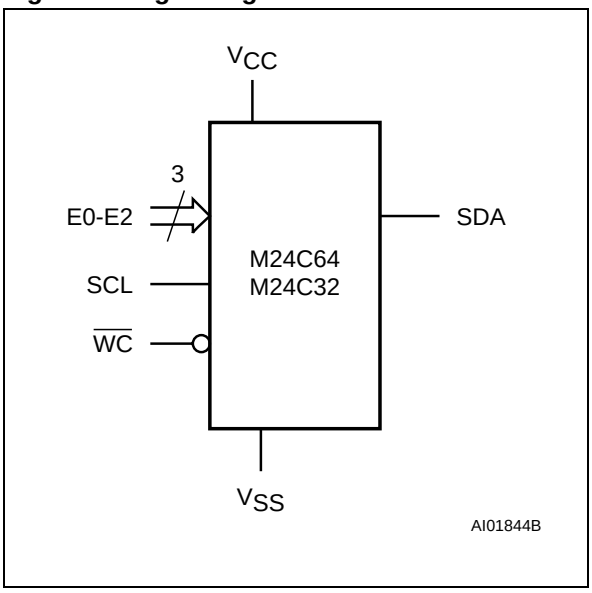
CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
DC Input Voltage	V_{IN}		7	V
Lead Temperature (Soldering, 5 Seconds)	T_{SOL}		260	℃
Storage Temperature Range	T_{STG}	-65	150	℃
Operating Junction Temperature Range	T_{OPR}	0	125	℃

HTC

SUMMARY DESCRIPTION

These I^2C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 8192 x 8 bits (M24C64) and 4096 x 8 bits (M24C32).

Figure 2. Logic Diagram



I^2C uses a two-wire serial interface, comprising a bi-directional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a Device Select Code and Read/Write bit (RW) (as described in Table 3.), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Table 2. Signal Names

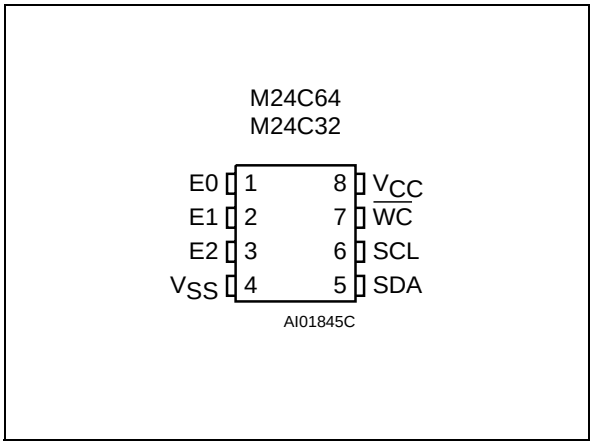
E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. At Power-up, the internal reset is held active until V_{CC} has reached the Power On Reset (POR) threshold voltage, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the Power On Reset (POR) threshold voltage, all operations are disabled and the device will not respond to any command.

A stable and valid V_{CC} (as defined in Table 9. and Table 10.) must be applied before applying any logic signal.

Figure 3. DIP, SO, TSSOP and UFDFPN Connections



Note: See PACKAGE MECHANICAL section for package dimensions, and how to identify pin-1.

FAIRCHILD SEMICONDUCTOR®

www.fairchildsemi.com

MC78XX/LM78XX/MC78XXA

3-Terminal 1A Positive Voltage Regulator

Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

TO-220

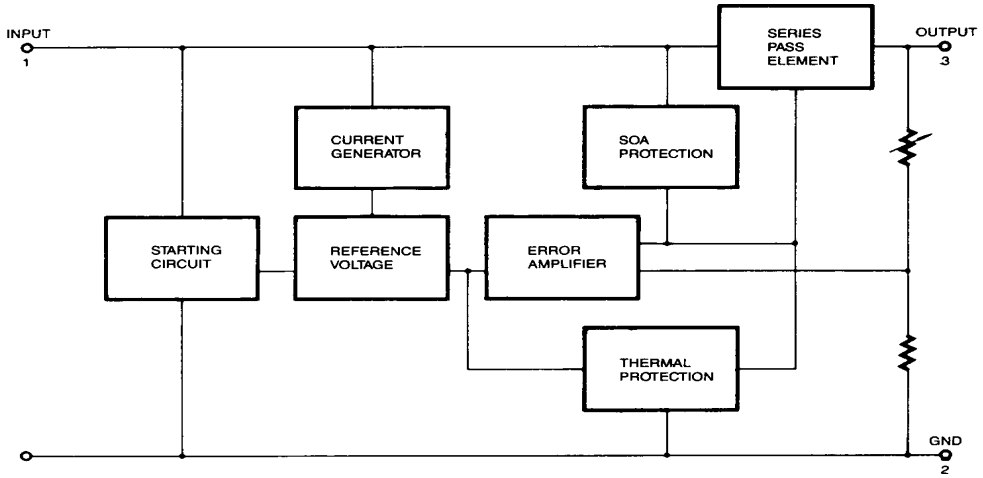
1

D-PAK

1

1. Input 2. GND 3. Output

Internal Block Digram



Rev. 1.0.1

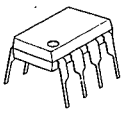
JRC **NJM2068**

LOW-NOISE DUAL OPERATIONAL AMPLIFIER

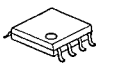
■ GENERAL DESCRIPTION

The NJM2068 is a high performance, low noise dual operational amplifier. This amplifier features popular pin-out, superior noise performance, and superior total harmonic distortion. This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product and slew rate which far exceeds that of the 4558 type amplifier. The specially designed low noise input transistors allow the NJM2068 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifier.

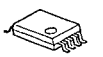
■ PACKAGE OUTLINE



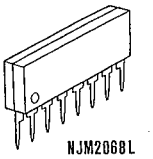
NJM2068D



NJM2068M



NJM2068V



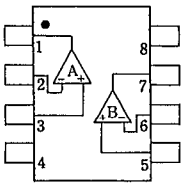
NJM2068L

■ FEATURES

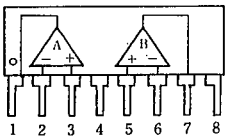
- Operating Voltage (±4V~±18V)
- Low Total Harmonic Distortion (0.001% typ.)
- Low Noise Voltage (FLAT+JISA, 0.56 μV typ.)
- High Slew Rate (6V/μs typ.)
- Unity Gain Bandwidth (27MHz @f=10kHz)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

4

■ PIN CONFIGURATION



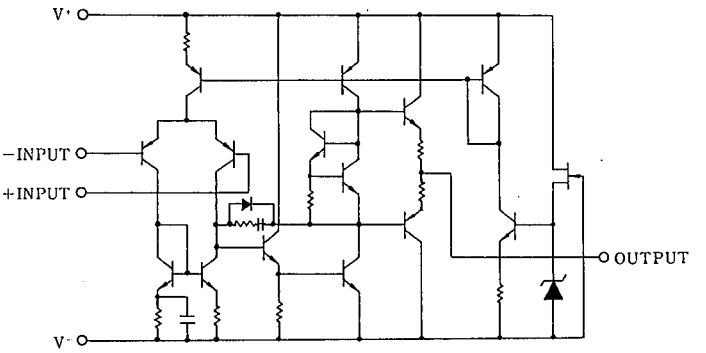
NJM2068D
NJM2068M
NJM2068V



NJM2068L

PIN FUNCITON
1. A OUTPUT
2. A−INPUT
3. A+INPUT
4. V⁻
5. B+INPUT
6. B−INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



JRC

NJM2137

ULTRA WIDE BAND, HIGH SLUE RATE DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2137 is an ultra wide band, high slew rate dual operational amplifier operated from low voltage (±1.35V).

It can apply to active filter, high speed analog and digital signal processor, line driver, HDTV, industrial measurement equipment and others.

It can also apply to portable communication items because of low operating voltage and low operating current.

■ PACKAGE OUTLINE

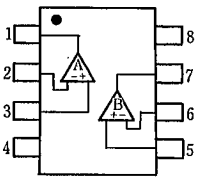
NJM2137V

NJM2137M

■ FEATURES

- Operating Voltage (±1.35V ~ ±6V)
- Ultra Wide Band (200MHz typ.)
- High Slew Rate (45V/μs typ.)
- Low Operating Current (1.14mA typ.)
- Bipolar Technology
- Package Outline SSOP8, DMP8

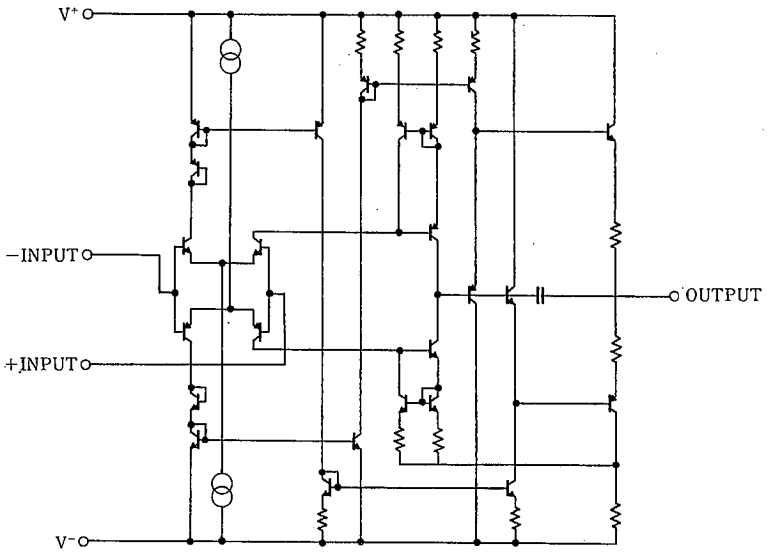
■ PIN CONFIGURATION



NJM2137M
NJM2137V

PIN FUNCTION
1. A OUTPUT
2. A −INPUT
3. A +INPUT
4. V⁻
5. B +INPUT
6. B −INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



JRC **NJM2391**

LOW DROPOUT VOLTAGE REGULATOR

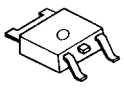
■ GENERAL DESCRIPTION

The NJM2391 is low dropout voltage regulators featuring high precision voltage.

It is suitable for Notebook PCs, PC cards and hard disks where 3.3V need to be generated from 5V supply.

A small TO-252 package is adopted for the space saving.

■ PACKAGE OUTLINE

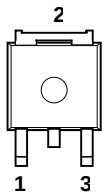


NJM2391DL1

■ FEATURES

- ●Output Current Io(max.)=1A
- ●High Precision Output Voltage Vo±1%
- ●Low Dropout Voltage ΔV_{I-O} =1.1V typ. At Io=1A
- ●Internal Excessive Voltage Protection Circuit
- ●Internal Short Circuit Current Limit
- ●Internal Thermal Overload Protection
- ●Bipolar Technology
- ●Package Outline TO-252

■ PIN CONFIGURATION



PIN FUNCTION
1.V_{IN}
2.GND
3.V_{OUT}

NJM2391DL1

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V^+	+10	V
Power Dissipation	P_D	TO-252 8 (Tc=25°C) 0.8(Ta≤25°C)	W
Operating Temperature	Topr	–40 ~ +85	°C
Storage Temperature	Tstg	–50 ~ +125	°C

■ OUTPUT VOLTAGE RANK LIST

Device Name	V_{OUT}
NJM2391DL1-25	2.5V
NJM2391DL1-26	2.6V
NJM2391DL1-28	2.85V
NJM2391DL1-03	3.0V
NJM2391DL1-33	3.3V
NJM2391DL1-35	3.5V
NJM2391DL1-05	5.0V

JRC **NJM2595**

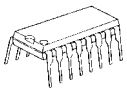
5-INPUT 3-OUTPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

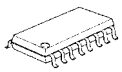
The **NJM2595** is a 5-input 3-output video switch. Its switches select one from five signals received from VTR,TV,DVD, TV-GAME and others.

The NJM2595 is designed for audio items, such as AV amplifier and others.

■ PACKAGE OUTLINE



NJM2595D

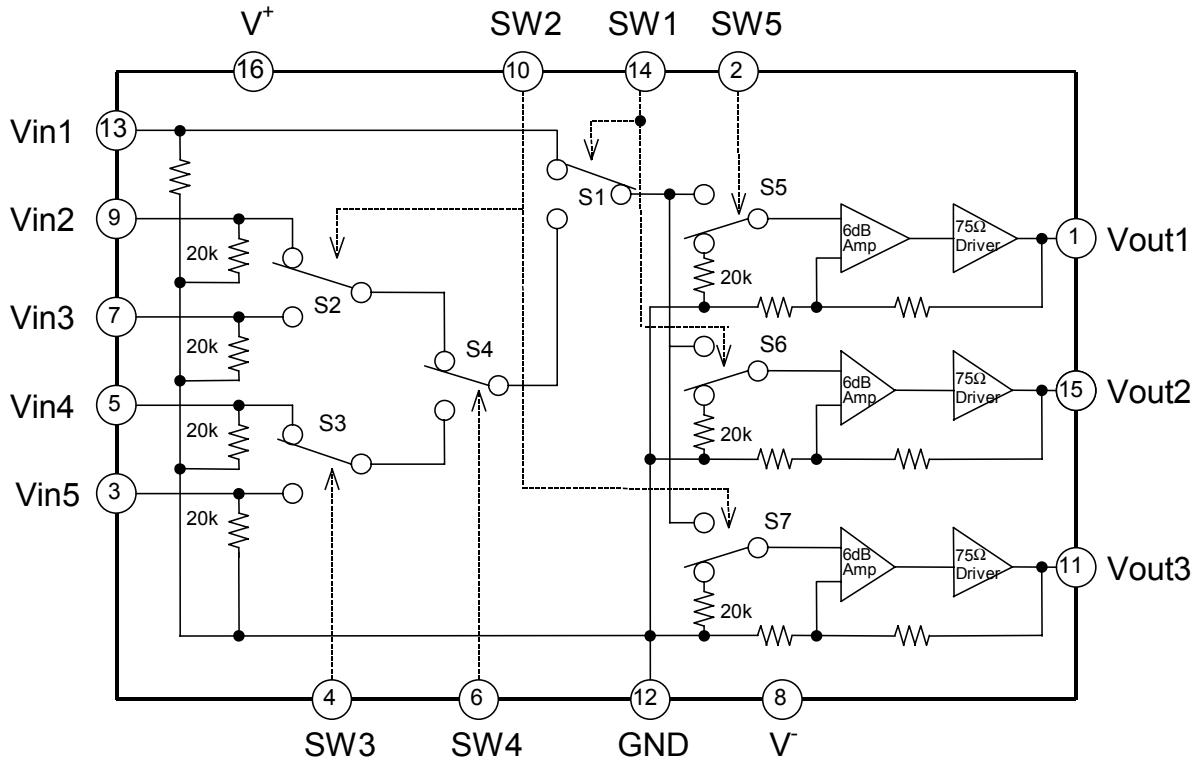


NJM2595M

■ FEATURES

- 5-input 3-output
- Operating Voltage ±4.0 to ±6.5V
- Operating current ±15mAtyp. at Vcc=±5V
- Crosstalk -65dBtyp.
- Internal 6dB Amplifier
- Internal 75Ω Driver
- Bipolar Technology
- Package Outline DIP16,DMP16

■ PIN CONFIGURATION and BLOCK DIAGRAM



JRC **NJM2845/46**

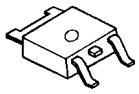
LOW DROPOUT VOLTAGE REGULATOR

■ GENERAL DESCRIPTION

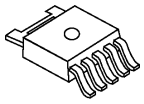
The NJM2845 is low dropout voltage regulator. Advanced Bipolar technology achieves low noise, high ripple rejection and low quiescent current.

NJM2845 is 3 terminal type and NJM2846 is ON/OFF control built in type. These product can be selected according to the applications.

■ PACKAGE OUTLINE



NJM2845DL1

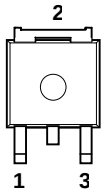


NJM2846DL3

■ FEATURES

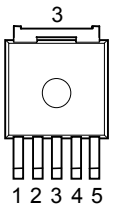
- ● High Ripple Rejection 75dB typ. (f=1kHz,3V Version)
- ● Output Noise Voltage Vno=45μVrms typ. (Vo=3V Version)
- ● Output capacitor with 2.2μF ceramic capacitor (Vo≥2.6V)
- ● Output Current Io(max.)=800mA
- ● High Precision Output Vo ±1.0%
- ● Low Dropout Voltage 0.18V typ. (Io=500mA)
- ● ON/OFF Control (NJM2846)
- ● Internal Short Circuit Current Limit
- ● Internal Thermal Overload Protection
- ● Bipolar Technology
- ● Package Outline TO-252-3 (NJM2845DL1), TO-252-5 (NJM2846DL3)

■ PIN CONFIGURATION



1.V_{IN}
2.GND
3.V_{OUT}

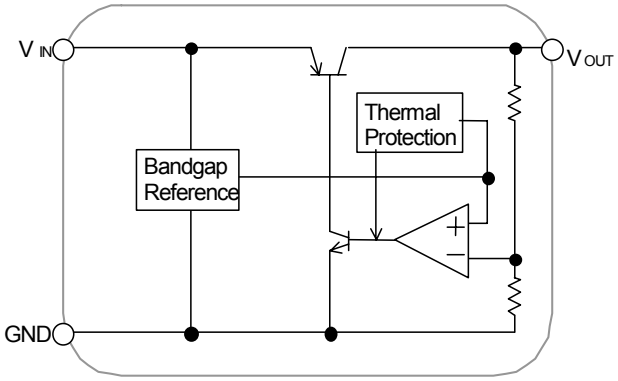
NJM2845DL1



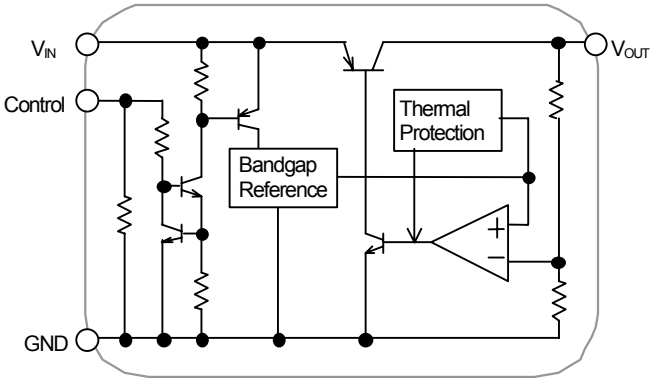
1.CONTROL
2.V_{IN}
3.GND
4.Vo
5.NC

NJM2846DL3

■ EQUIVALENT CIRCUIT



NJM2845DL1



NJM2846DL3

JRC

NJM4556A

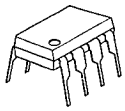
DUAL HIGH CURRENT OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM4556A integrated circuit is a high-gain, high output current dual operational amplifier capable of driving ±70mA into 150 Ω loads (±10.5V output voltage), and operating low supply voltage (V^+/V^-=±2V~).

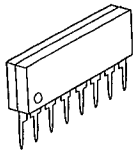
The NJM4556A combines many of the fetures of the popular NJM4558 as well as having the capability of driving 150Ω loads. In addition, the wide band-width, low noise, high slew rate and low distortion of the NJM4556A make it ideal for many audio, telecommunications and instrumentation applications.

■ PACKAGE OUTLINE

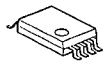


NJM4556AD

NJM4556AM



NJM4556AL

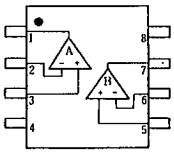


NJM4556AV

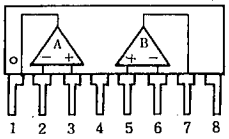
■ FEATURES

- Operating Voltage (±2V~±18V)
- High Output Current (Io=70mA)
- Slew Rate (3V/μs typ.)
- Gain Band Width Product (8MHz typ.)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

■ PIN CONFIGURATION



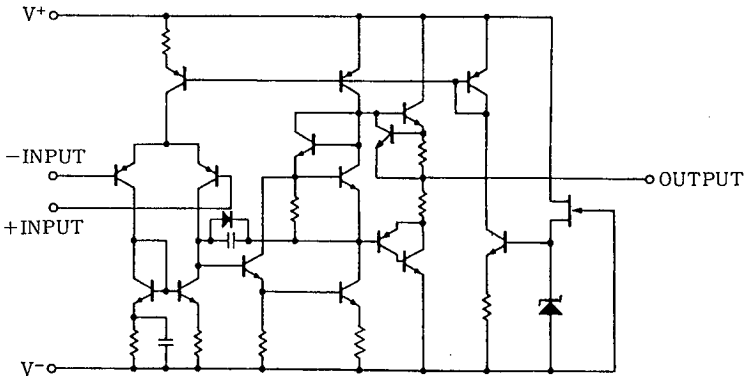
NJM4556AD
NJM4556AM
NJM4556AV



NJM4556AL

PIN FUNCTION
1. A OUTPUT
2. A−INPUT
3. A+INPUT
4. V⁻
5. B+INPUT
6. B−INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



JRC

NJM7800

3-TERMINAL POSITIVE VOLTAGE REGULATOR

■ GENERAL DESCRIPTION

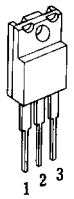
The NJM7800 series of monolithic 3-Terminal Positive Voltage Regulators is constructed using the New JRC Planar epitaxial process. These regulators employ internal current-limiting, thermal-shutdown and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on card) regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

■ FEATURES

- Operating Voltage
- Internal Short Circuit Current Limit
- Internal Thermal Overload Protection
- Excellent Ripple Rejection
- Guarantee'd 1.5A Output Current
- Package Outline TO-220F, TO-252
- Bipolar Technology

■ PACKAGE OUTLINE

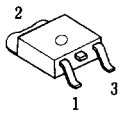
(TO-220F)



NJM7800FA

1. IN
2. GND
3. OUT

(TO-252)

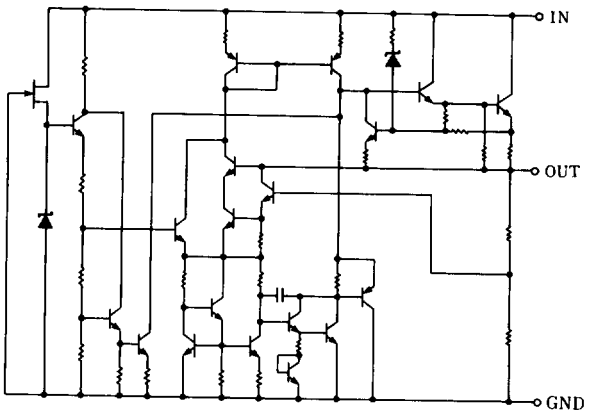


NJM7800DLA

1. IN
2. GND
3. OUT

(note) The radiation fin is connected pin2.

■ EQUIVALENT CIRCUIT



6

JRC

NJM7900

3-TERMINAL NEGATIVE VOLTAGE REGULATOR

■ GENERAL DESCRIPTION

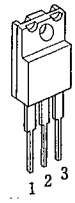
The NJM7900 series of Monolithic 3-Terminal Negative Regulators is constructed using the New JRC Planar epitaxial process. These negative regulators are intended as complements to the popular NJM7800 series of positive voltage regulators, and they are available in the same voltage options from −5 to −24V. The 7900 series employ internal current-limiting, safe-area protection, and thermal shutdown, making the virtually indestructible.

■ FEATURES

- Internal Short Circuit Current Limit
- Internal Thermal Overload Protection
- Excellent Ripple Rejection
- Guarantee'd 1.5A Output Current
- Package Outline TO-220F
- Bipolar Technology

■ PACKAGE OUTLINE

(TO-220F)

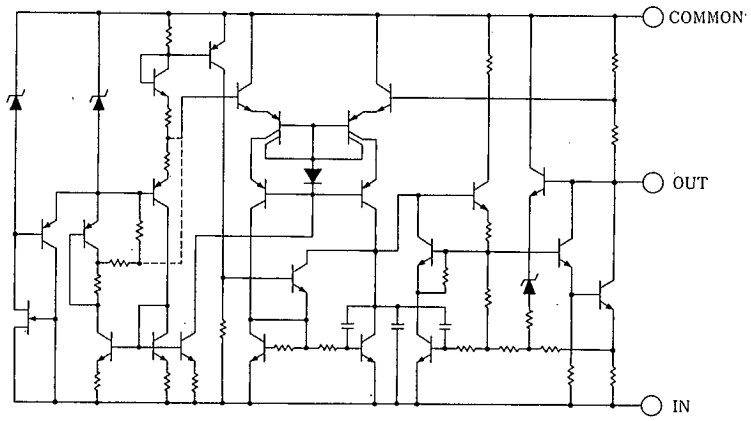


1. COMMON
2. IN
3. OUT

NJM7900FA

(note) The radiation fin is connected to Pin 2.

■ EQUIVALENT CIRCUIT



6

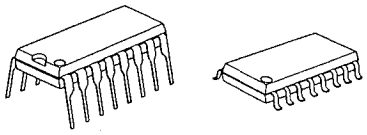
C-MOS QUAD SPST ANALOG SWITCH

■ GENERAL DESCRIPTION

The NJU7301 is a quad break-before-make SPST analog switch protected up to 44V operating voltage.

Each switch is controlled by TTL or C-MOS compatible input.

■ PACKAGE OUTLINE

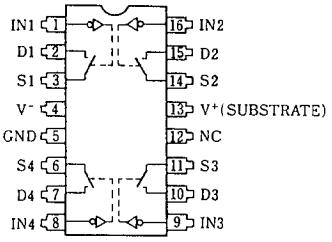


NJU7301D NJU7301M

■ FEATURES

- High Break Down Voltage -- 44V
- Package Outline -- DIP/DMP 16
- C-MOS Technology

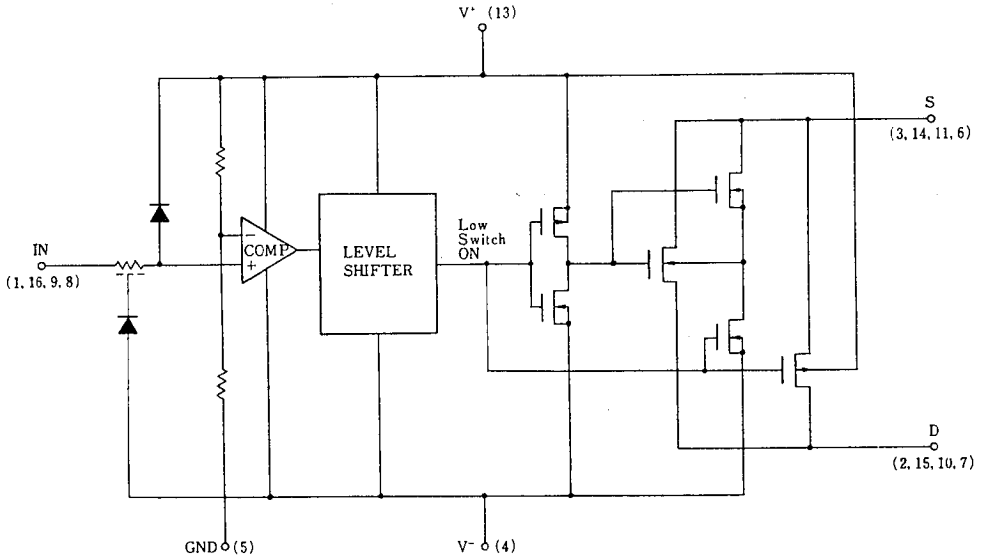
■ PIN CONFIGURATION



■ TRUTH TABLE

Logic (In)	Switch
0	ON
1	OFF

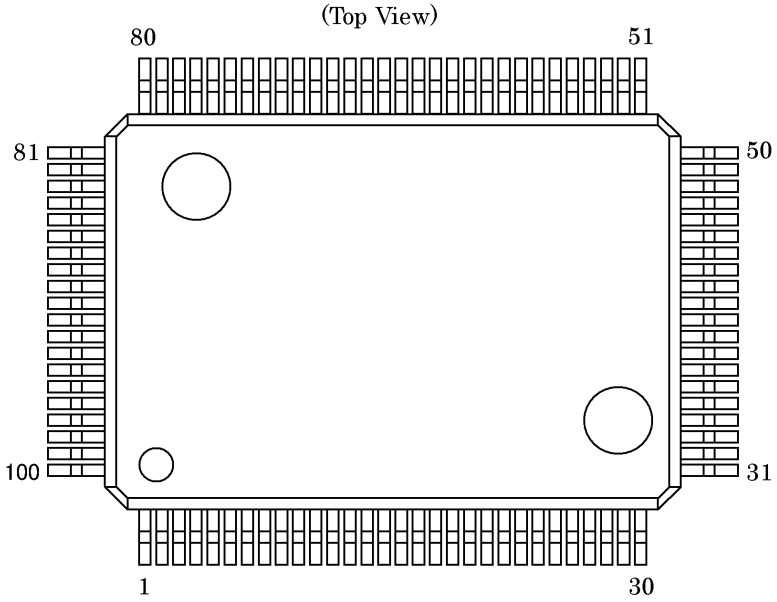
■ EQUIVALENT CIRCUIT



* Logic input threshold voltage V_{TH} is about V^+ x 0.128(V).
When the designing, enough margin is required.

■PIN CONFIGURAITON

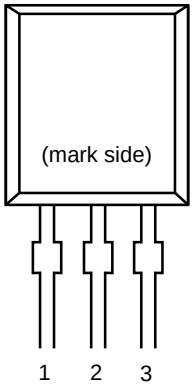
BEE-45919-000-00



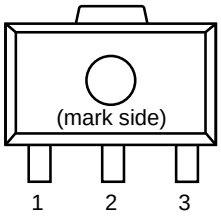
No.	SYMBOL	No.	SYMBOL	No.	SYMBOL	No.	SYMBOL
1	ROUT	26	DCCAP_RS	51	DCR_IN	76	GND
2	COUT	27	L3IN	52	DCR_OUT	77	LSCIN
3	LSOUT	28	DCCAP_LS	53	GND	78	RSCIN
4	RSOUT	29	R3IN	54	DCL_IN	79	LBCIN
5	LBOUT	30	DCCAP_C	55	DCL_OUT	80	RBCIN
6	RBOUT	31	L4IN	56	GND	81	GND
7	SWOUT	32	DCCAP_R	57	REC_B1R	82	LAIN
8	GND	33	R4IN	58	REC_B1L	83	RAIN
9	FIL_BL2	34	DCCAP_L	59	REC_A4R	84	CAIN
10	FIL_BL1	35	L5IN	60	REC_A4L	85	LSAIN
11	FIL_TL	36	GND	61	REC_A3R	86	RSAIN
12	TCAP	37	R5IN	62	REC_A3L	87	LBAIN
13	FIL_BR2	38	GND	63	REC_A2R	88	RBAIN
14	FIL_BR1	39	L6IN	64	REC_A2L	89	SWAIN
15	FIL_TR	40	L9IN	65	REC_A1R	90	GND
16	V^+	41	R6IN	66	REC_A1L	91	LBIN
17	ADR	42	R9IN	67	VDDOUT	92	RBIN
18	V^-	43	L7IN	68	DATA	93	CBIN
19	L1IN	44	L10IN	69	CLOCK	94	LSBIN
20	DCCAP_SW	45	R7IN	70	LATCH	95	RSBIN
21	R1IN	46	R10IN	71	MUTE	96	LBBIN
22	DCCAP_RB	47	L8IN	72	FL+	97	RBBIN
23	L2IN	48	L11IN	73	FL-	98	SWBIN
24	DCCAP_LB	49	R8IN	74	FR+	99	GND
25	R2IN	50	R11IN	75	FR-	100	LOUT

PIN CONFIGURATION

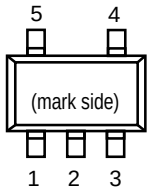
• **TO-92**



• **SOT-89**



• **SOT-23-5**



PIN DESCRIPTION

• **TO-92**

Pin No	Symbol
1	OUT
2	V_{DD}
3	GND

• **SOT-89**

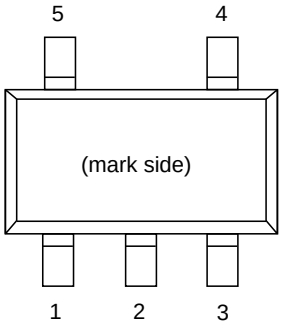
Pin No	Symbol
1	OUT
2	V_{DD}
3	GND

• **SOT-23-5**

Pin No	Symbol
1	OUT
2	V_{DD}
3	GND
4	NC
5	NC

PIN CONFIGURATION

• SOT-23-5



PIN DESCRIPTION

Pin No.	Symbol	Description
1	GND	Ground Pin
2	V_{DD}	Input Pin
3	V_{OUT}	Output Pin
4	NC	No Connection
5	CE or $\overline{CE}$	Chip Enable Pin

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Ratings	Unit
V_{IN}	Input Voltage	9	V
V_{CE}	Input Voltage (CE or $\overline{CE}$ Pin)	–0.3 to V_{IN} +0.3	V
V_{OUT}	Output Voltage	–0.3 to V_{IN} +0.3	V
I_{OUT}	Output Current	200	mA
P_D	Power Dissipation	250	mW
Topt	Operating Temperature	–40 to +85	˚C
Tstg	Storage Temperature	–55 to +125	˚C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

SiI 9030 Pin Diagram

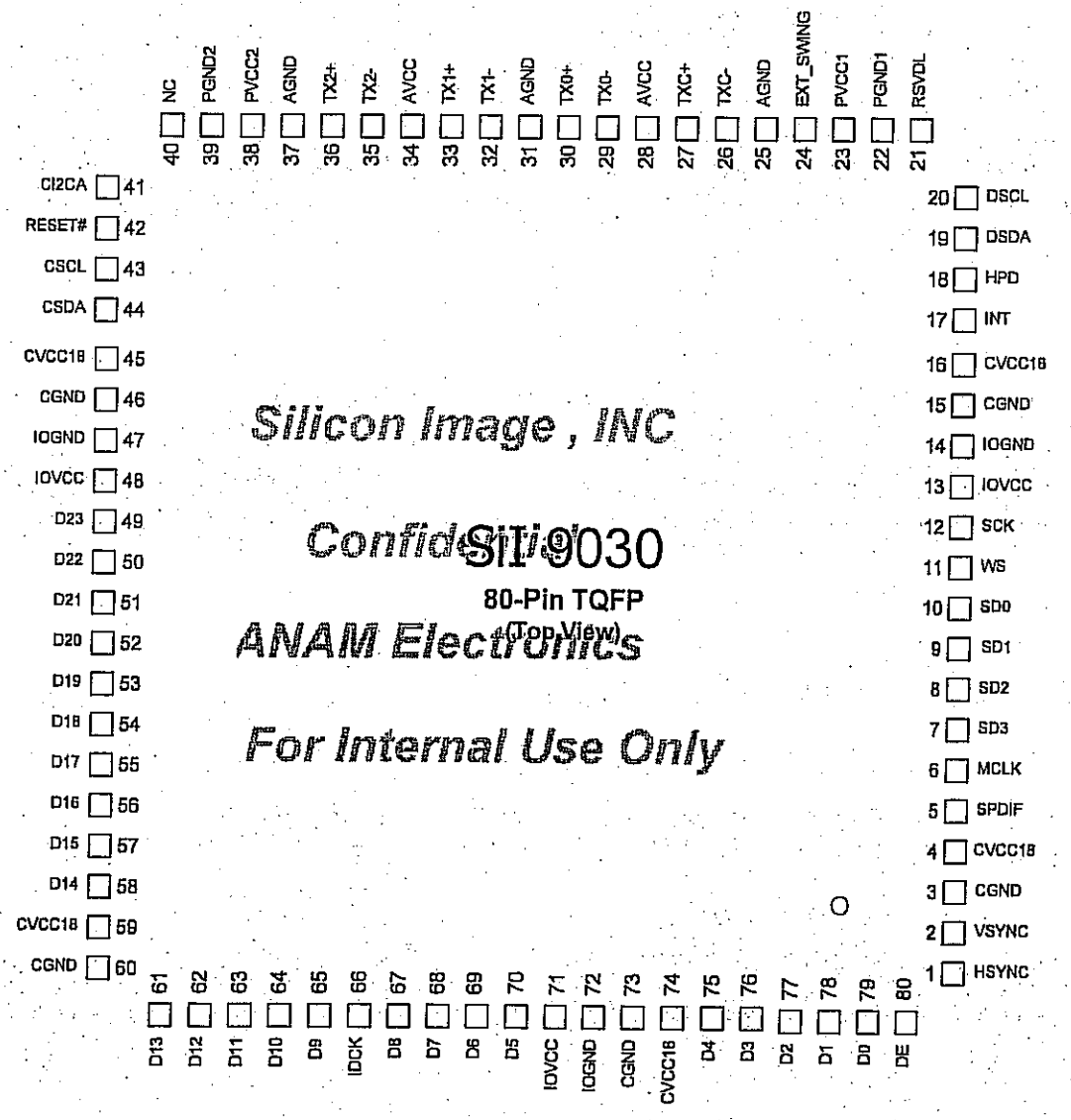


Figure 1. Pin Diagram

Pin Diagram

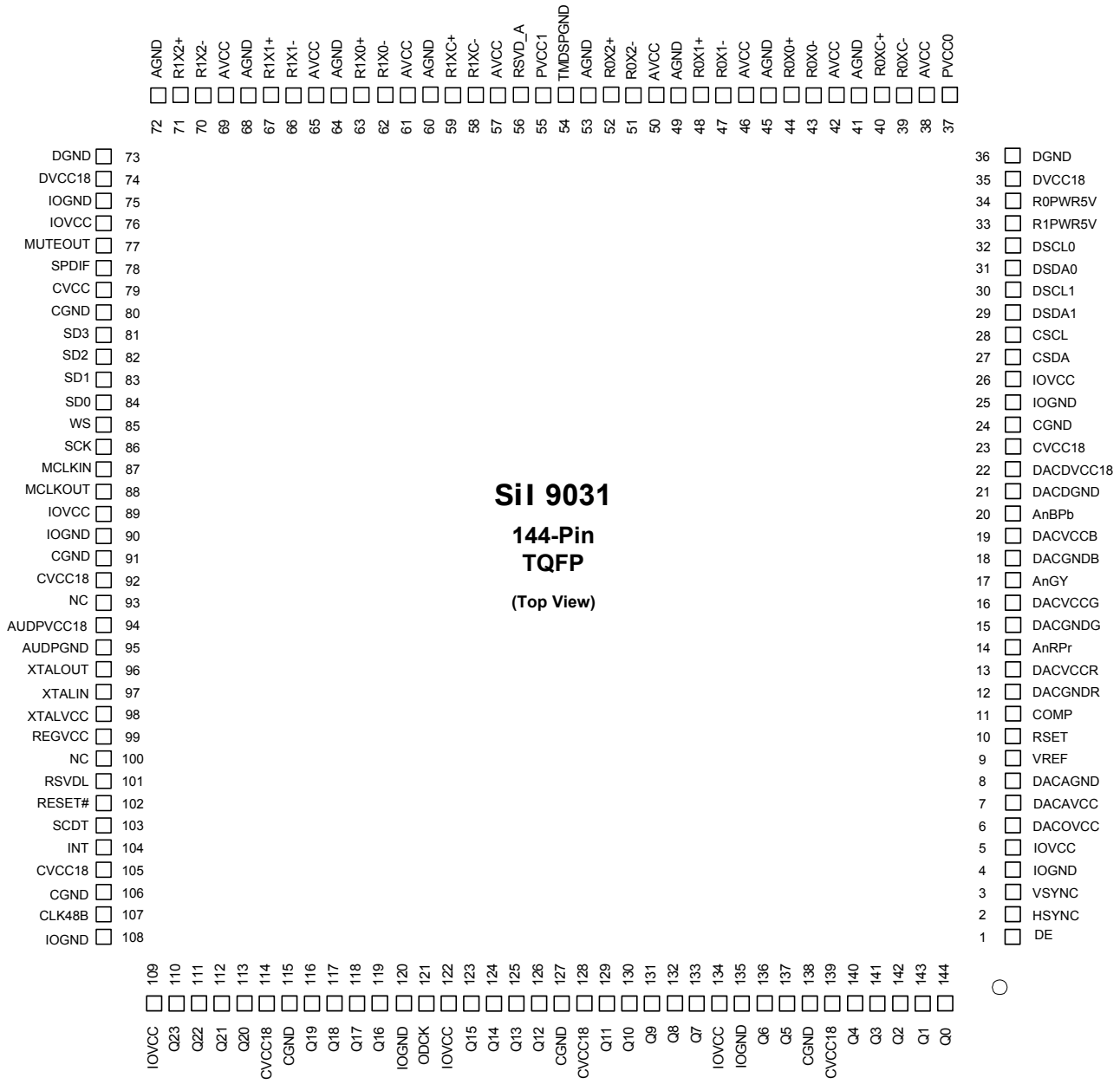


Figure 1. Pin Diagram

Individual pin functions are described beginning on page 37.

8 Mbit SPI Serial Flash
SST25VF080B

Data Sheet

PIN DESCRIPTION

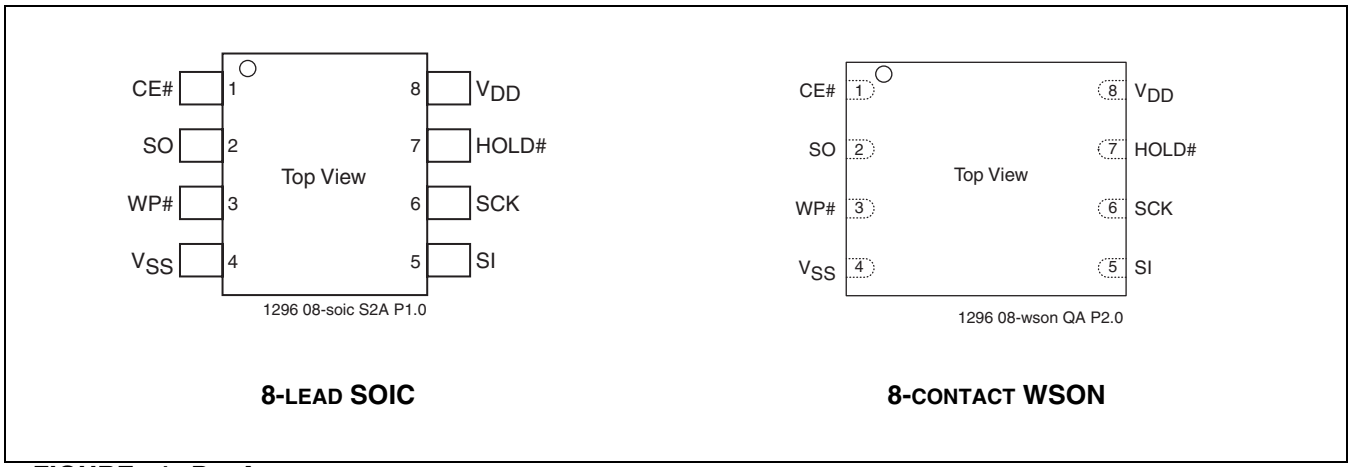


FIGURE 1: PIN ASSIGNMENTS

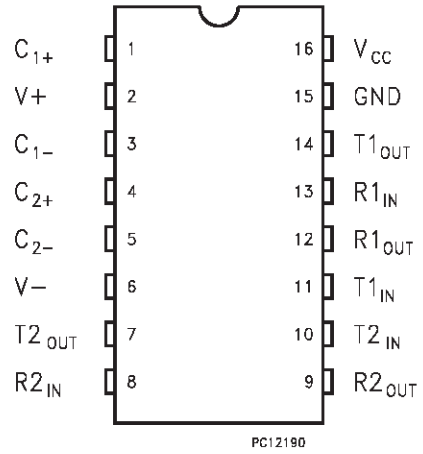
TABLE 1: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. Outputs Flash busy status during AAI Programming when reconfigured as RY/BY# pin. See “Hardware End-of-Write Detection” on page 12 for details.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence.
WP#	Write Protect	The Write Protect (WP#) pin is used to enable/disable BPL bit in the status register.
HOLD#	Hold	To temporarily stop serial communication with SPI flash memory without resetting the device.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V for SST25VF080B
V_{SS}	Ground	

T1.0 1296

ST202E/ST232E

PIN CONFIGURATION



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	C_1+	Positive Terminal for the first Charge Pump Capacitor
2	V+	Doubled Voltage Terminal
3	C_1-	Negative Terminal for the first Charge Pump Capacitor
4	C_2+	Positive Terminal for the second Charge Pump Capacitor
5	C_2-	Negative Terminal for the second Charge Pump Capacitor
6	V-	Inverted Voltage Terminal
7	$T2_{OUT}$	Second Transmitter Output Voltage
8	$R2_{IN}$	Second Receiver Input Voltage
9	$R2_{OUT}$	Second Receiver Output Voltage
10	$T2_{IN}$	Second Transmitter Input Voltage
11	$T1_{IN}$	First Transmitter Input Voltage
12	$R1_{OUT}$	First Receiver Output Voltage
13	$R1_{IN}$	First Receiver Input Voltage
14	$T1_{OUT}$	First Transmitter Output Voltage
15	GND	Ground
16	V_{CC}	Supply Voltage

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the T5CC1, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the T5CC1.

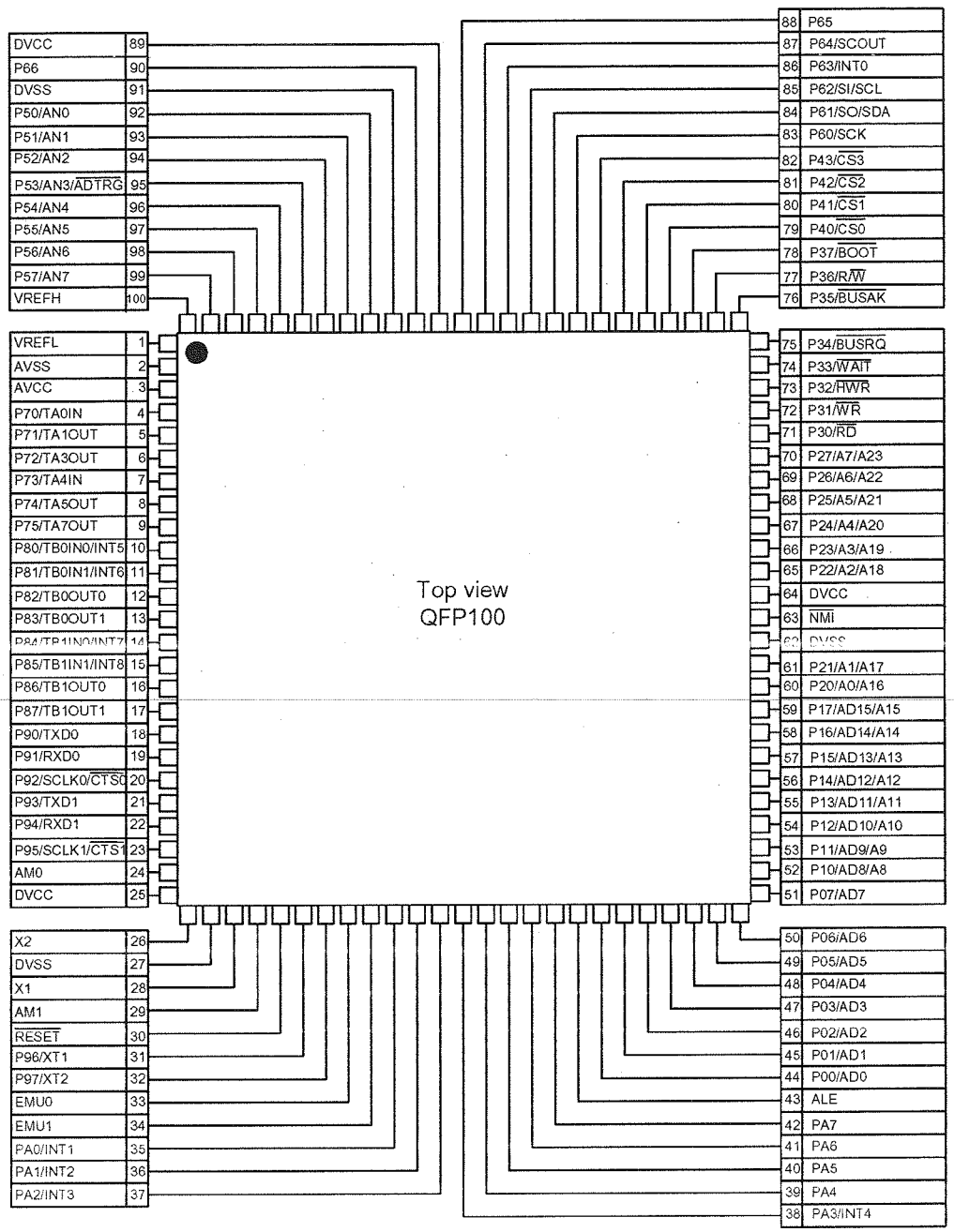
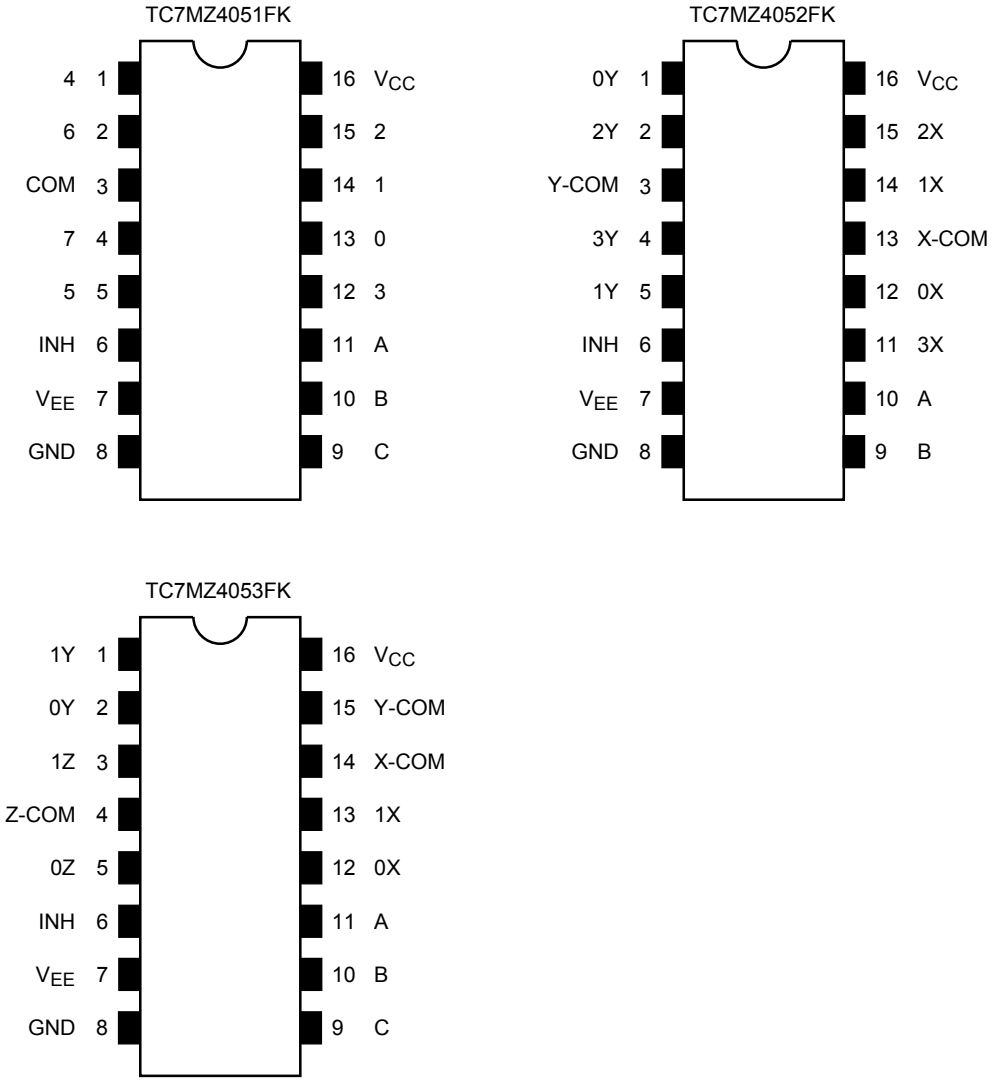


Figure 2.1.1 Pin assignment diagram (100-pin LQFP)

Pin Assignment (top view)



Truth Table

Control Inputs				"ON" Channel		
Inhibit	C*	B	A	MZ4051FK	MZ4052FK	MZ4053FK
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	—	0X, 0Y, 1Z
L	H	L	H	5	—	1X, 0Y, 1Z
L	H	H	L	6	—	0X, 1Y, 1Z
L	H	H	H	7	—	1X, 1Y, 1Z
H	X	X	X	None	None	None

X: Don't care, *: Except MZ4052FK

TOSHIBA TC74HCU04AP/AF/AFN

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HCU04AP, TC74HCU04AF, TC74HCU04AFN

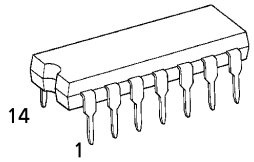
HEX INVERTER

(Note) The JEDEC SOP (FN) is not available in Japan.

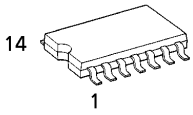
The TC74HCU04A is a high speed CMOS INVERTER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Since the internal circit is composed of a single stage inverter, it can be used in analog applications such as crystal oscllators.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

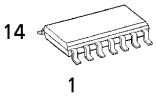
- High Speed ····· t_{pd} = 4ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 1 μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIH}$ = 10% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ·· V_{CC}(opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS04



P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)

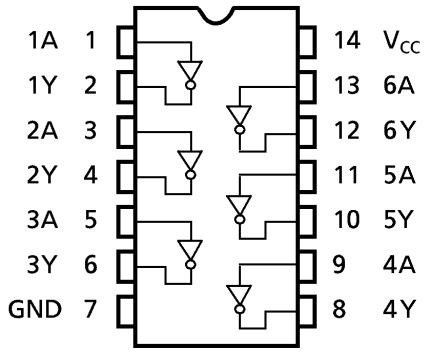


F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)



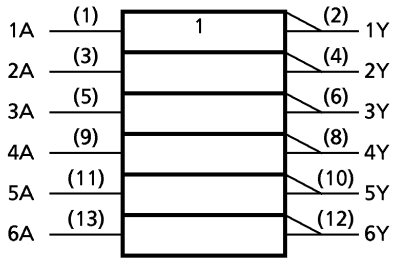
FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

961001EBA2

TOSHIBA TC74VHC157F/FN/FT

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC157F, TC74VHC157FN, TC74VHC157FT

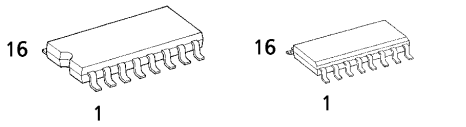
QUAD 2 - CHANNEL MULTIPLEXER

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74VHC157 is an advanced high speed CMOS QUAD 2 - CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
It consists of four 2 - input digital multiplexers with common select and strobe inputs.
When the $\overline{STROBE}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level.
The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.
An Input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

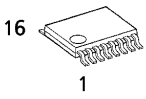
FEATURES :

- High Speed ····· t_{pd} = 4.1ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr) = 2V ~ 5.5V
- Low Noise ····· V_{OLP} = 0.8V (Max.)
- Pin and Function Compatible with 74ALS157



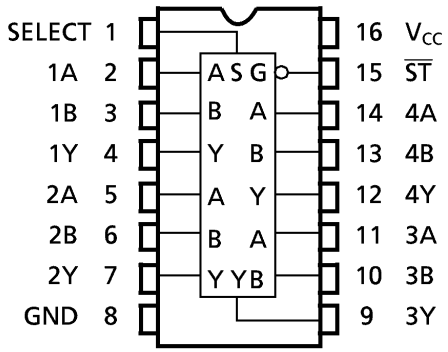
F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)



FT (TSSOP16-P-0044-0.65)
Weight : 0.06g (Typ.)

PIN ASSIGNMENT

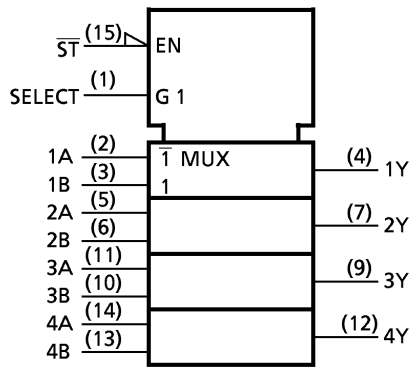


TRUTH TABLE

INPUTS				OUTPUT
$\overline{ST}$	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X : Don't Care

IEC LOGIC SYMBOL



980910EBA2

NEC

MOS FIELD EFFECT TRANSISTOR

μPA672T

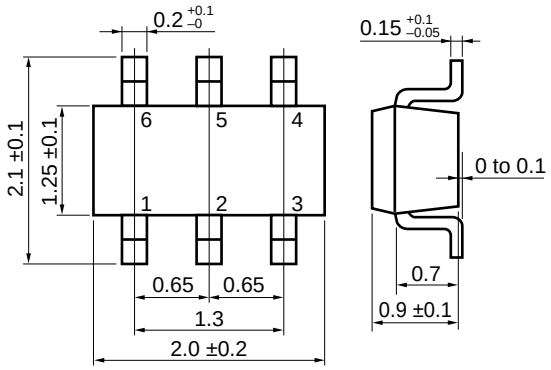
N-CHANNEL MOS FET ARRAY FOR SWITCHING

The μPA672T is a super-mini-mold device provided with two MOS FET elements. It achieves high-density mounting and saves mounting costs.

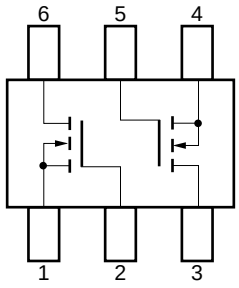
FEATURES

- Two MOS FET circuits in package the same size as SC-70
- Automatic mounting supported

PACKAGE DIMENSIONS (in millimeters)



PIN CONNECTION



1. Source 1 (S1)
2. Gate 1 (G1)
3. Drain 2 (D2)
4. Source 2 (S2)
5. Gate 2 (G2)
6. Drain 1 (D1)

Marking: MA

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}		50	V
Gate to Source Voltage	V_{GSS}		±7.0	V
Drain Current (DC)	$I_{D(DC)}$		100	mA
Drain Current (pulse)	$I_{D(pulse)}$	PW ≤ 10 ms, Duty Cycle ≤ 50 %	200	mA
Total Power Dissipation	P_T		200 (Total)	mW
Channel Temperature	T_{ch}		150	°C
Storage Temperature	T_{stg}		–55 to +150	°C

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