MK2302S-01

Multiplier and Zero Delay Buffer

Description

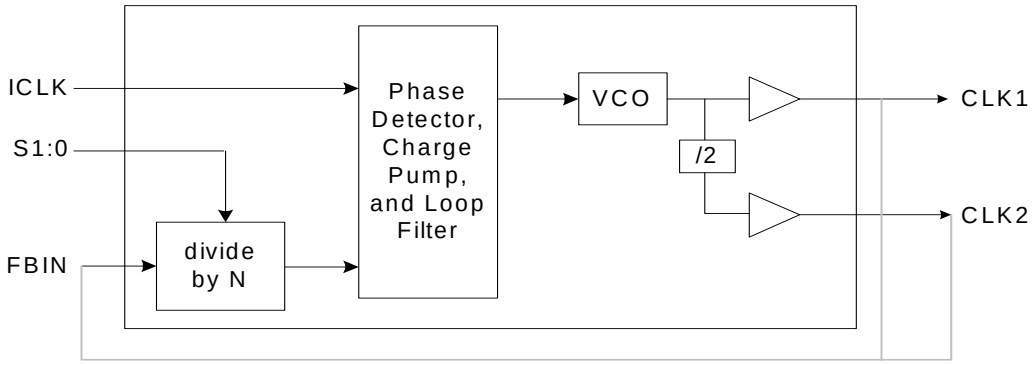
The MK2302S-01is a high performance Zero Delay Buffer (ZDB) which integrates ICS' proprietary analog/digital Phase Locked Loop (PLL) techniques. The chip is part of ICS' ClockBlocks™ family and was designed as a performance upgrade to meet today's higher speed and lower voltage requirements. The zero delay feature means that the rising edge of the input clock aligns with the rising edges of both output clocks, giving the appearance of no delay through the device. There are two outputs on the chip, one being a low-skew divide by two of the other output.

The MK2302S-01 is ideal for synchronizing outputs in a large variety of systems, from personal computers to data communications to graphics/video. By allowing off-chip feedback paths, the device can eliminate the delay through other devices.

Features

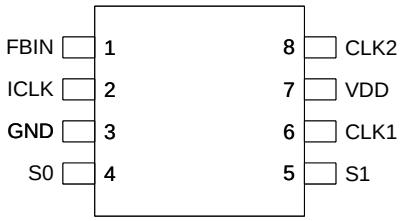
- 8 pin SOIC package
- Low input to output skew of 250ps max
- Absolute jitter ± 500ps
- Propagation Delay ± 350ps
- Ability to choose between different multipliers from 0.5X to 16X
- Output clock frequency up to 133 MHz at 3.3V
- Can recover degraded input clock duty cycle
- Output clock duty cycle of 45/55
- Full CMOS clock swings with 25mA drive capability at TTL levels
- Advanced, low power CMOS process
- Operating voltage of 3.3V or 5V
- Industrial temperature version available

Block Diagram



External feedback can come from CLK1 or CLK2 (see table on page 2)

Pin Assignment



8 pin (150 mil) SOIC

Clock Multiplier Decoding Table 1

(Multiplies Input clock by shown amount)

FBIN	S1	S0	CLK1	CLK2
CLK1	0	0	2 X ICLK	ICLK
CLK1	0	1	4 X ICLK	2 X ICLK
CLK1	1	0	ICLK	ICLK/2
CLK1	1	1	8 X ICLK	4 X ICLK
CLK2	0	0	4 X ICLK	2 X ICLK
CLK2	0	1	8 X ICLK	4 X ICLK
CLK2	1	0	2 X ICLK	ICLK
CLK2	1	1	16 X ICLK	8 XICLK

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	FBIN	Input	Feedback clock input.
2	ICLK	Input	Reference clock input.
3	GND	Power	Connect to ground.
4	S0	Input	Select 0 for output clock per decoding table above. Pull-up.
5	S1	Input	Select 1 for output clock per decoding table above. Pull up.
6	CLK1	Output	Clock output per table above.
7	VDD	Power	Connect to +3.3V or +5.0V.
8	CLK2	Output	Clock output per table above. Low skew divide by two of pin 6 clock.

Multiformat Video Encoder Six, 11-Bit, 297 MHz DACs

ADV7342/ADV7343

FEATURES

- 74.25 MHz 20-/30-bit high definition input support
  - Compliant with SMPTE 274M (1080i), 296M (720p), and 240M (1035i)
- 6, 11-bit, 297 MHz video DACs
  - 16× (216 MHz) DAC oversampling for SD
  - 8× (216 MHz) DAC oversampling for ED
  - 4× (297 MHz) DAC oversampling for HD
  - 37 mA maximum DAC output current
- NTSC M, PAL B/D/G/H/I/M/N, PAL 60 support
- NTSC and PAL square pixel operation (24.54 MHz/29.5 MHz)
- Multiformat video input support
  - 4:2:2 YCrCb (SD, ED, and HD)
  - 4:4:4 YCrCb (ED and HD)
  - 4:4:4 RGB (SD, ED, and HD)
- Multiformat video output support
  - Composite (CVBS) and S-Video (Y/C)
  - Component YPrPb (SD, ED, and HD)
  - Component RGB (SD, ED, and HD)
- Macrovision® Rev 7.1.L1 (SD) and Rev 1.2 (ED) compliant
- Simultaneous SD and ED/HD operation
- EIA/CEA-861B compliance support
- Programmable features
  - Luma and chroma filter responses
  - Vertical blanking interval (VBI)
  - Subcarrier frequency (F_{SC}) and phase
  - Luma delay
- Copy generation management system (CGMS)
- Closed captioning and wide screen signaling (WSS)
- Integrated subcarrier locking to external video source
- Complete on-chip video timing generator
- On-chip test pattern generation
- On-board voltage reference (optional external input)
- Serial MPU interface with dual I²C® and SPI® compatibility
- 3.3 V analog operation
- 1.8 V digital operation
- 3.3 V I/O operation
- Temperature range: −40°C to +85°C

APPLICATIONS

- DVD recorders and players
- High definition Blu-ray DVD players
- HD-DVD players

FUNCTIONAL BLOCK DIAGRAM

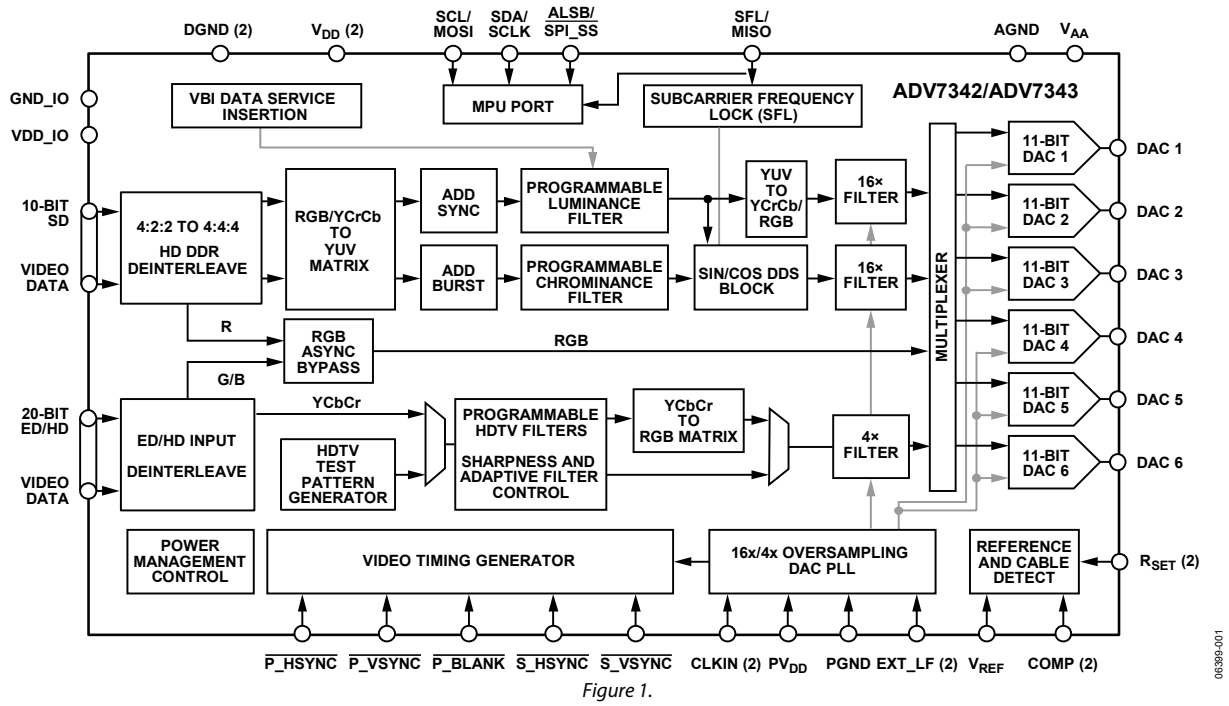


Figure 1.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

ADV7342/ADV7343

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

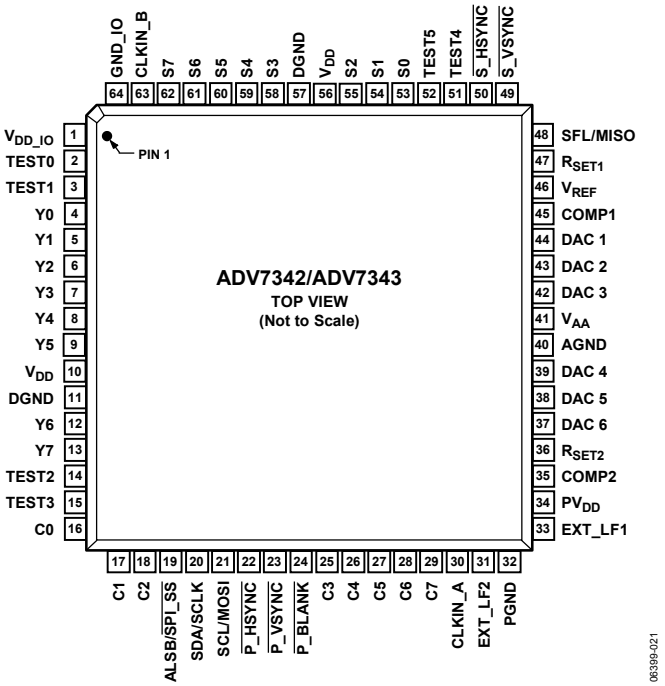


Figure 21. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output	Description
13, 12, 9 to 4	Y7 to Y0	I	8-Bit Pixel Port. Y0 is the LSB. Refer to Table 31 for input modes.
29 to 25, 18 to 16	C7 to C0	I	8-Bit Pixel Port. C0 is the LSB. Refer to Table 31 for input modes.
62 to 58, 55 to 53	S7 to S0	I	8-Bit Pixel Port. S0 is the LSB. Refer to Table 31 for input modes.
52, 51, 15, 14, 3, 2	TEST5 to TEST0	I	Unused. These pins should be connected to DGND.
30	CLKIN_A	I	Pixel Clock Input for HD Only (74.25 MHz), ED[1] Only (27 MHz or 54 MHz) or SD Only (27 MHz).
63	CLKIN_B	I	Pixel Clock Input for Dual Modes Only. Requires a 27 MHz reference clock for ED operation or a 74.25 MHz reference clock for HD operation.
50	$\overline{\text{S\_HSYNC}}$	I/O	SD Horizontal Synchronization Signal. This pin can also be configured to output an SD, ED, or HD horizontal synchronization signal. See the External Horizontal and Vertical Synchronization Control section.
49	$\overline{\text{S\_VSYNC}}$	I/O	SD Vertical Synchronization Signal. This pin can also be configured to output an SD, ED, or HD vertical synchronization signal. See the External Horizontal and Vertical Synchronization Control section.
22	$\overline{\text{P\_HSYNC}}$	I	ED/HD Horizontal Synchronization Signal. See the External Horizontal and Vertical Synchronization Control section.
23	$\overline{\text{P\_VSYNC}}$	I	ED/HD Vertical Synchronization Signal. See the External Horizontal and Vertical Synchronization Control section.
24	$\overline{\text{P\_BLANK}}$	I	ED/HD Blanking Signal. See the External Horizontal and Vertical Synchronization Control section.
48	SFL/MISO	I/O	Multifunctional Pin: Subcarrier Frequency Lock (SFL) Input/SPI Data Output. The SFL input is used to drive the color subcarrier DDS system, timing reset, or subcarrier reset.
47	R_{SET1}	I	This pin is used to control the amplitudes of the DAC 1, DAC 2, and DAC 3 outputs. For full-drive operation (for example, into a 37.5 Ω load), a 510 Ω resistor must be connected from R_{SET1} to AGND. For low drive operation (for example, into a 300 Ω load), a 4.12 kΩ resistor must be connected from R_{SET1} to AGND.

Pin No.	Mnemonic	Input/ Output	Description
36	R_{SET2}	I	This pin is used to control the amplitudes of the DAC 4, DAC 5, and DAC 6 outputs. A 4.12 kΩ resistor must be connected from R_{SET2} to AGND.
45, 35	COMP1, COMP2	O	Compensation Pins. Connect a 2.2 nF capacitor from both COMP pins to V_{AA}.
44, 43, 42	DAC 1, DAC 2, DAC 3	O	DAC Outputs. Full and low drive capable DACs.
39, 38, 37	DAC 4, DAC 5, DAC 6	O	DAC Outputs. Low drive only capable DACs.
21	SCL/MOSI	I	Multifunctional Pin: I²C Clock Input/SPI Data Input.
20	SDA/SCLK	I/O	Multifunctional Pin: I²C Data Input/Output. Also, SPI clock input.
19	ALSB/$\overline{\text{SPI\_SS}}$	I	Multifunctional Pin: This signal sets up the LSB[2] of the MPU I²C address. Also, SPI slave select.
46	V_{REF}		Optional External Voltage Reference Input for DACs or Voltage Reference Output.
41	V_{AA}	P	Analog Power Supply (3.3 V).
10, 56	V_{DD}	P	Digital Power Supply (1.8 V). For dual-supply configurations, V_{DD} can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering.
1	V_{DD_IO}	P	Input/Output Digital Power Supply (3.3 V).
34	PV_{DD}	P	PLL Power Supply (1.8 V). For dual-supply configurations, PV_{DD} can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering.
33	EXT_LF1	I	External Loop Filter for On-Chip PLL 1.
31	EXT_LF2	I	External Loop Filter for On-Chip PLL 2.
32	PGND	G	PLL Ground Pin.
40	AGND	G	Analog Ground Pin.
11, 57	DGND	G	Digital Ground Pin.
64	GND_IO	G	Input/Output Supply Ground Pin.

[1] ED = enhanced definition = 525p and 625p.
[2] LSB = least significant bit. In the ADV7342, setting the LSB to 0 sets the I²C address to 0xD4. Setting it to 1 sets the I²C address to 0xD6. In the ADV7343, setting the LSB to 0 sets the I²C address to 0x54. Setting it to 1 sets the I²C address to 0x56.

TOSHIBA TC74HCU04AP/AF/AFN

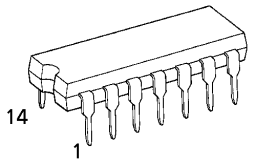
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HCU04AP, TC74HCU04AF, TC74HCU04AFN

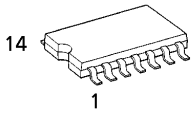
HEX INVERTER

(Note) The JEDEC SOP (FN) is not available in Japan.

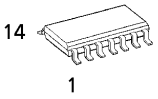
The TC74HCU04A is a high speed CMOS INVERTER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Since the internal circit is composed of a single stage inverter, it can be used in analog applications such as crystal oscllators.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)



F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

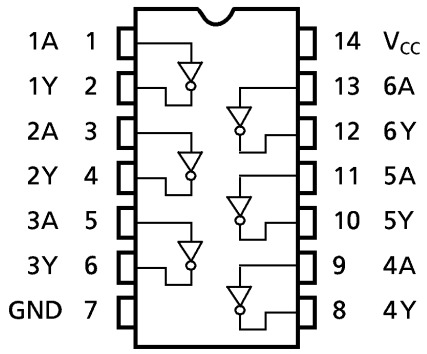


FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

FEATURES :

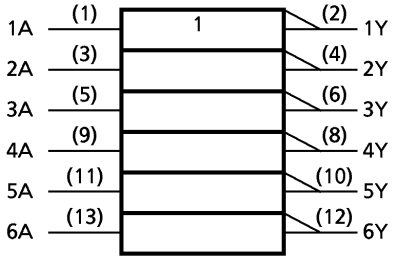
- High Speed ····· t_{pd} = 4ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 1μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIH}$ = 10% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ·· V_{CC}(opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS04

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

961001EBA2

IC51 XM IC

1. Overview

The XM Digital Transceiver Integrated Circuit (XM/DT IC) provides a cost effective means for an electronics equipment manufacturer to be XM Satellite Radio compatible by multiplexing data and audio streams between the XM Receiver and User Interface Controller into a 2 wire time division duplex (TDD) high frequency serial link.

In a typical application, two XM/ DT IC devices connect to each other via a differential link as depicted on Figure 1.1 below. In the 'Slave' unit ("XM/DT Digital Transceiver" (antenna)), the XM/DT IC interfaces directly to the XM Radio receiver chipset taking in a real-time PCM (I2S) audio stream along with data information. The XM/DT IC stores this data in internal RAM and then time division multiplexes the data on a 2-wire serial communication link. This link provides for the physical decoupling of the Slave and Master side of up 100 meters with software transparency between the Master side processor and audio circuitry and the Slave side XM Satellite Radio receiver chip set.

In the Master unit ("XM/DT Ready Radio"), the XM/DT IC demultiplexes the received data, buffers it internally and reproduces it for consumption. The XM/DT IC is capable of simultaneously sending and receiving serial frames while multiplexing and de-multiplexing them in real time, formatting them and then routing them into the appropriate Slave or Master side interfaces.

The software interface between the user interface and the receiver is unaffected by the introduction of the XM/DT IC link pair.

An input pin on the XM/DT IC configures the part's functionality as either Master (user interface end) or Slave (XM Digital Transceiver end) allowing the same IC to be used at either end of the link.

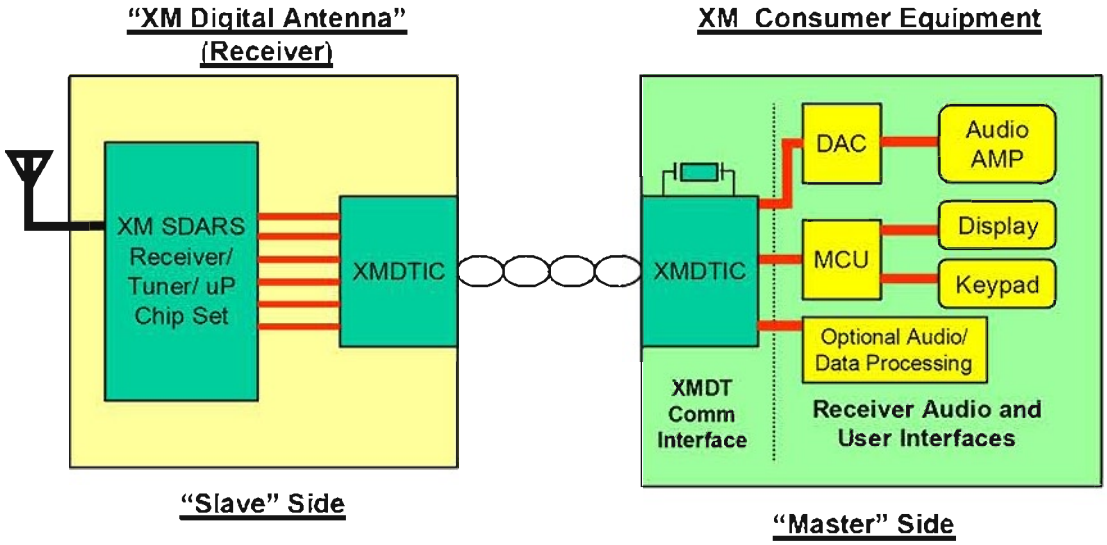


Figure 1.1 - Typical XM/DT Application

2. Functional Description

Figure 2.1 below shows a basic top level diagram showing each functional block in the XM/DT device.

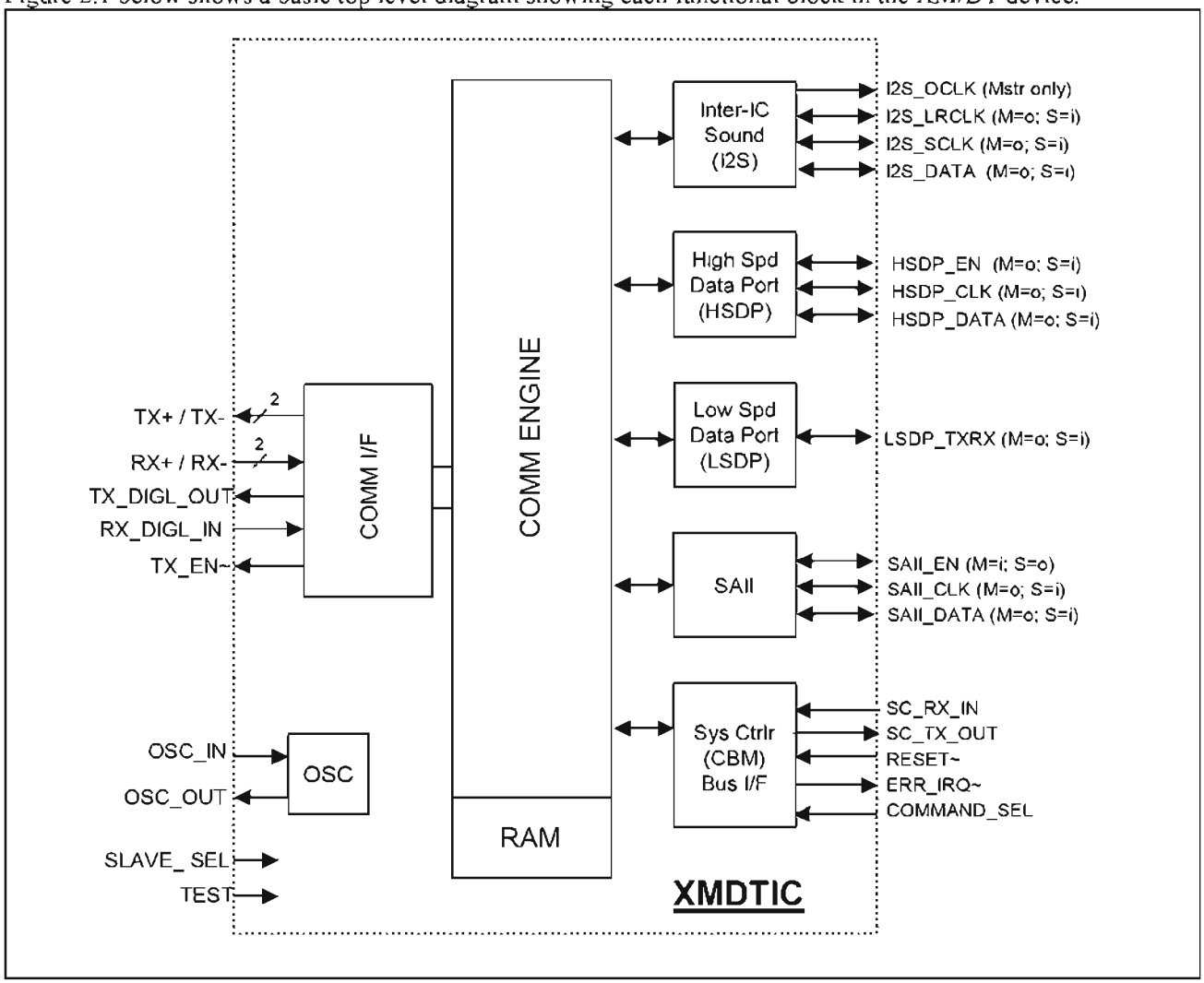


Figure 2.1 XM/DT Top Level Diagram

The XM/DT IC is broken into the following functional blocks:

SC I/F – System Controller Interface

The System Controller Interface transports the serial communication commands and data between the microprocessor in the user interface device and the microprocessor in the XM Digital Antenna. The commands and data transported follow typically follow the XM CBM (Common Bus Messaging) protocol.

The System Controller Interface functional block consists of a full duplex asynchronous serial interface. The SC I/F is used for both the software configuration of the XM/DT IC, monitoring of XM/DT link status, and transparent communications with the SC I/F at the other end of the communications link. The SC I/F block contains five signals, SC_RX_IN, SC_TX_OUT, COMMAND_SEL, ERR_IRQ#, and RESET#.

The SC_RX_IN and SC_TX_OUT connect the asynchronous serial communications to the respective microprocessors. The SC I/F

communicates at a default mode of 9600 baud, no parity, 8 data bits, and 1 stop bit. The baud rate can be changed using the XM/DT IC Command Mode. The Master and Slave baud rates must be set to the same rate by their respective microprocessors.

The COMMAND_SEL input allows configuration of the XM/DT IC and to retrieve feedback of the link status during normal operation. This signal is logic low for normal operation and logic high for Command/Stat Mode. Details of the operation of this signal are described in the Programming section of this specification.

The ERR_IRQ# output signal is active low when an error occurs on the link if interrupts are enabled via the Interrupt Mask register. Access to the Interrupt Mask register is gained via the Command Mode and the interrupt source identification is obtained via the Status Mode. Details of these modes are described in the Programming section of this specification.

The RESET# input signal is used to perform a complete asynchronous reset of the XM/DT IC. The RESET# signal is also used to place the XM/DT IC into Command Mode. Refer to the Programming section.

SAII – Synchronous Audio Input Interface

The SAII Interface functional block provides a synchronous interface with hardware flow control from the Master to the Slave devices.

In Master mode, the XM/DT IC receives SAII Data and SAII Clock from the SAII source in the "playback unit". The SAII Enable (SAII_EN) output signal is fed back to the SAII source to control the flow of input data based on the state of the SAII_EN signal at the Slave Device.

In Slave mode, the XM/DT IC sends SAII Data and SAII Clock to the Slave device SAII receiver, and receives the SAII_EN signal from the SAII receiver to control the flow of transmitted data.

The Master XM/DT IC adapts to the incoming SAII data rate.

LSDP – Low Speed Data Port

The LSDP functional block consists of a unidirectional asynchronous serial interface.

In Master mode, the LSDP transmits data out of the device. In Slave mode, the LSDP receives data into the device.

This interface operates in default mode at 115200, no parity, 8 data bits, and 1 stop bit.

HSDP – High Speed Data Port Interface

The HSDP Interface functional block provides a synchronous serial interface combined with a framing signal from the Slave XM/DT IC to the Master XM/DT IC.

The source of the HSDP is typically the XM receiver chipset. The HSDP data is typically received by the Host microprocessor. The HSDP signals include a serial data bitstream (HSDP_DA), a synchronous clock (HSDP_CLK), and a framing signal (HSDP_EN). The framing signal can be used as a gating mechanism for the clock or an interrupt source to indicate the beginning and end of the HSDP data burst.

In Slave mode, the HSDP Interface receives HSDP_DA, HSDP_CLK, and HSDP_EN from the HSDP source. In Master mode, the HSDP Interface transmits HSDP_DA, HSDP_CLK, and HSDP_EN.

I2S – Inter-IC Sound (I2S) digital audio Interface

The I2S functional block receives and transmits timing and frame sensitive data. The I2S interface is also referred to as the PCM interface.

In Slave mode, the XM/DT IC I2S Interface receives the I2S digital audio from the XM Receiver chipset. The XM/DT IC automatically adjusts to the incoming I2S data sampling rate.

In Master mode, the XM/DT IC I2S Interface generates all required signals to drive an I2S compatible audio DAC.

COMM2W – Two Wire Communications Interface

The COMM2W functional block enables communications between two XM/DT ICs. The COMM2W is differential Time-Division-Duplex Interface.

3. Physical Description

3.1 Device Pin-out

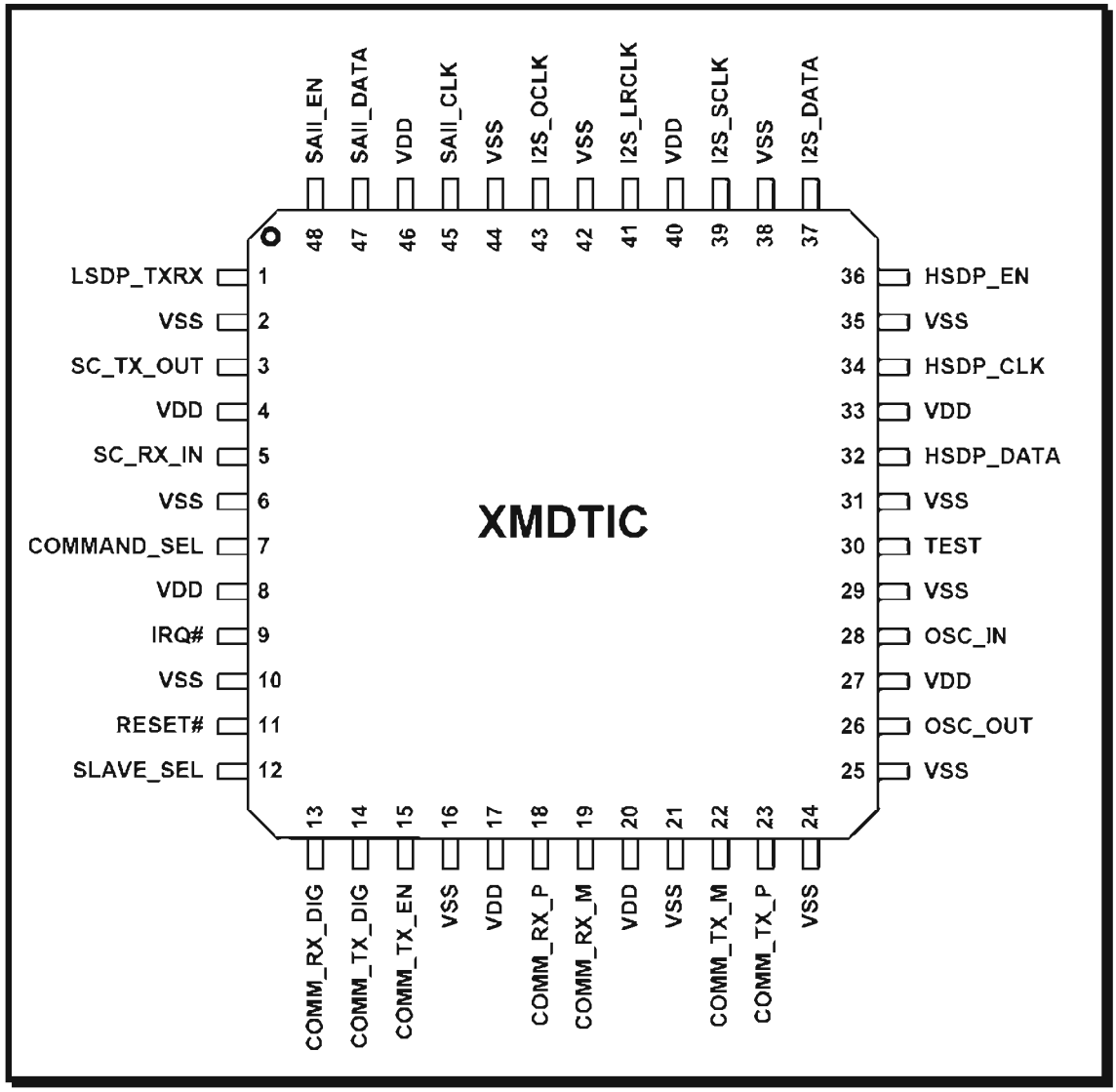


Figure 3.1 – Pin Connection (Top View)

3.2 Pin Descriptions

Table 3.2 Pin Descriptions

Pin #	Pin Name	Type	Function in Slave Mode	Function in Master Mode	Notes
1	LSDP_TXRX	S=In M=Out	Low Speed Data Port Output	Low Speed Data Port Input	LVTTL S/T
3	SC_TX_OUT	S=Out M=Out	System Controller Bus (CBM) Transmit Data Out	System Controller Bus (CBM) Transmit Data Out	4mA, SLC
5	SC_RX_IN	S=In M=In	System Controller Bus (CBM) Receive Data In	System Controller Bus (CBM) Receive Data In	LVTTL S/T
7	COMMAND_SEL	S=In M=In	Command Mode Select In (1= Command Mode, 0=Normal Mode)	Command Mode Select In (1= Command Mode, 0=Normal Mode)	LVTTL S/T
9	IRQ#	S=Out M=Out	Interrupt Request Out (Active Low)	Interrupt Request Out (Active Low)	4mA Open Drain
11	RESET#	S=In M=In	Asynchronous Reset In, (Active Low)	Asynchronous Reset In, (Active Low)	LVTTL S/T
12	SLAVE_SEL	S=In M=In	M/S Mode Select In (High = Slave Mode)	M/S Mode Select In (Low = Master Mode)	LVTTL S/T
13	COMM_RX_DIG	S=In M=In	DT Comm Bus External Transceiver Receive Data In	DT Comm Bus External Transceiver Receive Data In	LVTTL S/T
14	COMM_TX_DIG	Output	DT Comm Bus External Transceiver Transmit Data Out	DT Comm Bus External Transceiver Transmit Data Out	LVTTL S/T
15	COMM_TX_EN	Output	DT Comm Bus External Transceiver Direction Out (1=Transmit, 0=Receive)	DT Comm Bus External Transceiver Direction Out (1=Transmit, 0=Receive)	LVTTL S/T
18	COMM_RX_P	S=In M=In	DT Comm Bus Internal Receiver Differential Positive In	DT Comm Bus Internal Receiver Differential Positive In	LVDS in+
19	COMM_RX_M	S=In M=In	DT Comm Bus Internal Receiver Differential Negative In	DT Comm Bus Internal Receiver Differential Negative In	LVDS in–
22	COMM_TX_M	Output	DT Comm Bus Internal Transmitter Differential Negative Out	DT Comm Bus Internal Transmitter Differential Negative Out	LVDS out–
23	COMM_TX_P	Output	DT Comm Bus Internal Transmitter Differential Positive Out	DT Comm Bus Internal Transmitter Differential Positive Out	LVDS out+
26	OSC_OUT	Output	Crystal Output	Crystal Output	Crystal Buffer
28	OSC_IN	S=In M=In	Crystal Input	Crystal Input	Crystal Buffer
30	TEST	S=In M=In	Factory Test Mode Select (1=Test, 0= Normal Oper.)	Factory Test Mode Select (1=Test, 0= Normal Oper.)	LVTTL S/T
32	HSDP_DATA	S=In M=Out	High Speed Data Port Data Input	High Speed Data Port Data Output	Out= 4mA, SLC In=LVTTL S/T
34	HSDP_CLK	S=In M=Out	High Speed Data Port Clock Input	High Speed Data Port Clock Output	Out= 4mA, SLC In=LVTTL S/T
36	HSDP_EN	S=Out M=In	High Speed Data Port Enable Output	High Speed Data Port Enable Input	Out= 4mA, SLC In=LVTTL S/T
37	I2S_DATA	S=In M=Out	I2S Digital Port Data In	I2S Digital Audio Port Data Out	Out= 4mA, SLC In=LVTTL S/T

Pin #	Pin Name	Type	Function in Slave Mode	Function in Master Mode	Notes
39	I2S_SCLK	S=In M=Out	I2S Digital Audio Port Bit Clock In	I2S Digital Audio Port Bit Clock Out	Out= 4mA, SLC In=LVTTL S/T
41	I2S_LRCLK	S=In M=Out	I2S Digital Audio Port Left/Right Clock In	I2S Digital Audio Port Left/Right Clock Out	Out= 4mA, SLC In=LVTTL S/T
43	I2S_OCLK	S=In M=Out	I2S Digital Audio Port Oversample Clock (not used - connect to Gnd???)	I2S Digital Audio Port Oversample Clock Out	Out= 4mA, SLC
45	SAII_CLK	S=Out M=In	SAII Port Clock Output	SAII Port Clock Input	Out= 4mA, SLC 3.3V S/T
47	SAII_DATA	S=Out M=In	SAII Port Data Output	SAII Port Data Input	Out= 4mA, SLC In=LVTTL S/T
48	SAII_REQ	S=In M=Out	SAII Port Request Input	SAII Port Request Output	Out= 4mA, SLC In=LVTTL S/T

Pin#	Pin Name	Type	Function in Slave Mode	Function in Master Mode	Notes
4, 8, 17, 20, 27, 33, 40, 46	VDD	PWR	+3.3V Supply Voltage	+3.3V Supply Voltage	
2, 6, 10, 16, 21, 24, 25, 29, 31, 25, 38, 42, 44	VSS	GND	Digital Ground	Digital Ground	

Notes: All Inputs are 3.3V LVTTL compatible; S/T = Schmitt Trigger inputs; SLC = Slew Rate Controller Output

JRC **NJM2566A**

6CH VIDEO AMPLIFIER WITH SD/ HD LPF

■ GENERAL DESCRIPTION

The NJM2566A is a single supply voltage 6ch Video amplifier.

It includes LPF, Y/C MIX circuit and SDC interface. LPF for the component signal can select SD/HD.

The NJM2566A is suitable for DVD recorder, set top box and the high quality AV systems with the SD/HD output.

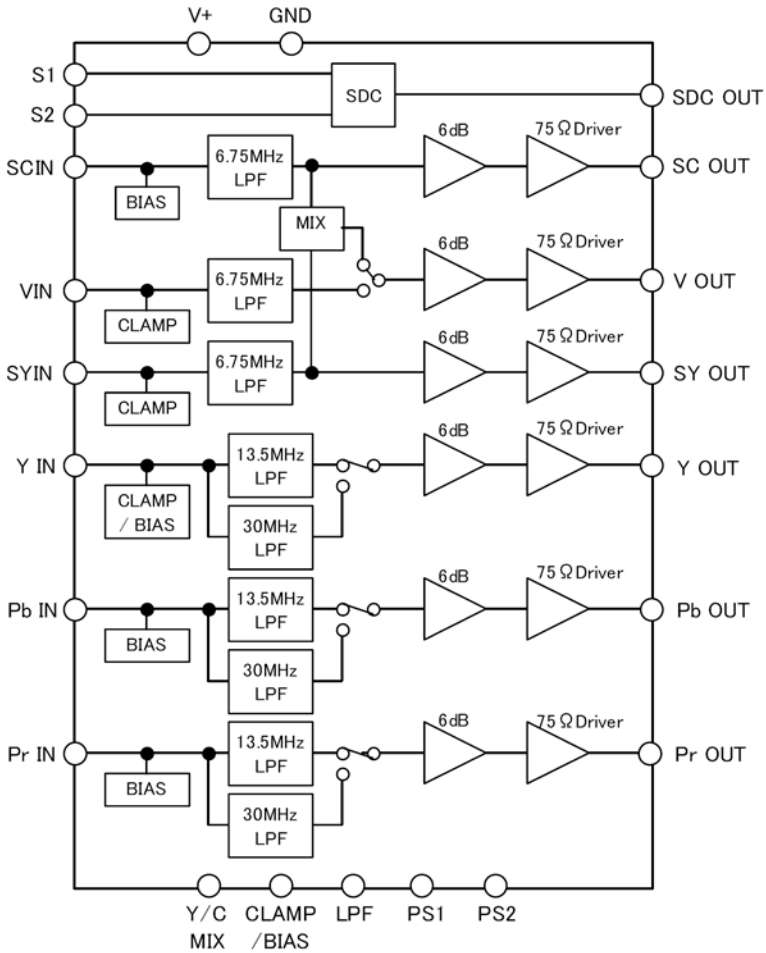
■ PACKAGE OUTLINE

NJM2566AV

■ FEATURES

- Operating Voltage 4.5 to 5.5V
- 6dB amplifier
- Internal 75Ω Driver Circuit (2-system drive)
- Internal LPF V,SY,SC 6.75MHz
  Y,Pb,Pr 13.5MHz (Progressive)
  30MHz (HD)
- Y/C MIX Circuit
- SDC Interface (S1/ S2)
- CLAMP/ BIAS Select (Y,Pb,Pr/ RGB)
- Power Save Circuit
- Bipolar Technology
- Package Outline SSOP32

■ BLOCK DIAGRAM



JRC **NJM2566A**

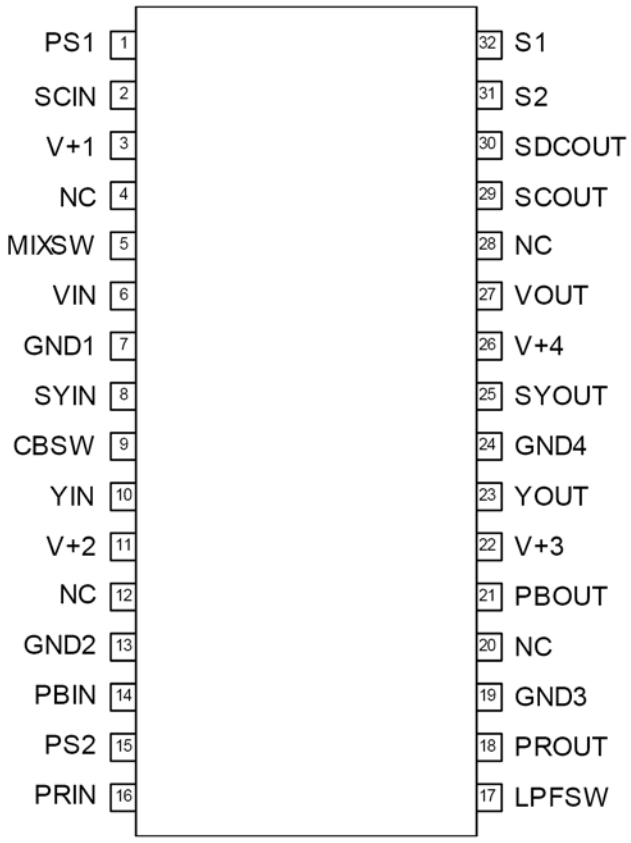
■ **CONTROL TERMINAL**

PARAMETER	STATUS	NOTE
PS1 (Power Save1)	H	(SYOUT, VOUT, SCOUT) Power Save: OFF
	L	(SYOUT, VOUT, SCOUT) Power Save: ON
	OPEN	(SYOUT, VOUT, SCOUT) Power Save: ON
PS2 (Power Save2)	H	(YOUT, PbOUT, PrOUT) Power Save: OFF
	L	(YOUT, PbOUT, PrOUT) Power Save: ON
	OPEN	(YOUT, PbOUT, PrOUT) Power Save: ON
MIX SW (Y/C MIX)	H	M/C MIX ON
	L	M/C MIX OFF
	OPEN	M/C MIX OFF
C/B SW (CLAMP/BIAS)	H	BIAS (RGB)
	L	CLAMP (Y,Pb,Pr)
	OPEN	CLAMP (Y,Pb,Pr)
LPF SW (LPF)	H	30MHz LPF
	L	13.5MHz LPF
	OPEN	13.5MHz LPF

■ **SDC OUT**

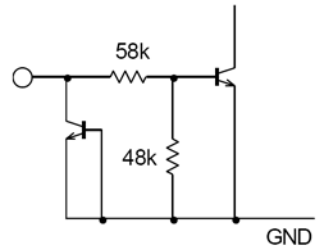
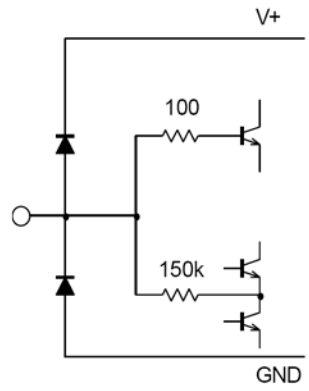
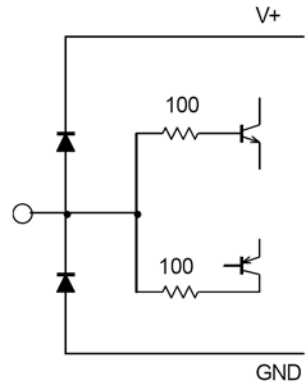
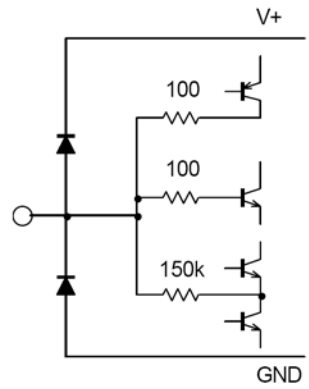
S1	S2	SDC OUT	
L (OPEN)	L (OPEN)	0V	4:3 Normal
L (OPEN)	H	2.1V	4:3 Letter box
H	H	2.1V	4:3 Letter box
H	L (OPEN)	4.6V	16:9 Squeeze

■ **PIN CONFIGURATION**

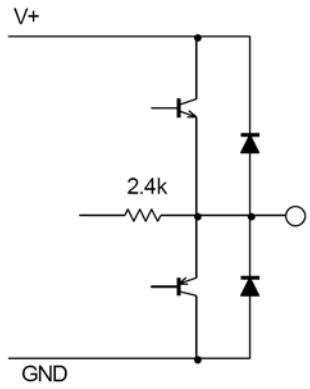
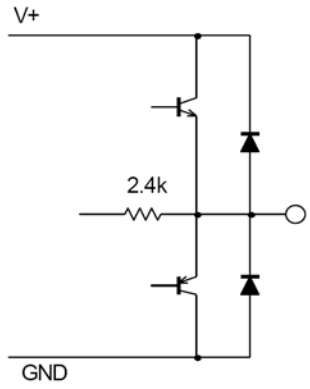
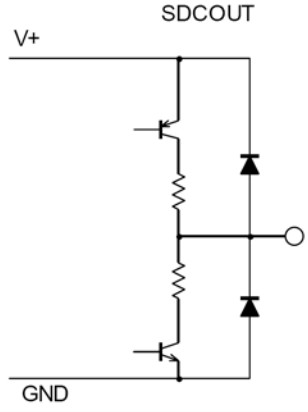


JRC **NJM2566A**

■ **TERMINAL FUNCTION**

PIN No.	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT	DC VOLTAGE
1 5 9 15 17 31 32	PS1 MIXSW CBSW PS2 LPFSW S2 S1	(SY, V, SC, SDC) Power save Y/C MIX control CLAMP/ BIAS control (Y, Pb, Pr) Power save (Y, Pb, Pr) LPF control SDC control SDC control		-
2 14 16	SCIN PBIN PRIN	Chroma signal input Component signal(Pb), R input Component signal(Pr), B input		2.5V
6 8	VIN SYIN	Composite video signal input Y signal input		1.7V
10	YIN	Component signal(Y), G input (Note) Y signal: CLAMP G signal: BIAS		(CLAMP) 1.7V (BIAS) 2.5V

JRC **NJM2566A**

PIN No.	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT	DC VOLTAGE
18 21 29	PROUT PBOUT SCOUT	Component signal(Cr) output Component signal(Cb) output Chroma signal output		2.5V
23 25 27	YOUT SYOUT VOUT	Component signal(Y) output Y signal output Composite video signal output		1.3V (Note) YOUT BIAS: 2.5V
30	SDCOUT	SDC output		-

NJW1197FC2
[8-CHANNEL ELECTRONIC VOLUME WITH INPUT SELECTOR]

[STRUCTURE] Bi-CMOS
[CATEGORIES] 3D Surround & Sound Enhancement
[PACKAGE OUTLINE] QFP100-C2
[SOLDERING METHOD] For this device, soldering method is recommended Reflow.
[NOTE] —

BAE-45919-000-00

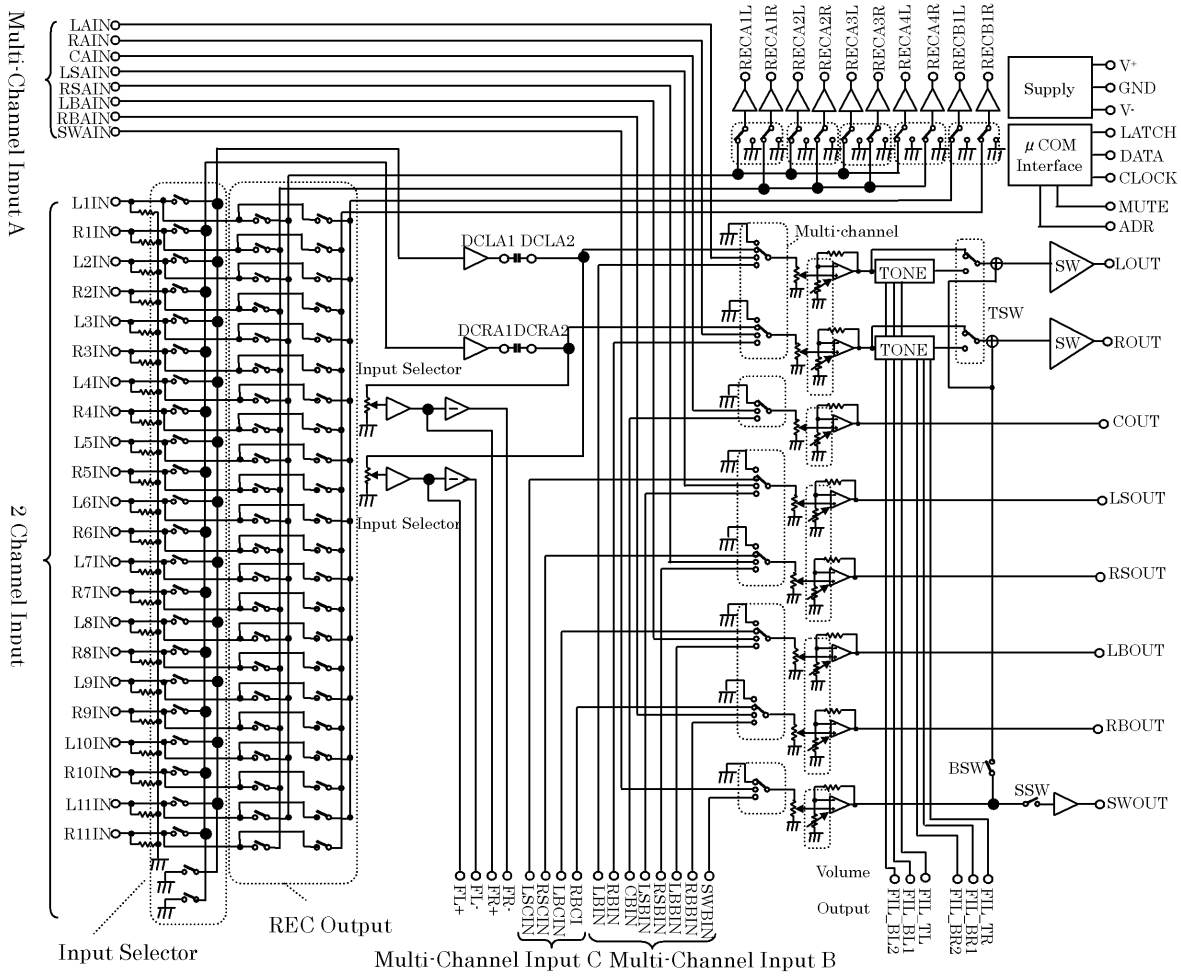
■ABSOLUTE MAXIMUM RATINGS Ta=25℃

Power Supply Voltage ····· +8/-8 [V]	Operating Temperature Range ····· -40 to +75 [℃]
Maximum Input Voltage ····· V^+/V^- [V]	Storage Temperature Range ····· -40 to +150 [℃]
Power Dissipation ····· 1600 [mW] (Note)	

(Note) EIA/JEDEC STANDARD Test board (76.2×114.3×1.6mm, 2layer, FR-4) mounting.

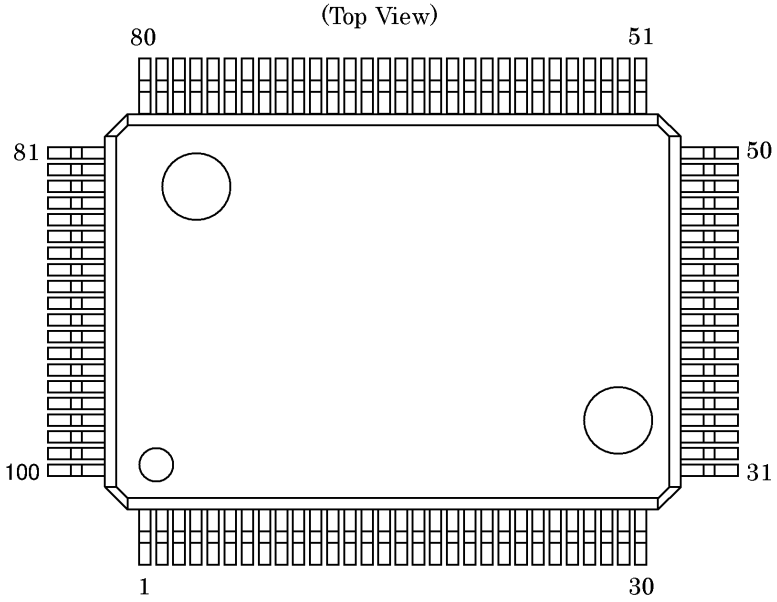
■BLOCK DIAGRAM

BDE-45919-000-00



■PIN CONFIGURAITON

BEE-45919-000-00



No.	SYMBOL	No.	SYMBOL	No.	SYMBOL	No.	SYMBOL
1	ROUT	26	DCCAP_RS	51	DCR_IN	76	GND
2	COUT	27	L3IN	52	DCR_OUT	77	LSCIN
3	LSOUT	28	DCCAP_LS	53	GND	78	RSCIN
4	RSOUT	29	R3IN	54	DCL_IN	79	LBCIN
5	LBOUT	30	DCCAP_C	55	DCL_OUT	80	RBCIN
6	RBOUT	31	L4IN	56	GND	81	GND
7	SWOUT	32	DCCAP_R	57	REC_B1R	82	LAIN
8	GND	33	R4IN	58	REC_B1L	83	RAIN
9	FIL_BL2	34	DCCAP_L	59	REC_A4R	84	CAIN
10	FIL_BL1	35	L5IN	60	REC_A4L	85	LSAIN
11	FIL_TL	36	GND	61	REC_A3R	86	RSAIN
12	TCAP	37	R5IN	62	REC_A3L	87	LBAIN
13	FIL_BR2	38	GND	63	REC_A2R	88	RBAIN
14	FIL_BR1	39	L6IN	64	REC_A2L	89	SWAIN
15	FIL_TR	40	L9IN	65	REC_A1R	90	GND
16	V^+	41	R6IN	66	REC_A1L	91	LBIN
17	ADR	42	R9IN	67	VDDOUT	92	RBIN
18	V^-	43	L7IN	68	DATA	93	CBIN
19	L1IN	44	L10IN	69	CLOCK	94	LSBIN
20	DCCAP_SW	45	R7IN	70	LATCH	95	RSBIN
21	R1IN	46	R10IN	71	MUTE	96	LBBIN
22	DCCAP_RB	47	L8IN	72	FL+	97	RBBIN
23	L2IN	48	L11IN	73	FL-	98	SWBIN
24	DCCAP_LB	49	R8IN	74	FR+	99	GND
25	R2IN	50	R11IN	75	FR-	100	LOUT

■FUNCTIONAL DESCRIPTION

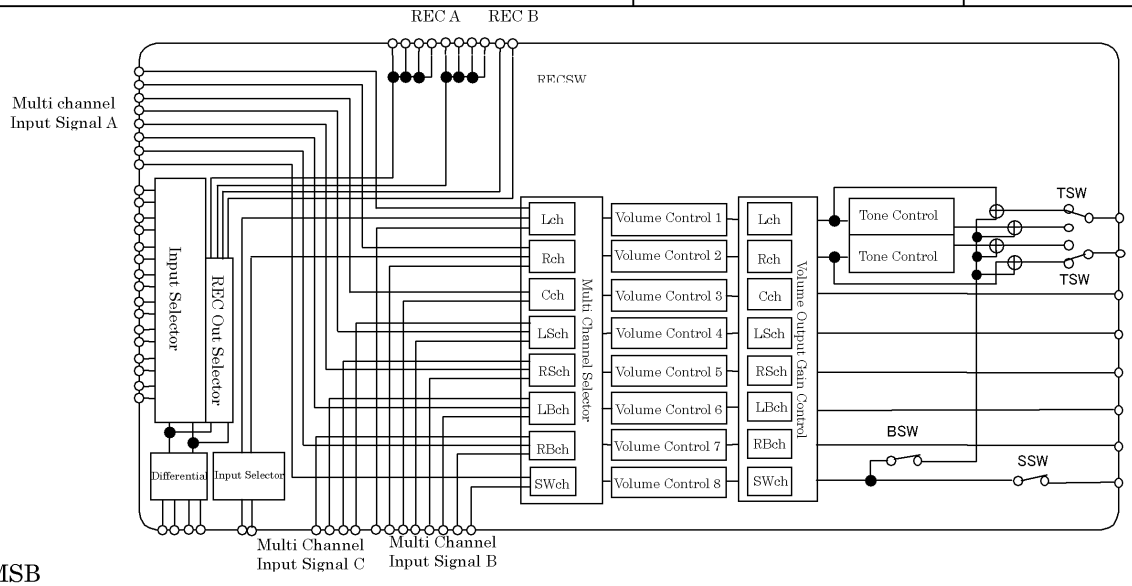
BGE-45919-000-00

(1) CONTROL DATA

NJW1197 control data is constructed with 16bits.

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data								Select Address				Chip Address			



MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L channel Volume Control								0	0	0	0	*	*	*	*
R channel Volume Control								0	0	0	1	*	*	*	*
C channel Volume Control								0	0	1	0	*	*	*	*
LS channel Volume Control								0	0	1	1	*	*	*	*
RS channel Volume Control								0	1	0	0	*	*	*	*
LB channel Volume Control								0	1	0	1	*	*	*	*
RB channel Volume Control								0	1	1	0	*	*	*	*
SW channel Volume Control								0	1	1	1	*	*	*	*
Input Selector Gain Control			Input Selector				SSW	1	0	0	0	*	*	*	*
TC/B	Tone Control Treble				TSW	BSW	*	1	0	0	1	*	*	*	*
BC/B	Tone Control Bass				*	*	*	1	0	1	0	*	*	*	*
REC B Selector				Input Selector				1	0	1	1	*	*	*	*
SWch Volume Output Gain Control		REC B1	REC A4	REC A3	REC A2	REC A1		1	1	0	0	*	*	*	*
L, Rch Volume Output Gain Control		Cch, Volume Output Gain Control			*	*		1	1	0	1	*	*	*	*
LS, RSch Volume Output Gain Control		LB, RBch Volume Output Gain Control			SWch Selector			1	1	1	0	*	*	*	*
L, Rch Selector		Cch Selector		LS, RSch Selector		LB, RBch Selector		1	1	1	1	*	*	*	*

*: Don't Care

* Chip address is set by chip address select terminal (ADR) status.

Chip Address Select Terminal (ADR: 17pin)	Chip Address			
	D3	D2	D1	D0
Low	0	1	0	0
High	0	1	0	1

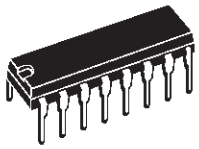
* The mute function can be controlled externally. If the Mute control terminal (71pin) is switched to High, Multi-Channel outputs are muted immediately (hardware mute).

External mute control terminal (MUTE: 71pin)	Setting
Low	Mute cancellation
High	Mute

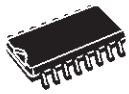
ST232

5V POWERED MULTI-CHANNEL RS-232 DRIVERS AND RECEIVERS

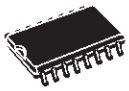
- SUPPLY VOLTAGE RANGE: 4.5 TO 5.5V
- SUPPLY CURRENT NO LOAD (TYP): 5mA
- TRANSMITTER OUTPUT VOLTAGE SWING (TYP): ±7.8V
- CONTROLLED OUTPUT SLEW RATE
- RECEIVER INPUT VOLTAGE RANGE: ±30V
- DATA RATE (TYP): 220Kbps
- OPERATING TEMPERATURE RANGE: -40 TO 85 °C, 0 TO 70 °C
- COMPATIBLE WITH MAX232 AND MAX202



N
(Plastic Package)



D
(Micro Package)



W
(Micro Package Large)

T
(TSSOP Package)

DESCRIPTION

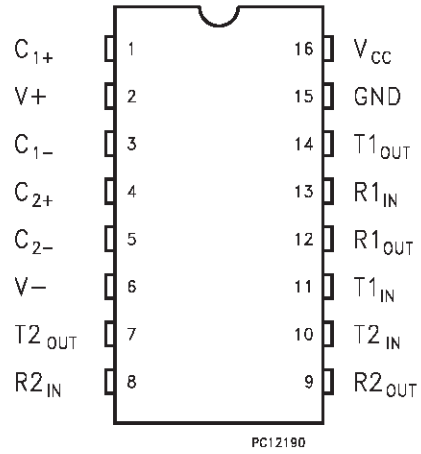
The ST232 is a 2 driver, 2 receiver device following EIA/TIA-232 and V.28 communication standard. It is particularly suitable for applications where ±12V is not available. The ST232 uses a single 5V power supply and only four external capacitors (0.1µF). Typical applications are in: Portable Computers, Low Power Modems, Interfaces Translation, Battery Powered RS-232 System, Multi-Drop RS-232 Networks.

ORDER CODES

Type	Temperature Range	Package	Comments
ST232CN	0 to 70 °C	DIP-16	25 parts per tube / 40 tube per box
ST232BN	-40 to 85 °C	DIP-16	25 parts per tube / 40 tube per box
ST232CD	0 to 70 °C	SO-16 (Tube)	50 parts per tube / 20 tube per box
ST232BD	-40 to 85 °C	SO-16 (Tube)	50 parts per tube / 20 tube per box
ST232CDR	0 to 70 °C	SO-16 (Tape & Reel)	2500 parts per reel
ST232BDR	-40 to 85 °C	SO-16 (Tape & Reel)	2500 parts per reel
ST232CW	0 to 70 °C	SO-16 Large (Tube)	49 parts per tube / 25 tube per box
ST232BW	-40 to 85 °C	SO-16 Large (Tube)	49 parts per tube / 25 tube per box
ST232CWR	0 to 70 °C	SO-16 Large (Tape & Reel)	1000 parts per reel
ST232BWR	-40 to 85 °C	SO-16 Large (Tape & Reel)	1000 parts per reel
ST232CT	0 to 70 °C	TSSOP16 (Tube)	only for samples
ST232BT	-40 to 85 °C	TSSOP16 (Tube)	only for samples
ST232CTR	0 to 70 °C	TSSOP16 (Tape & Reel)	2500 parts per reel
ST232BTR	-40 to 85 °C	TSSOP16 (Tape & Reel)	2500 parts per reel

ST232

PIN CONFIGURATION



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	C_1+	Positive Terminal for the first Charge Pump Capacitor
2	V+	Doubled Voltage Terminal
3	C_1-	Negative Terminal for the first Charge Pump Capacitor
4	C_2+	Positive Terminal for the second Charge Pump Capacitor
5	C_2-	Negative Terminal for the second Charge Pump Capacitor
6	V-	Inverted Voltage Terminal
7	$T2_{OUT}$	Second Transmitter Output Voltage
8	$R2_{IN}$	Second Receiver Input Voltage
9	$R2_{OUT}$	Second Receiver Output Voltage
10	$T2_{IN}$	Second Transmitter Input Voltage
11	$T1_{IN}$	First Transmitter Input Voltage
12	$R1_{OUT}$	First Receiver Output Voltage
13	$R1_{IN}$	First Receiver Input Voltage
14	$T1_{OUT}$	First Transmitter Output Voltage
15	GND	Ground
16	V_{CC}	Supply Voltage

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.3 to 6	V
T_{IN}	Transmitter Input Voltage Range	-0.3 to (V_{CC} + 0.3)	V
R_{IN}	Receiver Input Voltage Range	±30	V
T_{OUT}	Transmitter Output Voltage Range	(V+ + 0.3) to (V- - 0.3)	V
R_{OUT}	Receiver Output Voltage Range	-0.3 to (V_{CC} + 0.3)	V
T_{SCTOUT}	Short Circuit Duration on T_{OUT}	infinite	
T_{stg}	Storage Temperature Range	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
Note1: No external supply can be applied to V+ terminal and V- terminal.

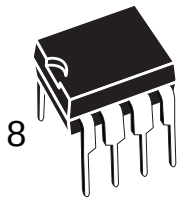
M24C64
M24C32

64Kbit and 32Kbit Serial I²C Bus EEPROM

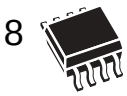
FEATURES SUMMARY

- Two-Wire I^2C Serial Interface
  Supports 400kHz Protocol
- Single Supply Voltage:
  - 4.5 to 5.5V for M24Cxx
  - 2.5 to 5.5V for M24Cxx-W
  - 1.8 to 5.5V for M24Cxx-R
- Write Control Input
- BYTE and PAGE WRITE (up to 32 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Protection
- More than 1 Million Erase/Write Cycles
- More than 40-Year Data Retention

Figure 1. Packages



PDIP8 (BN)



SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

UFDFPN8 (MB)
2x3mm² (MLP)

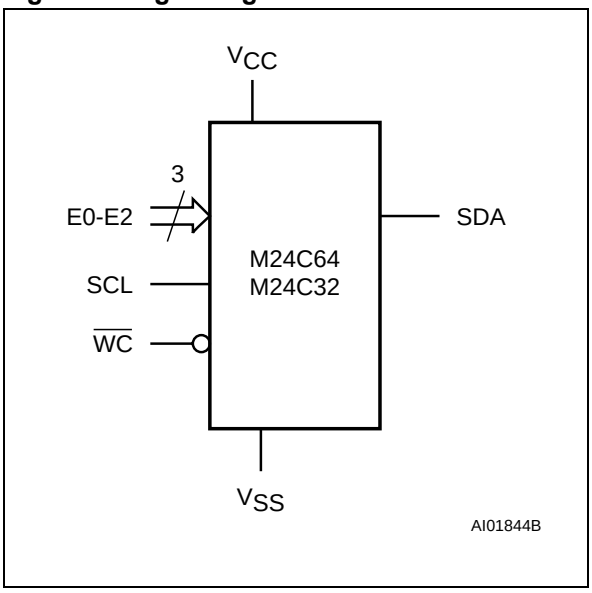
Table 1. Product List

Reference	Part Number
M24C64	M24C64
	M24C64-W
	M24C64-R
M24C32	M24C32
	M24C32-W
	M24C32-R

SUMMARY DESCRIPTION

These I^2C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 8192 x 8 bits (M24C64) and 4096 x 8 bits (M24C32).

Figure 2. Logic Diagram



I^2C uses a two-wire serial interface, comprising a bi-directional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a Device Select Code and Read/Write bit (RW) (as described in Table 3.), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Table 2. Signal Names

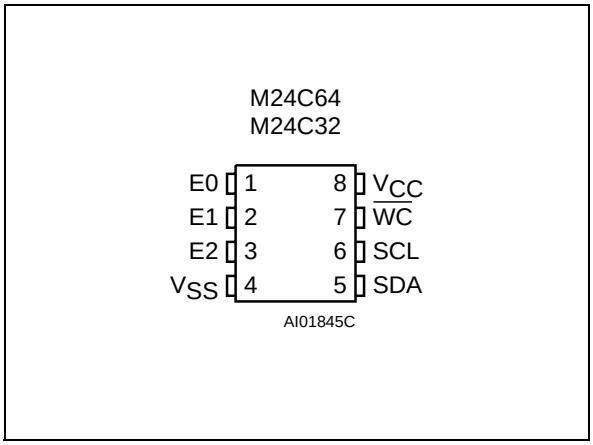
E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. At Power-up, the internal reset is held active until V_{CC} has reached the Power On Reset (POR) threshold voltage, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the Power On Reset (POR) threshold voltage, all operations are disabled and the device will not respond to any command.

A stable and valid V_{CC} (as defined in Table 9. and Table 10.) must be applied before applying any logic signal.

Figure 3. DIP, SO, TSSOP and UFDFPN Connections



Note: See PACKAGE MECHANICAL section for package dimensions, and how to identify pin-1.

KEC

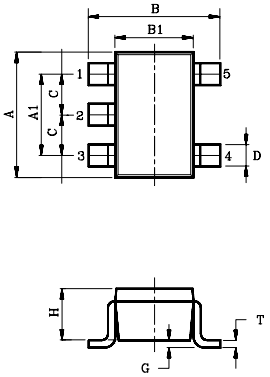
SEMICONDUCTOR
TECHNICAL DATA

KIC7SZ08FU
SILICON MONOLITHIC CMOS
DIGITAL INTEGRATED CIRCUIT

2 INPUT AND GATE

FEATURES

- High Output Drive : ±24mA (Typ.)
  @V_{CC}=3V
- Super High Speed Operation : t_{PD}=2.7ns(Typ.)
  @V_{CC}=5V, 50pF
- Operation Voltage Range : $V_{CC(opr)}$=1.8~5.5V.
- Supply Voltage Data Retention : V_{CC}=1.5~5.5V.
- 5V Tolerant Function



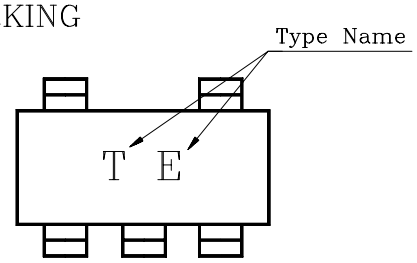
DIM	MILLIMETERS
A	2.00± 0.20
A1	1.3± 0.1
B	2.1± 0.1
B1	1.25± 0.1
C	0.65
D	0.2+0.10/−0.05
G	0~0.1
H	0.9± 0.1
T	0.15+0.1/−0.05

USV

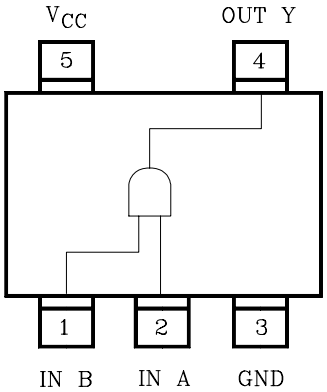
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~6	V
DC Input Voltage	V_{IN}	-0.5~6	V
DC Output Voltage	V_{OUT}	-0.5~6	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	200	mW
Storage Temperature	T_{stg}	-65~150	℃
Lead Temperature (10s)	T_L	260	℃

MARKING



PIN CONNECTION(TOP VIEW)



JRC **NJM2845/46**

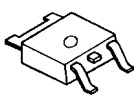
LOW DROPOUT VOLTAGE REGULATOR

■ GENERAL DESCRIPTION

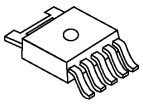
The NJM2845 is low dropout voltage regulator. Advanced Bipolar technology achieves low noise, high ripple rejection and low quiescent current.

NJM2845 is 3 terminal type and NJM2846 is ON/OFF control built in type. These product can be selected according to the applications.

■ PACKAGE OUTLINE



NJM2845DL1

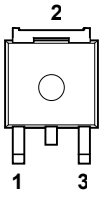


NJM2846DL3

■ FEATURES

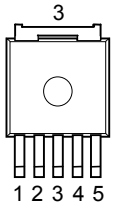
- High Ripple Rejection 75dB typ. (f=1kHz,3V Version)
- Output Noise Voltage Vno=45μVrms typ. (Vo=3V Version)
- Output capacitor with 2.2μF ceramic capacitor (Vo≥2.6V)
- Output Current Io(max.)=800mA
- High Precision Output Vo ±1.0%
- Low Dropout Voltage 0.18V typ. (Io=500mA)
- ON/OFF Control (NJM2846)
- Internal Short Circuit Current Limit
- Internal Thermal Overload Protection
- Bipolar Technology
- Package Outline TO-252-3 (NJM2845DL1), TO-252-5 (NJM2846DL3)

■ PIN CONFIGURATION



1.V_{IN}
2.GND
3.V_{OUT}

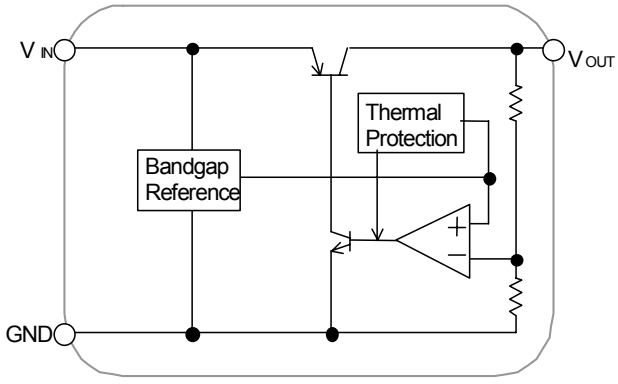
NJM2845DL1



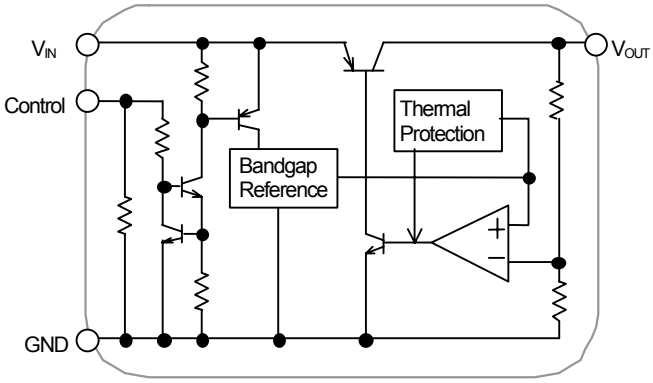
1.CONTROL
2.V_{IN}
3.GND
4.Vo
5.NC

NJM2846DL3

■ EQUIVALENT CIRCUIT



NJM2845DL1



NJM2846DL3

TOSHIBA TC74VHC157F/FN/FT

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC157F, TC74VHC157FN, TC74VHC157FT

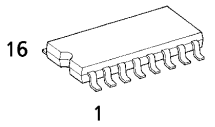
QUAD 2 - CHANNEL MULTIPLEXER

(Note) The JEDEC SOP (FN) is not available in Japan.

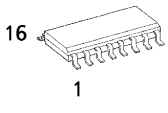
The TC74VHC157 is an advanced high speed CMOS QUAD 2 - CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
It consists of four 2 - input digital multiplexers with common select and strobe inputs.
When the $\overline{STROBE}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level.
The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.
An Input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

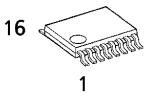
- High Speed ····· t_{pd} = 4.1ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr) = 2V ~ 5.5V
- Low Noise ····· V_{OLP} = 0.8V (Max.)
- Pin and Function Compatible with 74ALS157



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

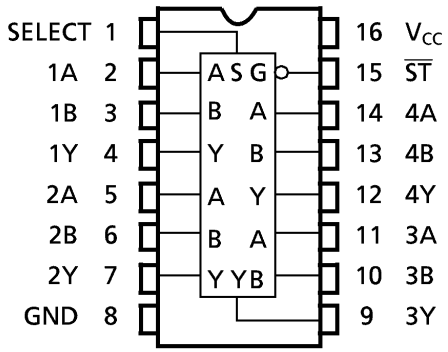


FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)



FT (TSSOP16-P-0044-0.65)
Weight : 0.06g (Typ.)

PIN ASSIGNMENT



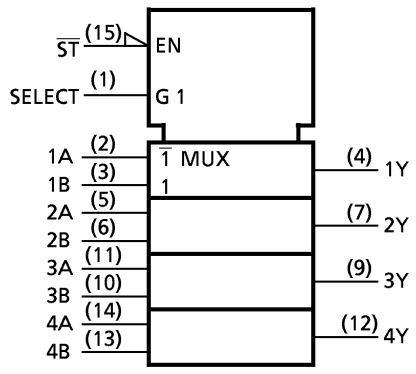
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUT
$\overline{ST}$	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

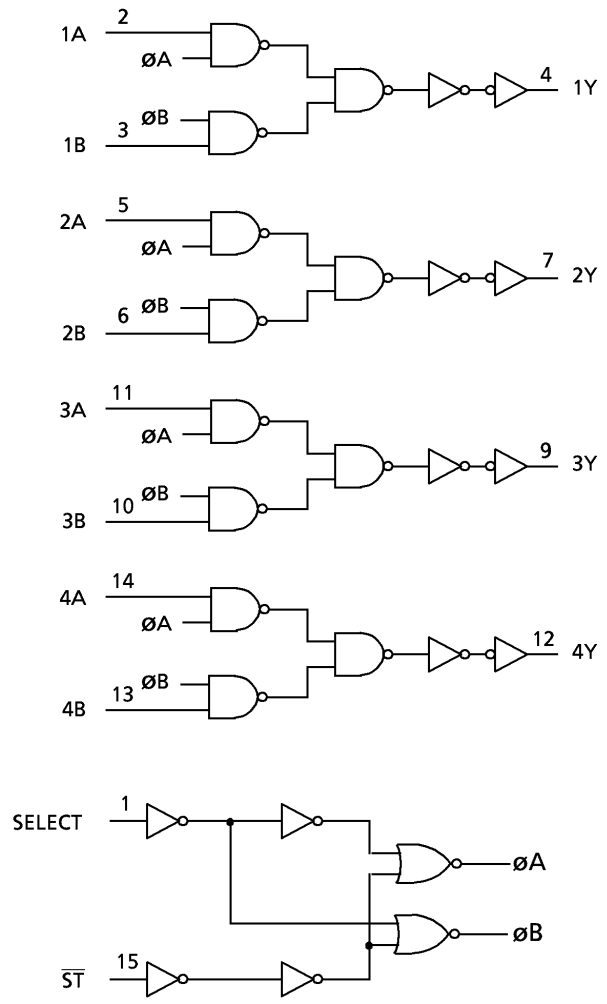
X : Don't Care

IEC LOGIC SYMBOL



980910EBA2

SYSTEM DIAGRAM



TOSHIBA TC74LCX541F/FW/FT

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

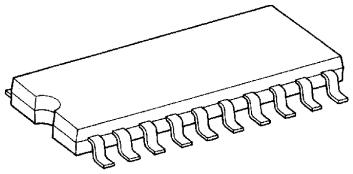
TC74LCX541F, TC74LCX541FW, TC74LCX541FT

LOW VOLTAGE OCTAL BUS BUFFER
WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX541 is a high performance CMOS OCTAL BUS BUFFER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.
The 74LCX541 is a non-inverting 3-state buffer having two active-low output enables. When either $\overline{OE}1$ or $\overline{OE}2$ are high, the terminal outputs are in the high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge.

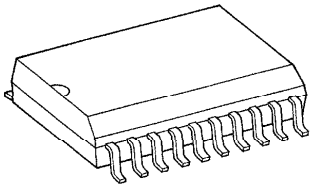
(Note) The JEDEC SOP (FW) is not available in Japan.

TC74LCX541F



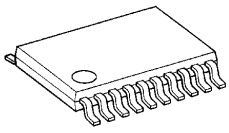
SOP20-P-300-1.27

TC74LCX541FW



SOL20-P-300-1.27

TC74LCX541FT



TSSOP20-P-0044-0.65

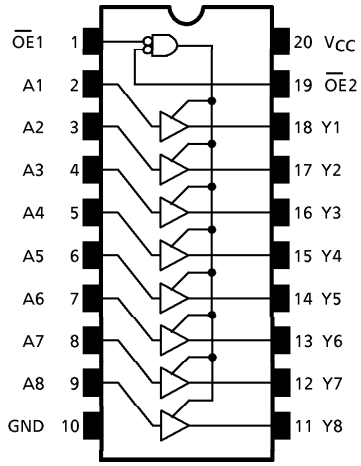
FEATURES

- Low voltage operation : $V_{CC} = 2.0 \sim 3.6V$
- High speed operation : t_{pd} = 6.5ns (Max.) ($V_{CC} = 3.0 \sim 3.6V$)
- Output current : $|I_{OH}| / I_{OL}$ = 24mA (Min.) ($V_{CC} = 3.0V$)
- Latch-up performance : ±500mA
- Available in JEDEC SOP, EIAJ SOP and TSSOP
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC / VHC / HC / F / ALS / LS etc.) 541 type.

Weight
SOP20-P-300-1.27 : 0.22g (Typ.)
SOL20-P-300-1.27 : 0.46g (Typ.)
TSSOP20-P-0044-0.65 : 0.08g (Typ.)

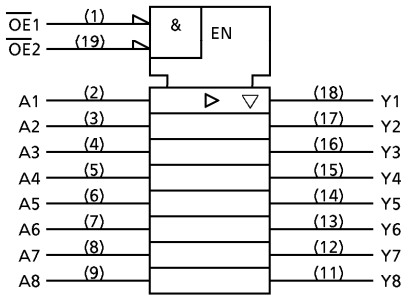
961001EBA2

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}1$	$\overline{OE}2$	An	
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

X : Don't Care
Z : High Impedance

MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~7.0 (Note 1)	V
		−0.5~V_{CC}+0.5 (Note 2)	
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (Note 3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	180	mW
DC V_{CC}/Ground Current	I_{CC} / I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

(Note 1) Output in Off-State
(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.
(Note 3) V_{OUT}<GND, V_{OUT}>V_{CC}

961001EBA2'

TOSHIBA TC74VHCT14AF/AFN/AFT

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

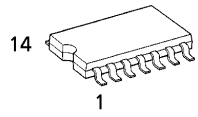
TC74VHCT14AF, TC74VHCT14AFN, TC74VHCT14AFT

HEX SCHMITT INVERTER

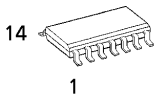
The TC74VHCT14A is an advanced high speed CMOS SCHMITT INVERTER fabricated with silicon gate C2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
Pin configuration and function are the same as the TC74VHC04 but the inputs have hysteresis and with its schmitt trigger function, the TC74VHC14 can be used as a line receivers which will receive slow input signals.
The input voltage are compatible with TTL output voltage.
This device may be used as a level converter for interfacing 3.3V to 5V system.
Input protection and output circuit ensure that 0 to 5.5V can be applied to the input and output*1 pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input / output voltages such as battery back up, hot board insertion, etc.
*1: Vcc = 0V

FEATURES:
- High Speed ..... t_{pd} = 5.0ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 2μA(Max.) at Ta = 25°C
- Compatible with TTL outputs .... V_{IL} = 0.8V (Max.), V_{IH} = 2.0V (Min.)
- Power Down Protection is provided on all inputs and outputs.
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Low Noise ..... V_{OLP} = 0.8V (Max.)
- Pin and Function Compatible with the 74 series (74AC / HC / F / ALS / LS etc.) 14 type.

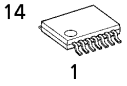
(Note) The JEDEC SOP (FN) is not available in Japan.



F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

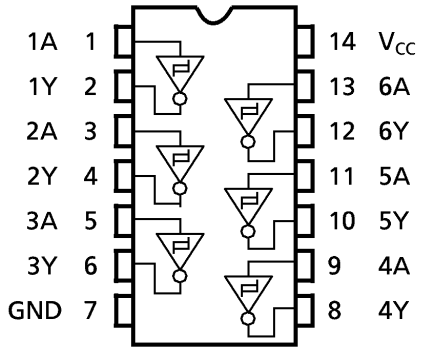


FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

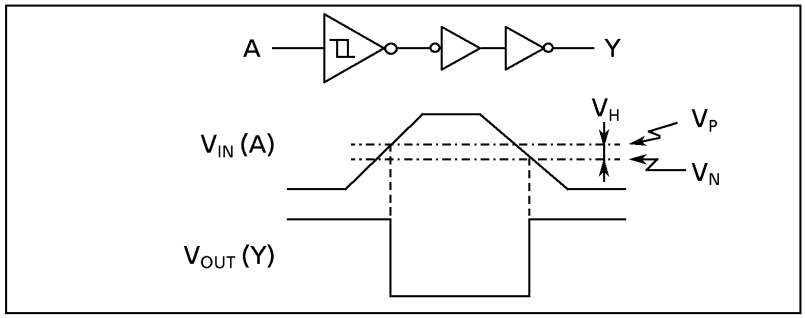


FT (TSSOP14-P-0044-0.65)
Weight : 0.06g (Typ.)

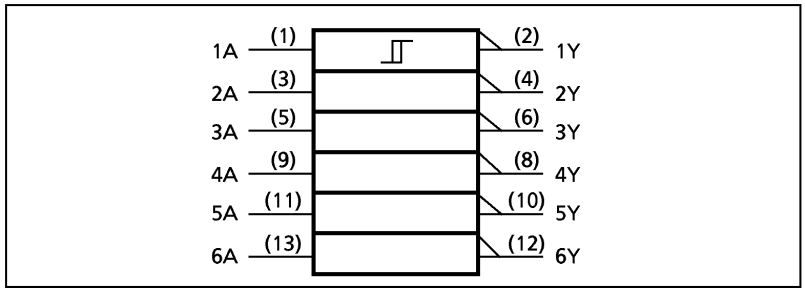
PIN ASSIGNMENT



SYSTEM DIAGRAM, WAVEFORM



IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

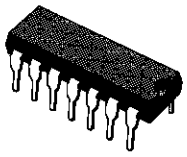
980910EBA2

SGS-THOMSON MICROELECTRONICS

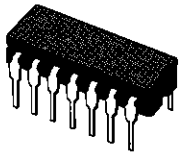
M54HCU04
M74HCU04

HEX INVERTER (SINGLE STAGE)

- HIGH SPEED
  t_{PD} = 5 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 10 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 54/74LS04



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

M54HCU04F1R M74HCU04M1R
M74HCU04B1R M74HCU04C1R

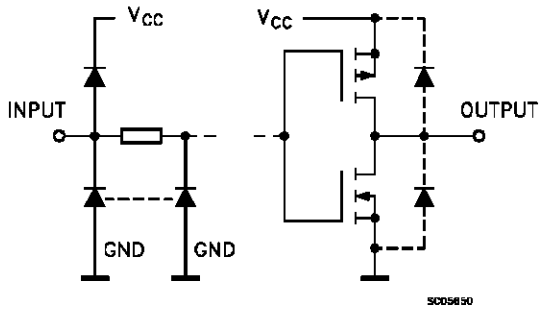
DESCRIPTION

The M54/74HCU04 is a high speed CMOS HEX INVERTER (SINGLE STAGE) fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

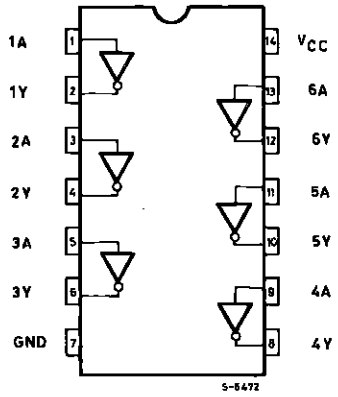
As the intrnal circuit is composed of a single stage inverter, it can be used in crystal oscillator.

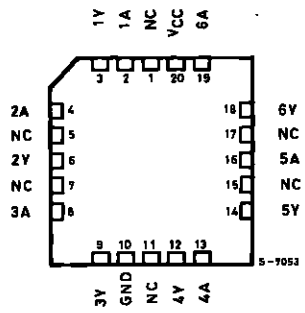
All inputs are equipped with circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



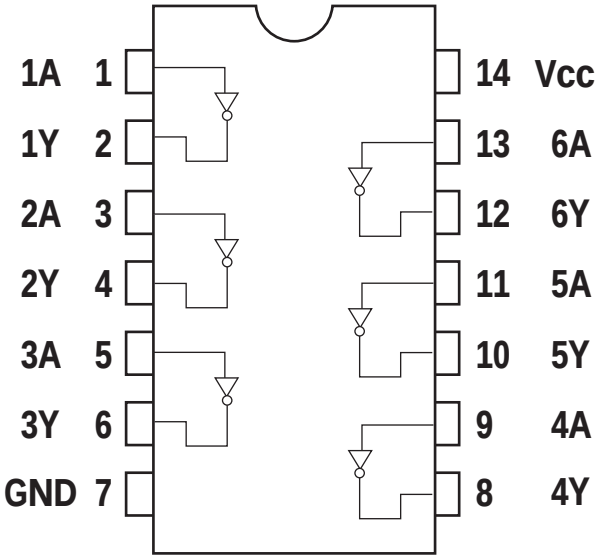
PIN CONNECTIONS (top view)



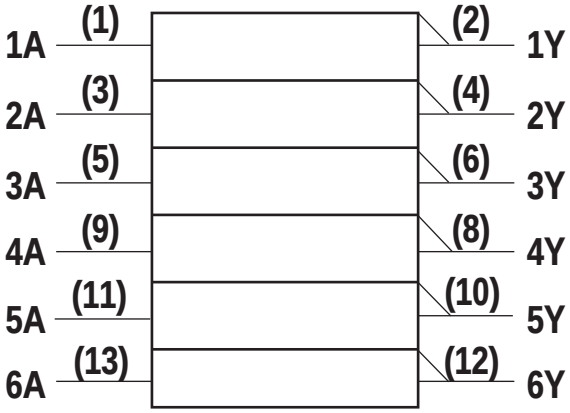


NC =
No Internal
Connection

■ PIN ASSIGNMENT (74HCU04AFN : IC72,76)



■ LOGIC SYMBOL



■ TRUTH TABLE

A	Y
L	H
H	L

CMOS 16-Bit Microcontrollers

T5CC1

1. Outline and Features

T5CC1 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

T5CC1 comes in a 100-pin flat package.

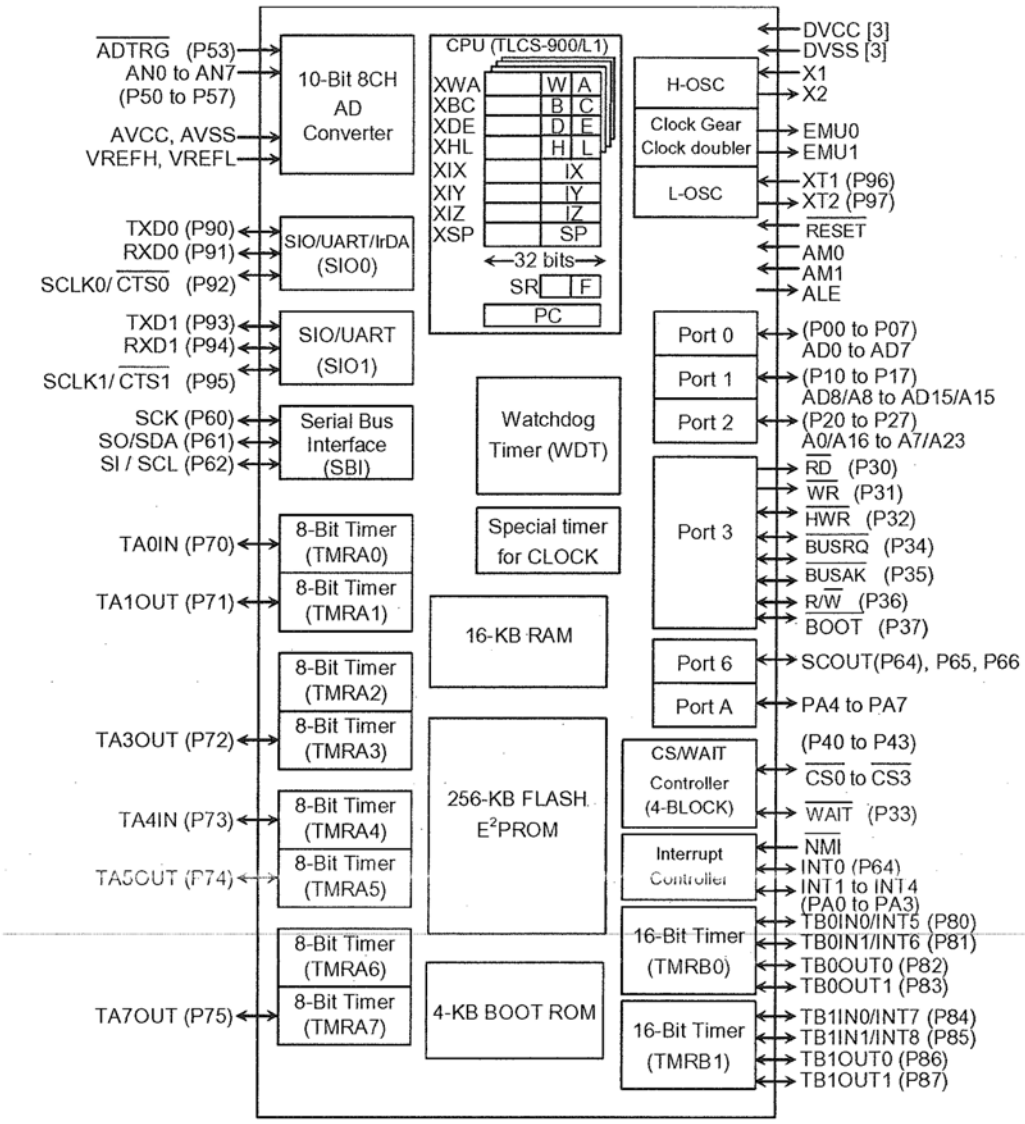
Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)

- Instruction mnemonics are upward-compatible with TLCS-90/900
- General-purpose registers and register banks
- 16 Mbytes of linear address space
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: 4-channels (593 ns/2 bytes at 27 MHz)

(2) Minimum instruction execution time: 148 ns (at 27 MHz)

(3) Built-in RAM: 16 Kbytes
Built-in ROM: 256 Kbytes Flash memory
4 Kbytes mask ROM (used for booting)



( ): Initial function after reset

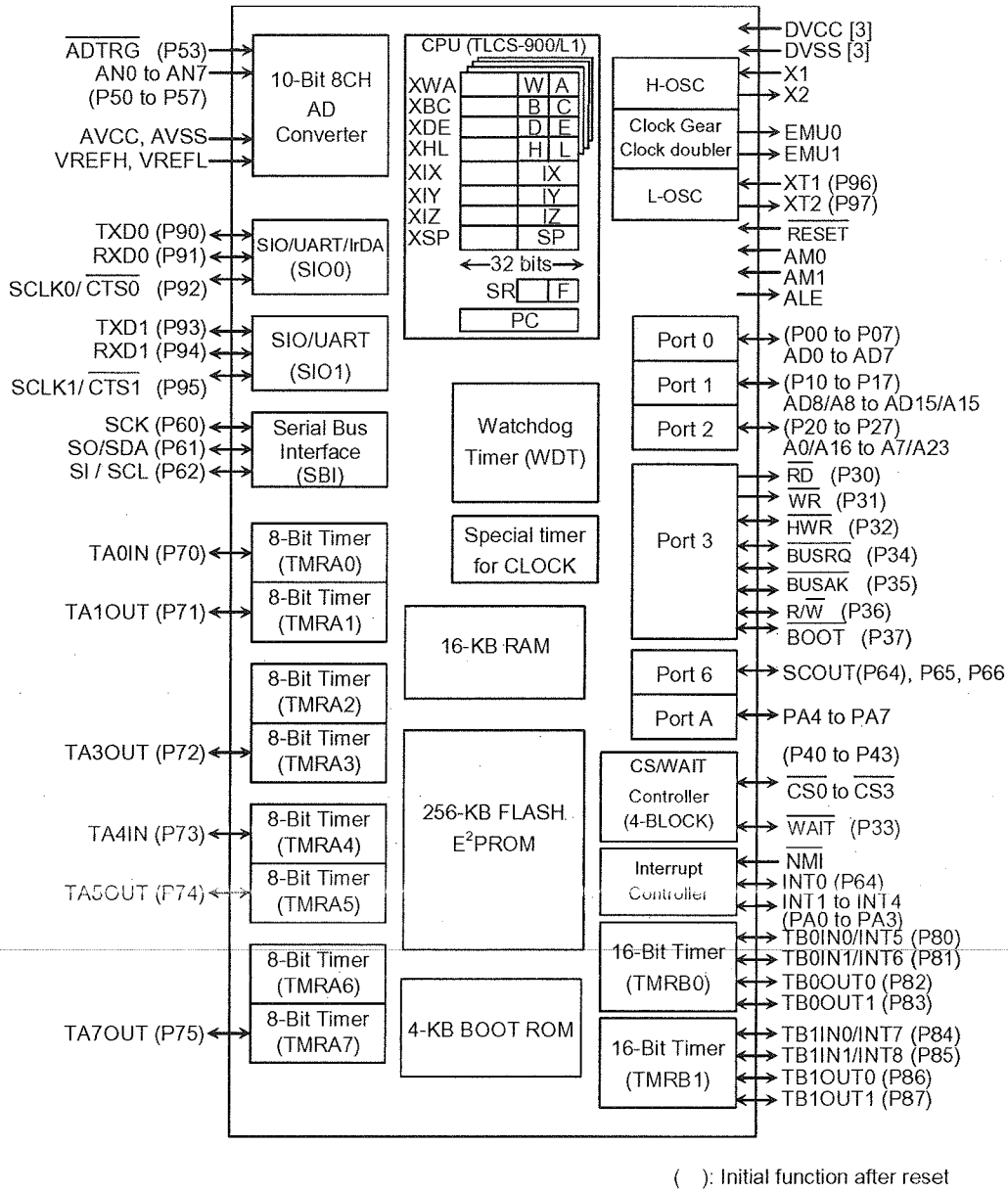


Figure 1.1 T5CC1 Block Diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the T5CC1, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the T5CC1.

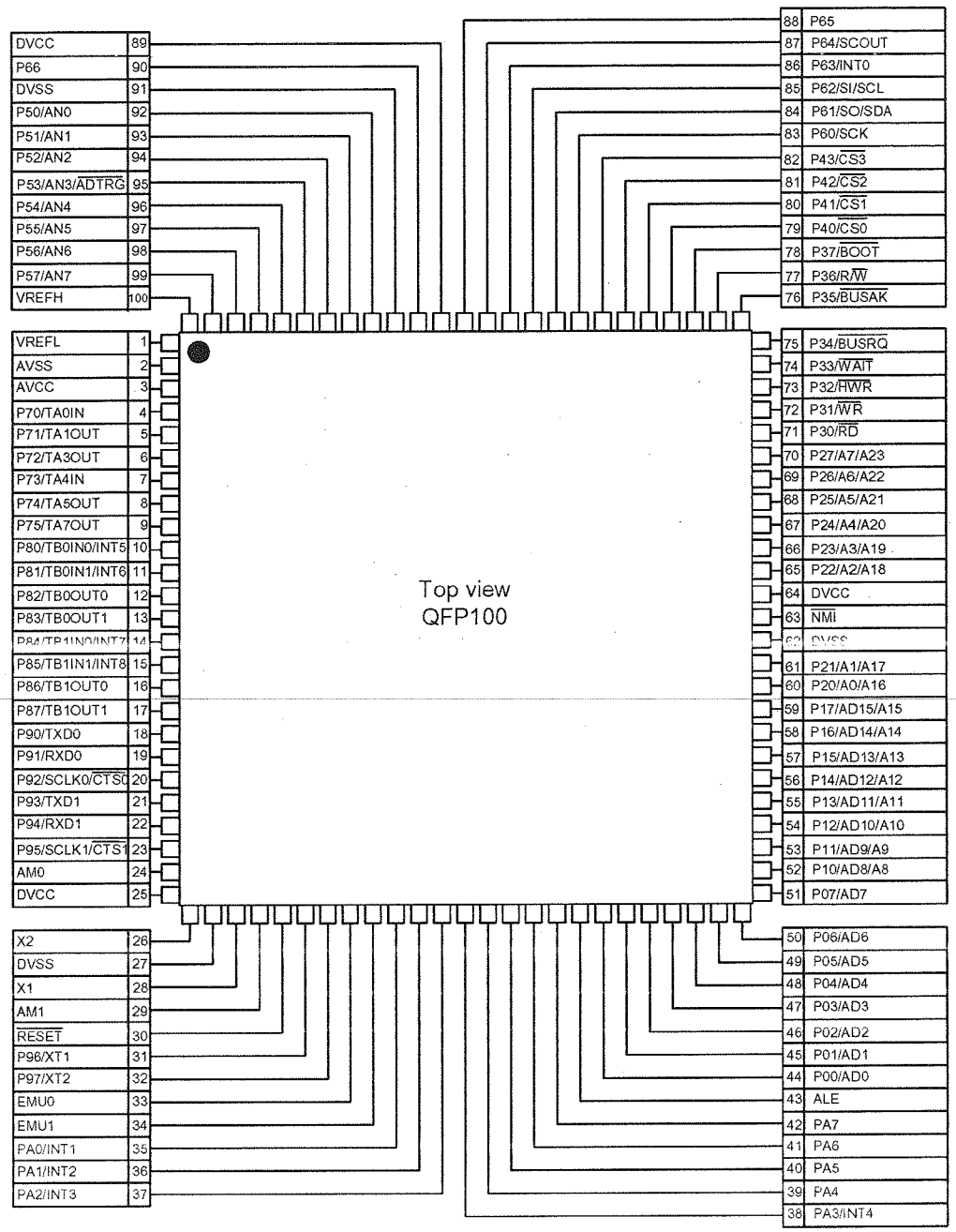


Figure 2.1.1 Pin assignment diagram (100-pin LQFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.
Table 2.2.1 Pin names and functions.

Table 2.2.1 Pin names and functions (1/3)

Pin Name	Number of Pins	I/O	Functions
P00~P07	8	I/O	Port 0: I/O port that allows I/O to be selected at the bit level
AD0~AD7		I/O	Address and data (lower): Bits 0 to 7 of address and data bus
P10~P17	8	I/O	Port 1: I/O port that allows I/O to be selected at the bit level
AD8~AD15		I/O	Address and data (upper): Bits 8 to 15 for address and data bus
A8~A15		Output	Address: Bits 8 to 15 of address bus
P20~P27	8	I/O	Port 2: I/O port that allows I/O to be selected at the bit level
A0~A7		Output	Address: Bits 0 to 7 of address bus
A16~A23		Output	Address: Bits 16 to 23 of address bus
P30	1	Output	Port 30: Output port
$\overline{RD}$		Output	Read: Strobe signal for reading external memory This port output RD signal also case of reading internal-area by setting P3 <P30> = 0 and P3FC <P30F> = 1.
P31	1	Output	Port 31: Output port
$\overline{WR}$		Output	Write: Strobe signal for writing data to pins AD0 to AD7
P32	1	I/O	Port 32: I/O port (with pull-up resistor)
$\overline{HWR}$		Output	High Write: Strobe signal for writing data to pins AD8 to AD15
P33	1	I/O	Port 33: I/O port (with pull-up resistor)
$\overline{WAIT}$		Input	Wait: Pin used to request CPU bus wait ((1+N) WAIT mode)
P34	1	I/O	Port 34: I/O port (with pull-up resistor)
BUSRQ		Input	Bus Request: Signal used to request Bus Release
P35	1	I/O	Port 35: I/O port (with pull-up resistor)
$\overline{BUSAK}$		Output	Bus Acknowledge: Signal used to acknowledge Bus Release
P36	1	I/O	Port 36: I/O port (with pull-up resistor)
R/$\overline{W}$		Output	Read/Write: 1 represents Read or Dummy cycle; 0 represents Write cycle.
P37	1	I/O	Port 36: I/O port (with pull-up resistor)
$\overline{BOOT}$		Input	This pin sets single boot mode. When released reset, Single boot mode is started at P37=Low level.
P40	1	I/O	Port 40: I/O port (with pull-up resistor)
$\overline{CS0}$		Output	Chip Select 0: Outputs 0 when address is within specified address area
P41	1	I/O	Port 41: I/O port (with pull-up resistor)
$\overline{CS1}$		Output	Chip Select 1: Outputs 0 if address is within specified address area
P42	1	I/O	Port 42: I/O port (with pull-up resistor)
$\overline{CS2}$		Output	Chip Select 2: Outputs 0 if address is within specified address area
P43	1	I/O	Port 43: I/O port (with pull-up resistor)
$\overline{CS3}$		Output	Chip Select 3: Outputs 0 if address is within specified address area
P50~P57	8	Input	Port 5: Pin used to input port
AN0~AN7		Input	Analog input: Pin used to input to AD converter
$\overline{ADTRG}$		Input	AD Trigger: Signal used to request start of AD converter (Shared with53 pin)

Table 2.2.1 Pin names and functions (2/3)

Pin Name	Number of Pins	I/O	Functions
P60 SCK	1	I/O I/O	Port 60: I/O port Serial bus interface clock in SIO Mode
P61 SO SDA	1	I/O Output I/O	Port 61: I/O port Serial bus interface send data at SIO mode Serial bus interface send/recive data at I^2C bus mode Open-drain output mode by programmable
P62 SI SCL	1	I/O Input I/O	Port 62: I/O port Serial bus interface recive data at SIO mode Serial bus interface clock I/O data at I^2C bus mode Open-drain output mode by programmable
P63 INT0	1	I/O Input	Port 63: I/O port Interrupt Request Pin 0: Interrupt request pin with programmable level / rising edge / falling edge
P64 SCOUT	1	I/O Output	Port 64: I/O port System Clock Output: Outputs f_{FPH} or fs clock.
P65	1	I/O	Port 65 I/O port
P66	1	I/O	Port 66 I/O port
P70 TA0IN	1	I/O Input	Port 70I/O port 8bitt timer 0 input:: Timer 0 input
P71 TA1OUT	1	I/O Output	Port 71I/O port 8-bit timer 1 output: Timer 0 or Timer 1 output
P72 TA3OUT	1	I/O Output	Port 72I/O port 8bit 8-bit timer 3 output: Timer 2 or Timer 3 output
P73 TA4IN	1	I/O Input	Port 73: I/O port 8-bit timer 4 input: Timer 4 input
P74 TA5OUT	1	I/O Output	Port 74: I/O port 8-bit timer 5 output: Timer 4 or Timer 5 output
P75 TA7OUT	1	I/O Output	Port 75: I/O port 88-bit timer 7 output: Timer 6 or Timer 7 output
P80 TB0IN0 INT5	1	I/O Input Input	Port 80: I/O port 16bit timer 0 input 0: 16bit Timer 0 count / capture trigger input Interrupt Request Pin 5: Interrupt request pin with programmable rising edge / falling edge.
P81 TB0IN1 INT6	1	I/O Input Input	Port 81: I/O port 16bit timer 0 input 1: 16bit Timer 0 count / capture trigger input Interrupt Request Pin 6: Interrupt request on rising edge
P82 TB0OUT0	1	I/O Output	Port 82: I/O port 16bit timer 0 output 0: 16bit Timer 0 output
P83 TB0OUT1	1	I/O Output	Port 83: I/O port 16bit timer 0 output 1: 16bit Timer 0 output
P84 TB1IN0 INT7	1	I/O Input Input	Port 84: I/O port 16bit timer 1 input 0: 16bit Timer 1 count / capture trigger input Interrupt Request Pin 7: Interrupt request pin with programmable rising edge / falling edge.
P85 TB1IN1 INT8	1	I/O Input Input	Port 85: I/O port 16bit timer 1 input 1: 16bit Timer 1 count / capture trigger input Interrupt Request Pin 8: Interrupt request on rising edge
P86 TB1OUT0	1	I/O Output	Port 86: I/O port 16bit timer 1 output 0: 16bit Timer 1 output 16bit
P87 TB1OUT1	1	I/O Output	Port 87: I/O port 16bit timer 1 output 1: 16bit Timer 1 output 16bit 16bit

Table 2.2.1 Pin names and functions (3/3)

Pin Name	Number of Pins	I/O	Functions
P90 TXD0	1	I/O Output	Port 90: I/O port Serial Send Data 0 (programmable open-drain)
P91 RXD0	1	I/O Input	Port 91: I/O port Serial Receive Data 0
P92 SCLK0 $\overline{\text{CTS0}}$	1	I/O I/O Input	Port 92: I/O port Serial Clock I/O 0 Serial Data Send Enable 0 (Clear to Send)
P93 TXD1	1	I/O Output	Port 93: I/O port Serial Send Data 1 (programmable open-drain)
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial Receive Data 1
P95 SCLK1 $\overline{\text{CTS1}}$	1	I/O I/O Input	Port 95: I/O port (with pull-up resistor) Serial Clock I/O 1 Serial Data Send Enable 1 (Clear to Send)
P96 XT1	1	I/O Input	Port 96: I/O port (open-drain output) Low-frequency oscillator connection pin
P97 XT2	1	I/O Output	Port 97: I/O port (open-drain output) Low-frequency oscillator connection pin
PA0~PA3 INT1~INT4	4	I/O Input	Ports A0 to A3: I/O ports Interrupt Request Pins 1 to 4: Interrupt request pins with programmable rising edge / falling edge.
PA4~PA7	4	I/O	Ports A4 to A7: I/O ports
ALE	1	Output	Address Latch Enable Can be disabled to reduce noise.
$\overline{\text{NMI}}$	1	Input	Non-Maskable Interrupt Request Pin: Interrupt request pin with programmable falling edge or both edge.
AM0~1	2	Input	Operation mode: Fixed to AM1 = 1, AM0 = 1
EMU0	1	Output	Open pin
EMU1	1	Output	Open pin
$\overline{\text{RESET}}$	1	Input	Reset: initializes T5CC1. (With pull-up resistor)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)
X1/X2	2	I/O	High-frequency oscillator connection pins
DVCC	3		Power supply pins (All DVCC pins should be connected with the power supply pin.)
DVSS	3		GND pins (0 V) (All DVSS pins should be connected with the power supply pin.)

Note: An external DMA controller cannot access the device's built-in memory or built-in I/O devices using the $\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$ signal.

JRC **NJM2595**

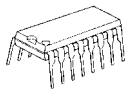
5-INPUT 3-OUTPUT VIDEO SWITCH

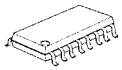
■ GENERAL DESCRIPTION

The **NJM2595** is a 5-input 3-output video switch. Its switches select one from five signals received from VTR,TV,DVD, TV-GAME and others.

The NJM2595 is designed for audio items, such as AV amplifier and others.

■ PACKAGE OUTLINE



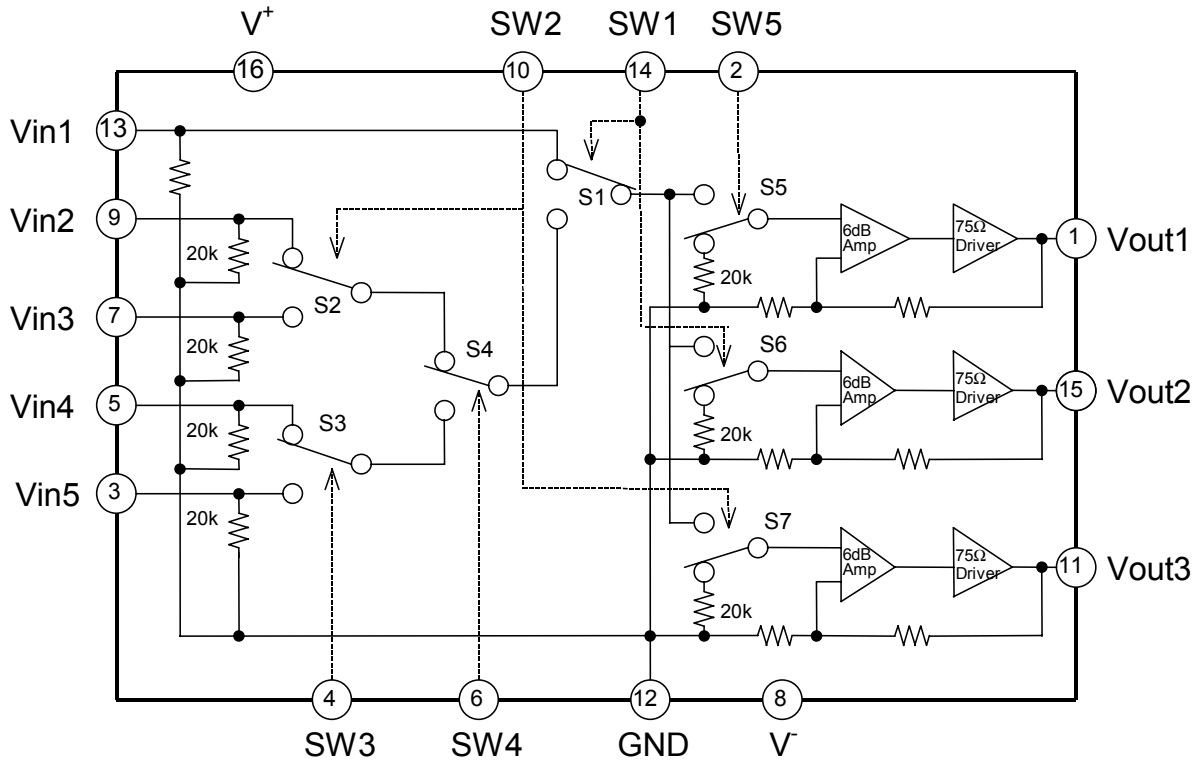


NJM2595D **NJM2595M**

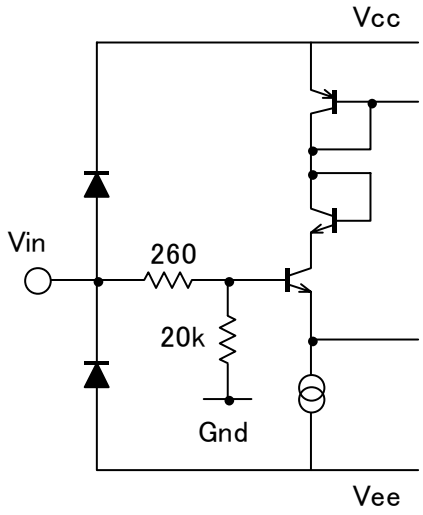
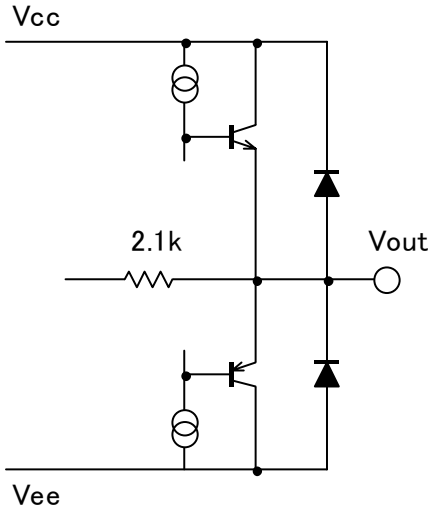
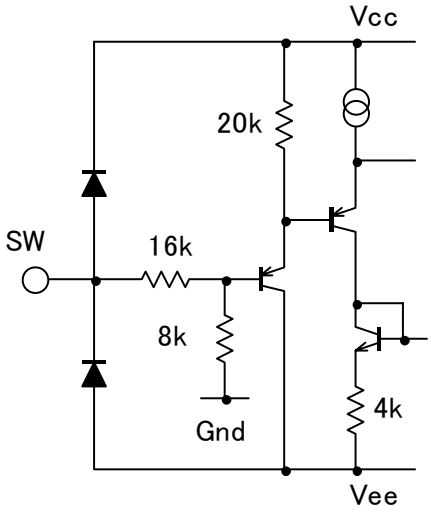
■ FEATURES

- 5-input 3-output
- Operating Voltage ±4.0 to ±6.5V
- Operating current ±15mAtyp. at Vcc=±5V
- Crosstalk -65dBtyp.
- Internal 6dB Amplifier
- Internal 75Ω Driver
- Bipolar Technology
- Package Outline DIP16,DMP16

■ PIN CONFIGURATION and BLOCK DIAGRAM

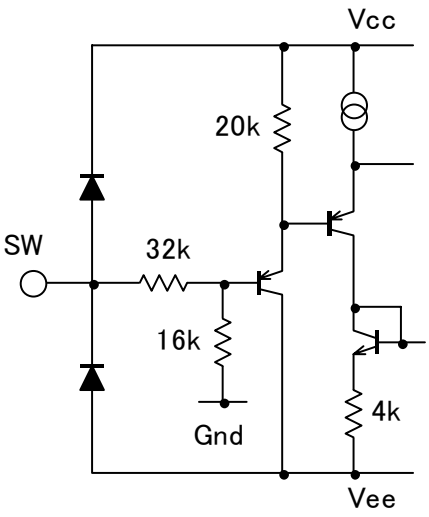


■ **EQUIVALENT CIRCUIT**

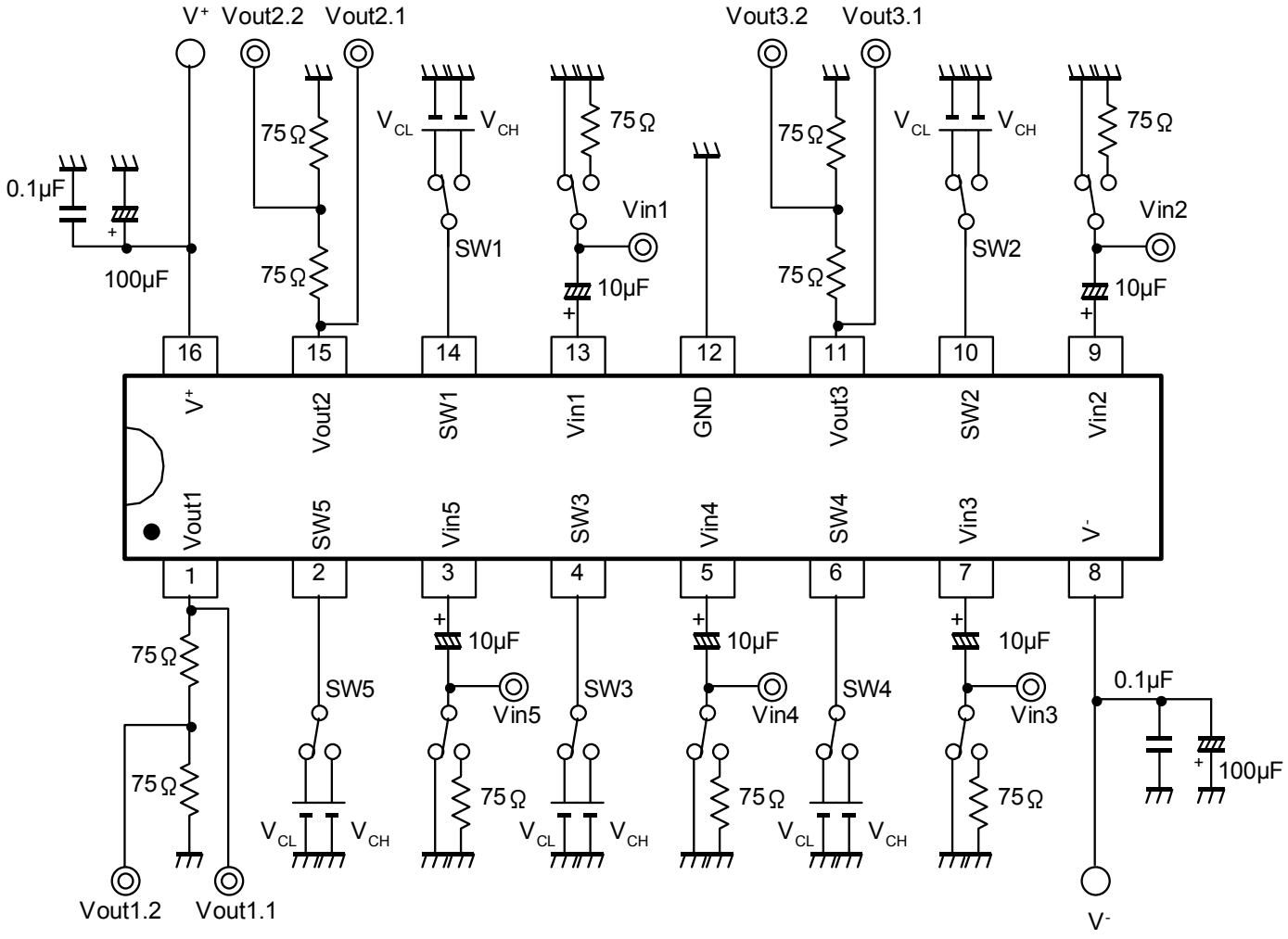
PIN No.	PIN NAME	INSIDE EQUIVALENT CIRCUIT	VOLTAGE
16	V^+		5V
8	V^-		-5V
12	GND		-
13 9 7 5 3	Vin1 Vin2 Vin3 Vin4 Vin5		0V
1 15 11	Vout1 Vout2 Vout3		0V
4 6 2	SW3 SW4 SW5		-

NJM2595

■ EQUIVALENT CIRCUIT

PIN No.	PIN NAME	INSIDE EQUIVALENT CIRCUIT	VOLTAGE
14 10	SW1 SW2		-

■ TEST CIRCUIT



NJM2068M (OP - AMP)

JRC

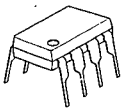
NJM2068

LOW-NOISE DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2068 is a high performance, low noise dual operational amplifier. This amplifier features popular pin-out, superior noise performance, and superior total harmonic distortion. This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product and slew rate which far exceeds that of the 4558 type amplifier. The specially designed low noise input transistors allow the NJM2068 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifier.

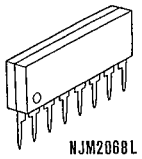
■ PACKAGE OUTLINE



NJM2068D

NJM2068M

NJM2068V



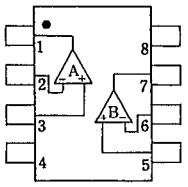
NJM2068L

■ FEATURES

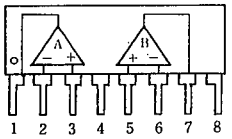
- Operating Voltage (±4V～±18V)
- Low Total Harmonic Distortion (0.001% typ.)
- Low Noise Voltage (FLAT+JISA, 0.56 μV typ.)
- High Slew Rate (6V/μs typ.)
- Unity Gain Bandwidth (27MHz @f=10kHz)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

4

■ PIN CONFIGURATION



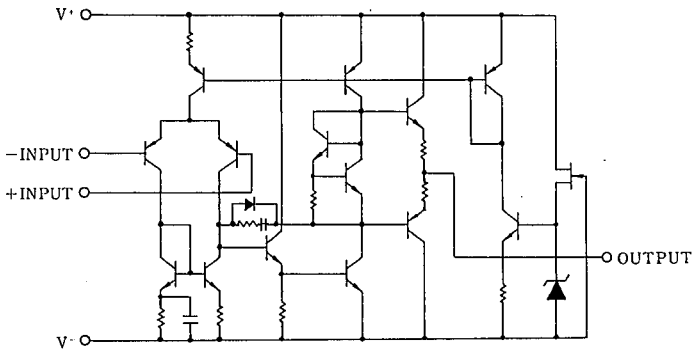
NJM2068D
NJM2068M
NJM2068V



NJM2068L

PIN FUNCITON
1. A OUTPUT
2. A−INPUT
3. A+INPUT
4. V⁻
5. B+INPUT
6. B−INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



JRC

NJM2137

ULTRA WIDE BAND, HIGH SLUE RATE DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2137 is an ultra wide band, high slew rate dual operational amplifier operated from low voltage (±1.35V).

It can apply to active filter, high speed analog and digital signal processor, line driver, HDTV, industrial measurement equipment and others.

It can also apply to portable communication items because of low operating voltage and low operating current.

■ PACKAGE OUTLINE

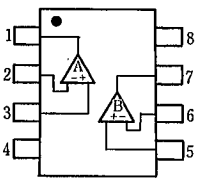
NJM2137V

NJM2137M

■ FEATURES

- Operating Voltage (±1.35V ~ ±6V)
- Ultra Wide Band (200MHz typ.)
- High Slew Rate (45V/μs typ.)
- Low Operating Current (1.14mA typ.)
- Bipolar Technology
- Package Outline SSOP8, DMP8

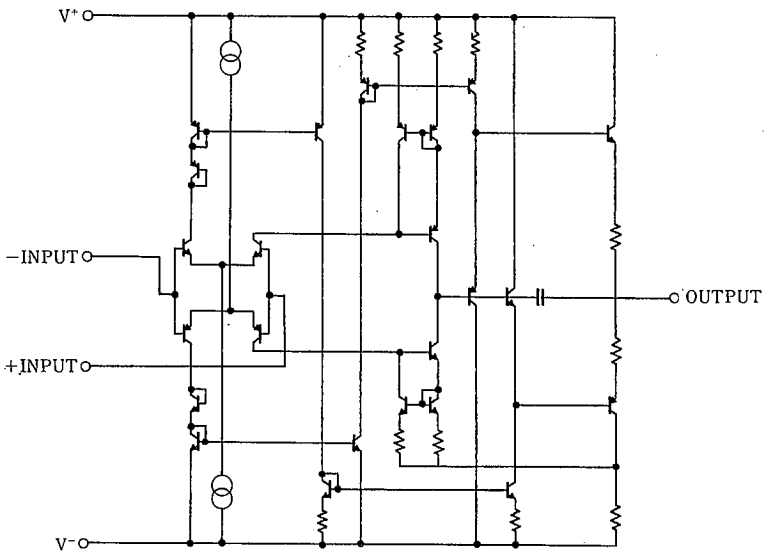
■ PIN CONFIGURATION



NJM2137M
NJM2137V

PIN FUNCTION
1. A OUTPUT
2. A −INPUT
3. A +INPUT
4. V⁻
5. B +INPUT
6. B −INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



JRC

IC86

NJM4556A

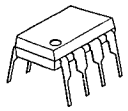
DUAL HIGH CURRENT OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM4556A integrated circuit is a high-gain, high output current dual operational amplifier capable of driving ±70mA into 150 Ω loads (±10.5V output voltage), and operating low supply voltage (V^+/V^-=±2V~).

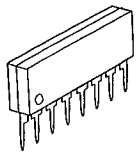
The NJM4556A combines many of the fetures of the popular NJM4558 as well as having the capability of driving 150Ω loads. In addition, the wide band-width, low noise, high slew rate and low distortion of the NJM4556A make it ideal for many audio, telecommunications and instrumentation applications.

■ PACKAGE OUTLINE

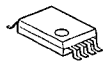


NJM4556AD

NJM4556AM



NJM4556AL

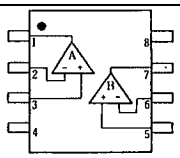


NJM4556AV

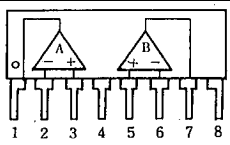
■ FEATURES

- Operating Voltage (±2V~±18V)
- High Output Current (Io=70mA)
- Slew Rate (3V/μs typ.)
- Gain Band Width Product (8MHz typ.)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

■ PIN CONFIGURATION



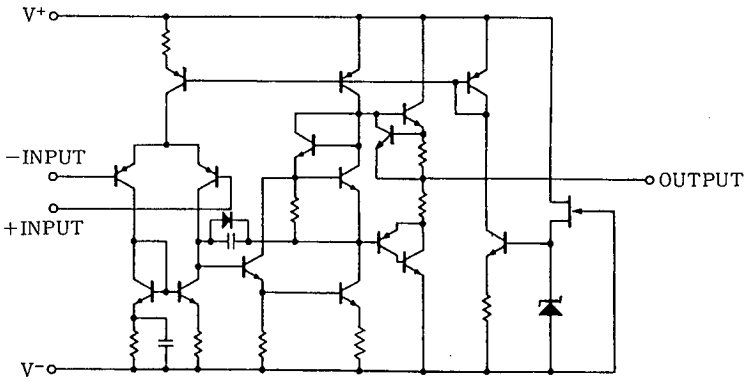
NJM4556AD
NJM4556AM
NJM4556AV



NJM4556AL

PIN FUNCTION
1. A OUTPUT
2. A−INPUT
3. A+INPUT
4. V⁻
5. B+INPUT
6. B−INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



AK4384

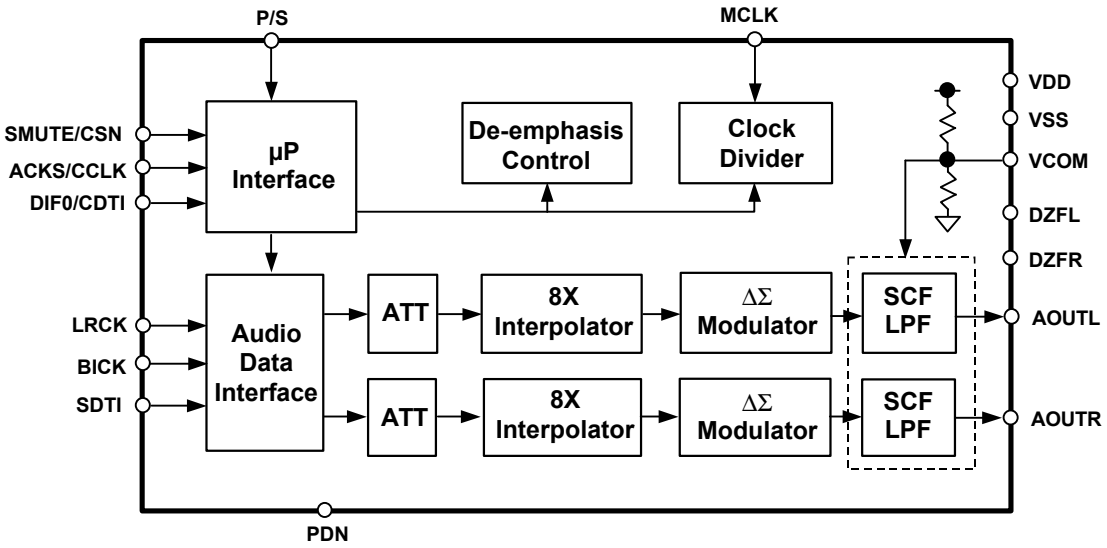
106dB 192kHz 24-Bit 2ch ΔΣ DAC

GENERAL DESCRIPTION

The AK4384 offers the perfect mix for cost and performance based audio systems. Using AKM's multi bit architecture for its modulator the AK4384 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4384 integrates a combination of SCF and CTF filters increasing performance for systems with excessive clock jitter. The 24 Bit word length and 192kHz sampling rate make this part ideal for a wide range of applications including DVD-Audio. The AK4384 is offered in a space saving 16pin TSSOP package.

FEATURES

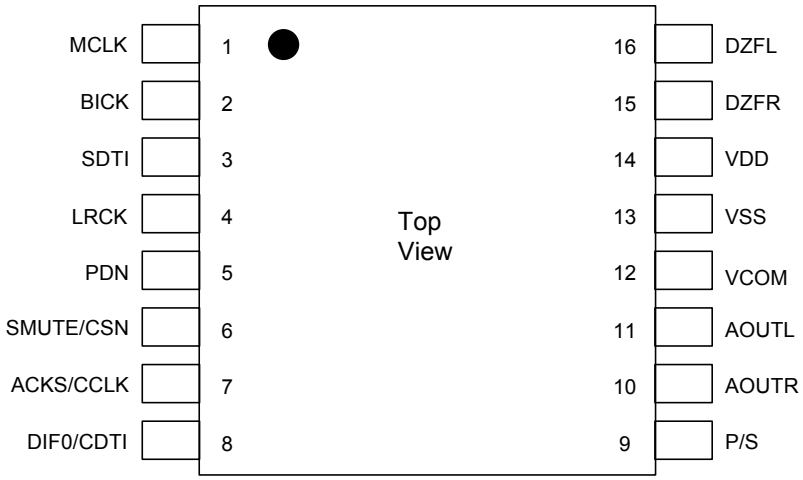
- ☐ Sampling Rate Ranging from 8kHz to 192kHz
- ☐ 128 times Oversampling (Normal Speed Mode)
- ☐ 64 times Oversampling (Double Speed Mode)
- ☐ 32 times Oversampling (Quad Speed Mode)
- ☐ 24-Bit 8 times FIR Digital Filter
- ☐ SCF with High Tolerance to Clock Jitter
- ☐ 2nd order Analog LPF
- ☐ Single Ended Output Buffer
- ☐ Digital de-emphasis for 32k, 44.1k and 48kHz sampling
- ☐ Soft mute
- ☐ Digital Attenuator (Linear 256 steps)
- ☐ I/F format: 24-Bit MSB justified, 24/20/16-Bit LSB justified or I^2S
- ☐ Master clock: 256fs, 384fs, 512fs, 768fs or 1152fs (Normal Speed Mode)
  128fs, 192fs, 256fs or 384fs (Double Speed Mode)
  128fs, 192fs (Quad Speed Mode)
- ☐ THD+N: -94dB
- ☐ Dynamic Range: 106dB
- ☐ Power supply: 4.5 to 5.5V
- ☐ Very Small Package: 16pin TSSOP (6.4mm x 5.0mm)



■ Ordering Guide

AK4384VT	-40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4384	Evaluation Board for AK4384	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin
5	PDN	I	Power-Down Mode Pin When at "L", the AK4384 is in the power-down mode and is held in reset. The AK4384 should always be reset upon power-up.
6	SMUTE	I	Soft Mute Pin in parallel mode "H": Enable, "L": Disable
	CSN	I	Chip Select Pin in serial mode
7	ACKS	I	Auto Setting Mode Pin in parallel mode "L": Manual Setting Mode, "H": Auto Setting Mode
	CCLK	I	Control Data Clock Pin in serial mode
8	DIF0	I	Audio Data Interface Format Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial mode
9	P/S	I	Parallel/Serial Select Pin (Internal pull-up pin) "L": Serial control mode, "H": Parallel control mode
10	AOUTR	O	Rch Analog Output Pin
11	AOUTL	O	Lch Analog Output Pin
12	VCOM	O	Common Voltage Pin, VDD/2 Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
13	VSS	-	Ground Pin
14	VDD	-	Power Supply Pin
15	DZFR	O	Rch Data Zero Input Detect Pin
16	DZFL	O	Lch Data Zero Input Detect Pin

Note: All input pins except pull-up pin should not be left floating.

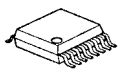
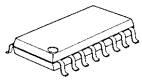
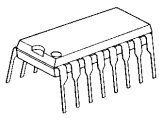
JRC **NJW1159**

2-CHANNEL ELECTRONIC VOLUME

■ GENERAL DESCRIPTION

NJW1159 is a two channel electronic volume IC. It is included output buffer amplifier and also resistor output terminal for using external amplifier to customize for your application. These functions are controlled by three-wired serial data. And the chip selector is available for using four chips on same serial bus line. It's available for two-channel stereo and or multi-channel audio volume.

■ PACKAGE OUTLINE

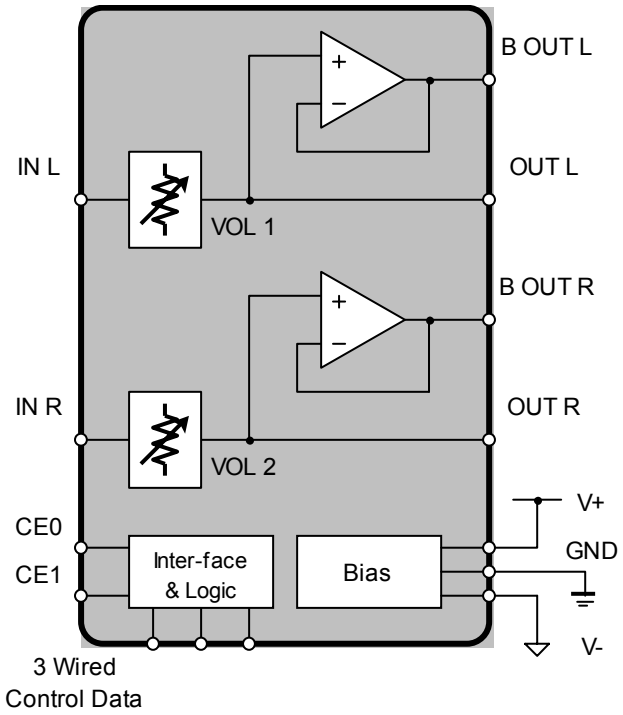




NJW1159V **NJW1159M** **NJW1159D**

■ FEATURES

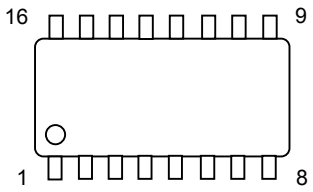
● Operating Voltage	±4.5 to ±7.5V
● Three-Wired Serial Data Control	
● Chip Selector	available for using four chips on same serial bus line.
● Volume	0 to -95dB/1dBstep, MUTE
● Bi-CMOS Technology	
● Package Outline	SSOP16, DMP16, DIP16

■ BLOCK DIAGRAM



NJW1159

■ PIN ASSIGNMENT



No.	Symbol	Function
1	OUTL	Lch External Opamp Input Connection Terminal
2	BOUTL	Lch Output
3	VDD_OUT	Internal VDD Noise Rejection Capacitor Terminal
4	BOUTR	Rch Output
5	OUTR	Rch External Opamp Input Connection Terminal
6	VSS_OUT	Internal VSS Noise Rejection Capacitor Terminal
7	V+	+ Power supply voltage input
8	V-	- Power supply voltage input
9	INL	Lch Input
10	INR	Rch Input
11	CE0	Chip Enable Terminal 0
12	CE1	Chip Enable Terminal 1
13	DATA	Control data signal input
14	CLOCK	Clock signal input
15	LACTH	Latch signal input
16	GND	Ground

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

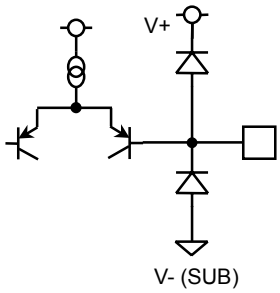
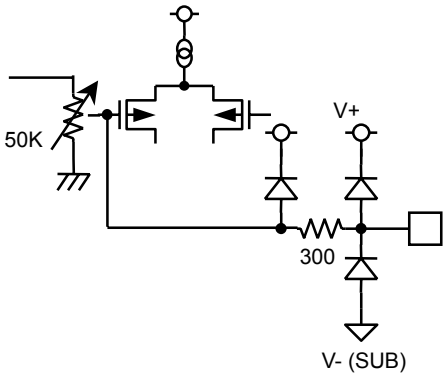
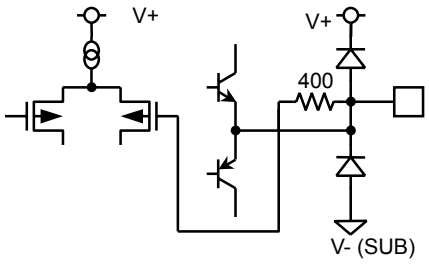
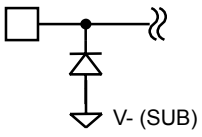
PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V^+/V^-	+8/-8	V
Maximum Input Voltage	V_{IM}	$V^+/V^{-(*)}$	V
Power Dissipation	P_D	SSOP16 ; 300 DMP16 ; 300 DIP16 ; 500	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +125	°C

(✳) For the maximum input voltage less than V^+/V^-

■ ELECTRICAL CHARACTERISTICS (Ta=25°C,V+/V- = +7V/-7V, R_L=47kΩ)

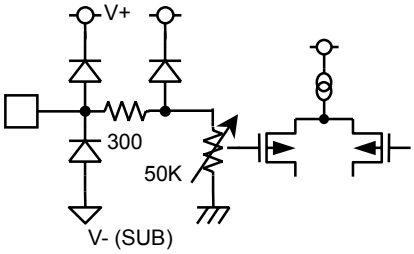
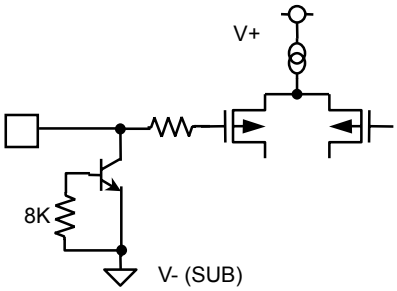
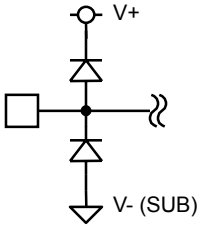
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
◆ Power Supply						
Operating Voltage 1	V+		4.5	7.0	7.5	V
Operating Voltage 2	V-		-7.5	-7.0	-4.5	V
Supply Current 1	I_{CC}	No signal	-	4.5	9.0	mA
Supply Current 2	I_{EE}	No signal	-	4.5	9.0	mA
◆ Input/Output Characteristics (BOUTL : 2pin, BOUTR : 4pin)						
Maximum Output Voltage	V_{OM}	f=1kHz,THD=1% Volume=0dB	3.0	4.0	-	Vrms
Voltage Gain	G_V	V_{IN}=1Vrms, f=1kHz Volume=0dB	-0.5	0	0.5	dB
Channel Gain Balance 1	ΔG_{V1}	V_{IN}=1Vrms, f=1kHz Volume=0dB	-0.5	0	0.5	dB
Channel Gain Balance 2	ΔG_{V2}	V_{IN}=1Vrms, f=1kHz Volume=-60dB	-1.0	0	1.0	dB
Maximum Attenuation	A_{TT}	V_{IN}=1Vrms, f=1kHz Volume=-95dB, A-weight	-	-95	-	dB
Mute Level	Mute	V_{IN}=1Vrms, f=1kHz Volume=Mute, A-weight	-	-110	-	dB
Output Noise Voltage	V_{NO}	Volume=0dB, Rg=0Ω, A-weight	-	-105 (5.6μ)	-95 (17.8μ)	dBV (Vrms)
Total Harmonic Distortion	THD	Vo=1Vrms, f=1kHz, Volume=0dB, BW=400-30kHz	-	0.005	0.05	%
Channel Separation	CS	Vo=1Vrms, f=1kHz, A-weight Volume=0dB, Rg=0Ω	-	-100	-90	dB

NJW1159

PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
3 6	VDD_OUT VSS_OUT	Internal VDD Noise Rejection Capacitor Terminal Internal VSS Noise Rejection Capacitor Terminal		2.5V (VDD_OUT) -2.5V (VSS_OUT)
1 5	OUTL OUTR	Lch External Opamp Input Connection Terminal Rch External Opamp Input Connection Terminal		0V 0V
2 4	BOUTL BOUTR	Lch Output Rch Output		0V 0V
7	V+	+Power Supply Voltage Input		V+

■ TERMINAL DESCRIPTION

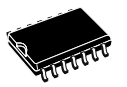
NJW1159

PIN NO.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	TERMINAL DC VOLTAGE
9 10	INL INR	Lch Input Rch Input		0V
11 12 13 14 15	CE0 CE1 DATA CLOCK LATCH	Chip Enable Terminal 0 Chip Enable Terminal 1 Control data signal input Clock signal input Latch signal input		0V
16	GND	Ground		0V

74LCX32

LOW VOLTAGE CMOS QUAD 2-INPUT OR GATE WITH 5V TOLERANT INPUTS

- 5V TOLERANT INPUTS
- HIGH SPEED:
  t_{PD} = 5.2ns (MAX.) at V_{CC} = 3V
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24mA (MIN) at V_{CC} = 3V
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2.0V to 3.6V (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 32
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:
  HBM > 2000V (MIL STD 883 method 3015);
  MM > 200V



SOP

TSSOP

Table 1: Order Codes

PACKAGE	T & R
SOP	74LCX32MTR
TSSOP	74LCX32TTR

DESCRIPTION

The 74LCX32 is a low voltage CMOS QUAD 2-INPUT OR GATE fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for inputs.

It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols

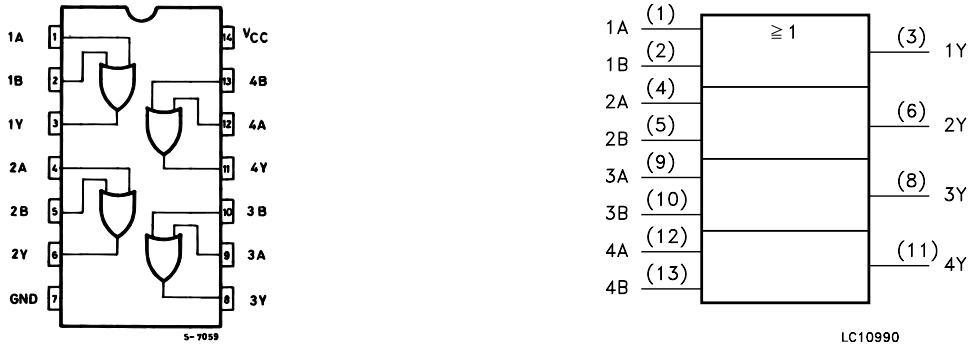


Figure 2: Input And Output Equivalent Circuit

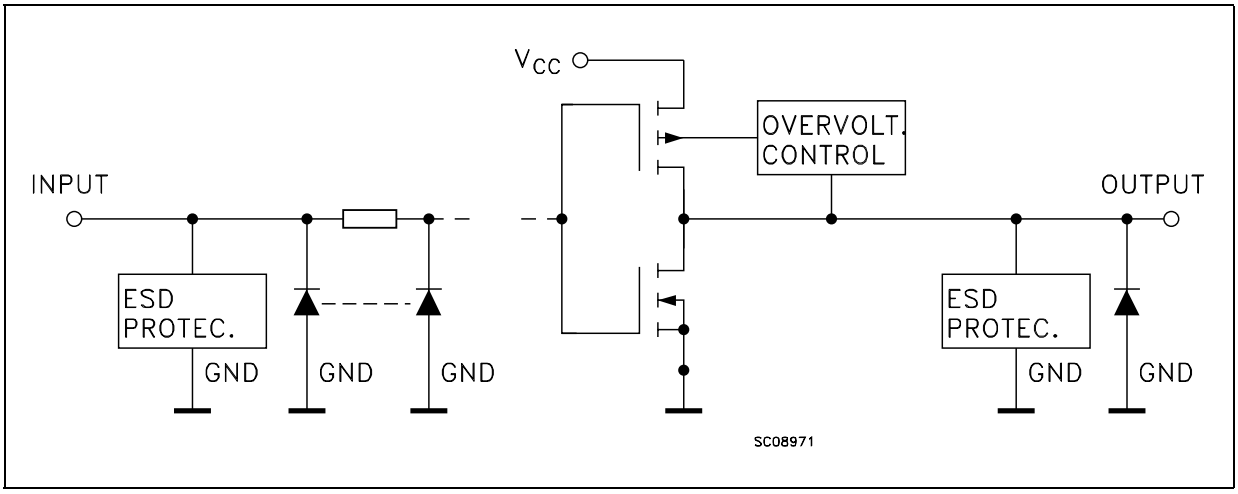


Table 2: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

Table 3: Truth Table

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

Table 4: Absolute Maximum Ratings

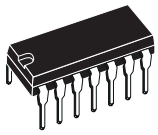
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (V_{CC} = 0V)	-0.5 to +7.0	V
V_O	DC Output Voltage (High or Low State) (note 1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current	± 50	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Supply Pin	± 100	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
1) I_O absolute maximum rating must be observed
2) V_O < GND

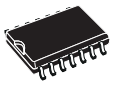
74ACT04

HEX INVERTER

- HIGH SPEED: t_{PD} = 5.0ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION: I_{CC} = 2µA(MAX.) at T_A=25°C
- COMPATIBLE WITH TTL OUTPUTS V_{IH} = 2V (MIN.), V_{IL} = 0.8V (MAX.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 24mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 04
- IMPROVED LATCH-UP IMMUNITY



DIP



SOP

TSSOP

ORDER CODES

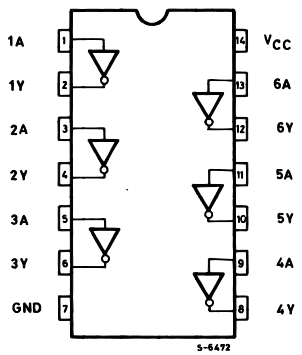
PACKAGE	TUBE	T & R
DIP	74ACT04B	
SOP	74ACT04M	74ACT04MTR
TSSOP		74ACT04TTR

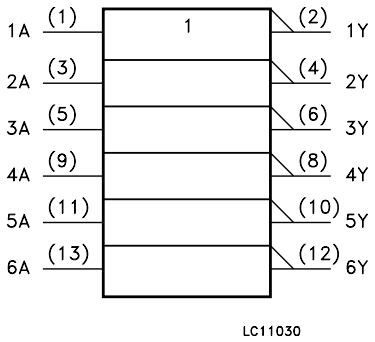
DESCRIPTION

The 74ACT04 is an advanced high-speed CMOS HEX INVERTER fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.
The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

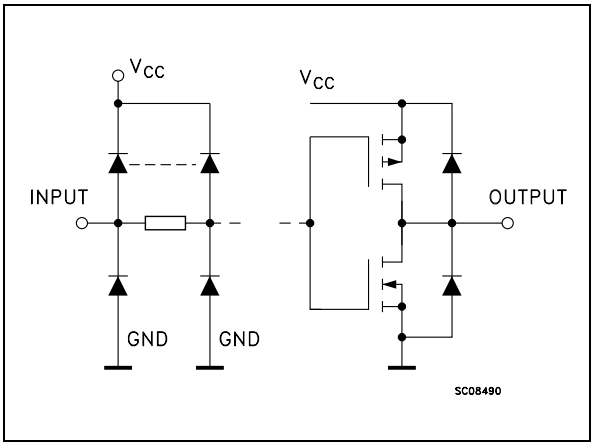
PIN CONNECTION AND IEC LOGIC SYMBOLS





74ACT04

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data Inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 200	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time V_{CC} = 4.5 to 5.5V (note 1)	8	ns/V

1) V_{IN} from 0.8V to 2.0V

CIRRUS LOGIC
Leading the Digital Entertainment Revolution™

CS42528

114 dB, 192 kHz 8-Ch Codec with S/PDIF Receiver

Features

- Eight 24-bit D/A, two 24-bit A/D Converters
- 114 dB DAC / 114 dB ADC Dynamic Range
- -100 dB THD+N
- System Sampling Rates up to 192 kHz
- S/PDIF Receiver Compatible with EIAJ CP1201 and IEC-60958
- Recovered S/PDIF Clock or System Clock Selection
- 8:2 S/PDIF Input MUX
- ADC High-pass Filter for DC Offset Calibration
- Expandable ADC Channels and One-line Mode Support
- Digital Output Volume Control with Soft Ramp
- Digital +/-15dB Input Gain Adjust for ADC
- Differential Analog Architecture
- Supports logic levels between 5 V and 1.8 V.

General Description

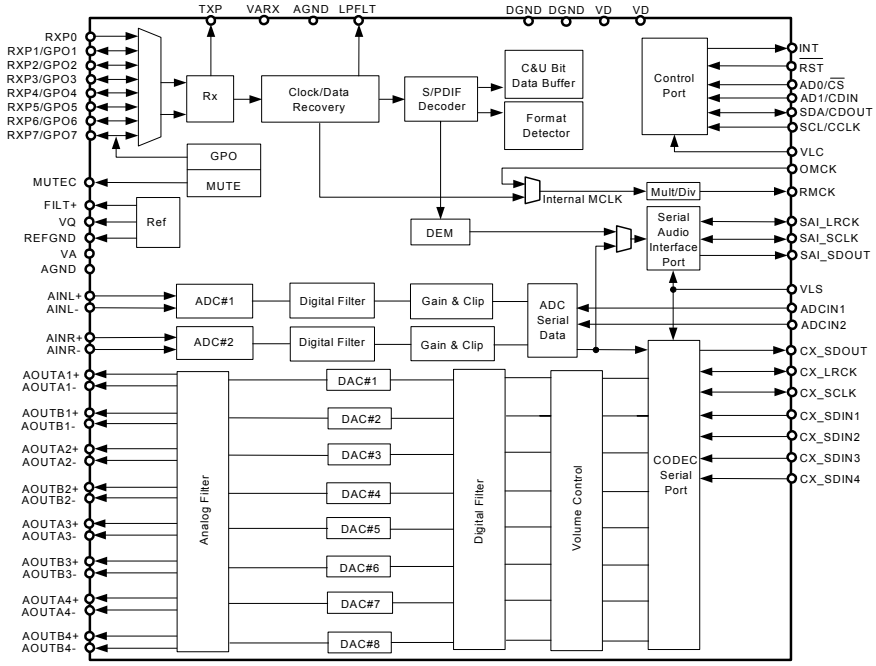
The CS42528 codec provides two analog-to-digital and eight digital-to-analog delta-sigma converters, as well as an integrated S/PDIF receiver, in a 64-pin LQFP package.

The CS42528 integrated S/PDIF receiver supports up to eight inputs, clock recovery circuitry and format auto-detection. The internal stereo ADC is capable of independent channel gain control for single-ended or differential analog inputs. All eight channels of DAC provide digital volume control and differential analog outputs. The general purpose outputs may be driven high or low, or mapped to a variety of DAC mute controls or ADC overflow indicators.

The CS42528 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, digital speaker and automotive audio systems.

ORDERING INFORMATION

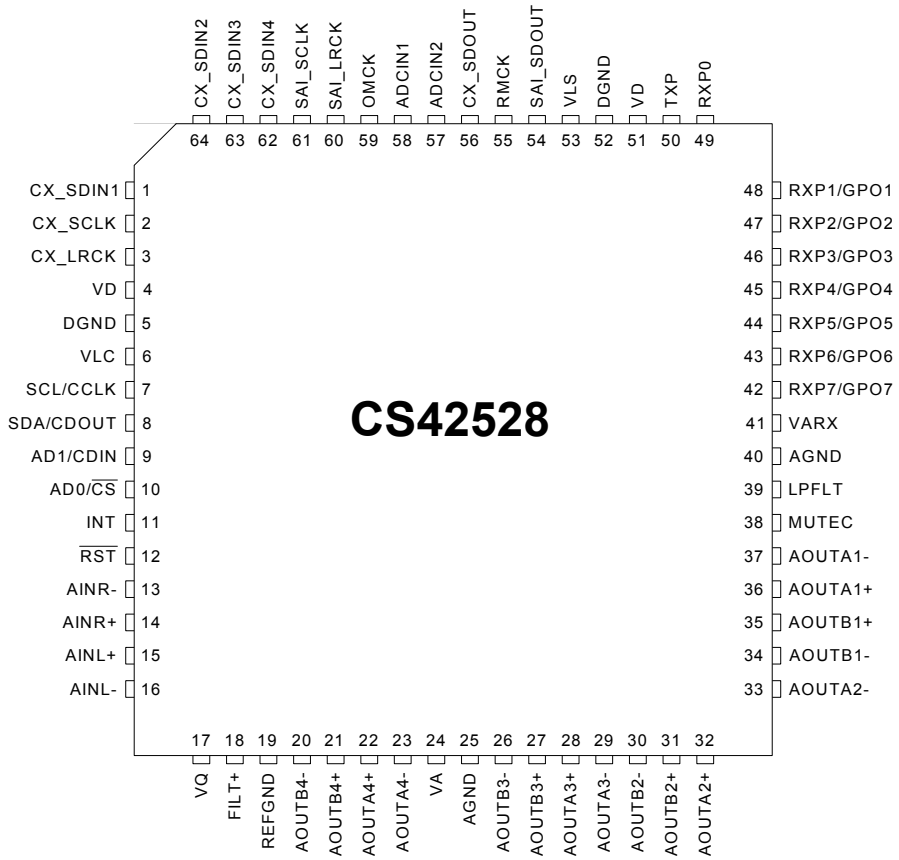
CS42528-CQZ	-10° to 70° C	64-pin LQFP	Lead Free
CS42528-DQZ	-40° to 85° C	64-pin LQFP	Lead Free
CDB42528	Evaluation Board		



Preliminary Product Information

Cirrus Logic, Inc.
http://www.cirrus.com

2. PIN DESCRIPTIONS



Pin Name	#	Pin Description
CX_SDIN1 **CX_SDIN2** **CX_SDIN3** **CX_SDIN4**	1 64 63 62	**Codec Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
CX_SCLK	2	**CODEC Serial Clock** *(Input/Output)* - Serial clock for the CODEC serial audio interface.
CX_LRCK	3	**CODEC Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the CODEC serial audio data line.
VD	4 51	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	5 52	**Digital Ground** (*Input*) - Ground reference. Should be connected to digital ground.
VLC	6	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port.
SCL/CCLK	7	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I^2C mode as shown in the Typical Connection Diagram.
SDA/CDOUT	8	**Serial Control Data** (*Input/Output*) **-** SDA is a data I/O line in I^2C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDOUT is the output data line for the control port interface in SPI mode.
AD1/CDIN	9	**Address Bit 1 (I^2C)/Serial Control Data (SPI)** (*Input*) - AD1 is a chip address pin in I^2C mode; CDIN is the input data line for the control port interface in SPI mode.

AD0/$\overline{CS}$	10	**Address Bit 0 (I^2C)/Control Port Chip Select (SPI)** *(Input)* **-** AD0 is a chip address pin in I^2C mode; $\overline{CS}$ is the chip select signal in SPI mode.
INT	11	**Interrupt** *(Output)* - The CS42528 will generate an interrupt condition as per the Interrupt Mask register. See “Interrupts” on page 40 for more details.
$\overline{RST}$	12	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
AINR- **AINR+**	13 14	**Differential Right Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
AINL+ **AINL-**	15 16	**Differential Left Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins.
VQ	17	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
REFGND	19	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
AOUTA1 +,- **AOUTB1 +,-** **AOUTA2 +,-** **AOUTB2 +,-** **AOUTA3 +,-** **AOUTB3 +,-** **AOUTA4 +,-** **AOUTB4 +,-**	36,37 35,34 32,33 31,30 28,29 27,26 22,23 21,20	**Differential Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
VA **VARX**	24 41	**Analog Power** (*Input*) - Positive power supply for the analog section.
AGND	25 40	**Analog Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MUTEC	38	**Mute Control** (*Output*) - The Mute Control pin outputs high impedance following an initial power-on condition or whenever the PDN bit is set to a ‘1’, forcing the codec into power-down mode. The signal will remain in a high impedance state as long as the part is in power-down mode. The Mute Control pin goes to the selected “active” state during reset, muting, or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
LPFLT	39	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and ground.
RXP7/GPO7 **RXP6/GPO6** **RXP5/GPO5** **RXP4/GPO4** **RXP3/GPO3** **RXP2/GPO2** **RXP1/GPO1**	42 43 44 45 46 47 48	**S/PDIF Receiver Input/ General Purpose Output** (*Input/Output*) - Receiver inputs for S/PDIF encoded data. The CS42528 has an internal 8:2 multiplexer to select the active receiver port, according to the Receiver Mode Control 2 register. These pins can also be configured as general purpose output pins, ADC Overflow indicators or Mute Control outputs according to the RXP/General Purpose Pin Control registers.
RXP0	49	**S/PDIF Receiver Input** (*Input*) - Dedicated receiver input for S/PDIF encoded data.
TXP	50	**S/PDIF Transmitter Output** (*Output*) - S/PDIF encoded data output, mapped directly from one of the receiver inputs as indicated by the Receiver Mode Control 2 register.
VLS	53	**Serial Port Interface Power** (*Input*) - Determines the required signal level for the serial port interfaces.
SAI_SDOUT	54	**Serial Audio Interface Serial Data Output** (*Output*) - Output for two’s complement serial audio PCM data from the S/PDIF incoming stream. This pin can also be configured to transmit the output of the internal and external ADCs.
RMCK	55	**Recovered Master Clock** (*Output*) - Recovered master clock output from the External Clock Reference (OMCK, pin 59) or the PLL which is locked to the incoming S/PDIF stream or CX_LRCK.

CX_SDOUT	56	**CODEC Serial Data Output** (*Output*) - Output for two's complement serial audio data from the internal and external ADCs.
ADCIN1 **ADCIN2**	58 57	**External ADC Serial Input** (*Input*) - The CS42528 provides for up to two external stereo analog to digital converter inputs to provide a maximum of six channels on one serial data output line when the CS42528 is placed in One Line mode.
OMCK	59	**External Reference Clock** (*Input*) - External clock reference that must be within the ranges specified in the register "OMCK Frequency (OMCK Freqx)" on page 54.
SAI_LRCK	60	**Serial Audio Interface Left/Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SAI_SCLK	61	**Serial Audio Interface Serial Clock** *(Input/Output)* - Serial clock for the Serial Audio Interface.

KEC

SEMICONDUCTOR TECHNICAL DATA

KIA378R05PI~KIA378R15PI

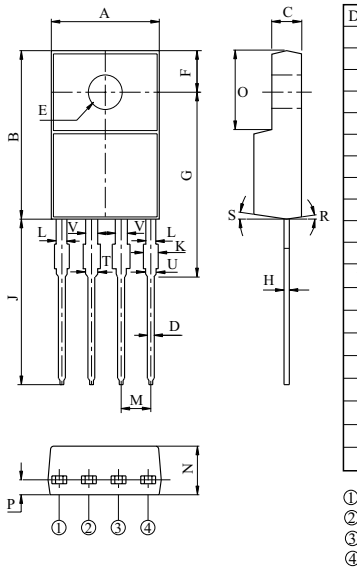
BIPOLAR LINEAR INTEGRATED CIRCUIT

4 TERMINAL 3A OUTPUT LOW DROP VOLTAGE REGULATOR

The KIA378R × × Series are Low Drop Voltage Regulator suitable for various electronic equipments. It provides constant voltage power source with TO-220IS-4 terminal lead full molded PKG. The Regulator has multi-function such as over current protection, overheat protection and ON/OFF control.

FEATURES

- 3.0A Output Low Drop Voltage Regulator.
- Built in ON/OFF Control Terminal.
- Built in Over Current Protection, Over Heat Protection Function.



DIM	MILLIMETERS
A	10.00±0.20
B	15.00±0.20
C	2.70±0.20
D	0.60±0.10
E	Φ3.20±0.20
F	3.50±0.10
G	15.70±0.20
H	0.40±0.10
J	14.3+0.2/-0.1
K	1.45±0.10
L	1.00±0.10
M	2.54
N	4.50±0.20
O	7.5±0.1
P	1.50±0.10
R	5°
S	8°
T	1.30±0.1
U	3-1.00±0.1
V	1.30±0.1

TO-220IS-4

LINE UP

ITEM	OUTPUT VOLTAGE (Typ.)	UNIT
KIA378R05PI	5	V
KIA378R06PI	6	
KIA378R08PI	8	
KIA378R09PI	9	
KIA378R10PI	10	
KIA378R12PI	12	
KIA378R15PI	15	

MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT	Remark
Input Voltage	V_{IN}	35	V	-
ON/OFF Control Voltage	V_C	35	V	-
Output Current	I_O	3	A	-
Power Dissipation 1	P_{d1}	1.5	W	No heatsink
Power Dissipation 2	P_{d2}	15	W	with heatsink
Junction Temperature	T_j	-40～150	℃	-
Operating Temperature	T_{opr}	-30～85	℃	-
Storage Temperature	T_{stg}	-40～150	℃	-
Soldering Temperature (10sec)	T_{sol}	260	℃	-

KEC

SEMICONDUCTOR
TECHNICAL DATA

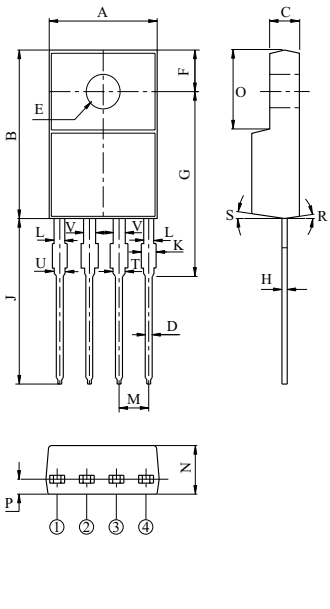
KIA278R00PI
BIPOLAR LINEAR INTEGRATED CIRCUIT

2A ADJUSTABLE LOW DROP VOLTAGE REGULATOR

The KIA278R00PI is a Low Drop Voltage Regulator suitable for various electronic equipments. It provides constant voltage power source with TO-220-4 terminal lead full molded PKG. The Regulator has multi function such as over current protection, overheat protection.

FEATURES

- Adjustable Output Voltage (Range : 1.5~30V)
- 1.0A Output Low Drop Voltage Regulator.
- Built in Over Current Protection, Over Heat Protection Function.



DIM	MILLIMETERS
A	10.00±0.20
B	15.00±0.20
C	2.70±0.20
D	0.60±0.10
E	Φ3.20±0.20
F	3.50±0.10
G	15.70±0.20
H	0.40±0.10
J	14.3+0.2/-0.1
K	1.45±0.10
L	1.00±0.10
M	2.54
N	4.50±0.20
O	7.5±0.1
P	1.50±0.10
R	5°
S	8°
T	1.30±0.1
U	3-1.00±0.1
V	1.30±0.1

① DC INPUT (V_{IN})
② DC OUTPUT (V_O)
③ GND
④ ADJUSTABLE TERMINAL (V_{ADJ})

TO-220IS-4

MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT	Remark
Input Voltage	V_{IN}	35	V	-
Output Current	I_{OUT}	2	A	-
Power Dissipation 1	P_{D1}	1.5	W	No heatsink
Power Dissipation 2	P_{D2}	15	W	with heatsink
Junction Temperature	T_j	150	℃	-
Operating Temperature	T_{opr}	-20～80	℃	-
Storage Temperature	T_{stg}	-30～150	℃	-
Soldering Temperature (10sec)	T_{sol}	260	℃	-

KEC

SEMICONDUCTOR
TECHNICAL DATA

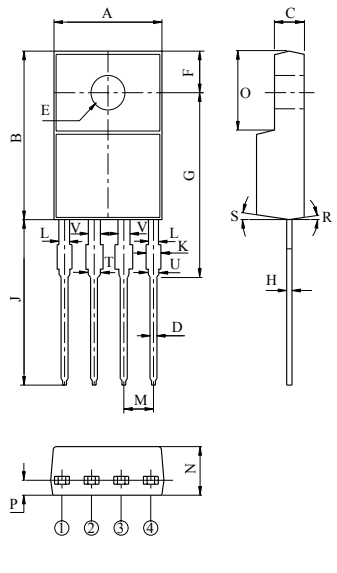
KIA278R05PI~KIA278R15PI
BIPOLAR LINEAR INTEGRATED CIRCUIT

4 TERMINAL 2A OUTPUT LOW DROP
VOLTAGE REGULATOR

The KIA278R×× Series are Low Drop Voltage Regulator suitable for various electronic equipments.
It provides constant voltage power source with TO-220 4 terminal lead full molded PKG. The Regulator has multi function such as over current protection, overheat protection and ON/OFF control.

FEATURES

- 2.0A Output Low Drop Voltage Regulator.
- Built in ON/OFF Control Terminal.
- Built in Over Current Protection, Over Heat Protection Function.



DIM	MILLIMETERS
A	10.00±0.20
B	15.00±0.20
C	2.70±0.20
D	0.60±0.10
E	Φ3.20±0.20
F	3.50±0.10
G	15.70±0.20
H	0.40±0.10
J	14.3+0.2/-0.1
K	1.45±0.10
L	1.00±0.10
M	2.54
N	4.50±0.20
O	7.5± 0.1
P	1.50±0.10
R	5°
S	8°
T	1.30±0.1
U	3-1.00±0.1
V	1.30±0.1

TO-220IS-4

LINE UP

ITEM	OUTPUT VOLTAGE (Typ.)	UNIT
KIA278R05PI	5	V
KIA278R06PI	6	
KIA278R08PI	8	
KIA278R09PI	9	
KIA278R10PI	10	
KIA278R12PI	12	
* KIA278R15PI	15	

* Note) * : Under Development.

MAXIMUM RATING (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT	Remark
Input Voltage	V_{IN}	35	V	-
ON/OFF Control Voltage	V_C	35	V	-
Output Current	I_O	2	A	-
Power Dissipation 1	P_{d1}	1.5	W	No heatsink
Power Dissipation 2	P_{d2}	15	W	with heatsink
Junction Temperature	T_j	125	℃	-
Operating Temperature	T_{opr}	-20～80	℃	-
Storage Temperature	T_{stg}	-30～125	℃	-
Soldering Temperature (10sec)	T_{sol}	260	℃	-

KEC

SEMICONDUCTOR
TECHNICAL DATA

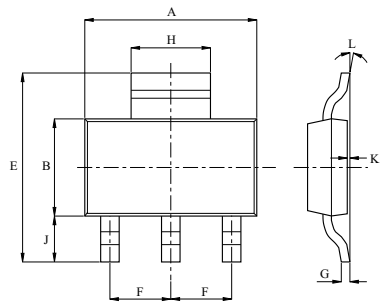
KIA1117S/F00~ KIA1117S/F50
BIPOLAR LINEAR INTEGRATED CIRCUIT

LOW DROP FIXED AND ADJUSTABLE
POSITIVE VOLTAGE REGULATOR

The KIA1117S/F × × is a Low Drop Voltage Regulator able to provide up to 1A of output current, available even in adjustable version (Vref=1.25V)

FEATURES

- Low Dropout Voltage : 1.1V/Typ. (Iout=1.0A)
- Very Low Quiescent Current : 4.2㎃/Typ.
- Output Current up to 1A
- Fixed Output Voltage of 1.5V, 1.8V, 2.5V, 2.85V, 3.3V, 5.0V
- Adjustable Version Availability : Vref=1.25V
- Internal Current and Thermal Limit
- Only 10㎌ for stability
- Available in ±2%(at 25℃) and 4% in full Temperature range
- High Ripple Rejection : 80dB/Typ
- Temperature Range : 0℃~125℃



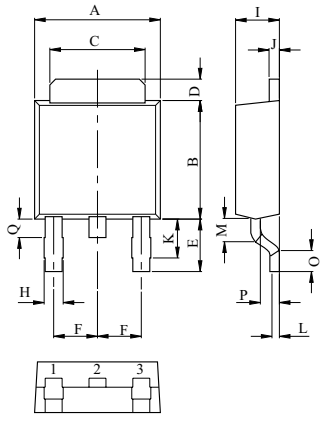
DIM	MILLIMETERS
A	6.5±0.2
B	3.5±0.2
C	1.8 MAX
D	0.7+0.15/-0.1
E	7±0.3
F	2.3 TYP
G	0.26+0.09/-0.02
H	3.0+0.15/-0.1
J	1.75±0.25
K	0.1 MAX
L	10° MAX

1. COMMOIN (ADJ.)
2. OUTPUT
3. INPUT

SOT-223

LINE UP

ITEM	OUTPUT VOLTAGE (V)	PACKAGE
KIA1117S/F00	Adjustable (1.25~10V)	S : SOT-223 F : DPAK
KIA1117S/F15	1.5	
KIA1117S/F18	1.8	
KIA1117S/F25	2.5	
KIA1117S/F28	2.85	
KIA1117S/F33	3.3	
KIA1117S/F50	5.0	



DIM	MILLIMETERS
A	6.60±0.2
B	6.10±0.2
C	5.0±0.2
D	1.10±0.2
E	2.70±0.2
F	2.30±0.1
H	1.00 MAX
I	2.30±0.2
J	0.5±0.1
K	2.00±0.20
L	0.50±0.10
M	0.91±0.10
O	0.90±0.1
P	1.00±0.10
Q	0.95 MAX

1. COMMOIN (ADJ.)
2. OUTPUT
3. INPUT

DPAK

MAXIMUM RATINGS (Ta=25℃)

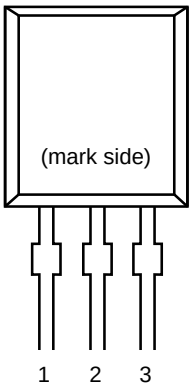
CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage		V_{IN}	10	V
Output Current	S/F	I_{OUT}	1.0	A
Power Dissipation 1 (No heatsink)	S (Note)	P_{D1}	1.0	W
	F		1.3	
Power Dissipation 2 (Without heatsink)	S	P_{D2}	8.3	W
	F		13	
Operating Temperature		T_{opr}	0~125	℃
Storage Temperature		T_{stg}	-55~150	℃

Note) Package Mounted on FR-4 PCB 36 ×18 ×1.5㎜.
: mounting pad for the GND Lead min. 6㎠

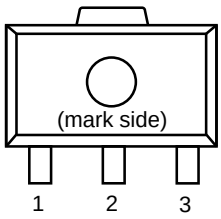
R E5VT28C A TZ

PIN CONFIGURATION

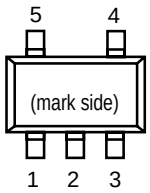
• TO-92



• SOT-89



• SOT-23-5



PIN DESCRIPTION

• TO-92

Pin No.	Symbol
1	OUT
2	VDD
3	GND

• SOT-89

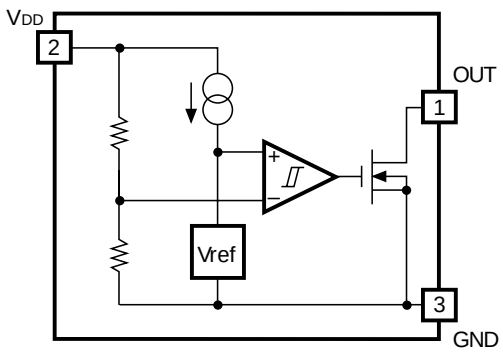
Pin No.	Symbol
1	OUT
2	VDD
3	GND

• SOT-23-5

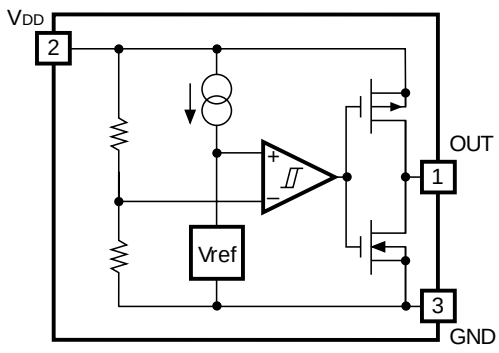
Pin No.	Symbol
1	OUT
2	VDD
3	GND
4	NC
5	NC

BLOCK DIAGRAMS

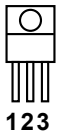
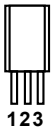
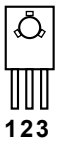
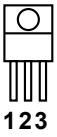
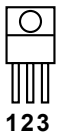
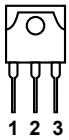
• Nch Open Drain Output (R5VT××A)



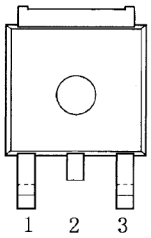
• CMOS Output (R5VT××C)



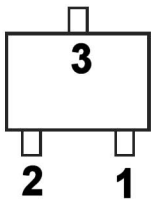
TRANSISTOR, REGULATOR IC BLOCK DIAGRAM

TO-92M  123 1. Emitter 2. Collector 3. Base KTC2874B KSC2785Y KRA107M KRC107M KRA104MT KRC104M KTA1267	TO-92  123 1. Emitter 2. Collector 3. Base KTD1302T KTA1268GR KTC3200GR KTC3198Y KTA1271Y KSA1175YT	TO-220  123 1. GND 2. INPUT 3. OUTPUT MCNJM7905 MC7915C NJM7908 L7905 L7915	TO-92L  123 1. Emitter 2. Collector 3. Base KTA1024Y KSC2316Y
TO-126  123 1. Emitter 2. Collector 3. Base KTD600KG	TO-92  123 1. Emitter 2. Base 3. Collector KSA733CYT	TO-220  123 1. INPUT 2. GND 3. OUTPUT MC7815C MC7805C MC7809 L7805 NJM7824 L7815 L7812 L7808	TO-3P  1 2 3 1. Base 2. Collector 3. Emitter 2SB1560 2SC3423O 2SD2390 2SA1360 2SB1647 2SD2560

NJM2391DL1-25 NJM2391DL1-33
LOW DROPOUT VOLTAGE REGULATOR



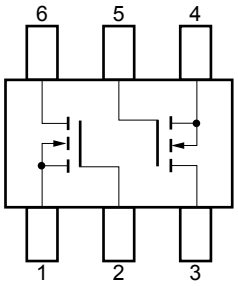
PIN FUNCTION
1. IN
2. GND
3. OUT



1) Emitter
2) Base
3) Collector

KRC102S
KRA102S
KRC103S
KRC107S
KRC111S
KRA107S KRC1114S

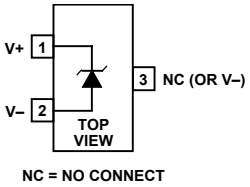
N-CHANNEL MOS FET ARRAY
μPA672T



1. Source 1 (S1)
2. Gate 1 (G1)
3. Drain 2 (D2)
4. Source 2 (S2)
5. Gate 2 (G2)
6. Drain 1 (D1)

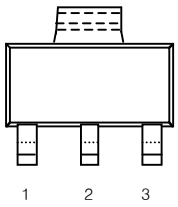
Marking: MA

PIN CONFIGURATION
SOT-23 Package
AD1580



NC = NO CONNECT

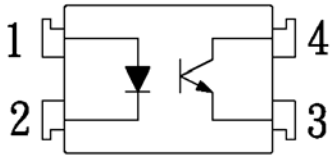
SOT–223 PKG (FRONT VIEW)



LM1117
REGULATOR

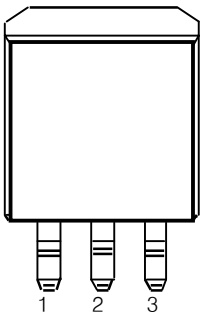
PIN FUNCTION
1. Adj/Gnd
2. Vout
3. Vin

KP1010 photocoupler



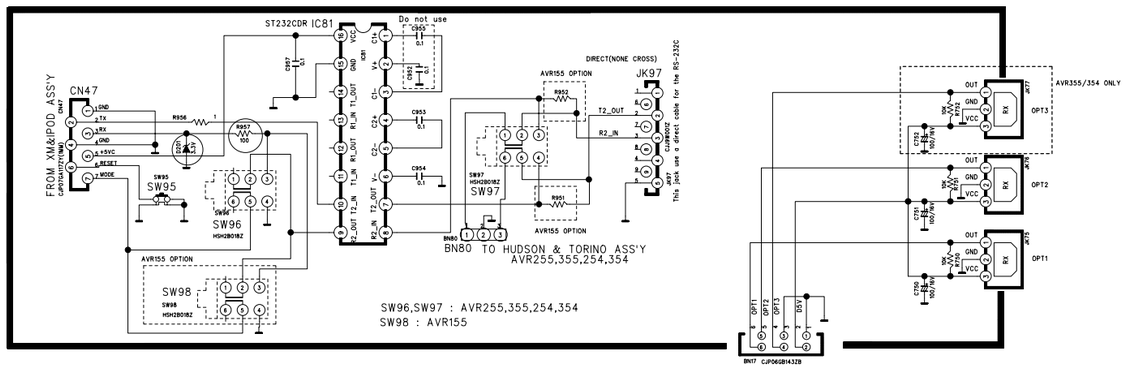
1. Anode
2. Cathode
3. Emitter
4. Collector

TO–263 (D2 PKG, FRONT VIEW)



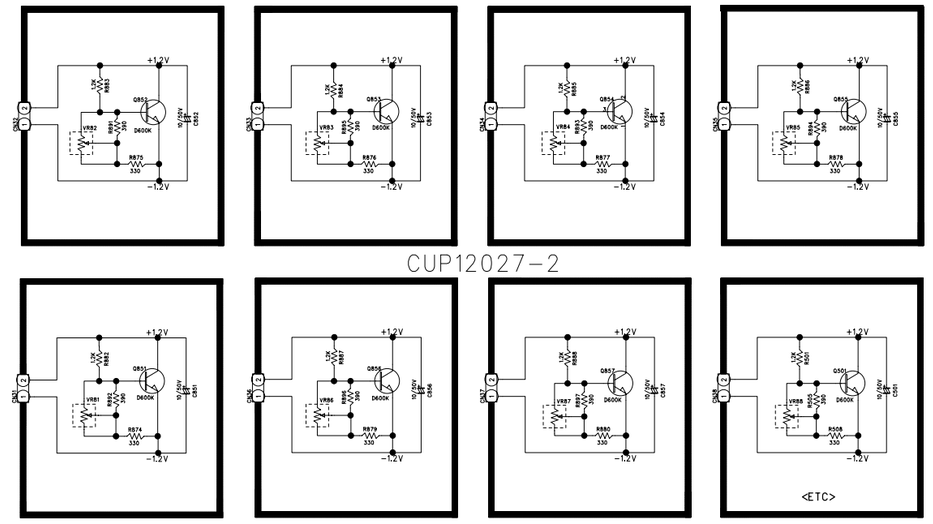
PIN FUNCTION
1. Adj/Gnd
2. Vout
3. Vin

CUP12027-1

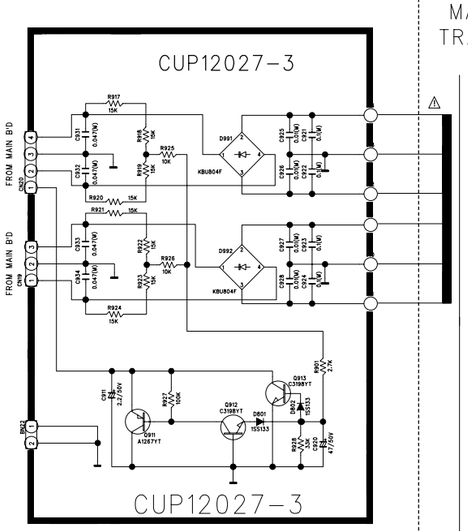


< OPTICAL IN & RS-232 PCB >

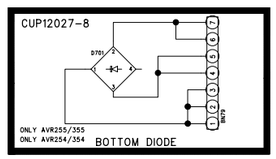
< BIAS T.R PCB >



CUP12027-3

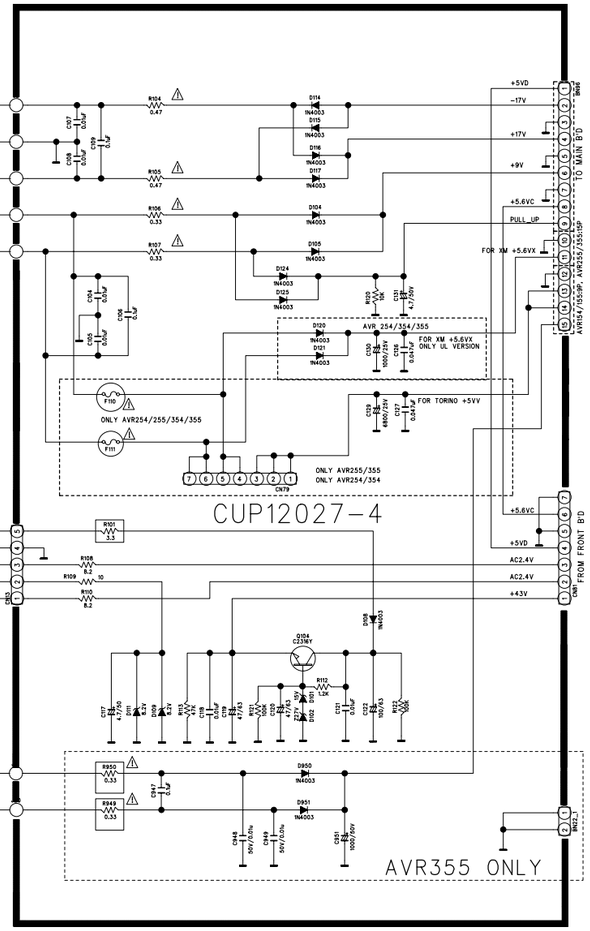


CUP12027-8

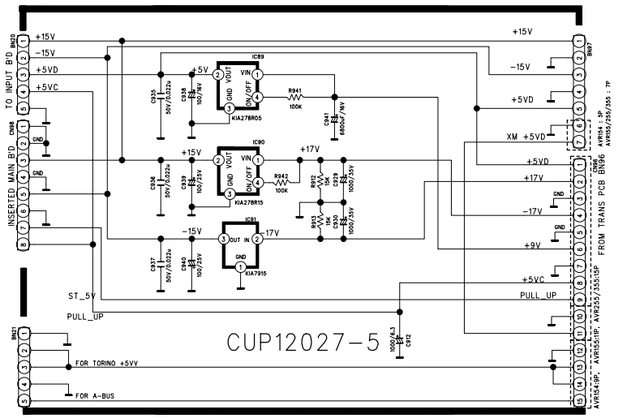


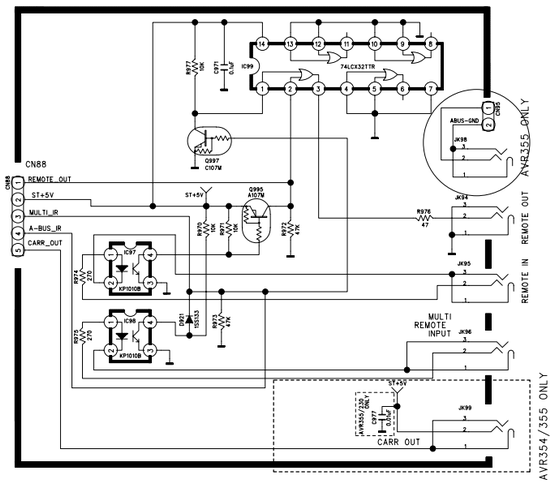
USA : AC120V 60Hz
EUR : AC230V 50Hz

MAIN TRANS



< TRANS PCB >

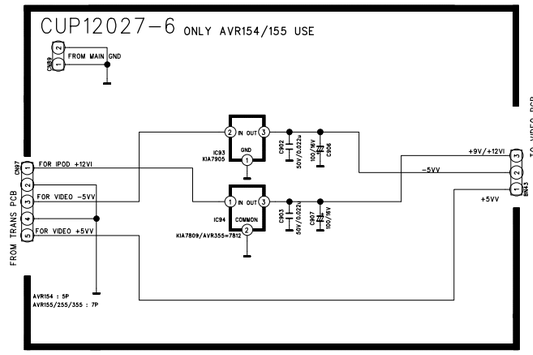




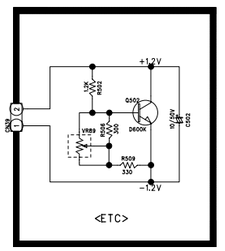
AVR254/255/354/355 ONLY CUP12027-7

< REMOTE IN/OUT PCB >

CUP12027-6 ONLY AVR154/155 USE



< REGULATOR PCB >



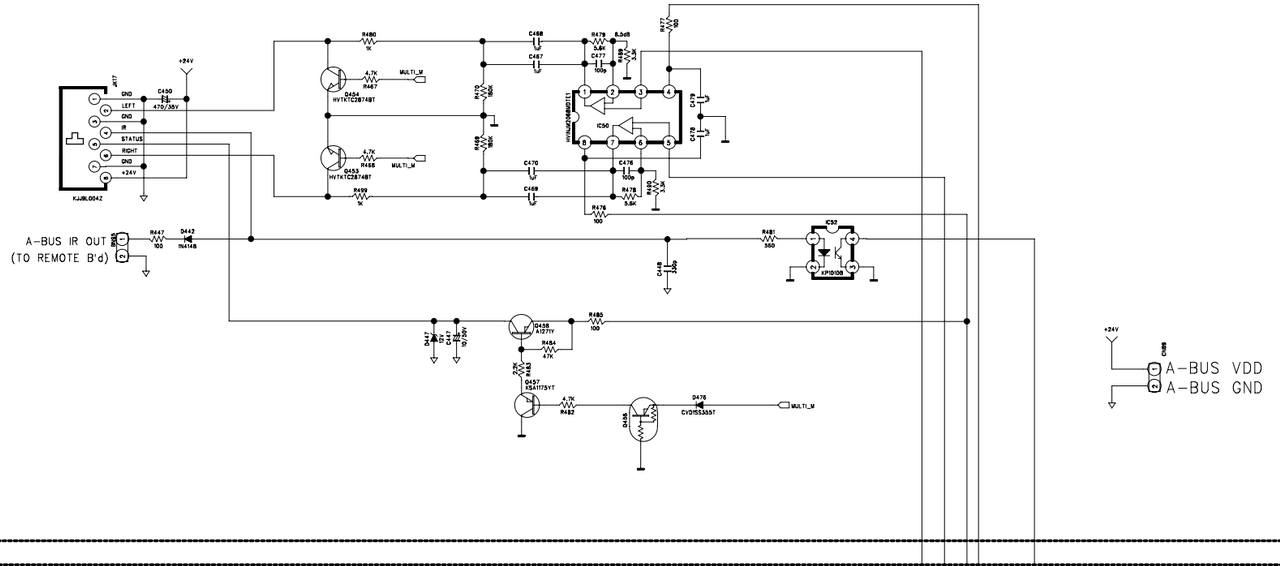
M P

SUE
2008.01.2

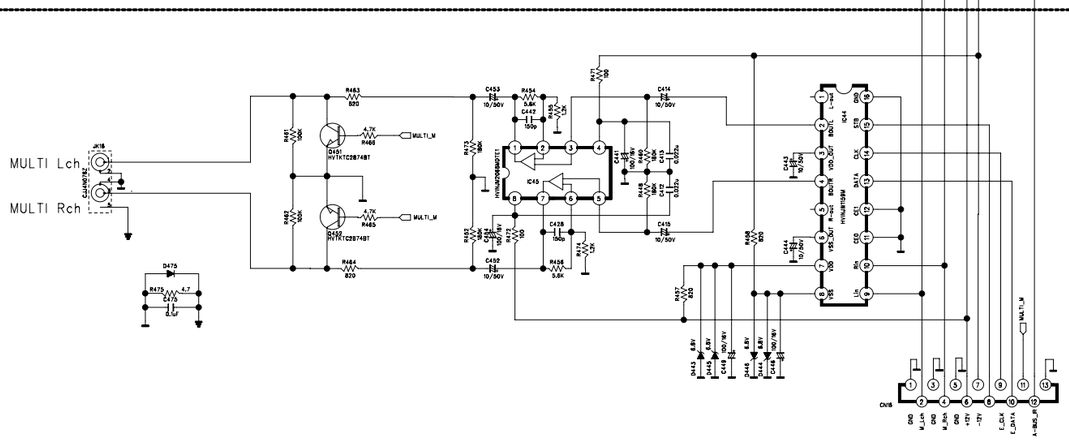
REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR x54/x55		1/1
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.B	Y.Y.W	K.S.W	CUP12027Z
08.01.22			(POWER) 1/1

A-BUS PART : ONLY FOR AVR355 & AVR355/230



MULTI ROOM VOLUME : AVR355, AVR354, AVR355/230



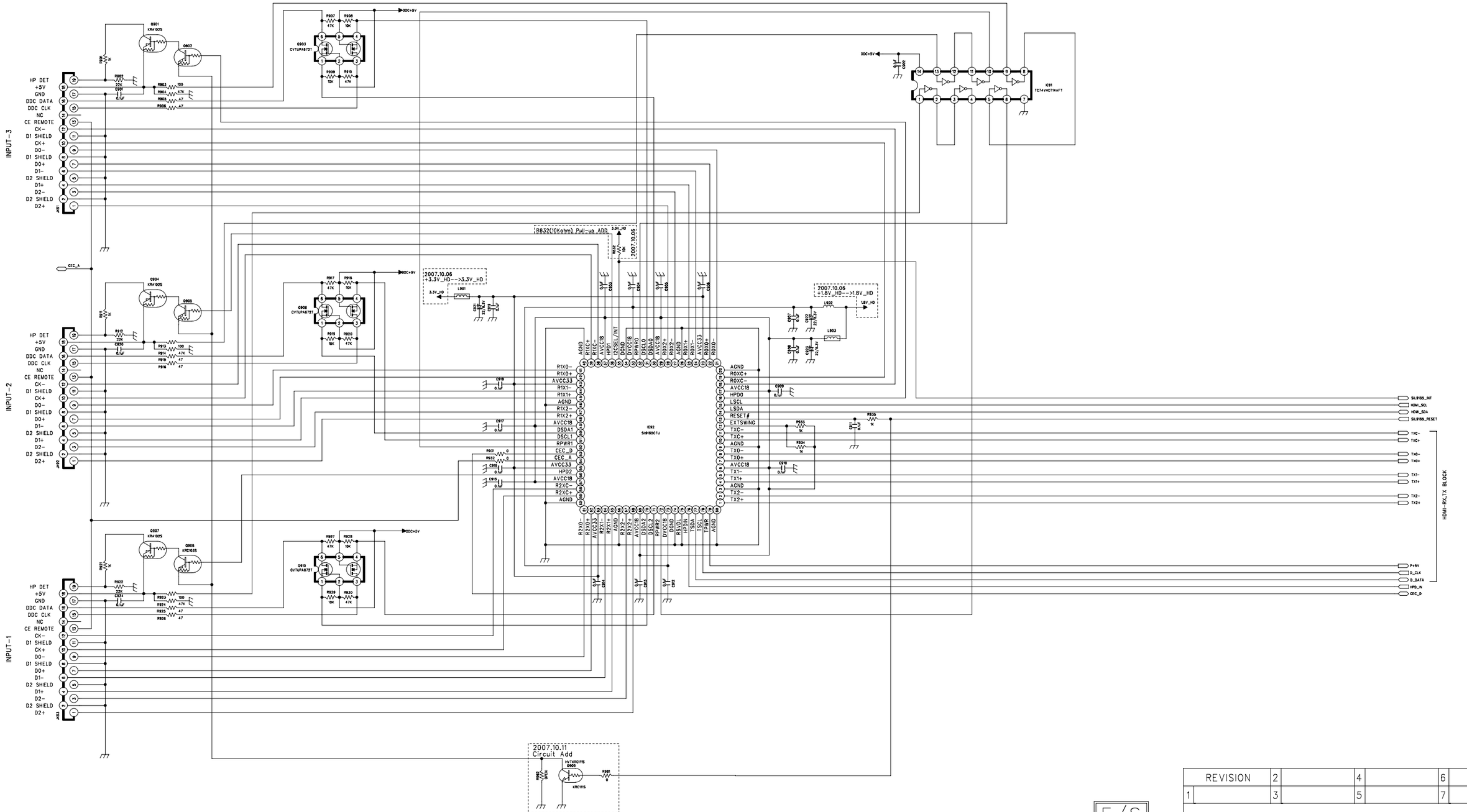
REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM				SHEET
MODEL	AVR354/355			1/1
DESIGN	CHECK	APPROVE	DRAWING NO	
K.S.S	W.Y.Y	G.S.W	CUP12036Z (MULTI)	1/1
07.10.18				

8.08

E/S

CUP12035Z



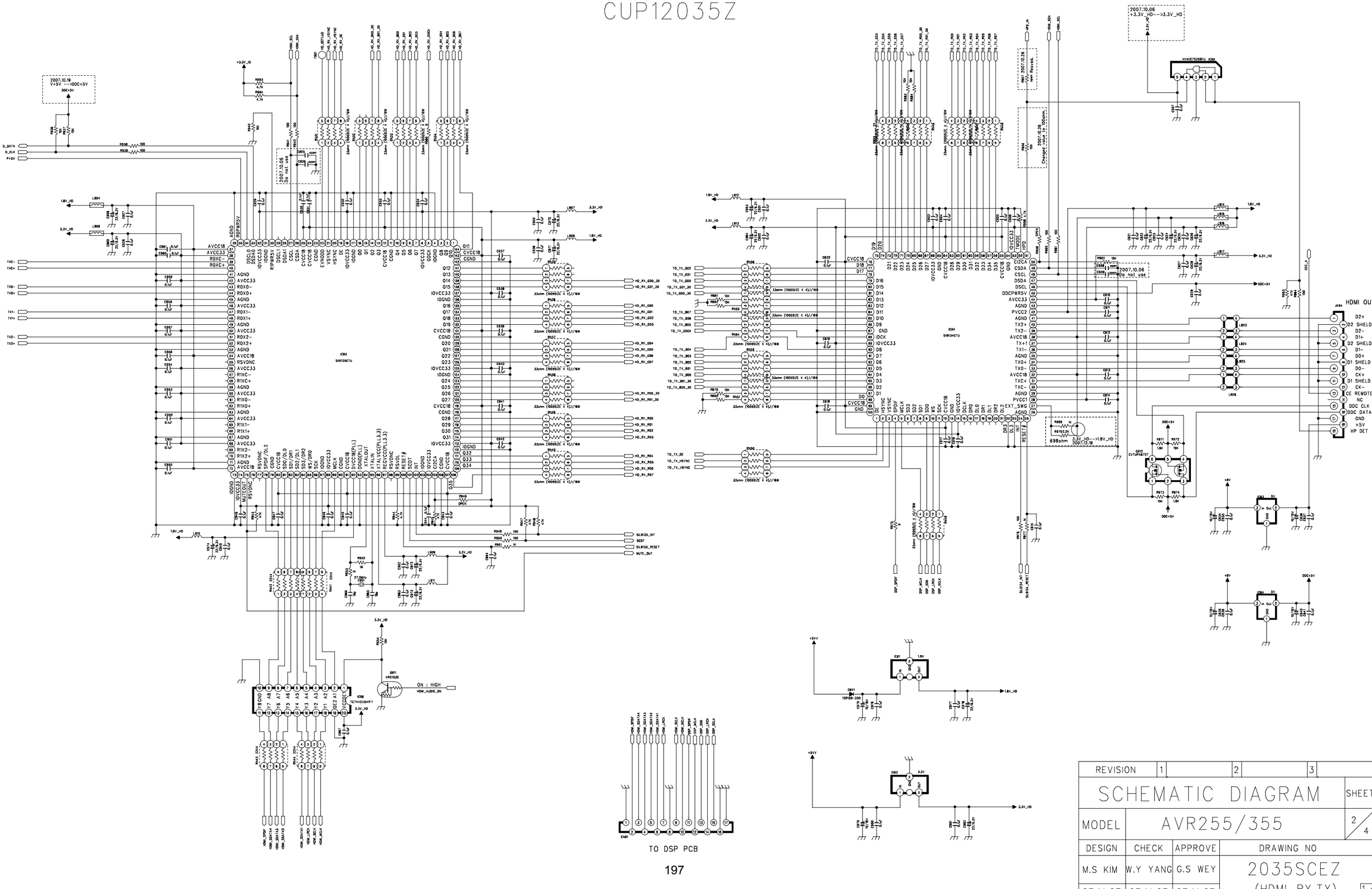
REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR255/355		1/4
DESIGN	CHECK	APPROVE	DRAWING NO
M.S KIM	W.Y YANG	G.S WEY	2035SCEZ (HDMI-INPUT) 1/1
07.14.07	07.14.07	07.14.07	

E/S

E

CUP12035Z



REVISION	1	2	3	
SCHEMATIC DIAGRAM				SHEET
MODEL	AVR255/355			2/4
DESIGN	CHECK	APPROVE	DRAWING NO	
M.S KIM	W.Y YANG	G.S WEY	2035SCEZ (HDMI-RX,TX)	1/1
07.14.07	07.14.07	07.14.07		

CUP12035Z

ANALOG VIDEO INPUT PORT

COMPONENT IN : 3EA
COMPOSITE IN : 1EA
S_VIDEO IN : 1EA

RGB 10BIT INPUT

B 8BIT INPUT

G 8BIT INPUT

R 8BIT INPUT

*OPTION(Do not use)

*GPROBE

*COMMUNICATION WITH MCU

*CONTROL ROM/VIDEO ENCODER

*EEPROM

*IR_IN/NO USE

*Add 08.01.16 Reserved GPIOs.

*DDR MEMORY INTERFACE

*FLASH MEMORY INTERFACE

B 8BIT OUTPUT

G 8BIT OUTPUT

R 8BIT OUTPUT

TTL OUTPUT

RGB 10BIT OUTPUT
TTL OUTPUT

* Need to change 2A

2007.10.06
Connect pin3 to CHGND

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 3/4

MODEL: AVR 255/355

DESIGN	CHECK	APPROVE	DRAWING NO
M.S KIM	W.Y YANG	G.S WEY	2035SCEZ (TORINO) 1/1
07.14.07	07.14.07	07.14.07	

CUP12035Z

DO NOT MOVE.

FLI30336 ANALOG INPUT

ADV7342 ANALOG OUTPUT

TO MCU

*OPTION(Do not use)

#VIDEO ENCORDER PART

44	DAC A	Y
43	DAC B	Pb
42	DAC C	Pr
39	DAC D	CVBS
38	DAC E	S-Y
37	DAC F	S-C

R854: 3.9kohm---->6.8kohm
R855: 6.8kohm---->4.3kohm
2007.11.03

Red DATA Input

Blue DATA Input

Green DATA Input

CLOCK DOUBLER(13.5MHz * 2 = 27MHz)

#DDR SDRAM *2EA

DRAWING NO

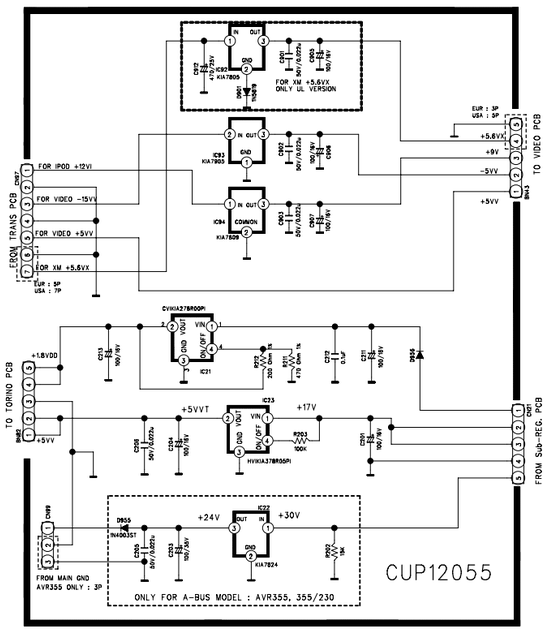
#FLASH MEMORY

REVISION	2	4	6	
1	3	5	7	

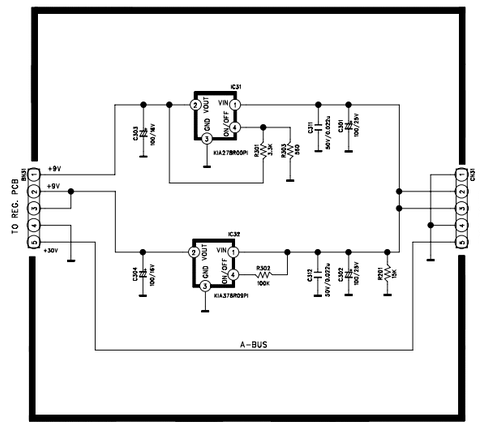
SCHEMATIC DIAGRAM — SHEET 1/4

MODEL	AVR255/355		
DESIGN	CHECK	APPROVE	DRAWING NO
M.S KIM	W.Y YANG	G.S WEY	2035SCEZ (ADV7342+MEM.) 1/1
07.14.07	07.14.07	07.14.07	

< REGULATOR PCB >



< Sub-REGULATOR PCB >



LPP

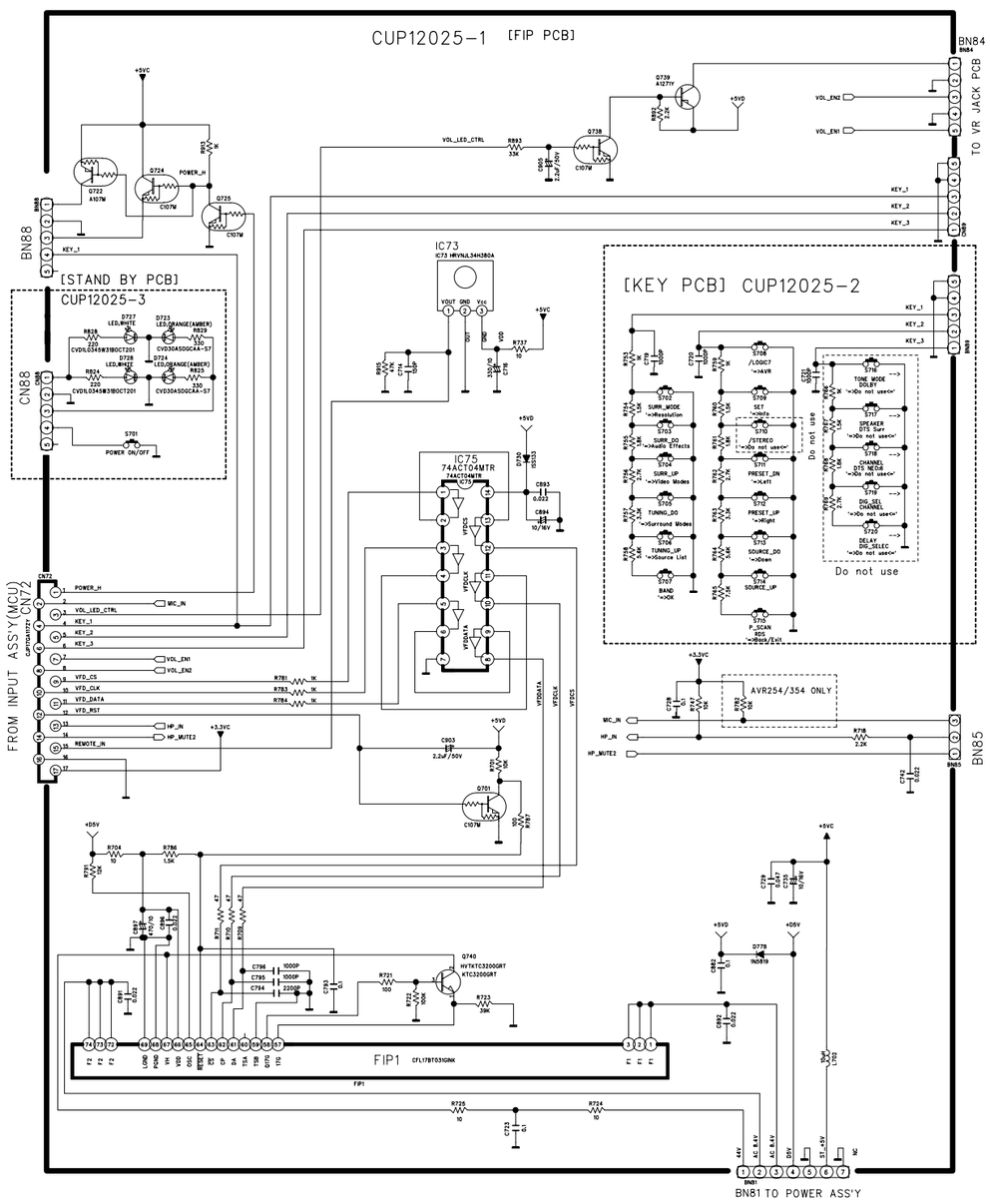
ISSUE

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM				SHEET
MODEL	AVR 254/255/354/355			1/1
DESIGN	CHECK	APPROVE	DRAWING NO	
J.T.B	Y.Y.W	K.S.W	CUP12055Z (REGULATOR)	1/1
08.01.19				

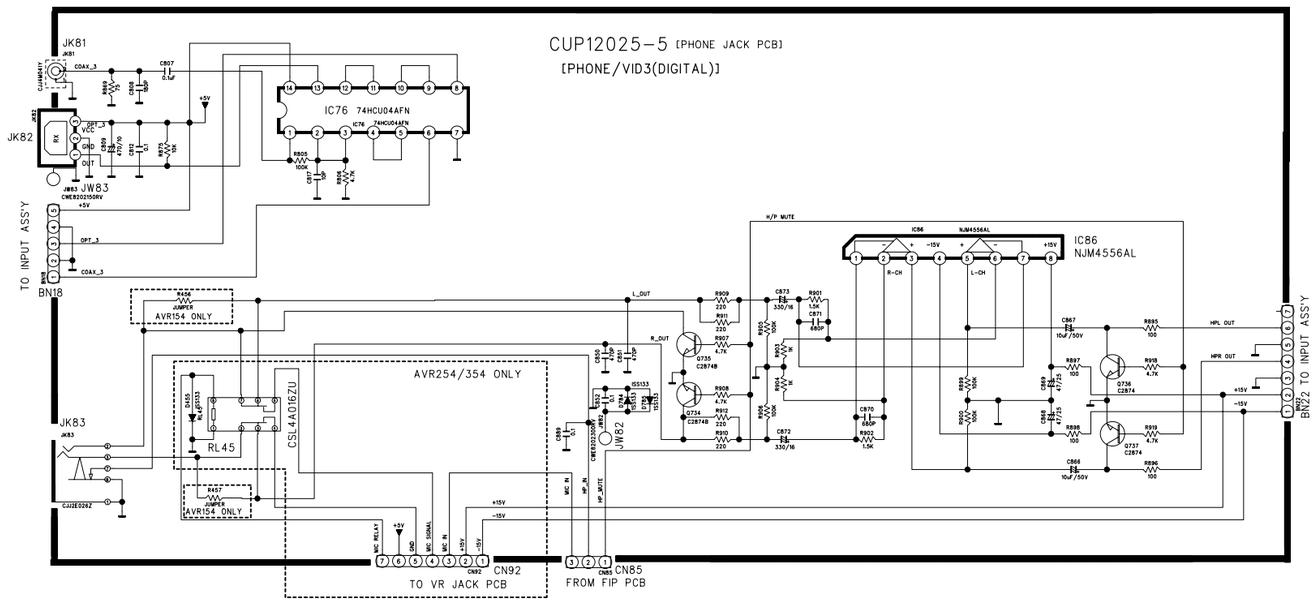
CUP12025Z

CUP12025-1 [FIP PCB]

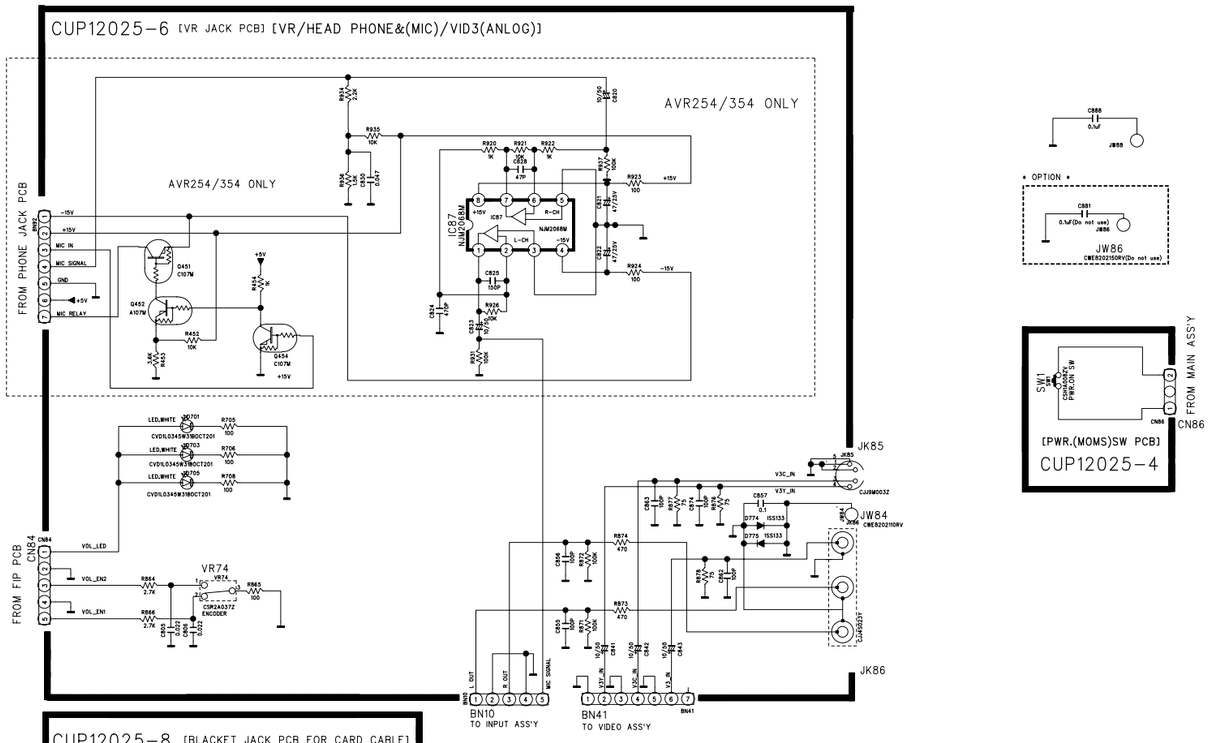


CUP12025-5 [PHONE JACK PCB]

[PHONE/VID3(DIGITAL)]



CUP12025-6 [VR JACK PCB] [VR/HEAD PHONE&(MIC)/VID3(ANLOG)]



CUP12025-8 [BLACKET JACK PCB FOR CARD CABLE]

CUP12025-9 [BLACKET JACK PCB FOR PHONE JACK]

* OPTION *

JW86 (CWE8202508V)(Do not use)

[PWR.(MOMS)SW PCB]
CUP12025-4
FROM MAIN ASS'Y
CN86

REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR154/254/354		1/7
DESIGN	CHECK	APPROVE	DRAWING NO
S.H.YANG	W.Y.YANG	G.S.WEY	2025SCDZ (FRONT)
07.12.07	07.12.07	07.12.07	1/1

LPP

ML 2007.12.07

R201 ~ R216 : 470ohm --> 100ohm
R219 ~ R223 : 470ohm --> 100ohm
R225 ~ R226 : 470ohm --> 100ohm

CD
TAPE R/O P/B
VIDEO3 R/O
VIDEO2
VIDEO1 P/B
DVD
8CH Lch
8CH Rch
8CH SLch
8CH SRch
8CH Cch
8CH SUB
8CH SBL
8CH SBR

AVR345(UL) ONLY
AVR345 (EUR) ONLY

MIC SIGNAL
From FRONT INPUT
CVJN81197CFC2
IC20

D_FR- D_FR+ D_FL+ D_FL- D_SW- D_SW+ D_CT+ D_CT- D_SR- D_SR+ D_SL+ D_SL- D_BR- D_BR+ D_BL+ D_BL-
exchange
option
DAC-R DAC-L DAC-SW DAC-C DAC-SR DAC-SL DAC-BR DAC-BL

VOL01 VOL-L VOL02 VOL-R VOL03 VOL-C VOL08 VOL-SW VOL04 VOL-SL VOL05 VOL-SR VOL06 VOL-BL VOL07 VOL-BR
IC21 IC31 IC22 IC32 IC23 IC33 IC24 IC34 IC25 IC35
HPL-OUT HPR-OUT L-OUT R-OUT C-OUT SW-OUT SL-OUT SR-OUT SBL-OUT SBR-OUT
FUNC_MUTE2 SB_MUTE2

FROM CONNECT B'D
DGND
FROM TUNER MODULE
T_CE T_DATA T_CLK T_DOUT TUNED STEREO TUNER-L TUNER-R MPX_OUT

IC36 HV9KIA7808API
IC37 CVKIA7908PI
IN4003

MULTI_PRE_L MULTI_PRE_R MULTI_LCH MULTI_RCH
I159_LATCH I159_CLK I159_DATA MULTI_MUTE2 ABUS_IR

FROM REG. B'D
ST+5V +5VD -15V +15V

** IMPORTANT SAFETY NOTICS.
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS.
IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS USE ONLY MANUFACTURER'S SPECIFIED PARTS.
** THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM , M=1000 KOHM
** THE UNIT OF CAPACITANCE IS MICROFARAD. (uF)
pF=10^{-6} uF
** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WITH THE IMPROVEMENT OF PERFORMANCE.

DPP

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM — SHEET

MODEL	AVR254/255/354/355	1/3
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2029SCLZ (INPUT) 1/1
07.10.18			

CUP12029

HDMI SPDIF MODE : DIR MASTER
HDMI I2S MODE : HDMI MASTER
ADC MODE : DSP MASTER
DIR MODE : DIR MASTER

CRJ10DJ1R0T

*OPTION : EMC COUNTERMEASUER

<=> HDMI BOARD

DATA	CS49700	SDRAM
EXT_D15/SD_D7	29	12
EXT_D14/SD_D6	30	11
EXT_D13/SD_D5	31	9
EXT_D12/SD_D4	32	8
EXT_D11/SD_D3	34	6
EXT_D10/SD_D2	35	5
EXT_D9/SD_D1	37	3
EXT_D8/SD_D0	39	2
EXT_D7/SD_D15	40	49
EXT_D6/SD_D14	41	48
EXT_D5/SD_D13	42	46
EXT_D4/SD_D12	43	45
EXT_D3/SD_D11	45	43
EXT_D2/SD_D10	46	42
EXT_D1/SD_D9	48	40
EXT_D0/SD_D8	49	39

Address	CS49700	SDRAM
EXT_A19	88	
EXT_A18	87	
EXT_A17	85	
EXT_A16	84	
EXT_A15	82	
EXT_A14/SD_A13	77	
EXT_A13/SD_A14	75	19
EXT_A12/SD_A10	74	20
EXT_A11/SD_A12	55	
EXT_A10/SD_A11	56	
EXT_A9/SD_A9	58	32
EXT_A8/SD_A8	59	31
EXT_A7/SD_A7	61	30
EXT_A6/SD_A6	62	29
EXT_A5/SD_A5	64	28
EXT_A4/SD_A4	67	27
EXT_A3/SD_A3	68	24
EXT_A2/SD_A2	70	23
EXT_A1/SD_A1	71	22
EXT_A0/SD_A0	72	21

DPP

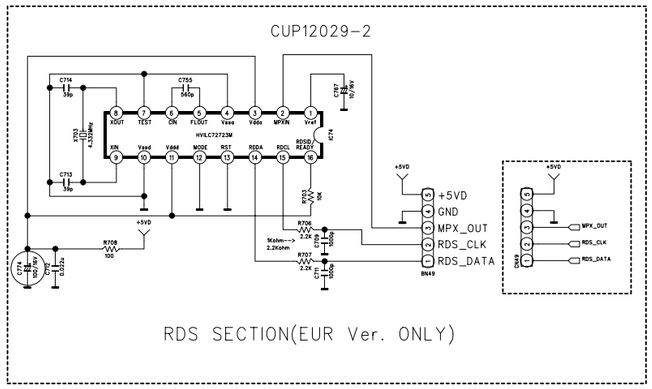
. UE
ML
2007.10.18

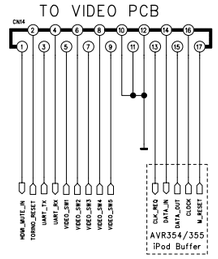
REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET

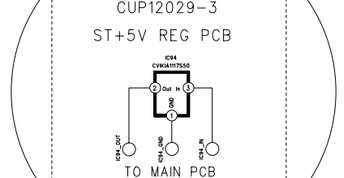
MODEL	AVR254/255/354/355	2/3

DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2029SCLZ (DSP) 1/1
07.10.18			



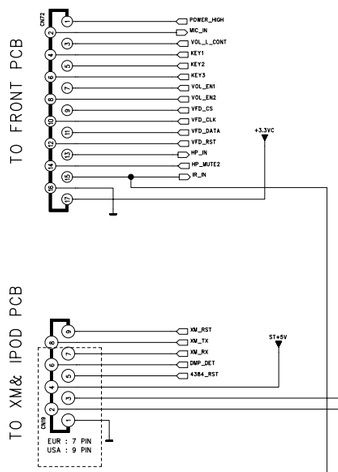


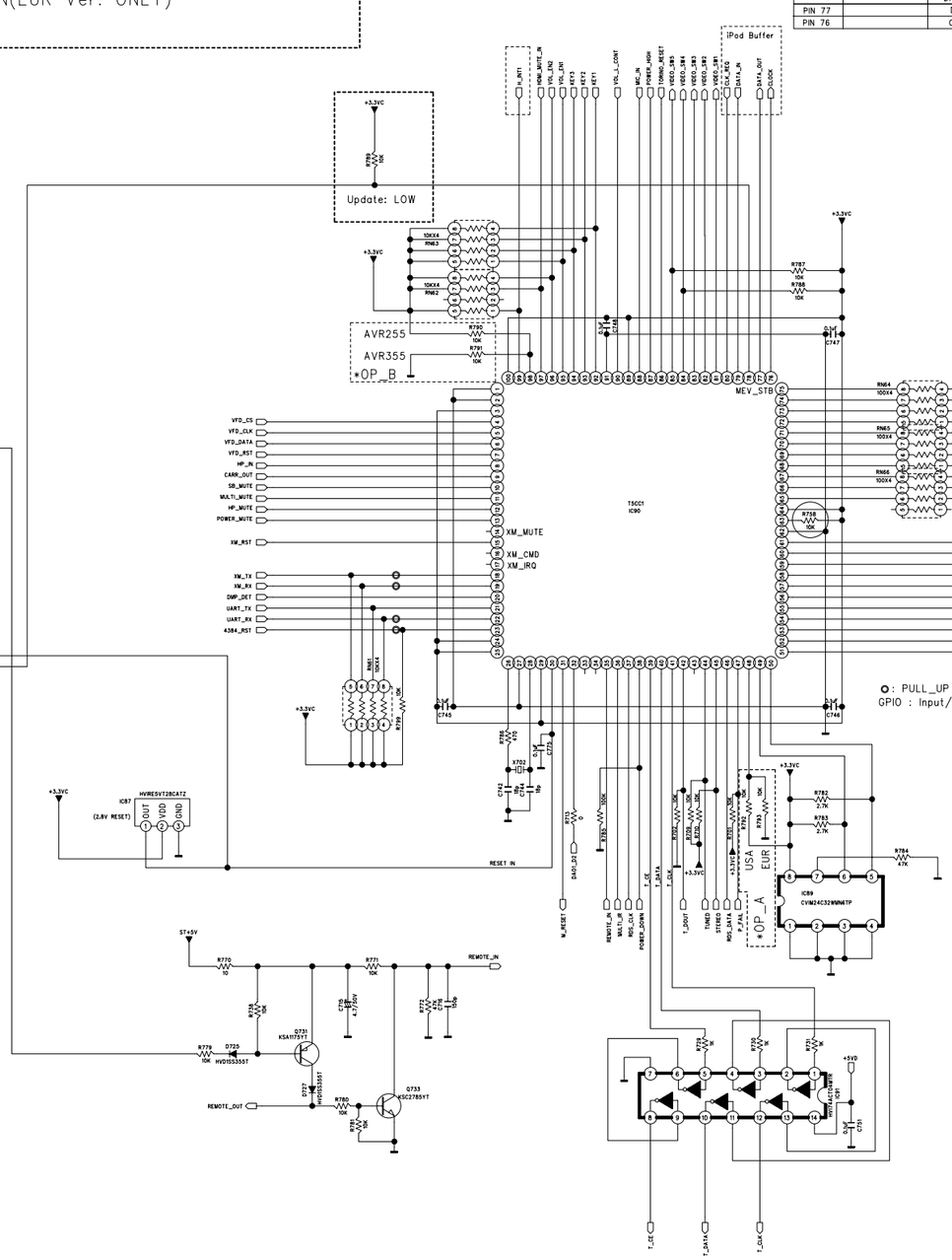
U-COM	AVR255	AVR355	AVR155
PIN 97	HDMI_MUTE_IN	HDMI_MUTE_IN	N.A
PIN 86	TORINO_RESET	TORINO_RESET	N.C
PIN 21	UART_TX(TORNO&PC)	UART_TX(TORNO&PC)	UART_TX(PC)
PIN 22	UART_RX(TORNO&PC)	UART_RX(TORNO&PC)	UART_RX(PC)
PIN 81	VIDEO_SW1	VIDEO_SW1	N.A
PIN 82	VIDEO_SW2	VIDEO_SW2	OSD_CS1
PIN 83	VIDEO_SW3	VIDEO_SW3	OSD_CLK
PIN 84	VIDEO_SW4	VIDEO_SW4	OSD_DA
PIN 85	VIDEO_SW5	VIDEO_SW5	OSD_M
PIN 80		CLOCK	HDMI MUX_SDA
PIN 79		DATA_OUT	HDMI MUX_SCLK
PIN 77		DATA_IN	OSD_H
PIN 76		CLK-REQ	



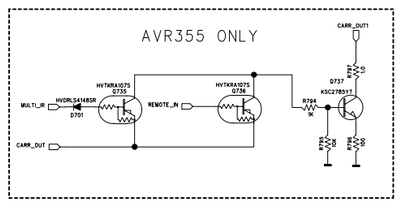
* MODEL OPTION *

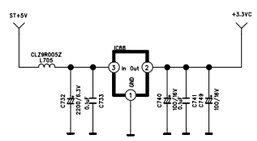
MODEL	OP_A(PIN48)	OP_B(PIN98)
AVR355	HIGH(R792)	LOW(R791)
AVR354	HIGH(R792)	LOW(R791)
AVR254	HIGH(R792)	HIGH(R790)
AVR355/230	LOW(R793)	LOW(R791)
AVR255/230	LOW(R793)	HIGH(R790)

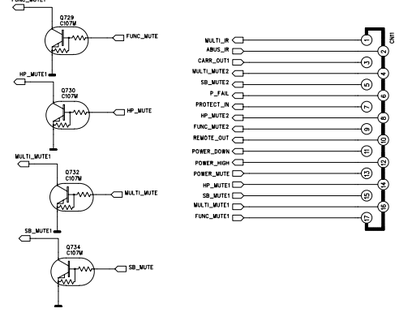




O : PULL_UP
GPIO : Input/Out Port(without pull_up resistor)







DPP

UE
MI
2007.10.18

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM — SHEET 3/3

MODEL	AVR254/255/354/355		
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2029SCLZ (CPU) 1/1
07.10.18			

CUP12033Z

FROM FRONT VIDEO JACK B'D

CN41

V3 S-V Y

V3 S-V C

V3 COMP

CVBS/S-VIDEO1

VIDEO2 OUT

CVBS/S-VIDEO2 IN

CVBS/S-VIDEO3 IN

MONITOR OUT

IC41 NJM2595M

IC42 NJM2595M

IC43 NJM2595M

Do not USE

ADD : R415"R420 2008.01.18

*NJM2595M OPTION
==>V_MUTE "LOW" ACTIVE

FUNC.	SW1	SW2	SW3	SW4	SW5
CVBS/S-V1	H	L	L	L	H
CVBS/S-V2	L	H	L	L	H
CVBS/S-V3	H	L	L	H	H
FRONT CVBS/S-V	H	H	L	L	H
IPOD	H	L	H	H	H

* DEFINITION OF I2C REGISTER (NJW1321)

I2C BUS FORMAT

MSB	LSB	MSB	LSB	MSB	LSB		
S(1BIT)	SLAVE ADDRESS(8BIT)	A(1BIT)	DATA(8BIT)	A(1BIT)	DATA(8BIT)	A(1BIT)	P(1BIT)

S : Starting Term
A : Acknowledge Bit
P : Ending Term

SLAVE ADDRESS

MSB	Slave Address(8BIT)							MSB	Hex
1	0	0	0	0	0	ADR(1BIT)		R/NOT W(1BIT)	--

R/NOT W : Set the Write Mode or Read Mode.
ADR : Set the Slave Address by " ADR" terminal.
R/NOT W = 0 : WRITE MODE, ADR = 0/1 ; ADR=0 Hex94(h), ADR=1 Hex96(h)
R/NOT W = 0 : READ MODE, ADR = 0/1 ; ADR=0 Hex95(h), ADR=1 Hex97(h)

CONTROL REGISTER TABLE
<WRITE MODE>

NO.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
DATA 1	PS1	PS2	OUT1			OUT2		
DATA 2	AUX0		AUX1		AUX2		AUX3	

PS : POWER SAVE
=> PS = 1 ; POWER SAVE ON (MUTE), PS = 0 ; POWER SAVE OFF (OUT ON)
OUT : OUTPUT
AUX : AUXILIARY (CONTROL SIGNAL OUTPUT)

<READ MODE>

NO.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
DATA	PORT0		PORT1		PORT2		PORT3	

PORT : INPUT

JK62 COMPONENT IN1 & COMPONENT IN2

JK69 COMPONENT OUT

22P-->2P EUR Ver. ONLY

FROM POWER PCB

EUR Ver. : 3P
USA Ver. : 5P

FLI30336 ANALOG INPUT

ADV7342 ANALOG OUTPUT

FROM MCU

BN81

CN14

FROM MCU PCB

iPod Buffer AVR354/355

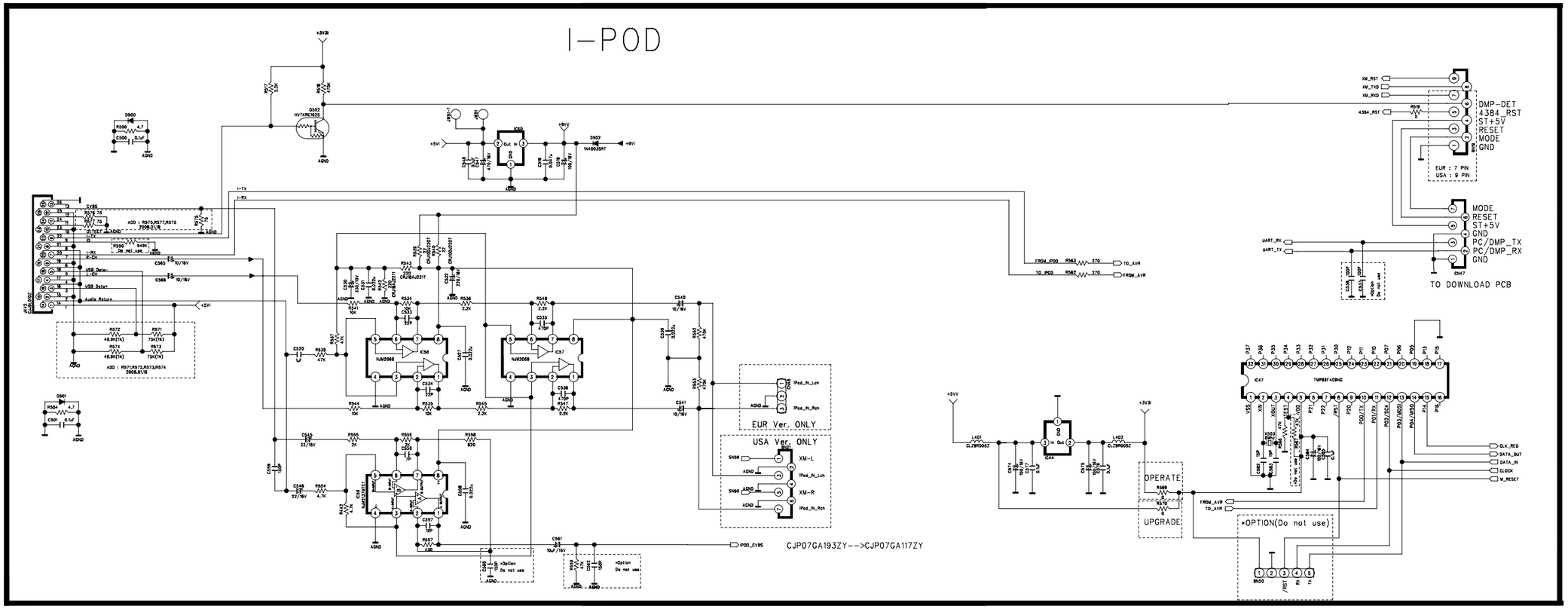
* AVR345 =NO.4

REVISION	2		4		6	
1		3		5		7

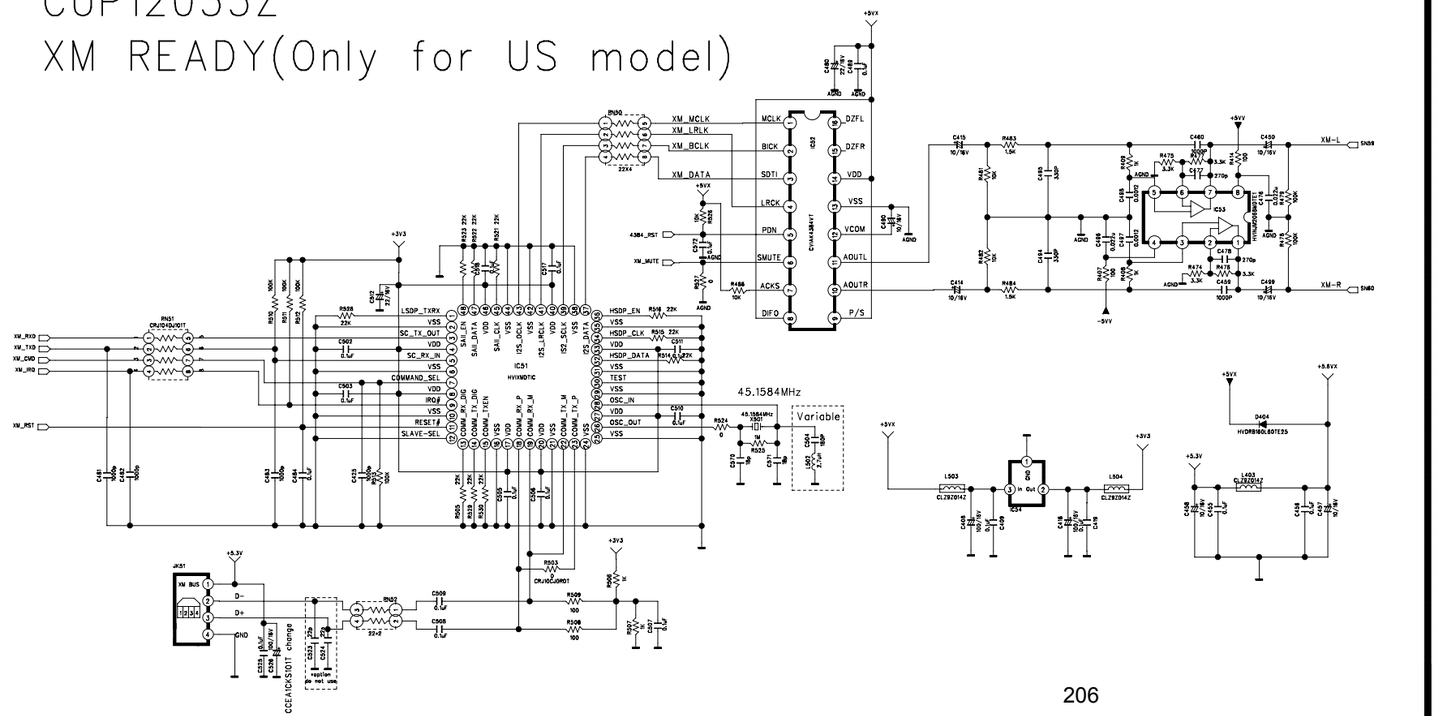
SCHEMATIC DIAGRAM				SHEET
MODEL	AVR354 /355			1/2
DESIGN	CHECK	APPROVE	DRAWING NO	
M.S.K	W.Y.Y	K.S.W	2033SCEZ	
06.08.23	06.	06.	(VIDEO)	1/1

DPP

I-POD



CUP12033Z
XM READY(Only for US model)



206

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR354 / 355		1/4
DESIGN	CHECK	APPROVE	DRAWING NO
M.S.K	W.Y.Y	K.S.W	2033SCEZ (AMP)
05.00.00	05.00.00	05.00.00	1/1

SR-CH

BL-CH

SL-CH

BR-CH

C-CH

FR-CH

FL-CH

EXCEPT AVR154/155

ONLY FAN USING

DC PROTECTOR

THERMAL PROTECTOR

OVERLOAD DETECTION

FOR USING FAN

JK91

JK92

BN19

BN20

BN87

EXCEPT AVR154/155

ONLY AVR154/155

AVR354/355 ONLY

JW90,JW91 : ALL MODELS

AVR254/255/354/355 PART

TO REMOTE IN/OUT B'D

FROM TRANS

AC IN

TO REG B'D

JW93, OL91, F902 : EXCEPT AVR154

FROM INPUT B'D

FROM TRANS B'D

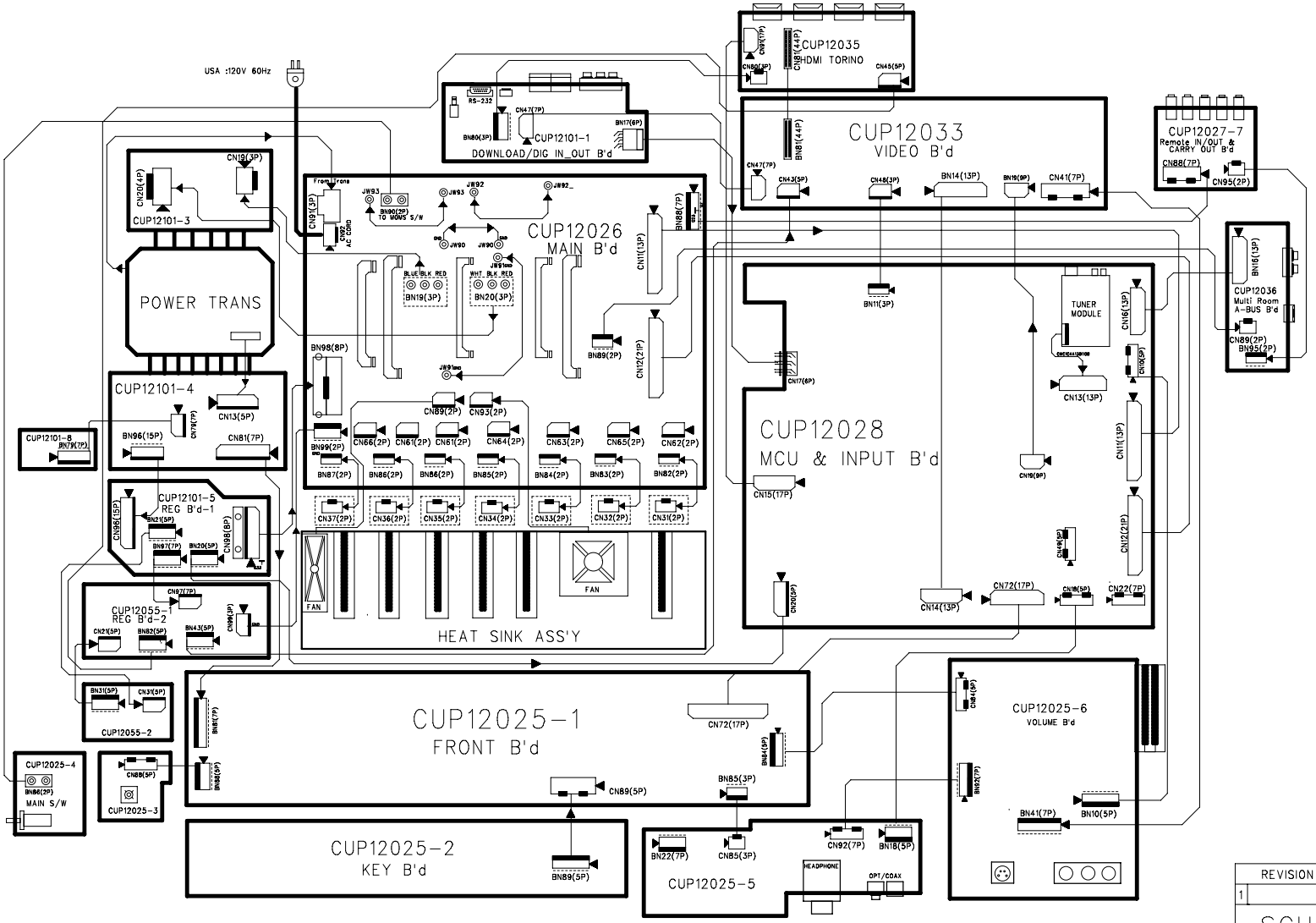
AVR254/255/354/355 OPTION

GAIN	R561, R562, R563, R564, R565, R850 R851
AVR154/155	1.8K
AVR255/355	1.6K

** IMPORTNAT SAFETY NOTICE.
INPORTANT FOR SAFETY WHEN REPLACING ANY OF THESE COMPONENTS USE ONLY MANUFACTURE'S SPECIFIED PARTS.
** THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM.
** THE UNIT OF CAPACITANCE IS MICROFARAD (uF)
pF = 10^-6 uF
** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WIHE THE IMPROVEMENT OF PERFORMANCE

REVISION	1	2	3	SHEET
SCHEMATIC DIAGRAM				
MODEL	AVR154/155/254/255/354/355			2 / 7
DESIGN	CHECK	APPROVE	DRAWING NO	
C.B.LEE	W.Y.YANG	G.S.WEY	2026SCLZ (MAIN)	1/1
07.08.23				

AVR354 WIRING DIAGRAM



REVISION					
SCHEMATIC DIAGRAM				SHEET	
MODEL	AVR354			1/1	
DESIGN	CHECK	APPROVE	DRAWING NO		
J.T.B	W.Y.Y	K.S.W	WIRING DIAGRAM		
08.03.11	08.03.11	08.03.11	1190SCDZ	1/1	