9. 8bit Serial Expansion Interface (SEI): 1 channel

   (MSB/LSB selectable and max. 4Mbps at 16MHz)

10. 10-bit successive approximation type AD converter
    - Analog input: 6 ch
11. Key-on wakeup : 4 channels
12. Clock operation

    Single clock mode

    Dual clock mode

13. Low power consumption operation

    STOP mode: Oscillation stops. (Battery/Capacitor back-up.)

    SLOW1 mode: Low power consumption operation using low-frequency clock.(High-frequency clock stop.)

    SLOW2 mode: Low power consumption operation using low-frequency clock.(High-frequency clock oscillate.)

    IDLE0 mode: CPU stops, and only the Time-Based-Timer(TBT) on peripherals operate using high frequency clock. Release by falling edge of the source clock which is set by TBTCR<TBTCK>.

    IDLE1 mode: CPU stops and peripherals operate using high frequency clock. Release by interruputs(CPU restarts).

    IDLE2 mode: CPU stops and peripherals operate using high and low frequency clock. Release by interruputs. (CPU restarts).

    SLEEP0 mode: CPU stops, and only the Time-Based-Timer(TBT) on peripherals operate using low frequency clock.Release by falling edge of the source clock which is set by TBTCR<TBTCK>.

    SLEEP1 mode: CPU stops, and peripherals operate using low frequency clock. Release by interruput.(CPU restarts).

    SLEEP2 mode: CPU stops and peripherals operate using high and low frequency clock. Release by interruput.

14. Wide operation voltage:

    4.5 V to 5.5 V at 16MHz /32.768 kHz

    2.7 V to 5.5 V at 8 MHz /32.768 kHz

TOSHIBA

1.2 Pin Assignment

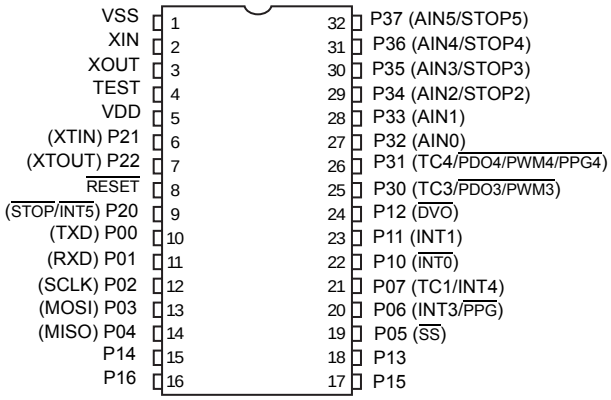


Figure 1-1 Pin Assignment

1.3 Block Diagram

1.3 Block Diagram

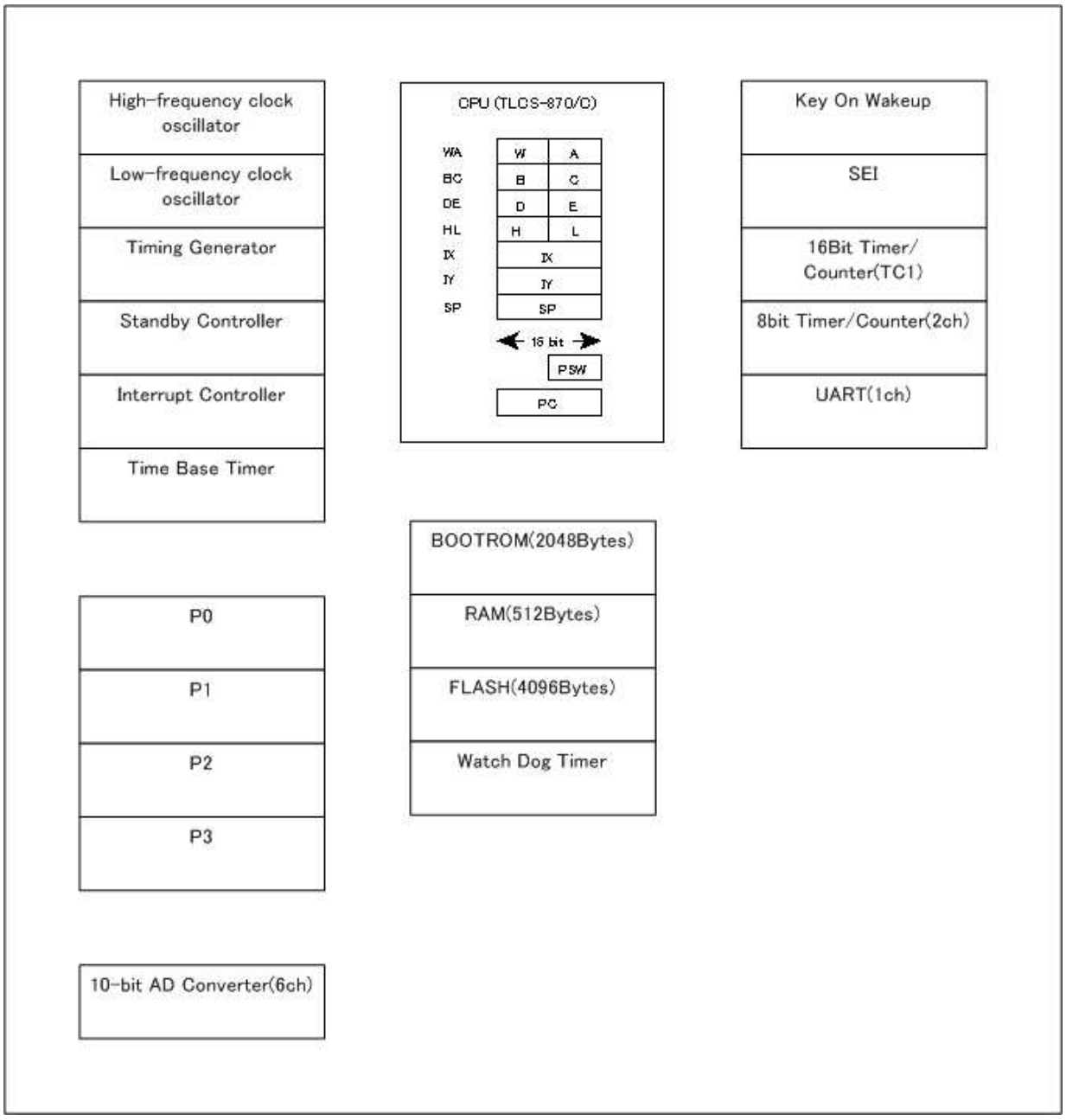


Figure 1-2 Block Diagram

1.4 Pin Names and Functions

The TMP86F409NG has MCU mode, parallel PROM mode, and serial PROM mode. Table 1-1 shows the pin functions in MCU mode. The serial PROM mode is explained later in a separate chapter.

Table 1-1 Pin Names and Functions(1/2)

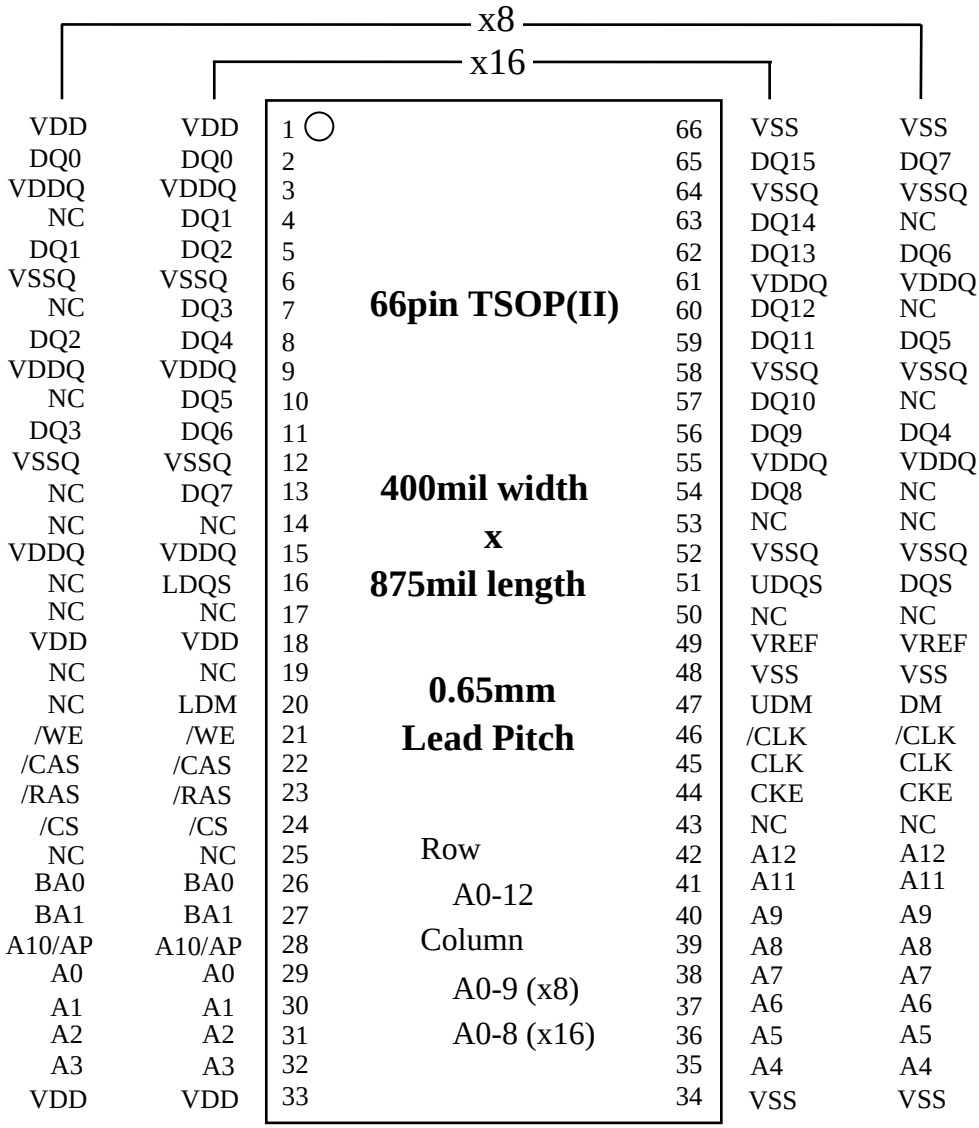
Pin Name	Pin Number	Input/Output	Functions
P07 TC1 INT4	21	IO I I	PORT07 TC1 input External interrupt 4 input
P06 INT3 $\overline{PPG}$	20	IO I O	PORT06 External interrupt 3 input PPG output
P05 $\overline{SS}$	19	IO I	PORT05 SEI master/slave select input
P04 MISO	14	IO IO	PORT04 SEI master input, slave output
P03 MOSI	13	IO IO	PORT03 SEI master input, slave output
P02 SCLK	12	IO IO	PORT02 SEI serial clock input/output pin
P01 RXD	11	IO I	PORT01 UART data input
P00 TXD	10	IO O	PORT00 UART data output
P16	16	IO	PORT16
P15	17	IO	PORT15
P14	15	IO	PORT14
P13	18	IO	PORT13
P12 $\overline{DVO}$	24	IO O	PORT12 Divider Output
P11 INT1	23	IO I	PORT11 External interrupt 1 input
P10 $\overline{INT0}$	22	IO I	PORT10 External interrupt 0 input
P22 XTOUT	7	IO O	PORT22 Resonator connecting pins(32.768kHz) for inputting external clock
P21 XTIN	6	IO I	PORT21 Resonator connecting pins(32.768kHz) for inputting external clock
P20 $\overline{INT5}$ $\overline{STOP}$	9	IO I I	PORT20 External interrupt 5 input STOP mode release signal input
P37 AIN5 STOP5	32	IO I I	PORT37 Analog Input5 STOP5
P36 AIN4 STOP4	31	IO I I	PORT36 Analog Input4 STOP4

Table 1-1 Pin Names and Functions(2/2)

Pin Name	Pin Number	Input/Output	Functions
P35 AIN3 STOP3	30	IO I I	PORT35 Analog Input3 STOP3
P34 AIN2 STOP2	29	IO I I	PORT34 Analog Input2 STOP2
P33 AIN1	28	IO I	PORT33 Analog Input1
P32 AIN0	27	IO I	PORT32 Analog Input0
P31 TC4 $\overline{\text{PDO4/PWM4/PPG4}}$	26	IO I O	PORT31 TC4 input PDO4/PWM4/PPG4 output
P30 TC3 $\overline{\text{PDO3/PWM3}}$	25	IO I O	PORT30 TC3 input PDO3/PWM3 output
XIN	2	I	Resonator connecting pins for high-frequency clock
XOUT	3	O	Resonator connecting pins for high-frequency clock
$\overline{\text{RESET}}$	8	I	Reset signal
TEST	4	I	Test pin for out-going test. Normally, be fixed to low.
VDD	5	I	+5V
VSS	1	I	0(GND)

A3S56D30ETP
A3S56D40ETP
256M Double Data Rate Synchronous DRAM

Pin Assignment (Top View) 66-pin TSOP



x16	x8	Pin	Pin	x16	x8
VDD	VDD	1	66	VSS	VSS
DQ0	DQ0	2	65	DQ15	DQ7
VDDQ	VDDQ	3	64	VSSQ	VSSQ
NC	DQ1	4	63	DQ14	NC
DQ1	DQ2	5	62	DQ13	DQ6
VSSQ	VSSQ	6	61	VDDQ	VDDQ
NC	DQ3	7	60	DQ12	NC
DQ2	DQ4	8	59	DQ11	DQ5
VDDQ	VDDQ	9	58	VSSQ	VSSQ
NC	DQ5	10	57	DQ10	NC
DQ3	DQ6	11	56	DQ9	DQ4
VSSQ	VSSQ	12	55	VDDQ	VDDQ
NC	DQ7	13	54	DQ8	NC
NC	NC	14	53	NC	NC
VDDQ	VDDQ	15	52	VSSQ	VSSQ
NC	LDQS	16	51	UDQS	DQS
NC	NC	17	50	NC	NC
VDD	VDD	18	49	VREF	VREF
NC	NC	19	48	VSS	VSS
NC	LDM	20	47	UDM	DM
/WE	/WE	21	46	/CLK	/CLK
/CAS	/CAS	22	45	CLK	CLK
/RAS	/RAS	23	44	CKE	CKE
/CS	/CS	24	43	NC	NC
NC	NC	25	42	A12	A12
BA0	BA0	26	41	A11	A11
BA1	BA1	27	40	A9	A9
A10/AP	A10/AP	28	39	A8	A8
A0	A0	29	38	A7	A7
A1	A1	30	37	A6	A6
A2	A2	31	36	A5	A5
A3	A3	32	35	A4	A4
VDD	VDD	33	34	VSS	VSS

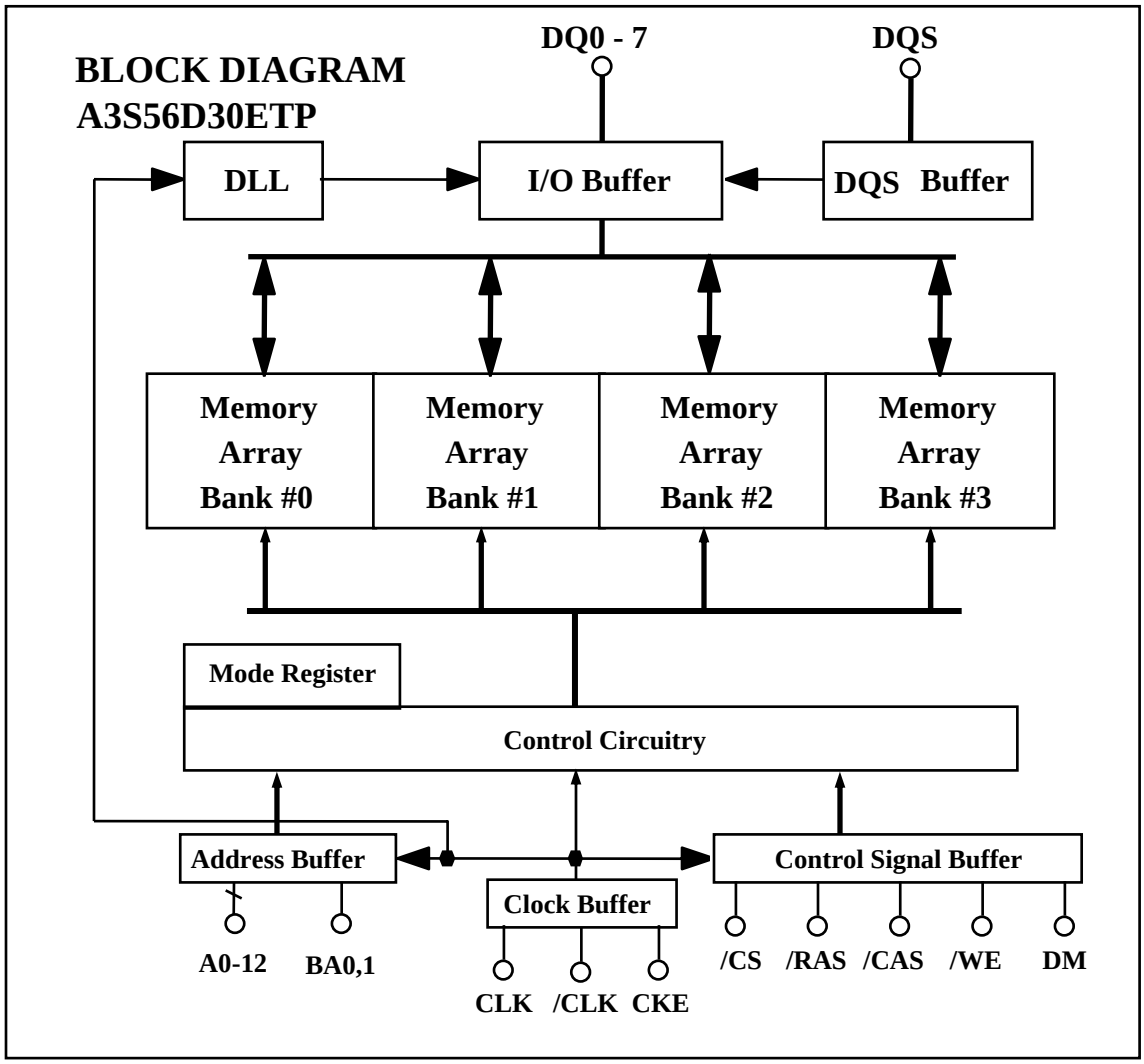
CLK, /CLK	**: Master Clock**	**A0-12**	**: Address Input**
CKE	**: Clock Enable**	**BA0,1**	**: Bank Address Input**
/CS	**: Chip Select**	**Vdd**	**: Power Supply**
/RAS	**: Row Address Strobe**	**VddQ**	**: Power Supply for Output**
/CAS	**: Column Address Strobe**	**Vss**	**: Ground**
/WE	**: Write Enable**	**VssQ**	**: Ground for Output**
DQ0-15	**: Data I/O (x16)**		
DQ0-7	**: Data I/O (x8)**		
UDM, LDM	**: Write Mask (x16)**		
DM	**: Write Mask (x8)**		
UDQS, LDQS	**: Data Strobe (x16)**		
DQS	**: Data Strobe (x8)**		

A3S56D30ETP
A3S56D40ETP
256M Double Data Rate Synchronous DRAM

PIN FUNCTION

SYMBOL	TYPE	DESCRIPTION
CLK, /CLK	Input	Clock: CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK. Output (read) data is referenced to the crossings of CLK and /CLK (both directions of crossing).
CKE	Input	Clock Enable: CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low.
/CS	Input	Chip Select: When /CS is high, any command means No Operation.
/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
A0-12	Input	A0-12 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-12. The Column Address is specified by A0-9(x8) and A0-8(x16). A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
BA0,1	Input	Bank Address: BA0,1 specifies one of four banks to which a command is applied. BA0,1 must be set with ACT, PRE, READ, WRITE commands.
DQ0-7 (x8), DQ0-15 (x16),	Input / Output	Data Input/Output: Data bus
DQS (x8) UDQS, LDQS (x16)	Input / Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS correspond to the data on DQ8-DQ15
DM (x8) UDM, LDM (x16)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-DQ7; UDM corresponds to the data on DQ8-DQ15.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
VddQ, VssQ	Power Supply	VddQ and VssQ are supplied to the Output Buffers only.
Vref	Input	SSTL_2 reference voltage.

A3S56D30ETP
A3S56D40ETP
256M Double Data Rate Synchronous DRAM



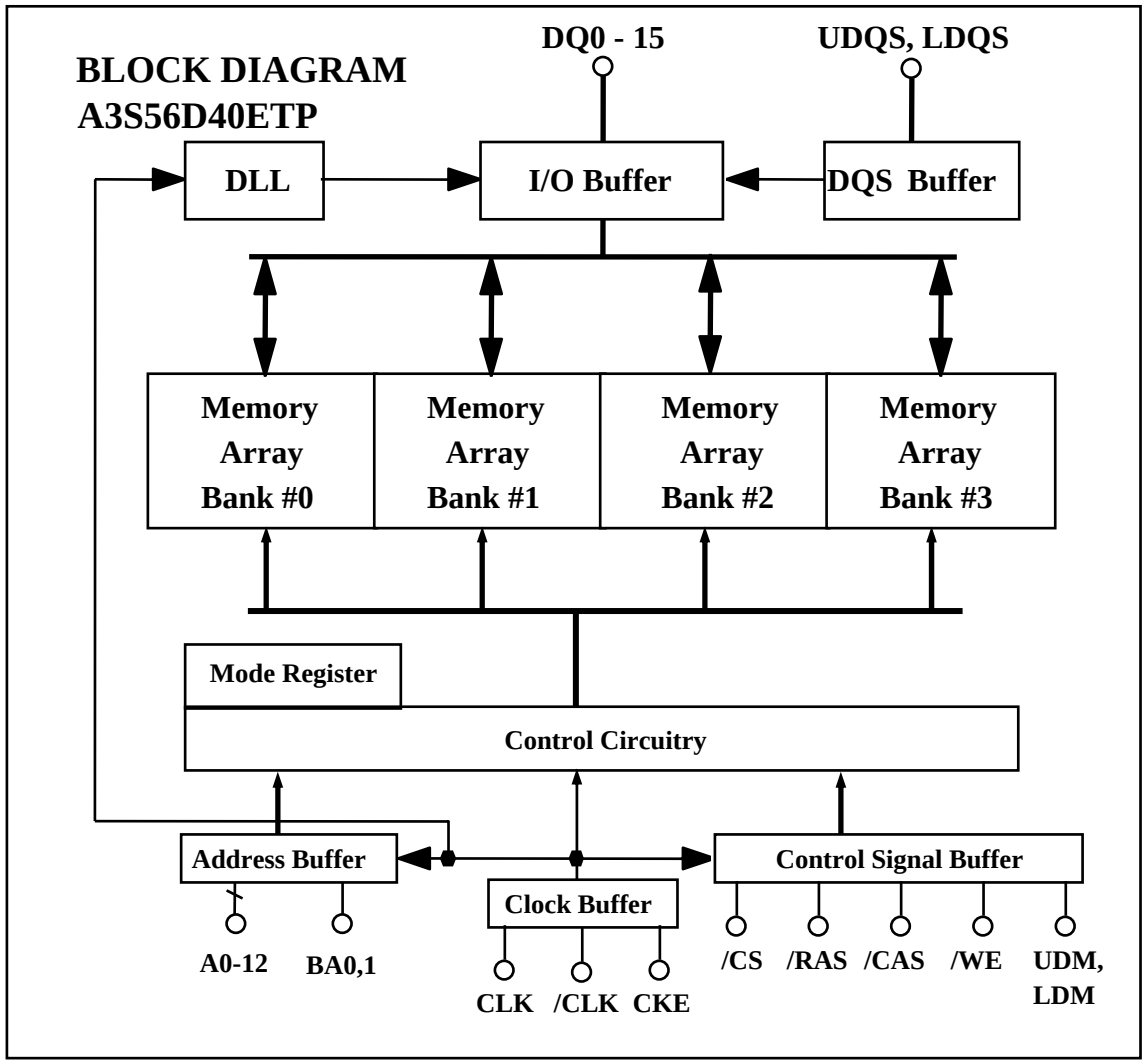
Type Designation Code

This rule is applied to only Synchronous DRAM family.

A 3 S 56 D 3 0 E TP –G5

- Speed Grade 6: 166MHz @CL=3.0/2.5, and 133MHz @CL=2.0
  5: 200MHz @CL=3.0, 166MHz @CL=2.5, and 133MHz @CL=2.0
  5E: 200MHz @CL=3.0/2.5, and 133MHz @CL=2.0
- Package Type TP: TSOP(II)
- Process Generation
- Function Reserved for Future Use
- Organization 2^n 3: x8
- **DDR Synchronous DRAM**
- Density 56: 256M bits
- Interface S:SSTL_3, _2
- Memory Style (DRAM)
- Zentel DRAM

A3S56D30ETP
A3S56D40ETP
256M Double Data Rate Synchronous DRAM



Type Designation Code

This rule is applied to only Synchronous DRAM family.

A 3 S 56 D 4 0 E TP –G5

- Speed Grade — 6: 166MHz @CL=3.0/2.5, and 133MHz @CL=2.0; 5: 200MHz @CL=3.0, 166MHz @CL=2.5, and 133MHz @CL=2.0; 5E: 200MHz @CL=3.0/2.5, and 133MHz @CL=2.0
- Package Type TP: TSOP(II)
- Process Generation
- Function Reserved for Future Use
- Organization 2^n 4: x16
- **DDR Synchronous DRAM**
- Density 56: 256M bits
- Interface S:SSTL_3, _2
- Memory Style (DRAM)
- Zentel DRAM

Excel Semiconductor inc.

ES29LV320E

32Mbit(4M x 8/2M x 16)
CMOS 3.0 Volt-only, Boot Sector Flash Memory

GENERAL FEATURES

- **Single power supply operation**
  - 2.7V ~ 3.6V for read, program and erase operations
- **Sector Structure**
  - 8Kbyte x 8 boot sectors
  - 64Kbyte x 63 sectors
  - 256byte security sector
- **Top or Bottom boot block**
  - ES29LV320ET for Top boot block device
  - ES29LV320EB for Bottom boot block device
- **A 256 bytes of extra sector for security code**
  - Factory locked
  - Customer lockable
- **Package Options**
  - 48-pin TSOP
  - 48-ball FBGA
  - Pb-free packages
  - All Pb-free products are RoHS-Compliant
- **Low Vcc write inhibit**
- **Manufactured on 0.18um process technology**
- **Compatible with JEDEC standards**
  - Pinout and software compatible with single-power supply flash standard

DEVICE PERFORMANCE

- **Read access time**
  - 70ns/90ns for normal Vcc range (2.7V ~ 3.6V)
- **Program and erase time**
  - Program time : 6us/byte, 8us/word (typical)
  - Accelerated program time : 4us/word (typical)
  - Sector erase time : 0.7sec/sector (typical)
- **Power consumption (typical values)**
  - 15uA in standby or automatic sleep mode
  - 10mA active read current at 5MHz
  - 15mA active write current during program or erase
- **Minimum 100,000 program/erase cycles per sector**
- **20 Year data retention at 125^{O}C**

SOFTWARE FEATURES

- **Erase Suspend / Erase Resume**
- **Data# poll and toggle for Program/erase status**
- **CFI (Common Flash Interface) supported**
- **Unlock Bypass Program**
- **Autoselect mode**
- **Auto-sleep mode after t_{ACC} + 30ns**

HARDWARE FEATURES

- **Hardware reset input pin (RESET#)**
  - Provides a hardware reset to device
  - Any internal device operation is terminated and the device returns to read mode by the reset
- **Ready/Busy# output pin (RY/BY#)**
  - Provides a program or erase operational status about whether it is finished for read or still being progressed
- **WP#/ACC input pin**
  - Two outermost boot sectors are protected when WP# is set to low, regardless of sector protection
  - Program speed is accelerated by raising WP#/ACC to a high voltage (11.5V~12.5V)
- **Sector protection / unprotection (RESET# , A9)**
  - Hardware method of locking a sector to prevent any program or erase operation within that sector
  - Two methods are provided :
    - In-system method by RESET# pin
    - A9 high-voltage method for PROM programmers
- **Temporary Sector Unprotection (RESET#)**
  - Allows temporary unprotection of previously protected sectors to change data in-system

ES29LV320E

GENERAL PRODUCT DESCRIPTION

The ES29LV320 is a 32 megabit, 3.0 volt-only flash memory device, organized as 4M x 8 bits (Byte mode) or 2M x 16 bits (Word mode) which is configurable by BYTE#. Eight boot sectors and sixty three main sectors with uniform size are provided : 8Kbytes x 8 and 64Kbytes x 63. The device is manufactured with ESI's proprietary, high performance and highly reliable 0.18um CMOS flash technology. The device can be programmed or erased in-system with standard 3.0 Volt Vcc supply (2.7V~3.6V) and can also be programmed in standard EPROM programmers. The device offers minimum endurance of 100,000 program/erase cycles and more than 10 years of data retention.

The ES29LV320 offers access time as fast as 70ns or 90ns, allowing operation of high-speed microprocessors without wait states. Three separate control pins are provided to eliminate bus contention : chip enable (CE#), write enable (WE#) and output enable (OE#).

All program and erase operation are automatically and internally performed and controlled by embedded program/erase algorithms built in the device. The device automatically generates and times the necessary high-voltage pulses to be applied to the cells, performs the verification, and counts the number of sequences. Some status bits (DQ7, DQ6 and DQ5) read by data# polling or toggling between consecutive read cycles provide to the users the internal status of program/erase operation: whether it is successfully done or still being progressed.

Extra Security Sector of 256 bytes

In the device, an extra security sector of 256 bytes is provided to customers. This extra sector can be used for various purposes such as storing ESN (Electronic Serial Number) or customer's security codes. Once after the extra sector is written, it can be permanently locked by the device manufacturer (**factory-locked**) or a customer(**customer-lockble**). At the same time, a **lock indicator bit** (**DQ7**) is permanently set to a 1 if the part is factory- locked, or set to 0 if it is customer-lockable. Therefore, this lock indicator bit (DQ7) can be properly used to avoid that any customer-lockable part is used to replace a factory-locked part. The extra security sector is an extra memory space for customers when it is used as a customer-lockable version. So, it can be read and written like any other sectors. But it should be noted that the number of E/W(Erase and Write) cycles is limited to 300 times (maximum) only in the Security Sector.

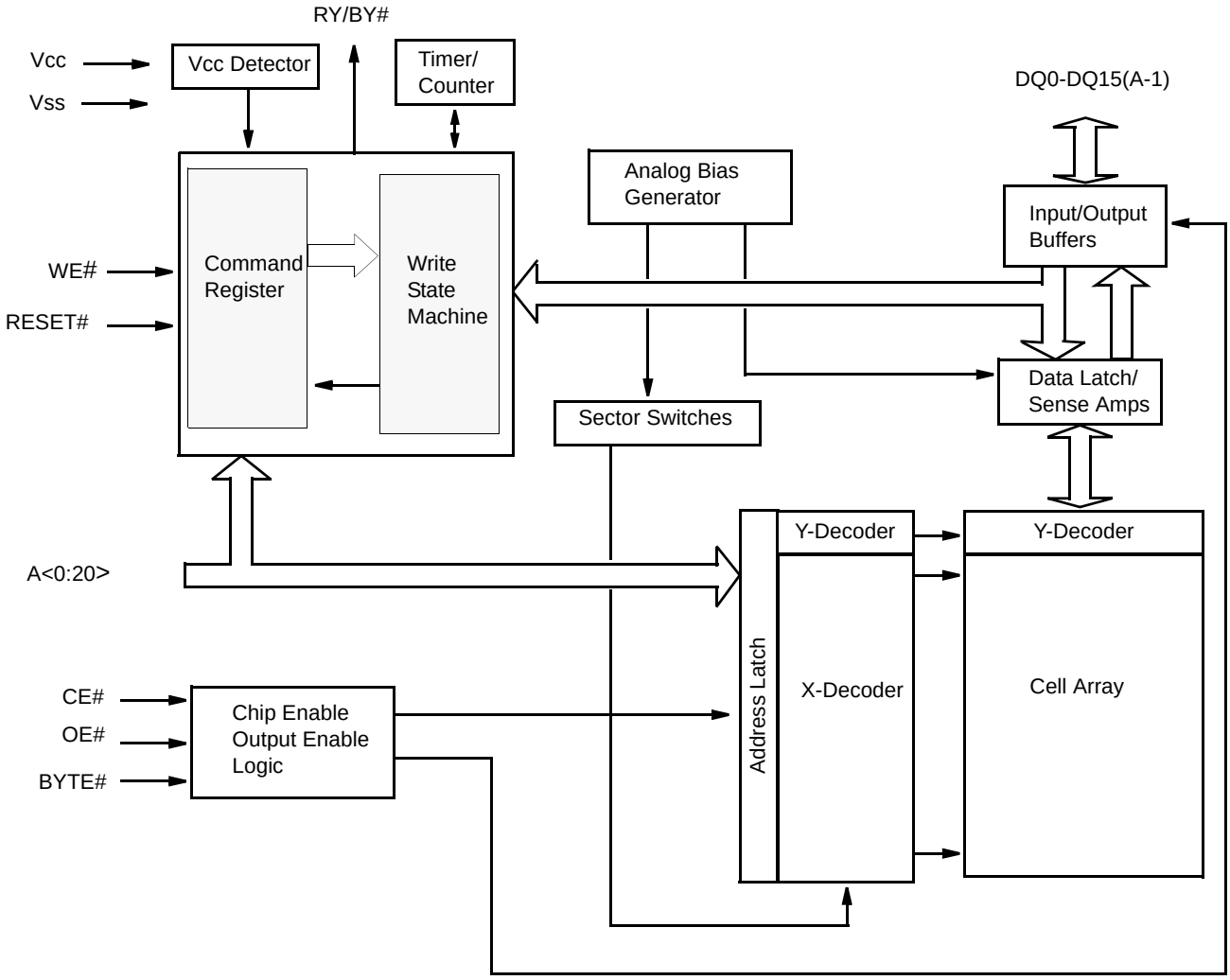
Special services such as ESN and factory-lock are available to customers (ESI's **Special-Code service**) The ES29LV320 is completely compatible with the JEDEC standard command set of single power supply Flash. Commands are written to the internal command register using standard write timings of microprocessor and data can be read out from the cell array in the device with the same way as used in other EPROM or flash devices.

PRODUCT SELECTOR GUIDE

Family Part Number	ES29LV320E	
Voltage Range	2.7V ~ 3.6 V	
Speed Option	**70**	**90**
Max Access Time (ns)	70	90
CE# Access (ns)	70	90
OE# Access (ns)	30	40

ES29LV320E

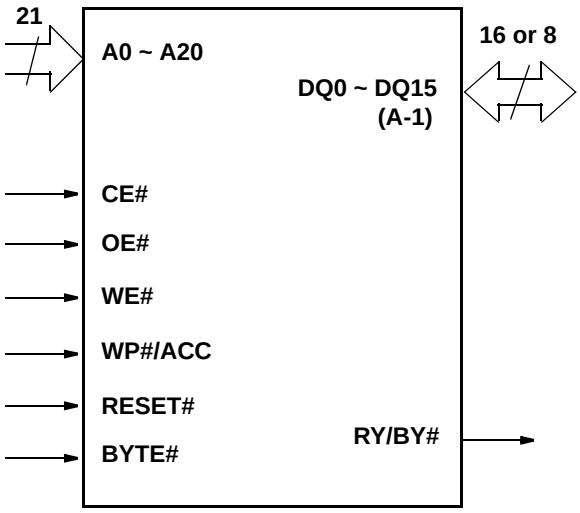
FUNCTION BLOCK DIAGRAM



PIN DESCRIPTION ES29LV320E

Pin	Description
A0-A20	21 Addresses
DQ0-DQ14	15 Data Inputs/Outputs
DQ15/A-1	DQ15 (Data Input/Output, Word Mode) A-1 (LSB Address Input, Byte Mode)
CE#	Chip Enable
OE#	Output Enable
WE#	Write Enable
WP#/ACC	Hardware Write Protect/Acceleration Pin
RESET#	Hardware Reset Pin, Active Low
BYTE#	Selects 8-bit or 16-bit mode
RY/BY#	Ready/Busy Output
Vcc	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
Vss	Device Ground
NC	Pin Not Connected Internally

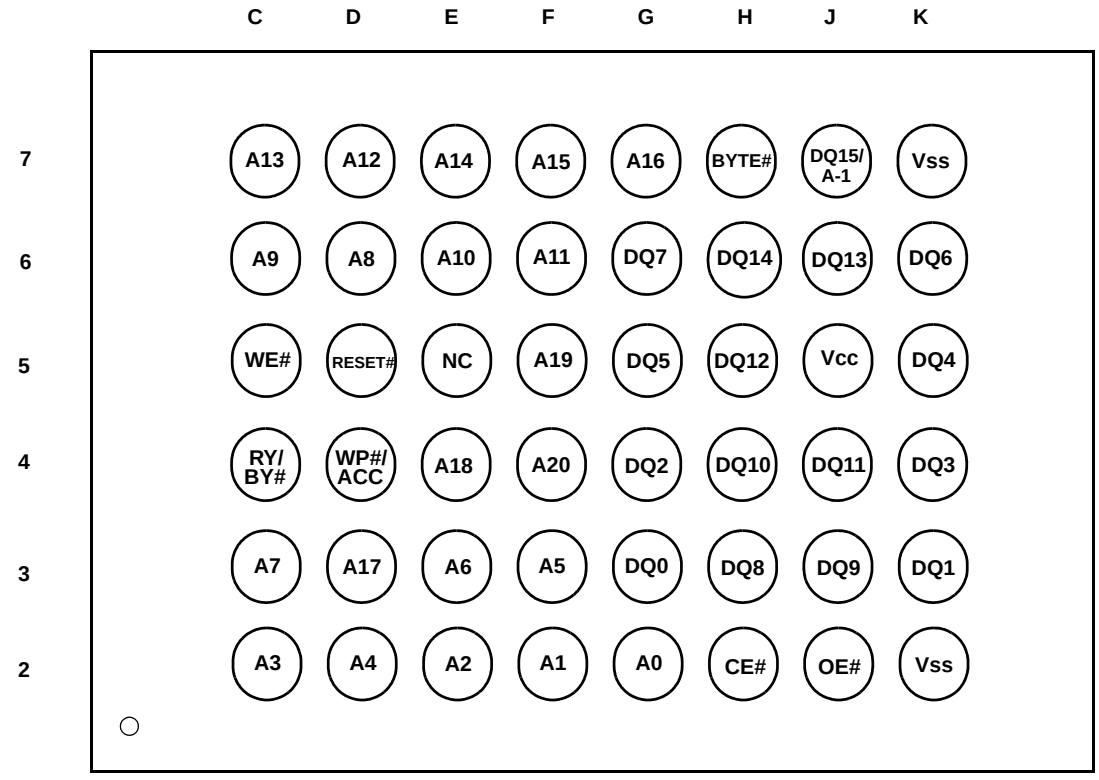
LOGIC SYMBOL



CONNECTION DIAGRAM

48-Ball FBGA 6 x 8 mm)

(Top View, Balls Facing Down)



32 Mbit (4M x 8/2M x 16) 3V Only CMOS Flash Memory

1. FEATURES

- Single supply voltage 2.7V-3.6V
- Fast access time: 70/90 ns
- 4,194,304x8 / 2,097,152x16 switchable by $\overline{BYTE}$ pin
  Compatible with JEDEC standard
  - Pin-out, packages and software commands compatible with single-power supply Flash
- Low power consumption
  - 20mA typical active current
  - 25uA typical standby current
- 100,000 program/erase cycles typically
- 20 Years Data Retention
- Command register architecture
  - Byte Word Programming (9 μs/11 μs typical)
  - Byte Mode : eight 8KB, sixty three 64KB sectors.
  - Word Mode : eight 4K word, sixty-three 32 K word sectors.
- Auto Erase (chip & sector) and Auto Program
  - Any combination of sectors can be erased concurrently; Chip erase also provided.
  - Automatically program and verify data at specified address
- Erase Suspend/Erase Resume
  - Suspend or Resume erasing sectors to allow the read/program in another sector
- Secured Silicon Sector
  - 128word sector for permanent, secure identification through an 8- word random Electronic Serial Number
  - May be programmed and locked at the factory or by the customer
  - Accessible through a command sequence.
- Ready/Busy (RY/$\overline{BY}$)
  - RY/$\overline{BY}$ output pin for detection of program or erase operation completion
- End of program or erase detection
  - Data polling
  - Toggle bits
- Hardware reset
  - Hardware pin ($\overline{RESET}$) resets the internal state machine to the read mode
- Sector Protection /Unprotection
  - Hardware Protect/Unprotect any combination of sectors from a program or erase operation.
- Low V_{CC} Write inhibit is equal to or less than 2.0V
- Boot Sector Architecture
  - U = Upper Boot Block
  - B = Bottom Boot Block
- Packages available:
  - 48-pin TSOPI
  - All Pb-free products are RoHS-Compliant
- CFI (Common Flash Interface) complaint
  - Provides device-specific information to the system, allowing host software to easily reconfigure to different Flash devices.

2. ORDERING INFORMATION

Part No	Boot	Speed	Package	Comments	Part No	Boot	Speed	Package	Comments
F49L320UA-70TG	Upper	70 ns	TSOPI	Pb-free	F49L320UA-90TG	Upper	90 ns	TSOPI	Pb-free
F49L320BA-70TG	Bottom	70 ns	TSOPI	Pb-free	F49L320BA-90TG	Bottom	90 ns	TSOPI	Pb-free

3. GENERAL DESCRIPTION

The F49L320UA/F49L320BA is a 32 Megabit, 3V only CMOS Flash memory device organized as 4M bytes of 8 bits or 2M words of 16bits. This device is packaged in standard 48-pin TSOP. It is designed to be programmed and erased both in system and can in standard EPROM programmers.

With access times of 70 ns and 90 ns, the F49L320UA/F49L320BA allows the operation of high-speed microprocessors. The device has separate chip enable $\overline{CE}$, write enable $\overline{WE}$, and output enable $\overline{OE}$ controls. ESMT's memory devices reliably store memory data even after 100,000 program and erase cycles.

The F49L320UA/F49L320BA is entirely pin and command set compatible with the JEDEC standard for 32 Megabit Flash memory devices. Commands are written to

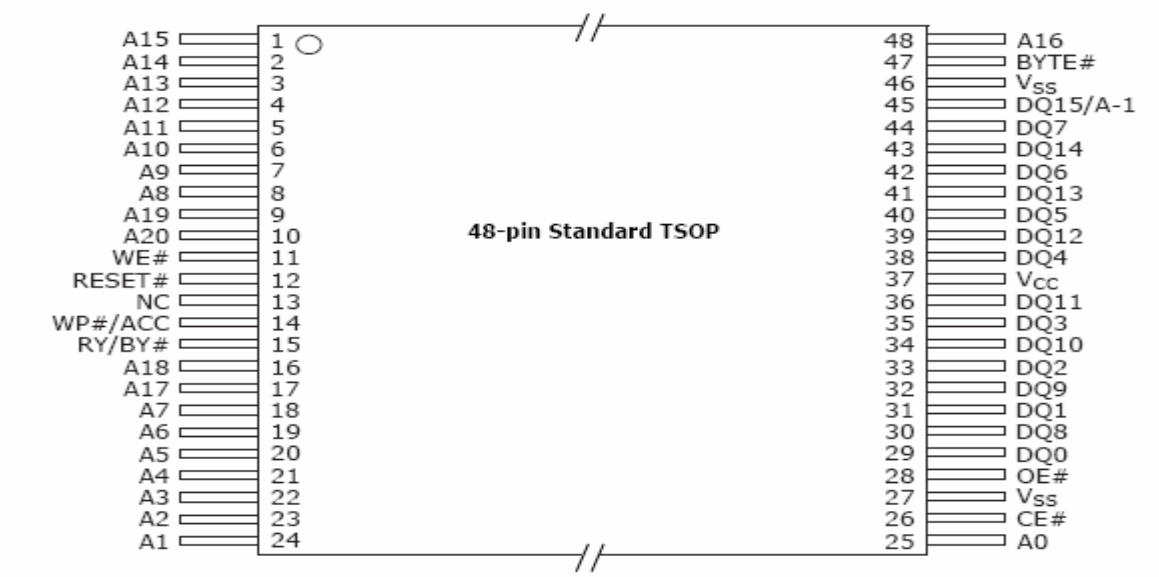
The F49L320UA/F49L320BA features a sector erase architecture. The device array is divided into eight 8KB, sixty-three 64KB for byte mode. The device memory array is divided into eight 4K word, sixty-three 32K word sectors for word mode. Sectors can be erased individually or in groups without affecting the data in other sectors. Multiple-sector erase and whole chip erase capabilities provide the flexibility to revise the data in the device.

The sector protect/unprotect feature disables both program and erase operations in any combination of the sectors of the memory. This can be achieved in-system or via programming equipment.

A low V_{CC} detector inhibits write operations on loss of power. End of program or erase is detected by the Ready/Busy status pin, Data Polling of DQ7, or by the Toggle Bit I feature on DQ6. Once the program or erase cycle has been successfully completed, the device internally resets to the Read mode. The command register using standard microprocessor write timings.

4. PIN CONFIGURATIONS

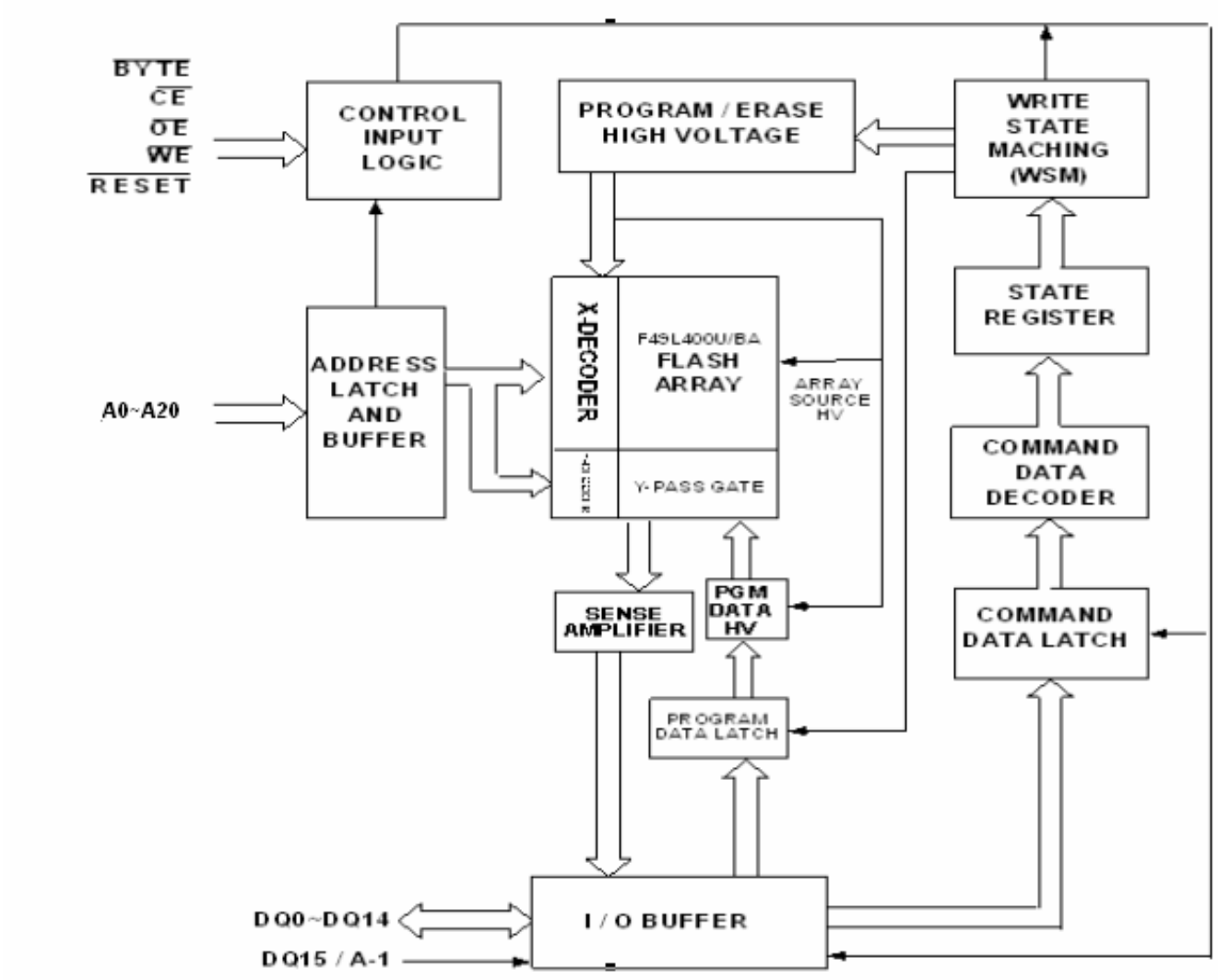
4.1 48-pin TSOP



4.2 Pin Description

Symbol	Pin Name	Functions
A0~A20	Address Input	To provide memory addresses.
DQ0~DQ14	Data Input/Output	To output data when Read and receive data when Write. The outputs are in tri-state when $\overline{OE}$ or $\overline{CE}$ is high.
DQ15/A-1	Q15 (Word mode) / LSB addr (Byte Mode)	To bi-direction date I/O when $\overline{BYTE}$ is High To input address when $\overline{BYTE}$ is Low
$\overline{CE}$	Chip Enable	To activate the device when $\overline{CE}$ is low.
$\overline{OE}$	Output Enable	To gate the data output buffers.
$\overline{WE}$	Write Enable	To control the Write operations.
$\overline{RESET}$	Reset	Hardware Reset Pin/Sector Protect Unprotect
$\overline{BYTE}$	Word/Byte selection input	To select word mode or byte mode
RY/$\overline{BY}$	Ready/Busy	To check device operation status
V_{CC}	Power Supply	To provide power
GND	Ground	
NC	No connection	

6. FUNCTIONAL BLOCK DIAGRAM



FLI30336

Single-chip enhanced LCD TV controller

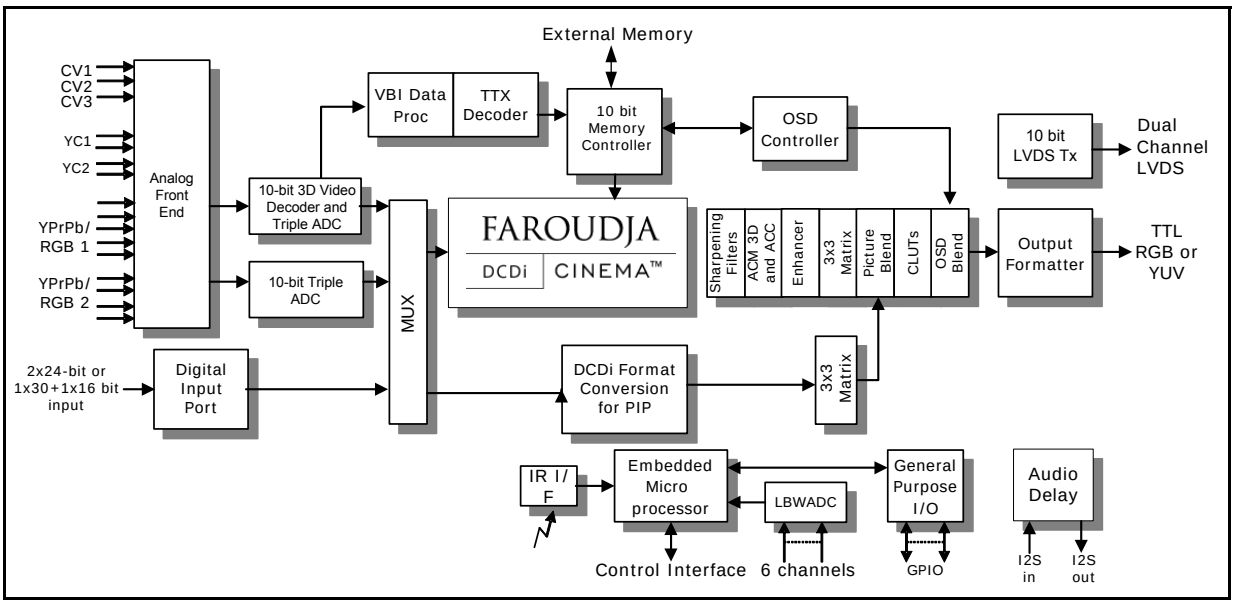
Data Brief

Features

- Integrated 3D video decoder
- Flexible digital capture up to 165 MHz and analog capture up to 162 MHz
- VBI signal processing including WST version 2.5 support
- Flexible DDR memory interface
- Faroudja® TrueLife™ video enhancer
- Advanced Picture-in-Picture (PIP) features
- Advanced Color Management (ACM-3D) and Adaptive Contrast Control (ACC)
- On-chip microprocessor
- Advanced bitmapped OSD controller
- LCD overdrive
- Embedded 10-bit dual-channel LVDS for 1080p and WUXGA panel support
- Package: 416 PBGA

Applications

- LCD and PDP TV
- DLP®, LCD, and LCOS front and rear projection



1 Description

The FLI30336 offers high integration for advanced applications of Picture-in-Picture (PIP) and Picture-by-Picture (PBP) with an integrated video decoder and a 3D comb filter. The FLI30336 can power up to 1080p/WUXGA displays with the proven Faroudja DCDi Cinema branded technology.

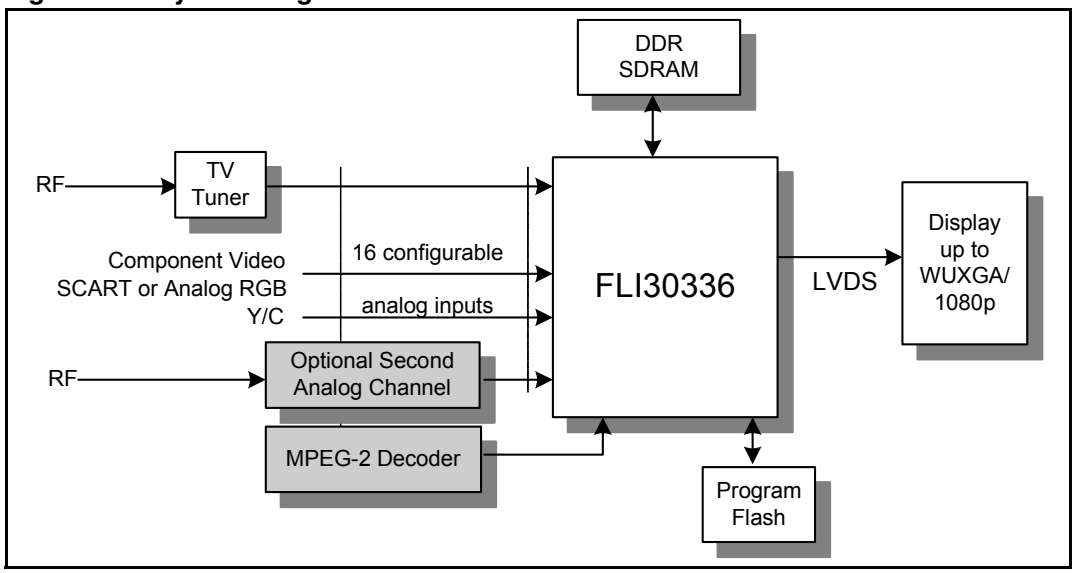
Special performance features such as the Faroudja DCDi Cinema video format converter, 10-bit performance in the device, and the Advanced Color Management (ACM-3D) provide exceptional video quality. This exclusive level of video quality technology only seen on Faroudja Home Theater Systems is now available in a single-chip solution.

The FLI30336 also comprises an integrated Analog Front-End (AFE) that includes triple ADCs and an integrated cross-point switch. The flexible AFE ensures simple PCB design with direct connections to TV tuners and input video connectors. In essence, the FLI30336 is the only device needed for a single LCD TV chassis supporting worldwide standards. For regional variations, only connector and firmware changes are required.

The integrated VBI dataslicer and decoder remove the need for external components resulting in significant cost reduction. The FLI30336 supports many worldwide VBI standards for applications of Teletext, Closed Captioning, V-Chip, and other VBI services.

The FLI30336 can be used in digital TV solutions requiring Faroudja DCDi Cinema video performance levels. An embedded microprocessor and a versatile OSD in a single device will facilitate rapid development of a reliable and attractive product. The FLI30336 utilizes the common Cortez family firmware for easy and effortless migration across different hardware platforms within this family.

Figure 1. System diagram



2 Feature attributes

- Flexible digital and analog capture
  - 16 configurable analog inputs
  - Direct connection from tuner or connector to analog input pin
  - Supports analog RGB/YUV capture up to 162 MHz and digital input capture up to 165 MHz
  - Full SCART support including RGB fast blank
  - 4:4:4/4:2:2/CCIR656/601 8/16/24/30-bit digital input port
  - Simple connection to JPEG and MPEG processors with a 8-bit bi-directional media port
- Integrated 3D video decoder
  - Faroudja IntelliComb™ technology
  - 3D adaptive comb filters for luma–chroma separation
  - Supports Composite, S-Video, and Component (including High Definition) video input signals
  - Supports all broadcast TV video standards—NTSC (North America and Japan), PAL (I, B, G, H, M, D, N), SECAM (D, K, L, B, G)
  - Supports playback video standards—NTSC443 and PAL-60
  - Macrovision™ and VCR trick mode support
- VBI signal processing
  - Multi-standard digital VBI dataslicer
  - WST FastText page support access with > 2048 page cache
  - Supports WST level 2.5
  - V-chip, VPS, Closed Captioning, XDS, CGMS, and WSS decoder
  - Supports VBI frame freeze
- Faroudja DCDI Cinema format conversion
  - Low angle de-interlacing processing
  - Per pixel Motion Adaptive De-interlacing (MADi) up to 1080i format
  - Format conversion up to WUXGA resolutions
  - Panoramic and anamorphic non-linear scaling
  - Adaptive media display processing for 3:2 and 2:2 video content
  - Special 2:2 and 3:3 film mode for improved film processing
  - Adaptive 3D/TNR noise reduction
  - Media noise reduction for MPEG inputs
- On-chip microprocessor
  - Integrated x186-based microprocessor with rich function library
  - General Purpose Inputs/Outputs (GPIOs) available for managing system devices (keypad, backlight, NVRAM, etc.)
  - Advanced power control for low power stand-by mode
  - 2-wire serial master bus interface for external device control

- Faroudja TrueLife video enhancer
  - High performance and programmable sharpening filters with noise coring
  - Programmable main channel horizontal and vertical filter coefficients
  - Non-linear chroma and luma enhancement
  - Removal of the DVD Chroma Upsampling Error (CUE) introduced by some DVD sources
- Advanced Color Management (ACM-3D)
  - ACM-3D allows flexible flesh-tone compensation, blue stretch, and other image enhancements
  - ACM-3D provides flexible programming, polar coordinate representation, and six-axis color control
  - ACC ensures full dynamic range is used in video content
- Picture-in-Picture (PIP)
  - Programmable PIP channel horizontal and vertical filter coefficients
  - Supports high performance programmable sharpening filters with noise coring
  - Video PIP over full screen graphics and video backgrounds
  - Supports graphics and video PIP (CVBS/S-Video/Component ED/HD) over full screen video background (CVBS/S-Video)
  - Side-by-side window support
  - PIP zoom support
  - DCDi Edge® processing for second channel window
- Output formats
  - Dual-channel 8-bit wide TTL output
  - Dual-channel 10-bit LVDS transmitters for direct connection to LCD modules
  - 30-bit single-wide TTL output; 24-bit 4:2:2 YUV TTL output—12 bits per color 1080p panel support
  - 120 Hz WXGA panel support using FRC and Black Frame Insertion (BFI) technique
- Other features
  - Integrated infrared decoder
  - Integrated low bandwidth ADC with 6 input channels
  - 4 integrated PWM outputs for LCD backlight control
  - Integrated I2S audio delay to exact audio and video synchronization
  - I2S channel MUX to support two I2S input streams
  - Supports DDR1-500 memory devices and 512 Mb
  - Reduce LCD video smearing artifacts
  - Advanced bitmapped OSD controller

MK2302S-01

Multiplier and Zero Delay Buffer

Description

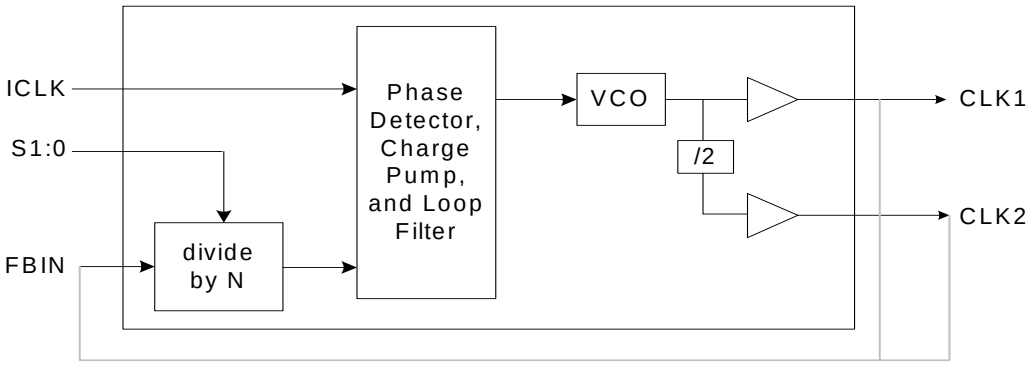
The MK2302S-01is a high performance Zero Delay Buffer (ZDB) which integrates ICS' proprietary analog/digital Phase Locked Loop (PLL) techniques. The chip is part of ICS' ClockBlocks™ family and was designed as a performance upgrade to meet today's higher speed and lower voltage requirements. The zero delay feature means that the rising edge of the input clock aligns with the rising edges of both output clocks, giving the appearance of no delay through the device. There are two outputs on the chip, one being a low-skew divide by two of the other output.

The MK2302S-01 is ideal for synchronizing outputs in a large variety of systems, from personal computers to data communications to graphics/video. By allowing off-chip feedback paths, the device can eliminate the delay through other devices.

Features

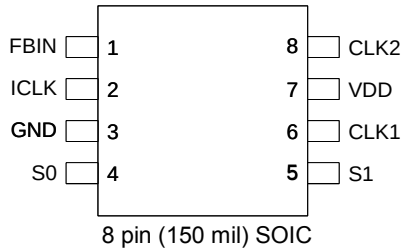
- 8 pin SOIC package
- Low input to output skew of 250ps max
- Absolute jitter ± 500ps
- Propagation Delay ± 350ps
- Ability to choose between different multipliers from 0.5X to 16X
- Output clock frequency up to 133 MHz at 3.3V
- Can recover degraded input clock duty cycle
- Output clock duty cycle of 45/55
- Full CMOS clock swings with 25mA drive capability at TTL levels
- Advanced, low power CMOS process
- Operating voltage of 3.3V or 5V
- Industrial temperature version available

Block Diagram



External feedback can come from CLK1 or CLK2 (see table on page 2)

Pin Assignment



8 pin (150 mil) SOIC

Clock Multiplier Decoding Table 1

(Multiplies Input clock by shown amount)

FBIN	S1	S0	CLK1	CLK2
CLK1	0	0	2 X ICLK	ICLK
CLK1	0	1	4 X ICLK	2 X ICLK
CLK1	1	0	ICLK	ICLK/2
CLK1	1	1	8 X ICLK	4 X ICLK
CLK2	0	0	4 X ICLK	2 X ICLK
CLK2	0	1	8 X ICLK	4 X ICLK
CLK2	1	0	2 X ICLK	ICLK
CLK2	1	1	16 X ICLK	8 XICLK

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	FBIN	Input	Feedback clock input.
2	ICLK	Input	Reference clock input.
3	GND	Power	Connect to ground.
4	S0	Input	Select 0 for output clock per decoding table above. Pull-up.
5	S1	Input	Select 1 for output clock per decoding table above. Pull up.
6	CLK1	Output	Clock output per table above.
7	VDD	Power	Connect to +3.3V or +5.0V.
8	CLK2	Output	Clock output per table above. Low skew divide by two of pin 6 clock.

ANALOG DEVICES

Multiformat Video Encoder
Six, 11-Bit, 297 MHz DACs
ADV7342/ADV7343

FEATURES

- 74.25 MHz 20-/30-bit high definition input support
  - Compliant with SMPTE 274M (1080i), 296M (720p), and 240M (1035i)
- 6, 11-bit, 297 MHz video DACs
  - 16× (216 MHz) DAC oversampling for SD
  - 8× (216 MHz) DAC oversampling for ED
  - 4× (297 MHz) DAC oversampling for HD
  - 37 mA maximum DAC output current
- NTSC M, PAL B/D/G/H/I/M/N, PAL 60 support
- NTSC and PAL square pixel operation (24.54 MHz/29.5 MHz)
- Multiformat video input support
  - 4:2:2 YCrCb (SD, ED, and HD)
  - 4:4:4 YCrCb (ED and HD)
  - 4:4:4 RGB (SD, ED, and HD)
- Multiformat video output support
  - Composite (CVBS) and S-Video (Y/C)
  - Component YPrPb (SD, ED, and HD)
  - Component RGB (SD, ED, and HD)
- Macrovision® Rev 7.1.L1 (SD) and Rev 1.2 (ED) compliant
- Simultaneous SD and ED/HD operation
- EIA/CEA-861B compliance support
- Programmable features
  - Luma and chroma filter responses
  - Vertical blanking interval (VBI)
  - Subcarrier frequency (F_{SC}) and phase
  - Luma delay
- Copy generation management system (CGMS)
- Closed captioning and wide screen signaling (WSS)
- Integrated subcarrier locking to external video source
- Complete on-chip video timing generator
- On-chip test pattern generation
- On-board voltage reference (optional external input)
- Serial MPU interface with dual I²C® and SPI® compatibility
- 3.3 V analog operation
- 1.8 V digital operation
- 3.3 V I/O operation
- Temperature range: −40°C to +85°C

APPLICATIONS

- DVD recorders and players
- High definition Blu-ray DVD players
- HD-DVD players

FUNCTIONAL BLOCK DIAGRAM

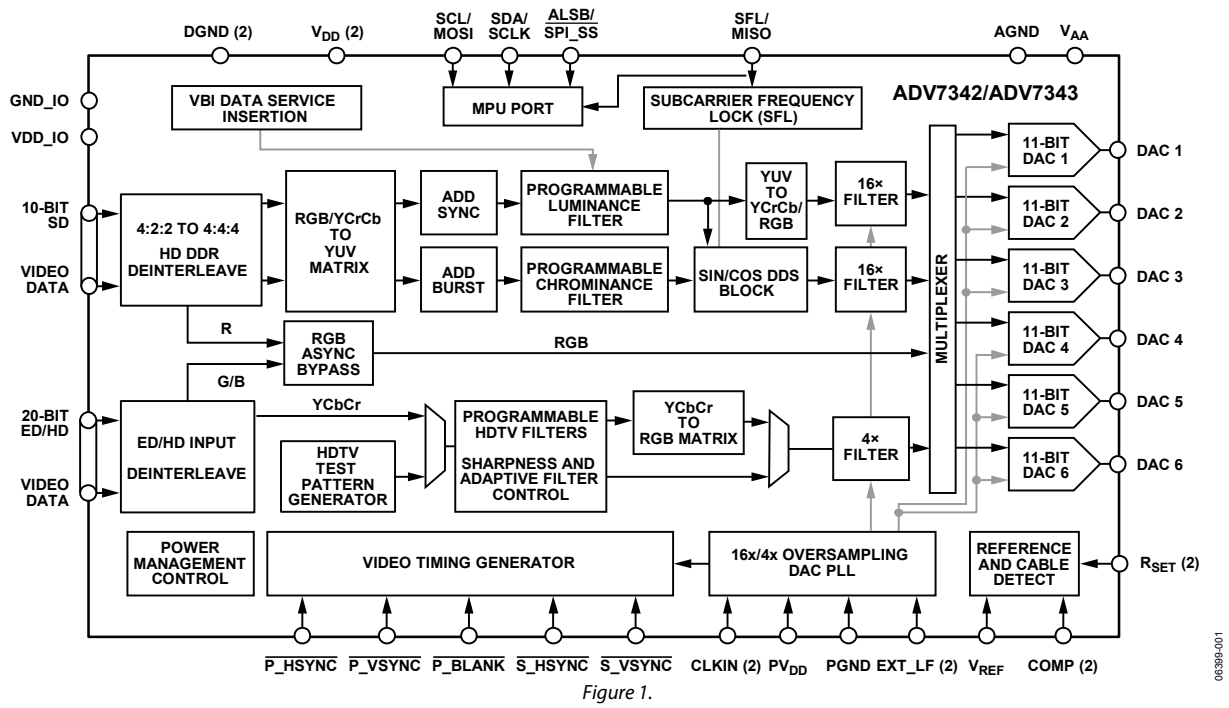


Figure 1.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

ADV7342/ADV7343

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

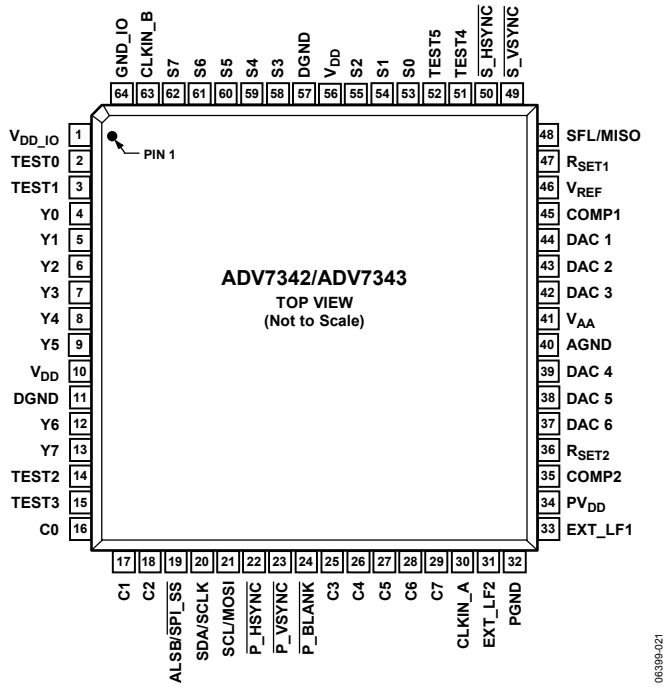


Figure 21. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output	Description
13, 12, 9 to 4	Y7 to Y0	I	8-Bit Pixel Port. Y0 is the LSB. Refer to Table 31 for input modes.
29 to 25, 18 to 16	C7 to C0	I	8-Bit Pixel Port. C0 is the LSB. Refer to Table 31 for input modes.
62 to 58, 55 to 53	S7 to S0	I	8-Bit Pixel Port. S0 is the LSB. Refer to Table 31 for input modes.
52, 51, 15, 14, 3, 2	TEST5 to TEST0	I	Unused. These pins should be connected to DGND.
30	CLKIN_A	I	Pixel Clock Input for HD Only (74.25 MHz), ED[1] Only (27 MHz or 54 MHz) or SD Only (27 MHz).
63	CLKIN_B	I	Pixel Clock Input for Dual Modes Only. Requires a 27 MHz reference clock for ED operation or a 74.25 MHz reference clock for HD operation.
50	$\overline{\text{S\_HSYNC}}$	I/O	SD Horizontal Synchronization Signal. This pin can also be configured to output an SD, ED, or HD horizontal synchronization signal. See the External Horizontal and Vertical Synchronization Control section.
49	$\overline{\text{S\_VSYNC}}$	I/O	SD Vertical Synchronization Signal. This pin can also be configured to output an SD, ED, or HD vertical synchronization signal. See the External Horizontal and Vertical Synchronization Control section.
22	$\overline{\text{P\_HSYNC}}$	I	ED/HD Horizontal Synchronization Signal. See the External Horizontal and Vertical Synchronization Control section.
23	$\overline{\text{P\_VSYNC}}$	I	ED/HD Vertical Synchronization Signal. See the External Horizontal and Vertical Synchronization Control section.
24	$\overline{\text{P\_BLANK}}$	I	ED/HD Blanking Signal. See the External Horizontal and Vertical Synchronization Control section.
48	SFL/MISO	I/O	Multifunctional Pin: Subcarrier Frequency Lock (SFL) Input/SPI Data Output. The SFL input is used to drive the color subcarrier DDS system, timing reset, or subcarrier reset.
47	R_{SET1}	I	This pin is used to control the amplitudes of the DAC 1, DAC 2, and DAC 3 outputs. For full-drive operation (for example, into a 37.5 Ω load), a 510 Ω resistor must be connected from R_{SET1} to AGND. For low drive operation (for example, into a 300 Ω load), a 4.12 kΩ resistor must be connected from R_{SET1} to AGND.

Pin No.	Mnemonic	Input/ Output	Description
36	R_{SET2}	I	This pin is used to control the amplitudes of the DAC 4, DAC 5, and DAC 6 outputs. A 4.12 kΩ resistor must be connected from R_{SET2} to AGND.
45, 35	COMP1, COMP2	O	Compensation Pins. Connect a 2.2 nF capacitor from both COMP pins to V_{AA}.
44, 43, 42	DAC 1, DAC 2, DAC 3	O	DAC Outputs. Full and low drive capable DACs.
39, 38, 37	DAC 4, DAC 5, DAC 6	O	DAC Outputs. Low drive only capable DACs.
21	SCL/MOSI	I	Multifunctional Pin: I²C Clock Input/SPI Data Input.
20	SDA/SCLK	I/O	Multifunctional Pin: I²C Data Input/Output. Also, SPI clock input.
19	ALSB/$\overline{\text{SPI\_SS}}$	I	Multifunctional Pin: This signal sets up the LSB[2] of the MPU I²C address. Also, SPI slave select.
46	V_{REF}		Optional External Voltage Reference Input for DACs or Voltage Reference Output.
41	V_{AA}	P	Analog Power Supply (3.3 V).
10, 56	V_{DD}	P	Digital Power Supply (1.8 V). For dual-supply configurations, V_{DD} can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering.
1	V_{DD_IO}	P	Input/Output Digital Power Supply (3.3 V).
34	PV_{DD}	P	PLL Power Supply (1.8 V). For dual-supply configurations, PV_{DD} can be connected to other 1.8 V supplies through a ferrite bead or suitable filtering.
33	EXT_LF1	I	External Loop Filter for On-Chip PLL 1.
31	EXT_LF2	I	External Loop Filter for On-Chip PLL 2.
32	PGND	G	PLL Ground Pin.
40	AGND	G	Analog Ground Pin.
11, 57	DGND	G	Digital Ground Pin.
64	GND_IO	G	Input/Output Supply Ground Pin.

[1] ED = enhanced definition = 525p and 625p.
[2] LSB = least significant bit. In the ADV7342, setting the LSB to 0 sets the I²C address to 0xD4. Setting it to 1 sets the I²C address to 0xD6. In the ADV7343, setting the LSB to 0 sets the I²C address to 0x54. Setting it to 1 sets the I²C address to 0x56.

TOSHIBA TC74VHC14F/FN/FT/FK

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC14F,TC74VHC14FN,TC74VHC14FT,TC74VHC14FK

Hex Schmitt Inverter

The TC74VHC14 is an advanced high speed CMOS SCHMITT INVERTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74VHC04 but the inputs have hysteresis and with its schmitt trigger function, the TC74VHC14 can be used as a line receivers which will receive slow input signals.

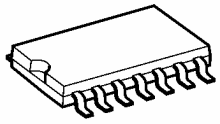
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

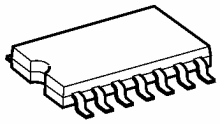
- High speed: t_{pd} = 5.5 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 2 μA (max) at Ta = 25°C
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2 V to 5.5 V
- Low noise: V_{OLP} = 0.8 V (max)
- Pin and function compatible with 74ALS14

Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74VHC14F

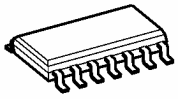


SOP14-P-300-1.27A



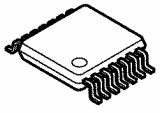
SOP14-P-300-1.27

TC74VHC14FN



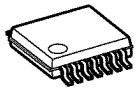
SOL14-P-150-1.27

TC74VHC14FT



TSSOP14-P-0044-0.65A

TC74VHC14FK

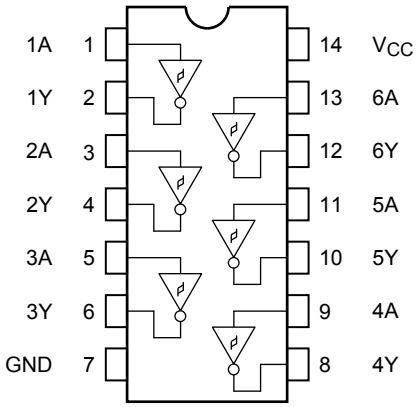


VSSOP14-P-0030-0.50

Weight

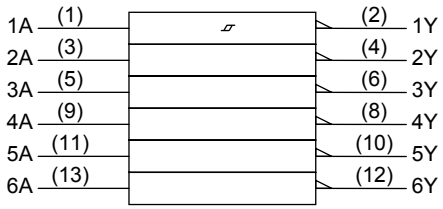
SOP14-P-300-1.27A	: 0.18 g (typ.)
SOP14-P-300-1.27	: 0.18 g (typ.)
SOL14-P-150-1.27	: 0.12 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)
VSSOP14-P-0030-0.50	: 0.02 g (typ.)

Pin Assignment



(top view)

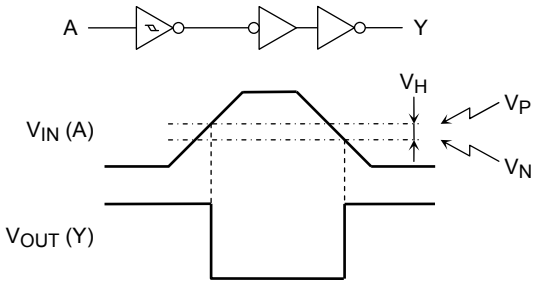
IEC Logic Symbol



Truth Table

A	Y
L	H
H	L

System Diagram, Waveform



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

SIL 9185

Sil 9185 Three Input, Single Output Deep Color HDMI Switch
Data Sheet

Silicon Image, Inc.

General Description

The Sil 9185 is the first generation of TMDS Switch devices supporting Revision 1.3 of the HDMI Specification (HDMI Consortium; June 2006). With three HDMI inputs and a single output, the Sil 9185 provides a low cost method of adding additional HDMI ports to the latest Digital TV's. New DTV's can easily connect to the many HDMI sources coming on the market including DVD's, STB, Game Consoles, PCs, Camcorders and Digital Still Cameras. The Sil 9185 is a fully HDMI compliant device providing a simple, low cost method of retransmitting protected digital audio and video, giving end users a truly all-digital experience. Built in backward compatibility with DVI 1.0 allows HDMI systems to connect to any DVI 1.0 source.

The Sil 9185 provides additional integrated features to help lower system cost and provide enhance features to the end consumer. To lower system cost, the Sil 9185 provides a complete solution for switching HDMI signals. This includes DDC switching, individual HPD control and 5V sense. The addition of these features eliminates additional external components helping to lower cost.

The Sil 9185 is the first generation of devices from Silicon Image to integrate the Extended Display Identification Data (EDID). The EDID is stored in on-board RAM that is downloaded from the system microcontroller during power up or initialization. The EDID is reflected on each of the three HDMI ports thru the DDC bus. Flexibility is built in to allow mixing different EDID formats in an application. This allows elimination of up to three EDID ROMs while also saving board space.

Finally, the Sil 9185 provides a complete, simple, solution to enabling Consumer Electronics Control (CEC) in a DTV. CEC is a single wire bus that transmits remote control commands throughout a home network. The Sil 9185 integrates both an HDMI compliant I/O and Silicon Image's CEC API. The CEC I/O meets all HDMI compliance tests and eliminates the need for additional external components, again saving board space. The CEC API manages reception and transmission of all CEC signals according to the CEC protocol and makes the information available to the system microcontroller. This significantly lowers the system level control by the system microcontroller, simplifying firmware overhead.

A very low power standby mode is available, allowing DTVs to meet industry low power requirements such as Energy Star. During this mode both the CEC and EDID are still functional.

Silicon Image's Sil 9185 uses the latest generation of TMDS core technology. These TMDS cores are guaranteed to pass all HDMI compliance tests.

Sil 9185 Pin Mapping

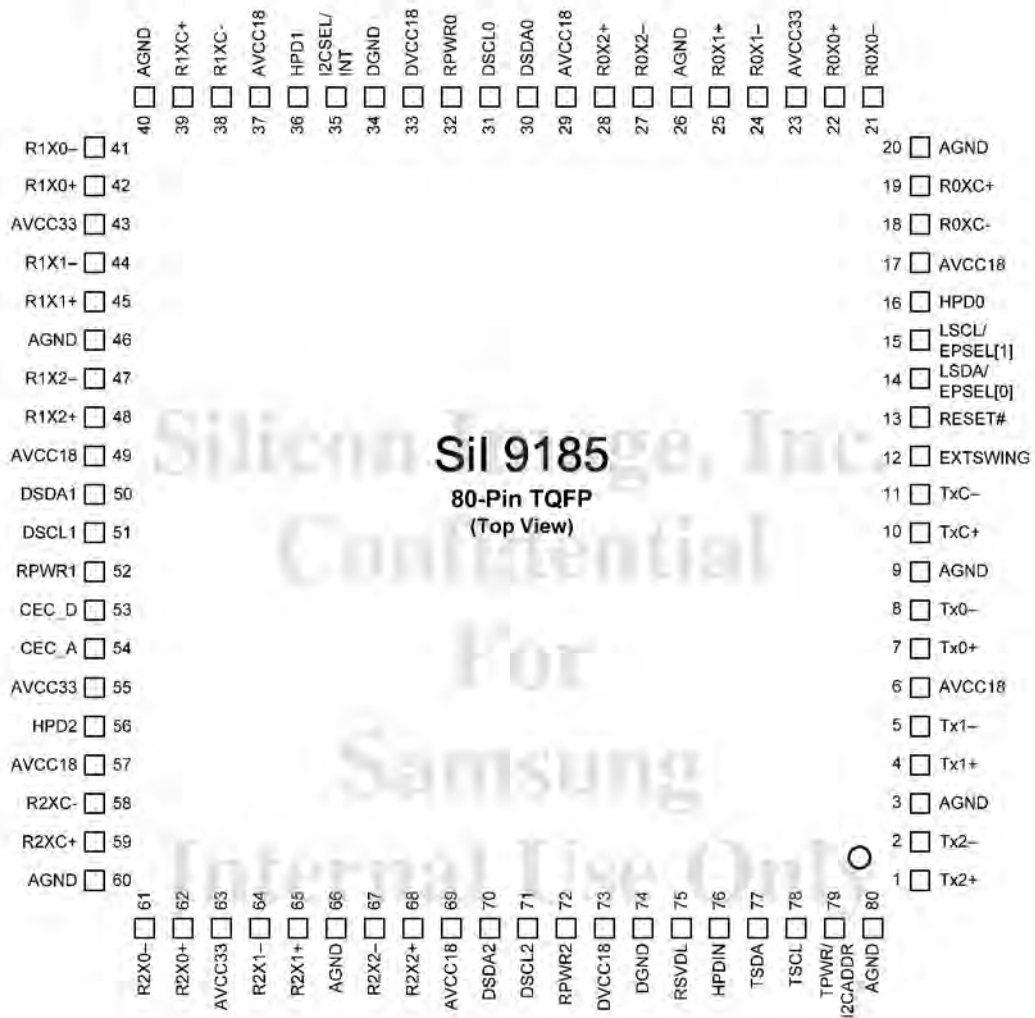


Figure 1. Pin Mapping

Functional Description

The SiI 9185 provides a low cost method of providing additional HDMI inputs to a DTV. System cost is reduced by integrating DDC and HPD switching along with integrated EDID. Feature enhancements like the embedded CEC API provide a simple method of adding CEC to a DTV without burdening the system microcontroller.

Figure 2 shows the functional blocks of the device. Pin descriptions begin on page 27.

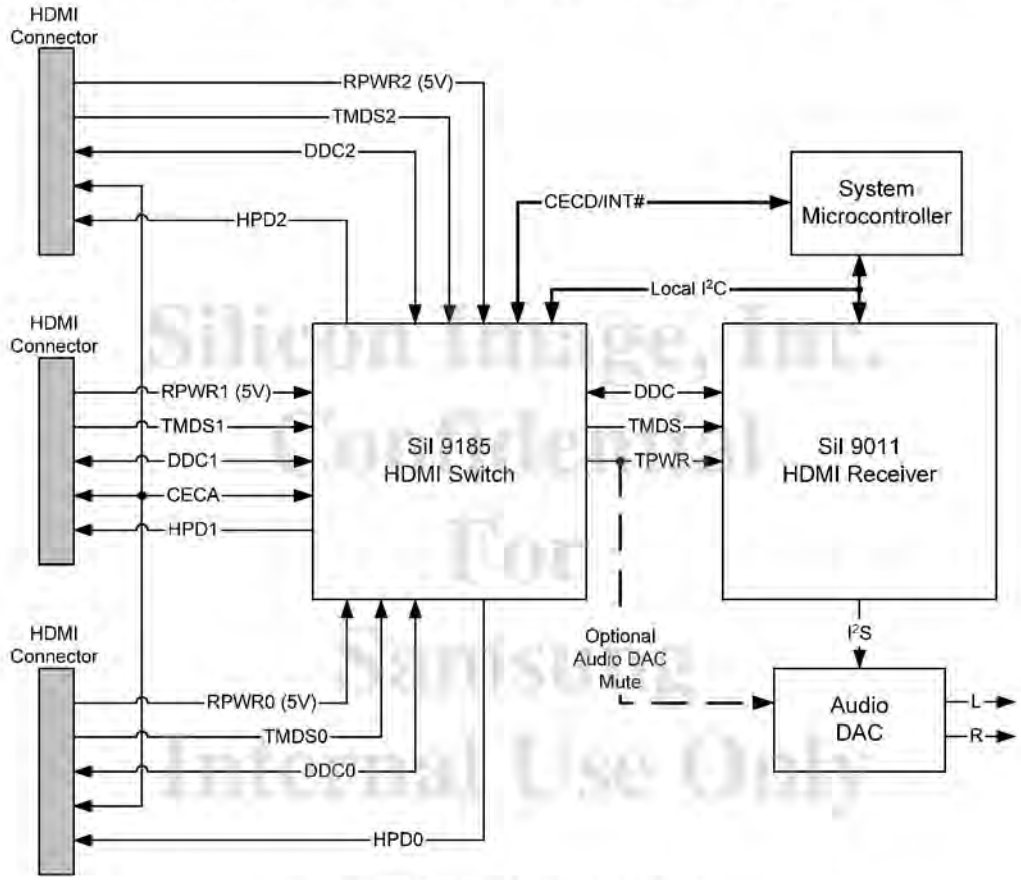


Figure 2. System Architecture

Block Level Functionality

The SiI 9185 Three Input, Single Output Deep Color HDMI Switch is used to select a single set of HDMI/DVI signals from one of three HDMI/DVI receiver-ports, and to generate a fully compliant HDMI/DVI stream as an output. It also provides DDC/HDCP, HPD, and +5V switching to allow full compliance to the HDMI/DVI Specification.

The combination of programmable equalizer and state-of-the-art DPLL can overcome signal distortion due to the long lengths of HDMI/DVI cables. SiI 9185-based switches can be cascaded many times to regenerate TMDS and HDCP signals.

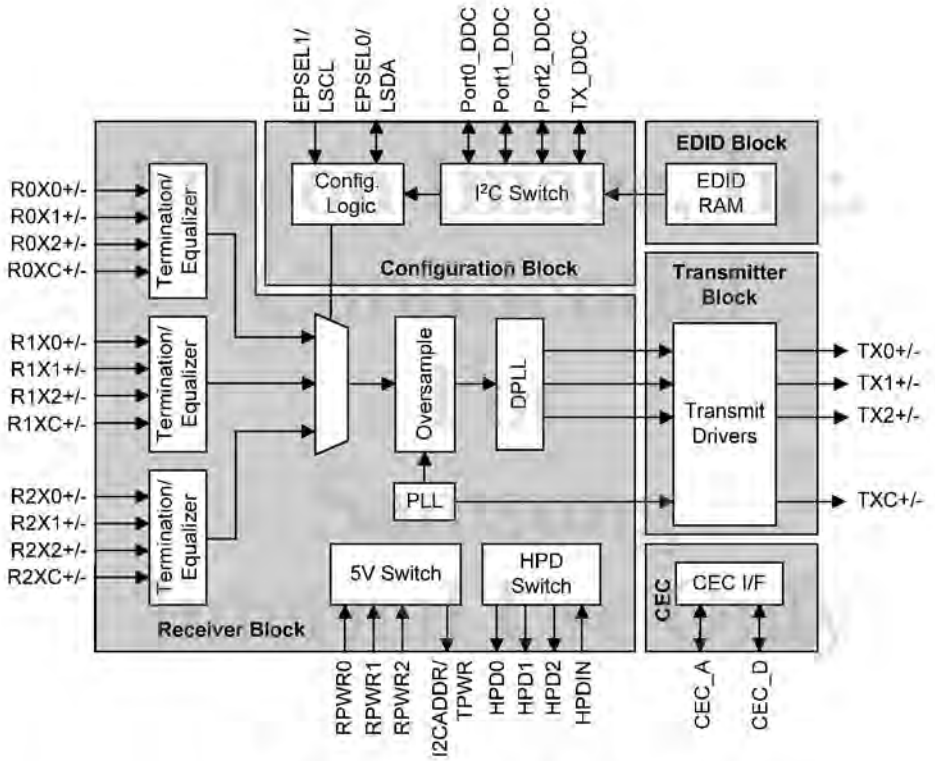


Figure 3. Functional Block Diagram

As shown in Figure 3, the SiI 9185 consists of five major blocks:

- Receiver block
- Transmitter block
- CEC Interface block
- EDID RAM block
- Configuration Block

Pin Descriptions

System Switching Pins

Pin Name	Pin #	Type	Dir	Description
DSDA0, DSDA1, DSDA2	30, 50, 70	LVTTL, Schmitt Trigger, 5V tolerant	Input/ Output	DDC I^2C Data for respective port. Note 1.
DSCL0, DSCL1, DSCL2	31, 51, 71	LVTTL, Schmitt Trigger, 5V tolerant	Input	DDC I^2C Clock for respective port. Note 1.
RPWR0, RPWR1, RPWR2	32, 52, 72	LVTTL, 5V Tolerant	Input	5V Port detection input for respective port. Connect to 5V signal from HDMI input connector.
HPD0, HDP1, HPD2	16, 36, 56	LVTTL, 2mA, 5V Tolerant	Output	Hot Plug Detect Output for respective port. Connect to HOTPLUG of HDMI input connector.
HPDIN	76	LVTTL, 5V Tolerant	Input	Hot Plug Detect Input.
TSCL	78	LVTTL, Schmitt Trigger. Open Drain 5V tolerant	Output	Master DDC I^2C Clock (Open Drain Output) to HDMI receiver. I^2C transactions required for HDCP operation are performed over this I^2C bus. Note 1.
TSDA	77	LVTTL, Schmitt Trigger, 5V tolerant	Input/ Output	Master DDC Data (Open drain output.) to HDMI receiver. I^2C transactions required for HDCP operation are performed over this I^2C bus. Note 1.

Note:

1. These signals are true open drain, and do not pull to ground when power is not applied to the device. These signals require an external pull-up.

Configuration Pins

Pin Name	Pin #	Type	Dir	Description
I2CADDR/ TPWR	79	LVTTL, 4mA, 5V Tolerant	Input/ Output	I^2C Slave Address input / Transmit Power Sense output pin. When RESET# is low, this pin is used as an input to latch the I^2C sub-address. The level on this pin is latched when the RESET# pin transitions from low to high. When RESET# is high, this pin is used as the TPWR output, indicating that the selected Rx-port is has 5V present. When none of the Rx ports are selected, this signal is low. See page 15 for more information.
I2CSEL/INT#	35	Schmitt Trigger, Open Drain, 4mA, 5V Tolerant	Input/ Output	I^2C Selection input / Interrupt output pin. When RESET# is low, this pin is used as an input to latch the External Port Detection signal. The level on this pin is latched when the RESET# pin transitions from low to high. When this pin is high during reset, the external pins EPSEL1/LSCL and EPSEL0/LSDA are used to select the Rx-port as EPSEL[1:0]. When this pin is low during reset, the internal local I^2C register is used to select the Rx-port. After reset, this pin becomes the Interrupt output. This is an open-drain output and requires an external pull-up. See page 14 for more information.
RSVDL	75		Input	Reserved for use by Silicon Image and must be tied low.

Control Pins

Pin Name	Pin #	Type	Dir	Description
RESET#	13	LVTTL, Schmitt Trigger. 5V tolerant	Input	Reset Pin (Active LOW). Certain configuration inputs are latched when RESET# transitions from low to high. See page 14 for more information.
LSCL/EPSEL1	15	Schmitt 5V tolerant	Input	Local I^2C Clock / External Port Select 1. When I2CSEL is high, this becomes the Local I^2C bus clock pin, LSCL. When I2CSEL is low, this becomes the external port select pin, EPSEL1. True open drain, so does not pull to ground if power not applied. An external pull-up is required. See page 14 for more information.
LSDA/EPSEL0	14	LVTTL, Schmitt Trigger. Open Drain 5V tolerant	Input/ Output	Local I^2C Data / External Port Select 0. When I2CSEL is high, this becomes the Local I^2C bus data pin, LSDA. When I2CSEL is low, this becomes the external port select pin, EPSEL0. True open drain, so does not pull to ground if power not applied. An external pull-up is required. See page 14 for more information.

CEC Pins

Pin Name	Pin #	Type	Direction	Description
CEC_A	54	CEC Compliant, 5V tolerant.	Input/ Output	HDMI compliant CEC I/O used to interface to CEC devices. CEC electrically compliant signal. This pin connects to the CEC signal of all HDMI connectors in the system. As an input, the pad acts as a LVTTL Schmitt triggered input and is 5V tolerant. As an output, the pad acts as an NMOS driver with resistive pull-up. This pin has an internal pull-up resistor.
CEC_D	53	LVTTL, Schmitt Trigger 5V tolerant.	Input/ Output	CEC interface to local system. True open-drain. An external pull-up is required. This pin typically connects to the local CPU.

Differential Signal Data Pins

Pin Name	Pin #	Type	Dir	Description
R0X0+	22	TMDS	Input	TMDS input Port 0 data pairs.
R0X0-	21	TMDS	Input	
R0X1+	25	TMDS	Input	
R0X1-	24	TMDS	Input	
R0X2+	28	TMDS	Input	
R0X2-	27	TMDS	Input	
R0C+	19	TMDS	Input	TMDS input Port 0 clock pair.
R0C-	18	TMDS	Input	
R1X0+	42	TMDS	Input	TMDS input port 1 data pairs.
R1X0-	41	TMDS	Input	
R1X1+	45	TMDS	Input	
R1X1-	44	TMDS	Input	
R1X2+	48	TMDS	Input	
R1X2-	47	TMDS	Input	
R1C+	39	TMDS	Input	TMDS input Port 1 clock pair.
R1C-	38	TMDS	Input	
R2X0+	62	TMDS	Input	TMDS input port 2 data pairs.
R2X0-	61	TMDS	Input	
R2X1+	65	TMDS	Input	
R2X1-	64	TMDS	Input	
R2X2+	68	TMDS	Input	
R2X2-	67	TMDS	Input	
R2C+	59	TMDS	Input	TMDS input Port 2 clock pair.
R2C-	58	TMDS	Input	
TX0+	7	TMDS	Output	TMDS output data pairs.
TX0-	8	TMDS	Output	
TX1+	4	TMDS	Output	
TX1-	5	TMDS	Output	
TX2+	1	TMDS	Output	
TX2-	2	TMDS	Output	
TXC+	10	TMDS	Output	TMDS output clock pair.
TXC-	11	TMDS	Output	
EXT_SWING	12	Analog	Input	Voltage Swing Adjust. A resistor tied from this pin to AVCC18 determines the amplitude of the voltage swing. The recommended value is 500Ω.

Power and Ground Pins

Pin Name	Pin #	Type	Description
AVCC33	23, 43, 55, 63	Power	Analog VCC. Connect to 3.3V supply.
AVCC18	6, 17, 29, 37, 49, 57, 69	Power	Analog VCC. Connect to 1.8V supply.
AGND	3, 9, 20, 26, 40, 46, 60, 66, 80	Ground	Analog GND.
DVCC18	33, 73	Power	Digital VCC. Connect to 1.8V supply.
DGND	34, 74	Ground	Digital GND.

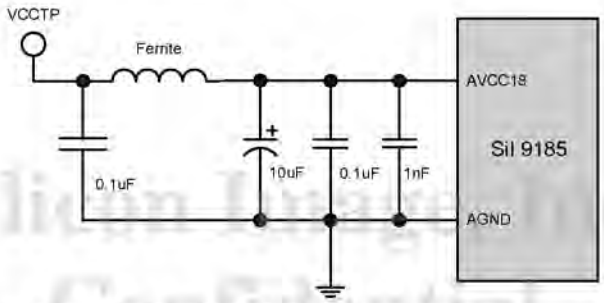


Figure 12. Test Point VCCTP for VCC Noise Tolerance Spec

General Description

The SiI 9135 is the second generation HDMI v1.3 Receiver that is compatible with the SiI9133 but adds audio support for DTS-HD and Dolby TrueHD. Digital televisions that can display 10/12-bit color depth can now provide the highest quality protected digital audio/video over a single cable. The SiI 9135 can receive deep color video up thru 12-bit, 1080p. Backward compatibility with DVI 1.0 allows HDMI systems to connect to existing DVI 1.0 hosts (such as HD set-top boxes and PCs).

The SiI 9135 is capable of receiving and outputting up to eight channels of uncompressed digital audio at 192 kHz and 2-channel digital audio up to 192 kHz. Compressed streams are also supported thru either the S/PDIF port or over I^2S for DTS-HD and Dolby TrueHD. An industry-standard I^2S port allows direct connection to low-cost audio DACs at up to 192 kHz. An S/PDIF port supports up to 192 kHz audio. The SiI 9135 supports SACD (Super Audio Compact Disc) and provides DSD (Direct Stream Digital) ports that support 44.1 and 88.2 kHz one-bit audio.

The SiI 9135 also comes pre-programmed with HDCP keys. This simplifies the manufacturing process and lowers costs, while providing the highest level of HDCP key security.

Silicon Image's HDMI Receivers use the latest generation of TMDS core technology. These TMDS cores pass all HDMI compliancy tests.

Features

- Dual-Input HDMI 1.3, HDCP 1.1, and DVI 1.0 compliant Receiver
- Integrated TMDS® core.
- Digital video interface supports video processors:
  - 36-bit RGB / YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
  - 12/15/18-bit DMO (Digital Multimedia Output) RGB/YCbCr 4:4:4 (clocked with rising & falling edges)
  - Color Space Conversion for both RGB-to-YCbCr and YCbCr-to-RGB (both 601 and 709)
    - True 12-bit accurate data using 14-bit processing
  - Auto video mode configuration simplifies system firmware design
- Digital audio interface supports high-end audio systems:
  - DTS-HD and Dolby TrueHD high bit rate audio support
  - 4 x I^2S inputs accept Dolby Digital, DVD-Audio input (2-channel 192 kHz, 8-channel 192 kHz)
  - S/PDIF input supports PCM, Dolby Digital, DTS digital audio transmission (32-192 kHz Fs sample rate)
  - IEC60958 or IEC61937 compatible
  - Flexible, programmable I^2S channel mapping
  - 2:1 and 4:1 down-sampling to handle 96 kHz and 192 kHz audio streams.
- Integrated HDCP decryption engine for receiving protected audio and video content:
  - Pre-programmed HDCP keys provide highest level of key security and simplify manufacturing
  - Full support for HDCP Repeaters (up to 16 attached downstream devices)
  - Built in HDCP BIST
- Software compatible with SiI 9033 and SiI 9133
  - Additional register programming required for deep color, DTS-HD, Dolby TrueHD support
- Flexible power management
- 20 mm x 20 mm 144-pin TQFP package with ePad

Pin Diagram

Figure 1 shows the pin connections for the Sil 9135 in the 144-pin TQFP package.

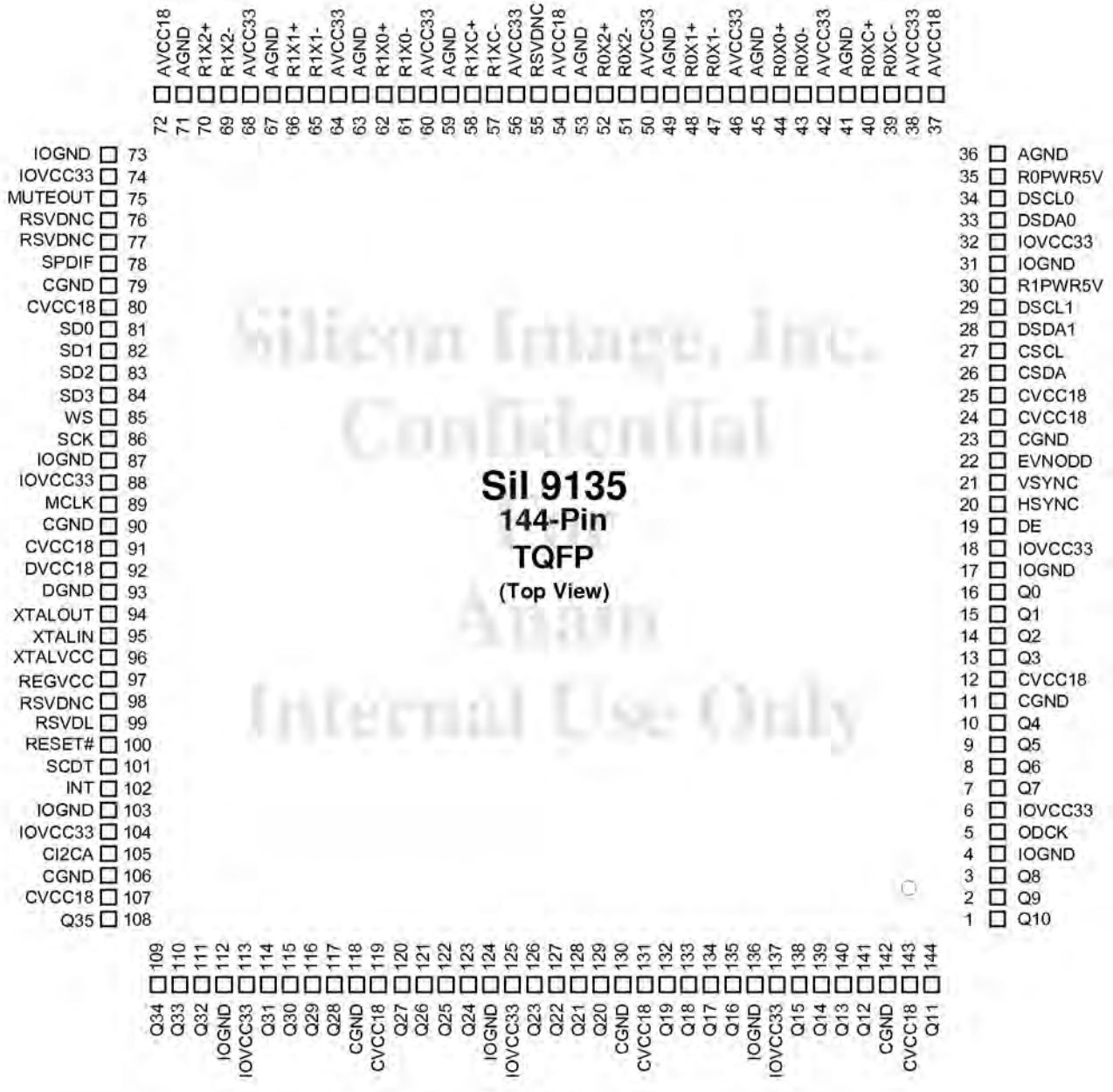


Figure 1. Pin Diagram

Individual pin functions are described beginning on page 41.

System Applications

The Sil 9135 is designed for AV Receivers that require support for HDMI v1.3 Deeper Color and the latest audio technologies; DTS-HD and Dolby TrueHD. The Sil 9135 supports the HDMI v1.3 specification and allows receipt of 10/12-bit color depth up to 1080p resolutions. A single Sil 9135 provides two HDMI input ports. The video output goes to a video processor or HDMI transmitter. Besides DTS-HD and Dolby TrueHD, the Sil 9135 supports full surround sound audio including DVD-Audio and SACD. The audio output can go directly to an audio DAC or an Audio DSP for further processing as shown in Figure 2.

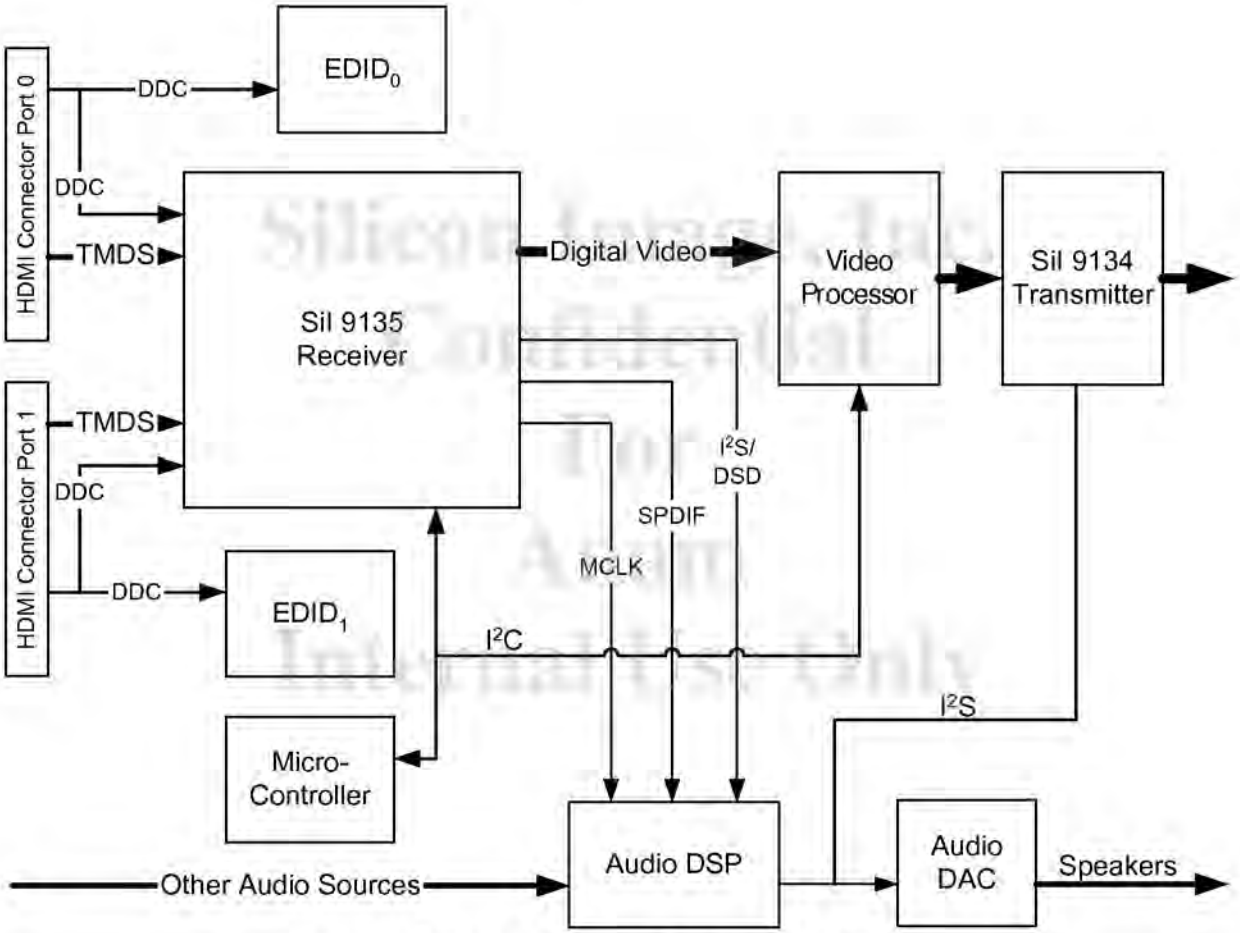


Figure 2. Digital Television Receiver Block Diagram

Functional Description

The SiI 9135 provides a complete solution for receiving HDMI-compliant digital audio and video. Specialized audio and video processing is available within the HDMI Receiver to add HDMI capability to consumer electronics such as AV Receivers. Figure 3 shows the functional blocks of the chip.

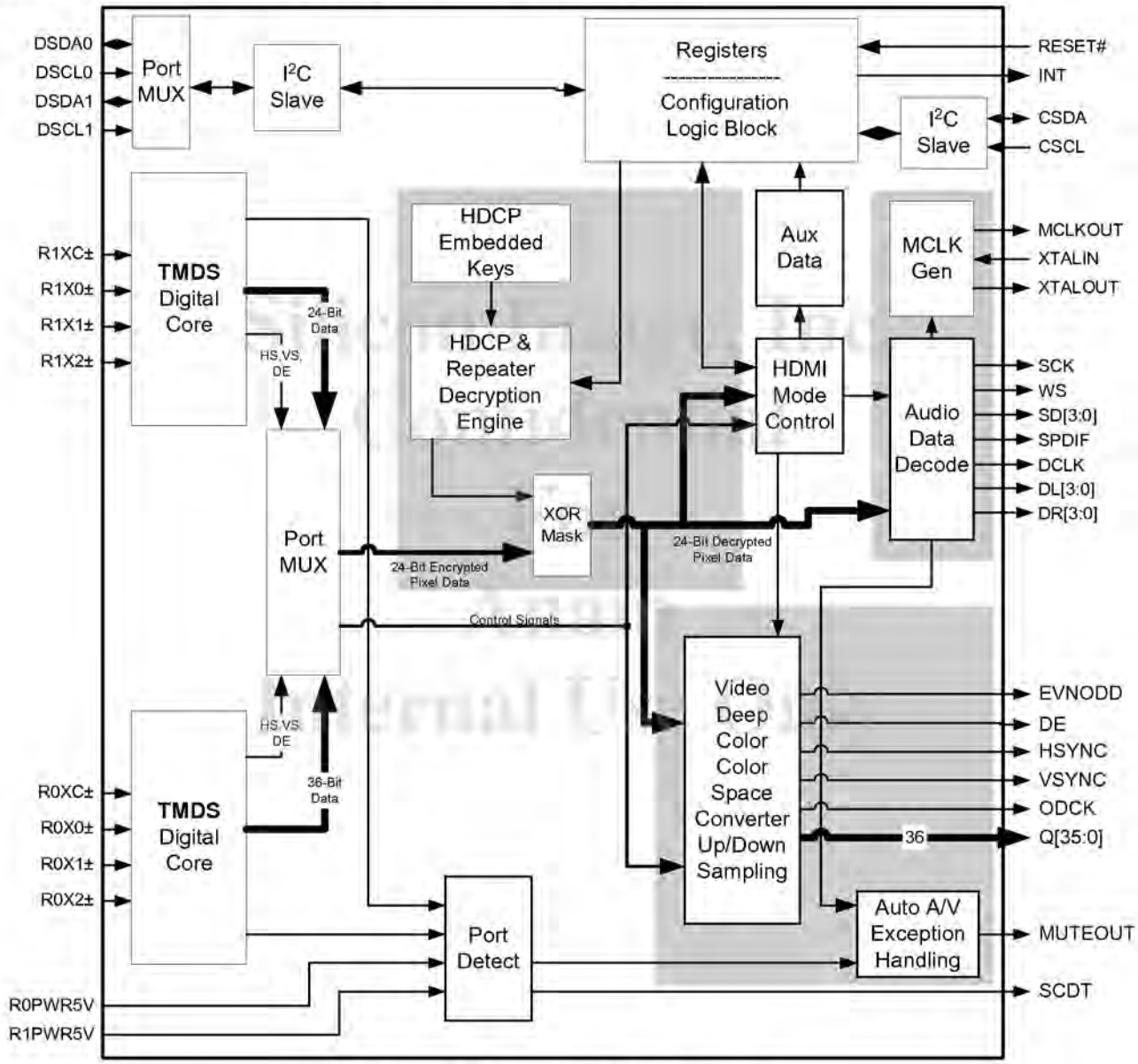


Figure 3. Functional Block Diagram

The SiI 9135 supports two HDMI input ports. Only one port can be active at any time.

144-Pin TQFP Pin Descriptions

Digital Video Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
Q0	16	8 mA	LVTTL	Output	36-Bit Output Pixel Data Bus. Q35:0 is highly configurable using the VDD_CONFIG register. It supports a wide array of output formats, including multiple RBG and YCbCr bus formats. Using the appropriate bits in the PD register, the output drivers can be put into a high impedance (tri-state) mode. A weak, internal pull-down device brings each output to ground.
Q1	15		LVTTL	Output	
Q2	14		LVTTL	Output	
Q3	13		LVTTL	Output	
Q4	10		LVTTL	Output	
Q5	9		LVTTL	Output	
Q6	8		LVTTL	Output	
Q7	7		LVTTL	Output	
Q8	3		LVTTL	Output	
Q9	2		LVTTL	Output	
Q10	1		LVTTL	Output	
Q11	144		LVTTL	Output	
Q12	141		LVTTL	Output	
Q13	140		LVTTL	Output	
Q14	139		LVTTL	Output	
Q15	138		LVTTL	Output	
Q16	135		LVTTL	Output	
Q17	134		LVTTL	Output	
Q18	133		LVTTL	Output	
Q19	132		LVTTL	Output	
Q20	129		LVTTL	Output	
Q21	128		LVTTL	Output	
Q22	127		LVTTL	Output	
Q23	126		LVTTL	Output	
Q24	123		LVTTL	Output	
Q25	122		LVTTL	Output	
Q26	121		LVTTL	Output	
Q27	120		LVTTL	Output	
Q28	117		LVTTL	Output	
Q29	116		LVTTL	Output	
Q30	115		LVTTL	Output	
Q31	114		LVTTL	Output	
Q32	111		LVTTL	Output	
Q33	110		LVTTL	Output	
Q34	109		LVTTL	Output	
Q35	108		LVTTL	Output	
DE	19	8 mA	LVTTL	Output	Data Enable.
HSYNC	20	8 mA	LVTTL	Output	Horizontal Sync Output
VSYNC	21	8 mA	LVTTL	Output	Vertical Sync Output
EVNODD	22	8 mA	LVTTL	Output	Indicates Even or Odd Field for Interlaced Formats.
ODCK	5	12 mA	LVTTL	Output	Output Data Clock.

Digital Audio Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
XTALIN	95	—	5V Tolerant LVTTL	In	Crystal Clock Input. Also allows LVTTL input. Frequency required: 26-28.5 MHz
XTALOUT	94	4 mA	LVTTL	Out	Crystal Clock Output
MCLK	89	8 mA	LVTTL	Out	Audio Master Clock Output
SCK/DCLK	86	4 mA	LVTTL	Out	I^2S Serial Clock Output.
					DSD Clock Out.
WS/DR0	85	4 mA	LVTTL	Out	I^2S Word Select Output.
					DSD Serial Right Ch0 Data Output
SD0/DL0	81	4 mA	LVTTL	Out	I^2S Serial Data Output / DSD Audio Output Configurable to be shared with DSD. SD0 = DSD Serial Left Ch0 Data Output SD1 = DSD Serial Right Ch1 Data Output SD2 = DSD Serial Left Ch1 Data Output SD3 = DSD Serial Right Ch2 Data Output
SD1/DR1	82	4 mA	LVTTL	Out	
SD2/DL1	83	4 mA	LVTTL	Out	
SD3/DR2	84	4 mA	LVTTL	Out	
SPDIF/DL2	78	4 mA	LVTTL	Out	S/PDIF Audio Output. Configurable to be shared with DSD
					DSD Serial Left Ch2 Data Output
MUTEOUT	75	4 mA	LVTTL	Out	Mute Audio Output. Signal to the external downstream audio device, audio DAC, etc. to mute audio output.

Note: The XTALIN pin can either be driven at LVTTL levels by a clock (leaving XTALOUT unconnected), or connected through a crystal to XTALOUT. Refer to the schematic on page 74.

Configuration/Programming Pins

Pin Name	Pin #	Strength	Type	Dir	Description
INT	102	4 mA	LVTTL	Out	Interrupt Output. Configurable polarity and push-pull output. Multiple sources of interrupt can be enabled through the INT_EN register. See Note.
RESET#	100	—	Schmitt	In	Reset Pin. Active LOW. 5V Tolerant
DSCL0	34	—	SchmittOD	In	DDC I^2C Clock for Port 0. 5V Tolerant. HDCP KSV, An and Ri values are exchanged over an I^2C port during authentication. True open drain, so does not pull to GND if power is not applied.
DSDA0	33	3 mA	SchmittOD	Bi-Di	DDC I^2C Data for Port 0. 5V Tolerant. HDCP KSV, An and Ri values are exchanged over an I^2C during authentication. True open drain, so does not pull to GND if power is not applied.
DSCL1	29	—	SchmittOD	In	DDC I^2C Clock for Port 1. 5V Tolerant. 5V Tolerant. HDCP KSV, An and Ri values are exchanged over an I^2C port during authentication. True open drain, so does not pull to GND if power is not applied.
DSDA1	28	3 mA	SchmittOD	Bi-Di	DDC I^2C Data for Port 1. 5V Tolerant. 5V Tolerant. HDCP KSV, An and Ri values are exchanged over an I^2C port during authentication. True open drain, so does not pull to GND if power is not applied.
CSCL	27	—	Schmitt	In	Configuration/Status I^2C Clock. 5V Tolerant. Chip configuration/status, CEA-861 support and downstream HDCP repeater-specific registers are accessed via this I^2C port. True open drain, so does not pull to GND if power is not applied.
CSDA	26	3 mA	Schmitt	Bi-Di	Configuration/Status I^2C Data. 5V Tolerant. Chip configuration/status, CEA-861 support and downstream HDCP repeater-specific registers are accessed via this I^2C port. True open drain, so does not pull to GND if power is not applied.
CI2CA	105		LLVTTL	In	Local I^2C Address Select. 5V Tolerant. Low = Addresses 0x60/0x68 High = Addresses 0x62/0x6A
SCDT	101	12 mA	LVTTL	Out	Indicates Active Video at HDMI Input Port. Sync detection indicator.
R0PWR5V	35	—	LVTTL	In	Port 0 Transmitter Detect. 5V Tolerant. Used for MUTEIN function.
R1PWR5V	30	—	LVTTL	In	Port 1 Transmitter Detect. 5V Tolerant. Used for MUTEIN function.
RSVDNC	98, 77, 76, 55				Reserved, must be left unconnected
RSVDL	99			In	Reserved, must be tied to ground

Note: The INT pin can be programmed to be either a push-pull LVTTL output or an open-drain output.

Differential Signal Data Pins

Pin Name	Pin #	Type	Description	
R0XC+	40	Analog	TMDS Input Clock Pair	HDMI Port 0
R0XC-	39	Analog		
R0X0+	44	Analog	TMDS Input Data Pair	
R0X0-	43	Analog		
R0X1+	48	Analog	TMDS Input Data Pair	
R0X1-	47	Analog		
R0X2+	52	Analog	TMDS Input Data Pair	
R0X2-	51	Analog		
R1XC+	58	Analog	TMDS Input Clock Pair	HDMI Port 1
R1XC-	57	Analog		
R1X0+	62	Analog	TMDS Input Data Pair	
R1X0-	61	Analog		
R1X1+	66	Analog	TMDS Input Data Pair	
R1X1-	65	Analog		
R1X2+	70	Analog	TMDS Input Data Pair	
R1X2-	69	Analog		

Power and Ground Pins

Pin Name	Pin #	Type	Description	Supply
CVCC18	12, 24, 25, 80, 91, 107, 119, 131, 143	Power	Digital Logic VCC	1.8V
CGND	11, 23, 79, 90, 106, 118, 130, 142	Ground	Digital Logic GND	
IOVCC33	6, 18, 32, 74, 88, 104, 113, 125, 137	Power	Input/Output Pin VCC	3.3V
IOGND	4, 17, 31, 73, 87, 103, 112, 124, 136	Ground	Input/Output Pin GND	
AVCC33	38, 42, 46, 50, 56, 60, 64, 68	Power	TMDS Analog VCC 3.3V	3.3V
AGND	36, 41, 45, 49, 53, 59, 63, 67, 71	Ground	TMDS Analog GND	
AVCC18	37, 54, 72	Power	TMDS Analog VCC 1.8V	1.8V
DVCC18	92	Power	Audio Clock Regeneration PLL Analog VCC. Must be connected to 1.8V	1.8V
DGND	93	Ground	Audio Clock Regeneration PLL Analog Ground.	
XTALVCC	96	Power	Audio Clock Regeneration PLL Crystal Oscillator Power. Must be connected to 3.3V	3.3V
REGVCC	97	Power	Audio Clock Regeneration PLL Crystal Regulator Power. Must be connected to 3.3V	3.3V

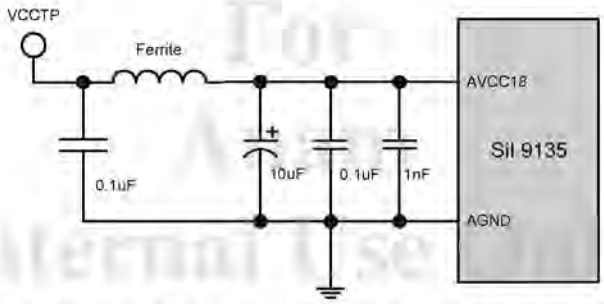


Figure 21. Test Point VCCTP for VCC Noise Tolerance Spec

Sil 9134 Pin Diagram

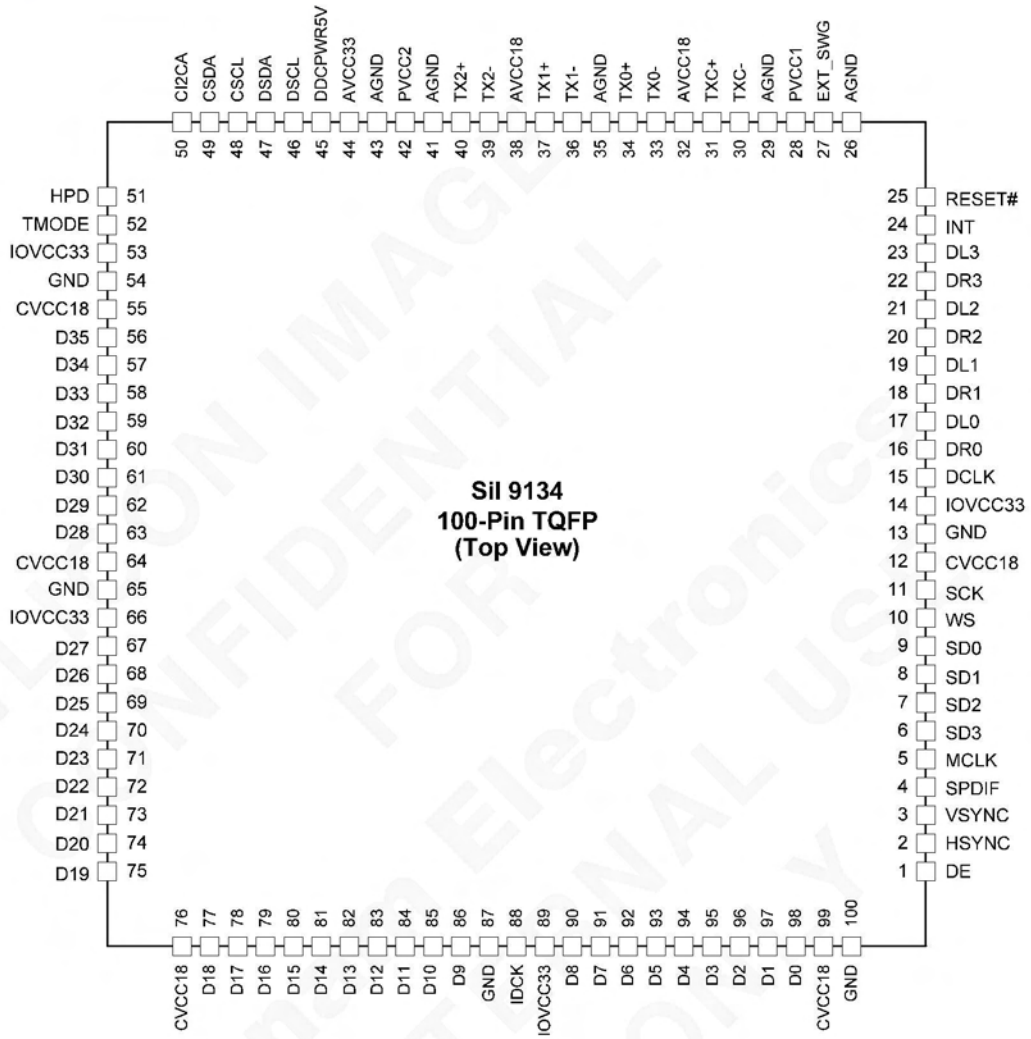


Figure 1. 100-Pin TQFP Pinout Diagram

Functional Description

The Sil 9134 provides a complete solution for transmitting HDMI compliant digital audio/video. Specialized audio/video processing available within the Sil 9134 easily and cost effectively adds HDMI capability to consumer electronics devices. Figure 2 shows the functional blocks of the device. Pin descriptions begin on page 35.

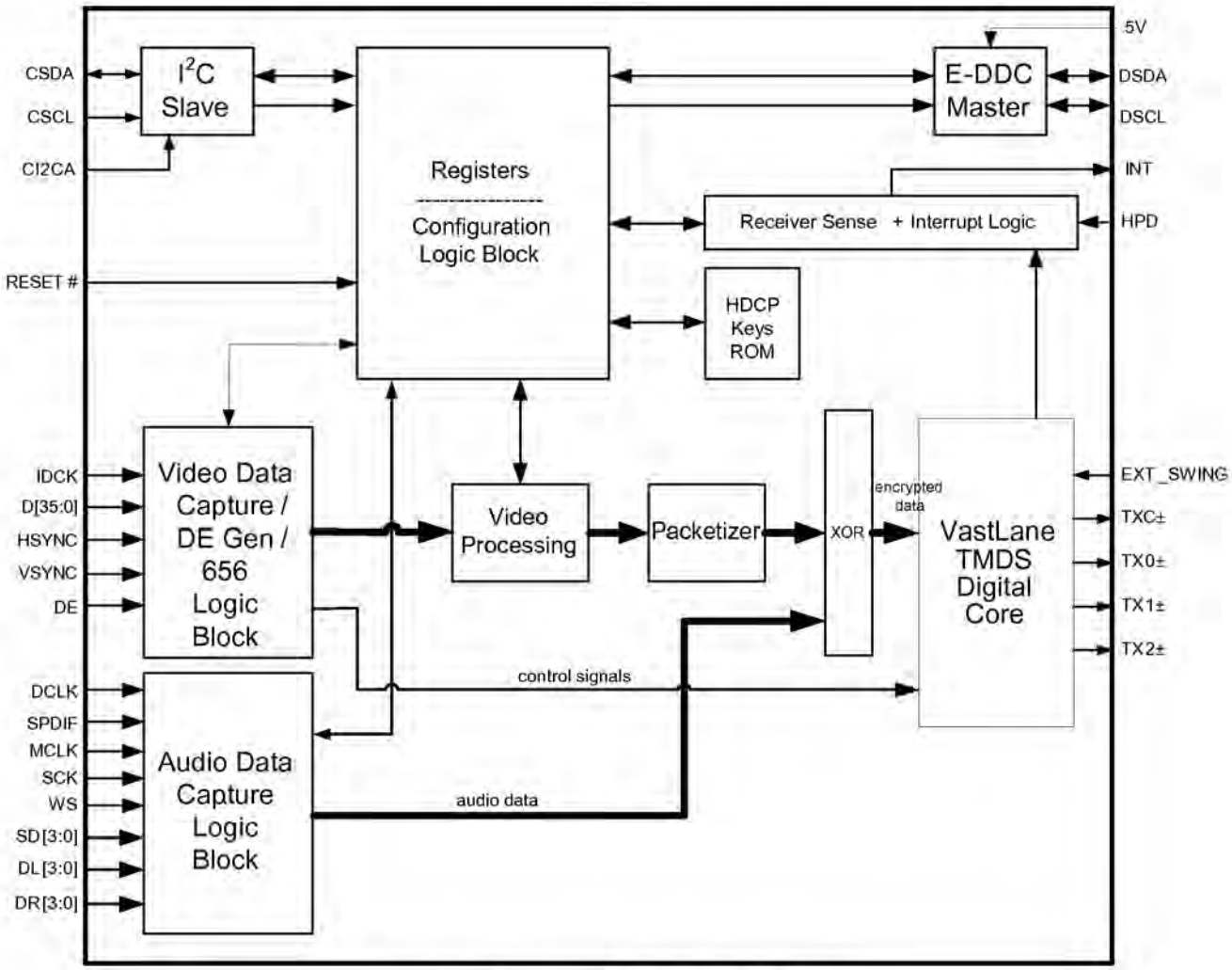


Figure 2. Functional Block Diagram

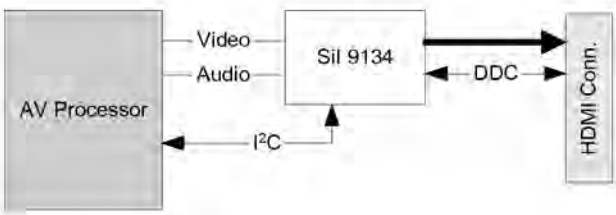


Figure 3. Simplified Host I²C Ports

Pin Descriptions

The following tables provide SiI 9134 pin descriptions.

Video and Audio Input Pins

Table 6 describes the SiI 9134 video and audio pins.

Table 6. Video and Audio Pins

Pin Name	Pin #	Type	Dir	Description
D0	98	LVTTL	Input	These are the lower 12 bits of the 36-bit pixel bus. These pins are highly configurable, and support multiple RGB and YCbCr formats. See Data Bus Mappings on page 39 for complete information.
D1	97	LVTTL	Input	
D2	96	LVTTL	Input	
D3	95	LVTTL	Input	
D4	94	LVTTL	Input	
D5	93	LVTTL	Input	
D6	92	LVTTL	Input	
D7	91	LVTTL	Input	
D8	90	LVTTL	Input	
D9	86	LVTTL	Input	
D10	85	LVTTL	Input	
D11	84	LVTTL	Input	
D12	83	LVTTL	Input	These are the middle 12 bits of the 36-bit pixel bus.
D13	82	LVTTL	Input	
D14	81	LVTTL	Input	
D15	80	LVTTL	Input	
D16	79	LVTTL	Input	
D17	78	LVTTL	Input	
D18	77	LVTTL	Input	
D19	75	LVTTL	Input	
D20	74	LVTTL	Input	
D21	73	LVTTL	Input	
D22	72	LVTTL	Input	
D23	71	LVTTL	Input	
D24	70	LVTTL	Input	These are the upper 12 bits of the 36-bit pixel bus.
D25	69	LVTTL	Input	
D26	68	LVTTL	Input	
D27	67	LVTTL	Input	
D28	63	LVTTL	Input	
D29	62	LVTTL	Input	
D30	61	LVTTL	Input	
D31	60	LVTTL	Input	
D32	59	LVTTL	Input	
D33	58	LVTTL	Input	
D34	57	LVTTL	Input	
D35	56	LVTTL	Input	

IDCK	88	LVTTL	Input	Input Data Clock
DE	1	LVTTL	Input	Data enable
HSYNC	2	LVTTL	Input	Horizontal Sync input control signal
VSYNC	3	LVTTL	Input	Vertical Sync input control signal
SCK	11	LVTTL	Input	I^2S Serial Clock
WS	10	LVTTL	Input	I^2S Word Select
SD0	9	LVTTL	Input	I^2S Serial Data
SD1	8	LVTTL	Input	I^2S Serial Data
SD2	7	LVTTL	Input	I^2S Serial Data
SD3	6	LVTTL	Input	I^2S Serial Data
DL0	17	LVTTL	Input	One-bit Audio Data Left 0
DR0	16	LVTTL	Input	One-bit Audio Data Right 0
DL1	19	LVTTL	Input	One-bit Audio Data Left 1
DR1	18	LVTTL	Input	One-bit Audio Data Right 1
DL2	21	LVTTL	Input	One-bit Audio Data Left 2
DR2	20	LVTTL	Input	One-bit Audio Data Right 2
DL3	23	LVTTL	Input	One-bit Audio Data Left 3
DR3	22	LVTTL	Input	One-bit Audio Data Right 3
DCLK	15	LVTTL	Input	One-bit Audio Clock Input
MCLK	5	LVTTL	Input	Audio Input Master Clock
SPDIF	4	LVTTL	Input	S/PDIF Audio Input.

ESMT **F25L004A**

4Mbit (512Kx8)

3V Only Serial Flash Memory

■ FEATURES

- Single supply voltage 2.7~3.6V
- Speed
  - Read max frequency : 33MHz
  - Fast Read max frequency : 50MHz; 75MHz; 100MHz
- Low power consumption
  - typical active current
  - 15μA typical standby current
- Reliability
  - 100,000 typical program/erase cycles
  - 20 years Data Retention
- Program
  - Byte program time 7μs(typical)
- Erase
  - Chip erase time 4s(typical)
  - Sector erase time 60ms(typical), block erase time 1sec (typical)
- Auto Address Increment (AAI) WORD Programming
  - Decrease total chip programming time over Byte-Program operations
- SPI Serial Interface
  - SPI Compatible : Mode 0 and Mode3
- End of program or erase detection
- Write Protect ($\overline{WP}$)
- Hold Pin ($\overline{HOLD}$)
- Package available
  - 8-pin SOIC 150-mil
  - 8-pin SOIC 200-mil

ORDERING INFORMATION

Part No.	Speed	Package		COMMENTS
F25L004A -50PG	50MHz	8 lead SOIC	150 mil	Pb-free
F25L004A -100PG	100MHz	8 lead SOIC	150 mil	Pb-free
F25L004A -50PAG	50MHz	8 lead SOIC	200 mil	Pb-free

Part No.	Speed	Package		COMMENTS
F25L004A –100PAG	100MHz	8 lead SOIC	200 mil	Pb-free
F25L004A –50DG	50MHz	8 lead PDIP	300 mil	Pb-free
F25L004A –100DG	100MHz	8 lead PDIP	300 mil	Pb-free

GENERAL DESCRIPTION

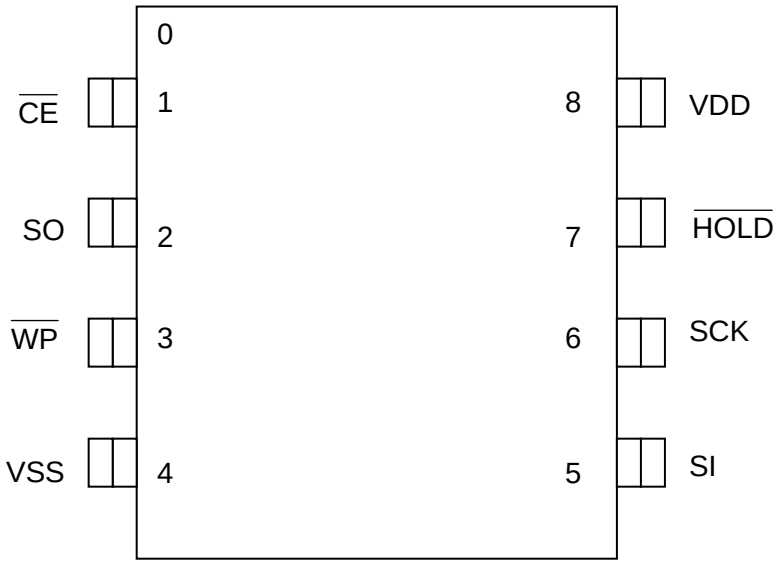
The F25L004A is a 4Megablt, 3V only CMOS Serial Flash memory device organized as 512K bytes of 8 bits. This device is packaged in 8-lead SOIC 200mil. ESMT's memory devices reliably store memory data even after 100,000 program and erase cycles.

The F25L004A features a sector erase architecture. The device memory array is divided into 128 uniform sectors with 4K byte each ; 8 uniform blocks with 64K byte each. Sectors can be erased individually without affecting the data in other sectors. Blocks can be erased individually without affecting the data in other blocks. Whole chip erase capabilities provide the flexibility to revise the data in the device.

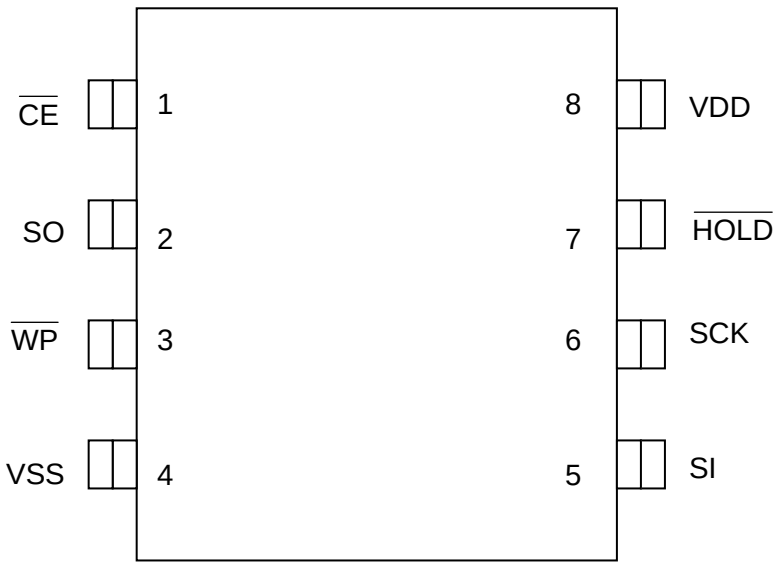
The sector protect/unprotect feature disables both program and erase operations in any combination of the sectors of the memory.

PIN CONFIGURATIONS

8-PIN SOIC



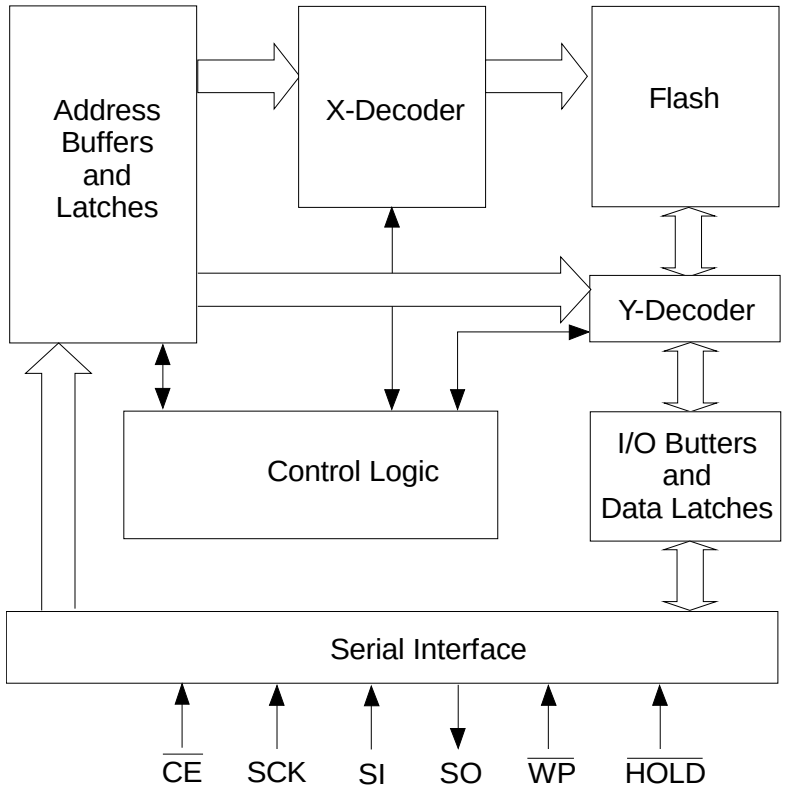
8-PIN PDIP



PIN Description

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing for serial input and output operations
SI	Serial Data Input	To transfer commands, addresses or data serially into the device. Data is latched on the rising edge of SCK.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of SCK.
$\overline{CE}$	Chip Enable	To activate the device when $\overline{CE}$ is low.
$\overline{WP}$	Write Protect	The Write Protect ($\overline{WP}$) pin is used to enable/disable BPL bit in the status register.
$\overline{HOLD}$	Hold	To temporality stop serial communication with SPI flash memory without resetting the device.
VDD	Power Supply	To provide power.
VSS	Ground	

FUNTIONAL BLOCK DIAGRAM



TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

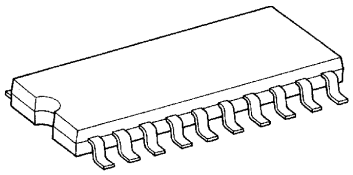
TC74LCX541F, TC74LCX541FW, TC74LCX541FT

LOW VOLTAGE OCTAL BUS BUFFER WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX541 is a high performance CMOS OCTAL BUS BUFFER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.
The 74LCX541 is a non-inverting 3-state buffer having two active-low output enables. When either $\overline{OE}1$ or $\overline{OE}2$ are high, the terminal outputs are in the high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge.

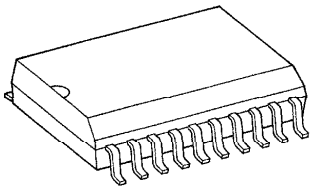
(Note) The JEDEC SOP (FW) is not available in Japan.

TC74LCX541F



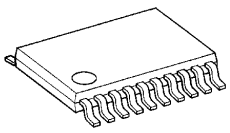
SOP20-P-300-1.27

TC74LCX541FW



SOL20-P-300-1.27

TC74LCX541FT



TSSOP20-P-0044-0.65

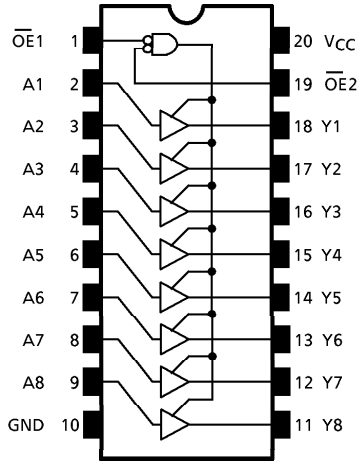
Weight
SOP20-P-300-1.27 : 0.22g (Typ.)
SOL20-P-300-1.27 : 0.46g (Typ.)
TSSOP20-P-0044-0.65 : 0.08g (Typ.)

FEATURES

- Low voltage operation : $V_{CC} = 2.0 \sim 3.6V$
- High speed operation : t_{pd} = 6.5ns (Max.) ($V_{CC} = 3.0 \sim 3.6V$)
- Output current : $|I_{OH}| / I_{OL}$ = 24mA (Min.) (V_{CC} = 3.0V)
- Latch-up performance : ±500mA
- Available in JEDEC SOP, EIAJ SOP and TSSOP
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC / VHC / HC / F / ALS / LS etc.) 541 type.

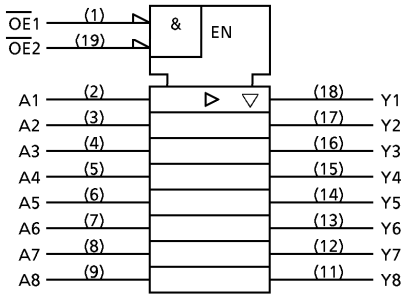
961001EBA2

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}1$	$\overline{OE}2$	An	
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

X : Don't Care
Z : High Impedance

MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~7.0 (Note 1)	V
		−0.5~V_{CC}+0.5 (Note 2)	
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (Note 3)	mA
DC Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	180	mW
DC V_{CC}/Ground Current	I_{CC}/I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

(Note 1) Output in Off-State
(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.
(Note 3) $V_{OUT}<GND$, $V_{OUT}>V_{CC}$

961001EBA2'

CS4970x4 Data Sheet

FEATURES

- Multi-standard 32-bit High Definition Audio Decoding plus Post Processing
- Supports high-definition audio formats including:
  - Dolby Digital® Plus
  - Dolby® TrueHD
  - DTS-HD™ High Resolution Audio
  - DTS-HD™ Master Audio
  - DSD®
- Additional Applications Library
  - Dolby Digital® EX, Dolby® Pro Logic® IIx, Dolby Headphone®, Dolby® Virtual Speaker®
  - DTS-ES 96/24™, DTS-ES™ Discrete 6.1, DTS-ES™ Matrix 6.1
  - AAC™ Multichannel 5.1
  - SRS® CS2® and TSXT®
  - THX® Ultra2™, THX® ReEQ™
  - Crossbar Mixer, Signal Generator
  - Advanced Post-Processor including: 7.1 Bass Manager, Tone Control, 11- Band Parametric EQ, Delay, 1:2 Upsampler
  - Microsoft® HDCD®
  - Thomson MP3 Surround, DTS:Neo6™, DSD-to-PCM Conversion, Neural Surround, Cirrus Original Multi-Channel Surround 2 (COMS2), and more. Please contact your local FAE for more information on available applications.
- Up to 12 Channels of 32-bit Serial Audio Input

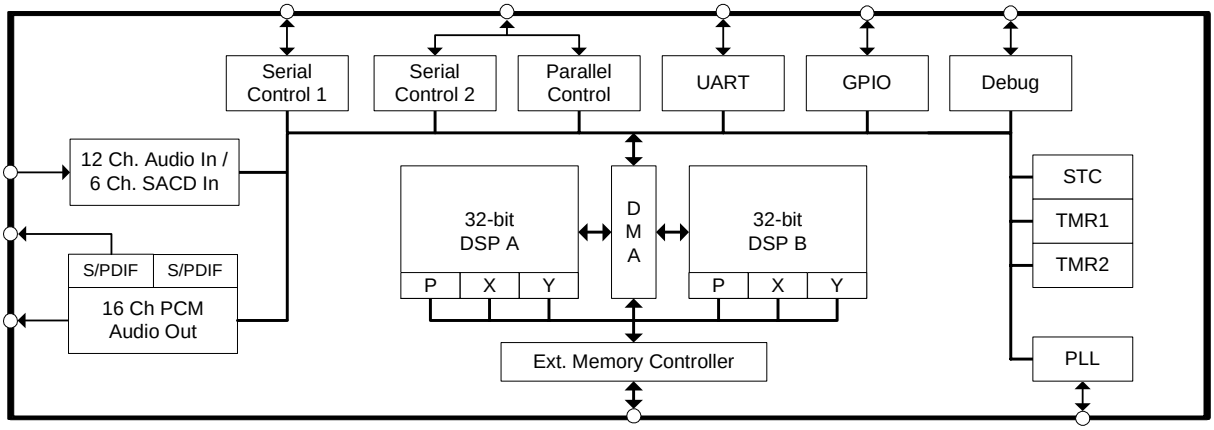
32-bit High Definition Audio Decoder DSP Family with Dual DSP Engine Technology

- Customer Software Security Keys
- 6 Channel DSD® Input
- 16 Ch x 32-bit PCM Out with Dual 192 kHz SPDIF Tx
- Two SPI™/I²C®, One Parallel and One UART Port
- Large On-chip X, Y, and Program RAM & ROM
- SDRAM and Serial Flash Memory Support

The CS4970x4 DSP family is an enhanced version of the CS4953x DSP family with higher overall performance. In addition to all the mainstream audio processing codes in on-chip ROM that the CS4953x DSP offers, the CS4970x4 device family also supports the decoding of major high-definition audio formats. Additionally, the CS4970x4, a dual-core device, performs the high-definition audio decoding on the first core, leaving the second core available for audio post-processing and audio enhancement. The CS4970x4 device will support the most demanding audio post processing requirements. It is also designed as an easy upgrade path to systems currently using the CS495xx or CS4953x device with minor hardware and software changes.

Ordering Information

See page 30 for ordering information.



Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

SEP '08
DS752PP7

8. Device Pin-Out Diagram

8.1 128-Pin LQFP Pin-Out Diagram

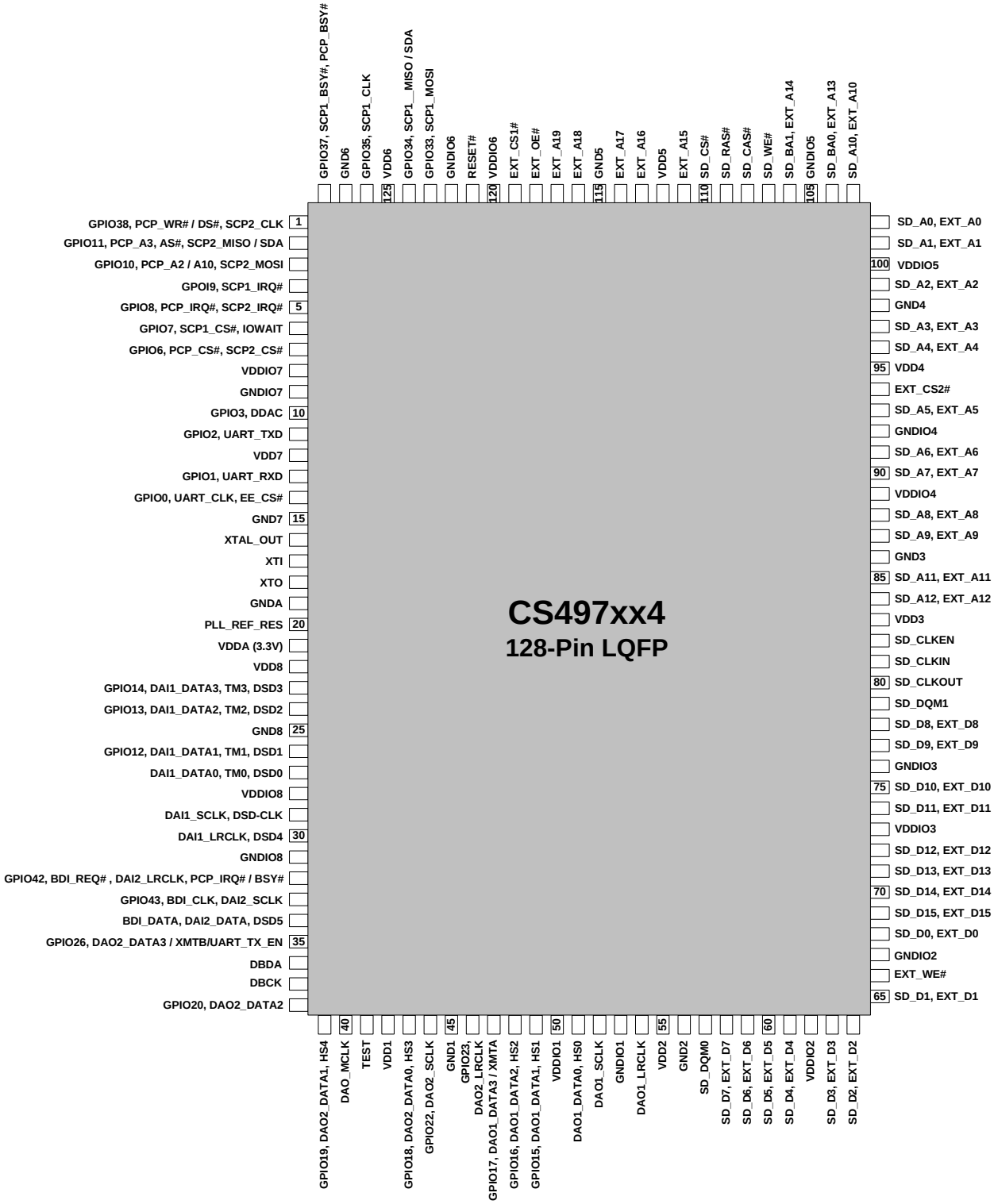


Figure 20. 128-Pin LQFP Pin-Out Diagram

8.2 144-Pin LQFP Pin-Out Diagram

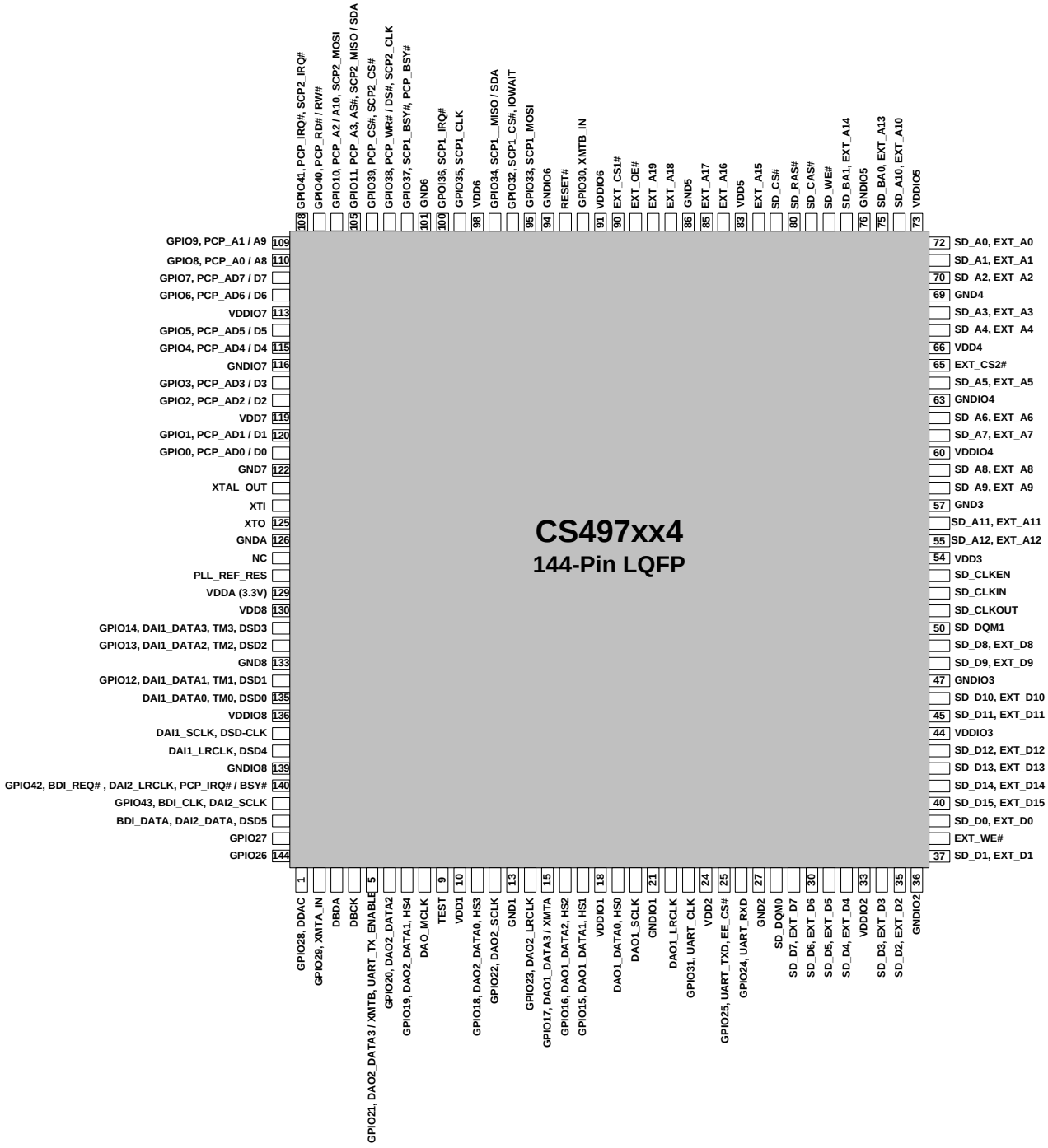


Figure 21. 144-Pin LQFP Pin-Out Diagram

ESMT M12L16161A

SDRAM 512K x 16Bit x 2Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst Read Single-bit Write operation
- DQM for masking
- Auto & self refresh
- 32ms refresh period (2K cycle)

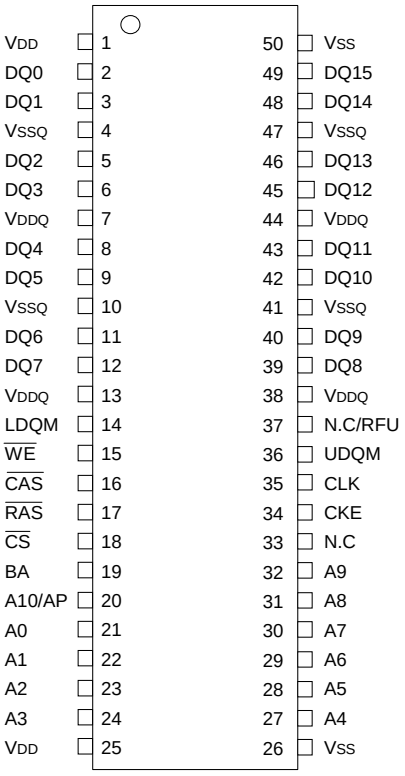
GENERAL DESCRIPTION

The M12L16161A is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 524,288 words by 16 bits, fabricated with high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

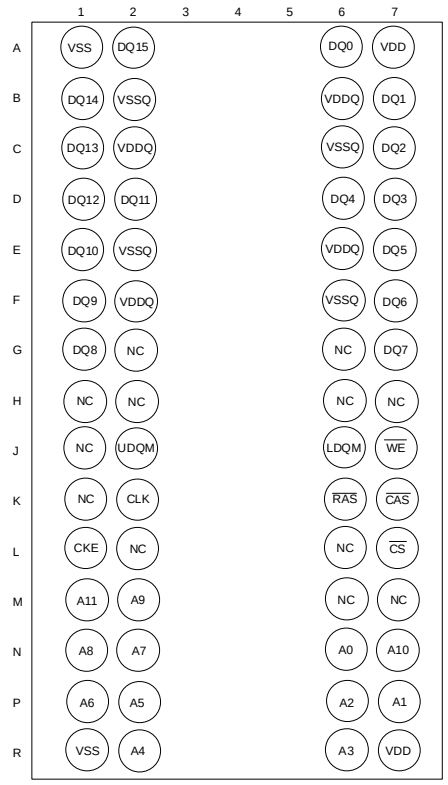
ORDERING INFORMATION

Part NO.	MAX Freq.	PACKAGE	COMMENTS
M12L16161A-5TG	200MHz	TSOP(II)	Pb-free
M12L16161A-7TG	143MHz	TSOP(II)	Pb-free
M12L16161A-7BG	143MHz	VFBGA	Pb-free

PIN CONFIGURATION (TOP VIEW)

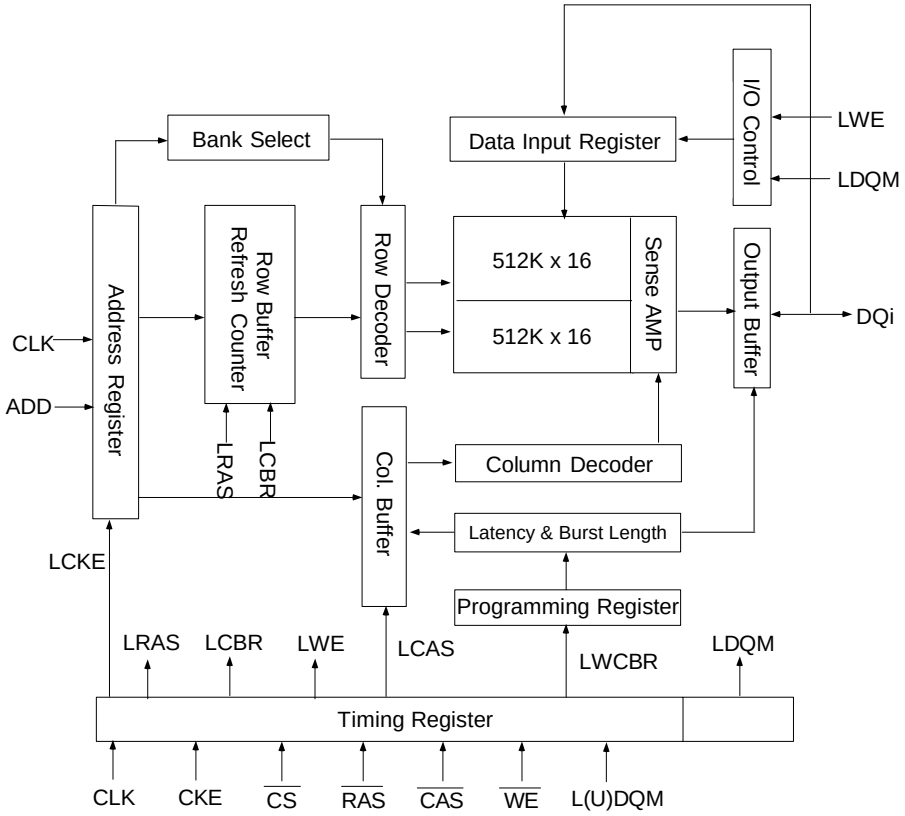


50PIN TSOP(II)
(400mil x 825mil)
(0.8 mm PIN PITCH)



60 Ball VFBGA
(6.4x10.1mm)
(0.65mm ball pitch)

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM.
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA7
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data Input / Output Mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when L(U)DQM active.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A10/AP	A9~A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
				L									3
	Self Refresh	Entry											
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	4
	Both Banks									X	H		4
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
			H		L	H	H	H					

(V= Valid, X= Don't Care, H= Logic High , L = Logic Low)

Note:

1. OP Code: Operation Code

   A0~ A10/AP, BA: Program keys.(@MRS)

2. MRS can be issued only at both banks precharge state.

   A new command can be issued after 2 clock cycle of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

   The automatical precharge without row precharge command is meant by "Auto".
   Auto / self refresh can be issued only at both banks idle state.

4. BA: Bank select address.

   If "Low": at read, write, row active and precharge, bank A is selected.
   If "High": at read, write, row active and precharge, bank B is selected.
   If A10/AP is "High" at row precharge, BA ignored and both banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

   Another bank read /write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes
   Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

ROHM

◇ STRUCTURE Silicon Monolithic Integrated Circuit
◇ PRODUCT I^2C BUS Serial EEPROMs
◇ SERIES ADVANTAGE SERIES
◇ FAMILY BR24C□□ family
◇ TYPE Supply voltage 1.8V～5.5V/Opreating temperature -40℃～+85℃type
◇ PART NUMBER BR24C□□-10□U-1.8

PART NUMBER	PACKAGE	DENSITY
BR24C01A -10SU-1.8	8-lead JEDECSOIC	1Kbit
BR24C02N -10SU-1.8		2Kbit
BR24C04N -10SU-1.8		4Kbit
BR24C08AN -10SU-1.8		8Kbit
BR24C16AN -10SU-1.8		16Kbit
BR24C32AN -10SU-1.8		32Kbit
BR24C01A -10TU-1.8	8-lead TSSOP	1Kbit
BR24C02 -10TU-1.8		2Kbit
BR24C04 -10TU-1.8		4Kbit
BR24C08A -10TU-1.8		8Kbit
BR24C16A -10TU-1.8		16Kbit
BR24C32A -10TU-1.8		32Kbit

◇ FEATURE
Two wire serial interface
Endurance : 1,000,000 erase/write cycles
Data retention : 100years
Intial Data FFh in all address

◇ ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Operating Temperature	Topr	-40～85	℃
Storage Temperature	Tstg	-65～125	℃
Voltage on Any Pin with Respect to Ground	-	-0.3～Vcc+0.3	V
Maximum Operating Voltage	Vcc	-0.3～6.5	V

◇ POWER DISSIPATION (Ta=25℃)

PACKAGE	Rating	Unit
8-lead JEDECSOIC	450 *1	mW
8-lead TSSOP	330 *2	mW

* Degradation is done at 4.5mW/℃(*1), 3.3mW/℃(*2)for operation above 25℃

ROHM

◇ DC OPERATING CHARACTERISTICS

BR24C01A/02/04/08A/16A.Unless otherwise specified,Vcc=1.8V to 5.5V, Ta=-40℃ to 85℃

Parameter	Symbol	Min	Max	Unit	Test Conditions
Supply Current Vcc=5.0V	I_{CC1}	-	1.0	mA	READ at 100 kHz
Supply Current Vcc=5.0V	I_{CC2}	-	3.0	mA	WRITE at 100 kHz
Standby Current Vcc=1.8V	I_{SB1}	-	3.0	μA	V_{IN}=V_{CC} or GND
Standby Current Vcc=2.5V	I_{SB2}	-	4.0	μA	V_{IN}=V_{CC} or GND
Standby Current Vcc=2.7V	I_{SB3}	-	4.0	μA	V_{IN}=V_{CC} or GND
Standby Current Vcc=5.0V	I_{SB4}	-	18.0	μA	V_{IN}=V_{CC} or GND
Input Leakage Current	I_{LI}	-	3.0	μA	V_{IN}=V_{CC} or GND
Output Leakage Current	I_{LO}	-	3.0	μA	V_{OUT}=V_{CC} or GND
Input Low Level	V_{IL}	-	Vccx0.3	V	2.5V≦Vcc≦5.5V
		-	Vccx0.2		1.8V≦Vcc<2.5V
Input High Level	V_{IH}	Vccx0.7	-	V	2.5V≦Vcc≦5.5V
		Vccx0.8	-		1.8V≦Vcc<2.5V
Output Low Level Vcc=3.0V	V_{OL1}	-	0.4	V	I_{OL}=2.1mA
Output Low Level Vcc=1.8V	V_{OL2}	-	0.2	V	I_{OL}=0.15mA

◇ AC OPERATING CHARACTERISTICS

BR24C01A/02/04/08A/16A.Unless otherwise specified,Vcc=1.8V to 5.5V, Ta=-40℃ to 85℃

Parameter	Symbol	1.8V		2.5V,2.7V,5.0V		Unit
		Min	Max	Min	Max	
Clock Frequency, SCL	f_{SCL}	-	100	-	400	kHz
Clock Pulse Width Low	t_{LOW}	4.7	-	1.2	-	μs
Clock Pulse Width High	t_{HIGH}	4.0	-	0.6	-	μs
Noise Suppression Time	t_I	-	100	-	50	ns
Clock Low to Data Out Valid	t_{AA}	0.1	4.5	0.1	0.9	μs
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	-	1.2	-	μs
Start Hold Time	$t_{HD.STA}$	4.0	-	0.6	-	μs
Start Setup Time	$t_{SU.STA}$	4.7	-	0.6	-	μs
Data In Hold Time	$t_{HD.DAT}$	0	-	0	-	μs
Data In Setup Time	$t_{SU.DAT}$	200	-	100	-	ns
Inputs Rise Time *1	t_R	-	1.0	-	0.3	μs
Inputs Fall Time *1	t_F	-	300	-	300	ns
Stop Setup Time	$t_{SU.STO}$	4.7	-	0.6	-	μs
Data Out Hold Time	t_{DH}	100	-	50	-	ns
Write Cycle Time	t_{WR}	-	5	-	5	ms
Endurance *1 5.0V, 25℃	Endurance	1M	-	1M	-	Write Cycles

*1 Not 100% TESTED

BR24C32A Unless otherwise specified,Vcc=1.8V to 5.5V, Ta=-40℃ to 85℃

Parameter	Symbol	Min	Max	Unit	Test Conditions
Supply Current Vcc=5.0V	I_{CC1}	-	1.0	mA	READ at 400 kHz
Supply Current Vcc=5.0V	I_{CC2}	-	3.0	mA	WRITE at 400 kHz
Standby Current Vcc=1.8V	I_{SB1}	-	1.0	μA	V_{IN}=V_{CC} or GND
Standby Current Vcc=2.5V	I_{SB2}	-	2.0	μA	V_{IN}=V_{CC} or GND
Standby Current Vcc=2.7V	I_{SB3}	-	2.0	μA	V_{IN}=V_{CC} or GND
Standby Current Vcc=5.0V	I_{SB4}	-	6.0	μA	V_{IN}=V_{CC} or GND
Input Leakage Current	I_{LI}	-	3.0	μA	V_{IN}=V_{CC} or GND
Output Leakage Current	I_{LO}	-	3.0	μA	V_{OUT}=V_{CC} or GND
Input Low Level	V_{IL}	-	Vccx0.3	V	2.5V≦Vcc≦5.5V
		-	Vccx0.2		1.8V≦Vcc<2.5V
Input High Level	V_{IH}	Vccx0.7	-	V	2.5V≦Vcc≦5.5V
		Vccx0.8	-		1.8V≦Vcc<2.5V
Output Low Level Vcc=3.0V	V_{OL1}	-	0.4	V	I_{OL}=2.1mA
Output Low Level Vcc=1.8V	V_{OL2}	-	0.2	V	I_{OL}=0.15mA

BR24C32A.Unless otherwise specified,Vcc=1.8V to 5.5V, Ta=-40℃ to 85℃

Parameter	Symbol	1.8V		2.5V,2.7V,5.0V		Unit
		Min	Max	Min	Max	
Clock Frequency, SCL	f_{SCL}	-	100	-	400	kHz
Clock Pulse Width Low	t_{LOW}	4.7	-	1.3	-	μs
Clock Pulse Width High	t_{HIGH}	4.0	-	0.6	-	μs
Noise Suppression Time	t_I	-	100	-	50	ns
Clock Low to Data Out Valid	t_{AA}	0.1	4.5	0.1	0.9	μs
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	-	1.3	-	μs
Start Hold Time	$t_{HD.STA}$	4.0	-	0.6	-	μs
Start Setup Time	$t_{SU.STA}$	4.7	-	0.6	-	μs
Data In Hold Time	$t_{HD.DAT}$	0	-	0	-	μs
Data In Setup Time	$t_{SU.DAT}$	200	-	100	-	ns
Inputs Rise Time *1	t_R	-	1.0	-	0.3	μs
Inputs Fall Time *1	t_F	-	300	-	300	ns
Stop Setup Time	$t_{SU.STO}$	4.7	-	0.6	-	μs
Data Out Hold Time	t_{DH}	100	-	50	-	ns
Write Cycle Time	t_{WR}	-	5	-	5	ms
Endurance *1 5.0V, 25℃	Endurance	1M	-	1M	-	Write Cycles

*1 Not 100% TESTED

○This product is not designed for protection against radioactive rays.

◇ BLOCK DIAGRAM

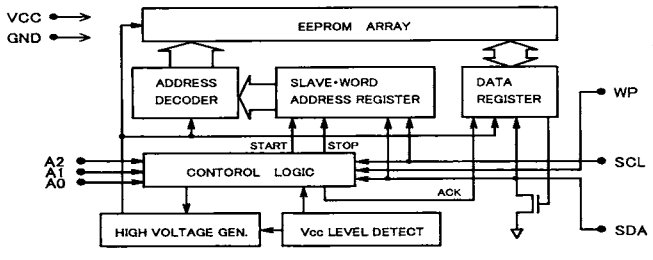


Fig.-1 BLOCK DIAGRAM

◇ PIN No., PIN NAME

PIN No.	PIN NAME
1	A0
2	A1
3	A2
4	GND
5	SDA
6	SCL
7	WP
8	Vcc

IC51 XM IC

1. Overview

The XM Digital Transceiver Integrated Circuit (XM/DT IC) provides a cost effective means for an electronics equipment manufacturer to be XM Satellite Radio compatible by multiplexing data and audio streams between the XM Receiver and User Interface Controller into a 2 wire time division duplex (TDD) high frequency serial link.

In a typical application, two XM/ DT IC devices connect to each other via a differential link as depicted on Figure 1.1 below. In the 'Slave' unit ("XM/DT Digital Transceiver" (antenna)), the XM/DT IC interfaces directly to the XM Radio receiver chipset taking in a real-time PCM (I2S) audio stream along with data information. The XM/DT IC stores this data in internal RAM and then time division multiplexes the data on a 2-wire serial communication link. This link provides for the physical decoupling of the Slave and Master side of up 100 meters with software transparency between the Master side processor and audio circuitry and the Slave side XM Satellite Radio receiver chip set.

In the Master unit ("XM/DT Ready Radio"), the XM/DT IC demultiplexes the received data, buffers it internally and reproduces it for consumption. The XM/DT IC is capable of simultaneously sending and receiving serial frames while multiplexing and de-multiplexing them in real time, formatting them and then routing them into the appropriate Slave or Master side interfaces.

The software interface between the user interface and the receiver is unaffected by the introduction of the XM/DT IC link pair.

An input pin on the XM/DT IC configures the part's functionality as either Master (user interface end) or Slave (XM Digital Transceiver end) allowing the same IC to be used at either end of the link.

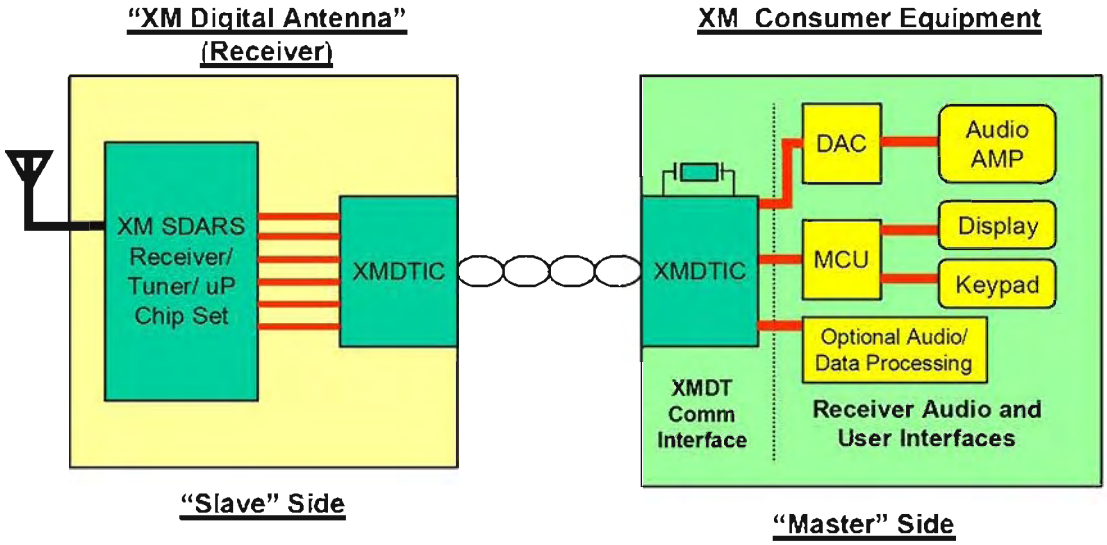


Figure 1.1 - Typical XM/DT Application

2. Functional Description

Figure 2.1 below shows a basic top level diagram showing each functional block in the XM/DT device.

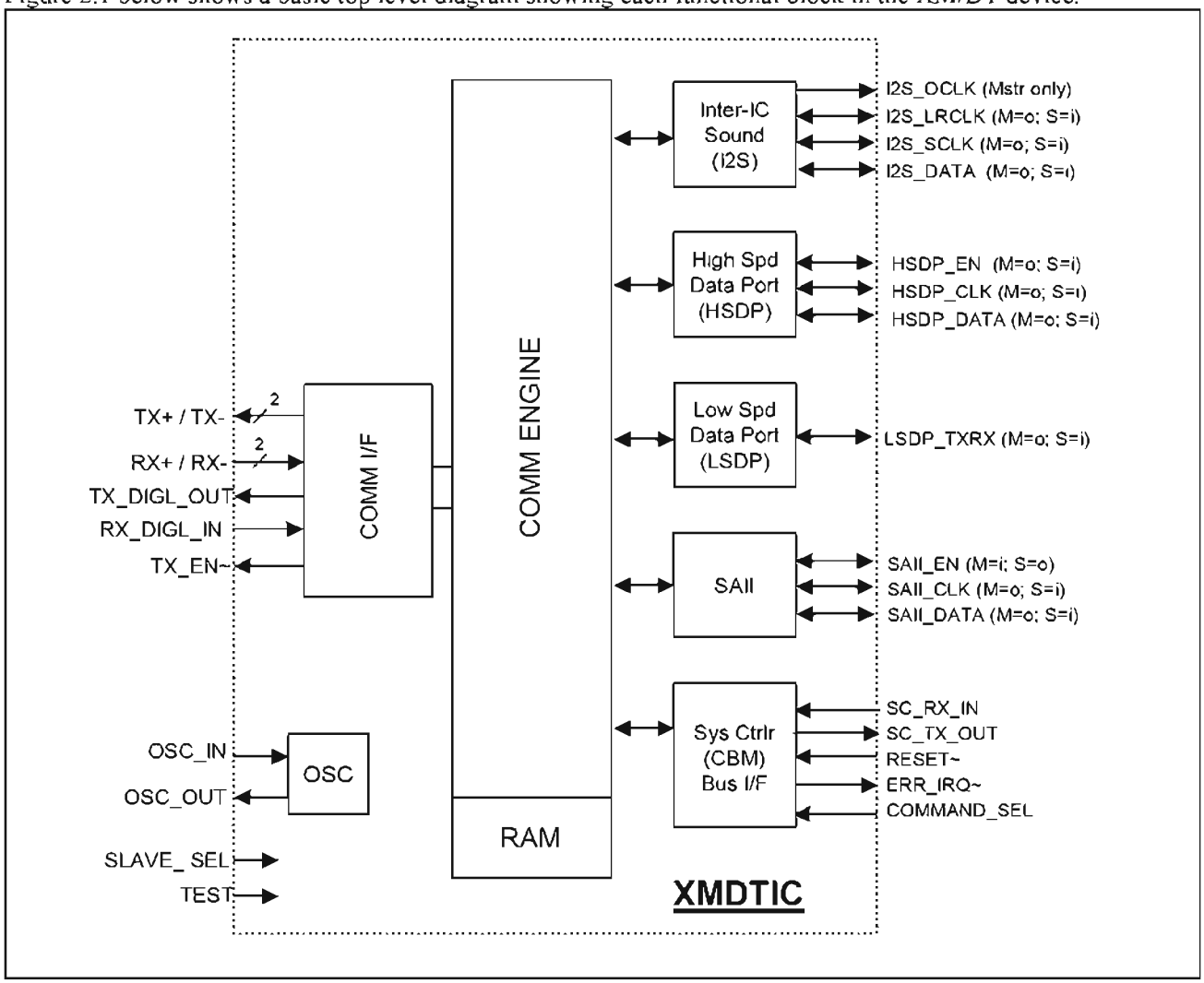


Figure 2.1 XM/DT Top Level Diagram

The XM/DT IC is broken into the following functional blocks:

SC I/F – System Controller Interface

The System Controller Interface transports the serial communication commands and data between the microprocessor in the user interface device and the microprocessor in the XM Digital Antenna. The commands and data transported follow typically follow the XM CBM (Common Bus Messaging) protocol.

The System Controller Interface functional block consists of a full duplex asynchronous serial interface. The SC I/F is used for both the software configuration of the XM/DT IC, monitoring of XM/DT link status, and transparent communications with the SC I/F at the other end of the communications link. The SC I/F block contains five signals, SC_RX_IN, SC_TX_OUT, COMMAND_SEL, ERR_IRQ#, and RESET#.

The SC_RX_IN and SC_TX_OUT connect the asynchronous serial communications to the respective microprocessors. The SC I/F

communicates at a default mode of 9600 baud, no parity, 8 data bits, and 1 stop bit. The baud rate can be changed using the XM/DT IC Command Mode. The Master and Slave baud rates must be set to the same rate by their respective microprocessors.

The COMMAND_SEL input allows configuration of the XM/DT IC and to retrieve feedback of the link status during normal operation. This signal is logic low for normal operation and logic high for Command/Stat Mode. Details of the operation of this signal are described in the Programming section of this specification.

The ERR_IRQ# output signal is active low when an error occurs on the link if interrupts are enabled via the Interrupt Mask register. Access to the Interrupt Mask register is gained via the Command Mode and the interrupt source identification is obtained via the Status Mode. Details of these modes are described in the Programming section of this specification.

The RESET# input signal is used to perform a complete asynchronous reset of the XM/DT IC. The RESET# signal is also used to place the XM/DT IC into Command Mode. Refer to the Programming section.

SAII – Synchronous Audio Input Interface

The SAII Interface functional block provides a synchronous interface with hardware flow control from the Master to the Slave devices.

In Master mode, the XM/DT IC receives SAII Data and SAII Clock from the SAII source in the "playback unit". The SAII Enable (SAII_EN) output signal is fed back to the SAII source to control the flow of input data based on the state of the SAII_EN signal at the Slave Device.

In Slave mode, the XM/DT IC sends SAII Data and SAII Clock to the Slave device SAII receiver, and receives the SAII_EN signal from the SAII receiver to control the flow of transmitted data.

The Master XM/DT IC adapts to the incoming SAII data rate.

LSDP – Low Speed Data Port

The LSDP functional block consists of a unidirectional asynchronous serial interface.

In Master mode, the LSDP transmits data out of the device. In Slave mode, the LSDP receives data into the device.

This interface operates in default mode at 115200, no parity, 8 data bits, and 1 stop bit.

HSDP – High Speed Data Port Interface

The HSDP Interface functional block provides a synchronous serial interface combined with a framing signal from the Slave XM/DT IC to the Master XM/DT IC.

The source of the HSDP is typically the XM receiver chipset. The HSDP data is typically received by the Host microprocessor. The HSDP signals include a serial data bitstream (HSDP_DA), a synchronous clock (HSDP_CLK), and a framing signal (HSDP_EN). The framing signal can be used as a gating mechanism for the clock or an interrupt source to indicate the beginning and end of the HSDP data burst.

In Slave mode, the HSDP Interface receives HSDP_DA, HSDP_CLK, and HSDP_EN from the HSDP source. In Master mode, the HSDP Interface transmits HSDP_DA, HSDP_CLK, and HSDP_EN.

I2S – Inter-IC Sound (I2S) digital audio Interface

The I2S functional block receives and transmits timing and frame sensitive data. The I2S interface is also referred to as the PCM interface.

In Slave mode, the XM/DT IC I2S Interface receives the I2S digital audio from the XM Receiver chipset. The XM/DT IC automatically adjusts to the incoming I2S data sampling rate.

In Master mode, the XM/DT IC I2S Interface generates all required signals to drive an I2S compatible audio DAC.

COMM2W – Two Wire Communications Interface

The COMM2W functional block enables communications between two XM/DT ICs. The COMM2W is differential Time-Division-Duplex Interface.

3. Physical Description

3.1 Device Pin-out

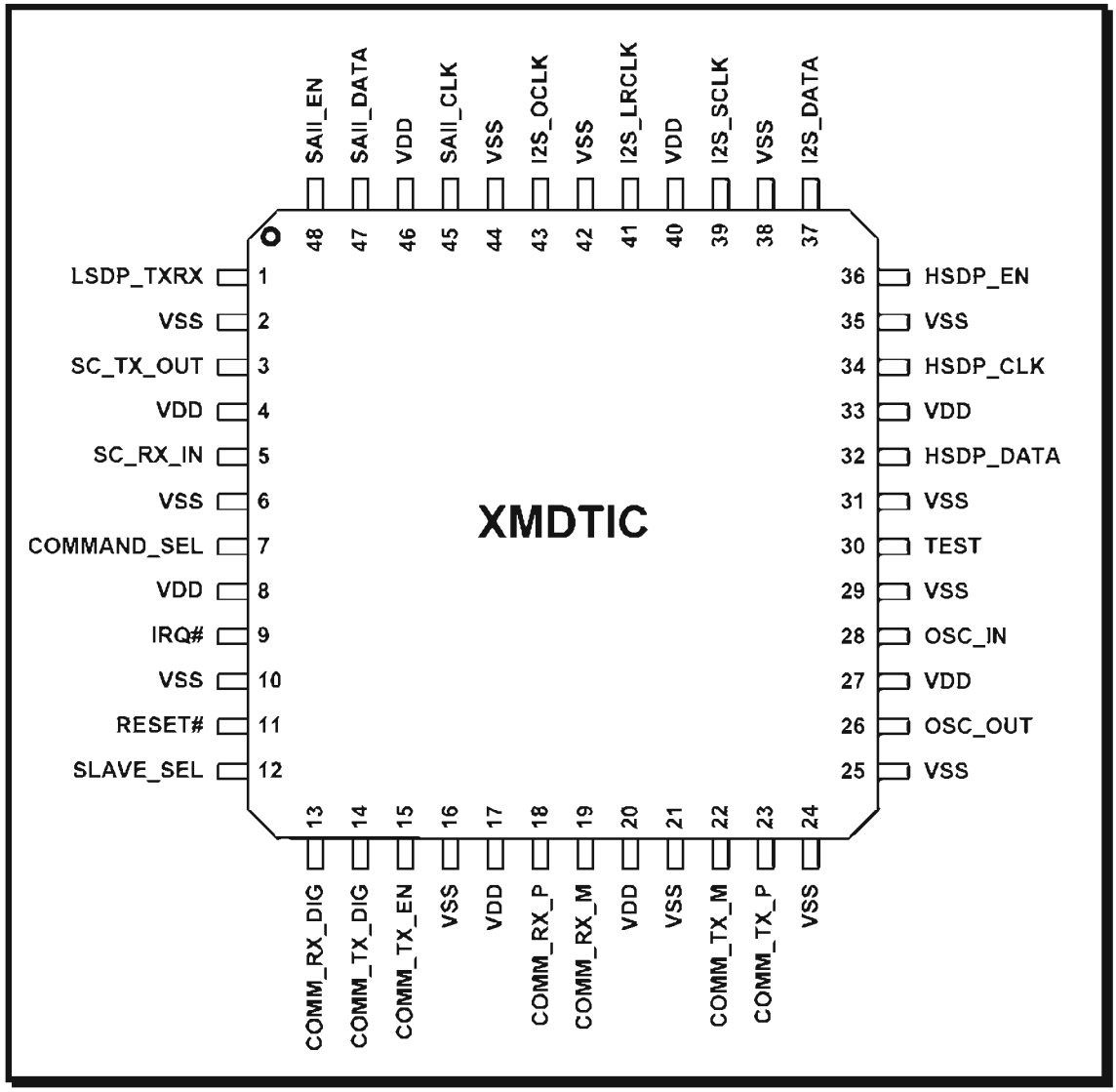


Figure 3.1 – Pin Connection (Top View)

3.2 Pin Descriptions

Table 3.2 Pin Descriptions

Pin #	Pin Name	Type	Function in Slave Mode	Function in Master Mode	Notes
1	LSDP_TXRX	S=In M=Out	Low Speed Data Port Output	Low Speed Data Port Input	LVTTL S/T
3	SC_TX_OUT	S=Out M=Out	System Controller Bus (CBM) Transmit Data Out	System Controller Bus (CBM) Transmit Data Out	4mA, SLC
5	SC_RX_IN	S=In M=In	System Controller Bus (CBM) Receive Data In	System Controller Bus (CBM) Receive Data In	LVTTL S/T
7	COMMAND_SEL	S=In M=In	Command Mode Select In (1= Command Mode, 0=Normal Mode)	Command Mode Select In (1= Command Mode, 0=Normal Mode)	LVTTL S/T
9	IRQ#	S=Out M=Out	Interrupt Request Out (Active Low)	Interrupt Request Out (Active Low)	4mA Open Drain
11	RESET#	S=In M=In	Asynchronous Reset In, (Active Low)	Asynchronous Reset In, (Active Low)	LVTTL S/T
12	SLAVE_SEL	S=In M=In	M/S Mode Select In (High = Slave Mode)	M/S Mode Select In (Low = Master Mode)	LVTTL S/T
13	COMM_RX_DIG	S=In M=In	DT Comm Bus External Transceiver Receive Data In	DT Comm Bus External Transceiver Receive Data In	LVTTL S/T
14	COMM_TX_DIG	Output	DT Comm Bus External Transceiver Transmit Data Out	DT Comm Bus External Transceiver Transmit Data Out	LVTTL S/T
15	COMM_TX_EN	Output	DT Comm Bus External Transceiver Direction Out (1=Transmit, 0=Receive)	DT Comm Bus External Transceiver Direction Out (1=Transmit, 0=Receive)	LVTTL S/T
18	COMM_RX_P	S=In M=In	DT Comm Bus Internal Receiver Differential Positive In	DT Comm Bus Internal Receiver Differential Positive In	LVDS in+
19	COMM_RX_M	S=In M=In	DT Comm Bus Internal Receiver Differential Negative In	DT Comm Bus Internal Receiver Differential Negative In	LVDS in–
22	COMM_TX_M	Output	DT Comm Bus Internal Transmitter Differential Negative Out	DT Comm Bus Internal Transmitter Differential Negative Out	LVDS out–
23	COMM_TX_P	Output	DT Comm Bus Internal Transmitter Differential Positive Out	DT Comm Bus Internal Transmitter Differential Positive Out	LVDS out+
26	OSC_OUT	Output	Crystal Output	Crystal Output	Crystal Buffer
28	OSC_IN	S=In M=In	Crystal Input	Crystal Input	Crystal Buffer
30	TEST	S=In M=In	Factory Test Mode Select (1=Test, 0= Normal Oper.)	Factory Test Mode Select (1=Test, 0= Normal Oper.)	LVTTL S/T
32	HSDP_DATA	S=In M=Out	High Speed Data Port Data Input	High Speed Data Port Data Output	Out= 4mA, SLC In=LVTTL S/T
34	HSDP_CLK	S=In M=Out	High Speed Data Port Clock Input	High Speed Data Port Clock Output	Out= 4mA, SLC In=LVTTL S/T
36	HSDP_EN	S=Out M=In	High Speed Data Port Enable Output	High Speed Data Port Enable Input	Out= 4mA, SLC In=LVTTL S/T
37	I2S_DATA	S=In M=Out	I2S Digital Port Data In	I2S Digital Audio Port Data Out	Out= 4mA, SLC In=LVTTL S/T

Pin #	Pin Name	Type	Function in Slave Mode	Function in Master Mode	Notes
39	I2S_SCLK	S=In M=Out	I2S Digital Audio Port Bit Clock In	I2S Digital Audio Port Bit Clock Out	Out= 4mA, SLC In=LVTTL S/T
41	I2S_LRCLK	S=In M=Out	I2S Digital Audio Port Left/Right Clock In	I2S Digital Audio Port Left/Right Clock Out	Out= 4mA, SLC In=LVTTL S/T
43	I2S_OCLK	S=In M=Out	I2S Digital Audio Port Oversample Clock (not used - connect to Gnd???)	I2S Digital Audio Port Oversample Clock Out	Out= 4mA, SLC
45	SAII_CLK	S=Out M=In	SAII Port Clock Output	SAII Port Clock Input	Out= 4mA, SLC 3.3V S/T
47	SAII_DATA	S=Out M=In	SAII Port Data Output	SAII Port Data Input	Out= 4mA, SLC In=LVTTL S/T
48	SAII_REQ	S=In M=Out	SAII Port Request Input	SAII Port Request Output	Out= 4mA, SLC In=LVTTL S/T

Pin#	Pin Name	Type	Function in Slave Mode	Function in Master Mode	Notes
4, 8, 17, 20, 27, 33, 40, 46	VDD	PWR	+3.3V Supply Voltage	+3.3V Supply Voltage	
2, 6, 10, 16, 21, 24, 25, 29, 31, 25, 38, 42, 44	VSS	GND	Digital Ground	Digital Ground	

Notes: All Inputs are 3.3V LVTTL compatible; S/T = Schmitt Trigger inputs; SLC = Slew Rate Controller Output

JRC **NJM2566A**

6CH VIDEO AMPLIFIER WITH SD/ HD LPF

■ GENERAL DESCRIPTION

The NJM2566A is a single supply voltage 6ch Video amplifier.

It includes LPF, Y/C MIX circuit and SDC interface. LPF for the component signal can select SD/HD.

The NJM2566A is suitable for DVD recorder, set top box and the high quality AV systems with the SD/HD output.

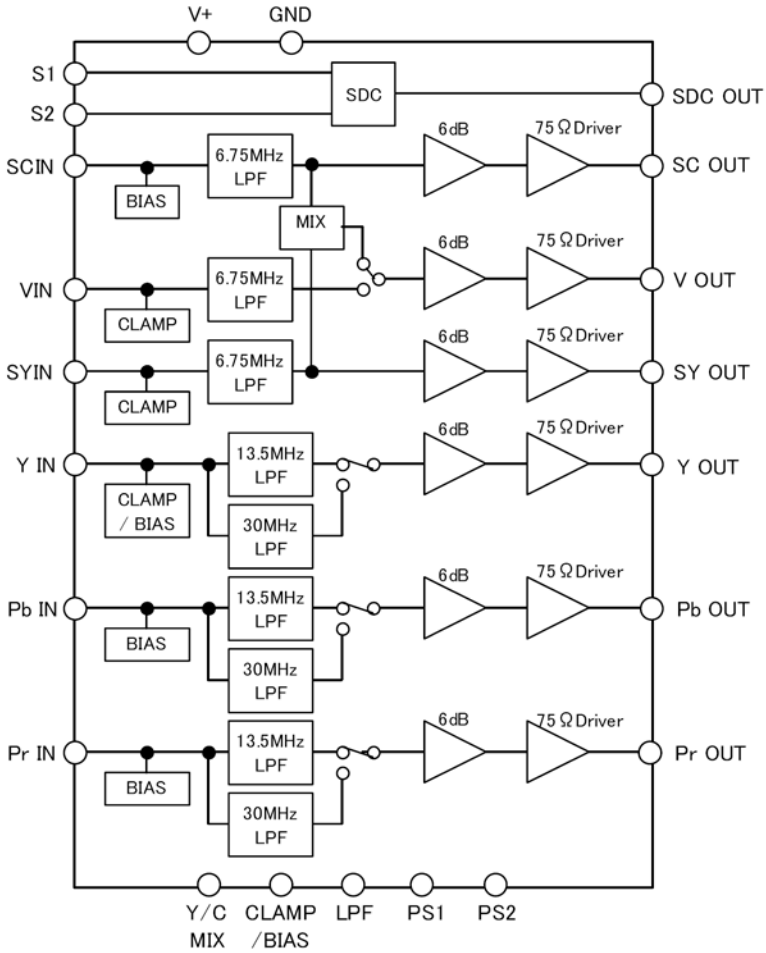
■ PACKAGE OUTLINE

NJM2566AV

■ FEATURES

- Operating Voltage 4.5 to 5.5V
- 6dB amplifier
- Internal 75Ω Driver Circuit (2-system drive)
- Internal LPF V,SY,SC 6.75MHz
  Y,Pb,Pr 13.5MHz (Progressive)
  30MHz (HD)
- Y/C MIX Circuit
- SDC Interface (S1/ S2)
- CLAMP/ BIAS Select (Y,Pb,Pr/ RGB)
- Power Save Circuit
- Bipolar Technology
- Package Outline SSOP32

■ BLOCK DIAGRAM



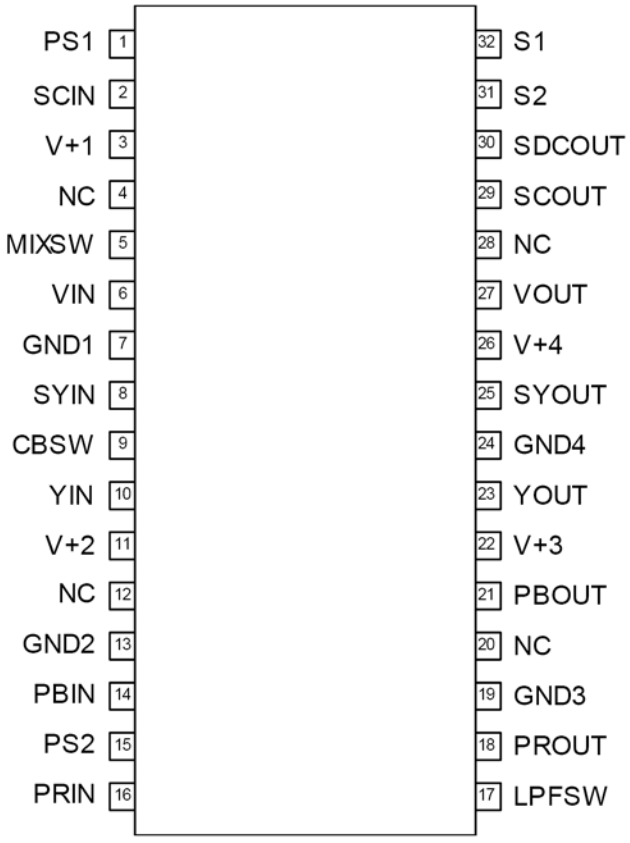
■ CONTROL TERMINAL

PARAMETER	STATUS	NOTE
PS1 (Power Save1)	H	(SYOUT, VOUT, SCOUT) Power Save: OFF
	L	(SYOUT, VOUT, SCOUT) Power Save: ON
	OPEN	(SYOUT, VOUT, SCOUT) Power Save: ON
PS2 (Power Save2)	H	(YOUT, PbOUT, PrOUT) Power Save: OFF
	L	(YOUT, PbOUT, PrOUT) Power Save: ON
	OPEN	(YOUT, PbOUT, PrOUT) Power Save: ON
MIX SW (Y/C MIX)	H	M/C MIX ON
	L	M/C MIX OFF
	OPEN	M/C MIX OFF
C/B SW (CLAMP/BIAS)	H	BIAS (RGB)
	L	CLAMP (Y,Pb,Pr)
	OPEN	CLAMP (Y,Pb,Pr)
LPF SW (LPF)	H	30MHz LPF
	L	13.5MHz LPF
	OPEN	13.5MHz LPF

■ SDC OUT

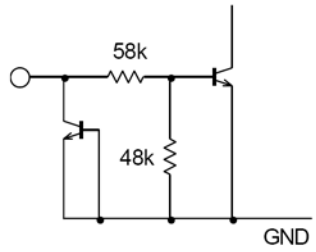
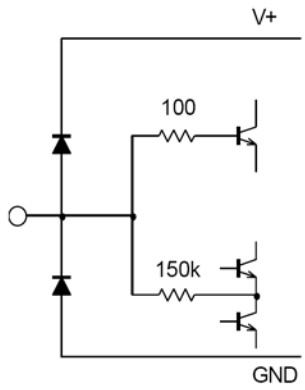
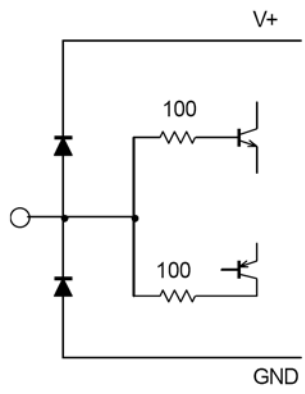
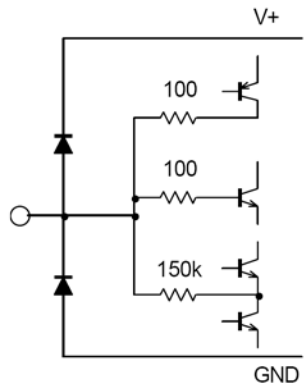
S1	S2	SDC OUT	
L (OPEN)	L (OPEN)	0V	4:3 Normal
L (OPEN)	H	2.1V	4:3 Letter box
H	H	2.1V	4:3 Letter box
H	L (OPEN)	4.6V	16:9 Squeeze

■ PIN CONFIGURATION

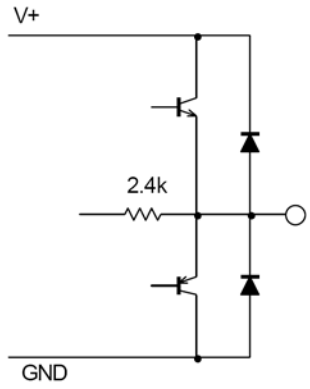
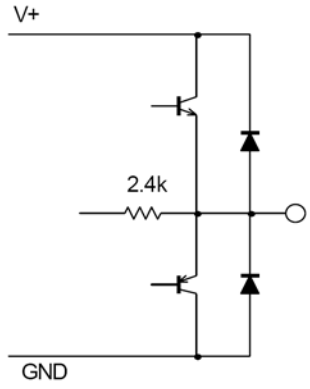
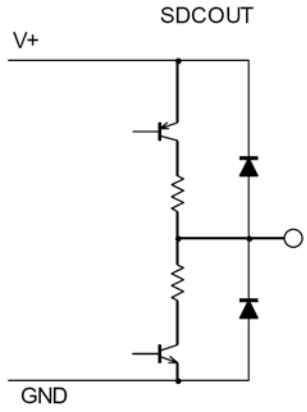


JRC **NJM2566A**

■ **TERMINAL FUNCTION**

PIN No.	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT	DC VOLTAGE
1 5 9 15 17 31 32	PS1 MIXSW CBSW PS2 LPFSW S2 S1	(SY, V, SC, SDC) Power save Y/C MIX control CLAMP/ BIAS control (Y, Pb, Pr) Power save (Y, Pb, Pr) LPF control SDC control SDC control		-
2 14 16	SCIN PBIN PRIN	Chroma signal input Component signal(Pb), R input Component signal(Pr), B input		2.5V
6 8	VIN SYIN	Composite video signal input Y signal input		1.7V
10	YIN	Component signal(Y), G input (Note) Y signal: CLAMP G signal: BIAS		(CLAMP) 1.7V (BIAS) 2.5V

JRC **NJM2566A**

PIN No.	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT	DC VOLTAGE
18 21 29	PROUT PBOUT SCOUT	Component signal(Cr) output Component signal(Cb) output Chroma signal output		2.5V
23 25 27	YOUT SYOUT VOUT	Component signal(Y) output Y signal output Composite video signal output		1.3V (Note) YOUT BIAS: 2.5V
30	SDCOUT	SDC output		-

NJW1197FC2
[8-CHANNEL ELECTRONIC VOLUME WITH INPUT SELECTOR]

[STRUCTURE] Bi-CMOS
[CATEGORIES] 3D Surround & Sound Enhancement
[PACKAGE OUTLINE] QFP100-C2
[SOLDERING METHOD] For this device, soldering method is recommended Reflow.
[NOTE] —

BAE-45919-000-00

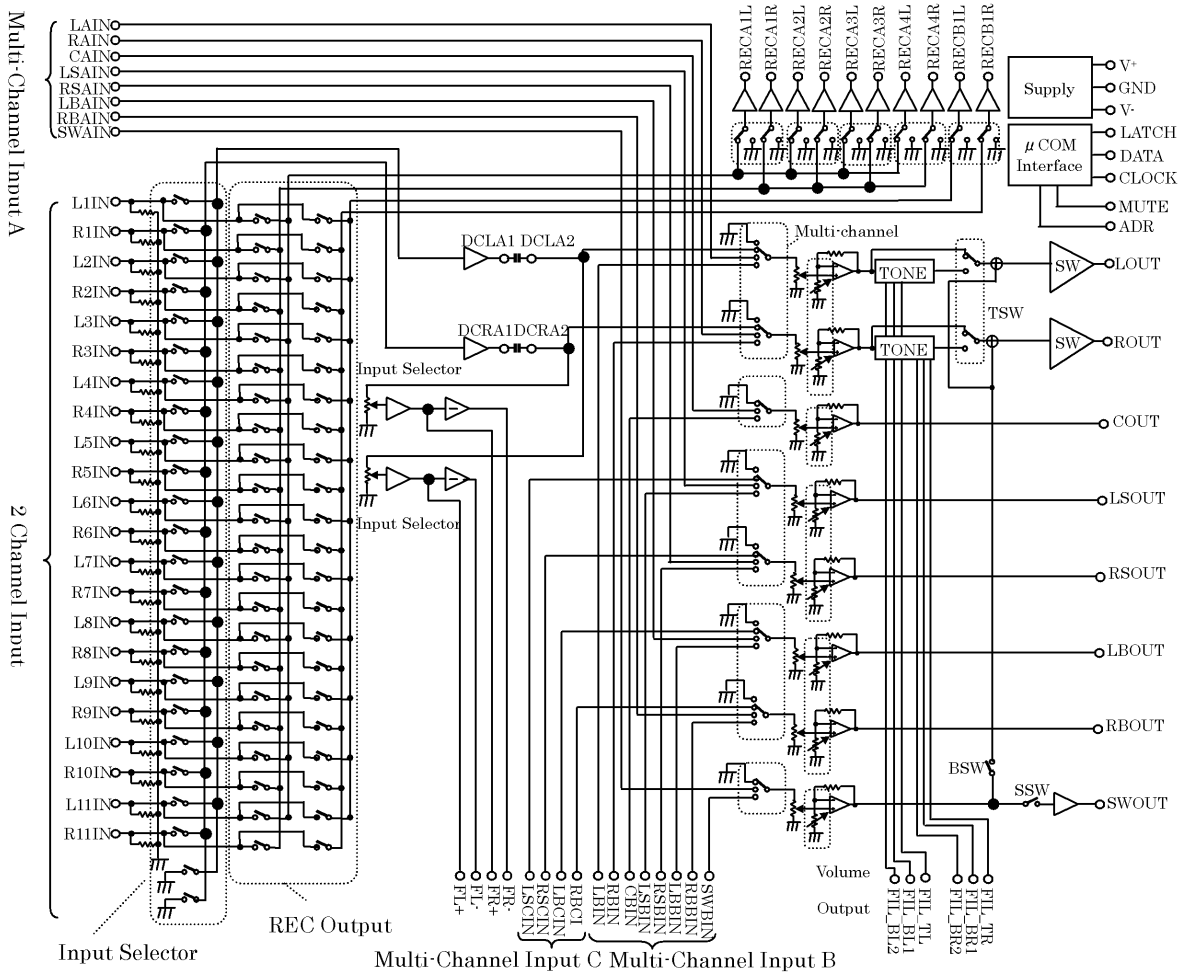
■ABSOLUTE MAXIMUM RATINGS Ta=25℃

Power Supply Voltage ····· +8/-8 [V]	Operating Temperature Range ····· -40 to +75 [℃]
Maximum Input Voltage ····· V^+/V^- [V]	Storage Temperature Range ····· -40 to +150 [℃]
Power Dissipation ····· 1600 [mW] (Note)	

(Note) EIA/JEDEC STANDARD Test board (76.2×114.3×1.6mm, 2layer, FR-4) mounting.

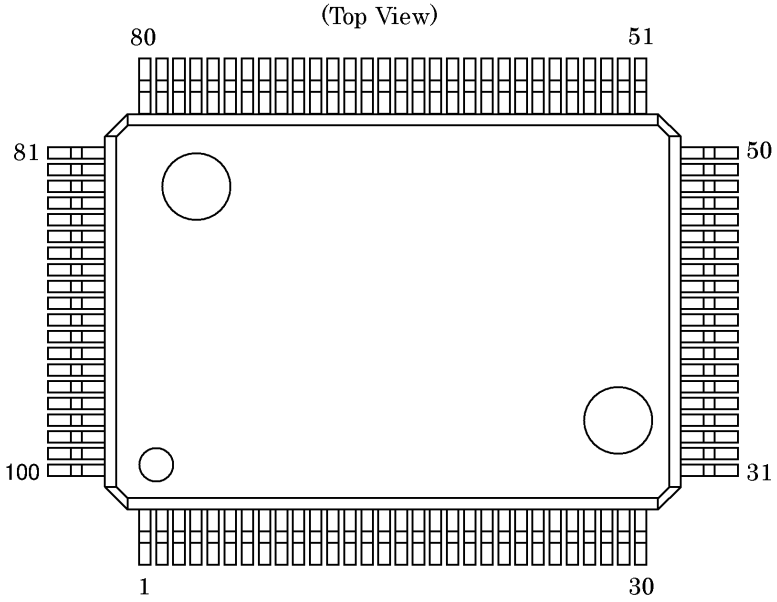
■BLOCK DIAGRAM

BDE-45919-000-00



■PIN CONFIGURAITON

BEE-45919-000-00



No.	SYMBOL	No.	SYMBOL	No.	SYMBOL	No.	SYMBOL
1	ROUT	26	DCCAP_RS	51	DCR_IN	76	GND
2	COUT	27	L3IN	52	DCR_OUT	77	LSCIN
3	LSOUT	28	DCCAP_LS	53	GND	78	RSCIN
4	RSOUT	29	R3IN	54	DCL_IN	79	LBCIN
5	LBOUT	30	DCCAP_C	55	DCL_OUT	80	RBCIN
6	RBOUT	31	L4IN	56	GND	81	GND
7	SWOUT	32	DCCAP_R	57	REC_B1R	82	LAIN
8	GND	33	R4IN	58	REC_B1L	83	RAIN
9	FIL_BL2	34	DCCAP_L	59	REC_A4R	84	CAIN
10	FIL_BL1	35	L5IN	60	REC_A4L	85	LSAIN
11	FIL_TL	36	GND	61	REC_A3R	86	RSAIN
12	TCAP	37	R5IN	62	REC_A3L	87	LBAIN
13	FIL_BR2	38	GND	63	REC_A2R	88	RBAIN
14	FIL_BR1	39	L6IN	64	REC_A2L	89	SWAIN
15	FIL_TR	40	L9IN	65	REC_A1R	90	GND
16	V^+	41	R6IN	66	REC_A1L	91	LBIN
17	ADR	42	R9IN	67	VDDOUT	92	RBIN
18	V^-	43	L7IN	68	DATA	93	CBIN
19	L1IN	44	L10IN	69	CLOCK	94	LSBIN
20	DCCAP_SW	45	R7IN	70	LATCH	95	RSBIN
21	R1IN	46	R10IN	71	MUTE	96	LBBIN
22	DCCAP_RB	47	L8IN	72	FL+	97	RBBIN
23	L2IN	48	L11IN	73	FL-	98	SWBIN
24	DCCAP_LB	49	R8IN	74	FR+	99	GND
25	R2IN	50	R11IN	75	FR-	100	LOUT

■FUNCTIONAL DESCRIPTION

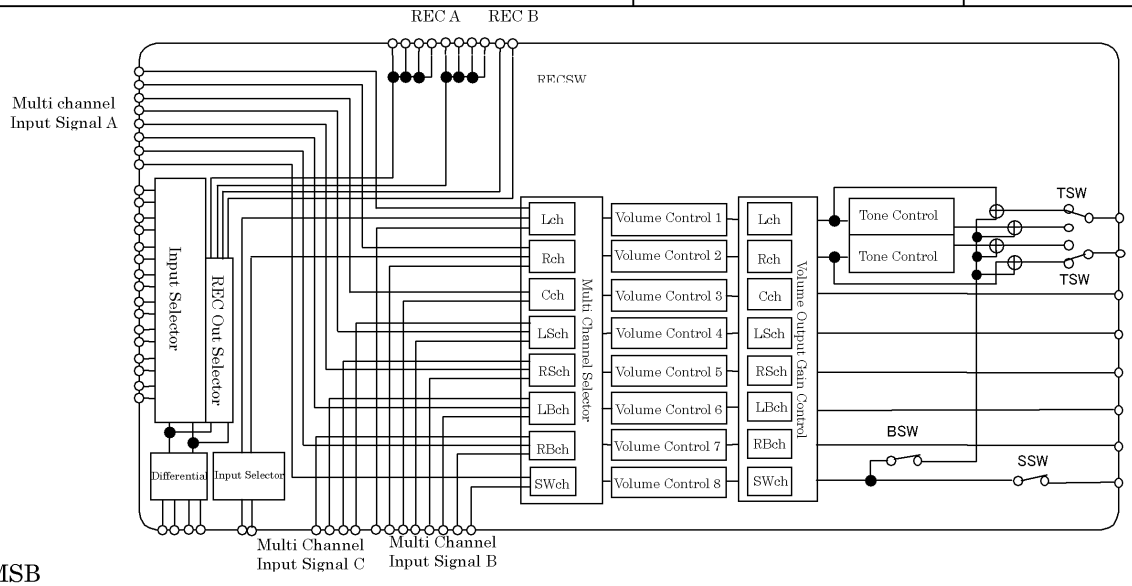
BGE-45919-000-00

(1) CONTROL DATA

NJW1197 control data is constructed with 16bits.

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data								Select Address				Chip Address			



MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L channel Volume Control								0	0	0	0	*	*	*	*
R channel Volume Control								0	0	0	1	*	*	*	*
C channel Volume Control								0	0	1	0	*	*	*	*
LS channel Volume Control								0	0	1	1	*	*	*	*
RS channel Volume Control								0	1	0	0	*	*	*	*
LB channel Volume Control								0	1	0	1	*	*	*	*
RB channel Volume Control								0	1	1	0	*	*	*	*
SW channel Volume Control								0	1	1	1	*	*	*	*
Input Selector Gain Control			Input Selector				SSW	1	0	0	0	*	*	*	*
TC/B	Tone Control Treble				TSW	BSW	*	1	0	0	1	*	*	*	*
BC/B	Tone Control Bass				*	*	*	1	0	1	0	*	*	*	*
REC B Selector				Input Selector				1	0	1	1	*	*	*	*
SWch Volume Output Gain Control		REC B1	REC A4	REC A3	REC A2	REC A1		1	1	0	0	*	*	*	*
L, Rch Volume Output Gain Control		Cch, Volume Output Gain Control			*	*		1	1	0	1	*	*	*	*
LS, RSch Volume Output Gain Control		LB, RBch Volume Output Gain Control			SWch Selector			1	1	1	0	*	*	*	*
L, Rch Selector		Cch Selector		LS, RSch Selector		LB, RBch Selector		1	1	1	1	*	*	*	*

*: Don't Care

* Chip address is set by chip address select terminal (ADR) status.

Chip Address Select Terminal (ADR: 17pin)	Chip Address			
	D3	D2	D1	D0
Low	0	1	0	0
High	0	1	0	1

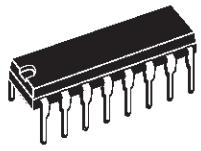
* The mute function can be controlled externally. If the Mute control terminal (71pin) is switched to High, Multi-Channel outputs are muted immediately (hardware mute).

External mute control terminal (MUTE: 71pin)	Setting
Low	Mute cancellation
High	Mute

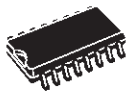
ST202E
ST232E

± 15KV ESD PROTECTED 5V RS-232 TRANSCEIVER

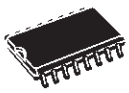
- ESD PROTECTION FOR RS-232 I/O PINS: ± 15 KV HUMAN BODY MODEL
- GUARANTEED 120 kbps DATE RATE
- GUARANTEED SLEW RATE RANGE 3 to 30V/µs
- OPERATE FROM A SINGLE 5V POWER SUPPLY



N
(Plastic Package)



D
(Micro Package)



W
(Micro Package Large)

T
(TSSOP Package)

DESCRIPTION

The ST202E/ST232E are a 2 driver 2 receiver devices designed for RS-232 and V.28 communications in harsh enviroments. Each transmitter output and receiver input is protected against ± 15KV electrostatic discharge (ESD) shocks. The drivers meet all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120Kbps, when loaded in accordance with the EIA/TIA-232E specification.

The ST202E/232E use a single 5V supply voltage.

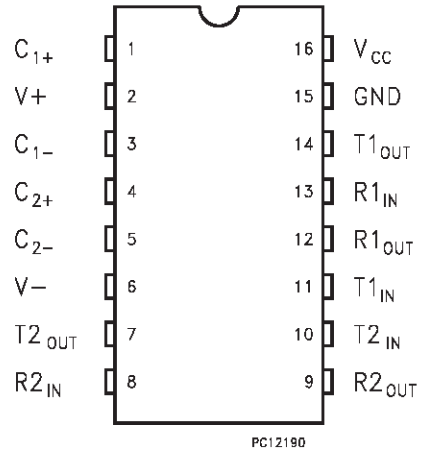
The ST232E operates with four 1µF capacitors, while the ST202E operates with four 0.1µF capacitors, further reducing cost and board space.

ORDER CODES

Type		Temperature Range	Package	Comments
ST202ECN	ST232ECN	0 to 70 °C	DIP-16	25 parts per tube / 40 tube per box
ST202EBN	ST232EBN	-40 to 85 °C	DIP-16	25 parts per tube / 40 tube per box
ST202ECD	ST232ECD	0 to 70 °C	SO-16 (Tube)	50 parts per tube / 20 tube per box
ST202EBD	ST232EBD	-40 to 85 °C	SO-16 (Tube)	50 parts per tube / 20 tube per box
ST202ECDR	ST232ECDR	0 to 70 °C	SO-16 (Tape & Reel)	2500 parts per reel
ST202EBDR	ST232EBDR	-40 to 85 °C	SO-16 (Tape & Reel)	2500 parts per reel
ST202ECW	ST232ECW	0 to 70 °C	SO-16 Large (Tube)	50 parts per tube / 20 tube per box
ST202EBW	ST232EBW	-40 to 85 °C	SO-16 Large (Tube)	50 parts per tube / 20 tube per box
ST202ECWR	ST232ECWR	0 to 70 °C	SO-16 Large (Tape & Reel)	1000 parts per reel
ST202EBWR	ST232EBWR	-40 to 85 °C	SO-16 Large (Tape & Reel)	1000 parts per reel
ST202ECTR	ST232ECTR	0 to 70 °C	TSSOP16 (Tape & Reel)	2500 parts per reel
ST202EBTR	ST232EBTR	-40 to 85 °C	TSSOP16 (Tape & Reel)	2500 parts per reel

ST202E/ST232E

PIN CONFIGURATION



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	C_1+	Positive Terminal for the first Charge Pump Capacitor
2	V+	Doubled Voltage Terminal
3	C_1-	Negative Terminal for the first Charge Pump Capacitor
4	C_2+	Positive Terminal for the second Charge Pump Capacitor
5	C_2-	Negative Terminal for the second Charge Pump Capacitor
6	V-	Inverted Voltage Terminal
7	$T2_{OUT}$	Second Transmitter Output Voltage
8	$R2_{IN}$	Second Receiver Input Voltage
9	$R2_{OUT}$	Second Receiver Output Voltage
10	$T2_{IN}$	Second Transmitter Input Voltage
11	$T1_{IN}$	First Transmitter Input Voltage
12	$R1_{OUT}$	First Receiver Output Voltage
13	$R1_{IN}$	First Receiver Input Voltage
14	$T1_{OUT}$	First Transmitter Output Voltage
15	GND	Ground
16	V_{CC}	Supply Voltage

JRC **NJM2137**

ULTRA WIDE BAND, HIGH SLUE RATE DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2137 is an ultra wide band, high slew rate dual operational amplifier operated from low voltage (±1.35V).

It can apply to active filter, high speed analog and digital signal processor, line driver, HDTV, industrial measurement equipment and others.

It can also apply to portable communication items because of low operating voltage and low operating current.

■ PACKAGE OUTLINE

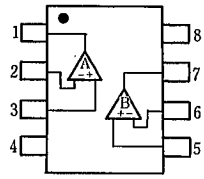
NJM2137V

NJM2137M

■ FEATURES

- Operating Voltage (±1.35V ~ ±6V)
- Ultra Wide Band (200MHz typ.)
- High Slew Rate (45V/μs typ.)
- Low Operating Current (1.14mA typ.)
- Bipolar Technology
- Package Outline SSOP8, DMP8

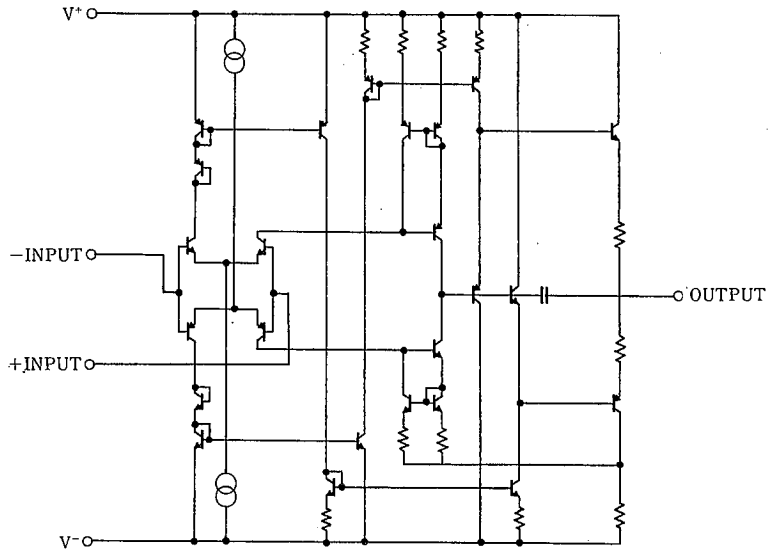
■ PIN CONFIGURATION



NJM2137M
NJM2137V

PIN FUNCTION
1. A OUTPUT
2. A −INPUT
3. A +INPUT
4. V⁻
5. B +INPUT
6. B −INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



M24C64
M24C32

64Kbit and 32Kbit Serial I²C Bus EEPROM

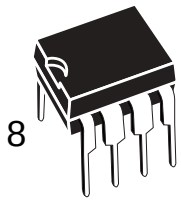
FEATURES SUMMARY

- Two-Wire I^2C Serial Interface
  Supports 400kHz Protocol
- Single Supply Voltage:
  - 4.5 to 5.5V for M24Cxx
  - 2.5 to 5.5V for M24Cxx-W
  - 1.8 to 5.5V for M24Cxx-R
- Write Control Input
- BYTE and PAGE WRITE (up to 32 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Protection
- More than 1 Million Erase/Write Cycles
- More than 40-Year Data Retention

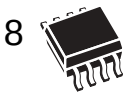
Table 1. Product List

Reference	Part Number
M24C64	M24C64
	M24C64-W
	M24C64-R
M24C32	M24C32
	M24C32-W
	M24C32-R

Figure 1. Packages



PDIP8 (BN)



SO8 (MN)
150 mil width

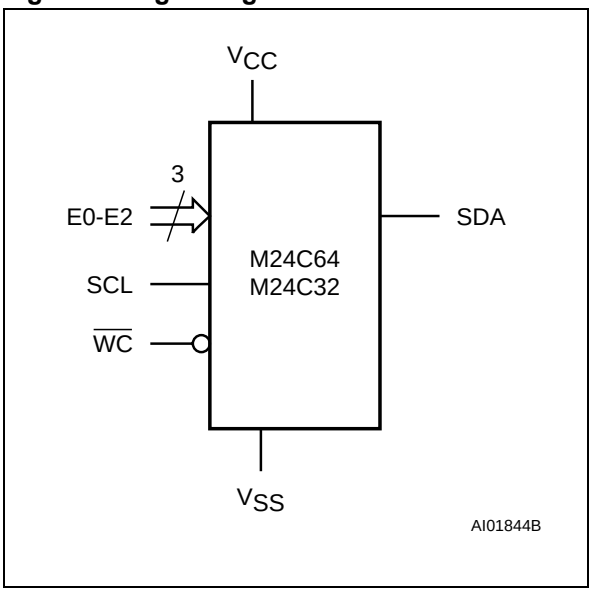
TSSOP8 (DW)
169 mil width

UFDFPN8 (MB)
2x3mm² (MLP)

SUMMARY DESCRIPTION

These I^2C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 8192 x 8 bits (M24C64) and 4096 x 8 bits (M24C32).

Figure 2. Logic Diagram



I^2C uses a two-wire serial interface, comprising a bi-directional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a Device Select Code and Read/Write bit (RW) (as described in Table 3.), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Table 2. Signal Names

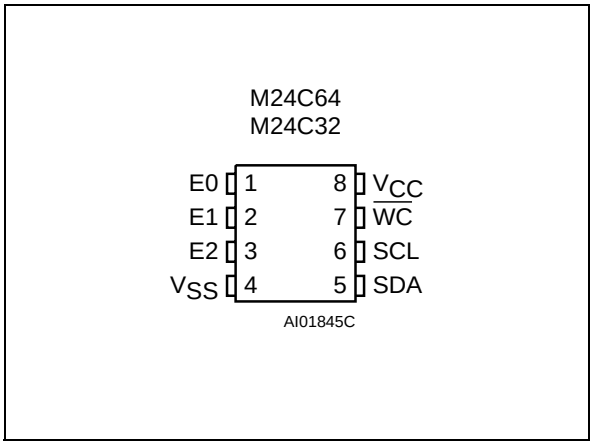
E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. At Power-up, the internal reset is held active until V_{CC} has reached the Power On Reset (POR) threshold voltage, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the Power On Reset (POR) threshold voltage, all operations are disabled and the device will not respond to any command.

A stable and valid V_{CC} (as defined in Table 9. and Table 10.) must be applied before applying any logic signal.

Figure 3. DIP, SO, TSSOP and UFDFPN Connections



Note: See PACKAGE MECHANICAL section for package dimensions, and how to identify pin-1.

KEC

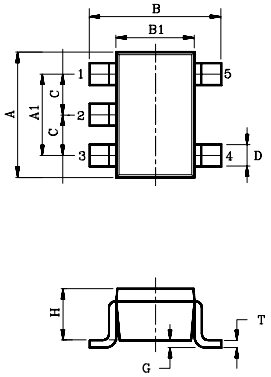
SEMICONDUCTOR
TECHNICAL DATA

KIC7SZ08FU
SILICON MONOLITHIC CMOS
DIGITAL INTEGRATED CIRCUIT

2 INPUT AND GATE

FEATURES

- High Output Drive : ±24mA (Typ.)
  @V_{CC}=3V
- Super High Speed Operation : t_{PD}=2.7ns(Typ.)
  @V_{CC}=5V, 50pF
- Operation Voltage Range : $V_{CC(opr)}$=1.8~5.5V.
- Supply Voltage Data Retention : V_{CC}=1.5~5.5V.
- 5V Tolerant Function



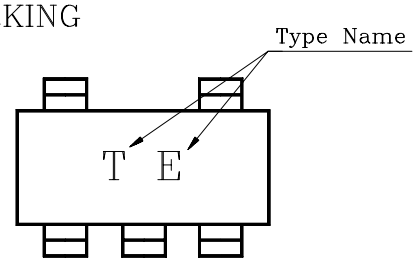
DIM	MILLIMETERS
A	2.00± 0.20
A1	1.3± 0.1
B	2.1± 0.1
B1	1.25± 0.1
C	0.65
D	0.2+0.10/−0.05
G	0~0.1
H	0.9± 0.1
T	0.15+0.1/−0.05

USV

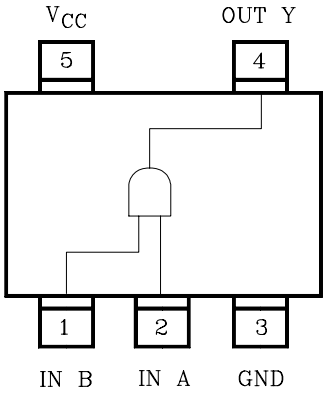
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~6	V
DC Input Voltage	V_{IN}	-0.5~6	V
DC Output Voltage	V_{OUT}	-0.5~6	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	200	mW
Storage Temperature	T_{stg}	-65~150	℃
Lead Temperature (10s)	T_L	260	℃

MARKING



PIN CONNECTION(TOP VIEW)



JRC **NJM2845/46**

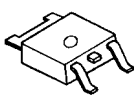
LOW DROPOUT VOLTAGE REGULATOR

■ GENERAL DESCRIPTION

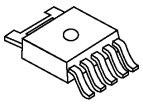
The NJM2845 is low dropout voltage regulator. Advanced Bipolar technology achieves low noise, high ripple rejection and low quiescent current.

NJM2845 is 3 terminal type and NJM2846 is ON/OFF control built in type. These product can be selected according to the applications.

■ PACKAGE OUTLINE



NJM2845DL1

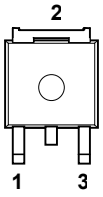


NJM2846DL3

■ FEATURES

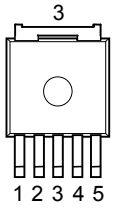
- High Ripple Rejection 75dB typ. (f=1kHz,3V Version)
- Output Noise Voltage Vno=45μVrms typ. (Vo=3V Version)
- Output capacitor with 2.2μF ceramic capacitor (Vo≥2.6V)
- Output Current Io(max.)=800mA
- High Precision Output Vo ±1.0%
- Low Dropout Voltage 0.18V typ. (Io=500mA)
- ON/OFF Control (NJM2846)
- Internal Short Circuit Current Limit
- Internal Thermal Overload Protection
- Bipolar Technology
- Package Outline TO-252-3 (NJM2845DL1), TO-252-5 (NJM2846DL3)

■ PIN CONFIGURATION



1.V_{IN}
2.GND
3.V_{OUT}

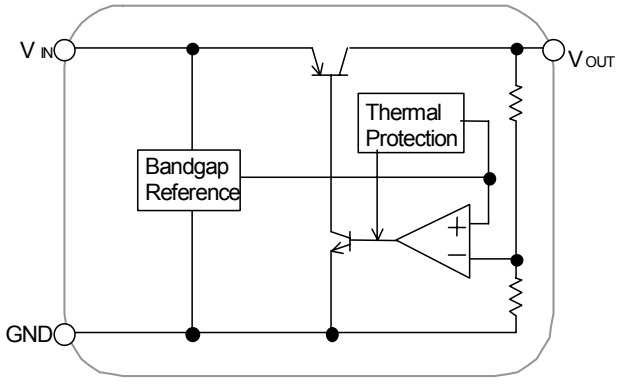
NJM2845DL1



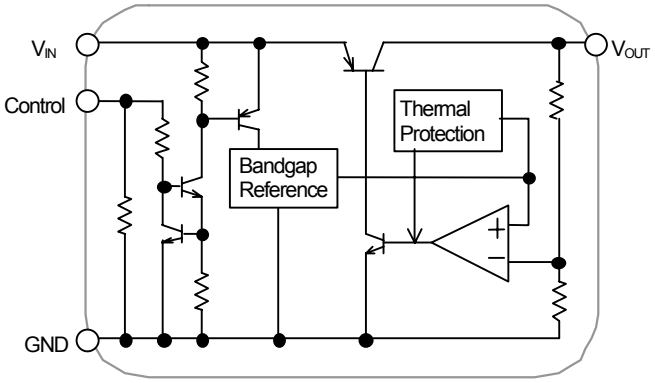
1.CONTROL
2.V_{IN}
3.GND
4.Vo
5.NC

NJM2846DL3

■ EQUIVALENT CIRCUIT



NJM2845DL1



NJM2846DL3

TOSHIBA TC74VHC157F/FN/FT

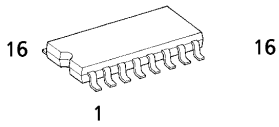
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC157F, TC74VHC157FN, TC74VHC157FT

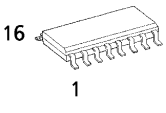
QUAD 2 - CHANNEL MULTIPLEXER

(Note) The JEDEC SOP (FN) is not available in Japan.

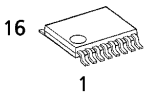
The TC74VHC157 is an advanced high speed CMOS QUAD 2 - CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
It consists of four 2 - input digital multiplexers with common select and strobe inputs.
When the $\overline{STROBE}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level.
The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.
An Input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

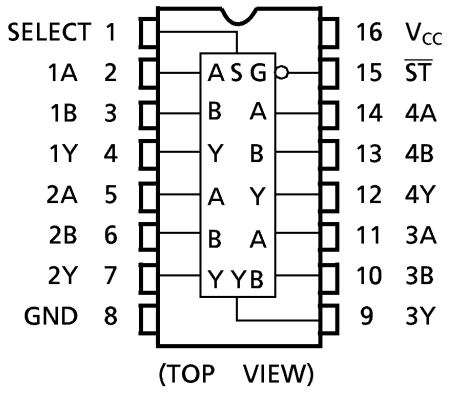


FT (TSSOP16-P-0044-0.65)
Weight : 0.06g (Typ.)

FEATURES :

- High Speed ····· t_{pd} = 4.1ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr) = 2V ~ 5.5V
- Low Noise ····· V_{OLP} = 0.8V (Max.)
- Pin and Function Compatible with 74ALS157

PIN ASSIGNMENT



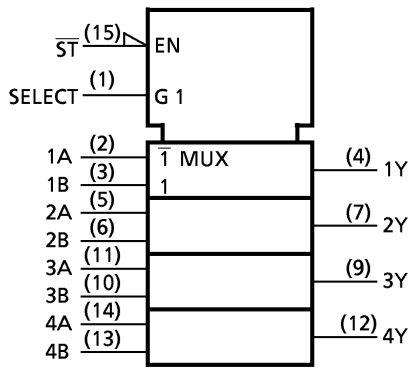
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUT
$\overline{ST}$	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

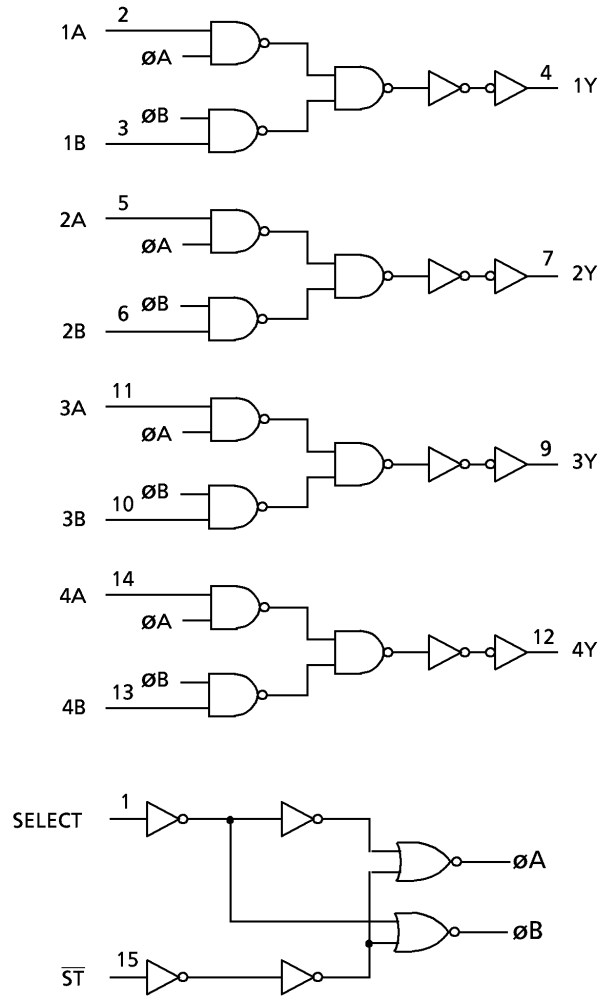
X : Don't Care

IEC LOGIC SYMBOL



980910EBA2

SYSTEM DIAGRAM



8 Mbit SPI Serial Flash
SST25VF080B

Data Sheet

FEATURES:

- **Single Voltage Read and Write Operations**
  - 2.7-3.6V
- **Serial Interface Architecture**
  - SPI Compatible: Mode 0 and Mode 3
- **High Speed Clock Frequency**
  - 50 MHz
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Read Current: 10 mA (typical)
  - Standby Current: 5 µA (typical)
- **Flexible Erase Capability**
  - Uniform 4 KByte sectors
  - Uniform 32 KByte overlay blocks
  - Uniform 64 KByte overlay blocks
- **Fast Erase and Byte-Program:**
  - Chip-Erase Time: 35 ms (typical)
  - Sector-/Block-Erase Time: 18 ms (typical)
  - Byte-Program Time: 7 µs (typical)
- **Auto Address Increment (AAI) Programming**
  - Decrease total chip programming time over Byte-Program operations
- **End-of-Write Detection**
  - Software polling the BUSY bit in Status Register
  - Busy Status readout on SO pin in AAI Mode
- **Hold Pin (HOLD#)**
  - Suspends a serial sequence to the memory without deselecting the device
- **Write Protection (WP#)**
  - Enables/Disables the Lock-Down function of the status register
- **Software Write Protection**
  - Write protection through Block-Protection bits in status register
- **Temperature Range**
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
- **Packages Available**
  - 8-lead SOIC (200 mils)
  - 8-contact WSON (6mm x 5mm)
- **All non-Pb (lead-free) devices are RoHS compliant**

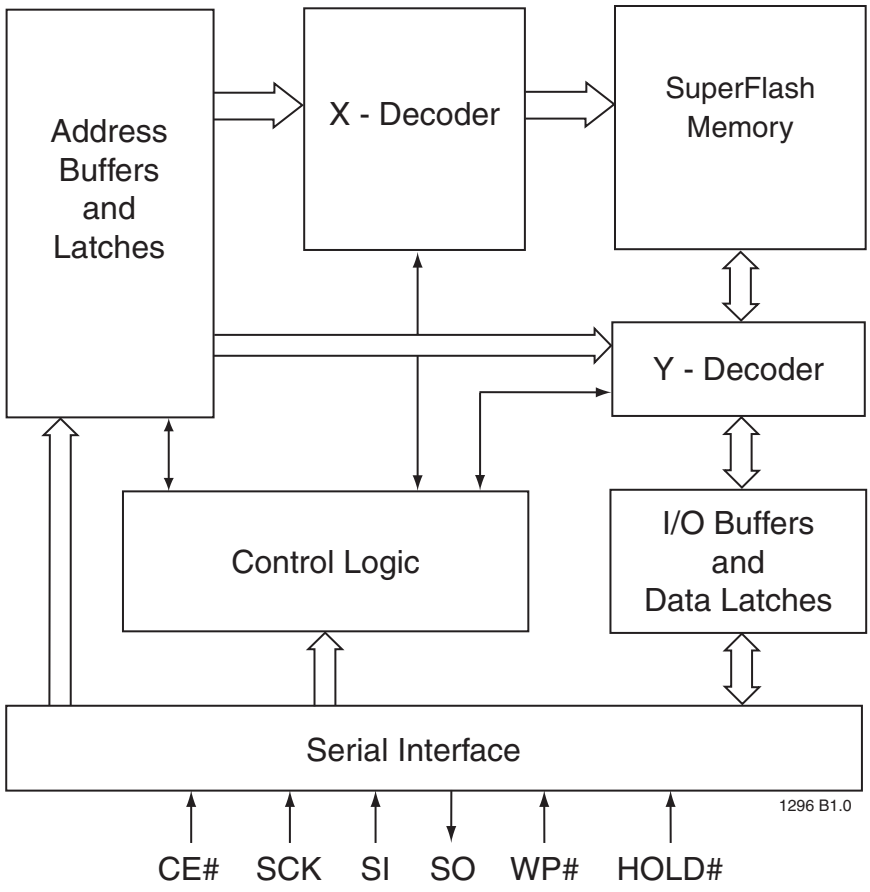
PRODUCT DESCRIPTION

SST's 25 series Serial Flash family features a four-wire, SPI-compatible interface that allows for a low pin-count package which occupies less board space and ultimately lowers total system costs. The SST25VF080B devices are enhanced with improved operating frequency and even lower power consumption than the original SST25VFxxxA devices. SST25VF080B SPI serial flash memories are manufactured with SST's proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

The SST25VF080B devices significantly improve performance and reliability, while lowering power consumption. The devices write (Program or Erase) with a single power supply of 2.7-3.6V for SST25VF080B. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies.

The SST25VF080B device is offered in both 8-lead SOIC (200 mils) and 8-contact WSON (6mm x 5mm) packages. See Figure 1 for pin assignments.

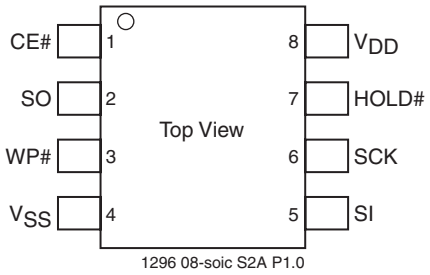
FUNCTIONAL BLOCK DIAGRAM



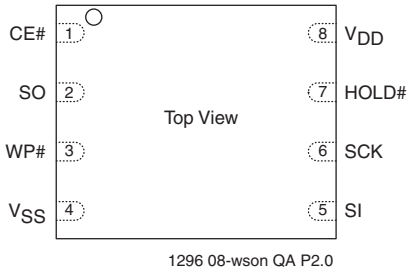
8 Mbit SPI Serial Flash
SST25VF080B

Data Sheet

PIN DESCRIPTION



8-LEAD SOIC



8-CONTACT WSON

FIGURE 1: PIN ASSIGNMENTS

TABLE 1: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. Outputs Flash busy status during AAI Programming when reconfigured as RY/BY# pin. See “Hardware End-of-Write Detection” on page 12 for details.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence.
WP#	Write Protect	The Write Protect (WP#) pin is used to enable/disable BPL bit in the status register.
HOLD#	Hold	To temporarily stop serial communication with SPI flash memory without resetting the device.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V for SST25VF080B
V_{SS}	Ground	

T1.0 1296

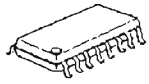
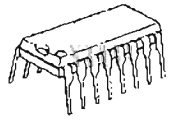
JRC **NJW1159**

2-CHANNEL ELECTRONIC VOLUME

■ GENERAL DESCRIPTION

NJW1159 is a two channel electronic volume IC. It is included output buffer amplifier and also resistor output terminal for using external amplifier to customize for your application. These functions are controlled by three-wired serial data. And the chip selector is available for using four chips on same serial bus line. It's available for two-channel stereo and or multi-channel audio volume.

■ PACKAGE OUTLINE

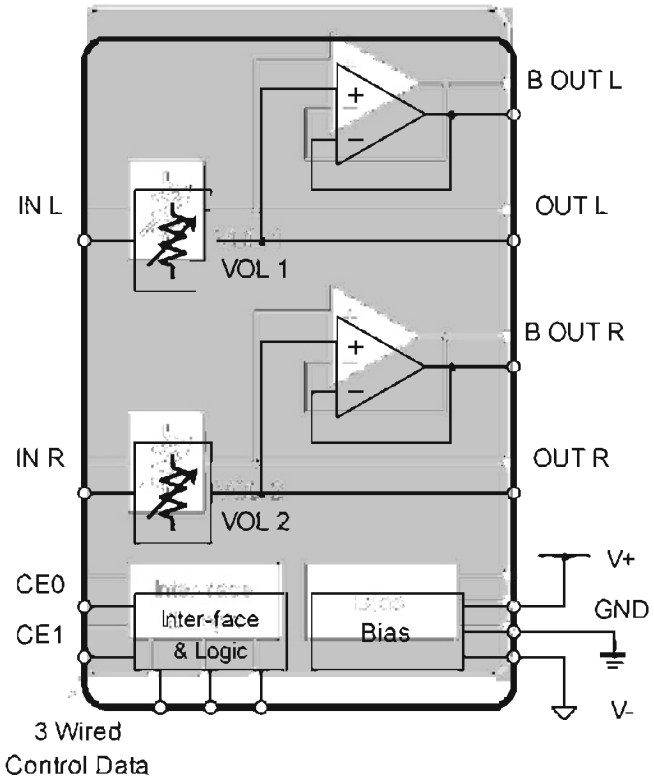




NJW1159V **NJW1159M** **NJW1159D**

■ FEATURES

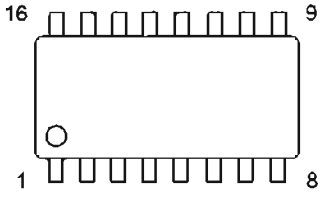
● Operating Voltage	±4.5 to ±7.5V
● Three-Wired Serial Data Control	
● Chip Selector	available for using four chips on same serial bus line.
● Volume	0 to -95dB/1dBstep, MUTE
● Bi-CMOS Technology	
● Package Outline	SSOP16, DMP16, DIP16

■ BLOCK DIAGRAM



NJW1159

■ PIN ASSIGNMENT



No.	Symbol	Function
1	OUTL	Lch External Opamp Input Connection Terminal
2	BOUTL	Lch Output
3	VDD_OUT	Internal VDD Noise Rejection Capacitor Terminal
4	BOUTR	Rch Output
5	OUTR	Rch External Opamp Input Connection Terminal
6	VSS_OUT	Internal VSS Noise Rejection Capacitor Terminal
7	V+	+ Power supply voltage input
8	V-	- Power supply voltage input
9	INL	Lch Input
10	INR	Rch Input
11	CE0	Chip Enable Terminal 0
12	CE1	Chip Enable Terminal 1
13	DATA	Control data signal input
14	CLOCK	Clock signal input
15	LACTH	Latch signal input
16	GND	Ground

■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V^+/V^-	+8/-8	V
Maximum Input Voltage	V_{IM}	$V^+/V^{-(*)}$	V
Power Dissipation	P_D	SSOP16 ; 300 DMP16 ; 300 DIP16 ; 500	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +125	°C

(*) For the maximum input voltage less than V^+/V^-

■ ELECTRICAL CHARACTERISTICS (Ta=25°C,V+/V- = +7V/-7V, R_L=47kΩ)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
◆ Power Supply						
Operating Voltage 1	V+		4.5	7.0	7.5	V
Operating Voltage 2	V-		-7.5	-7.0	-4.5	V
Supply Current 1	I_{CC}	No signal	-	4.5	9.0	mA
Supply Current 2	I_{EE}	No signal	-	4.5	9.0	mA
◆ Input/Output Characteristics (BOUTL : 2pin, BOUTR : 4pin)						
Maximum Output Voltage	V_{OM}	f=1kHz,THD=1% Volume=0dB	3.0	4.0	-	Vrms
Voltage Gain	G_V	V_{IN}=1Vrms, f=1kHz Volume=0dB	-0.5	0	0.5	dB
Channel Gain Balance 1	ΔG_{V1}	V_{IN}=1Vrms, f=1kHz Volume=0dB	-0.5	0	0.5	dB
Channel Gain Balance 2	ΔG_{V2}	V_{IN}=1Vrms, f=1kHz Volume=-60dB	-1.0	0	1.0	dB
Maximum Attenuation	A_{TT}	V_{IN}=1Vrms, f=1kHz Volume=-95dB, A-weight	-	-95	-	dB
Mute Level	Mute	V_{IN}=1Vrms, f=1kHz Volume=Mute, A-weight	-	-110	-	dB
Output Noise Voltage	V_{NO}	Volume=0dB, Rg=0Ω, A-weight	-	-105 (5.6μ)	-95 (17.8μ)	dBV (Vrms)
Total Harmonic Distortion	THD	Vo=1Vrms, f=1kHz, Volume=0dB, BW=400-30kHz	-	0.005	0.05	%
Channel Separation	CS	Vo=1Vrms, f=1kHz, A-weight Volume=0dB, Rg=0Ω	-	-100	-90	dB

CMOS 16-Bit Microcontrollers

T5CC1

1. Outline and Features

T5CC1 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

T5CC1 comes in a 100-pin flat package.

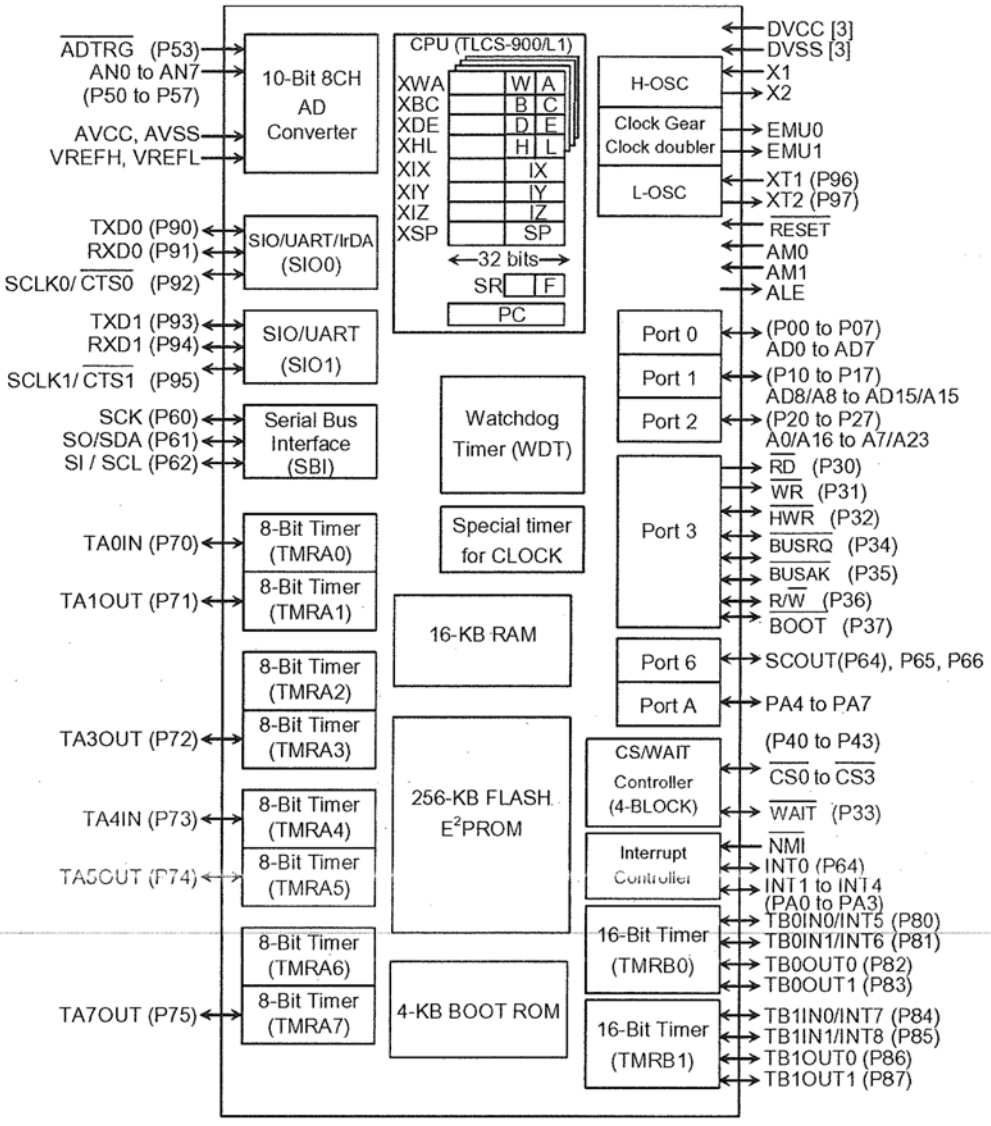
Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)

- Instruction mnemonics are upward-compatible with TLCS-90/900
- General-purpose registers and register banks
- 16 Mbytes of linear address space
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: 4-channels (593 ns/2 bytes at 27 MHz)

(2) Minimum instruction execution time: 148 ns (at 27 MHz)

(3) Built-in RAM: 16 Kbytes
Built-in ROM: 256 Kbytes Flash memory
4 Kbytes mask ROM (used for booting)



( ): Initial function after reset

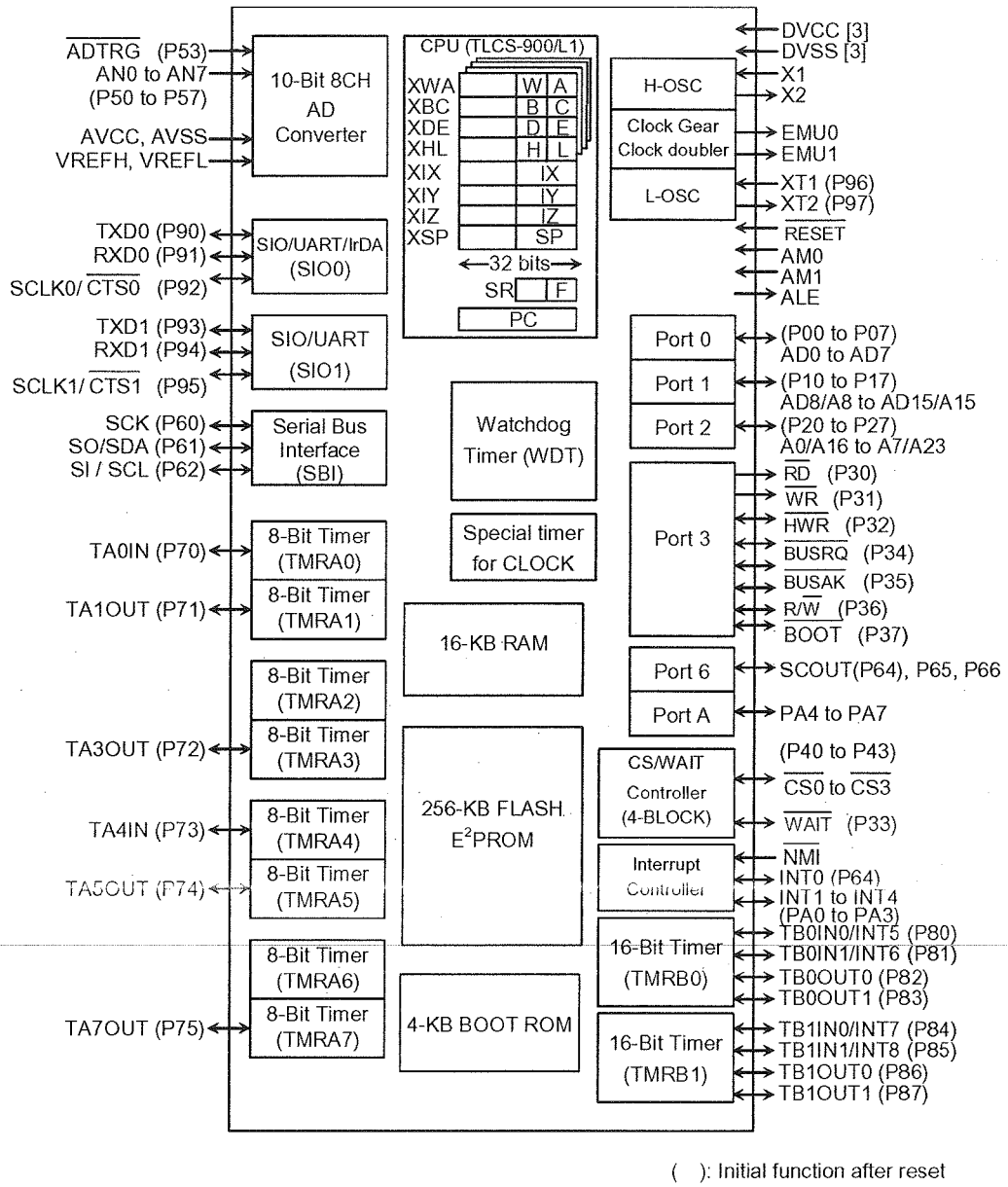


Figure 1.1 T5CC1 Block Diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the T5CC1, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the T5CC1.

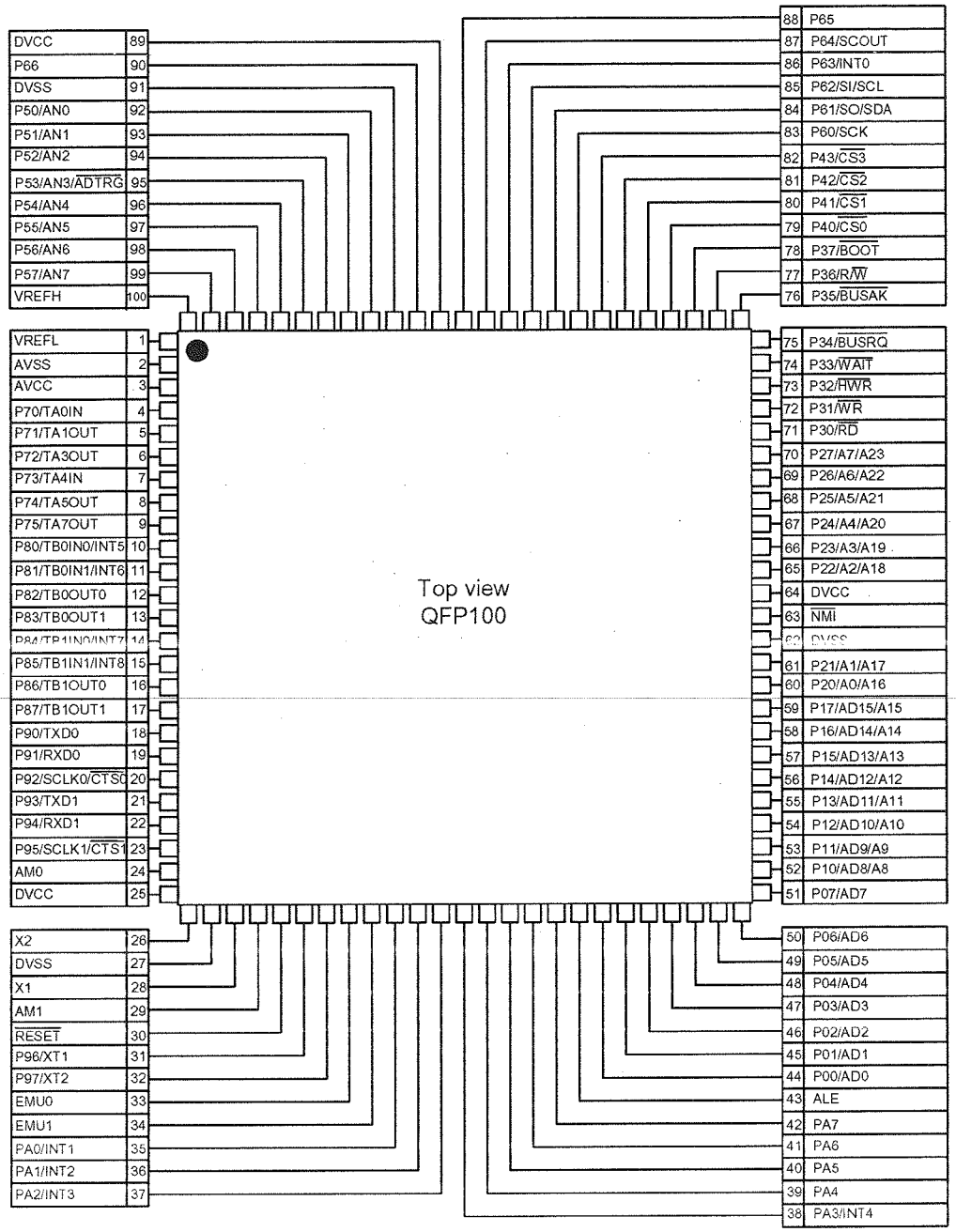


Figure 2.1.1 Pin assignment diagram (100-pin LQFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.
Table 2.2.1 Pin names and functions.

Table 2.2.1 Pin names and functions (1/3)

Pin Name	Number of Pins	I/O	Functions
P00~P07 AD0~AD7	8	I/O I/O	Port 0: I/O port that allows I/O to be selected at the bit level Address and data (lower): Bits 0 to 7 of address and data bus
P10~P17 AD8~AD15 A8~A15	8	I/O I/O Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 of address bus
P20~P27 A0~A7 A16~A23	8	I/O Output Output	Port 2: I/O port that allows I/O to be selected at the bit level Address: Bits 0 to 7 of address bus Address: Bits 16 to 23 of address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory This port output RD signal also case of reading internal-area by setting P3 <P30> = 0 and P3FC <P30F> = 1.
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data to pins AD0 to AD7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High Write: Strobe signal for writing data to pins AD8 to AD15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait ((1+N) WAIT mode)
P34 BUSRQ	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus Request: Signal used to request Bus Release
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus Acknowledge: Signal used to acknowledge Bus Release
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/Write: 1 represents Read or Dummy cycle; 0 represents Write cycle.
P37 $\overline{BOOT}$	1	I/O Input	Port 36: I/O port (with pull-up resistor) This pin sets single boot mode. When released reset, Single boot mode is started at P37=Low level.
P40 $\overline{CS0}$	1	I/O Output	Port 40: I/O port (with pull-up resistor) Chip Select 0: Outputs 0 when address is within specified address area
P41 $\overline{CS1}$	1	I/O Output	Port 41: I/O port (with pull-up resistor) Chip Select 1: Outputs 0 if address is within specified address area
P42 $\overline{CS2}$	1	I/O Output	Port 42: I/O port (with pull-up resistor) Chip Select 2: Outputs 0 if address is within specified address area
P43 $\overline{CS3}$	1	I/O Output	Port 43: I/O port (with pull-up resistor) Chip Select 3: Outputs 0 if address is within specified address area
P50~P57 AN0~AN7 $\overline{ADTRG}$	8	Input Input Input	Port 5: Pin used to input port Analog input: Pin used to input to AD converter AD Trigger: Signal used to request start of AD converter (Shared with53 pin)

Table 2.2.1 Pin names and functions (2/3)

Pin Name	Number of Pins	I/O	Functions
P60 SCK	1	I/O I/O	Port 60: I/O port Serial bus interface clock in SIO Mode
P61 SO SDA	1	I/O Output I/O	Port 61: I/O port Serial bus interface send data at SIO mode Serial bus interface send/recive data at I^2C bus mode Open-drain output mode by programmable
P62 SI SCL	1	I/O Input I/O	Port 62: I/O port Serial bus interface recive data at SIO mode Serial bus interface clock I/O data at I^2C bus mode Open-drain output mode by programmable
P63 INT0	1	I/O Input	Port 63: I/O port Interrupt Request Pin 0: Interrupt request pin with programmable level / rising edge / falling edge
P64 SCOUT	1	I/O Output	Port 64: I/O port System Clock Output: Outputs f_{FPH} or fs clock.
P65	1	I/O	Port 65 I/O port
P66	1	I/O	Port 66 I/O port
P70 TA0IN	1	I/O Input	Port 70I/O port 8bitt timer 0 input:: Timer 0 input
P71 TA1OUT	1	I/O Output	Port 71I/O port 8-bit timer 1 output: Timer 0 or Timer 1 output
P72 TA3OUT	1	I/O Output	Port 72I/O port 8bit 8-bit timer 3 output: Timer 2 or Timer 3 output
P73 TA4IN	1	I/O Input	Port 73: I/O port 8-bit timer 4 input: Timer 4 input
P74 TA5OUT	1	I/O Output	Port 74: I/O port 8-bit timer 5 output: Timer 4 or Timer 5 output
P75 TA7OUT	1	I/O Output	Port 75: I/O port 88-bit timer 7 output: Timer 6 or Timer 7 output
P80 TB0IN0 INT5	1	I/O Input Input	Port 80: I/O port 16bit timer 0 input 0: 16bit Timer 0 count / capture trigger input Interrupt Request Pin 5: Interrupt request pin with programmable rising edge / falling edge.
P81 TB0IN1 INT6	1	I/O Input Input	Port 81: I/O port 16bit timer 0 input 1: 16bit Timer 0 count / capture trigger input Interrupt Request Pin 6: Interrupt request on rising edge
P82 TB0OUT0	1	I/O Output	Port 82: I/O port 16bit timer 0 output 0: 16bit Timer 0 output
P83 TB0OUT1	1	I/O Output	Port 83: I/O port 16bit timer 0 output 1: 16bit Timer 0 output
P84 TB1IN0 INT7	1	I/O Input Input	Port 84: I/O port 16bit timer 1 input 0: 16bit Timer 1 count / capture trigger input Interrupt Request Pin 7: Interrupt request pin with programmable rising edge / falling edge.
P85 TB1IN1 INT8	1	I/O Input Input	Port 85: I/O port 16bit timer 1 input 1: 16bit Timer 1 count / capture trigger input Interrupt Request Pin 8: Interrupt request on rising edge
P86 TB1OUT0	1	I/O Output	Port 86: I/O port 16bit timer 1 output 0: 16bit Timer 1 output 16bit
P87 TB1OUT1	1	I/O Output	Port 87: I/O port 16bit timer 1 output 1: 16bit Timer 1 output 16bit 16bit

Table 2.2.1 Pin names and functions (3/3)

Pin Name	Number of Pins	I/O	Functions
P90 TXD0	1	I/O Output	Port 90: I/O port Serial Send Data 0 (programmable open-drain)
P91 RXD0	1	I/O Input	Port 91: I/O port Serial Receive Data 0
P92 SCLK0 $\overline{\text{CTS0}}$	1	I/O I/O Input	Port 92: I/O port Serial Clock I/O 0 Serial Data Send Enable 0 (Clear to Send)
P93 TXD1	1	I/O Output	Port 93: I/O port Serial Send Data 1 (programmable open-drain)
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial Receive Data 1
P95 SCLK1 $\overline{\text{CTS1}}$	1	I/O I/O Input	Port 95: I/O port (with pull-up resistor) Serial Clock I/O 1 Serial Data Send Enable 1 (Clear to Send)
P96 XT1	1	I/O Input	Port 96: I/O port (open-drain output) Low-frequency oscillator connection pin
P97 XT2	1	I/O Output	Port 97: I/O port (open-drain output) Low-frequency oscillator connection pin
PA0~PA3 INT1~INT4	4	I/O Input	Ports A0 to A3: I/O ports Interrupt Request Pins 1 to 4: Interrupt request pins with programmable rising edge / falling edge.
PA4~PA7	4	I/O	Ports A4 to A7: I/O ports
ALE	1	Output	Address Latch Enable Can be disabled to reduce noise.
$\overline{\text{NMI}}$	1	Input	Non-Maskable Interrupt Request Pin: Interrupt request pin with programmable falling edge or both edge.
AM0~1	2	Input	Operation mode: Fixed to AM1 = 1, AM0 = 1
EMU0	1	Output	Open pin
EMU1	1	Output	Open pin
$\overline{\text{RESET}}$	1	Input	Reset: initializes T5CC1. (With pull-up resistor)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)
X1/X2	2	I/O	High-frequency oscillator connection pins
DVCC	3		Power supply pins (All DVCC pins should be connected with the power supply pin.)
DVSS	3		GND pins (0 V) (All DVSS pins should be connected with the power supply pin.)

Note: An external DMA controller cannot access the device's built-in memory or built-in I/O devices using the $\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$ signal.

JRC **NJM2595**

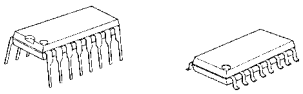
5-INPUT 3-OUTPUT VIDEO SWITCH

■ GENERAL DESCRIPTION

The **NJM2595** is a 5-input 3-output video switch. Its switches select one from five signals received from VTR,TV,DVD, TV-GAME and others.

The NJM2595 is designed for audio items, such as AV amplifier and others.

■ PACKAGE OUTLINE

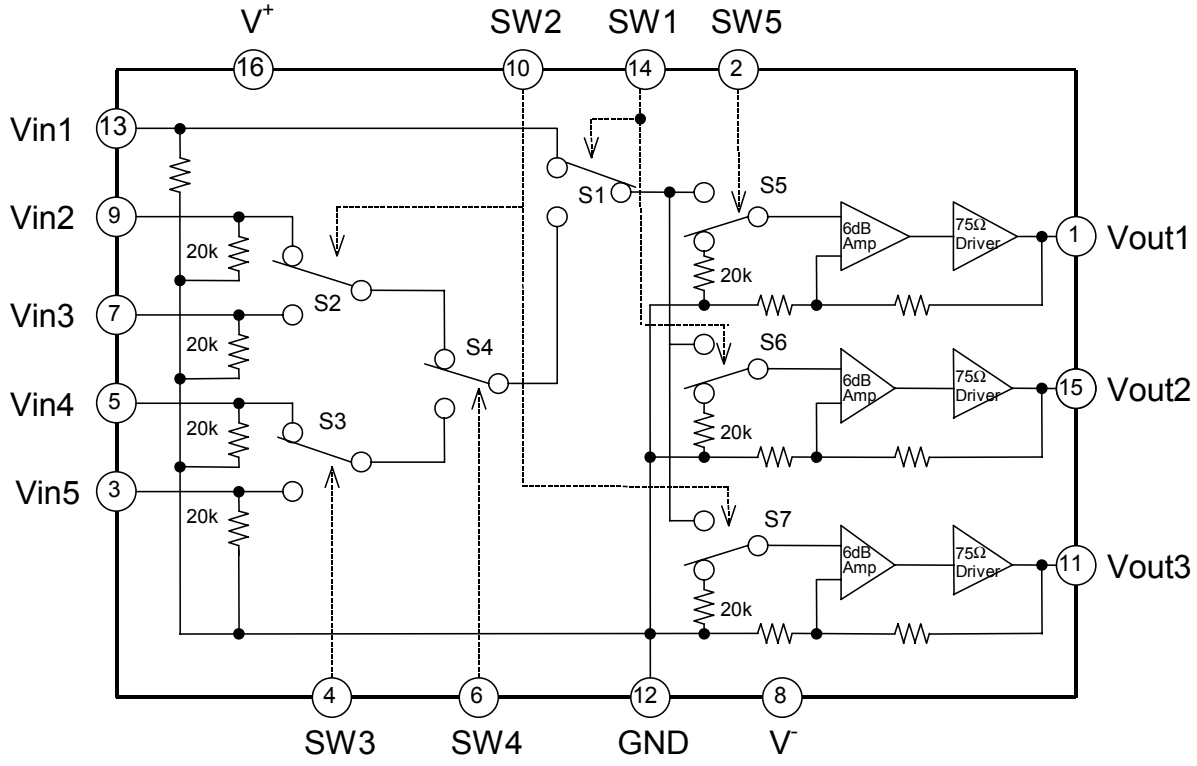


NJM2595D **NJM2595M**

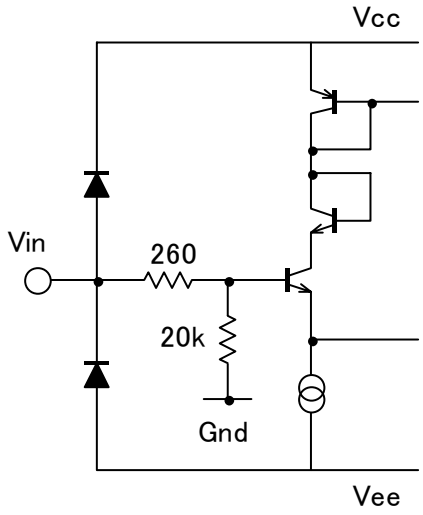
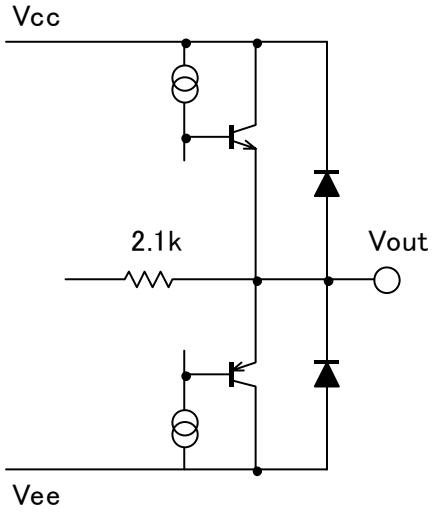
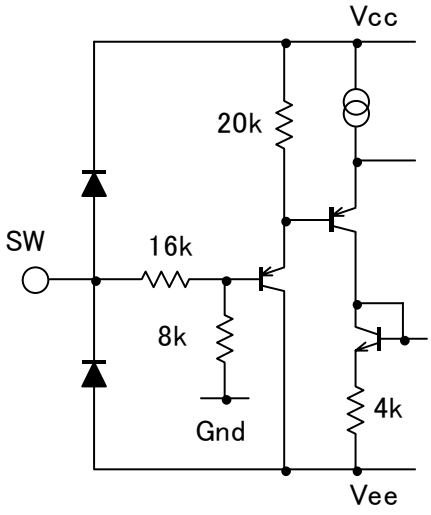
■ FEATURES

- 5-input 3-output
- Operating Voltage ±4.0 to ±6.5V
- Operating current ±15mAtyp. at Vcc=±5V
- Crosstalk -65dBtyp.
- Internal 6dB Amplifier
- Internal 75Ω Driver
- Bipolar Technology
- Package Outline DIP16,DMP16

■ PIN CONFIGURATION and BLOCK DIAGRAM

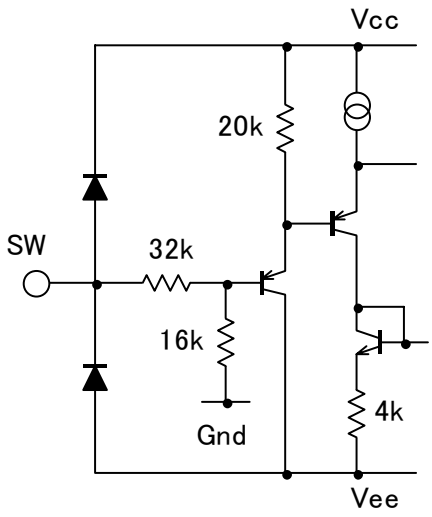


■ **EQUIVALENT CIRCUIT**

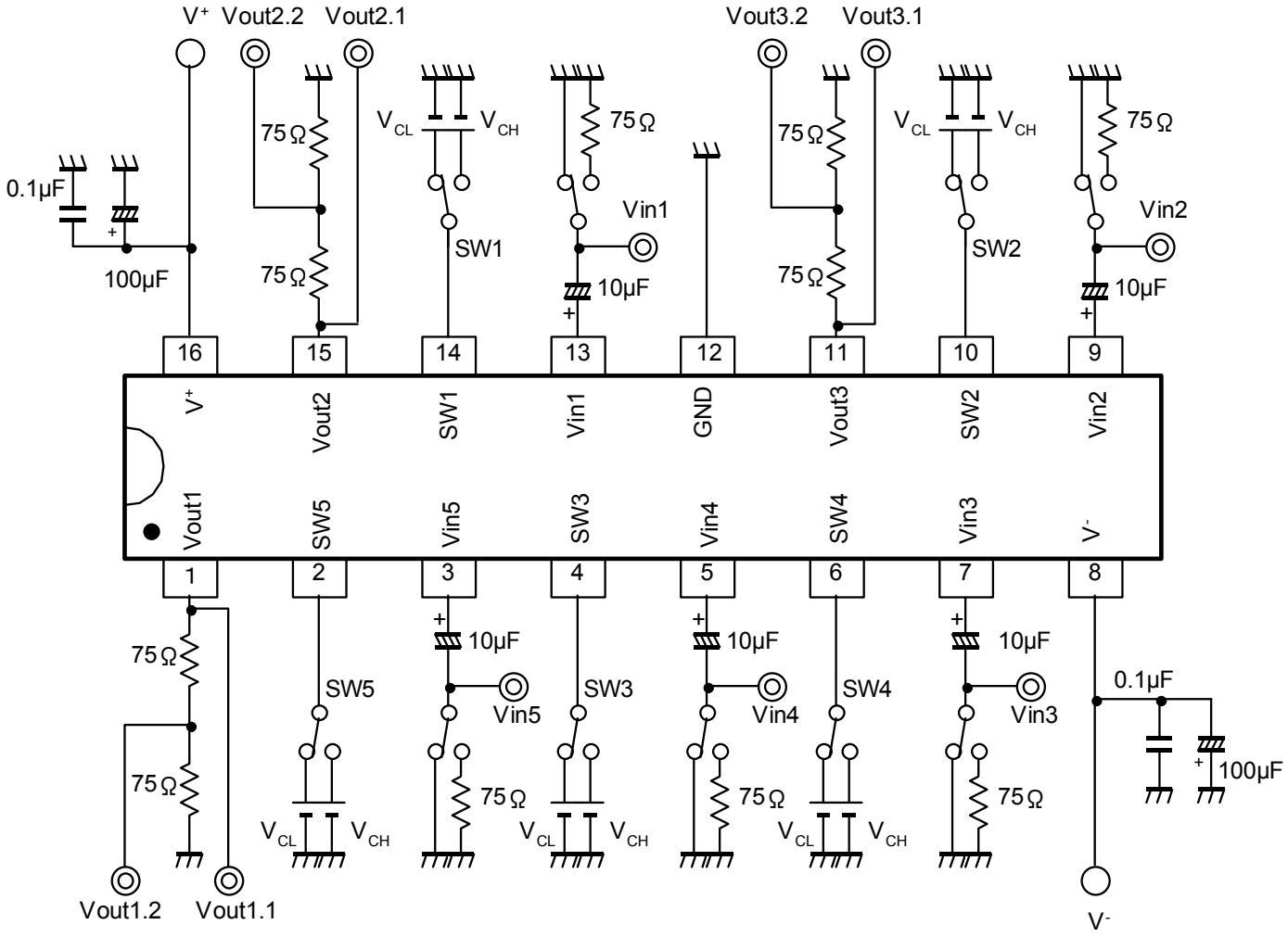
PIN No.	PIN NAME	INSIDE EQUIVALENT CIRCUIT	VOLTAGE
16	V^+		5V
8	V^-		-5V
12	GND		-
13 9 7 5 3	Vin1 Vin2 Vin3 Vin4 Vin5		0V
1 15 11	Vout1 Vout2 Vout3		0V
4 6 2	SW3 SW4 SW5		-

NJM2595

■ EQUIVALENT CIRCUIT

PIN No.	PIN NAME	INSIDE EQUIVALENT CIRCUIT	VOLTAGE
14 10	SW1 SW2		-

■ TEST CIRCUIT



JRC

NJM2068M (OP - AMP)

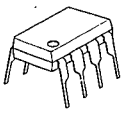
NJM2068

LOW-NOISE DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2068 is a high performance, low noise dual operational amplifier. This amplifier features popular pin-out, superior noise performance, and superior total harmonic distortion. This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product and slew rate which far exceeds that of the 4558 type amplifier. The specially designed low noise input transistors allow the NJM2068 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifier.

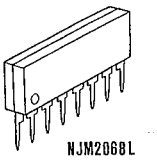
■ PACKAGE OUTLINE



NJM2068D

NJM2068M

NJM2068V



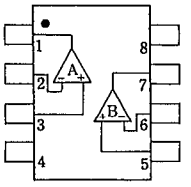
NJM2068L

■ FEATURES

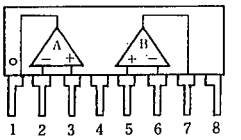
- Operating Voltage (±4V～±18V)
- Low Total Harmonic Distortion (0.001% typ.)
- Low Noise Voltage (FLAT+JISA, 0.56 μV typ.)
- High Slew Rate (6V/μs typ.)
- Unity Gain Bandwidth (27MHz @f=10kHz)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

4

■ PIN CONFIGURATION



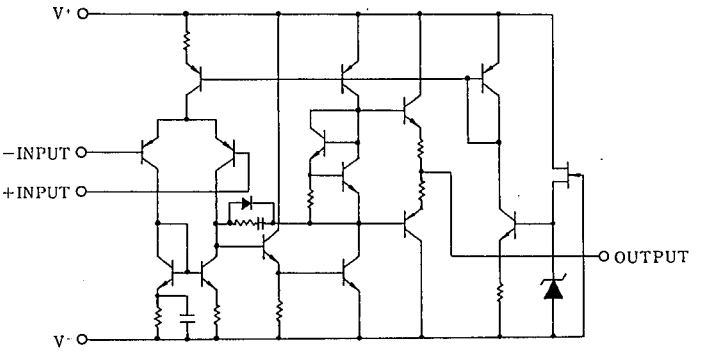
NJM2068D
NJM2068M
NJM2068V



NJM2068L

PIN FUNCITON
1. A OUTPUT
2. A−INPUT
3. A+INPUT
4. V⁻
5. B+INPUT
6. B−INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



JRC

IC86

NJM4556A

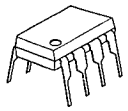
DUAL HIGH CURRENT OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM4556A integrated circuit is a high-gain, high output current dual operational amplifier capable of driving ±70mA into 150 Ω loads (±10.5V output voltage), and operating low supply voltage (V^+/V^-=±2V~).

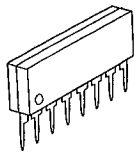
The NJM4556A combines many of the fetures of the popular NJM4558 as well as having the capability of driving 150Ω loads. In addition, the wide band-width, low noise, high slew rate and low distortion of the NJM4556A make it ideal for many audio, telecommunications and instrumentation applications.

■ PACKAGE OUTLINE

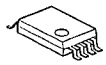


NJM4556AD

NJM4556AM



NJM4556AL

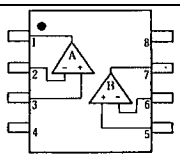


NJM4556AV

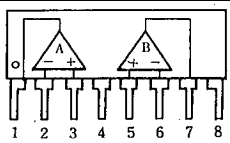
■ FEATURES

- Operating Voltage (±2V~±18V)
- High Output Current (Io=70mA)
- Slew Rate (3V/μs typ.)
- Gain Band Width Product (8MHz typ.)
- Package Outline DIP8, DMP8, SIP8, SSOP8
- Bipolar Technology

■ PIN CONFIGURATION



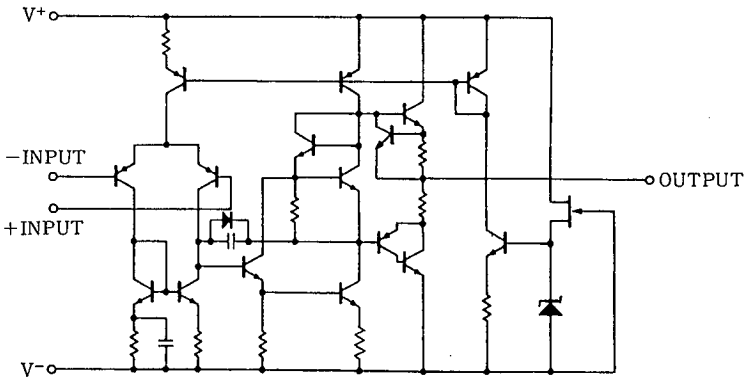
NJM4556AD
NJM4556AM
NJM4556AV



NJM4556AL

PIN FUNCTION
1. A OUTPUT
2. A−INPUT
3. A+INPUT
4. V⁻
5. B+INPUT
6. B−INPUT
7. B OUTPUT
8. V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



TOSHIBA TC74HCU04AP/AF/AFN

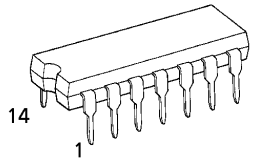
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HCU04AP, TC74HCU04AF, TC74HCU04AFN

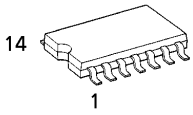
HEX INVERTER

(Note) The JEDEC SOP (FN) is not available in Japan.

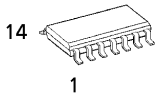
The TC74HCU04A is a high speed CMOS INVERTER fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Since the internal circit is composed of a single stage inverter, it can be used in analog applications such as crystal oscllators.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)



F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

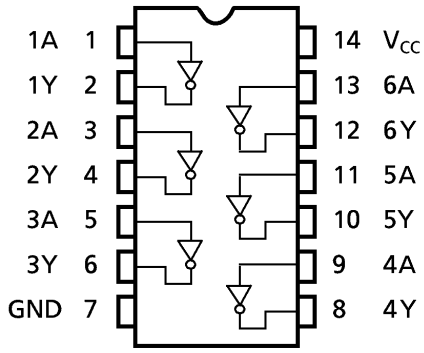


FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

FEATURES :

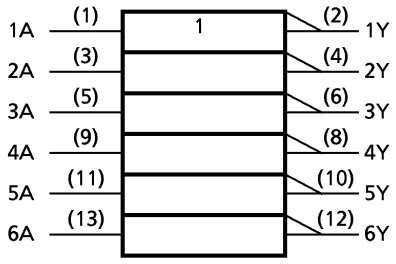
- High Speed ····· t_{pd} = 4ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 1 μA(Max.) at Ta = 25°C
- High Noise Immunity ····· V_{NIH} = V_{NIH} = 10% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$ = I_{OL} = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ·· V_{CC}(opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS04

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

961001EBA2

AK4384

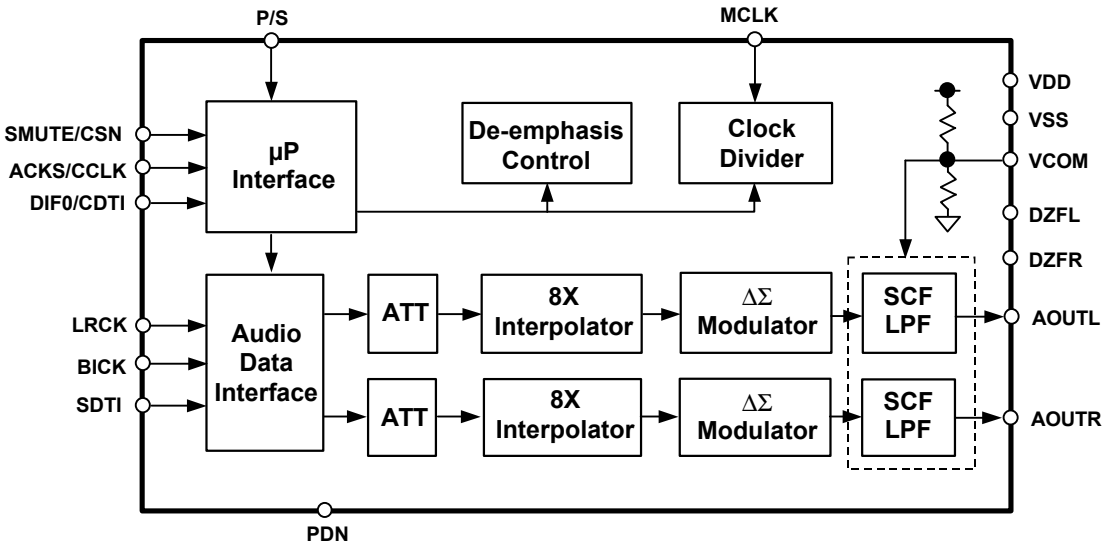
106dB 192kHz 24-Bit 2ch ΔΣ DAC

GENERAL DESCRIPTION

The AK4384 offers the perfect mix for cost and performance based audio systems. Using AKM's multi bit architecture for its modulator the AK4384 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4384 integrates a combination of SCF and CTF filters increasing performance for systems with excessive clock jitter. The 24 Bit word length and 192kHz sampling rate make this part ideal for a wide range of applications including DVD-Audio. The AK4384 is offered in a space saving 16pin TSSOP package.

FEATURES

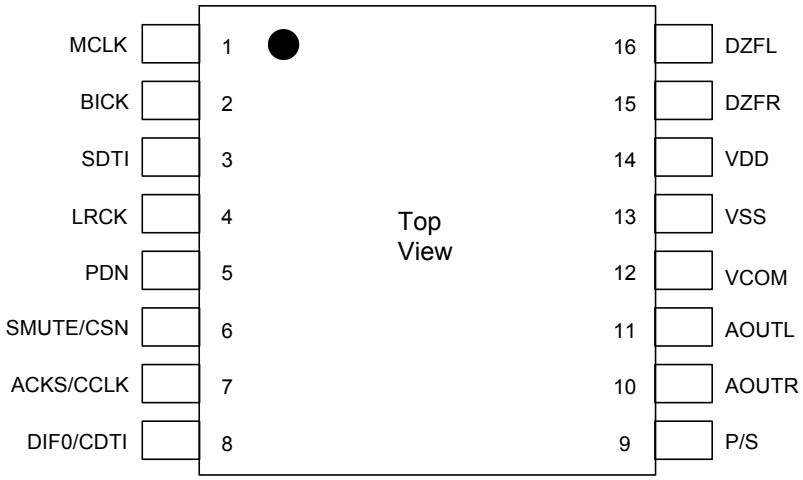
- ☐ Sampling Rate Ranging from 8kHz to 192kHz
- ☐ 128 times Oversampling (Normal Speed Mode)
- ☐ 64 times Oversampling (Double Speed Mode)
- ☐ 32 times Oversampling (Quad Speed Mode)
- ☐ 24-Bit 8 times FIR Digital Filter
- ☐ SCF with High Tolerance to Clock Jitter
- ☐ 2nd order Analog LPF
- ☐ Single Ended Output Buffer
- ☐ Digital de-emphasis for 32k, 44.1k and 48kHz sampling
- ☐ Soft mute
- ☐ Digital Attenuator (Linear 256 steps)
- ☐ I/F format: 24-Bit MSB justified, 24/20/16-Bit LSB justified or I^2S
- ☐ Master clock: 256fs, 384fs, 512fs, 768fs or 1152fs (Normal Speed Mode)
  128fs, 192fs, 256fs or 384fs (Double Speed Mode)
  128fs, 192fs (Quad Speed Mode)
- ☐ THD+N: -94dB
- ☐ Dynamic Range: 106dB
- ☐ Power supply: 4.5 to 5.5V
- ☐ Very Small Package: 16pin TSSOP (6.4mm x 5.0mm)



■ Ordering Guide

AK4384VT	-40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4384	Evaluation Board for AK4384	

■ Pin Layout



PIN/FUNCTION

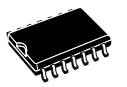
No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin
5	PDN	I	Power-Down Mode Pin When at "L", the AK4384 is in the power-down mode and is held in reset. The AK4384 should always be reset upon power-up.
6	SMUTE	I	Soft Mute Pin in parallel mode "H": Enable, "L": Disable
	CSN	I	Chip Select Pin in serial mode
7	ACKS	I	Auto Setting Mode Pin in parallel mode "L": Manual Setting Mode, "H": Auto Setting Mode
	CCLK	I	Control Data Clock Pin in serial mode
8	DIF0	I	Audio Data Interface Format Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial mode
9	P/S	I	Parallel/Serial Select Pin (Internal pull-up pin) "L": Serial control mode, "H": Parallel control mode
10	AOUTR	O	Rch Analog Output Pin
11	AOUTL	O	Lch Analog Output Pin
12	VCOM	O	Common Voltage Pin, VDD/2 Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
13	VSS	-	Ground Pin
14	VDD	-	Power Supply Pin
15	DZFR	O	Rch Data Zero Input Detect Pin
16	DZFL	O	Lch Data Zero Input Detect Pin

Note: All input pins except pull-up pin should not be left floating.

74LCX32

LOW VOLTAGE CMOS QUAD 2-INPUT OR GATE WITH 5V TOLERANT INPUTS

- 5V TOLERANT INPUTS
- HIGH SPEED:
  t_{PD} = 5.2ns (MAX.) at V_{CC} = 3V
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24mA (MIN) at V_{CC} = 3V
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2.0V to 3.6V (1.5V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 32
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:
  HBM > 2000V (MIL STD 883 method 3015);
  MM > 200V



SOP

TSSOP

Table 1: Order Codes

PACKAGE	T & R
SOP	74LCX32MTR
TSSOP	74LCX32TTR

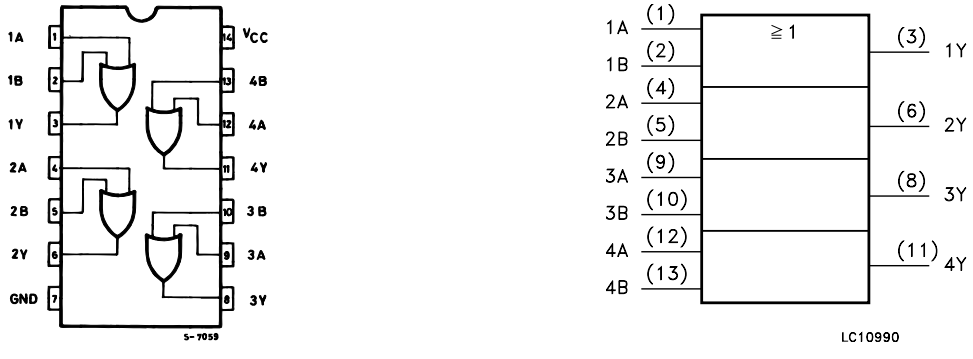
DESCRIPTION

The 74LCX32 is a low voltage CMOS QUAD 2-INPUT OR GATE fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for inputs.

It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols



74LCX32

Figure 2: Input And Output Equivalent Circuit

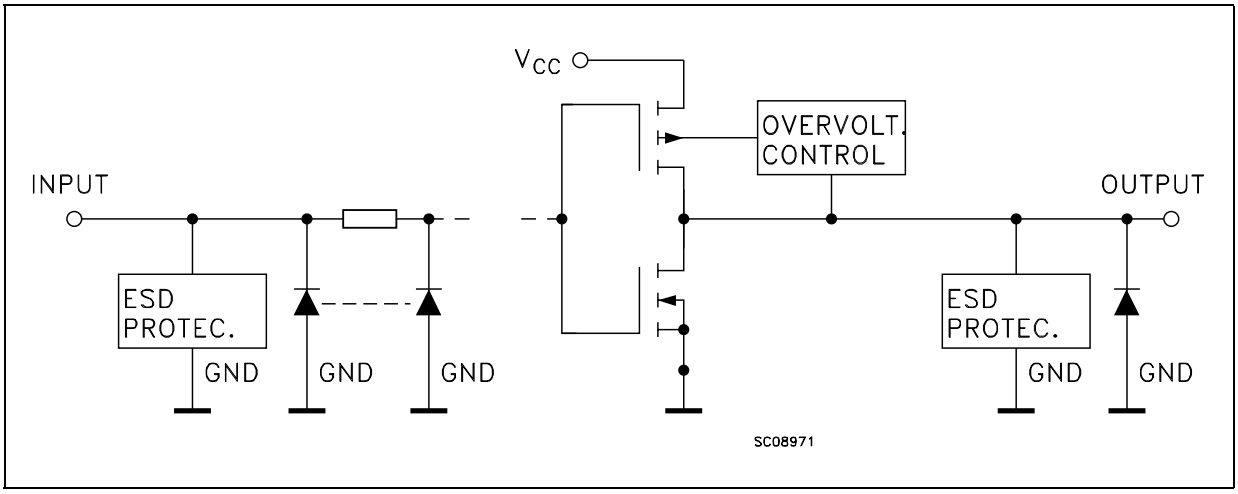


Table 2: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

Table 3: Truth Table

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

Table 4: Absolute Maximum Ratings

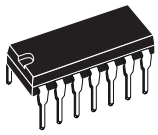
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (V_{CC} = 0V)	-0.5 to +7.0	V
V_O	DC Output Voltage (High or Low State) (note 1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current	± 50	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Supply Pin	± 100	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
1) I_O absolute maximum rating must be observed
2) V_O < GND

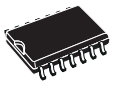
74ACT04

HEX INVERTER

- HIGH SPEED: t_{PD} = 5.0ns (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION: I_{CC} = 2µA(MAX.) at T_A=25°C
- COMPATIBLE WITH TTL OUTPUTS V_{IH} = 2V (MIN.), V_{IL} = 0.8V (MAX.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE: $|I_{OH}| = I_{OL}$ = 24mA (MIN)
- BALANCED PROPAGATION DELAYS: $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE: V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 04
- IMPROVED LATCH-UP IMMUNITY



DIP



SOP

TSSOP

ORDER CODES

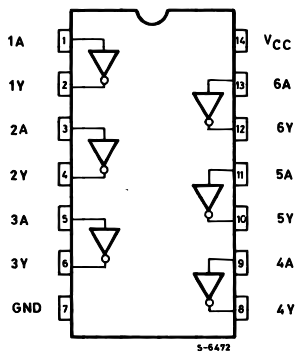
PACKAGE	TUBE	T & R
DIP	74ACT04B	
SOP	74ACT04M	74ACT04MTR
TSSOP		74ACT04TTR

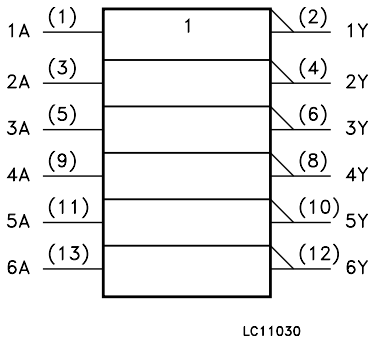
DESCRIPTION

The 74ACT04 is an advanced high-speed CMOS HEX INVERTER fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.
The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels.
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

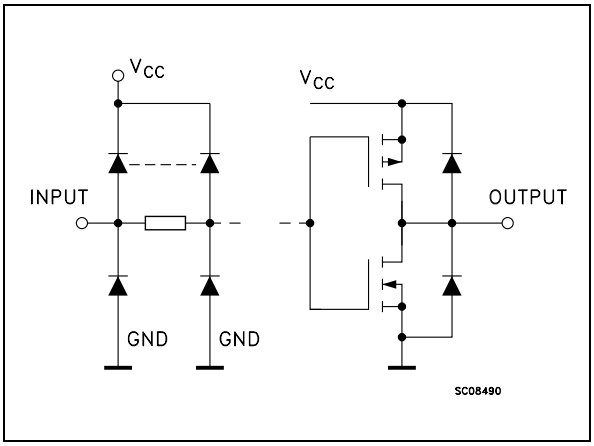
PIN CONNECTION AND IEC LOGIC SYMBOLS





74ACT04

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	Data Inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 200	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time V_{CC} = 4.5 to 5.5V (note 1)	8	ns/V

1) V_{IN} from 0.8V to 2.0V

CIRRUS LOGIC
Leading the Digital Entertainment Revolution™

CS42528

114 dB, 192 kHz 8-Ch Codec with S/PDIF Receiver

Features

- Eight 24-bit D/A, two 24-bit A/D Converters
- 114 dB DAC / 114 dB ADC Dynamic Range
- -100 dB THD+N
- System Sampling Rates up to 192 kHz
- S/PDIF Receiver Compatible with EIAJ CP1201 and IEC-60958
- Recovered S/PDIF Clock or System Clock Selection
- 8:2 S/PDIF Input MUX
- ADC High-pass Filter for DC Offset Calibration
- Expandable ADC Channels and One-line Mode Support
- Digital Output Volume Control with Soft Ramp
- Digital +/-15dB Input Gain Adjust for ADC
- Differential Analog Architecture
- Supports logic levels between 5 V and 1.8 V.

General Description

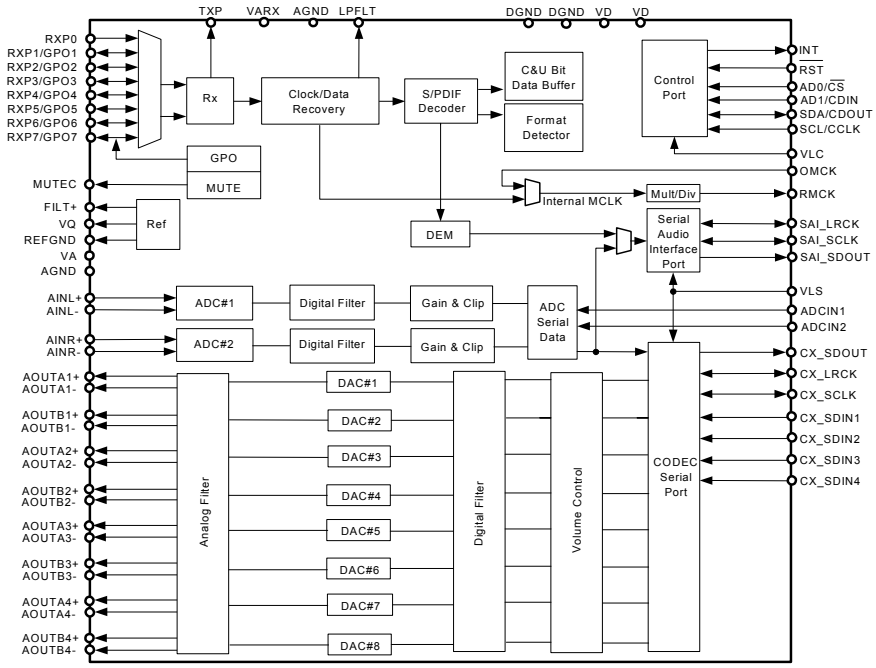
The CS42528 codec provides two analog-to-digital and eight digital-to-analog delta-sigma converters, as well as an integrated S/PDIF receiver, in a 64-pin LQFP package.

The CS42528 integrated S/PDIF receiver supports up to eight inputs, clock recovery circuitry and format auto-detection. The internal stereo ADC is capable of independent channel gain control for single-ended or differential analog inputs. All eight channels of DAC provide digital volume control and differential analog outputs. The general purpose outputs may be driven high or low, or mapped to a variety of DAC mute controls or ADC overflow indicators.

The CS42528 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as A/V receivers, DVD receivers, digital speaker and automotive audio systems.

ORDERING INFORMATION

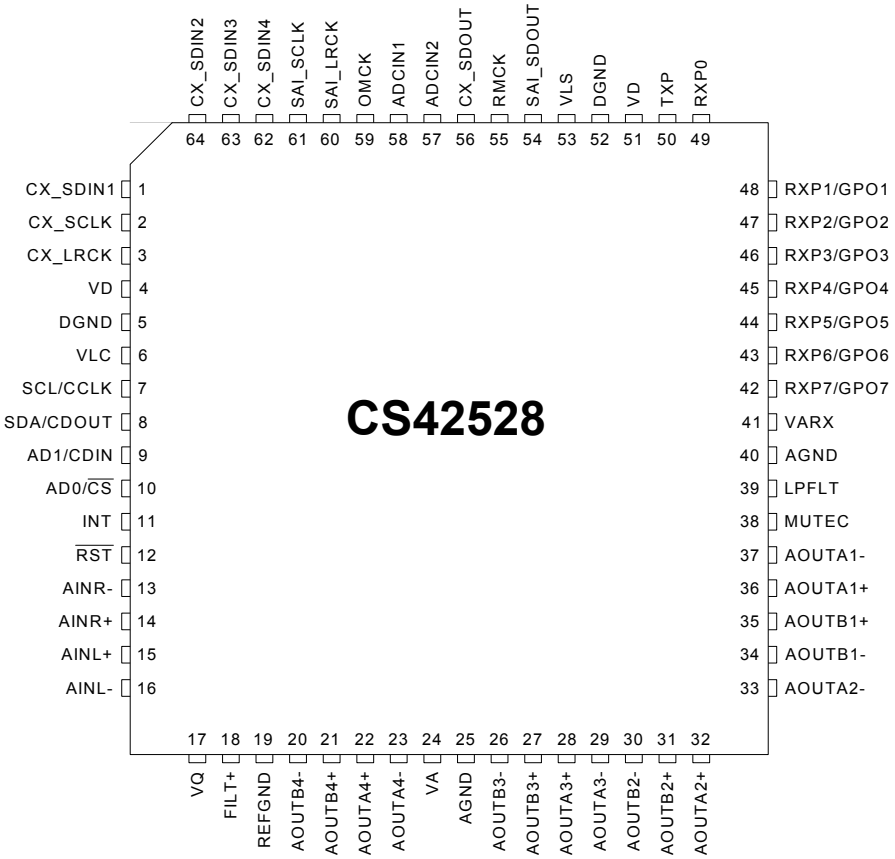
CS42528-CQZ	-10° to 70° C	64-pin LQFP	Lead Free
CS42528-DQZ	-40° to 85° C	64-pin LQFP	Lead Free
CDB42528	Evaluation Board		



Preliminary Product Information

Cirrus Logic, Inc.
http://www.cirrus.com

2. PIN DESCRIPTIONS

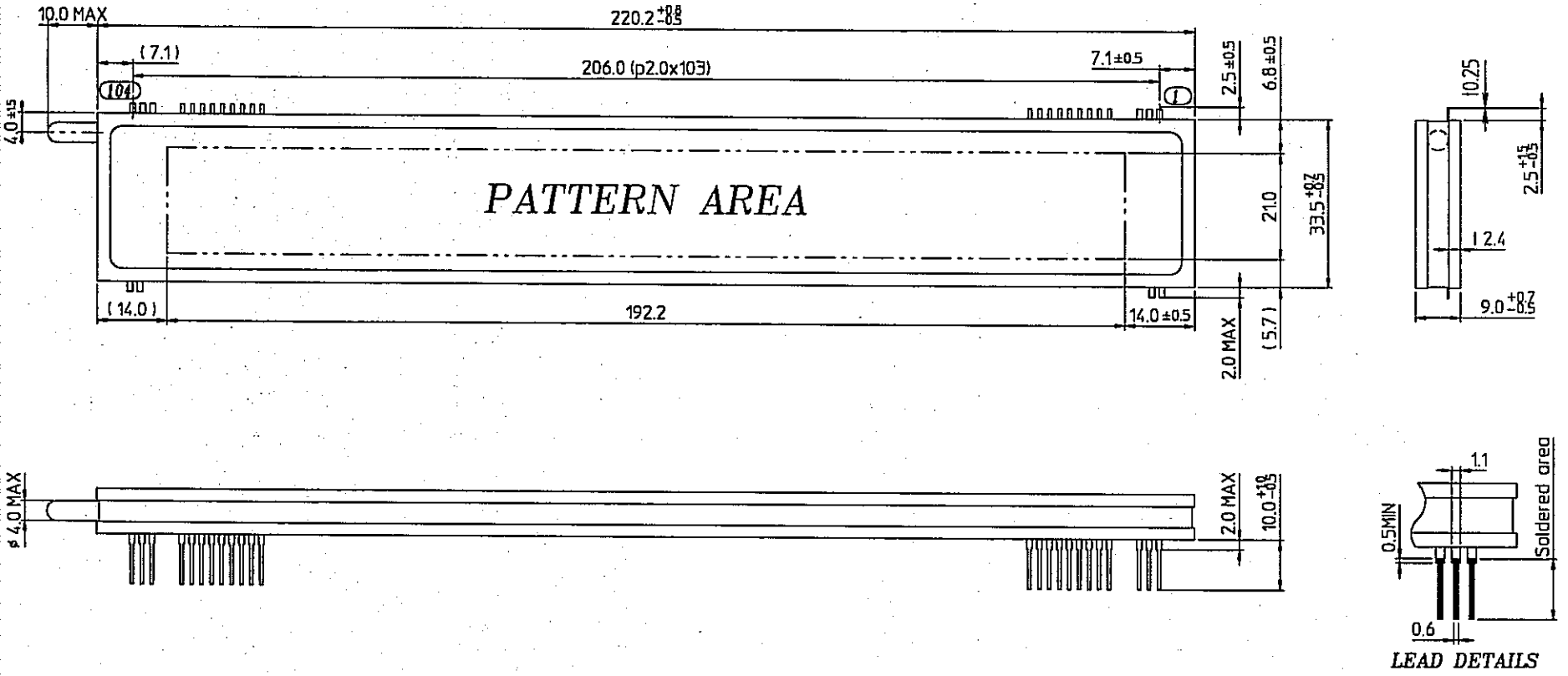


Pin Name	#	Pin Description
CX_SDIN1 **CX_SDIN2** **CX_SDIN3** **CX_SDIN4**	1 64 63 62	**Codec Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
CX_SCLK	2	**CODEC Serial Clock** *(Input/Output)* - Serial clock for the CODEC serial audio interface.
CX_LRCK	3	**CODEC Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the CODEC serial audio data line.
VD	4 51	**Digital Power** (*Input*) - Positive power supply for the digital section.
DGND	5 52	**Digital Ground** (*Input*) - Ground reference. Should be connected to digital ground.
VLC	6	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port.
SCL/CCLK	7	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I^2C mode as shown in the Typical Connection Diagram.
SDA/CDOUT	8	**Serial Control Data** (*Input/Output*) **-** SDA is a data I/O line in I^2C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDOUT is the output data line for the control port interface in SPI mode.
AD1/CDIN	9	**Address Bit 1 (I^2C)/Serial Control Data (SPI)** (*Input*) - AD1 is a chip address pin in I^2C mode; CDIN is the input data line for the control port interface in SPI mode.

AD0/$\overline{CS}$	10	**Address Bit 0 (I^2C)/Control Port Chip Select (SPI)** *(Input)* **-** AD0 is a chip address pin in I^2C mode; $\overline{CS}$ is the chip select signal in SPI mode.
INT	11	**Interrupt** *(Output)* - The CS42528 will generate an interrupt condition as per the Interrupt Mask register. See “Interrupts” on page 40 for more details.
$\overline{RST}$	12	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
AINR- **AINR+**	13 14	**Differential Right Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
AINL+ **AINL-**	15 16	**Differential Left Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins.
VQ	17	**Quiescent Voltage** (*Output*) **-** Filter connection for internal quiescent reference voltage.
FILT+	18	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
REFGND	19	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
AOUTA1 +,- **AOUTB1 +,-** **AOUTA2 +,-** **AOUTB2 +,-** **AOUTA3 +,-** **AOUTB3 +,-** **AOUTA4 +,-** **AOUTB4 +,-**	36,37 35,34 32,33 31,30 28,29 27,26 22,23 21,20	**Differential Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
VA **VARX**	24 41	**Analog Power** (*Input*) - Positive power supply for the analog section.
AGND	25 40	**Analog Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MUTEC	38	**Mute Control** (*Output*) - The Mute Control pin outputs high impedance following an initial power-on condition or whenever the PDN bit is set to a ‘1’, forcing the codec into power-down mode. The signal will remain in a high impedance state as long as the part is in power-down mode. The Mute Control pin goes to the selected “active” state during reset, muting, or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
LPFLT	39	**PLL Loop Filter** (*Output*) - An RC network should be connected between this pin and ground.
RXP7/GPO7 **RXP6/GPO6** **RXP5/GPO5** **RXP4/GPO4** **RXP3/GPO3** **RXP2/GPO2** **RXP1/GPO1**	42 43 44 45 46 47 48	**S/PDIF Receiver Input/ General Purpose Output** (*Input/Output*) - Receiver inputs for S/PDIF encoded data. The CS42528 has an internal 8:2 multiplexer to select the active receiver port, according to the Receiver Mode Control 2 register. These pins can also be configured as general purpose output pins, ADC Overflow indicators or Mute Control outputs according to the RXP/General Purpose Pin Control registers.
RXP0	49	**S/PDIF Receiver Input** (*Input*) - Dedicated receiver input for S/PDIF encoded data.
TXP	50	**S/PDIF Transmitter Output** (*Output*) - S/PDIF encoded data output, mapped directly from one of the receiver inputs as indicated by the Receiver Mode Control 2 register.
VLS	53	**Serial Port Interface Power** (*Input*) - Determines the required signal level for the serial port interfaces.
SAI_SDOUT	54	**Serial Audio Interface Serial Data Output** (*Output*) - Output for two’s complement serial audio PCM data from the S/PDIF incoming stream. This pin can also be configured to transmit the output of the internal and external ADCs.
RMCK	55	**Recovered Master Clock** (*Output*) - Recovered master clock output from the External Clock Reference (OMCK, pin 59) or the PLL which is locked to the incoming S/PDIF stream or CX_LRCK.

CX_SDOUT	56	**CODEC Serial Data Output** (*Output*) - Output for two's complement serial audio data from the internal and external ADCs.
ADCIN1 **ADCIN2**	58 57	**External ADC Serial Input** (*Input*) - The CS42528 provides for up to two external stereo analog to digital converter inputs to provide a maximum of six channels on one serial data output line when the CS42528 is placed in One Line mode.
OMCK	59	**External Reference Clock** (*Input*) - External clock reference that must be within the ranges specified in the register "OMCK Frequency (OMCK Freqx)" on page 54.
SAI_LRCK	60	**Serial Audio Interface Left/Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SAI_SCLK	61	**Serial Audio Interface Serial Clock** *(Input/Output)* - Serial clock for the Serial Audio Interface.

OUTER DIMENSIONS



LEAD DETAILS

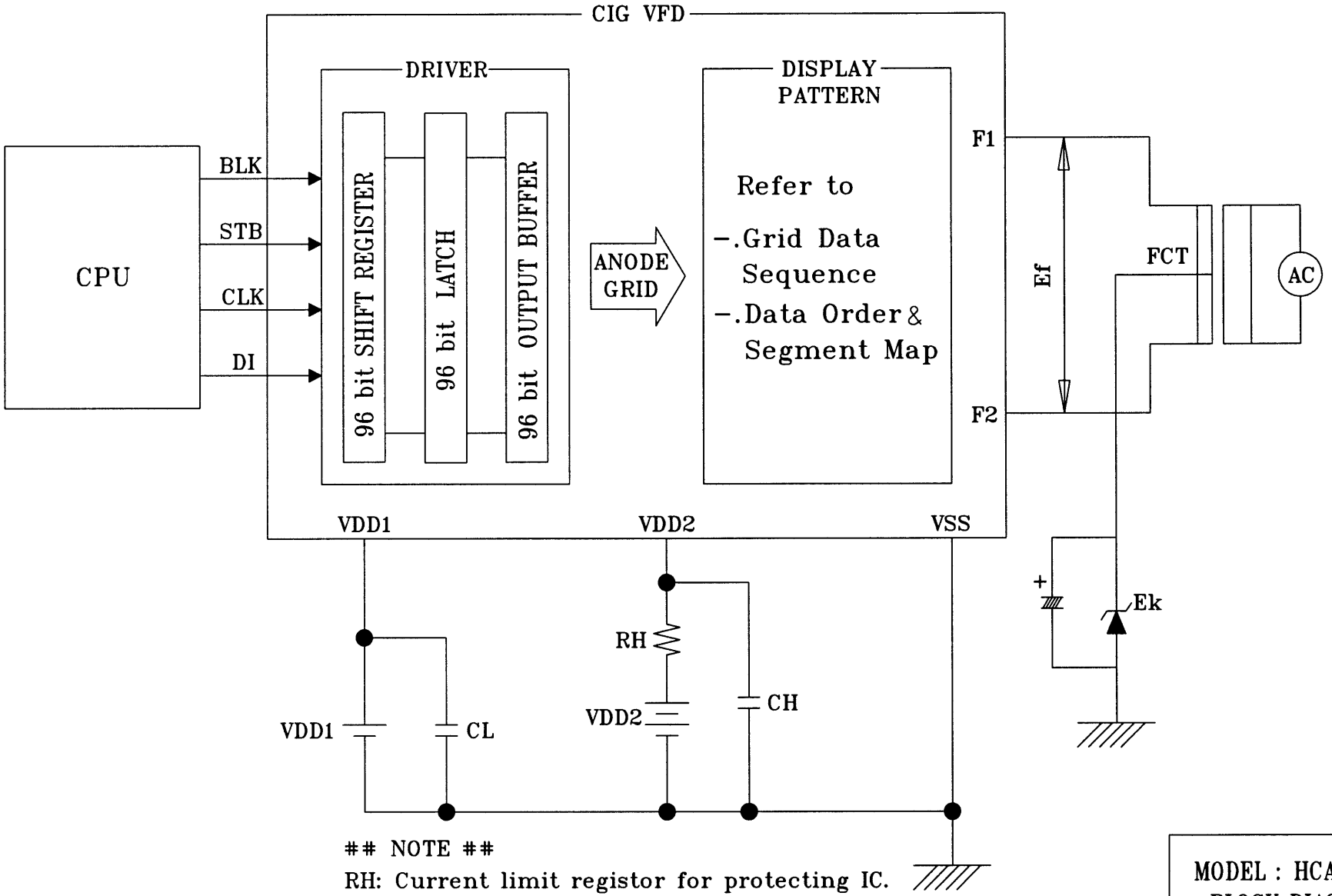
PIN CONNECTION

PIN NO.	104	103	102	101	100	99	98	97	96	95	94	93	92	91	90~15	14~6	5	4	3	2	1
CONNECTION	F2	F2	F2	NP	NP	V_{DISP}	L-GND	D-GND	V_{DD}	OSCO	/RST	/CS	/CP	DA	NP	NC	NP	NP	F1	F1	F1

*Notes
Fn : Filament Pin
NP : No Pin
NC : No Connection Pin

MODEL : HCA-18ML03
OUTER DIMENSIONS
Rev.(1) 20-Jan-2005

BLOCK DIAGRAM



NOTE

RH: Current limit registor for protecting IC.

CH,CL: Low pass filter for noise filtering.

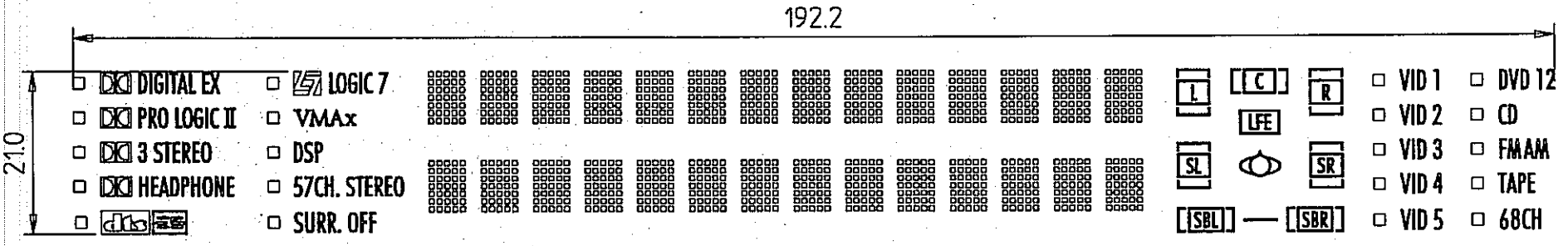
RH: 22Ω, CH: 0.1μF, CL: 0.1μF

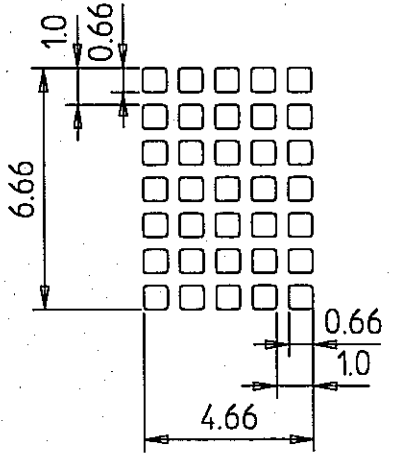
FCT: Filament is center-tab grounded.

MODEL : HCA-18ML01
BLOCK DIAGRAM
Rev. ① 20-Feb-2003

PATTERN DETAILS

SAMSUNG SDI





◎ Color of Illumination ◎

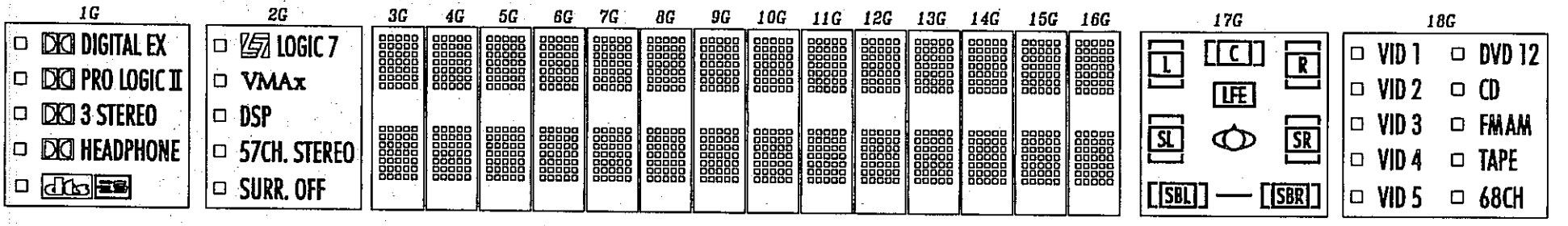
· Green (G. x=0.250, y=0.439) --- All patterns.

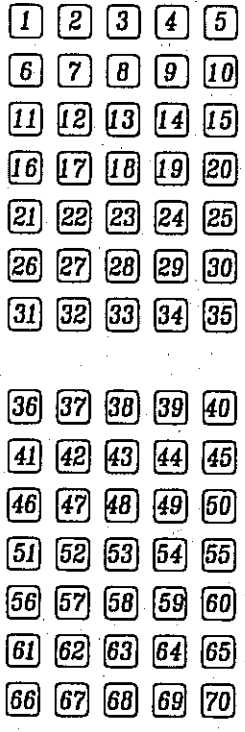
◎ Negative Patterns --- dts

MODEL : HCA-18ML03
PATTERN DETAILS
Rev. (1) 20-Jan-2005

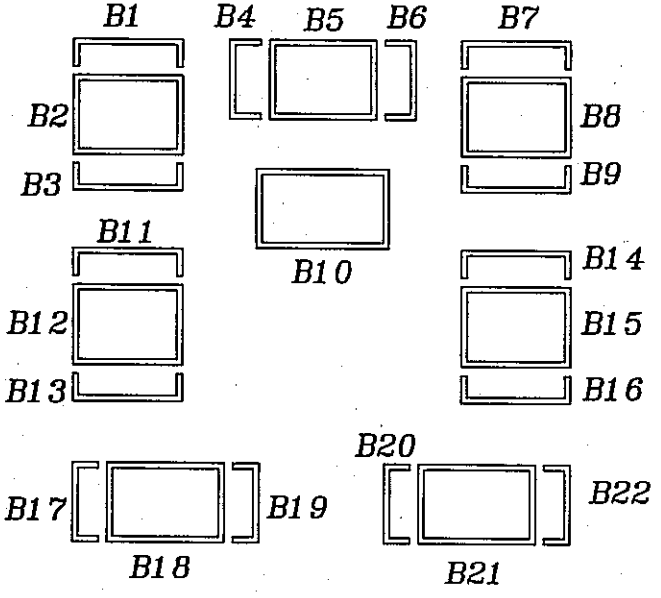
GRID ASSIGNMENT

SAMSUNG SDI





(3G-16G)



(17G)

MODEL : HCA-18ML03
GRID ASSIGNMENT
Rev.① 20-Jan-2005

ANODE CONNECTION

SAMSUNG SDI

	COM1	COM2	COM3	~	COM16	COM17	COM18
	1G	2G	3G	~	16G	17G	18G
SEGB 1	□(DIGITAL EX)	□(LOGIC 7)	1	1	1	B1	□(VID 1)
SEGB 2			2	2	2	B2	VID1
SEGB 3			3	3	3	L	□(DVD 12)
SEGB 4			4	4	4	B3	DVD
SEGB 5			5	5	5	B4	1
SEGB 6	DIGITAL	LOGIC7	6	6	6	B5	2
SEGB 7			7	7	7	C	□(VID 2)
SEGB 8			8	8	8	B6	VID2
SEGB 9			9	9	9	B7	□(CD)
SEGB10			10	10	10	B8	CD
SEGB11	EX	□(VMAx)	11	11	11	R	□(VID 3)
SEGB12			12	12	12	B9	VID3
SEGB13			13	13	13	B10	□(FM AM)
SEGB14			14	14	14	LFE	FM
SEGB15			15	15	15	B11	AM
SEGB16	□(PRO LOGIC)	VMAx	16	16	16	B12	□(VID 4)
SEGB17			17	17	17	SL	VID4
SEGB18			18	18	18	B13	□(TAPE)
SEGB19			19	19	19		TAPE
SEGB20			20	20	20	B14	□(VID 5)
SEGB21	PRO LOGIC	□(DSP)	21	21	21	B15	VID5
SEGB22			22	22	22	SR	□(6&8CH)
SEGB23			23	23	23	B16	6
SEGB24			24	24	24	B17	8
SEGB25			25	25	25	B18	CH
SEGB26	II	DSP	26	26	26	SBL	
SEGB27			27	27	27	B19	
SEGB28			28	28	28	—	
SEGB29			29	29	29	B20	
SEGB30			30	30	30	B21	
SEGB31	□(3 STEREO)	□(5&7CH.)	31	31	31	SBR	
SEGB32			32	32	32	B22	
SEGB33			33	33	33		
SEGB34			34	34	34		
SEGB35			35	35	35		

	COM1	COM2	COM3	~	COM16	COM17	COM18
	1G	2G	3G	~	16G	17G	18G
SEGA 1	EX	5	36	36	36		
SEGA 2			37	37	37		
SEGA 3			38	38	38		
SEGA 4			39	39	39		
SEGA 5			40	40	40		
SEGA 6	3	7	41	41	41		
SEGA 7			42	42	42		
SEGA 8			43	43	43		
SEGA 9			44	44	44		
SEGA10			45	45	45		
SEGA11	STEREO	CH. STEREO	46	46	46		
SEGA12			47	47	47		
SEGA13			48	48	48		
SEGA14			49	49	49		
SEGA15			50	50	50		
SEGA16	□(HEADPHONE)	□(SURR.OFF)	51	51	51		
SEGA17			52	52	52		
SEGA18			53	53	53		
SEGA19			54	54	54		
SEGA20			55	55	55		
SEGA21	HEADPHONE	SURR. OFF	56	56	56		
SEGA22			57	57	57		
SEGA23			58	58	58		
SEGA24			59	59	59		
SEGA25			60	60	60		
SEGA26	□(DTS,ES)		61	61	61		
SEGA27			62	62	62		
SEGA28			63	63	63		
SEGA29			64	64	64		
SEGA30			65	65	65		
SEGA31			66	66	66		
SEGA32			67	67	67		
SEGA33			68	68	68		
SEGA34			69	69	69		
SEGA35			70	70	70		

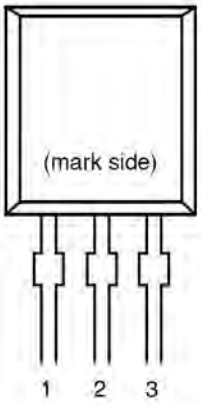
MODEL : HCA-18LM03
ANODE CONNECTION
Rev.① 20-Jan-2005

LOW VOLTAGE DETECTOR

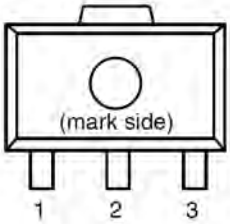
R×5VT SERIES

PIN CONFIGURATION

• TO-92



• SOT-89



• SOT-23-5

PIN DESCRIPTION

• TO-92

Pin No.	Symbol
1	OUT
2	VDD
3	GND

• SOT-89

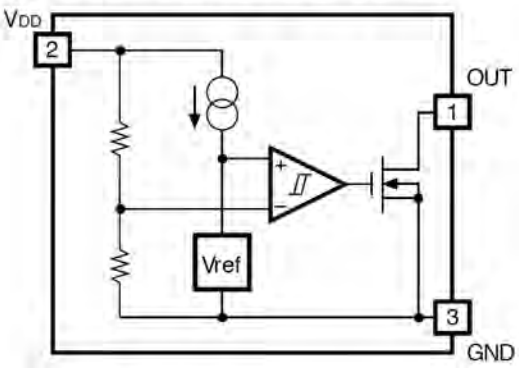
Pin No.	Symbol
1	OUT
2	VDD
3	GND

• SOT-23-5

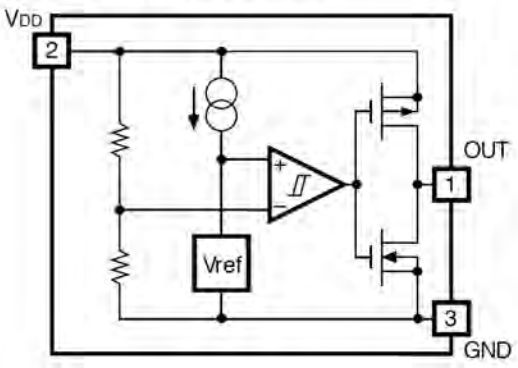
Pin No.	Symbol
1	OUT
2	VDD
3	GND
4	NC
5	NC

BLOCK DIAGRAMS

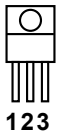
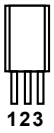
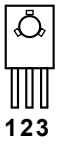
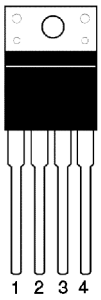
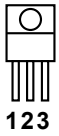
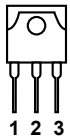
• Nch Open Drain Output (R×5VT××A)



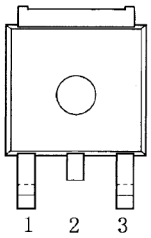
• CMOS Output (R×5VT××C)



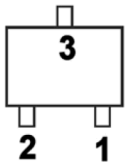
TRANSISTOR, REGULATOR IC BLOCK DIAGRAM

TO-92M  1. Emitter 2. Collector 3. Base KTC2874B KSC2785Y KRA107M KRC107M KRA104MT KRC104M	TO-92  1. Emitter 2. Collector 3. Base KTD1302T KTA1268GR KTC3200GR KTC3198Y KTA1271Y KSA1175YT	TO-220  1. GND 2. INPUT 3. OUTPUT MCNJM7905 MC7915C KIA7908 L7905 L7915	TO-92L  1. Emitter 2. Collector 3. Base KTA1024Y KSC2316Y
TO-126  1. Emitter 2. Collector 3. Base 2SA1360O 2SC3423O KTD600KG	TO-220  KIA278R05PI KIA278R15PI KIA278R00PI KIA378R05PI KIA378R09PI 1. Input 2. Output 3. Ground 4. on/off Control	TO-220  1. INPUT 2. GND 3. OUTPUT MC7815C MC7805C MC7809 L7805 NJM7824 L7815 KIA7808	TO-3P  1. Base 2. Collector 3. Emitter 2SB1560 2SD2390 2SA1360 2SB1647

NJM2391DL1-25 NJM2391DL1-33
LOW DROPOUT VOLTAGE REGULATOR



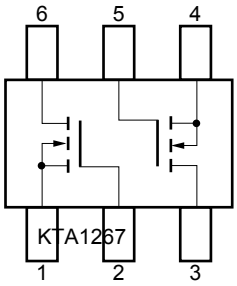
PIN FUNCTION
1. IN
2. GND
3. OUT



1) Emitter
2) Base
3) Collector

KRC102S
KRA102S
KRC103S
KRC107S
KRC111S
KRA107S

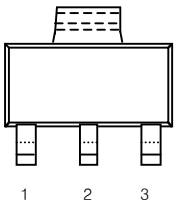
N-CHANNEL MOS FET ARRAY
μPA672T



1. Source 1 (S1)
2. Gate 1 (G1)
3. Drain 2 (D2)
4. Source 2 (S2)
5. Gate 2 (G2)
6. Drain 1 (D1)

Marking: MA

SOT-223 PKG (FRONT VIEW)

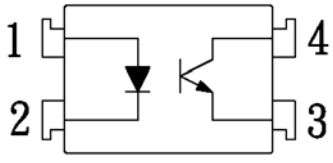


KIA1117S18
KIA1117S33
KIA1117S50

PIN FUNCTION
1. Adj/Gnd
2. Vout
3. Vin

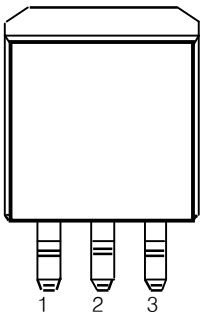
REGULATOR

KP1010 photocoupler

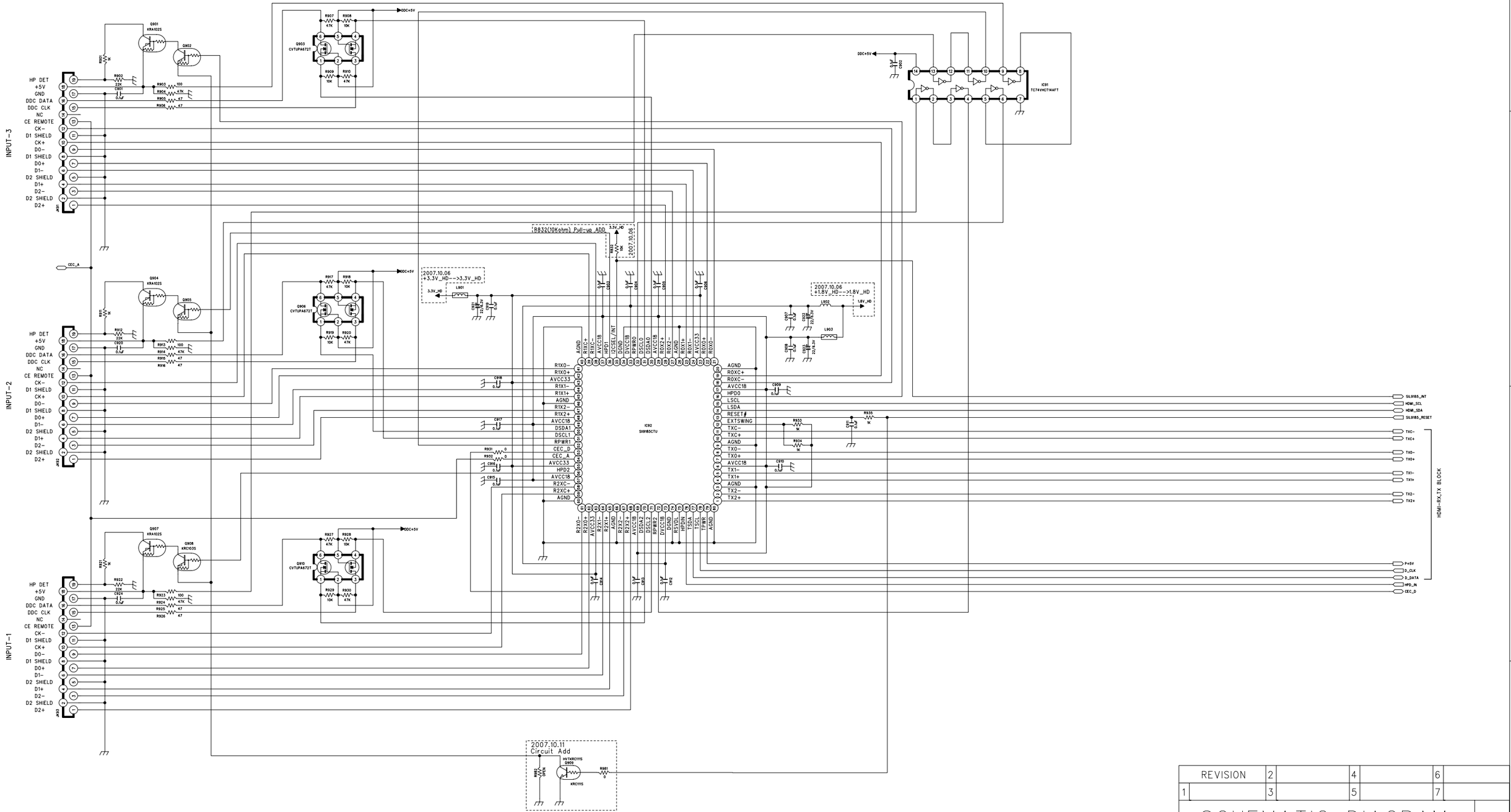


1. Anode
2. Cathode
3. Emitter
4. Collector

TO-263 (D2 PKG, FRONT VIEW)



PIN FUNCTION
1. Adj/Gnd
2. Vout
3. Vin



REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM — SHEET

MODEL: AVR254/255/355/3550HD — 1/4

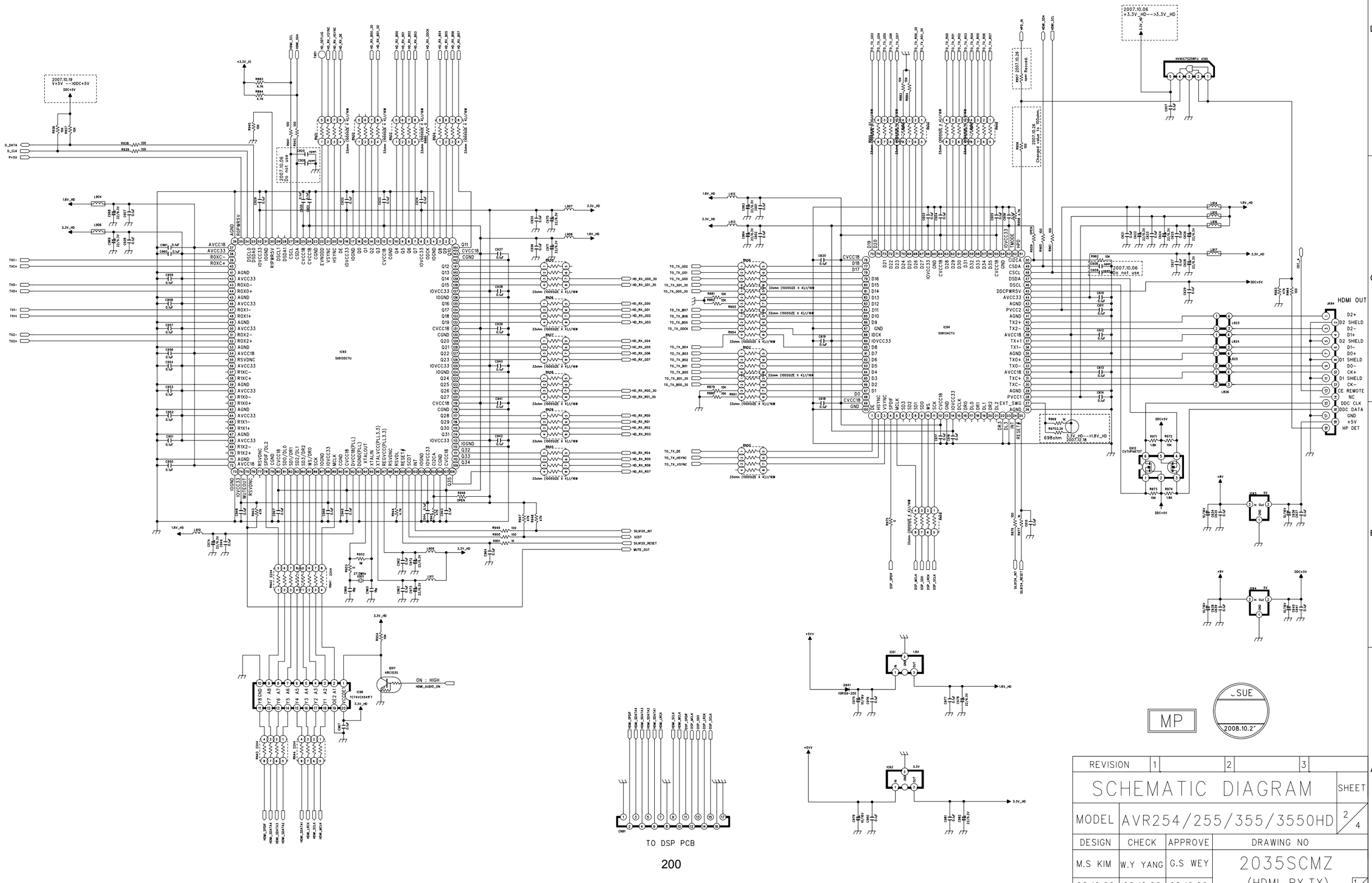
DESIGN	CHECK	APPROVE	DRAWING NO
M.S KIM	W.Y YANG	G.S WEY	2035SCMZ (HDMI-INPUT) 1/1
08.10.22	08.10.22	08.10.22	

MP

ISSUE 2008.10.27

CUP12035

AVR3550HD harman/kardon



REVISION	1	2	3	
SCHEMATIC DIAGRAM				SHEET
MODEL	AVR254/255/355/3550HD			2/4
DESIGN	CHECK	APPROVE	DRAWING NO	
M.S KIM	W.Y YANG	G.S WEY	2035SCMZ (HDMI-RX,TX)	1/1
08.10.22	08.10.22	08.10.22		

CUP12035

ANALOG VIDEO INPUT PORT

COMPONENT IN : 3EA
COMPOSITE IN : 1EA
S_VIDEO IN : 1EA

RGB 10BIT INPUT

B 8BIT INPUT

G 8BIT INPUT

R 8BIT INPUT

*OPTION(Do not use)

*IR_IN/NO USE

*GPROBE

*COMMUNICATION WITH MCU

*CONTROL ROM/VIDEO ENCODER

*EEPROM

*Add 08.01.16 Reserved GPIOs.

*DDR MEMORY INTERFACE

B 8BIT OUTPUT

G 8BIT OUTPUT

R 8BIT OUTPUT

TTL OUTPUT

*FLASH MEMORY INTERFACE

RGB 10BIT OUTPUT
TTL OUTPUT

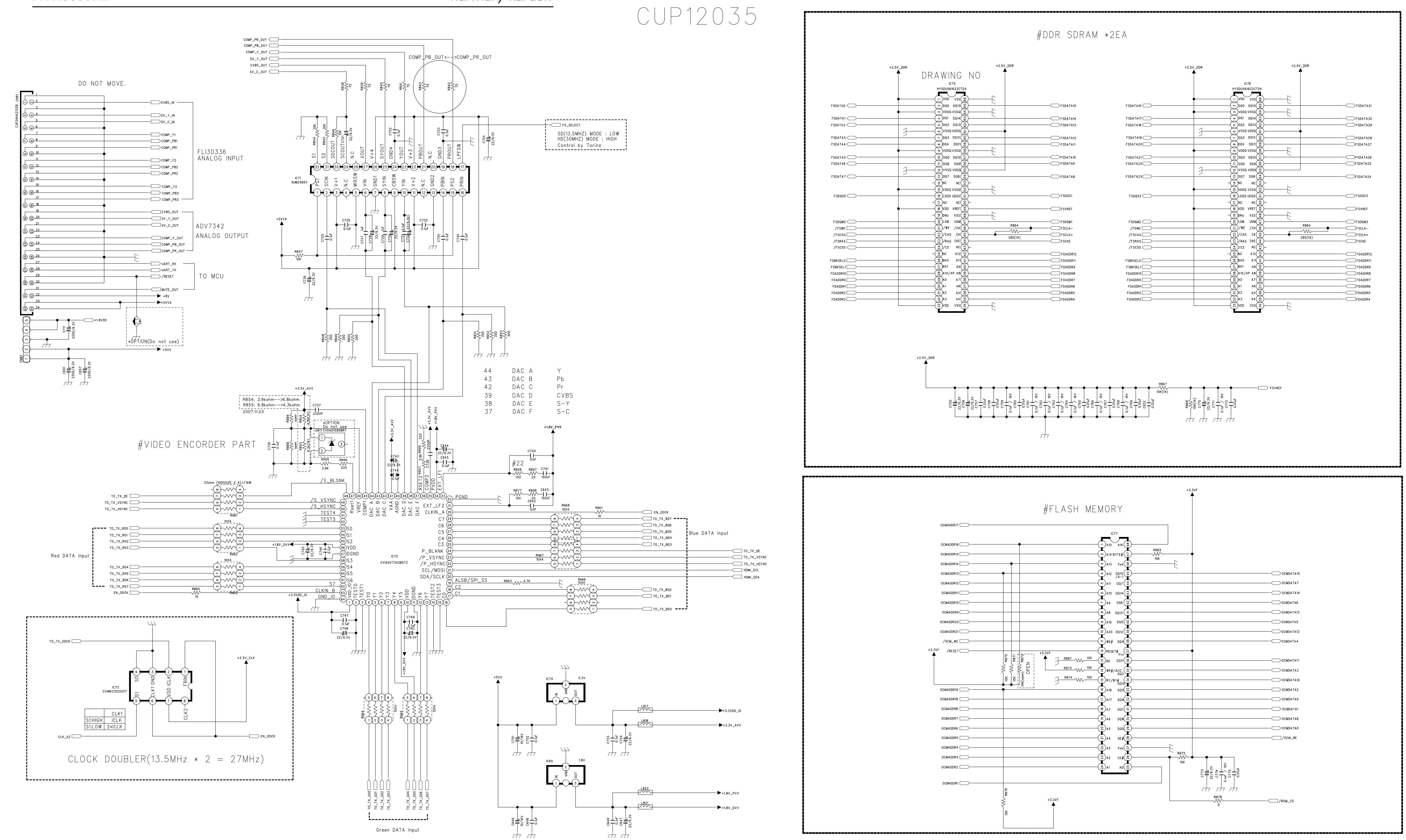
* Need to change 2A

MP

ISSUE
2008.10.27

REVISION	2		4		6	
1		3		5		7	

SCHEMATIC DIAGRAM			SHEET 3/4
MODEL	AVR254/255/355/3550HD		
DESIGN	CHECK	APPROVE	DRAWING NO
M.S KIM	W.Y YANG	G.S WEY	2035SCMZ (TORINO) 1/1
08.10.22	08.10.22	08.10.22	



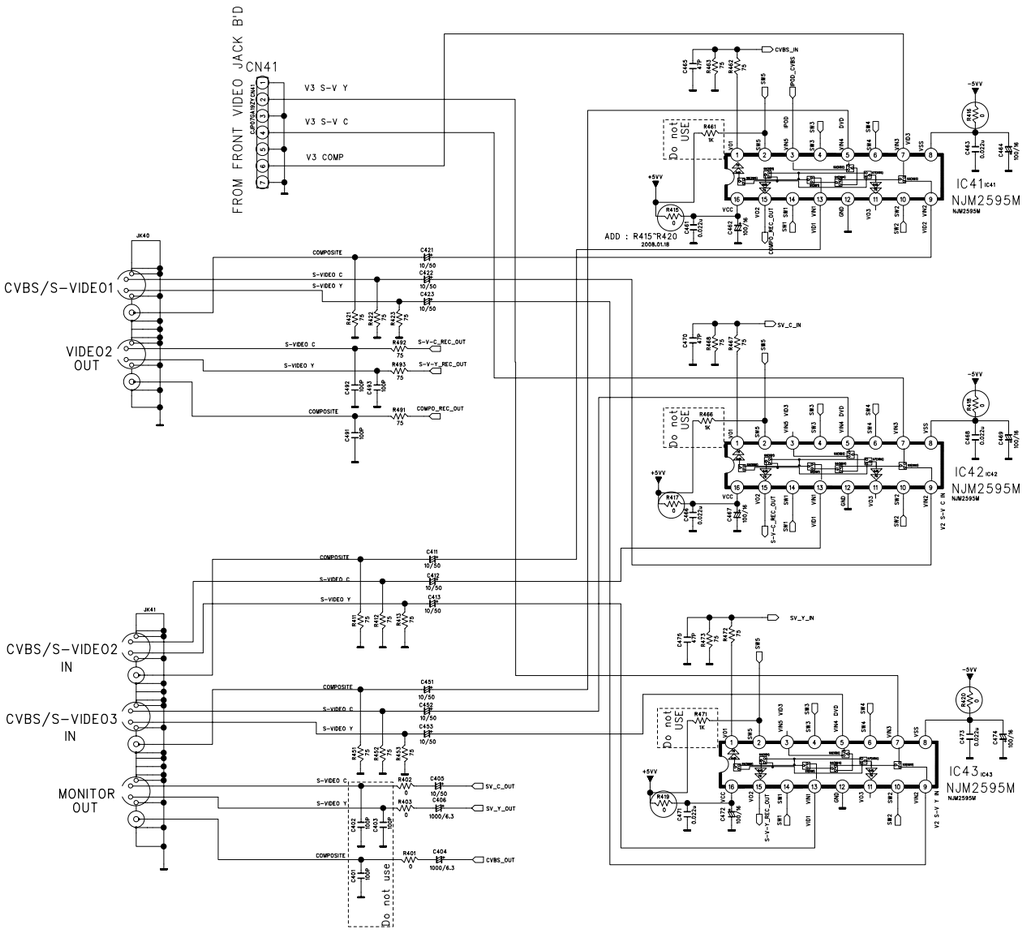
MP

SUE 2008.10.2

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR254/255/355/3550HD		1/4
DESIGN	CHECK	APPROVE	DRAWING NO
M.S KIM	W.Y YANG	G.S WEY	2035SCMZ (ADV7342+MEM.) 1/1
08.10.22	08.10.22	08.10.22	

CUP12033



*NJM2595M OPTION
==>V_MUTE "LOW" ACTIVE

FUNC.	SW1	SW2	SW3	SW4	SW5
CVBS/S-V1	H	L	L	L	H
CVBS/S-V2	L	H	L	L	H
CVBS/S-V3	H	L	L	H	H
FRONT CVBS/S-V	H	H	L	L	H
IPOD	H	L	H	H	H

* DEFINITION OF I2C REGISTER (NJW1321)

I2C BUS FORMAT

MSB				LSB	MSB		LSB	MSB		LSB	
S(1BIT)	SLAVE ADDRESS(7BIT)			A(1BIT)	DATA(8BIT)		A(1BIT)	DATA(8BIT)		A(1BIT)	P(1BIT)

SLAVE ADDRESS

MSB	Slave Address(8BIT)						MSB	Hex
1	0	0	0	0	0	ADR(1BIT)	R/NOT W(1BIT)	--

S : Starting Term
A : Acknowledge Bit
P : Ending Term
R/NOT W : Set the Write Mode or Read Mode.
ADR : Set the Slave Address by " ADR" terminal.
R/NOT W = 0 : WRITE MODE, ADR = 0/1 ; ADR=0 Hex94(h), ADR=1 Hex96(h)
R/NOT W = 0 : READ MODE, ADR = 0/1 ; ADR=0 Hex95(h), ADR=1 Hex97(h)

CONTROL REGISTER TABLE
<WRITE MODE>

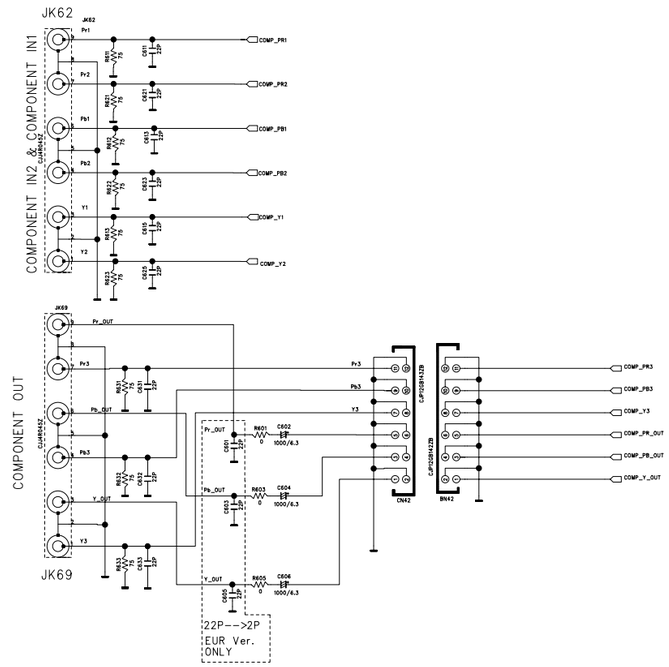
NO.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
DATA 1	PS1	PS2	OUT1				OUT2	
DATA 2	AUX0		AUX1		AUX2		AUX3	

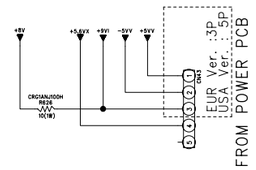
PS : POWER SAVE
=> PS = 1 ; POWER SAVE ON (MUTE), PS = 0 ; POWER SAVE OFF (OUT ON)
OUT : OUTPUT
AUX : AUXILIARY (CONTROL SIGNAL OUTPUT)

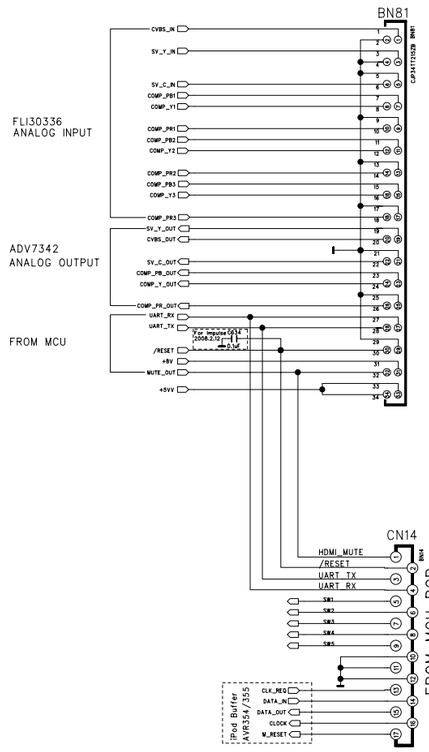
<READ MODE>

NO.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
DATA	PORT0		PORT1		PORT2		PORT3	

PORT : INPUT







* AVR345
*NO.4

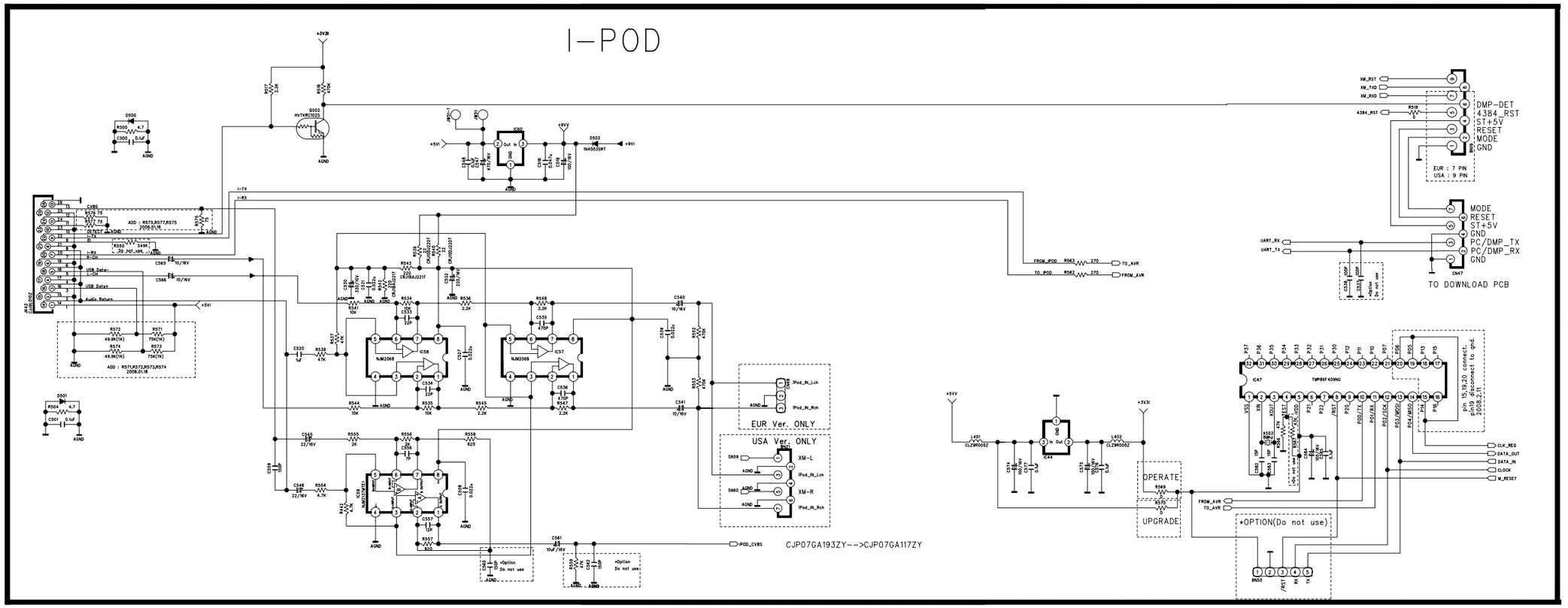
REVISION	2		4		6	
1		3		5		7

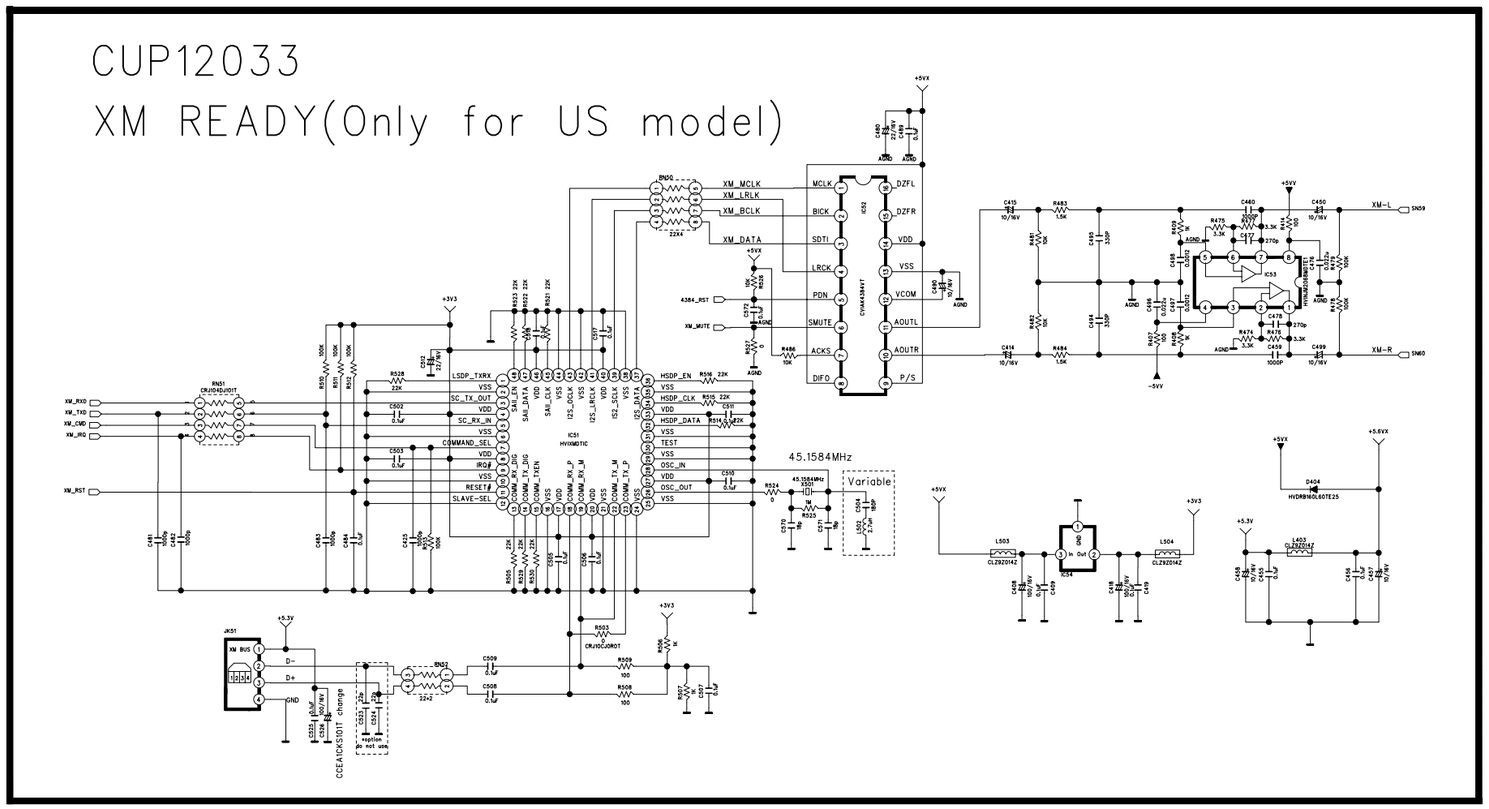
SCHEMATIC DIAGRAM — SHEET 1/2

MODEL: AVR354/355/3550HD

DESIGN	CHECK	APPROVE	DRAWING NO
M.S.K	W.Y.Y	G.S.W	2033SCMZ (VIDEO) 1/1
08.10.22	08.10.22	08.10.22	

MP — SUE 2008.10.22





REVISION	2		4		6		
1	3		5		7		

SCHEMATIC DIAGRAM			SHEET 1/4
MODEL	AVR354/355/3550HD		
DESIGN	CHECK	APPROVE	DRAWING NO
M.S.K	W.Y.Y	G.S.W	2033SCMZ (XM & IPOD) 1/1
08.10.22	08.10.22	08.10.22	

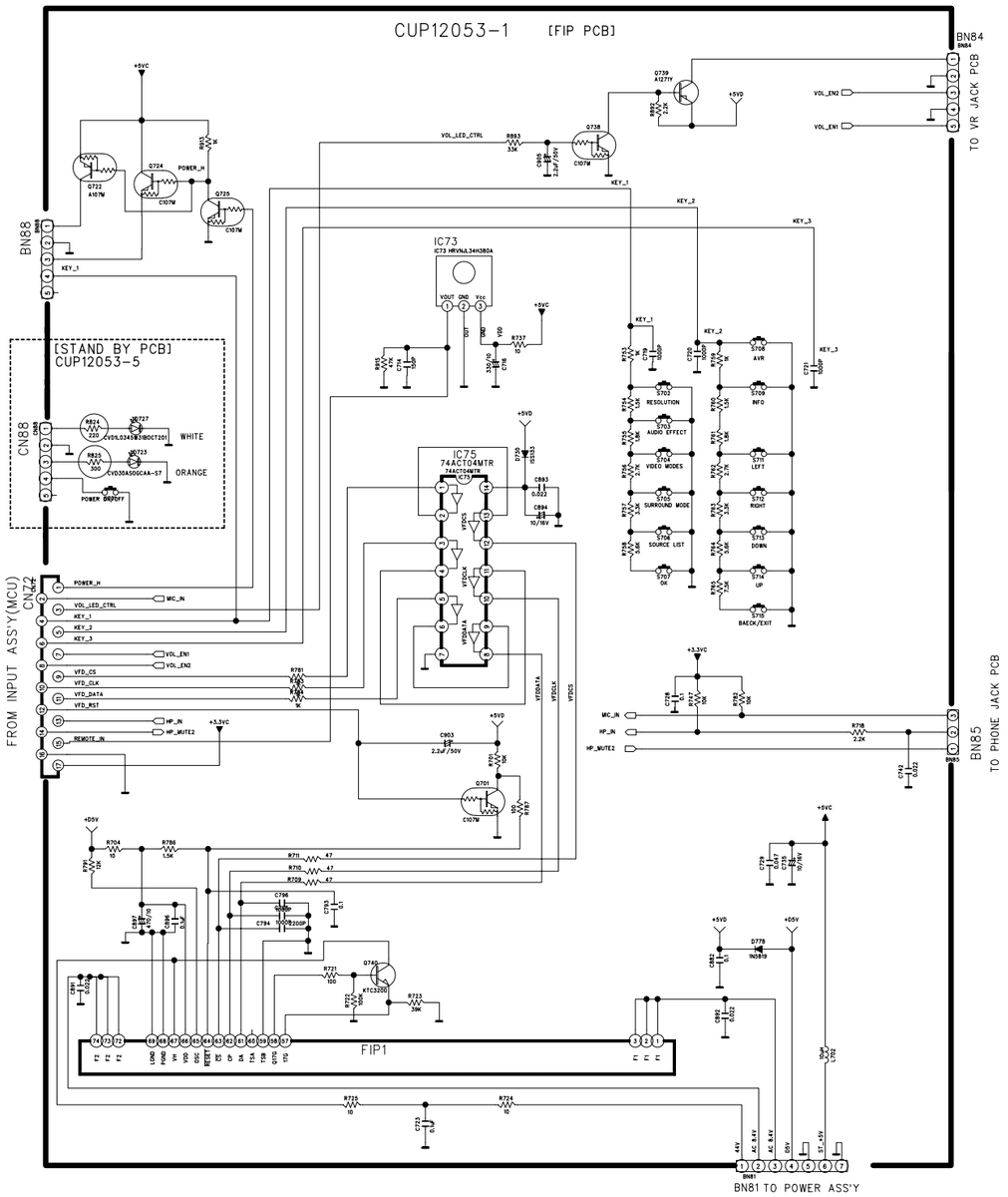
MP

ISSUE 2008.10.22

AVR3550HD harman/kardon

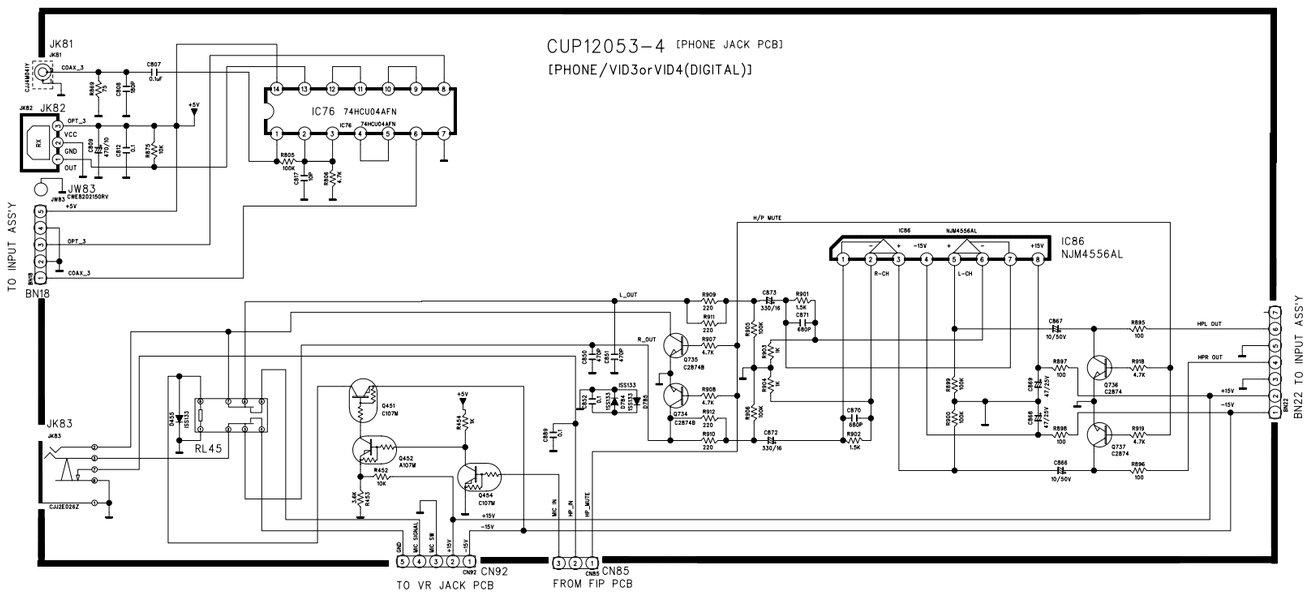
CUP12053

CUP12053-1 [FIP PCB]

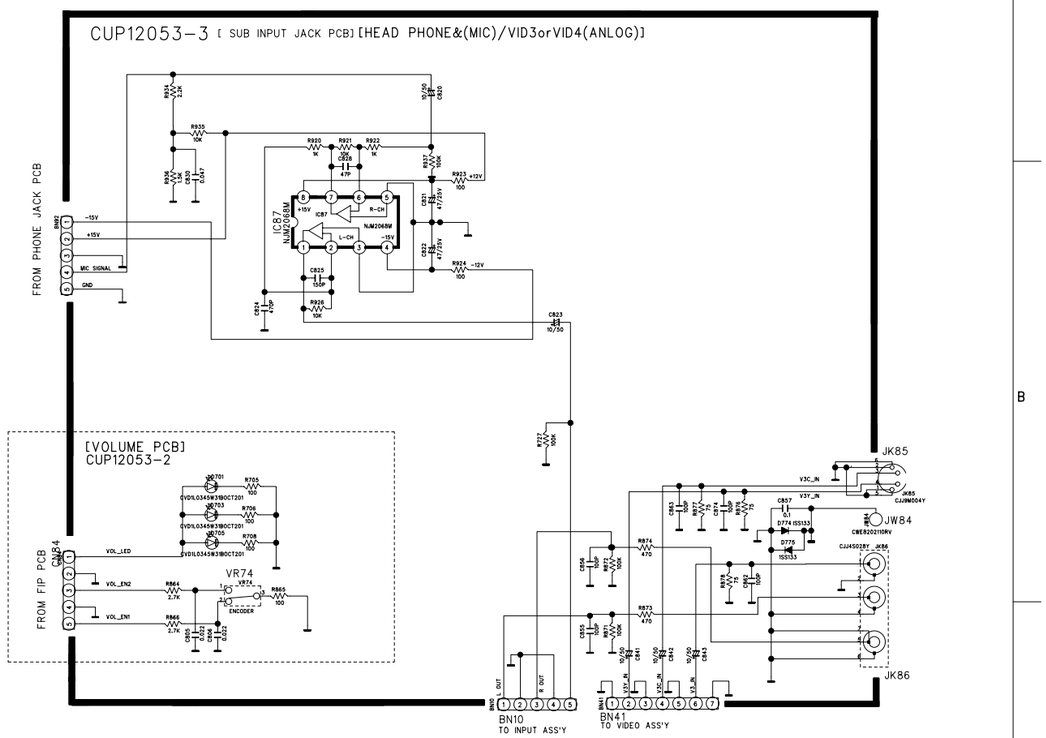


CUP12053-4 [PHONE JACK PCB]

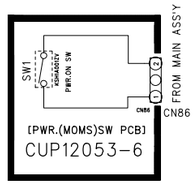
[PHONE/VID3orVID4(DIGITAL)]



CUP12053-3 [SUB INPUT JACK PCB] [HEAD PHONE&(MIC)/VID3orVID4(ANLOG)]

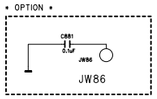


SW1 PWR.ON SW

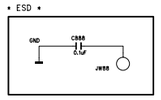


AVR255/355 NO USE

• OPTION •



• ESD •



REVISION	2		4		6		
1	3		5		7		

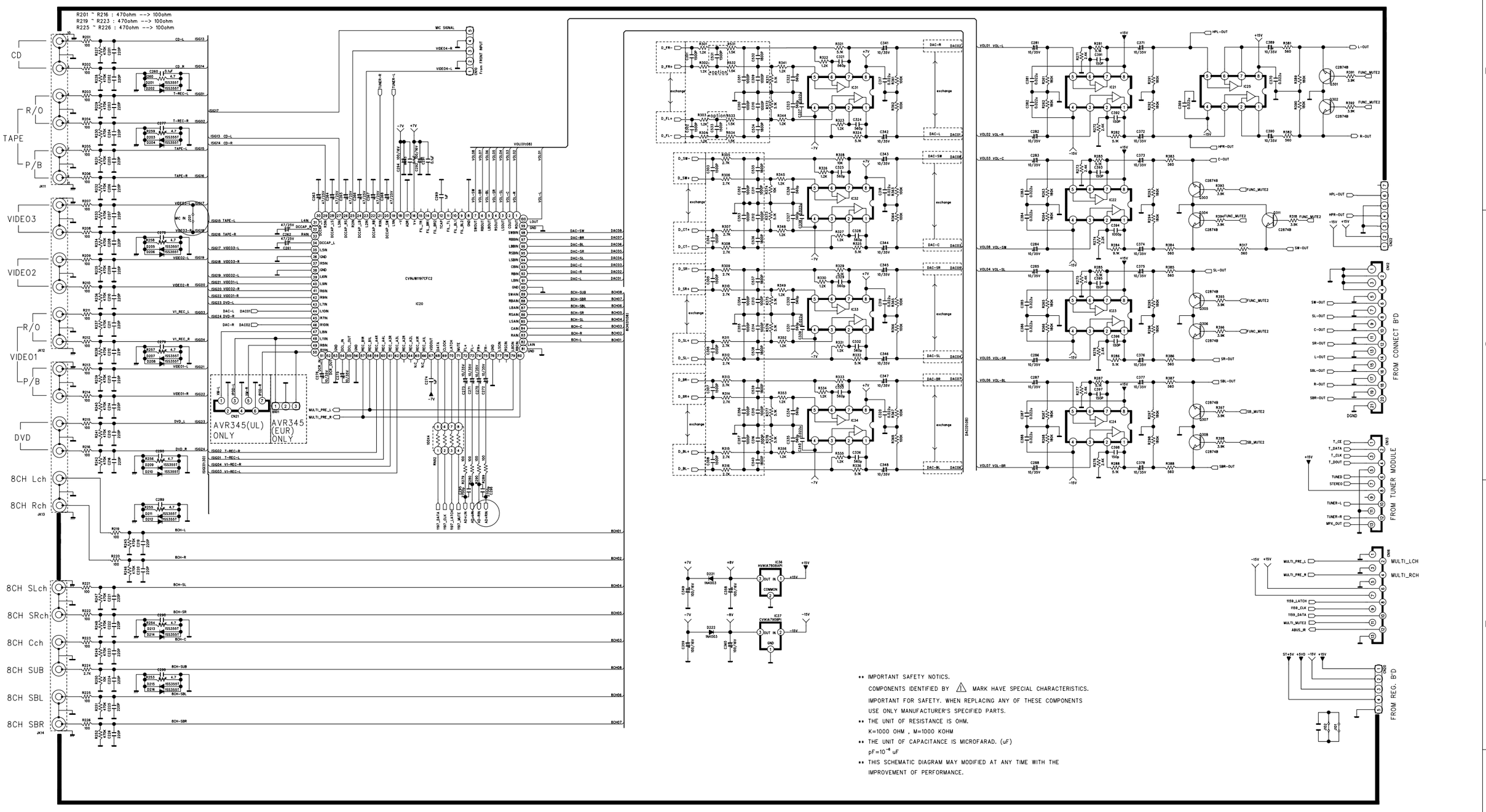
SCHEMATIC DIAGRAM — SHEET 1/7

MODEL	AVR255/355/3550HD	
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.B	W.Y.Y	G.S.W	2053SCMZ (FRONT) 1/1
08.10.22	08.10.22	08.10.22	

M P — ISSUE 2008.10.

CUP12029

R201 ~ R216 : 470ohm --> 100ohm
R219 ~ R223 : 470ohm --> 100ohm
R225 ~ R226 : 470ohm --> 100ohm



MP

SUE 2008.10.22

REVISION	2	4	6	
1	3	5	7	

SCHEMATIC DIAGRAM — SHEET

MODEL	AVR254/255/354/355/3550HD	1/3

DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2029SCMZ (INPUT) 1/1
08.10.22	08.10.22	08.10.22	

CUP12029

HDMI SPDIF MODE : DIR MASTER
HDMI I2S MODE : HDMI MASTER
ADC MODE : DSP MASTER
DIR MODE : DIR MASTER

*OPTION : EMC COUNTERMEASUER

DATA	CS49700	SDRAM
EXT_D15/SD_D7	29	12
EXT_D14/SD_D6	30	11
EXT_D13/SD_D5	31	9
EXT_D12/SD_D4	32	8
EXT_D11/SD_D3	34	6
EXT_D10/SD_D2	35	5
EXT_D9/SD_D1	37	3
EXT_D8/SD_D0	39	2
EXT_D7/SD_D15	40	49
EXT_D6/SD_D14	41	48
EXT_D5/SD_D13	42	46
EXT_D4/SD_D12	43	45
EXT_D3/SD_D11	45	43
EXT_D2/SD_D10	46	42
EXT_D1/SD_D9	48	40
EXT_D0/SD_D8	49	39

Address	CS49700	SDRAM
EXT_A19	88	
EXT_A18	87	
EXT_A17	85	
EXT_A16	84	
EXT_A15	82	
EXT_A14/SD_A13	77	
EXT_A13/SD_A14	75	19
EXT_A12/SD_A10	74	20
EXT_A11/SD_A12	55	
EXT_A10/SD_A11	56	
EXT_A9/SD_A9	58	32
EXT_A8/SD_A8	59	31
EXT_A7/SD_A7	61	30
EXT_A6/SD_A6	62	29
EXT_A5/SD_A5	64	28
EXT_A4/SD_A4	67	27
EXT_A3/SD_A3	68	24
EXT_A2/SD_A2	70	23
EXT_A1/SD_A1	71	22
EXT_A0/SD_A0	72	21

<=> HDMI BOARD

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET

MODEL	AVR254/255/354/355/3550HD	2/3

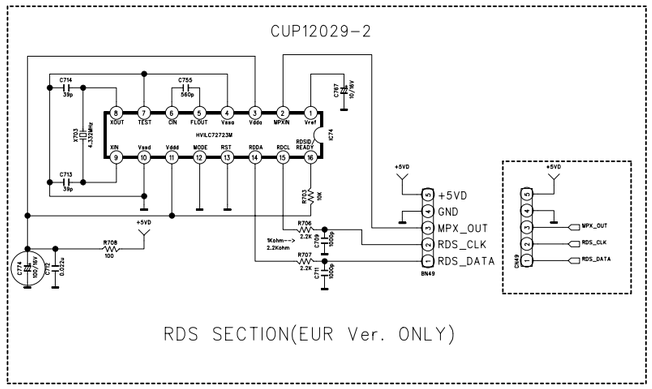
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2029SCMZ (DSP) 1/1
08.10.22	08.10.22	08.10.22	

ISSUE 2008.10.27

MP

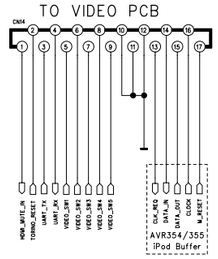
CUP12029

CUP12029-2



RDS SECTION(EUR Ver. ONLY)

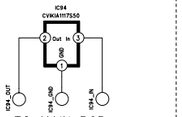
TO VIDEO PCB



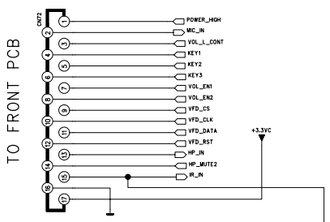
U-COM	AVR255	AVR355	AVR155
PIN 97	HDMI_MUTE_IN	HDMI_MUTE_IN	N.A
PIN 86	TORINO_RESET	TORINO_RESET	N.C
PIN 21	UART_TX(TORINO&PC)	UART_TX(TORINO&PC)	UART_TX(PC)
PIN 22	UART_RX(TORINO&PC)	UART_RX(TORINO&PC)	UART_RX(PC)
PIN 81	VIDEO_SW1	VIDEO_SW1	N.A
PIN 82	VIDEO_SW2	VIDEO_SW2	OSD_CS1
PIN 83	VIDEO_SW3	VIDEO_SW3	OSD_CLK
PIN 84	VIDEO_SW4	VIDEO_SW4	OSD_DA
PIN 85	VIDEO_SW5	VIDEO_SW5	OSD_M
PIN 80		CLOCK	HDMI MUX_SDA
PIN 79		DATA_OUT	HDMI MUX_SCLK
PIN 77		DATA_IN	OSD_H
PIN 76		CLK-REQ	

CUP12029-3

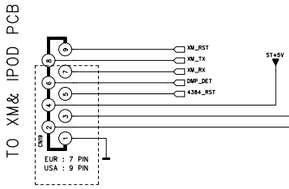
ST+5V REG PCB

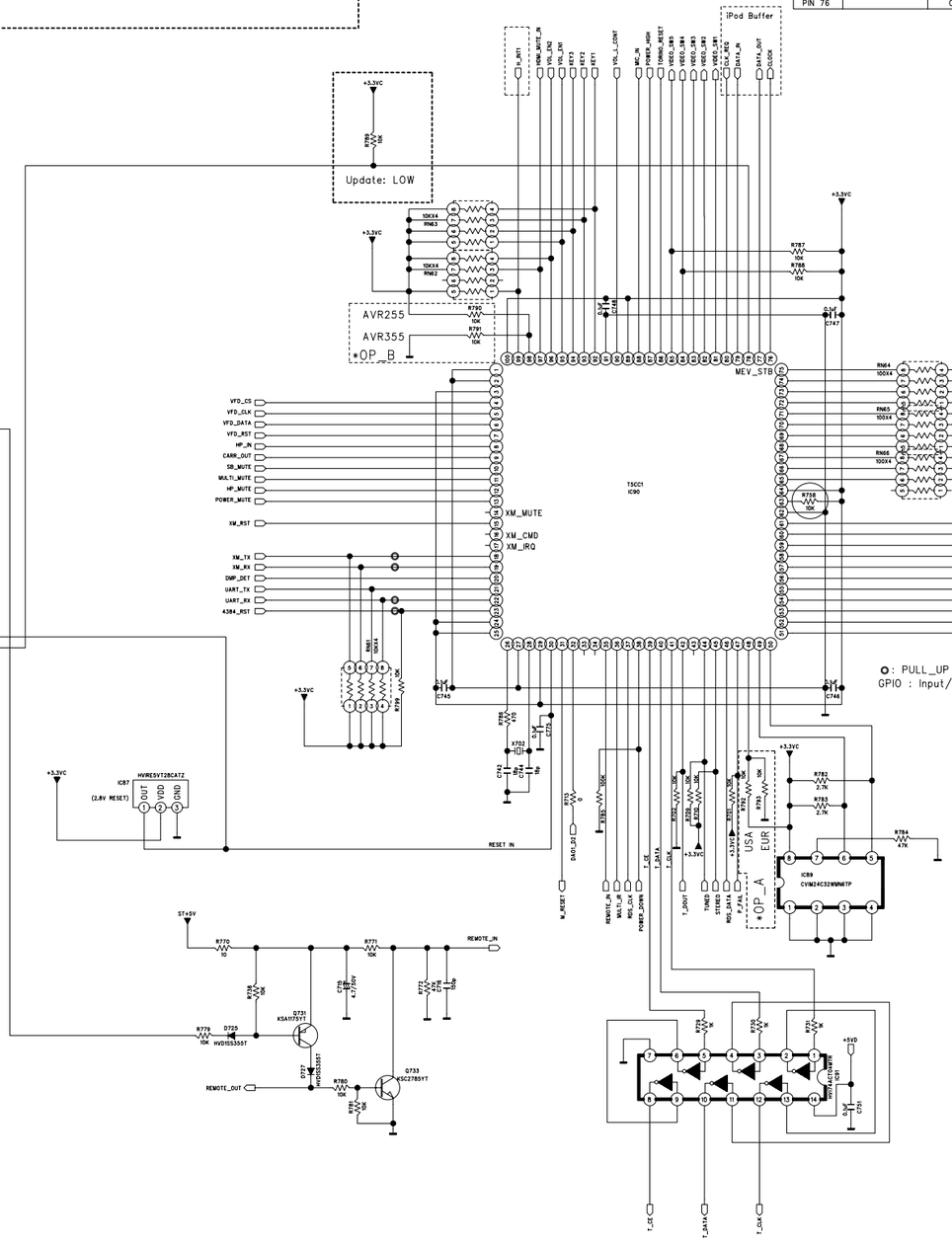


TO FRONT PCB



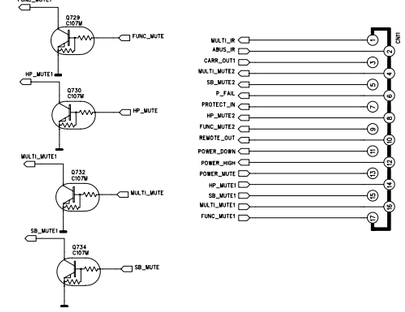
TO XM& IPOD PCB

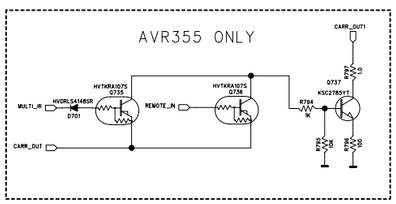


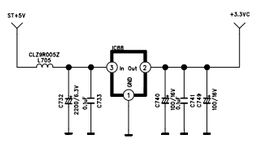


* MODEL OPTION *

MODEL	OP_A(PIN48)	OP_B(PIN98)
AVR355	HIGH(R792)	LOW(R791)
AVR354	HIGH(R792)	LOW(R791)
AVR254	HIGH(R792)	HIGH(R790)
AVR355/230	LOW(R793)	LOW(R791)
AVR255/230	LOW(R793)	HIGH(R790)







MP

ISSUE 2008.10.2?

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR254/255/354/355/3550HD		3/3
DESIGN	CHECK	APPROVE	DRAWING NO
C.B.LEE	W.Y.YANG	G.S.WEY	2029SCMZ (CPU) 1/1
08.10.22	08.10.22	08.10.22	

SR-CH

BL-CH

SL-CH

EXCEPT AVR154/155

BR-CH

C-CH

FR-CH

FL-CH

GAIN	R561, R562, R563, R564, R565, R850 R851
AVR154/155	1.8K
AVR255/355	1.6K

ONLY FAN USING

DC PROTECTOR

THERMAL PROTECTOR

OVERLOAD DETECTION

FAN

FOR USING FAN

EXCEPT AVR154/155

ONLY AVR154/155

JW92: AVR154/155 ONLY

AVR354/355 ONLY

JW90,JW91 : ALL MODELS

AVR254/255/354/355 PART

TO REMOTE IN/OUT B'D

FROM TRANS

AC IN

MOMS S/W BN90

TO REG B'D

TO MULTI PCB

JW93, OL91, F902 : EXCEPT AVR154

FROM INPUT B'D

FROM TRANS B'D

AVR254/255/354/355 OPTION

2SD2389P:AVR154
2SD2390:AVR155/254/255
2SD2560:AVR354/355

2SB1559P:AVR154
2SB1560:AVR155/254/255
2SB1647:AVR354/355

6800/50V : (AVR154/155) 8200/50V : (AVR254/255) 8200/63V : (AVR354/355) C902 C909

6800/50V : (AVR154/155) 10000/50V : (AVR254/255) 12000/63V : (AVR354/355) C915 C916

F901 : 6.3A (KBA2C6300TLEY) USA AVR354
F901 : 8A (KBA2C8000TLEY) USA AVR254/354/355
F901 : 4A (KBA2C4000TLEZ) EUR AVR155/230
F901 : 6.3A (KBA2C6300TLEZ) EUR AVR255/230,355/230

* BN90, CN90 OPTION
AVR154/254/354 : BN90
AVR155/230, 255/230, 355, 355/230 : CN90

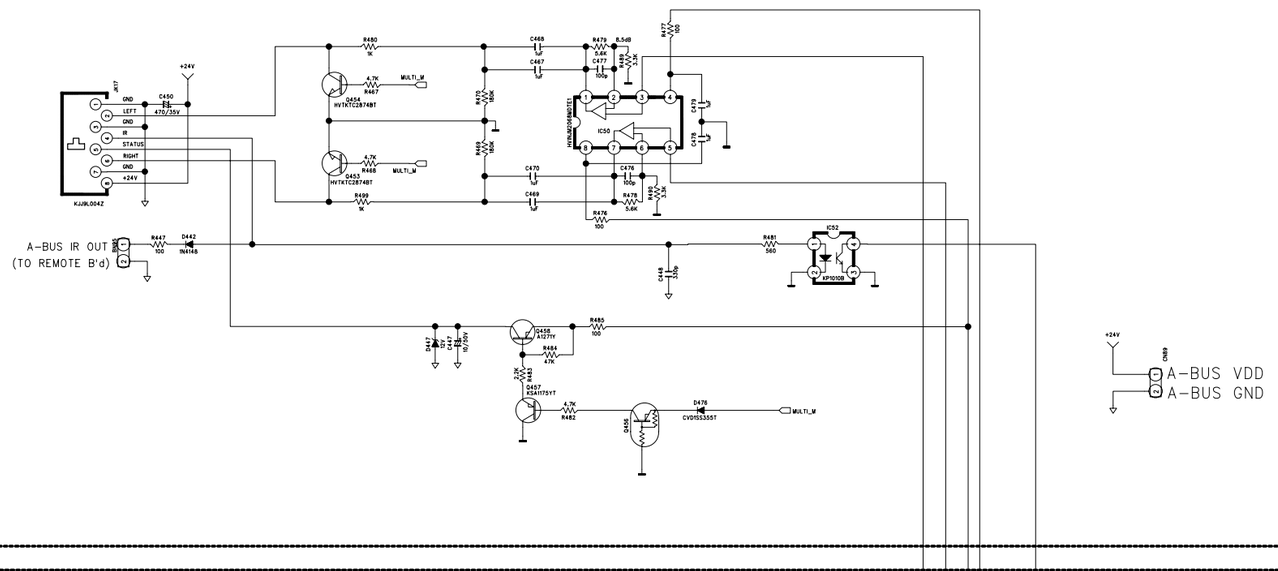
CJA6537BY4 (USA) : AVR154/155/254/255
CJA2B0432A (EUR) : AVR154/230,155/230,254/230,255/230
AVR354,355,354/230,355/230 : CWZ5R4001BNHA, CJA8A006ZW
CJA2A0752 (USA) : AVR354/355
CJA2B0542 (EUR) : AVR354/230, 355/230

REVISION	1	2	3	SHEET
SCHEMATIC DIAGRAM				
MODEL	AVR154/155 AVR254/255/354/355/3550HD			2 / 7
DESIGN	CHECK	APPROVE	DRAWING NO	
C.B.LEE	W.Y.YANG	G.S.WEY	2026SCMZ (MAIN)	1/1
08.10.22	08.10.22	08.10.22		

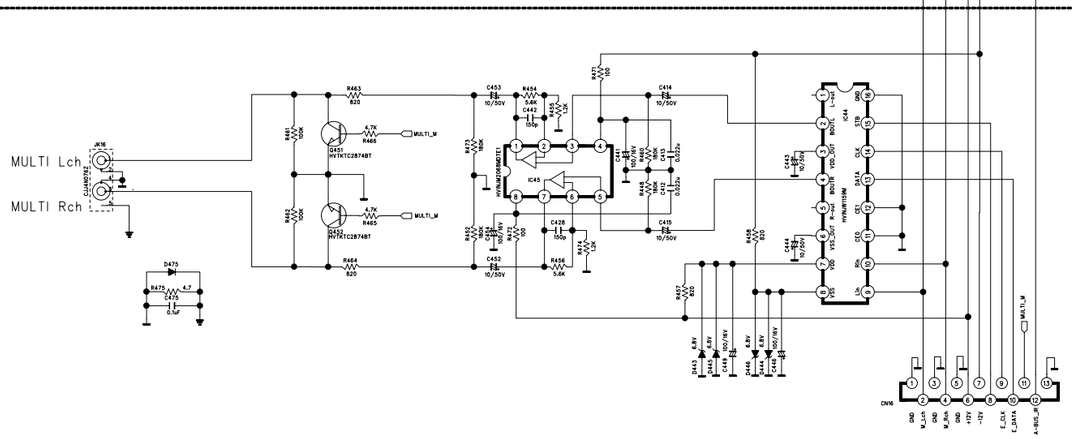
.10.22

** IMPORTNAT SAFETY NOTICE.
INPORTANT FOR SAFETY WHEN REPLACING ANY OF THESE COMPONENTS USE ONLY MANUFACTURE'S SPECIFIED PARTS.
** THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM.
** THE UNIT OF CAPACITANCE IS MICROFARAD (uF)
pF = 10^-6 uF
** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WIHE THE IMPROVEMENT OF PERFORMANCE

A-BUS PART : ONLY FOR AVR3550HD & AVR355/230



MULTI ROOM VOLUME : AVR3550HD, AVR354, AVR355/230



MP

ISSUE
2008.10.2

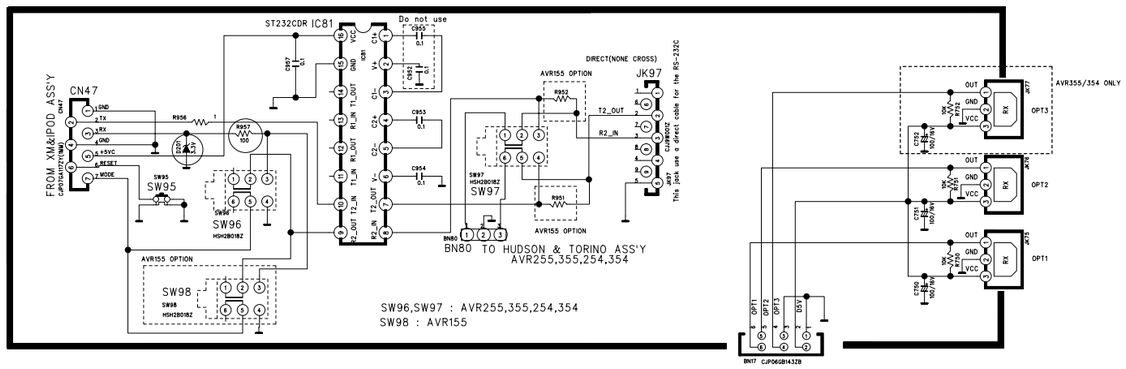
REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 1/1

MODEL	AVR354/355/3550HD	
DESIGN	CHECK	APPROVE	DRAWING NO
M.S.K	W.Y.Y	G.S.W	2036SCMZ (MULTI) 1/1
08.10.22	08.10.22	08.10.22	

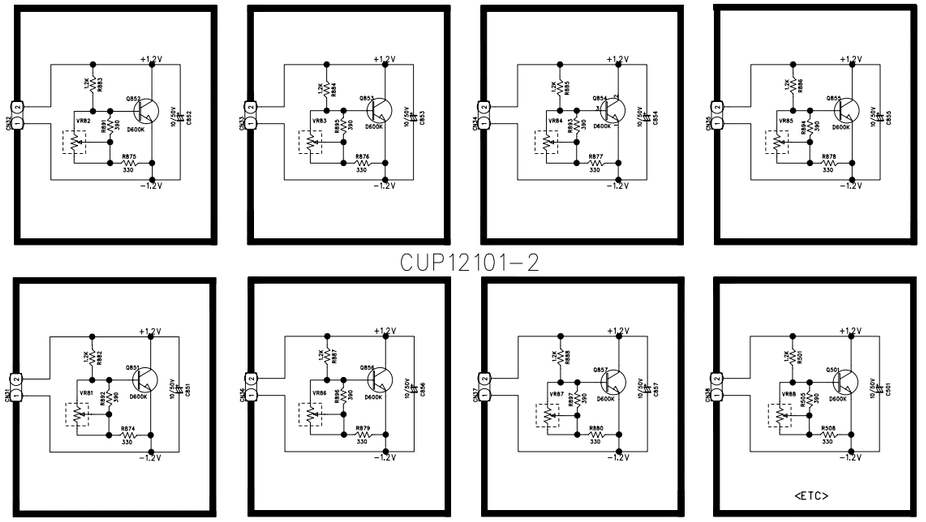
CUP12101

CUP12101-1

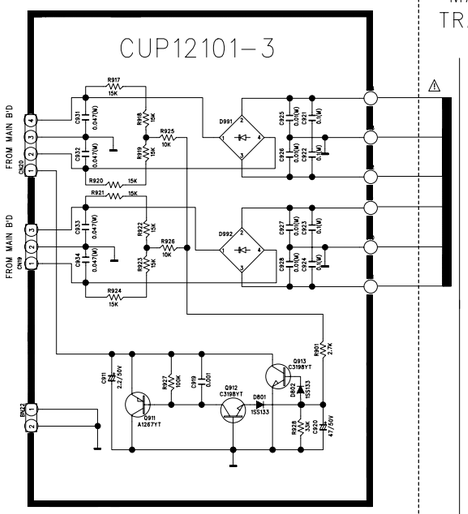


< OPTICAL IN & RS-232 PCB >

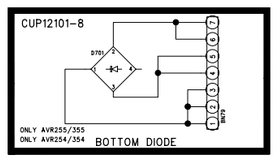
< BIAS T.R PCB >



CUP12101-3



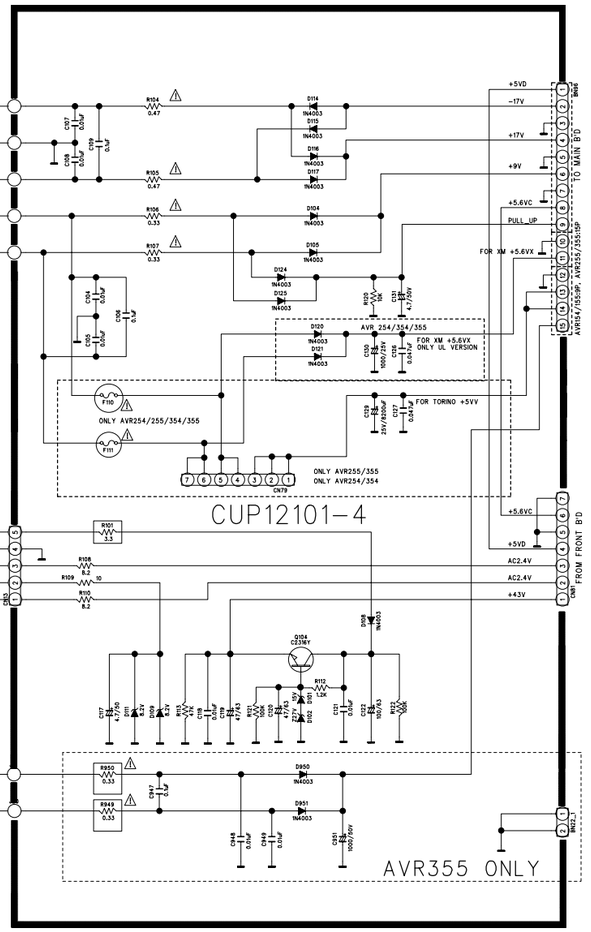
CUP12101-8



USA : AC120V 60Hz
EUR : AC230V 50Hz

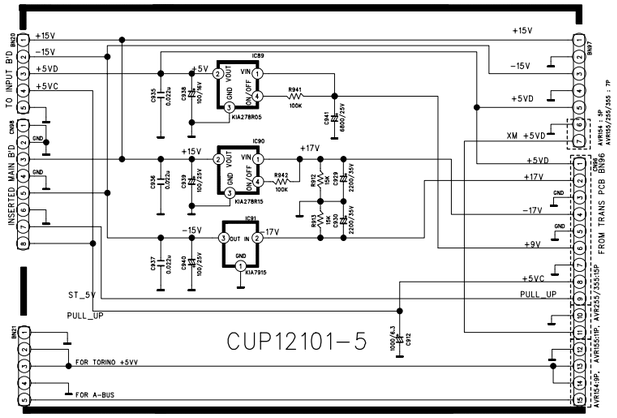
MAIN TRANS

CUP12101-4

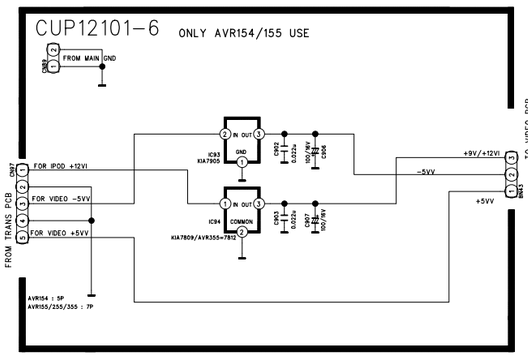


< TRANS PCB >

CUP12101-5



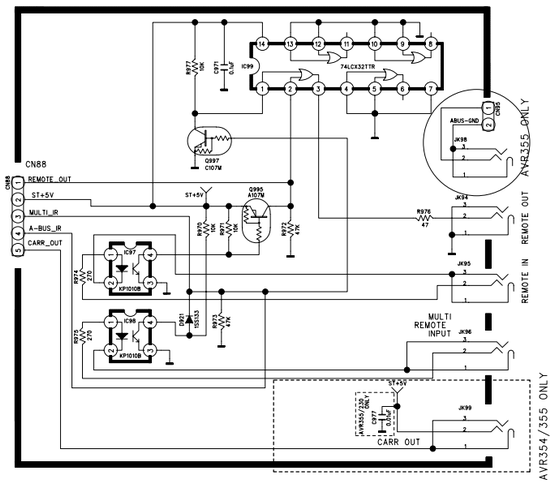
CUP12101-6 ONLY AVR154/155 USE



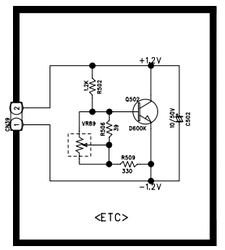
< REGULATOR PCB >

CUP12101-7

AVR254/255/354/355 ONLY



< REMOTE IN/OUT PCB >



M P

SUE
2008.10.2

REVISION	2	4	6
1	3	5	7

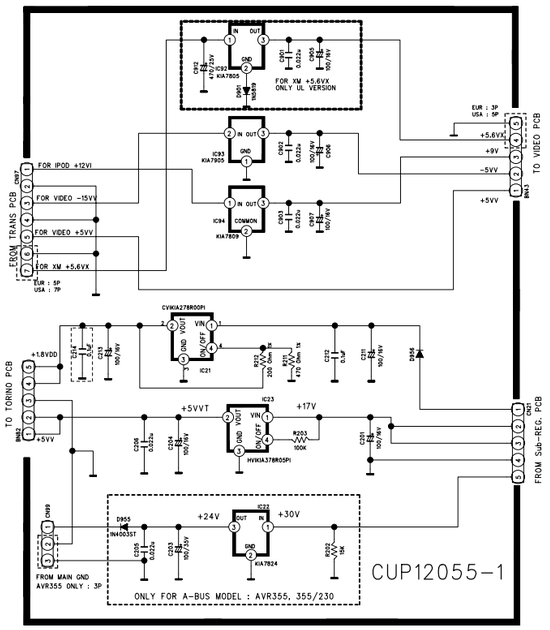
SCHEMATIC DIAGRAM — SHEET 1/1

MODEL: AVR154/AVR155 AVR254/255/354/355/3550HD

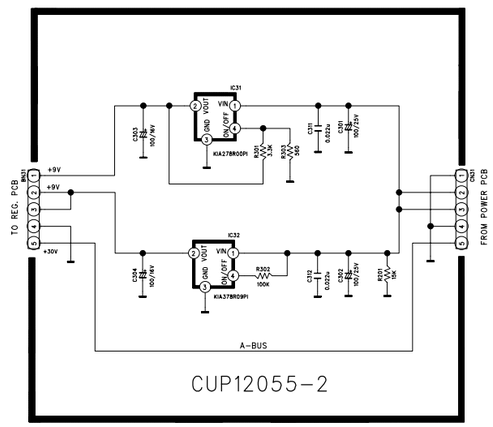
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.B	Y.Y.W	G.S.W	2101SCMZ (POWER) 1/1
08.10.22	08.10.22	08.10.22	

CUP12055

< REGULATOR PCB >



< Sub-REGULATOR PCB >



REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET 1/1

MODEL: AVR 254/255/354/355/3550HD

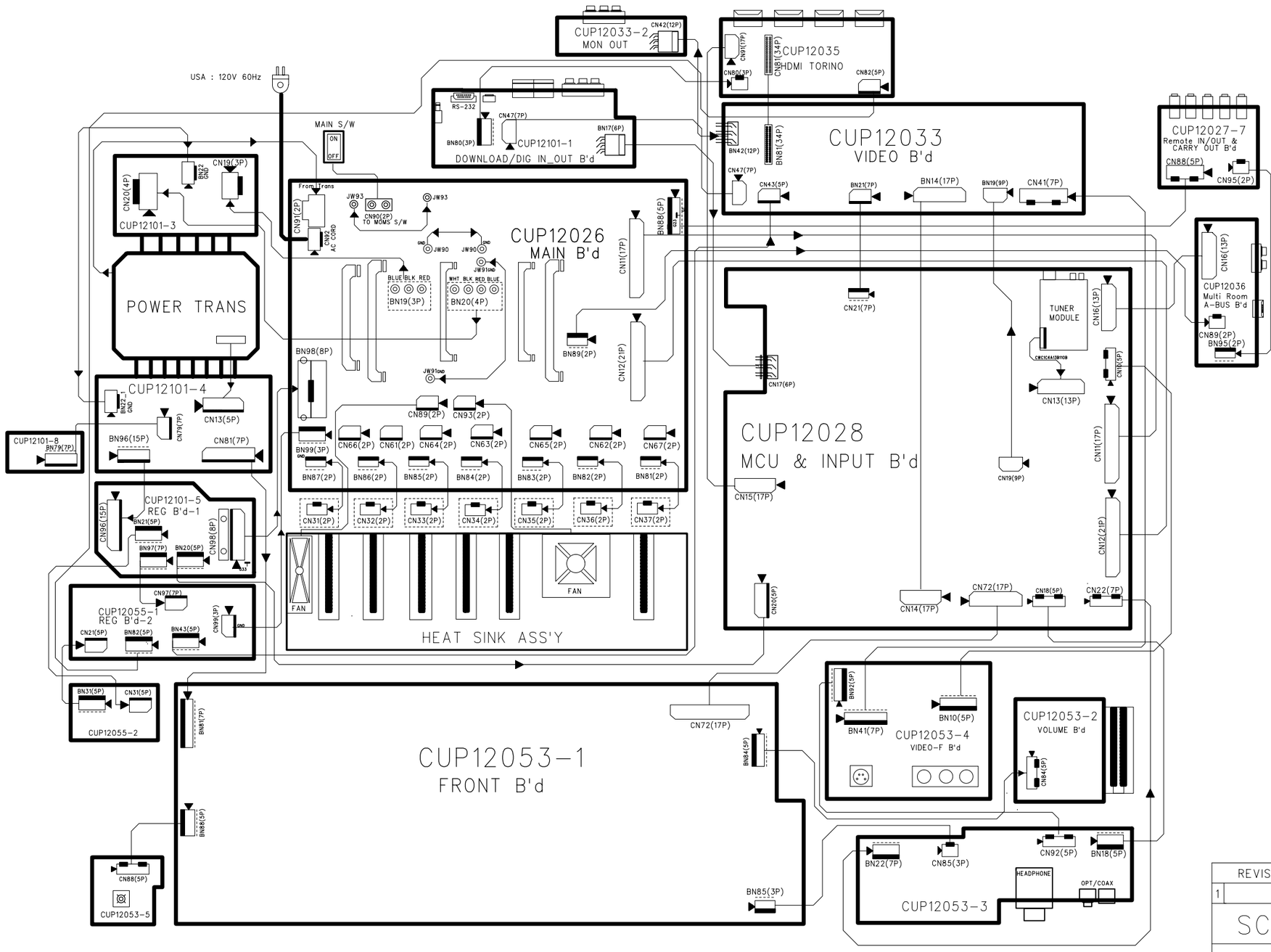
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.B	W.Y.Y	G.S.W	2055SCMZ (REGULATOR) 1/1
08.10.22	08.10.22	08.10.22	

MP

SUE

2008.10.2

AVR3550HD WIRING DIAGRAM



TI.LAB
2008.10.22

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM			SHEET
MODEL	AVR3550HD		1/1
DESIGN	CHECK	APPROVE	DRAWING NO
J.T.B	W.Y.Y	G.S.W	WIRING DIAGRAM
08.10.22	08.10.22	08.10.22	2029WDMZ 1/1