harman kardon

Model DVD 37 Eu version

DVD/CD/CD-R/CD-RW/VCD MP3 Player

Service Manual

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250 Crossways Park Dr.
Woodbury, New York, 11797

Released 2007
Discontinued XXXX

Rev 0, 8/2007

ESD PRECAUTIONS

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded-tip soldering iron to solder or unsolder ESD devices.
4. Use only an anti-static solder removal device. Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ESD devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
6. Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).
7. Immediately before removing the protective material from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will by installed.

CAUTION : BE SURE NO POWER IS APPLIED TO THE CHASSIS OR CIRCUIT, AND OBSERVE ALL OTHER SAFETY PRECAUTIONS.

8. Minimize bodily motions when handing unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

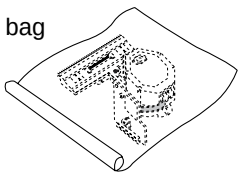
SERVICING PRECAUTIONS

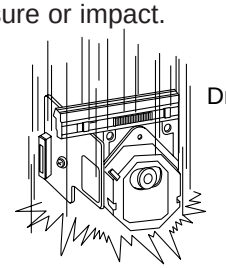
NOTES REGARDING HANDLING OF THE PICK-UP

1. Notes for transport and storage

1) The pick-up should always be left in its conductive bag until immediately prior to use.
2) The pick-up should never be subjected to external pressure or impact.

Storage in conductive bag

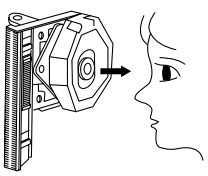




Drop impact

2. Repair notes

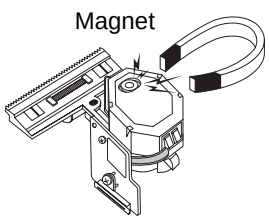
1) The pick-up incorporates a strong magnet, and so should never be brought close to magnetic materials.
2) The pick-up should always be handled correctly and carefully, taking care to avoid external pressure and impact. If it is subjected to strong pressure or impact, the result may be an operational malfunction and/or damage to the printed-circuit board.
3) Each and every pick-up is already individually adjusted to a high degree of precision, and for that reason the adjustment point and installation
screws should absolutely never be touched.
4) Laser beams may damage the eyes!
Absolutely never permit laser beams to enter the eyes!
Also NEVER switch ON the power to the laser output part (lens, etc.) of the pick-up if it is damaged.

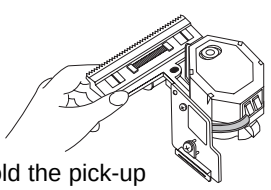


NEVER look directly at the laser beam, and don't let contact fingers or other exposed skin.

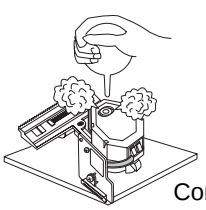
5) Cleaning the lens surface
If there is dust on the lens surface, the dust should be cleaned away by using an air bush (such as used for camera lens). The lens is held by a delicate spring. When cleaning the lens surface, therefore, a cotton swab should be used, taking care not to distort this.

Magnet



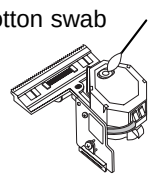


How to hold the pick-up



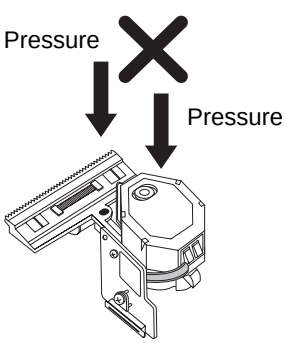
Conductive Sheet

Cotton swab



Pressure

Pressure



6) Never attempt to disassemble the pick-up.
Spring by excess pressure. If the lens is extremely dirty, apply isopropyl alcohol to the cotton swab. (Do not use any other liquid cleaners, because they will damage the lens.) Take care not to use too much of this alcohol on the swab, and do not allow the alcohol to get inside the pick-up.

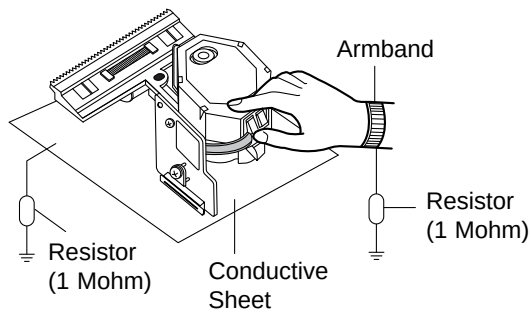
NOTES REGARDING COMPACT DISC PLAYER REPAIRS

1. Preparations

1) Compact disc players incorporate a great many ICs as well as the pick-up (laser diode). These components are sensitive to, and easily affected by, static electricity. If such static electricity is high voltage, components can be damaged, and for that reason components should be handled with care.
2) The pick-up is composed of many optical components and other high-precision components. Care must be taken, therefore, to avoid repair or storage where the temperature of humidity is high, where strong magnetism is present, or where there is excessive dust.

2. Notes for repair

1) Before replacing a component part, first disconnect the power supply lead wire from the unit
2) All equipment, measuring instruments and tools must be grounded.
3) The workbench should be covered with a conductive sheet and grounded.
   When removing the laser pick-up from its conductive bag, do not place the pick-up on the bag. (This is because there is the possibility of damage by static electricity.)
4) To prevent AC leakage, the metal part of the soldering iron should be grounded.
5) Workers should be grounded by an armband (1MΩ)
6) Care should be taken not to permit the laser pick-up to come in contact with clothing, in order to prevent static electricity changes in the clothing to escape from the armband.
7) The laser beam from the pick-up should NEVER be directly facing the eyes or bare skin.



DVD 37 TECHNICAL SPECIFICATIONS

Applicable Disc:	Disc formats: 5-inch (12cm) or 3-inch (8cm) DVD-Video, DVD-Audio, standard-conforming DVD-R, DVD+R, DVD-RW, DVD+RW, VCD, CD, CD-R, CD-RW or MP3 discs Region code: DVD video disc with Code 1 or 0 only DVD layers: Single side/single layer, single side/dual layer, dual side/dual layer Audio formats: DVD Audio MLP lossless, linear PCM, MPEG, Windows Media® 9, Dolby® Digital or DTS® audio discs Still-image format: JPEG
Video Signal System:	NTSC
HDMI™ Output:	Video: 480p, 720p, 1080i HDMI Version 1.0-compliant HDCP Version 1.1-compliant
Composite Video Output:	1V p-p/75 ohms, sync negative polarity
S-Video Output:	Y/luminance: 1V p-p/75 ohms, sync negative polarity C/chrominance: 0.286V p-p
Component Video Output:	Y: 1V p-p/75 ohms, sync negative polarity Pr: 0.7V p-p/75 ohms Pb: 0.7V p-p/75 ohms
Analog Audio Output:	2V RMS (1kHz, 0dB)
Frequency Response:	DVD (linear PCM): 2Hz – 22kHz +0/–0.5dB (48kHz sampling) 2Hz – 44kHz +0/–1.5dB (96kHz sampling) 2Hz – 88kHz +0/–0.5dB (192kHz sampling) CD: 2Hz – 20kHz +0/–0.5dB
Signal/Noise Ratio (SNR):	105dB (A-weighted)
Dynamic Range:	DVD: 100dB (18-bit)/105dB (20-bit) CD/DVD: 96dB (16-bit)
THD/1kHz:	DVD/CD: 0.0025%
Wow & Flutter:	Below measurable limits
AC Power:	110–240V AC/50–60Hz
Power Consumption:	1 Watt (on/standby)/13 watts (max)
Dimensions (H x W x D):	2" x 17-3/10" x 11-1/4" (50mm x 440mm x 285mm)
Weight:	6 lb (2.7kg)
Shipping Dimensions (H x W x D):	5" x 14-3/8" x 20" (127mm x 365mmx 508mm)
Shipping Weight:	8.8 lb (4kg)

Depth measurement includes knobs and connectors.

Height measurement includes feet and chassis.

All specifications subject to change without notice.

MODEL NAME : DVD 37 & DVD 37/230

Description : Characteristics Specification of Audio
Test Disc : YEDS7 (SONY), TDV-540A (ABEX)
Test Conditions : 10kΩ Load Terminated, AC100V 50/60Hz
Test Measuerment : VP-7722A (Audio Analyzer) ,CASCADE SYS-2522(AP)

1.ANALOG AUDIO OUTPUT

Measurement Item			Limit	Result	TEST DISC
Output Level[Vrms]		L R	2.0 ± 0.2		YEDS7 (SONY) TRACK 1
Level difference [Vrms]			< 0.2		
F/ response [dB] Ref.1kHz 0dB	20 Hz	L R	0 ± 1.0		YEDS7 (SONY) TRACK 2
	100 Hz	L R	0 ± 1.0		YEDS7 (SONY) TRACK 4
	10 KHz	L R	0 ± 1.0		YEDS7 (SONY) TRACK 10
	20 KHz	L R	0 ± 1.5		YEDS7 (SONY) TRACK 13
	44 KHz	L R	0 ± 1.5		TDV-540A (ABEX) TITLE 4,CHAPTER 16 AUDIO STREAM 3
Emphasis Characteristic[dB] Ref.1kHz 0dB	5 KHz	L R	-4.53±1.0		YEDS7 (SONY) TRACK 40
	16 KHz	L R	-9.04 ± 1.0		YEDS7 (SONY) TRACK 41
S/N [dB]		L R	> 105		YEDS7 (SONY) TRACK 23
Channel Separation [dB]		L→R R→L	> 95		YEDS7 (SONY) TRACK 30,34
Linearity [dB] -90dB playback		L R	89.5±3		YEDS7 (SONY) TRACK 22
T.H.D [%]		L R	< 0.01		YEDS7 (SONY) TRACK 1
Dynamic Range [dB] -60dB playback		L R	> 93		YEDS7 (SONY) TRACK 20
全高調波歪率 [%] DVD 96k		L R	< 0.01		TDV-540A (ABEX) TITLE 3, CHAPTER 1
Dynamic Range [dB] DVD 96k		L R	> 95		TDV-540A (ABEX) TITLE 3, CHAPTER 2
全高調波歪率 [%] DVD 48k		L R	< 0.01		TDV-540A (ABEX) TITLE 2, CHAPTER 1 AUDIO STREAM 2
Dynamic Range [dB] DVD 48k		L R	> 95		TDV-540A (ABEX) TITLE 2, CHAPTER 2 AUDIO STREAM 2

2. DIGITAL OUTPUT

1) OPTICAL OUT

JITTER 44.1kHz (mUI)		< 50mUI		Normal 44.1kHz CD Playback
JITTER 96kHz (mUI)		< 50mUI		Normal 96kHz DVD Playback

2) COAXIAL OUT

OUTPUT Level [mV] Peak to Peak Level at 75ohm Lo		500±50 (mV)		Normal CD or DVD Playback

MODEL NAME : DVD 37& DVD 37/230
Description : Characteristics Specification of Video
Test Disc : TDV-540A (ABEX) , MDVD-111 (TEAC) Serial NO.:
Test Conditions : 75Ω Load Terminated
AC Input : For USA (120V/60Hz) , For Europe (230V/50Hz)
Test Measuerment : VM-700T

4. Video Frequency Respoens (75Ω Terminated)

Measurement Item		Limit	Result	Test Disc
Composite [dB]	0.5MHz 0dB Ref.	0		MDVD-111 TITLE2,CHAPTER9 100% Multi Brust
	1MHz	0dB ± 2dB		
	2MHz	0dB ± 2dB		
	3MHz	0dB ± 2dB		
	4MHz	0dB ± 2dB		
	5.8MHz	-3dB ± 2dB		

Measurement Item		Limit	Result	Test Disc
S-Video Y [dB]	0.5MHz 0dB Ref.	0		MDVD-111 TITLE2,CHAPTER9 100% Multi Brust
	1MHz	0dB ± 2dB		
	2MHz	0dB ± 2dB		
	3MHz	0dB ± 2dB		
	4MHz	0dB ± 2dB		
	5.8MHz	-3dB ± 2dB		

Measurement Item		Limit	Result	Test Disc
Component Y [dB] Interace Mode	0.5MHz 0dB Ref.	0		MDVD-111 TITLE2,CHAPTER9 100% Multi Brust
	1MHz	0dB ± 2dB		
	2MHz	0dB ± 2dB		
	3MHz	0dB ± 2dB		
	4MHz	0dB ± 2dB		
	5.8MHz	-3dB ± 2dB		

MODEL NAME : DVD 37& DVD 37/230
Description : Characteristics Specification of Video
Test Disc : TDV-540A (ABEX) , MDVD-111 (TEAC) Serial NO.:
Test Conditions : 75Ω Load Terminated
AC Input : For USA (120V/60Hz) , For Europe (230V/50Hz)
Test Measuerment : VM-700T

1. Video Level Test (75Ω Terminated)

Measurement Item		Limit	Result	Test Disc
Video output [V]	Composite	1.0V ± 0.1V		MDVD-111 TITLE2,CHAPTER1 100% COLOR BAR
	S-Video Y	1.0V ± 0.1V		
	S-Video C	286mV ± 30mV		
	Component Y	1.0V ± 0.1V		
	Component Pb	700mV ± 100mV		
	Component Pr	700mV ± 100mV		
	Scart CVBS	1.0V ± 0.15V		
	Scart Red	700mV ± 100mV		
	Scart Green	700mV ± 100mV		
	Scart Blue	700mV ± 100mV		

** Pb/Pr & RGB Video Level check before please setting the Black Level off in the set-up menu **

2. Video S/N Raito Test (75Ω Terminated)

Measurement Item		Limit	Result	Test Disc
Video SNR [dB] 100KHz~4.2MHz Use SC Trap	Composite	≥ 65.0 dB		MDVD-111 TITLE2,CHAPTER 4 50% Gray Color
	S-Video Y	≥ 65.0 dB		
	Component Y	≥ 65.0 dB		
	Component Pb	≥ 65.0 dB		
	Component Pr	≥ 65.0 dB		

3. Chroma Signal AM.PM Test (75Ω Terminated)

Measurement Item		Limit	Result	Test Disc
Chroma AM [dB] 10KHz~500KHz	Composite Chroma	≥ 65.0 dB		TDV-540A TITLE2,CHAPTER17 100% Magenta Color
	S-Video Chroma	≥ 65.0 dB		
Chroma PM [dB] 10KHz~500KHz	Composite Chroma	≥ 60.0 dB		
	S-Video Chroma	≥ 60.0 dB		

2. DVD-Audio Part (Test Disc V-612 , JVC)

		Track Inform.	Limit	Downmix 2CH		Muiti 5 CH					SW
				LT	RT	FL	FR	SL	SR	C	
Output Level (V)		Tr.38 1KHz 0dB	2.1±0.2Vrms								
T.H.D (%) 20KHz LPF		Tr.38 1KHz 0dB	↓0.01%								
Frequency Respones (dB) Ref. : Tr. 38	48 / 24	Tr.59 17Hz	0±1.0dB								
		Tr.54 10KHz	0±1.0dB								
		Tr.53 20KHz	0±2.0dB								
	96 / 20	Tr.49 17Hz	0±1.0dB								
		Tr.45 10KHz	0±1.0dB								
		Tr.44 20KHz	0±2.0dB								
	192 / 24	Tr.22 17Hz	0±1.0dB								
		Tr.18 10KHz	0±1.0dB								
		Tr.17 20KHz	0±2.0dB								
S/N (dB) "A" Filter		Tr.40 Infinity Zero	↑90dB								
Dynamic Range (dB) 20KHz LPF		Tr.39 -60dB	↑85dB								

★ SW Level & THD --> Track 38 (30Hz) Play.

★ SW Frequency Respones -> Track 55(31Hz , 0dB) Reference

★ Track 54 (61Hz) , Track 53 (81Hz) , Track 51(127Hz) Play

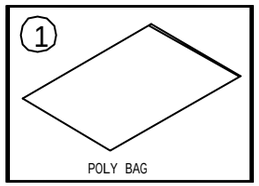
TROUBLESHOOTING GUIDE

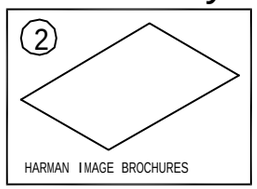
TROUBLESHOOTING GUIDE

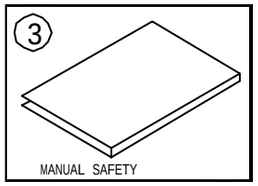
SYMPTOM	POSSIBLE CAUSE	SOLUTION
Unit does not turn on	• No AC power	• Check AC power plug and make certain any switched outlet is turned on.
Disc does not play	• Disc loaded improperly	• Load disc label-side up; align the disc with the guides and place it in its proper position.
	• Incorrect disc type	• Check to see that disc is SACD, CD, CD-R, CD-RW, VCD, MP3, WMA, JPEG, DVD-R, DVD-RW, DVD+R, DVD+RW (standard-conforming), DVD-Audio or DVD-Video; other types will not play.
	• Invalid Region Code	• Use Region 1 or Open Region (0) disc only.
	• Rating is above parental preset	• Enter password to override or change rating settings (see page 20).
No picture	• Intermittent connections	• Check all video connections.
	• Wrong input	• Check input selection of TV or receiver.
	• Progressive Scan output selected	• Use Progressive Scan mode only with compatible TV. Press **Progressive Scan/ Interlaced Button** ⑲ to toggle to the correct mode (see page 23).
	• Video Off feature active	• Press **Video Off Button** ⑯ to reactivate video circuitry.
	• **HDMI Output** ❸ is connected to a video display that is not HDCP-compliant.	• The **HDMI Output** ❸ may not be used with video displays that are not HDCP-compliant. Unplug the cable and select another audio and video connection (see pages 14 through 16).
No sound	• Intermittent connections	• Check all audio connections.
	• Incorrect digital audio selection	• Check digital audio settings on DVD 47 and on receiver.
	• DVD disc is in fast or slow mode	• There is no audio playback on DVD discs during fast or slow modes.
	• Surround receiver not compatible with 96kHz PCM audio	• Use analog audio outputs.
	• DVD Audio or SACD disc is loaded without using analog audio connection	• Use **6-Channel Audio Outputs** ⑩ or **Analog Audio Outputs** ❾.
Picture is distorted or jumps during fast forward or reverse play	• MPEG-2 decoding	• It is a normal artifact of DVD playback for pictures to jump or show some distortion during rapid play.
Some remote buttons do not operate during DVD play; prohibited symbol ⃠ appears (see below)	• Function not permitted at this time	• With most discs, some functions are not permitted at certain times (e.g., Track Skip) or at all (e.g., direct audio track selection).
The OSD menu is in a foreign language	• Incorrect OSD language	• Change the display language selection (see page 23).
The ⃠ symbol appears	• Requested function not available at this time	• Certain functions may be disabled by the DVD itself during passages of a disc.
Picture is displayed in the wrong aspect ratio	• Incorrect match of aspect ratio settings to disc	• Change aspect ratio settings (see page 23).
Remote control inoperative	• Weak batteries	• Change both batteries.
	• Sensor is blocked	• Clear path to sensor or use optional outboard remote sensor.
Disc will not copy to VCR	• Copy protection	• Many DVDs are encoded with copy protection to prevent copying to VCR.
Password not accepted.	• Incorrect password being used or password has been forgotten.	• Stop play of disc. Press and hold **Clear Button** ❹ until the display blinks. This resets the password and all settings to their defaults.

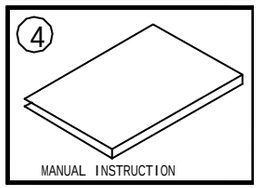
DVD37/230

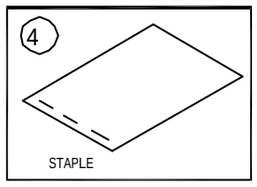
1. Instruction manual ass'y - Accessories





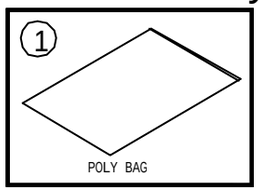


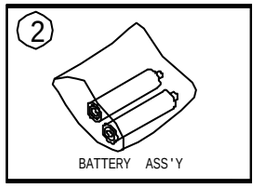


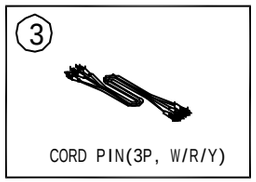


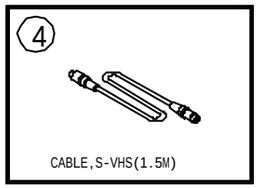
NO	DESCRIPTION	PARTS NO.	Q,ty
1	POLY BAG	CPB1061Y	1
2	HARMAN IMAGE BROCHURES	HQE1A273Z	1
3	SAFETY MANUAL	CQX1A1049Z	1
4	INSTRUCTION MANUAL	CQX1A1053Z	1
5	STAPLE	CPL0905	3

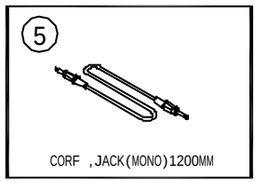
1. Cable ass'y - Accessories

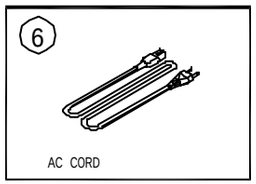


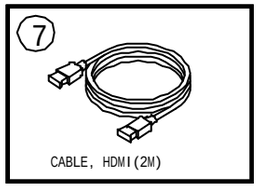


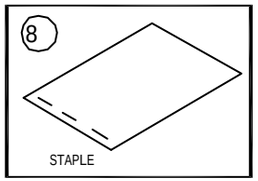






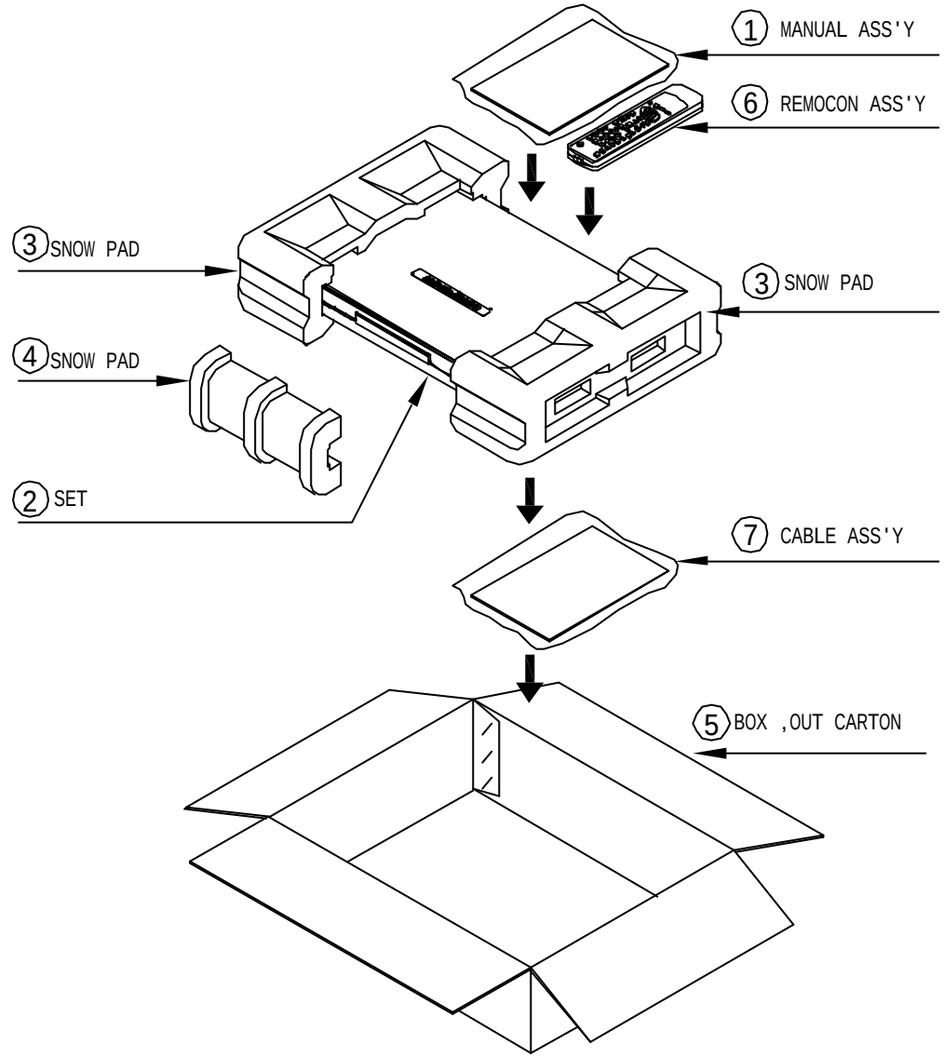






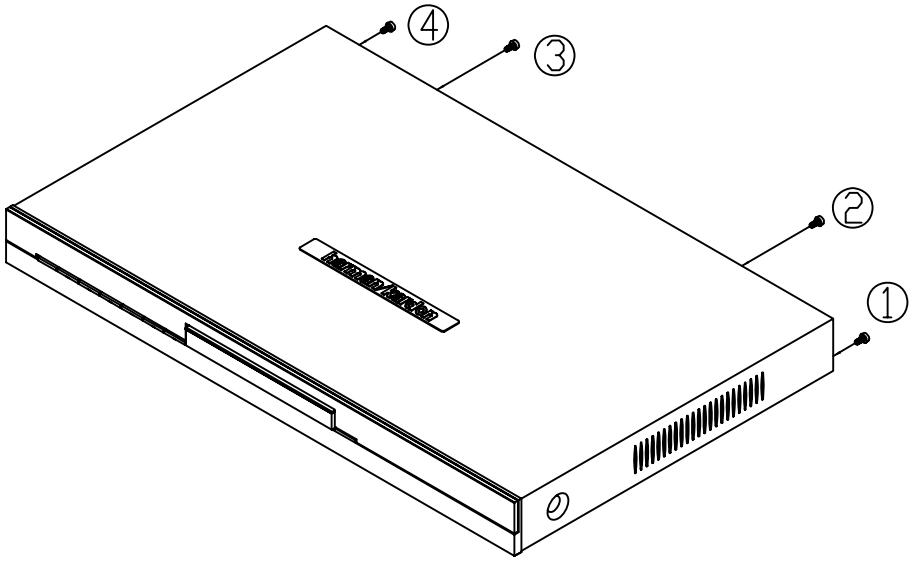
NO	DESCRIPTION	PARTS NO.	Q,ty
1	POLY BAG	CPB1061Y	1
2	BATTERY	CABR03P	2
3	CORD,PIN(3P,W/R/Y)	CJS4S004Z	1
4	CABLE,S-VHS(1.5M)	CJS01006Z	1
5	CORD,JACK(MONO)1200MM	CJS9D002Z	1
6	AC CORD	CJA2B020Z	1
7	CABLE,HDMI(2M)	CJS8T001Z	1
8	STAPLE	KPL0905	3

2. Package Drawing

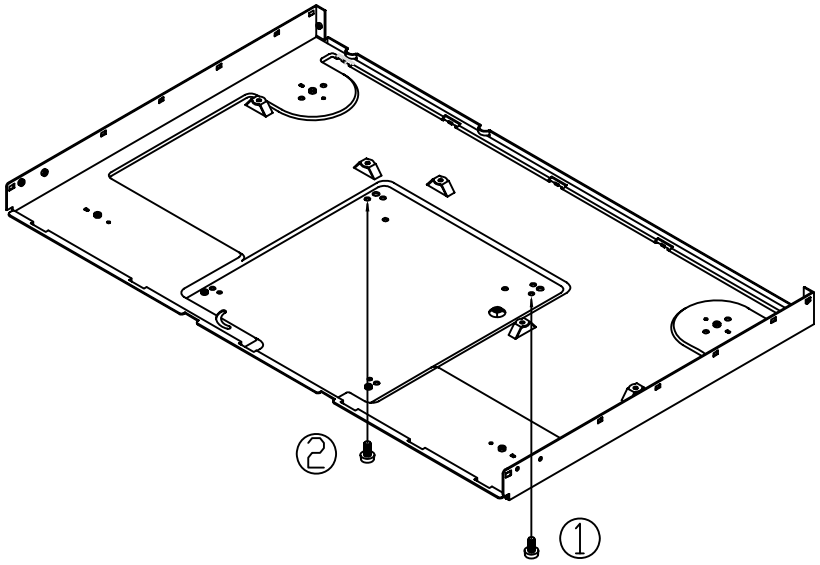


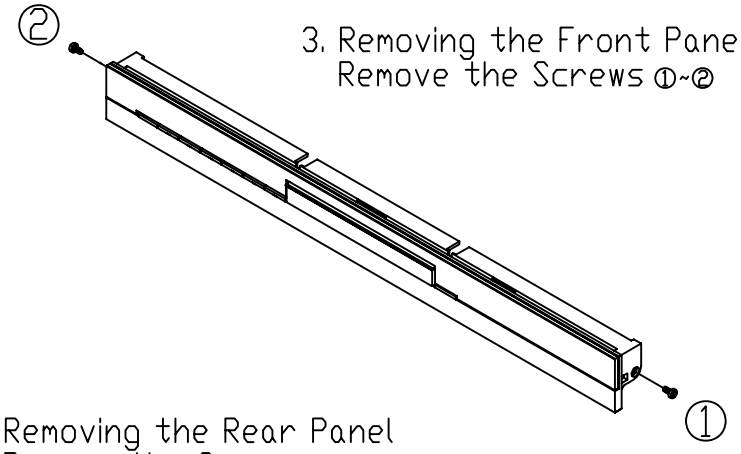
NO	DESCRIPTION	PARTS NO.	Q,ty
1	MANUAL ASS'Y	CQXDVD37A/230	1
2	SET	DVD37/230	1
3	SNOW,PAD	CPS1A714	2
4	SNOW,PAD	CPS1A715	1
5	BOX,OUT CARTON	CPG1A798V	1
6	REMOCON ASS'Y	CARTDVD37A	1
7	CABLE ASS'Y	CQXDVD47	1

1. Removing the Top Cabinet
Remove the Screws ①~④



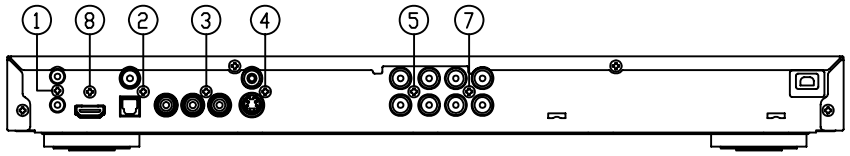
2. Removing the Bottom Chassis
Remove the Screws ①~②

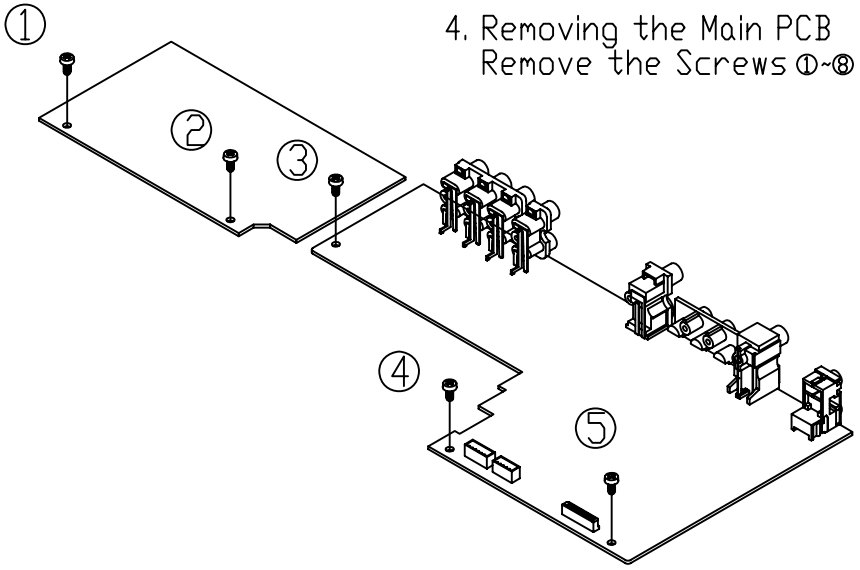




3. Removing the Front Panel
Remove the Screws ①~②

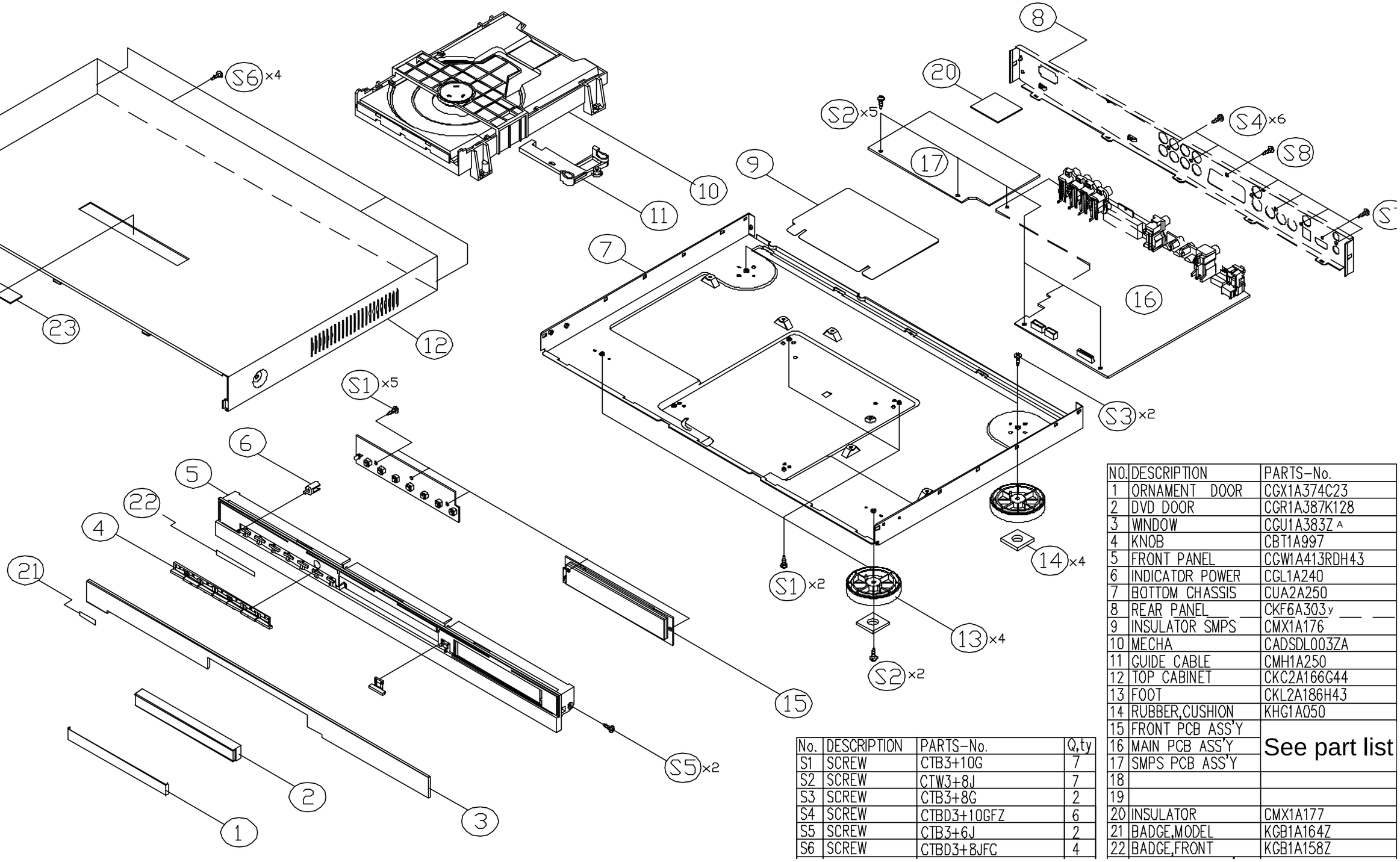
3. Removing the Rear Panel
Remove the Screws ①~⑧





4. Removing the Main PCB
Remove the Screws ①~⑧

EXPLODED VIEW



No.	DESCRIPTION	PARTS-No.	Q,ty
S1	SCREW	CTB3+10G	7
S2	SCREW	CTW3+8J	7
S3	SCREW	CTB3+8G	2
S4	SCREW	CTBD3+10GFZ	6
S5	SCREW	CTB3+6J	2
S6	SCREW	CTBD3+8JFC	4

NO.	DESCRIPTION	PARTS-No.
1	ORNAMENT DOOR	CGX1A374C23
2	DVD DOOR	CGR1A387K128
3	WINDOW	CGU1A383Z A
4	KNOB	CBT1A997
5	FRONT PANEL	CGW1A413RDH43
6	INDICATOR POWER	CGL1A240
7	BOTTOM CHASSIS	CUA2A250
8	REAR PANEL	CKF6A303y
9	INSULATOR SMPS	CMX1A176
10	MECHA	CADSDL003ZA
11	GUIDE CABLE	CMH1A250
12	TOP CABINET	CKC2A166G44
13	FOOT	CKL2A186H43
14	RUBBER,CUSHION	KHG1A050
15	FRONT PCB ASS'Y	See part list
16	MAIN PCB ASS'Y	
17	SMPS PCB ASS'Y	
18		
19		
20	INSULATOR	CMX1A177
21	BADGE,MODEL	KGB1A164Z
22	BADGE,FRONT	KGB1A158Z

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
	COP11842F	DVD37/230 MAIN PCB ASS'Y	DVD37A/230 (EUR)
	COP11842F-1	FRONT PCB DISPLAY ASS'Y	DVD37A/230 (EUR)
	COP11842F-2	FRONT PCB CONTROL ASS'Y	DVD37A/230 (EUR)
CN11	CJP24GA195ZM	SMT FFC/FPC WAFER(0.5MM PITCH	52559-2472 (PB FREE)
C100	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C101	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C102	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C103	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C104	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C106	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C107	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C110	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C112	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C113	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C115	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C117	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C120	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C122	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C124	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C126	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C127	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C129	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C131	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C132	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C133	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C138	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C140	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C141	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C143	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C144	CCUS1H103KC	CAP , CHIP	0.01UF ZF 1608
C146	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C148	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C149	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C151	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C152	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C153	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C154	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C156	CCUS1H180JA	CHIP, CAP 18PF/50V/1608	18PF/50V/1608
C156	CCUS1H180JA	CHIP, CAP 18PF/50V/1608	18PF/50V/1608
C157	CCUS1H330JA	CAP , CHIP	33PF JA 1608
C158	CCUS1H330JA	CAP , CHIP	33PF JA 1608
C159	CCUS1H562KC	CHIP CERAMIC CAP. 1608 (5600p)	5600PF KC 1608
C160	CCUS1H562KC	CHIP CERAMIC CAP. 1608 (5600p)	5600PF KC 1608
C161	CCUS1H562KC	CHIP CERAMIC CAP. 1608 (5600p)	5600PF KC 1608
C163	CCUS1H471JA	CAP , CHIP	470PF JA 1608
C164	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C165	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C166	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C167	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C168	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C169	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C170	CCUS1H102KC	CAP , CHIP	1000PF KC 1608

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
C172	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C173	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C174	CCUS1H333KC	CAP , CHIP	0.033PF KC 1608 SIZE
C175	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C176	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C178	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C179	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C180	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C181	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C183	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C185	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C186	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C187	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C188	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C189	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C190	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C191	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C192	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C193	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C194	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C195	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C196	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C197	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C199	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C200	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C201	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C204	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C205	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C207	CCUS1H272KC	CAP , CHIP	2700PF KC 1608
C208	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C209	CCUS1H273KC	CAP , CHIP	27000P KC 1608
C210	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C214	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C215	CCUS1H561JA	CAP , CHIP	560PF JA 1608
C217	CCUS1H273KC	CAP , CHIP	0.027UF KC 1608
C218	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C220	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C222	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C225	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C227	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C228	CCUS1H222KC	CAP , CHIP	2200PF KC 1608
C229	CCUS1H222KC	CAP , CHIP	2200PF KC 1608
C230	CCUS1H222KC	CAP , CHIP	2200PF KC 1608
C231	CCUS1H222KC	CAP , CHIP	2200PF KC 1608
C232	CCUS1H330JA	CAP , CHIP	33PF JA 1608
C234	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C235	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C237	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C240	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C242	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C244	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C245	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
C247	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C249	CCUS1H150JA	CHIP, CAP 15PF/50V/1608	15PF JA 1608
C250	CCUS1H150JA	CHIP, CAP 15PF/50V/1608	15PF JA 1608
C252	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C253	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C254	CCUS1H272KC	CAP , CHIP	2700PF KC 1608
C255	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C256	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C257	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C260	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C261	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C262	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C263	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C266	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C267	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C276	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C277	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C279	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C280	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C281	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C282	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C283	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C284	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C285	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C286	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C287	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C295	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C304	HCSHB21A220B	CAP , TANTAL B2 SIZE	22UF/50V
C306	HCSHB21A220B	CAP , TANTAL B2 SIZE	22UF/50V
C307	HCSHB21A220B	CAP , TANTAL B2 SIZE	22UF/50V
C308	HCSHB21A220B	CAP , TANTAL B2 SIZE	22UF/50V
C310	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C311	CCUS1H560JA	CAP , CHIP	56PF JA 1608
C312	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C313	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C336	CCUS1H682KC	CAP , CHIP	6800PF KB 1608
C337	CCUS1H223KC	CAP , CHIP	0.022UF KC 1608
C338	CCUS1H221JA	CAP , CHIP	220PF JA 1608
C339	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C346	CCUS1H070DA	CAP , CHIP	7PF D 1608
C380	CCUS1H150JA	CHIP, CAP 15PF/50V/1608	15PF JA 1608
C401	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C402	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C403	CCUS1H102KC	CAP , CHIP	1000PF KC 1608
C405	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C406	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C408	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C429	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C430	CRJ10DJ0R0T	RES , CHIP	0 ohm 1608
C431	CCUS1H221JA	CAP , CHIP	220PF JA 1608
C432	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C511	CCUS1H151JA	CAP , CHIP	150PF JA 1608

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
C531	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C533	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C552	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C553	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C555	CCUS1H150JA	CHIP, CAP 15PF/50V/1608	15PF JA 1608
C556	CCUS1H150JA	CHIP, CAP 15PF/50V/1608	15PF JA 1608
C578	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C580	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C581	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C584	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C585	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C593	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C594	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C615	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C617	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C620	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C630	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C631	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C636	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C638	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C639	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C641	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C644	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C646	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C650	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C657	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C659	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C660	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C662	CCUS1H391JA	CAP , CHIP	390PF JA 1608
C664	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C665	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C668	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C671	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C672	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C674	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C677	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C678	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C679	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C809	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C810	CCUS1H560JA	CAP , CHIP	56PF JA 1608
C812	CCUS1H101JA	CAP , CHIP	100PF JA 1608
C817	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C819	CCUS1H101JA	CAP , CHIP	100PF JA 1608
C820	CCUS1H101JA	CAP , CHIP	100PF JA 1608
C822	CCUS1H560JA	CAP , CHIP	56PF JA 1608
C823	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
C828	CCUS1H220JA	CAP , CHIP	22PF JA 1608
C830	CCUS1H150JA	CHIP, CAP 15PF/50V/1608	15PF JA 1608
C831	CCUS1H150JA	CHIP, CAP 15PF/50V/1608	15PF JA 1608
C834	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608
D101	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11
D102	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
D501	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11
D502	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11
D511	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11
D601	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11
D602	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11
D603	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11
IC10	HVIZR36778	IC,MPEG (ZORAN)	ZR36778
IC11	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	1117S-3.3V
IC12	HVILM1117S-1V8	I.C , REGULATOR (1.8V)	LM1117-1V8
IC13	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	1117S-3.3V
IC14	HVILM1117S-1V8	I.C , REGULATOR (1.8V)	LM1117-1V8
IC15	HVIAT24C08N10SC	I.C	AT24C08N10SC2.7
IC16	HVISAA7893HLC2	IC,DSD DECODER (Philips)	SAA7893HL/C2 (PB FR
IC17	HVI74VHC04MX	I.C , INVERTER	74VHC04M
IC18	HVIM12L64164A7T	IC, 64M SDRAM (4X16)	M12L64164A7T
IC19	HVIZR36721	IC,HDMI TRANSMITTER(ZORAN)	ZR36721
IC20	HVITL3472IDR	IC,OP AMP 8-SOIC (TI)	TL3472
IC21	HVIM29W160ET70N	IC,16M FLASH (ST)	M29W160ET-70N6
IC22	HVIM12L64164A7T	IC, 64M SDRAM (4X16)	M12L64164A7T
IC23	HVIAM5888SLF	I. C , Motor Driver(AMtek,Pb f	AM5888S L/F
IC24	HVIZR36707	IC,RF (ZORAN)	ZR36707
IC40	HVICS4382-KQ	I.C , DAC	CS4382-KQ
IC41	BVIBH7862FS	IC , 6CH VIDEO DRIVER	ROHM (BH7862FS)
IC42	HVIBA7660FS	IC , R.G.B DRIVER	BA7660FS
IC43	HVI74LVC157ADBR	I.C , MULTIPLEXER	SN74LVC157A
IC44	HVI74LVC157ADBR	I.C , MULTIPLEXER	SN74LVC157A
IC45	HVIST72F324K2	IC,FLASH (ST)	ST72F324K2
IC47	HVITC74HCT7007F	I.C	TC74HC7007AFEL
IC51	HVILM1117S-5.0	IC REGULATOR/SOT-223	LM1117-1V8 (1.8V)
IC52	HVINJM2068MDTE1	I.C , OP AMP	NJM2068MD-TE1
IC53	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	1117S-3.3V
IC54	HVINJM2068MDTE1	I.C , OP AMP	NJM2068MD-TE1
IC55	HVINJM2068MDTE1	I.C , OP AMP	NJM2068MD-TE1
IC56	HVILM1117S-5.0	IC REGULATOR/SOT-223	LM1117-5V0 (5V)
IC57	HVTHN1K05FU	MOS FET	HN1K05FU
JK07	HJJ9H003Z	JACK,HDMI (JALCO)	YKF45-7009
L101	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L102	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L103	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L104	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L105	HLQ06E100KRZ	INDUCTOR , CHIP	10UH 3225 SIZE
L106	HLQ06E100KRZ	INDUCTOR , CHIP	10UH 3225 SIZE
L107	HLQ06E100KRZ	INDUCTOR , CHIP	10UH 3225 SIZE
L109	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L110	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L111	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L112	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L113	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L114	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L115	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L116	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L117	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A

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Ref#	Component	Description	Drawing No
L118	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L119	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L120	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L121	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L122	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L123	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L124	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L125	HLZ9R006Z	BEAD , CHIP	
L126	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L127	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L128	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L217	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L518	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L519	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L520	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L521	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L522	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L601	BLZ9R004Z	BEAD CHIP 90 OHM (2012 SIZE)	ACM2012H-900
L602	BLZ9R004Z	BEAD CHIP 90 OHM (2012 SIZE)	ACM2012H-900
L603	BLZ9R004Z	BEAD CHIP 90 OHM (2012 SIZE)	ACM2012H-900
L604	BLZ9R004Z	BEAD CHIP 90 OHM (2012 SIZE)	ACM2012H-900
L610	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L611	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L612	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L613	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L614	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L615	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L616	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L617	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L696	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L801	HLQ08ER68KRZ	CHIP FERRITE INDUCTOR	2012-R68UH
L802	HLQ08E1R8KRZ	CHIP , COIL (1.8UH)	1.8UH 2012 SIZE
L803	HLQ08E1R8KRZ	CHIP , COIL (1.8UH)	1.8UH 2012 SIZE
L804	HLQ09E8R2KRZ	CHIP , COIL	8.2UH 2012 SIZE
L805	HLQ08ER68KRZ	CHIP FERRITE INDUCTOR	2012-R68UH
L806	HLQ08ER39KRZ	CHIP FERRITE INDUCTOR	2012-R39UH
L807	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L808	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A
L809	HLQ09E8R2KRZ	CHIP , COIL	8.2UH
L884	HLQ08E1R8KRZ	CHIP , COIL (1.8UH)	1.8UH 2012 SIZE
Q105	HVTKTA1664YP	tr	KTA1664
Q106	HVTKTA1664YP	tr	KTA1664
Q108	HVT2N3904SP	TR, CHIP (KEC)	2N3904S-RTK/PS
Q109	HVT2N3904SP	TR, CHIP (KEC)	2N3904S-RTK/PS
Q110	HVT2N3904SP	TR, CHIP (KEC)	2N3904S-RTK/PS
Q307	HVT2SA1955B	T.R, TE85L,F, SSM Type, hFE=B	TE85L,F SSM TYPE HFE
Q308	HVT2N3904SP	TR, CHIP (KEC)	2N3904S-RTK/PS
Q315	HVTKRC107S	TR , CHIP	KRC107S
Q316	HVTKTA1504SYRTK	T.R , CHIP	KTA1504S Y RTK
Q404	HVT2N3904SP	TR, CHIP (KEC)	2N3904S-RTK/PS
Q407	HVTKRC107S	TR , CHIP	KRC107S
Q408	HVTKRA107ST	T.R , CHIP	KRA107S

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Ref#	Component	Description	Drawing No
Q501	HVTKTA1504SYRTK	T.R , CHIP	KTA1504S Y RTK
Q502	HVTKTC3875SYRTK	T.R , CHIP	KTC3875S Y RTK
Q604	HVTKRA107ST	T.R , CHIP	KRA107S
Q606	HVTKRA107ST	T.R , CHIP	KRA107S
Q607	HVTKRA107ST	T.R , CHIP	KRA107S
Q608	HVTKRC107S	TR , CHIP	KRC107S
Q609	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q610	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q611	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q612	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q613	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q614	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q615	HVTKRA107ST	T.R , CHIP	KRA107S
Q616	HVTKRC107S	TR , CHIP	KRC107S
Q617	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q618	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q619	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q620	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q621	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q622	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q801	HVTKRC107S	TR , CHIP	KRC107S
Q802	HVTKRC107S	TR , CHIP	KRC107S
Q803	HVTKTA1504SYRTK	T.R , CHIP	KTA1504S Y RTK
Q804	HVTKTA1504SYRTK	T.R , CHIP	KTA1504S Y RTK
Q805	HVTKTD1304T	T.R , CHIP (MUTE)	KTD1304
Q806	HVTKRA107ST	T.R , CHIP	KRA107S
Q821	HVTKTA1504SYRTK	T.R , CHIP	KTA1504S Y RTK
R100	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R101	CRJ10DF4700T	RES, CHIP 470 OHM/1608/1%	470 OHM(1%) 1608 SIZ
R102	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R103	CRJ10DF4300T	RES	430 OHM(1%) 1608 SIZ
R104	CRJ10DF3920T	RES. CHIP (392R 1%)	3.9K OHM 1608 SIZE
R105	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R106	CRJ104DJ101T	RES, ARRAY, 100R (1608)	100 OHM 1608 SIZE
R107	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R108	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE
R109	CRJ10DJ472T	RES , CHIP	100 OHM 1608 SIZE
R110	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R111	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R112	CRJ10DJ202T	RES , CHIP	2K OHM 1608 SIZE
R113	CRJ10DJ202T	RES , CHIP	2K OHM 1608 SIZE
R114	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE
R115	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R116	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE
R117	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE
R118	CRJ10DJ103T	RES , CHIP	10K OHM1608 SIZE
R119	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R120	CRJ10DJ123T	RES , CHIP	12K OHM 1608 SIZE
R121	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R122	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R123	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R124	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
R125	CRJ10DJ113T	RES , CHIP	11K OHM 1608 SIZE
R126	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R127	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R128	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE
R129	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R130	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R131	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R132	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R133	CRJ10DF3920T	RES. CHIP (392R 1%)	3.9K OHM 1608 SIZE
R134	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R135	CRJ10DJ100T	RES , CHIP	10 OHM 1608 SIZE
R136	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R137	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R138	CRJ10DJ100T	RES , CHIP	10 OHM 1608 SIZE
R139	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R140	CRJ10DJ133T	RES , CHIP	13K OHM 1608 SIZE
R141	CRJ10DJ474T	RES , CHIP	470K OHM 1608 SIZE
R142	CRJ10DJ474T	RES , CHIP	470K OHM 1608 SIZE
R143	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R144	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R145	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE
R146	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R147	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE
R148	CRJ10DJ750T	RES , CHIP	57 OHM 1608 SIZE
R149	CRJ104DJ470T	RES , 4ARRAY (1608*4)	47 OHM/1608X4
R150	CRJ104DJ470T	RES , 4ARRAY (1608*4)	47 OHM/1608X4
R151	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R152	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R153	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R154	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R155	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE
R156	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE
R157	CRJ10DJ0R0T	RES , CHIP	1608 SIZE
R158	CRJ104DJ101T	RES, ARRAY, 100R (1608)	100R (1608)
R159	CRJ10DJ472T	RES , CHIP	1608 SIZE
R160	CRJ10DJ330T	RES , CHIP	1608 SIZE
R161	CRJ10DJ0R0T	RES , CHIP	1608 SIZE
R162	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R163	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R164	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R165	CRJ10DJ330T	RES , CHIP	1608 SIZE
R166	CRJ10DJ330T	RES , CHIP	1608 SIZE
R167	CRJ10DJ330T	RES , CHIP	1608 SIZE
R168	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R169	CRJ10DJ750T	RES , CHIP	1608 SIZE
R170	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R171	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R172	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R173	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R174	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R175	CRJ10DJ912T	RES , CHIP	9.1K OHM/1608
R176	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
R177	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R178	CRJ10DJ272T	RES , CHIP	2.7K OHM 1608 SIZE
R180	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R181	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R182	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R183	CRJ10DF1202T	RES , CHIP 1%	1.2K OHM(1%) 1608 SI
R184	CRJ10DJ471T	RES , CHIP	470 OHM 1608 SIZE
R185	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R186	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R187	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R188	CRJ10DJ113T	RES , CHIP	11K OHM 1608 SIZE
R189	CRJ10DJ105T	RES , CHIP	1M OHM 1608 SIZE
R190	CRJ10DJ223T	RES , CHIP	22K OHM 1608 SIZE
R191	CRJ10DJ223T	RES , CHIP	22K OHM 1608 SIZE
R192	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R193	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R194	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R195	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE
R196	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R197	CRJ10DJ753T	RES , CHIP	75K OHM 1608 SIZE
R198	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R199	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R200	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R201	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R202	CRJ10DJ622T	RES , CHIP	6.2K OHM 1608 SIZE
R203	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE
R204	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE
R205	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE
R206	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R207	CRJ10DF4700T	RES, CHIP 470 OHM/1608/1%	470 OHM(1%) 1608 SIZ
R209	CRJ10DF1002T	RES , CHIP 1%	10K OHM(1%) 1608 SIZ
R210	CRJ10DF1002T	RES , CHIP 1%	10K OHM(1%) 1608 SIZ
R211	CRJ10DF1002T	RES , CHIP 1%	10K OHM(1%) 1608 SIZ
R212	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R213	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R214	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R215	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R216	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R217	CRJ10DJ330T	RES , CHIP	1608 SIZE
R218	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4
R219	CRJ10DJ273T	RES , CHIP	27K OHM 1608 SIZE
R220	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE
R221	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE
R222	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE
R223	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R224	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R225	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R226	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R227	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R228	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE
R230	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R241	CRJ10DF75R0T	RES, CHIP 1% 75 OHM	75 OHM, 1%

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Ref#	Component	Description	Drawing No
R243	CRJ10DF75R0T	RES, CHIP 1% 75 OHM	75 OHM, 1%
R244	CRJ10DF75R0T	RES, CHIP 1% 75 OHM	75 OHM, 1%
R265	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R284	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R285	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R287	CRJ10DJ113T	RES , CHIP	11K OHM 1608 SIZE
R297	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R298	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R299	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R301	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R302	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R303	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R305	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R306	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R307	CRJ10DJ272T	RES , CHIP	2.7K OHM 1608 SIZE
R308	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R309	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R377	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R404	CRJ10DJ333T	RES , CHIP	33K OHM 1608 SIZE
R409	CRJ10DJ100T	RES , CHIP	10 OHM 1608 SIZE
R410	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R412	CRJ10DJ681T	RES , CHIP	680 OHM 1608 SIZE
R413	CRJ10DJ821T	RES , CHIP	820 OHM 1608 SIZE
R414	CRJ10DJ122T	RES , CHIP	1.2K OHM 1608 SIZE
R415	CRJ10DJ152T	RES , CHIP	1.5K OHM 1608 SIZE
R416	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R417	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R418	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R419	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R420	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE
R421	CRJ10DJ680T	RES , CHIP	68 OHM 1608 SIZE
R422	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE
R423	CRJ10DJ820T	RES , CHIP	82 OHM 1608 SIZE
R424	CRJ10DJ4R7T	RES , CHIP	4.7 OHM 1608 SIZE
R425	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R501	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE
R502	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE
R503	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R504	CRJ10DJ473T	RES , CHIP	47K OHM 1608 SIZE
R505	CRJ10DJ470T	RES , CHIP	47 OHM 1608 SIZE
R506	CRJ10DJ271T	RES , CHIP	270 OHM 1608 SIZE
R511	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R512	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R513	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R514	CRJ10DJ100T	RES , CHIP	10 OHM 1608 SIZE
R515	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R516	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R517	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R518	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE
R519	CRJ10DJ473T	RES , CHIP	47K OHM 1608 SIZE
R522	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R533	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
R544	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R549	CRJ10DJ105T	RES , CHIP	1M OHM 1608 SIZE
R552	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R553	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R564	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE
R593	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R600	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R601	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R602	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R603	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R604	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R605	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R606	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R607	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R608	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R609	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R611	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R612	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R618	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R619	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE
R620	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R621	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R622	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R623	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R624	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R625	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R626	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R627	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R628	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R629	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R630	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R631	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R632	CRJ10DJ104T	RES , CHIP	1M OHM 1608 SIZE
R633	CRJ10DJ104T	RES , CHIP	1M OHM 1608 SIZE
R641	CRJ10DJ224T	RES , CHIP	220K OHM 1608 SIZE
R642	CRJ10DJ224T	RES , CHIP	220K OHM 1608 SIZE
R650	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R651	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R652	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R653	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R654	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R655	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R656	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R657	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R658	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R659	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R660	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R661	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R662	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE
R663	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE
R664	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R665	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
R666	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R667	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R668	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE
R669	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE
R670	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R671	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R672	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R673	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R674	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE
R675	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R676	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R677	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R678	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R679	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R680	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R681	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R682	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R683	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R684	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R685	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE
R686	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R687	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R688	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R689	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R690	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R691	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R692	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R694	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R695	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R698	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R699	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE
R726	CRJ10DJ474T	RES , CHIP	470K OHM 1608 SIZE
R727	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R728	CRJ10DJ223T	RES , CHIP	22K OHM 1608 SIZE
R729	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R730	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R731	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R732	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R733	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R734	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R735	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R736	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R737	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R738	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R739	CRJ10DJ224T	RES , CHIP	220K OHM 1608 SIZE
R744	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R745	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R746	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R747	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R748	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R749	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R801	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
R802	CRJ10DJ820T	RES , CHIP	82 OHM 1608 SIZE
R803	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R806	CRJ10DJ820T	RES , CHIP	82 OHM 1608 SIZE
R807	CRJ10DJ680T	RES , CHIP	68 OHM 1608 SIZE
R808	CRJ10DJ680T	RES , CHIP	68 OHM 1608 SIZE
R809	CRJ10DJ680T	RES , CHIP	68 OHM 1608 SIZE
R810	CRJ10DJ471T	RES , CHIP	470 OHM 1608 SIZE
R811	CRJ10DJ471T	RES , CHIP	470 OHM 1608 SIZE
R812	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R813	CRJ10DJ821T	RES , CHIP	820 OHM 1608 SIZE
R814	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE
R815	CRJ10DJ181T	RES , CHIP	1608 SIZE
R816	CRJ10DJ390T	RES , CHIP	39 OHM 1608 SIZE
R817	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE
R818	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE
R821	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R823	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE
R824	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE
R825	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE
R826	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE
R827	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R828	CRJ18AJ221T	RES , CHIP	220 OHM 1608 SIZE
R829	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE
R830	CRJ10DJ390T	RES , CHIP	39 OHM 1608 SIZE
R831	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE
R832	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE
R833	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE
R834	CRJ10DJ820T	RES , CHIP	82 OHM 1608 SIZE
R878	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE
R879	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE
R880	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R895	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE
R896	CRJ10DJ680T	RES , CHIP	68 OHM 1608 SIZE
X101	HOX27000E180S	CRYSTAL , CHIP(27MHZ,SMD)	HC-49/US
C105	CCEA1CH470T	CAP , ELECT	47UF 16V
C108	CCEA1CH101T	CAP , ELECT	100UF 16V
C109	CCEA1CH101T	CAP , ELECT	100UF 16V
C111	CCEA1CH101T	CAP , ELECT	100UF 16V
C114	CCEA1CH101T	CAP , ELECT	100UF 16V
C116	CCEA1CH101T	CAP , ELECT	100UF 16V
C118	CCEA1CH101T	CAP , ELECT	100UF 16V
C119	CCEA1CH101T	CAP , ELECT	100UF 16V
C121	CCEA1CH101T	CAP , ELECT	100UF 16V
C123	CCEA1CH101T	CAP , ELECT	100UF 16V
C125	CCEA1CH101T	CAP , ELECT	100UF 16V
C128	CCEA1CH101T	CAP , ELECT	100UF 16V
C130	CCEA1CH101T	CAP , ELECT	100UF 16V
C137	CCEA1CH470T	CAP , ELECT	47UF 16V
C139	CCEA1CH470T	CAP , ELECT	47UF 16V
C142	CCEA1CH470T	CAP , ELECT	47UF 16V
C150	CCEA1CH101T	CAP , ELECT	100UF 16V
C155	CCEA1CH470T	CAP , ELECT	47UF 16V

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
C177	CCEA1CH101T	CAP , ELECT	100UF 16V
C182	CCEA1CH470T	CAP , ELECT	47UF 16V
C184	CCEA1CH470T	CAP , ELECT	47UF 16V
C198	CCEA1CH101T	CAP , ELECT	100UF 16V
C202	CCEA1CH470T	CAP , ELECT	47UF 16V
C203	CCEA1CH470T	CAP , ELECT	47UF 16V
C206	CCEA1CH470T	CAP , ELECT	47UF 16V
C213	CCEA1CH221T	CAP , ELECT	220UF 16V
C219	CCEA1CH470T	CAP , ELECT	47UF 16V
C221	CCEA1CH101T	CAP , ELECT	100UF 16V
C223	CCEA1CH101T	CAP , ELECT	100UF 16V
C224	CCEA1CH101T	CAP , ELECT	100UF 16V
C226	CCEA1CH101T	CAP , ELECT	100UF 16V
C233	CCEA1CH101T	CAP , ELECT	100UF 16V
C236	CCEA1CH470T	CAP , ELECT	47UF 16V
C241	CCEA1CH470T	CAP , ELECT	47UF 16V
C243	CCEA1CH470T	CAP , ELECT	47UF 16V
C251	CCEA1CH470T	CAP , ELECT	47UF 16V
C258	CCEA1HH4R7T	CAP , ELECT	4.7UF 50V
C301	CCEA1CH101T	CAP , ELECT	100UF 16V
C404	CCEA1CKS470T	CAP , ELECT	47UF 16V
C504	CCEA1CH221T	CAP , ELECT	220UF 16V
C508	CCEA1CH221T	CAP , ELECT	220UF 16V
C510	CCEA1HH4R7T	CAP , ELECT	4.7UF 50V
C530	CCEA1CH221T	CAP , ELECT	220UF 16V
C532	CCEA1CH221T	CAP , ELECT	220UF 16V
C548	CCEA1CH221T	CAP , ELECT	220UF 16V
C549	CCEA1CH221T	CAP , ELECT	220UF 16V
C561	CCEA1CH100T	CAP , ELECT	10UF 16V
C562	CCEA1HH1R0T	CAP , ELECT	1UF 50V
C574	CCEA1CH221T	CAP , ELECT	220UF 16V
C579	CCEA1CH221T	CAP , ELECT	220UF 16V
C582	CCEA1CH470T	CAP , ELECT	47UF 16V
C583	CCEA1CH221T	CAP , ELECT	220UF 16V
C586	CCEA1CH221T	CAP , ELECT	220UF 16V
C616	CCEA1CH220T	CAP , ELECT	22UF 16V
C618	CCEA1CH101T	CAP , ELECT	100UF 16V
C628	CCEA1CH101T	CAP , ELECT	100UF 16V
C629	CCEA1CH101T	CAP , ELECT	100UF 16V
C637	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C640	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C642	CCEA1CH220T	CAP , ELECT	22UF 16V
C643	CCEA1CH220T	CAP , ELECT	22UF 16V
C645	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C648	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C653	CCEA1CH220T	CAP , ELECT	22UF 16V
C658	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C661	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C666	CCEA1CH101T	CAP , ELECT	100UF 16V
C667	CCEA1CH101T	CAP , ELECT	100UF 16V
C669	CCEA1CH101T	CAP , ELECT	100UF 16V
C670	CCEA1CH101T	CAP , ELECT	100UF 16V

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
C673	CCEA1CH101T	CAP , ELECT	100UF 16V
C675	CCEA1CH470T	CAP , ELECT	47UF 16V
C676	CCEA1HH1R0T	CAP , ELECT	1UF 50V
C680	CCEA1CH221T	CAP , ELECT	220UF 16V
C681	CCEA1CH101T	CAP , ELECT	100UF 16V
C685	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C687	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C688	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C689	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C690	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C692	HCQI1H222JZT	CAP , MYLAR	2200PF 50V J
C733	CCEA1HH3R3T	CAP , ELECT	3.3UF 50V
C751	CCEA1CH220T	CAP , ELECT	22UF 16V
C752	CCEA1CH220T	CAP , ELECT	22UF 16V
C795	CCEA1CH221T	CAP , ELECT	220UF 16V
C801	CCEA1AH331T	CAP , ELECT	330UF 10V
C802	CCEA1AH331T	CAP , ELECT	330UF 10V
C803	CCEA1CH220T	CAP , ELECT	22UF 16V
C804	CCEA1CH101T	CAP , ELECT	100UF 16V
C811	CCEA1AH331T	CAP , ELECT	330UF 10V
C813	CCEA1AH331T	CAP , ELECT	330UF 10V
C815	CCEA1AH331T	CAP , ELECT	330UF 10V
C818	CCEA1AH331T	CAP , ELECT	330UF 10V
C824	CCEA1HH1R0T	CAP , ELECT	1UF 50V
C825	CCEA1HH1R0T	CAP , ELECT	1UF 50V
C826	CCEA1CH470T	CAP , ELECT	47UF 16V
C827	CCEA1CH470T	CAP , ELECT	47UF 16V
C829	CCEA1AH471T	CAP , ELECT	470UF 10V
C835	CCEA1CH221T	CAP , ELECT	220UF 16V
C882	CCEA1AH471T	CAP , ELECT	470UF 10V
C891	CCEA1AH471T	CAP , ELECT	470UF 10V
IC50	HVIKA79L08AZT	REGULATOR, -8V	KA79LXXAZTA
Q605	HVTKSA916YT	T.R	KSA916Y
S401	HST1A020ZT	SW , TACT	switch, Front panel
S402	HST1A020ZT	SW , TACT	switch, Front panel
S403	HST1A020ZT	SW , TACT	switch, Front panel
S404	HST1A020ZT	SW , TACT	switch, Front panel
S405	HST1A020ZT	SW , TACT	switch, Front panel
S406	HST1A020ZT	SW , TACT	switch, Front panel
S407	HST1A020ZT	SW , TACT	switch, Front panel
S408	HST1A020ZT	SW , TACT	switch, Front panel
	CMD1A504	BRACKET , FIP	
BN01	CWB1C912060EN	WIRE ASS'Y	12Pin, 60mm
BN07	CWB1A906190EN	WIRE ASS'Y	6Pin, 190mm
CN01	CJP15GA117ZY	WAFER , CARD CABLE	15Pin connector
CN03	CJP07GA01ZY	WAFER, STRAIGHT, 7PIN	7Pin connector
CN05	CJP15GB113ZY	WAFER	15Pin connector
CN07	CJP06GA19ZY	WAFER, STRAIGHT, 6PIN	6Pin connector
CN12	CJP05GA19ZY	WAFER, STRAIGHT, 5PIN	5Pin connector
CN13	CJP06GA19ZY	WAFER, STRAIGHT, 6PIN	6Pin connector
D103	CVD1N4003ST	RECT , DIODE	1N4003
D104	CVD1N4003ST	RECT , DIODE	1N4003

FRONT AND MAIN PCB

Ref#	Component	Description	Drawing No
D105	CVD1N4003ST	RECT , DIODE	1N4003
D107	CVD1N4003ST	RECT , DIODE	1N4003
D109	CVD1N4003ST	RECT , DIODE	1N4003
D110	CVD1N4003ST	RECT , DIODE	1N4003
D401	CVD50BOBBWGA	L.E.D , 2 COLOR (ORG , BLUE)	TOL-50BOBBWGA
ET01	CMC1A111	PLATE , EARTH	
ET02	CMC1A111	PLATE , EARTH	
F401	HFL13BT229GINK	F.I.P	13-BT-229GINK
IC46	BVIKP1010B	IC, PHOTO COUPLER	
IC49	HVIKIA7808API	REGULATOR, +8V	KIA7808 (KEC)
IC61	HRVKSM603TH2	SENSOR IR	KSM-603TH2
JK01	CJJ4R041Z	6P JACK, BOARD	RCA-601DAG-11
JK02	CJJ4N067Z	2P, JACK	RCA-201DAG-01
JK03	CJJ4S043Z	JACK , BOARD	
JK04	CJJ9N003Z	JACK , (S-VIDEO+VHS)	
JK05	CJJ6K003Z	JACK, SCART	CS-1071PB
JK06	HJS9U008Z	Optical+Coaxial Jack (Gold Pla	YKC22-0732N
JK08	HJJ1D002Z	JACK, HOSIDEN	SR7400
X501	HOX08000E160C	CRYSTAL 8MHz	

SMPS PCB

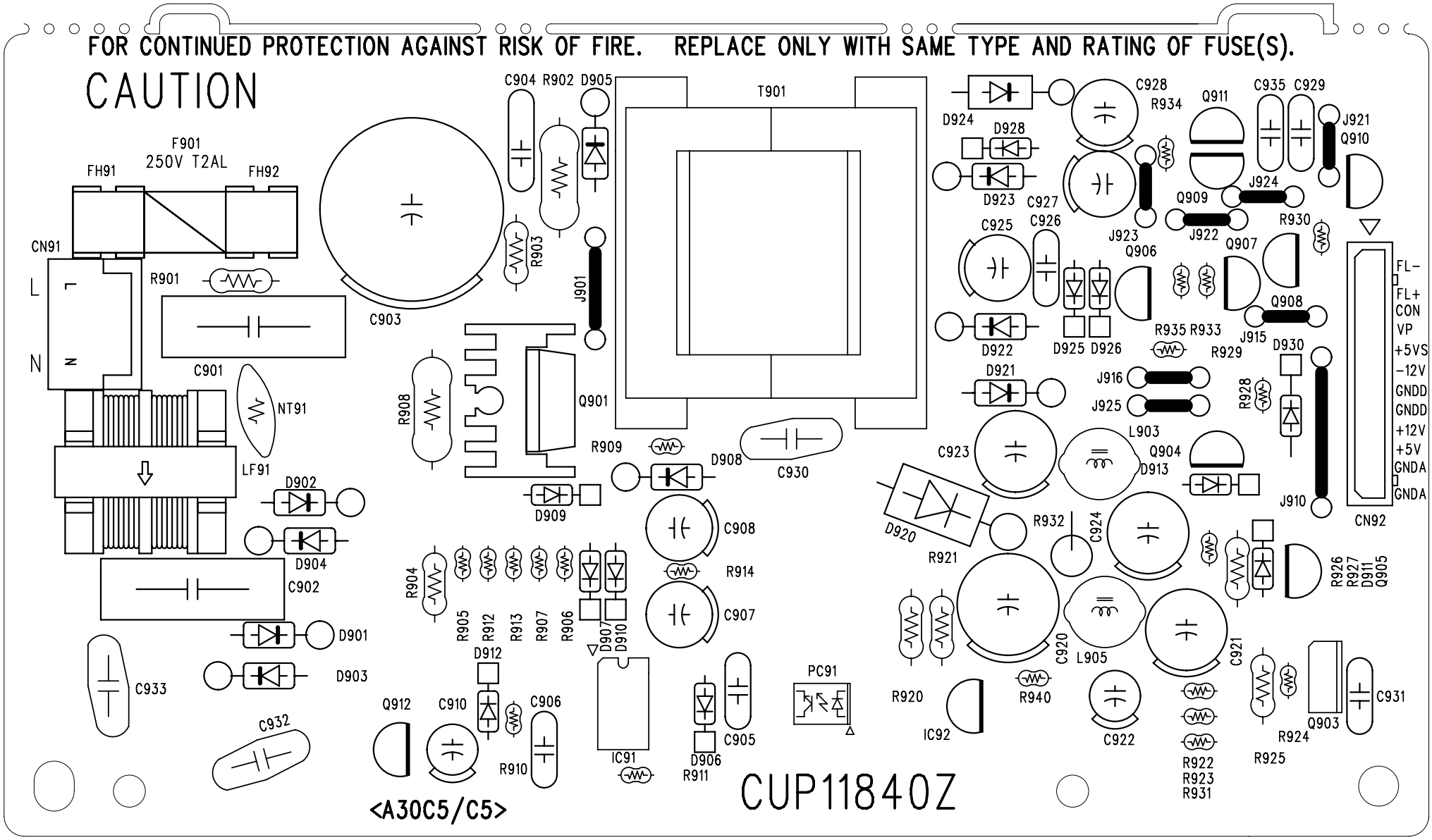
Ref#	Component	Description	Drawing No
	COP11840C	SMPS ASS'Y (DVD37/47)	DVD37 SMPS
C905	CCFT1H104ZF	CAP , SEMICONDUCTOR	
C906	CCKT1H391KB	CAP , CERAMIC	
C907	CCEA1HH100T	CAP , ELECT	10UF 50V
C908	CCEA1HH470T	CAP , ELECT	47UF 50V
C910	CCEA1HH1R0T	CAP , ELECT	1UF 50V
C921	CCEA1EH331T	CAP , ELECT	33OUF 25V
C922	CCEA1HH0R1T	CAP , ELECT	0.1UF 50V
C923	CCEA1EH331T	CAP , ELECT	33OUF 25V
C924	CCEA1VH101T	CAP , ELECT	100UF 35V
C925	CCEA1EH331T	CAP , ELECT	33OUF 25V
C926	HCQI1H102JZT	CAP , MYLAR	1000PF 50V J
C927	CCEA1HH470T	CAP , ELECT	47UF 50V
C928	CCEA1HH470T	CAP , ELECT	47UF 50V
C929	CCFT1H104ZF	CAP , SEMICONDUCTOR	0.1UF 50V ZF
C931	CCFT1H104ZF	CAP , SEMICONDUCTOR	0.1UF 50V ZF
C935	CCFT1H104ZF	CAP , SEMICONDUCTOR	0.1UF 50V ZF
D906	HVDMTZJ12BT	DIODE , ZENER	MTZJ12B 1/2W
D907	HVD1N4148T	DIODE	1N4148
D909	HVDMTZJ24BT	DIODE , ZENER	MTZJ24BT 1/2W
D910	HVD1N4148T	DIODE	1N4148
D911	HVD1N4148T	DIODE	1N4148
D912	HVDMTZJ5.1BT	DIODE , ZENER	MTZJ5.1B 1/2W
D925	HVD1N4148T	DIODE	1N4148
D926	HVDMTZJ12BT	DIODE , ZENER	MTZJ12B 1/2W
D928	HVDMTZJ2.7BT	DIODE , ZENER	MTZJ2.7B 1/2W
FH91	KJCFC5S	HOLDER , FUSE	
FH92	KJCFC5S	HOLDER , FUSE	
IC92	HVIKIA431BAT	I.C , REGULATOR	KIA431B
J901	C3A206	WIRE , COPPER	SN95/PB5 , 0.6
J910	C3A206	WIRE , COPPER	SN95/PB5 , 0.6

SMPS PCB

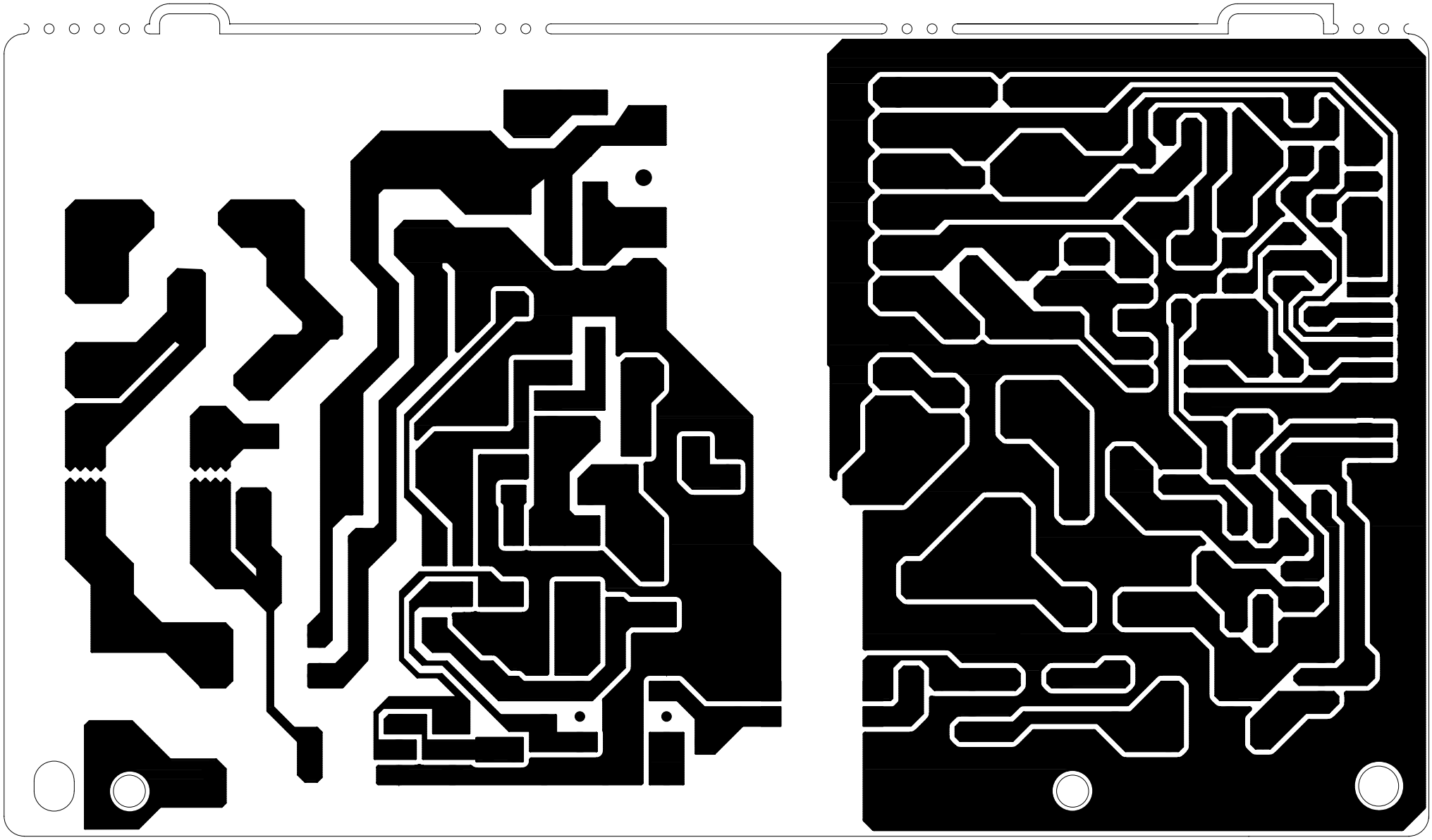
Ref#	Component	Description	Drawing No
J915	C3A206	WIRE , COPPER	SN95/PB5 , 0.6
J916	C3A206	WIRE , COPPER	SN95/PB5 , 0.6
J923	C3A206	WIRE , COPPER	SN95/PB5 , 0.6
J924	C3A206	WIRE , COPPER	SN95/PB5 , 0.6
J925	C3A206	WIRE , COPPER	SN95/PB5 , 0.6
L903	CLZ9Z040Z	COIL , CHOKE(6.8UH)	DR 6.5*7.5
L905	CLZ9Z040Z	COIL , CHOKE(6.8UH)	DR 6.5*7.5
NT91	KRT10D9MSFT	THERMISTER	
Q904	HVTKTC3198YT	T.R	KTC3198Y
Q905	HVTKTA1273YT	TR NORMAL KTA1273/PNP/TO-92L	
Q906	HVTKSC1008YT	T.R	KSC1008Y
Q907	HVTKRC102MT	T.R	KRC102M
Q908	HVTKRA102MT	T.R	KRA102M
Q910	HVTKSC1008YT	T.R	KSC1008Y
Q911	HVTKSA708YT	T.R	KSA708Y
Q912	HVDMCR100-6ZL1G	SCR (ON SEMI)	
R901	KROS1TJ105V	RES , METAL FILM (1/2W , 1M OH	
R903	CRD25TJ754T	RES	
R904	CRD25TJ754T	RES	
R905	CRD20TJ222T	RES , CARBON	2.2K OHM 1/5W J
R906	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J
R907	CRD20TJ103T	RES , CARBON	10K OHM 1/5W J
R909	CRD20TJ100T	RES , CARBON	10 OHM 1/5W J
R910	CRD20TJ103T	RES , CARBON	10K OHM 1/5W J
R911	CRD20TJ104T	RES , CARBON	100K OHM 1/5W J
R912	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J
R913	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J
R914	CRD20TJ333T	RES , CARBON	33K OHM 1/5W J
R920	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J
R921	CRD20TJ222T	RES , CARBON	2.2K OHM 1/5W J
R922	CRD20TF3481T	RES , CARBON	3.48K OHM 1/5W J
R923	CRD20TF3001T	RES , CARBON	3K 1/5W F
R924	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J
R925	CRD25TJ101T	RES , CARBON	100 OHM 1/4W J
R926	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J
R928	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J
R929	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J
R930	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J
R934	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J
R935	CRD20TJ153T	RES , CARBON	15K OHM 1/5W J
R940	CRD20TJ472T	RES , CARBON	4.7K OHM 1/5W J
CN91	KJP02KA060ZY	WAFER	7.92MM(YUNHO)
CN92	CJP12GA19ZY	WAFER	0.1UF
C901	HCQF2E104KZE	CAP , POLYPROPYLENE FILM	0.1UF
C902	HCQF2E104KZE	CAP , POLYPROPYLENE FILM	400V/47uF
C903	CCET400VKRH470K	CAP , ELECT(400V/47uF)	KOSHIN KRH SERIES (S
C904	CCKT3A222KBL	CAP , CERAMIC	EKR3A222K05FK5
C920	CCEA1EH102T	CAP , ELECT	1000UF 25V
C930	CCKDHS222ME	CAP , CERAMIC (400V Y-CAP)	SDE2G222M10FF7
C932	CCKDHS102ME	CAP , CERAMIC (400V Y-CAP)	SDE2G102M10FF7
C933	CCKDHS102ME	CAP , CERAMIC (400V Y-CAP)	SDE2G102M10FF7
D901	HVD1N4007T	DIODE	1N4007 (1000V/1A)

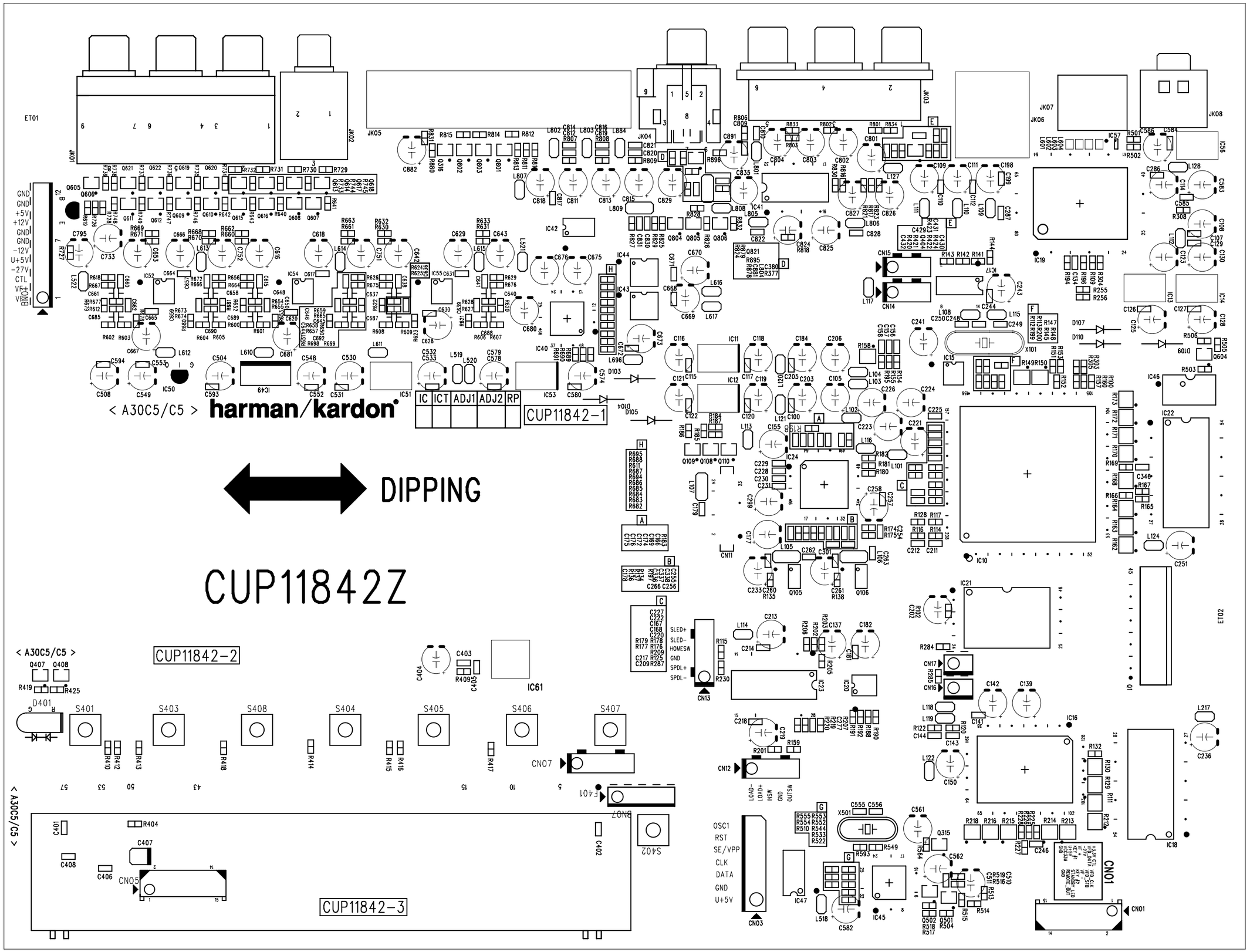
SMPS PCB

Ref#	Component	Description	Drawing No
D902	HVD1N4007T	DIODE	1N4007 (1000V/1A)
D903	HVD1N4007T	DIODE	1N4007 (1000V/1A)
D904	HVD1N4007T	DIODE	1N4007 (1000V/1A)
D905	HVDUF4007T	DIODE , SCHOTTKY	UF4007
D908	HVD1N4007T	DIODE	1N4007 (1000V/1A)
D913	HVD1N4148T	DIODE	1N4148
D920	HVD31DQ06H	DIODE	31DQ06-FC5
D921	HVDUF4007T	DIODE , SCHOTTKY	UF4007
D922	HVD1N4937T	DIODE , RECTIFIERS	1N4937(600V/1A)
D923	HVD1N4937T	DIODE , RECTIFIERS	1N4937(600V/1A)
D924	HVDSF26T	DIODE , SUPER FAST	1N4007 (1000V/1A)
IC91	BVISG6848DZ	IC,PWM	SG6848DZ
LF91	CLZ9Z060Y	LINE FILTER	CLZ9Z060Y
PC91	HVIPC17L1CB	I.C , PHOTO COUPLER	PC17L1C
Q901	CVICEF04N6YA	FET. HEAT SINK ASS`Y	
	BVICEF04N6	FET , CEF04N6	
	CMY2A223	HEAT SINK	
	CTB3+8JR	SCREW	
Q903	HVTKSB1151Y	T.R	KSB1151Y
R902	KRG1SANJ104H	RES,METAL OXIDE FILM	100K OHM
R908	KRW1PJ1R5V	RES, WIRE WOUND	1W 1.5(J) NON-INDUCT
R927	KRDS1TJ681V	RES , CARBON	680OHM 1/2W J
T901	CLT9Z018ZE	TRANS (DVD 27)	EER2828H



H/K DVD 37 EU PCB DRAWING

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ET02
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JK06
JK07
JK08
GND
GND
+5V
+12V
GND
GND
-12V
U+5V
-27V
CTL
VFD
VND
IC
ICT
ADJ1
ADJ2
RP
OSC1
RST
SE/VPP
CLK
DATA
GND
U+5V
SLED+
SLED-
HOMESW
GND
SPDL+
SPDL-
LOAD-
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MSW
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CN01
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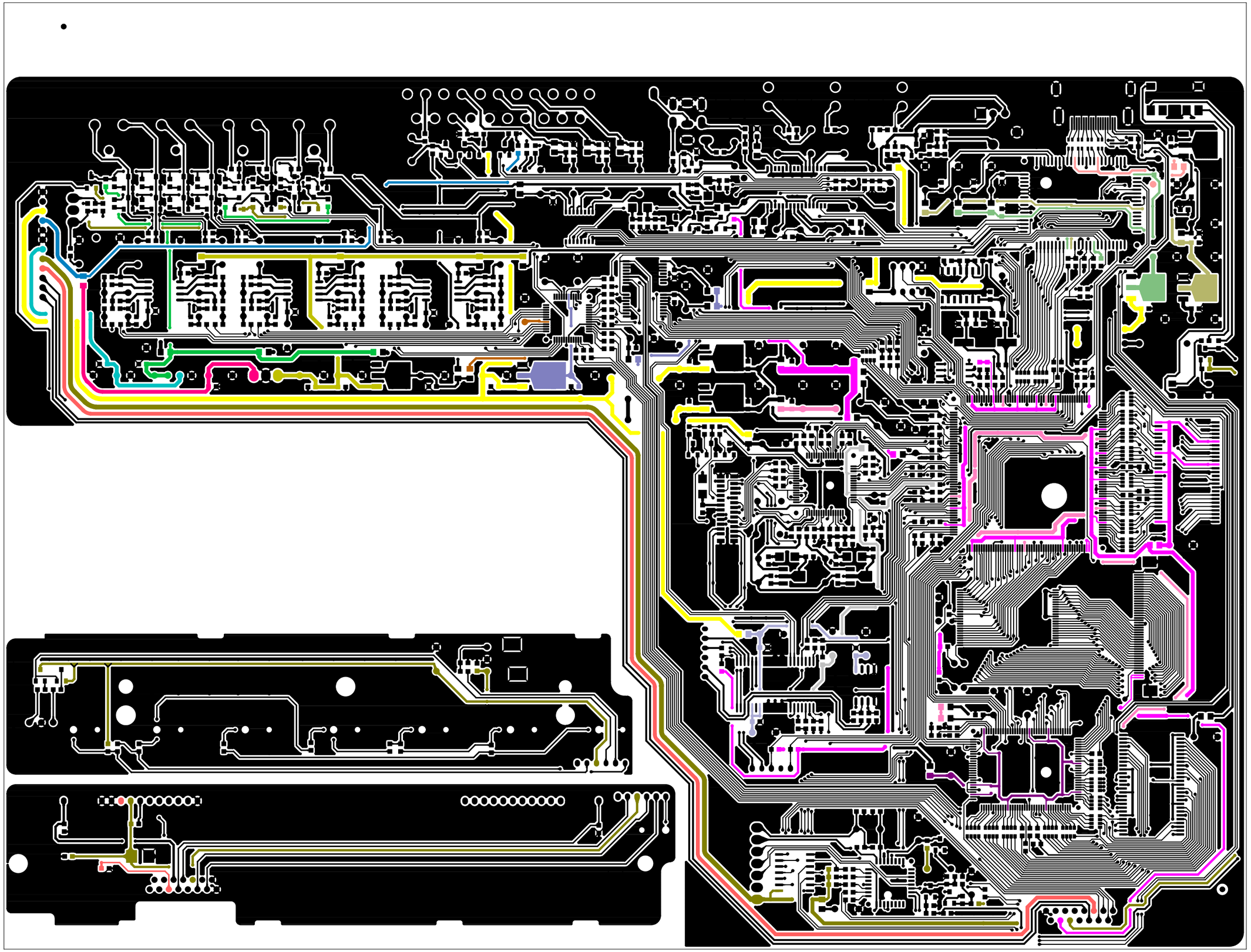

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Data Sheet

ZR36778HQCG

Vaddis® 778 Advanced Featured DVD SoC

Version 0.9
19 Sep 2004

ZORAN Proprietary

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1 Introduction

1.1 General

This document describes the technical specification of the **Vaddis 778** disc loader controller, flash memory card reader and decoder device.

The **Vaddis 778** can control disc loaders and read bitstreams using the following media: DVD- ROM, DVD- R, DVD+ R, DVD- RW, DVD+ RW, CD- DA, CD- ROM, CD- ROM (XA), CD- R and CD- RW discs.

The **Vaddis 778** can read the following types of serial and parallel flash memory cards: Secure Digital (SD), Memory Stick (MS and MS Pro), Compact Flash (CF) and Smart Media (SM) and XD.

The **Vaddis 778** can playback all discs conforming to the above standards (including support of sub- pictures, highlights and closed captions) with the exception of DVD- Audio ASV transition effects. The **Vaddis 778** can playback MP3 (MPEG 1 Layer 3), MPEG 2, Layer 3 (including low sampling rates) DTS, AAC or WMA type audio files from CD- ROM, CD- R and CD- R/ W discs. The **Vaddis 778** can playback various types of JPEG, MPEG 4 and DivX bitstreams from files on DVD- ROM, DVD- R, DVD- RW, CD- ROM, CD- R and CD- RW, or on flash cards, or SACD with external SACD decoder chip.

Vaddis 778 is pin compatible with Vaddis 770.

It is assumed that the reader is familiar with the various discs, JPEG, MPEG 4, MPEG 2 and MPEG 1 international standards and the industrial standards for DivX, DVD- Video, DVD- Audio and the various types of CD and flash card formats. Note: This document contains information from industrial standards that were obtained by Zoran from other corporations under a Non Disclosure Agreement.

The **Vaddis 778** receives data from the disc loader optical pick- up unit OPU through an external RF amplifier, limit switches and other sensors and control the disc loader focus and tracking coils, sled, spindle and tray motors through a servo amplifier external device(s). The **Vaddis 778** implements all the signal processing, multi- pass ECC, EDC, track buffer management and servo functions that result in a (error corrected) bitstream.

The **Vaddis 778** can perform the decryption processes for bitstreams originating from a DVD- Video or DVD- Audio discs or from DivX bitstreams.

The max data read rate for all types of CD discs is 8x (8*1.411 Mbits/ Sec). The max data read rate for DVD discs is 2x (2*10.08 Mbits/ Sec).

The **Vaddis 778** outputs interlaced or progressive CCIR size (also called SD or D1 size), 4:2:2, Y, U and V digital video. The representation of each component sample is 8 bits. Suitable post- processing, to transform the original decoded size and format (e.g., SIF size or CCIR size MPEG 1 format, SIF size, "half D1" size, "2/ 3 D1" size or CCIR size MPEG 2 format) to the interlaced CCIR size, 4:2:2, Y, U and V format, is performed by the **Vaddis 778.**

The interlaced video display frame rate is either 25 or 29.97 frames per second. Frame rate conversion is performed from coded MPEG frame rates of 23.976, 25, or 29.97 per second, to one of the two display frame rates mentioned above. For example, for display frame rate of 29.97 and coded frame rate of 23.976, "3/ 2 pull down" is performed.

The progressive video display frame rate is either 50 or 59.94 frames per second. Frame rate

conversion is performed from coded MPEG frame rates of 23.976, 25, or 29.97 per second, to one of the two display frame rates mentioned above by a de-interlacing unit using 2 fields edge adaptive interpolation.

The interlaced or progressive 8 bits digital video output is synchronous with an output video clock and sync signals, and contiguous along each video line.

Image display "location" relative to the sync signals, and size (up to the max specified above), are specified by **Vaddis 778** SW. The size of the displayed part of the decoded image can be less than or equal to the size of the decoded image

Format conversion between PAL, NTSC, 16:9 or 4:3 is supported, with pixel aspect ratio conservation, using (e.g.) either the "Pan-scan" or the "Letterbox" methods.

When the digital video output is interlaced, the **Vaddis 778** output analog interlaced video through a video encoder and four 10 bits DACs that are included in the **Vaddis 778.** Analog outputs can be either composite (CVBS and Y, C of "S-video") or component (R, G and B, or Y, U and V). When the digital video output is progressive, the **Vaddis 778** output analog progressive video in components format only, through the three components DACs or compatible interlaced video. The video encoder and DACs operate with a 54 MHz clock.

The audio output is 16, 18, 20 or 24 bits, two to eight channels, PCM samples at 16, 22.05, 24, 32, 44.1, 48, 96 or 192 KHz with each pair of (e.g., left and right) samples interleaved on a serial bus according to several flavours of the I2S standard. Post processing of the decoded audio and one stereo digital audio input, suitable for Karaoke and similar applications is supported. Audio coded data or reconstructed data can be output on a single line using an internal S/PDIF transmitter. PCM or coded audio data can be also input through one of two S/PDIF (TTL) inputs using a S/PDIF receiver to recover the input bit clock.

The Vaddis 778 can also output 8 bits, Y, U and V, 4:2:2, digital ("still") video to the HDXtreme companion chip, in various formats, compatible with the HDXtreme, as long as the sample rate is less than 135 MHz and the width of the Y component is less than 2047. In this mode, no other digital or analog video is output.

The **Vaddis 778** uses Synchronous DRAMs (SDRAM) for external buffers and generates all address and control signals for this external buffer. The required Synchronous DRAMs are of -7 type (max clock rate of 147 MHz). The required size is 64 Mbits using one 4M*16 bit device. The internal structure of the devices has to be four banks of 2048 rows by 256 cells each. Some limited applications can be supported by a single or dual 16 Mbits device(s). A single 128 Mbits device with four banks of 2048 rows by 512 cells each is also supported.

The **Vaddis 778** interfaces directly (through external buffers only) to several types of serial and parallel flash cards connectors. The interface is sharing some of the pins also used for disc loader control, so that the disc loader can not be operational while reading a card. For parallel flash cards, the interface is sharing some of the flash memory pins, so that the flash memory can not be accessed while reading a sector from a card.

The **Vaddis 778** interfaces to the other devices of a player (e.g., IR remote control receiver, front panel controller, audio DACs and ADCs) mainly through GPIO functions controlled by SW to implement protocols like SPI and I2C. There are on-chip HW aids to interface to a master SSC type device (e.g., a front panel concentrator).

1.3 Typical Applications

Stand- alone DVD and CD disc players. See example block diagram in the figure below.

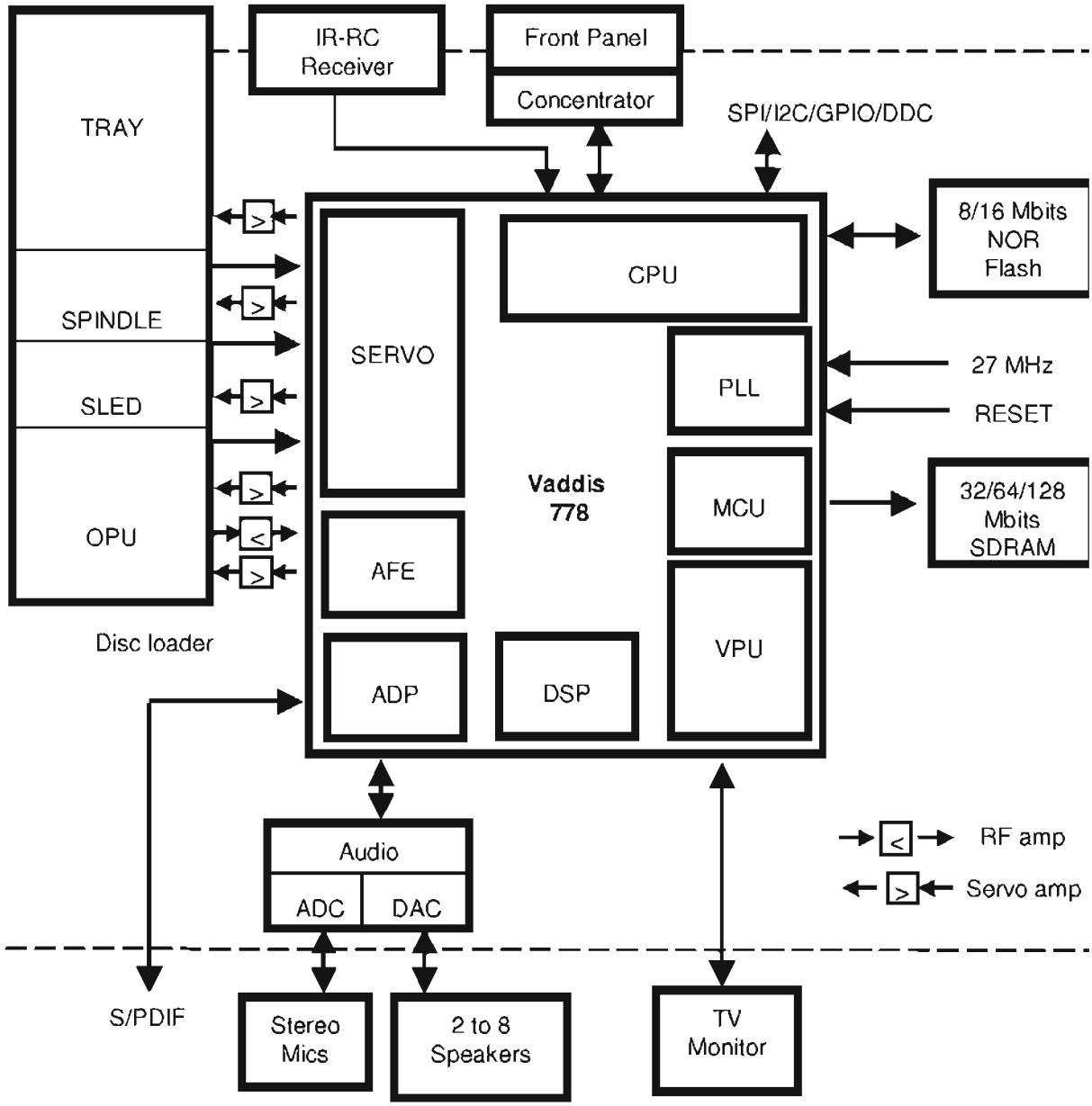

Figure 1 – DVD Player Block Diagram

The pins used for disc loader and NOR flash interface have a second function for direct flash card reading (not shown). Interface to an HD TV monitor is through an HDXtreme companion chip (not shown). When needed, the 64 Mbits SDRAM can be replaced by a 128 Mbits SDRAM.

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2 Functional Description

2.1 External interface

The main external interfaces of the **Vaddis 778** are shown in the next figure. The pins used for disc loader and NOR flash interface have a second function for direct flash card reading (not shown). Interface to an HD TV monitor is through an **HDXtreme** companion chip (not shown).

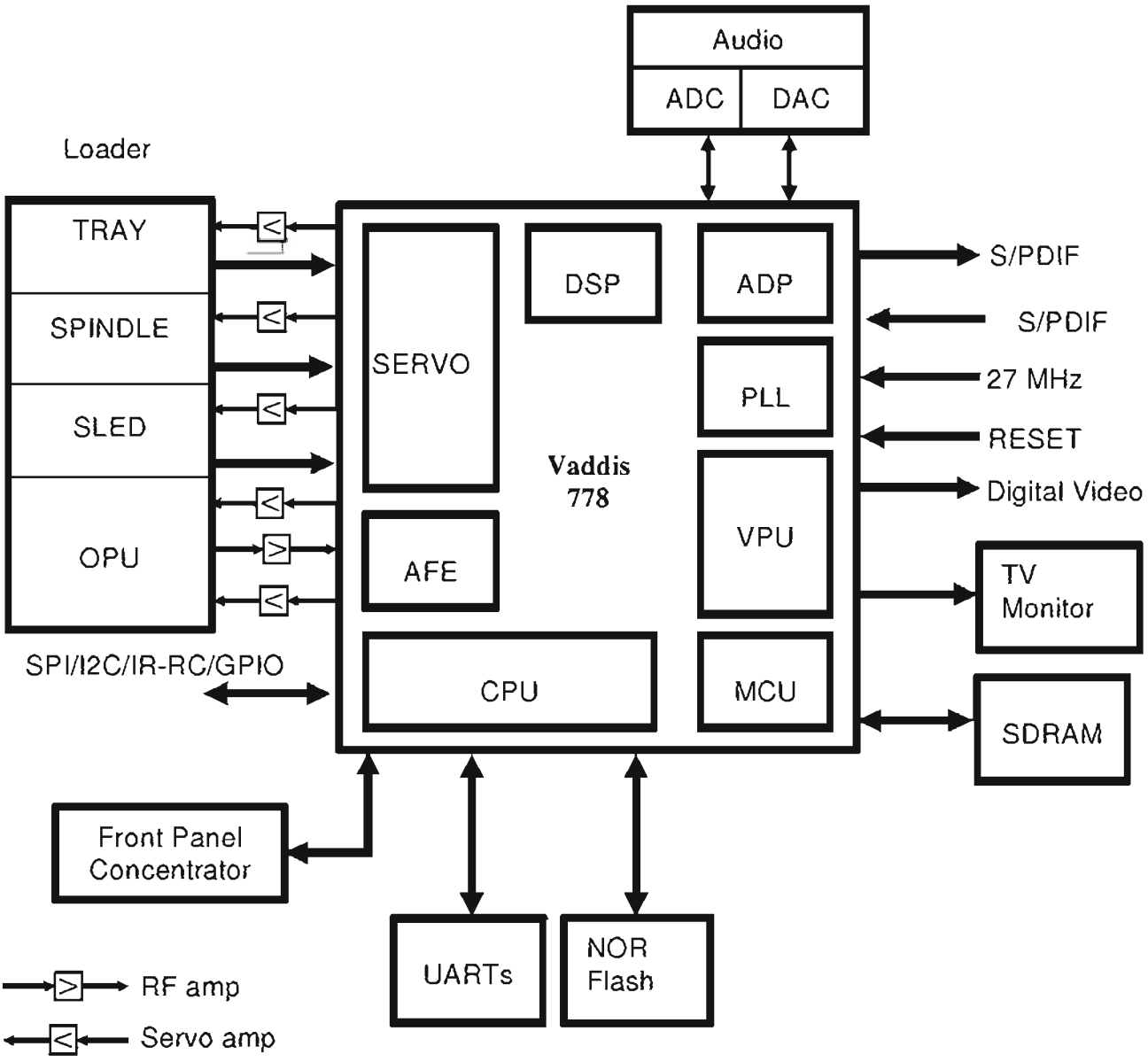

Figure 2 – Vaddis 778 Main External Interfaces

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3 Pin Description

3.1 Pin List

The **Vaddis 778** has 208 pins. The table below lists the pins, their functions, the direction or nature of each function (according to the legend below). Note that some of the functional pins may have additional function(s) dedicated for testing which are not described here. Following is the table legend:

I - standard input-only. O - standard active driver, with a 3-state option. I/O - bi-directional I/O pin, with a 3-state option. AI - Analog input signal. AO - Analog output signal. AI/O - Analog connection. ID - input, not sampled by PCLK. S - Power supply or ground.

If different functions have different direction, the **Vaddis 778** I/O supports all of them. Directions needed at RESET or for testing, when are different, are not shown in the table. All I and I/O pins have a level retaining HW.

Pins that are designated AI, S or ID should not be left not connected or floating.

Table 1 – Vaddis 778 Pinouts

Pin Number	Pin Functions	Direction	Description
1	*SSCRXD*	I	SSC data input.
	GPCI/O[17]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW
	PM[15]	O	Probe mux data output
2	*MEMCS[1]#*	O	PNVM/SRAM chip select (active low) output
	GPCI/O[18]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
3	*VDDP*	S	3.3 V Digital periphery power supply
4,5	*MEMAD*	O	PNVM/SRAM address bus outputs
	[15,16]		
	SYSIND[1,0]	I	General purpose system configuration Indication input. Level sampled during RESET
6	*MEMAD[14]*	O	PNVM/SRAM address bus output
	GCLKSEL	I	*GCLKPOUT* or *GCLKA* function selection. Level sampled during RESET
7	*MEMAD[13]*	O	PNVM/SRAM address bus output
	FCUIF[29]	O	Flash card interface unit output signal

Pin Number	Pin Functions	Direction	Description
8	*MEMAD[12]*	O	PNVM/ SRAM address bus output
	PLLCFGA	I	Audio PLL configuration input. Level sampled during RESET. In normal operation the pin must be low during RESET
9	*MEMDA[15]*	I/ O	PNVM/ SRAM bi- directional data bus
	FCUIF[28]	I/ O	Flash card interface unit input/ output signal
10	*MEMAD[11]*	O	PNVM/ SRAM address bus output
	PLLCFGP	I	Process PLL configuration input. Level sampled during RESET. In normal operation the pin must be low during RESET
11	*MEMDA[7]*	I/ O	PNVM/ SRAM bi- directional data bus
	FCUIF[9]	I/ O	Flash card interface unit input/ output signals
12	*GNDP*	S	Digital periphery ground of 3.3 V supply
13	*MEMAD[10]*	O	PNVM/ SRAM address bus output
	FCUIF[20]	O	Flash card interface unit output signal
14	*MEMDA[14]*	I/ O	PNVM/ SRAM bi- directional data bus
	FCUIF[27]	I/ O	Flash card interface unit input/ output signal
15	*MEMAD[9]*	O	PNVM/ SRAM address bus outputs
	FCUIF[19]	O	Flash card interface unit output signal
16	*MEMDA[6]*	I/ O	PNVM/ SRAM bi- directional data bus
	FCUIF[8]	I/ O	Flash card interface unit input/ output signals
17	*MEMAD[8]*	O	PNVM/ SRAM address bus outputs
	FCUIF[18]	O	Flash card interface unit output signal
18- 19	*MEMDA[13,5]*	I/ O	PNVM/ SRAM bi- directional data bus
	FCUIF[26.7]	I/ O	Flash card interface unit input/ output signals
20	*MEMAD[20]*	O	PNVM/ SRAM address bus outputs
	MEMCS[2]#	O	PNVM/ SRAM chip select (active low) output
	GPCI/ O[19]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW
21	*VDDP*	S	3.3 V Digital periphery power supply
22	*MEMDA[12]*	I/ O	PNVM/ SRAM bi- directional data bus

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Pin Number	Pin Functions	Direction	Description
	FCUIF[25]	I/O	Flash card interface unit input/output signal
23	*MEMWR#*	O	PNVM/SRAM write enable (active low) output
	FCUIF[0]	O	Flash card interface unit output signal
24	*MEMDA[4]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[6]	O	Flash card interface unit output signal
25	*VDDC*	S	1.8 V Digital core power supply
26	*MEMDA[11]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[24]	I/O	Flash card interface unit input/output signal
27	*MEMDA[3]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[5]	I/O	Flash card interface unit input/output signals
28	*MEMAD[19]*	O	PNVM/SRAM address bus outputs
	PLLSEL	I	PLL frequency selection - 108 MHz (low) or 135 MHz (high). Level sampled during RESET
29	*GNDC*	S	Digital core ground of 1.8 V supply
30	*MEMDA[10]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[23]	I/O	Flash card interface unit input/output signal
31	*MEMAD[18]*	O	PNVM/SRAM address bus output
32	*GNDP*	S	Digital periphery ground of 3.3 V supply
33	*MEMDA[2]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[4]	I/O	Flash card interface unit input/output signals
34	*MEMAD[17]*	O	PNVM/SRAM address bus output
35	*MEMDA[9]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[22]	I/O	Flash card interface unit input/output signal
36	*MEMAD[7]*	O	PNVM/SRAM address bus outputs
	FCUIF[17]	O	Flash card interface unit output signal
37	*MEMDA[1]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[3]	I/O	Flash card interface unit input/output signals
38	*MEMAD[6]*	O	PNVM/SRAM address bus outputs
	FCUIF[16]	O	Flash card interface unit output signal
39	*MEMDA[8]*	I/O	PNVM/SRAM bi-directional data bus

Pin Number	Pin Functions	Direction	Description
	FCUIF[21]	I/O	Flash card interface unit input/output signal
40	*MEMAD[5]*	O	PNVM/SRAM address bus outputs
	FCUIF[15]	O	Flash card interface unit output signal
41	*VDDP*	S	3.3 V Digital periphery power supply
42	*MEMDA[0]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[2]	O	Flash card interface unit output signal
43	*MEMAD[4]*	I/O	PNVM/SRAM address bus outputs
	FCUIF[14]	O	Flash card interface unit output signal
44	*MEMRD#*	O	PNVM/SRAM read enable (active low) output
	FCUIF[1]	I/O	Flash card interface unit input/output signal
45-46	*MEMAD[3,2]*	O	PNVM/SRAM address bus outputs
	FCUIF[13,12]	O	Flash card interface unit output signal
47	*MEMCS[0]#*	O	PNVM/SRAM chip select (active low) output
48	*MEMAD[1]*	O	PNVM/SRAM address bus outputs
	FCUIF[11]	O	Flash card interface unit output signals
	BOOTSEL[2]	I	CPU SW boot (and execute) source selection: (high, high) - For production testing; (high, low) - Flash+SRAM (for debug monitor); (low, high) - First debug UART (low, low) - Flash (low) or Level sampled during RESET
49	*MEMAD[0]*	O	PNVM/SRAM address bus outputs
	FCUIF[10]	O	Flash card interface unit output signals
	BOOTSEL[1]	I	CPU SW boot (and execute) source selection: (high, high) - For production testing; (high, low) - Flash+SRAM (for debug monitor); (low, high) - First debug UART (low, low) - Flash (low) or Level sampled during RESET
50	*GNDP*	S	Digital periphery ground of 3.3 V supply

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Pin Number	Pin Functions	Direction	Description
51	*VDD-IP*	S	3.3 V periphery reference voltage
52	*VDDP*	S	3.3 V Digital periphery power supply
53-57	*RAMADD [4,3,5,2,6]*	O	SDRAM address bus output
58	*VDDP*	S	3.3 V Digital periphery power supply
59-61	*RAMADD [1,7,0]*	O	SDRAM address bus output
62	*GNDP*	S	Digital periphery ground of 3.3 V supply
63	*RAMADD[8]*	O	SDRAM address bus output
64	*VDDC*	S	1.8 V Digital core power supply
65	*RAMADD[10]*	O	SDRAM address bus output
66	*GNDC*	S	Digital core ground of 1.8 V supply
67	*RAMADD[9]*	O	SDRAM address bus output
68	*VDDP*	S	3.3 V Digital periphery power supply
69	*RAMADD[11]*	O	SDRAM address bus output
70	*RAMCS[0]#*	O	SDRAM chip select (active low)
	RAMBA[1]	O	SDRAM bank select output
71	*RAMBA[0]*	O	SDRAM bank select output
72	*GNDP*	S	Digital periphery ground of 3.3 V supply
73	*RAMCS[1]#*	O	SDRAM chip select (active low) output
74	*RAMRAS#*	O	SDRAM row select (active low) output
75	*RAMCAS#*	O	SDRAM column select (active low) output
76	*VDDP*	S	3.3 V Digital periphery power supply
77	*RAMWE#*	O	SDRAM write enable (active low) output
78	*RAMDQM*	O	SDRAM data masking (active high) output
79	*GNDPCLK*	S	Digital ground of filtered 3.3 V supply for PCLK
80	*PCLK*	O	SDRAM clock output (same as internal processing clock)
81	*VDDPCLK*	S	3.3 V filtered digital power supply for PCLK
82	*RAMDAT[8]*	I/O	SDRAM bi-directional data bus

Pin Number	Pin Functions	Direction	Description
83	*GNDP*	S	Digital periphery ground of 3.3 V supply
84-86	*RAMDAT [7,9,6]*	I/O	SDRAM bi-directional data bus
87	*VDDP*	S	3.3 V Digital periphery power supply
88-90	*RAMDAT [10,5,11]*	I/O	SDRAM bi-directional data bus
91	*GNDP*	S	Digital periphery ground of 3.3 V supply
92	*RAMDAT[4]*	I/O	SDRAM bi-directional data bus
93	*VDDC*	S	1.8 V Digital core power supply
94	*RAMDAT[12]*	I/O	SDRAM bi-directional data bus
95	*GNDC*	S	Digital core ground of 1.8 V supply
96	*RAMDAT[3]*	I/O	SDRAM bi-directional data bus
97	*VDDP*	S	3.3 V Digital periphery power supply
98-100	*RAMDAT [13,2,14]*	I/O	SDRAM bi-directional data bus
101	*GNDP*	S	Digital periphery ground of 3.3 V supply
102-104	*RAMDAT [1,15,0]*	I/O	SDRAM bi-directional data bus
105	*VDDP*	S	3.3 V Digital periphery power supply
106	*GPCI/O[20]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	CPUNMI	I	CPU non-maskable interrupt input
	SDATA[0]	I	SERVO channel sample data input for AFE by-pass
	PM[0]	O	Probe mux data output
107	*GNDP*	S	Digital periphery ground of 3.3 V supply
108	*ICGPCI/O[0]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
	AOUT[3]	O	Serial output of digital stereo audio

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Pin Number	Pin Functions	Direction	Description
	SDATA[1]	I	SERVO channel sample data input for AFE by-pass
	PM[1]	O	Probe mux data output
109	*IDGPCI/O[0]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	RAMCKE	O	Clock enable signal to the SDRAM (for power down)
	SDATA[2]	I	SERVO channel sample data input for AFE by-pass
	PM[2]	O	Probe mux data output
110	*S/PDIFOUT*	O	S/PDIF transmitter output for digital coded or reconstructed audio data
	SDATA[3]	I	SERVO channel sample data input for AFE by-pass
	PM[3]	O	Probe mux data output
111	*AOUT[2]*	O	Serial outputs of digital stereo audio
	GPCI/O[21]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	SDATA[4]	I	SERVO channel sample data inputs for AFE by-pass
	PM[4]	O	Probe mux data outputs
112	*AOUT[1]*	O	Serial outputs of digital stereo audio
	GPCI/O[22]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	PM[5]	O	Probe mux data outputs
113	*AOUT[0]*	O	Serial output of digital stereo audio
	SDATA[6]	I	SERVO channel sample data input for AFE by-pass
	PM[6]	O	Probe mux data outputs

Pin Number	Pin Functions	Direction	Description
114	*GPAI/O*	I/O	General purpose input/output, monitored/controlled by the ADP SW
	AOUT[3]	O	Serial output of digital stereo audio
	IDGPCI/O[0]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	PM[7]	O	Probe mux data output
115	*ALRCLK*	O	Digital audio left/right select output for the audio port. Square wave, at the sampling frequency. Programmable polarity
116	*ABCLK*	O	Digital audio bit-clock output. Data on AOUT and AIN is output or latched, respectively, with the rising or falling (programmable) edge of this clock
117	*GNDP_A2*	S	Digital ground of filtered 3.3 V supply for AMCLK
118	*AMCLK*	I/O	Audio Master Clock input/output. 128, 192, 256 or 384 times the sampling frequency (programmable).
119	*VDDP_A2*	S	3.3 V filtered digital power supply for AMCLK
120	*AIN*	I	Serial input of digital stereo audio
	GPCI/O[23]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	PM[8]	O	Probe mux data output
121	*GNDC*	S	Digital core ground of 1.8 V supply
122	*VSYNC#*	O	SD digital video vertical sync output signal
	HDFI	I	HD digital video field index input signal
	GPCI/O[24]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	DACTEST[9]	I	DACs test input
	PM[9]	O	Probe mux data output
123	*VDDC*	S	1.8 V Digital core power supply
124	*HSYNC#*	O	SD digital video horizontal sync output signal

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Pin Number	Pin Functions	Direction	Description
	HDHS	I	HD digital video horizontal sync input signal
	GPCI/O[25]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
125	*GNDP*	S	Digital periphery ground of 3.3 V supply
126	*VCLKx2*	O	Digital video clock output. 27.000 (for SD interlaced), 54.000 (SD progressive) or 135.000 (for HD) MHz
	COSYNC	O	Composite sync output. Active only when component analog output is selected
	ICGPCI/O[1]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
127	*VDDP*	S	3.3 V Digital periphery power supply
128	*VID[7]*	O	Digital 4:2:2 video luma/chroma output, interleaved U, Y V Y
	GPCI/O[26]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
129	*VID[6]*	O	Digital 4:2:2 video luma/chroma output, interleaved U, Y V Y
	ICGPCI/O[2]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
130	*VID[5]*	O	Digital4:2:2 video luma/chroma output, interleaved U, Y V Y
	IDGPCI/O[1]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
131	*GNDP*	S	Digital periphery ground of 3.3 V supply
132	*VID[4]*	O	Digital 4:2:2 video luma/chroma output, interleaved U, Y V Y
	GPCI/O[27]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW

Pin Number	Pin Functions	Direction	Description
133	*VID[3]*	O	Digital 4:2:2 video luma/ chroma output, interleaved U, Y V Y
	GPCI/ O[28]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW
	SERVOCLK	O	SERVO channel clock output for AFE by- pass
134	*VID[2]*	O	Digital 4:2:2 video luma/ chroma output, interleaved U, Y V Y
	GPCI/ O[29]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW
	SSEL[0]	O	SERVO channel select output for AFE by- pass
135	*VDDP*	S	3.3 V Digital periphery power supply
136	*VID[1]*	O	Digital 4:2:2 video luma/ chroma output, interleaved U, Y V Y
	GPCI/ O[30]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW
	SSEL[1]	O	SERVO channel select output for AFE by- pass
137	*VID[0]*	O	Digital 4:2:2 video luma/ chroma output, interleaved U, Y V Y
	ICGPCI/ O[3]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
138	*GNDP*	S	Digital periphery ground of 3.3 V supply
139	*GNDA*	S	Ground plane of internal PLL circuit
140	*RESET#*	ID	Reset input (active low)
141	*VDDA*	S	1.8 V Power supply for internal PLL circuit
142	*XO*	AO	Output to a crystal that is connected to *GCLKP*. If a crystal is not used at *GCLKP*, *XO* must be left not connected
143	*GCLKP*	ID	27.000MHz clock or crystal input for main processing clock generation.
144	*GCLKA*	ID	27.000MHz clock input for audio master clock generation.
	GPCI/ O[31]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW

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Pin Number	Pin Functions	Direction	Description
	GCLKPOUT	O	*GCLKP* output
145	*VDDP*	S	3.3 V Digital periphery power supply
146	*ICGPCI/O[4]*	I/O	General purpose input/output monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
147	*S/PDIFIN[0]*	I	S/PDIF receiver inputs for digital coded or reconstructed audio data
	GPCI/O[33]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW.
148	*ICGPCI/O[4]*	I/O	General purpose input/output monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
149	*S/PDIFIN[1]*	I	S/PDIF receiver inputs for digital coded or reconstructed audio data
	GPCI/O[34]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW.
150	*IDGPCI/O[3]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[33]	I	Flash card interface unit input signal
151	*GNDP*	S	Digital periphery ground of 3.3 V supply
152	*DUPRD0*	I	First debug UART data input
	GPCI/O[35]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
153	*DUPTD0*	O	First debug UART data output
	GPCI/O[36]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
154	*VDD-IP*	S	3.3 V periphery reference voltage
155	*DUPRD1*	I	Second debug UART data output
	GPCI/O[37]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
156	*DUPTD1*	O	Second debug UART data output

Pin Number	Pin Functions	Direction	Description
	GPCI/O[38]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
157	*GNDDACD*	S	Ground for the video DACs 3.3 V analog power supply
158	*CVBS/G/Y* (DAC A)	AO	When the Vaddis 778 outputs composite (SCART or non-SCART) video, this line is CVBS output When the Vaddis 778 outputs RGB, this line is the Green output When the Vaddis 778 outputs YUV, this line is the Y output
159	*CVBS/C/Y* (DAC D)	AO	When the other Vaddis 778 outputs are not SCART video, the output on this line can be either CVBS or C. The selection is independent of the specific selection of the other three DACs. When the Vaddis 778 outputs composite SCART video, this line is the Y output
160	*VDDDAC*	S	3.3 V Analog power supply for the video DACs
161	*Y/R/V/C* (DAC B)	AO	When the Vaddis 778 outputs composite non-SCART video, this line is Y output When the Vaddis 778 outputs RGB, this line is the Red output When the Vaddis 778 outputs YUV, this line is the V output When the Vaddis 778 outputs composite SCART video, this line is the C output
162	*C/B/U* (DAC C)	AO	When the Vaddis 778 outputs composite (SCART or non-SCART) video, this line is C output When the Vaddis 778 outputs RGB, this line is the Blue output When the Vaddis 778 outputs YUV, this line is the U output
163	*RSET*	AI	Resistive load for gain adjustment of the DACs

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Pin Number	Pin Functions	Direction	Description
164	*GNDDACP*	S	Ground for the video DACs 3.3 V analog power supply
165	*GNDDABS2*	S	Common Ground for the video and SERVO DACs
166	*GNDDACPS*	S	Grounds for the SERVO DAC 3.3 V analog power
167	*DACDRIVE[0]*	AO	Drive DACs output signal
168	*VDDDACS*	S	3.3 V SERVO DACs power supply
169	*DACDRIVE[1]*	AO	Drive DACs output signal
170	*GNDDACDS*	S	Grounds for the SERVO DAC 3.3 V analog power supply
171	*VDDAFERF*	S	3.3 V Analog RF (AFE) power supply
172	*RFINP*	AI	RF positive input signal (differential input) / / RF input signal (single ended)
173	*RFINN*	AI	RF negative input signal (differential input) / / RF reference input signal
174	*GNDAFERF*	S	Analog RF (AFE) ground of 3.3 V supply
175	*VDDAFES*	S	3.3 V Analog SERVO (AFE) power supply
176	*ADCIN[7]*	AI	SERVO ADC input signal (e.g. from RF amplifier)
177	*ADCIN[6]*	AI	SERVO ADC input signal from RF amplifier
178-183	*ADCIN[5-0]*	AI	SERVO ADC input signals (e.g. from RF amplifier)
184,185	*VBIASS[0,1]*	AI	Servo analog signal reference voltage inputs
186	*GNDAFES*	S	Analog SERVO (AFE) ground of 3.3 V supply
187	*PWMACT[0]*	O	PWM0 output signal
	GPCI/O[39]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW
	DVDDAT[0]	I	AV data input for FE by-pass
	NRZDATA	I	NRZ data input for AFE and DRC by-pass
188	*PWMACT[1]*	O	PWM1 output signal

Pin Number	Pin Functions	Direction	Description
	GPCI/O[40]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW
	DVDDAT[1]	I	AV data input for FE by-pass
	NRZCLK	I	NRZ clock input for AFE and DRC by-pass
189	*PWMCO[0]*	O	PWM2 output signal
	GPCI/O[41]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	DVDDAT[2]	I	AV data input for FE by-pass
	NRZLOCK	I	NRZ lock input for AFE and DRC by-pass
190	*GNDC*	S	Digital core ground of 1.8 V supply
191	*PWMCO[1]*	O	PWM3 output signal
	GPCI/O[42]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	DVDDAT[3]	I	AV data input for FE by-pass
	NRZDFCT	I	NRZ defect input for AFE and DRC by-pass
192	*VDDC*	S	1.8 V Digital core power supply
193	*PWMCO[2]*	O	PWM4 output signal
	GPCI/O[43]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	FCUIF[34]	O	Flash card interface unit input signal
	DVDDAT[4]	I	AV data inputs for FE by-pass
194	*PWMCO[3]*	O	PWM5 output signal
	GPCI/O[44]]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	FCUIF[35]	I/O	Flash card interface unit input/output signal
	IDGPCI/O[2]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	DVDDAT[5]	I	AV data inputs for FE by-pass
195	*GNDPWMS*	S	SERVO PWMs ground of 3.3 V supply
196	*PWMCO[4]*	O	PWM6 output signal

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Pin Number	Pin Functions	Direction	Description
	GPCI/O[45]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	DVDDAT[6]	I	AV data input for FE by-pass
197	*VDDPWMS*	S	3.3 V SERVO PWM power supply
198	*PWMCO[5]*	O	PWM7 output signal
	GPCI/O[46]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	FCUIF[36]	I/O	Flash card interface unit input/output signal
	DVDDAT[7]	I	AV data inputs for FE by-pass
199	*PWMCO[6]*	O	PWM8 output signal
	IDGPCI/O[4]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[32]	I/O	Flash card interface unit input/output signal
	DVDSTRB	I	AV data input for FE by-pass
	RFDAT[4]	I	RF channel sample data inputs for AFE by-pass
200	*DEFECT*	I/O	Disc defect input or output signal
	IDGPCI/O[5]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[37]	I/O	Flash card interface unit input/output signal
	DVDREQ	O	AV data request output for FE by-pass. Programmable polarity
201	*ICGPCI/O[6]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW. When input, the pin can be used as general purpose external interrupt to the CPU
	DVDVALID	I	AV data valid input for FE by-pass. Programmable polarity
202	*GNDP*	S	Digital periphery ground of 3.3 V supply

Pin Number	Pin Functions	Direction	Description
203	*ICGPCI/O[7]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW. When input, the pin can be used as general purpose external interrupt to the CPU
	DVDERR	I	AV error input for FE by-pass. Programmable polarity
204	*VDDP*	S	3.3 V Digital periphery power supply
205	*SLEDPULSE*	I	Sled optical encoder input
	IDGPCI/O[6]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[30]	I	Flash card interface unit output signal
	DVDSOS	I	AV start of sector indication input for FE by-pass. Programmable polarity
206	*SPINDLE-PULSE*	I	Spindle optical encoder input
	IDGPCI/O[7]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[31]	I/O	Flash card interface unit input/output signal
207	*SSCCLK*	I/O	SSC clock input signal
	GPCI/O[47]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW
208	*SSCTXD*	O	SSC data output signal
	GPCI/O[16]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW

3.2 Signal Status During RESET and After RESET

Only I, I/O and O type pins are mentioned in this section.

In the following table, the status of the pins signals during RESET and just after RESET are specified.

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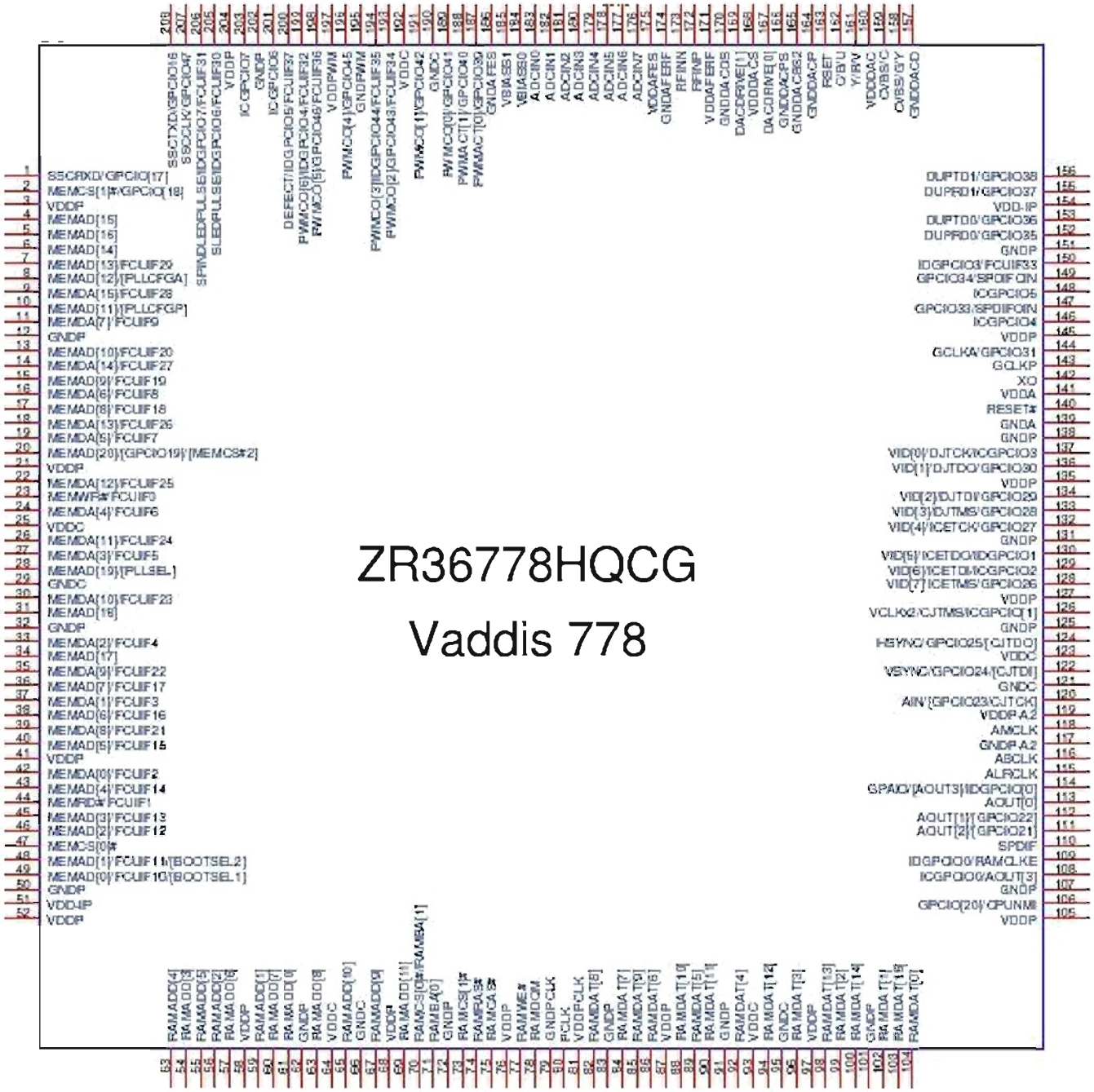
9 Package information

ZR36778HQCG is a green package



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Data Sheet

ZR36721

HD*Xtreme*®

HD up-scaling and HDMI transmitter processor

Version 1.2
25 July 2004

ZORAN Proprietary

ZORAN Corporation, 1390 Kifer Road, Sunnyvale, CA 94086-5305
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1 Product brief

1.1 Introduction

HDMI is the emerging digital interface for audio and video consumer products. It enables the next generation of DVD players to digitally transfer the highest quality video and audio to HDMI equipped high definition televisions. As a companion to the high-performance Vaddis 7 DVD solution, Zoran's HDXtreme processor upscales standard definition digital video and digital images to high definition resolution, which can then be displayed on HDTV / VGA monitors using the built-in HDMI/ DVI interface or the analog video output. The HDXtreme, when used with the Vaddis 778, enables decoded JPEG images to be shown at the display's native high definition resolution. The output can be digital via HDMI or analog via the DACs. Digital video or digital images are received from the Vaddis V778, in YUV, 4:2:2, 8 bits, progressive 480p and 576p, with embedded sync signals in a CCIR656-like protocol. HDXtreme introduces upscaling that adapts to all HDTV modes, including 720p (1280 pixels X 720 lines, progressive) and 1080i (1920 pixels X 1080 lines, interlaced). HDXtreme supports the progressive frame rate and the interlaced field rate: 59.94Hz, 50Hz, and color space conversion from standard definition YUV to high definition YUV and RGB.

1.2 Features

- Enables cost optimized Vaddis DVD system with HDMI/DVI interface
- No external SDRAM or CPU required
- Zoran proprietary adaptive high definition upscaler for 1080i, 720p and other resolutions
- JPEGXtreme™ feature displays JPEG at native resolution
- HDMI v1.0 standard compliant
- High-bandwidth Digital Content Protection (HDCP) r1.1 encryption support
- RGB or YPbPr component analog output via three High Definition video DACs
- Supports sidebars, wide-screen or anamorphic scaling from 4:3 inputs to 16:9 outputs
- Supports DDC and CEC via Vaddis IC
- Simultaneous HDMI digital and analog outputs
- Simultaneous Progressive HD video out from HDXtreme™ and SD interlaced video out from Vaddis
- 0.7W typical power consumption
- Power management for optimum system power consumption
- 80-pin PQFP Package

2.1 Block Diagram

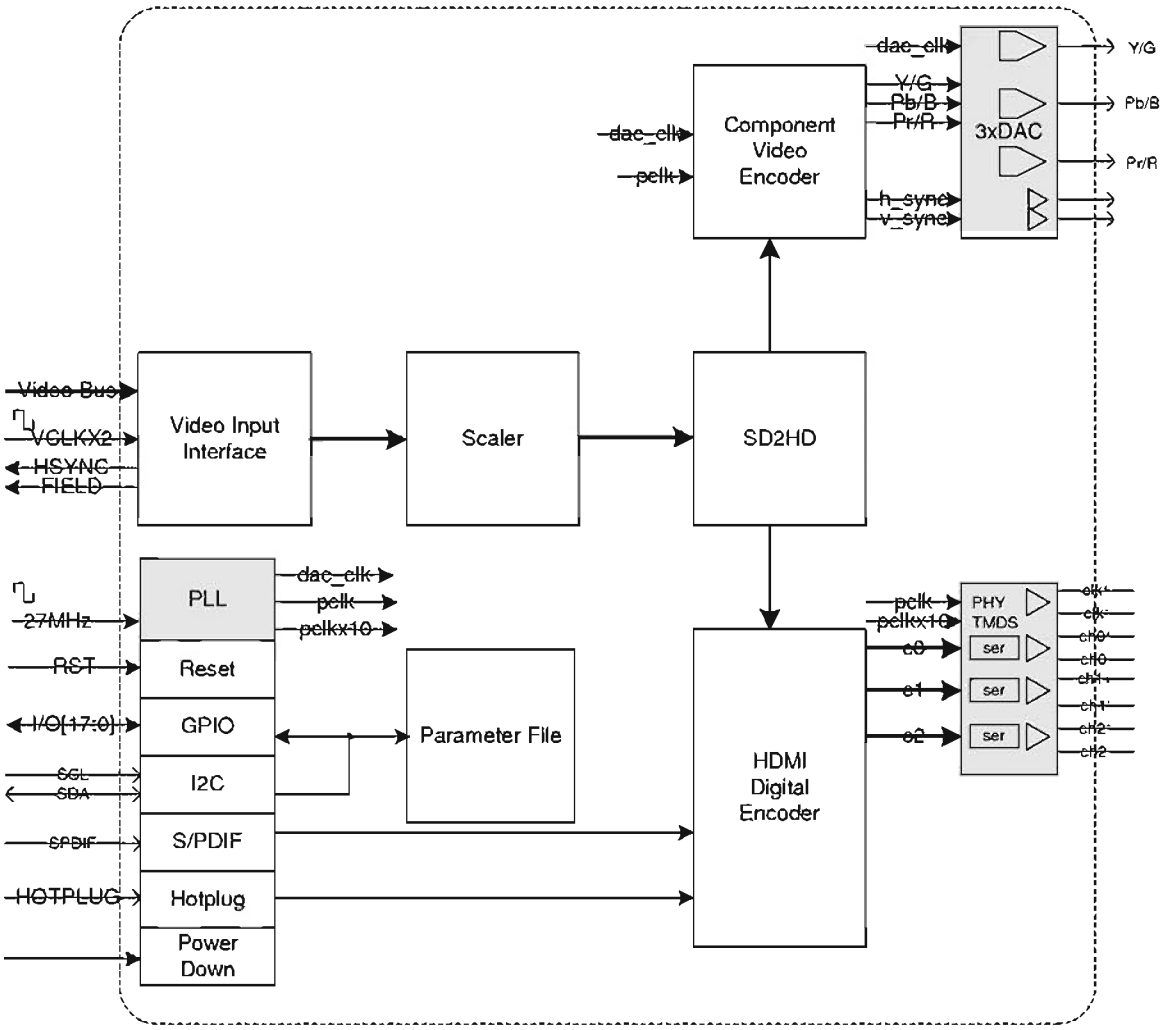

Figure 1 . Block Diagram

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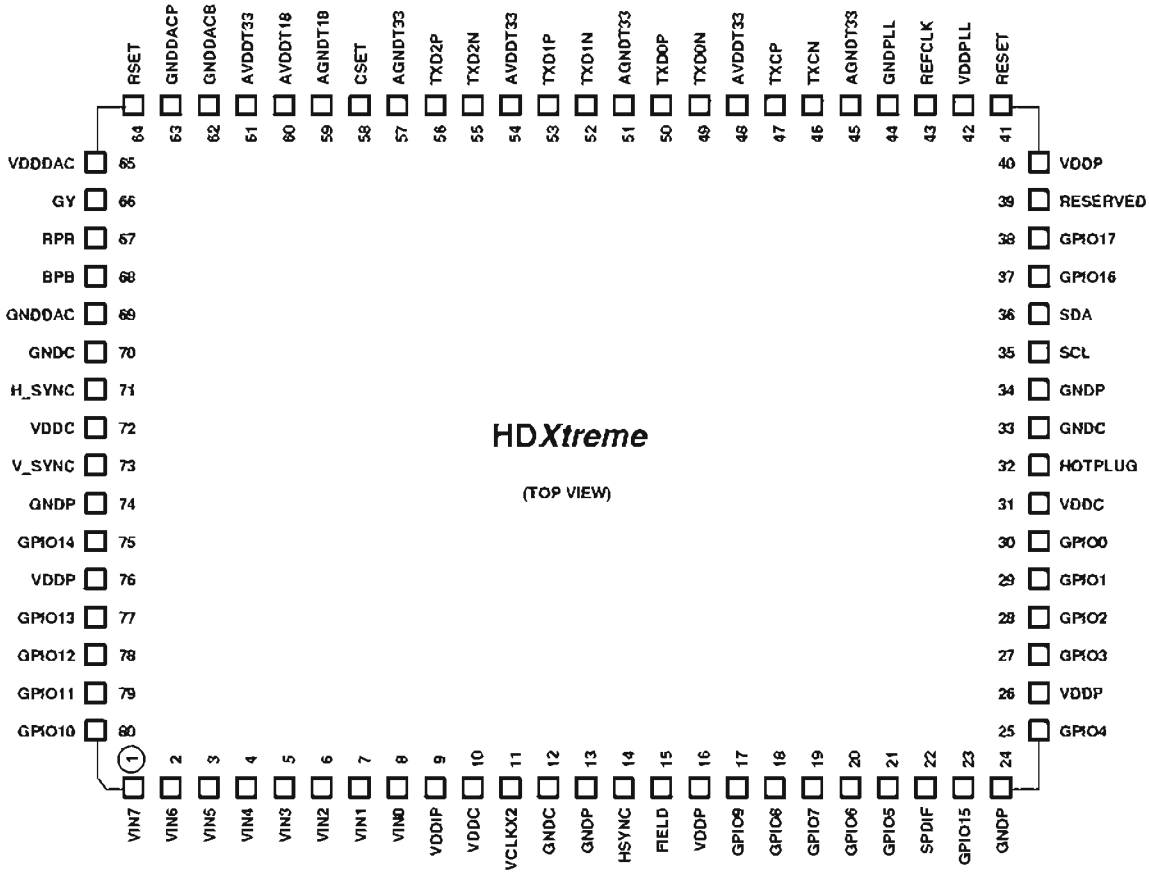
3 PIN DIAGRAM



4 PIN DESCRIPTION

Table 7. Pin Description

Pin Name	Pin #	Type	Description
			Digital Pins
VIN[7:0]	8-1	I	Video data bus. Video and control data are multiplexed on this bus in accordance to the c656 format.
VCLKX2	11	I	Video data bus clock (54MHz or 135MHz).
HSYNC/ I2CCFG2/ PD	14	I/O	1. Horizontal sync output control while in master mode. 2. I2C address select (bit 6) input. The value read on this pin is latched in during RESET# active. 3. Power down control input. While in ready for power down (see programming reference), a high value driven on this pin will activate the power down mode (see functional description).
FIELD/ I2CCFG1	15	I/O	1. Vertical sync output control while in master mode. 2. I2C address select (bit 4) input. The value read on this pin is latched in during RESET# active.
GPIO[17:0]	38,37,23 75,77-80 17-21,25 27-30	I/O	General-purpose input/output pins.
SPDIF/ I2CCFG0	22	I	1. Audio input serial interface – SPDIF format 2. I2C address select (bit 4) input. The value read on this pin is latched in during RESET# active.
HOTPLUG	32	I	Input used to monitor the "Hotplug" detect signal. This input is 5V tolerant.
SCL	35	I	I2C compatible clock input. This pin requires a pullup resistor connected to VDDP.
SDA	36	I/O	I2C compatible bidirectional data line. This pin requires a pullup resistor connected to VDDP.
RESERVED	39	I	This pin is reserved and must be left unconnected.
RESET#	41	I	General asynchronous reset, active low.
REFCLK	43	I	27MHz reference clock input.

H_SYNC	71	O	Horizontal sync output control that drive the display monitor (see VESA Standard)
V_SYNC	73	O	Vertical sync output control that drive the display monitor (see VESA Standard)
Differential Signal Pins			
TXCP	47	O	Differential driver output clock
TXCN	46		
TXD0P	50	O	Channel – 0 differential driver output data
TXD0N	49		
TXD1P	53	O	Channel – 1 differential driver output data
TXD1N	52		
TXD2P	56	O	Channel – 2 differential driver output data
TXD2N	55		
CSET	58	I	Current setting. This pin requires a pull down resistor connected to AGNDT33. The value of this resistor will control the amplitude of the differential output voltage swing. Typical 390 Ohms.

Pin Name	Pin #	Type	Description
Analog Video Pins			
G/Y	66	O	Analog green or Y output. Capable of driving 37 Ohms load.
R/PR	67	O	Analog red or PR output. Capable of driving 37 Ohms load.
B/PB	68	O	Analog blue or PB output. Capable of driving 37 Ohms load.
AVDDT33	61	I	Differential drivers power supply (3.3V – nominal). See HD*Xtreme* Design Considerations Application Note.
RSET	64	I	Full-scale adjust. This pin requires a pull down resistor connected to GNDDAC. The value of this resistor will control the full-scale current drive on each of the analog outputs.
Power and Ground Pins			
VDDIP	9		Digital high-speed I/O power supply (3.3V – nominal).
VDDP	16,26,40,76		Digital I/O power supply (3.3V – nominal).
GNDP	13,24,34,74		Digital I/O ground.

VDDC	10,31,72		Digital core power supply (1.8V – nominal).
GNDC	12,33,70		Digital core ground.
VDDPLL	42		PLL power supply (3.3V – nominal).
GNDPLL	44		PLL ground.
AVDDT33	48,54		Differential drivers power supply (3.3V – nominal).
AGNDT33	45,51,57		Differential drivers ground.
AVDDT18	60		High-speed serialize power supply (1.8V – nominal).
AGNDT18	59		High-speed serialize ground.
GNDDACB	62		Internal bandgap ground
GNDDACP	63		Current control ground
AVDDDAC	65		DAC power supply (3.3V – nominal)
GNDDAC	69		DAC ground (3.3V – nominal)

5 ELECTRICAL SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65^0 to 150^0	C
VDDP, VDDIP, AVDDT33, VDDDAC Supply Voltage to Ground	-0.5 to 4.6	V
VDDC, VDDPLL, AVDDT18 Supply Voltage to Ground	-0.5 to 3.6	V
DC Voltage Applied to Outputs in High Impedance Output State at all pins but VIN[7:0]	-0.5 to 5.5	V
DC Voltage Applied to Outputs in High Impedance Output State at VIN[7:0]	-0.5 to 5.5	V
DC Voltage Applied to Digital Inputs at all pins but the VIN[7:0]	-0.5 to 5.5	V
DC Voltage Applied to Digital Inputs at all pins but the VIN[7:0]	-0.5 to 3.6	V
DC Input Current, any single input	-10 to 3.0	mA
DC Output Current, any single output apart form DACs	20	mA
Total Power Dissipation (P_{TOT})	2	W
ESD Voltage	2.0	kV

ZORAN CORPORATION

ZR36707TQCG

DVD 16x Analog Front-end IC

Electrical Specification

Revision 1.0 June 29, 2004

Print Date: September 15, 2004

TITLE	DOCUMENT NO.	REV.
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1.1.1 Features (continued)

Channel
- 100MHz bandwidth
- Supports individual RF inputs for DVD(differential or single_ended) and CD(single_ended)
- Supports internal summing mode for RF signal for DVD and CD respectively
- Programmable attenuator (min:-24dB, 4bit resolution)
- Fast attack mode for rapid AGC recovery
- Low drift AGC hold circuitry
- Signal Swing qualification circuit
- Temperature compensated, exponential control AGC
- Supports internal AGC HOLD control function
- Supports four ranges of Programmable cutoff frequency : 1 to 4.0MHz, 3.5 to 12MHz, 11 to 36MHz, 30 to 72MHz
- Programmable boost/equalization of 0 to 11dB
- Single-ended normal outputs for pulse qualification
- Differential normal signal outputs
- ± 20% Fc accuracy (Fc = 1 to 12 MHz)
- ± 15% Fc accuracy (Fc = 11 to 72 MHz)
- Less than 2% total harmonic distortion
- No external filter components required

Auto Laser Power Control
- Supports power mode selection
- Provides dual APC circuits for twin laser

VC reference voltage
- Supports VC (VPB/2) reference voltage output for internal and external circuits
- Supports V125(V25/2, reference voltage output) for internal servo output reference voltage

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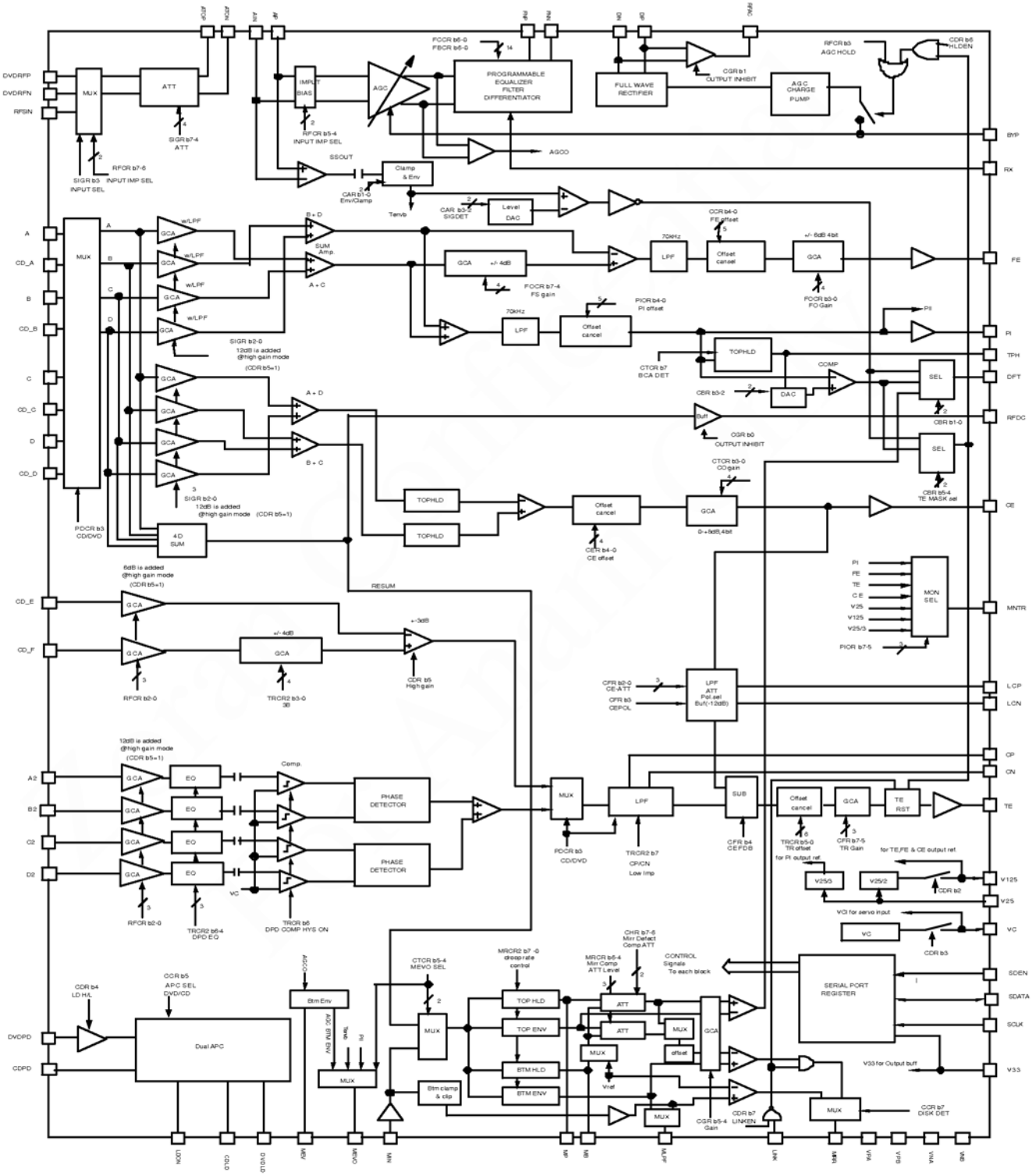
1.1.2 Block Diagram(Figure 1)



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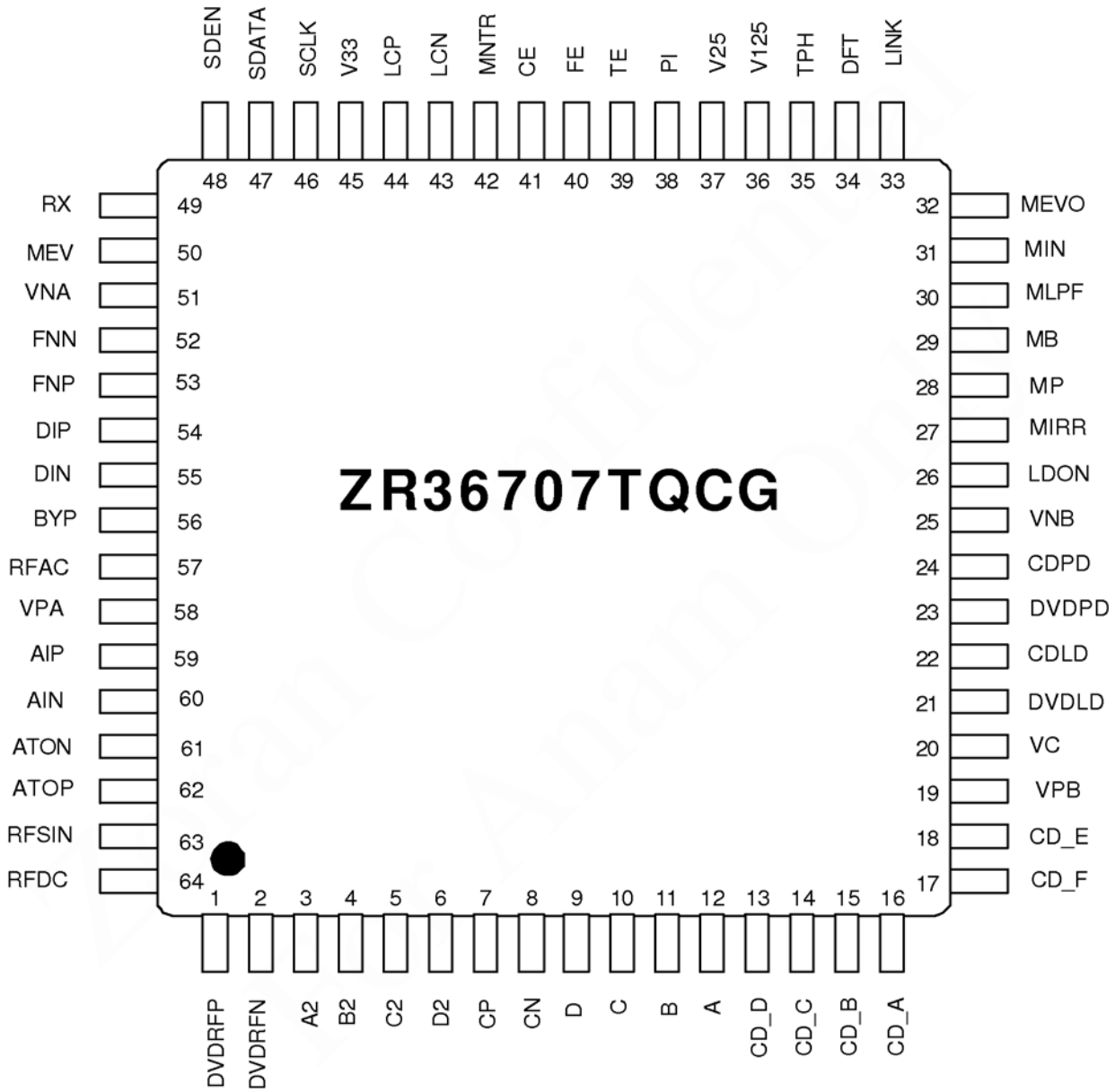
PACKAGE PIN DESIGNATIONS
(Top view)



CIRRUS LOGIC®

CS4382

114 dB, 192 kHz 8-Channel D/A Converter

Features

- 24-Bit Conversion
- Up to 192 kHz Sample Rates
- 114 dB Dynamic Range
- -100 dB THD+N
- Supports PCM and DSD Data Formats
- Selectable Digital Filters
- Volume Control with Soft Ramp
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- Dedicated DSD inputs
- Low Clock Jitter Sensitivity
- Simultaneous Support for Two Synchronous Sample Rates for DVD Audio
- µC or Stand-Alone Operation

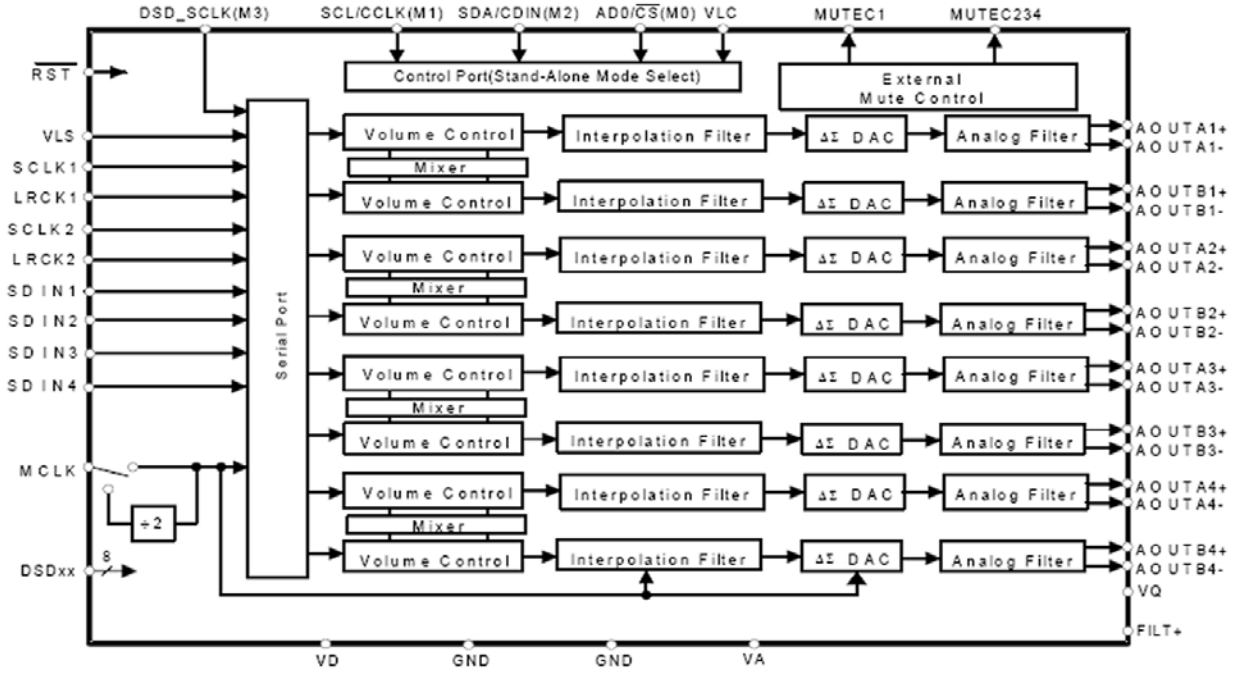
Description

The CS4382 is a complete 8-channel digital-to-analog system including digital interpolation, fifth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4382 accepts PCM data at sample rates from 4 kHz to 192 kHz, DSD audio data, and operates over a wide power supply range. These features are ideal for multi-channel audio systems including DVD players, SACD players, A/V receivers, digital TV's and VCR's, mixing consoles, effects processors, set-top boxes, and automotive audio systems.

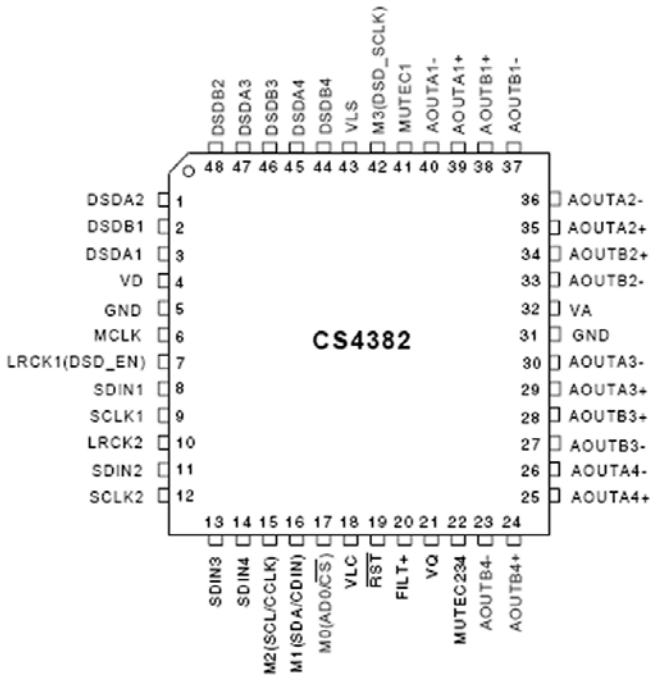
ORDERING INFORMATION

CS4382-KQZ, Lead Free	-10 to 70 °C	48-pin LQFP
CS4382-BQ	-40 to 85 °C	48-pin LQFP
CDB4382		Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

4. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	4	**Digital Power** (*Input*) **-** Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	5 31	**Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MCLK	6	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters. Table 5 illustrates several standard audio sample rates and the required master clock frequency.
LRCK1 LRCK2	7 10	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SDIN1 SDIN2 SDIN3 SDIN4	8 11 13 14	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK1 SCLK2	9 12	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
VLC	18	**Control Port Power** (*Input*) **-** Determines the required signal level for the control port. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{\text{RST}}$	19	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
FILT+	20	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to analog ground, as shown in the Typical Connection Diagram.
VQ	21	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage. VQ must be capacitively coupled to analog ground, as shown in the Typical Connection Diagram. The nominal voltage level is specified in the Analog Characteristics and Specifications section. VQ presents an appreciable source impedance and any current drawn from this pin will alter device performance. However, VQ can be used to bias the analog circuitry assuming there is no AC signal component and the DC current is less than the maximum specified in the Analog Characteristics and Specifications section.

Pin Name	#	Pin Description
MUTEC1 **MUTEC234**	41 22	**Mute Control** (*Output*) - The Mute Control pins go high during power-up initialization, reset, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect. These pins are intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
AOUTA1 +,- **AOUTB1 +,-** **AOUTA2 +,-** **AOUTB2 +,-** **AOUTA3 +,-** **AOUTB3 +,-** **AOUTA4 +,-** **AOUTB4 +,-**	39, 40 38, 37 35, 36 34, 33 29, 30 28, 27 25, 26 24, 23	**Differential Analog Output** (*Output*) - The full scale differential analog output level is specified in the Analog Characteristics specification table.
VA	32	**Analog Power** (*Input*) **-** Positive power supply for the analog section. Refer to the Recommended Operating Conditions for appropriate voltages.
VLS	43	**Serial Audio Interface Power** (*Input*) **-** Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
Control Port Definitions		
SCL/CCLK	15	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I^2C mode as shown in the Typical Connection Diagram.
SDA/CDIN	16	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line in I^2C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDIN is the input data line for the control port interface in SPI mode.
AD0/$\overline{CS}$	17	**Address Bit 0 (I^2C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I^2C mode; $\overline{CS}$ is the chip select signal for SPI format.
Stand-Alone Definitions		
M0 **M1** **M2** **M3**	17 16 15 42	**Mode Selection** (*Input*) - Determines the operational mode of the device as detailed in Tables 6 and 7.
DSD Definitions		
DSD_SCLK	42	**DSD Serial Clock** (*Input*) - Serial clock for the Direct Stream Digital audio interface.
DSD_EN	7	**DSD-Enable** *(Input)* - When held at logic '1' the device will enter DSD mode (Stand-Alone mode only).
DSDA1 **DSDB1** **DSDA2** **DSDB2** **DSDA3** **DSDB3** **DSDA4** **DSDB4**	3 2 1 48 47 46 45 44	**Direct Stream Digital Input** (*Input*) - Input for Direct Stream Digital serial audio data.

ESMT **M12L64164A**

SDRAM 1M x 16 Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

ORDERING INFORMATION

54 Pin TSOP (Type II)
(400mil x 875mil)

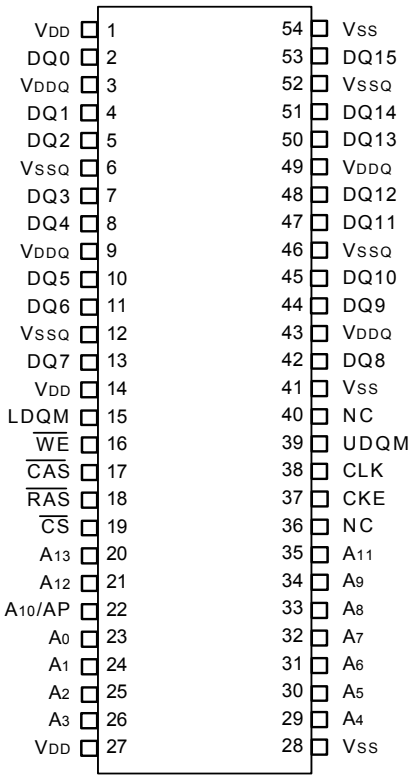
PRODUCT NO.	MAX FREQ.	PACKAGE
M12L64164A-6T	166MHz	TSOP II
M12L64164A-7T	143MHz	

GENERAL DESCRIPTION

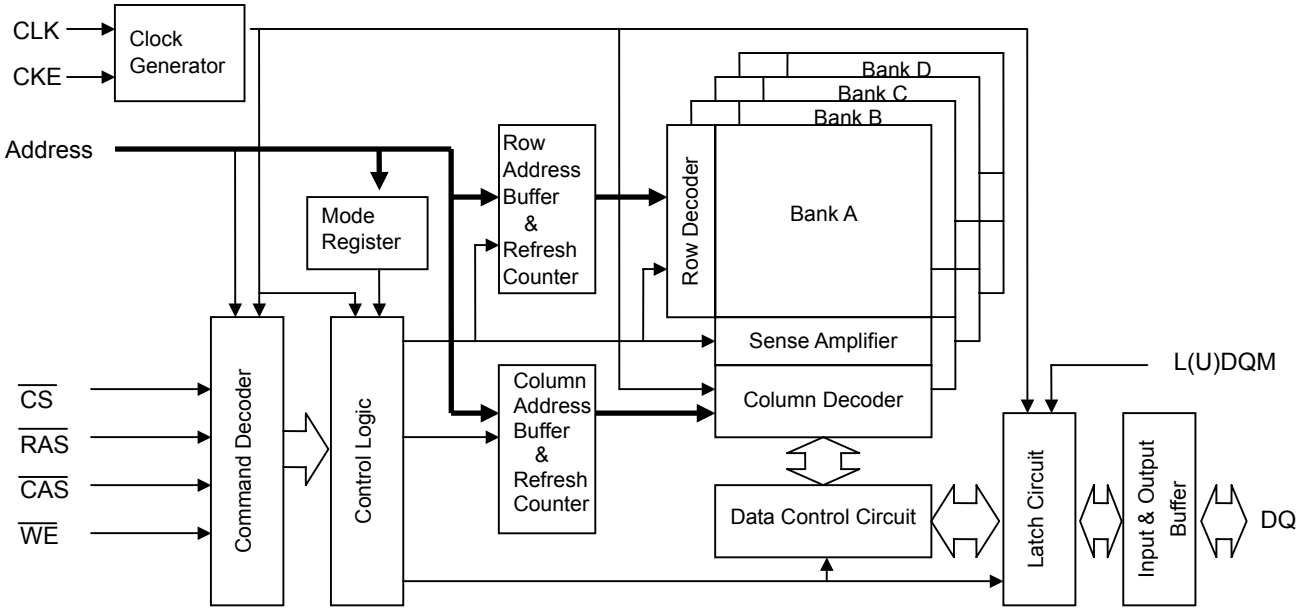
The M12L64164A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits. Synchronous design allows precise cycle controls with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

PIN ASSIGNMENT

Top View



FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK , CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row / column address are multiplexed on the same pins. Row address : RA0~RA11, column address : CA0~CA7
A12 , A13	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column address on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	Data Input / Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ DQ15	Data Input / Output	Data inputs / outputs are multiplexed on the same pins.
VDD / VSS	Power Supply / Ground	Power and ground for the input buffers and the core logic.
VDDQ / VSSQ	Data Output Power / Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left No Connection on the device.

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of setup and hold time around positive edge of the clock for proper functionality and Icc specifications.

CLOCK ENABLE(CKE)

The clock enable (CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + t_{SS}" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK ADDRESSES (A13~A12)

This SDRAM is organized as four independent banks of 1,048,576 words x 16 bits memory arrays. The A13~A12 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The banks addressed A13~A12 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0~A11)

The 20 address bits are required to decode the 1,048,576 word locations are multiplexed into 12 address input pins (A0~A11). The 12 row addresses are latched along with $\overline{RAS}$ and A13~A12 during bank active command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and A13~A12 during read or with command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, The SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

1. Apply power and start clock, Attempt to maintain CKE = "H", DQM = "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for minimum of 200us.
3. Issue precharge commands for both banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
   cf.) Sequence of 4 & 5 is regardless of the order.

   The device is now ready for normal operation.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0~A11 and A13~A12 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields into depending on functionality. The burst length field uses A0~A2, burst type uses A3, CAS latency (read latency from column address) use A4~A6, vendor specific options or test mode use A7~A8, A10/AP~A11 and A13~A12. The write burst length is programmed using A9. A7~A8, A10/AP~A11 and A13~A12 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

DEVICE OPERATIONS (Continued)

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of $t_{RCD\ (min)}$ from the time of bank activation. t_{RCD} is the internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing $t_{RCD\ (min)}$ with cycle time of the clock and then rounding of the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before another bank can be sensed reliably. $t_{RRD\ (min)}$ specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by $t_{RAS\ (min)}$. Every SDRAM bank activate command must satisfy $t_{RAS\ (min)}$ specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by $t_{RAS\ (max)}$ and $t_{RAS\ (max)}$ can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{RAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least $t_{RCD\ (min)}$ before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be complete by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

DQM OPERATION

The DQM is used mask input and output operations. It works similar to $\overline{OE}$ during operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is required. Please refer to DQM timing diagram also.

PRECHARGE

The precharge is performed on an active bank by asserting low on clock cycles required between bank activate and clock cycles required between bank activate and $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A10/AP with valid A13~A12 of the bank to be procharged. The precharge command can be asserted anytime after $t_{RAS\ (min)}$ is satisfy from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing tRP with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by $t_{RAS\ (max)}$. Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to power-down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

DEVICE OPERATIONS (Continued)

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy $t_{RAS\ (min)}$ and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst write by asserting high on A10/AP, the bank is precharge command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A10/AP after all banks have satisfied $t_{RAS\ (min)}$ requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge all, all banks are in idle state.

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by $t_{RFC\ (min)}$. The minimum number of clock cycles required can be calculated by driving t_{RFC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or the burst of 4096 auto refresh cycles in 64ms.

SELF REFRESH

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption. The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the refresh.
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 4096 auto refresh cycles immediately after exiting self refresh.

TOSHIBA TC74HCT7007AP/AF

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

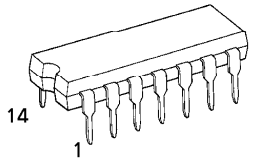
TC74HCT7007AP, TC74HCT7007AF

HEX BUFFER

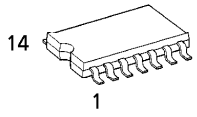
The TC74HCT7007A is a high speed CMOS BUFFER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
The internal circuit is composed of 4 stages including a buffer output, which provides high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 11ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 1μA(Max.) at Ta = 25°C
- Compatible with TTL outputs .... V_{IH} = 2V (Min.)
  V_{IL} = 0.8V (Max.)
- Wide Interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74LS07

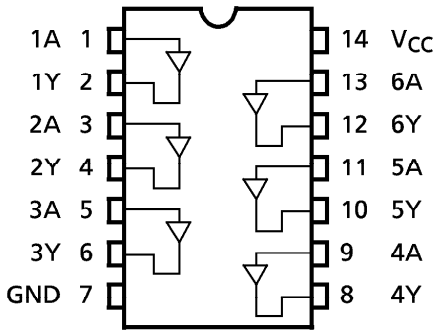


P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)



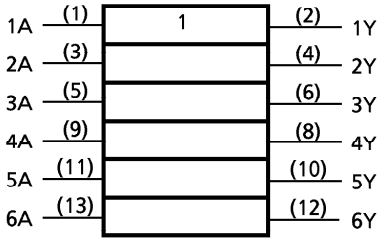
F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



PIN ASSIGNMENT

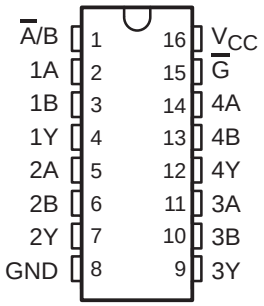
A	Y
L	L
H	H

SN74LVC157A
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS292G – JANUARY 1993 – REVISED OCTOBER 1998

- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Inputs Accept Voltages to 5.5 V**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC157A features a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The device provides true data.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC157A is characterized for operation from –40°C to 85°C.

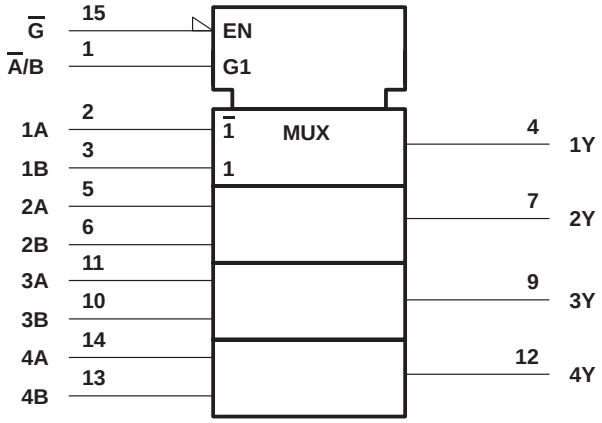
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN74LVC157A
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

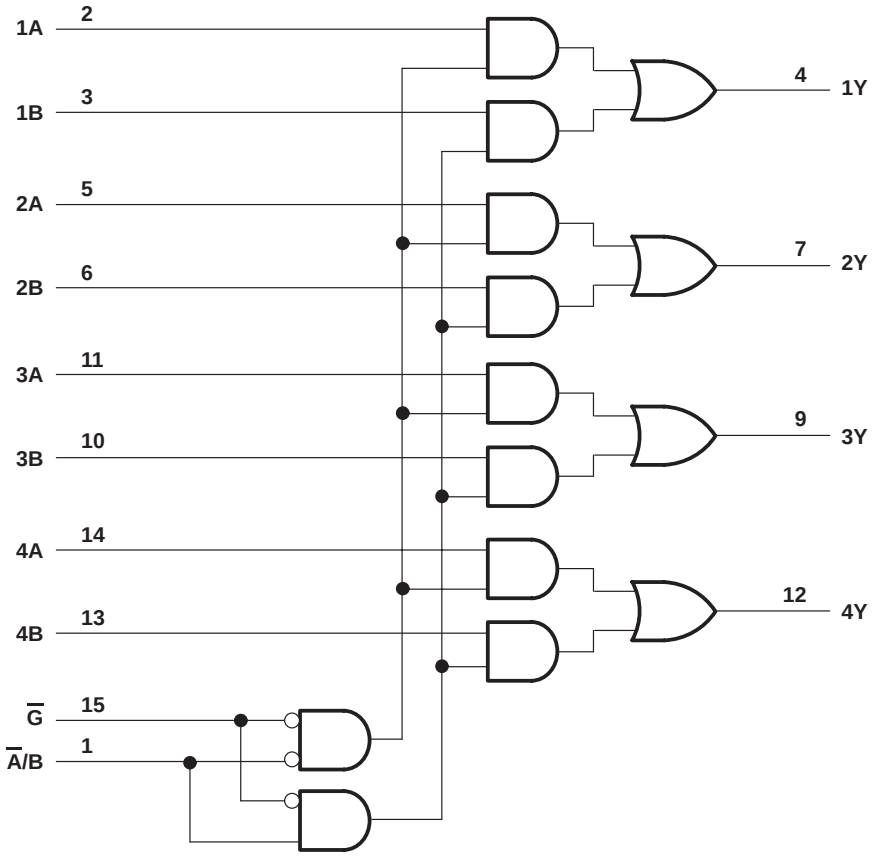
SCAS292G – JANUARY 1993 – REVISED OCTOBER 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FAIRCHILD SEMICONDUCTOR®

November 1992
Revised February 2005

74VHC04
Hex Inverter

General Description

The VHC04 is an advanced high speed CMOS Inverter fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: t_{PD} = 3.8 ns (typ) at V_{CC} = 5V
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- Power down protection is provided on all inputs
- Low Noise: V_{OLP} = 0.4V (typ)
- Low power dissipation: I_{CC} = 2 μA (Max) @ T_A = 25°C
- Pin and function compatible with 74HC04

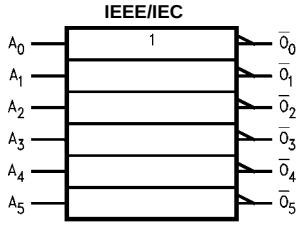
Ordering Code:

Order Number	Package Number	Package Description
74VHC04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC04MX_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC04SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC04MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

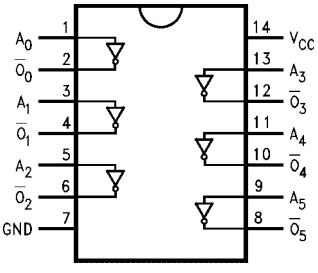
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

A	$\overline{O}$
L	H
H	L

5-channel BTL Driver for DVD player AM5888S

The AM5888S is a five-channel BTL driver IC for driving the motors and actuators such as used in DVD player and consists of two independent precision voltage regulators with adjustable range from 1.5V to 4 V. It supports a variety of applications. Also, Pb free package is selectable (Please refer to Marking Identification).

● Applications

BTL driver for CD, CD-ROM and DVD.

● Features

1) Two channels are voltage-type BTL drivers for actuators of tracking and focus. Two channels are voltage-type BTL driver for sled and spindle motors. It is also built-in one channel bi-direction DC motor driver for tray.
2) Wide dynamic range [9.0V (*typ.*) when Vcc1= Vcc2= 12V, at R_L= 20Ω load].
3) Separating power of Vcc1 and Vcc2 is to improve power efficiency by a low supply voltage for tracking, focus, and spindle.
4) Level shift circuit built-in.
5) Thermal shut down circuit built-in.
6) Mute mode built-in.
7) **Dual actuator drivers:**
   A general purpose input OP provides differential input for signal addition. The output structure is two power OPAMPS in bridge configuration.
8) **Sled motor driver:**
   A general purpose input OP provides differential input for signal addition. The output structure is one power OPAMP in bridge configuration.
9) **Spindle driver:**
   Single input linear BTL driver. The output structure are two power OPAMPS in bridge configuration.
10) **Tray in-out driver:**
    The DC motor driver supports forward/reverse control for tray motor.
11) 2 **Built-in regulator controllers**
    Adjustable range 1.5V ~ 4V

AM5888S
Motor Driver ICs

● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	Vcc1 Vcc2	13.5	V
Power dissipation	P_d	*1.7	W
Operate Temp range	T_{opr}	-35 ~ +85	℃
Storage Temp range	T_{stg}	**-55 ~ +150	℃

*When mounted on a 70mm×70mm×1.6mm glass epoxy board.

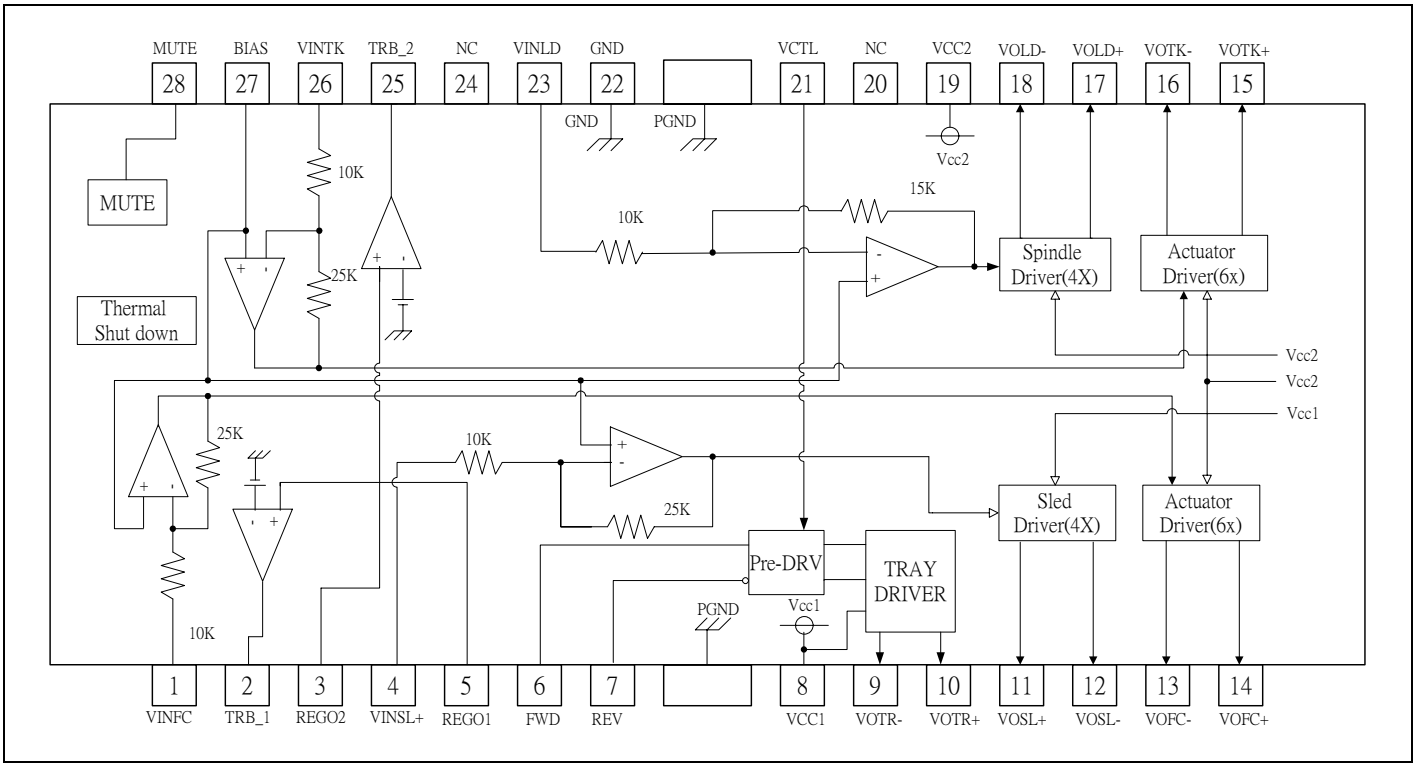
*Reduced by 13.6mW for each increase in T_a of 1℃ over 25℃.

**Should not exceed Pd or ASO and T_j=150℃ values

● Guaranteed operating conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc1	4.3 ~ 13.2	V
	Vcc2	4.3 ~ Vcc1	V

● Block diagram



● Pin description

PIN No	Pin Name	Function
1	VINFC	Input for focus driver
2	TRB_1	Connect to external transistor base
3	REGO2	Regulator voltage output, connect to external transistor collector
4	VINSL+	Input for the sled driver
5	REGO1	Regulator voltage output, connect to external transistor collector
6	FWD	Tray driver forward input
7	REV	Tray driver reverse input
8	Vcc1	Vcc for pre-drive block and power block of sled and tray
9	VOTR-	Tray driver output (-)
10	VOTR+	Tray driver output (+)
11	VOSL+	Sled driver output (+)
12	VOSL-	Sled driver output (-)
13	VOFC-	Focus driver output (-)
14	VOFC+	Focus driver output (+)
15	VOTK+	Tracking driver output (+)
16	VOTK-	Tracking driver output (-)
17	VOLD+	Spindle driver output (+)
18	VOLD-	Spindle driver output (-)
19	Vcc2	Vcc for power block of spindle, tracking and focus
20	NC	No Connection
21	VCTL	Speed control input of tray driver
22	GND	Ground
23	VINLD	Input for spindle driver
24	NC	No Connection
25	TRB_2	Connect to external transistor base
26	VINTK	Input for tracking driver
27	BIAS	Input for reference voltage
28	MUTE	Input for mute control

Notes) Symbol of + and – (output of drivers) means polarity to input pin.
(For example, if voltage of pin1 is high, pin14 is high.)

Features

- **Medium-voltage and Standard-voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
- **Automotive Temperature Range –40°C to 125°C**
- **Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)**
- **Two-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **400 kHz (2.7V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **8-byte Page (1K, 2K), 16-byte Page (4K, 8K, 16K) Write Modes**
- **Partial Page Writes are Allowed**
- **Self-timed Write Cycle (5 ms max)**
- **High-reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP Packages**

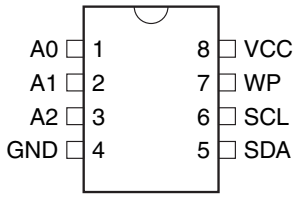
Description

The AT24C01A/02/04/08A/16A provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many automotive applications where low-power and low-voltage operation are essential. The AT24C01A/02/04/08A/16A is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP packages and is accessed via a two-wire serial interface. In addition, the entire family is available in 2.7V (2.7V to 5.5V) versions.

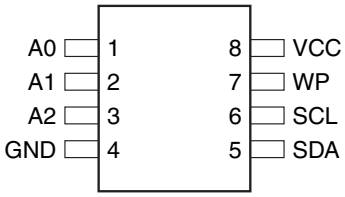
Table 1. Pin Configurations

Pin Name	Function
A0 – A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

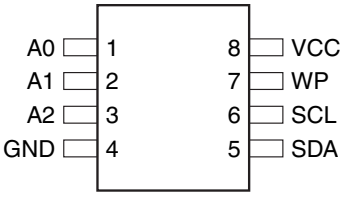
8-lead PDIP



8-lead SOIC



8-lead TSSOP



Two-wire Automotive Temperature Serial EEPROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

AT24C01A
AT24C02
AT24C04
AT24C08A
AT24C16A

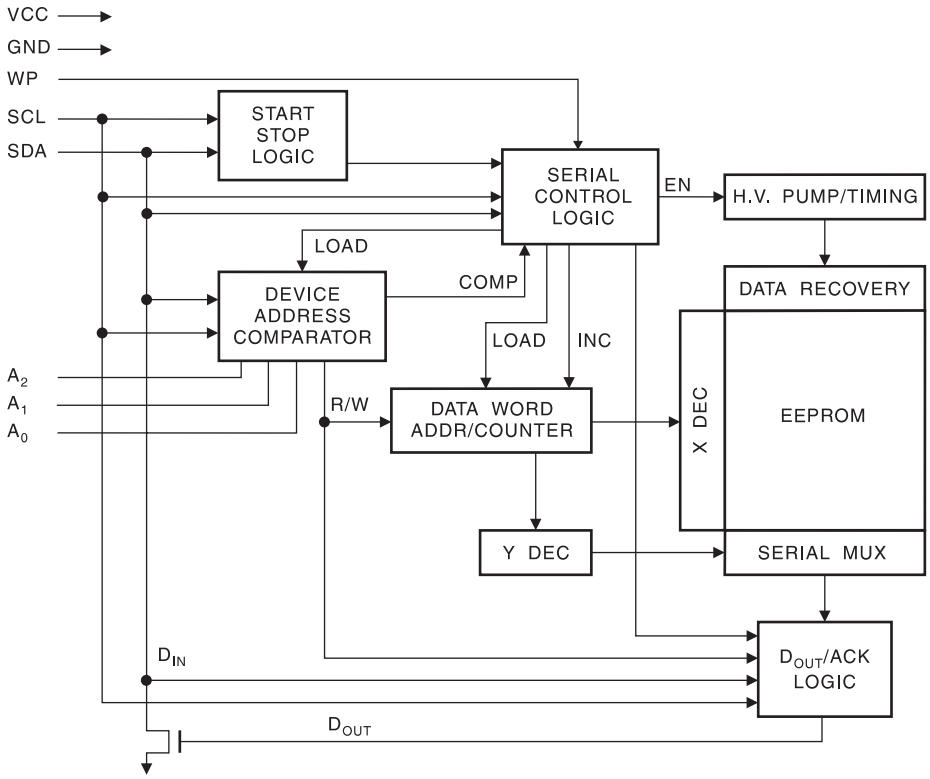
5092B–SEEPR–9/05

Absolute Maximum Ratings

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

AT24C01A/02/04/08A/16A

The AT24C08A only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16A does not use the device address pins, which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

WRITE PROTECT (WP): The AT24C01A/02/04/08A/16A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

Table 2. Write Protect

WP Pin Status	Part of the Array Protected				
	24C01A	24C02	24C04	24C08A	24C16A
At V_{CC}	Full (1K) Array	Full (2K) Array	Full (4K) Array	Full (8K) Array	Full (16K) Array
At GND	Normal Read/Write Operations				

Memory Organization

AT24C01A, 1K SERIAL EEPROM: Internally organized with 16 pages of 8 bytes each, the 1K requires a 7-bit data word address for random word addressing.

AT24C02, 2K SERIAL EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

AT24C04, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

AT24C08A, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

AT24C16A, 16K SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

AT24C01A/02/04/08A/16A

Table 5. AC Characteristics

Applicable over recommended operating range from T_A = –40°C to +125°C, V_{CC} = +2.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	AT24C01A/02/04/08A/16A		Units
		Min	Max	
f_{SCL}	Clock Frequency, SCL		400	kHz
t_{LOW}	Clock Pulse Width Low	1.2		µs
t_{HIGH}	Clock Pulse Width High	0.6		µs
t_I	Noise Suppression Time(1)		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(2)	1.2		µs
$t_{HD.STA}$	Start Hold Time	0.6		µs
$t_{SU.STA}$	Start Set-up Time	0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		ns
t_R	Inputs Rise Time(2)		300	ns
t_F	Inputs Fall Time(2)		300	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		µs
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		5	ms
Endurance(2)	5.0V, 25°C, Page Mode	1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested (T_A = 25°C).
2. This parameter is characterized.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4 on page 7). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 5 on page 7).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 5 on page 7).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C01A/02/04/08A/16A features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

High-performance 6-channel video driver IC for progressive DVD

BH7862FS

BH7862FS is a 6-channel video driver IC developed for progressive DVD player/recorder. Special filters adjusted to each band of various video signals are incorporated into a single chip. Extended definition, size reduction, and high cost performance can be achieved in DVD players.

●Application

DVD players, DVD recorders

●Features

1) Each high-performance filter, 6dB amplifier, and 75Ω driver for DVD are incorporated into a single chip.
2) Driver 6ch (Y, C, MIX, and PY, Pb, Pr for progressive)
3) Group delay difference between chroma signal and luminance signal is a small number of nsec.
4) Drive 2 lines of each signal
5) Operating by 5V single power supply
6) Built-in mute circuit

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Impressed voltage	V_{CC} max	6.0	V
Power dissipation	Pd	0.95*	W
Operating temperature range	Topr	−10~+70	°C
Storage temperature range	Tstg	−55~+150	°C

* Reduced by −7.6mW for each increase in Ta of 1°C over 25°C.
PCB (70mm×70mm, t=1.6mm) glass epoxy mounting.

●Recommended operating conditions (Ta = 25°C)

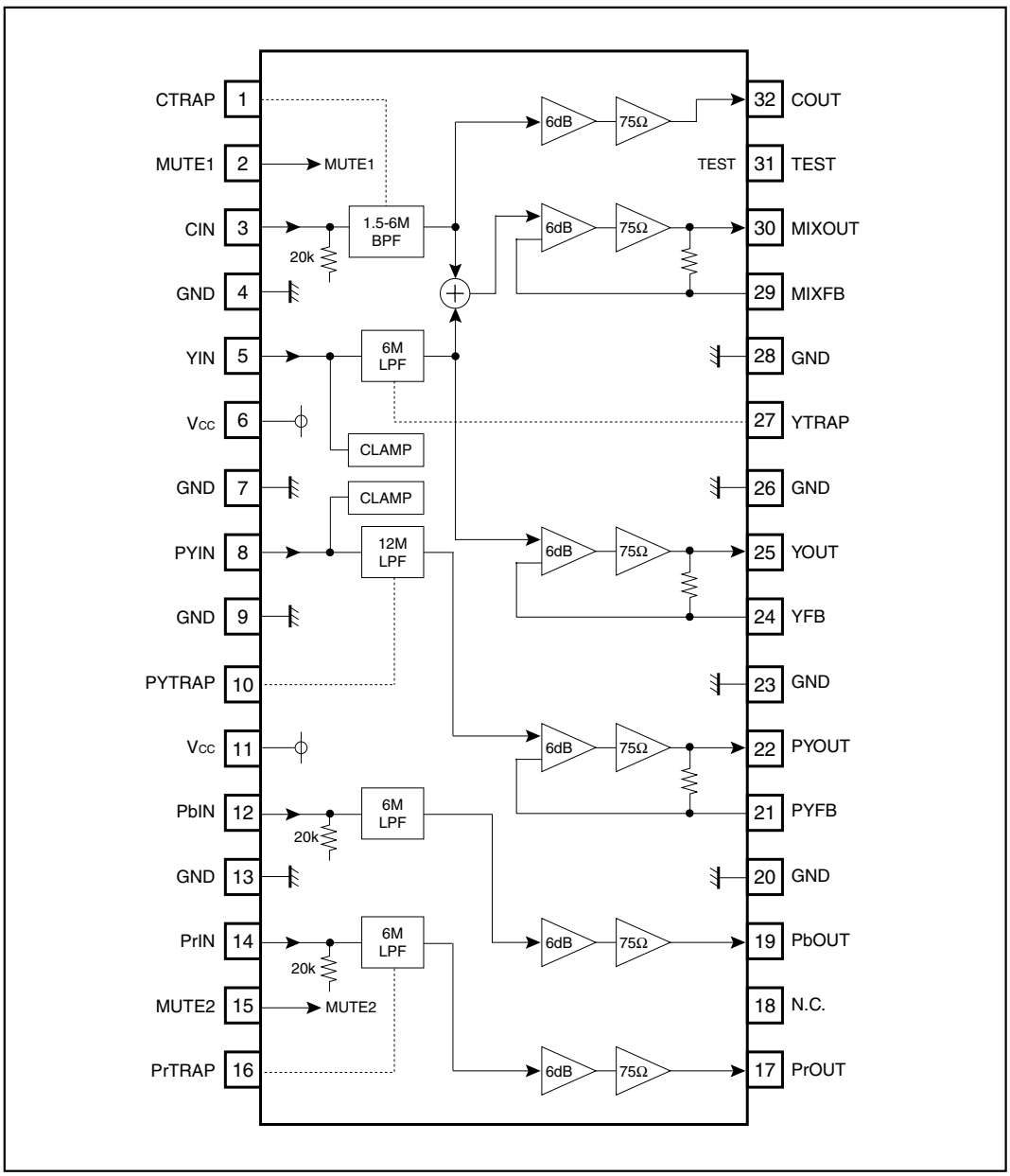
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	−	5.5	V

◎Radiation resistance is not included in the design.

BH7862FS

Multimedia ICs

●Block diagram

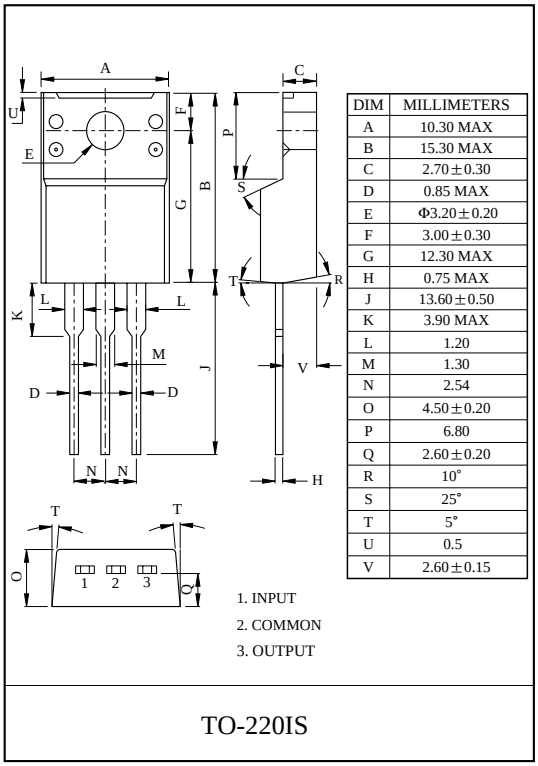


KEC

SEMICONDUCTOR
TECHNICAL DATA

KIA7805API~ KIA7824API
BIPOLAR LINEAR INTEGRATED CIRCUIT

THREE TERMINAL POSITIVE VOLTAGE REGULATORS
5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V.



DIM	MILLIMETERS
A	10.30 MAX
B	15.30 MAX
C	2.70±0.30
D	0.85 MAX
E	Φ3.20±0.20
F	3.00±0.30
G	12.30 MAX
H	0.75 MAX
J	13.60±0.50
K	3.90 MAX
L	1.20
M	1.30
N	2.54
O	4.50±0.20
P	6.80
Q	2.60±0.20
R	10°
S	25°
T	5°
U	0.5
V	2.60±0.15

TO-220IS

FEATURES

· Suitable for C-MOS, TTL, the Other Digital IC's Power Supply.
· Internal Thermal Overload Protection.
· Internal Short Circuit Current Limiting.
· Output Current in Excess of 1A.
· Satisfies IEC-65 Specification. (International Electronical Commission)

MAXIMUM RATINGS (Ta=25℃)

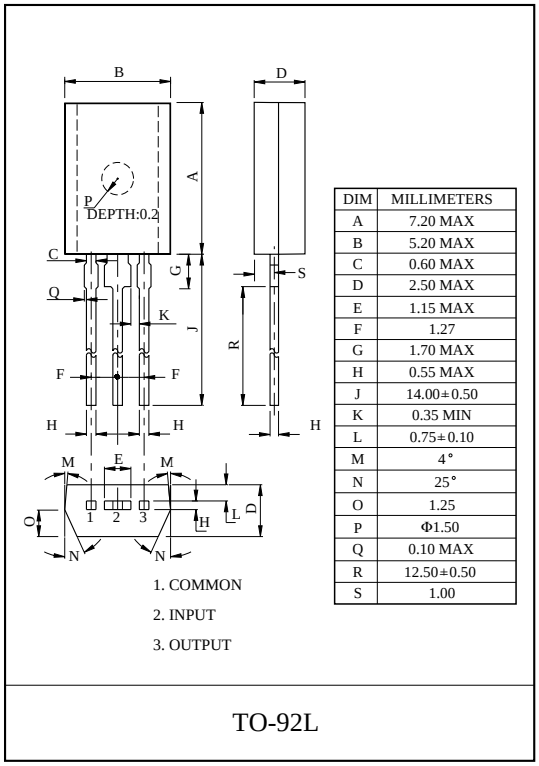
CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	KIA7805API ~ KIA7815API	V_{IN}	35	V
	KIA7818API ~ KIA7824API		40	
Power Dissipation (Tc=25℃)		P_D	20.8	W
Power Dissipation (Without Heatsink)	KIA7805API ~ KIA7824API	P_D	2.0	W
Operating Junction Temperature		T_j	-30 ~150	℃
Storage Temperature		T_{stg}	-55 ~150	℃

KEC

KIA79L05BP~ KIA79L24BP

BIPOLAR LINEAR INTEGRATED CIRCUIT

THREE TERMINAL POSITIVE VOLTAGE REGULATORS
5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V.



DIM	MILLIMETERS
A	7.20 MAX
B	5.20 MAX
C	0.60 MAX
D	2.50 MAX
E	1.15 MAX
F	1.27
G	1.70 MAX
H	0.55 MAX
J	14.00±0.50
K	0.35 MIN
L	0.75±0.10
M	4°
N	25°
O	1.25
P	Φ1.50
Q	0.10 MAX
R	12.50±0.50
S	1.00

TO-92L

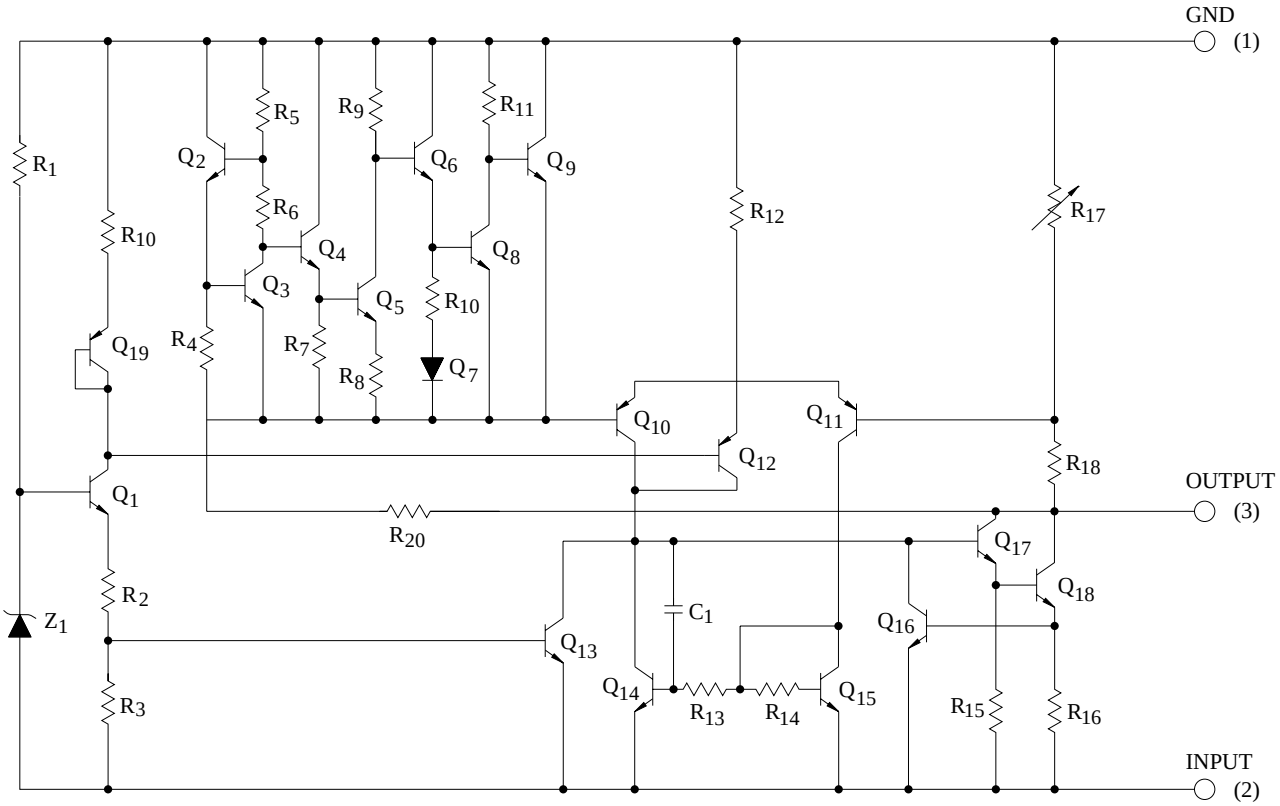
FEATURES

- Best Suited to a Power Supply for TTL and CMOS.
- Built-in Overcurrent Protective Circuit.
- Built-in Thermal Protective Circuit.
- Max. Output Current 150mA (T_j=25 ℃).
- Packaged in TO-92L.

MAXIMUM RATINGS (Ta=25 ℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	KIA79L05BP ~ KIA79L15BP	V_{IN}	-35	V
	KIA79L18BP ~ KIA79L24BP		-40	
Power Dissipation (Tc=25℃)		P_D	800	mW
Operating Junction Temperature		T_j	-30 ~ 150	℃
Operating Temperature		T_{opr}	-30 ~ 75	℃
Storage temperature		T_{stg}	-55 ~ 150	℃

EQUIVALENT CIRCUIT



Optic receiver modules

KODENSHI

KSM - 60 钡 TH2 · KSM - 70 钡 TH2

The KSM - 60钡TH2 consist of a PIN Photodiode of high speed and a preamplifier IC in the package as an receiver for Infrared remote control systems

FEATURES

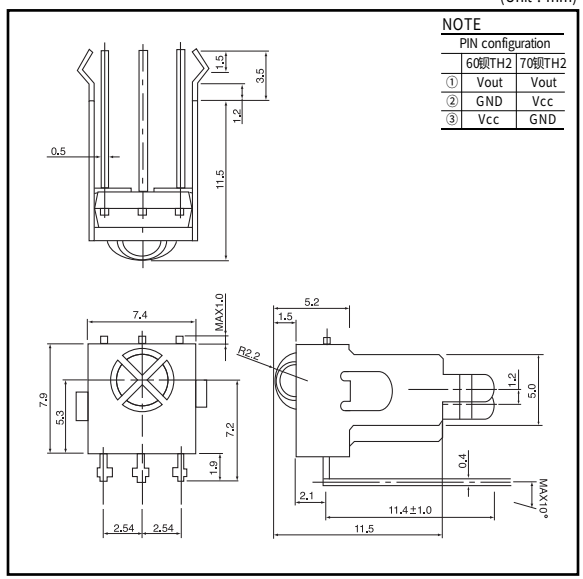
- One mold small package
- 5 Volt supply voltage, low power consumption
- Shielded against electrical field disturbance
- High immunity against ambient light
- Easy interface with the main board
- TTL and CMOS compatibility

APPLICATIONS

- TV, VTR, Acoustic Devices, Air Conditioners, Car Stereo Units, Computers, Interior controlling appliances, and all appliances that require remote controlling

DIMENSIONS

(Unit : mm)



MAXIMUM RATINGS

(Ta=25℃ Unless otherwise noted)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	5.5	V
Operating Temperature	Topr.	- 10~+60	℃
Storage Temperature	Tstg.	- 20~+75	℃
Soldering Temperature	Tsol.	260(Max 5 sec)	℃

B.P.F CENTER FREQUENCY

Model NO.	B.P.F Center Frequency(kHz)
KSM - ◯◯1 TH2	40.0
KSM - ◯◯2 TH2	36.7
KSM - ◯◯3 TH2	37.9
KSM - ◯◯4 TH2	32.7
KSM - ◯◯5 TH2	56.9

ELECTRO-OPTICAL CHARACTERISTICS

(Ta=25℃), Vcc=5.0V

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit.
Supply Voltage	V_{CC}			4.5	5.0	5.5	V
Current Consumption	I_{CC}	Input Signal=0		-	1.2	2.5	mA
Peak Wavelength *1	λp			-	940	-	nm
B.P.F Center Frequency	fo			-	37.9	-	kHz
Transmission Distance *1	L	200±50lx	0°	10	-	-	m
			±30°	7	-	-	m
H Level Output Voltage *1	V_{OH}	30cm over the ray axis		4.5	5.0	-	V
L Level Output Voltage *1	V_{OL}			-	0.1	0.5	V
H Level Output Pulse Width *1	T_{WH}	Burst Wave=600μs Period=1.2ms		500	600	700	μs
L Level Output Pulse Width *1	T_{WL}			500	600	700	μs
Output Form				Active Low Output			

Note : *1. It specifies the maximum distance between emitter and detector that the output waveform satisfies the standard under the conditions below against the standard transmitter

1) Measuring place : Indoor without extreme reflection of light
2) Ambient light source : Detecting surface illumination shall be irradiate 200±50lx under ordinary white fluorescence lamp without high frequency lightning
3) Standard transmitter : Burst wave of standard transmitter shall be arranged to 50mVp - p under the measuring circuit

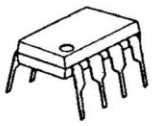
NJM2068

LOW-NOISE DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2068 is a high performance, low noise dual operational amplifier. This amplifier features popular pin-out, superior noise performance, and superior total harmonic distortion. This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product and slew rate, which far exceeds that of the 4558 type amplifier. The specially designed low noise input transistors allow the NJM2068 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifier.

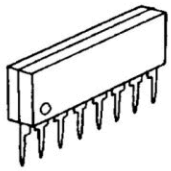
■ PACKAGE OUTLINE



NJM2068D

NJM2068M

NJM2068V

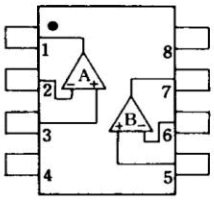


NJM2068L

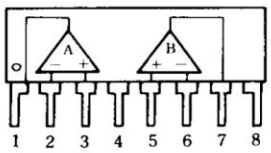
■ FEATURES

● Operating Voltage	(±4V~±18V)
● Low Total Harmonic Distortion	(0.001% typ.)
● Low Noise Voltage	(FLAT+JISA,0.56μV typ.)
● High Slew Rate	(6V/μs typ.)
● Unity Gain Bandwidth	(27MHz @ f=10kHz)
● Package Outline	DIP8,DMP8,SIP8,SSOP8
● Bipolar Technology	

■ PIN CONFIGURATION



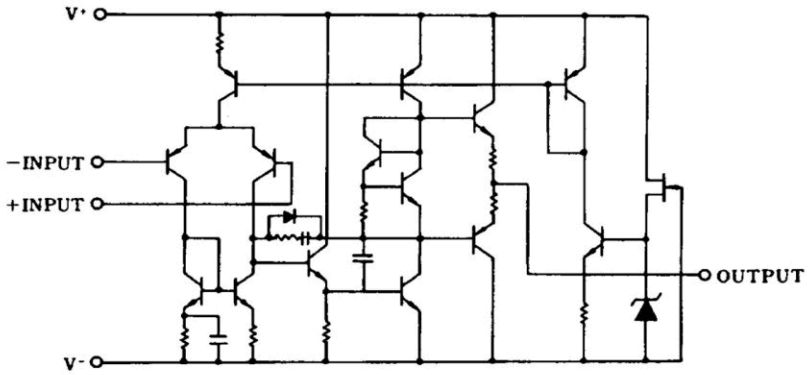
NJM2068D
NJM2068M
NJM2068V



NJM2068L

PIN FUNCTION
1.A OUTPUT
2.A –INPUT
3.A +INPUT
4.V^-
5.B +INPUT
6.B –INPUT
7.B OUTPUT
8.V^+

■ EQUIVALENT CIRCUIT (1/2 Shown)



National Semiconductor

October 2002

LM1117/LM1117I
800mA Low-Dropout Linear Regulator

General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V.

The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%.

The LM1117 series is available in LLP, TO-263, SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

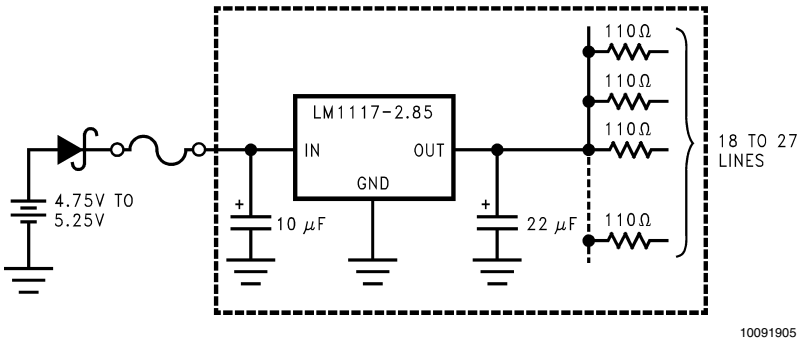
- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 and LLP Packages
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
  - — LM1117 0˚C to 125˚C
  - — LM1117I –40˚C to 125˚C

Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators
- Battery Charger
- Battery Powered Instrumentation

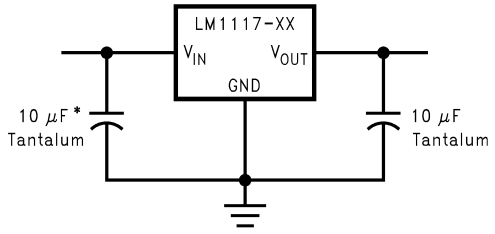
Typical Application

Active Terminator for SCSI-2 Bus



10091905

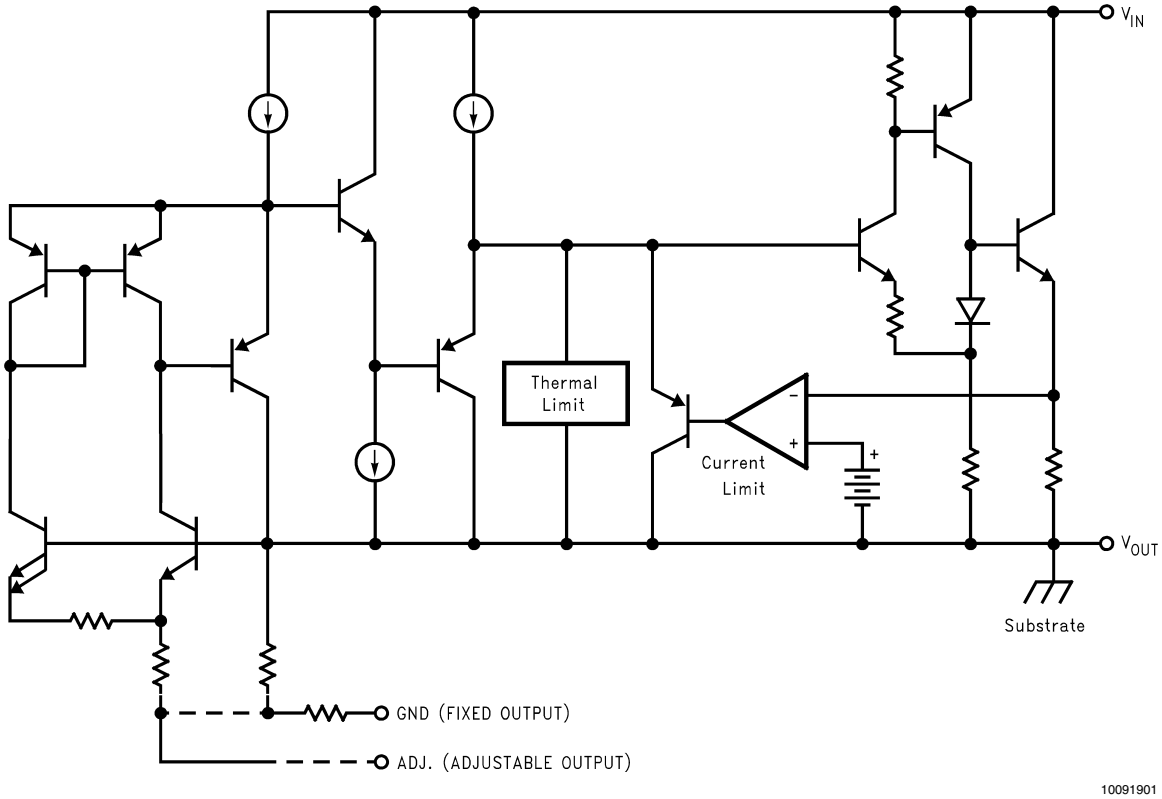
Fixed Output Regulator



*Required if the regulator is located far from the power supply filter.

10091928

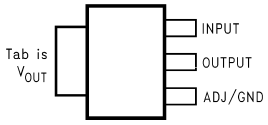
Block Diagram



10091901

Connection Diagrams

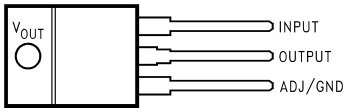
SOT-223



10091904

Top View

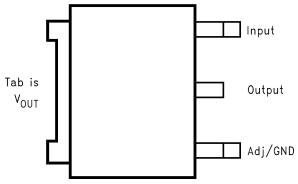
TO-220



10091902

Top View

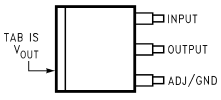
TO-252



10091938

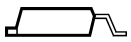
Top View

TO-263



10091944

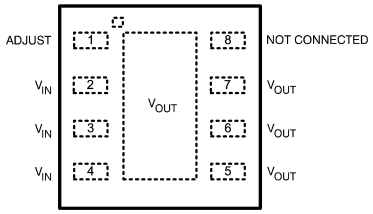
Top View



10091945

Side View

LLP



10091946

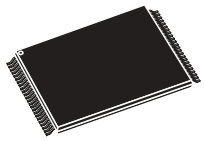
When using the LLP package
Pins 2, 3 & 4 must be connected together and
Pins 5, 6 & 7 must be connected together

Top View

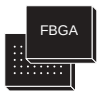
FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{CC} = 2.7V to 3.6V for Program, Erase and Read
- ACCESS TIMES: 70, 90ns
- PROGRAMMING TIME
  - 10µs per Byte/Word typical
- 35 MEMORY BLOCKS
  - 1 Boot Block (Top or Bottom Location)
  - 2 Parameter and 32 Main Blocks
- PROGRAM/ERASE CONTROLLER
  - Embedded Byte/Word Program algorithms
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- TEMPORARY BLOCK UNPROTECTION MODE
- COMMON FLASH INTERFACE
  - 64 bit Security Code
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Top Device Code M29W160ET: 22C4h
  - Bottom Device Code M29W160EB: 2249h

Figure 1. Packages



TSOP48 (N)
12 x 20mm



TFBGA48 (ZA)
6 x 8mm

SUMMARY DESCRIPTION

The M29W160E is a 16 Mbit (2Mb x8 or 1Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The blocks in the memory are asymmetrically arranged, see Figures 5 and 6, Block Addresses. The first or last 64 KBytes have been divided into four additional blocks. The 16 KByte Boot Block can be used for small initialization code to start the microprocessor, the two 8 KByte Parameter Blocks can be used for parameter storage and the remaining 32K is a small Main Block where the application may be stored.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered TSOP48 (12 x 20mm) and TFBGA48 (0.8mm pitch) packages. The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

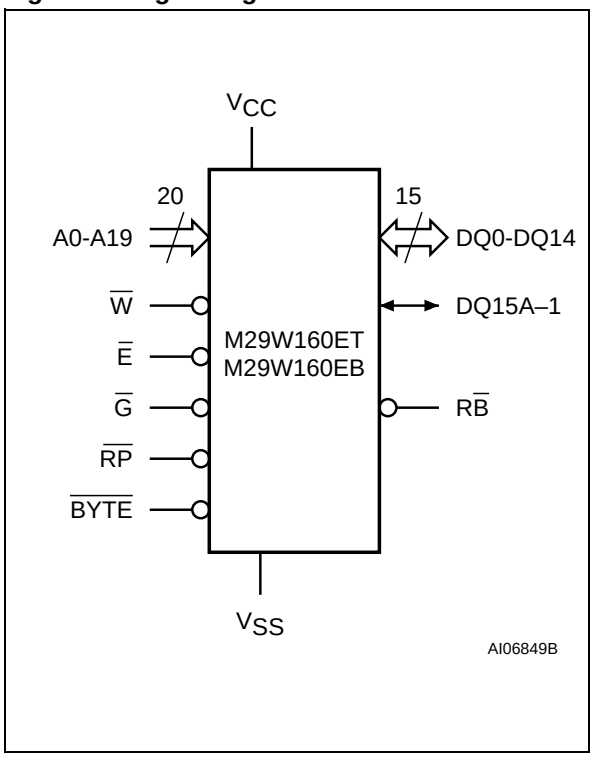
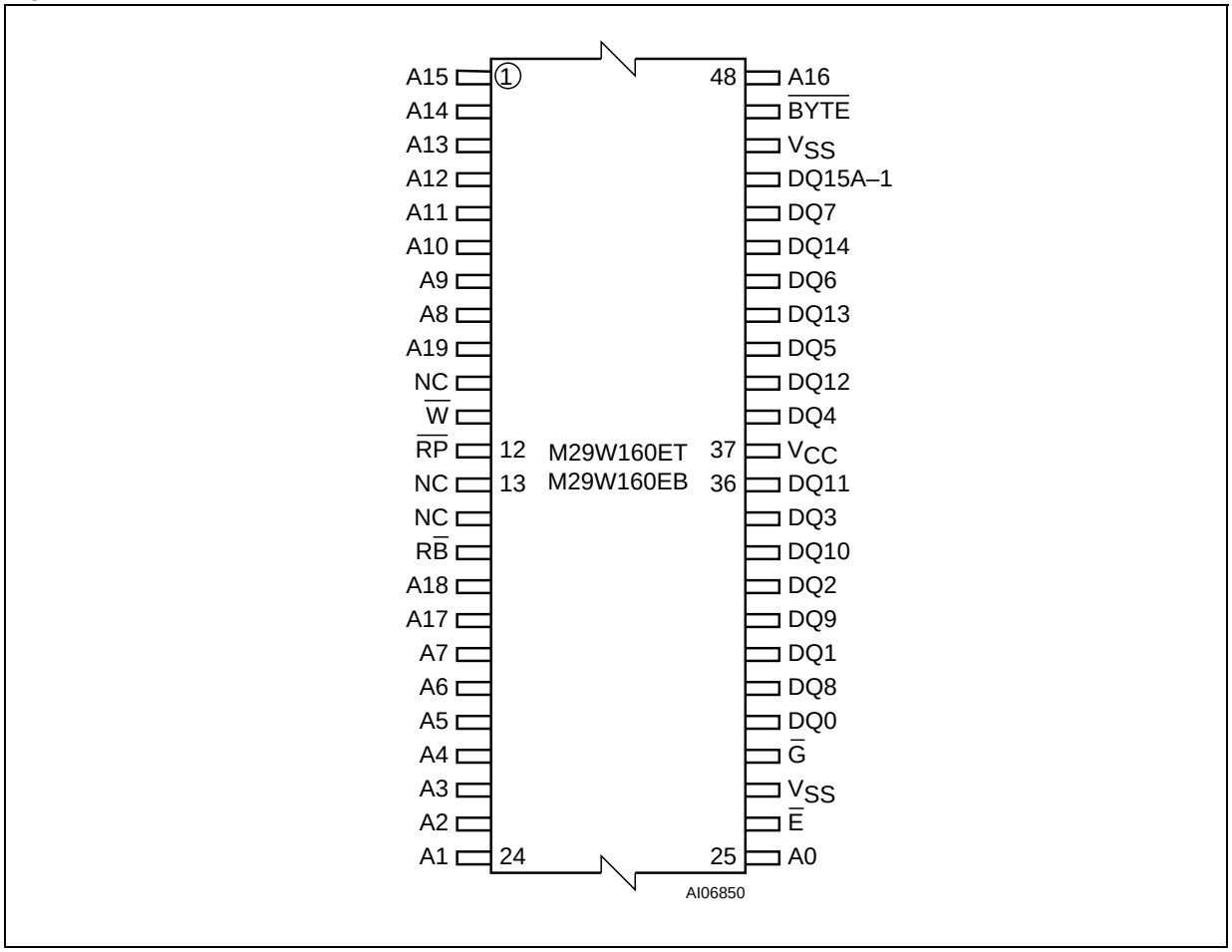


Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A–1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$R\overline{B}$	Ready/Busy Output
$\overline{BYTE}$	Byte/Word Organization Select
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

M29W160ET, M29W160EB

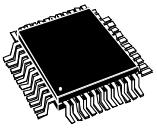
Figure 3. TSOP Connections



ST72F324L, ST72324BL

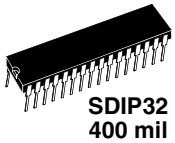
3V RANGE 8-BIT MCU WITH 8 TO 32K FLASH/ROM, 10-BIT ADC, 4 TIMERS, SPI, SCI INTERFACE

- **Memories**
  - 8 to 32K dual voltage High Density Flash (HDFlash) or ROM with read-out protection capability. In-Application Programming and In-Circuit Programming for HDFlash devices
  - 384 to 1K bytes RAM
  - HDFlash endurance: 100 cycles, data retention: 20 years at 55°C
- **Clock, Reset And Supply Management**
  - Clock sources: crystal/ceramic resonator oscillators, internal RC oscillator, and bypass for external clock
  - PLL for 2x frequency multiplication
  - Four Power Saving Modes: Halt, Active-Halt, Wait and Slow
- **Interrupt Management**
  - Nested interrupt controller
  - 10 interrupt vectors plus TRAP and RESET
  - 9/6 external interrupt lines (on 4 vectors)
- **Up to 32 I/O Ports**
  - 32/24 multifunctional bidirectional I/O lines
  - 22/17 alternate function lines
  - 12/10 high sink outputs
- **4 Timers**
  - Main Clock Controller with: Real time base, Beep and Clock-out capabilities
  - Configurable watchdog timer
  - 16-bit Timer A with: 1 input capture, 1 output compare, external clock input, PWM and pulse generator modes
  - 16-bit Timer B with: 2 input captures, 2 output compares, PWM and pulse generator modes



TQFP44
10 x 10

TQFP32
7 x 7



SDIP32
400 mil

- **2 Communication Interfaces**
  - SPI synchronous serial interface
  - SCI asynchronous serial interface
- **1 Analog Peripheral**
  - 10-bit ADC with up to 12 input ports
- **Instruction Set**
  - 8-bit Data Manipulation
  - 63 Basic Instructions
  - 17 main Addressing Modes
  - 8 x 8 Unsigned Multiply Instruction
- **Development Tools**
  - Full hardware/software development package
  - In-Circuit Testing capability

Device Summary

Features	ST72F324L(J/K)6	ST72F324L(J/K)4	ST72F324L(J/K)2	ST72324BL(J/K)4	ST72324BL(J/K)2
Program memory - bytes	Flash 32K	Flash 16K	Flash 8K	ROM 16K	ROM 8K
RAM (stack) - bytes	1024 (256)	512 (256)	384 (256)	512 (256)	384 (256)
Voltage Range	2.85 to 3.6V				
Temp. Range	up to -40°C to +85°C				
Packages	TQFP44 10x10, SDIP32, TQFP32 7x7				

Rev. 3

1 INTRODUCTION

The ST72F324L and ST72324BL devices are members of the ST7 microcontroller family designed for the 3V operating range. They can be grouped as follows:

– The 32-pin devices are designed for mid-range applications

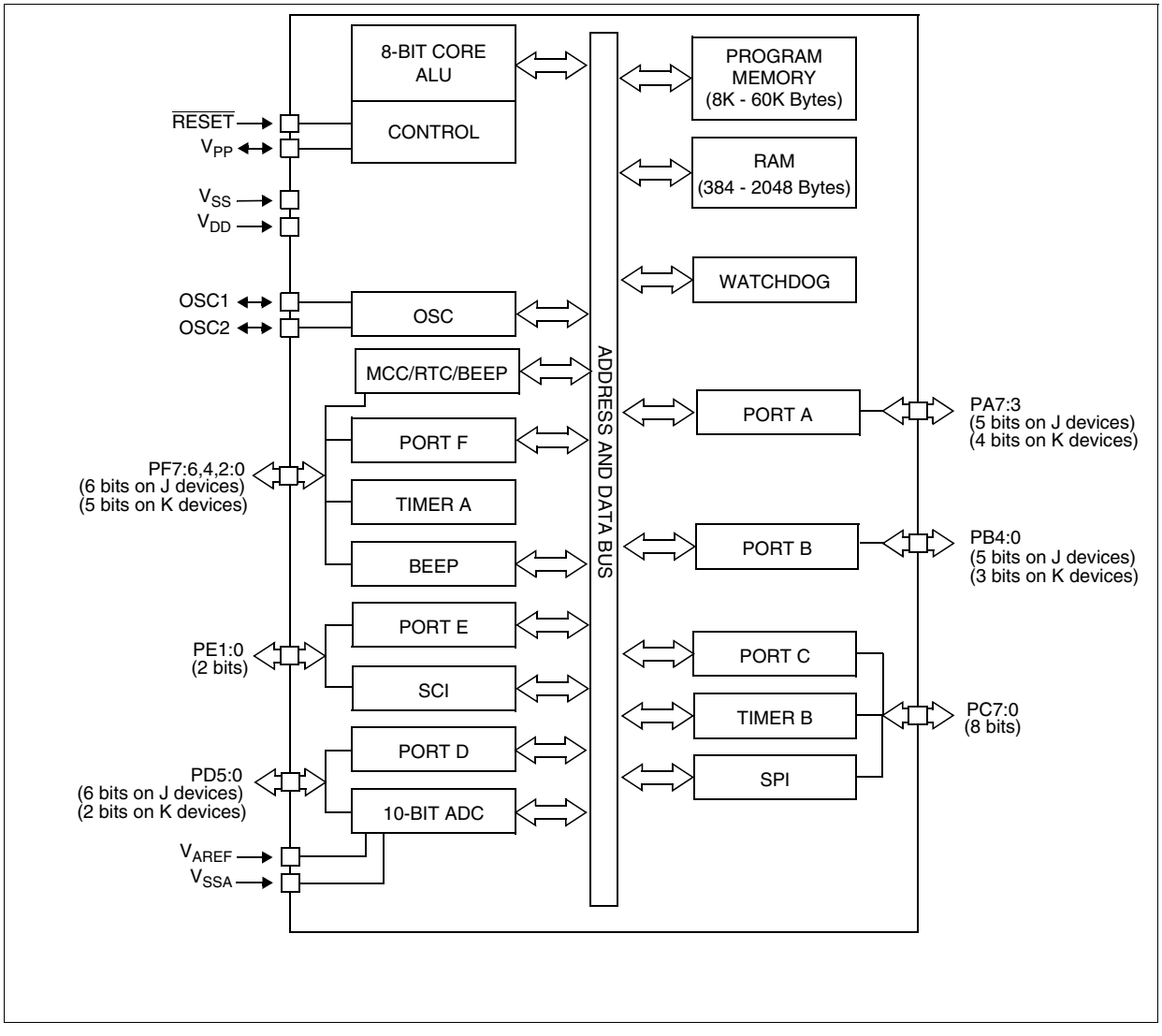
– The 44-pin devices target the same range of applications requiring more than 24 I/O ports.

All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with FLASH or ROM program memory.

Under software control, all devices can be placed in WAIT, SLOW, ACTIVE-HALT or HALT mode, reducing power consumption when the application is in idle or stand-by state.

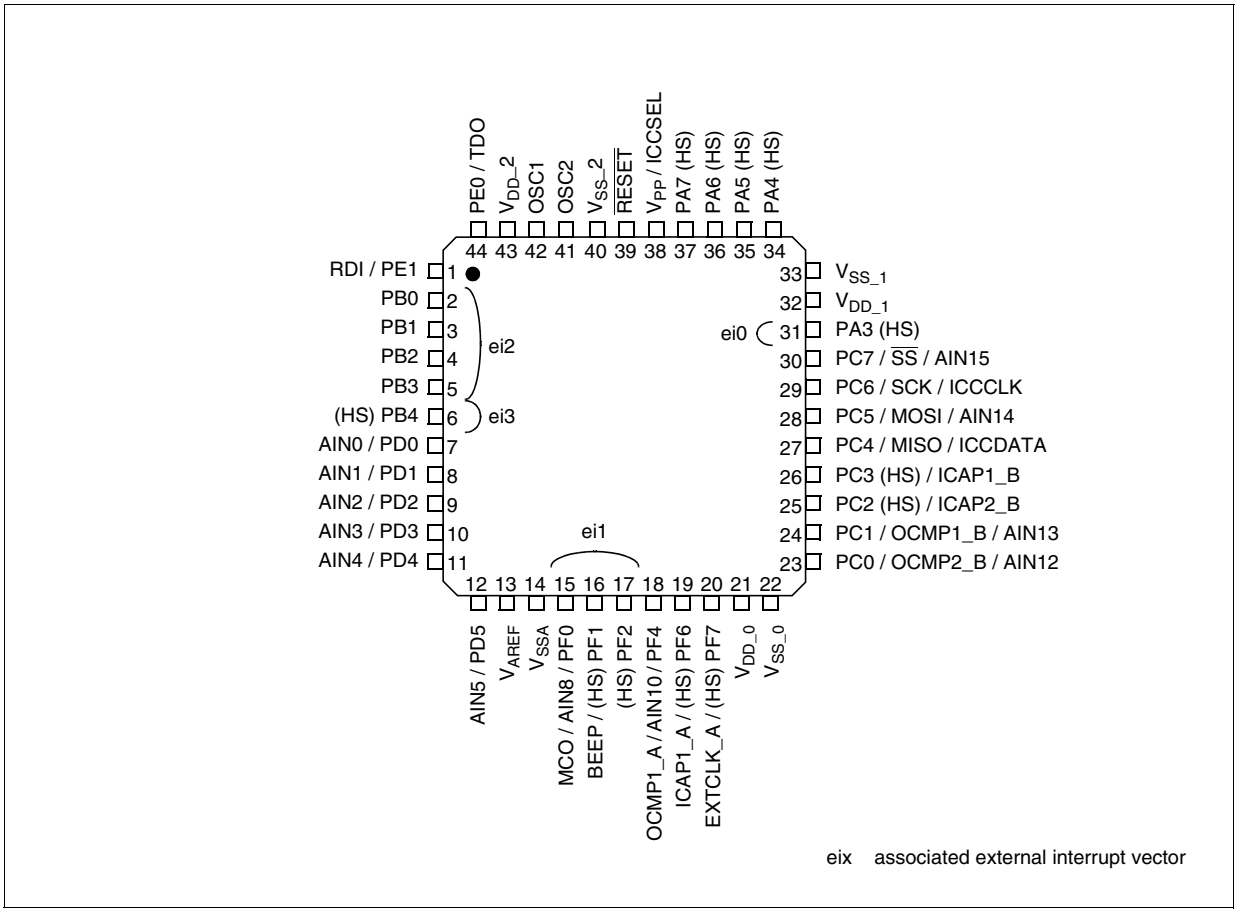
The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

Figure 1. Device Block Diagram



2 PIN DESCRIPTION

Figure 2. 44-Pin TQFP Package Pinouts



PIN DESCRIPTION (Cont'd)

Figure 3. 32-Pin SDIP Package Pinout

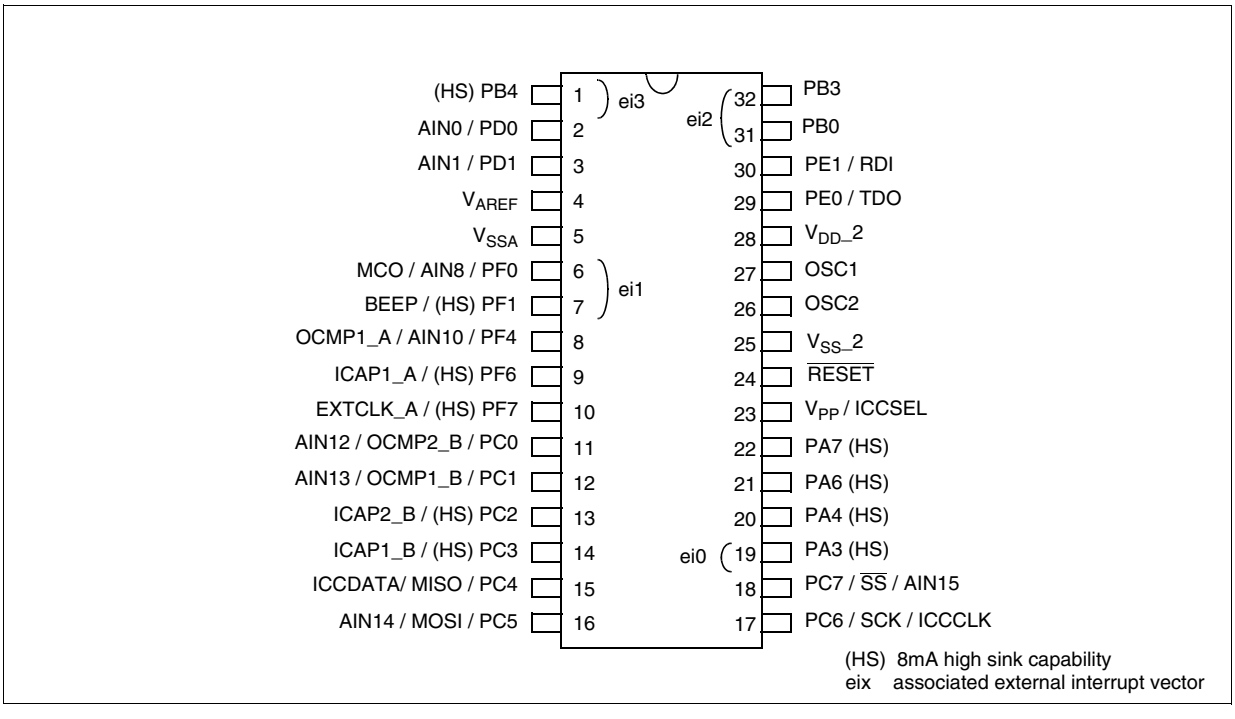
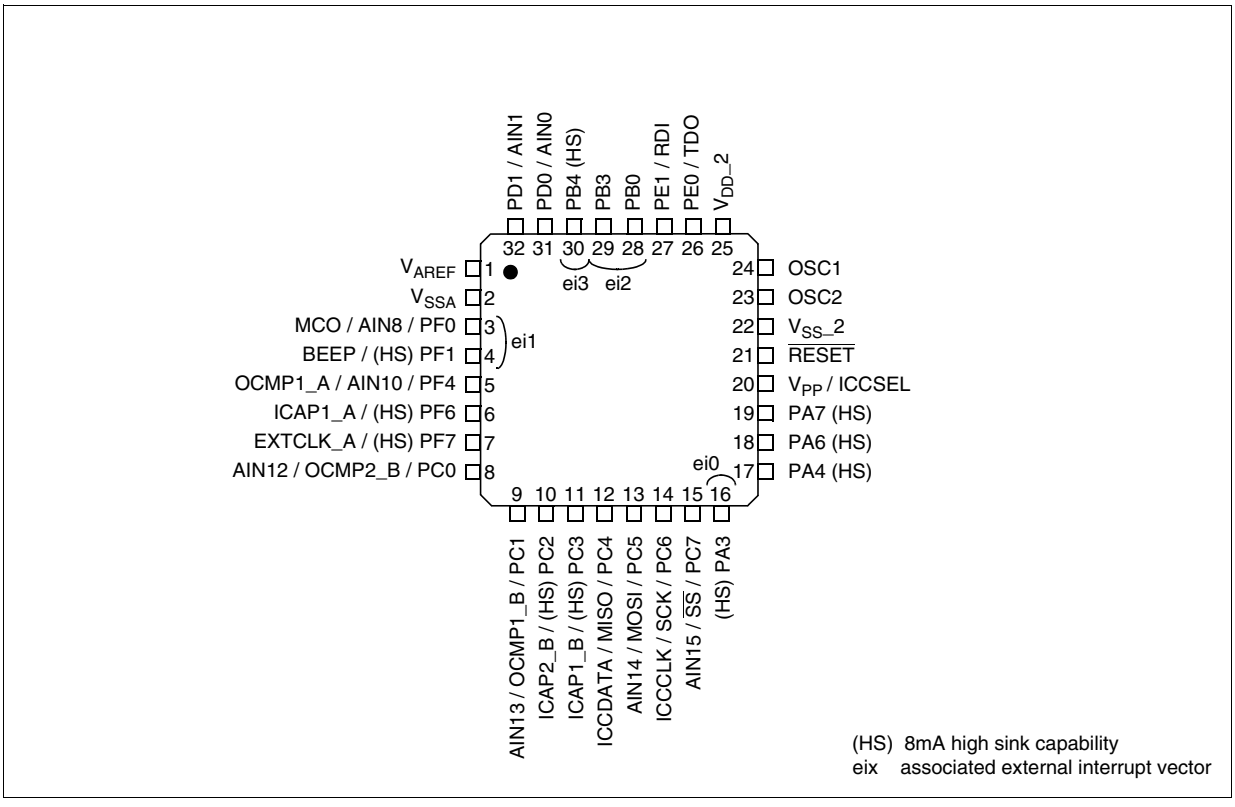


Figure 4. 32-Pin TQFP 7x7 Package Pinout



PIN DESCRIPTION (Cont'd)

For more details, refer to "ELECTRICAL CHARACTERISTICS" on page 110

Legend / Abbreviations for Table 1:

Type: I = input, O = output, S = supply

In/Output level: C = CMOS
C_T= CMOS with input trigger

Output level: HS = high sink (on N-buffer only)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up, int = interrupt [1], ana = analog ports
- Output: OD = open drain [2], PP = push-pull

Refer to "I/O PORTS" on page 39 for more details on the software configuration of the I/O ports.

The RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Table 1. Device Pin Description

Pin n°			Pin Name	Type	Level		Port						Main function (after reset)	Alternate Function	
							Input				Output				
TQFP44	TQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD	PP			
6	30	1	PB4 (HS)	I/O	C_T	HS	**X**	ei3			X	X	Port B4		
7	31	2	PD0/AIN0	I/O	C_T		**X**	X		X	X	X	Port D0	ADC Analog Input 0	
8	32	3	PD1/AIN1	I/O	C_T		**X**	X		X	X	X	Port D1	ADC Analog Input 1	
9			PD2/AIN2	I/O	C_T		**X**	X		X	X	X	Port D2	ADC Analog Input 2	
10			PD3/AIN3	I/O	C_T		**X**	X		X	X	X	Port D3	ADC Analog Input 3	
11			PD4/AIN4	I/O	C_T		**X**	X		X	X	X	Port D4	ADC Analog Input 4	
12			PD5/AIN5	I/O	C_T		**X**	X		X	X	X	Port D5	ADC Analog Input 5	
13	1	4	V_{AREF}	S									Analog Reference Voltage for ADC		
14	2	5	V_{SSA}	S									Analog Ground Voltage		
15	3	6	PF0/MCO/AIN8	I/O	C_T		**X**	ei1		X	X	X	Port F0	Main clock out (f_{OSC}/2)	ADC Analog Input 8
16	4	7	PF1 (HS)/BEEP	I/O	C_T	HS	**X**	ei1			X	X	Port F1	Beep signal output	
17			PF2 (HS)	I/O	C_T	HS	**X**		ei1		X	X	Port F2		
18	5	8	PF4/OCMP1_A/ AIN10	I/O	C_T		**X**	X		X	X	X	Port F4	Timer A Output Compare 1	ADC Analog Input 10
19	6	9	PF6 (HS)/ICAP1_A	I/O	C_T	HS	**X**	X			X	X	Port F6	Timer A Input Capture 1	
20	7	10	PF7 (HS)/ EXTCLK_A	I/O	C_T	HS	**X**	X			X	X	Port F7	Timer A External Clock Source	
21			V_{DD_0}	S									Digital Main Supply Voltage		
22			V_{SS_0}	S									Digital Ground Voltage		
23	8	11	PC0/OCMP2_B/ AIN12	I/O	C_T		**X**	X		X	X	X	Port C0	Timer B Output Compare 2	ADC Analog Input 12
24	9	12	PC1/OCMP1_B/ AIN13	I/O	C_T		**X**	X		X	X	X	Port C1	Timer B Output Compare 1	ADC Analog Input 13

ST72F324L, ST72324BL

Pin n°			Pin Name	Type	Level		Port						Main function (after reset)	Alternate Function	
							Input				Output				
TQFP44	TQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD	PP			
25	10	13	PC2 (HS)/ICAP2_B	I/O	C_T	HS	**X**	X			X	X	Port C2	Timer B Input Capture 2	
26	11	14	PC3 (HS)/ICAP1_B	I/O	C_T	HS	**X**	X			X	X	Port C3	Timer B Input Capture 1	
27	12	15	PC4/MISO/ICCDATA	I/O	C_T		**X**	X			X	X	Port C4	SPI Master In / Slave Out Data	ICC Data Input
28	13	16	PC5/MOSI/AIN14	I/O	C_T		**X**	X		X	X	X	Port C5	SPI Master Out / Slave In Data	ADC Analog Input 14
29	14	17	PC6/SCK/ICCCLK	I/O	C_T		**X**	X			X	X	Port C6	SPI Serial Clock	ICC Clock Output
30	15	18	PC7/$\overline{SS}$/AIN15	I/O	C_T		**X**	X		X	X	X	Port C7	SPI Slave Select (active low)	ADC Analog Input 15
31	16	19	PA3 (HS)	I/O	C_T	HS	**X**		ei0		X	X	Port A3		
32			V_{DD_1}	S									Digital Main Supply Voltage		
33			V_{SS_1}	S									Digital Ground Voltage		
34	17	20	PA4 (HS)	I/O	C_T	HS	**X**	X			X	X	Port A4		
35			PA5 (HS)	I/O	C_T	HS	**X**	X			X	X	Port A5		
36	18	21	PA6 (HS)	I/O	C_T	HS	**X**				T		Port A6 [1)]		
37	19	22	PA7 (HS)	I/O	C_T	HS	**X**				T		Port A7 [1)]		
38	20	23	V_{PP} /ICCSEL	I									Must be tied low. In the flash programming mode, this pin acts as the programming voltage input V_{PP}. See Section 12.9.2 for more details. High voltage must not be applied to ROM devices.		
39	21	24	$\overline{RESET}$	I/O	C_T								Top priority non maskable interrupt.		
40	22	25	V_{SS_2}	S									Digital Ground Voltage		
41	23	26	OSC2	O									Resonator oscillator inverter output		
42	24	27	OSC1	I									External clock input or Resonator oscillator inverter input		
43	25	28	V_{DD_2}	S									Digital Main Supply Voltage		
44	26	29	PE0/TDO	I/O	C_T		**X**	X			X	X	Port E0	SCI Transmit Data Out	
1	27	30	PE1/RDI	I/O	C_T		**X**	X			X	X	Port E1	SCI Receive Data In	
2	28	31	PB0	I/O	C_T		**X**	ei2			X	X	Port B0		
3			PB1	I/O	C_T		**X**	ei2			X	X	Port B1		
4			PB2	I/O	C_T		**X**	ei2			X	X	Port B2		
5	29	32	PB3	I/O	C_T		**X**		ei2		X	X	Port B3		

Notes:

1. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input.

2. In the open drain output column, “T” defines a true open drain I/O (P-Buffer and protection diode to V_{DD}

are not implemented). See See “I/O PORTS” on page 39. and Section 12.8 I/O PORT PIN CHARACTERISTICS for more details.

3. OSC1 and OSC2 pins connect a crystal/ceramic resonator, or an external source to the on-chip oscillator; see Section 1 INTRODUCTION and Section 12.5 CLOCK AND TIMING CHARACTERISTICS for more details.

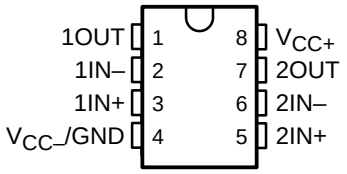
4. On the chip, each I/O port has 8 pads. Pads that are not bonded to external pins are in input pull-up configuration after reset. The configuration of these pads must be kept at reset state to avoid added current consumption.

TL3472
HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

- **Wide Gain-Bandwidth Product . . . 4 MHz**
- **High Slew Rate . . . 13 V/μs**
- **Fast Settling Time . . . 1.1 μs to 0.1%**
- **Wide-Range Single-Supply Operation . . . 4 V to 36 V**
- **Wide Input Common-Mode Range Includes Ground ($V_{CC–}$)**
- **Low Total Harmonic Distortion . . . 0.02%**
- **Large-Capacitance Drive Capability . . . 10,000 pF**
- **Output Short-Circuit Protection**

D OR P PACKAGE
(TOP VIEW)



description/ordering information

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, 13-V/μs slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential ($V_{CC–}$). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 25	TL3472CP	TL3472CP
	SOIC (D)	Tube of 50	TL3472CD	3472C
		Reel of 2500	TL3472CDR	
–40°C to 105°C	PDIP (P)	Tube of 25	TL3472IP	TL3472IP
	SOIC (D)	Tube of 50	TL3472ID	Z3472
		Reel of 2500	TL3472IDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type HN1K05FU

TOSHIBA HN1K05FU

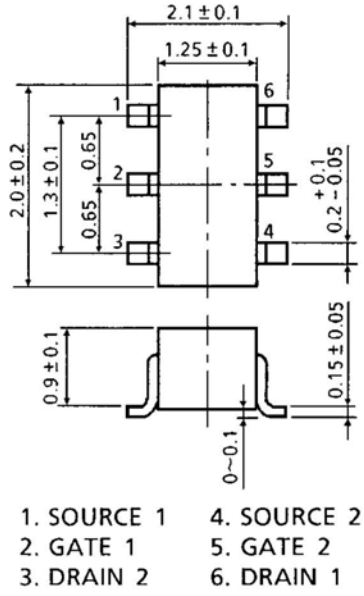
Unit: mm

For Portable Devices

High Speed Switching Applications

Interface Applications

- High input impedance and extremely low drive current.
- V_{th} is low and it is possible to drive directly at low-voltage CMOS.
  : V_{th} = 0.5 to 1.0 V
- Suitable for high-density mounting because of a compact package.



US6

JEDEC	—
JEITA	—
TOSHIBA	2-2J1C

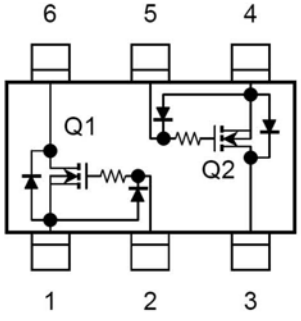
Weight: 6.8 mg

Maximum Ratings (Ta = 25°C) (Q1, Q2 common)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GSS}	10	V
DC drain current	I_D	100	mA
Drain power dissipation	P_D (Note)	200	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C

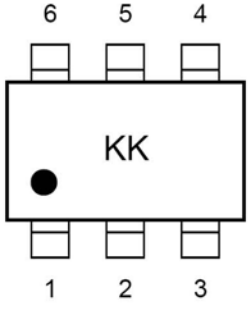
Note: TOTAL rating

Equivalent Circuit (top view)



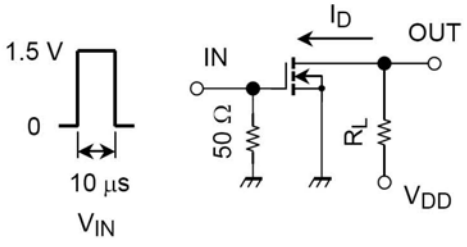
(Q1, Q2 common)

Marking



Switching Time Test Circuit

(a) Test circuit



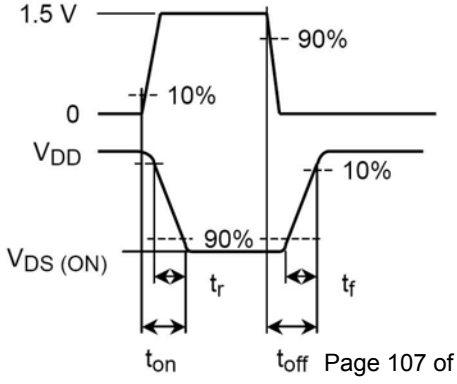
V_{DD} = 1.5 V
D.U. ≦ 1%
V_{IN}: t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
Common Source
Ta = 25°C

(b) V_{IN}

V_{GS}

(c) V_{OUT}

V_{DS}



Low Cost Green-Mode PWM Controller for Flyback Converters **SG6848**

FEATURES

- Green-Mode PWM
- Supports the “Blue Angel” Standard
- Low Start-up Current (5uA)
- Low Operating Current (2mA)
- Leading-Edge Blanking
- Constant Output Power Limit
- Universal Input
- Built-in Synchronized Slope Compensation
- Current Mode Operation
- Cycle-by-cycle Current Limiting
- Under Voltage Lockout (UVLO)
- Programmable PWM Frequency
- Gate Output Voltage Clamped at 15V
- Low Cost
- Few External Components Required
- Small SOT-26 Package

APPLICATIONS

General-purpose switching mode power supplies and flyback power converters, such as

- Battery chargers for cellular phones, cordless phones, PDAs, digital cameras, and power tools
- Power adapters for ink jet printers, video game consoles, and portable audio players
- Open-frame SMPS for TV/DVD standby and other auxiliary supplies, home appliances, and consumer electronics
- Replacements for linear transformers and RCC SMPS
- PC 5V standby power.

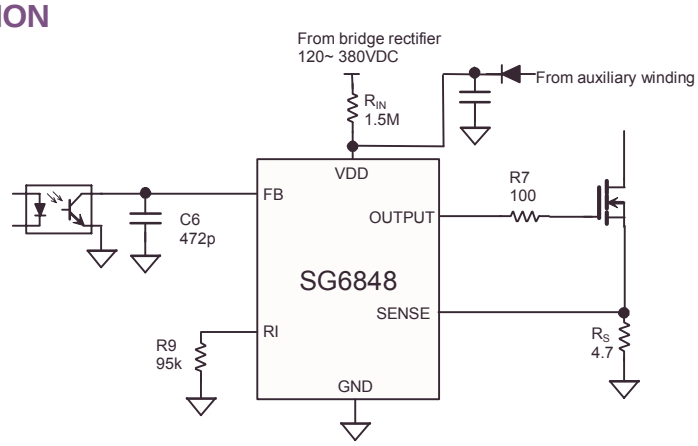
DESCRIPTION

This highly-integrated PWM controller provides several special enhancements designed to meet the low standby-power needs of low-power SMPS. To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. This green-mode function enables the power supply to easily meet even the strictest power conservation requirements.

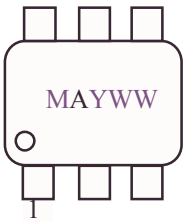
The BiCMOS fabrication process enables reducing the start-up current to 5uA, and the operating current to 2mA. To further improve power conservation, a large start-up resistance can be used. Built-in synchronized slope compensation ensures the stability of peak current mode control. Proprietary internal compensation provides a constant output power limit over a universal AC input range (90VAC to 264VAC). Pulse-by-pulse current limiting ensures safe operation even during short-circuits.

To protect the external power MOSFET from being damaged by supply over voltage, the SG6848’s output driver is clamped at 15V. SG6848 controllers can be used to improve the performance and reduce the production cost of power supplies. The SG6848 is the best choice for replacing linear and RCC-mode power adapters. It is available in 8-pin DIP and 6-pin SOT-26 packages.

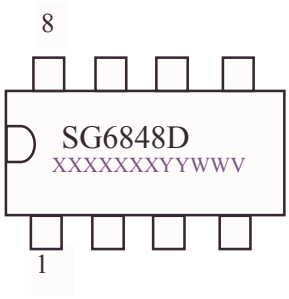
TYPICAL APPLICATION



MARKING DIAGRAMS

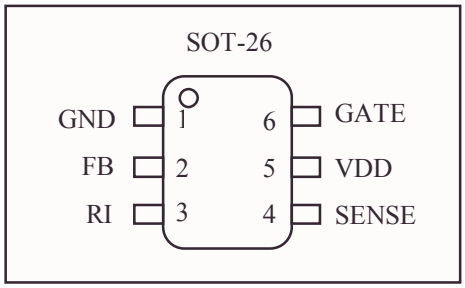


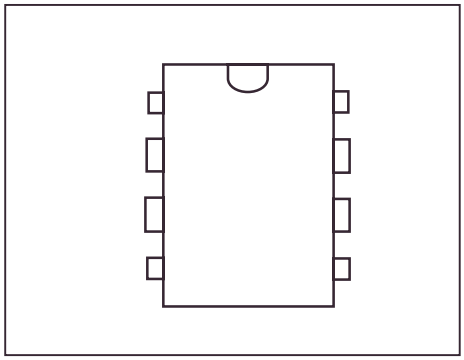
M: Mask Version
Y: Year; WW: Work Week



XXXXXXX: Wafer Lot
YY: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION





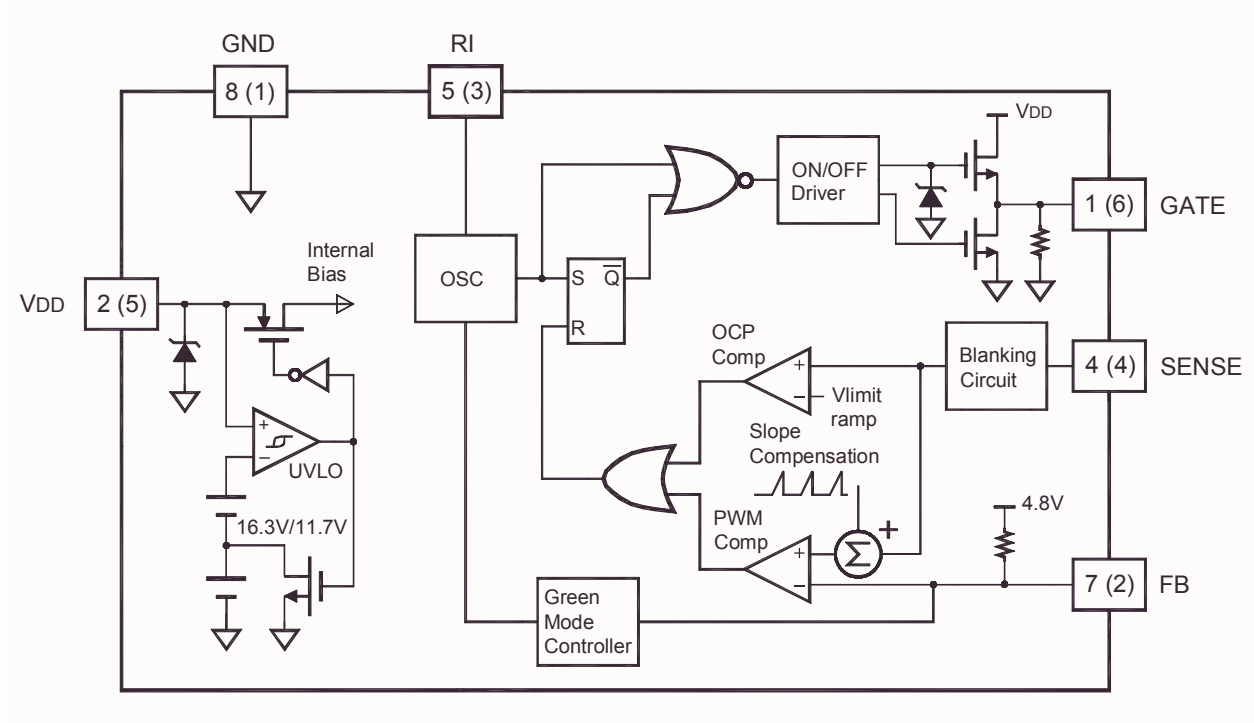
ORDERING INFORMATION

Part Number	PWM Frequency	Package
SG6848T	70kHz	6-Pin SOT-26
SG6848D	70kHz	8-pin DIP-8

PIN DESCRIPTIONS

Name	Pin No. DIP-8 / (SOT-26)	Type	Function
GATE	1 / (6)	Driver Output	The totem-pole output driver for driving the power MOSFET.
VDD	2 / (5)	Supply	Power supply.
NC	3		NC pin.
SENSE	4 / (4)	Analog Input	Current sense. This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled. This activates over-current protection. This pin also provides current amplitude information for current-mode control.
RI	5 / (3)	Analog Input/Output	A resistor connected from the RI pin to ground will generate a constant current source for the SG6848. This current is used to charge an internal capacitor, to determine the switching frequency. Increasing the resistance will reduce the amplitude of the current source and reduce the switching frequency. A 95kΩ resistor R_i results in a 50uA constant current I_i and a 70kHz switching frequency.
NC	6		NC pin.
FB	7 / (2)	Analog Input	Feedback. The FB pin provides the output voltage regulation signal. It provides feedback to the internal PWM comparator, so that the PWM comparator can control the duty cycle.
GND	8 / (1)	Supply	Ground.

BLOCK DIAGRAM



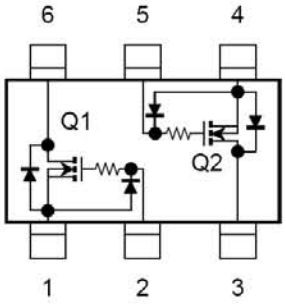
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Value	Unit
V_{DD}	DC Supply Voltage *			25	V
	Zener Clamp			26	V
	Zener Current			10	mA
V_{FB}	Input Voltage to FB Pin			-0.3 to 6 V	V
V_{Sense}	Input Voltage to Sense Pin			-0.3 to 6V	V
P_d	Power Dissipation			300	mW
T_J	Operating Junction Temperature			150	℃
$R_{\theta JA}$	Thermal Resistance (Junction to Air)	SOT-26		208.4	°C/W
		DIP-8		82.5	°C/W
T_{stg}	Storage Temperature Range			-55 to +150	℃
T_L	Lead Temperature (Soldering)	20 sec	SOT-26	220	°C
		10 sec	DIP-8	260	
	ESD Capability, HBM Model			3.0	kV
	ESD Capability, Model			300	V

* All voltage values, except differential voltages, are given with respect to the network ground terminal.

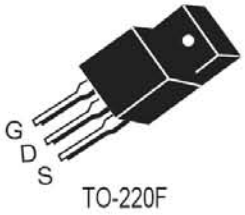
Semiconductors

HN1K05FU N Channel



1. Source 1
2, Gate 1
3. Drain 2
4. Source 2
5. Gate 2
6. Drain 1

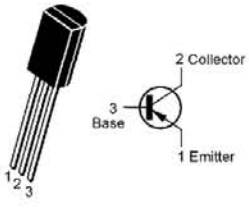
CEF04N6 N Channel



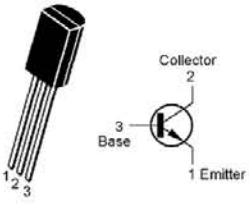
(SCR) MCR100

PIN ASSIGNMENT	
1	Cathode
2	Gate
3	Anode

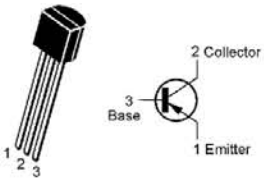
KTA1273Y
KSA916Y



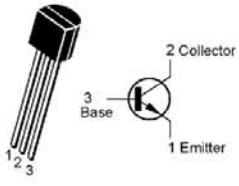
KTC3206



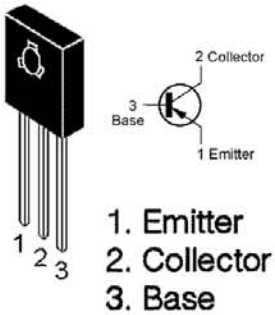
KRA102M
KTA708



KRC102M
KTC1008
KTC3198Y

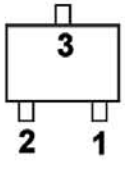


KSB1151Y PNP



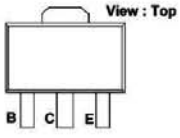
1. Emitter
2. Collector
3. Base

KRC107 PNP
KTC3875S NPN
KTA1504S PNP
KRA107S PNP
KTD1304 NPN
2N3904S NPN
KRC 107S NPN
2SA1955 PNP



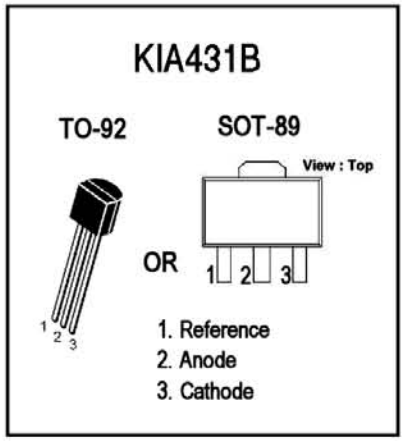
1) Emitter
2) Base
3) Collector

KTA1664 PNP



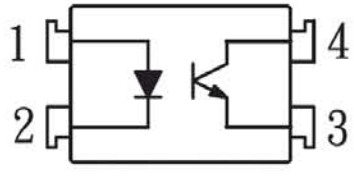
1 Base
2 Collector
3 Emitter

KIA431B



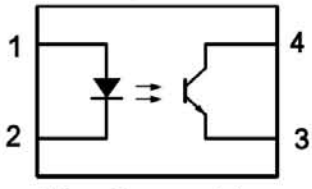
1. Reference
2. Anode
3. Cathode

Photo Coupler K1010



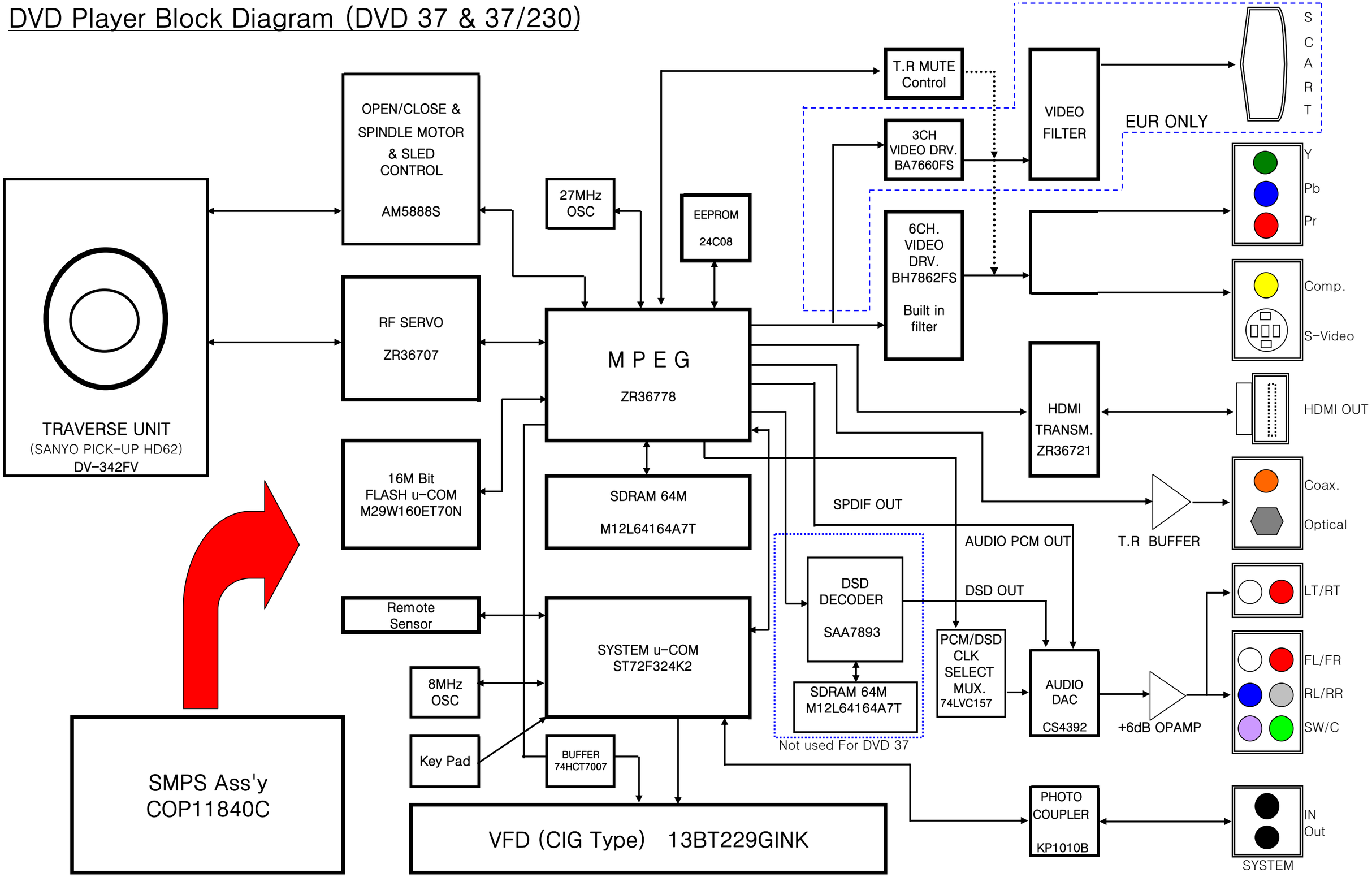
1. Anode
2. Cathode
3. Emitter
4. Collector

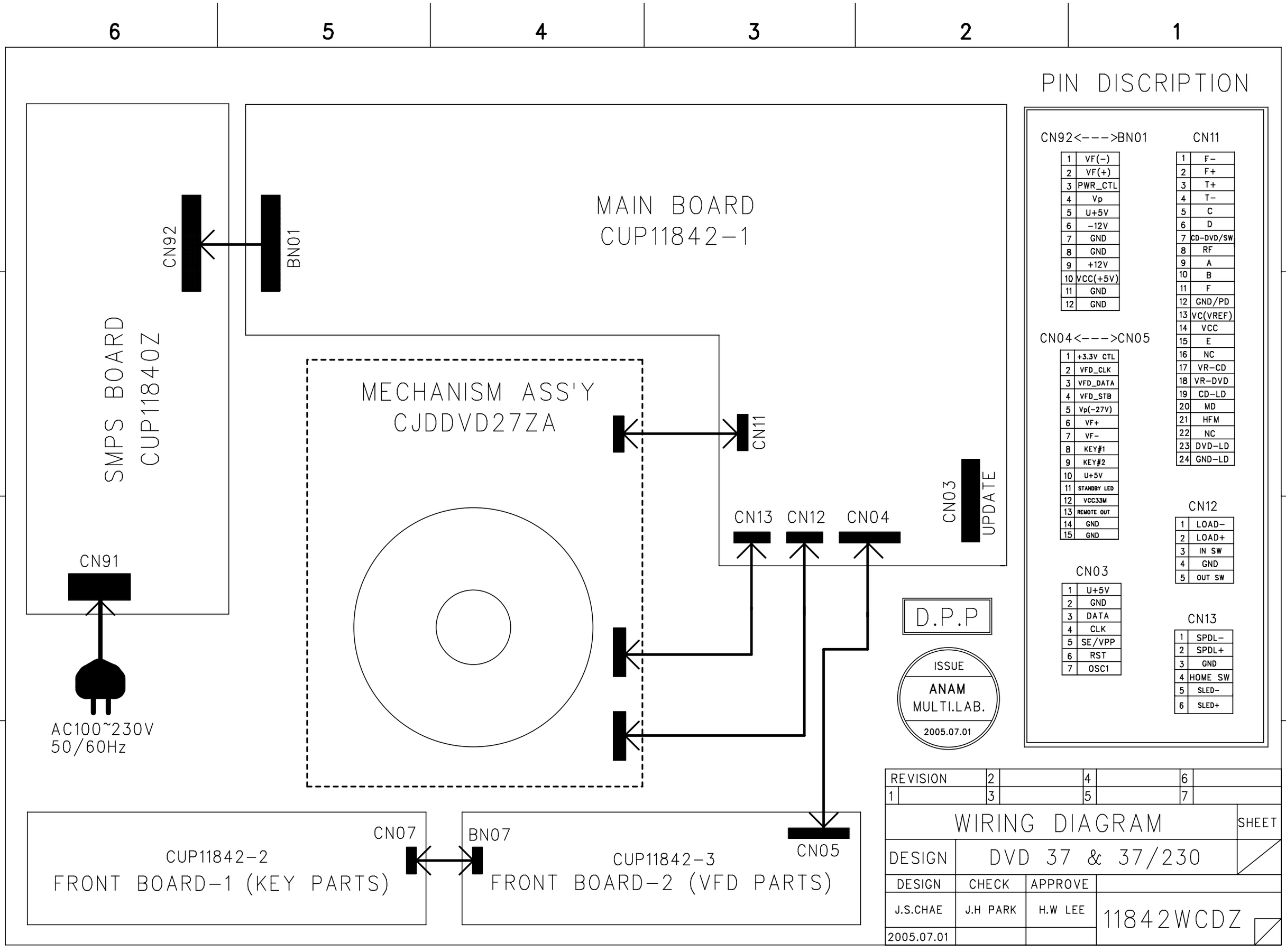
PC17L

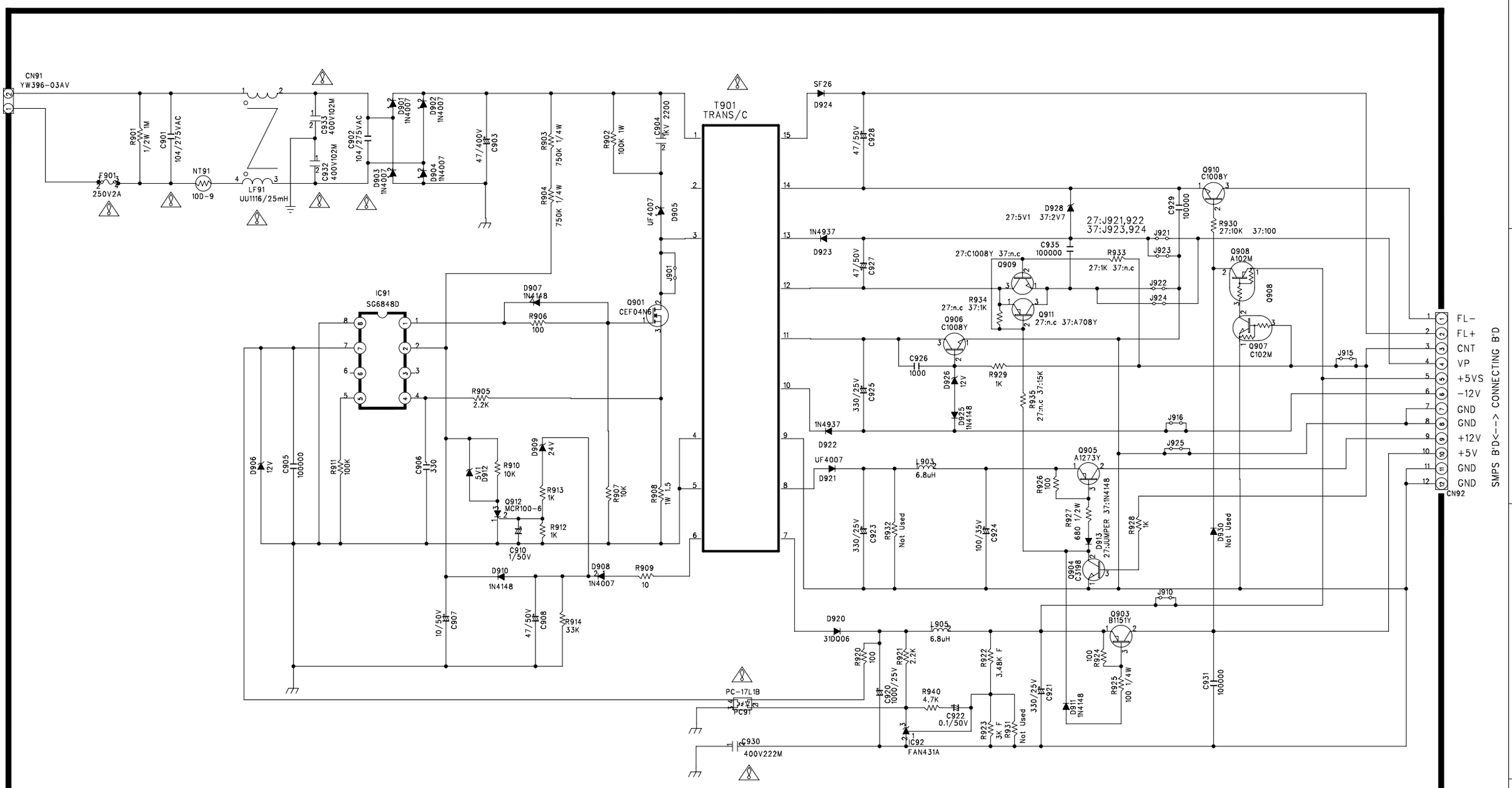


Pin Connections
1. Anode
2. Cathode
3. Emitter
4. Collector

DVD Player Block Diagram (DVD 37 & 37/230)




6
5
4
3
2
1
D
C
B
A
SMPS BOARD
CUP11840Z
CN92
BN01
MAIN BOARD
CUP11842-1
MECHANISM ASS'Y
CJDDVD27ZA
CN11
CN03
UPDATE
CN13
CN12
CN04
CN91
AC100~230V
50/60Hz
D.P.P
ISSUE
ANAM
MULTI.LAB.
2005.07.01
CN07
BN07
CN05
CUP11842-2
FRONT BOARD-1 (KEY PARTS)
CUP11842-3
FRONT BOARD-2 (VFD PARTS)
PIN DISCRIPTION
CN92<--->BN01
1 VF(-)
2 VF(+)
3 PWR_CTL
4 Vp
5 U+5V
6 -12V
7 GND
8 GND
9 +12V
10 VCC(+5V)
11 GND
12 GND
CN11
1 F-
2 F+
3 T+
4 T-
5 C
6 D
7 CD-DVD/SW
8 RF
9 A
10 B
11 F
12 GND/PD
13 VC(VREF)
14 VCC
15 E
16 NC
17 VR-CD
18 VR-DVD
19 CD-LD
20 MD
21 HFM
22 NC
23 DVD-LD
24 GND-LD
CN04<--->CN05
1 +3.3V CTL
2 VFD_CLK
3 VFD_DATA
4 VFD_STB
5 Vp(-27V)
6 VF+
7 VF-
8 KEY#1
9 KEY#2
10 U+5V
11 STANDBY LED
12 VCC33M
13 REMOTE OUT
14 GND
15 GND
CN12
1 LOAD-
2 LOAD+
3 IN SW
4 GND
5 OUT SW
CN03
1 U+5V
2 GND
3 DATA
4 CLK
5 SE/VPP
6 RST
7 OSC1
CN13
1 SPDL-
2 SPDL+
3 GND
4 HOME SW
5 SLED-
6 SLED+
REVISION
1 2 3 4 5 6 7
WIRING DIAGRAM
SHEET
DESIGN
DVD 37 & 37/230
DESIGN CHECK APPROVE
J.S.CHAE J.H PARK H.W LEE
2005.07.01
11842WCDZ



**IMPORTANT SAFETY NOTICE.
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS.
IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS.
USE ONLY MANUFACTUREY'S SPECIFIED PARTS.

**THE UNIT OF RESISTANCE IS OHM.
K=1000 OHM, M=1000 KOHM

**THE UNIT OF CAPACITANCE IS MICROFARAD (uF)
1pF = 10^{-6} uF

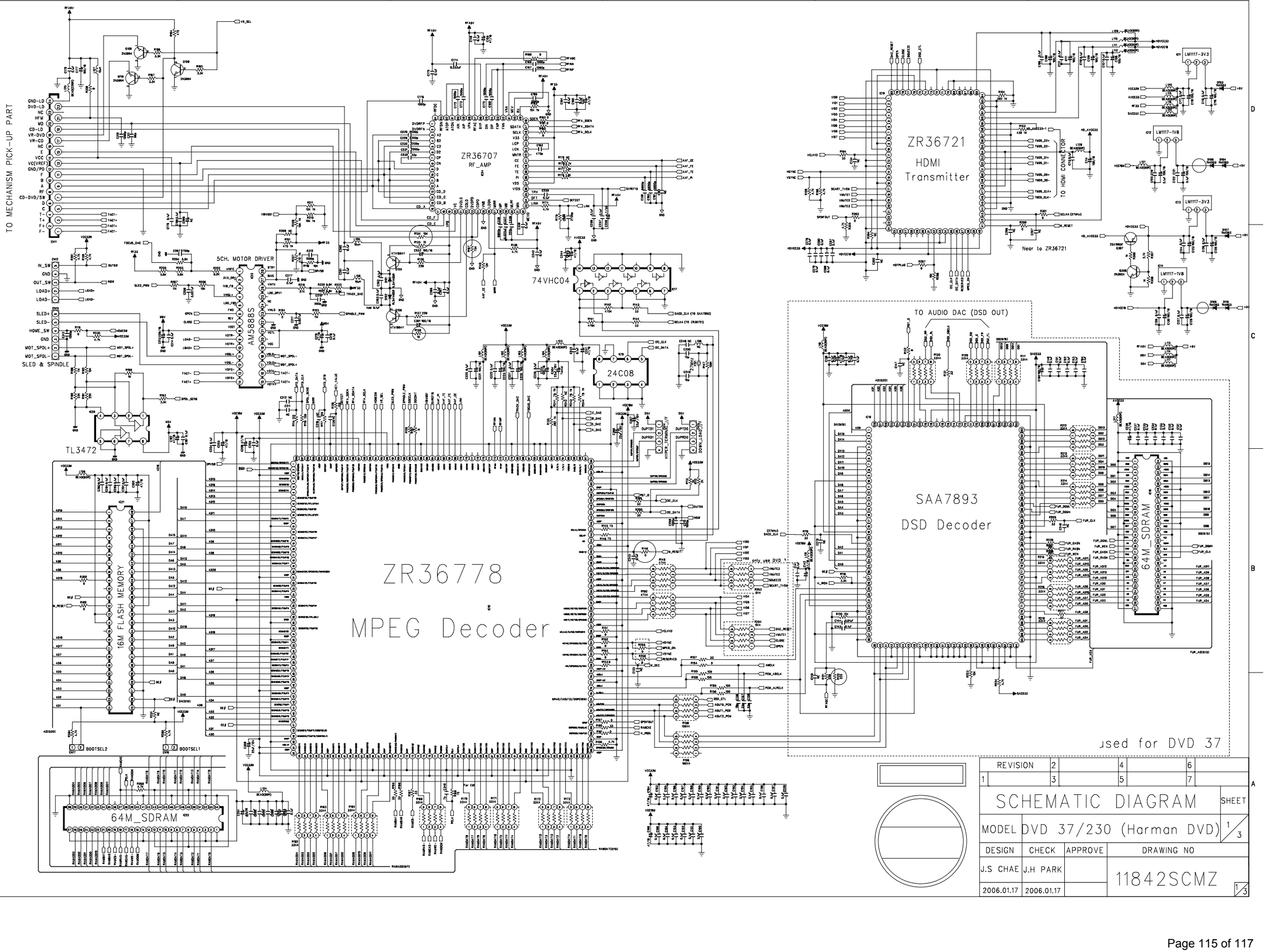
**THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANYTIME
WITH THE IMPROVEMENT OF PERFORMANCE

M.P

REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET

MODEL	DVD 27/37/47		
DESIGN	CHECK	APPROVE	DRAWING NO
S.M.KIM	J.H.PARK		11840SCMZ
06.01.17	06.01.17		(SMPS) 1/1

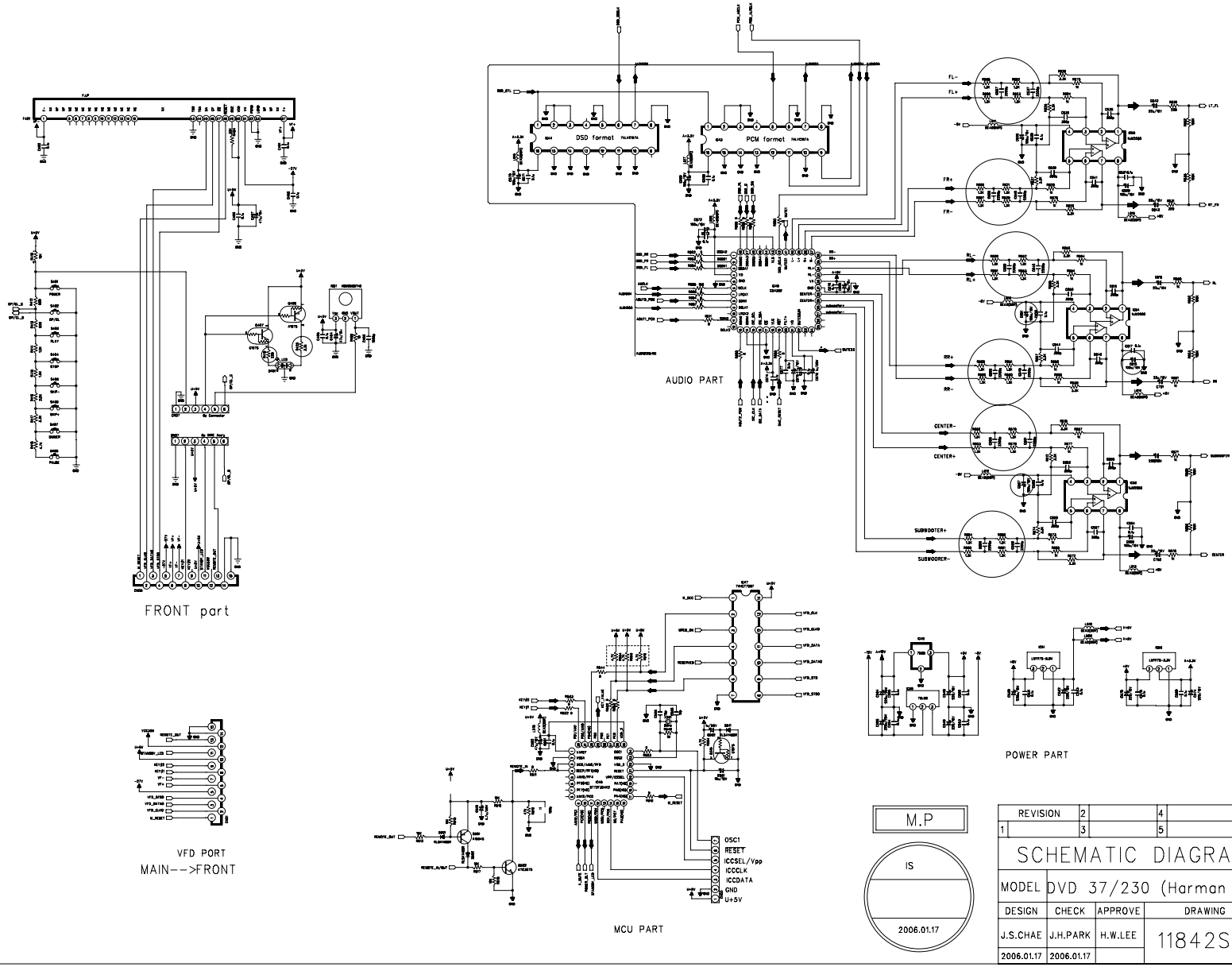


REVISION	2	4	6
1	3	5	7

SCHEMATIC DIAGRAM — SHEET

MODEL: DVD 37/230 (Harman DVD) — 1/3

DESIGN	CHECK	APPROVE	DRAWING NO
J.S CHAE	J.H PARK		11842SCMZ 1/3
2006.01.17	2006.01.17		


FRONT part
AUDIO PART
DSD format
PCM format
FL-
FL+
FR+
FR-
CENTER-
CENTER+
SUBWOOFER+
SUBWOOFER-
POWER PART
VFD PORT
MAIN-->FRONT
MCU PART
OSC1
RESET
ICCSEL/Vpp
ICCCLK
ICCDATA
GND
U+5V
M.P
IS
2006.01.17
REVISION
SCHEMATIC DIAGRAM
SHEET
MODEL
DVD 37/230 (Harman DVD)
2/3
DESIGN
CHECK
APPROVE
DRAWING NO
J.S.CHAE
J.H.PARK
H.W.LEE
11842SCMZ
2006.01.17
2006.01.17

SPDIF OUT

HDMI OUT

FOR DVD 47

POWER PORT

REMOTE_IN/OUT

AUDIO OUT

VIDEO OUT

FOR PAL version

M.P		REVISION	2	4	6
		1	3	5	7
ISSUE		SCHEMATIC DIAGRAM			SHEET
2'		MODEL	DVD 37/230 (Harman DVD)		3/3
		DESIGN	CHECK	APPROVE	DRAWING NO
		J.S.CHAE	J.H.PARK	H.W.LEE	11842SCMZ
		2006.01.17	2006.01.17		3/3