harman kardon

Model DVD 48

DVD/CD/CD-R/CD-RW/VCD MP3 Player

Service Manual

- Contents -

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Woodbury, New York 11797

Rev0 8/2007

Released 2007
Discontinued XXXX

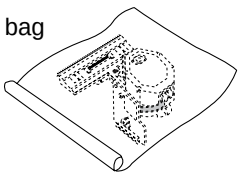
SERVICING PRECAUTIONS

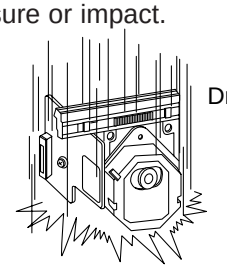
NOTES REGARDING HANDLING OF THE PICK-UP

1. Notes for transport and storage

1) The pick-up should always be left in its conductive bag until immediately prior to use.
2) The pick-up should never be subjected to external pressure or impact.

Storage in conductive bag

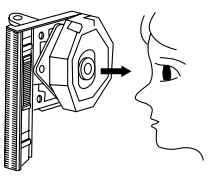




Drop impact

2. Repair notes

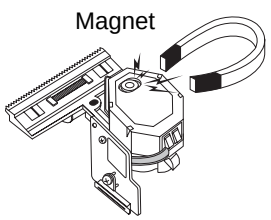
1) The pick-up incorporates a strong magnet, and so should never be brought close to magnetic materials.
2) The pick-up should always be handled correctly and carefully, taking care to avoid external pressure and impact. If it is subjected to strong pressure or impact, the result may be an operational malfunction and/or damage to the printed-circuit board.
3) Each and every pick-up is already individually adjusted to a high degree of precision, and for that reason the adjustment point and installation
screws should absolutely never be touched.
4) Laser beams may damage the eyes!
Absolutely never permit laser beams to enter the eyes!
Also NEVER switch ON the power to the laser output part (lens, etc.) of the pick-up if it is damaged.

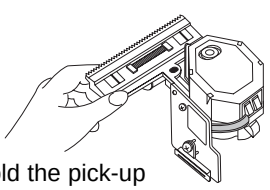


NEVER look directly at the laser beam, and don't let contact fingers or other exposed skin.

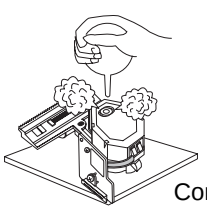
5) Cleaning the lens surface
If there is dust on the lens surface, the dust should be cleaned away by using an air bush (such as used for camera lens). The lens is held by a delicate spring. When cleaning the lens surface, therefore, a cotton swab should be used, taking care not to distort this.

Magnet



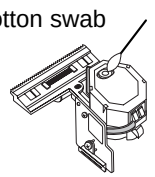


How to hold the pick-up



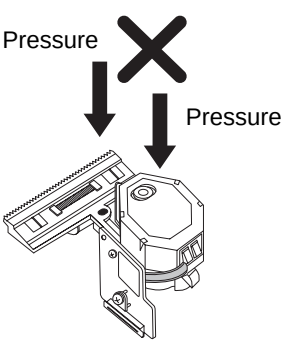
Conductive Sheet

Cotton swab



Pressure

Pressure



6) Never attempt to disassemble the pick-up.
Spring by excess pressure. If the lens is extremely dirty, apply isopropyl alcohol to the cotton swab. (Do not use any other liquid cleaners, because they will damage the lens.) Take care not to use too much of this alcohol on the swab, and do not allow the alcohol to get inside the pick-up.

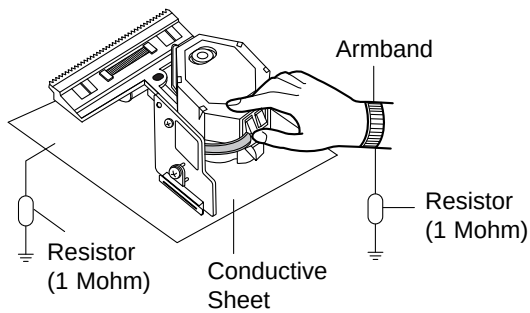
NOTES REGARDING COMPACT DISC PLAYER REPAIRS

1. Preparations

1) Compact disc players incorporate a great many ICs as well as the pick-up (laser diode). These components are sensitive to, and easily affected by, static electricity. If such static electricity is high voltage, components can be damaged, and for that reason components should be handled with care.
2) The pick-up is composed of many optical components and other high-precision components. Care must be taken, therefore, to avoid repair or storage where the temperature of humidity is high, where strong magnetism is present, or where there is excessive dust.

2. Notes for repair

1) Before replacing a component part, first disconnect the power supply lead wire from the unit
2) All equipment, measuring instruments and tools must be grounded.
3) The workbench should be covered with a conductive sheet and grounded.
   When removing the laser pick-up from its conductive bag, do not place the pick-up on the bag. (This is because there is the possibility of damage by static electricity.)
4) To prevent AC leakage, the metal part of the soldering iron should be grounded.
5) Workers should be grounded by an armband (1MΩ)
6) Care should be taken not to permit the laser pick-up to come in contact with clothing, in order to prevent static electricity changes in the clothing to escape from the armband.
7) The laser beam from the pick-up should NEVER be directly facing the eyes or bare skin.



ESD PRECAUTIONS

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded-tip soldering iron to solder or unsolder ESD devices.
4. Use only an anti-static solder removal device. Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ESD devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
6. Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).
7. Immediately before removing the protective material from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will by installed.

CAUTION : BE SURE NO POWER IS APPLIED TO THE CHASSIS OR CIRCUIT, AND OBSERVE ALL OTHER SAFETY PRECAUTIONS.

8. Minimize bodily motions when handing unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

DVD 48 TECHNICAL SPECIFICATIONS

Applicable Disc:	
Disc formats:	5-inch (12cm) or 3-inch (8cm) DVD-Video, DVD-Audio, SACD,™ standard-conforming DVD-R, DVD+R, DVD-RW, DVD+RW, VCD, CD, CD-R, CD-RW or MP3 discs
Region code:	DVD video disc with Code 1 or 0 only
DVD layers:	Single side/single layer, single side/dual layer, dual side/dual layer
Audio formats:	DVD Audio MLP Lossless,™ SACD, Linear PCM, MPEG, Windows Media® 9, Dolby® Digital or DTS® audio discs
Still-image format:	JPEG
Video Signal System:	NTSC or PAL
HDMI™ Output:	Video: 480p, 720p, 1080i, 1080p HDMI Version 1.1-compliant HDCP Version 1.1-compliant
Composite Video Output:	1V p-p/75 ohms, sync negative polarity
S-Video Output:	
Y/luminance:	1V p-p/75 ohms, sync negative polarity
C/chrominance:	0.286V p-p
Component Video Output:	Y: 1V p-p/75 ohms, sync negative polarity
	Pr: 0.7V p-p/75 ohms
	Pb: 0.7V p-p/75 ohms
Analog Audio Output:	2V RMS (1kHz, 0dB)

Frequency Response:	
DVD (linear PCM):	2Hz – 22kHz +0/–0.5dB (48kHz sampling) 2Hz – 44kHz +0/–1.5dB (96kHz sampling) 2Hz – 88kHz +0/–0.5dB (192kHz sampling)
CD:	2Hz – 20kHz +0/–0.5dB
SACD:	2Hz – 100kHz +0/–0.5dB
Signal/Noise Ratio (SNR):	105dB (A-weighted)
Dynamic Range:	
DVD:	100dB (18-bit)/105dB (20-bit)
CD/DVD:	96dB (16-bit)
THD/1kHz:	DVD/CD: 0.0025%
Wow & Flutter:	Below measurable limits
AC Power:	110–240V AC/50–60Hz
Power Consumption:	1 Watt (on/standby)/13 watts (max)
Dimensions (H x W x D):	2" x 17-3/10" x 11-1/4" (50mm x 440mm x 285mm)
Weight:	6 lb (2.7kg)
Shipping Dimensions (H x W x D):	5" x 14-3/8" x 20" (127mm x 365mmx 508mm)
Shipping Weight:	8.8 lb (4kg)

Simplay HD The DVD 48 is Simplay HD™-verified for compatibility via the HDMI connection with other Simplay HD-verified products.

Depth measurement includes knobs, buttons and terminal connections. Height measurement includes feet and chassis.

All features and specifications are subject to change without notice.

Please register your product on our Web site at www.harmankardon.com. Note: You'll need your serial number. At the same time, you can choose to be notified about our new products and/or special promotions.

MODEL NAME : DVD 48

MP用

Description : Characteristics Specification of Audio
Test Disc : YEDS7 (SONY), TDV-540A (ABEX)
Test Conditions : 10kΩ Load Terminated, AC100V 50/60Hz
Test Measuerment : VP-7722A (Audio Analyzer) ,CASCADE SYS-2522(AP)

1.ANALOG AUDIO OUTPUT

Measurement Item			Limit	Result	TEST DISC
Output Level[Vrms]		L R	2.0 ± 0.2		YEDS7 (SONY) TRACK 1
Level difference [Vrms]			< 0.2		
F/ response [dB] Ref.1kHz 0dB	20 Hz	L R	0 ± 1.0		YEDS7 (SONY) TRACK 2
	100 Hz	L R	0 ± 1.0		YEDS7 (SONY) TRACK 4
	10 KHz	L R	0 ± 1.0		YEDS7 (SONY) TRACK 10
	20 KHz	L R	0 ± 1.5		YEDS7 (SONY) TRACK 13
	44 KHz	L R	0 ± 1.5		TDV-540A (ABEX) TITLE 4,CHAPTER 16 AUDIO STREAM 3
Emphasis Characteristic[dB] Ref.1kHz 0dB	5 KHz	L R	-4.53±1.0		YEDS7 (SONY) TRACK 40
	16 KHz	L R	-9.04 ± 1.0		YEDS7 (SONY) TRACK 41
S/N [dB] "A"		L R	>105		YEDS7 (SONY) TRACK 23
Channel Separation [dB] "22K"		L→R R→L	> 95		YEDS7 (SONY) TRACK 30,34
Linearity [dB] -90dB playback "22K"		L R	89.5±3		YEDS7 (SONY) TRACK 22
T.H.D [%] "22K"		L R	< 0.01		YEDS7 (SONY) TRACK 1
Dynamic Range [dB] -60dB playback "20K AES17"		L R	> 93		YEDS7 (SONY) TRACK 20
全高調波歪率 [%] DVD 96k "22K"		L R	< 0.01		TDV-540A (ABEX) TITLE 3, CHAPTER 1
Dynamic Range [dB] DVD 96k "20K AES17"		L R	> 95		TDV-540A (ABEX) TITLE 3, CHAPTER 2
全高調波歪率 [%] DVD 48k "22K"		L R	< 0.01		TDV-540A (ABEX) TITLE 2, CHAPTER 1
Dynamic Range [dB] DVD 48k "20K AES17"		L R	> 95		TDV-540A (ABEX) TITLE 2, CHAPTER 2

2. DIGITAL OUTPUT

1) OPTICAL OUT

JITTER 44.1kHz (mUI)		< 50mUI		Normal 44.1kHz CD Playback
JITTER 96kHz (mUI)		< 50mUI		Normal 96kHz DVD Playback

2) COAXIAL OUT

OUTPUT Level [mV] Peak to Peak Level at 75ohm Lo		500±50 (mV)		Normal CD or DVD Playback

MP用

2. DVD-Audio Part (Test Disc V-612 , JVC)

		Track Inform.	Limit	Downmix 2CH		Muiti 5 CH					SW
				LT	RT	FL	FR	SL	SR	C	
Output Level (V)		Tr.38 1KHz 0dB	2.1±0.2Vrms								
T.H.D (%) 20KHz LPF		Tr.38 1KHz 0dB	↓0.01%								
Frequency Respones (dB) Ref. : Tr. 38	48 / 24	Tr.59 17Hz	0±1.0dB								
		Tr.54 10KHz	0±1.0dB								
		Tr.53 20KHz	0±2.0dB								
	96 / 20	Tr.49 17Hz	0±1.0dB								
		Tr.45 10KHz	0±1.0dB								
		Tr.44 20KHz	0±2.0dB								
	192 / 24	Tr.22 17Hz	0±1.0dB								
		Tr.18 10KHz	0±1.0dB								
		Tr.17 20KHz	0±2.0dB								
S/N (dB) "A" Filter		Tr.40 Infinity Zero	↑90dB								
Dynamic Range (dB) "20KHz LPF AES17"		Tr.39 -60dB	↑85dB								

★ SW Level & THD --> Track 38 (30Hz) Play.

★ SW Frequency Respones -> Track 55(31Hz , 0dB) Reference

★ Track 54 (61Hz) , Track 53 (81Hz) , Track 51(127Hz) Play

3. SACD Part (Test Disc : DAC Ver1.2 , Philips)

	Track Inform.	Limit	Downmix 2CH		Muiti 5 CH					SW
			LT	RT	FL	FR	SL	SR	C	
Output Level (V)	Tr.25 1KHz 0dB	2.1±0.2Vrms								
T.H.D (%) 20KHz LPF	Tr.25 1KHz 0dB	↓0.01%								
Frequency Respones (dB) Ref. : Tr.17	Tr.9 20Hz	0±1.0dB								
	Tr.18 20KHz	0±2.0dB								
	Tr.21 50KHz	-4±4.0dB								
S/N (dB) "A" Filter	Tr.47 Infinity Zero	↑90dB								
Dynamic Range (dB) "20KHz LPF AES17"	Tr.32 -60dB	↑80dB								

★ SACD Frequency Respones -> Track 14(1KHz , -3dB) Reference

MODEL NAME : DVD48
Description : Characteristics Specification of Video
Test Disc : TDV-540A (ABEX) , MDVD-111 (TEAC) Serial NO.:
Test Conditions : 75Ω Load Terminated
AC Input : For USA (120V/60Hz) , For Europe (230V/50Hz)
Test Measuerment : VM-700T

MP用

1. Video Level Test (75Ω Terminated)

Measurement Item		Limit	Result	Test Disc
Video output [V]	Composite	1.0V ± 0.1V		MDVD-W111 TITLE1,CHAPTER2 100% COLOR BAR
	S-Video Y	1.0V ± 0.1V		
	S-Video C	286mV ± 30mV		
	Component Y	1.0V ± 0.1V		
	Component Pb	700mV ± 70mV		
	Component Pr	700mV ± 70mV		
	Scart CVBS	1.0V ± 0.1V		
	Scart Red	700mV ± 70mV		
	Scart Green	700mV ± 70mV		
	Scart Blue	700mV ± 70mV		

2. Video S/N Raito Test (75Ω Terminated)

Measurement Item		Limit	Result	Test Disc
Video SNR [dB] 100KHz~4.2MHz Use SC Trap	Composite	≥ 65.0 dB		TDV-540A TITLE2,CHAPTER 4 50% Gray Color
	S-Video Y	≥ 65.0 dB		
	Component Y	≥ 65.0 dB		
	Component Pb	≥ 65.0 dB		
	Component Pr	≥ 65.0 dB		

3. Chroma Signal AM.PM Test (75Ω Terminated)

Measurement Item		Limit	Result	Test Disc
Chroma AM [dB] 10KHz~500KHz	Composite Chroma	≥ 65.0 dB		TDV-540A TITLE2,CHAPTER17 100% Magenta Color
	S-Video Chroma	≥ 65.0 dB		
Chroma PM [dB] 10KHz~500KHz	Composite Chroma	≥ 60.0 dB		
	S-Video Chroma	≥ 60.0 dB		

MODEL NAME : DVD48
Description : Characteristics Specification of Video
Test Disc : TDV-540A (ABEX) , MDVD-111 (TEAC) Serial NO.:
Test Conditions : 75Ω Load Terminated
AC Input : For USA (120V/60Hz) , For Europe (230V/50Hz)
Test Measuerment : VM-700T

MP用

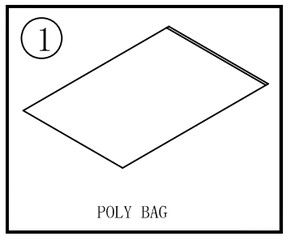
4. Video Frequency Respoens (75Ω Terminated)

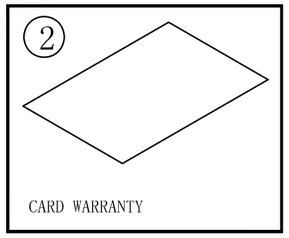
Measurement Item		Limit	Result	Test Disc
Composite [dB]	0.5MHz 0dB Ref.	0		MDVD-W111 TITLE1,CHAPTER7 100% Multi Brust
	1MHz	0dB ± 2dB		
	2MHz	0dB ± 2dB		
	3MHz	0dB ± 2dB		
	4MHz	0dB ± 2dB		
	5.8MHz	-3dB ± 2dB		

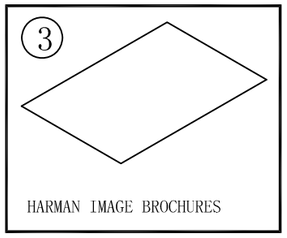
Measurement Item		Limit	Result	Test Disc
S-Video Y [dB]	0.5MHz 0dB Ref.	0		MDVD-W111 TITLE1,CHAPTER7 100% Multi Brust
	1MHz	0dB ± 2dB		
	2MHz	0dB ± 2dB		
	3MHz	0dB ± 2dB		
	4MHz	0dB ± 2dB		
	5.8MHz	-3dB ± 2dB		

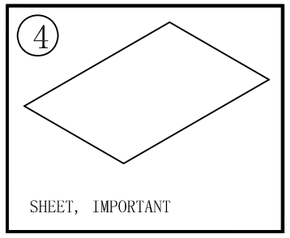
Measurement Item		Limit	Result	Test Disc
Component Y [dB] Interace Mode	0.5MHz 0dB Ref.	0		MDVD-W111 TITLE1,CHAPTER7 100% Multi Brust
	1MHz	0dB ± 2dB		
	2MHz	0dB ± 2dB		
	3MHz	0dB ± 2dB		
	4MHz	0dB ± 2dB		
	5.8MHz	-3dB ± 2dB		

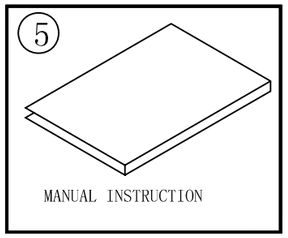
1. Instruction manual ass'y - Accessories

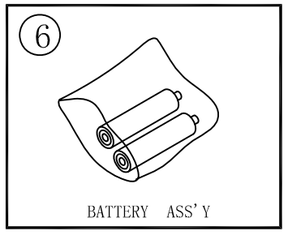


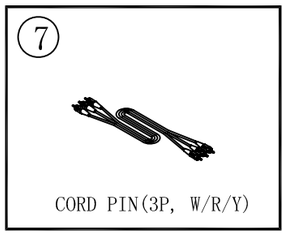


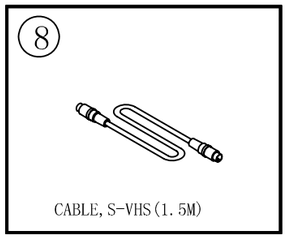


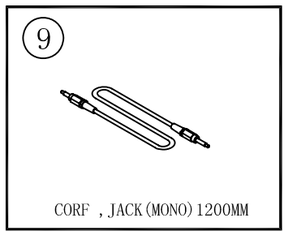


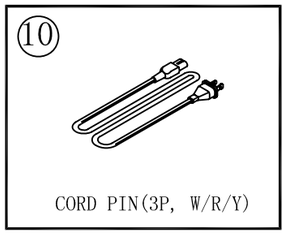


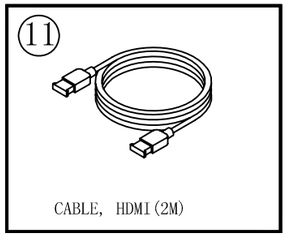


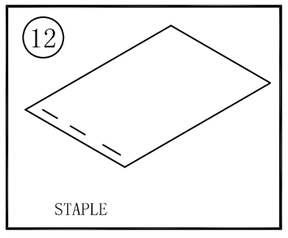






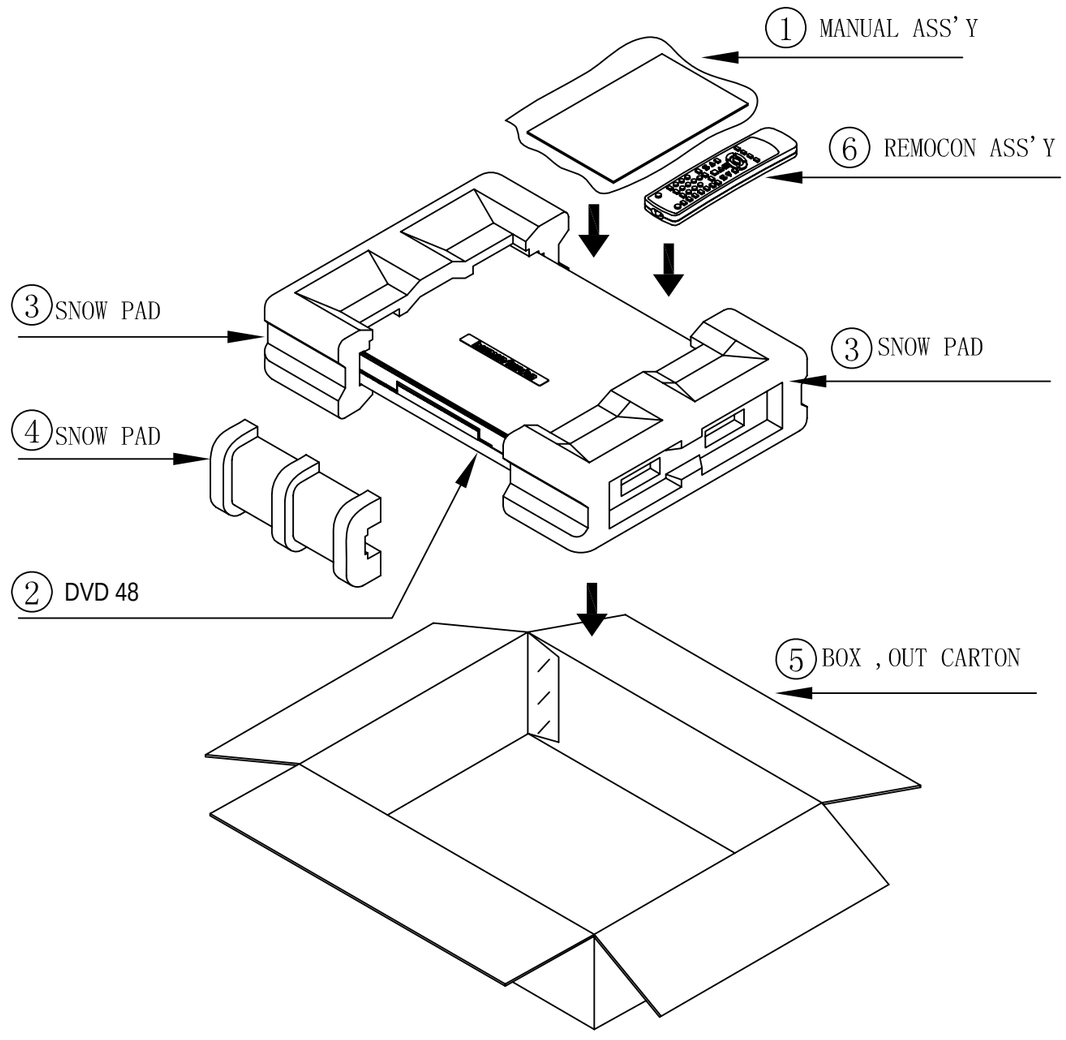






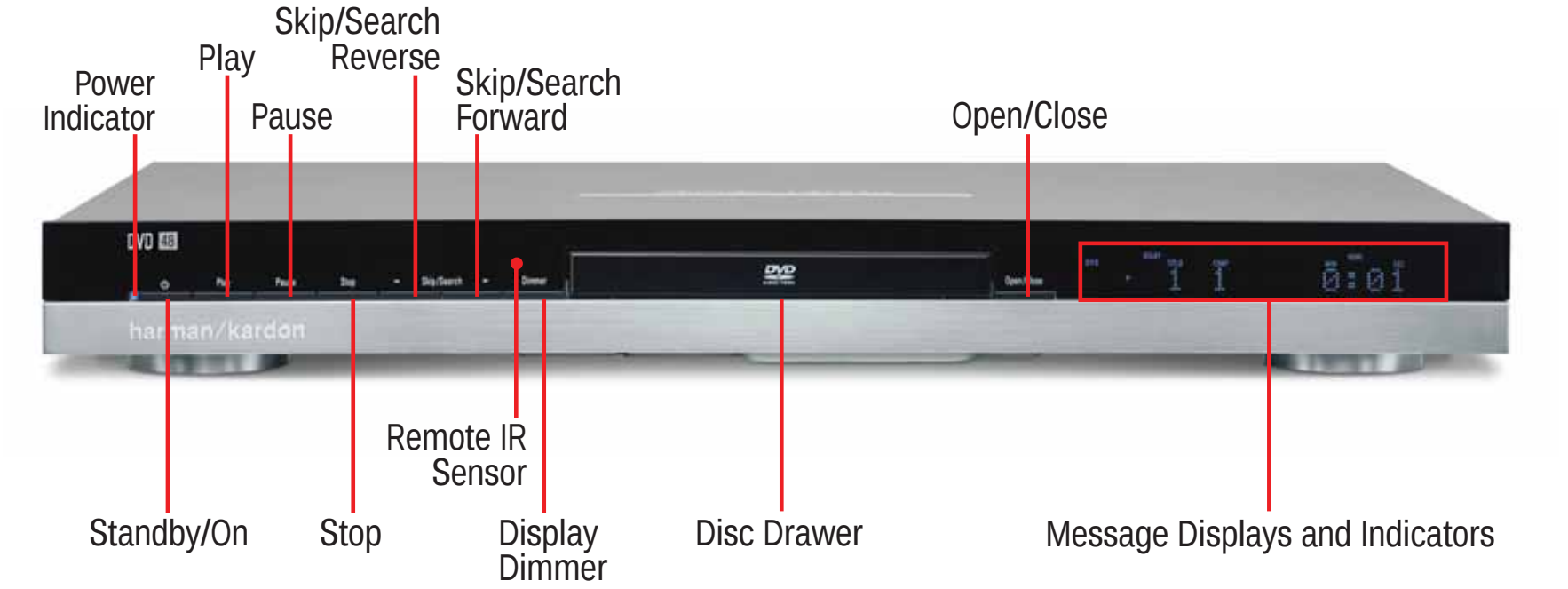
NO	DESCRIPTION	PARTS NO.	Q,ty
1	POLY BAG		1
2	CARD WARRANTY	CQE1A172X	1
3	HARMAN IMAGE BROCHURES		1
4	SHEET, IMPORTANT		1
5	INSTRUCTION MANUAL		1
6	BATTERY		2
7	CORD,PIN(3P,W/R/Y)	CJS4S004Z	1
8	CABLE,S-VHS(1.5M)	CJS0I006Z	1
9	CORD,JACK(MONO)1200MM	CJS9D002Z	1
10	AC CORD	CJA2A085Z	1
11	CABLE,HDMI(2M)	CJS8T001Z	1
12	STAPLE		3

2. Package Drawing



NO	DESCRIPTION	PARTS NO.	Q,ty
1	MANUAL ASS'Y		1
2	DVD 48	DVD 48	1
3	SNOW,PAD	CPS1A714	2
4	SNOW,PAD	CPS1A715	1
5	BOX,OUT CARTON	CPG1A798R	1
6	REMOCON ASS'Y	CARTDVD48	1
7			

FRONT PANEL CONTROLS



NOTE: To make it easier to follow the instructions throughout the manual that refer to this illustration, a copy of this page may be downloaded from the Product Support section at www.harmankardon.com.

FRONT-PANEL CONTROLS

Standby/On Switch: This electrical switch turns the DVD 48 on for playback, or leaves it in Standby mode for quick turn-on using this switch or the remote control.

Power Indicator: This LED is next to the Standby/On Switch. When the DVD 48 is plugged into AC power, the LED turns amber to indicate that the DVD 48 is in Standby mode (ready to be turned on). When the DVD 48 is turned on (by pressing the Standby/On Switch), the LED turns blue. If this LED ever turns red, immediately unplug the DVD 48. Check the wire connections. If the LED remains red, bring the DVD 48 to an authorized Harman Kardon service provider.

Open/Close: Press this button to open or close the disc drawer. When the DVD 48 is in Standby mode, press this button to turn it on and open the drawer. Before pressing this button, always make sure that no objects are blocking the drawer. Remember to close the door or turn off the DVD 48 when you have finished. The door will close automatically after two and a half minutes.

Message Display: Various messages appear in this display in response to commands. In addition, a variety of indicators will light at various times to display the current playback mode, video settings or other aspects of the DVD 48's status.

Disc Drawer: This drawer holds a disc that is played in the DVD 48. Press the Open/Close Button to access it. Be sure to carefully seat all discs in the recess in the drawer tray. To avoid damaging the drawer accidentally, do not press down on it when open. The drawer will close automatically after two and a half minutes of inactivity to prevent dust or dirt from entering the DVD 48 and to prevent damage. If a disc is present, it will begin playing.

Play: Press to start playback of a loaded disc, or to resume play after the disc has been paused.

Pause: Press to pause play, or to resume after play has been momentarily paused. When a DVD is playing, a still image of the frozen action will appear on-screen. In Pause mode, you may access the Frame-by-Frame Advance and Slow Search functions by pressing the forward or reverse Step or Skip Buttons on the remote.

Stop: Press once to stop play and enter Resume mode, in which pressing Play resumes playback from the point at which it was stopped. Press this button twice to fully stop play of the disc. Resume mode is not available for WMA files or VCDs without playback control.

Skip/Search Reverse: Press once to return to the beginning of the current chapter or track. Quickly press again to skip to previous chapters or tracks. Press and hold for fast search reverse within the current chapter or track at the speed indicated on screen.

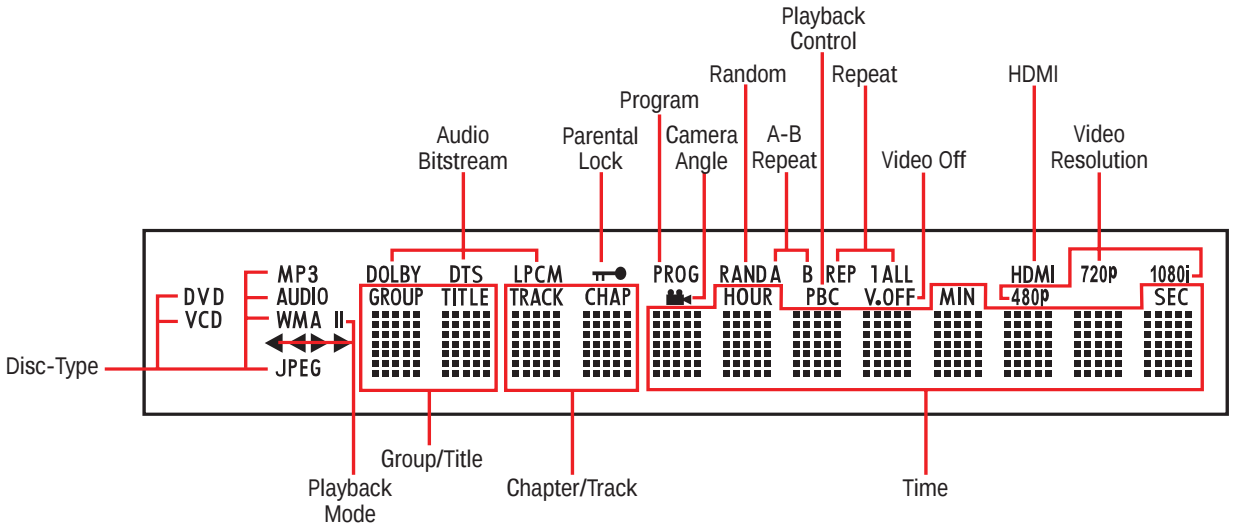
Skip/Search Forward: Each press advances to the next chapter or track. Press and hold for fast search forward within the current chapter or track at the speed indicated on-screen.

Remote IR Sensor: This sensor receives infrared commands from the remote control. It is important to ensure that it is not blocked. If covering the sensor is unavoidable, such as when the DVD 48 is placed inside a cabinet, you may use an optional Harman Kardon HE 1000, or other infrared receiver, connecting it to the Remote IR Input on the DVD 48's rear panel. Alternatively, connect the Remote IR Output of another compatible component, such as a Harman Kardon AVR, to the DVD 48's Remote IR Input. Point the remote at the other device's remote sensor, and the command will be transmitted to the DVD 48. An external IR "blaster" may also be used, positioned to point at this area.

Dimmer: Some people find the front-panel display distracting, especially while watching a movie. Each press of this button cycles through the front-panel brightness options of Full Brightness, Half Brightness and Off. The Power Indicator always remains lit to remind you that the DVD 48 is turned on, but the display will remain dimmed or off, even when a command is entered. Dimming is canceled when the DVD 48 is turned off.

Open/Close: Press this button to open or close the disc drawer.

FRONT-PANEL INFORMATION DISPLAY



NOTE: To make it easier to follow the instructions that refer to the controls and connectors in this illustration, a larger copy may be downloaded from the Product Support section for this product at www.harmankardon.com.

Disc-Type Indicators: The SACD, DVD, DVD-Audio, CD, VCD, MP3, WMA or JPEG indicator will light to show the type of disc currently being played.

Audio Bitstream Indicators: When a Dolby Digital, DTS or Linear PCM digital audio signal is detected, one of these indicators will light. DVD-Audio, MP3 and WMA bitstreams will be indicated by the Disc-Type Indicator.

Parental-Lock Indicator: This indicator lights in red when the parental-lock system is engaged to prevent changing the rating level without a code.

Program Indicator: This indicator lights when a playlist has been programmed using the menu system (available for CDs only).

Angle Indicator: This indicator blinks when alternative viewing angles are available on the DVD currently playing.

Random Indicator: This indicator lights when the unit is in the Random Play mode.

A-B Repeat Indicator: This indicator lights when a specific passage for repeat playback has been selected.

VCD Playback Control Indicator: This indicator lights when the playback control function is turned on for VCDs.

Repeat Indicators: These indicators light when any of the Repeat functions are in use.

Video OFF Indicator: This indicator lights in red when the unit's video output has been turned off by pressing the Video OFF Button on the remote control.

HDMI Indicator: This indicator lights when the HDMI Output is enabled. Press the HDMI Button on the remote to toggle between turning the HDMI Output on and off. When the HDMI Output is on (and this indicator is lit), the Component Video Outputs are deactivated, and vice versa.

Video Resolution Indicators: One of these indicators will light to indicate the current video resolution of the HDMI Output, based on what your video display is capable of handling. The HDMI Output will upscale source materials to the higher resolution, as indicated in the HDMI SETUP menu (explained in the Initial Setup section). You may change the HDMI Video setting to a lower resolution to improve picture quality using the VIDEO SETUP menu. As you select a specific HDMI Output video resolution and the DVD 48 successfully determines that the video display is capable of handling that resolution, its indicator will light and will appear briefly in the Message Display.

Time Indicators: These positions show the running time of a disc in play.

NOTE: These positions will also display text messages about the DVD's status, including Loading when a disc is loading, Power Off when the unit is turned off, and Unknown Disc when a disc not compatible with the DVD 48 is loaded.

Chapter/Track Number Indicators: When a DVD disc is playing, these two positions show the current chapter. When a DVD-Audio, SACD or CD disc is playing, they will show the current track number.

Group/Title Indicators: These two positions show the current title number when a DVD disc is playing, or the current group for a DVD-Audio disc.

Playback-Mode Indicators: These indicators light to show the current playback mode:

▶ Lights when a disc is playing in the Normal mode. This indicator will flash when the disc is in Forward Slow Play mode. The on-screen banner display indicates the selected speed (1/2x, 1/4x, 1/8x or 1/16x).

▶▶ When the DVD 48 is in the Fast Search Play mode, two of these indicators will light to show that the unit is in a Fast Play mode. The selection will be displayed on screen as one of six steps that correspond to the following speeds: ~1-1/2x, 4x, 6x, 8x, 16x or 32x. Fast Play mode is not available for WMA files.

❙❙ Lights when the disc is paused.

◀◀ Lights when the disc is in the Fast Search Reverse mode. The selection will be displayed on screen as one of six steps that correspond to the following speeds: ~1-1/2x, 4x, 6x, 8x, 16x or 32x. Fast Search Reverse mode is not available for WMA files.

◀ Flashes when the disc is in Reverse Slow Play mode. The on-screen banner display indicates the selected speed (1/2x, 1/4x or 1/8x).

REAR-PANEL CONNECTIONS

Remote Infrared (IR) Input and Output: When the Remote IR sensor on the front panel is blocked, such as when the DVD 48 is placed inside a cabinet, connect the IR Output of your receiver/processor or an optional IR receiver to the Remote IR Input jack for use with the remote control. The Remote IR Output may be connected to the Remote IR Input of a compatible source device (or other product) to enable remote control through the DVD 48. When several devices are used, connect them in "daisy chain" fashion.

HDMI Output: If you have an HDMI-compatible receiver or video display device, connect this output to an HDMI input on the receiver or video display for high-quality digital audio and video. Even if your receiver is not capable of processing audio in the HDMI format, you will still experience the superb reproduction of HDMI video.

In all cases, the video display must be HDCP-compliant in order to use the HDMI output. For best results, we do not recommend HDMI connections in excess of ten feet without a repeater. If your video display has a DVI input, you may use an optional HDMI-to-DVI cable or adapter for the video connection to the display, and a separate audio connection.

The DVD 48 is Simplay HD-verified for compatibility via the HDMI connection with other Simplay HD-verified products.

NOTE: To use the HDMI Output, make sure to turn it on by pressing the HDMI Button on the remote. When the HDMI Output is turned on, the Component Video Outputs are not available for use.

The following audio formats may be output via the HDMI connection:
Audio CD – 2-Channel PCM or 5.1-channel DTS
DVD-Audio – 2-Channel or 5.1-channel PCM
DVD-Video – Up to 5.1-channel Dolby Digital, DTS or PCM

NOTE: To hear the high-resolution surround sound recorded on SACD discs, connect the 6-Channel Audio Outputs to the corresponding input jacks on your receiver or processor. This format is not output digitally. If your receiver is not capable of processing the audio portion of an HDMI signal, use the 6-Channel Audio Outputs to enjoy DVD-Audio discs as well.

To hear a 2-channel analog downmix via the 2-Channel Analog Audio Outputs, select Stereo at the Analog Output setting in the AUDIO SETUP submenu, or press the Audio Mode Button on the remote repeatedly until the Stereo setting is selected.

Coaxial and Optical Digital Audio Outputs: If your receiver or processor has an available digital audio input, connect either of these digital audio outputs to the corresponding input on the receiver/processor to enjoy digital audio formats such as Dolby Digital, DTS or standard PCM (traditionally found on CDs and may be available on other discs). Never connect both of these outputs to the same device simultaneously. However, it is okay to connect one of the digital audio outputs plus the analog audio outputs to the same device.

NOTE: The Coaxial Digital Output should only be connected to a digital input. Even though it is the same RCA-type connector as standard analog audio connections, DO NOT connect it to a conventional analog input jack.

Component Video Outputs: If your television or video display and receiver are component video-capable, and your display does not have an HDMI input, connect these jacks to the corresponding inputs on the receiver or TV that are labeled "Y/Pr/Pb" or "Y/Cr/Cb." If your video display is capable of handling resolutions of 480p or better, connect these outputs to the HD (high-definition) component video inputs on your display. If the display is capable of displaying progressive-scan video, select On at the Progressive Scan setting in the VIDEO SETUP submenu.

IMPORTANT NOTE: Do not connect the Component Video Output jacks to standard composite video inputs on any device.

Composite and S-Video Outputs: If your video display does not have HDMI or component video inputs, connect one of these two video outputs to your receiver/processor or directly to the display. If available, S-video is preferred. Do not connect more than one of the DVD 48's analog video outputs (component video, S-video, composite video) to any other device at the same time. You may connect both the HDMI Output and the Composite Video Output to your receiver if your receiver distributes composite video through a multiroom system.

2-Channel Analog Audio Outputs: Connect these outputs to the left and right analog audio inputs on your receiver/processor or TV. You may connect these jacks in addition to a digital audio connection, and it is recommended that you do so as a backup if you wish to use the DVD 48 as a source device for a multiroom system or if you wish to make analog recordings, as it is not possible to make digital recordings of most DVDs.

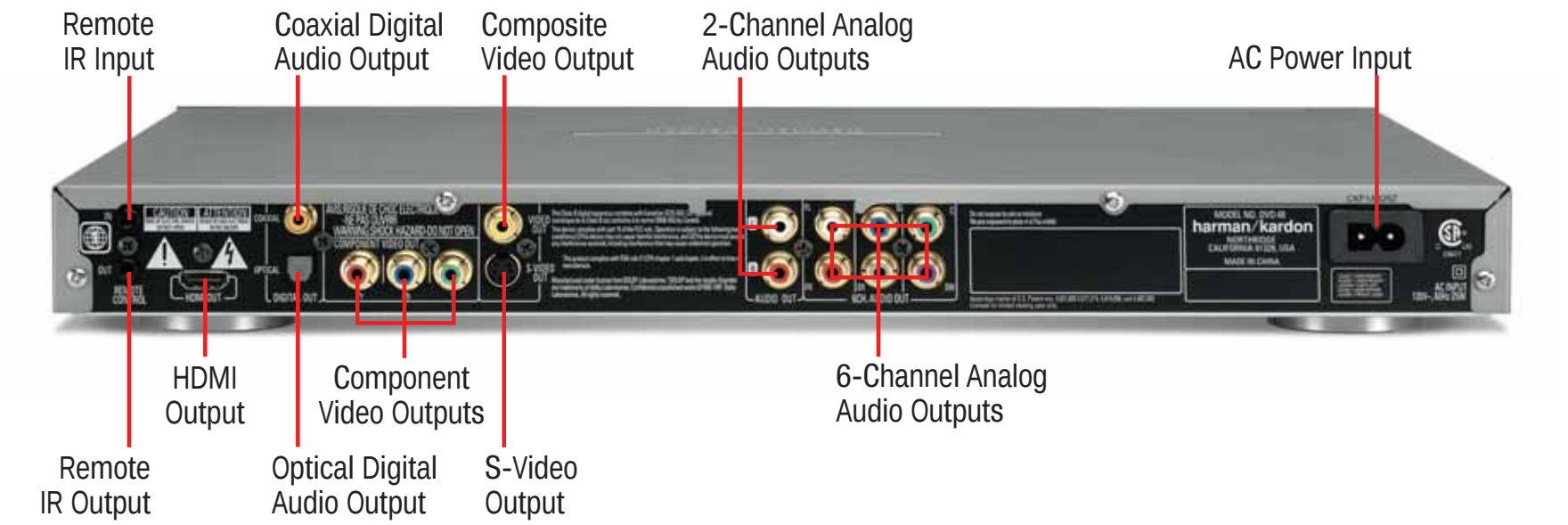
6-Channel Analog Audio Outputs: Connect these outputs to the matching 6-channel analog audio inputs on your receiver or surround sound processor. This connection is required to listen to the multichannel tracks on SACD discs. If the disc also contains a Linear PCM, Dolby Digital or DTS track, you may listen to it using the HDMI Output, the Coaxial or Optical Digital Audio Output or the 2-Channel Analog Audio Outputs.

NOTE: A 2-channel downmix is not available simultaneously with a 6-channel presentation. Set the Analog Output in the AUDIO SETUP menu to Stereo to hear a 2-channel downmix, available at both the 2-Channel Analog Audio Outputs and the front left and right outputs of the 6-Channel Analog Audio Outputs. In Stereo mode, no audio will be available at the center and surround outputs of the 6-Channel Analog Audio Outputs.

If the 6-Channel Analog Audio Outputs are connected to corresponding 6-channel inputs on your receiver, set the Analog Output in the AUDIO SETUP menu to Multichannel to hear all six channels (if available on the disc). In Multichannel mode, only the front left and right channel information will be available at the 2-Channel Analog Audio Outputs, without any center or surround information.

AC Power Input: Connect the AC power cord to an AC outlet, and plug the cord's female end into this receptacle. If the outlet is controlled by a switch, make certain that it is in the ON position. If the cord somehow becomes damaged, contact your authorized Harman Kardon dealer for a replacement.

REAR PANEL CONNECTIONS



NOTE: To make it easier to follow the instructions throughout the manual that refer to this illustration, a copy of this page may be downloaded from the Product Support section at www.harmankardon.com.

REMOTE CONTROL FUNCTIONS

IR Transmitter Lens: As buttons are pressed on the remote, infrared codes are emitted through this lens. Make sure it is pointing toward the component being operated.

Power On: Press this button to turn on the DVD 48 when it is in Standby mode (plugged in with the Power Indicator lit up in amber).

Power Off: Press this button to turn off the DVD 48, placing it in Standby mode.

Open/Close: Press this button to open or close the disc drawer. If the DVD 48 is in Standby mode, pressing this button will turn it on.

Page Up/Down: Some DVD-Audio discs allow you to select from several still images associated with an audio selection while it is playing. If the disc has implemented this feature, press these buttons to view the images in forward or reverse order. If this feature is not available, the feature-prohibited icon "Ø" will be displayed in the upper right corner of the screen.

Audio: Press this button while a DVD is playing to display the current audio track information and to select another audio format.

Clear: Press this button to clear a number you have started to enter. This button may also be used to clear the on-screen displays. Press and hold this button for five seconds while in Stop mode and with all on-screen displays cleared, to reset the DVD 48 to its factory-default settings.

Title: This button allows you to select from the titles stored on the disc, which may include "making of" or other featurettes. Some DVD-Audio and Video discs may display their disc menu.

Subtitle: Press this button while a DVD containing subtitle information is playing, to turn subtitles off or to select a subtitle language. This setting will only be in effect for the current disc.

NOTE: Due to the variations in how DVD discs are authored, the subtitle languages displayed by the DVD 48 may not accurately reflect the actual languages available on the disc. It is recommended that subtitles be selected using the disc's menu.

Program: Press this button to display the Program screen, where you may program a playlist in which the tracks may be played in a different order than the order in which they appear on the disc. See the Programming a Playlist section for more information.

Repeat: Press this button repeatedly to cycle through the Repeat modes available with the current disc. This button is not used to access A-B Repeat mode.

A-B Repeat: While a disc is playing, the A-B Repeat function allows you to repeatedly play a passage, which may include several tracks or chapters. Press the button once to select the starting point ("A"), and a second time to select the end of the passage ("B"). Press the button again to end repeat play.

Random: This button turns Random Play mode – which plays the tracks on a CD in random order – on or off.

Numeric Keys: Use these buttons to directly enter a track or chapter number to skip to that section of the disc, or to enter a password for the parental control system.

Group: This button allows you to select from the groups stored on the disc, which may include the same content recorded using different audio formats. When the dialog box appears, the total number of groups will be indicated. Use the Numeric Keys to enter the number of the desired group, and press the Enter Button. The dialog box will disappear, and the DVD 48 will begin playing the new group.

System Setup: Press this button to access the SYSTEM SETUP menu. See the Initial Setup section for more information.

Disc Menu: Press this button while a DVD is playing to view the disc's menu. Some DVD-Audio discs may require you to press the Title Button to access the disc menu.

Status: When a disc is playing, press this button to view the Status Display, which contains playback mode information. The Status Display is not available for MP3, WMA or JPEG discs.

Return: Press this button while viewing the DVD 48's Setup menus or Status Display to return to a previous screen or clear the display. It has no effect on a disc's menus.

Transport Controls: These buttons are used to operate the disc player. Use the controls to skip forward or in reverse by track or chapter; to fast-search forward or in reverse; and to play, pause or stop the disc. After pressing the Pause Button, the Skip Buttons may be used to step frame by frame through a video presentation, and the Fast-Search Buttons may be used for slow play.

Angle: When a DVD encoded with multiple camera angles is playing and when the Angle Icon appears to indicate that the multiple-angle passage has been reached, press this button to cycle through the various available angles.

This button is also used to rotate still images. Each press rotates the image 90 degrees clockwise.

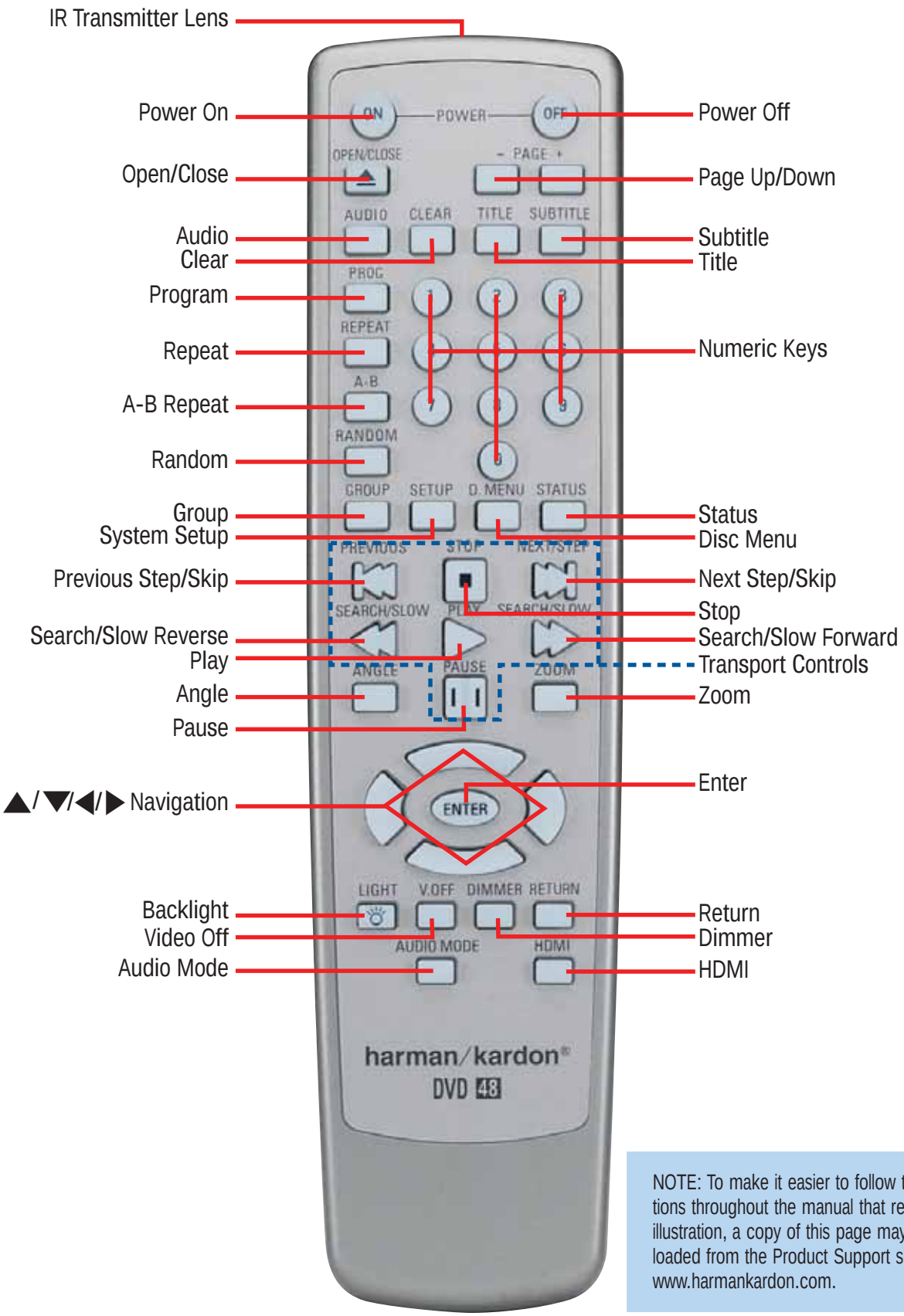
Zoom: When viewing a DVD, VCD or JPEG still image, press this button repeatedly to enlarge the on-screen image by 1-1/2x, 2x, 3x or 4x (1-1/2x, 2x or 3x only for VCDs) before returning to the original size. Use the Navigation Buttons to explore the enlarged image.

▲/▼/◀/▶ Navigation and Enter Buttons: These buttons are used together to make selections within the on-screen menu system.

Backlight: Press this button to turn on the backlight to make it easier to see the buttons in a darkened room. The backlight will remain on for a few seconds after your last button press before going out, or you may turn off the backlight by pressing this button again.

Video Off: Some people prefer to turn off the video display when listening to audio-only discs. Pressing this button deactivates the video circuitry, avoiding any possible interference with the audio. Moreover, plasma and CRT video displays are subject to "burn-in" when a still image, such as a menu, remains on screen for more than a short time.

REMOTE CONTROL FUNCTIONS



NOTE: To make it easier to follow the instructions throughout the manual that refer to this illustration, a copy of this page may be downloaded from the Product Support section at www.harmankardon.com.

REMOTE CONTROL FUNCTIONS

We strongly recommend that plasma and CRT owners use the Video Off function liberally. Press the button a second time to reactivate the video displays.

NOTE: The DVD 48 features a screen saver that you may set to appear automatically after a period of inactivity. However, the screen saver does not become activated when the DVD 48's Setup menus are on screen. The DVD 48 also allows you to set one of two Auto Power Off modes in the GENERAL SETUP menu that turn off the DVD 48 after a longer period of inactivity. See the Initial Setup section for more information.

Dimmer: Some people find the front-panel displays distracting, especially while watching a movie in a darkened room. Each press of this button cycles through the Full Brightness, Half Brightness and Off settings. The Power Indicator will always remain lit to remind you that the DVD 48 is turned on.

NOTE: You may enter commands and operate the DVD 48 normally even with the front-panel display fully dimmed. The display will wake for about one second when a command is entered.

Audio Mode: This button adjusts the Analog Output setting, which is also found in the AUDIO SETUP menu.

There are two available settings: Multichannel and Stereo. The first button press displays the current setting, and each additional press toggles between the settings.

The Stereo, or 2-Channel, setting outputs a 2-channel downmixed signal to both sets of Left/Right Analog Audio Outputs. The downmix incorporates center and surround channel information, but no signal is available at the center or surround jacks of the 6-Channel Analog Audio Outputs.

The Multichannel, or 6-Channel, setting outputs only the front left and right channel information to both sets of Left/Right Analog Audio Outputs. Although the correct signals are available at all of the 6-Channel Analog Audio Output jacks, the 2-Channel Analog Audio Outputs will contain incomplete information.

The DVD 48 does not make a 2-channel downmix available at the 2-Channel Analog Audio Outputs simultaneously with a multichannel signal at the 6-Channel Analog Audio Outputs.

HDMI: Press this button to turn the HDMI Output on or off. When the HDMI Output is on, the Component Video Outputs are off. If your video display is HDMI-capable, turn this setting on and use the HDMI connection. If your video display does not have an HDMI input, turn this setting off to use the Component Video Outputs.

CONNECTIONS

There are different types of audio and video connections used to connect the DVD 48 to your receiver or processor and video display. To make it easier to keep them all straight, the Consumer Electronics Association (CEA®) has established a color-coding standard. Table 1 may be helpful to you as a reference while you set up your system.

Table 1 – Connection Color Guide

Audio Connections		
	Left	Right
Front **(FL/FR)**		
Center **(C)**		
Surround **(SL/SR)**		
Subwoofer **(SUB)**		
Digital Audio Connections		
Coaxial		
Optical	Input	Output
Video Connections		
Component	Y	Pb Pr
Composite		
S-Video		
HDMI™ Connections (digital audio and video)		
HDMI		

Types of Connections

This section will briefly review different types of cables and connections that you may use to set up your system.

Audio and video signals originate in what are known as "source devices," including a DVD/CD player such as the DVD 48.

Separate connections are required for the audio and video portions of the signal unless an HDMI connection is used (see below). The types of connections used depend upon what's available on your receiver, and for video signals, the capabilities of your video display.

Audio Connections

There are two formats for audio connections: digital and analog. Digital audio signals are required for listening to sources encoded with digital surround modes, such as Dolby Digital and DTS. There are two types of digital audio connections commonly used: coaxial and optical. Either type of digital audio connection may be used, but never both simultaneously. However, it's okay to make both analog and digital audio connections at the same time to the same source.

NOTE: The DVD 48 outputs digital audio signals through the HDMI connection. If your receiver/processor or video display is capable of *processing* the audio portion of the HDMI signal, then you will not need to make a separate digital audio connection. However, as explained in the Analog Audio section below, you may still need to make the analog audio connections.

If your receiver/processor is only capable of *switching* HDMI signals, use HDMI for your video connection only and connect either the DVD 48's coaxial or optical digital audio output to the corresponding input on your receiver.

In addition, SACD audio is not transmitted via HDMI. Use the 2- or 6-Channel Analog Audio Outputs to enjoy your SACD discs.

Digital Audio

Coaxial digital audio jacks are usually color-coded in orange. Although they look similar to analog jacks, they should not be confused, and you should not connect coaxial digital audio outputs to analog inputs or vice versa. See Figure 1.

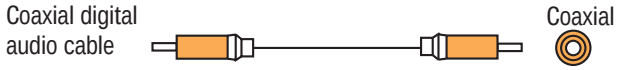


Figure 1 – Coaxial Digital Audio

Optical digital audio connectors are normally covered by a shutter to protect them from dust. The shutter opens as the cable is inserted. See Figure 2.

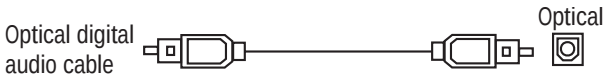


Figure 2 – Optical Digital Audio

Due to the nature of digital signals as binary bits, they aren't subject to signal degradation the way analog signals are. Therefore, the quality of coaxial and optical digital audio connections should be the same, although it is important to limit the length of the cable. Whichever type of connection you choose, Harman Kardon recommends that you always select the highest quality cables available within your budget.

Analog Audio

Analog connections require two cables, one for the left channel (white) and one for the right channel (red). See Figure 3. These two cables are often attached to each other for most of their length. Most devices that have digital audio jacks also have analog audio jacks. We recommend that you always connect the DVD 48's 2-Channel Analog Audio Outputs to your receiver/processor, or to your TV if you are not using a receiver. There are four reasons to use analog audio connections, even if you are using one of the digital audio connections:

1. To make recordings. Most DVDs are protected from digital copying and only analog copies are permitted. Please make sure to comply with all copyright laws when making recordings for personal use.
2. In a multiroom system. Many receivers and processors require sources used in multiroom systems to output analog audio signals.
3. When connecting the DVD 48 directly to a non-HDMI TV. The TV may not have digital audio inputs.
4. When playing high-resolution 96kHz PCM audio discs. If your receiver is not capable of processing 96kHz audio, you may need to use the analog audio connection.

NOTE: The DVD 48 is capable of downmixing multichannel materials and outputting a 2-channel downmix. Make sure to adjust the Analog Output setting in the AUDIO SETUP menu to Stereo.

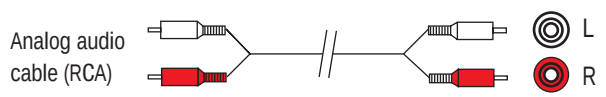


Figure 3 – Analog Audio

Multichannel analog connections are used with high-resolution audio discs, where the copy-protected digital content is decoded inside the DVD 48. These connections are required for playing SACD discs, and depending on your receiver's capabilities, may also be required for DVD-Audio, HD-DVD or Blu-ray discs, unless the disc also carries two-channel PCM and 5.1-channel Dolby Digital or DTS soundtracks for use with receivers/processors that are not equipped with 5.1-channel analog inputs. Check the disc's jacket for more information on alternate audio tracks. See Figure 4.

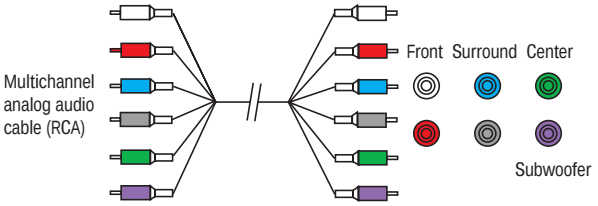


Figure 4 – Multichannel Analog Audio

NOTE: In order to enjoy the full benefit of lossless multichannel recordings, make sure the Analog Output setting in the AUDIO SETUP menu is set to Multichannel. When the Stereo setting is selected, the center and surround channel information will be combined with the left and right channels, and will only be heard through the front channels. This setting may also be accessed by pressing the Audio Mode Button on the remote.

Video Connections

As mentioned above, the video signal is often transmitted separately from the audio signal. Even when the HDMI connection described below is used, sometimes the receiver is not capable of accessing the audio portion of the HDMI signal, and a separate audio connection is required.

Digital Video

The DVD 48 is equipped with an HDMI (High-Definition Multimedia Interface) output. HDMI is capable of carrying digital audio and video information using a single cable, delivering high-quality picture and sound.

The DVD 48 is capable of outputting up to 720p, 1080i or 1080p video and 2- or 6-channel PCM or up to 5.1-channel Dolby Digital or DTS audio through its HDMI connection. The DVD 48 is in compliance with HDCP (High-Definition Copy Protection) and the video display must also be HDCP-compliant to be used with the DVD 48's HDMI output.

SimplayHD The DVD 48 is Simplay HD-verified for compatibility via the HDMI connection with other Simplay HD-verified products.

The physical HDMI connection is simple. The connector is shaped for easy plug-in (see Figure 5). If your video display has a DVI input, you may use an HDMI-to-DVI adapter (not included) to connect it to the HDMI Output, but a separate audio connection is required.

Figure 5 – HDMI Connection

Analog Video

There are three types of analog video connections: composite video, S-video and component video.

Composite video is the basic connection most commonly available. The jack is usually color-coded yellow, and looks like an analog audio jack, although it is important never to confuse the two. Do not plug a composite video cable into an analog or coaxial digital audio jack, or vice versa. Both the chrominance (color) and luminance (intensity) components of the video signal are transmitted using a single cable. See Figure 6.

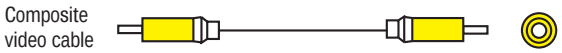


Figure 6 – Composite Video

S-video, or "separate" video, transmits the chrominance and luminance components using separate wires contained within a single cable. The plug on an S-video cable contains four metal pins, plus a plastic guide pin. Be careful to line up the plug correctly when you insert it into the jack on the receiver, source or video display. See Figure 7.

Figure 7 – S-Video

Component video separates the video signal into three components – one luminance ("Y") and two sub-sampled color signals ("Pb" and "Pr") – that are transmitted using three separate cables. The "Y" cable is color-coded green, the "Pb" cable is colored blue and the "Pr" cable is colored red. See Figure 8.

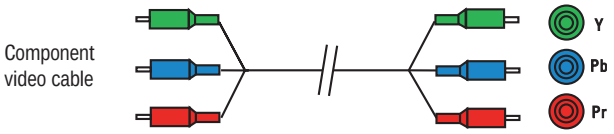


Figure 8 – Component Video

Do not confuse component video connections with composite video (described above). Although the plugs and jacks may look similar, they are not compatible and cross-connecting them will result in no picture or a very distorted picture. Remember that component video uses three connections, colored green, blue and red, while composite video uses a single connection, which is often color-coded yellow.

If your video display is capable of handling progressive-scan signals (480p or better), then connect the DVD 48's Component Video Outputs to the input jacks on your video display marked "HD Component". Make sure to configure your display for use with 480p video signals. Set the Progressive Scan setting in the DVD 48's VIDEO SETUP menu to On.

NOTES:

- The DVD 48's component and HDMI outputs are not available simultaneously. Press the HDMI Button on the remote to turn the HDMI Output On or Off. When it is On, the Component Video Outputs are Off, and vice versa.
- For simplified operation, connect one of the DVD 48's video outputs to your receiver or processor, and use the receiver/processor as a switching device for all of your sources,

CONNECTIONS

connecting only the receiver/processor to your video display. However, if your receiver is not capable of switching HDMI signals, connect the DVD 48's HDMI Output directly to an HDMI-capable video display for superior picture quality.

- If you are using the DVD 48 with a multiroom receiver/processor that is capable of distributing video, connect the DVD 48's Composite Video Output to the receiver in addition to the HDMI, Component Video or S-Video Output.

If it's available on your video display, HDMI is recommended as the best-quality connection, followed in preference by component video, S-video and then composite video. Except as indicated above for use in a multiroom system, do not connect more than one video output from the DVD 48 to another device.

Remote IR Input and Output

The DVD 48 is equipped with an infrared input and output to facilitate use of your system with a remote control in a variety of situations.

When the DVD 48 is placed in such a way that aiming the remote at the front-panel IR sensor is difficult, such as inside a cabinet or facing away from the listener, you may connect an external IR receiver, such as the optional Harman Kardon HE 1000, to the Remote IR Input jack.

If your receiver or any of your other components are equipped with a compatible remote IR input, you may use the included 1/8" mini-plug interconnect cable to connect the Remote IR Output to the device's remote IR input, which will pass any applicable remote signals transmitted through the DVD 48 to the other device. This enables you to control your devices even when the DVD 48 itself is controlled via an external IR receiver.

To control more than one device using the Remote IR Output, connect all devices in "daisy chain" fashion, with the receiver's remote IR output connected to the DVD 48's Remote IR input, then the DVD 48's Remote IR Output connected to the next device's remote IR input, that device's remote IR output connected to the next device's remote IR input, and so forth.

NOTE: Not all remote controllable devices are equipped with compatible IR inputs and outputs. Check with the manufacturer of the source device for more information on the type of IR signal expected. The DVD 48 will output a "stripped carrier" IR signal.

You are now ready to connect the DVD 48 to your system. Before beginning, make sure that all components, including the DVD 48, are turned completely off and their power cords are unplugged. Don't plug any of the power cords back in until you have finished making all of your connections.

Many components in a home theater system, such as a receiver or power amplifier, generate a great deal of heat that can interfere with the operation of the DVD 48. Therefore, it is best to place the DVD 48 on its own shelf instead of stacking it directly on top of another component. It is also a good idea to check the finish of your shelf. Some wood or other finishes can be affected over time by the DVD 48's rubber feet.

Step One – Connect the DVD 48 to Other Components

Select one of the following two sections, depending on whether you are connecting the DVD 48 directly to a television or video display, or if you are using an audio/video receiver or processor (this manual will use the term "receiver" to refer to either a receiver or a processor) that incorporates the DVD 48 as part of a home theater system.

Connecting the DVD 48 Directly to a Television

If your television is HDMI-capable and HDCP-compliant, then only one cable connection is required, and it will carry both audio and video signals. Use the included HDMI cable to connect the DVD 48's HDMI output to your television's HDMI input. See Figure 9. If your television has a DVI input rather than an HDMI input, purchase an HDMI-to-DVI cable or adapter, and make a separate audio connection to the TV.

Simplay HD The DVD 48 is Simplay HD-verified for compatibility via the HDMI connection with other Simplay HD-verified products.

Figure 9 – HDMI Output

NOTE: When using the HDMI connection, turn on the television or video display *before* the DVD 48.

If your video display does not have an HDMI input, then separate audio and video connections are required. Select one of these types of video connections, in order of preference: component video, S-video, composite video. See Figure 10.

Figure 10 – Component, S- and Composite Video Outputs

Most video displays are not equipped with coaxial or optical digital audio inputs. If your display is, then it would be preferable to connect one of the DVD 48's digital audio outputs to the corresponding input on your display. However, most likely you will use the 2-Channel Analog Audio Outputs. See Figure 11.

Figure 11 – 2-Channel Analog Audio Outputs

NOTE: The DVD 48 is capable of downmixing 5.1-channel materials to the 2-channel format, but it is necessary to adjust the Analog Output setting in the AUDIO SETUP menu to Stereo. You may also access this setting by pressing the Audio Mode Button on the remote. If you leave the Analog Output setting at Multichannel, the DVD 48 will only output content specific to the front left and right channels through the 2-Channel Analog Audio Outputs, losing the center and surround channel information.

After you have connected the DVD 48 to your television, skip to Step Two for more information.

Connecting the DVD 48 to an Audio/Video Receiver

One of the major advantages of the DVD format is its ability to use a variety of digital audio formats for the ultimate in sonic performance. In addition, the DVD 48 is capable of playing DVD-Audio and SACD discs, which contain high-resolution multichannel audio materials. In order to benefit from these audio formats, we strongly recommend that you connect the DVD 48 to a 5.1-, 6.1- or 7.1-channel audio/video receiver with the ability to decode digital audio such as Dolby Digital and DTS, and with 5.1-channel "direct" analog audio inputs. Harman Kardon AVR Series receivers are compatible with the DVD 48.

The DVD 48 may also be used with an analog A/V receiver by connecting the 2-Channel Analog Audio Outputs to any one of the receiver's inputs (in addition to a video connection).

If your receiver is HDMI-capable, connect the DVD 48's HDMI Output to one of the receiver's HDMI inputs. See Figure 9. If the receiver is equipped with a DVI port, purchase an HDMI-to-DVI cable or adapter, and make a separate audio connection from the DVD 48 to the receiver.

Simplay HD The DVD 48 is Simplay HD-verified for compatibility via the HDMI connection with other Simplay HD-verified products.

Figure 9 (repeated) – HDMI Output

Check your receiver's owner's manual to determine how it handles HDMI signals. It may simply switch the signal, it may process the audio portion of the signal but not the video portion, or it may be capable of processing both the audio and video portions of the signal. If the receiver only switches the signal, but is not capable of accessing and processing the audio or video data, then a separate audio connection is required, as explained below.

If the receiver is *not* HDMI-capable, then separate audio and video connections are required. Select *one* of these types of video connections, in order of preference: component video, S-video, composite video. See Figure 10.

INSTALLATION

Figure 10 (repeated) – Component, S- and Composite Video Outputs

If your receiver is equipped with digital audio inputs, then select *either* a coaxial or optical digital audio input, and connect it to the corresponding output on the DVD 48. See Figure 12. This step also applies to a receiver that is only capable of HDMI switching and cannot process the audio portion of the HDMI signal. If your HDMI-capable receiver processes the HDMI audio, then do not make another digital audio connection.

Figure 12 – Coaxial and Optical Digital Audio Outputs

If you wish to enjoy SACD discs in their native lossless format, connect the DVD 48's 6-Channel Analog Audio Outputs to the corresponding 6-channel analog audio inputs on the receiver. This connection is necessary because the digital content is copy-protected and decoded by the DVD 48, with only the analog audio output available. If your receiver is not capable of processing the audio portion of an HDMI signal, use the 6-Channel Analog Audio Outputs to enjoy DVD-Audio discs, or change the DVD Audio mode setting in the GENERAL SETUP menu to DVD-Video to listen to any Dolby Digital, DTS or PCM materials that may be available on the disc (check the disc's jacket). See Figure 13.

Figure 13 – 6-Channel Analog Audio Outputs

NOTE: When using the 6-Channel Analog Audio Outputs, remember to adjust the Analog Output setting in the AUDIO SETUP menu to Multichannel for full 5.1-channel playback.

As explained in the Connections section, there may be several reasons for using the DVD 48's 2-channel Analog Audio Outputs in addition to the Digital Audio Outputs. If you wish to make recordings, to use the DVD 48 as an audio source for a multiroom system, to play 96kHz discs when your receiver is not capable of processing 96kHz audio, or if your receiver is not equipped with digital audio inputs, then connect the DVD 48's 2-Channel Analog Audio Outputs to any pair of analog audio inputs on the receiver. See Figure 11.

Figure 11 (repeated) – 2-Channel Analog Audio Outputs

Even if you connected one of the DVD 48's digital audio outputs to your receiver, you may wish to connect the 2-Channel Analog Audio Outputs to your TV (if it isn't HDMI-capable) so that you may watch a DVD without turning on your complete home theater system. If you make this connection, remember to also connect one of the DVD 48's video outputs directly to the TV.

Step Two – Plug In AC Power

Having made all of your wiring connections, it is now time to power up the DVD 48. Plug the AC Power cord into a working, unswitched AC outlet, and plug the female end into the receptacle on the DVD 48's rear panel. See Figure 14.

Figure 14 – AC Input for Power Cord

Step Three – Insert Batteries in Remote

The DVD 48 remote control uses two AAA batteries (included).

To remove the battery cover located on the back of the remote, firmly press the ridged area and slide the cover towards the bottom of the remote.

Insert the batteries as shown in Figure 15, making sure to observe the correct polarity.

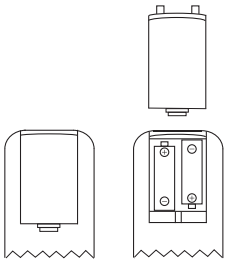


Figure 15 – Remote Battery Compartment

When using the remote, remember to point the lens toward the front panel of the DVD 48. Make sure no objects, such as furniture, are blocking the remote's path. Bright lights, fluorescent lights and plasma video displays may interfere with the remote's functioning. The remote has a range of about 20 feet, depending on the lighting conditions. It may be used at an angle of up to 30 degrees to either side of the DVD 48.

If the remote seems to operate intermittently, make sure the batteries have been inserted correctly, or replace all three batteries with fresh ones.

Step Four – Turn On the DVD 48

Plugging the DVD 48 into AC power places it in Standby mode, which is indicated by the Power Indicator (next to the Standby/On Switch) turning amber.

NOTE: When HDMI connections are used, turn on your television or video display before turning on the receiver and DVD 48.

There are several ways in which the DVD 48 may be turned on from Standby mode.

a) Press the Standby/On Switch on the front panel or remote. See Figure 16.

Figure 16 – Standby/On Switch

b) Press the Open/Close Button on the front panel or remote. See Figure 17.

Figure 17 – Open/Close Button

Pressing the Open/Close Button will also open the disc drawer.

c) Press the Play Button on the front panel or remote. If a disc is present, it will begin playing automatically. See Figure 18.

Figure 18 – Play Button

After customizing a few settings in the Initial Setup section, you may soon enjoy the finest in home entertainment.

TROUBLESHOOTING GUIDE

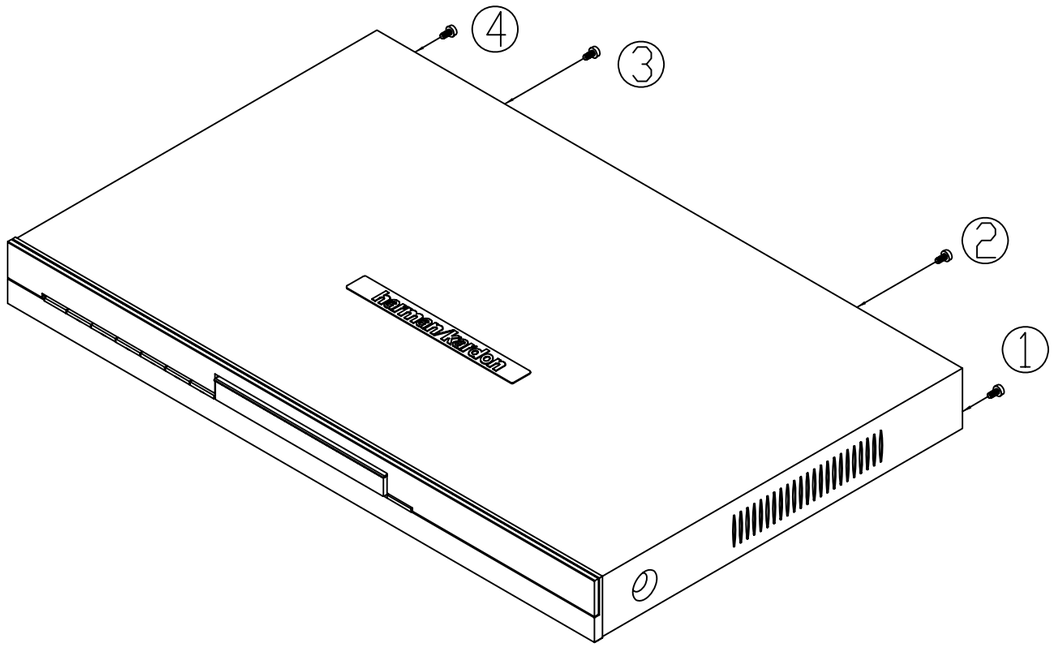
SYMPTOM	CAUSE	SOLUTION
Unit does not turn on	• No AC power	• Make certain AC power cord is plugged into a live outlet. • Check to see whether outlet is switch-controlled.
Unit does not respond to remote commands	• Weak batteries in remote • Remote sensor is obscured	• Change remote batteries and insert with correct polarity. • Make certain front panel sensor is in line of sight of remote or connect an optional remote sensor.
No picture	• Intermittent connections • Wrong input • Progressive Scan output selected	• Check all video connections. • Check input selection of TV or receiver. • Use Progressive Scan mode only with compatible TV. Reset to Interlaced Scan by following these steps: 1. Press the Open/Close Button on the front panel to open the disc drawer. 2. Press the Clear Button on the remote control. 3. Enter the numeric code "1211" on the remote. 4. Press the Audio Button (not Audio Mode). Or perform a system reset that will require you to reenter all user settings. Press and hold the Clear Button on the remote for 5 seconds. The display will blink, and all user settings will return to their factory defaults.
	• HDMI Output is connected to a video display that is not HDCP-compliant	• The HDMI Output may not be used with video displays that are not HDCP-compliant. Unplug the cable and select another audio and video connection.
	• Video Off feature active • Wrong HDMI output setting	• Press Video Off Button to reactivate video circuitry. • The HDMI and Component Video Outputs are not available simultaneously. Press the HDMI Button on the remote to turn the HDMI Output on or off. When the HDMI Output is on, the Component Video Outputs are deactivated, and vice versa.
Disc does not play	• Disc loaded improperly	• Load disc label-side up; align the disc with the guides and place it in its proper position.
	• Incorrect disc type	• Check to see that the disc is SACD, CD, CD-R, CD-RW, VCD, MP3, WMA, JPEG, DVD-R/RW, DVD+R/RW (standard-conforming), DVD-Audio or DVD-Video; other types will not play.
	• SA-CD Mode setting in CD mode for non-hybrid SACD disc	• Non-hybrid SACD discs are not recognized by the DVD 48. Change the SACD Mode setting in the GENERAL SETUP menu to SACD.
	• Invalid Region Code	• Use Region 1 or Open Region (0) disc only.
	• Rating is above parental control setting	• Enter password to override or change rating settings.
No sound	• Intermittent connections • Incorrect digital audio input selection • DVD disc is in fast or slow mode	• Check all audio connections. • Check digital audio settings on DVD 48 and on receiver. • There is no audio playback on DVD discs during fast or slow modes.
	• Surround receiver not compatible with 96kHz PCM audio	• Change LPCM Output setting in AUDIO SETUP menu to 48kHz.
	• SACD disc is loaded without using analog audio connection	• Use 6-Channel Audio Outputs or Analog Audio Outputs.
	• Wrong Analog Output setting in AUDIO SETUP menu	• In order to hear a downmixed 2-channel signal at the Analog Audio Outputs, make sure to change the Analog Output setting to Stereo, or press the Audio Mode Button to change the setting.
	• DVD-Audio disc is playing with DVD-Audio Mode setting in DVD-Video mode.	• Change DVD-Audio Mode setting in GENERAL SETUP menu to DVD-Audio.

TROUBLESHOOTING GUIDE

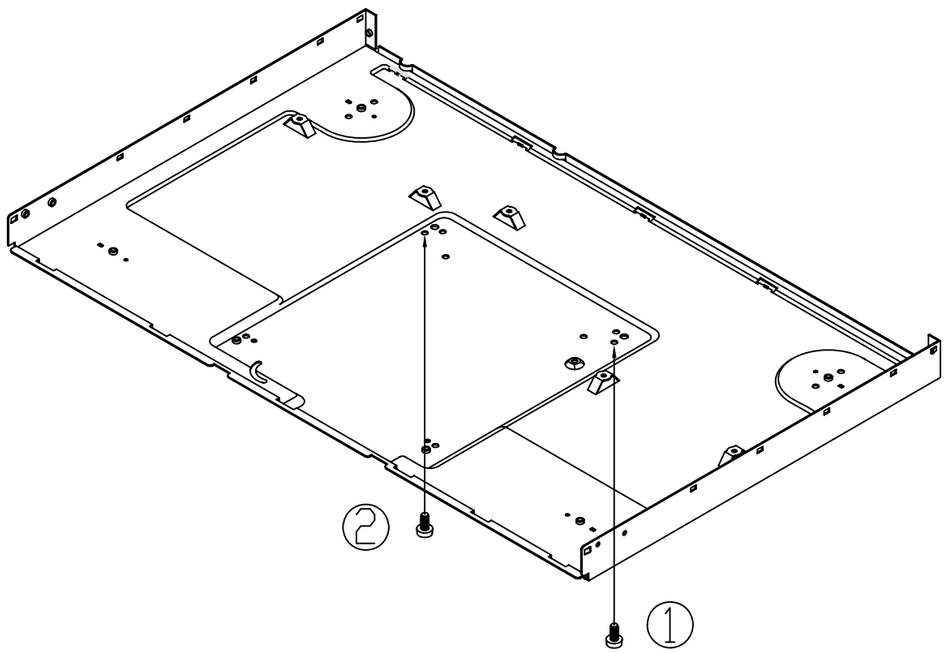
SYMPTOM	CAUSE	SOLUTION
Picture is distorted or jumps during fast forward or reverse play	• MPEG-2 decoding	• It is a normal artifact of DVD playback for pictures to jump or show some distortion during rapid play.
Unit turns off by itself	• Auto Power Off setting is active	• Check Auto Power Off setting in GENERAL SETUP menu.
Some remote buttons do not operate during DVD play; prohibited symbol Ø appears	• Function not permitted at this time	• With most discs, some functions are not permitted at certain times (e.g., Track Skip) or at all (e.g., direct audio track selection).
The OSD menu is in a foreign language	• Incorrect OSD language	• Change the display language selection in the GENERAL SETUP menu.
The Ø symbol appears	• Requested function not available at this time	• Certain functions may be disabled by the DVD itself during some passages of a disc.
Picture is displayed in the wrong aspect ratio	• Incorrect match of aspect-ratio settings to disc	• Change aspect-ratio settings.
Disc will not copy to VCR	• Copy protection	• Many DVDs are encoded with copy protection to prevent copying to VCR.
Password not accepted	• Incorrect password being used or password has been forgotten	• Factory default password “1211” always remains active.
Screen saver not activated	• Screen saver will not activate when on-screen menus are displayed	• Clear on-screen menus or press Video Off Button to avoid burn-in on plasma and CRT displays.
Cannot program playlist	• Programmed play is not available for all disc types • DVD 48 must be in Stop mode to program a playlist	• Programmed play is available only for CDs. • Stop play of disc before programming a playlist.

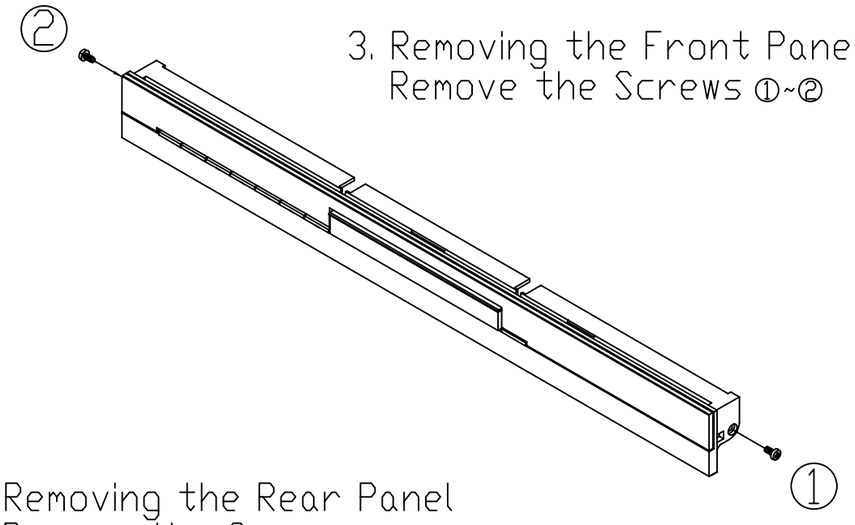
Additional information on troubleshooting possible problems with your DVD 48, or installation-related issues, may be found in the list of "Frequently Asked Questions" which is located in the Product Support section of our Web site at www.harmankardon.com.

1. Removing the Top Cabinet
Remove the Screws ①~④



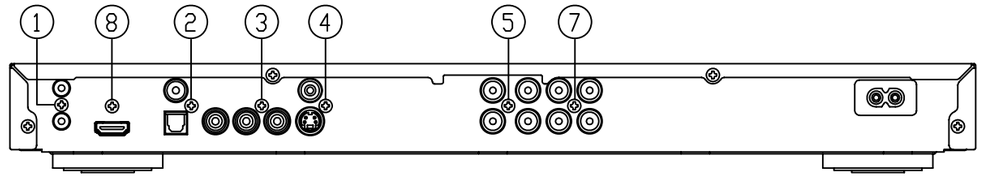
2. Removing the Bottom Chassis
Remove the Screws ①~②



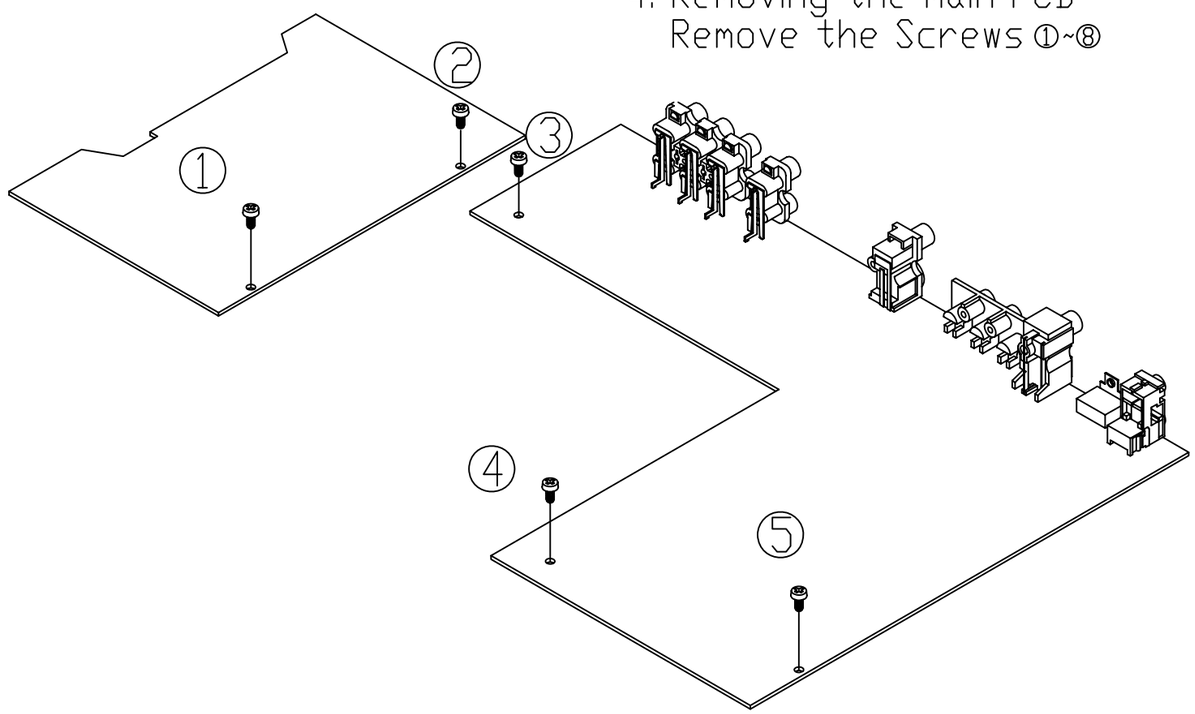


3. Removing the Front Panel
Remove the Screws ①~②

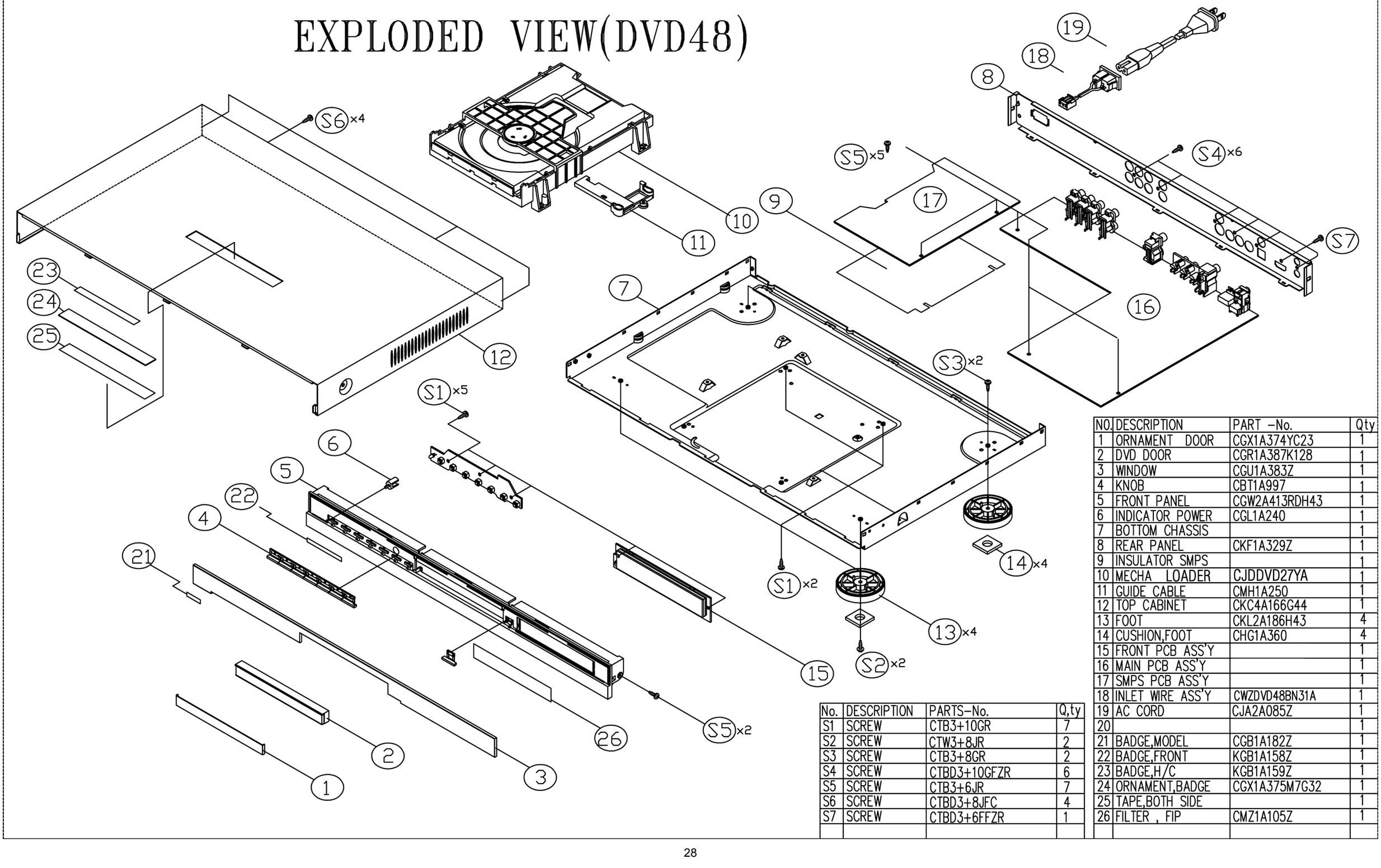
3. Removing the Rear Panel
Remove the Screws ①~㊳



4. Removing the Main PCB
Remove the Screws ①~⑧



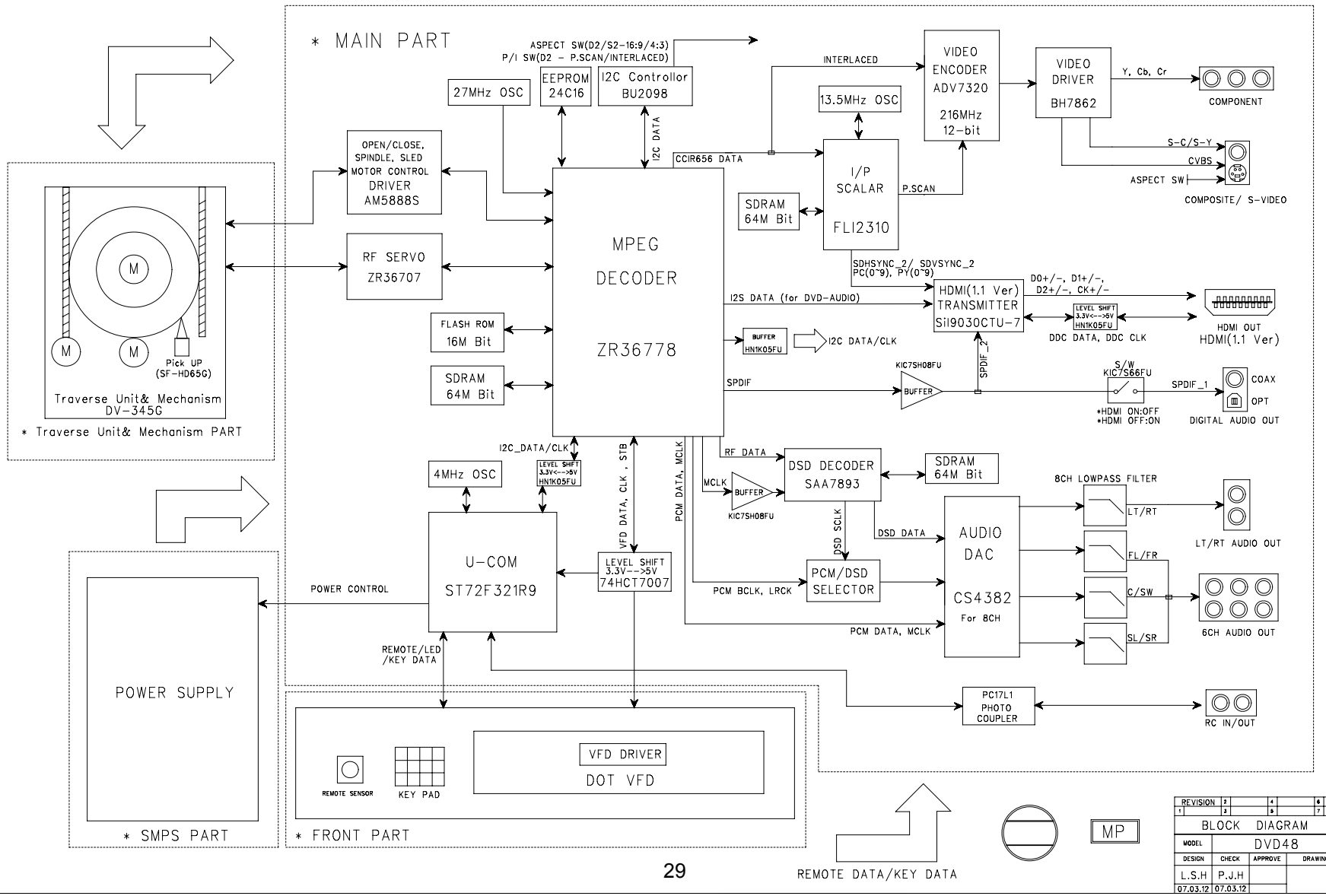
EXPLODED VIEW(DVD48)



No.	DESCRIPTION	PARTS-No.	Q,ty
S1	SCREW	CTB3+10GR	7
S2	SCREW	CTW3+8JR	2
S3	SCREW	CTB3+8GR	2
S4	SCREW	CTBD3+10GFZR	6
S5	SCREW	CTB3+6JR	7
S6	SCREW	CTBD3+8JFC	4
S7	SCREW	CTBD3+6FFZR	1

NO.	DESCRIPTION	PART -No.	Qty
1	ORNAMENT DOOR	CGX1A374YC23	1
2	DVD DOOR	CGR1A387K128	1
3	WINDOW	CGU1A383Z	1
4	KNOB	CBT1A997	1
5	FRONT PANEL	CGW2A413RDH43	1
6	INDICATOR POWER	CGL1A240	1
7	BOTTOM CHASSIS		1
8	REAR PANEL	CKF1A329Z	1
9	INSULATOR SMPS		1
10	MECHA LOADER	CJDDVD27YA	1
11	GUIDE CABLE	CMH1A250	1
12	TOP CABINET	CKC4A166G44	1
13	FOOT	CKL2A186H43	4
14	CUSHION,FOOT	CHG1A360	4
15	FRONT PCB ASS'Y		1
16	MAIN PCB ASS'Y		1
17	SMPS PCB ASS'Y		1
18	INLET WIRE ASS'Y	CWZDVD48BN31A	1
19	AC CORD	CJA2A085Z	1
20			1
21	BADGE,MODEL	CGB1A182Z	1
22	BADGE,FRONT	KGB1A158Z	1
23	BADGE,H/C	KGB1A159Z	1
24	ORNAMENT,BADGE	CGX1A375M7G32	1
25	TAPE,BOTH SIDE		1
26	FILTER , FIP	CMZ1A105Z	1

BLOCK DIAGRAM



REVISION					
BLOCK DIAGRAM					
MODEL	DVD48				
DESIGN	CHECK	APPROVE	DRAWING NO		
L.S.H	P.J.H				
07.03.12	07.03.12				

DVD48 Electrical Parts List					
Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
Capacitors					
C105	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C110	CCUS1H330JA	CAP , CHIP	33PF JA 1608	1	EA
C115	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C116	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C123	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C125	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C126	CCUS1H562KC	CAP , CHIP CERAMIC(1608, 5600p	5600PF KC 1608	1	EA
C128	CCUS1H562KC	CAP , CHIP CERAMIC(1608, 5600p	5600PF KC 1608	1	EA
C130	CCUS1H471JA	CAP , CHIP	470PF JA 1608	1	EA
C131	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C132	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C133	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C134	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C135	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C136	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C140	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C147	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C156	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
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C160	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C161	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C162	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C163	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C164	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C165	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C170	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C183	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C184	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
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C214	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C215	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C216	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C217	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
C218	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C219	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C220	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C222	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C224	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C248	CCSJB1A220B	CAP , CHIP TANTAL(B TYPE, 22uF	22UF/50V	1	EA
C249	CCSJB1A220B	CAP , CHIP TANTAL(B TYPE, 22uF	22UF/50V	1	EA
C251	CCSJB1A220B	CAP , CHIP TANTAL(B TYPE, 22uF	22UF/50V	1	EA
C269	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C279	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C280	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C281	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C282	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C283	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C284	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C285	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C286	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C401	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C403	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C461	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C462	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C506	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C507	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C508	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C522	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C533	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C586	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C601	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C602	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C603	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C604	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C607	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C609	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C610	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C611	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C612	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C613	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C614	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C615	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C616	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C618	CCUS1H103KC	CAP , CHIP	0.01UF ZF 1608	1	EA
C619	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C620	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C621	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C626	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C627	CCUS1H103KC	CAP , CHIP	0.01UF ZF 1608	1	EA
C630	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C631	CCUS1H103KC	CAP , CHIP	0.01UF ZF 1608	1	EA
C632	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C633	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C634	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C635	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C636	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C637	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C639	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C640	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C641	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C642	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C643	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C644	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C803	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
C805	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C904	CCSJA0J220B	CAP , CHIP TANTAL(A TYPE, 22uF	22UF/50V	1	EA
C905	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C906	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C907	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C908	CCSJA0J220B	CAP , CHIP TANTAL(A TYPE, 22uF	22UF/50V	1	EA
C911	CCSJA0J220B	CAP , CHIP TANTAL(A TYPE, 22uF	22UF/50V	1	EA
C912	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C913	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C914	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C915	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C916	CCSJA0J220B	CAP , CHIP TANTAL(A TYPE, 22uF	22UF/50V	1	EA
C918	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C919	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C101	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C102	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C103	CCUS1H560JA	CAP , CHIP	56PF JA 1608	1	EA
C104	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C106	CCUS1H222KC	CAP , CHIP	2200PF KC 1608	1	EA
C107	CCUS1H222KC	CAP , CHIP	2200PF KC 1608	1	EA
C108	CCUS1H222KC	CAP , CHIP	2200PF KC 1608	1	EA
C109	CCUS1H222KC	CAP , CHIP	2200PF KC 1608	1	EA
C111	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C112	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C113	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C114	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C117	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C118	CCUS1H682KC	CAP , CHIP	6800PF KB 1608	1	EA
C119	CCUS1H223KC	CAP , CHIP	0.022UF KC 1608	1	EA
C120	CCUS1H221JA	CAP , CHIP	220PF JA 1608	1	EA
C121	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C122	CCUS1H272KC	CAP , CHIP	270PF JA 1608	1	EA
C124	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C127	CCUS1H562KC	CAP , CHIP CERAMIC(1608, 5600p	0.1UF ZF 1608	1	EA
C137	CRJ10DJ0R0T	RES , CHIP	0.1UF ZF 1608	1	EA
C138	CCUS1H102KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C139	CCUS1H102KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C141	CCUS1E333KC	CAP , CHIP CERAMIC(1608)	0.1UF ZF 1608	1	EA
C142	CCUS1H102KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C143	CCUS1H102KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C144	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C145	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C146	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C148	CCUS1H272KC	CAP , CHIP	270PF JA 1608	1	EA
C149	CCUS1H273KC	CAP , CHIP	0.027UF KC 1608	1	EA
C150	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C151	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C152	CCUS1H273KC	CAP , CHIP	0.027UF KC 1608	1	EA
C153	CCUS1H561JA	CAP , CHIP	560PF JA 1608	1	EA
C154	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C155	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C166	CCUS1H7R0DT	CAP , CHIP CERAMIC(1608, 7p)	7PF D 1608	1	EA
C169	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C174	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C175	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C176	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C177	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C178	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C205	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C206	CCUS1H103KC	CAP , CHIP	0.01UF ZF 1608	1	EA
C207	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
C223	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C226	CCUS1H150JA	CAP , CHIP(15PF/50V)	15PF JA 1608	1	EA
C227	CCUS1H150JA	CAP , CHIP(15PF/50V)	15PF JA 1608	1	EA
C228	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C229	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C230	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C231	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C232	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C233	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C234	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C273	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C275	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C277	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C287	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C289	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C405	CCUS1H150JA	CAP , CHIP(15PF/50V)	15PF JA 1608	1	EA
C406	CCUS1H150JA	CAP , CHIP(15PF/50V)	15PF JA 1608	1	EA
C410	CCUS1H151JA	CAP , CHIP	150PF JA 1608	1	EA
C502	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C504	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C505	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C510	CCUS1H101JA	CAP , CHIP	0.1UF ZF 1608	1	EA
C511	CCUS1H821JA	CAP , CHIP	820PF JA 1608	1	EA
C512	CCUS1H392KC	CAP , CHIP CERAMIC(1608, 3900p	390PF KC 1608	1	EA
C513	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C514	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C515	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C516	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C518	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C519	CCUS1A105KC	CAP , CHIP	1UF ZF 1608	1	EA
C521	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C524	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C525	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C526	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C527	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C529	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C530	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C531	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C534	CCUS1H560JA	CAP , CHIP	0.1UF ZF 1608	1	EA
C535	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C538	CCUS1H220JA	CAP , CHIP	22PF JA 1608	1	EA
C547	CCUS1H560JA	CAP , CHIP	56PF JA 1608	1	EA
C550	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C552	CCUS1H470JA	CAP , CHIP	47PF JA 1608	1	EA
C553	CCUS1H470JA	CAP , CHIP	47PF JA 1608	1	EA
C554	CCUS1H470JA	CAP , CHIP	47PF JA 1608	1	EA
C555	CCUS1H470JA	CAP , CHIP	47PF JA 1608	1	EA
C556	CCUS1H470JA	CAP , CHIP	47PF JA 1608	1	EA
C557	CCUS1H470JA	CAP , CHIP	47PF JA 1608	1	EA
C574	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C576	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C579	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C605	CCUS1H103KC	CAP , CHIP	0.01UF ZF 1608	1	EA
C608	CCUS1H103KC	CAP , CHIP	0.01UF ZF 1608	1	EA
C622	CCUS1H180JA	CAP , CHIP(18PF/50V)	18PF JA 1608	1	EA
C623	CCUS1H180JA	CAP , CHIP(18PF/50V)	18PF JA 1608	1	EA
C646	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C648	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C649	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C654	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C655	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
C658	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C659	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C662	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C663	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C665	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C701	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C702	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C703	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C704	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C706	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C708	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C801	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C806	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C808	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C811	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C814	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C815	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C817	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C821	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C822	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C823	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C828	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C829	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C832	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C835	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C836	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C837	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C842	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C843	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C846	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C849	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C850	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C851	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C856	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C857	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C860	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C863	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C864	CCUS1H391JA	CAP , CHIP	390PF JA 1608	1	EA
C865	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C868	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C869	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C870	CCUS1H221JA	CAP , CHIP	220PF JA 1608	1	EA
C871	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C872	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C874	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C876	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C878	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C879	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C882	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C884	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C886	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C888	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C898	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C900	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C902	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C903	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C909	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C910	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C917	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C920	CCUS1H102KC	CAP , CHIP	1000PF KC 1608	1	EA
C923	CCSJA1C100B	CAP , CHIP TANTAL(A TYPE, 10uF	10UF/16V	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
C924	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C925	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C926	CCSJA1C100B	CAP , CHIP TANTAL(A TYPE, 10uF	10UF/16V	1	EA
C927	CCSJA1C100B	CAP , CHIP TANTAL(A TYPE, 10uF	10UF/16V	1	EA
C928	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C929	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C930	CCSJA1C100B	CAP , CHIP TANTAL(A TYPE, 10uF	10UF/16V	1	EA
C931	CCSJA1C100B	CAP , CHIP TANTAL(A TYPE, 10uF	10UF/16V	1	EA
C932	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C933	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C934	CCSJA0J220B	CAP , CHIP TANTAL(A TYPE, 22uF	22UF/50V	1	EA
C935	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C936	CCSJA0J220B	CAP , CHIP TANTAL(A TYPE, 22uF	22UF/50V	1	EA
C937	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C938	CCSJA0J220B	CAP , CHIP TANTAL(A TYPE, 22uF	22UF/50V	1	EA
C948	CCSJA1C100B	CAP , CHIP TANTAL(A TYPE, 10uF	10UF/16V	1	EA
C949	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C950	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C951	CCSJA0J220B	CAP , CHIP TANTAL(A TYPE, 22uF	22UF/50V	1	EA
C952	CCSJA0J220B	CAP , CHIP TANTAL(A TYPE, 22uF	22UF/50V	1	EA
C991	CCUS1H104KC	CAP , CHIP	0.1UF ZF 1608	1	EA
C992	CCSJA0J220B	CAP , CHIP TANTAL(A TYPE, 22uF	22UF/50V	1	EA
C235	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C237	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C238	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C239	CCEA1HH4R7T	CAP , ELECT	4.7UF 50V	1	EA
C240	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C241	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C242	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C243	CCEA1EH221T	CAP , ELECT	220UF 25V	1	EA
C244	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C245	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C246	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C247	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C250	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C252	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C253	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C254	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C255	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C256	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C257	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C258	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C259	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C260	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C261	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C262	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C263	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C264	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C265	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C266	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C267	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C268	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C270	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C271	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C272	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C274	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C276	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C278	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C288	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C402	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C407	CCEA1HH1R0T	CAP , ELECT	1UF 50V	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
C408	CCEA1HH100T	CAP , ELECT	10UF 50V	1	EA
C409	CCEA1HH4R7T	CAP , ELECT	4.7UF 50V	1	EA
C501	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C503	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C517	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C523	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C528	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C532	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C536	CCEA1HH1R0T	CAP , ELECT	1UF 50V	1	EA
C537	CCEA1HH1R0T	CAP , ELECT	1UF 50V	1	EA
C539	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C540	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C541	CCEA1AH331T	CAP , ELECT	330UF 10V	1	EA
C542	CCEA1AH331T	CAP , ELECT	330UF 10V	1	EA
C543	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C544	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C545	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C546	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C548	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C549	CCEA1AH331T	CAP , ELECT	330UF 10V	1	EA
C573	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C577	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C578	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C606	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C617	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C624	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C625	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C628	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C629	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C638	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C645	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C647	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C650	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C653	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C656	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C660	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C661	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C664	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C666	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C667	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C707	CCEA1CKS470T	CAP , ELECT	47UF 16V	1	EA
C802	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C804	CCEA1HH100T	CAP , ELECT	10UF 50V	1	EA
C807	CCEA1EH470T	CAP , ELECT	47UF 25V	1	EA
C809	CCEA1HH1R0T	CAP , ELECT	1UF 50V	1	EA
C810	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C812	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C813	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C816	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C818	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C819	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C820	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C824	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C825	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C826	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C827	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C830	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C831	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C833	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C834	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C838	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
C839	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C840	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C841	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C844	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C845	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C847	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C848	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C852	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C853	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C854	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C855	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C858	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C859	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C861	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C862	HCQI1H222JZT	CAP , MYLAR	2200UF 50V J	1	EA
C866	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C867	CCEA1HH220T	CAP , ELECT	22UF 50V	1	EA
C873	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C875	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C877	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C880	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C881	CCEA1EH221T	CAP , ELECT	220UF 25V	1	EA
C883	CCEA1EH221T	CAP , ELECT	220UF 25V	1	EA
C885	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C887	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C895	CCEA1CH221T	CAP , ELECT	220UF 16V	1	EA
C896	CCEA1HH0R1T	CAP , ELECT	0.1UF 50V	1	EA
C897	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C901	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
C922	CCEA1CH101T	CAP , ELECT	100UF 16V	1	EA
Semiconductors					
D101	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D102	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D401	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D402	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D403	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D802	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D803	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
D804	HVDRLS4148SR	DIODE, SWITCHING, SMD TYPE	RLS4148 TE-11	1	EA
IC11	HVIZR36778	IC,MPEG (ZORAN)	ZR36778	1	EA
IC12	HVIM29W160ET70N	IC,16M FLASH (ST)	M29W160ET-70N6	1	EA
IC13	HVIM12L64164A7T	IC, 64M SDRAM (4X16)	M12L64164A7	1	EA
IC14	CVIBR24L16FWE2	EEPROM 16K BR24L16F-WE2	BR24L16F-WE2	1	EA
IC15	HVIKIC7SH08FU	HIGH SPEED 2 INPUT AND GATE (U	KIC7SHO8FU-RTK	1	EA
IC16	HVTHN1K05FU	MOS FET	HN1K05FU	1	EA
IC17	HVIZR36707	IC,RF (ZORAN)	ZR36707	1	EA
IC18	HVIAM5888SLF	I. C , Motor Driver (AMtek,Pb free)	AM5888S L/F	1	EA
IC19	HVITL3472IDR	IC, DUAL OP AMP 8-SOIC (TI)	TL3472IDR	1	EA
IC20	HVISAA7893HLC2	IC,DSD DECODER (Philips)	SAA7893HL/C2 (PB FRE	1	EA
IC21	HVIM12L64164A7T	IC, 64M SDRAM (4X16)	M12L64164A7	1	EA
IC22	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	1117S-3.3V	1	EA
IC23	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	1117S-3.3V	1	EA
IC24	BVIBA18BC0FP	REGULATOR ,CHIP (1.8V)	BA18BC0FP-E2	1	EA
IC25	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	1117S-3.3V	1	EA
IC26	BVIBA50BC0FP	I.C , REGULATOR CHIP (+5V)	BA50BC0FP-E2	1	EA
IC27	HVIKIC7SH08FU	HIGH SPEED 2 INPUT AND GATE (U	KIC7SHO8FU-RTK	1	EA
IC28	HVIKIC7S66FU	SWITCH IC (USV PACKAGE)	KIC7S66FU-RTK/3	1	EA
IC41	CVIST72F321BR9T6	I.C , FLASH U-COM	ST72F321B9T6	1	EA
IC43	HVTHN1K05FU	MOS FET	HN1K05FU	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
IC51	CVIADV7320KSTZ	I.C , VIDEO ENCODER	ADV7320	1	EA
IC52	BVIBH7862FS	IC , 6CH VIDEO DRIVER	ROHM (BH7862FS)	1	EA
IC54	HVIBU2098F	IC , I2C BUS	ROHM (BU2098F)	1	EA
IC55	HVITC74HCT7007F	I.C HEX BUFFER	TC74HC7007AFEL	1	EA
IC56	BVIBA50BC0FP	I.C , REGULATOR CHIP (+5V)	BA50BC0FP-E2	1	EA
IC61	CVIFLI2310LFCF	I/P CONVERTER, FLI2310-LF-CF	FLI2310-LF-CF	1	EA
IC62	CVI57V643220TP6	64M SDRAM, 6nS,86P TSOP II	HY57V643220B 6NS	1	EA
IC63	HVISN74AHC541PW	OCTAL BUFFERS IC(TSSOP-20 PKG)	SN74AHC541PWR	1	EA
IC64	HVILM1117S-2V5	I.C , REGULATOR (2.5V)	1117S-2.5	1	EA
IC65	BVIBA18BC0FP	REGULATOR ,CHIP (1.8V)	BA18BC0FP-E2	1	EA
IC66	HVITA48033FTE16	I.C , REGULATOR (3.3V)	TA48033FTE16	1	EA
IC67	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	1117S-3.3V	1	EA
IC78	HVIKIC7SH08FU	HIGH SPEED 2 INPUT AND GATE (U	KIC7SHO8FU-RTK	1	EA
IC81	HVICS4382-KQ	I.C , DAC	CS4382-KQ	1	EA
IC82	HVINJM2068MDTE1	I.C , DUAL OP AMP	NJM2068MD-TE1	1	EA
IC83	HVINJM2068MDTE1	I.C , DUAL OP AMP	NJM2068MD-TE1	1	EA
IC84	HVINJM2068MDTE1	I.C , DUAL OP AMP	NJM2068MD-TE1	1	EA
IC85	HVINJM2068MDTE1	I.C , DUAL OP AMP	NJM2068MD-TE1	1	EA
IC86	HVI74LVC157ADBR	I.C , MULTIPLEXER	SN74LVC157A	1	EA
IC87	HVIKIC7S66FU	SWITCH IC (USV PACKAGE)	KIC7S66FU-RTK/3	1	EA
IC88	HVILM1117S-5.0	IC REGULATOR/SOT-223	LM1117S-5V	1	EA
IC89	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	LM1117S-3.3V	1	EA
IC90	HVIKIC7SH08FU	HIGH SPEED 2 INPUT AND GATE (U	KIC7SHO8FU-RTK	1	EA
IC91	CVISII9030CTU7	I.C , HDMI TX	SII9030CTU7	1	EA
IC92	HVILM1117S-5.0	IC REGULATOR/SOT-223	LM1117S-5V	1	EA
IC93	HVILM1117S-1V8	I.C , REGULATOR (1.8V)	LM1117-1V8	1	EA
IC94	HVILM1117S-3V3	I.C , REGULATOR (3.3V)	LM1117S-3.3V	1	EA
IC95	HVIKIC7SH08FU	HIGH SPEED 2 INPUT AND GATE (U	KIC7SHO8FU-RTK	1	EA
IC96	HVTHN1K02FUTE85	TR , MOS FET (S-MOS)	HN1K02FU-TE85L	1	EA
IC97	HVIKIC7SH08FU	HIGH SPEED 2 INPUT AND GATE (U	KIC7SHO8FU-RTK	1	EA
IC98	HVIKIC7SZ08FU	I.C ,INPUT AND GATE (USV PACKA	KIC7SZ08FU-RTK	1	EA
Q101	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1	EA
Q102	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1	EA
Q103	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1	EA
Q104	HVTKTA1664YP	TRANSISTOR PNP	KTA1664YP	1	EA
Q105	HVTKTA1664YP	TRANSISTOR PNP	KTA1664YP	1	EA
Q401	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1	EA
Q402	HVTKTA1504SYRTK	TRANSISTOR , CHIP	KTA1504S Y RTK	1	EA
Q403	HVTKTC3875SYRTK	TRANSISTOR , CHIP	KTC3875S Y RTK	1	EA
Q501	HVTKTA2014GR	TRANSISTOR, SMD	KTA2014	1	EA
Q502	HVTKTA2014GR	TRANSISTOR, SMD	KTA2014	1	EA
Q503	HVTKTA2014GR	TRANSISTOR, SMD	KTA2014	1	EA
Q504	HVTKTA2014GR	TRANSISTOR, SMD	KTA2014	1	EA
Q505	HVTKTA2014GR	TRANSISTOR, SMD	KTA2014	1	EA
Q604	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
Q701	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
Q702	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1	EA
Q801	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1	EA
Q802	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
Q803	HVTKRC107S	TRANSISTOR , CHIP	KRC107S	1	EA
Q804	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
Q805	HVTKRA107ST	TRANSISTOR , CHIP	KRA107S	1	EA
Q807	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q808	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q809	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q810	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q811	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q812	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q813	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q814	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q815	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
Q816	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q817	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q818	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q819	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q820	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q821	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q822	HVTKTD1304T	TRANSISTOR , CHIP (MUTE)	KTD1304	1	EA
Q823	HVT2N3904SP	TRANSISTOR, CHIP (KEC)	2N3904S-RTK/PS	1	EA
D106	CVD1N4003SRT	RECT , DIODE	1N4003	1	EA
D107	CVD1N4003SRT	RECT , DIODE	1N4003	1	EA
D701	CVD50BOBBWGA	L.E.D , 2 COLOR (ORG , BLUE)	TOL-50BOBBWGA	1	EA
Q806	HVTKSA916YT	TRANSISTOR PNP	KSA916Y	1	EA
IC46	HVIPC17L1CB	I.C , PHOTO COUPLER	PC17L1CB	1	EA
IC71	HRVKSM603TH2A	SENSOR , REMOCON	KSM-603TH2A	1	EA
IC79	HVIKIA7809API	IC , REGULATOR (+9V)	KIA7809 (KEC)	1	EA
IC80	HVIKIA7909PI	IC , REGULATOR (-9V)	KIA7909 (KEC)	1	EA
Resistors					
RN01	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN02	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN03	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN04	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN05	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN06	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN07	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN08	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN09	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN11	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN12	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN15	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN16	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN17	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN18	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN19	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN20	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN21	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN22	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN23	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN24	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN25	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN51	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN52	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN53	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN54	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN55	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN56	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN57	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN61	CRJ104DJ103T	RES, ARRAY, 10K (1608)	10K(1608)	1	EA
RN62	CRJ104DJ103T	RES, ARRAY, 10K (1608)	10K(1608)	1	EA
RN63	CRJ104DJ103T	RES, ARRAY, 10K (1608)	10K(1608)	1	EA
RN64	CRJ104DJ103T	RES, ARRAY, 10K (1608)	10K(1608)	1	EA
RN65	CRJ104DJ103T	RES, ARRAY, 10K (1608)	10K(1608)	1	EA
RN66	CRJ104DJ103T	RES, ARRAY, 10K (1608)	10K(1608)	1	EA
RN67	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN68	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN69	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN70	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN71	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN72	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN73	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
RN91	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN92	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN93	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
RN94	CRJ104DJ330T	RES , 4ARRAY (1608*4)	33 OHM/1608*4	1	EA
R101	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R102	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R103	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R104	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R105	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R106	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R107	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R108	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R109	CRJ10DJ113T	RES , CHIP	11K OHM 1608 SIZE	1	EA
R110	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R111	CRJ10DJ105T	RES , CHIP	1M OHM 1608 SIZE	1	EA
R112	CRJ10DJ223T	RES , CHIP	22K OHM 1608 SIZE	1	EA
R113	CRJ10DJ223T	RES , CHIP	22K OHM 1608 SIZE	1	EA
R114	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R115	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE	1	EA
R116	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE	1	EA
R117	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE	1	EA
R118	CRJ10DJ622T	RES , CHIP	6.2K OHM 1608 SIZE	1	EA
R119	CRJ10DJ113T	RES , CHIP	11K OHM 1608 SIZE	1	EA
R120	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R121	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R122	CRJ10DJ113T	RES , CHIP	11K OHM 1608 SIZE	1	EA
R123	CRJ10DJ273T	RES , CHIP	27K OHM 1608 SIZE	1	EA
R124	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE	1	EA
R125	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE	1	EA
R126	CRJ10DJ562T	RES , CHIP	5.6K OHM 1608 SIZE	1	EA
R127	CRJ10DF4700T	RES, CHIP 470 OHM/1608/1%	470 OHM(1%) 1608 SIZE	1	EA
R128	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R129	CRJ10DF4700T	RES, CHIP 470 OHM/1608/1%	470 OHM(1%) 1608 SIZE	1	EA
R131	CRJ10DF1002T	RES , CHIP 1%	10K /1/10W/F	1	EA
R132	CRJ10DF1002T	RES , CHIP 1%	10K /1/10W/F	1	EA
R133	CRJ10DF1002T	RES , CHIP 1%	10K /1/10W/F	1	EA
R134	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R135	CRJ10DJ100T	RES , CHIP	10 OHM 1608 SIZE	1	EA
R136	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R137	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R138	CRJ10DJ100T	RES , CHIP	10 OHM 1608 SIZE	1	EA
R139	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R140	CRJ10DJ133T	RES , CHIP	13K OHM 1608 SIZE	1	EA
R142	CRJ10DJ474T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R143	HLZ9R005Z	BEAD CHIP 60(1608 SIZE)	HH-1M1608-600	1	EA
R145	CRJ10DJ912T	RES , CHIP	9.1K OHM/1608	1	EA
R146	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R147	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R148	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R149	CRJ10DJ272T	RES , CHIP	2.7K OHM 1608 SIZE	1	EA
R151	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R152	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R153	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R155	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R156	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R157	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R159	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R160	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R161	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R162	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R163	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
R164	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE	1	EA
R166	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R167	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R168	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R169	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R170	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R171	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R174	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R175	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R176	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R177	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R178	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R179	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R180	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R181	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R182	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE	1	EA
R183	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE	1	EA
R184	CRJ10DJ471T	RES , CHIP	470 OHM 1608 SIZE	1	EA
R185	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R186	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R187	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R188	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R189	CRJ10DF39R0T	CHIP RES, 1% 39 Ohm	39 OHM(1%) 1608 SIZE	1	EA
R193	CRJ10DF3920T	RES. CHIP (392R 1%)	39 OHM(1%) 1608 SIZE	1	EA
R194	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R195	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R196	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE	1	EA
R197	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE	1	EA
R198	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE	1	EA
R199	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE	1	EA
R201	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R202	CRJ10DJ123T	RES , CHIP	12K OHM 1608 SIZE	1	EA
R203	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R204	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE	1	EA
R205	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R206	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R207	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R208	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R209	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R210	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R211	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R212	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R213	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R214	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE	1	EA
R216	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R217	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R218	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R219	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R220	HLZ9R005Z	BEAD CHIP 60(1608 SIZE)	HH-1M1608-600	1	EA
R221	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R222	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R223	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R293	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R294	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R298	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R299	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R402	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R404	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R405	CRJ10DJ220T	RES , CHIP	22 OHM 1608 SIZE	1	EA
R407	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE	1	EA
R409	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
R410	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE	1	EA
R411	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R412	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R413	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R414	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R415	CRJ10DJ105T	RES , CHIP	1M OHM 1608 SIZE	1	EA
R416	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R417	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R418	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R423	CRJ10DJ220T	RES , CHIP	22 OHM 1608 SIZE	1	EA
R424	CRJ10DJ220T	RES , CHIP	22 OHM 1608 SIZE	1	EA
R425	CRJ10DJ100T	RES , CHIP	10 OHM 1608 SIZE	1	EA
R426	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R427	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R428	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R429	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R430	CRJ10DJ473T	RES , CHIP	47K OHM 1608 SIZE	1	EA
R431	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R432	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R434	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R471	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R501	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R503	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R504	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R506	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R507	HLZ9R005Z	BEAD CHIP 60(1608 SIZE)	HH-1M1608-600	1	EA
R508	CRJ10DJ391T	RES , CHIP	390 OHM 1608 SIZE	1	EA
R509	CRJ10DJ272T	RES , CHIP	2.7K OHM 1608 SIZE	1	EA
R510	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R511	CRJ10DJ681T	RES , CHIP	680 OHM 1608 SIZE	1	EA
R512	CRJ10DJ682T	RES , CHIP	6.8K OHM 1608 SIZE	1	EA
R513	CRJ10DJ682T	RES , CHIP	6.8K OHM 1608 SIZE	1	EA
R515	CRJ10DJ272T	RES , CHIP	2.7K OHM 1608 SIZE	1	EA
R516	CRJ10DJ391T	RES , CHIP	390 OHM 1608 SIZE	1	EA
R519	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R520	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R521	CRJ10DJ681T	RES , CHIP	680 OHM 1608 SIZE	1	EA
R522	CRJ10DJ561T	RES , CHIP	560 OHM 1608 SIZE	1	EA
R523	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R524	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R525	CRJ10DJ681T	RES , CHIP	680 OHM 1608 SIZE	1	EA
R526	CRJ10DJ561T	RES , CHIP	560 OHM 1608 SIZE	1	EA
R527	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R528	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R529	CRJ10DJ681T	RES , CHIP	680 OHM 1608 SIZE	1	EA
R530	CRJ10DJ561T	RES , CHIP	560 OHM 1608 SIZE	1	EA
R531	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R532	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R533	CRJ10DJ681T	RES , CHIP	680 OHM 1608 SIZE	1	EA
R534	CRJ10DJ561T	RES , CHIP	560 OHM 1608 SIZE	1	EA
R535	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R536	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R537	CRJ10DJ681T	RES , CHIP	680 OHM 1608 SIZE	1	EA
R538	CRJ10DJ561T	RES , CHIP	560 OHM 1608 SIZE	1	EA
R541	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R544	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R545	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE	1	EA
R546	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE	1	EA
R547	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE	1	EA
R548	CRJ10DJ820T	RES , CHIP	82 OHM 1608 SIZE	1	EA
R549	CRJ10DJ820T	RES , CHIP	82 OHM 1608 SIZE	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
R551	CRJ10DJ820T	RES , CHIP	82 OHM 1608 SIZE	1	EA
R575	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R576	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R577	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R578	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R579	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R580	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R581	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R582	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R583	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R584	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R585	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R586	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R587	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R589	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R590	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R592	CRJ10DJ220T	RES , CHIP	22 OHM 1608 SIZE	1	EA
R593	CRJ10DJ220T	RES , CHIP	22 OHM 1608 SIZE	1	EA
R596	CRJ10DJ271T	RES , CHIP	270 OHM 1608 SIZE	1	EA
R597	CRJ10DJ473T	RES , CHIP	47K OHM 1608 SIZE	1	EA
R598	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R599	CRJ10DJ470T	RES , CHIP	47 OHM 1608 SIZE	1	EA
R601	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R602	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R603	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R604	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R605	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R606	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R607	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R608	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R609	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R610	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R611	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R612	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R613	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R620	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R621	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R623	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R624	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R625	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R626	CRJ10DJ105T	RES , CHIP	1M OHM 1608 SIZE	1	EA
R627	HLZ9R005Z	BEAD CHIP 60(1608 SIZE)	HH-1M1608-600	1	EA
R628	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R629	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R631	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R632	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R635	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R636	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R637	CRJ10DJ471T	RES , CHIP	470 OHM 1608 SIZE	1	EA
R639	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R644	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R645	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R647	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R650	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R651	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R652	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R655	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R656	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R701	CRJ10DJ333T	RES , CHIP	33K OHM 1608 SIZE	1	EA
R702	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R703	CRJ10DJ681T	RES , CHIP	680 OHM 1608 SIZE	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
R704	CRJ10DJ821T	RES , CHIP	820 OHM 1608 SIZE	1	EA
R705	CRJ10DJ122T	RES , CHIP	1.2K OHM 1608 SIZE	1	EA
R706	CRJ10DJ152T	RES , CHIP	1.5K OHM 1608 SIZE	1	EA
R707	CRJ10DJ222T	RES , CHIP	2.2K OHM 1608 SIZE	1	EA
R708	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R709	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R710	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R711	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R712	CRJ10DJ100T	RES , CHIP	10 OHM 1608 SIZE	1	EA
R713	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R750	CRJ10DJ750T	RES , CHIP	75 OHM 1608 SIZE	1	EA
R751	CRJ10DJ680T	RES , CHIP	68 OHM 1608 SIZE	1	EA
R752	CRJ10DJ121T	RES , CHIP	120 OHM 1608 SIZE	1	EA
R753	CRJ10DJ820T	RES , CHIP	82 OHM 1608 SIZE	1	EA
R754	CRJ10DJ4R7T	RES , CHIP	4.7 OHM 1608 SIZE	1	EA
R755	CRJ10DJ223T	RES , CHIP	22K OHM 1608 SIZE	1	EA
R771	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R772	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R773	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R774	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R775	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R776	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R777	CRJ10DJ474T	RES , CHIP	470K OHM 1608 SIZE	1	EA
R778	CRJ10DJ223T	RES , CHIP	22K OHM 1608 SIZE	1	EA
R779	CRJ10DJ224T	RES , CHIP	220K OHM 1608 SIZE	1	EA
R781	CRJ10DJ224T	RES , CHIP	220K OHM 1608 SIZE	1	EA
R783	CRJ10DJ224T	RES , CHIP	220K OHM 1608 SIZE	1	EA
R784	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R785	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R786	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R787	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R788	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R789	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R790	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R791	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R792	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R793	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R794	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R795	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R796	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R797	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R798	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R799	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R800	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R801	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R802	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R803	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R804	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R805	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R806	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R807	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R808	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R809	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R810	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R811	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R812	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R813	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R814	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R815	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R816	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R817	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
R818	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R819	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R820	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R821	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R822	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R823	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R824	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R825	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R826	CRJ10DJ104T	RES , CHIP	1M OHM 1608 SIZE	1	EA
R827	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R828	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R829	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R830	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R831	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R832	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R833	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R834	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R835	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R836	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE	1	EA
R837	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R838	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R839	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R840	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R841	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R842	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R843	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R844	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R845	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R846	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE	1	EA
R847	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R848	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R849	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R850	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R851	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R852	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R853	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R854	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R855	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R856	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE	1	EA
R857	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R858	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R859	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R860	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R861	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R862	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R863	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R864	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R865	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R866	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE	1	EA
R867	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R868	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R869	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R870	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R871	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R872	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R873	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R874	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R875	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R876	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE	1	EA
R877	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R878	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
R879	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R880	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R881	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R882	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R883	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R884	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R885	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R886	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE	1	EA
R887	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R888	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R889	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R890	CRJ10DJ132T	RES , CHIP	1.3K OHM 1608 SIZE	1	EA
R891	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R892	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R893	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R894	CRJ10DJ332T	RES , CHIP	3.3K OHM 1608 SIZE	1	EA
R895	CRJ10DJ102T	RES , CHIP	1K OHM 1608 SIZE	1	EA
R896	CRJ10DJ104T	RES , CHIP	100K OHM 1608 SIZE	1	EA
R901	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R902	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R903	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R904	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R905	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R906	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R907	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R908	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R909	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R910	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R911	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R912	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R915	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R916	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R917	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R918	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R919	CRJ10DJ473T	RES , CHIP	47K OHM 1608 SIZE	1	EA
R920	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R921	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R923	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R924	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R925	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R926	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R927	CRJ10DJ182T	RES , CHIP	1.8K OHM 1608 SIZE	1	EA
R928	CRJ10DJ391T	RES , CHIP	390 OHM 1608 SIZE	1	EA
R929	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R930	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R931	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R932	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R933	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R934	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R935	CRJ10DJ101T	RES , CHIP	100 OHM 1608 SIZE	1	EA
R937	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R938	CRJ10DJ103T	RES , CHIP	10K OHM 1608 SIZE	1	EA
R939	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R940	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R941	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R943	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R944	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R991	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
L608	CRJ10DJ0R0T	RES , CHIP	0 OHM 1608 SIZE	1	EA
R154	CRJ10DF1202T	RES , CHIP 1%	1.2K OHM(1%) 1608 SIZE	1	EA
R165	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA

Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
R190	CRJ10DF39R0T	CHIP RES, 1% 39 Ohm	39 OHM(1%) 1608 SIZE	1	EA
R191	CRJ10DF39R0T	CHIP RES, 1% 39 Ohm	39 OHM(1%) 1608 SIZE	1	EA
R192	CRJ10DF39R0T	CHIP RES, 1% 39 Ohm	39 OHM(1%) 1608 SIZE	1	EA
R200	CRJ10DJ330T	RES , CHIP	33 OHM 1608 SIZE	1	EA
R505	CRJ10DJ0R0T	RES , CHIP	0 OHM1608 SIZE	1	EA
R614	CRJ10DJ0R0T	RES , CHIP	0 OHM1608 SIZE	1	EA
R622	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R634	CRJ10DJ0R0T	RES , CHIP	0 OHM1608 SIZE	1	EA
R646	CRJ10DJ472T	RES , CHIP	4.7K OHM 1608 SIZE	1	EA
R897	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R898	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R899	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R900	CRJ10DJ221T	RES , CHIP	220 OHM 1608 SIZE	1	EA
R913	CRJ10DF4700T	RES, CHIP 470 OHM/1608/1%	470 OHM(1%) 1608 SIZE	1	EA
Miscellaneous					
	CVICEF04N7YA	HEAT SINK ASS'Y FOR IC33	CVICEF04N7/CMY5A222	1	EA
L901	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
F701	HFL13BT229GINK	F.I.P	13-BT-229GINK (FUTAB	1	EA
JK91	HJJ9H003Z	JACK,HDMI (JALCO)	YKF45-7009	1	EA
L101	HLQ06E100KRZ	INDUCTOR , CHIP	3225 SIZE	1	EA
L102	HLZ9R006Z	BEAD , CHIP		1	EA
L103	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L104	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L105	HLQ06E100KRZ	INDUCTOR , CHIP	3225 SIZE	1	EA
L106	HLQ06E100KRZ	INDUCTOR , CHIP	3225 SIZE	1	EA
L107	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L108	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L109	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L110	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L112	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L114	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L115	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L116	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L117	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L118	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L119	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L120	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L122	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L123	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L124	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L401	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L501	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L502	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L503	HLQ06E100KRZ	INDUCTOR , CHIP	3225 SIZE	1	EA
L504	HLQ08ER68KRZ	CHIP FERRITE INDUCTOR	2012-R68UH	1	EA
L505	HLQ08ER39KRZ	CHIP FERRITE INDUCTOR	2012-R39UH	1	EA
L509	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L510	HLQ08ER68KRZ	CHIP FERRITE INDUCTOR	2012-R68UH	1	EA
L515	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L601	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L603	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L604	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L605	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L607	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L609	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L610	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L611	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L801	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L802	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA

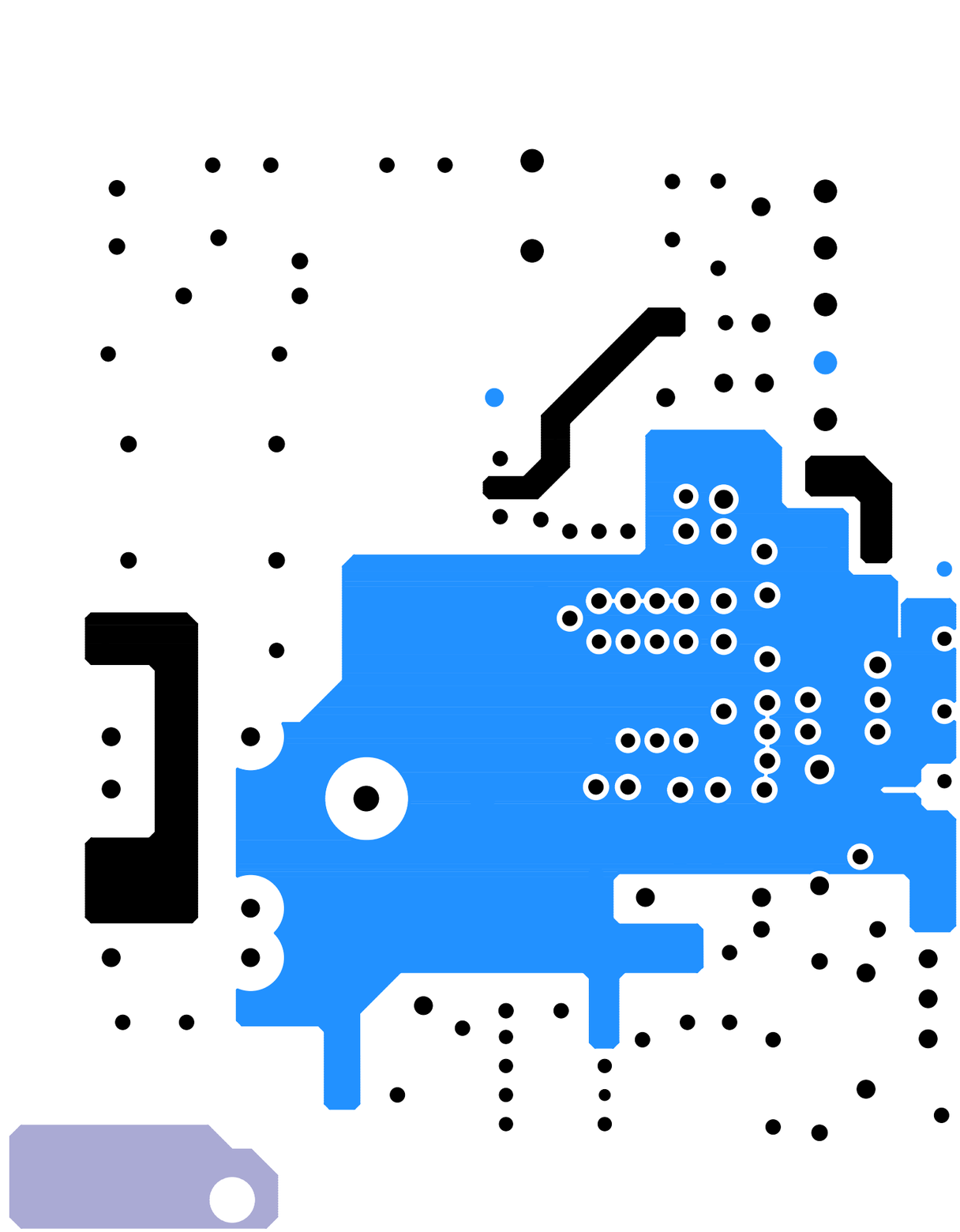
Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
L803	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L804	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L805	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L806	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L807	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L808	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L809	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L810	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L811	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L812	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L813	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L814	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L815	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L902	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L903	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L905	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L906	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L907	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L908	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L909	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L910	CLZ9R009Z	CHOKE COIL, CHIP (FOR HDMI)		1	EA
L911	CLZ9R009Z	CHOKE COIL, CHIP (FOR HDMI)		1	EA
L912	CLZ9R009Z	CHOKE COIL, CHIP (FOR HDMI)		1	EA
L913	CLZ9R009Z	CHOKE COIL, CHIP (FOR HDMI)		1	EA
L991	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
X101	HOX27000E180S	CRYSTAL , CHIP(27MHZ,SMD)	HC-49/US	1	EA
X601	COX13500E160S	X'TAL (13.5MHz) 16p		1	EA
F301	KBA2C2000TLEY	FUSE	(2A/250V)	1	EA
L113	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
L516	HLZ9R001Z	FB, 2012(0805)600E, 1.5A,POWER	600E, 1.5A	1	EA
CN11	CJP24GA195ZM	SMT FFC/FPC WAFER(0.5MM PITCH)	52559-2472 (PB FREE)	1	EA
S701	HST1A020ZT	SW , TACT	switch, Front panel	1	EA
S702	HST1A020ZT	SW , TACT	switch, Front panel	1	EA
S703	HST1A020ZT	SW , TACT	switch, Front panel	1	EA
S704	HST1A020ZT	SW , TACT	switch, Front panel	1	EA
S705	HST1A020ZT	SW , TACT	switch, Front panel	1	EA
S706	HST1A020ZT	SW , TACT	switch, Front panel	1	EA
S707	HST1A020ZT	SW , TACT	switch, Front panel	1	EA
S708	HST1A020ZT	SW , TACT	switch, Front panel	1	EA
BK71	CMD1A504	BRACKET , FIP		1	EA
BK72	CMD1A504	BRACKET , FIP		1	EA
BNO7	CWB1A906190EN	WIRE ASS'Y		1	EA
BN42	CWB1C914080EN	WIRE ASS'Y		1	EA
CNO2	CJP07GA01ZY	WAFER, STRAIGHT, 7PIN	7Pin connector	1	EA
CNO7	CJP06GA19ZY	WAFER, STRAIGHT, 6PIN	6Pin connector	1	EA
CN12	CJP05GA19ZY	WAFER, STRAIGHT, 5PIN	5Pin connector	1	EA
CN13	CJP06GA19ZY	WAFER, STRAIGHT, 6PIN	6Pin connector	1	EA
CN35	CJP14GA19ZY	CARD CABLE WAFER	14Pin connector	1	EA
CY41	CJP17GB113ZY	WAFER	17Pin connector	1	EA
CX41	CJP17GA117ZY	WAFER	17Pin connector	1	EA
	CHD1A012R	SCREW , SPECIAL		1	EA
	CMY5A222	HEAT SINK(25mm)		1	EA
JK47	HJJ1D002Z	JACK, HOSIDEN		1	EA
JK51	CJJ9N006Z	JACK (S-VIDEO + CVBS) GOLD, 2P		1	EA
JK52	CJJ4S043Z	JACK , BOARD		1	EA
JK81	CJJ4R041Z	6P JACK, BOARD	RCA-601DAG-11	1	EA
JK82	CJJ4N067Z	JACK , 2P	RCA-201DAG-01	1	EA
JK83	CJS9U011Z	JACK, OPTICAL+COXIAL(GOLD PLAT		1	EA
VT31	CRVSVC471D14A	VARISTOR	SVC471D14A	1	EA
X401	HOX04000E150C	CRYSTAL , 4MHZ		1	EA
	CTB3+10GR	SCREW		2	EA

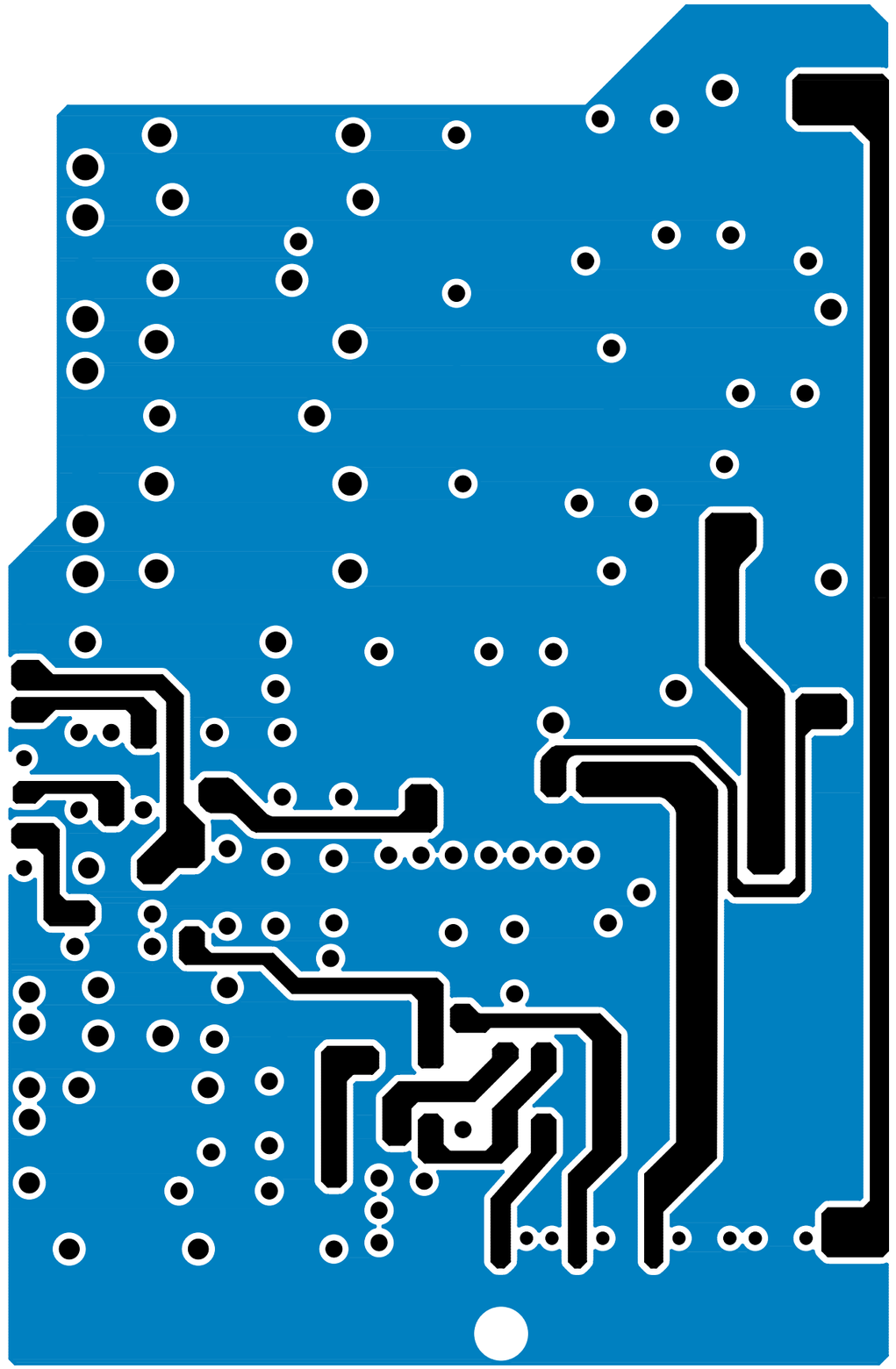
Ref. Designator	Part Number	Description		Qty	
MAIN/FRONT PCB ASS'YS					
	CTB3+6JR	SCREW		5	EA
	CTB3+8GR	SCREW		3	EA
	CTW3+8JR	SCREW		2	EA
	CJJ8A004Z	RECEPTACLE,(2.5A 250V AC) UL		1	EA
	CWZDVD48BN31	WIRE , 2P INLET(2P, 200mm)	2P, 200MM	1	EA
	KHG1A326Z	LUG CUSHION		2	EA
	KMC1A264	cushion,shield		1	EA
SMPS PCB ASS'Y					
Capacitors					
C302	CCEA1HH220TS	CAP , ELECT	50V/22UF/105'C	1	EA
C304	CCEA1HHR47TS	CAP , ELECT	50V/0.47UF/105'C	1	EA
C306	CCEA1HH220TS	CAP , ELECT	50V/22UF/105'C	1	EA
C307	CCEA1HH220TS	CAP , ELECT	50V/22UF/105'C	1	EA
C308	HCQI2A472JZT	Capacitor, Mylar 100V 4700pF	4700PF 100V	1	EA
C309	CCUMT1H101KC	CAP , MLCC(100PF/50V)	100PF 50V	1	EA
C311	CCEA1HH1R0TS	CAP , ELECT	50V/1.0UF/105'C	1	EA
C312	HCQI2A472JZT	Capacitor, Mylar 100V 4700pF	4700PF 100V	1	EA
C313	CCET400VKLH100TKS	CAP , ELECT(KLH, 400V/10UF, 10	KLH, 400V/10UF, 10X2	1	EA
C321	CCKT3A102KBL	CAP , CERAMIC	EKR3A102K05FK5	1	EA
C322	CCEA1AH471TS	CAP , ELECT	10V/470UF/105'C	1	EA
C323	CCEA1HH1R0TS	CAP , ELECT	50V/1.0UF/105'C	1	EA
C324	CCEA1AH471TS	CAP , ELECT	10V/470UF/105'C	1	EA
C325	CCEA1HH470TS	CAP , ELECT	50V/47UF/105'C	1	EA
C326	CCEA1HH470TS	CAP , ELECT	50V/47UF/105'C	1	EA
C327	CCUMT1H104KB	CAP , MONO	0.1UF 50V	1	EA
C328	CCUMT1H104KB	CAP , MONO	0.1UF 50V	1	EA
C332	CCEA1HH1R0TS	CAP , ELECT	50V/1.0UF/105'C	1	EA
C333	CCEA1AH471TS	CAP , ELECT	10V/470UF/105'C	1	EA
C335	CCKT3A102KBL	CAP , CERAMIC	EKR3A102K05FK5	1	EA
C336	CCEA1EH681TS	CAP , ELECT	25V/680UF/105'C	1	EA
C337	CCEA1EH681TS	CAP , ELECT	25V/680UF/105'C	1	EA
C338	CCEA1EH101TS	CAP , ELECT	25V/100UF/105'C	1	EA
C339	CCEA1EH101TS	CAP , ELECT	25V/100UF/105'C	1	EA
C340	CCEA1EH331TS	CAP , ELECT	25V/330UF/105'C	1	EA
C341	CCEA1EH101TS	CAP , ELECT	25V/100UF/105'C	1	EA
C342	CCEA1EH681TS	CAP , ELECT	25V/680UF/105'C	1	EA
C343	CCEA1EH331TS	CAP , ELECT	25V/330UF/105'C	1	EA
C344	CCKT3A102KBL	CAP , CERAMIC	EKR3A102K05FK5	1	EA
C346	CCEA1AH471TS	CAP , ELECT	10V/470UF/105'C	1	EA
CX31	HCQF2E104KZE	CAP , POLYPROPYLENE FILM	1UF (275V)	1	EA
CX32	HCQF2E104KZE	CAP , POLYPROPYLENE FILM	1UF (275V)	1	EA
CY31	CCKDHS102ME	CAP , CERAMIC (400V Y-CAP)	1000pF (400V)	1	EA
CY32	CCKDHS102ME	CAP , CERAMIC (400V Y-CAP)	1000pF (400V)	1	EA
CY34	CCKDHS102ME	CAP , CERAMIC (400V Y-CAP)	1000pF (400V)	1	EA
CY35	CCKDHS102ME	CAP , CERAMIC (400V Y-CAP)	1000pF (400V)	1	EA
C301	CCET400VK3J101NKZ	CAP , ELECT(100uF/400V,25X25,K	100UF/400V,25X25,K3J	1	EA
C305	CCKT3A222KBL	CAP , CERAMIC	2200pF (1KV)	1	EA
C310	CCKT3A222KBL	CAP , CERAMIC	2200pF (1KV)	1	EA
C331	CCEA1CH222ES	CAP , ELECT	2200UF/16V/105'C	1	EA
C345	CCEA1CH222ES	CAP , ELECT	2200UF/16V/105'C	1	EA
Semiconductors					
D311	CVD1SS133MT	DIODE	1SS133	1	EA
D313	HVDMTZJ20BT	DIODE , ZENER	MTZJ20B 1/2W	1	EA
D314	HVDMTZJ20BT	DIODE , ZENER	MTZJ20B 1/2W	1	EA
D315	HVDMTZJ20BT	DIODE , ZENER	MTZJ20B 1/2W	1	EA
D321	HVD11EQ06T	DIODE , SCHOTTKY (60V/1A)	11EQ06	1	EA

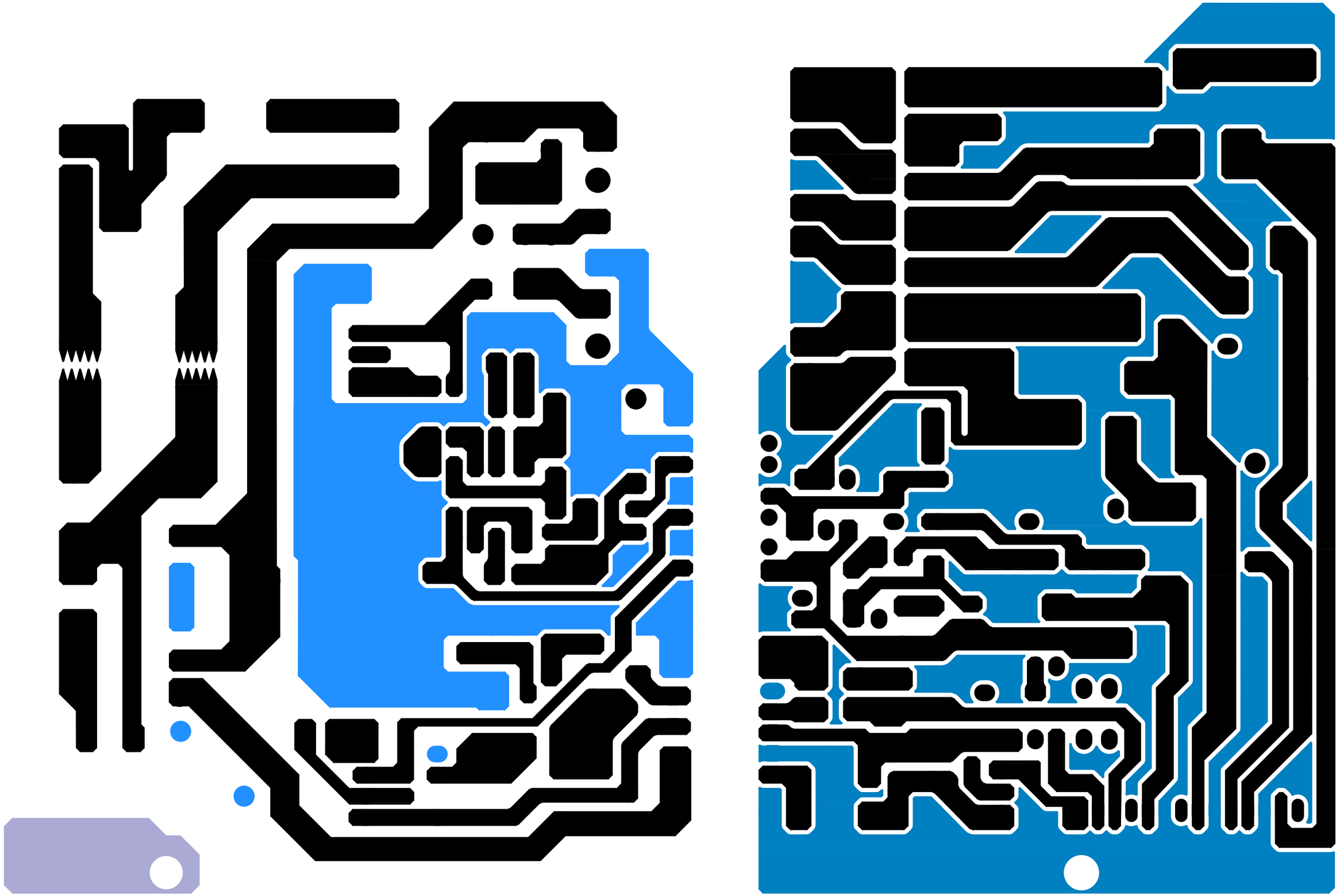
Ref. Designator	Part Number	Description		Qty	
SMPS PCB ASS'Y					
D322	HVD11EQ06T	DIODE , SCHOTTKY (60V/1A)	11EQ06	1	EA
D334	HVD1N4148T	DIODE	1N4148	1	EA
D335	HVDMTZJ2.7BT	DIODE , ZENER	MTZJ2.7B 1/2W	1	EA
IC34	HVIKIA431BAT	PROGRAMMABLE PRECISION REFERENCE	KIA431B	1	EA
IC35	HVIKIA431BAT	PROGRAMMABLE PRECISION REFERENCE	KIA431B	1	EA
Q301	HVTKSA708YT	TRANSISTOR PNP	KSA708Y	1	EA
Q310	CVTKTN2222A	TRANSISTOR NPN	KTN2222A	1	EA
Q311	HVTKSA708YT	TRANSISTOR PNP	KSA708Y	1	EA
Q314	HVTKRC102MT	TRANSISTOR NPN	KRC102M	1	EA
D301	HVDRL207T	DIODE	RL207T	1	EA
D302	HVDRL207T	DIODE	RL207T	1	EA
D303	HVDRL207T	DIODE	RL207T	1	EA
D304	HVDRL207T	DIODE	RL207T	1	EA
D305	HVDFR107T	DIODE , F-R	FR107T	1	EA
D306	HVDFR107T	DIODE , F-R	FR107T	1	EA
D307	HVDFR107T	DIODE , F-R	FR107T	1	EA
D308	HVDFR107T	DIODE , F-R	FR107T	1	EA
D309	HVDFR107T	DIODE , F-R	FR107T	1	EA
D310	HVDFR107T	DIODE , F-R	FR107T	1	EA
D312	HVDRL207T	DIODE	RL207T	1	EA
D323	HVDUF4004T	DIODE , SCHOTTKY	UF4004	1	EA
D325	HVD31DQ06H	DIODE	31DQ06-FC5	1	EA
D326	CVDSF24T	DIODE , RECTIFIFER	SF24T	1	EA
D327	HVDUF5404H	DIODE , ULTRA FAST	UF5404H	1	EA
D328	HVD31DQ06H	DIODE	31DQ06-FC5	1	EA
D329	HVD31DQ06H	DIODE	31DQ06-FC5	1	EA
D330	HVDUF4004T	DIODE , SCHOTTKY	UF4004	1	EA
IC31	CVIICE3B0365J	IC, CooLSET SMPS Current Mode Controller	ICE3B0365J DIP-8P	1	EA
IC32	BVISG6842JLDZ	IC , PWM	SG6842JLDZ	1	EA
IC33	CVICEF04N7	FET CEF04N7 (TO-220 TYPE)	CVICEF04N7/CMY5A222	1	EA
PC31	HVIPC17L1CB	I.C , PHOTO COUPLER	PC17L1C	1	EA
PC32	HVIPC17L1CB	I.C , PHOTO COUPLER	PC17L1C	1	EA
PC33	HVIPC17L1CB	I.C , PHOTO COUPLER	PC17L1C	1	EA
Resistors					
R301	KROS1TJ105V	RES , METAL FILM (1/2W , 1M OH	1M OHM 1/2W J	1	EA
R303	CRD25TJ100T	RES , CARBON	10 OHM 1/4W J	1	EA
R304	CRD20TJ4R7T	RES , CARBON	4.7 OHM 1/5W J	1	EA
R307	CRD20TJ273T	RES , CARBON	27K OHM 1/5W J	1	EA
R309	CRD20TJ273T	RES , CARBON	27K OHM 1/5W J	1	EA
R311	CRD25TJ330T	RES , CARBON	33 OHM 1/4W J	1	EA
R312	CRD20TJ273T	RES , CARBON	27K OHM 1/5W J	1	EA
R313	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1	EA
R314	CRD20TJ103T	RES , CARBON	10K OHM 1/5W J	1	EA
R315	CRD20TJ433T	RES , CARBON	43K OHM 1/5W J	1	EA
R316	CRD20TJ470T	RES , CARBON	47 OHM 1/5W J	1	EA
R317	CRD20TJ103T	RES , CARBON	10K OHM 1/5W J	1	EA
R318	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1	EA
R319	CRD20TJ104T	RES , CARBON	100K OHM 1/5W J	1	EA
R320	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J	1	EA
R321	CRD20TJ222T	RES , CARBON	2.2K OHM 1/5W J	1	EA
R322	CRD20TJ222T	RES , CARBON	2.2K OHM 1/5W J	1	EA
R323	CRD20TF3001T	RES , CARBON	3K 1/5W F	1	EA
R324	CRD20TF3001T	RES , CARBON	3K 1/5W F	1	EA
R325	CRD20TJ104T	RES , CARBON	100K OHM 1/5W J	1	EA
R326	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1	EA
R327	CRD20TJ153T	RES , CARBON	15K OHM 1/5W J	1	EA
R328	CRD20TJ123T	RES , CARBON	12K OHM 1/5W J	1	EA
R330	CRD20TJ681T	RES , CARBON	680 OHM 1/5W J	1	EA
R340	CRD20TJ101T	RES , CARBON	100 OHM 1/5W J	1	EA

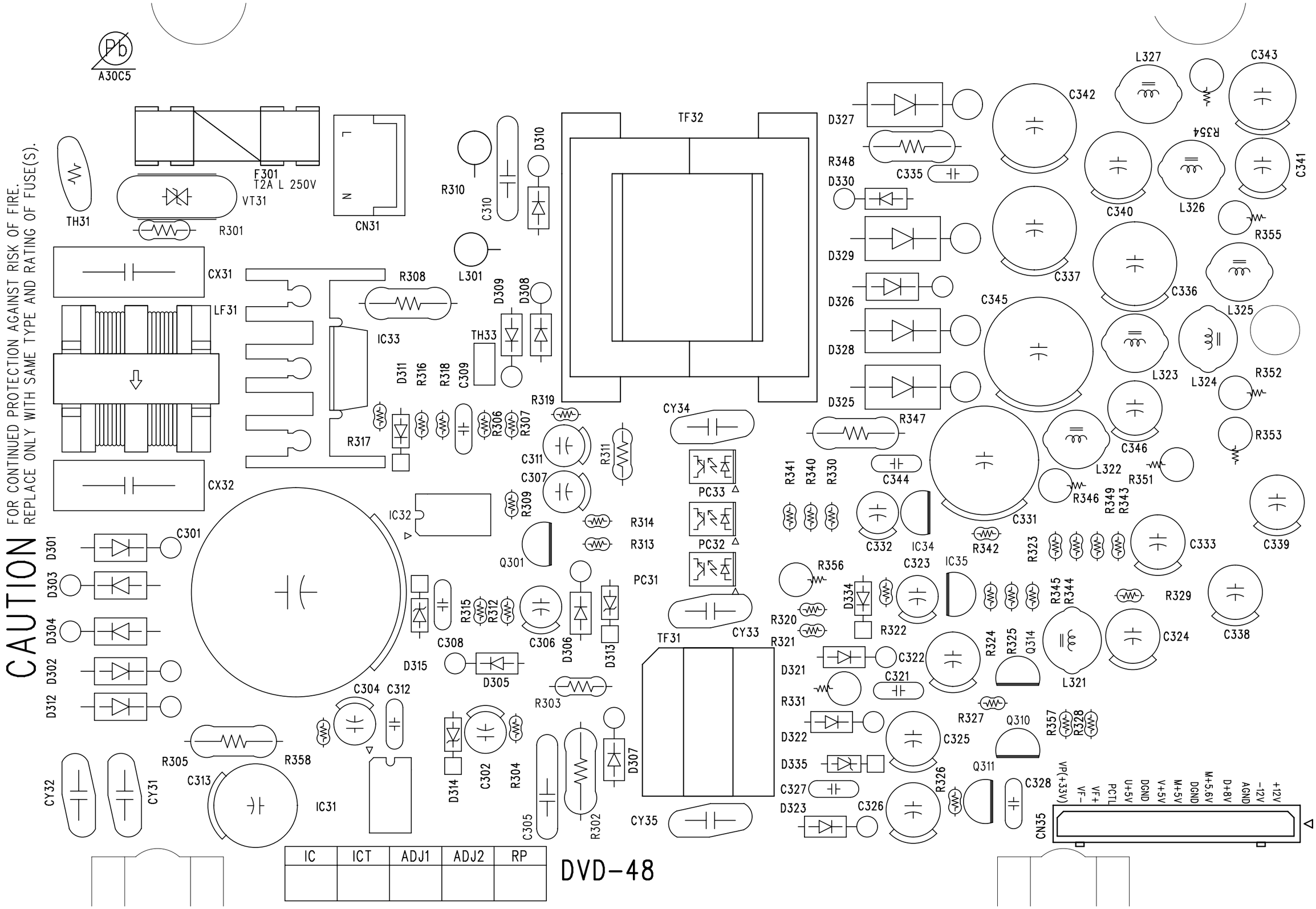
Ref. Designator	Part Number	Description		Qty	
SMPS PCB ASS'Y					
R341	CRD20TJ222T	RES , CARBON	2.2K OHM 1/5W J	1	EA
R342	CRD20TJ222T	RES , CARBON	2.2K OHM 1/5W J	1	EA
R343	CRD20TF3001T	RES , CARBON	3K 1/5W F	1	EA
R344	CRD20TF3001T	RES , CARBON	3K 1/5W F	1	EA
R345	CRD20TJ753T	RES , CARBON	75K OHM 1/5W J	1	EA
R357	CRD20TJ102T	RES , CARBON	1K OHM 1/5W J	1	EA
R358	CRD20TJ204T	RES , CARBON	200K OHM 1/5W J	1	EA
R302	CRG1ANJ154H	RES , METAL OXIDE FILM (150K J	150K OHM 1W J	1	EA
R305	CRG1ANJ2R7B	RES , METAL OXIDE(1W, 2.7ohm)	2.7 OHM 1W J	1	EA
R308	KRW1PJ0R5V	RES , WIRE WOUND(1W, 0.5Ohm)	1W 0.5(J) NON-INDUCT	1	EA
R310	CRG2ANJ683R	RES , METAL OXIDE FILM	68K OHM 2W J	1	EA
R331	CRG1ANJ220R	RES , METAL OXIDE FILM(1W, 20o	22 OHM 1W J	1	EA
R346	CRG1ANJ101R	RES , METAL OXIDE FILM (100 J	100 OHM 1W J	1	EA
R347	CRG1ANJ220H	RES , METAL OXIDE FILM	22 OHM 1W J	1	EA
R348	CRG1ANJ220H	RES , METAL OXIDE FILM	22 OHM 1W J	1	EA
R351	CRG1ANJ101R	RES , METAL OXIDE FILM (100 J	100 OHM 1W J	1	EA
R352	CRG1ANJ271R	RES , METAL OXIDE FILM (270 J	270 OHM 1W J	1	EA
R353	CRG1ANJ271R	RES , METAL OXIDE FILM (270 J	270 OHM 1W J	1	EA
R354	CRG1ANJ471R	RES , METAL OXIDE FILM (470 J	470 OHM 1W J	1	EA
R355	CRG1ANJ471R	RES , METAL OXIDE FILM (470 J	470 OHM 1W J	1	EA
R356	CRG1ANJ101R	RES , METAL OXIDE FILM (100 J	100 OHM 1W J	1	EA
Miscellaneous					
	CHD1A012R	SCREW , SPECIAL		1	EA
	CMY5A222	HEAT SINK(25mm)	for FET CEF04N7	1	EA
L301	HLZ93001Z	CORE , BEAD	UL94-V0	1	EA
L321	CLZ9Z074Z	COIL , CHOKE(20uH)	6700F-20M	1	EA
L322	CLZ9Z040Y	COIL , CHOKE(6.8uH)	6700F-6R8M	1	EA
L323	CLZ9Z040Y	COIL , CHOKE(6.8uH)	6700F-6R8M	1	EA
L324	CLZ9Z040Y	COIL , CHOKE(6.8uH)	6700F-6R8M	1	EA
L325	CLZ9Z040Y	COIL , CHOKE(6.8uH)	6700F-6R8M	1	EA
L326	CLZ9Z040Y	COIL , CHOKE(6.8uH)	6700F-6R8M	1	EA
L327	CLZ9Z040Y	COIL , CHOKE(6.8uH)	6700F-6R8M	1	EA
TH31	KRT10D9MSFT	THERMISTER	10D9M	1	EA
CN31	CJP02KA060ZY	WAFER, STRAIGHT, 2PIN	2Pin connector	1	EA
CN35	CJP14GA19ZY	WAFER, STRAIGHT, 14PIN	14Pin connector	1	EA
LF31	CLZ9Z072Z	LINE FILTER (DVD-S1700)	CLZ9Z072Z	1	EA
TF31	CLT9Z032ZE	TRANS(DVD48)	CLT9Z032ZE	1	EA
TF32	CLT9Z033ZE	TRANS(DVD48)	CLT9Z033ZE	1	EA
	CWZDVD48BN31A	INLET WIRE ASS'Y	CWZDVD48BN31A	1	EA
	CJJ8A004Z	RECEPTACLE , AC(2.5A 250V, UL)	0721-SS	1	EA
	CWZDVD48BN31	WIRE , 2P INLET(2P, 200mm)	CWZDVD48BN31	1	EA
F301	KBA2C2000TLEY	FUSE	EUR (2A/250V)	1	EA
FH31	KJCFC5S	HOLDER , FUSE	KJCFC5S	1	EA
FH32	KJCFC5S	HOLDER , FUSE	KJCFC5S	1	EA
MECHANICAL					
	CWZDVD48BN31A	INLET WIRE ASS'Y		1	EA
	CHE154	CLAMPER , ARM		0.12	M
	CGWDVD48	FRONT PANEL ASS'Y	DVD48	1	EA
	CBT1A997	KNOB, FUNCTION		1	EA
	CGL1A240	INDICATOR, POWER		1	EA
	CGR1A387K128	DOOR, DVD		1	EA
	CGUDVD48	WINDOW ASS'Y	DVD48	1	EA
	CGB1A182Z	BADGE , HARMAN(DVD48)	DVD48	1	EA
	CGU1A383Z	WINDOW, FIP		1	EA
	CGW2A413RDH43	PANEL,FRONT		1	EA
	CGX1A374YC23	ORNAMENT, DOOR		1	EA
	CMC1A214	PLATE , EARTH		2	EA

Ref. Designator	Part Number	Description		Qty	
MECHANICAL					
	CMZ1A105Z	FILTER, FIP		1	EA
	CTB3+10GR	SCREW		5	EA
	CTB3+6JR	SCREW		2	EA
	CWC1B4A17A080B	CABLE , CARD		1	EA
	KGB1A158Z	BADGE , HARMAN/KARDON(FRONT)		1	EA
	CGX1A375ZA	BADGE ASS'Y		1	EA
	CGX1A375M7G32	ORNAMENT , BADGE		1	EA
	KGB1A159Z	BADGE , HARMAN/KARDON(TOP)		1	EA
	CKC4A166G44	CABINET , TOP		1	EA
	CTBD3+10GFZR	SCREW		6	EA
	CTBD3+8JFC	SCREW , DOT		4	EA
	CTB3+6FFZR	SCREW		1	EA
	CADDVD27ZA	DVD MECHANISM ASS'Y (KOMI)		1	EA
	CMH1A250	GUIDE, CABLE			EA
	CWB1B905150EE	WIRE ASS'Y			EA
	CWB5A906150SE	WIRE ASS'Y			EA
	CWC1G2A24G250B	CABLE , CARD			EA
	CMH1A250	GUIDE, CABLE			EA
	CWB1B905150EE	WIRE ASS'Y			EA
	CWB5A906150SE	WIRE ASS'Y			EA
	CWC1G2A24G250B	CABLE , CARD			EA
	CHG1A360	CUSHION , FOOT		4	EA
	CHR301	CLAMPER		3	EA
	CKF1A329Z	PANEL , REAR(DVD48)	DVD48	1	EA
	CKL2A186H43	FOOT		4	EA
	CLZ9Z070Z	FERRITE CORE		1	EA
	CLZ9Z071Z	FERRITE CORE		1	EA








CAUTION FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE AND RATING OF FUSE(S).
Pb
A30C5
F301 T2A L 250V
VT31
TH31
R301
CN31
L
N
CX31
LF31
CX32
CX32
CY32
CY31
R308
IC33
D309
D308
TH33
D311
R316
R318
C309
R317
R319
C311
C307
R311
R310
C310
D310
L301
TF32
CY34
PC33
PC32
PC31
CY33
TF31
CY35
D327
R348
D330
D329
D326
D328
D325
R347
C335
C342
C340
C337
C345
C336
C346
C344
C331
C332
IC34
R342
C333
C339
C338
C324
L321
C322
C321
C325
C326
C327
D323
D321
D322
D335
R331
R321
R320
R356
D334
C323
IC35
R322
R329
R345
R344
R324
R325
Q314
Q310
Q311
R327
R357
R328
C328
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R346
R349
R343
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C346
IC32
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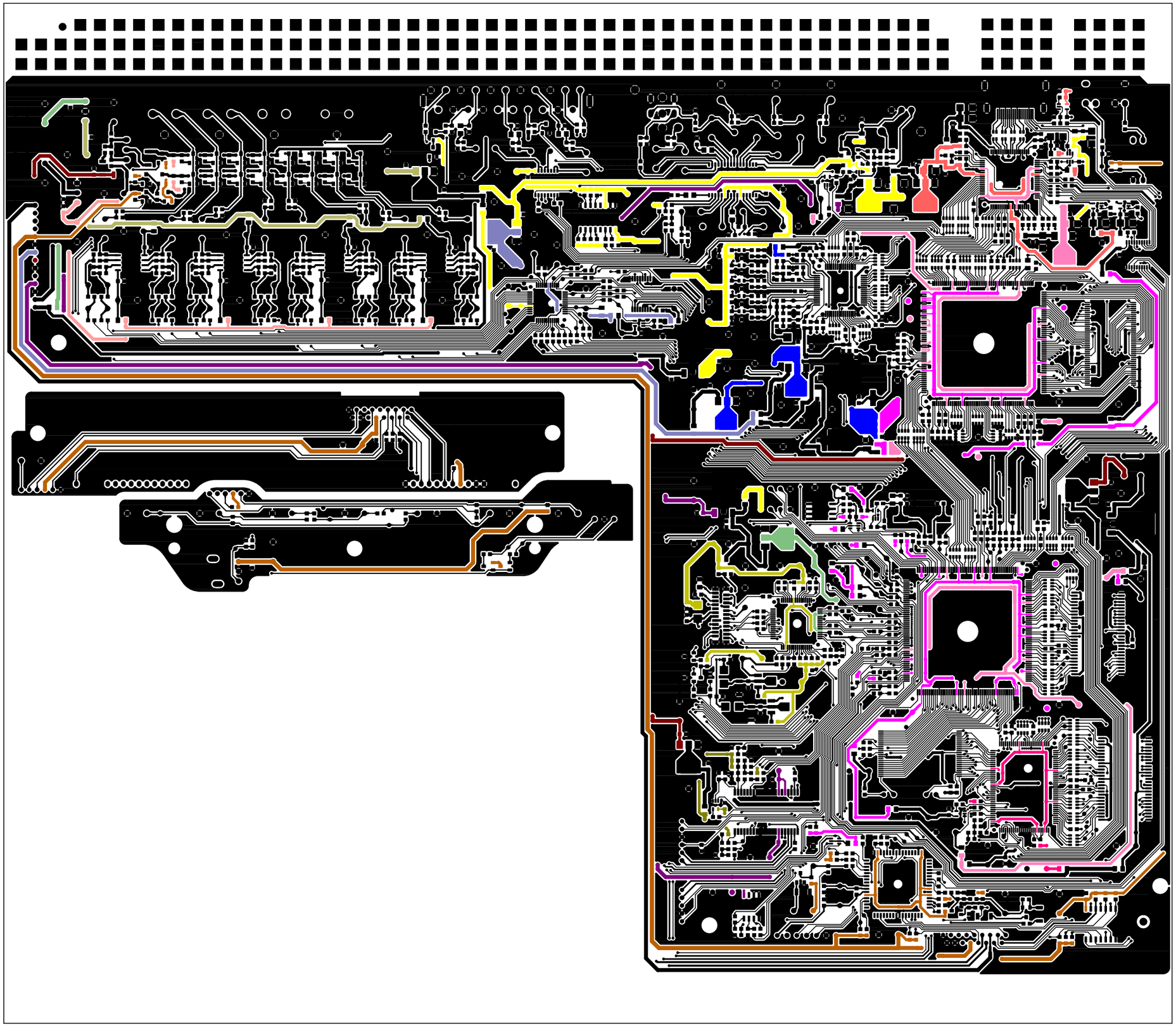
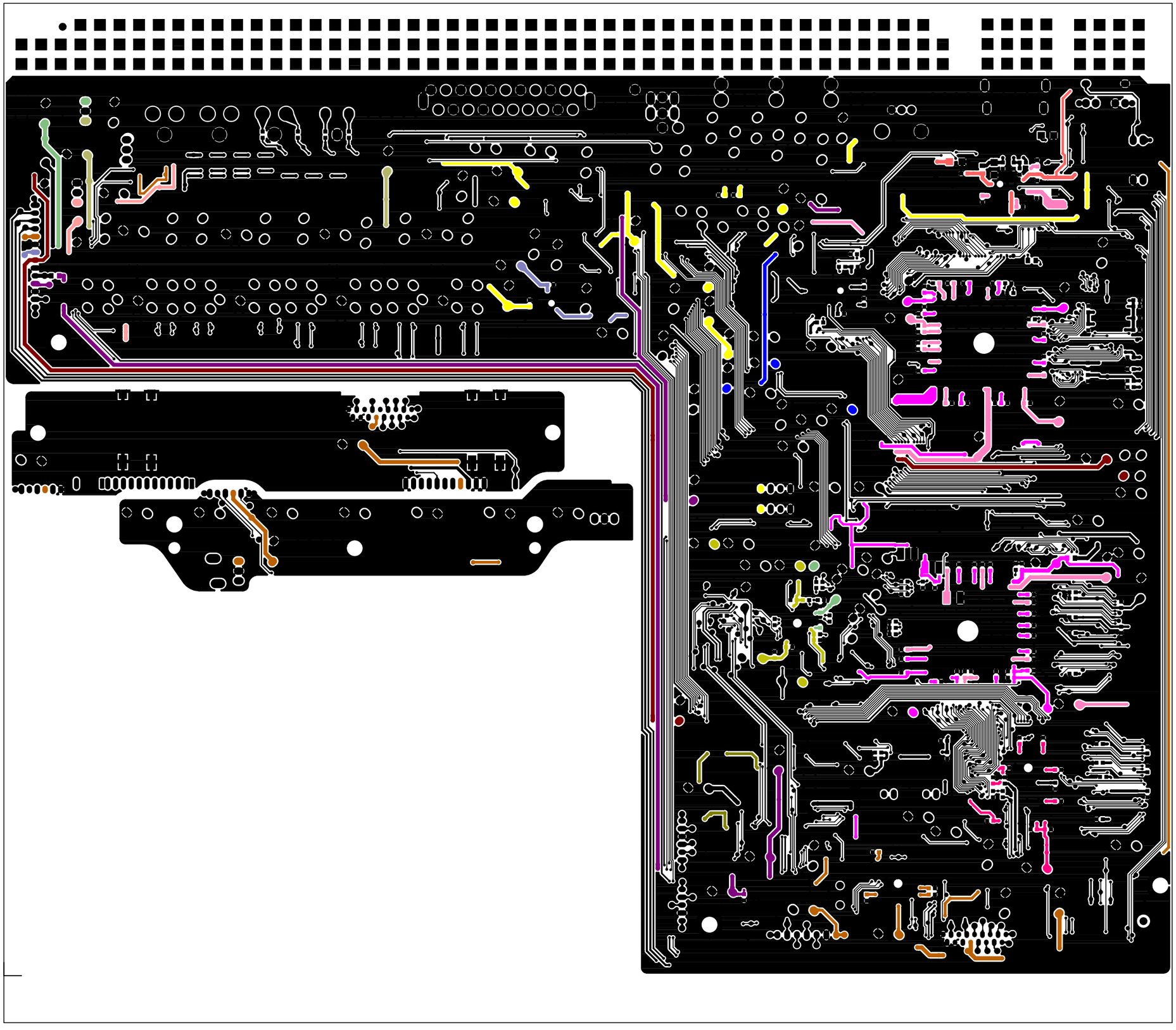
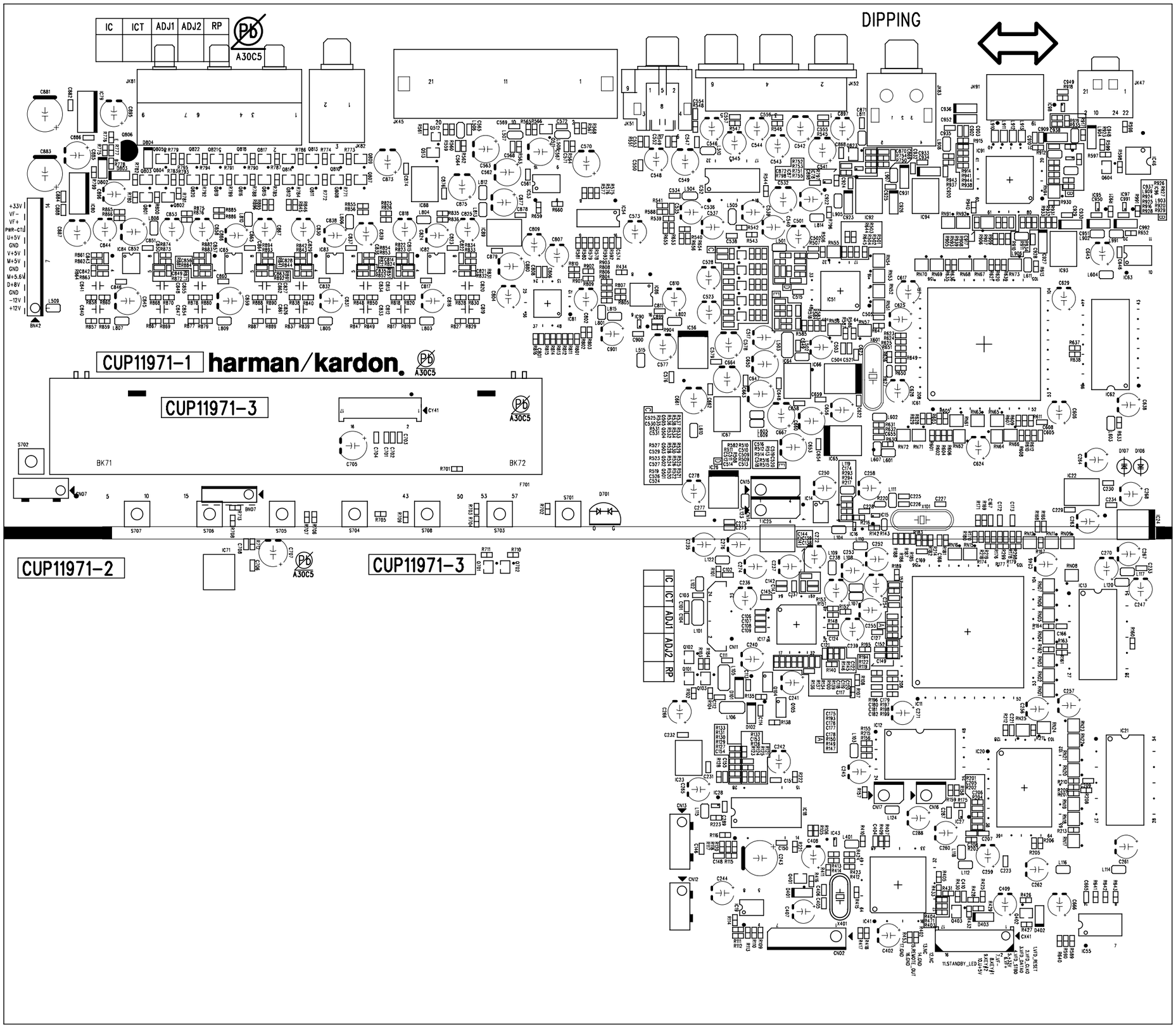
R358
C313
IC31
D314
C302
R304
C305
R302
D307
VP(+33V)
VF-
VF+
PCTL
U+5V
DGND
V+5V
M+5V
DGND
M+5.6V
D+8V
AGND
-12V
+12V
CN35
IC
ICT
ADJ1
ADJ2
RP
DVD-48

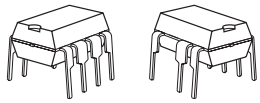





DIPPING
IC ICT ADJ1 ADJ2 RP
A30C5
CUP11971-1
harman/kardon
CUP11971-3
CUP11971-2
CUP11971-3
BK71
BK72
IC ICT ADJ1 ADJ2 RP
+33V
VF-
VF+
PWR-CTL
U+5V
GND
V+5V
M+5V
GND
M+5.6V
D+8V
GND
-12V
+12V
11.STANDBY_LED

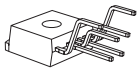
CoolSET™-F3

Off-Line SMPS Current Mode Controller with integrated 650V Startup Cell/Depletion CoolMOS™

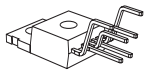


PG-DIP-7-1

PG-DIP-8-6



PG-TO220-6-46 (I2Pak)



PG-TO220-6-47

Product Highlights

- **Best in class in DIP7, DIP8, TO220/I2Pak packages**
- **Active Burst Mode to reach the lowest Standby Power Requirements < 100mW**
- **Protection features (Auto Restart Mode) to increase robustness and safety of the system**
- **Adjustable Blanking Window for high load jumps to increase system reliability**
- **Isolated drain package for TO220/I2Pak**
- **Wide creepage distance for DIP7/TO220/I2Pak**
- **Wide power class of products for various applications**
- **Pb-free lead plating for all packages; RoHS compliant**

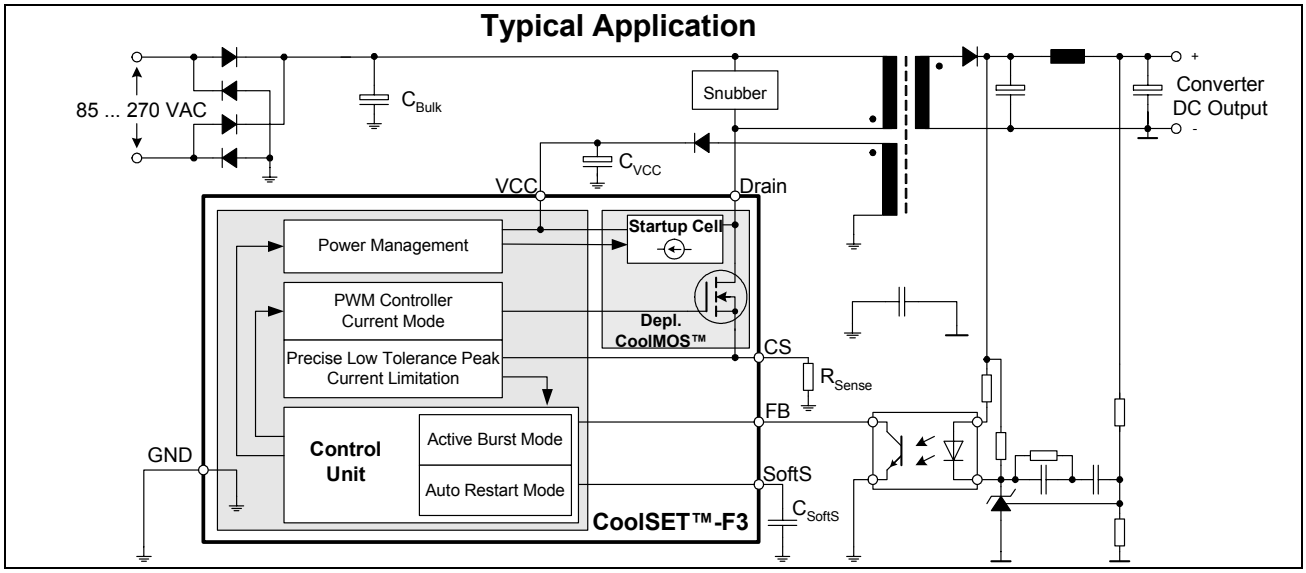
Features

- 650V avalanche rugged CoolMOS™ with built in switchable Startup Cell
- Active Burst Mode for lowest Standby Power @ light load controlled by Feedback signal
- Fast load jump response in Active Burst Mode
- 67/100 kHz fixed switching frequency
- Auto Restart Mode for Overtemperature Detection
- Auto Restart Mode for Overvoltage Detection
- Auto Restart Mode for Overload and Open Loop
- Auto Restart Mode for VCC Undervoltage
- Blanking Window for short duration high current
- User defined Soft Start
- Minimum of external components required
- Max Duty Cycle 72%
- Overall tolerance of Current Limiting < ±5%
- Internal PWM Leading Edge Blanking
- Soft driving for low EMI

Description

The new generation CoolSET™-F3 provides Active Burst Mode to reach the lowest Standby Power Requirements <100mW at no load. As the controller is always active during Active Burst Mode, there is an immediate response on load jumps without any black out in the SMPS. In Active Burst Mode the ripple of the output voltage can be reduced <1%. Furthermore, to increase the robustness and safety of the system, the device enters into Auto Restart Mode in the cases of Overtemperature, VCC Overvoltage, Output Open Loop or Overload and VCC Undervoltage. By means of the internal precise peak current limitation, the dimension of the transformer and the secondary diode can be lowered which leads to more cost efficiency. An adjustable blanking window prevents the IC from entering Auto Restart or Active Burst Mode unintentionally during high load jumps. The CoolSET™-F3 family consists a wide power class range of products for various applications.

Typical Application



1 Pin Configuration and Functionality

1.1 Pin Configuration with PG-DIP-8-6

Pin	Symbol	Function
1	SoftS	Soft-Start
2	FB	Feedback
3	CS	Current Sense/ 650V[1] Depl. CoolMOS™ Source
4	Drain	650V[1] Depl. CoolMOS™ Drain
5	Drain	650V[1] Depl. CoolMOS™ Drain
6	n.c.	Not Connected
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

[1] at $T_j = 110°C$

1.2 Pin Configuration with PG-DIP-7-1

Pin	Symbol	Function
1	SoftS	Soft-Start
2	FB	Feedback
3	CS	Current Sense/ 650V[1] Depl. CoolMOS™ Source
4	n.c.	Not connected
5	Drain	650V[1] Depl. CoolMOS™ Drain
-	-	-
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

[1] at $T_j = 110°C$

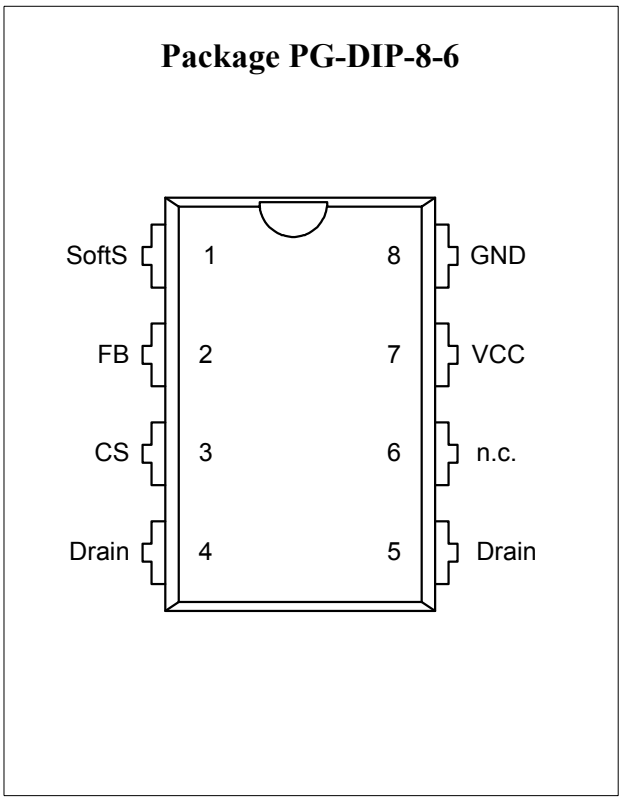


Figure 1 Pin Configuration PG-DIP-8-6(top view)

Note: Pin 4 and 5 are shorted within the DIP 8 package.

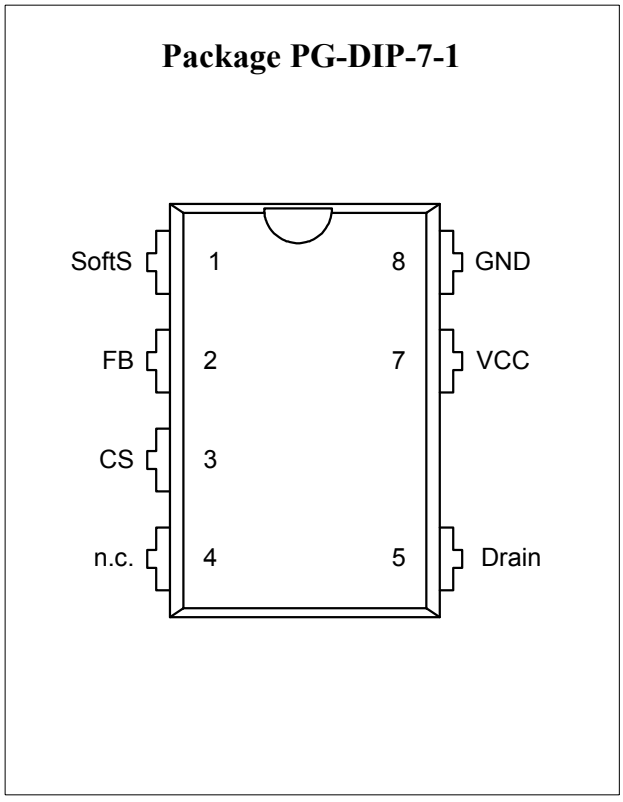


Figure 2 Pin Configuration PG-DIP-7-1(top view)

2 Representative Blockdiagram

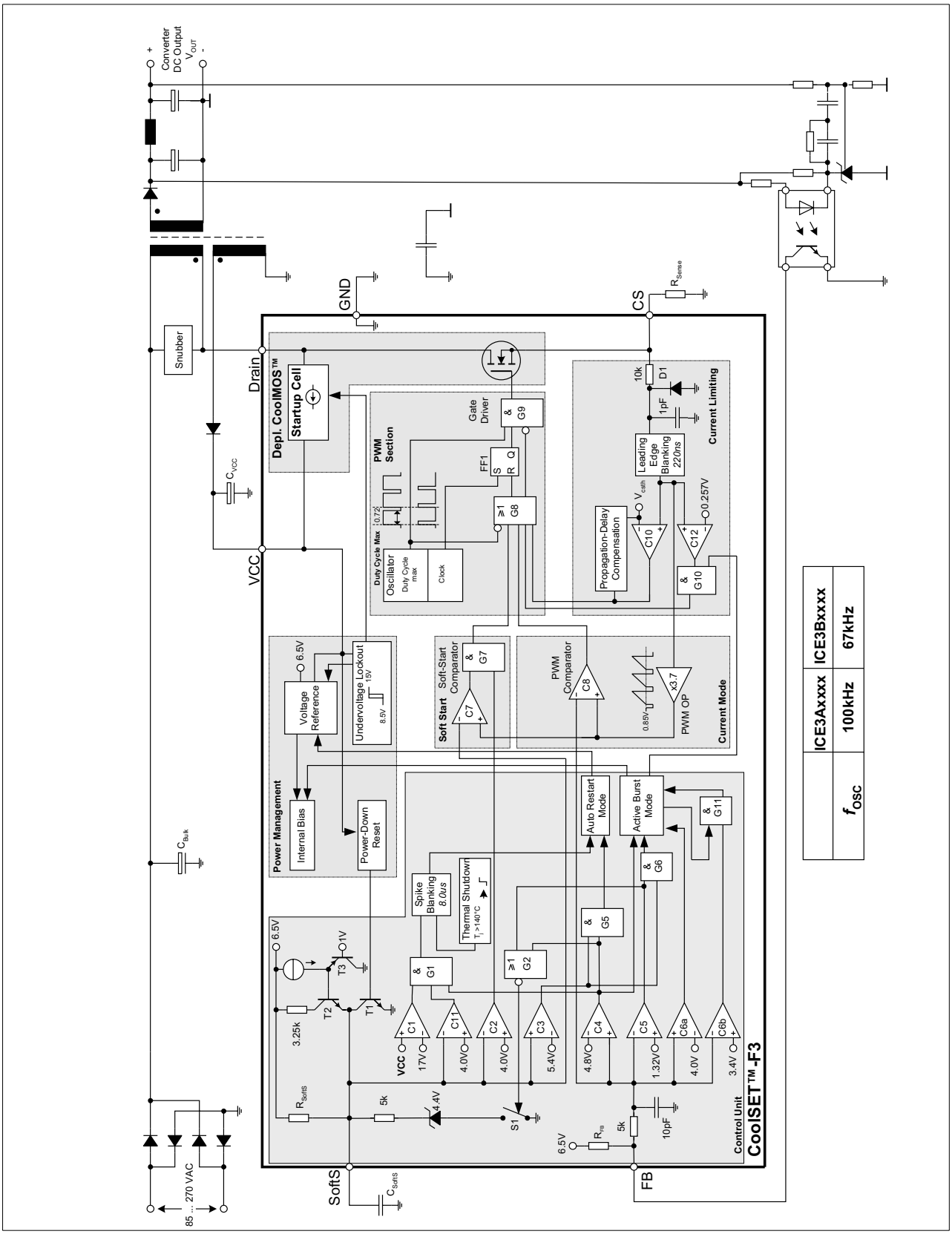


Figure 5 Representative Blockdiagram

KEC

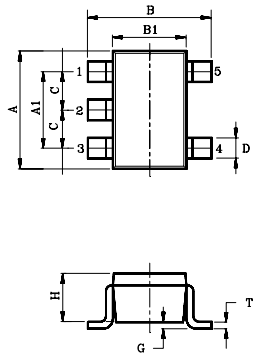
SEMICONDUCTOR
TECHNICAL DATA

KIC7SZ08FU
SILICON MONOLITHIC CMOS
DIGITAL INTEGRATED CIRCUIT

2 INPUT AND GATE

FEATURES

- High Output Drive : ±24mA (Typ.)
  @V_{CC}=3V
- Super High Speed Operation : t_{PD}=2.7ns(Typ.)
  @V_{CC}=5V, 50pF
- Operation Voltage Range : $V_{CC(opr)}$=1.8~5.5V.
- Supply Voltage Data Retention : V_{CC}=1.5~5.5V.
- 5V Tolerant Function



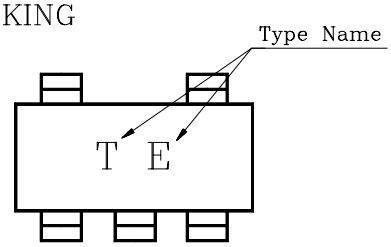
DIM	MILLIMETERS
A	2.00± 0.20
A1	1.3± 0.1
B	2.1± 0.1
B1	1.25± 0.1
C	0.65
D	0.2+0.10/−0.05
G	0~0.1
H	0.9± 0.1
T	0.15+0.1/−0.05

USV

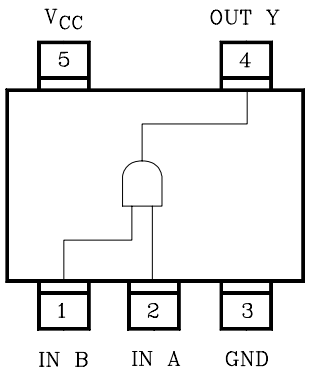
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~6	V
DC Input Voltage	V_{IN}	-0.5~6	V
DC Output Voltage	V_{OUT}	-0.5~6	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	200	mW
Storage Temperature	T_{stg}	-65~150	℃
Lead Temperature (10s)	T_L	260	℃

MARKING

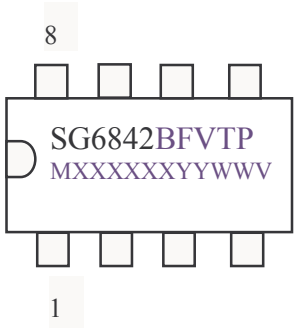


PIN CONNECTION(TOP VIEW)



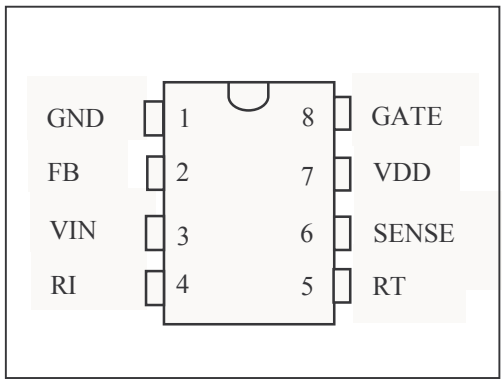
LOGIC DIAGRAM

MARKING DIAGRAMS



B: B = Linearly Decreasing Frequency + Burst-Mode
F: L = OTP Latch: The pin is reset when AC is disconnected.
C = Hysteresis OTP : The pin is reset when the temperature cools down.
V: V = OVP Latch
T: D = DIP, S = SOP
P : Z =Lead Free + ROHS Compatible
Null=regular package
M: Mask Version
XXXXXX: Wafer Lot
YY: Year; WW: Week
V: Assembly Location

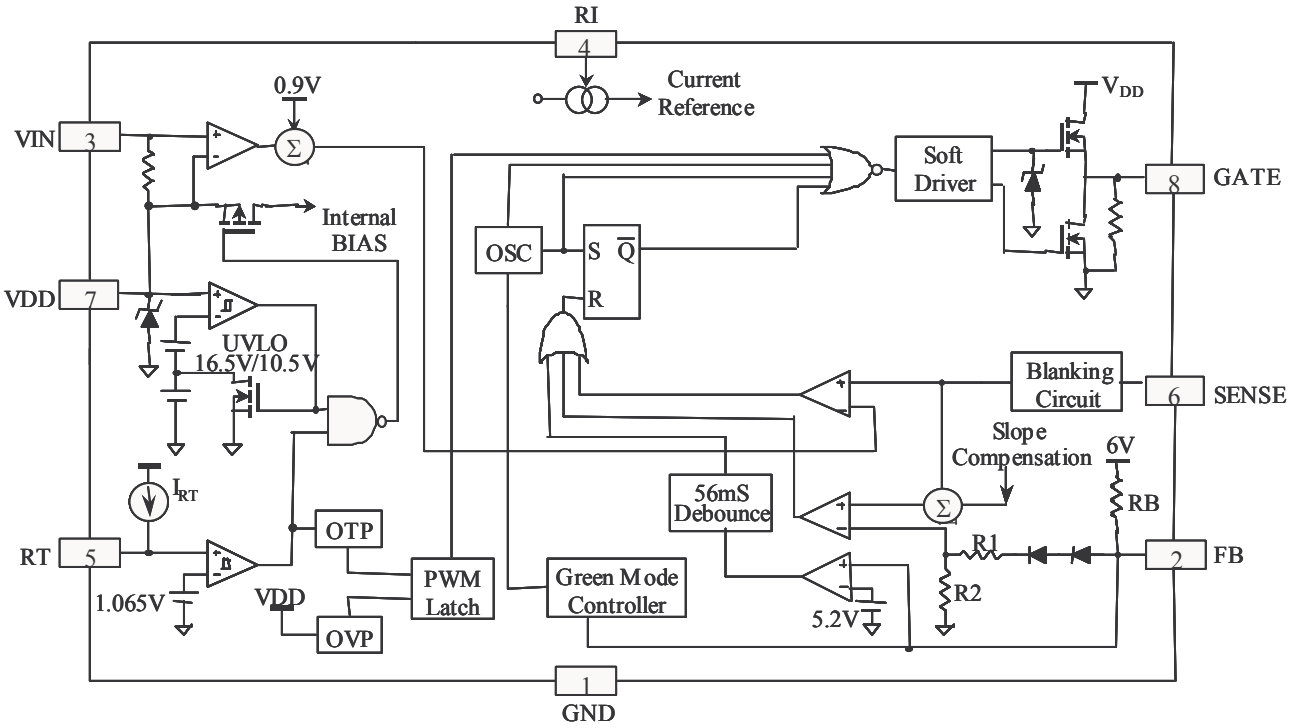
PIN CONFIGURATION



PIN DESCRIPTIONS

Pin No.	Symbol	Function	Description
1	GND	Ground	Ground.
2	FB	Feedback	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal from this pin and the current-sense signal from Pin 6.
3	VIN	Start-Up Input	For start-up, this pin is pulled high to the rectified line input. This pin is pulled via a resistor. Since the start-up current requirement of the SG6842 is very small, a large start-up resistance can be used to minimize power loss. Under normal operation, this pin is also used to detect the line voltage. The line voltage is detected to compensate the output power limit, so that it can be kept constant over a universal AC input range
4	RI	Reference Setting	A resistor connected from the RI pin to ground will provide the SG6842 with a constant current source. This current charges an internal capacitor. This determines the switching frequency. Increasing the resistance will decrease the amplitude of the current from the current source, and thereby reduce the switching frequency. Using a 26kΩ resistor R_I results in a 50uA constant current I_I and a 65kHz switching frequency.
5	RT	Temperature Detection	For over-temperature protection. An external NTC thermistor is connected from this pin to ground. The impedance of the NTC will decrease at high temperatures. Once the voltage of the RT pin drops below a fixed limit of 1.05V, PWM output will be disabled.
6	SENSE	Current Sense	Current sense. The sensed voltage is used for current-mode control and pulse-by-pulse current limiting.
7	VDD	Power Supply	Power Supply. If an open circuit failure occurs in the feedback loop, the internal protection circuit will disable PWM output as long as VDD remains higher than 26V.
8	GATE	Driver Output	The totem-pole output driver for the power MOSFET. A soft driving waveform is implemented for improved EMI.

BLOCK DIAGRAM



TOSHIBA TA48018,02,025,03,033,05F/S

TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

TA48018F, TA4802F, TA48025F, TA4803F, TA48033F, TA4805F, TA48018S, TA4802S, TA48025S, TA4803S, TA48033S, TA4805S

1.8 V, 2 V, 2.5 V, 3 V, 3.3 V, 5 V

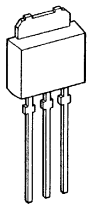
Three-Terminal Low Dropout Voltage Regulator with Output Current of 1 A

The TA48**F/S series consists of fixed-positive-output, low-dropout regulators with an output current of 1 A (max) that utilize V-PNP transistors for the output stage. In response to the need for low-voltage and low-power dissipation devices which are used in consumer electronics and industrial appliances, the series offers devices with low output voltages: 1.8 V, 2 V, 2.5 V, 3 V, 3.3 V, 5 V.

Features

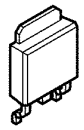
- Maximum output current: 1 A
- Output voltage accuracy: V_{OUT} ± 3% (@T_j = 25°C)
- Low standby current: 800 μA (typ.) (@I_{OUT} = 0 A)
- Low starting quiescent current
- Low-dropout voltage: V_D = 0.5 V (max) (@I_{OUT} = 0.5 A)
- Protection function: overheat/overcurrent
- Package type: PW-MOLD (TA48**F Series)
  TO-220NIS (TA48**S Series)
- TA48**F Series has a lead bending type package which is a surface-mountable package and can be used for reflow soldering.

(1) TA48**F



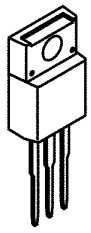
HSIP3-P-2.30B

(2) TA48**F (TE16L1, N)



HSOP3-P-2.30D

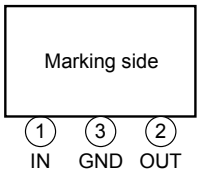
(3) TA48**S



HSIP3-P-2.54A

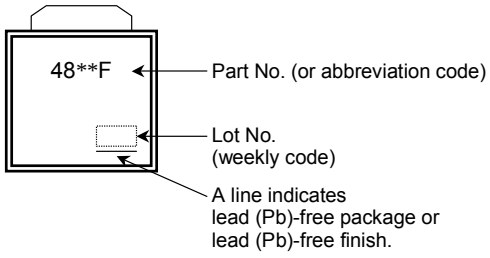
Weight
HSIP3-P-2.30B : 0.36 g (typ.)
HSOP3-P-2.30D : 0.36 g (typ.)
HSIP3-P-2.54A : 1.7 g (typ.)

Pin Assignment

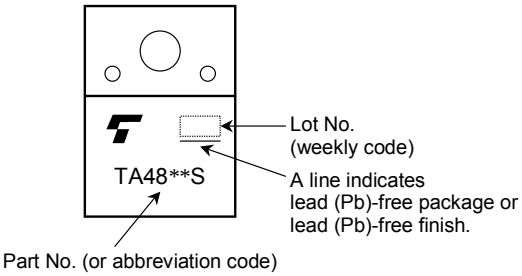


Marking

(1) (2) TA48F** Series



(3) TA48**S Series

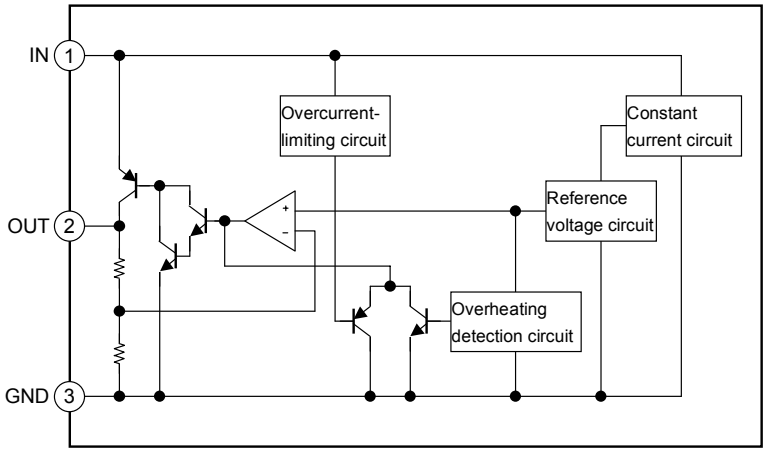


Note: The "**" part of each product number varies according to the output voltage of the product.

How to Order

	Product No.	Package	Packing Type and Unit for Orders
(1)	TA48**F	PW-MOLD: Straight-lead package	Loose in bag: 200 (1 bag)
(2)	TA48**F (TE16L1, N)	PW-MOLD: Surface-mount package	Embossed-tape packing: 2000 (1 tape)
(3)	TA48**S	TO-220NIS	Loose in bag: 50 (1 bag)

Block Diagram



Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Input voltage		V_{IN}	16	V
Output current		I_{OUT}	1	A
Operating temperature		$Ta_{(opr)}$	−40~85	°C
Junction temperature		T_j	150	°C
Storage temperature		T_{stg}	−55~150	°C
Power dissipation (Ta = 25°C)	TA48**F	P_D	1	W
	TA48**S		2	
Power dissipation (Tc = 25°C)	TA48**F	P_D	10	W
	TA48**S		20	
Thermal resistance (junction to ambient)	TA48**F	$R_{th\ (j-a)}$	125	°C/W
	TA48**S		62.5	
Thermal resistance (junction to case)	TA48**F	$R_{th\ (j-c)}$	12.5	°C/W
	TA48**S		6.25	

Note 1: External current and voltage ((including negative voltage) should not be applied to pins not specified.

SN54AHCT541, SN74AHCT541 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS269O – DECEMBER 1995 – REVISED JULY 2003

- **Inputs Are TTL-Voltage Compatible**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

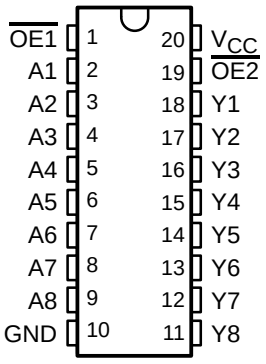
description/ordering information

The ’AHCT541 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

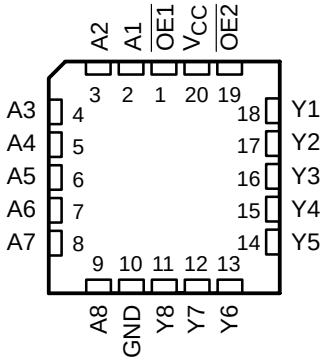
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHCT541 . . . J OR W PACKAGE
SN74AHCT541 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHCT541 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
– to 85°C	PDIP – N	Tube	SN74AHCT541N	SN74AHCT541N
	SOIC – DW	Tube	SN74AHCT541DW	AHCT541
		Tape and reel	SN74AHCT541DWR	
	SOP – NS	Tape and reel	SN74AHCT541NSR	AHCT541
	SSOP – DB	Tape and reel	SN74AHCT541DBR	HB541
	TSSOP – PW	Tube	SN74AHCT541PW	HB541
		Tape and reel	SN74AHCT541PWR	
	TVSOP – DGV	Tape and reel	SN74AHCT541DGVR	HB541
–55°C to 125°C	CDIP – J	Tube	SNJ54AHCT541J	SNJ54AHCT541J
	CFP – W	Tube	SNJ54AHCT541W	SNJ54AHCT541W
	LCCC – FK	Tube	SNJ54AHCT541FK	SNJ54AHCT541FK

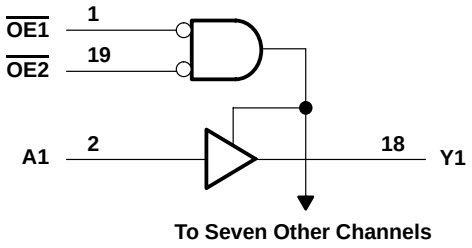
SN54AHCT541, SN74AHCT541
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCLS269O – DECEMBER 1995 – REVISED JULY 2003

FUNCTION TABLE
(each buffer/driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±75 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 70°C/W
DGV package . . . . . 92°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
PW package . . . . . 83°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

hynix

HY57V643220D(L/S)T(P) Series
4Banks x 512K x 32bits Synchronous DRAM

DESCRIPTION

The Hynix HY57V643220D(L/S)T(P) series is a 67,108,864bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. HY57V643220D(L/S)T(P) is organized as 4banks of 524,228x32.

HY57V643220D(L/S)T(P) is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a '2N' rule)

FEATURES

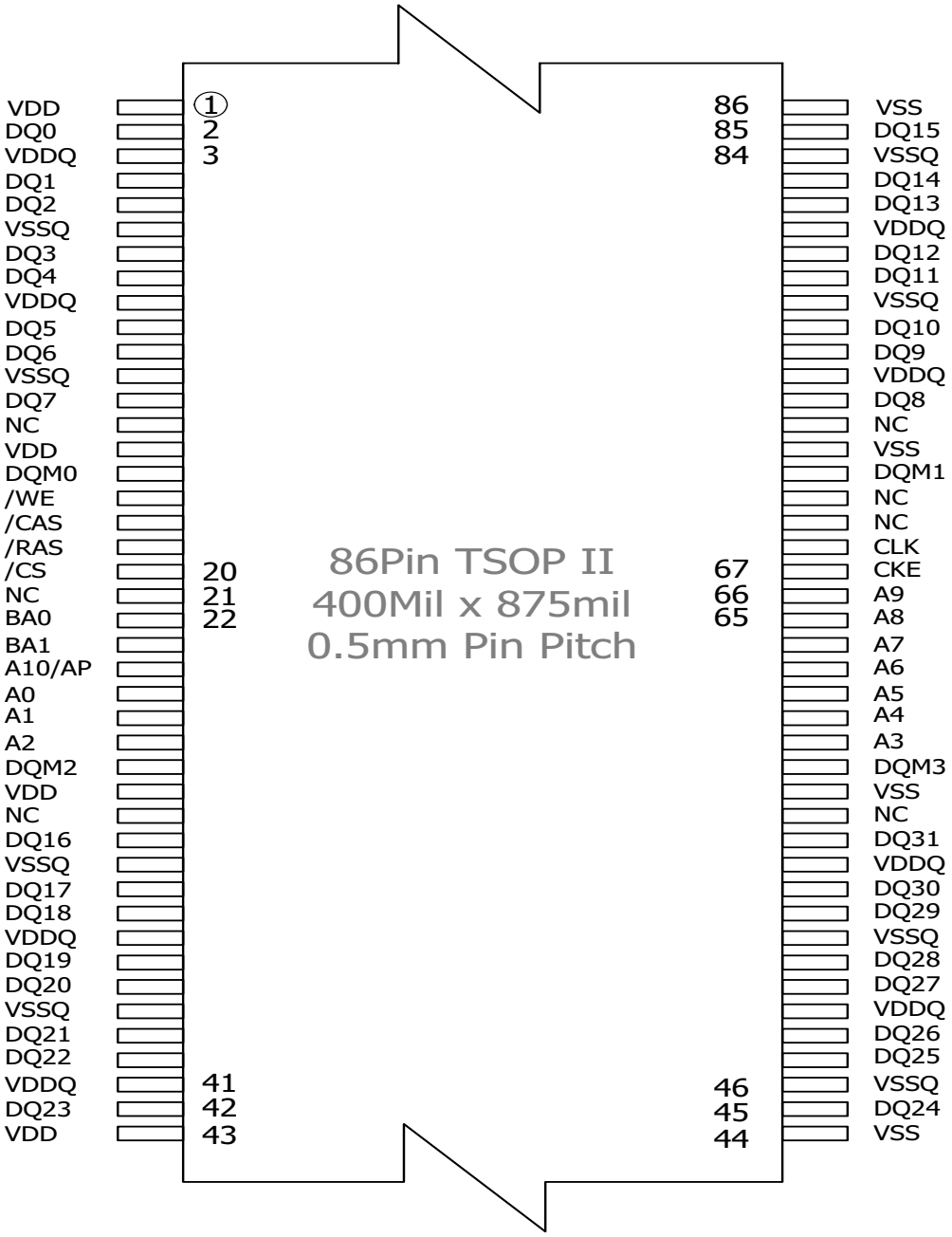
- Voltage : VDD, VDDQ 3.3V supply voltage
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 86pin TSOP-II with 0.5mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by DQM 0, 1, 2 and DQM 3
- Internal four banks operation
- Auto refresh and self refresh
- 4096 Refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{CAS}$ Latency ; 2, 3 Clocks
- Burst Read Single Write operation

ORDERING INFORMATION

Part No.	Clock Frequency	Organization	Interface	Package
HY57V643220D(L/S)T(P)-45	222MHz	4Banks x 512Kbits x32	LVTTL	86pin TSOP-II (Lead Free)
HY57V643220D(L/S)T(P)-5	200MHz			
HY57V643220D(L/S)T(P)-55	183MHz			
HY57V643220D(L/S)T(P)-6	166MHz			
HY57V643220D(L/S)T(P)-7	143MHz			

Note
1. HY57V643220DT(P) Series : Normal Power
2. HY57V643220DLT(P) Series : Low Power
3. HY57V643220DST(P) Series : Super Low Power
4. HY57V643220D(L/S)T Series : Leaded
5. HY57V643220D(L/S)TP Series : Lead Free

86PIN TSOP II CONFIGURATION

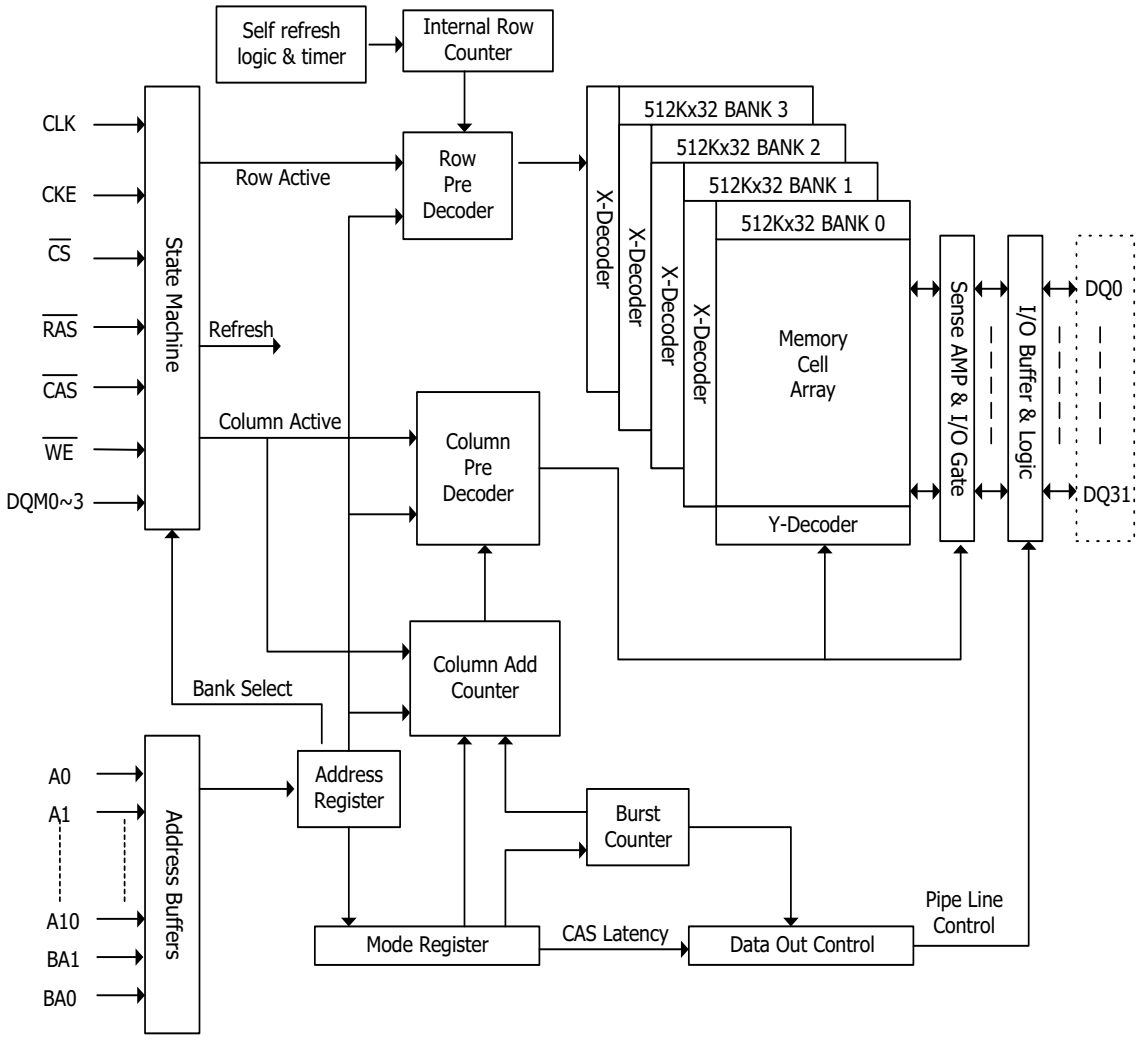


Pin FUNCTION DESCRIPTIONS

Pin	Pin Name	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0, BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A10	Address	Row Address : RA0 ~ RA10, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
DQM0~3	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ31	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/ Ground	Power supply for output buffers
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM

512Kbit x 4banks x 32 I/O Low Power Synchronous DRAM



FLI2310-LF-CF

Digital Video Format Converter

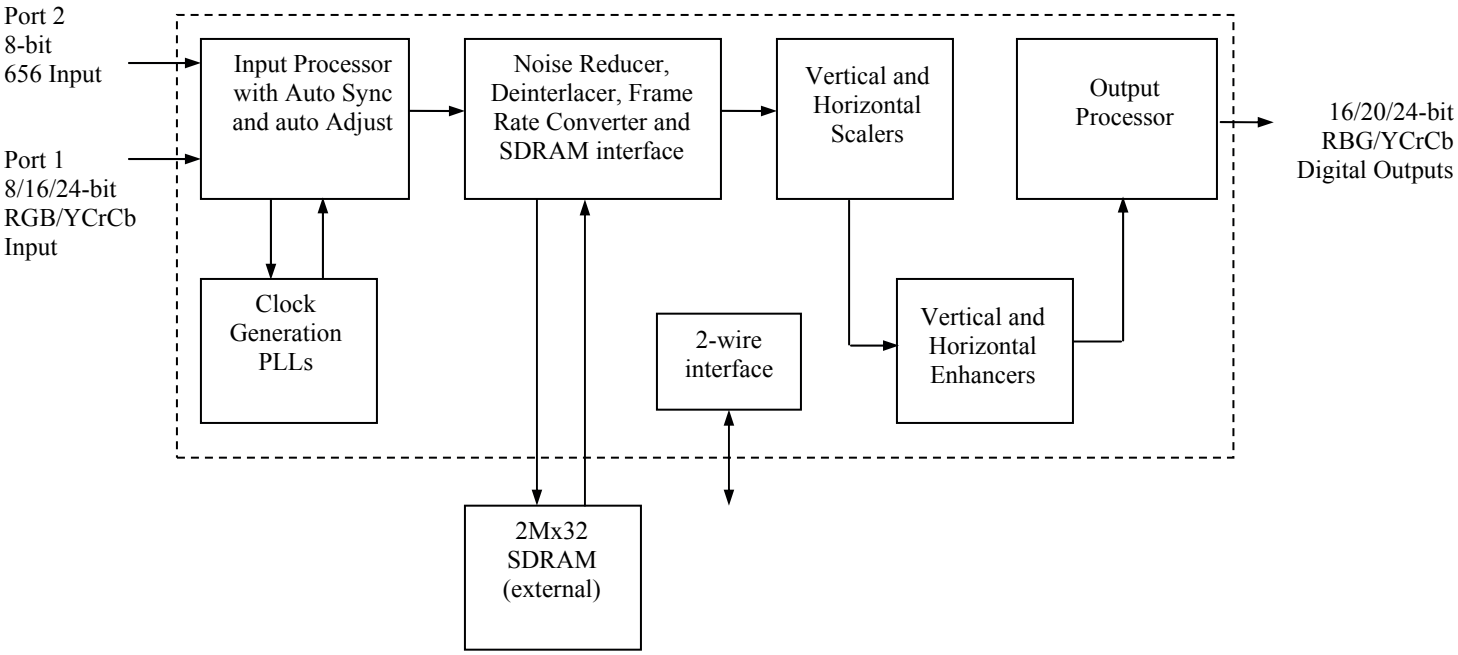
Lead Free

Publication number: C0702-DAT-15A

Publication date: November 2004

2 BLOCK DIAGRAMS

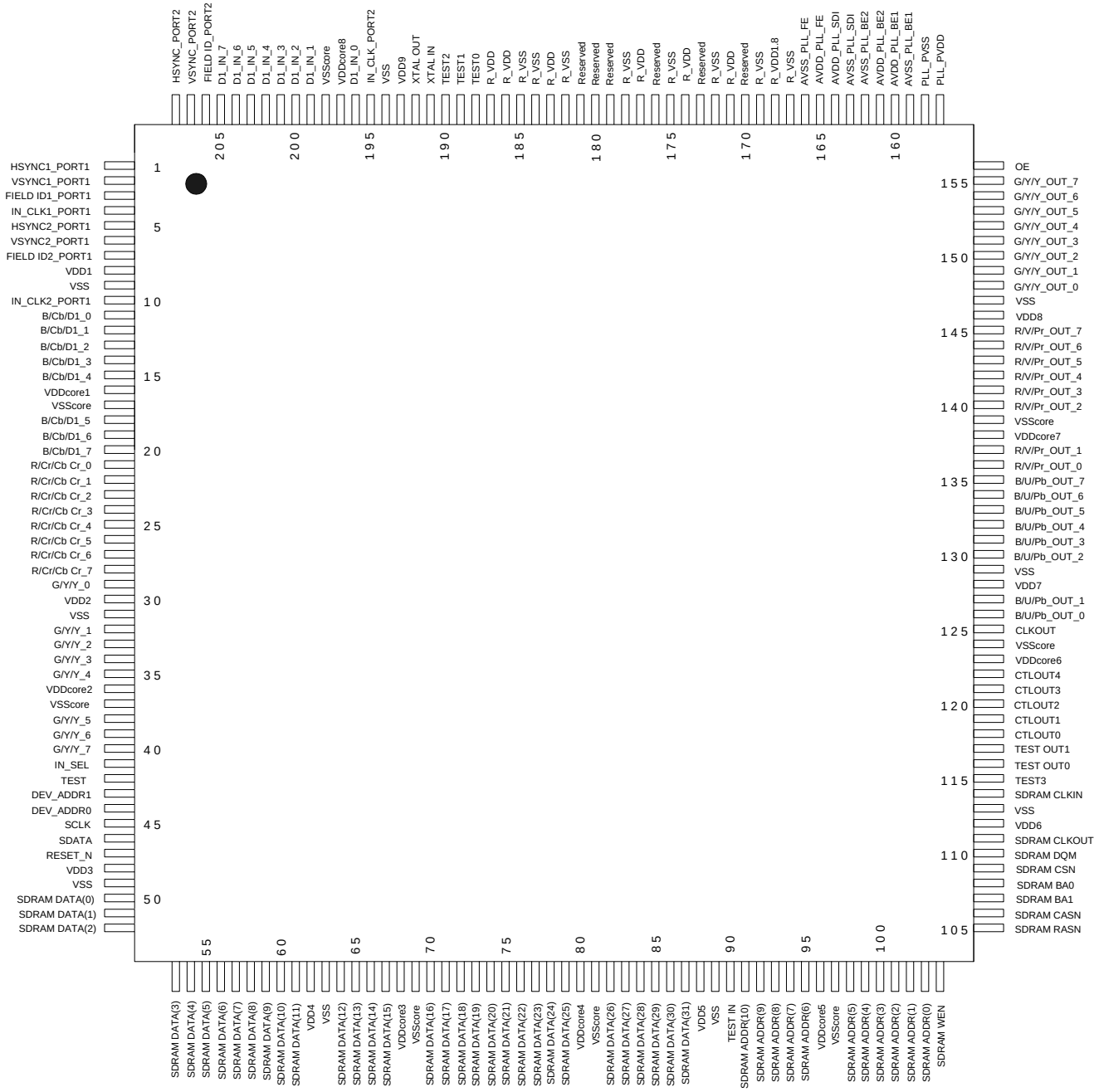
Figure 2.1: FLI2310 – Simplified Internal Block Diagram



3 PIN INFORMATION

3.1 Pin Diagram

Figure 3.1: Pinout Information



Package: 208-pin PQFP

3.2 Pin details

Table 3.1: FLI2310 pin details

Pin No	Pin Name	I/O Type	Voltage Tolerance	Drive	Internal Pull up/ Pulldown	Description
1	HSYNC1_PORT1	Input	5v			Horizontal sync or reference -CTL1 of Port 1
2	VSYNC1_PORT1	Input	5v			Vertical sync or reference -CTL1 of Port 1
3	FIELD ID1_PORT1	Input	5v			Odd/Even Field identification -CTL1 of Port 1
4	IN_CLK1_PORT1	Input	5v			Data Clock input -CTL1 of Port 1
5	HSYNC2_PORT1	Input	5v			Horizontal sync or reference –CTL2 of Port 1
6	VSYNC2_PORT1	Input	5v			Vertical sync or reference –CTL2 of Port 1
7	FIELD ID2_PORT1	Input	5v			Odd/Even Field identification –CTL2 of Port 1
8	VDD1	Power				3.3 V - Power pin for IO
9	VSS	Ground				Ground
10	IN_CLK2_PORT1	Input	5v			Data Clock input –CTL2 of Port 1
11	B/Cb/D1_0	Input	5v			Port 1 – Digital video input (Blue/Cb/D1)
12	B/Cb/D1_1	Input	5v			Port 1 – Digital video input (Blue/Cb/D1)
13	B/Cb/D1_2	Input	5v			Port 1 – Digital video input (Blue/Cb/D1)
14	B/Cb/D1_3	Input	5v			Port 1 – Digital video input (Blue/Cb/D1)
15	B/Cb/D1_4	Input	5v			Port 1 – Digital video input (Blue/Cb/D1)
16	VDDcore1	Power				1.8 V - Power pin for core
17	VSScore	Ground				Ground
18	B/Cb/D1_5	Input	5v			Port 1 – Digital video input (Blue/Cb/D1)
19	B/Cb/D1_6	Input	5v			Port 1 – Digital video input (Blue/Cb/D1)
20	B/Cb/D1_7	Input	5v			Port 1 – Digital video input (Blue/Cb/D1)
21	R/Cr/Cb Cr_0	Input	5v			Port 1 – Digital video input (Red/Cr/CrCb)
22	R/Cr/Cb Cr_1	Input	5v			Port 1 – Digital video input (Red/Cr/CrCb)
23	R/Cr/Cb Cr_2	Input	5v			Port 1 – Digital video input (Red/Cr/CrCb)
24	R/Cr/Cb Cr_3	Input	5v			Port 1 – Digital video input (Red/Cr/CrCb)
25	R/Cr/Cb Cr_4	Input	5v			Port 1 – Digital video input (Red/Cr/CrCb)
26	R/Cr/Cb Cr_5	Input	5v			Port 1 – Digital video input (Red/Cr/CrCb)
27	R/Cr/Cb Cr_6	Input	5v			Port 1 – Digital video input (Red/Cr/CrCb)
28	R/Cr/Cb Cr_7	Input	5v			Port 1 – Digital video input (Red/Cr/CrCb)
29	G/Y/Y_0	Input	5v			Port 1 – Digital video input (Green/Y)
30	VDD2	Power				3.3 V - Power pin for IO
31	VSS	Ground				Ground
32	G/Y/Y_1	Input	5v			Port 1 – Digital video input (Green/Y)
33	G/Y/Y_2	Input	5v			Port 1 – Digital video input (Green/Y)
34	G/Y/Y_3	Input	5v			Port 1 – Digital video input (Green/Y)
35	G/Y/Y_4	Input	5v			Port 1 – Digital video input (Green/Y)
36	VDDcore2	Power				1.8 V - Power pin for core
37	VSScore	Ground				Ground
38	G/Y/Y_5	Input	5v			Port 1 – Digital video input (Green/Y)
39	G/Y/Y_6	Input	5v			Port 1 – Digital video input (Green/Y)
40	G/Y/Y_7	Input	5v			Port 1 – Digital video input (Green/Y)
41	IN_SEL	Output	5v	8 mA		Output to select external video mux
42	TEST	Input	5v			Connect to Ground
43	DEV_ADDR1	Input	5v			Device address setting 1

Pin No	Pin Name	I/O Type	Voltage Tolerance	Drive	Internal Pull up/ Pulldown	Description
44	DEV_ADDR0	Input	5v			Device address setting 0
45	SCLK	I/O	5v	8 mA		2-wire serial control bus clock
46	SDATA	I/O	5v	8 mA		2-wire serial control bus data
47	RESET_N	Input	5v		PU	Reset
48	VDD3	Power				3.3 V – Power pin for IO
49	VSS	Ground				Ground
50	SDRAM DATA(0)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
51	SDRAM DATA(1)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
52	SDRAM DATA(2)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
53	SDRAM DATA(3)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
54	SDRAM DATA(4)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
55	SDRAM DATA(5)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
56	SDRAM DATA(6)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
57	SDRAM DATA(7)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
58	SDRAM DATA(8)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
59	SDRAM DATA(9)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
60	SDRAM DATA(10)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
61	SDRAM DATA(11)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
62	VDD4	Power				3.3 V – Power pin for IO
63	VSS	Ground				Ground
64	SDRAM DATA(12)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
65	SDRAM DATA(13)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
66	SDRAM DATA(14)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
67	SDRAM DATA(15)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
68	VDDcore3	Power				1.8 V - Power pin for core
69	VSScore	Ground				Ground
70	SDRAM DATA(16)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
71	SDRAM DATA(17)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
72	SDRAM DATA(18)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
73	SDRAM DATA(19)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
74	SDRAM DATA(20)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
75	SDRAM DATA(21)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
76	SDRAM DATA(22)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
77	SDRAM DATA(23)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
78	SDRAM DATA(24)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
79	SDRAM DATA(25)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
80	VDDcore4	Power				1.8 V – Power pin for core
81	VSScore	Ground				Ground
82	SDRAM DATA(26)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
83	SDRAM DATA(27)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
84	SDRAM DATA(28)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
85	SDRAM DATA(29)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
86	SDRAM DATA(30)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
87	SDRAM DATA(31)	Tristate I/O	5v	4 mA	PD	SDRAM data bus *
88	VDD5	Power				3.3 V – Power pin for IO
89	VSS	Ground				Ground

Pin No	Pin Name	I/O Type	Voltage Tolerance	Drive	Internal Pull up/ Pulldown	Description
90	TEST IN	Input	5V			Test input-Connect to ground
91	SDRAM ADDR(10)	Tristate O/P	5v	8 mA		SDRAM address bus *
92	SDRAM ADDR(9)	Tristate O/P	5v	8 mA		SDRAM address bus *
93	SDRAM ADDR(8)	Tristate O/P	5v	8 mA		SDRAM address bus *
94	SDRAM ADDR(7)	Tristate O/P	5v	8 mA		SDRAM address bus *
95	SDRAM ADDR(6)	Tristate O/P	5v	8 mA		SDRAM address bus *
96	VDDcore5	Power				1.8 V – Power pin for core
97	VSScor	Ground				Ground
98	SDRAM ADDR(5)	Tristate O/P	5v	8 mA		SDRAM address bus *
99	SDRAM ADDR(4)	Tristate O/P	5v	8 mA		SDRAM address bus *
100	SDRAM ADDR(3)	Tristate O/P	5v	8 mA		SDRAM address bus *
101	SDRAM ADDR(2)	Tristate O/P	5v	8 mA		SDRAM address bus *
102	SDRAM ADDR(1)	Tristate O/P	5v	8 mA		SDRAM address bus *
103	SDRAM ADDR(0)	Tristate O/P	5v	8 mA		SDRAM address bus *
104	SDRAM WEN	Tristate O/P	5v	8 mA		SDRAM write enable *
105	SDRAM RASN	Tristate O/P	5v	8 mA		SDRAM row address select *
106	SDRAM CASN	Tristate O/P	5v	8 mA		SDRAM column address select *
107	SDRAM BA1	Tristate O/P	5v	8 mA		SDRAM bank select 1*
108	SDRAM BA0	Tristate O/P	5v	8 mA		SDRAM bank select 0*
109	SDRAM CSN	Tristate O/P	5v	4 mA		SDRAM CS *
110	SDRAM DQM	Tristate O/P	5v	8 mA		SDRAM DQM *
111	SDRAM CLKOUT	Output	5v	12 mA		Clock out to SDRAM *
112	VDD6	Power				3.3 V - Power pin for IO
113	VSS	Ground				Ground
114	SDRAM CLKIN	Input	5v			Trace delayed SDRAM Clock in
115	TEST3	Input				Test input – Connect to ground
116	TEST OUT0	Output		12 mA		Test output – leave open
117	TEST OUT1	Output		8 mA		Test output – leave open
118	CTLOUT0	Tristate O/P	5v	8 mA		Control signal output selectable as HSync1/ CSync/HRef/Monitor coast
119	CTLOUT1	Tristate O/P	5v	8 mA		Control signal output selectable as VSync1/CRef/VRef/Film Indicator
120	CTLOUT2	Tristate O/P	5v	8 mA		Control signal output selectable as Monitor coast/HRef/VDD_en / HSync2
121	CTLOUT3	Tristate O/P	5v	8 mA		Control signal output selectable as Film Indicator/VRef/backlight_en/VSync2
122	CTLOUT4	Tristate O/P	5v	8 mA		Control signal output selectable as CRef/Field ID/CSync/Monitor coast
123	VDDcore6	Power				1.8 V - Power pin for core
124	VSScore	Ground				Ground
125	CLKOUT	Tristate O/P	5v	12 mA		Output data rate clock
126	B/U/Pb_OUT_0	Tristate O/P	5v	8 mA		Digital video output – Blue/U/Pb
127	B/U/Pb_OUT_1	Tristate O/P	5v	8 mA		Digital video output – Blue/U/Pb
128	VDD7	Power				3.3 V – Power pin for IO
129	VSS	Ground				Ground
130	B/U/Pb_OUT_2	Tristate O/P	5v	8 mA		Digital video output – Blue/U/Pb
131	B/U/Pb_OUT_3	Tristate O/P	5v	8 mA		Digital video output – Blue/U/Pb

Pin No	Pin Name	I/O Type	Voltage Tolerance	Drive	Internal Pull up/ Pulldown	Description
132	B/U/Pb_OUT_4	Tristate O/P	5v	8 mA		Digital video output – Blue/U/Pb
133	B/U/Pb_OUT_5	Tristate O/P	5v	8 mA		Digital video output – Blue/U/Pb
134	B/U/Pb_OUT_6	Tristate O/P	5v	8 mA		Digital video output – Blue/U/Pb
135	B/U/Pb_OUT_7	Tristate O/P	5v	8 mA		Digital video output – Blue/U/Pb
136	R/V/Pr_OUT_0	Tristate O/P	5v	8 mA		Digital video output – Red/V/Pr
137	R/V/Pr_OUT_1	Tristate O/P	5v	8 mA		Digital video output – Red/V/Pr
138	VDDcore7	Power				1.8 V – Power pin for core
139	VSScore	Ground				Ground
140	R/V/Pr_OUT_2	Tristate O/P	5v	8 mA		Digital video output – Red/V/Pr
141	R/V/Pr_OUT_3	Tristate O/P	5v	8 mA		Digital video output – Red/V/Pr
142	R/V/Pr_OUT_4	Tristate O/P	5v	8 mA		Digital video output – Red/V/Pr
143	R/V/Pr_OUT_5	Tristate O/P	5v	8 mA		Digital video output – Red/V/Pr
144	R/V/Pr_OUT_6	Tristate O/P	5v	8 mA		Digital video output – Red/V/Pr
145	R/V/Pr_OUT_7	Tristate O/P	5v	8 mA		Digital video output – Red/V/Pr
146	VDD8	Power				3.3 V – Power pin for IO
147	VSS	Ground				Ground
148	G/Y/Y_OUT_0	Tristate O/P	5v	8 mA		Digital video output – Green/Y
149	G/Y/Y_OUT_1	Tristate O/P	5v	8 mA		Digital video output – Green/Y
150	G/Y/Y_OUT_2	Tristate O/P	5v	8 mA		Digital video output – Green/Y
151	G/Y/Y_OUT_3	Tristate O/P	5v	8 mA		Digital video output – Green/Y
152	G/Y/Y_OUT_4	Tristate O/P	5v	8 mA		Digital video output – Green/Y
153	G/Y/Y_OUT_5	Tristate O/P	5v	8 mA		Digital video output – Green/Y
154	G/Y/Y_OUT_6	Tristate O/P	5v	8 mA		Digital video output – Green/Y
155	G/Y/Y_OUT_7	Tristate O/P	5v	8 mA		Digital video output – Green/Y
156	OE	Input	5v			Output data enable for Digital video output
157	PLL_PVDD	Power				1.8 V – Power pin for PLL pads
158	PLL_PVSS	Ground				Ground for PLL pads
159	AVSS_PLL_BE1	Ground				PLL Ground
160	AVDD_PLL_BE1	Power				1.8 V – Power pin for PLL
161	AVDD_PLL_BE2	Power				1.8 V – Power pin for PLL
162	AVSS_PLL_BE2	Ground				PLL Ground
163	AVSS_PLL_SDI	Ground				PLL Ground
164	AVDD_PLL_SDI	Power				1.8 V – Power pin for PLL
165	AVDD_PLL_FE	Power				1.8 V – Power pin for PLL
166	AVSS_PLL_FE	Ground				PLL Ground
167	R_VSS	Ground				Ground
168	R_VDD1.8	Power				1.8 V
169	R_VSS	Ground				Ground
170	Reserved	-				Leave open
171	R_VDD	Power				3.3 V
172	R_VSS	Ground				Ground
173	Reserved	-				Leave open
174	R_VDD	Power				3.3 V
175	R_VSS	Ground				Ground
176	Reserved	-				Leave open
177	R_VDD	Power				3.3 V

Pin No	Pin Name	I/O Type	Voltage Tolerance	Drive	Internal Pull up/ Pulldown	Description
178	R_VSS	Ground				Ground
179	Reserved	-				Leave open
180	Reserved	-				Leave open
181	Reserved	-				Leave open
182	R_VSS	Ground				Ground
183	R_VDD	Power				3.3 V
184	R_VSS	Ground				Ground
185	R_VSS	Ground				Ground
186	R_VDD	Power				3.3 V
187	R_VDD	Power				3.3 V
188	TEST0	Input	5v			Test pin – connect to ground
189	TEST1	Input	5v			Test pin – connect to ground
190	TEST2	Input	5v			Test pin – connect to ground
191	XTAL IN	Input				External parallel crystal oscillator
192	XTAL OUT	Output				External parallel crystal oscillator
193	VDD9	Power				3.3 V - Power pin for IO
194	VSS	Ground				Ground
195	IN_CLK_PORT 2	Input	5v	4 mA		Port 2 - Data Clock input
196	D1_IN_0	Input	5v	4 mA		Port 2 - ITU-R BT656 digital data input
197	VDDcore8	Power				1.8 V – Power pin for core
198	VSScore	Ground				Ground
199	D1_IN_1	Input	5v	4 mA		Port 2 - ITU-R BT656 digital data input
200	D1_IN_2	Input	5v	4 mA		Port 2 - ITU-R BT656 digital data input
201	D1_IN_3	Input	5v	4 mA		Port 2 - ITU-R BT656 digital data input
202	D1_IN_4	Input	5v	4 mA		Port 2 - ITU-R BT656 digital data input
203	D1_IN_5	Input	5v	4 mA		Port 2 - ITU-R BT656 digital data input
204	D1_IN_6	Input	5v	4 mA		Port 2 - ITU-R BT656 digital data input
205	D1_IN_7	Input	5v	4 mA		Port 2 - ITU-R BT656 digital data input
206	FIELD ID_PORT 2	Input	5v	4 mA		Port 2 - Odd/Even Field identification
207	VSYNC_ PORT 2	Input	5v	4 mA		Port 2 - Vertical sync or reference
208	HSYNC_PORT 2	Input	5v	4 mA		Port 2 - Horizontal sync or reference

Note: 1) * - The connection of these pins depends on the type of external SDRAM used. See Appendix 3
2) For 16/20 bit Y and muxed C output modes see Appendix 2 for pin configuration

ROHM 1/4

STRUCTURE Silicon Monolithic Integrated Circuit

TYPE **BU2098F**

FUNCTION 8bit Serial IN / Parallel Out Driver

FEATURES 1) Compatible with I^2C BUS

2) Nch open drain, capable of driving a maximum of 25mA

3) 18V high voltage output can be used.

● ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{DD}	7.0*	V
Power Dissipation	Pd	300	mW
Operating Temperature Range	T_{opr}	-40～+85	℃
Storage Temperature Range	T_{stg}	-55～+125	℃
Input Voltage	V_{IN}	-0.5～V_{DD}+0.5	V

* Output (Q0～Q7) are 18V (Max.)

・Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any difference in translation version of this document, formal version takes priority.

Rev.B

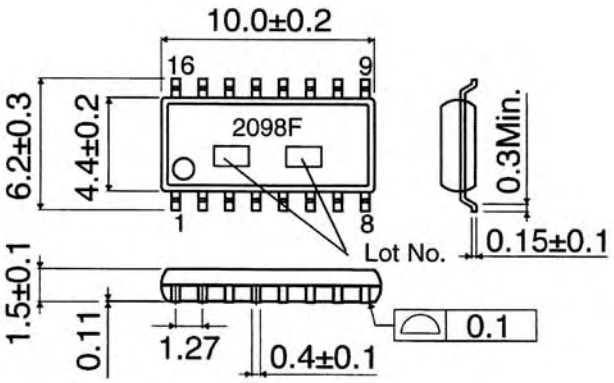
ROHM 2/4

● ELECTRICAL CHARACTERISTICS (unless otherwise noted, Ta=25℃, V_{DD}=5.0V)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Power Supply Voltage range	V_{DD}	2.7	-	5.5	V	VDD pin
Output Voltage range	V_o	0	-	15.0	V	
Supply current	I_{cc1}	-	-	2.0	μA	Static supply current
Input "H" voltage	V_{IH}	0.7	-	-	V/V	Ratio against VDD
Input "L" voltage	V_{IL}	-	-	0.3	V/V	Ratio against VDD
Output "L" voltage	V_{OL}	-	-	0.4	V	
Input "L" current	I_{IL}	-	-	2.0	μA	Vin=0
Input "L" current	I_{IH}	-	-	-2.0	μA	Vin=VDD
Output Leakage current	I_L	-	-	±5.0	μA	Output=OPEN,Vout=VDD
Data Minimum set up time	t_1	100	-	-	n S	High speed mode
Data hold time	t_2	-	-	900	nS	High speed mode
Minimum shift pulse width (High speed mode)	t_{31}	0	-	400	KHz	
Minimum shift pulse width (normal mode)	t_{32}	0	-	100	KHz	

This product is not assessed whether to be strategic materials in foreign exchange and trade law or not, so please confirm at trading. This product is not deigned against radioactive ray.

● PHYSICAL DIMENSIONS



SOP16 (UNIT : mm)

Rev.B

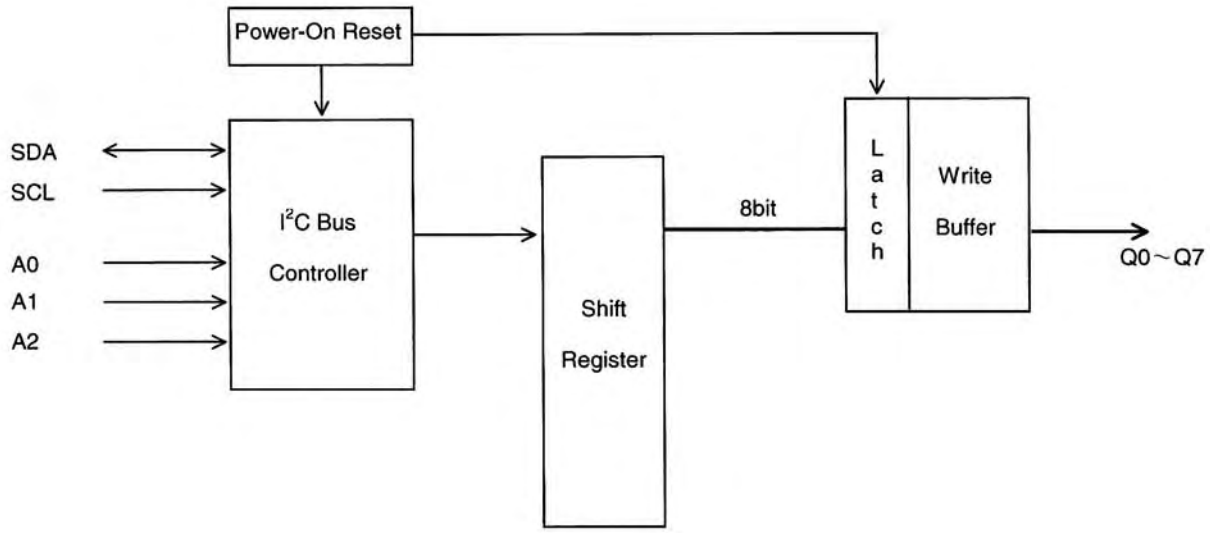
ROHM 3/4

● Pin Description

Pin. No	Terminal	Symbol	Function
14	SCL	C	Shift pulse for shift register
15	SDA	S_I	Data input for shift register, data is set at rising edge of shift pulse
1	A0	A_o	Address input 0
2	A1	A_1	Address input 1
3	A2	A_2	Address input 2
4	Q0	O_0	1st bit output, it becomes "1" when data in register is "1"
5	Q1	O_1	2nd bit output, it becomes "1" when data in register is "1"
6	Q2	O_2	3rd bit output, it becomes "1" when data in register is "1"
7	Q3	O_3	4th bit output, it becomes "1" when data in register is "1"
9	Q4	O_4	5th bit output, it becomes "1" when data in register is "1"
10	Q5	O_5	6th bit output, it becomes "1" when data in register is "1"
11	Q6	O_6	7th bit output, it becomes "1" when data in register is "1"
12	Q7	O_7	8th bit output, it becomes "1" when data in register is "1"
13	NC	NC	NC pin
8	VSS	GND	GND
16	VDD	VDD	Power supply

ROHM 4/4

● BLOCK DIAGRAM



● NOTES FOR USE

(1) Absolute maximum ratings
Exceeding the absolute maximum ratings, including applied voltage and operating temperature range, may damage or destroy the IC. Since the cause of the damage cannot be conclusively identified (as, for example, a short or open mode), be sure to take appropriate physical safety measures, such as incorporating fuses, whenever a special mode anticipated to exceed absolute maximum ratings is employed.

(2) Ground Potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode.

(3) Thermal design
Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.

(4) Electromagnetic fields
Use in strong electromagnetic fields may cause malfunctions. Be careful operating in electromagnetic fields.

(5) Ground wiring pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

Rev.B

Multiformat 216 MHz Video Encoder with Six NSV® 12-Bit DACs

ADV7320/ADV7321

FEATURES

High definition input formats
- 16-/20-, 24-/30-bit (4:2:2, 4:4:4) parallel YCrCb

Fully compliant with:
- SMPTE 274M (1080i, 1080p @ 74.25 MHz)
- SMPTE 296M (720p)
- SMPTE 240M (1035i)
- RGB in 3- × 10-bit 4:4:4 input format

HDTV RGB supported:
- RGB, RGBHV
- Other high definition formats using async timing mode

Enhanced definition input formats
- 8-/10-, 16-/20-, 24-/30-bit (4:2:2, 4:4:4) parallel YCrCb
- SMPTE 293M (525p)
- BTA T-1004 EDTV2 (525p)
- ITU-R BT.1358 (625p/525p)
- ITU-R BT.1362 (625p/525p)
- RGB in 3- × 10-bit 4:4:4 input format

Standard definition input formats
- CCIR-656 4:2:2 8-/10-bit or 16-/20-bit parallel input

High definition output formats
- YPrPb HDTV (EIA 770.3)
- RGB, RGBHV
- CGMS-A (720p/1080i)

Enhanced definition output formats
- Macrovision Rev 1.2 (525p/625p) (ADV7320 only)
- CGMS-A (525p/625p)
- YPrPb progressive scan (EIA-770.1, EIA-770.2)
- RGB, RGBHV

Standard definition output formats
- Composite NTSC M/N
- Composite PAL M/N/B/D/G/H/I, PAL-60
- SMPTE 170M NTSC-compatible composite video
- ITU-R BT.470 PAL-compatible composite video
- S-video (Y/C)
- EuroScart RGB
- Component YPrPb (Betacam, MII, SMPTE/EBU N10)
- Macrovision Rev 7.1.L1 (ADV7320 only)
  - CGMS/WSS
  - Closed captioning

GENERAL FEATURES

Simultaneous SD/HD, PS/SD inputs and outputs
Oversampling up to 216 MHz
Programmable DAC gain control
Sync outputs in all modes
On-board voltage reference
Six 12-bit NSV (noise shaped video) precision video DACs
2-wire serial I²C® interface, open-drain configuration
Dual I/O supply 2.5 V/3.3 V operation
Analog and digital supply 2.5 V
On-board PLL
64-lead LQFP package
Lead (Pb) free product

APPLICATIONS

EVD players (enhanced versatile disk)
High end /SD/PS DVD recorders/players
SD/progressive scan/HDTV display devices
SD/HDTV set top boxes
Professional video systems

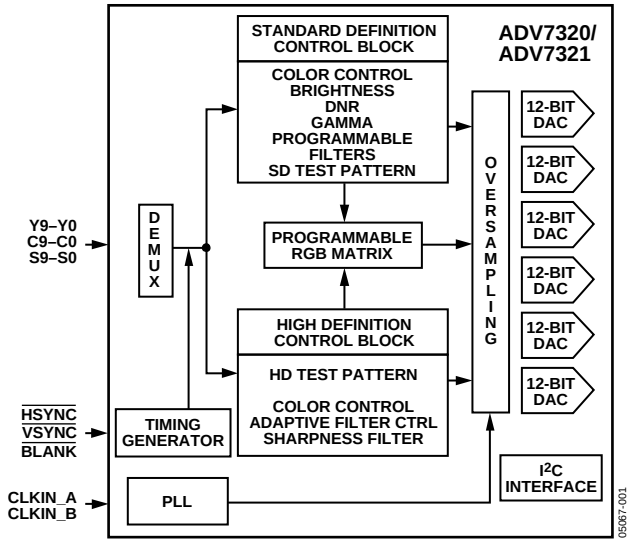


Figure 1. Simplified Functional Block Diagram

GENERAL DESCRIPTION

The ADV®7320/ADV7321 are high speed, digital-to-analog encoders on single monolithic chips. They include six high speed NSV video D/A converters with TTL compatible inputs. They have separate 8-/10-, 16-/20-, and 24-/30-bit input ports that accept data in high definition and/or standard definition video format. For all standards, external horizontal, vertical, and blanking signals or EAV/SAV timing codes control the insertion of appropriate synchronization signals into the digital data stream and, therefore, the output signal.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

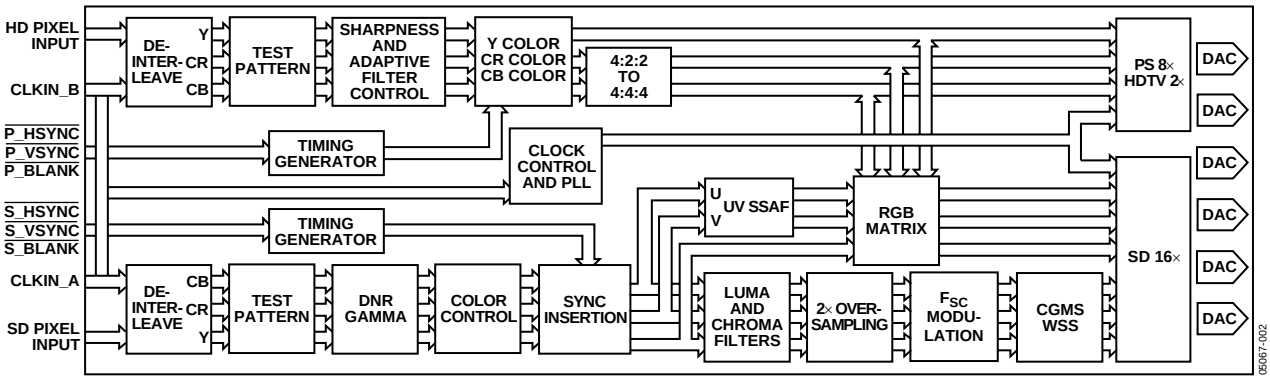


Figure 2. Detailed Functional Block Diagram

TERMINOLOGY

SD: standard definition video, conforming to ITU-R BT.601/ITU-R BT.656.

HD: high definition video, i.e., 720p/1080i/1035i.

EDTV: enhanced definition television (525p/625p)

PS: progressive scan video, conforming to SMPTE 293M, ITU-R BT.1358, BTAT-1004EDTV2, or ITU-R BT.13621362.

HDTV: high definition television video, conforming to SMPTE 274M, or SMPTE 296M and SMPTE240M.

YCrCb SD, PS, or HD component: digital video.

YPrPb SD, PS, or HD component: analog video.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

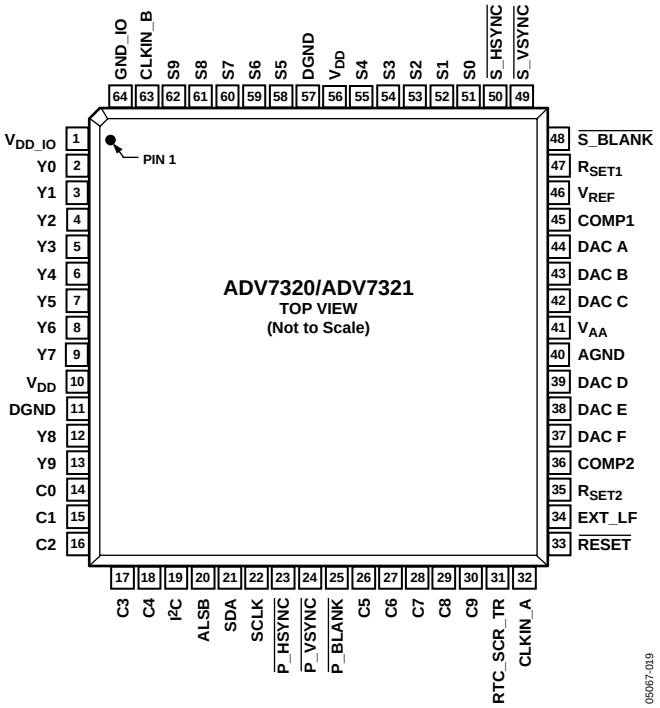


Figure 19. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Input/Output	Description
11, 57	DGND	G	Digital Ground.
40	AGND	G	Analog Ground.
32	CLKIN_A	I	Pixel Clock Input for HD (74.25 MHz Only, PS Only (27 MHz), SD Only (27 MHz).
63	CLKIN_B	I	Pixel Clock Input. Requires a 27 MHz reference clock for progressive scan mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV mode. This clock is only used in dual modes.
45, 36	COMP1, COMP2	O	Compensation Pin for DACs. Connect 0.1 µF capacitor from COMP pin to V_{AA}.
44	DAC A	O	CVBS/Green/Y/Y Analog Output.
43	DAC B	O	Chroma/Blue/U/Pb Analog Output.
42	DAC C	O	Luma/Red/V/Pr Analog Output.
39	DAC D	O	In SD Only Mode: CVBS/Green/Y Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Y/Green [HD] Analog Output.
38	DAC E	O	In SD Only Mode: Luma/Blue/U Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Pr/Red Analog Output.
37	DAC F	O	In SD Only Mode: Chroma/Red/V Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Pb/Blue [HD] Analog Output.
23	$\overline{\text{P\_HSYNC}}$	I	Video Horizontal Sync Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
24	$\overline{\text{P\_VSYNC}}$	I	Video Vertical Sync Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
25	$\overline{\text{P\_BLANK}}$	I	Video Blanking Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
48	$\overline{\text{S\_BLANK}}$	I/O	Video Blanking Control Signal for SD Only.
49	$\overline{\text{S\_VSYNC}}$	I/O	Video Vertical Sync Control Signal for SD Only.
50	$\overline{\text{S\_HSYNC}}$	I/O	Video Horizontal Sync Control Signal for SD Only.
13,12, 9–2	Y9 to Y0	I	SD or Progressive Scan/HDTV Input Port for Y Data. Input port for interleaved progressive scan data. The LSB is set up on Pin Y0. For 8-bit data input, LSB is set up on Y2.
30–26, 18–14	C9 to C0	I	Progressive Scan/HDTV Input Port 4:4:4 Input Mode. This port is used for the Cb[Blue/U] data. The LSB is set up on Pin C0. For 8-bit data input, LSB is set up on C2.

ADV7320/ADV7321

Pin No.	Mnemonic	Input/Output	Description
62–58, 55–51	S9 to S0	I	SD or Progressive Scan/HDTV Input Port for Cr[Red/V] Data in 4:4:4 Input Mode. LSB is set up on Pin S0. For 8-bit data input, LSB is set up on S2.
33	$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7320/ADV7321 into default register setting. $\overline{\text{RESET}}$ is an active low signal.
47, 35	R_{SET1}, R_{SET2}	I	A 3040 Ω resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs.
22	SCLK	I	I^2C Port Serial Interface Clock Input.
21	SDA	I/O	I^2C Port Serial Data Input/Output.
20	ALSB	I	TTL Address Input. This signal sets up the LSB of the I^2C address. When this pin is tied low, the I^2C filter is activated, which reduces noise on the I^2C interface.
1	V_{DD_IO}	P	Power Supply for Digital Inputs and Outputs.
10, 56	V_{DD}	P	Digital Power Supply.
41	V_{AA}	P	Analog Power Supply.
46	V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
34	EXT_LF	I	External Loop Filter for the Internal PLL.
31	RTC_SCR_TR	I	Multifunctional Input. Real-time control (RTC) input, timing reset input, subcarrier reset input.
19	I^2C	I	This input pin must be tied high (V_{DD_IO}) for the ADV7320/ADV7321 to interface over the I^2C port.
64	GND_IO		Digital Input/Output Ground.

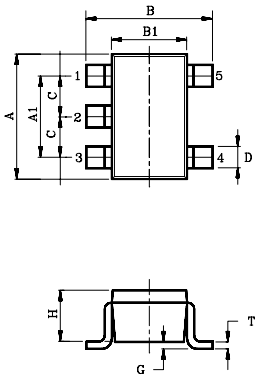
KEC SEMICONDUCTOR TECHNICAL DATA

KIC7S66FU

SILICON MONOLITHIC CMOS
DIGITAL INTEGRATED CIRCUIT

BILATERAL SWITCH

The KIC7S66FU is a high speed C^2MOS BILATERAL SWITCH fabricated with silicon gate C^2MOS technology. It consists of a high speed switch capable of controlling either digital or analog signals while maintaining the C^2MOS low power dissipation.
Control input (C) is provided to control the switch.
The switch turns ON while the C linput is high, and the switch turns OFF while low.
Input is equipped with protection circuits against static discharge or transient excess voltage.



DIM	MILLIMETERS
A	2.00± 0.20
A1	1.3± 0.1
B	2.1± 0.1
B1	1.25± 0.1
C	0.65
D	0.2+0.10/−0.05
G	0~0.1
H	0.9± 0.1
T	0.15+0.1/−0.05

USV

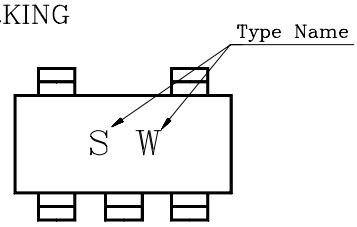
FEATURES

- High Speed : t_{pd}=7ns(Typ.) at V_{CC}=5V.
- Low Power Dissipation : I_{CC}=1μA(Max.) at Ta=25℃.
- High Noise Immunity : V_{NIH}=V_{NIL}=28% V_{CC}(Min.).
- Low ON Resistance : R_{ON}=100Ω(Typ.) at V_{CC}=9V.
- Low T.H.D : THD=0.05%(Typ.) at V_{CC}=5V.

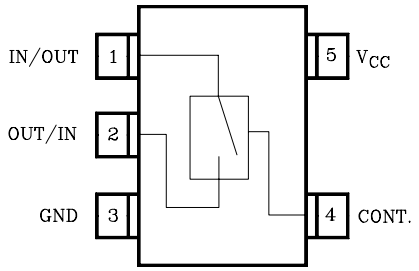
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{CC}	-0.5~10	V
Control Input Voltage	V_{IN}	-0.5~V_{CC}+0.5	V
Swith I/O Voltage	$V_{I/O}$	-0.5~V_{CC}+0.5	V
Control Diode Current	I_{CK}	±20	mA
Output Diode Current	I_{IOK}	±20	mA
Through I/O Current	I_T	±12.5	mA
DC V_{CC}/Ground Current	I_{CC}	±25	mA
Power Dissipation	P_D	200	mW
Storage Temperature	T_{stg}	-65~150	℃
Lead Temperature (10s)	T_L	260	℃

MARKING



PIN CONNECTION(TOP VIEW)



KIC7S66FU

LOGIC DIAGRAM

TRUTH TABLE

CONTROL	SWITCH FUNCTION
H	ON
L	OFF

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2~9	V
Control Input Voltage	V_{IN}	0~V_{CC}	V
Switch I/O Voltage	$V_{I/O}$	0~V_{CC}	V
Operating Temperature	T_{opr}	-40~85	℃
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0~ 500 (V_{CC}=4.5V) 0~ 400 (V_{CC}=6.0V) 0~ 250 (V_{CC}=9.0V)	ns

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION		Ta=25℃			Ta=-40~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Control Input Voltage	V_{IHC}	-	2.0 4.5 9.0	1.5 3.15 6.3	- - -	- - -	1.5 3.15 6.3	- - -	V
Low-Level Control Input Voltage	V_{ILC}	-	2.0 4.5 9.0	- - -	- - -	0.5 1.35 2.7	- - -	0.5 1.35 2.7	V
ON Resistance	R_{ON}	V_{IN}=V_{IHC} $V_{I/O}$=V_{CC} to GND $V_{I/O}$≦1mA	4.5 9.0	- -	192 110	340 170	- -	400 200	Ω
		V_{IN}=V_{IHC} $V_{I/O}$=V_{CC} to GND $V_{I/O}$≦1mA	2.0 4.5 9.0	- - -	320 140 100	- 200 150	- - -	- 260 190	
Input/Output Leakage Current (SWITCH OFF)	I_{OFF}	V_{OS}=V_{CC} or GND V_{IS}=GND or V_{CC} V_{IN}=V_{ILC}	9.0	-	-	±100	-	±1000	nA

ZORAN CORPORATION

ZR36707TQCG

DVD 16x Analog Front-end IC Electrical Specification

Revision 1.0 June 29,2004
Print Date: September 15, 2004

TITLE	DOCUMENT NO.	REV.
ZR36707TQCG Electrical Specification		**1.0**
	PAGE **4** OF **44**	

1. Requirements

1.1 General Description

The ZR36707 device is a high performance BiCMOS single chip analog front-end IC that contains the servo functions, RF attenuator, AGC and Programmable equalizer/filter for a DVD drive system, and dual auto laser power control circuit to support the twin pickups or twin lasers system. Programmable functions of the ZR36707 are controlled through a bi-directional serial port and banks of internal registers.

1.1.1 Features

General

- Supports AGC and equalizer/filter for CD 1x to 60x and DVD 1x to 16x (with RX=12.0kΩ , 1% accuracy)
- Low Power operation (650mW typical for 1x DVD mode)
- Bi-directional serial port register access
- Register programmed power management (Sleep mode <5mW)
- Power supply range (4.5 to 5.5volts)
- Supports 3.3V logic outputs
- Small footprint 64-Lead TQFP package

Servo

- Programmable equalizer for the Differential Phase tracking error Detection circuit(DPD)
- 70KHz bandwidth for the focus and PI circuits
- Input programmable gain control amplifier
  (1.2 to 4.3V/V for A,B,C,D (CD_A,B,C,D,E,F)and 3.6 to 12.9V/V for A2,B2,C2,D2, 3bit resolution)
- Servo algebra signals used for optical alignment, seeking, focusing, and track following
  - Pull-In Signal output
  - Mirror Signal output
  - Defect Signal output / BCA(Burst Cutting Area) code output
  - Tracking Error Signal output
    - 3-Beam tracking error detection
    - Differential Phase tracking error Detection
  - Focusing Error Signal output
  - Center Error Signal output

1.1.1 Features (continued)

Channel
- 100MHz bandwidth
- Supports individual RF inputs for DVD(differential or single_ended) and CD(single_ended)
- Supports internal summing mode for RF signal for DVD and CD respectively
- Programmable attenuator (min:-24dB, 4bit resolution)
- Fast attack mode for rapid AGC recovery
- Low drift AGC hold circuitry
- Signal Swing qualification circuit
- Temperature compensated, exponential control AGC
- Supports internal AGC HOLD control function
- Supports four ranges of Programmable cutoff frequency : 1 to 4.0MHz, 3.5 to 12MHz, 11 to 36MHz, 30 to 72MHz
- Programmable boost/equalization of 0 to 11dB
- Single-ended normal outputs for pulse qualification
- Differential normal signal outputs
- ± 20% Fc accuracy (Fc = 1 to 12 MHz)
- ± 15% Fc accuracy (Fc = 11 to 72 MHz)
- Less than 2% total harmonic distortion
- No external filter components required

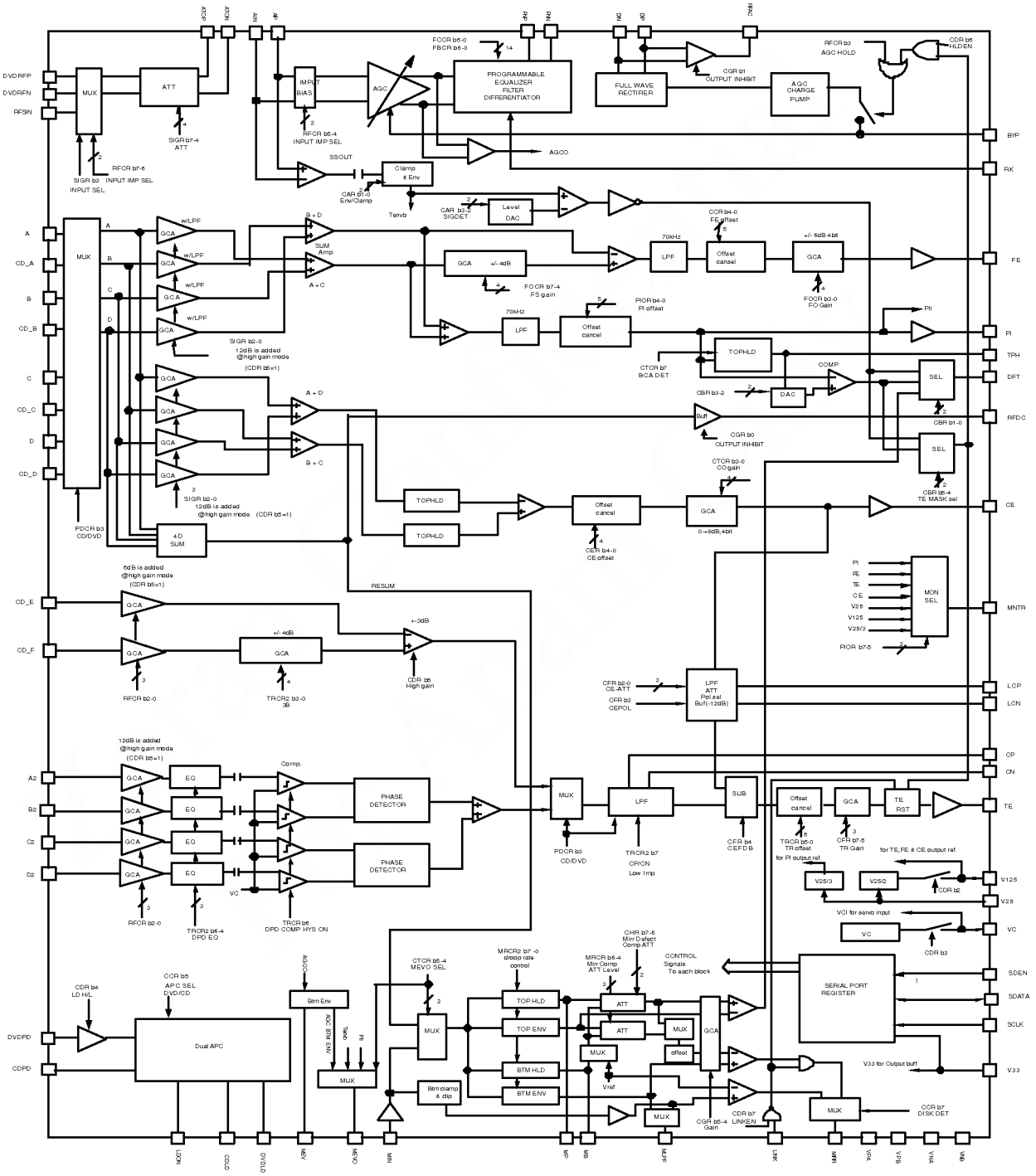
Auto Laser Power Control
- Supports power mode selection
- Provides dual APC circuits for twin laser

VC reference voltage
- Supports VC (VPB/2) reference voltage output for internal and external circuits
- Supports V125(V25/2, reference voltage output) for internal servo output reference voltage

TITLE
ZR36707TQCG Electrical Specification

DOCUMENT NO. REV.
1.0
PAGE 6 OF 44

1.1.2 Block Diagram(Figure 1)



CONTROL REGISTERS(CONTINUED)

1.3PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Power supply pin for the RF block and serial port
VPB	-	Power supply pin for the servo block
VNA	-	Ground pin for the RF block and serial port
VNB	-	Ground pin for the servo block
V33	-	Power supply pin for the output buffers
V25	-	Reference power supply for the servo output

INPUT PINS

NAME	TYPE	DESCRIPTION
DVDRFP,DVDRFN	I	RF SIGNAL INPUTS : Differential RF signal attenuator input pins.
RFSIN	I	RF SIGNAL INPUT : Single-ended RF signal attenuator input pin.
AIP, AIN	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DIP,DIN	I	ANALOG INPUTS FOR RF SINGLE BUFFER: Differential analog inputs to the RF single-end output buffer and full wave rectifier.
A,B,C,D	I	PHOTO DETECTOR INTERFACE INPUTS: Inputs from the main beam Photo detector matrix outputs.
A2,B2,C2,D2	I	PHOTO DETECTOR INTERFACE INPUTS: AC coupled inputs for the DPD from the main beam Photo detector matrix outputs.
CD_A,B,C,D	I	CD PHOTO DETECTOR INTERFACE INPUTS: CD_A,B,C,D come from the CD main beam Photo detector matrix outputs
CD_E,F	I	CD PHOTO DETECTOR INTERFACE INPUTS: CD side beam photo dector outputs and used for the CD tracking detection.
MIN	I	RF SIGNAL INPUT FOR MIRROR: AC coupled inputs for the mirror dection circuit from MEVO.
DVDPD	I	APC INPUT: DVD APC input pin from the monitor photo diode.
CDPD	I	APC INPUT: CD APC input pin from the monitor photo diode.
LDON	I	APC OUTPUT ON/OFF: APC output control pin. A high level activates LD output. (open low)
LINK	I	LINKING SIGNAL INPUT PIN:In the linking area, this pin goes high and the Mirror and TE outputs are disabled, when the link signal is enabled. (open low)
	O	MIRROR MONITOR OUTPUT: Monitor Output signal is selected by CHR bit3-0. Mirror related signal can be obseved from this monitor pin.

PIN DESCRIPTION (continued)

OUTPUT PINS

NAME	TYPE	DESCRIPTION
ATOP, ATON	O	DIFFERENTIAL ATTENUATOR OUTPUTS: Attenuator outputs.
FNP, FNN	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal outputs.
RFAC	O	SINGLE-ENDED NORMAL OUTPUT: Single-ended RF output.
RFDC	O	RF SIGNAL OUTPUT: Single-ended RF summing output reference to VPB-2.4 (V).
FE	O	FOCUSING ERROR SIGNAL OUTPUT: Focus error output reference to V125.
TE	O	TRACKING ERROR SIGNAL OUTPUT: Tracking error output reference to V125.
CE	O	CENTER ERROR SIGNAL OUTPUT: Center error output reference to V125.
MEVO	O	RFDDC BOTTOM ENVELOPE OUTPUT: Bottom envelope, PI or bottom clamped RF envelope signal output for Mirror detection.
DFT	O	DEFECT OUTPUT: CMOS output (V33or VPB). When the PI signal level is below the detection level or when the Rf signal level is below the detection level, the DFT output goes high. This output is selected by serial port.
MIRR	O	MIRROR DETECT OUTPUT: Mirror detect comparator output. CMOS output (V33or VPB).
PI	O	PULL-IN SIGNAL OUTPUT: The summing signal output of A,B,C,D, or CD_A,B,C,D. Reference to V25/3.
DVDLD	O	APC OUTPUT: DVD APC output pin to control the laser power.
CDLD	O	APC OUTPUT: CD APC output pin to control the laser power.
MNTR	O	MONITOR OUTPUT: Monitor Output signal is selected by PIOR bit7-5.

PIN DESCRIPTION (continued)

ANALOG PINS

NAME	TYPE	DESCRIPTION
BYP	-	The RF AGC integration capacitor CBYP, is connected between BYP and VPA.
CP	-	DIFFERENTIAL PHASE TRACKING LPF PIN: The external capacitance is connected between CN.
CN	-	DIFFERENTIAL PHASE TRACKING LPF PIN: The external capacitance is connected between CP.
LCP	-	LENS SHIFT OFFSET CANCEL LPF PIN: The external capacitance is connected between LCN.
LCN	-	LENS SHIFT OFFSET CANCEL LPF PIN: The external capacitance is connected between LCP.
MP	-	MIRR TOP HOLD PIN:The external capacitance is connected to VPB.
MB	-	MIRR BOTTOM HOLD PIN: The external capacitance is connected to VPB.
MEV	-	RFDC BOTTOM ENVELOPE PIN: The external capacitance is connected to VPA.
MLPF	-	MIRROR LPF PIN: An external capacitance is connected to VPB.
TPH	-	PI TOP HOLD PIN: An external capacitance is connected to VPB.
VC	-	REFERENCE VOLTAGE OUTPUT: This pin provides the DC bias reference voltage(VPB/2). Output impedance is less than 50Ω.
V125	-	REFERENCE VOLTAGE OUTPUT: DC bias voltage output and it is also used for servo output reference.(V25/2)
RX	-	REFERENCE RESISTOR INPUT: An external 12.0kΩ, 1% resistor is connected from this pin to ground.

SERIAL PORT PINS

NAME	TYPE	DESCRIPTION
SDEN	I	SERIAL DATA ENABLE: Serial enable CMOS input. A high level input enables the serial port. (not to be left open)
SDATA	I/O	SERIAL DATA: Serial data bidirectional CMOS pin(V33or VPA). NRZ programming data for the internal registers is applied to this input. (not to be left open)
SCLK	I	SERIAL CLOCK: Serial clock CMOS input. The clock applied to this pin is synchronized with the data applied to SDATA. (not to be left open)

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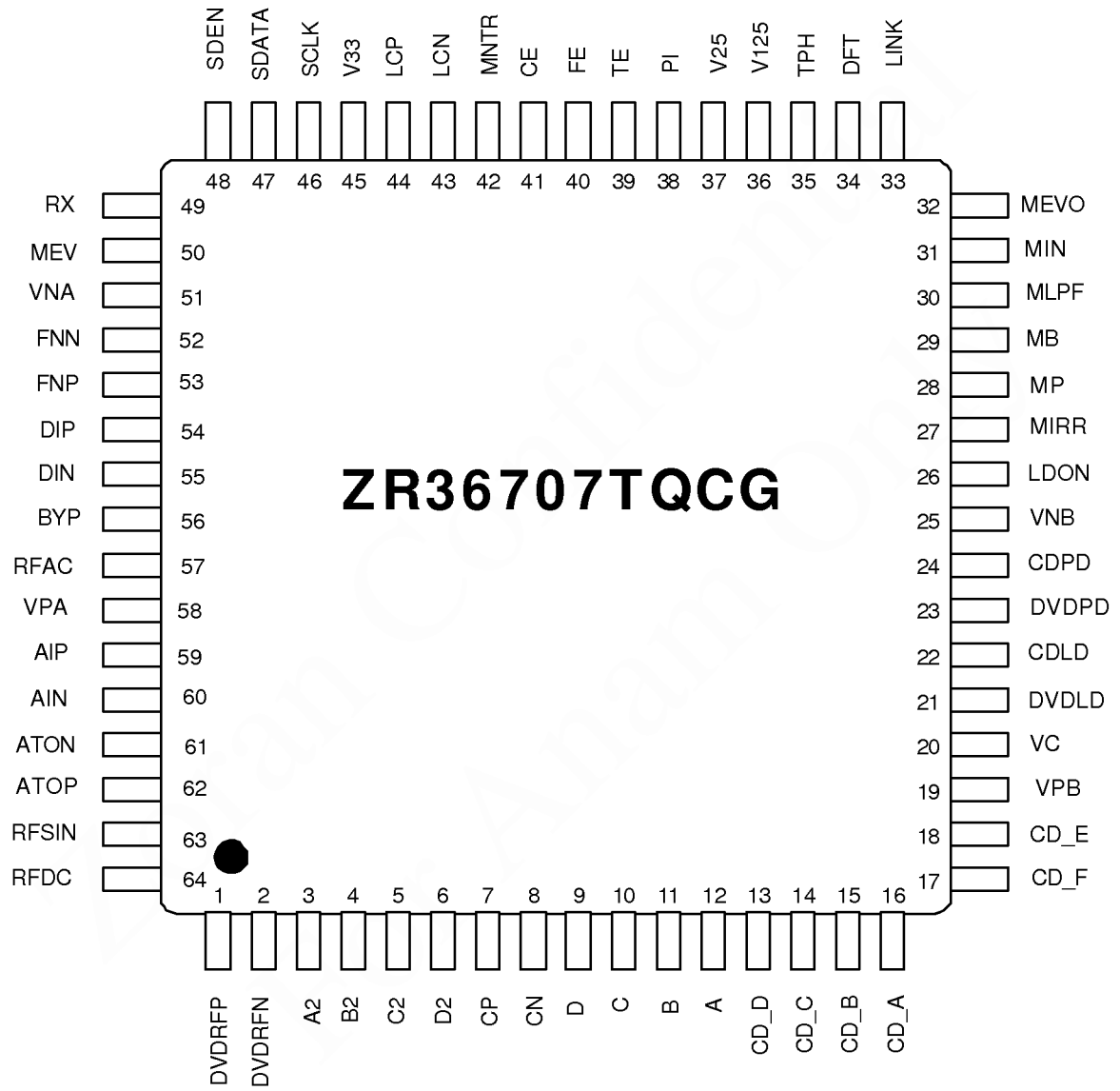
PACKAGE PIN DESIGNATIONS
(Top view)



2k×8 bit electrically erasable PROM

BR24L16-W / BR24L16F-W / BR24L16FJ-W BR24L16FV-W / BR24L16FVM-W

The BR24L16-W series is 2-wire (I^2C BUS type) serial EEPROMs which are electrically programmable.

∗ I^2C BUS is a registered trademark of Philips.

●Applications

General purpose

●Features

1) 2k registers × 8 bits serial architecture.
2) Single power supply (1.8V to 5.5V).
3) Two wire serial interface.
4) Self-timed write cycle with automatic erase.
5) 16 byte page write mode.
6) Low power consumption.
   Write (5V) : 1.2mA (Typ.)
   Read (5V) : 0.2mA (Typ.)
   Standby (5V) : 0.1μA (Typ.)
7) DATA security
   Write protect feature (WP pin) .
   Inhibit to WRITE at low V_{CC}.
8) Small package - - - DIP8 / SOP8 / SOP-J8 / SSOP-B8 / MSOP-8
9) High reliability EEPROM with Double-Cell structure.
10) High reliability fine pattern CMOS technology.
11) Endurance : 1,000,000 erase / write cycles
12) Data retention : 40 years
13) Filtered inputs in SCL•SDA for noise suppression.
14) Initial data FFh in all address.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	−0.3 to +6.5	V
Power dissipation	Pd	800 (DIP8) ∗1	mW
		450 (SOP8) ∗2	
		450 (SOP-J8) ∗3	
		300 (SSOP-B8) ∗4	
		310 (MSOP8) ∗5	
Storage temperature	Tstg	−65 to +125	°C
Operating temperature	Topr	−40 to +85	°C
Terminal voltage	−	−0.3 to V_{CC}+0.3	V

∗1 Degradation is done at 8.0mW/°C for operation above 25°C.
∗2, 3 Degradation is done at 4.5mW/°C for operation above 25°C.
∗4 Degradation is done at 3.0mW/°C for operation above 25°C.
∗5 Degradation is done at 3.1mW/°C for operation above 25°C.

●**Block diagram**

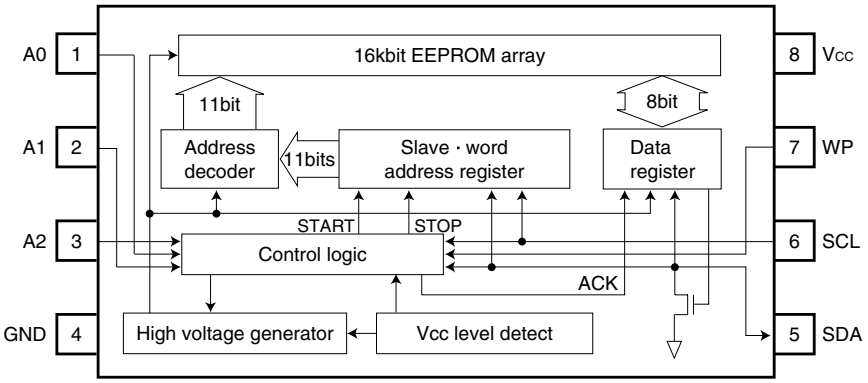


Fig.2 BLOCK DIAGRAM

●**Pin configuration**

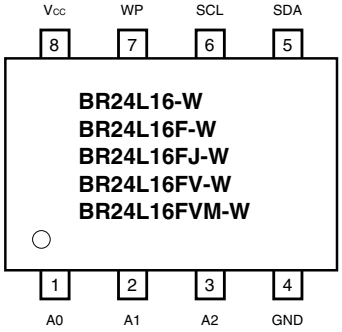


Fig.3 PIN LAYOUT

●**Pin name**

Pin name	I / O	Function
Vcc	–	Power supply
GND	–	Ground (0V)
A0, A1, A2	IN	Out of use
SCL	IN	Serial clock input
SDA	IN / OUT	Slave and word address, serial data input, serial data output ∗1
WP	IN	Write protect input

∗1 An open drain output requires a pull-up resistor.

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Data Sheet

ZR36778HQCG

Vaddis® 778 Advanced Featured DVD SoC

Version 0.9
19 Sep 2004

ZORAN Proprietary

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1 Introduction

1.1 General

This document describes the technical specification of the **Vaddis 778** disc loader controller, flash memory card reader and decoder device.

The **Vaddis 778** can control disc loaders and read bitstreams using the following media: DVD-ROM, DVD-R, DVD+R, DVD-RW, DVD+RW, CD-DA, CD-ROM, CD-ROM (XA), CD-R and CD-RW discs.

The **Vaddis 778** can read the following types of serial and parallel flash memory cards: Secure Digital (SD), Memory Stick (MS and MS Pro), Compact Flash (CF) and Smart Media (SM) and XD.

The **Vaddis 778** can playback all discs conforming to the above standards (including support of sub-pictures, highlights and closed captions) with the exception of DVD-Audio ASV transition effects. The **Vaddis 778** can playback MP3 (MPEG 1 Layer 3), MPEG 2, Layer 3 (including low sampling rates) DTS, AAC or WMA type audio files from CD-ROM, CD-R and CD-R/W discs. The **Vaddis 778** can playback various types of JPEG, MPEG 4 and DivX bitstreams from files on DVD-ROM, DVD-R, DVD-RW, CD-ROM, CD-R and CD-RW, or on flash cards, or SACD with external SACD decoder chip.

Vaddis 778 is pin compatible with Vaddis 770.

It is assumed that the reader is familiar with the various discs, JPEG, MPEG 4, MPEG 2 and MPEG 1 international standards and the industrial standards for DivX, DVD-Video, DVD-Audio and the various types of CD and flash card formats. Note: This document contains information from industrial standards that were obtained by Zoran from other corporations under a Non Disclosure Agreement.

The **Vaddis 778** receives data from the disc loader optical pick-up unit OPU through an external RF amplifier, limit switches and other sensors and control the disc loader focus and tracking coils, sled, spindle and tray motors through a servo amplifier external device(s). The **Vaddis 778** implements all the signal processing, multi-pass ECC, EDC, track buffer management and servo functions that result in a (error corrected) bitstream.

The **Vaddis 778** can perform the decryption processes for bitstreams originating from a DVD-Video or DVD-Audio discs or from DivX bitstreams.

The max data read rate for all types of CD discs is 8x (8*1.411 Mbits/Sec). The max data read rate for DVD discs is 2x (2*10.08 Mbits/Sec).

The **Vaddis 778** outputs interlaced or progressive CCIR size (also called SD or D1 size), 4:2:2, Y, U and V digital video. The representation of each component sample is 8 bits. Suitable post-processing, to transform the original decoded size and format (e.g., SIF size or CCIR size MPEG 1 format, SIF size, "half D1" size, "2/3 D1" size or CCIR size MPEG 2 format) to the interlaced CCIR size, 4:2:2, Y, U and V format, is performed by the **Vaddis 778.**

The interlaced video display frame rate is either 25 or 29.97 frames per second. Frame rate conversion is performed from coded MPEG frame rates of 23.976, 25, or 29.97 per second, to one of the two display frame rates mentioned above. For example, for display frame rate of 29.97 and coded frame rate of 23.976, "3/2 pull down" is performed.

The progressive video display frame rate is either 50 or 59.94 frames per second. Frame rate

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conversion is performed from coded MPEG frame rates of 23.976, 25, or 29.97 per second, to one of the two display frame rates mentioned above by a de-interlacing unit using 2 fields edge adaptive interpolation.

The interlaced or progressive 8 bits digital video output is synchronous with an output video clock and sync signals, and contiguous along each video line.

Image display "location" relative to the sync signals, and size (up to the max specified above), are specified by **Vaddis 778** SW. The size of the displayed part of the decoded image can be less than or equal to the size of the decoded image

Format conversion between PAL, NTSC, 16:9 or 4:3 is supported, with pixel aspect ratio conservation, using (e.g.) either the "Pan-scan" or the "Letterbox" methods.

When the digital video output is interlaced, the **Vaddis 778** output analog interlaced video through a video encoder and four 10 bits DACs that are included in the **Vaddis 778.** Analog outputs can be either composite (CVBS and Y, C of "S-video") or component (R, G and B, or Y, U and V). When the digital video output is progressive, the **Vaddis 778** output analog progressive video in components format only, through the three components DACs or compatible interlaced video. The video encoder and DACs operate with a 54 MHz clock.

The audio output is 16, 18, 20 or 24 bits, two to eight channels, PCM samples at 16, 22.05, 24, 32, 44.1, 48, 96 or 192 KHz with each pair of (e.g., left and right) samples interleaved on a serial bus according to several flavours of the I2S standard. Post processing of the decoded audio and one stereo digital audio input, suitable for Karaoke and similar applications is supported. Audio coded data or reconstructed data can be output on a single line using an internal S/PDIF transmitter. PCM or coded audio data can be also input through one of two S/PDIF (TTL) inputs using a S/PDIF receiver to recover the input bit clock.

The Vaddis 778 can also output 8 bits, Y, U and V, 4:2:2, digital ("still") video to the HDXtreme companion chip, in various formats, compatible with the HDXtreme, as long as the sample rate is less than 135 MHz and the width of the Y component is less than 2047. In this mode, no other digital or analog video is output.

The **Vaddis 778** uses Synchronous DRAMs (SDRAM) for external buffers and generates all address and control signals for this external buffer. The required Synchronous DRAMs are of -7 type (max clock rate of 147 MHz). The required size is 64 Mbits using one 4M*16 bit device. The internal structure of the devices has to be four banks of 2048 rows by 256 cells each. Some limited applications can be supported by a single or dual 16 Mbits device(s). A single 128 Mbits device with four banks of 2048 rows by 512 cells each is also supported.

The **Vaddis 778** interfaces directly (through external buffers only) to several types of serial and parallel flash cards connectors. The interface is sharing some of the pins also used for disc loader control, so that the disc loader can not be operational while reading a card. For parallel flash cards, the interface is sharing some of the flash memory pins, so that the flash memory can not be accessed while reading a sector from a card.

The **Vaddis 778** interfaces to the other devices of a player (e.g., IR remote control receiver, front panel controller, audio DACs and ADCs) mainly through GPIO functions controlled by SW to implement protocols like SPI and I2C. There are on-chip HW aids to interface to a master SSC type device (e.g., a front panel concentrator).

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1.3 Typical Applications

Stand- alone DVD and CD disc players. See example block diagram in the figure below.

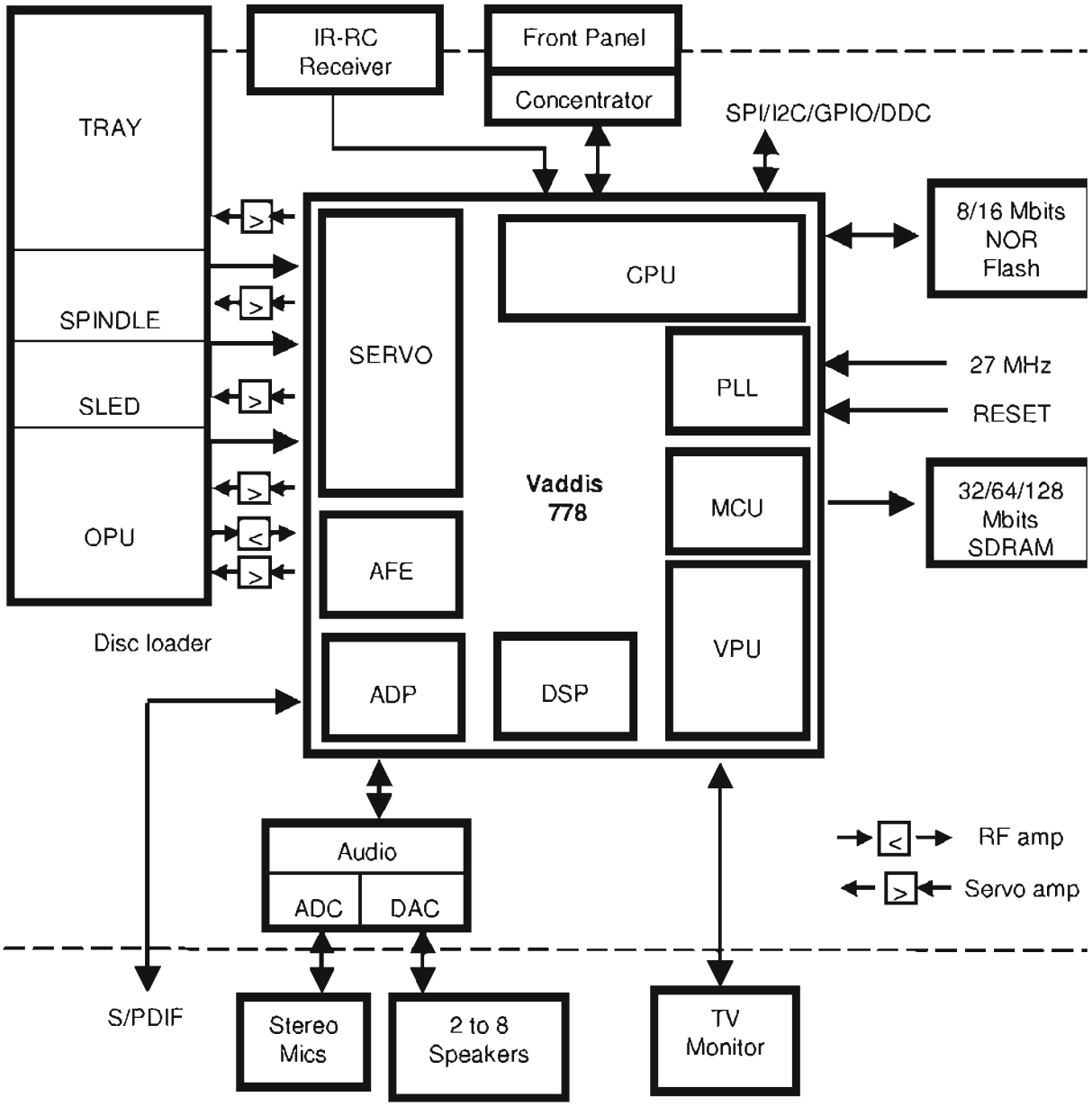

Figure 1 – DVD Player Block Diagram

The pins used for disc loader and NOR flash interface have a second function for direct flash card reading (not shown). Interface to an HD TV monitor is through an HDXtreme companion chip (not shown). When needed, the 64 Mbits SDRAM can be replaced by a 128 Mbits SDRAM.

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2 Functional Description

2.1 External interface

The main external interfaces of the **Vaddis 778** are shown in the next figure. The pins used for disc loader and NOR flash interface have a second function for direct flash card reading (not shown). Interface to an HD TV monitor is through an **HDXtreme** companion chip (not shown).

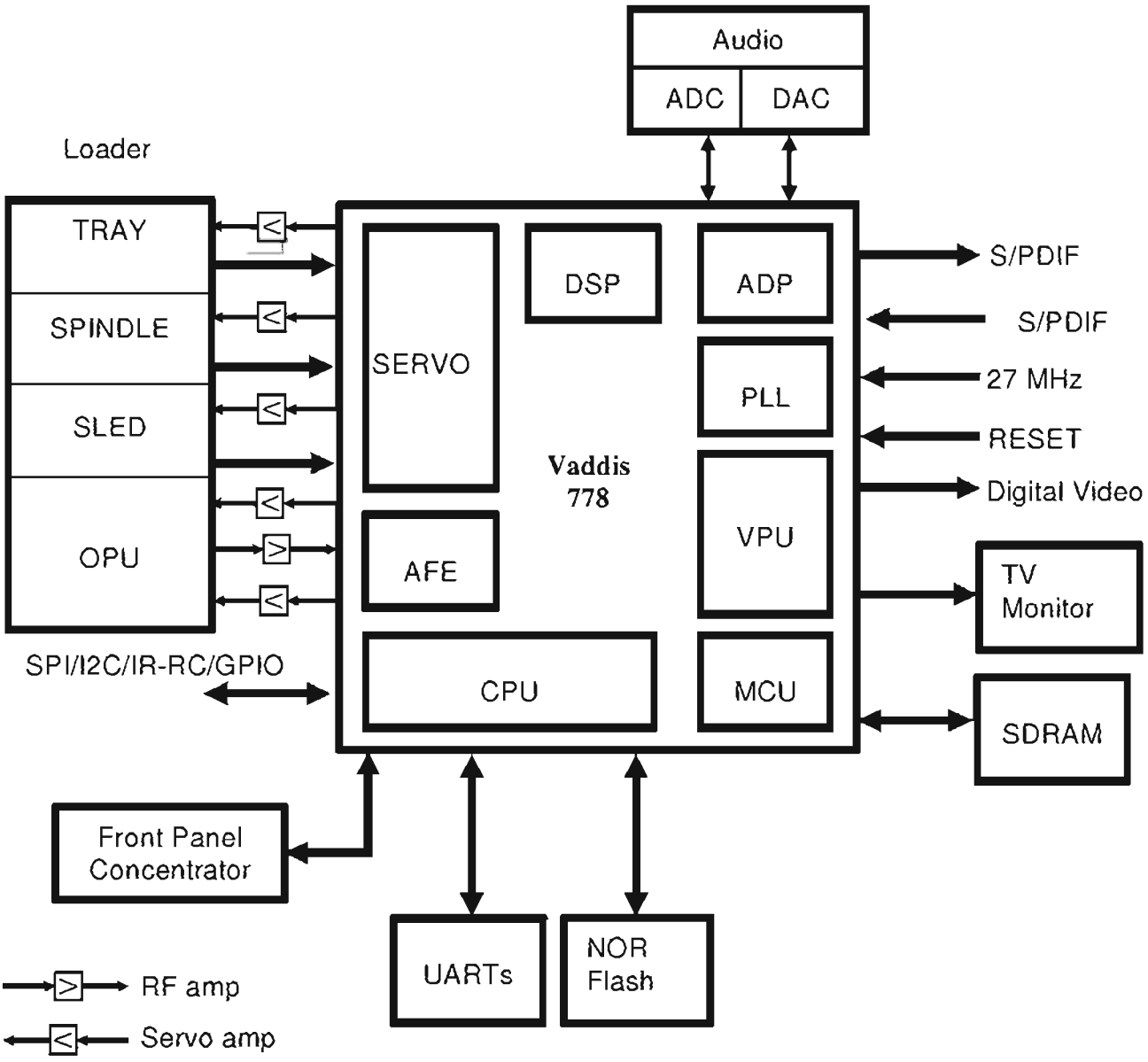

Figure 2 – Vaddis 778 Main External Interfaces

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3 Pin Description

3.1 Pin List

The **Vaddis 778** has 208 pins. The table below lists the pins, their functions, the direction or nature of each function (according to the legend below). Note that some of the functional pins may have additional function(s) dedicated for testing which are not described here. Following is the table legend:

I - standard input-only. O - standard active driver, with a 3-state option. I/O - bi-directional I/O pin, with a 3-state option. AI - Analog input signal. AO - Analog output signal. AI/O - Analog connection. ID - input, not sampled by PCLK. S - Power supply or ground.

If different functions have different direction, the **Vaddis 778** I/O supports all of them. Directions needed at RESET or for testing, when are different, are not shown in the table. All I and I/O pins have a level retaining HW.

Pins that are designated AI, S or ID should not be left not connected or floating.

Table 1 – Vaddis 778 Pinouts

Pin Number	Pin Functions	Direction	Description
1	*SSCRXD*	I	SSC data input.
	GPCI/O[17]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW
	PM[15]	O	Probe mux data output
2	*MEMCS[1]#*	O	PNVM/SRAM chip select (active low) output
	GPCI/O[18]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
3	*VDDP*	S	3.3 V Digital periphery power supply
4,5	*MEMAD*	O	PNVM/SRAM address bus outputs
	[15,16]		
	SYSIND[1,0]	I	General purpose system configuration Indication input. Level sampled during RESET
6	*MEMAD[14]*	O	PNVM/SRAM address bus output
	GCLKSEL	I	*GCLKPOUT* or *GCLKA* function selection. Level sampled during RESET
7	*MEMAD[13]*	O	PNVM/SRAM address bus output
	FCUIF[29]	O	Flash card interface unit output signal

Pin Number	Pin Functions	Direction	Description
8	*MEMAD[12]*	O	PNVM/ SRAM address bus output
	PLLCFGA	I	Audio PLL configuration input. Level sampled during RESET. In normal operation the pin must be low during RESET
9	*MEMDA[15]*	I/ O	PNVM/ SRAM bi- directional data bus
	FCUIF[28]	I/ O	Flash card interface unit input/ output signal
10	*MEMAD[11]*	O	PNVM/ SRAM address bus output
	PLLCFGP	I	Process PLL configuration input. Level sampled during RESET. In normal operation the pin must be low during RESET
11	*MEMDA[7]*	I/ O	PNVM/ SRAM bi- directional data bus
	FCUIF[9]	I/ O	Flash card interface unit input/ output signals
12	*GNDP*	S	Digital periphery ground of 3.3 V supply
13	*MEMAD[10]*	O	PNVM/ SRAM address bus output
	FCUIF[20]	O	Flash card interface unit output signal
14	*MEMDA[14]*	I/ O	PNVM/ SRAM bi- directional data bus
	FCUIF[27]	I/ O	Flash card interface unit input/ output signal
15	*MEMAD[9]*	O	PNVM/ SRAM address bus outputs
	FCUIF[19]	O	Flash card interface unit output signal
16	*MEMDA[6]*	I/ O	PNVM/ SRAM bi- directional data bus
	FCUIF[8]	I/ O	Flash card interface unit input/ output signals
17	*MEMAD[8]*	O	PNVM/ SRAM address bus outputs
	FCUIF[18]	O	Flash card interface unit output signal
18- 19	*MEMDA[13,5]*	I/ O	PNVM/ SRAM bi- directional data bus
	FCUIF[26.7]	I/ O	Flash card interface unit input/ output signals
20	*MEMAD[20]*	O	PNVM/ SRAM address bus outputs
	MEMCS[2]#	O	PNVM/ SRAM chip select (active low) output
	GPCI/ O[19]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW
21	*VDDP*	S	3.3 V Digital periphery power supply
22	*MEMDA[12]*	I/ O	PNVM/ SRAM bi- directional data bus

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Pin Number	Pin Functions	Direction	Description
	FCUIF[25]	I/O	Flash card interface unit input/output signal
23	*MEMWR#*	O	PNVM/SRAM write enable (active low) output
	FCUIF[0]	O	Flash card interface unit output signal
24	*MEMDA[4]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[6]	O	Flash card interface unit output signal
25	*VDDC*	S	1.8 V Digital core power supply
26	*MEMDA[11]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[24]	I/O	Flash card interface unit input/output signal
27	*MEMDA[3]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[5]	I/O	Flash card interface unit input/output signals
28	*MEMAD[19]*	O	PNVM/SRAM address bus outputs
	PLLSEL	I	PLL frequency selection - 108 MHz (low) or 135 MHz (high). Level sampled during RESET
29	*GNDC*	S	Digital core ground of 1.8 V supply
30	*MEMDA[10]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[23]	I/O	Flash card interface unit input/output signal
31	*MEMAD[18]*	O	PNVM/SRAM address bus output
32	*GNDP*	S	Digital periphery ground of 3.3 V supply
33	*MEMDA[2]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[4]	I/O	Flash card interface unit input/output signals
34	*MEMAD[17]*	O	PNVM/SRAM address bus output
35	*MEMDA[9]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[22]	I/O	Flash card interface unit input/output signal
36	*MEMAD[7]*	O	PNVM/SRAM address bus outputs
	FCUIF[17]	O	Flash card interface unit output signal
37	*MEMDA[1]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[3]	I/O	Flash card interface unit input/output signals
38	*MEMAD[6]*	O	PNVM/SRAM address bus outputs
	FCUIF[16]	O	Flash card interface unit output signal
39	*MEMDA[8]*	I/O	PNVM/SRAM bi-directional data bus

Pin Number	Pin Functions	Direction	Description
	FCUIF[21]	I/O	Flash card interface unit input/output signal
40	*MEMAD[5]*	O	PNVM/SRAM address bus outputs
	FCUIF[15]	O	Flash card interface unit output signal
41	*VDDP*	S	3.3 V Digital periphery power supply
42	*MEMDA[0]*	I/O	PNVM/SRAM bi-directional data bus
	FCUIF[2]	O	Flash card interface unit output signal
43	*MEMAD[4]*	I/O	PNVM/SRAM address bus outputs
	FCUIF[14]	O	Flash card interface unit output signal
44	*MEMRD#*	O	PNVM/SRAM read enable (active low) output
	FCUIF[1]	I/O	Flash card interface unit input/output signal
45-46	*MEMAD[3,2]*	O	PNVM/SRAM address bus outputs
	FCUIF[13,12]	O	Flash card interface unit output signal
47	*MEMCS[0]#*	O	PNVM/SRAM chip select (active low) output
48	*MEMAD[1]*	O	PNVM/SRAM address bus outputs
	FCUIF[11]	O	Flash card interface unit output signals
	BOOTSEL[2]	I	CPU SW boot (and execute) source selection: (high, high) - For production testing; (high, low) - Flash+SRAM (for debug monitor); (low, high) - First debug UART (low, low) - Flash (low) or Level sampled during RESET
49	*MEMAD[0]*	O	PNVM/SRAM address bus outputs
	FCUIF[10]	O	Flash card interface unit output signals
	BOOTSEL[1]	I	CPU SW boot (and execute) source selection: (high, high) - For production testing; (high, low) - Flash+SRAM (for debug monitor); (low, high) - First debug UART (low, low) - Flash (low) or Level sampled during RESET
50	*GNDP*	S	Digital periphery ground of 3.3 V supply

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Pin Number	Pin Functions	Direction	Description
51	*VDD-IP*	S	3.3 V periphery reference voltage
52	*VDDP*	S	3.3 V Digital periphery power supply
53-57	*RAMADD*	O	SDRAM address bus output
	[4,3,5,2,6]		
58	*VDDP*	S	3.3 V Digital periphery power supply
59-61	*RAMADD*	O	SDRAM address bus output
	[1,7,0]		
62	*GNDP*	S	Digital periphery ground of 3.3 V supply
63	*RAMADD[8]*	O	SDRAM address bus output
64	*VDDC*	S	1.8 V Digital core power supply
65	*RAMADD[10]*	O	SDRAM address bus output
66	*GNDC*	S	Digital core ground of 1.8 V supply
67	*RAMADD[9]*	O	SDRAM address bus output
68	*VDDP*	S	3.3 V Digital periphery power supply
69	*RAMADD[11]*	O	SDRAM address bus output
70	*RAMCS[0]#*	O	SDRAM chip select (active low)
	RAMBA[1]	O	SDRAM bank select output
71	*RAMBA[0]*	O	SDRAM bank select output
72	*GNDP*	S	Digital periphery ground of 3.3 V supply
73	*RAMCS[1]#*	O	SDRAM chip select (active low) output
74	*RAMRAS#*	O	SDRAM row select (active low) output
75	*RAMCAS#*	O	SDRAM column select (active low) output
76	*VDDP*	S	3.3 V Digital periphery power supply
77	*RAMWE#*	O	SDRAM write enable (active low) output
78	*RAMDQM*	O	SDRAM data masking (active high) output
79	*GNDPCLK*	S	Digital ground of filtered 3.3 V supply for PCLK
80	*PCLK*	O	SDRAM clock output (same as internal processing clock)
81	*VDDPCLK*	S	3.3 V filtered digital power supply for PCLK
82	*RAMDAT[8]*	I/O	SDRAM bi-directional data bus

Pin Number	Pin Functions	Direction	Description
83	*GNDP*	S	Digital periphery ground of 3.3 V supply
84-86	*RAMDAT [7,9,6]*	I/O	SDRAM bi-directional data bus
87	*VDDP*	S	3.3 V Digital periphery power supply
88-90	*RAMDAT [10,5,11]*	I/O	SDRAM bi-directional data bus
91	*GNDP*	S	Digital periphery ground of 3.3 V supply
92	*RAMDAT[4]*	I/O	SDRAM bi-directional data bus
93	*VDDC*	S	1.8 V Digital core power supply
94	*RAMDAT[12]*	I/O	SDRAM bi-directional data bus
95	*GNDC*	S	Digital core ground of 1.8 V supply
96	*RAMDAT[3]*	I/O	SDRAM bi-directional data bus
97	*VDDP*	S	3.3 V Digital periphery power supply
98-100	*RAMDAT [13,2,14]*	I/O	SDRAM bi-directional data bus
101	*GNDP*	S	Digital periphery ground of 3.3 V supply
102-104	*RAMDAT [1,15,0]*	I/O	SDRAM bi-directional data bus
105	*VDDP*	S	3.3 V Digital periphery power supply
106	*GPCI/O[20]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	CPUNMI	I	CPU non-maskable interrupt input
	SDATA[0]	I	SERVO channel sample data input for AFE by-pass
	PM[0]	O	Probe mux data output
107	*GNDP*	S	Digital periphery ground of 3.3 V supply
108	*ICGPCI/O[0]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
	AOUT[3]	O	Serial output of digital stereo audio

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Pin Number	Pin Functions	Direction	Description
	SDATA[1]	I	SERVO channel sample data input for AFE by-pass
	PM[1]	O	Probe mux data output
109	*IDGPCI/O[0]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	RAMCKE	O	Clock enable signal to the SDRAM (for power down)
	SDATA[2]	I	SERVO channel sample data input for AFE by-pass
	PM[2]	O	Probe mux data output
110	*S/PDIFOUT*	O	S/PDIF transmitter output for digital coded or reconstructed audio data
	SDATA[3]	I	SERVO channel sample data input for AFE by-pass
	PM[3]	O	Probe mux data output
111	*AOUT[2]*	O	Serial outputs of digital stereo audio
	GPCI/O[21]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	SDATA[4]	I	SERVO channel sample data inputs for AFE by-pass
	PM[4]	O	Probe mux data outputs
112	*AOUT[1]*	O	Serial outputs of digital stereo audio
	GPCI/O[22]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	PM[5]	O	Probe mux data outputs
113	*AOUT[0]*	O	Serial output of digital stereo audio
	SDATA[6]	I	SERVO channel sample data input for AFE by-pass
	PM[6]	O	Probe mux data outputs

Pin Number	Pin Functions	Direction	Description
114	*GPAI/O*	I/O	General purpose input/output, monitored/controlled by the ADP SW
	AOUT[3]	O	Serial output of digital stereo audio
	IDGPCI/O[0]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	PM[7]	O	Probe mux data output
115	*ALRCLK*	O	Digital audio left/right select output for the audio port. Square wave, at the sampling frequency. Programmable polarity
116	*ABCLK*	O	Digital audio bit-clock output. Data on AOUT and AIN is output or latched, respectively, with the rising or falling (programmable) edge of this clock
117	*GNDP-A2*	S	Digital ground of filtered 3.3 V supply for AMCLK
118	*AMCLK*	I/O	Audio Master Clock input/output. 128, 192, 256 or 384 times the sampling frequency (programmable).
119	*VDDP-A2*	S	3.3 V filtered digital power supply for AMCLK
120	*AIN*	I	Serial input of digital stereo audio
	GPCI/O[23]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	PM[8]	O	Probe mux data output
121	*GNDC*	S	Digital core ground of 1.8 V supply
122	*VSYNC#*	O	SD digital video vertical sync output signal
	HDFI	I	HD digital video field index input signal
	GPCI/O[24]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	DACTEST[9]	I	DACs test input
	PM[9]	O	Probe mux data output
123	*VDDC*	S	1.8 V Digital core power supply
124	*HSYNC#*	O	SD digital video horizontal sync output signal

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Pin Number	Pin Functions	Direction	Description
	HDHS	I	HD digital video horizontal sync input signal
	GPCI/O[25]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
125	*GNDP*	S	Digital periphery ground of 3.3 V supply
126	*VCLKx2*	O	Digital video clock output. 27.000 (for SD interlaced), 54.000 (SD progressive) or 135.000 (for HD) MHz
	COSYNC	O	Composite sync output. Active only when component analog output is selected
	ICGPCI/O[1]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
127	*VDDP*	S	3.3 V Digital periphery power supply
128	*VID[7]*	O	Digital 4:2:2 video luma/chroma output, interleaved U, Y V Y
	GPCI/O[26]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
129	*VID[6]*	O	Digital 4:2:2 video luma/chroma output, interleaved U, Y V Y
	ICGPCI/O[2]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
130	*VID[5]*	O	Digital4:2:2 video luma/chroma output, interleaved U, Y V Y
	IDGPCI/O[1]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
131	*GNDP*	S	Digital periphery ground of 3.3 V supply
132	*VID[4]*	O	Digital 4:2:2 video luma/chroma output, interleaved U, Y V Y
	GPCI/O[27]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW

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Pin Number	Pin Functions	Direction	Description
133	*VID[3]*	O	Digital 4:2:2 video luma/ chroma output, interleaved U, Y V Y
	GPCI/ O[28]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW
	SERVOCLK	O	SERVO channel clock output for AFE by-pass
134	*VID[2]*	O	Digital 4:2:2 video luma/ chroma output, interleaved U, Y V Y
	GPCI/ O[29]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW
	SSEL[0]	O	SERVO channel select output for AFE by-pass
135	*VDDP*	S	3.3 V Digital periphery power supply
136	*VID[1]*	O	Digital 4:2:2 video luma/ chroma output, interleaved U, Y V Y
	GPCI/ O[30]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW
	SSEL[1]	O	SERVO channel select output for AFE by-pass
137	*VID[0]*	O	Digital 4:2:2 video luma/ chroma output, interleaved U, Y V Y
	ICGPCI/ O[3]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
138	*GNDP*	S	Digital periphery ground of 3.3 V supply
139	*GNDA*	S	Ground plane of internal PLL circuit
140	*RESET#*	ID	Reset input (active low)
141	*VDDA*	S	1.8 V Power supply for internal PLL circuit
142	*XO*	AO	Output to a crystal that is connected to *GCLKP*. If a crystal is not used at *GCLKP*, *XO* must be left not connected
143	*GCLKP*	ID	27.000MHz clock or crystal input for main processing clock generation.
144	*GCLKA*	ID	27.000MHz clock input for audio master clock generation.
	GPCI/ O[31]	I/ O	General purpose input/ output, monitored/ controlled by the CPU or DSP SW

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Pin Number	Pin Functions	Direction	Description
	GCLKPOUT	O	*GCLKP* output
145	*VDDP*	S	3.3 V Digital periphery power supply
146	*ICGPCI/O[4]*	I/O	General purpose input/output monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
147	*S/PDIFIN[0]*	I	S/PDIF receiver inputs for digital coded or reconstructed audio data
	GPCI/O[33]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW.
148	*ICGPCI/O[4]*	I/O	General purpose input/output monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the CPU
149	*S/PDIFIN[1]*	I	S/PDIF receiver inputs for digital coded or reconstructed audio data
	GPCI/O[34]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW.
150	*IDGPCI/O[3]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[33]	I	Flash card interface unit input signal
151	*GNDP*	S	Digital periphery ground of 3.3 V supply
152	*DUPRD0*	I	First debug UART data input
	GPCI/O[35]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
153	*DUPTD0*	O	First debug UART data output
	GPCI/O[36]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
154	*VDD-IP*	S	3.3 V periphery reference voltage
155	*DUPRD1*	I	Second debug UART data output
	GPCI/O[37]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
156	*DUPTD1*	O	Second debug UART data output

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Pin Number	Pin Functions	Direction	Description
	GPCI/O[38]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
157	*GNDDACD*	S	Ground for the video DACs 3.3 V analog power supply
158	*CVBS/G/Y* (DAC A)	AO	When the Vaddis 778 outputs composite (SCART or non-SCART) video, this line is CVBS output When the Vaddis 778 outputs RGB, this line is the Green output When the Vaddis 778 outputs YUV, this line is the Y output
159	*CVBS/C/Y* (DAC D)	AO	When the other Vaddis 778 outputs are not SCART video, the output on this line can be either CVBS or C. The selection is independent of the specific selection of the other three DACs. When the Vaddis 778 outputs composite SCART video, this line is the Y output
160	*VDDDAC*	S	3.3 V Analog power supply for the video DACs
161	*Y/R/V/C* (DAC B)	AO	When the Vaddis 778 outputs composite non-SCART video, this line is Y output When the Vaddis 778 outputs RGB, this line is the Red output When the Vaddis 778 outputs YUV, this line is the V output When the Vaddis 778 outputs composite SCART video, this line is the C output
162	*C/B/U* (DAC C)	AO	When the Vaddis 778 outputs composite (SCART or non-SCART) video, this line is C output When the Vaddis 778 outputs RGB, this line is the Blue output When the Vaddis 778 outputs YUV, this line is the U output
163	*RSET*	AI	Resistive load for gain adjustment of the DACs

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Pin Number	Pin Functions	Direction	Description
164	*GNDDACP*	S	Ground for the video DACs 3.3 V analog power supply
165	*GNDDABS2*	S	Common Ground for the video and SERVO DACs
166	*GNDDACPS*	S	Grounds for the SERVO DAC 3.3 V analog power
167	*DACDRIVE[0]*	AO	Drive DACs output signal
168	*VDDDACS*	S	3.3 V SERVO DACs power supply
169	*DACDRIVE[1]*	AO	Drive DACs output signal
170	*GNDDACDS*	S	Grounds for the SERVO DAC 3.3 V analog power supply
171	*VDDAFERF*	S	3.3 V Analog RF (AFE) power supply
172	*RFINP*	AI	RF positive input signal (differential input) / / RF input signal (single ended)
173	*RFINN*	AI	RF negative input signal (differential input) / / RF reference input signal
174	*GNDAFERF*	S	Analog RF (AFE) ground of 3.3 V supply
175	*VDDAFES*	S	3.3 V Analog SERVO (AFE) power supply
176	*ADCIN[7]*	AI	SERVO ADC input signal (e.g. from RF amplifier)
177	*ADCIN[6]*	AI	SERVO ADC input signal from RF amplifier
178-183	*ADCIN[5-0]*	AI	SERVO ADC input signals (e.g. from RF amplifier)
184,185	*VBIASS[0,1]*	AI	Servo analog signal reference voltage inputs
186	*GNDAFES*	S	Analog SERVO (AFE) ground of 3.3 V supply
187	*PWMACT[0]*	O	PWM0 output signal
	GPCI/O[39]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW
	DVDDAT[0]	I	AV data input for FE by-pass
	NRZDATA	I	NRZ data input for AFE and DRC by-pass
188	*PWMACT[1]*	O	PWM1 output signal

Pin Number	Pin Functions	Direction	Description
	GPCI/O[40]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW
	DVDDAT[1]	I	AV data input for FE by-pass
	NRZCLK	I	NRZ clock input for AFE and DRC by-pass
189	*PWMCO[0]*	O	PWM2 output signal
	GPCI/O[41]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	DVDDAT[2]	I	AV data input for FE by-pass
	NRZLOCK	I	NRZ lock input for AFE and DRC by-pass
190	*GNDC*	S	Digital core ground of 1.8 V supply
191	*PWMCO[1]*	O	PWM3 output signal
	GPCI/O[42]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	DVDDAT[3]	I	AV data input for FE by-pass
	NRZDFCT	I	NRZ defect input for AFE and DRC by-pass
192	*VDDC*	S	1.8 V Digital core power supply
193	*PWMCO[2]*	O	PWM4 output signal
	GPCI/O[43]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	FCUIF[34]	O	Flash card interface unit input signal
	DVDDAT[4]	I	AV data inputs for FE by-pass
194	*PWMCO[3]*	O	PWM5 output signal
	GPCI/O[44]]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	FCUIF[35]	I/O	Flash card interface unit input/output signal
	IDGPCI/O[2]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	DVDDAT[5]	I	AV data inputs for FE by-pass
195	*GNDPWMS*	S	SERVO PWMs ground of 3.3 V supply
196	*PWMCO[4]*	O	PWM6 output signal

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Pin Number	Pin Functions	Direction	Description
	GPCI/O[45]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	DVDDAT[6]	I	AV data input for FE by-pass
197	*VDDPWMS*	S	3.3 V SERVO PWM power supply
198	*PWMCO[5]*	O	PWM7 output signal
	GPCI/O[46]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW
	FCUIF[36]	I/O	Flash card interface unit input/output signal
	DVDDAT[7]	I	AV data inputs for FE by-pass
199	*PWMCO[6]*	O	PWM8 output signal
	IDGPCI/O[4]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[32]	I/O	Flash card interface unit input/output signal
	DVDSTRB	I	AV data input for FE by-pass
	RFDAT[4]	I	RF channel sample data inputs for AFE by-pass
200	*DEFECT*	I/O	Disc defect input or output signal
	IDGPCI/O[5]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[37]	I/O	Flash card interface unit input/output signal
	DVDREQ	O	AV data request output for FE by-pass. Programmable polarity
201	*ICGPCI/O[6]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW. When input, the pin can be used as general purpose external interrupt to the CPU
	DVDVALID	I	AV data valid input for FE by-pass. Programmable polarity
202	*GNDP*	S	Digital periphery ground of 3.3 V supply

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Pin Number	Pin Functions	Direction	Description
203	*ICGPCI/O[7]*	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW. When input, the pin can be used as general purpose external interrupt to the CPU
	DVDERR	I	AV error input for FE by-pass. Programmable polarity
204	*VDDP*	S	3.3 V Digital periphery power supply
205	*SLEDPULSE*	I	Sled optical encoder input
	IDGPCI/O[6]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[30]	I	Flash card interface unit output signal
	DVDSOS	I	AV start of sector indication input for FE by-pass. Programmable polarity
206	*SPINDLE-PULSE*	I	Spindle optical encoder input
	IDGPCI/O[7]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW. When input, the pin can be used as general purpose external interrupt to the DSP
	FCUIF[31]	I/O	Flash card interface unit input/output signal
207	*SSCCLK*	I/O	SSC clock input signal
	GPCI/O[47]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP or FCU SW
208	*SSCTXD*	O	SSC data output signal
	GPCI/O[16]	I/O	General purpose input/output, monitored/controlled by the CPU or DSP SW

3.2 Signal Status During RESET and After RESET

Only I, I/O and O type pins are mentioned in this section.

In the following table, the status of the pins signals during RESET and just after RESET are specified.

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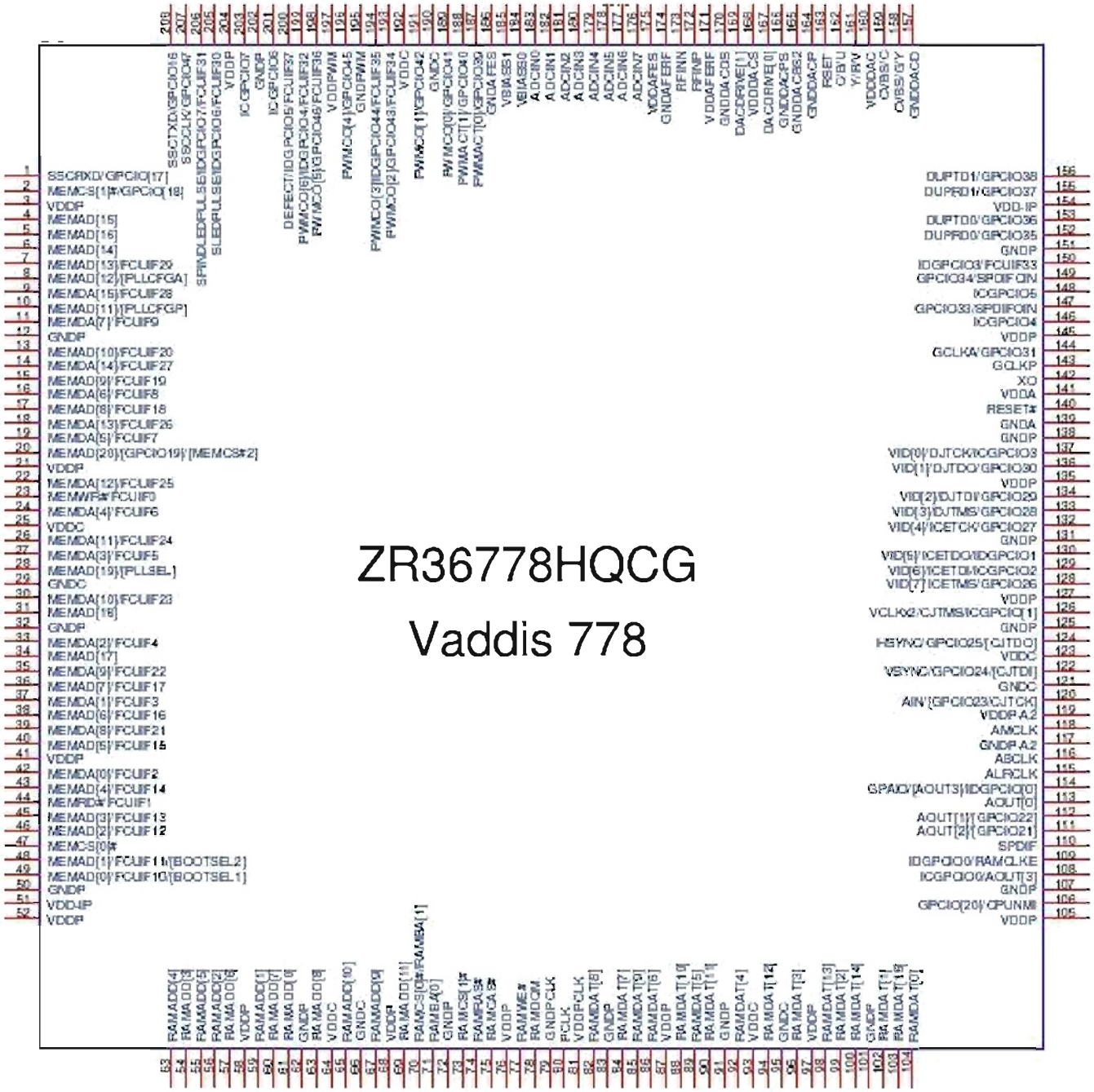
9 Package information

ZR36778HQCG is a green package



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CIRRUS LOGIC®

CS4382

114 dB, 192 kHz 8-Channel D/A Converter

Features

- 24-Bit Conversion
- Up to 192 kHz Sample Rates
- 114 dB Dynamic Range
- -100 dB THD+N
- Supports PCM and DSD Data Formats
- Selectable Digital Filters
- Volume Control with Soft Ramp
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- Dedicated DSD inputs
- Low Clock Jitter Sensitivity
- Simultaneous Support for Two Synchronous Sample Rates for DVD Audio
- µC or Stand-Alone Operation

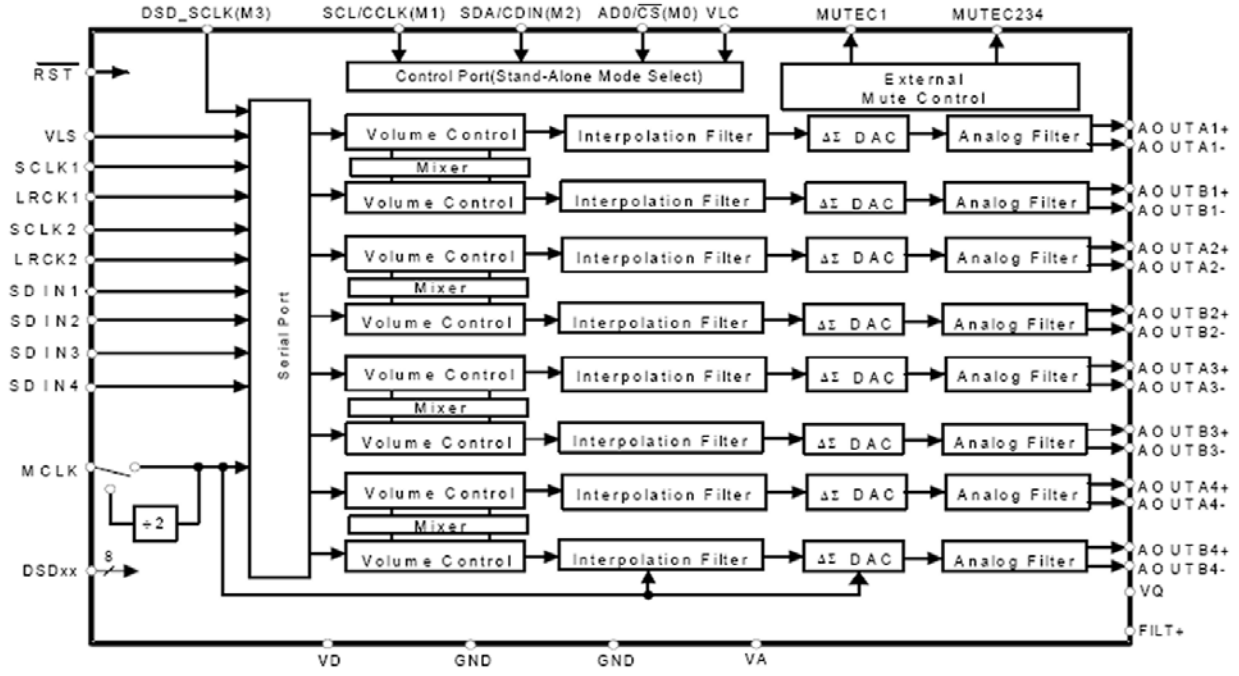
Description

The CS4382 is a complete 8-channel digital-to-analog system including digital interpolation, fifth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4382 accepts PCM data at sample rates from 4 kHz to 192 kHz, DSD audio data, and operates over a wide power supply range. These features are ideal for multi-channel audio systems including DVD players, SACD players, A/V receivers, digital TV's and VCR's, mixing consoles, effects processors, set-top boxes, and automotive audio systems.

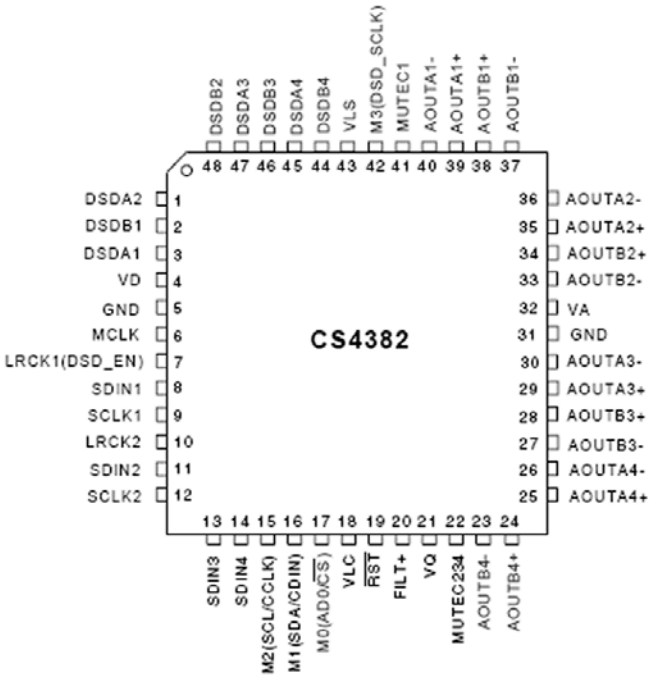
ORDERING INFORMATION

CS4382-KQZ, Lead Free	-10 to 70 °C	48-pin LQFP
CS4382-BQ	-40 to 85 °C	48-pin LQFP
CDB4382		Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

4. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	4	**Digital Power** (*Input*) - Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	5 31	**Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MCLK	6	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters. Table 5 illustrates several standard audio sample rates and the required master clock frequency.
LRCK1 LRCK2	7 10	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SDIN1 SDIN2 SDIN3 SDIN4	8 11 13 14	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK1 SCLK2	9 12	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
VLC	18	**Control Port Power** (*Input*) - Determines the required signal level for the control port. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{\text{RST}}$	19	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
FILT+	20	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to analog ground, as shown in the Typical Connection Diagram.
VQ	21	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage. VQ must be capacitively coupled to analog ground, as shown in the Typical Connection Diagram. The nominal voltage level is specified in the Analog Characteristics and Specifications section. VQ presents an appreciable source impedance and any current drawn from this pin will alter device performance. However, VQ can be used to bias the analog circuitry assuming there is no AC signal component and the DC current is less than the maximum specified in the Analog Characteristics and Specifications section.

Pin Name	#	Pin Description
MUTEC1 **MUTEC234**	41 22	**Mute Control** (*Output*) - The Mute Control pins go high during power-up initialization, reset, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect. These pins are intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
AOUTA1 +,- **AOUTB1 +,-** **AOUTA2 +,-** **AOUTB2 +,-** **AOUTA3 +,-** **AOUTB3 +,-** **AOUTA4 +,-** **AOUTB4 +,-**	39, 40 38, 37 35, 36 34, 33 29, 30 28, 27 25, 26 24, 23	**Differential Analog Output** (*Output*) - The full scale differential analog output level is specified in the Analog Characteristics specification table.
VA	32	**Analog Power** (*Input*) **-** Positive power supply for the analog section. Refer to the Recommended Operating Conditions for appropriate voltages.
VLS	43	**Serial Audio Interface Power** (*Input*) **-** Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
Control Port Definitions		
SCL/CCLK	15	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I^2C mode as shown in the Typical Connection Diagram.
SDA/CDIN	16	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line in I^2C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDIN is the input data line for the control port interface in SPI mode.
AD0/$\overline{CS}$	17	**Address Bit 0 (I^2C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I^2C mode; $\overline{CS}$ is the chip select signal for SPI format.
Stand-Alone Definitions		
M0 **M1** **M2** **M3**	17 16 15 42	**Mode Selection** (*Input*) - Determines the operational mode of the device as detailed in Tables 6 and 7.
DSD Definitions		
DSD_SCLK	42	**DSD Serial Clock** (*Input*) - Serial clock for the Direct Stream Digital audio interface.
DSD_EN	7	**DSD-Enable** *(Input)* - When held at logic '1' the device will enter DSD mode (Stand-Alone mode only).
DSDA1 **DSDB1** **DSDA2** **DSDB2** **DSDA3** **DSDB3** **DSDA4** **DSDB4**	3 2 1 48 47 46 45 44	**Direct Stream Digital Input** (*Input*) - Input for Direct Stream Digital serial audio data.

ESMT **M12L64164A**

SDRAM 1M x 16 Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

ORDERING INFORMATION

54 Pin TSOP (Type II)
(400mil x 875mil)

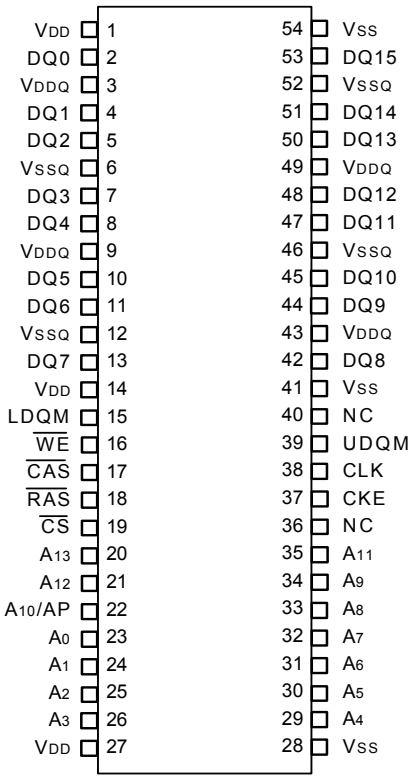
PRODUCT NO.	MAX FREQ.	PACKAGE
M12L64164A-6T	166MHz	TSOP II
M12L64164A-7T	143MHz	

GENERAL DESCRIPTION

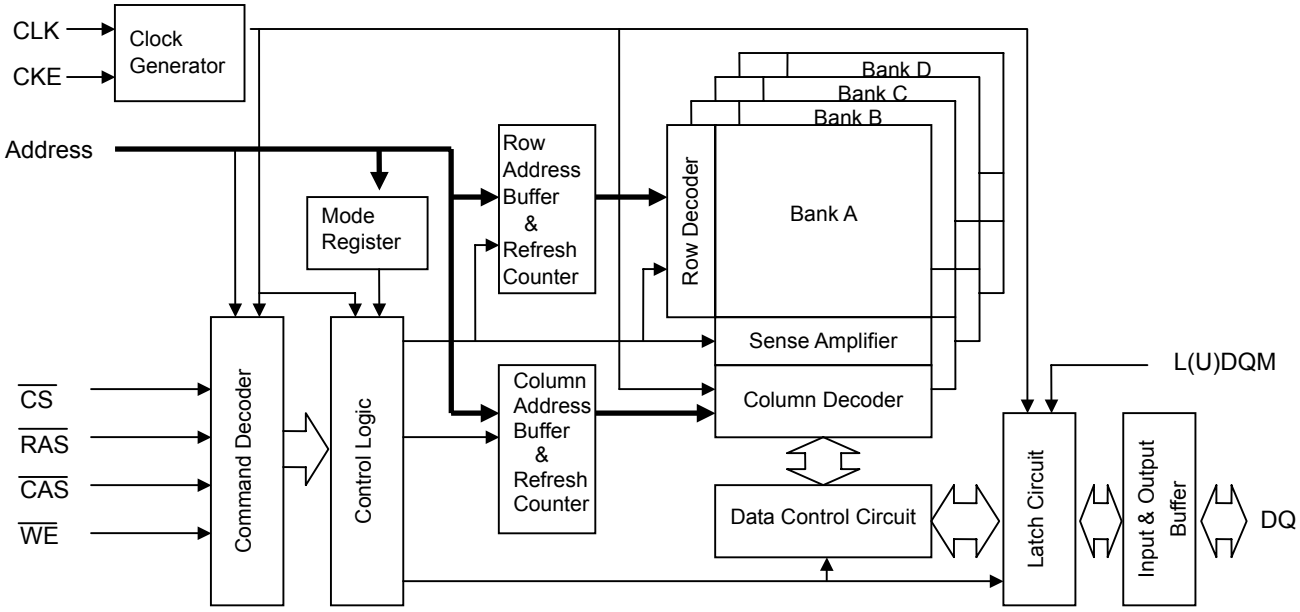
The M12L64164A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits. Synchronous design allows precise cycle controls with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

PIN ASSIGNMENT

Top View



FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK , CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row / column address are multiplexed on the same pins. Row address : RA0~RA11, column address : CA0~CA7
A12 , A13	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column address on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	Data Input / Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ DQ15	Data Input / Output	Data inputs / outputs are multiplexed on the same pins.
VDD / VSS	Power Supply / Ground	Power and ground for the input buffers and the core logic.
VDDQ / VSSQ	Data Output Power / Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left No Connection on the device.

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of setup and hold time around positive edge of the clock for proper functionality and Icc specifications.

CLOCK ENABLE(CKE)

The clock enable (CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least "1CLK + t_{SS}" before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK ADDRESSES (A13~A12)

This SDRAM is organized as four independent banks of 1,048,576 words x 16 bits memory arrays. The A13~A12 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The banks addressed A13~A12 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0~A11)

The 20 address bits are required to decode the 1,048,576 word locations are multiplexed into 12 address input pins (A0~A11). The 12 row addresses are latched along with $\overline{RAS}$ and A13~A12 during bank active command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and A13~A12 during read or with command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, The SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

1. Apply power and start clock, Attempt to maintain CKE = "H", DQM = "H" and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for minimum of 200us.
3. Issue precharge commands for both banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
   cf.) Sequence of 4 & 5 is regardless of the order.

   The device is now ready for normal operation.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0~A11 and A13~A12 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields into depending on functionality. The burst length field uses A0~A2, burst type uses A3, CAS latency (read latency from column address) use A4~A6, vendor specific options or test mode use A7~A8, A10/AP~A11 and A13~A12. The write burst length is programmed using A9. A7~A8, A10/AP~A11 and A13~A12 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

DEVICE OPERATIONS (Continued)

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of $t_{RCD\ (min)}$ from the time of bank activation. t_{RCD} is the internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing $t_{RCD\ (min)}$ with cycle time of the clock and then rounding of the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before another bank can be sensed reliably. $t_{RRD\ (min)}$ specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by $t_{RAS\ (min)}$. Every SDRAM bank activate command must satisfy $t_{RAS\ (min)}$ specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by $t_{RAS\ (max)}$ and $t_{RAS\ (max)}$ can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{RAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least $t_{RCD\ (min)}$ before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be complete by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

DQM OPERATION

The DQM is used mask input and output operations. It works similar to $\overline{OE}$ during operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is required. Please refer to DQM timing diagram also.

PRECHARGE

The precharge is performed on an active bank by asserting low on clock cycles required between bank activate and clock cycles required between bank activate and $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A10/AP with valid A13~A12 of the bank to be procharged. The precharge command can be asserted anytime after $t_{RAS\ (min)}$ is satisfy from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing tRP with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by $t_{RAS\ (max)}$. Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to power-down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

DEVICE OPERATIONS (Continued)

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy $t_{RAS\ (min)}$ and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst write by asserting high on A10/AP, the bank is precharge command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A10/AP after all banks have satisfied $t_{RAS\ (min)}$ requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge all, all banks are in idle state.

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by $t_{RFC\ (min)}$. The minimum number of clock cycles required can be calculated by driving t_{RFC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us or the burst of 4096 auto refresh cycles in 64ms.

SELF REFRESH

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption. The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the refresh.
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation. If the system uses burst auto refresh during normal operation, it is recommended to use burst 4096 auto refresh cycles immediately after exiting self refresh.

TOSHIBA TC74HCT7007AP/AF

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

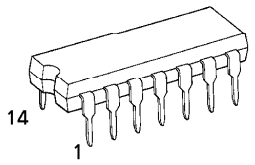
TC74HCT7007AP, TC74HCT7007AF

HEX BUFFER

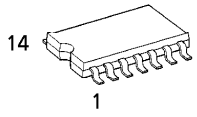
The TC74HCT7007A is a high speed CMOS BUFFER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
The internal circuit is composed of 4 stages including a buffer output, which provides high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 11ns(typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 1μA(Max.) at Ta = 25°C
- Compatible with TTL outputs .... V_{IH} = 2V (Min.)
  V_{IL} = 0.8V (Max.)
- Wide Interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74LS07

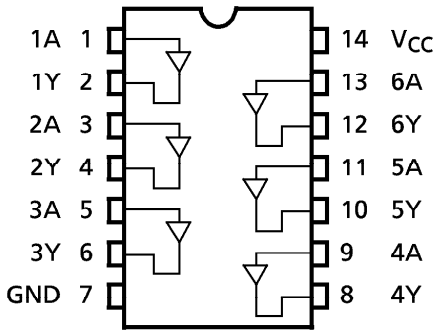


P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)



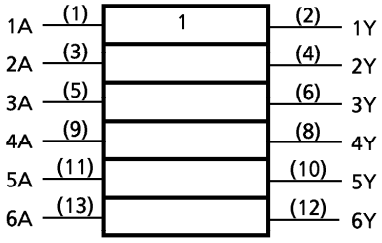
F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



PIN ASSIGNMENT

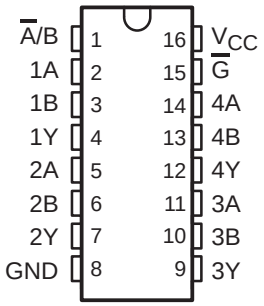
A	Y
L	L
H	H

SN74LVC157A
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS292G – JANUARY 1993 – REVISED OCTOBER 1998

- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Inputs Accept Voltages to 5.5 V**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC157A features a common strobe ($\overline{G}$) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The device provides true data.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC157A is characterized for operation from –40°C to 85°C.

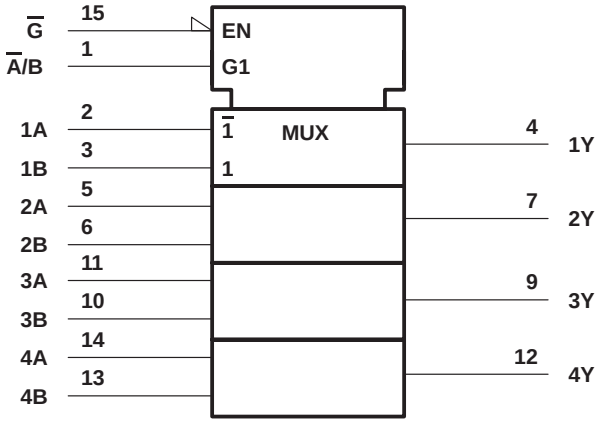
FUNCTION TABLE

INPUTS				OUTPUT
$\overline{G}$	$\overline{A}$/B	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

SN74LVC157A
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

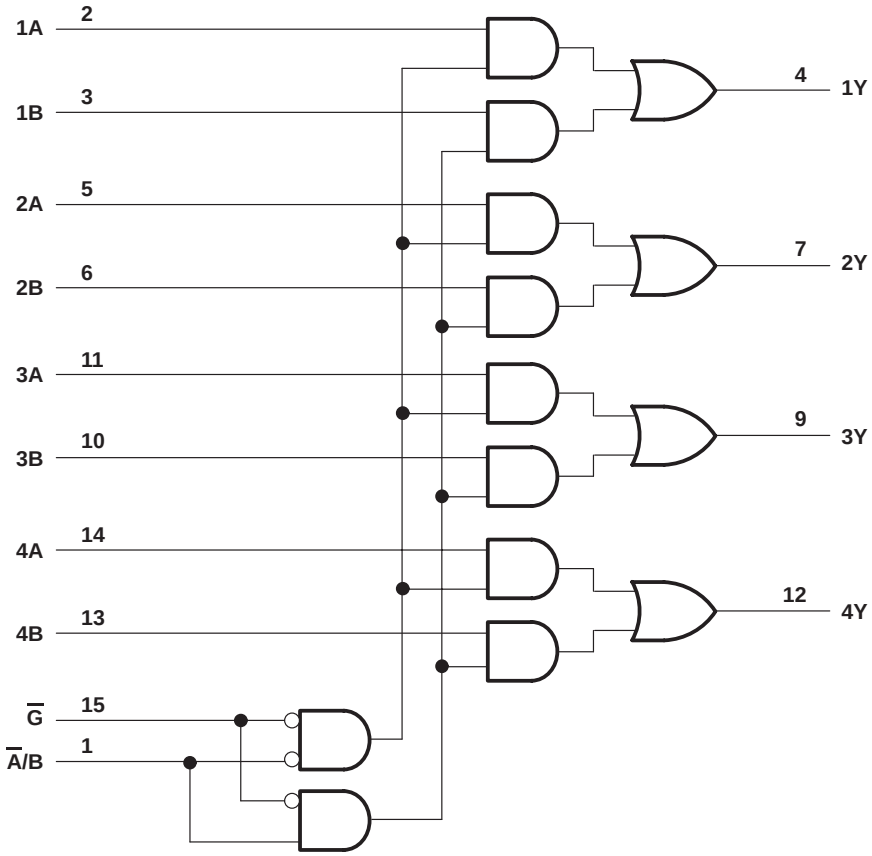
SCAS292G – JANUARY 1993 – REVISED OCTOBER 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



5-channel BTL Driver for DVD player AM5888S

The AM5888S is a five-channel BTL driver IC for driving the motors and actuators such as used in DVD player and consists of two independent precision voltage regulators with adjustable range from 1.5V to 4 V. It supports a variety of applications. Also, Pb free package is selectable (Please refer to Marking Identification).

● Applications

BTL driver for CD, CD-ROM and DVD.

● Features

1) Two channels are voltage-type BTL drivers for actuators of tracking and focus. Two channels are voltage-type BTL driver for sled and spindle motors. It is also built-in one channel bi-direction DC motor driver for tray.
2) Wide dynamic range [9.0V (*typ.*) when Vcc1= Vcc2= 12V, at R_L= 20Ω load].
3) Separating power of Vcc1 and Vcc2 is to improve power efficiency by a low supply voltage for tracking, focus, and spindle.
4) Level shift circuit built-in.
5) Thermal shut down circuit built-in.
6) Mute mode built-in.
7) **Dual actuator drivers:**
   A general purpose input OP provides differential input for signal addition. The output structure is two power OPAMPS in bridge configuration.
8) **Sled motor driver:**
   A general purpose input OP provides differential input for signal addition. The output structure is one power OPAMP in bridge configuration.
9) **Spindle driver:**
   Single input linear BTL driver. The output structure are two power OPAMPS in bridge configuration.
10) **Tray in-out driver:**
    The DC motor driver supports forward/reverse control for tray motor.
11) 2 **Built-in regulator controllers**
    Adjustable range 1.5V ~ 4V

● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply voltage	Vcc1 Vcc2	13.5	V
Power dissipation	P_d	*1.7	W
Operate Temp range	T_{opr}	-35 ~ +85	℃
Storage Temp range	T_{stg}	**-55 ~ +150	℃

*When mounted on a 70mm×70mm×1.6mm glass epoxy board.

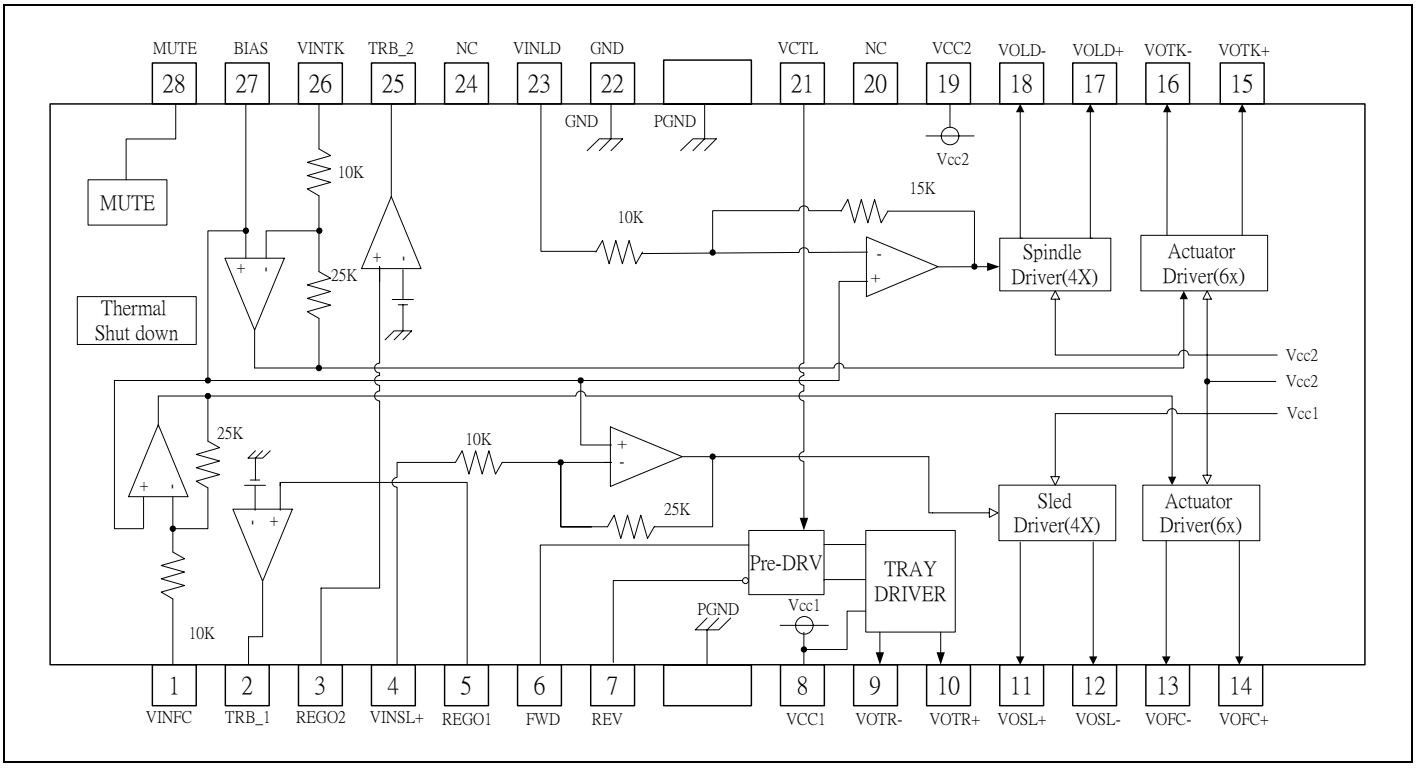
*Reduced by 13.6mW for each increase in T_a of 1℃ over 25℃.

**Should not exceed Pd or ASO and T_j=150℃ values

● Guaranteed operating conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc1	4.3 ~ 13.2	V
	Vcc2	4.3 ~ Vcc1	V

● Block diagram



● Pin description

PIN No	Pin Name	Function
1	VINFC	Input for focus driver
2	TRB_1	Connect to external transistor base
3	REGO2	Regulator voltage output, connect to external transistor collector
4	VINSL+	Input for the sled driver
5	REGO1	Regulator voltage output, connect to external transistor collector
6	FWD	Tray driver forward input
7	REV	Tray driver reverse input
8	Vcc1	Vcc for pre-drive block and power block of sled and tray
9	VOTR-	Tray driver output (-)
10	VOTR+	Tray driver output (+)
11	VOSL+	Sled driver output (+)
12	VOSL-	Sled driver output (-)
13	VOFC-	Focus driver output (-)
14	VOFC+	Focus driver output (+)
15	VOTK+	Tracking driver output (+)
16	VOTK-	Tracking driver output (-)
17	VOLD+	Spindle driver output (+)
18	VOLD-	Spindle driver output (-)
19	Vcc2	Vcc for power block of spindle, tracking and focus
20	NC	No Connection
21	VCTL	Speed control input of tray driver
22	GND	Ground
23	VINLD	Input for spindle driver
24	NC	No Connection
25	TRB_2	Connect to external transistor base
26	VINTK	Input for tracking driver
27	BIAS	Input for reference voltage
28	MUTE	Input for mute control

Notes) Symbol of + and – (output of drivers) means polarity to input pin.
(For example, if voltage of pin1 is high, pin14 is high.)

BH7862FS

Multimedia ICs

High-performance 6-channel video driver IC for progressive DVD

BH7862FS

BH7862FS is a 6-channel video driver IC developed for progressive DVD player/recorder. Special filters adjusted to each band of various video signals are incorporated into a single chip. Extended definition, size reduction, and high cost performance can be achieved in DVD players.

●Application

DVD players, DVD recorders

●Features

1) Each high-performance filter, 6dB amplifier, and 75Ω driver for DVD are incorporated into a single chip.
2) Driver 6ch (Y, C, MIX, and PY, Pb, Pr for progressive)
3) Group delay difference between chroma signal and luminance signal is a small number of nsec.
4) Drive 2 lines of each signal
5) Operating by 5V single power supply
6) Built-in mute circuit

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Impressed voltage	V_{CC} max	6.0	V
Power dissipation	Pd	0.95*	W
Operating temperature range	Topr	−10~+70	°C
Storage temperature range	Tstg	−55~+150	°C

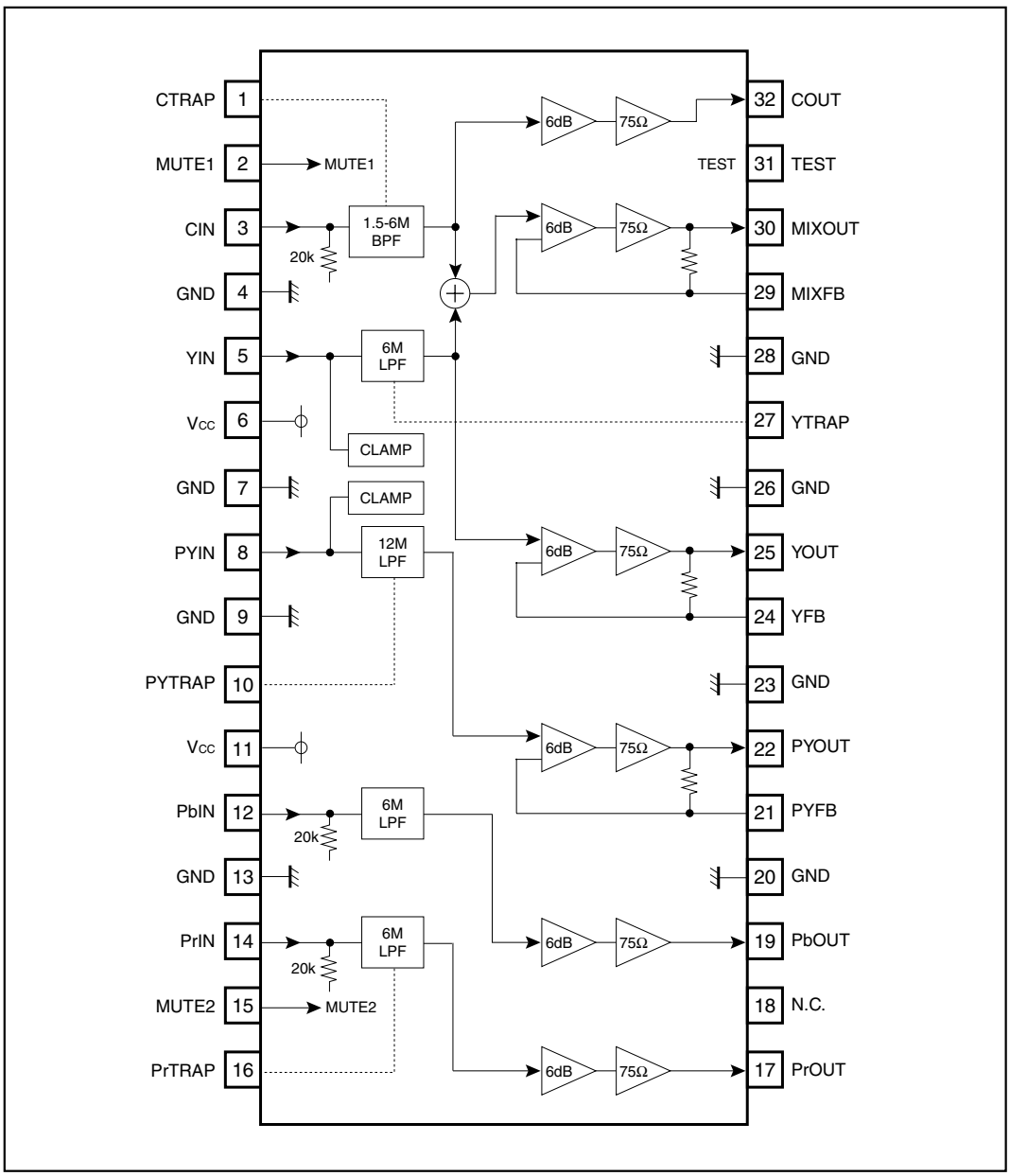
* Reduced by −7.6mW for each increase in Ta of 1°C over 25°C.
PCB (70mm×70mm, t=1.6mm) glass epoxy mounting.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	−	5.5	V

◎Radiation resistance is not included in the design.

●**Block diagram**



KEC

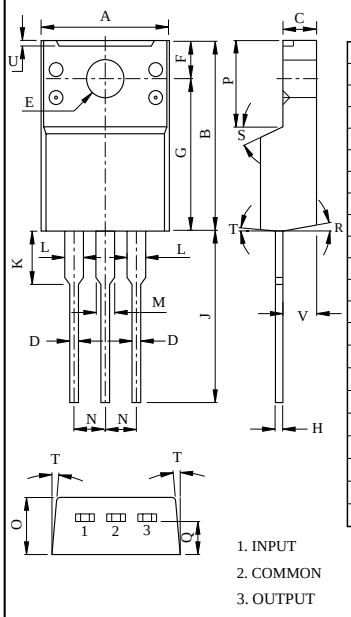
SEMICONDUCTOR
TECHNICAL DATA

KIA7805API~ KIA7824API
BIPOLAR LINEAR INTEGRATED CIRCUIT

THREE TERMINAL POSITIVE VOLTAGE REGULATORS
5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V.

FEATURES

· Suitable for C-MOS, TTL, the Other Digital IC's Power Supply.
· Internal Thermal Overload Protection.
· Internal Short Circuit Current Limiting.
· Output Current in Excess of 1A.
· Satisfies IEC-65 Specification. (International Electronical Commission)



DIM	MILLIMETERS
A	10.30 MAX
B	15.30 MAX
C	2.70±0.30
D	0.85 MAX
E	Φ3.20±0.20
F	3.00±0.30
G	12.30 MAX
H	0.75 MAX
J	13.60±0.50
K	3.90 MAX
L	1.20
M	1.30
N	2.54
O	4.50±0.20
P	6.80
Q	2.60±0.20
R	10°
S	25°
T	5°
U	0.5
V	2.60±0.15

TO-220IS

MAXIMUM RATINGS (Ta=25℃)

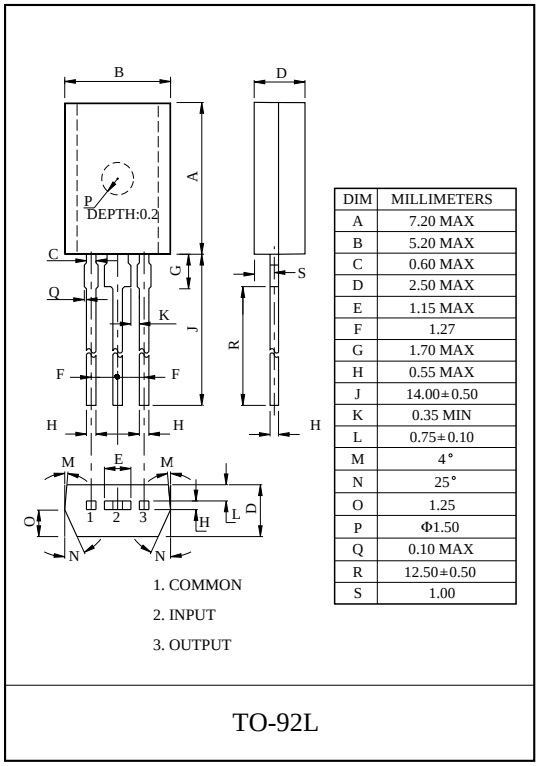
CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	KIA7805API ~ KIA7815API	V_{IN}	35	V
	KIA7818API ~ KIA7824API		40	
Power Dissipation (Tc=25℃)		P_D	20.8	W
Power Dissipation (Without Heatsink)	KIA7805API ~ KIA7824API	P_D	2.0	W
Operating Junction Temperature		T_j	-30 ~150	℃
Storage Temperature		T_{stg}	-55 ~150	℃

KEC

SEMICONDUCTOR
TECHNICAL DATA

KIA79L05BP~ KIA79L24BP
BIPOLAR LINEAR INTEGRATED CIRCUIT

THREE TERMINAL POSITIVE VOLTAGE REGULATORS
5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V.



DIM	MILLIMETERS
A	7.20 MAX
B	5.20 MAX
C	0.60 MAX
D	2.50 MAX
E	1.15 MAX
F	1.27
G	1.70 MAX
H	0.55 MAX
J	14.00±0.50
K	0.35 MIN
L	0.75±0.10
M	4°
N	25°
O	1.25
P	Φ1.50
Q	0.10 MAX
R	12.50±0.50
S	1.00

TO-92L

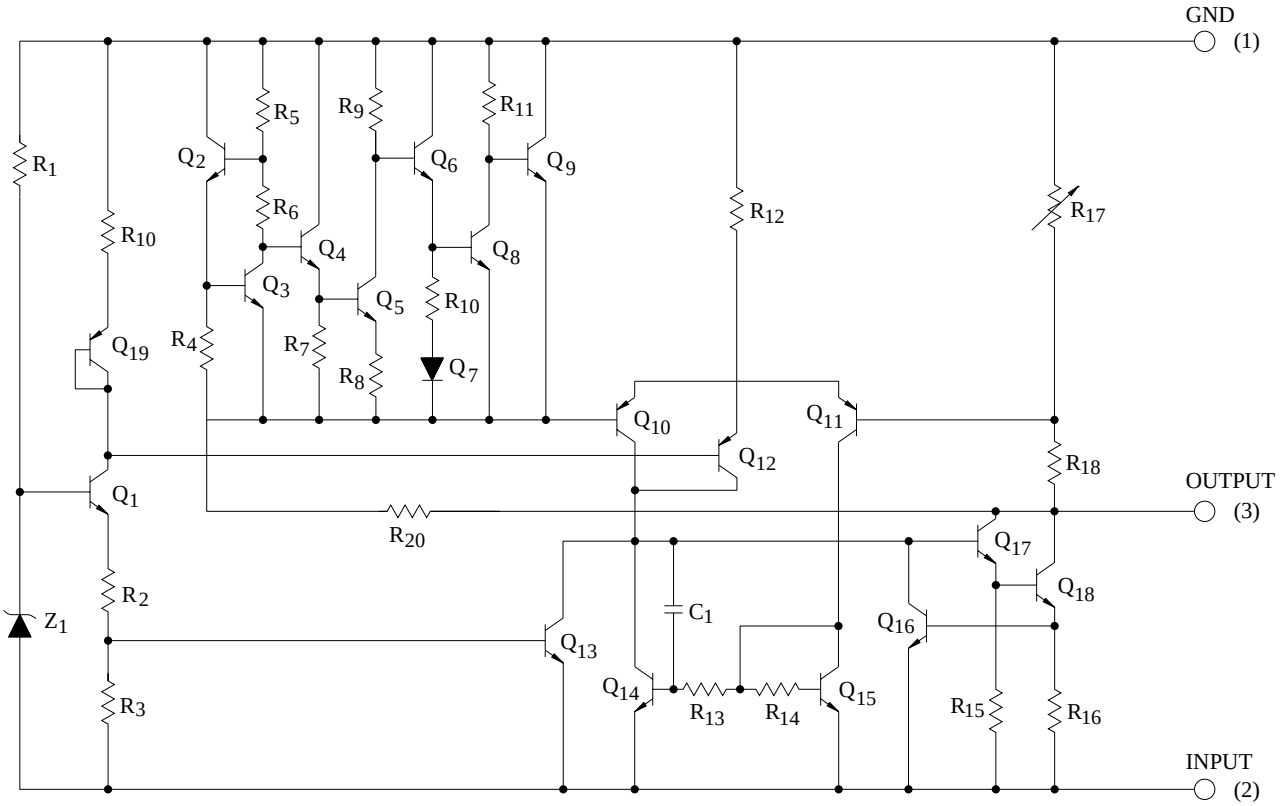
FEATURES

· Best Suited to a Power Supply for TTL and CMOS.
· Built-in Overcurrent Protective Circuit.
· Built-in Thermal Protective Circuit.
· Max. Output Current 150mA (T_j=25 ℃).
· Packaged in TO-92L.

MAXIMUM RATINGS (Ta=25 ℃)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	KIA79L05BP ~ KIA79L15BP	V_{IN}	-35	V
	KIA79L18BP ~ KIA79L24BP		-40	
Power Dissipation (Tc=25℃)		P_D	800	mW
Operating Junction Temperature		T_j	-30 ~ 150	℃
Operating Temperature		T_{opr}	-30 ~ 75	℃
Storage temperature		T_{stg}	-55 ~ 150	℃

EQUIVALENT CIRCUIT



Optic receiver modules

KODENSHI

KSM - 60 钡 TH2 · KSM - 70 钡 TH2

The KSM - 60钡TH2 consist of a PIN Photodiode of high speed and a preamplifier IC in the package as an receiver for Infrared remote control systems

FEATURES

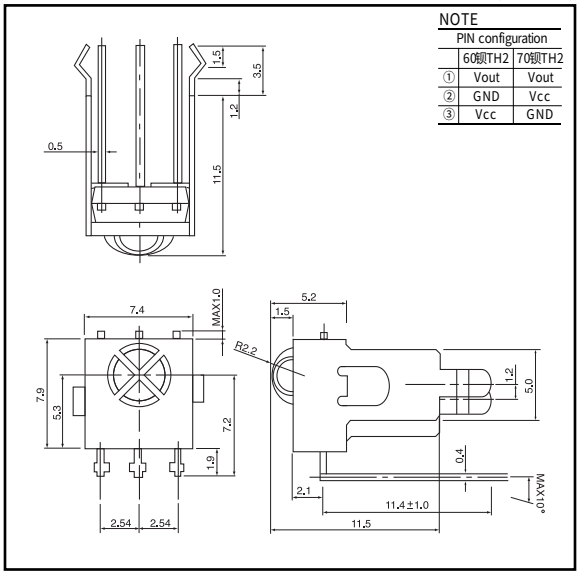
- One mold small package
- 5 Volt supply voltage, low power consumption
- Shielded against electrical field disturbance
- High immunity against ambient light
- Easy interface with the main board
- TTL and CMOS compatibility

APPLICATIONS

- TV, VTR, Acoustic Devices, Air Conditioners, Car Stereo Units, Computers, Interior controlling appliances, and all appliances that require remote controlling

DIMENSIONS

(Unit : mm)



MAXIMUM RATINGS

(Ta=25℃ Unless otherwise noted)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	5.5	V
Operating Temperature	Topr.	- 10~+60	℃
Storage Temperature	Tstg.	- 20~+75	℃
Soldering Temperature	Tsol.	260(Max 5 sec)	℃

B.P.F CENTER FREQUENCY

Model NO.	B.P.F Center Frequency(kHz)
KSM - ◯◯1 TH2	40.0
KSM - ◯◯2 TH2	36.7
KSM - ◯◯3 TH2	37.9
KSM - ◯◯4 TH2	32.7
KSM - ◯◯5 TH2	56.9

ELECTRO-OPTICAL CHARACTERISTICS

(Ta=25℃), Vcc=5.0V

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit.
Supply Voltage	V_{CC}			4.5	5.0	5.5	V
Current Consumption	I_{CC}	Input Signal=0		-	1.2	2.5	mA
Peak Wavelength *1	λp			-	940	-	nm
B.P.F Center Frequency	fo			-	37.9	-	kHz
Transmission Distance *1	L	200±50lx	0°	10	-	-	m
			±30°	7	-	-	m
H Level Output Voltage *1	V_{OH}	30cm over the ray axis		4.5	5.0	-	V
L Level Output Voltage *1	V_{OL}			-	0.1	0.5	V
H Level Output Pulse Width *1	T_{WH}	Burst Wave=600μs Period=1.2ms		500	600	700	μs
L Level Output Pulse Width *1	T_{WL}			500	600	700	μs
Output Form				Active Low Output			

Note : *1. It specifies the maximum distance between emitter and detector that the output waveform satisfies the standard under the conditions below against the standard transmitter

1) Measuring place : Indoor without extreme reflection of light
2) Ambient light source : Detecting surface illumination shall be irradiate 200±50lx under ordinary white fluorescence lamp without high frequency lightning
3) Standard transmitter : Burst wave of standard transmitter shall be arranged to 50mVp - p under the measuring circuit

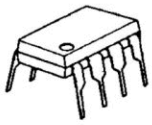
NJM2068

LOW-NOISE DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM2068 is a high performance, low noise dual operational amplifier. This amplifier features popular pin-out, superior noise performance, and superior total harmonic distortion. This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product and slew rate, which far exceeds that of the 4558 type amplifier. The specially designed low noise input transistors allow the NJM2068 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifier.

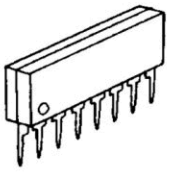
■ PACKAGE OUTLINE



NJM2068D

NJM2068M

NJM2068V

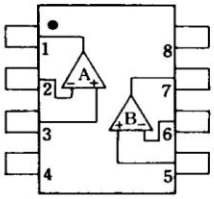


NJM2068L

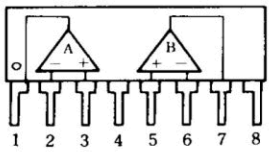
■ FEATURES

● Operating Voltage	(±4V~±18V)
● Low Total Harmonic Distortion	(0.001% typ.)
● Low Noise Voltage	(FLAT+JISA,0.56μV typ.)
● High Slew Rate	(6V/μs typ.)
● Unity Gain Bandwidth	(27MHz @ f=10kHz)
● Package Outline	DIP8,DMP8,SIP8,SSOP8
● Bipolar Technology	

■ PIN CONFIGURATION



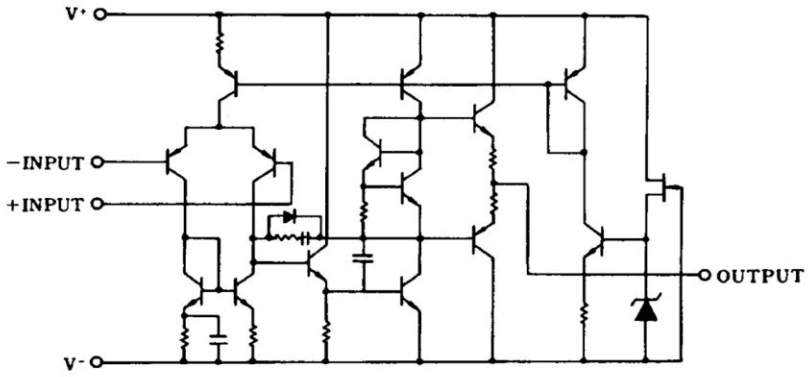
NJM2068D
NJM2068M
NJM2068V



NJM2068L

PIN FUNCTION
1.A OUTPUT
2.A –INPUT
3.A +INPUT
4.V^-
5.B +INPUT
6.B –INPUT
7.B OUTPUT
8.V^+

■ EQUIVALENT CIRCUIT (1/2 Shown)



National Semiconductor

October 2002

LM1117/LM1117I
800mA Low-Dropout Linear Regulator

General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V.

The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%.

The LM1117 series is available in LLP, TO-263, SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

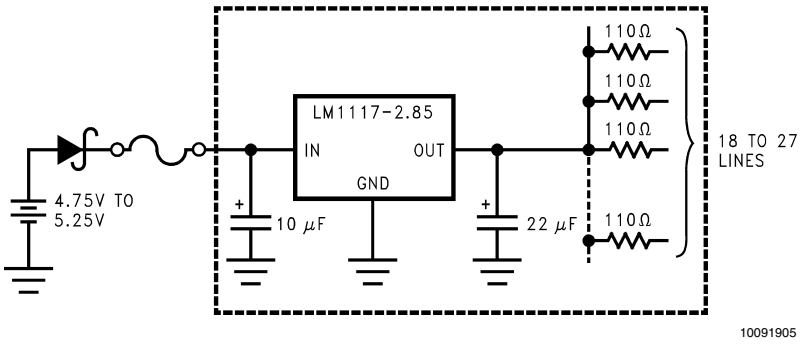
- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 and LLP Packages
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
  - — LM1117 0˚C to 125˚C
  - — LM1117I –40˚C to 125˚C

Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators
- Battery Charger
- Battery Powered Instrumentation

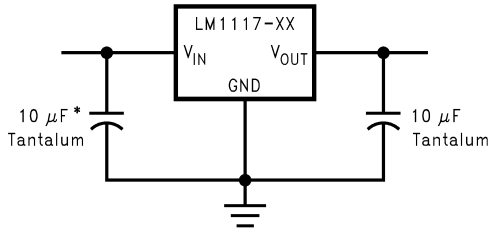
Typical Application

Active Terminator for SCSI-2 Bus



10091905

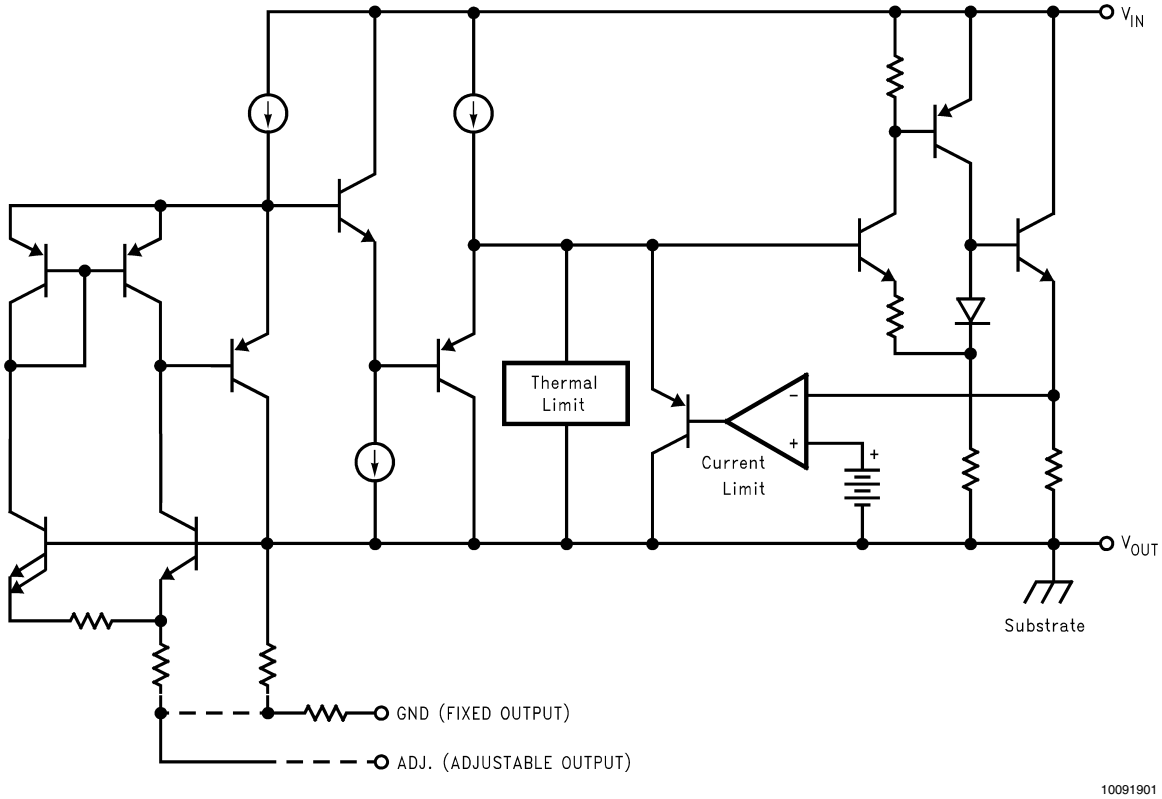
Fixed Output Regulator



* Required if the regulator is located far from the power supply filter.

10091928

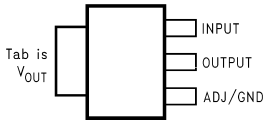
Block Diagram



10091901

Connection Diagrams

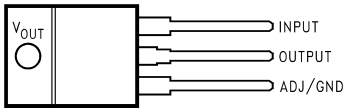
SOT-223



10091904

Top View

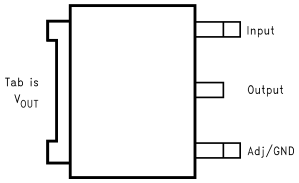
TO-220



10091902

Top View

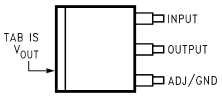
TO-252



10091938

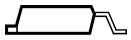
Top View

TO-263



10091944

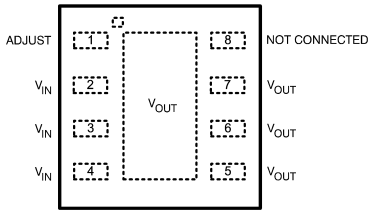
Top View



10091945

Side View

LLP



10091946

When using the LLP package
Pins 2, 3 & 4 must be connected together and
Pins 5, 6 & 7 must be connected together

Top View

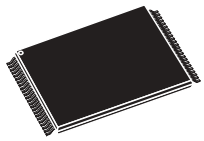
M29W160ET
M29W160EB

16 Mbit (2Mb x8 or 1Mb x16, Boot Block) 3V Supply Flash Memory

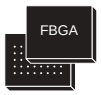
FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{CC} = 2.7V to 3.6V for Program, Erase and Read
- ACCESS TIMES: 70, 90ns
- PROGRAMMING TIME
  - 10µs per Byte/Word typical
- 35 MEMORY BLOCKS
  - 1 Boot Block (Top or Bottom Location)
  - 2 Parameter and 32 Main Blocks
- PROGRAM/ERASE CONTROLLER
  - Embedded Byte/Word Program algorithms
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- TEMPORARY BLOCK UNPROTECTION MODE
- COMMON FLASH INTERFACE
  - 64 bit Security Code
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Top Device Code M29W160ET: 22C4h
  - Bottom Device Code M29W160EB: 2249h

Figure 1. Packages



TSOP48 (N)
12 x 20mm



TFBGA48 (ZA)
6 x 8mm

SUMMARY DESCRIPTION

The M29W160E is a 16 Mbit (2Mb x8 or 1Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The blocks in the memory are asymmetrically arranged, see Figures 5 and 6, Block Addresses. The first or last 64 KBytes have been divided into four additional blocks. The 16 KByte Boot Block can be used for small initialization code to start the microprocessor, the two 8 KByte Parameter Blocks can be used for parameter storage and the remaining 32K is a small Main Block where the application may be stored.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered TSOP48 (12 x 20mm) and TFBGA48 (0.8mm pitch) packages. The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

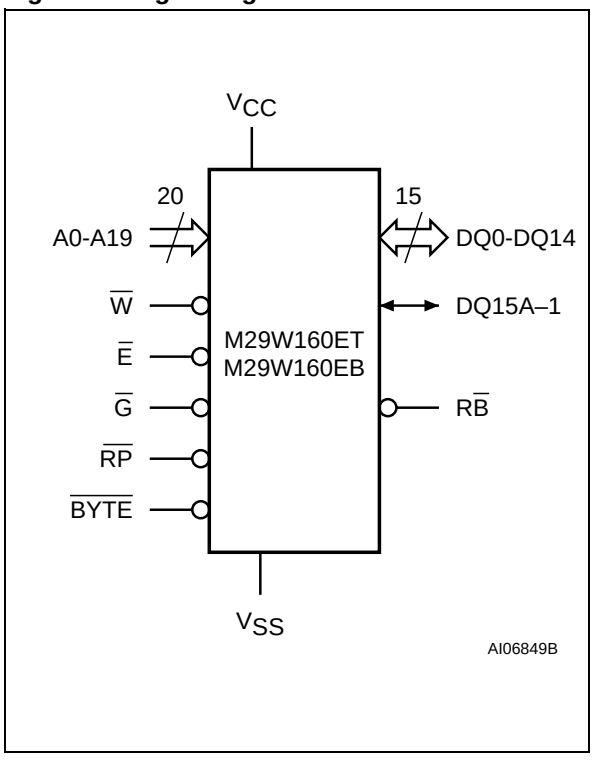
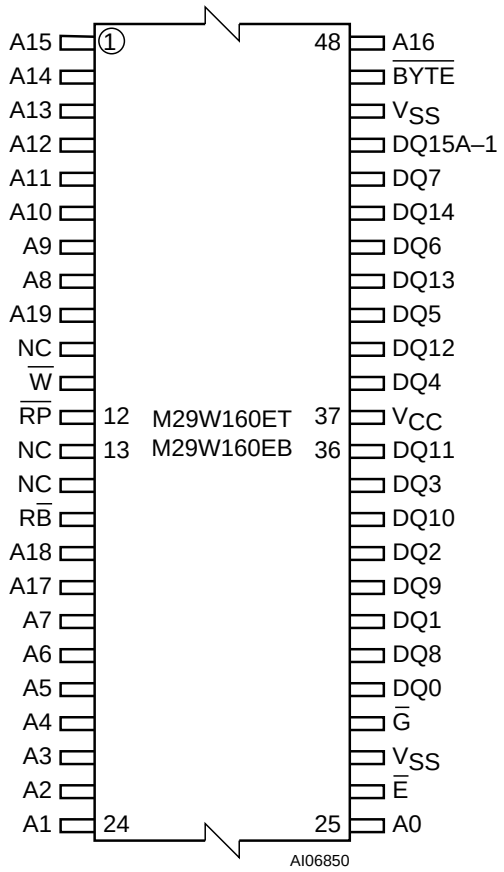


Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A–1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$R\overline{B}$	Ready/Busy Output
$\overline{BYTE}$	Byte/Word Organization Select
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. TSOP Connections



SAA7893HL

Super audio media player

Rev. 02 — 26 February 2003 **Product data**

1. General description

Thanks to the superior sound quality and multichannel capability of Super Audio CD (SACD) technology, multimedia devices such as DVD players and home cinema systems are incorporating SACD functionality. Philips' Super Audio Media Player (SA-MP) provides a flexible, state-of-the-art solution for SACD playback on DVD architectures.

Built around the SAA7893HL SACD processor, SA-MP system solution delivers complete SACD functionality, avoiding the need for continual redesign and re-integration of SACD into various applications. The system is completed with a single 64 Mbit SDRAM and has extensive software processing options, resulting in low total system cost (see Figure 1).

With integrated support for multiple loaders, the SAA7893 supports a variety of DVD platforms. High level and standard software interfaces – optimized for easy design-in – further enhance adaptability, enabling designers to build SACD players on many different hardware and software platforms. This ensures that the SA-MP can be left unchanged even if the SACD playback hardware is altered, again minimizing development effort.

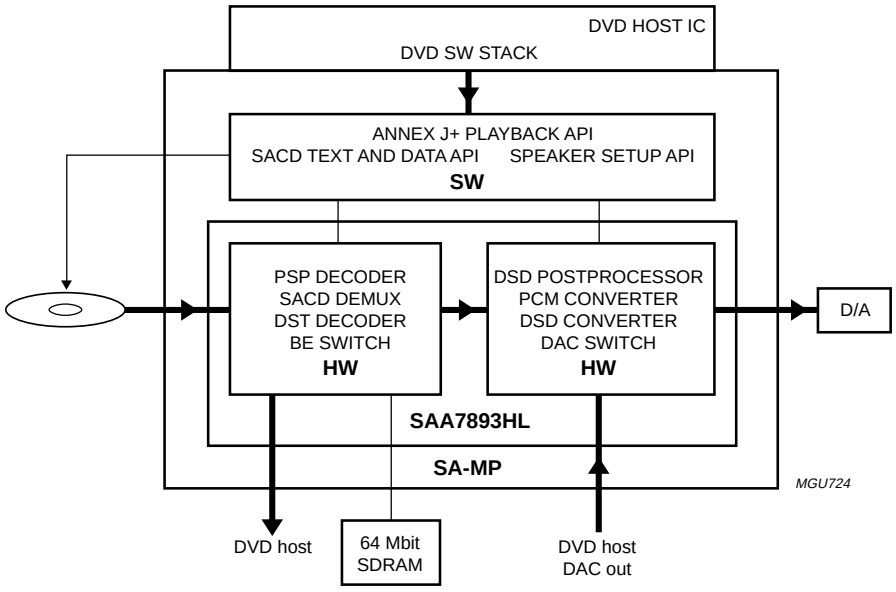


Fig 1. General block diagram.

1.1 Hardware

The SA-MP hardware consists of the SAA7893HL device. A typical HW block diagram of a DVD system incorporating the SAA7893HL is shown in Figure 2.

The SAA7893HL takes sector data from the front-end. The front-end is controlled by the DVD host via the SA-MP software stack. The SAA7893HL uses one 64 Mbit SDRAM for audio data buffering and storage of SACD TOCs. The front-end timing can be fully asynchronous from all clocks.

The 6-channel DAC outputs of the DVD host are routed via the SAA7893HL which provides a DAC switch function between SACD mode and DVD mode. The audio outputs of the SAA7893HL operate on the system audio clock.

The DVD back-end communicates with the SAA7893HL via a host bus. The system clock and the system audio clock are allowed to be asynchronous.

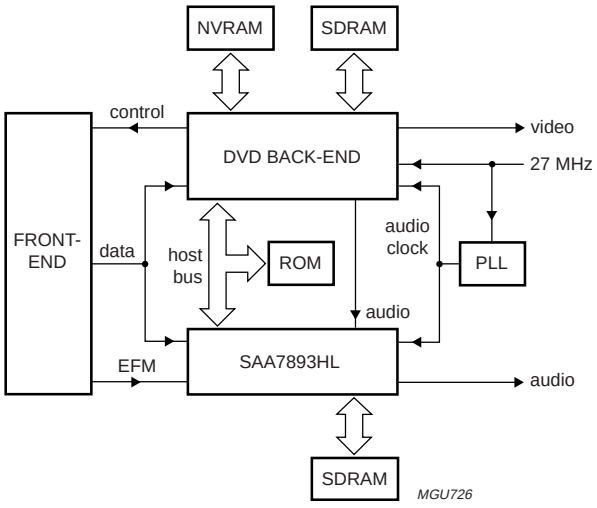


Fig 2. Hardware block diagram.

1.2 Software

The SA-MP software is delivered in the form of a library in the development environment of the DVD host. The SA-MP software has been developed in ANSI-C using conventional software technology to allow easy integration into any development environment. A typical software block diagram of a DVD system incorporating SA-MP is shown in Figure 3.

At the device driver and HW-level, SA-MP interfaces with the SAA7893HL and a front-end driver. At the infrastructure level, SA-MP interfaces with an Operating System Abstraction layer (OSA). At the application level, SA-MP provides a high-level playback and post-processing interface which is easy to integrate into typical applications.

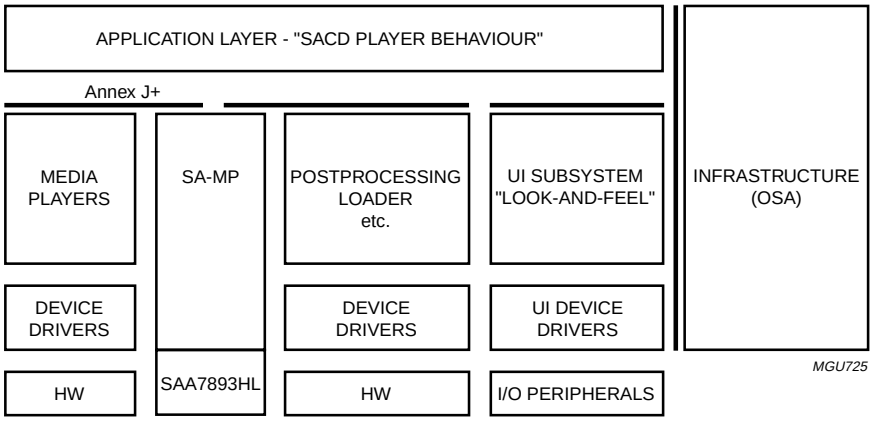


Fig 3. Software block diagram.

2. Features

2.1 Components

- SAA7893HL second generation SACD processor IC
- SA-MP Annex J+ level software stack.

2.2 HW interfaces

- Front-end, supports 3 types:
  - UDE
  - FEC
  - I^2S-bus
- Flexible PSP detection from EFM signal with AGC, without EFM clock (digital PLL)
- (DVD-)host bus, supports 3 types:
  - Separate address/data bus (SAD16) with 16-bit data bus (3 different modes)
  - Multiplexed address/data bus (MAD16) with 16-bit data bus (2 different modes)
  - Separate address/data bus (SAD08) with 8-bit data bus (1 mode)
- 16-bit 100 MHz SDRAM interface supports one 64 Mbit device
- 6-channel I^2S-PCM audio input 44.1, 48, 88.2, 96, 176.4 or 192 kHz at 16-bit or 24-bit
- 6-channel DSD or I^2S-PCM ($2f_s$ or $4f_s$) output with programmable pinning configuration
- 2-channel DSD or I^2S-PCM ($2f_s$ or $4f_s$) output with programmable pinning configuration
- Audio clock reference $256f_s$, $384f_s$, $512f_s$ or $768f_s$
- System clock 27 to 35 MHz.

2.3 SW interfaces

- Annex J+ level playback interface

- High-level audio post-processing control
- SACD data interface
- System configuration

2.4 System

- Full SACD Menu TOC and Area TOC storage in VBR
- Front-end clock asynchronous to other clocks

2.5 System configuration

- D/A converters:
  - DSD and PCM selectable pin sharing configuration
  - DSD clock polarity
- Audio and system clock asynchronous
- Front-end type

2.6 SACD playback

- SACD playback:
  - Multi-channel
  - 2-channel
- PSP processing
- Decrypting and demultiplexing
- VBR management
- DST decoding
- Fade processing
- Annex J+ level software interface:
  - Stop
  - Pause
  - Play
  - Fast forward
  - Fast reverse
  - Next/previous track
  - Program and play playlist
  - Repeat (Track, All or AB)
  - Shuffle
  - Introscan
  - Time search

2.7 Audio postprocessing

- DSD Bass Management with support of:
  - Dolby® configuration 0 (LLL1)
  - Dolby® configuration 1 (SSS1)
  - Dolby® configuration 2 (LSS0)
- Programmable bass filter frequency and slope:

- 60, 80, 100, 120 Hz
- 12, 18, 24 dB/Oct

(other frequencies or slopes are possible on customer request)

- DSD down mixing:
  - 2/2
  - 3/0
  - 2/0
  - separate 2/0
- DSD attenuation function 0 to −90 dB, programmable per channel
- DSD delay function total 65 ms (approximately 20 meters), programmable per channel
- 6-channel PCM input:
  - 44.1, 88.2, 176.4, 48, 96 or 192 kHz at 16-bit or 24-bit
  - PCM to DSD upsampling with 3 programmable Sigma-Delta and anti-aliasing filter modes
  - Attenuation and delay as with DSD
- DSD to PCM conversion 88.2, 176.4 kHz at 24-bit.

2.8 SACD data and text

- Album info
- Disc info
- Album or disc text
- Area text
- Track data
- Track text.

2.9 General

- E-JTAG for board test and debug
- 3.3 V pad supply voltage
- 1.8 V core supply voltage
- 1.8 V analog supply voltage
- LQFP128 package
- 0.18 µm CMOS process.

3. Applications

- Consumer DVD players
- Home cinema
- Car audio systems.

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
SAA7893HL	LQFP128	plastic low profile quad flat package; 128 leads; body 14 × 20 × 1.4 mm^2	SOT425-1

5. Block diagram

Figure 4 shows the block diagram of the SAA7893HL with all defined functions.

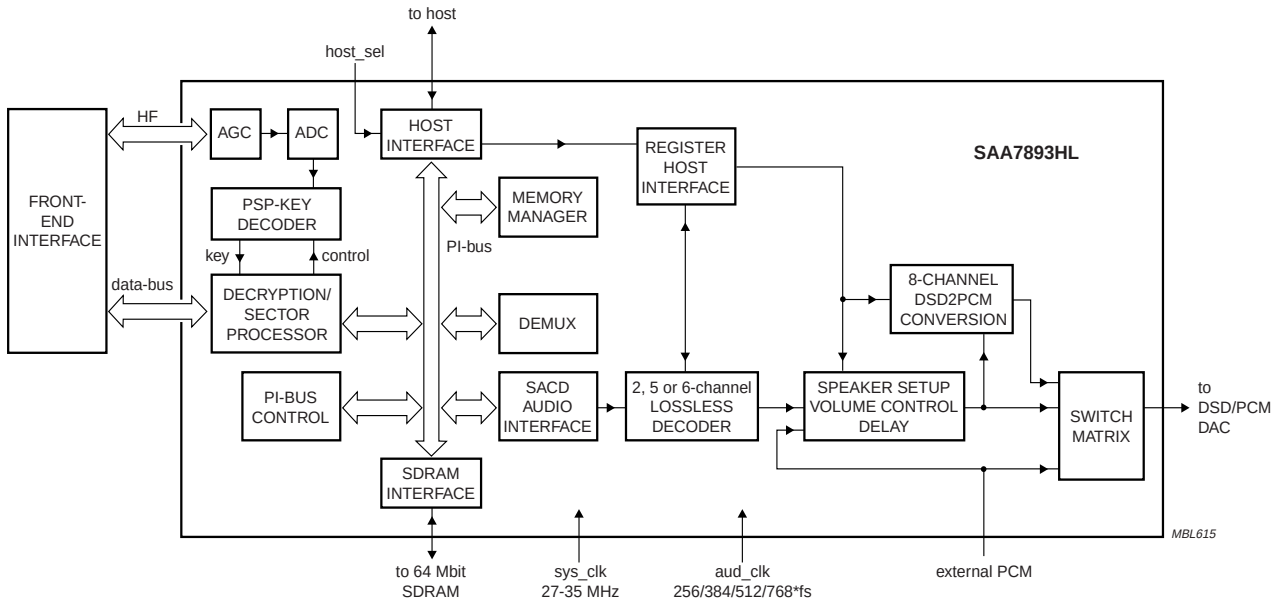


Fig 4. Block diagram.

6. Pinning information

6.1 Pinning

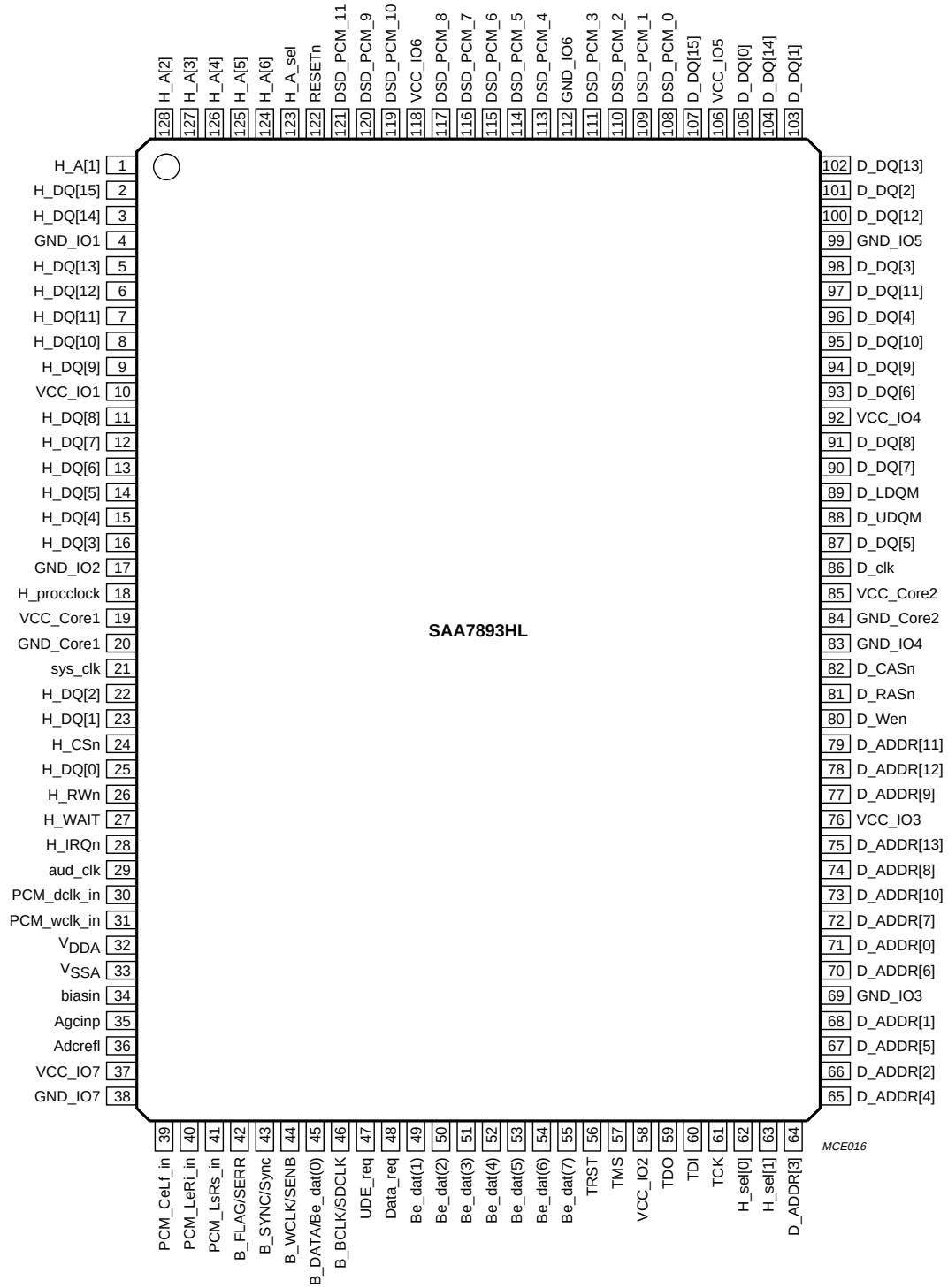


Fig 5. Pin configuration.

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Type[1]	Description
H_A[1]	1	IN	address bus
H_DQ[15]	2	I/O10	data bus
H_DQ[14]	3	I/O10	data bus
GND_IO1	4	GND_IO	GND I/O pads
H_DQ[13]	5	I/O10	data bus
H_DQ[12]	6	I/O10	data bus
H_DQ[11]	7	I/O10	data bus
H_DQ[10]	8	I/O10	data bus
H_DQ[9]	9	I/O10	data bus
VCC_IO1	10	VCC_IO	V_{CC} I/O pads
H_DQ[8]	11	I/O10	data bus
H_DQ[7]	12	I/O10	data bus
H_DQ[6]	13	I/O10	data bus
H_DQ[5]	14	I/O10	data bus
H_DQ[4]	15	I/O10	data bus
H_DQ[3]	16	I/O10	data bus
GND_IO2	17	GND_IO	GND I/O pads
H_procclock	18	IN	host processor EMI interface clock
VCC_Core1	19	VCC_core	core supply voltage
GND_Core1	20	GND_core	core ground
sys_clk	21	IN	system clock
H_DQ[2]	22	I/O10	data bus
H_DQ[1]	23	I/O10	data bus
H_CSn	24	IN	host chip select; active LOW
H_DQ[0]	25	I/O10	data bus
H_RWn	26	IN	read = 1; write = 0
H_WAIT	27	O10	wait signal
H_IRQn	28	O10	interrupt request; active LOW
aud_clk	29	IN	DSD audio clock
PCM_dclk_in	30	IN	PCM data clock
PCM_wclk_in	31	IN	PCM word clock
V_{DDA}	32	VDDCO	V_{DD} of ADC
V_{SSA}	33	VSSCO	V_{SS} of AGC and ADC; connected to substrate
biasin	34	APIO	bias current input
Agcinp	35	APIO	AGC positive input signal; HF in
Adcrefl	36	APIO	ADC decoupling
VCC_IO7	37	VCC_IO	V_{CC} I/O pads
GND_IO7	38	GND_IO	GND I/O pads
PCM_CeLf_in	39	IN	PCM data center or LFE

Table 2: Pin description *...continued*

Symbol	Pin	Type[1]	Description
PCM_LeRi_in	40	IN	PCM data left or right
PCM_LsRs_in	41	IN	PCM data left or right surround
B_FLAG/SERR	42	IN	I^2S-bus flag (EDC flag)
B_SYNC/Sync	43	IN	sector sync or absolute time sync
B_WCLK/SENB	44	IN	I^2S-bus word clock or UDE data sense from host
B_DATA/Be_dat(0)	45	IN	I^2S-bus data or LSB data of parallel interface
B_BCLK/SDCLK	46	IN	I^2S-bus bit clock
UDE_req	47	IN	host request data from front-end; routed via the SAA7893HL
Data_req	48	O10	data request for UDE
Be_dat(1)	49	IN	front-end parallel data interface
Be_dat(2)	50	IN	front-end parallel data interface
Be_dat(3)	51	IN	front-end parallel data interface
Be_dat(4)	52	IN	front-end parallel data interface
Be_dat(5)	53	IN	front-end parallel data interface
Be_dat(6)	54	IN	front-end parallel data interface
Be_dat(7)	55	IN	front-end parallel data interface
TRST	56	IN1	boundary scan reset
TMS	57	IN1	boundary scan mode select
VCC_IO2	58	VCC_IO	V_{CC} I/O pads
TDO	59	O10	output
TDI	60	IN1	boundary scan data input
TCK	61	IN	boundary scan clock
H_sel[0]	62	IN	host select signals: SAD16, MAD16 and SAD08
H_sel[1]	63	IN	host select signals: SAD16, MAD16 and SAD08
D_ADDR[3]	64	O10	SDRAM address bus
D_ADDR[4]	65	O10	SDRAM address bus
D_ADDR[2]	66	O10	SDRAM address bus
D_ADDR[5]	67	O10	SDRAM address bus
D_ADDR[1]	68	O10	SDRAM address bus
GND_IO3	69	GND_IO	GND I/O pads
D_ADDR[6]	70	O10	SDRAM address bus
D_ADDR[0]	71	O10	SDRAM address bus
D_ADDR[7]	72	O10	SDRAM address bus
D_ADDR[10]	73	O10	SDRAM address bus
D_ADDR[8]	74	O10	SDRAM address bus
D_ADDR[13]	75	O10	SDRAM address bus
VCC_IO3	76	VCC_IO	V_{CC} I/O pads
D_ADDR[9]	77	O10	SDRAM address bus

Table 2: Pin description *...continued*

Symbol	Pin	Type[1]	Description
D_ADDR[12]	78	O10	SDRAM address bus
D_ADDR[11]	79	O10	SDRAM address bus
D_Wen	80	O10	read or write
D_RASn	81	O10	row address select; active LOW
D_CASn	82	O10	column address select; active LOW
GND_IO4	83	GND_IO	GND I/O pads
GND_Core2	84	GND_core	core ground
VCC_Core2	85	VCC_core	core supply voltage
D_clk	86	O10	clock signal needed for SDRAM
D_DQ[5]	87	I/O10	data bus
D_UDQM	88	O10	DQ mask enable (upper)
D_LDQM	89	O10	DQ mask enable (lower)
D_DQ[7]	90	I/O10	data bus
D_DQ[8]	91	I/O10	data bus
VCC_IO4	92	VCC_IO	V_{CC} I/O pads
D_DQ[6]	93	I/O10	data bus
D_DQ[9]	94	I/O10	data bus
D_DQ[10]	95	I/O10	data bus
D_DQ[4]	96	I/O10	data bus
D_DQ[11]	97	I/O10	data bus
D_DQ[3]	98	I/O10	data bus
GND_IO5	99	GND_IO	GND I/O pads
D_DQ[12]	100	I/O10	data bus
D_DQ[2]	101	I/O10	data bus
D_DQ[13]	102	I/O10	data bus
D_DQ[1]	103	I/O10	data bus
D_DQ[14]	104	I/O10	data bus
D_DQ[0]	105	I/O10	data bus
VCC_IO5	106	VCC_IO	V_{CC} I/O pads
D_DQ[15]	107	I/O10	data bus
DSD_PCM_0	108	O10	6-channel data output
DSD_PCM_1	109	O10	6-channel data output
DSD_PCM_2	110	O10	6-channel data output
DSD_PCM_3	111	O10	6-channel data output
GND_IO6	112	GND_IO	GND I/O pads
DSD_PCM_4	113	O10	6-channel data output
DSD_PCM_5	114	O10	6-channel data output
DSD_PCM_6	115	O10	6-channel clock/control
DSD_PCM_7	116	O10	6-channel clock/control
DSD_PCM_8	117	O10	2-channel clock/control
VCC_IO6	118	VCC_IO	V_{CC} I/O pads

Table 2: Pin description *...continued*

Symbol	Pin	Type[1]	Description
DSD_PCM_10	119	O10	2-channel data output
DSD_PCM_9	120	O10	2-channel clock or control
DSD_PCM_11	121	O10	2-channel data output
RESETn	122	IN	asynchronous reset; active LOW
H_A_sel	123	IN	address select
H_A[6]	124	IN	address bus
H_A[5]	125	IN	address bus
H_A[4]	126	IN	address bus
H_A[3]	127	IN	address bus
H_A[2]	128	IN	address bus

[1] Explanation of input and output ports:
IN: digital input port; all dedicated inputs are TTL tolerant.
IN1: digital input port with internal pull-up resistor.
I/O10: bidirectional port with 10 ns slew rate.
O10: 3-state (in test mode) output port with 10 ns slew rate.
APIO: analog input port.
VDDCO: analog V_{DD} port (1.8 V).
VSSCO: analog V_{SS} port.
GND_IO: ground for I/O pads.
VCC_IO: V_{CC} for I/O pads (3.3 V).
GND_core: ground for core.
VCC_core: V_{CC} for core (1.8 V).

7. Interfaces

7.1 Host interface

Different types of host busses are supported:

- Separate address/data bus with 16-bit data bus (3 different modes)
- Multiplexed address/data bus with 16-bit data bus (2 different modes)
- Separate address/data bus with 8-bit data bus (1 mode).

The host interface type is set via the dedicated pins H_sel and sys_clk. The SAA7893HL has a dedicated interrupt output pin.

7.2 Front-end interface

7.2.1 Data input interface

The SAA7893HL supports three different front-end interfaces which are selectable via the host interface:

- I^2S-bus interface: the front-end interface is in essence an I^2S-bus interface and therefore, it has to conform to the I^2S-bus specification.
- FEC interface

- Parallel interface (UDE data interface part): a parallel front-end interface with a handshake protocol.

7.2.2 Analog HF input

The analog HF input, coming from the optical pickup unit, is also fed to the SAA7893HL to extract the copy protection information PSP.

7.3 Audio interface

7.3.1 Audio input

The audio input is a 6-channel PCM-I^{2}S input.

7.3.2 DAC interface

The audio output is a 6-channel output and a separate stereo output. Both outputs can be set in DSD and in PCM-I^{2}S mode.

7.4 SDRAM interface

The SDRAM interface forms a glueless interface to one 64 Mbit SDRAM device.

Supported devices are only PC100 compliant or faster SDRAM devices:

- Organization: 64 Mbit (1M $\times$ 16 $\times$ 4 banks)
- Refresh period: 4096 cycles per 64 ms
- Clock frequency: $f_{clk} \geq 100$ MHz
- Refresh cycle: $t_{rcar} \leq 70$ ns
- Command period: $t_{rc} \leq 70$ ns.

7.5 Clock and reset input

Different processing clocks are needed in the SAA7893HL:

- sys_clk: system clock for data processing part; frequency can be between 27 and 35 MHz; see Figure 6 and Table 3
- aud_clk: audio clock reference; can be 256/384/512/768 $\times$ f_s (f_s = 44.1 to 48 kHz); see Figure 7 and Table 4
- proc_clk: host processor clock (only used in SAD16_01/02 mode)
- B_BCLK: front-end bit/byte clock.

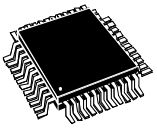
It is not required that these clocks are locked.

RESETn is an asynchronous reset and should be kept LOW for at least 10 periods of sys_clk.

ST72F324L, ST72324BL

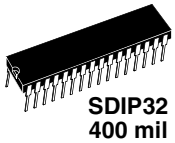
3V RANGE 8-BIT MCU WITH 8 TO 32K FLASH/ROM, 10-BIT ADC, 4 TIMERS, SPI, SCI INTERFACE

- **Memories**
  - 8 to 32K dual voltage High Density Flash (HDFlash) or ROM with read-out protection capability. In-Application Programming and In-Circuit Programming for HDFlash devices
  - 384 to 1K bytes RAM
  - HDFlash endurance: 100 cycles, data retention: 20 years at 55°C
- **Clock, Reset And Supply Management**
  - Clock sources: crystal/ceramic resonator oscillators, internal RC oscillator, and bypass for external clock
  - PLL for 2x frequency multiplication
  - Four Power Saving Modes: Halt, Active-Halt, Wait and Slow
- **Interrupt Management**
  - Nested interrupt controller
  - 10 interrupt vectors plus TRAP and RESET
  - 9/6 external interrupt lines (on 4 vectors)
- **Up to 32 I/O Ports**
  - 32/24 multifunctional bidirectional I/O lines
  - 22/17 alternate function lines
  - 12/10 high sink outputs
- **4 Timers**
  - Main Clock Controller with: Real time base, Beep and Clock-out capabilities
  - Configurable watchdog timer
  - 16-bit Timer A with: 1 input capture, 1 output compare, external clock input, PWM and pulse generator modes
  - 16-bit Timer B with: 2 input captures, 2 output compares, PWM and pulse generator modes



TQFP44
10 x 10

TQFP32
7 x 7



SDIP32
400 mil

- **2 Communication Interfaces**
  - SPI synchronous serial interface
  - SCI asynchronous serial interface
- **1 Analog Peripheral**
  - 10-bit ADC with up to 12 input ports
- **Instruction Set**
  - 8-bit Data Manipulation
  - 63 Basic Instructions
  - 17 main Addressing Modes
  - 8 x 8 Unsigned Multiply Instruction
- **Development Tools**
  - Full hardware/software development package
  - In-Circuit Testing capability

Device Summary

Features	ST72F324L(J/K)6	ST72F324L(J/K)4	ST72F324L(J/K)2	ST72324BL(J/K)4	ST72324BL(J/K)2
Program memory - bytes	Flash 32K	Flash 16K	Flash 8K	ROM 16K	ROM 8K
RAM (stack) - bytes	1024 (256)	512 (256)	384 (256)	512 (256)	384 (256)
Voltage Range	2.85 to 3.6V				
Temp. Range	up to -40°C to +85°C				
Packages	TQFP44 10x10, SDIP32, TQFP32 7x7				

Rev. 3

1 INTRODUCTION

The ST72F324L and ST72324BL devices are members of the ST7 microcontroller family designed for the 3V operating range. They can be grouped as follows:

– The 32-pin devices are designed for mid-range applications

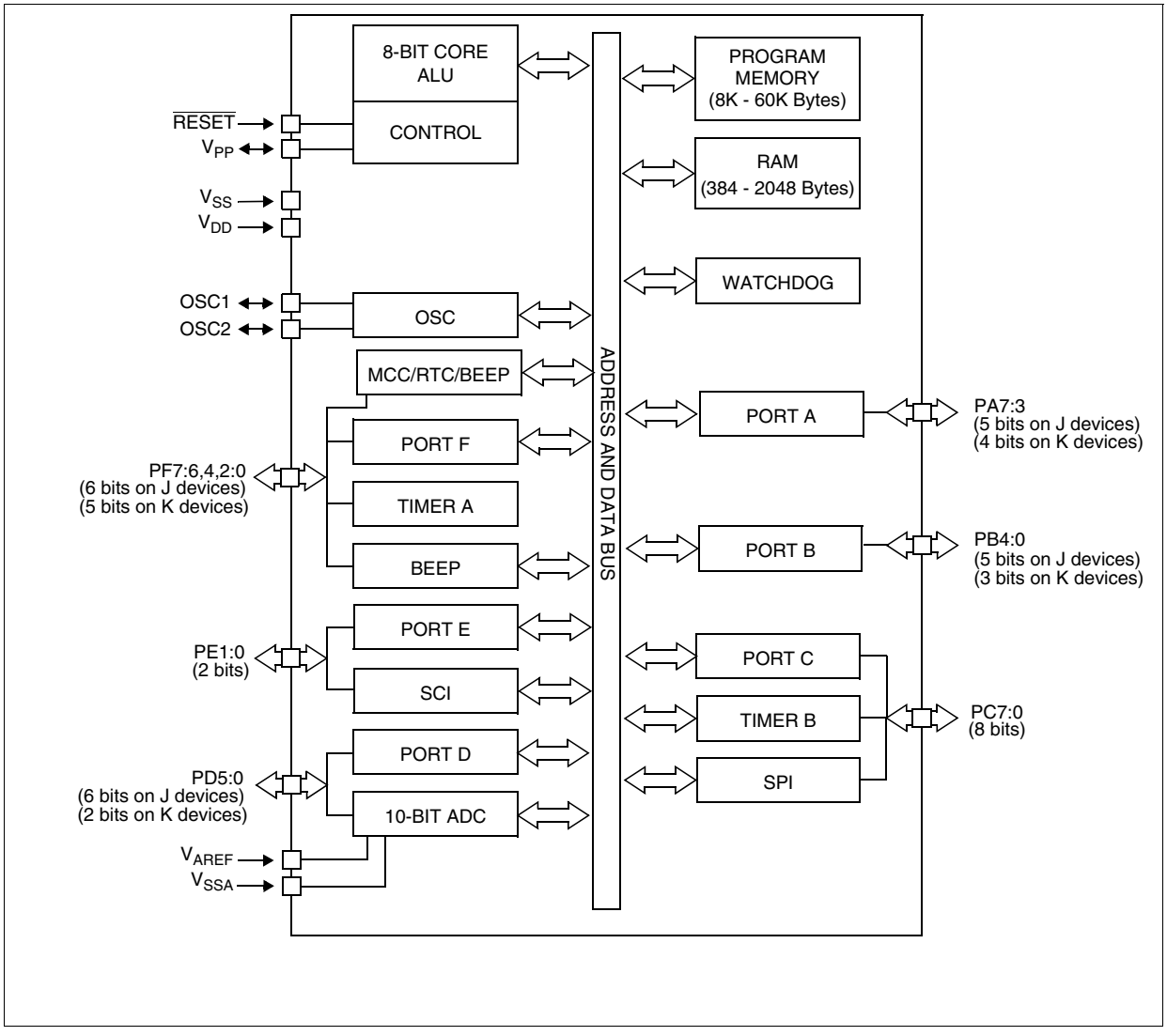
– The 44-pin devices target the same range of applications requiring more than 24 I/O ports.

All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with FLASH or ROM program memory.

Under software control, all devices can be placed in WAIT, SLOW, ACTIVE-HALT or HALT mode, reducing power consumption when the application is in idle or stand-by state.

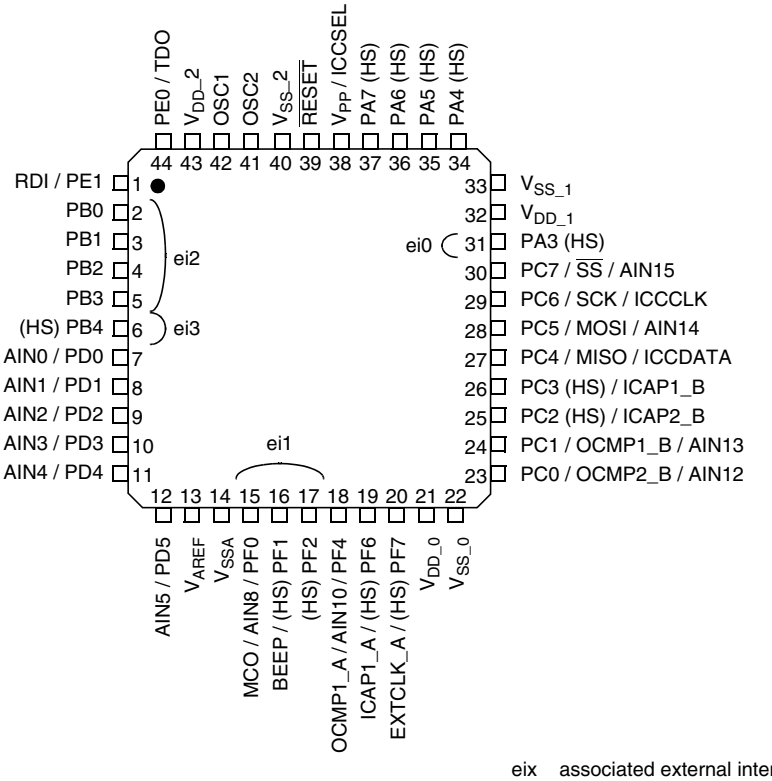
The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

Figure 1. Device Block Diagram



2 PIN DESCRIPTION

Figure 2. 44-Pin TQFP Package Pinouts



PIN DESCRIPTION (Cont'd)

Figure 3. 32-Pin SDIP Package Pinout

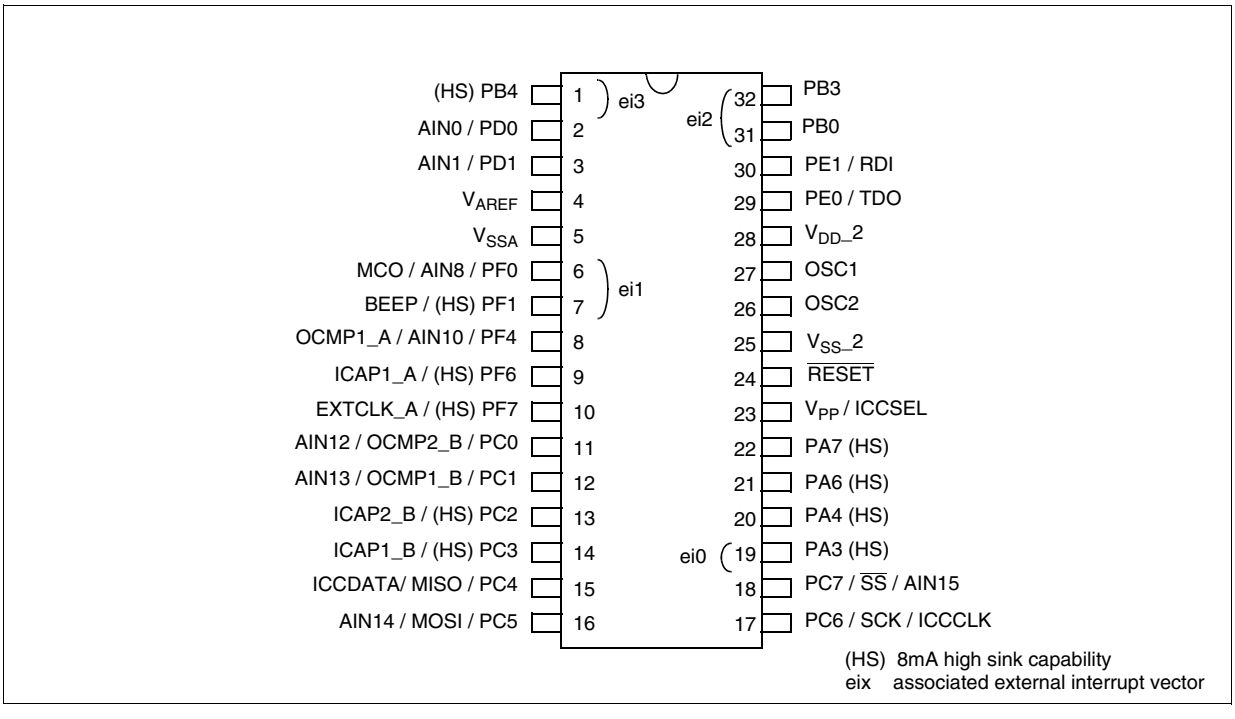
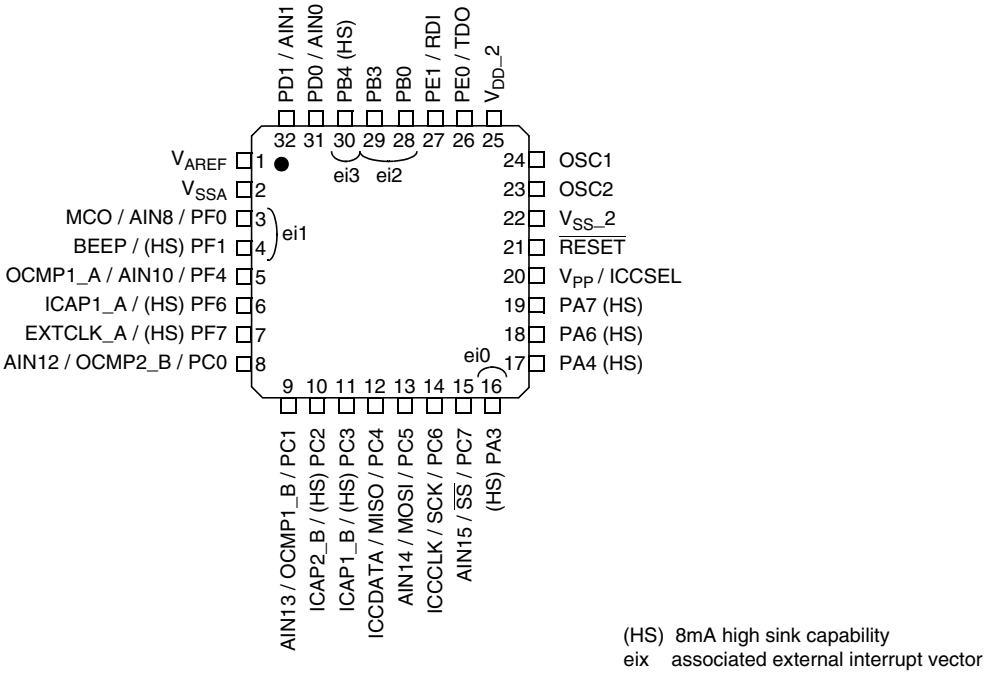


Figure 4. 32-Pin TQFP 7x7 Package Pinout



PIN DESCRIPTION (Cont'd)

For more details, refer to "ELECTRICAL CHARACTERISTICS" on page 110

Legend / Abbreviations for Table 1:

Type: I = input, O = output, S = supply

In/Output level: C = CMOS
C_T= CMOS with input trigger

Output level: HS = high sink (on N-buffer only)

Port and control configuration:

– Input: float = floating, wpu = weak pull-up, int = interrupt [1], ana = analog ports

– Output: OD = open drain [2], PP = push-pull

Refer to "I/O PORTS" on page 39 for more details on the software configuration of the I/O ports.

The RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Table 1. Device Pin Description

Pin n°			Pin Name	Type	Level		Port						Main function (after reset)	Alternate Function	
							Input				Output				
TQFP44	TQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD	PP			
6	30	1	PB4 (HS)	I/O	C_T	HS	**X**	ei3			X	X	Port B4		
7	31	2	PD0/AIN0	I/O	C_T		**X**	X		X	X	X	Port D0	ADC Analog Input 0	
8	32	3	PD1/AIN1	I/O	C_T		**X**	X		X	X	X	Port D1	ADC Analog Input 1	
9			PD2/AIN2	I/O	C_T		**X**	X		X	X	X	Port D2	ADC Analog Input 2	
10			PD3/AIN3	I/O	C_T		**X**	X		X	X	X	Port D3	ADC Analog Input 3	
11			PD4/AIN4	I/O	C_T		**X**	X		X	X	X	Port D4	ADC Analog Input 4	
12			PD5/AIN5	I/O	C_T		**X**	X		X	X	X	Port D5	ADC Analog Input 5	
13	1	4	V_{AREF}	S									Analog Reference Voltage for ADC		
14	2	5	V_{SSA}	S									Analog Ground Voltage		
15	3	6	PF0/MCO/AIN8	I/O	C_T		**X**	ei1		X	X	X	Port F0	Main clock out (f_{OSC}/2)	ADC Analog Input 8
16	4	7	PF1 (HS)/BEEP	I/O	C_T	HS	**X**	ei1			X	X	Port F1	Beep signal output	
17			PF2 (HS)	I/O	C_T	HS	**X**		ei1		X	X	Port F2		
18	5	8	PF4/OCMP1_A/ AIN10	I/O	C_T		**X**	X		X	X	X	Port F4	Timer A Output Compare 1	ADC Analog Input 10
19	6	9	PF6 (HS)/ICAP1_A	I/O	C_T	HS	**X**	X			X	X	Port F6	Timer A Input Capture 1	
20	7	10	PF7 (HS)/ EXTCLK_A	I/O	C_T	HS	**X**	X			X	X	Port F7	Timer A External Clock Source	
21			V_{DD_0}	S									Digital Main Supply Voltage		
22			V_{SS_0}	S									Digital Ground Voltage		
23	8	11	PC0/OCMP2_B/ AIN12	I/O	C_T		**X**	X		X	X	X	Port C0	Timer B Output Compare 2	ADC Analog Input 12
24	9	12	PC1/OCMP1_B/ AIN13	I/O	C_T		**X**	X		X	X	X	Port C1	Timer B Output Compare 1	ADC Analog Input 13

Pin n°			Pin Name	Type	Level		Port						Main function (after reset)	Alternate Function	
							Input				Output				
TQFP44	TQFP32	SDIP32			Input	Output	float	wpu	int	ana	OD	PP			
25	10	13	PC2 (HS)/ICAP2_B	I/O	C_T	HS	X	X			X	X	Port C2	Timer B Input Capture 2	
26	11	14	PC3 (HS)/ICAP1_B	I/O	C_T	HS	X	X			X	X	Port C3	Timer B Input Capture 1	
27	12	15	PC4/MISO/ICCDATA	I/O	C_T		X	X			X	X	Port C4	SPI Master In / Slave Out Data	ICC Data Input
28	13	16	PC5/MOSI/AIN14	I/O	C_T		X	X		X	X	X	Port C5	SPI Master Out / Slave In Data	ADC Analog Input 14
29	14	17	PC6/SCK/ICCCLK	I/O	C_T		X	X			X	X	Port C6	SPI Serial Clock	ICC Clock Output
30	15	18	PC7/$\overline{SS}$/AIN15	I/O	C_T		X	X		X	X	X	Port C7	SPI Slave Select (active low)	ADC Analog Input 15
31	16	19	PA3 (HS)	I/O	C_T	HS	X		ei0		X	X	Port A3		
32			V_{DD_1}	S									Digital Main Supply Voltage		
33			V_{SS_1}	S									Digital Ground Voltage		
34	17	20	PA4 (HS)	I/O	C_T	HS	X	X			X	X	Port A4		
35			PA5 (HS)	I/O	C_T	HS	X	X			X	X	Port A5		
36	18	21	PA6 (HS)	I/O	C_T	HS	X				T		Port A6 [1)]		
37	19	22	PA7 (HS)	I/O	C_T	HS	X				T		Port A7 [1)]		
38	20	23	V_{PP} /ICCSEL	I									Must be tied low. In the flash programming mode, this pin acts as the programming voltage input V_{PP}. See Section 12.9.2 for more details. High voltage must not be applied to ROM devices.		
39	21	24	$\overline{RESET}$	I/O	C_T								Top priority non maskable interrupt.		
40	22	25	V_{SS_2}	S									Digital Ground Voltage		
41	23	26	OSC2	O									Resonator oscillator inverter output		
42	24	27	OSC1	I									External clock input or Resonator oscillator inverter input		
43	25	28	V_{DD_2}	S									Digital Main Supply Voltage		
44	26	29	PE0/TDO	I/O	C_T		X	X			X	X	Port E0	SCI Transmit Data Out	
1	27	30	PE1/RDI	I/O	C_T		X	X			X	X	Port E1	SCI Receive Data In	
2	28	31	PB0	I/O	C_T		X	ei2			X	X	Port B0		
3			PB1	I/O	C_T		X	ei2			X	X	Port B1		
4			PB2	I/O	C_T		X	ei2			X	X	Port B2		
5	29	32	PB3	I/O	C_T		X		ei2		X	X	Port B3		

Notes:

1. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input, else the configuration is floating interrupt input.

2. In the open drain output column, “T” defines a true open drain I/O (P-Buffer and protection diode to V_{DD}

are not implemented). See See “I/O PORTS” on page 39. and Section 12.8 I/O PORT PIN CHARACTERISTICS for more details.

3. OSC1 and OSC2 pins connect a crystal/ceramic resonator, or an external source to the on-chip oscillator; see Section 1 INTRODUCTION and Section 12.5 CLOCK AND TIMING CHARACTERISTICS for more details.

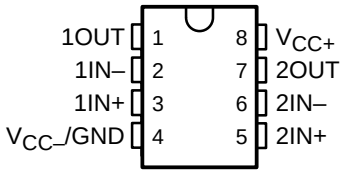
4. On the chip, each I/O port has 8 pads. Pads that are not bonded to external pins are in input pull-up configuration after reset. The configuration of these pads must be kept at reset state to avoid added current consumption.

TL3472
HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

- **Wide Gain-Bandwidth Product . . . 4 MHz**
- **High Slew Rate . . . 13 V/μs**
- **Fast Settling Time . . . 1.1 μs to 0.1%**
- **Wide-Range Single-Supply Operation . . . 4 V to 36 V**
- **Wide Input Common-Mode Range Includes Ground ($V_{CC–}$)**
- **Low Total Harmonic Distortion . . . 0.02%**
- **Large-Capacitance Drive Capability . . . 10,000 pF**
- **Output Short-Circuit Protection**

D OR P PACKAGE
(TOP VIEW)



description/ordering information

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, 13-V/μs slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential ($V_{CC–}$). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

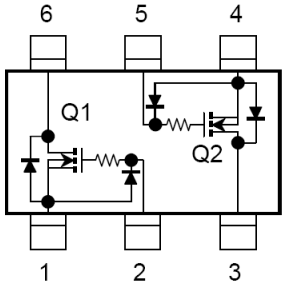
ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 25	TL3472CP	TL3472CP
	SOIC (D)	Tube of 50	TL3472CD	3472C
		Reel of 2500	TL3472CDR	
–40°C to 105°C	PDIP (P)	Tube of 25	TL3472IP	TL3472IP
	SOIC (D)	Tube of 50	TL3472ID	Z3472
		Reel of 2500	TL3472IDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

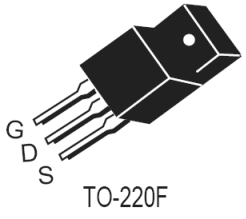
Semiconductors

HK1K02FU N CHANNEL IC96
HK1K05FU N CHANNEL IC16,43

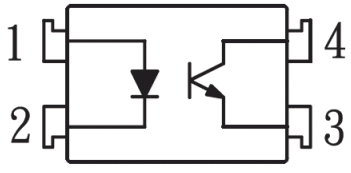


1. Source 1
2, Gate 1
3. Drain 2
4. Source 2
5. Gate 2
6. Drain 1

CEF04N7 N CHANNEL
IC33

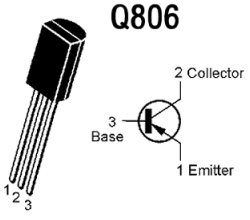


PC17L1 Photo Coupler
PC31-33 IC46

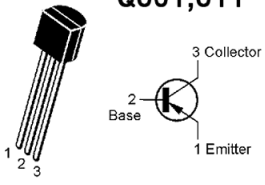


1. Anode
2. Cathode
3. Emitter
4. Collector

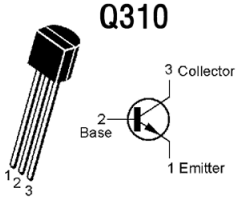
KSA916Y
Q806



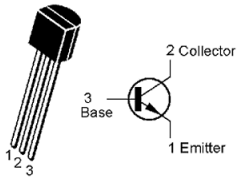
KSA708
Q301,311



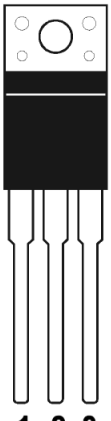
KTN2222A
Q310



KRC10M Q314

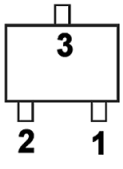


KIA7809 IC79



1. IN
2. GROUND
3. OUT

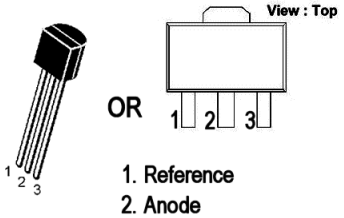
KTA2014 PNP Q501-505
KTC3875S NPN Q403
KTA1504S PNP Q402
KRA107S PNP Q604,701,702,801-805
KTD1304 NPN Q807-822
2N3904S NPN Q101-103,Q823
KRC 107S NPN Q401



1) Emitter
2) Base
3) Collector

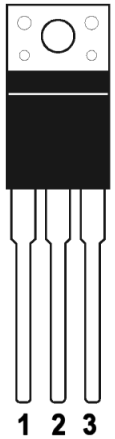
KIA431B
IC34,35

TO-92 SOT-89



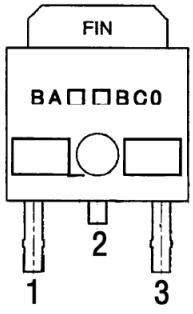
1. Reference
2. Anode
3. Cathode

KIA7909 IC80

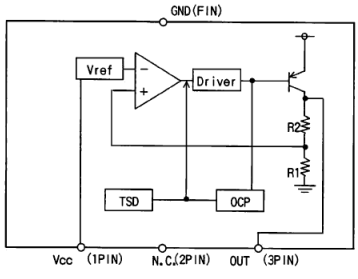


1. GROUND
2. IN
3. OUT

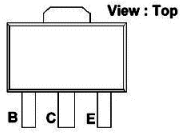
BA50BC0FP IC56
BA18BC0FP IC24,65



BLOCK DIAGRAM

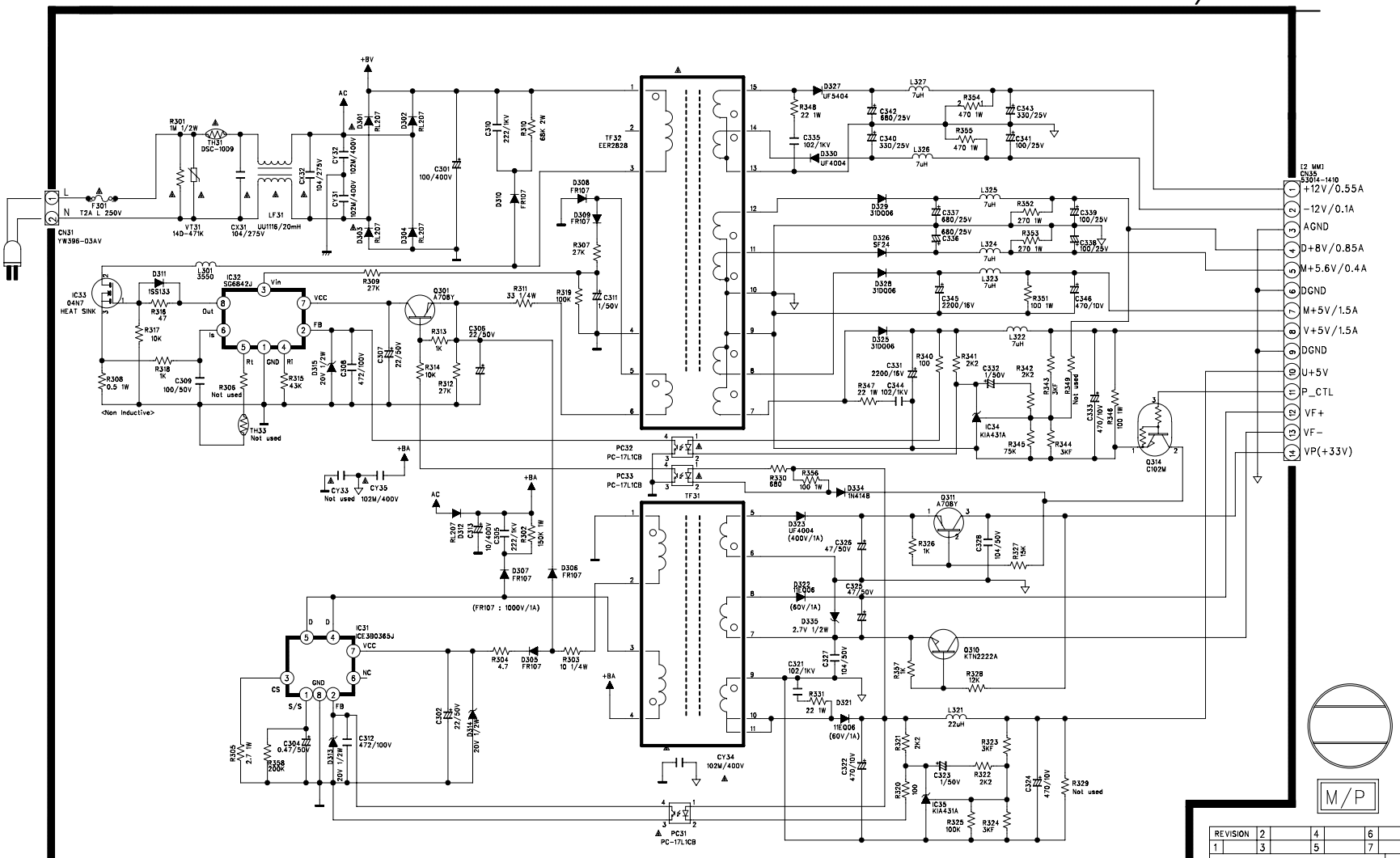


KTA1664
Q104,105



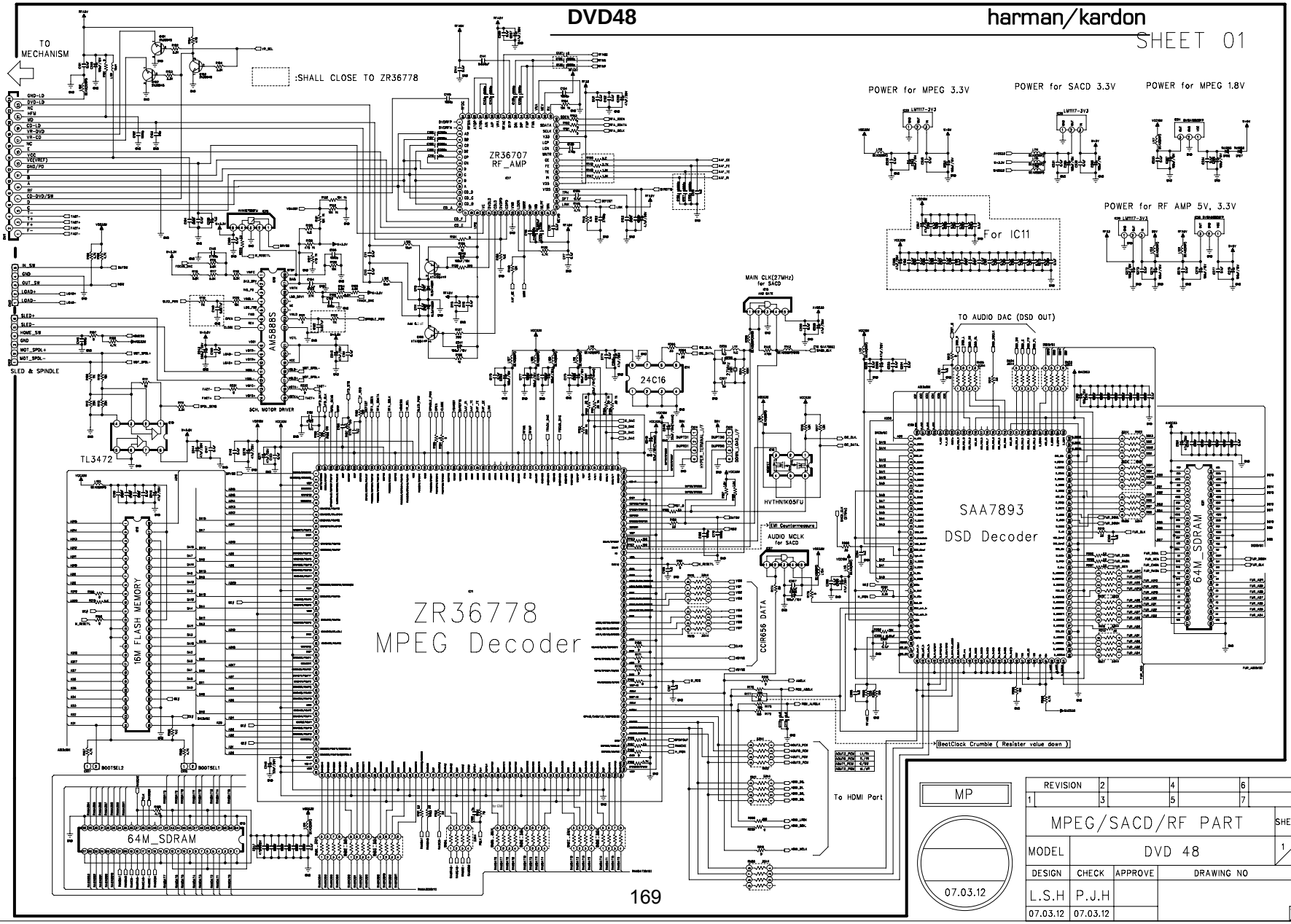
1 Base
2 Collector
3 Emitter

DVD-48 SMPS SCHEMATIC DIAGRAM



REVISION	2		4		6	
1		3		5		7

SCHEMATIC DIAGRAM			SHEET
MODEL	DVD-48		1/1
	CH		DRAWING NO
A.B.C	D.E.F	G.H.I	XXXXXXXX
06.11.06	06.11.06	06.11.06	(SMPS) 1/1



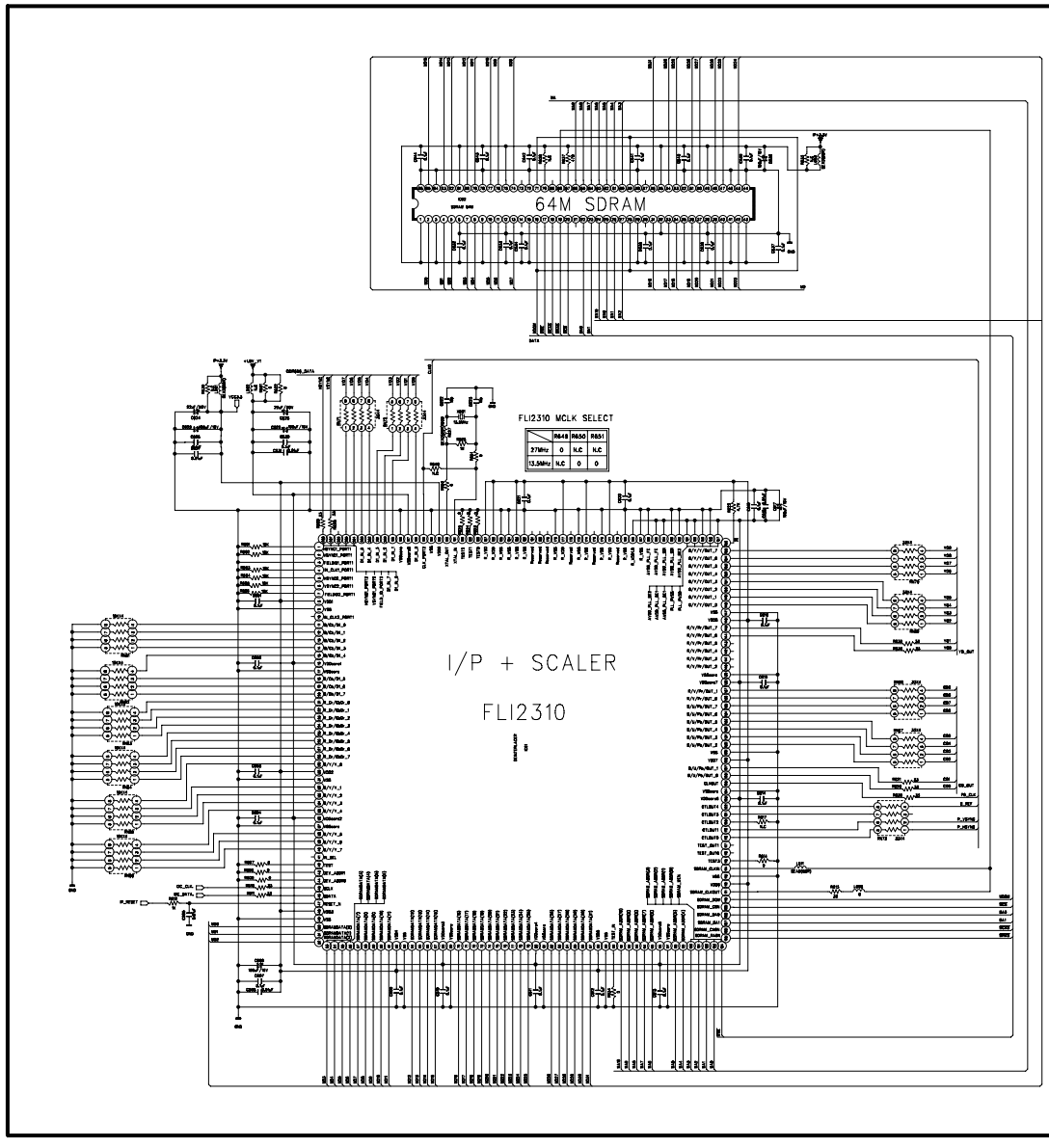
REVISION	2		4		6	
1		3		5		7

MP

07.03.12

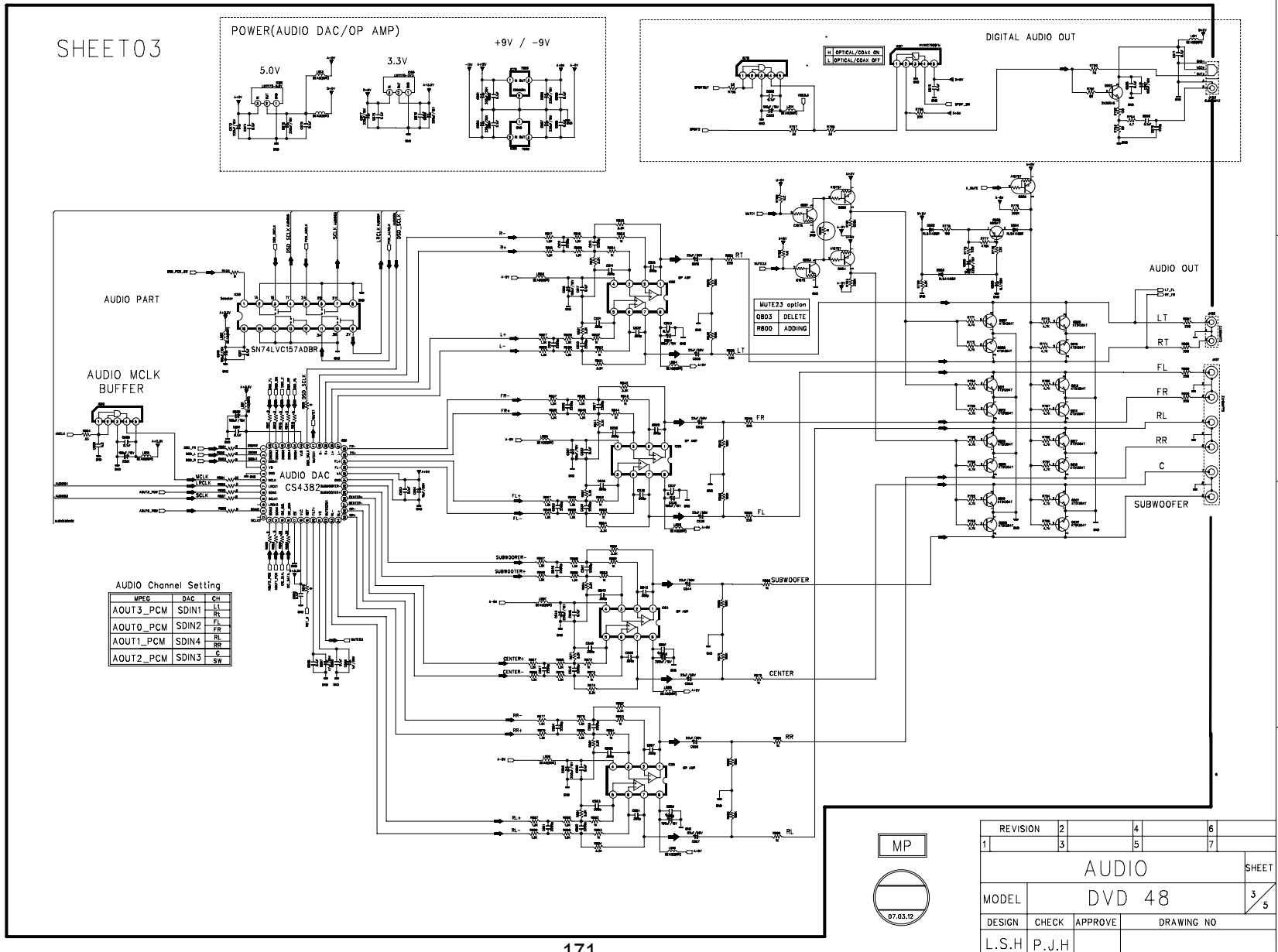
MPEG/SACD/RF PART — SHEET 1/5

MODEL	DVD 48	
DESIGN	CHECK	APPROVE	DRAWING NO
L.S.H	P.J.H		
07.03.12	07.03.12		1/5

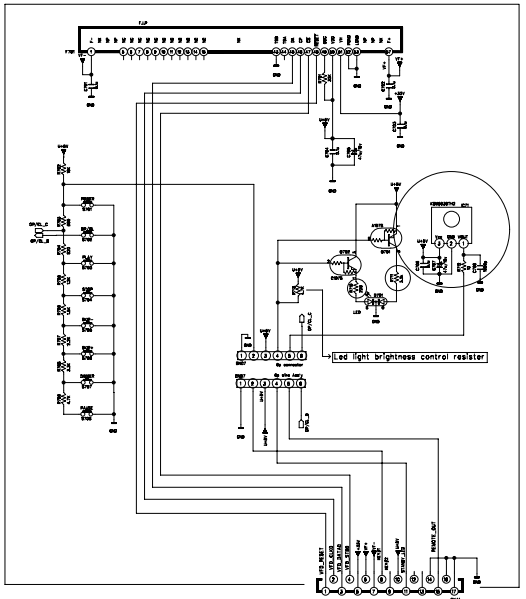


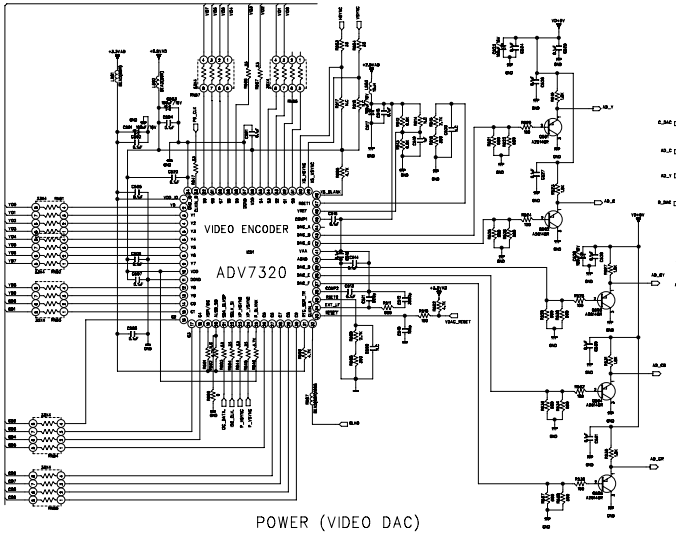
REVISION	2	4	6	
1	3	5	7	

I/P + UPSCALER			SHEET 2/5
MODEL	DVD 48		
DESIGN	CHECK	APPROVE	DRAWING NO
L.S.H	P.J.H		
07.03.12	07.03.12		2-5

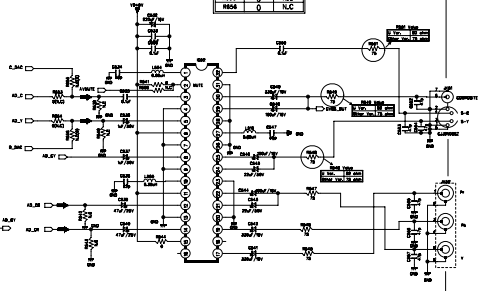

SHEET03
POWER(AUDIO DAC/OP AMP)
5.0V
3.3V
+9V / -9V
DIGITAL AUDIO OUT
H OPTICAL/COAX ON
L OPTICAL/COAX OFF
AUDIO PART
SN74LVC157ADBR
AUDIO MCLK BUFFER
AUDIO DAC CS4382
MUTE23 option
Q803 DELETE
R800 ADDING
AUDIO OUT
LT
RT
FL
FR
RL
RR
C
SUBWOOFER
AUDIO Channel Setting
MPEG DAC CH
AOUT3_PCM SDIN1 LT RT
AOUT0_PCM SDIN2 FL FR
AOUT1_PCM SDIN4 RL RR
AOUT2_PCM SDIN3 C SW
MP
07.03.12
REVISION
AUDIO
SHEET
MODEL DVD 48 3/5
DESIGN CHECK APPROVE DRAWING NO
L.S.H P.J.H
07.03.12 07.03.12
3/5

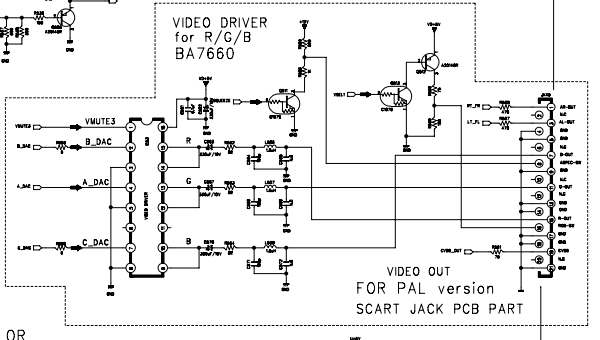
SHEET04 **DVD48** harman/kardon

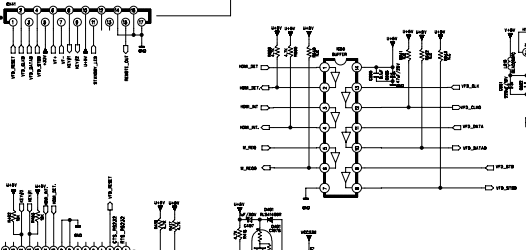


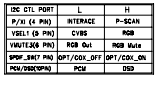


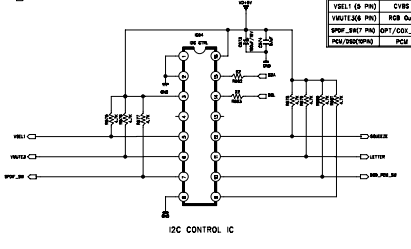
POWER (VIDEO DAC)

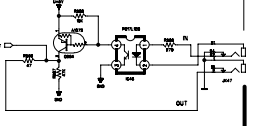






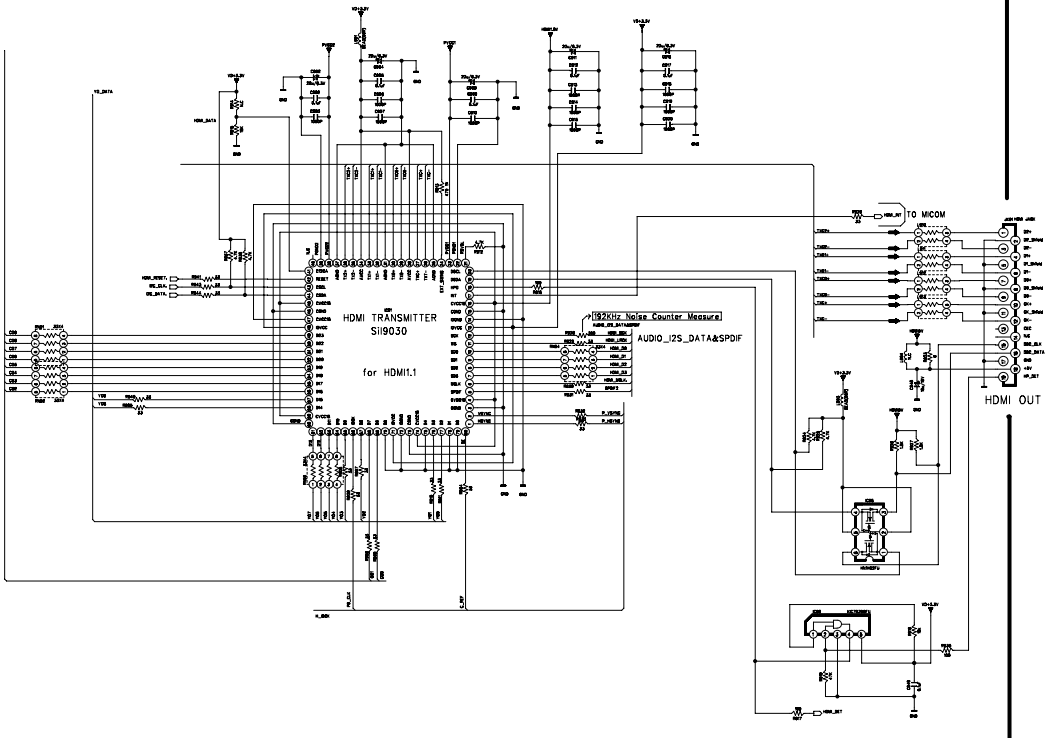




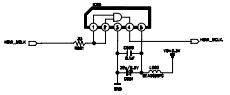


REVISION	2		4	6	
1	3		5	7	
MP	FRONT/HOST/VIDEO				SHEET 4/5
07.03.12	MODEL	DVD 48			
DESIGN	CHECK	APPROVE	DRAWING NO		
L.S.H	P.J.H				
07.03.12	07.03.12				4/5

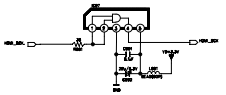
SHEET 5



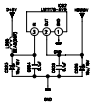
AUDIO MCLK BUFFER



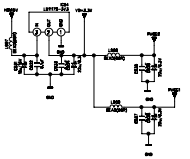
HDMI_BCK BUFFER



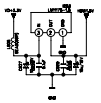
POWER (+8V -> +5V)



POWER (+5V -> +3.3V)



POWER (+3.3V -> +1.8V)



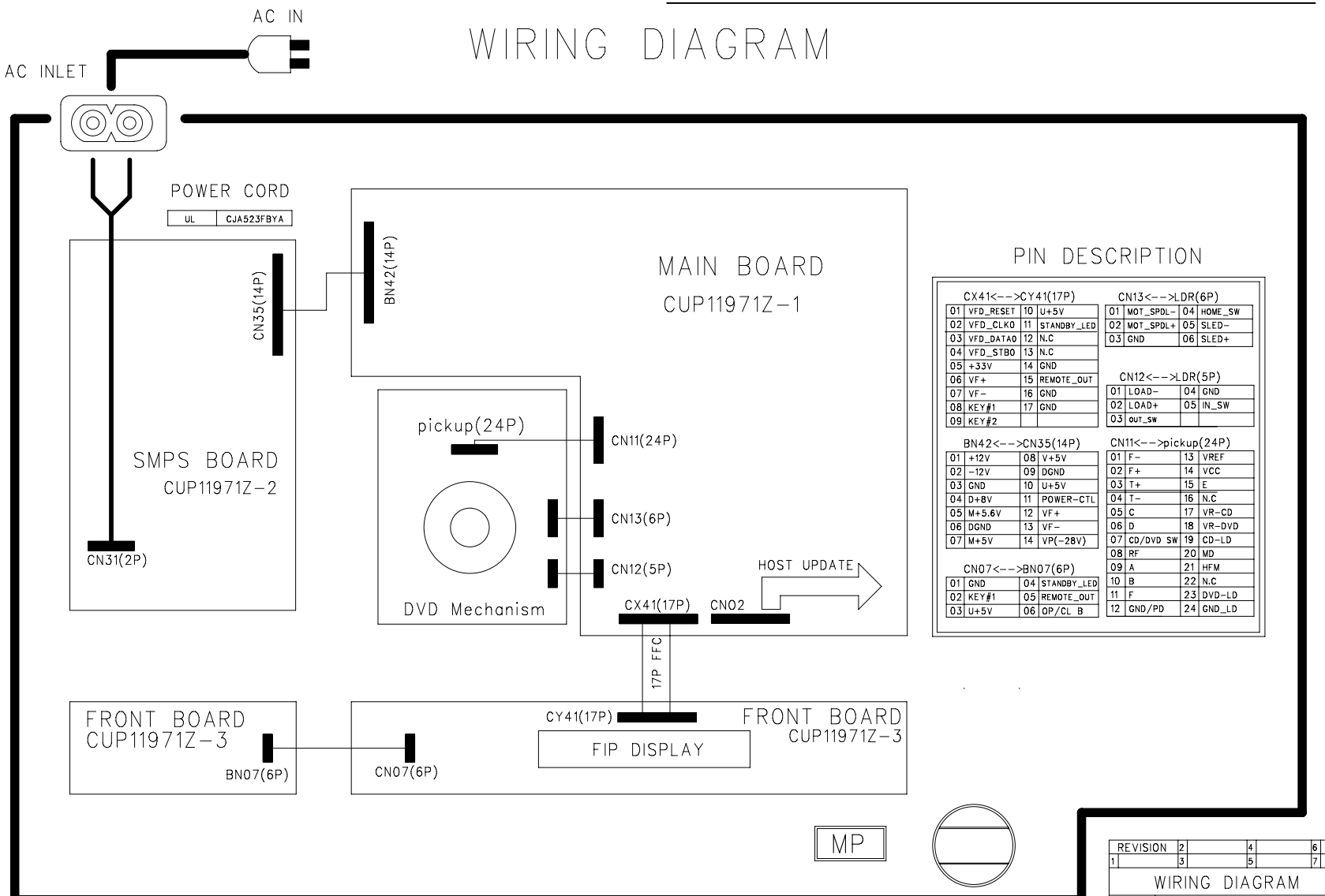
REVISION	2	4	6	
1	3	5	7	

MP

07.03.12

HDMI 1.1			SHEET
MODEL	DVD 48		5/5
DESIGN	CHECK	APPROVE	DRAWING NO
L.S.H	P.J.H		
07.03.12	07.03.12		5/5

WIRING DIAGRAM



PIN DESCRIPTION

CX41<-->CY41(17P)

01	VFD_RESET	10	U+5V
02	VFD_CLK0	11	STANDBY_LED
03	VFD_DATA0	12	N.C
04	VFD_STB0	13	N.C
05	+33V	14	GND
06	VF+	15	REMOTE_OUT
07	VF-	16	GND
08	KEY#1	17	GND
09	KEY#2		

CN13<-->LDR(6P)

01	MOT_SPDL-	04	HOME_SW
02	MOT_SPDL+	05	SLED-
03	GND	06	SLED+

CN12<-->LDR(5P)

01	LOAD-	04	GND
02	LOAD+	05	IN_SW
03	OUT_SW		

BN42<-->CN35(14P)

01	+12V	08	V+5V
02	-12V	09	DGND
03	GND	10	U+5V
04	D+8V	11	POWER-CTL
05	M+5.6V	12	VF+
06	DGND	13	VF-
07	M+5V	14	VP(-28V)

CN11<-->pickup(24P)

01	F-	13	VREF
02	F+	14	VCC
03	T+	15	E
04	T-	16	N.C
05	C	17	VR-CD
06	D	18	VR-DVD
07	CD/DVD SW	19	CD-LD
08	RF	20	MD
09	A	21	HFM
10	B	22	N.C
11	F	23	DVD-LD
12	GND/PD	24	GND_LD

CN07<-->BN07(6P)

01	GND	04	STANDBY_LED
02	KEY#1	05	REMOTE_OUT
03	U+5V	06	OP/CL B

REVISION							
1		3		5		7	
WIRING DIAGRAM						SHEET	
MODEL	DVD48					1/1	
DESIGN	CHECK	APPROVE	DRAWING NO				
L.S.H	P.J.H						
07.03.12	07.03.12					1/1	