

SERVICE MANUAL

English

No. 1193-1

1278

This unit employs the UD-1 standard mechanism. When inspecting and repairing this unit, read this together with the service manual (No. 1155) of the UD mechanism (UD-1).

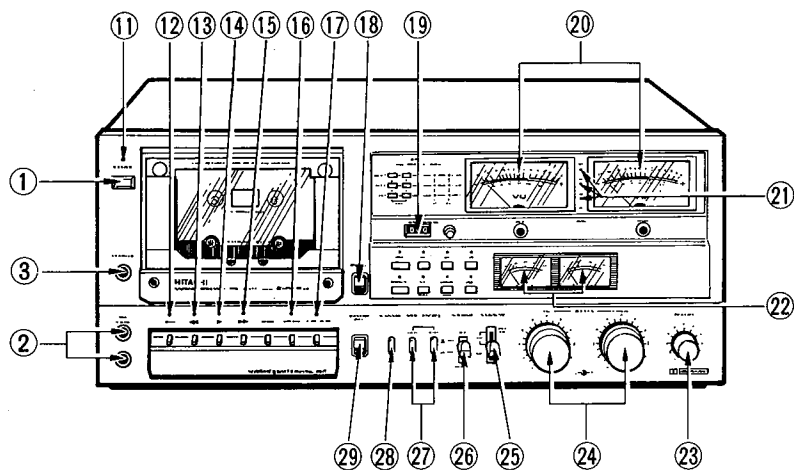
Note:

U USA
 C Canada
 W General Area

FS Switzerland and
 Scandinavia
 BS Great Britain
 AU Australia

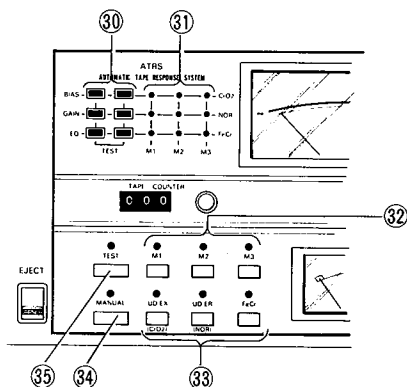
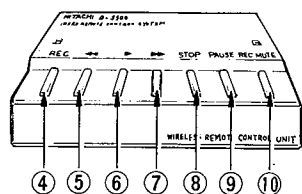
SAFETY PRECAUTION

- The following precautions should be observed when servicing.
1. Since many parts in the unit have special safety related characteristics, always use genuine Hitachi's replacement parts. Especially critical parts in the power circuit block should not be replaced with other makers. Critical parts are marked with Δ in the schematic diagram, and circuit board diagram.
 2. Before returning a repaired unit to the customer, the service technician must thoroughly test the unit to ascertain that it is completely safe to operate without danger of electrical shock.



KEY TO ILLUSTRATIONS

- 1 POWER SWITCH
- 2 MIC JACKS (MIC)
- 3 HEADPHONE JACK (PHONES)
- 4 RECORDING BUTTON (REC)
- 5 REWIND BUTTON (◀◀)
- 6 PLAYBACK BUTTON (▶▶)
- 7 FAST-FORWARD BUTTON (▶▶▶)
- 8 STOP BUTTONS (STOP)
- 9 PAUSE BUTTON (PAUSE)
- 10 REC MUTE SWITCH (REC MUTE)
- 11 POWER INDICATOR
- 12 REC INDICATOR
- 13 REWIND INDICATOR
- 14 PLAYBACK INDICATOR
- 15 FAST FORWARD INDICATOR
- 16 PAUSE INDICATOR
- 17 REC MUTE INDICATOR
- 18 EJECT BUTTON (EJECT)
- 19 TAPE COUNTER (TAPE COUNTER)
- 20 VU METERS
- 21 PEAK INDICATOR
- 22 BIAS/TAPE SENSITIVITY INDICATING METERS
- 23 OUTPUT LEVEL CONTROL (OUTPUT)
- 24 RECORDING LEVEL CONTROLS (RECORD)
- 25 DOLBY NOISE REDUCTION SWITCH/MPX FILTER SWITCH (DOLBY NR)
- 26 MONITOR SWITCH (MONITOR)
- 27 AUTO-REWIND SWITCHES
- 28 MEMORY SWITCH (MEMORY)
- 29 CONTROL UNIT REMOVAL BUTTON (REMOTE REMOVAL)
- 30 TEST INDICATOR
- 31 MEMORY INDICATORS
- 32 MEMORY BUTTONS
- 33 TAPE SELECT BUTTONS
- 34 MANUAL BUTTON (MANUAL)
- 35 TEST BUTTON (TEST)



STEREO CASSETTE TAPE DECK

CONTENTS

SPECIFICATIONS	4
BLOCK DIAGRAM (Amplifier and Power supply sections)	5
BLOCK DIAGRAM (Control section)	7
TECHNICAL INFORMATION OF ATRS	9
1. Operation and Description of Each Mode	9
2. Initial Start Circuit when the power is switched ON	10
1) Operation when power is switched ON	10
2) Operation immediately after power is switched OFF	10
3. Power OFF, Cassette and Test Mode Stop Detections	11
1) Power OFF detection	11
2) Cassette detection	11
3) Test mode stop detection	12
4. Tape Selector/Memory Selections	12
1) Tape selector selection	12
2) Memory selection	13
5. Test Mode Selection	13
6. Test Data Transfer to Memory	14
7. Stop Signal Generation Circuit	14
8. Battery Alarm Circuit	15
9. IC HD74145P	15
10. Memory Indicator Circuit	16
11. Data Storage when power is switched OFF	18
12. Recording/Playback Circuit Block Diagram	20
13. Playback High Frequency Range Compensation Circuit	20
14. Gain Control Circuit	21
1) Principle of D/A convertor (4 bit control signal)	21
2) When Z1 — Z4 has pure resistance (R)	22
3) When Z1 — Z4 are composed of pure resistance (R) and capacitance (C)	22
4) When Z1 — Z4 are composed of resistance (R) and inductance (L)	22
5) Low frequency range sensitivity compensation circuit	23
6) Medium frequency range compensation circuit	23
7) High frequency range compensation circuit	23
15. Data Transfer Circuit in Recording Equalizer Section	24
1) Sift resistor (IC511)	25
2) Multiplex (IC512)	25
3) Operation of data transfer circuit	25
4) Switching signal generation timing diagram	26
16. Bias Oscillator Circuit	27
1) Oscillator circuit	27
2) Variable recording bias circuit and temperature compensation circuit	27
3) Bias/EQ test and tape selector detection circuit	28
4) Bias setting	28
17. Test-in-progress Indicator	29
18. Playback Gain Detector Circuit	29
1) Amplifier and rectifier peak hold circuit	30
2) L/R channel switch	30
3) Comparison and peak detection circuits	31



HITACHI

D-5500

SERVICE MANUAL

No. 1193

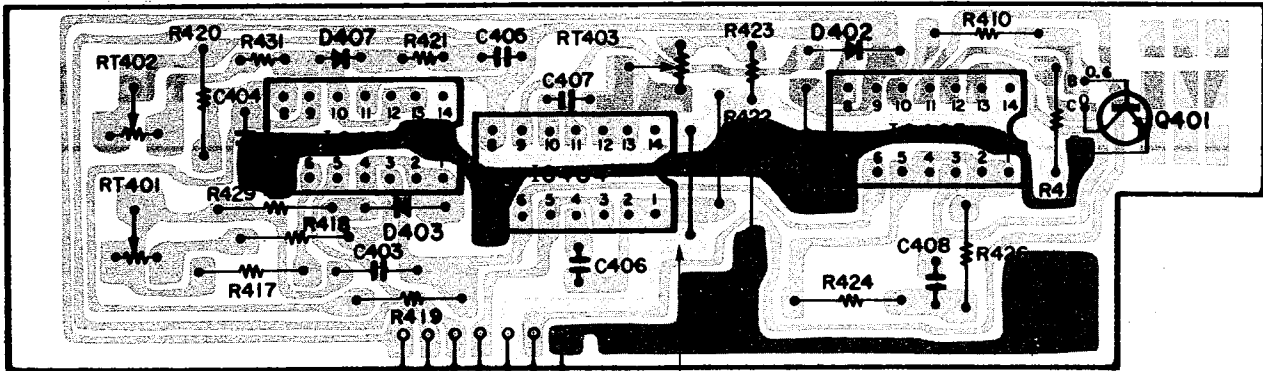
This service manual only shows the Schematic diagram, Circuit board diagram and Wiring diagram.
We will issue the completely service manual including Technical informations, Adjustments, Exploded views and Replacement parts list.

STEREO CASSETTE TAPE DECK

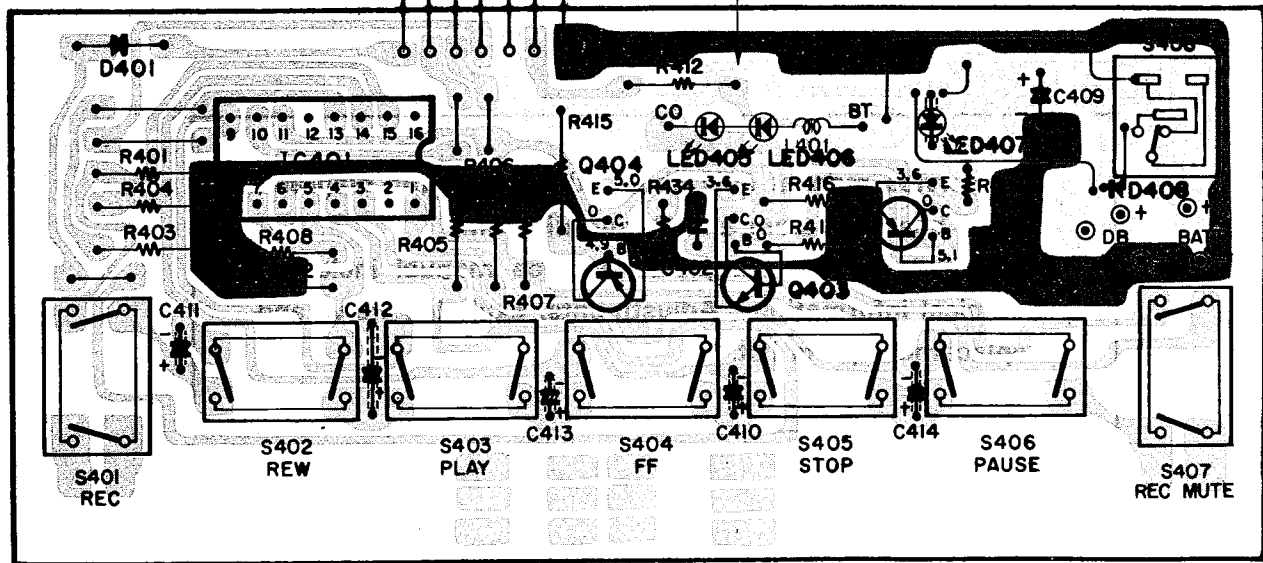
April. 1979

CIRCUIT BOARD DIAGRAM

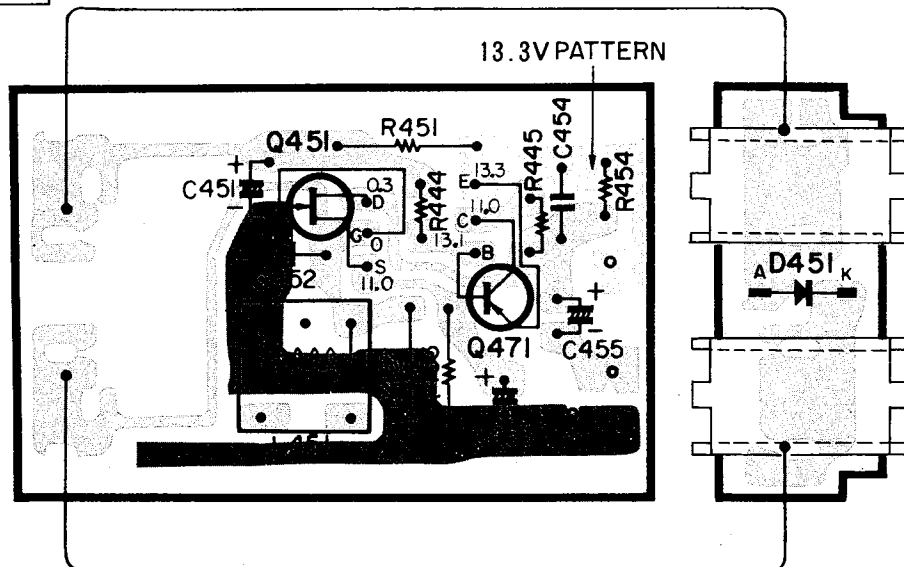
Transmission P.C.B.-A

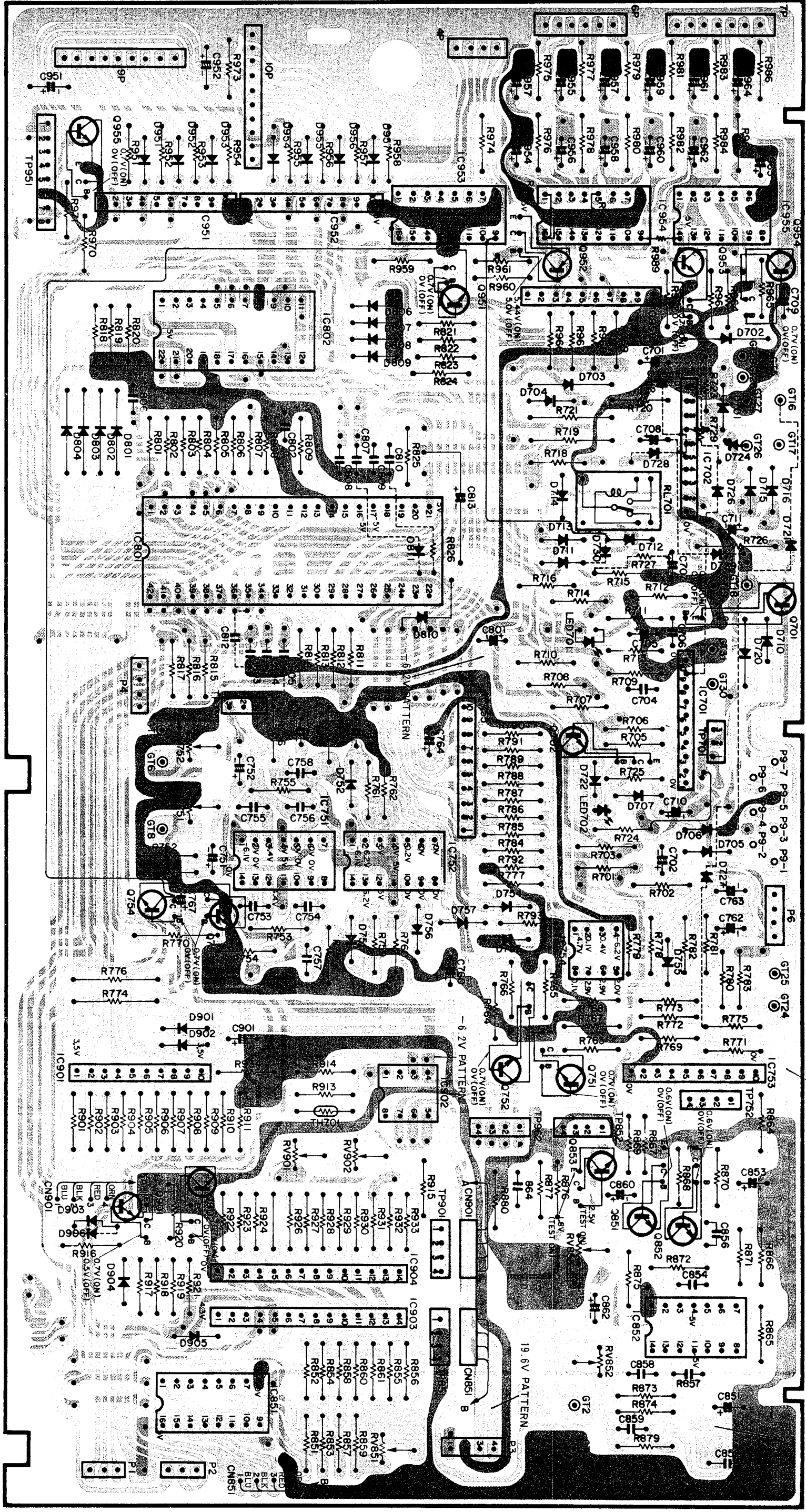


Transmission P.C.B.-B



Light Receiving P.C.B.

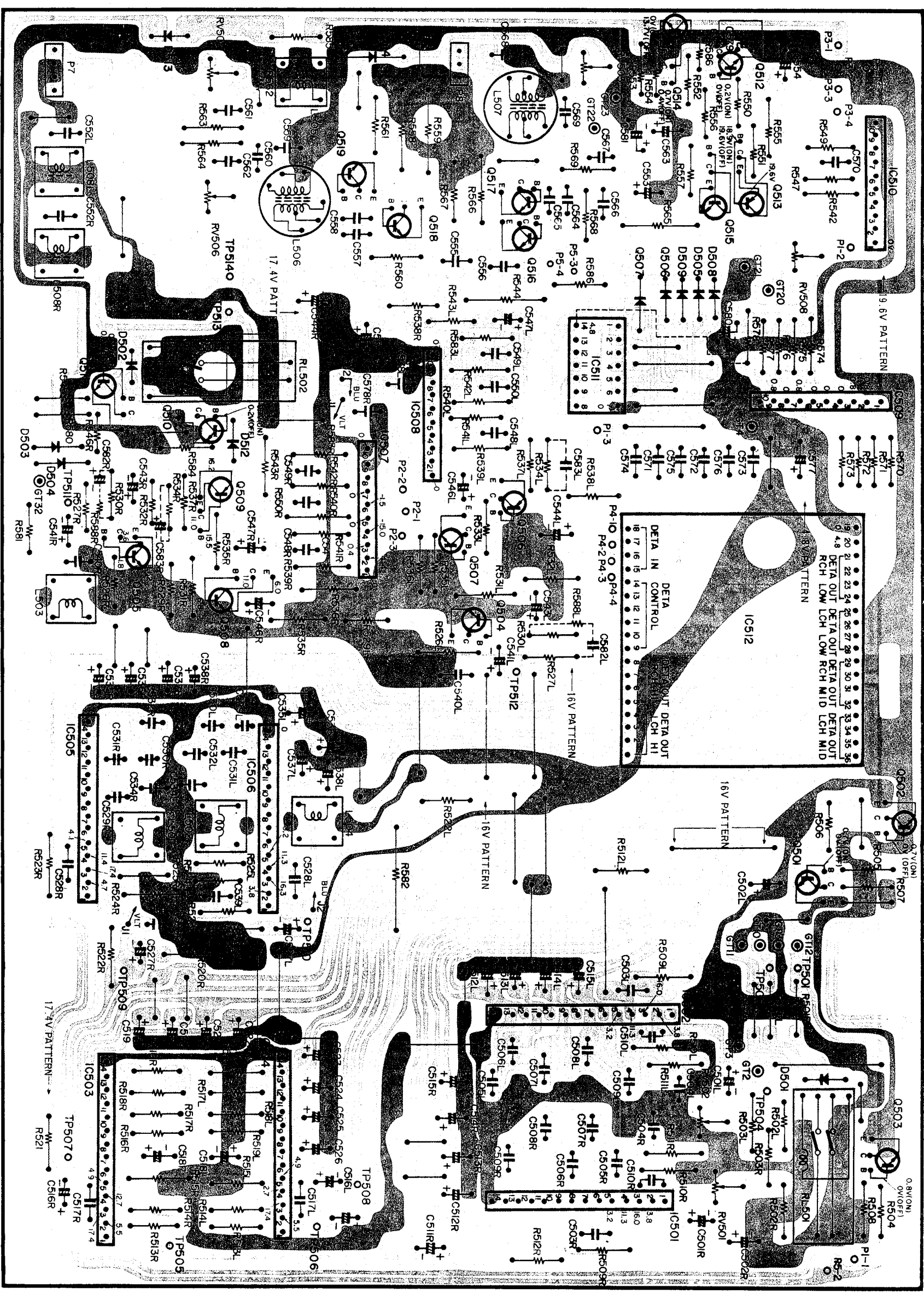


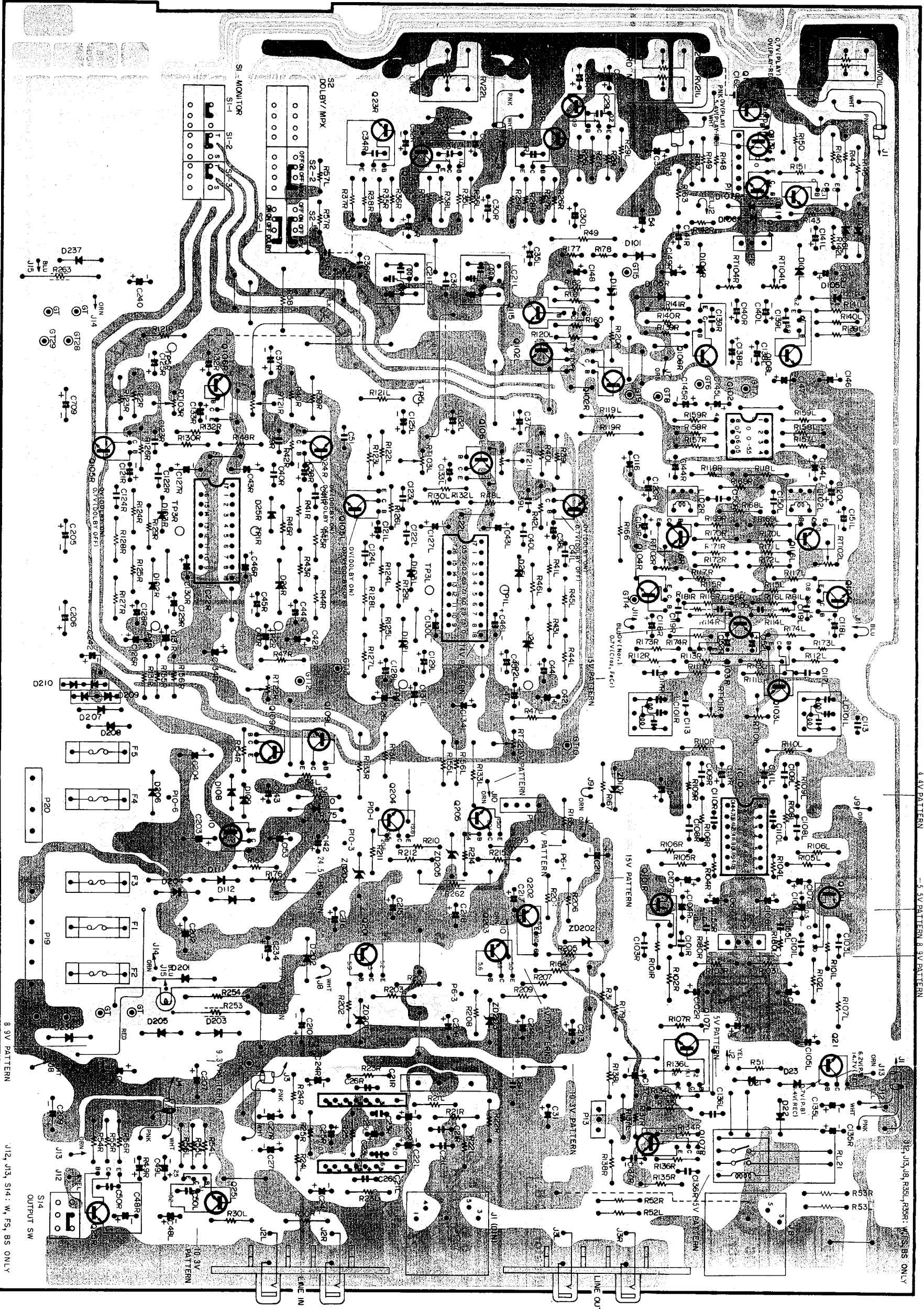


5V PATTERN

6.2V PATTERN

19.6V PATTERN





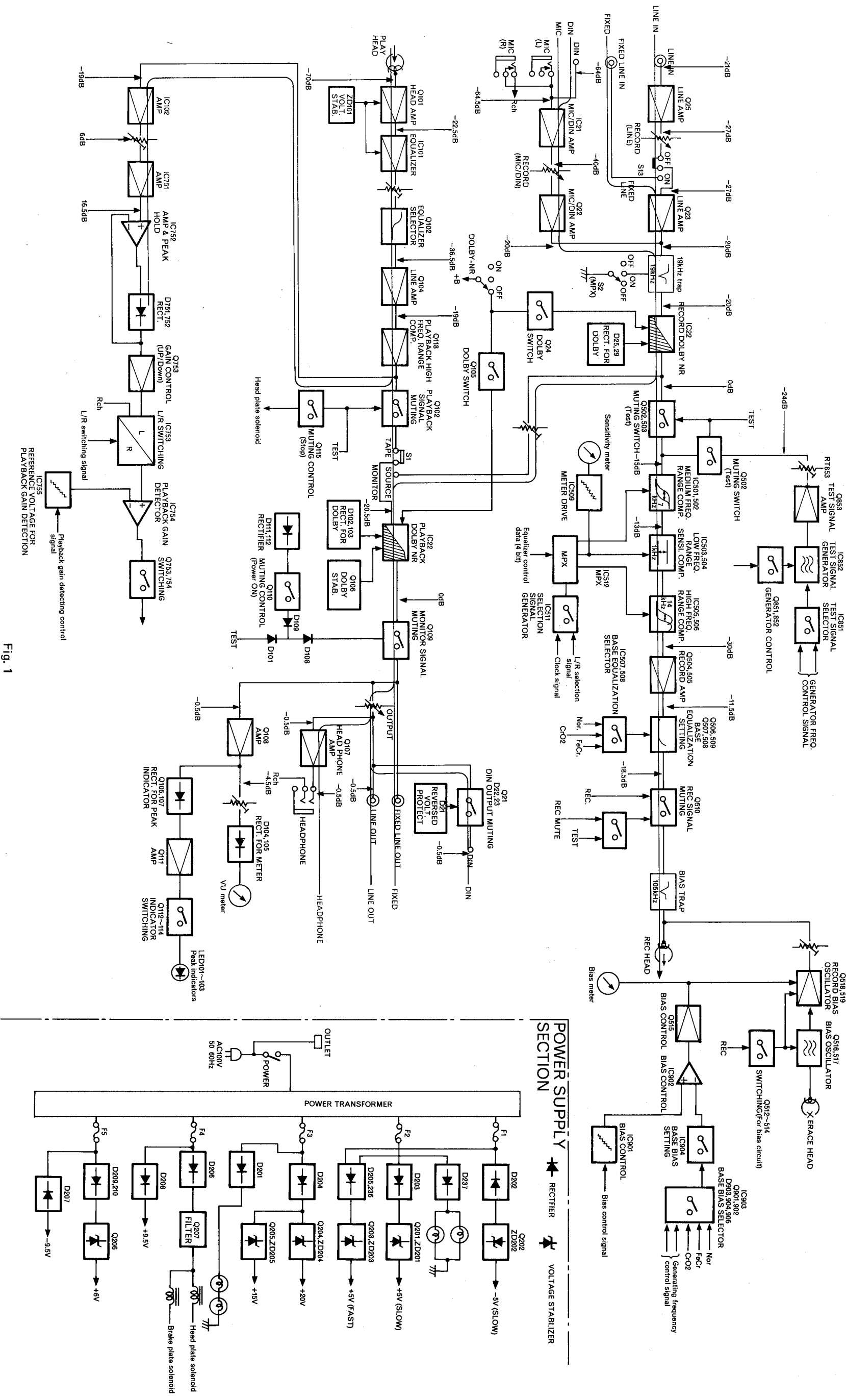


Fig. 1

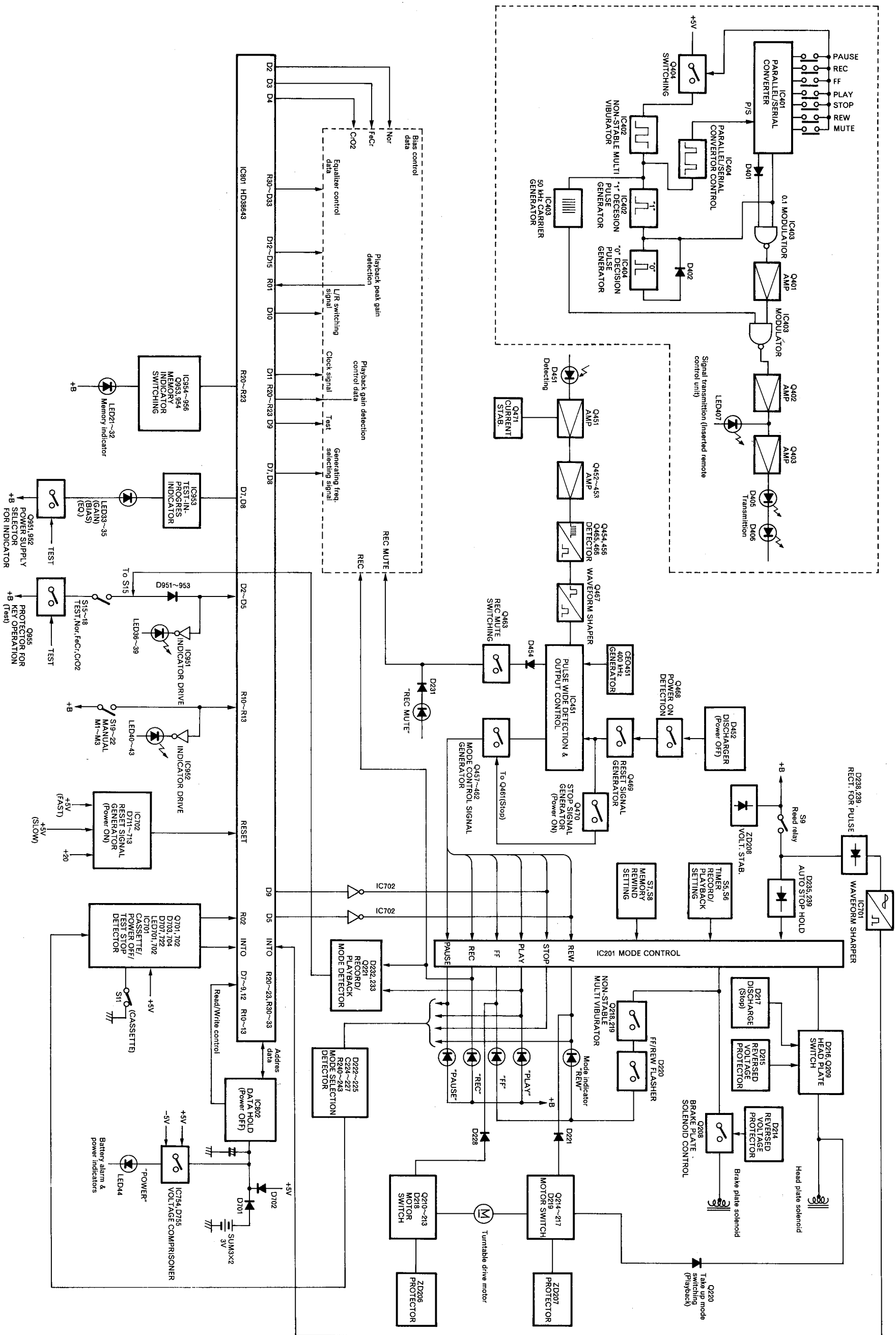


Fig. 2

TECHNICAL INFORMATION OF ATRS

1. Operation and Description of Each Mode

Deck status	Deck operation	Description	
		Description item	Page
Power-off	<p>* The status (tape/memory position) immediately before the power is turned off and data obtained by tests are moved to an external memory (IC802) which is backed-up by a battery.</p> <p>* The microcomputers in the remote control section and main control section (IC451 and IC801) are maintained in the reset state until the power supply is stable. At the same time, the stop signal is generated in the remote control section to prevent error operations at the beginning of power-on and the amplifier section is muted.</p> <p>* After the reset is released (the stop signal is removed), data is moved in from the external memory (IC802).</p>	<p>1. Preservation of power turn off time data.</p> <p>1. Initial reset at power-on. 2. Stop and reset circuits in remote control section.</p>	<p>18</p> <p>10 37</p>
Cassette Holder Open	<p>* The mechanism control section is forced into the stop mode.</p> <p>* The tape selector is switched to the NOR position after reset.</p> <p>* Only the memory indicators of memory registers containing data (M1 — M3 and TEST) light.</p>	<p>1. Cassette detection circuit 2. Stop signal generator circuit 3. Data preservation at power-off</p>	<p>11 14 18</p>
Cassette Holder Closed or Operation State	<p>* For CrO₂ tape, the CrO₂ tape position is automatically selected, and the tape selector is automatically switched to NOR for other tapes.</p> <p>* The memory position selected before power-off is selected if it contains data, or the MANUAL mode is selected; i.e., memory registers M1 — M3 are not held unless they contain data.</p> <p>* Data from the selected memory register is sent as time-shared data to the equalizer section and continuously to the bias section to control gain.</p> <p>* The voltage of the back-up battery is compared with a reference voltage. If the battery voltage is higher than or equal to the reference voltage, an indicator which functions as a power indicator is continuously lit; if the comparison finds that the voltage of the back-up battery is lower than the reference voltage, the indicator flashes to battery alarm.</p>	<p>1. Tape selector selection 2. Memory selector 3. Recording/playback circuit outline 4. Gain control circuit 5. Playback high frequency range compensation circuit 6. Data transfer circuit in recording equalizer section 7. Recording bias circuit 8. Memory indicator circuit 9. Battery alarm circuit</p>	<p>12 13 20 21 20 24 27 16 15</p>
Test State	<p>* The external signal input is cut off and the test signal from the internal oscillator is input to the recording equalizer circuits (low, medium and high frequency ranges).</p> <p>The oscillation signal is charged over for each test circuit, and recorded and played back to detect the gain in the playback gain detector circuit to obtain optimum equalization and bias values. The tests are performed in the following sequence:</p> <p>1. Sensitivity 2. Bias 3. Sensitivity 4. Medium range equalization 5. High range equalization 6. Bias 7. Sensitivity 8. Medium range equalization 9. High range equalization</p> <p>* Changing the tape selector is inhibited during the test.</p> <p>* If the mode is changed (if any button other than REC/PLAY is pushed), the test stops.</p> <p>* The length of tape transported from the beginning of the test to the completion of the high frequency range equalization test is measured.</p> <p>* If a tape is determined to be unsuitable by the test, the test is stopped and the test indicator flashes.</p> <p>* When the high frequency equalization test is completed, the REW signal is issued and the tape is rewound to the test start point.</p> <p>* After the test completion, the test data is transferred to the external memory when the test button and one of the memory buttons are pushed simultaneously.</p>	<p>1. Test stop circuit 2. Test selection 3. Test data transfer to memory 4. Stop signal generator circuit 5. Memory indicator circuit 6. Test-in-process indicator 7. Playback gain detector circuit 8. Test signal generator circuit 9. Tape length transported detector circuit</p>	<p>12 13 14 14 16 29 29 31 33</p>
Immediately after Power-off	<p>* When power-off is detected, data is transferred to the external memory.</p>	<p>1. Power-off detection 2. Data storage at power-off</p>	<p>11 18</p>

2. Initial Start Circuit when the power is switched ON

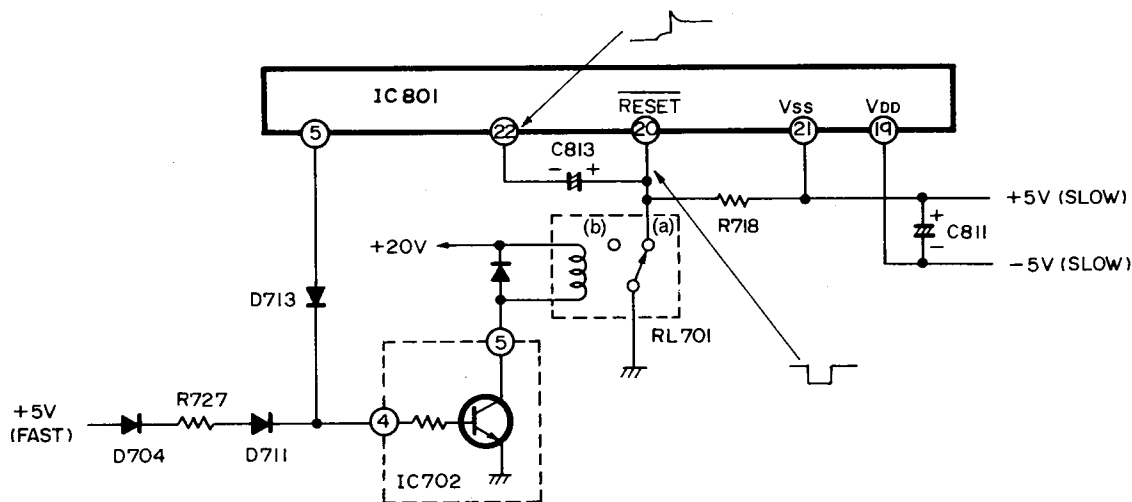


Fig. 3

1) Operation when power is switched OFF

When the power is turned on, microcomputer IC801 transfers the status immediately before power-off and other storage data from the external RAM and operates on the basis on this data. The data transfer from the external RAM is performed by the program start section of the microcomputer. To ensure that the program is started from the beginning when the power is turned on, an initial reset circuit is provided. Three powers supplies are provided by this circuit with different rise times.

- Ⓐ + 5V (FAST)
- Ⓑ + 5V (SLOW) and -5V (SLOW)
- Ⓒ + 20V

Though IC702 enters the operation state when the +5V (FAST) supply rises, contact (a) of relay (RL701) is closed since the +20V supply has not yet risen. Then, the -5V (SLOW) and +5V (SLOW) supplies rise to be fed to the microcomputer which enters the operation mode at this time. Since relay contact (a) is closed at this time, however, terminal (20) of IC801 is at low level (the microcomputer is in the reset state when this terminal is at low level), the microcomputer is reset. The subsequent rise of the +20V supply actuates the relay and contact (b) is closed to supply the high level to terminal (20) of IC801 and the reset is removed. The microcomputer checks the voltage at terminal (22) and starts operating the from biginning of program when terminal (22) is at high level.

2) Operation immediately after power-off

When the power is turned off, the relay is actuated (contact (b) is closed) to prevent resetting before the microcomputer data has been transferred to the external memory (IC802). Terminal (5) of IC801 goes to high level after detecting that power is turned off to perform data transmission to the external RAM and keep IC702 in the operating state.

3. Power-off, Cassette and Stop mode stop detection

Terminals (24) and (35) of the microcomputer (IC801) detects power-off, whether a cassette is loaded and test mode stop by changes in level as shown in Fig. 4.

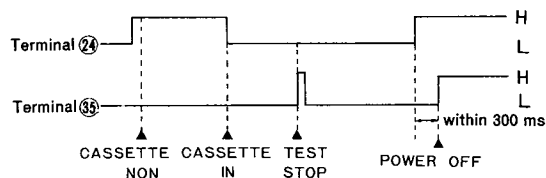


Fig. 4

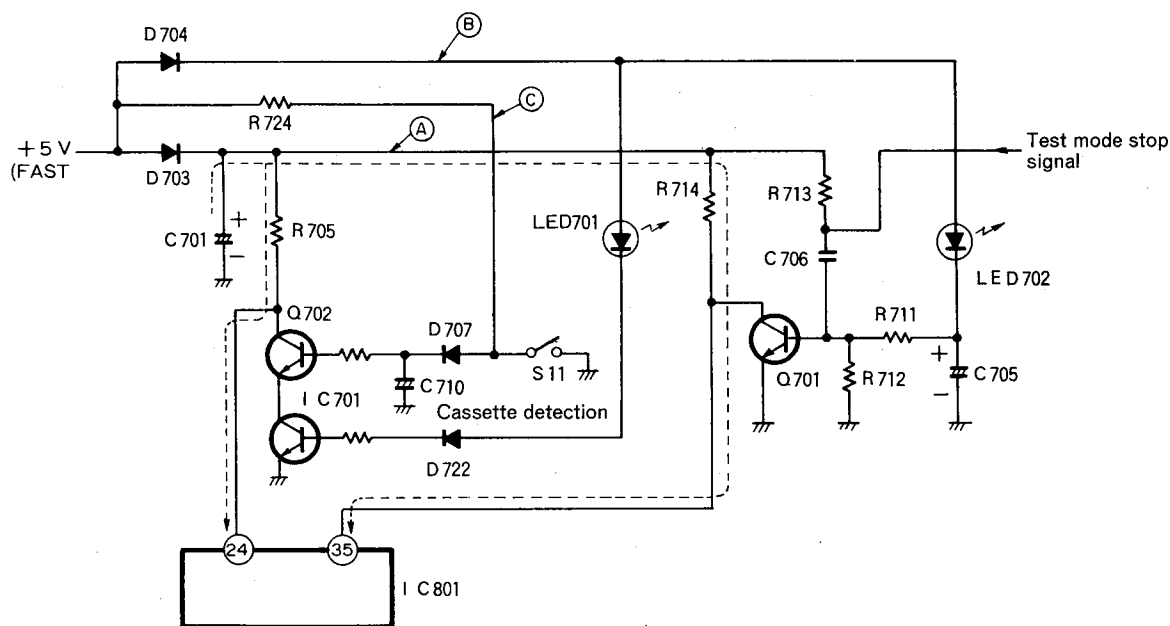


Fig. 5

1) Power-off detection

When the power is turned off, the external memory (IC802) is operated by the batteries and data stored in the internal memory of the microcomputer is transferred to the external memory and held there. When the power is turned off, this is detected immediately, and the data is transferred to the external memory before an electrolytic capacitor is discharged. The microcomputer is provided with a program that detects power-off when terminal (35) changes from low to high 300ms after terminal (24) changes from low to high. The following circuit is provided so that this program takes effect.

The +5V (FAST) supply is switched by D703 and D704 as shown in the figure and held by C701, C705 and C710. The +5V (FAST) supply is further divided into the three supplies (A), (B), and (C). Their voltages fall in the order of (B), (C) and (A) when the power is turned off according to their time constants. Since the voltages of lines (B) and (C) fall first, IC701 and Q702 are cut off and the voltage at C701 is fed to terminal (24) of IC801 through R705 to change it from low to high. Then, the discharge from C705 through R711 and R712 causes Q701 to be cut off so the voltage of C701 is fed to terminal (35) of IC801 through R714.

With high level at both terminals (24) and (35), IC801 detects power-off. In order to avoid errors due to the instantaneous disconnection of power, the level change at terminal (35) is tested later than terminal (24).

2) Cassette detection

A cassette detection function is provided to reset the tape selector when the cassette tape holder remains open for 360ms or longer, detecting a tape change (the NOR. position is selected after reset).

Opening the cassette tape holder causes S11 to be opened which in turn cuts off Q702 to feed the high level of +5V supply (A) to terminal (24) of IC801 through R705. At the same time, the mechanism section is forced into the stop mode until the cassette tape holder is closed.

3) Test mode stop detection

Changing the mode during testing causes operation of the mechanism to be stopped and the test mode stop instruction to be executed by the microcomputer.

If the mode is changed (if any operation button is pushed) during testing, the output terminal of IC201 corresponding to the operation button pushed becomes low. If the FF operation button is pushed, terminal (20) of IC201 becomes low and a charging current flows to C227 through R713 and D225 until C227 is fully charged. At this time, C706 is discharged through C227, and the voltage change at the junction of R713 and C225 is fed to the base of Q701 through C706, cutting Q701 off which generates a positive pulse at terminal (35) of IC801. The microcomputer detects this pulse and stops the test.

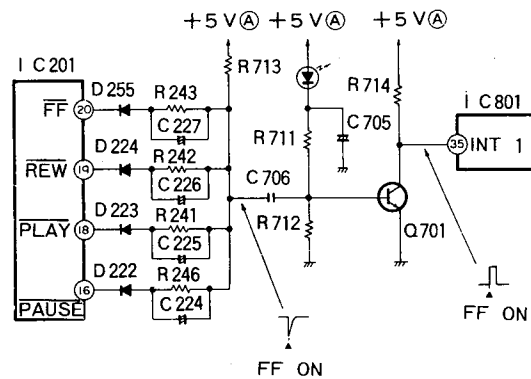


Fig. 6

4. Tape selector/Memory selection

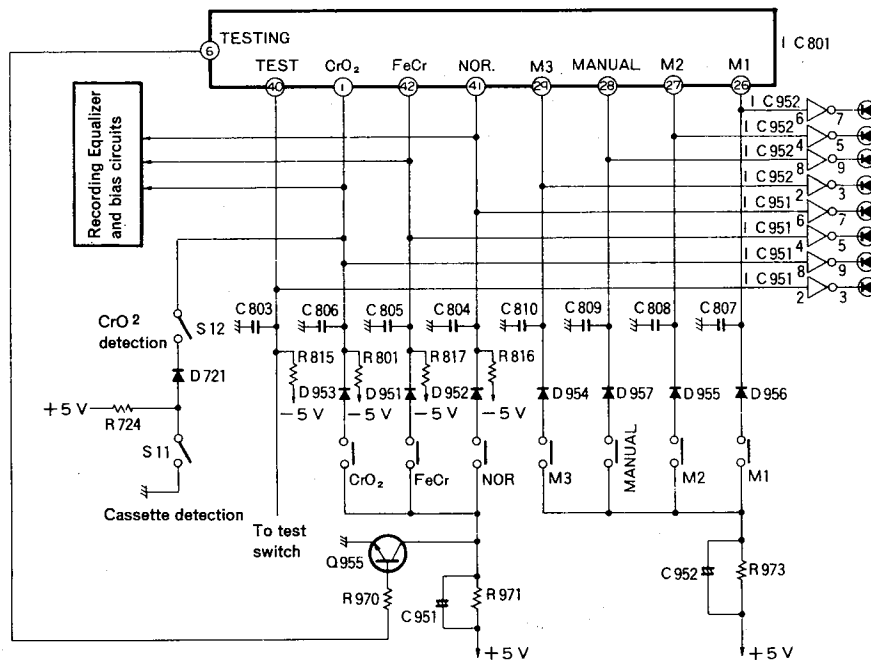


Fig. 7

1) Tape selector selection

Pushing a desired tape selector button causes high level to be applied to the microcomputer terminal associated with the button. The microcomputer detects this high level and, after checking that no other tape selector button has been pushed, holds the terminal at the high level. This high level signal is used to control the electronic switches in the recording equalizer circuit, recording bias circuit and the playback equalizer circuit and these circuits supply data giving the basic operation characteristics in accordance with the tape selected by the selector button. The high level signal also lights the associated tape indicator.

When a CrO₂ tape is used, it is detected whether the CrO₂ detection tabs are present or not on the cassette half and the CrO₂ position is automatically selected. For other tapes, however, the NORMAL position most frequently used is selected by a microcomputer program in the clear state since the automatic detection other types of tape impossible.

If the power is turned off without the cassette tape holder being opened, the selector position immediately before the power is turned off is preserved.

Tape selection is inhibited during testing. Since Q955 is on

during testing, the high level tape selector switch signal is removed.

2) Memory Selection

When one of the compensation data selection button switches M1 through M3, and MANUAL is pushed, the high level is applied to the microcomputer terminal associated with the switch pushed. The microcomputer detects this signal and, after checking that the external memory contains data corresponding to this terminal, holds the terminal at the high level. With this high level signal at the terminal, the associated memory indicator is lighted, and at the same time, the contents of the selected memory are sent out with time-sharing to the recording equalizer section and continuously to the recording bias section.

6. Test Data Transfer to Memory

The data obtained from the test is transferred to the external memory when the TEST button and desired memory button (M1 — M3) are pushed simultaneously. Q221 returns to the on state when the test is completed to remove the high level signal supplied to the test switch and the voltage across C239 which was charged when the test started is applied instead.

If the desired memory button and TEST button are pushed

simultaneously, since terminal (40) of the microcomputer was set to the high level when the test was completed, the microcomputer resets terminal (40) to the low level and then checks the level of this terminal again. If the high level is detected at this terminal after the reset, the microcomputer determines that the TEST button is pushed, and transfers the data to the selected memory.

5. Test Mode Selection

In order to prevent any test operation due to an erroneous operation, the selected test is started when the unit enters the tape transport mode after the recording mode is held in the test mode. The test indicator lights from when a test is started until the test data is stored in the memory or until data already stored by a previous test is selected. If playback gain cannot be determined by the sensitivity test or medium frequency range test because an unsuitable tape or the leader tape section is tested, the test is stopped and the test indicator flashes.

The record/playback mode is detected by the following circuit in this unit: The PLAY and REC outputs of IC201

control Q221 through an OR circuit composed of D233 and D232.

Q221 is cut off when both the record and playback mode signals are correct, and it is on in the other modes. If the test switch is set ON in the record/playback mode, a high level signal is applied to terminal (40) of the microcomputer. At this time, the microcomputer holds terminal (40) at the high level and starts the test after checking that the unit is not in the record/playback pause mode by examining the record and playback signals at terminals (22) and (23).

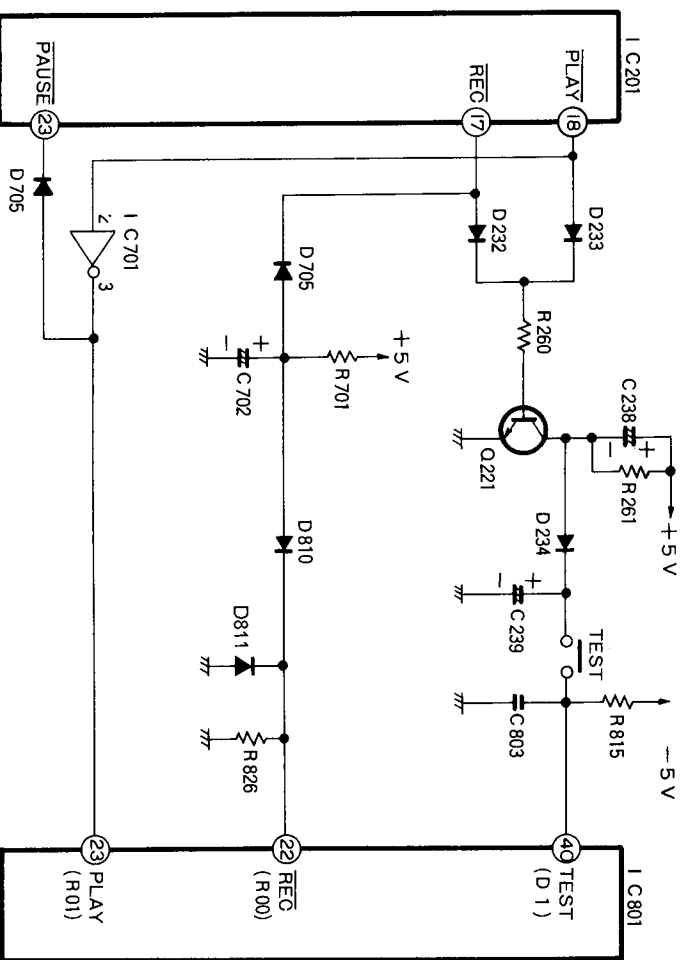


Fig. 8

7. Stop Signal Generator Circuit

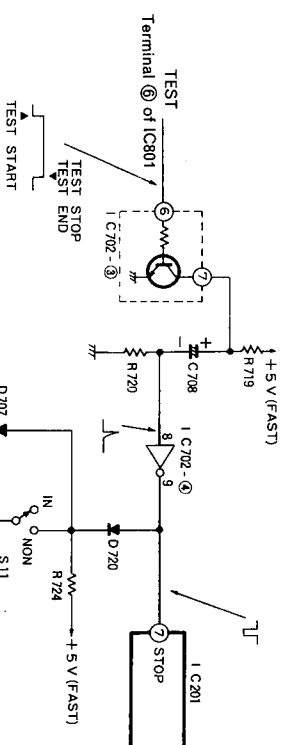


Fig. 9

The stop signal is automatically generated in the following conditions:

- (1) When a test terminates and the tape is rewound to the test start point.
- (2) When no playback signal is detected because an unsuitable tape or leader tape section is tested.
- (3) When the cassette holder is open.

When the power is turned on, a voltage drop is produced across R720 until C708 is fully charged by the rise of the +5V (FAST) supply. The waveform of this voltage is shaped and inverted by IC702 to be applied to the stop input terminal of the mode control IC(IC201). A pulse is thus generated by this circuit when power is turned on, and another stop pulse with a larger width is generated in the remote control section. The output at terminal (8) of IC702 is held at the high level by the test mode signal (terminal (6) of IC801) during testing; until the test terminates, or is stopped because the tested tape is unsuitable or a mode change is performed. The stop signal is also generated when terminal (8) of IC702 becomes low by discharging C708 immediately after IC702 (terminal (8) becomes on by the same operation as when power is turned on.

When the cassette holder is open, or it is opened while the mechanism is in action (during the FF, REW or PAUSE operation), the connection of the

cassette detection switch (S11) as shown in Fig. 9 switches to NON and the stop signal is generated until the cassette holder is closed. The cassette detector circuit is provided to detect tape replacement until the elapse of a predetermined time after the cassette holder is opened (see the explanation on the cassette detector circuit).

8. Battery Alarm Circuit

The status immediately before power is turned off and test data are transferred to the external RAM (IC802) which is put in the operating state by the batteries at this time to preserve the data. A battery alarm circuit is provided to check if the output voltage of the battery is below a pre-determined value when power is turned on. A blocking oscillator circuit is formed by IC754 and the peripheral circuits as shown in Fig. 10. The voltage at terminal (5) of IC754 is set at approx. 2.5V divided by R778 and R777. This reference voltage and the output voltage of the batteries are compared. The output of IC754 is negative when the voltage at terminal (6) (V1) is higher than the reference voltage (V2), and positive when V1 is lower than V2. Since the output of IC754 becomes negative when the battery voltage rises over the reference voltage, the LED lights and functions as the power indicator. Since the output of IC754 becomes positive when the battery voltage drops below the reference voltage, the LED goes out and capacitors C762 and C763 are charged. When the voltage at the positive terminal of C763 rises to the reference voltage (V2), the IC output reverses and the LED comes on and capacitors C762 and C763 are discharged. The LED flashes as this action is repeated.

9. IC HD7414P

HD7414P is a BCD to decimal decoder IC which is used to obtain a decimal output from 4-digit binary data (BCD). The output corresponding decimal values 0 to 9 is 0, or low. BCD code input A is the least significant bit (LSB) and input D is the most significant bit (MSB). The input and output codes are shown in the following table:

Input				Output									
D (MSB)	C	B	A (LSB)	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	Y ₈	Y ₉
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	1	0
1	0	0	1	1	1	1	1	1	1	1	1	1	0

Table 1

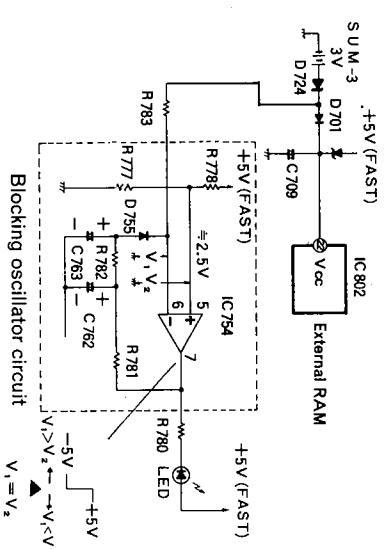


Fig. 10

10. Memory Indicator Circuit

The microcomputer can store and maintain a maximum of four sets of test data in memories M1 to M3 and TEST for up the three tape selector positions. The test data is transferred to a intended memory by simultaneously pushing the desired memory button and TEST button. If data is already contained in the selected memory, the old data is replaced by the new data. Twelve (12) LEDs are arranged in a matrix form as shown in Fig. 11 as external displays for the contents of the four memories M1 to M3 and TEST.

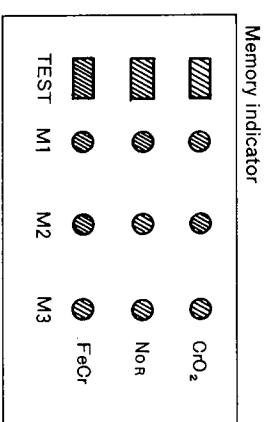


Fig. 11

The contents of a memory register within the microcomputer are checked by fine-sharing, output and held by latch capacitors C953 to C962. During testing a microcomputer program displays the contents of the external memory and flashes LEDs not in use to indicate that a test is in progress. LEDs are controlled by four (4)-bit control signals from the microcomputer. To encode information bits 0 to 12 into the 4-bit control signals, a BCD (binary) to decimal decoder circuit is provided between the microcomputer (IC801) and the twelve LEDs. Fig. 12 shows the memory indicator circuit. The 4-bit signals at terminals (30) to (33) of IC801 are inverted by IC956 and fed to the BCD to decimal decoder IC(IC954). Since the decimal outputs from IC954 are "0000" to "1001", i.e., decimal 0 to 9, inverters Q953 and Q954, and a dual 4 input NAND gate are added to form a logic circuit that decodes input data "1010" and "1011". Table 2 shows the data code used to light the LEDs. The 4-bit memory indicator control signals are used in common with the test time playback gain detection D/A converter control signals. Thus, each time the bias value is varied by one step, the control data used to detect the playback gain changes from "0000" until the peak value is obtained. Unused LEDs flash each time the bias value varies by one step. As the control data value gets close to the peak bias point more, LEDs flash since the variations of the control data increases.

31	27	28	29
30	21	22	23
32	24	25	26

Numbers show symbol No. of LEDs. (Refer to table 2)

Fig. 12

Microcomputer Output				IC954 Input				IC954 Output									IC955-②				IC955-①				Refer to Fig. 12				
R ₂₃	R ₂₂	R ₂₁	R ₂₀	D	C	B	A	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	Y ₈	Y ₉	D	\bar{C}	\bar{B}	\bar{A}	O	D	\bar{C}	\bar{B}	A	O'	LED lit	
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	1	1	0	1	1	1	—
0	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	—
0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	0	0	1	1	—
0	0	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0	0	1	—
0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	LED29
0	1	0	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	0	1	1	LED28
0	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	1	1	1	0	1	1	LED27
0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0	1	1	LED31
1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	0	1	1	0	0	1	1	1	LED26
1	0	0	1	0	1	1	0	1	1	1	1	1	1	0	1	1	1	0	0	1	1	1	1	0	0	1	0	1	LED25
1	0	1	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	0	0	0	0	1	1	0	0	0	1	1	LED24
1	0	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1	0	0	0	1	1	1	0	0	0	0	1	LED32
1	1	0	0	0	0	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	0	1	1	0	1	1	1	1	LED23
1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1	1	0	1	LED22
1	1	1	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	0	1	0	0	1	1	0	1	0	1	1	LED21
1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	0	1	1	1	0	1	0	0	1	LED30

Table 2

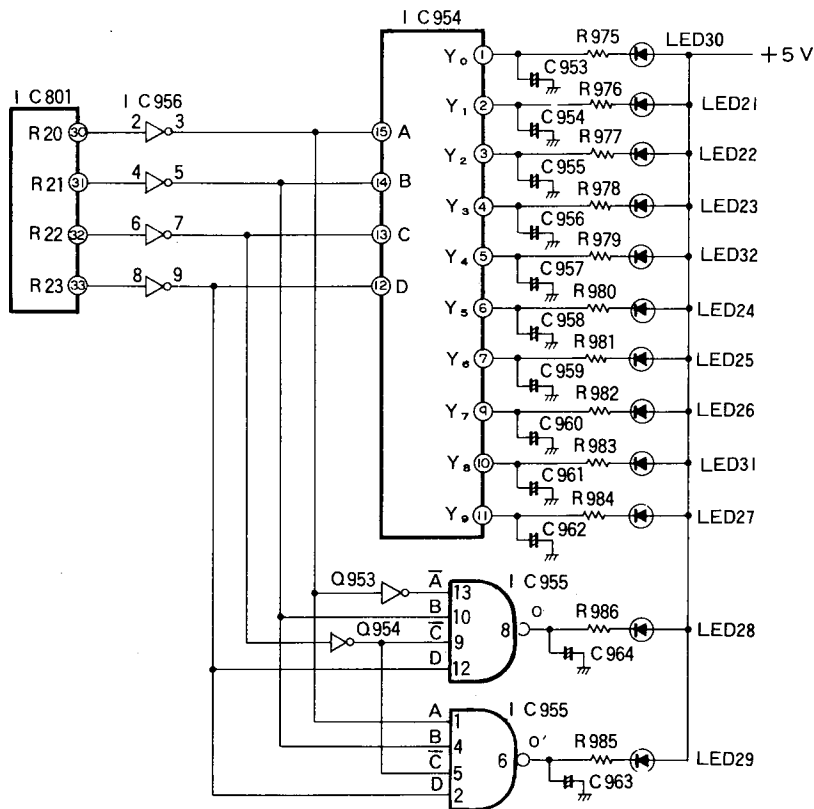


Fig. 13

11. Data Storage when power is turned off

This unit is provided with a function that, when the power is turned off the test data is preserved and the existing status (tape selector and compensation data memory positions) is held. (tape selector and compensation data memory positions are not preserved when the power is turned off with the cassette tape holder opened.)

The memory in which data is stored, the data stored in which can be changed and read out is called a RAM (random access memory), and test data in this deck is stored in a RAM. The RAM's contents are preserved as long as the power is supplied. Since the power supply of the microcomputer is removed when the power is turned off, an exclusive RAM is provided outside microcomputer, and immediately after power-off is detected, data is transferred to the RAM whose power supply is maintained by the back-up batteries.

The microcomputer transfers the data to the external memory by execution of a data transfer instruction in which X and Y addresses are selected and the microcomputer is synchronized with the memory as data becomes ready to be transferred.

Static RAM HM435101 (256 words x 4-bits) with low power consumption and a maximum stand-by current of 15 A is used for the external memory (IC802).

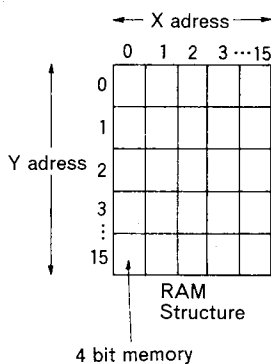


Fig. 14

Since both X and Y addresses run from 0 to 15, 8-bit address lines (4 bits x 2) are required, and since 4-bit data is stored in each address, four data lines are required. Further, 3-bit control lines are necessary as the signal lines between the microcomputer and RAM in addition to the address and data lines so there is a total 15 signal lines. In order to reduce the number of microcomputer terminals needed, the terminals that are used to control the recording equalizer circuit are used as the external RAM control terminals once power-off is detected.

Fig.16 shows the circuit between the microcomputer and the external RAM.

Lines $A_0 - A_7$ of the external RAM (IC802) are the address lines selected by the microcomputer. $DI_1 - DI_4$ and $DO_1 - DO_4$ are the RAM's data input and output lines respectively. The lines for the same bits are connected and used as common input/output lines. The data input/output lines are switched between input and output by control signal OD. When OD is low, the RAM is in the input mode and, when OD is high, the RAM is in the output mode. Control signal R/W controls the data transfer timing between the microcomputer and the RAM. When R/W is high, the microcomputer sends out selected data along the data lines and, when it is low, the external RAM stores the data on the data lines into the address selected by the microcomputer. Control signal CE allows the data on the data lines to be input to the microcomputer and data to be output along the data lines from the microcomputer. In addition, CE is used to synchronize data transfer between the microcomputer and the external RAM. When no data is being read or written, or when data is stored, this signal is held at the low level. This signal is also used to prevent the initial reset signal generation circuit from operating until data transfer terminates (see the explanation of the power-off time initial reset circuit).

When power is turned on, the data transferred to the external RAM when the power was turned off previously is moved into the microcomputer. This data transfer operation takes place when the reset signal is removed from the microcomputer and terminal (22) of IC801 becomes high. See the timing diagram as shown in Fig. 15.

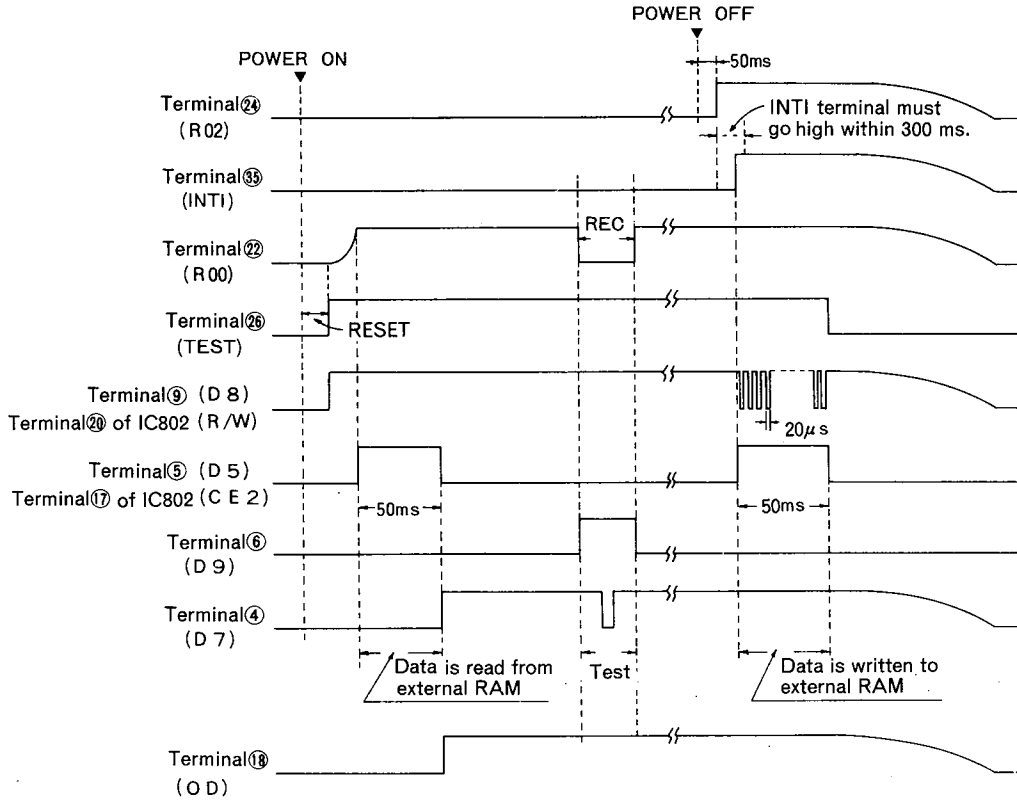


Fig. 15

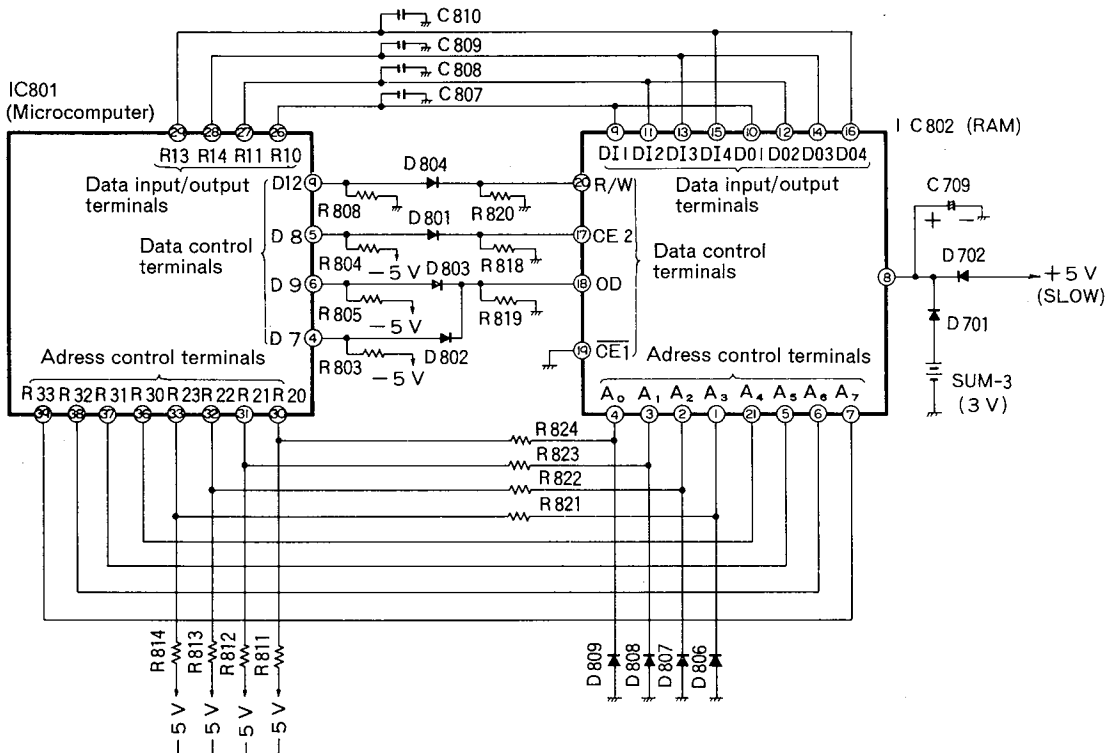


Fig. 16

12. Recording/Playback Circuit Block Diagram

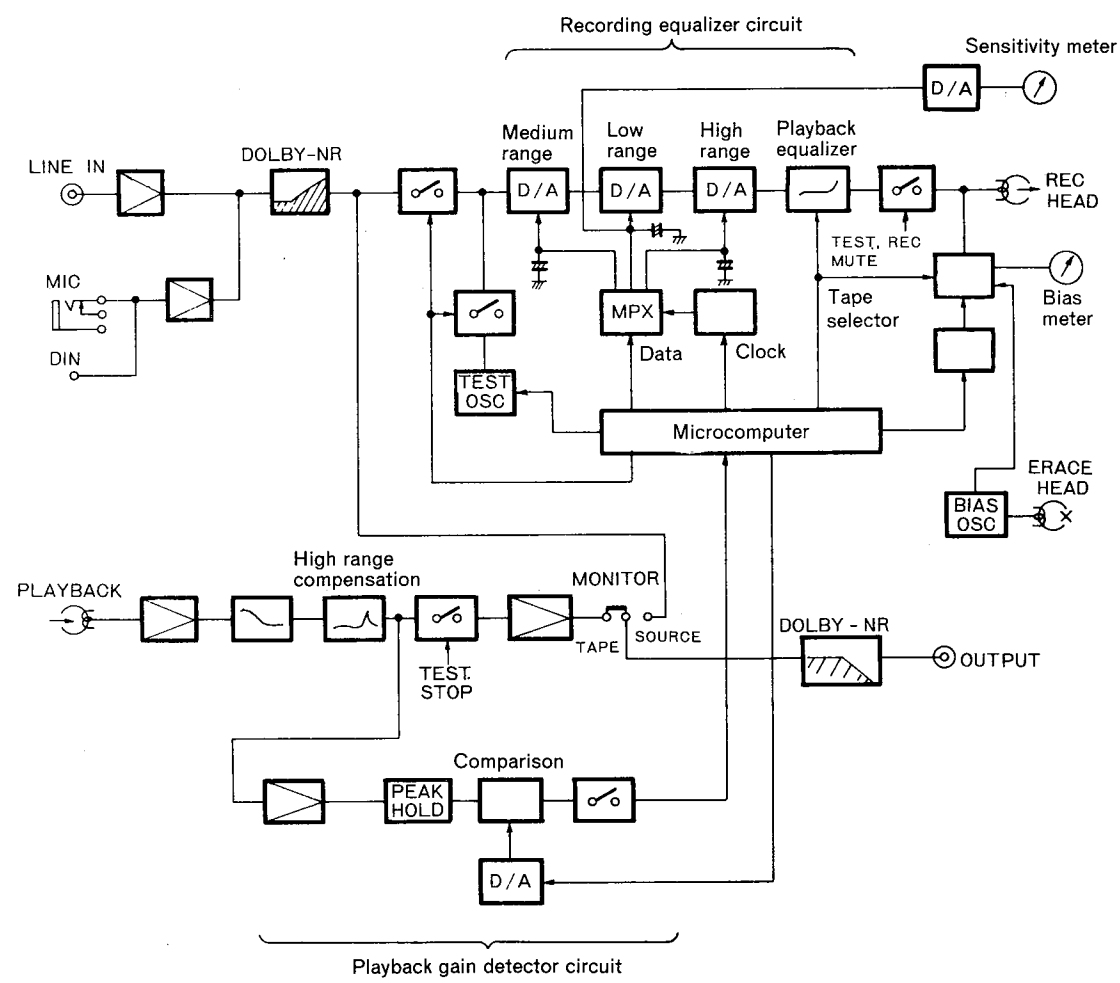


Fig. 17

13. Playback High Frequency Range Compensation Circuit

This is newly developed circuit used in the D-5500; it compensates for variations in high frequency range due to loss at the playback head because of a non-uniform gap. Principle of Operation

Amplification gain of Q104 (K1) is given by:

$$K_1 \doteq \frac{R171+R172}{R116}$$

and amplification gain of Q116 (K2) is given by

$$K_2 \doteq \frac{R172}{Z_E}$$

where $Z_E = R169 // (Z_C + Z_L)$

$$\begin{cases} Z_C = -j \frac{1}{\omega C_{150}} \\ Z_L = j \omega L_{102} \end{cases}$$

These two amplification gains are added across R172 as shown below assuming the attenuation due to RT102 to be k:

$$K = K_1 + k \cdot K_2 = \frac{R171+R172}{R116} + k \cdot \frac{R172}{Z_E}$$

Thus, the peaking effect in the high frequency range varies as K is changed.

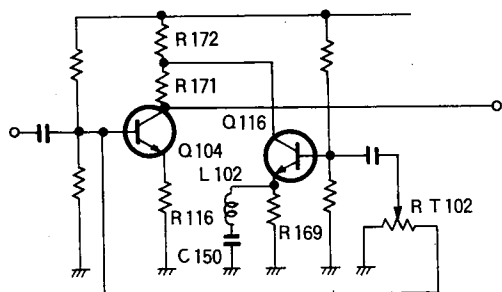


Fig. 18

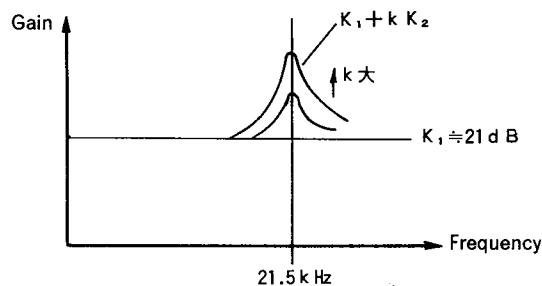


Fig. 19

14. Gain Control Circuit

The gain of the following circuits is controlled by the microcomputer:

1. Low frequency range sensitivity compensation circuit
2. Medium frequency range compensation circuit
3. High frequency range compensation circuit
4. Recording bias fine adjustment circuit
5. Recording sensitivity meter control circuit
6. Playback gain detector circuit

Data input to or output from the microcomputer is processed as "Hi" and "Lo" binary values, and sizes and values are represented by several binary digits. The voltage and gain, etc. of an amplifier circuit or other analog circuit cannot be directly controlled by these digital values. That is, voltage and gain, etc. must be controlled after the data is converted to a form "understandable" by the respective circuits.

Conversion is done by circuits called digital/analog converters (D/A converter).

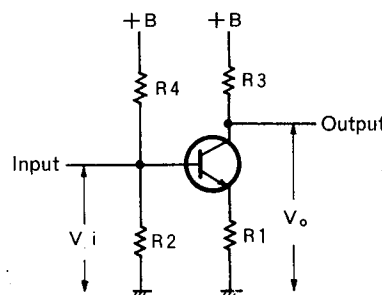


Fig. 20

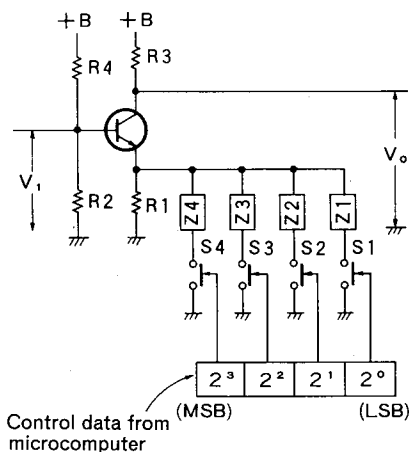


Fig. 21

1) Principle of D/A converter (4-bit control signals)

An increase of the emitter resistor (R1) in the circuit on the left causes a reduction in gain since the voltage drop across R1 has reverse phase to the input voltage. To apply this principle, impedances Z1 – Z4 are connected in parallel with R1 and Z1 – Z4 are grounded through switches S1 – S4 respectively which are closed by control data from microcomputer as follows:

$Z4 : Z3 : Z2 : Z1 = 1 : 2 : 4 : 8.$

S1 is closed when bit 2^0 is 1.

S2 is closed when bit 2^1 is 1.

S3 is closed when bit 2^2 is 1.

S4 is closed when bit 2^3 is 1.

A bit is the minimum increment in which data can be represented and four binary digits are output. The bit representing the least significant binary digit is called "LSB" and the bit representing the most significant binary digit is called "MSB".

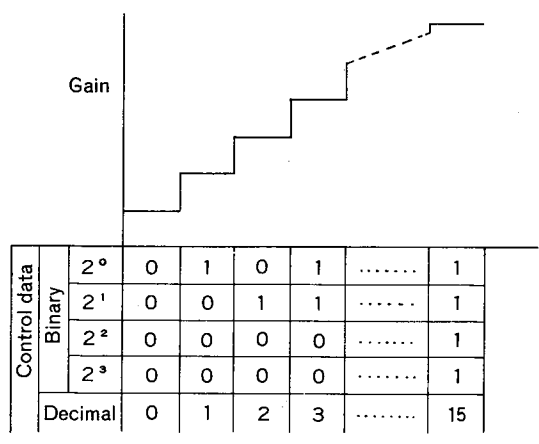


Fig. 22

If a 4-bit binary number is increased step by step from "0000" to "1111" (equivalent to decimal "0" to "15") following the above relationship and the input is constant, the gain increases in 16 steps as shown in Fig. 22. As indicated in the figure, the minimum gain is determined by R₁ and the variation rate per step is determined by Z₄. Further, by making impedances Z₁ - Z₄ with pure resistance (R), capacitance (C) and inductance (L), and varying the control data, the gains in specific frequency ranges can be changed.

2) When Z₁ - Z₄ has pure resistance (R)

If the input voltage is constant throughout the frequency range, the output voltage is constant regardless of frequency because the output voltage is divided by pure resistance.

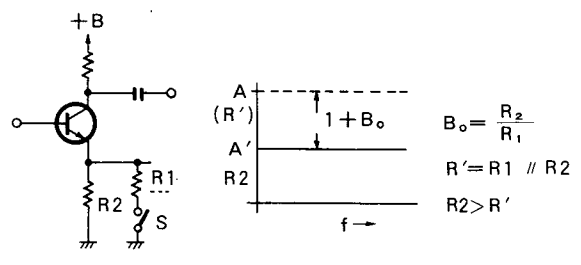


Fig. 23

3) When Z₁ - Z₄ are composed of pure resistance (R) and capacitance

Since capacitance (C) is provided in parallel with resistance (R₂), the gain is flat until f₁ at which the composite impedance of R₂ and C is equal to R₁, or above it, the output is doubled as the frequency is doubled; i.e., the output increases at a rate of 6 dB per octave, since X_C is inversely proportional to frequency. If C is changed, point f₁ varies for the reason explained above.

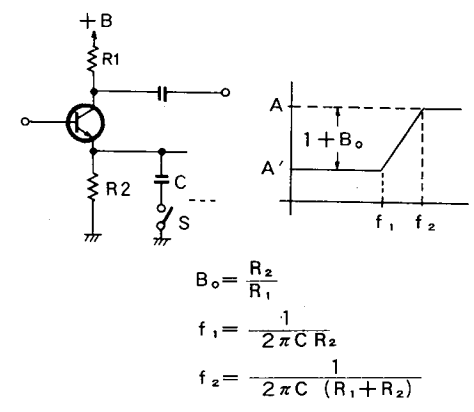


Fig. 24

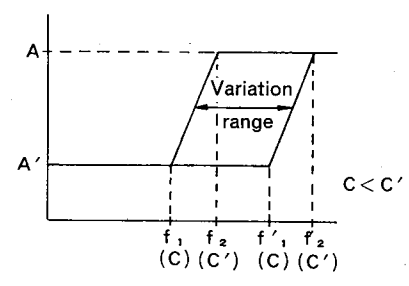


Fig. 25

4) When Z₁ - Z₂ are composed of resistance (R), capacitance (C) and inductance (L)

Insertion of a serial resonance circuit composed of L and C in parallel with resistance (R₂) causes a steep rise in gain at resonance frequency (f₁). If C is changed further, the tuned frequency (f₁) varies.

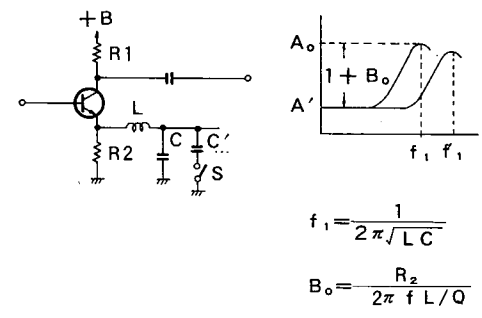


Fig. 26

D/A converter consisting of resistors are used in the low frequency range sensitivity compensation circuit, recording bias fine adjustment circuit, and playback gain detector circuit; a D/A converter consisting of capacitors is used for the medium frequency range compensation circuit; and a D/A converter circuit consisting of resistors, capacitors and coils is used for the high frequency range compensation circuit.

5) Low frequency range sensitivity compensation circuit

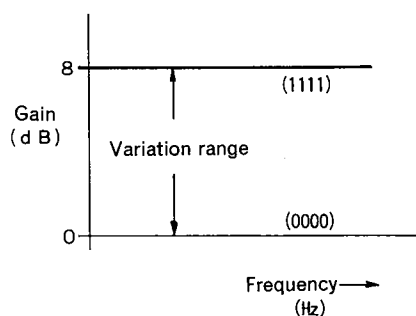


Fig. 27

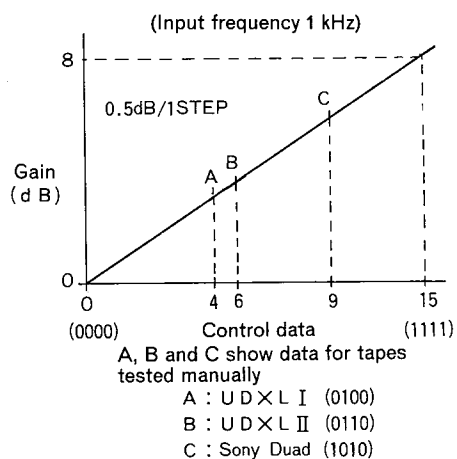


Fig. 28

6) Medium frequency range compensation circuit

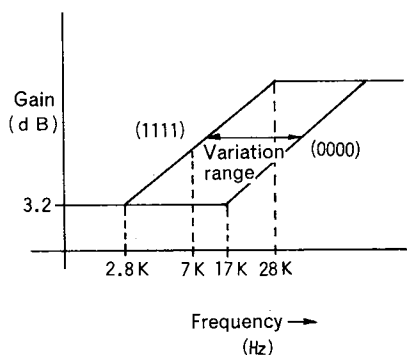


Fig. 29

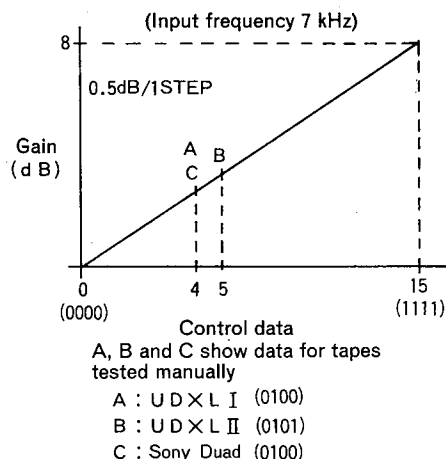


Fig. 30

7) High frequency range compensation circuit

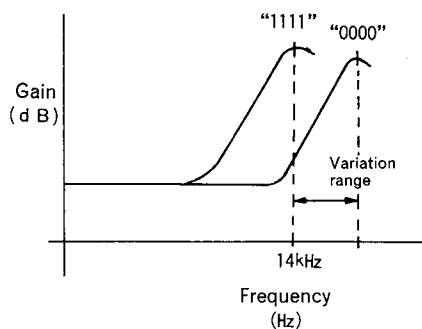


Fig. 31

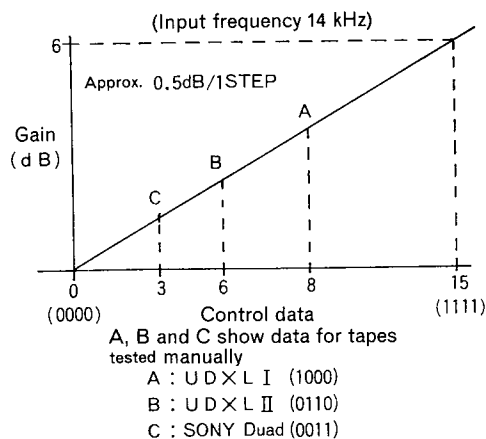


Fig. 32

15. Data Transfer Circuit in Recording Equalizer Section

Each of the low, medium and high frequency range recording equalizer sections is controlled by 4-bit binary data, and a total of 24 bits of control data is required for these sections since there are six equalizer circuits including both the L and R channels. These control data signals are controlled by the microcomputer. To lessen the number of input/output terminals of the microcomputer used, each group of 4-bit control signals and 2-bit switching signals are output from the microcomputer using time sharing using a

6-channel multiplexer (IC512). Fig. 33 shows the data control circuits. The recording equalizer control signals at terminals (36) – (39) of the microcomputer are output in the time sharing made in synchronization with the switching signals at terminals (7) and (8), and applied to input terminals (15) – (18) of IC512. From there, they are distributed to each recording equalizer circuit by a switching signals produced by IC511.

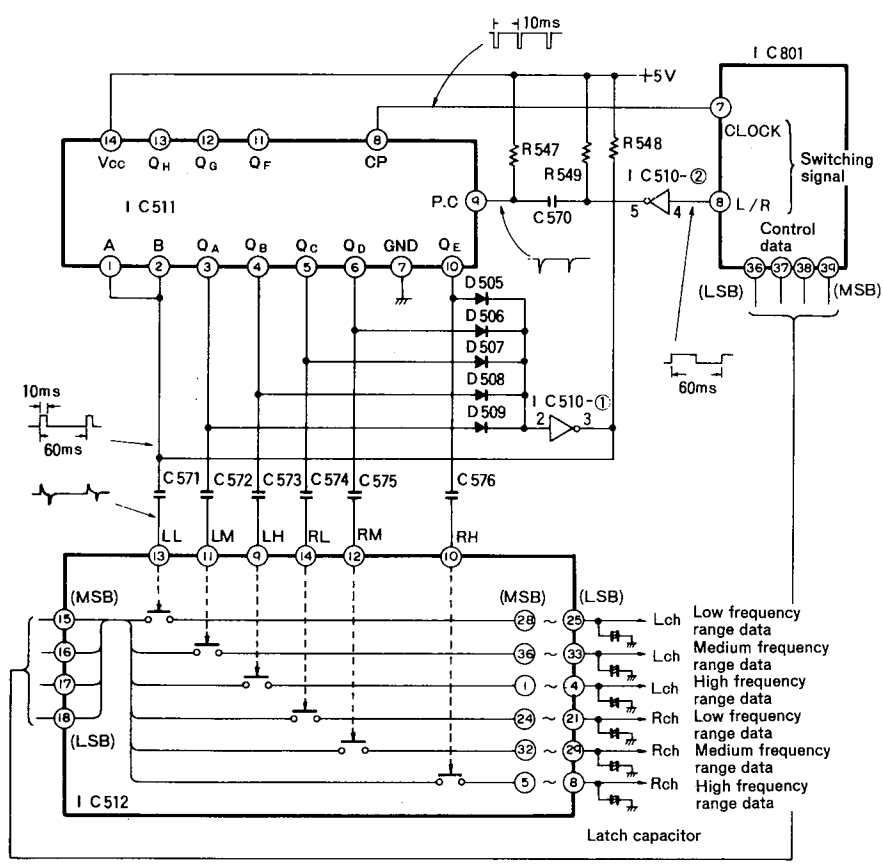


Fig. 33

Contents of control data in manual FeCr tape position

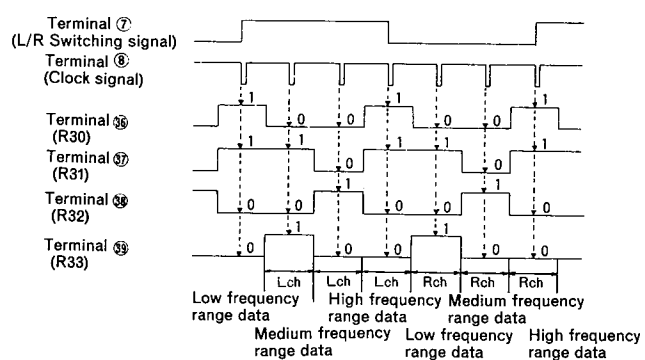


Fig. 34

1) Shift register (IC511)

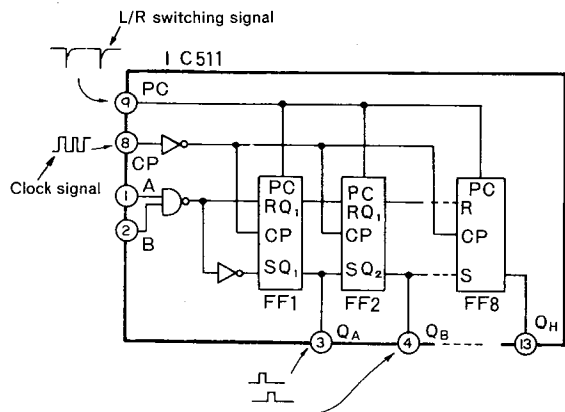


Fig. 35

IC511 is a shift register that converts serial input signals arriving bit serially to bit parallel signals.

The internal circuit of IC511 is composed of eight (8) RS flip-flop as shown in Fig. 35. When either input A or B is Lo, output Q_A of the first flip-flop does not go Hi if the clock pulse at terminal CP repeats a Hi/Lo transition. When the CP input changes from Lo to Hi with both inputs A and B at the Hi level, output Q_A is set Hi. When the CP input next changes from Lo to Hi, the second flip-flop is set Hi by the same principle, and the subsequent flip-flop operate in sequence as the CP input changes from Lo to Hi.

To reset these flip-flop, the PC terminal is set Lo.

The clock signal as shown in Fig. 35 is applied to terminal (8) of IC511, and the L/R switching signal is applied to terminal (9). The L/R switching signal output from the microcomputer is fed to IC511 through an inverter (IC510) and differential circuit (R547 and C570), and the internal flip-flop are reset by the rising edge of this pulse. Terminals (1) and (2) are input terminals used to control generation of the first output pulse (L ch low frequency range control data switching signal).

Terminals (1) and (2) are connected, and the output of an inverter (IC510) to which flip-flop outputs $Q_A - Q_E$ are fed to these terminals through OR diodes (D505 - D509). Thus, if any flip-flop output is Hi, the first pulse is prevented since terminals (1) and (2) are held at Lo.

2) Multiplexer (IC512)

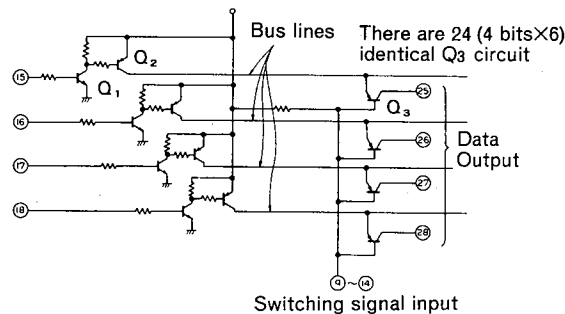


Fig. 36

The internal circuit of this multiplexer is shown above (Fig. 36). The control data signals from the microcomputer are applied to terminals (15) - (18). When a control data bit (e.g., terminal (15) is 1, Q_1 and Q_2 conduct, and data signal 1 is output on the bus line. When a negative trigger pulse is input to one of terminals (9) - (14) (e.g., terminal (9), Q_3 conducts and the control data signal is sent to the circuit associated with terminal (9). This signal is further maintained by a latch capacitor.

3) Operation of data transfer circuit

The output terminals of all the internal flip-flops in IC511 are Lo in the initial state since they are reset by the rising edge of the L/R switching signal. Since all the flip-flop outputs are Lo, the output at terminal (1) of IC510 is Hi and terminals (1) and (2) of IC511 are Hi. The rising edge of the clock signal at terminal 8 sets the first flip-flop to 1 and output terminal (3) becomes H. This output goes through D509, is inverted by IC510 and produces the Lo level at terminals (1) and (2). Thus, a Hi pulse is generated at terminals (1) and (2) of IC511 from the rise of the L/R switching signal to the rise of the clock signal. This pulse is fed to terminal (13) of the multiplexer (IC512) through capacitor C571. At this time, the L ch low frequency range control data is input to terminals (15) - (18) of IC512 so that the data from output terminals (25) - (28) is transferred when the pulse falls. This data is maintained by latch capacitors to control the low frequency range compensation circuit. The subsequent operations are performed by the switching pulses generated by the identical principle to allow the proper control data routings. The control data is transferred in the following sequence:

1. L ch low frequency range compensation circuit
2. L ch medium frequency range compensation circuit
3. L ch high frequency range compensation circuit
4. R ch low frequency range compensation circuit
5. R ch medium frequency range compensation circuit
6. R ch high frequency range compensation circuit

When the data transfer to all the above circuit is completed, the flip-flops are reset by the rising edge of the L/R switching signal, and the same operation is repeated. The recording equalizer control data is output from the

microcomputer 5 ms before the fall of the clock (at which time data is read by each circuit), so that the data is stored at its middle to prevent data for another circuit from being read by mistake.

4) Switching signal generation timing diagram

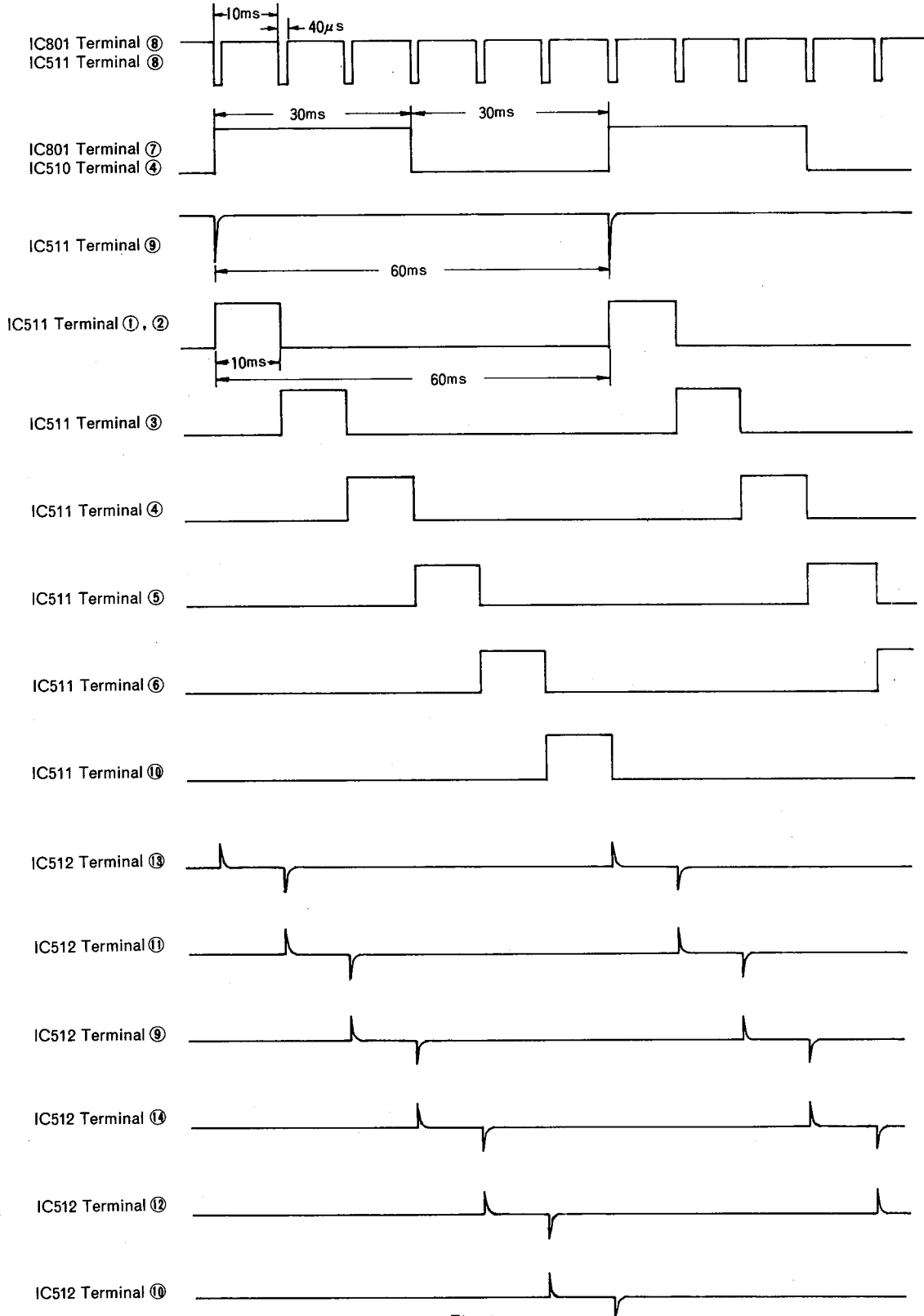


Fig. 37

16. Bias Oscillator Circuit

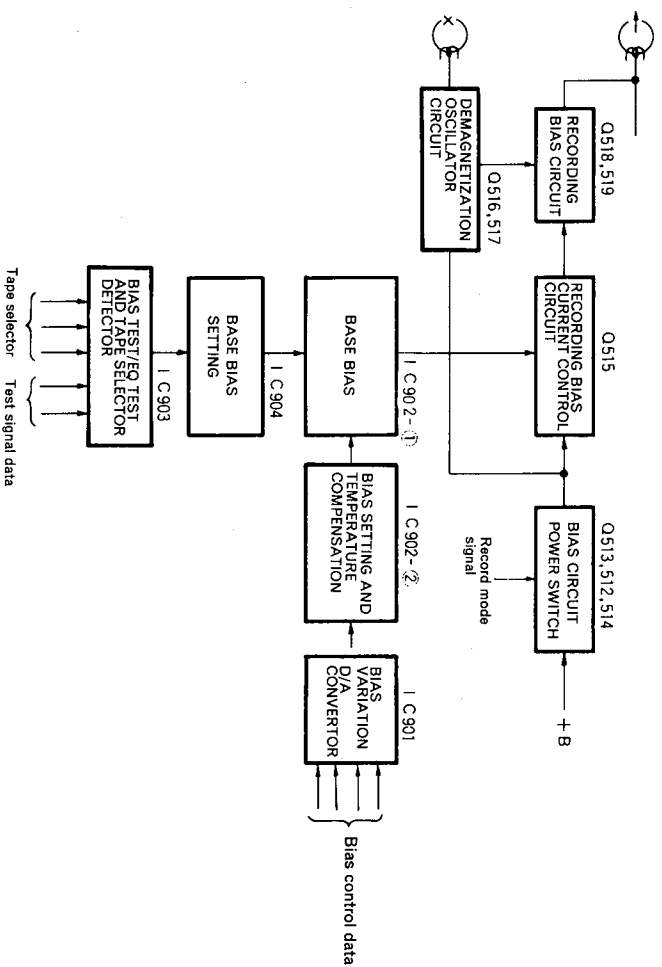


Fig. 38

1) Oscillator circuit

This is the demagnetization oscillator circuit composed of Q516 and Q517 which oscillates by feedback from the collectors of the two transistors to the base of the other transistors so as to repeat mutual ON/OFF switching. The output of the demagnetization oscillator is fed to the base of transistor Q518 (or Q519) making up the recording bias circuit in combination with Q519 (or Q518) so that it oscillates in synchronization with the demagnetization oscillator circuit so that the two oscillator circuits causes no beats. Because the recording bias circuit is isolated from the demagnetization circuit, the latter is not affected by variation in recording bias; so that it has sufficient demagnetizing efficiency.

C569 in the demagnetization oscillator is used to ensure that the circuit starts oscillation. The series resonance circuit composed of L505 and C560 in the recording bias circuit suppresses distortion of the bias current.

2) Variable recording bias circuit and temperature compensation circuit

In the variable recording bias circuit, a 16 step stair wave voltage is generated by adding the 4-bit bias control data output from the microcomputer which controls D/A converter IC901 in the variable recording bias circuit as shown in Fig. 39. This voltage is applied to terminal (3) in the first stage of IC902 whose output signal is divided by R913, TH701 and R914. The voltage across R714 is fed to the inverting input of the first stage of IC902 to control its output. TH701 is a temperature compensation thermister and increases the bias in accordance with the temperature characteristics of the head as the temperature varies.

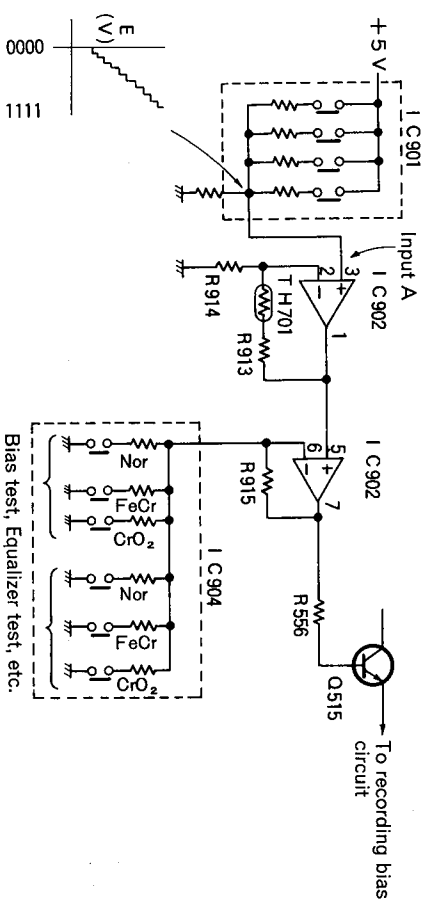


Fig. 39

3) Bias/EQ Test and tape selector detection circuit

Whether the recording bias circuit or recording equalizer circuit is to be tested is determined by a circuit composed of IC903, Q901, Q902, D903, D904 and D906 where the test signal switching data (2 bits) from the microcomputer is analyzed, and then the bias value is selected in accordance with the characteristics of the tape by the tape selector signal. In the recording bias test, a 5 kHz test signal is recorded to obtain the peak playback gain. If a test higher frequency is selected in this test, the bias value is decreased so as to be able to detect the peak point within the D/A converter variation range since the peak point of the playback output signal changes to a lower value of bias current.

4) Bias setting

The switches in IC904 as shown in Fig. 39 are opened or closed by the Bias/EQ Test and tape selector detection circuit to control the voltage at terminal (6) in the second stage of IC902. The bias is established according to the difference of the voltage applied to terminal (5) from this control signal. The base voltage of the bias current control transistor (Q515) is controlled by this.

Fig. 40 shows the recording bias variations of this unit. A base bias value is determined according to the tape selector switch position and, in addition, the base bias is varied through a D/A converter. In the manual mode, the recording bias values are set at A, B and C according to tape selector switch setting.

- A: UDXL I (650 μ A)
- B: Duad (875 μ A)
- C: UDXL II (970 μ A)

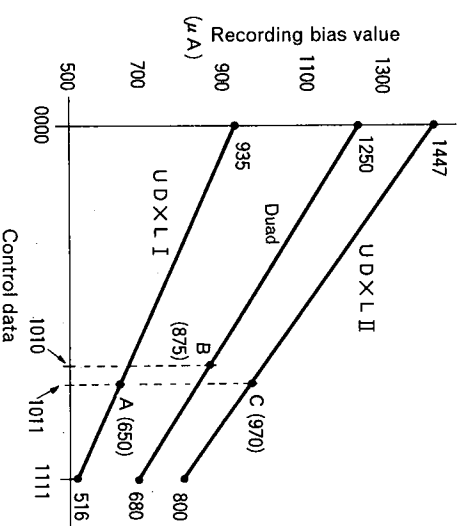


Fig. 40

3) Comparison and peak detection circuits

IC755 and its associated resistors makes up the D/A converter that generates an analog voltage from the 4-bit playback gain detection data from the microcomputer. This output voltage is fed to terminal (2) of the comparison circuit (IC754) shown in Fig. 46, and the playback output voltage is fed to the other input terminal (3). The output voltage of IC754 reverses when the reference voltage (V_2), increasing in increments from the minimum value, agrees

with the playback output voltage (V_1). The microcomputer reads the inverted output signal and the reference voltage control data at this time determines the playback gain. The maximum voltage of the reference voltage generator circuit is limited and if the playback output voltage is greater than the maximum reference voltage, Q769 is switched on to decrease the playback input level by 4 dB.

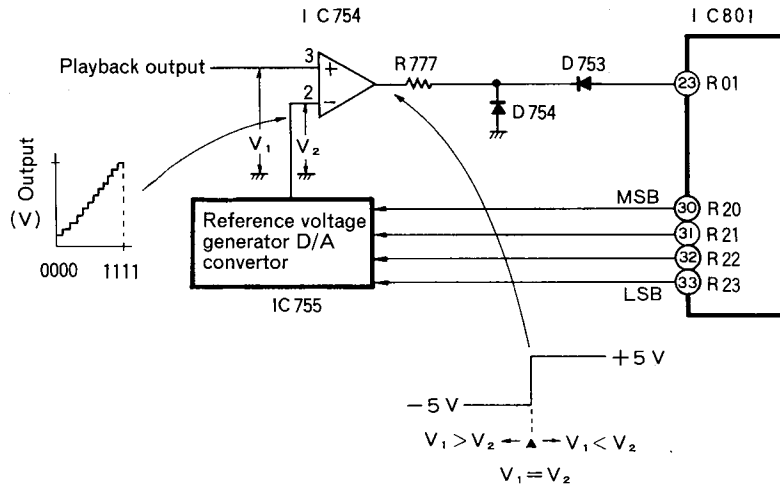


Fig. 46

19. Test Signal Oscillator Circuit

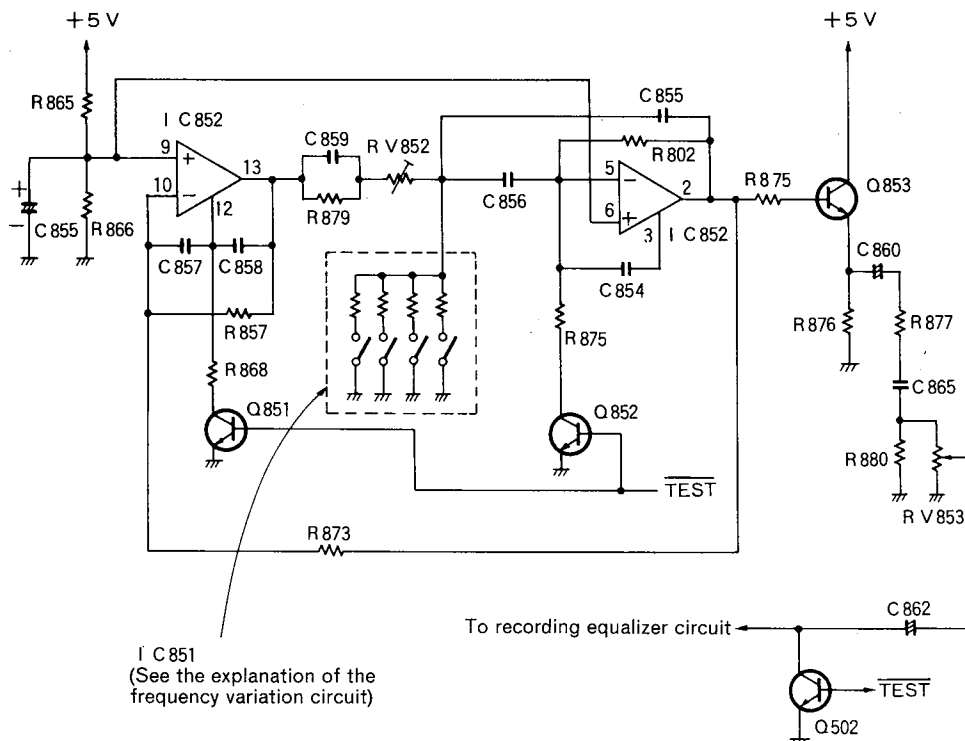


Fig. 47

When obtaining appropriate control data for the low (1 kHz), medium (7 kHz) and high (14 kHz) frequency range compensation circuits in the recording equalizer section, and the recording bias circuit (5 kHz), test circuit are switched together with the frequency of the test signal oscillator circuit.

1) Principle of oscillation

An simplified diagram of the test signal generator circuit is shown below:

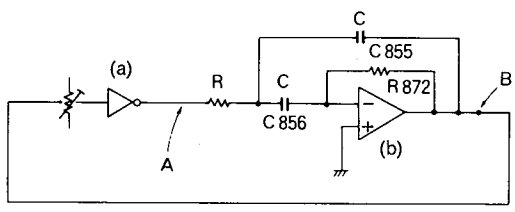


Fig. 48

2) Oscillation frequency variation control

The oscillation frequency is changed by varying R as previously described. 2-bit switching signals are output from terminals (4) and (5) of IC801 to control the oscillation frequency variation and these control the output of IC851. The table on the left shows oscillation frequency variation instruction input data from the microcomputer and the associated output data. "0" represents the open collector state. To oscillate the circuit at 1 kHz, output terminal (1) is grounded when the input data is "00".

Input Data		Output Data				Oscillation frequency
⑮	⑬	①	⑤	②	⑥	
0	0	0	1	1	1	1 kHz
0	1	1	0	1	1	5 kHz
1	0	1	1	0	1	7 kHz
1	1	1	1	1	0	14 kHz

Requirement:
Terminals (12) and (14) must be at 0V.

The transfer function between A and B is obtained by the following formula:

$$f = \frac{1}{2 \pi C \sqrt{R \cdot R872}}$$

The circuit forms a band-pass filter with a center frequency of f. Since amplifier (b) is an inverting amplifier, oscillations are obtained by feeding-back the output voltage at point B to point A after inverting the signal by amplifier (a). The oscillation is adjusted to a point where the sinusoidal waveform is not clipped with the amount of feedback controlled by RV852.

R in the above formula is the compound resistance consisting of the output impedance of amplifier (a) and frequency variation resistors (R851 - R860), and the oscillation frequency increases as the value of R is decreased. The actual circuit is as shown in Fig. 47.

Q851 and Q852 are cut off in the test mode, and are on otherwise to prevent oscillation. The output of the oscillator circuit from terminal (2) of IC852 is amplified by Q853, adjusted to the same output level as when 0VU - 20 dB is input and then supplied to the recording equalizer circuit. The test oscillator output is muted by Q502 other than in test mode.

The circuit oscillates at 1 kHz with a resistor of the value set for 1 kHz connected between terminal (1) of IC851 and the junction of RV852 and C856. Two resistors are connected at each of output terminals (4) and (11) of IC851 for oscillations of 1 kHz and 5 kHz respectively for adjustment in the factory.

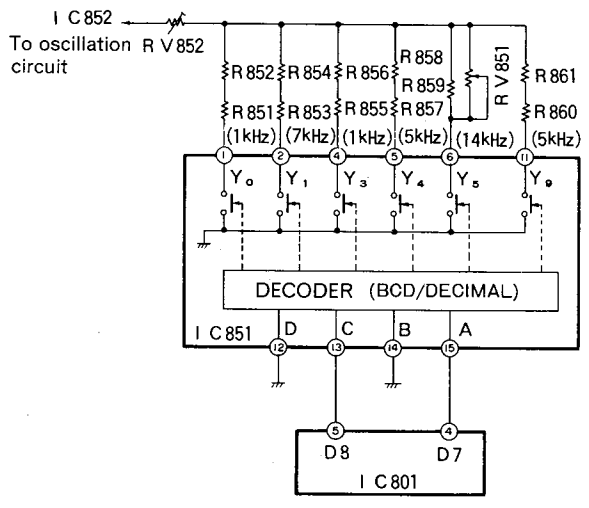


Fig. 49

20. Transported Tape Length Measurement Circuit

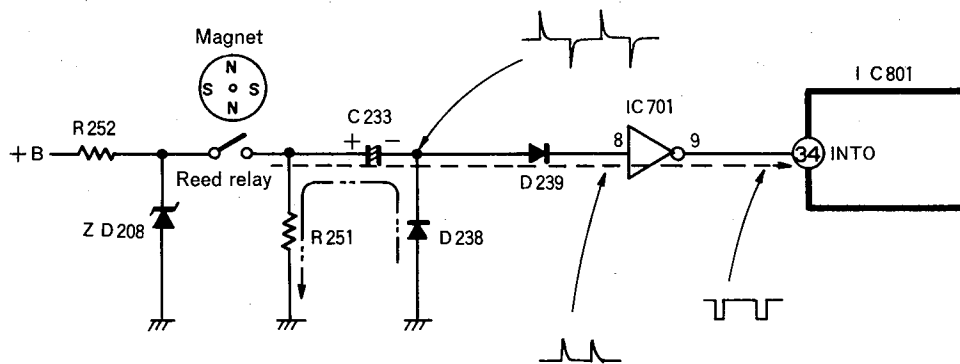


Fig. 50

During testing, the length of transported tape from the beginning of the test (when the test button switch is pushed in the REC/PLAY mode) until the termination of the entire circuit test (termination of the high frequency range compensation test) is measured and the tape is rewound to the start point after the test terminates.

The number of times the reel disc turns is counted by a reed relay and magnet attached to the pulley shaft of the tape counter as shown in the above diagram. Revolutions of the magnet cause the reed relay to repeatedly close and open. A voltage drop is produced across R251 when the reed relay contacts are closed causing the Lo level at terminal (34) of IC801 through C233, D239 and IC701. When the reed relay contacts open, C233 is discharged through D238 and R251 causing the output of IC701 to become Hi. Thus, terminal (34) of IC801 repeats Hi/Lo change-over as the reed relay repeats its closing and opening and opening action. When terminal (34) changes from Lo to Hi, the microcomputer program is interrupted to add 1 to the reel disc counter in the microcomputer. The tape is automatically rewound to the start point after the high frequency range compensation circuit test terminates. During the rewind operation, 1 is subtracted from the reel disc counter in the microcomputer each time terminal (34) of IC801 changes from Lo to Hi. When the reel disc counter value reaches "0", the test mode output terminal (6) of IC801 changes from Hi to Lo to open the stop signal generator circuit (see the explanation on the stop signal generator circuit).

Interrupt

An interrupt causes suspension of the program being executed in order to reply to an interrupt request arising from peripheral conditions, etc. Operation results obtained thus far are temporarily stored together with the program step number for future execution and the execution of program processing is interrupted. The execution of the interrupted program is resumed when the interrupt processing program execution is terminated.

21. Remote Control System

The remote control transmitter section generates a pulse train from push button information. A pushed button corresponds to a 1 pulse signal value in the pulse train while buttons not pushed are represent by pulse signals' values. Each push button corresponds to a specific pulse signal position in the train. This pulse train is pulse width modulated at 50 kHz and drives an infra-red ray emission diode. The receiver section captures this infra-red ray with a

photo diode and associated circuit through an infra-red filter. The captured signal is amplified, detected, its waveform is shaped and then it is supplied to the microcomputer (IC451). The microcomputer performs a "1" and "0" decision on the supplied signal and then discriminate each operation signal from the pulse train to output a single pulse operation signal. The operation pulse signal drives a switching transistor to control the mode control IC(IC201).

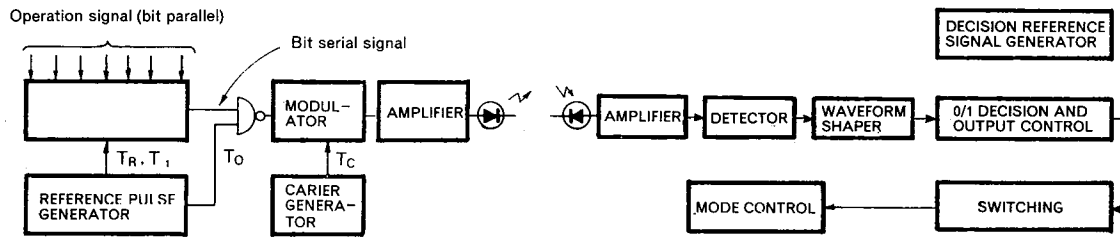


Fig. 51

1) Signal pulses

Because the "1" and "0" values of the arriving signal are determined based on the clock signal (400 kHz) of the microcomputer, margins are provided in the "1"/"0" decision as shown in the figure below in order to allow variations of the clock frequency, arriving signal pulses and threshold level of the detection circuit. Furthermore the microcomputer is provided with a program which examines the input signal twice and presence of an operating input signal is decided when the two test results match to prevent error action.

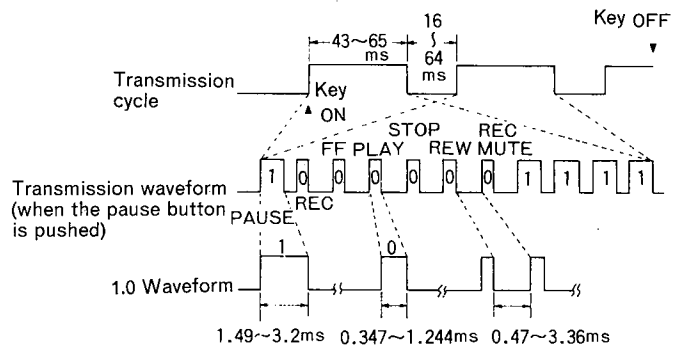


Fig. 53

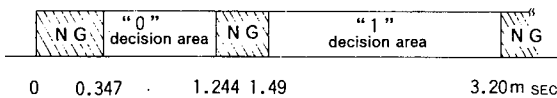


Fig. 52

2) Parallel/serial converter (IC451)

IC451 is a parallel/serial converter in which the bit parallel signals applied to terminals (1), (4), (5), (6), (7), (11), (13), (14) and (15) are set to an internal memory at the rising edge of the clock signal supplied to terminal (10) when terminal (9) is at the Hi level, and the data in the internal memory is sequentially converted to bit serial data at the rising edge of the input clock signal. Terminal (11) is held at the Hi level during data processing.

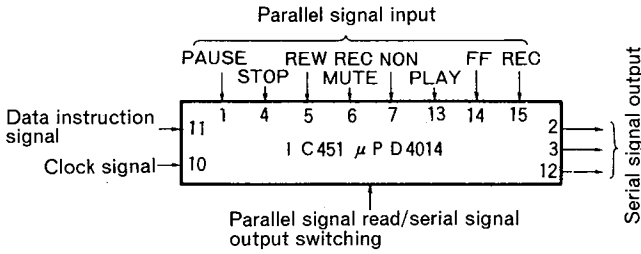


Fig. 54

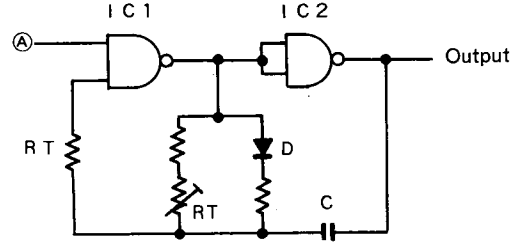


Fig. 55

3) Ta, Ti and Tc pulse generator circuit

Each Ta, Ti and Tc pulse generator circuit is a non stable multi-vibrator circuit composed of two NAND circuit (or two NOR circuits) and a combination of a C and Rs. The duration of the positive cycle is adjusted by RT and, for the Ta and Ti pulses only, the negative cycle duration is set at approx. 50% of the positive cycle duration by a by-pass resistor which is made effective by the switching action of a diode connected in series with the resistor.

4) To and Tr pulse generator circuits

Each of the To and Tr pulse generator circuits is a mono-stable multivibrator composed of two NAND circuits and a combination of C and R. This circuit generates one pulse each time terminal A changes from Lo to Hi.

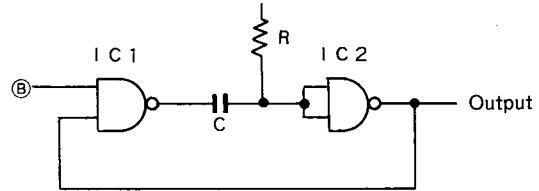


Fig. 56

Circuit Operation

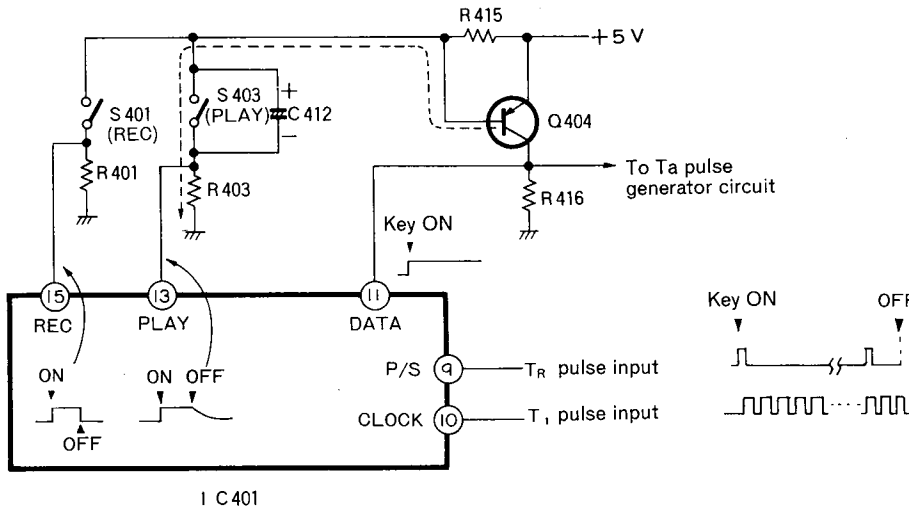


Fig. 57

The circuit operation is explained assuming that both the REC and PLAY buttons are pushed simultaneously. When both the REC and PLAY buttons are pushed simultaneously, the contacts of S401 and S403 are closed to supply current through R415, S401, R401 and through S403 and R403 from the +5V source. The voltage drops produced across R401 and R403 cause terminals (13) and (15) of

IC401 to be set to the Hi level. C412 connected in parallel with S403 is instantaneously discharged once S403 is closed and slowly charged through R415 while S403 is closed so as to act as if, S403 were closed until the second Ta pulse falls (approx. 0.14s to 0.17s) by charging C403 when the button switch is pushed for a very short period of time. When S401 and S403 are closed, Q404 is switched on to start the

operation of the pulse generator circuit and parallel/serial converter. The T_a pulse is generated first and then the T_r , T_i and T_c pulses are generated in this sequence. After the internal flip-flop memory of IC401 is reset at the first rising edge of the AND pulse signal gating from T_r and T_i pulses, only the flip-flop associated with terminals at the Hi level among the parallel input terminals (1), (15), (14), (13), (4), (5), (6) and (7)) are set to 1 (because terminals (13) and (15) are held at the Hi level, memory FFs 2 and 4 as shown in Fig. 58 are set to 1). Then 1 is added to all the eight bits and a 1-bit shift is performed by the rising edge of the first T_i pulse after T_r changes from Hi to Lo. Each memory flip-flop is set to 1 by the addition if it was previously 0, and is set to 0 otherwise. Adding 1 to memory FF1 when it is 1 causes it to be set to 0 and 1 (Hi level) is output from terminal (3) by the carry action. By a repetition of similar operation at the rising edge of the subsequent T_i pulses, 1 is output from terminal (3) at the rising edge of the second and fourth T_i pulses.

1 is output at the rising edge of the ninth and subsequent T_i pulses. The serial signal output from terminal (3) of IC401 (T_A) and T_O pulse are ORed by a gate composed of D401 and D402 ($T_A + T_O$) and applied to terminal (9) of IC403. The T_i pulse is fed to the other input terminal (8) of the NAND gate IC403 as a gate signal to generate an output pulse train satisfying $(T_O + T_A) \cdot T_i$. This pulse is inverted by Q401 and fed to terminal (12) of IC403 as a gate signal. The T_C pulse is applied to the other input terminal (13) of the NAND gate IC403 to generate a pulse width modulated signal which is amplified by Q402 to drive LED407. The collector output of Q402 is amplified by Q403 to drive D405 and D406 which transmit the infra-red rays. However, D405 and D406 do not operate when the remote control unit is installed in the main unit; only LED407 operates.

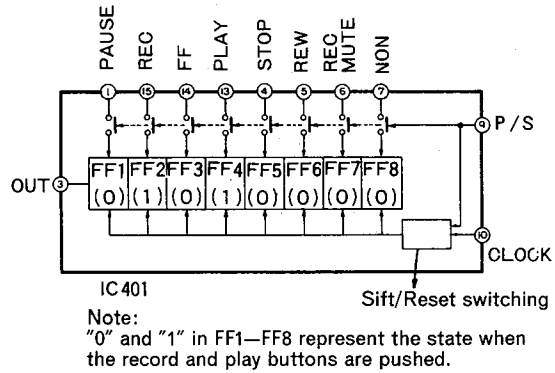


Fig. 58

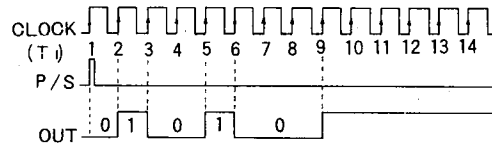


Fig. 59

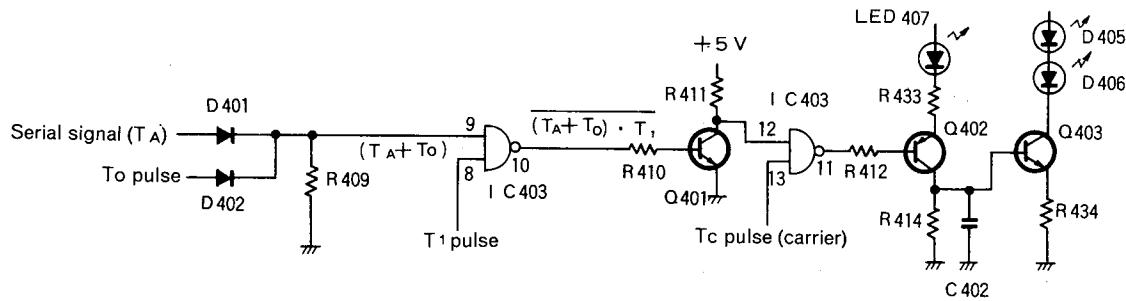


Fig. 60

5) Power supply in transmitter section

When the remote control unit is installed in the main unit, power is supplied from the main unit. When it is used as a remote control transmitter, the power supply is automatically switched to batteries, and power is supplied to the circuits when operation buttons are pushed.

6) Receiver section

The 50 kHz pulse width modulated infrared ray is captured by a photo diode and 50 kHz tuning circuit through an infrared filter. After being amplified by the following transistors (Q451 – Q453), the 50 kHz carrier component and noise are removed from the signal by a two-stage detector circuit. The output signal from the detector is waveform shaped by Q467 and then supplied to a microcomputer (IC407).

In the detector circuit, a noise signal with a reduced pulse width is attenuated by an integration circuit composed of C463 and C464, and then removed by raising the threshold voltage of Q455 and Q466. Thus, the control signal pulse width after detection is also less than the transmitted pulse width.

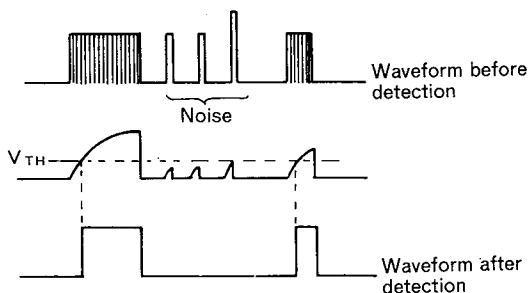


Fig. 61

7) IC451

IC451 (μ PD-550-25) is a microcomputer developed for the remote control of stereo components (tape decks, turntables, tuners, etc). The bit serial signal from terminal (21) after a time of 16 – 64 ms is tested for either 0 or 1 by comparing the value of an internal counter with a set reference value.

The internal counter is counted by the clock signal (400 kHz) while the incoming signal pulse remains at the Hi level. The decision result is sent to the 10-bit shift register A. The serial signal is valid until the tenth bit (tenth pulse) and the following pulses are ignored. To prevent erroneous operations, the serial signal in the next interval is also tested

for 0 and 1 by the identical operation and this is then sent to 10-bit shift register B. If comparison between shift registers A and B shows them to be equal, the key operation at the remote control transmitter section is regarded effective, if it is not, the signal is cancelled. To use this IC in the remote controller of this deck, terminal (22) is held at the Hi level and terminals (23) and (24) at the Lo level. Then, when a serial signal is input to terminals (2) – (8) as a deck mode output signal, the output terminal associated with a pulse of logical "1" is at the Hi level. Q457 – Q462 and the mode control IC (HA12001) are controlled by this signal.

8) Stop and initial reset circuits

When power is turned on, the microcomputer is reset to start executing the program from the beginning and this initial reset signal is used to generate the stop signal that forces the mechanism into the stop mode.

When the power is turned on, a voltage drop is produced across R494 until C465 has been charged. This voltage switches Q468 on. While Q468 is on, Q469 is cut off and the high voltage at the collector is supplied to reset terminal (26) of IC451 through R441 to reset the IC. The high voltage also switches Q470 on, and its high emitter voltage drives the stop pulse generator transistor through R442 and D453. D452 is the discharging path when the power is turned off.

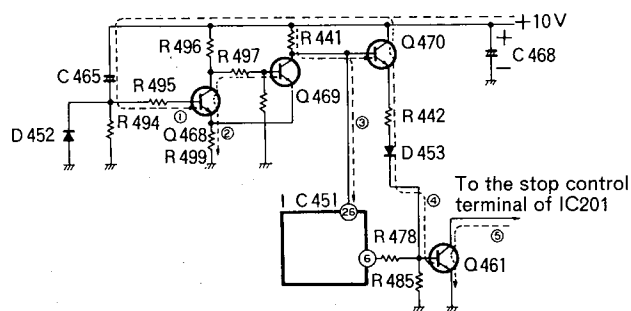


Fig. 62

9) Timing diagram of signals in transmitter section

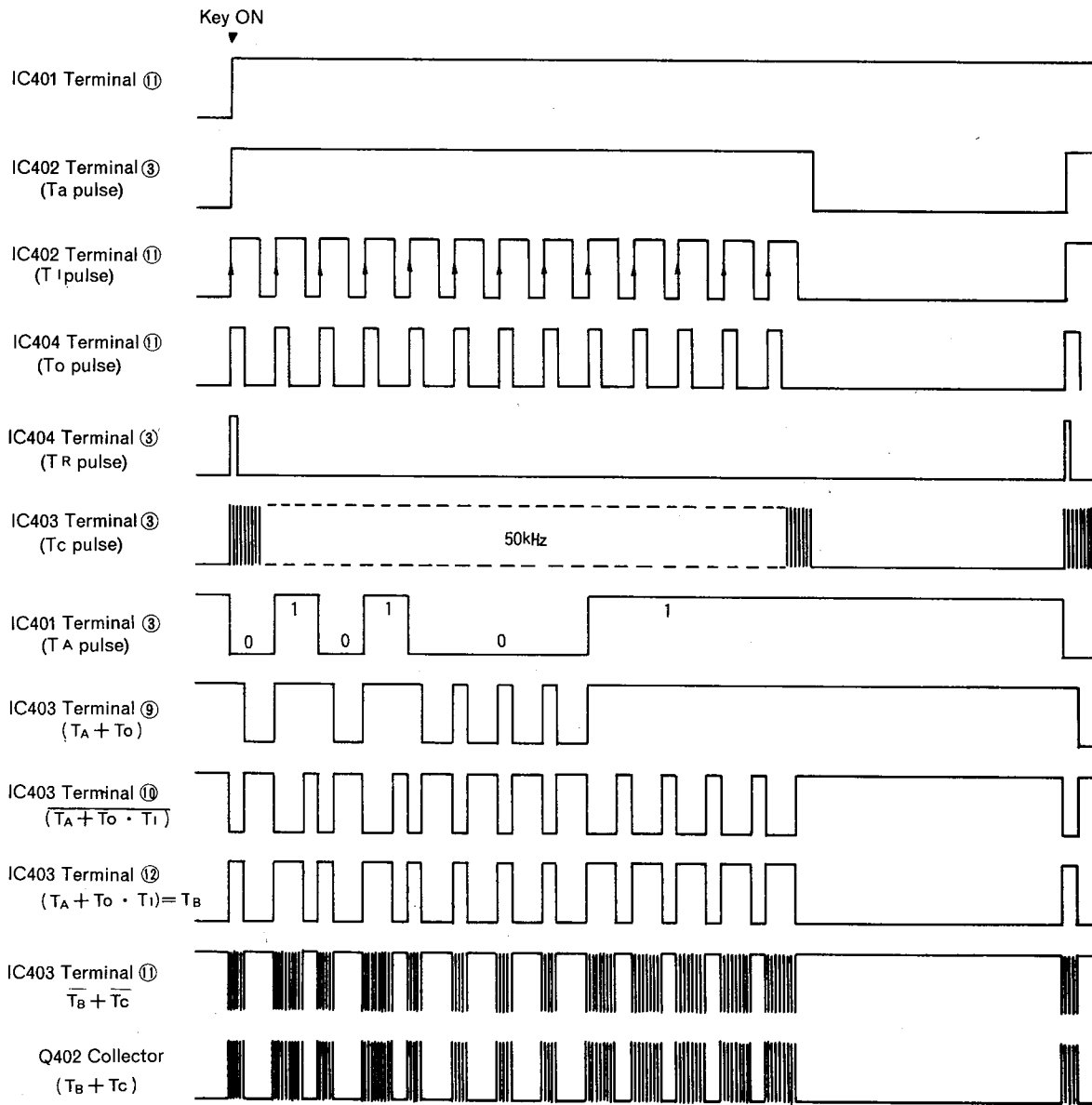


Fig. 63

10) Timing diagram of input signal test and output signals in receiver section

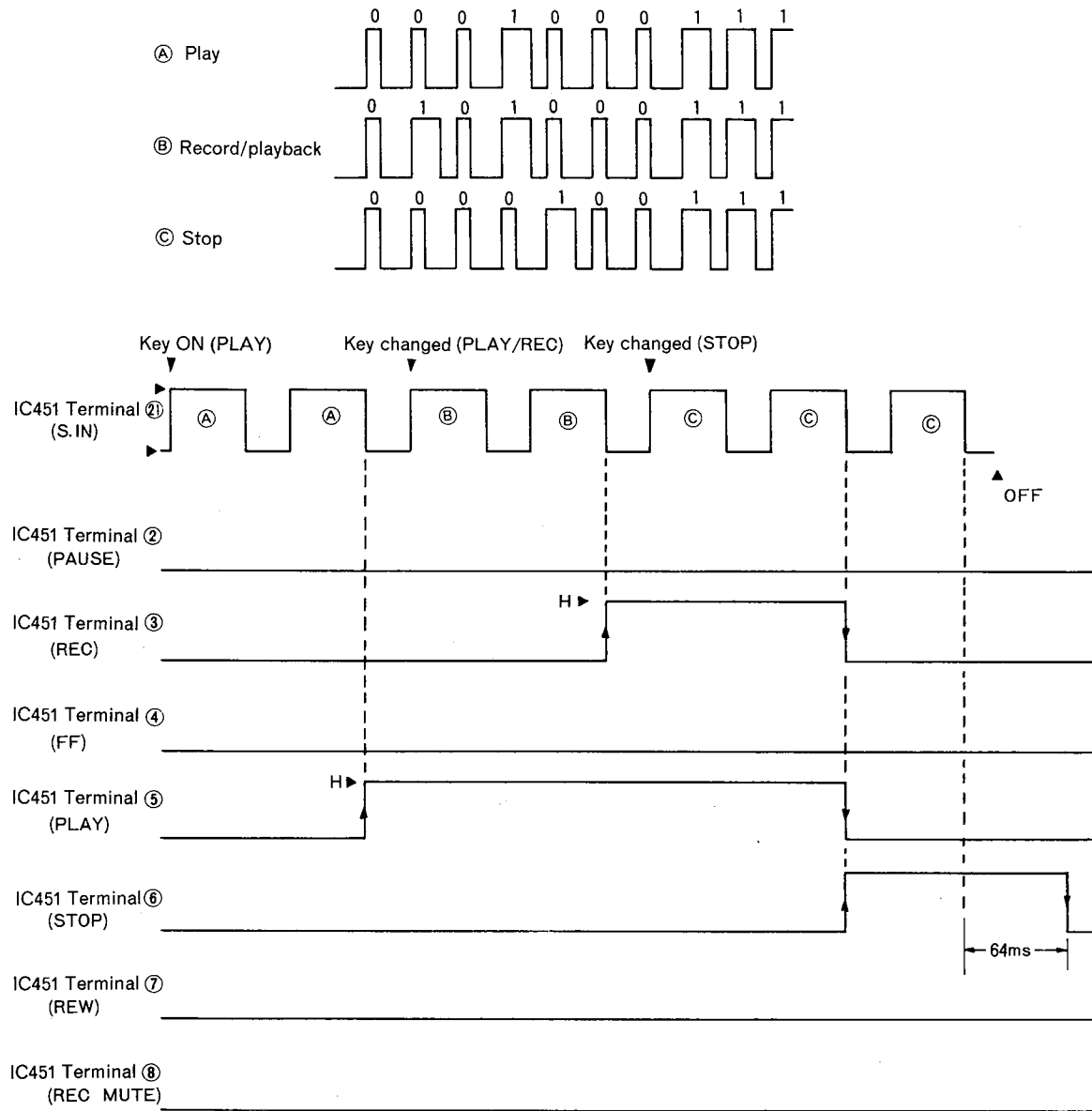


Fig. 64

22. Use of terminals of IC451

Terminal No.	Terminal symbol	Use
1	CL1	CLOCK setting terminals of microcomputer (Oscillation frequency: 400 kHz)
42	CL0	
2	PC0	PAUSE output terminal. Set to Lo potential during PAUSE operation.
3	PC1	REC output terminal. Set to Lo potential during REC operation.
4	PC2	FF output terminal. Set to Lo potential during FF operation.
5	PC3	PLAY output terminal. Set to Lo potential during PLAY operation.
6	PD0	STOP output terminal. Set to Lo potential during STOP operation.
7	PD1	REW output terminal. Set to Lo potential during REW operation.
8	PD2	REC MUTE output terminal. Set to Lo potential during REC MUTE operation.
9 ? 13	PD3 ? PE3	Idle terminals
14	Vss	Power terminal on Hi side
15	TEST	Microcomputer TEST terminal. Connected to Vss because it is not usually used.
16 ? 20	PF1 ? PG0	Idle terminals.
21	PA0	Serial signal input terminal. Serial signal is input only when remote control button on transmitter side is pressed.
22 ? 24	DEB 1 ? DEB 3	Terminals set to prevent interference between remote control and other equipment (especially from other makers). In this unit, terminals (23), (24) are set to Lo, terminal (22), to Hi.
25	INT	Interrupt terminal. Connected to Vss because it is not usually used.
26	RESET	Reset terminal. Perform initial resetting with this terminal set to Lo potential when power is first applied.
27	Vcc	Power terminal

Terminal No.	Terminal symbol	Uses of terminals in different modes			
		Just after power ON	Just after power OFF	Mode other than TEST	During testing
21	Vss	+5V potential to power terminal and terminal (14) (V dips) on Hi potential side.			
22	R00	Stops progress of program until this terminal becomes Hi potential after initial reset is complete.		REC mode signal input. Judged as REC mode if Lo potential	TEST operation starts when TEST operation input and the REC input of this terminal are input.
23	R01			PLAY mode signal input. Judged as PLAY mode if Lo potential.	Detects the output changeover potential of the comparator during PLAY gain detection when the peak PLAY gain is reached. Judges the peak value as the point where Lo potential changes to Hi.
24	R02		Power OFF is detected by potential change between this terminal and terminal (35). When terminal (35) is set to Hi within 300ms from the time when this terminal is set to Hi, power is judged to be OFF.	Detects EJECT of cassette lid. Cassette lid is judged to be OPEN when potential is Hi.	Operates D/A converter after one resetting PLAY gain held by capacitor during PLAY gain detection. Hi potential during resetting.
25	R03	Memory (RAM) CLEAR input of microcomputer. Memory is cleared when this terminal is set to Hi potential.			
26	R10	Input terminals of microcomputer to transfer data from external RAM.	Output terminals of microcomputer to transfer data to external RAM.	Input terminals to select memory (MANUAL, M1 – M3). When any of memories is selected, Hi potential is applied and this Hi potential is held. However, when no data is inside selected memory, HOLD is not performed.	
29	R13			Terminal (26) : M1 memory " (27) : M2 memory " (28) : MANUAL memory " (29) : M3 memory	
30	R20	Outputs Data address when transferring data from microcomputer to external RAM or from external RAM to microcomputer.		Outputs Tape position memorized in each memory (MANUAL, M1 – M3) by time sharing.	4-bit control signal output of play gain detecting D/A converter as well as during modes other than TEST mode.
33	R23	Terminal (30) : 2 ⁰ bit " (31) : 2 ¹ bit " (32) : 2 ² bit " (33) : 2 ³ bit			Terminal (30) : 2 ⁰ bit " (31) : 2 ¹ bit " (32) : 2 ² bit " (33) : 2 ³ bit
34	INT0				Detects revolution of reel disc by means of reed relay to detect distance from TEST start point to high pass REC equalizer TEST finish point. When this terminal changes to Hi potential from Lo potential, one is added/subtracted to/from the reel disk counter built in the microcomputer.
35	INT1		Detects power OFF by change of potential between this terminal and terminal (24). When this terminal is set to Hi within 300ms from time when terminal (24) is set to Hi, power is judged to be OFF.		Input to change TEST mode (STOP, FF, REW, PAUSE, (PLAY) (during REW) buttons pressed) during testing. When this terminal changes to Hi potential from Lo potential during TEST, TEST mode stops.
36	R30	Outputs data address when transferring data from microcomputer to external RAM or from external RAM to microcomputer.		Outputs REC equalizer control data of 6 circuits of both L/R channels synchronized with L/R selection signal of terminal (7) and CLOCK signal of terminal (8).	
39	R33	Terminal (36) : 2 ⁰ bit " (37) : 2 ¹ bit " (38) : 2 ² bit " (39) : 2 ³ bit		Terminal (36) : 2 ⁰ bit " (37) : 2 ¹ bit " (38) : 2 ² bit " (39) : 2 ³ bit	
40	D1			Outputs Hi potential when REC equalizer circuit and REC bias circuit are operating using test data. Set this terminal to Hi with tape running in REC mode when testing.	Holds Hi potential until test data is transferred to any of M1 – M3 memories from start of testing.
41	D2			Detects Tape selector "NOR". Hi potential is held with NOR button pressed. However, if any other tape selector is pressed simultaneously, HOLD is not done.	
42	D3			Detects "FeCr". Hi potential is held with FeCr button pressed. However, if another tape selector is pressed simultaneously, HOLD is not done.	

Terminal No.	Terminal symbol	Uses of terminals in different modes			
		Just after power ON	Just after power OFF	Mode other than TEST	During testing
1	D4			CrO ₂ detection of Tape selector. Hi potential held by pressing CrO ₂ button. However, when other buttons are pressed, HOLD is not done.	
2	D5				Generates 40μs positive pulse and instructs REW operation to mechanism, after testing of high pass equalizer is completed.
3	D6				Outputs Hi potential to reduce input of PLAY gain circuit by 4 dB when Peak point cannot be obtained with D/A converter over-flow during Play gain detection.
4	D7	Outputs Hi potential to Outputs Lo potential until data transfer is complete when microcomputer transfers data from external RAM.	Outputs Hi potential until data transfer is completed when microcomputer transfers data to external RAM.	Hi potential mode; no specified function	Test signal frequency control outputs Hi potential during 7 kHz, 14 kHz
5	D8	Outputs Hi potential until data transfer is completed when data transfer operation is started between microcomputer and external RAM.		Lo mode; no specified function	Test signal oscillation frequency control output. Outputs Hi potential during 5 kHz, 14 kHz.
6	D9			Lo mode; no specified function	Output Hi potential until testing is started, testing of high pass equalizer and rewinding to START point is completed.
7	D10			Since control data for all 6 recording equalizer circuits of both L/R channels are transmitted by time sharing, data is changed over to both L/R channels by this output. L channel is designated by Hi potential, R channel by Lo potential; potential changes at intervals of 30ms and is always output.	
8	D11			Since control data for all 6 recording equalizer circuits of both L/R channels is transmitted by time sharing, this outputs CLOCK output of shift register to generate changeover signals to distribute the data to Low, Medium, High pass equalizer circuits synchronized with the L/R changeover signal of terminal (7). Always outputs Hi potential for 10ms, Lo potential for 40μs repeatedly.	
9	D12		Generates 20μ negative pulse every time 4-bit data of designated address is transferred when microcomputer transfers data to external RAM, synchronizing with external RAM.	Outputs recording bias control data of selected memory (MANUAL, M1 – M3) during REC mode. Control output: 2-bit signal.	
10 ?	D13 ?			Outputs recording bias control data of selected memory (MANUAL, M1 – M3) during REC mode. Control output: Terminal (10) : 2 ¹ bit Terminal (11) : 2 ² bit " (12) : 2 ³ bit	
12	D15				
13	CLK	CLOCK oscillation frequency checking terminal which is standard of microcomputer operation (set to 400 kHz in this unit).			
14	V disp	Power terminal. Connected to 0V pattern.			
15	CGR	Sets oscillation frequency by means of external resistor and capacitor to operate built-in CLOCK oscillation circuit.			
16	Vdd	-5V potential to Power terminal, terminal (14) on Lo side.			
17	Vdd				
18	SYNC	TEST terminal of Microcomputer. Connected to Vss because it is not usually used.			
19	TEST2				
20	RESET	Initial reset input to operate program from top after power is switched on. Initial reset is done with Lo potential.	Should be at Hi potential until data transfer from microcomputer to external RAM is completed.	Should be at Hi potential	Should be at Hi potential

DISASSEMBLY

1. Cassette lid

- 1) Remove two screws as shown in Fig. 65 to clean the head, capstan, pressure roller, etc. (Shown (1)).
- 2) Remove four screws ((1) & (2)) as shown in Fig.65 for head adjustment.

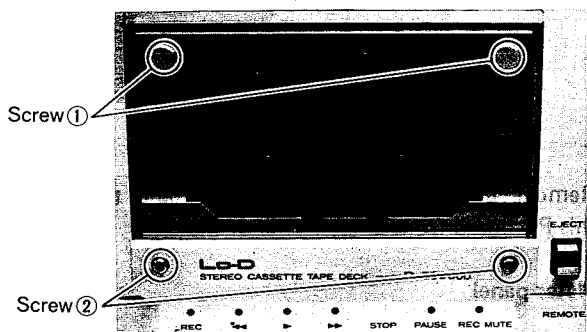


Fig. 65

4. Front metal

Remove six screws after removing monitor and Dolby NR knobs as shown in Fig. 68

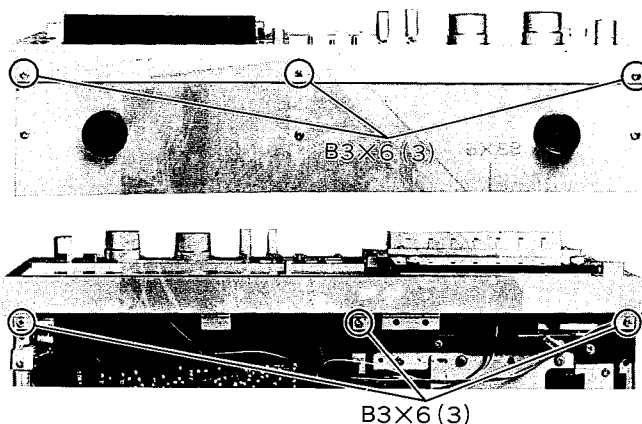


Fig. 68

2. Upper cover

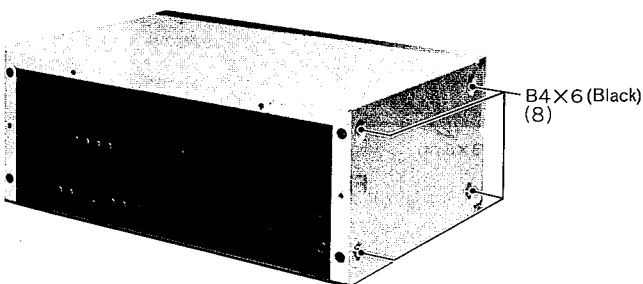


Fig. 66

5. Recording equalizer PC board

When checking the Amplifier PC board or the Recording equalizer control PC board, remove the Recording equalizer PC board.

Remove the screws and after this, this PC board will be able to open approx. 90° with connections.

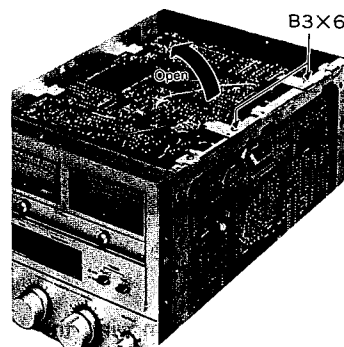


Fig. 69

3. Bottom cover

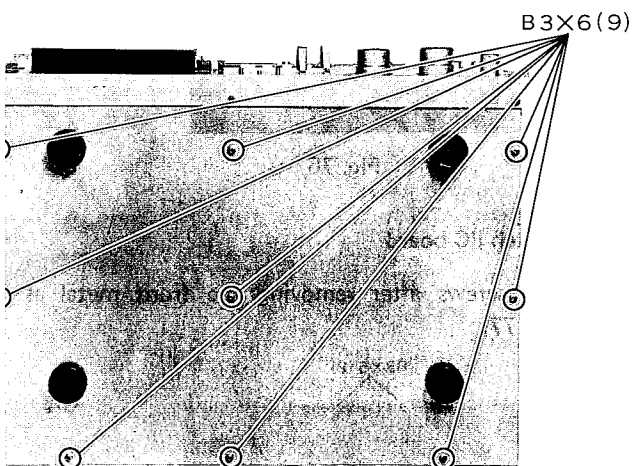


Fig. 67

6. Control PC board

When check the cassette chassis or power circuit block, remove the control PC board.

Remove two screws and after this, this PC board will be able to open approx. 90° with connections as shown in Fig. 70.

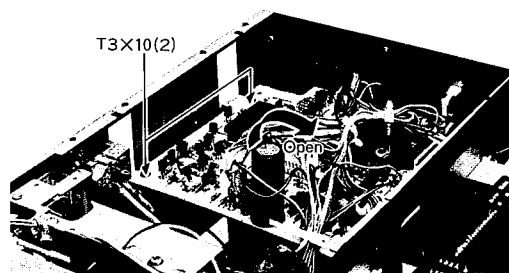


Fig. 70

7. Recording equalizer control PC board

It will be able to check this PC board by opening the recording equalizer PC board. And, remove two screws and pull out this PC board as shown in Fig. 71

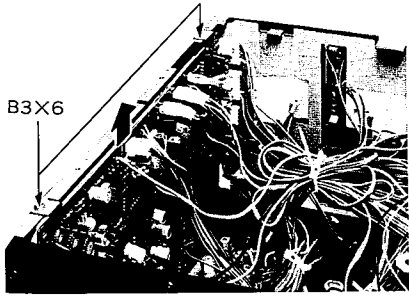


Fig. 71

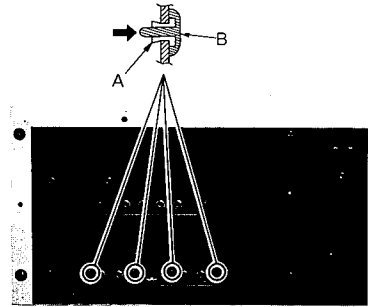


Fig. 74

4) Remove the connections and sockets and then remove this PC board from bottom side of the unit.

8. Amplifier PC board

It will be able to check this PC board by removing the bottom cover. When remove this PC board, take following procedures.

1) Remove four screws after removing the bottom cover as shown in Fig. 72.

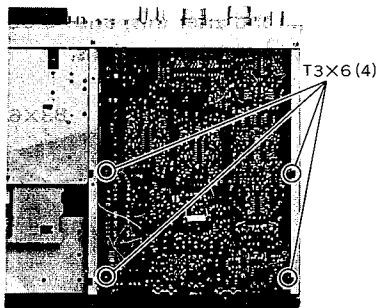


Fig. 72

2) Remove two screws after removing the front panel as shown in Fig. 73.

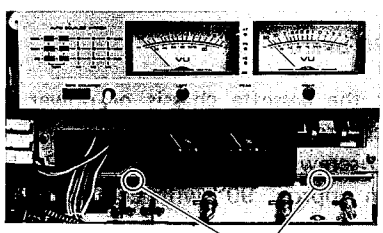


Fig. 73

3) Remove four rivets on the rear side of the upper cover. When remove the rivet, push the B as direction of narrow as shown in Fig. 74. When replace the rivet, replace the A and then, push the B.

9. Meter panel

Remove four screws and two stoppers as shown in Fig. 75.

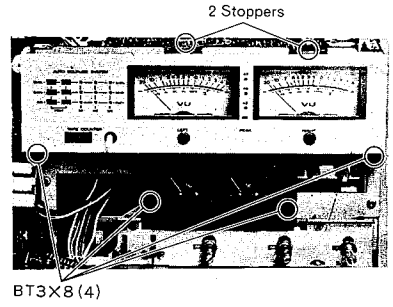


Fig. 75

10. Switch PC board

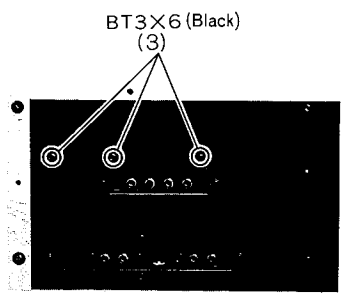


Fig. 76

11. Tape switch PC board

Remove two screws after removing the front metal as shown in Fig. 77.

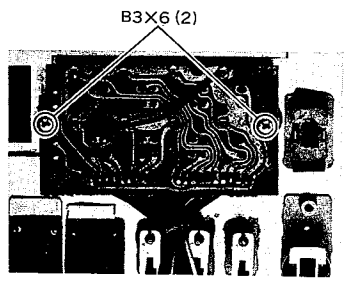


Fig. 77

12. Cassette deck chassis

1) Remove four screws as shown in Fig. 78.

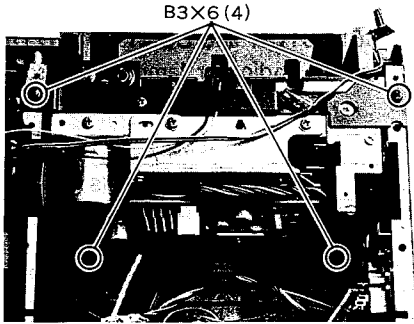


Fig. 78

2) Remove the counter belt on the pulley side of the counter.
And remove the Mode indicators PC board during pulling up the chassis as shown in Fig. 79.



Fig. 79

3) Move the chassis until the chrome detection piece on the chassis to the notched portion on the chassis as shown in Fig. 80.

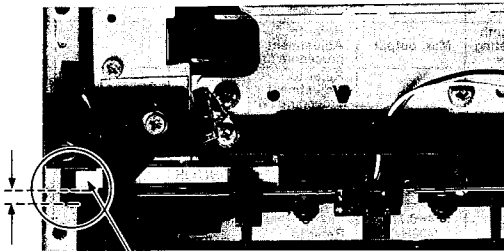


Fig. 80

4) Pull up the chassis and move from head plate solenoid side of the chassis during bending the chassis to direction of the arrow as shown in Fig. 81.

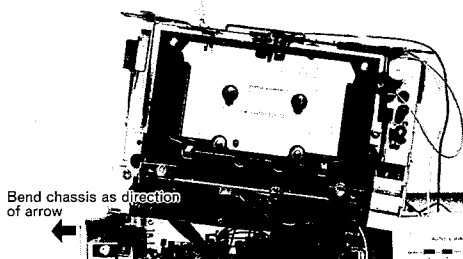


Fig. 81

13. Light receiving block

Remove two screws without the remote control unit.

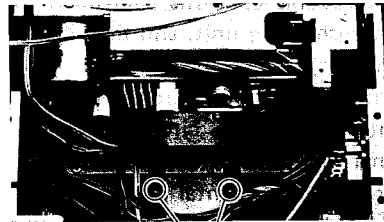


Fig. 82

14. Light receiving PC board

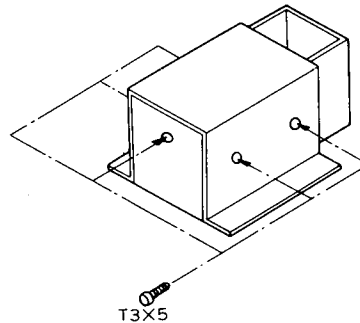


Fig. 83

15. Upper cover of the remote control unit

Remove two screws after removing the battery case.

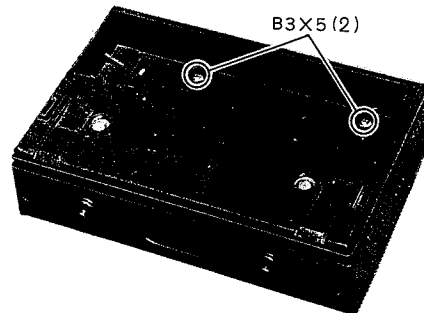


Fig. 84

16. Transmitting PC board

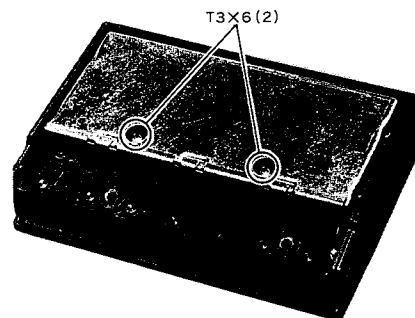


Fig. 85

ADJUSTMENT

This unit is divided into a remote control section for mode control and an amplification/ATRS control section: They can be adjusted independently. The adjustment of the remote control section concerns adjustment of the pulse width of the transmitting unit, and the adjustment of the receiver concerns adjustment of sensitivity.

The adjustment of the amplification/ATRS controller adds the adjustment of the ATRS circuit to the adjustment of the conventional functions. Adjust additional ATRS circuit after adjusting the fundamental circuits in the procedure shown in the table below. The table below is a list of adjustment items, connection of measuring instruments and the adjustment procedures.

Adjustment items (1) - (12) show the fundamental adjustments and (13) - (17), the adjustment of the additional ATRS circuit.

Positions of switches and knobs

Set the switches and knobs to the positions shown below; if not specified, the position is not important.

For TAPE SELECTOR and CONTROLLED DATA, check whether or not the indicator lamp of the selected button lights.

OUTPUT(RV101L,R)	MAX	MEMORY(S7)	OFF
RECORD MIC/DIN (RV21L,R)	MAX	TIMER PLAY/REC (S3, S4) (S7)	OFF
RECORD LINE (RV22L, R)	MAX	* TAPE SELECTOR	NOR
DOLBY-NR (S2)	OFF	*CONTROLLED DATA	MANUAL
MPX (S2)	OFF	RESET	OFF
MONITOR (S1)	TAPE	FIXED/VARIABLE (S13)	VARIABLE
AUTO REWIND STOP/PLAY (S5,S6)	OFF		

Adjustment of Amplifier and ATRS

Item No.	Job	Measuring instrument used and connection			Test or check tape used	Mode	Adjustment position	Adjusted Value	Adjustment procedure	Remarks
		Measuring instrument	Input terminal	Output terminal						
1	Setting positions of switches & knobs	Set positions of switches and knobs referring to Table 4.								
2	Adjustment of level meter with power OFF	-	-	-	-	Power OFF	Pointer adjusting knob	Set pointer to -20VU	-	-
3	Cleaning & demagnetizing tape running system									
4	Tape speed adjustment	Frequency counter	-	LINE OUT	Tape speed test tape (3kHz)	PLAY mode	RT1	3000Hz +30Hz -10Hz	Refer to Adjustment procedure (1)	-
5	Adjustment of REC/PLAY head	Height	-	-	-	-	-	-	Refer to Adjustment procedure (2)	
		Tilt	-	-	-	-	-	-	Refer to Adjustment procedure (2)	
		Azimuth	VTVM	-	LINE OUT	Azimuth adjusting test tape (10kHz)	PLAY mode	Azimuth adjusting screw	Max. output	Refer to Adjustment procedure (3)
6	Clearing external memory (IC802)	-	-	-	-	-	-	-	Refer to Adjustment procedure (4)	
7	Adjustment of source monitor level	• Audio oscillator (400Hz) • VTVM	LINE IN	TP2, TP4	-	PLAY mode	Input	TP2=0.775V (400Hz)	Refer to Adjustment procedure (5)	MONITOR "SOURCE"
							RT22L,R	TP4=0.775V (400Hz)		
8	Adjustment of level meter when input is as specified	Audio oscillator (400Hz) VTVM	LINE IN	TP4	-	PLAY mode	Input	TP4=0.775V (400Hz)	Refer to Adjustment procedure (6)	MONITOR "SOURCE"
							RT104L,R	Level meter indicates Dolby mark		
9	Adjustment of PLAY gain	VTVM	-	TP4	Dolby calibration test tape (400kHz)	PLAY mode	RT101L,R	TP4=0.775V (400Hz)	Refer to Adjustment procedure (7)	MONITOR "TAPE"
10	Adjustment of Dolby NR	• Audio oscillator (2kHz) • VTVM	LINE IN	TP1, TP2	-	REC mode	Input	TP1=-20dB (2kHz)	Refer to Adjustment procedure (8)	DOLBY-NR "OFF"
							RT21L,R	TP2=-15.7dB (2kHz)		
							Input	TP2=15.7dB (2kHz)	Refer to Adjustment procedure (9)	DOLBY-NR "ON"
							RT103L,R	TP4=-20dB (2kHz)		
11	Adjustment of bias trap	VTVM	-	Between TP513 and TP515, R CH Between TP514 and TP515, L CH	-	REC mode	L508L,R	Min. output	Refer to Adjustment procedure (10)	-

Item No.	Job	Measuring instrument used and connection			Test or check tape used	Mode	Adjustment position	Adjusted Value	Adjustment procedure	Remarks							
		Measuring instrument	Input terminal	Output terminal													
12	(1) Setting REC level and high pass trimmer	Set RV501, 502 (REC level) fully in clockwise direction viewed from parts side and RT102 R/L (setting PLAY high pass level), to center of variable range															
	(2) Rough adjustment of bias level when using Normal tape	• Audio oscillator (1kHz) • VTVM	LINE IN	LINE OUT	Check tape (C-90) Hitachi UD-ER	REC mode	Input	OVU-20dB (1kHz)	Refer to Adjustment procedure (11)	MONITOR "SOURCE"	This adjustment is to check monitor output when 1kHz is input. Assume output at this time to be V ₁ .						
	RV504,506						Max. output	MONITOR "TAPE"									
	(3) Adjustment of REC level when using Normal tape	• Audio oscillator (10kHz) • VTVM	LINE IN	LINE OUT	Check tape (C-90) Hitachi UD-ER	REC mode	Input	OVU-20dB (1kHz)	Refer to Adjustment procedure (12)	MONITOR "SOURCE"	This adjustment is to set input						
	RV501,502						=V ₁	MONITOR "TAPE"									
	(4) Fine adjustment of bias when using Chrome tape	• Audio oscillator (10kHz) • VTVM	LINE IN	LINE OUT	Check tape (C-90) Hitachi UD-ER	REC mode	Input	OVU-20dB (10kHz)	Refer to Adjustment procedure (13)	MONITOR "SOURCE"	This adjustment is to set input						
	RV504,506						=V ₁	MONITOR "TAPE"									
(5) Adjustment of PLAY high pass when using Normal tape	• Audio oscillator (15kHz) • VTVM	LINE IN	LINE OUT	Check tape (C-90) Hitachi UD-ER	REC mode	Input	OVU-20dB (15kHz)	Refer to Adjustment procedure (14)	MONITOR "SOURCE"	This adjustment is to set input							
RT102,L,R						=V ₁	MONITOR "TAPE"										
(6) Fine adjustment of bias when using Normal tape	• Audio oscillator • VTVM	LINE IN	LINE OUT	Check tape (C-90) Hitachi UD-EX	REC mode	Input	OVU-20dB (1kHz)	Refer to Adjustment procedure (15)	MONITOR "SOURCE"	This adjustment is to check monitor output when 1kHz signal is input. Assume output at this time to be V ₂ .							
RV902						OVU-20dB (10kHz)	MONITOR "SOURCE"		This adjustment is to set input when 10kHz signal is input.								
							=V ₂			MONITOR "TAPE"							
(7) Fine adjustment of bias when FeCr tape is used	• Audio oscillator • VTVM	LINE IN	LINE OUT	Check tape (C-90) SONY DUAD	REC mode	Input	OVU-20dB (1kHz)	Refer to Adjustment procedure (16)	MONITOR "SOURCE"	Assume LINE OUT output at that time to be V ₃ .							
RV901						OVU-20dB (10kHz)	MONITOR "SOURCE"										
							=V ₃		MONITOR "TAPE"								
13	(1) 1 kHz	Oscilloscope or synchroscope VTVM		Terminal (3) of TP852	Mode other than test mode	RV852 (oscillation output)	1kHz±100Hz Point where peak point of waveform is not clipped	Refer to Adjustment procedure (17)	—	Assume reading of valve voltmeter at this time to be V ₄ .							
	(2) 5 kHz					Checking	• 5kHz±300Hz • V ₄ ±1dB		—								
	(3) 7 kHz					Checking	• 7kHz±500Hz • V ₄ ±0.3dB		—								
	(4) 14 kHz					RV851 (oscillation frequency)	• 14kHz±200Hz • V ₄ ±0.5dB		—								
14	Adjustment of test signal oscillation output	• Audio oscillator • VTVM	LINE IN	Terminal (2) of IC502	Check tape (C-90) Hitachi UD-ER	REC mode	Input	OVU-20dB (1kHz)	Refer to Adjustment procedure (18)	MONITOR "SOURCE"	This adjustment is to check monitor output when 1kHz signal is input. Assume voltage at terminal(2) of IC501 to be V ₅ .						
						TEST mode	RV852	=V ₅									
15	Adjustment of input to PLAY gain detector circuit	• Audio oscillator • VTVM	LINE IN	LINE OUT	Check tape (C-90) Hitachi UD-ER	REC mode	Input	OVU-20dB (1kHz)	Refer to Adjustment procedure (19)	MONITOR "SOURCE"	This adjustment is to set input.						
				•Center terminal of RV751 •Center terminal of RV752			RV571 RV752	• -18.5dB (RV751) • -14.5dB (RV752)		MONITOR "TAPE"							
				(3) Test data. In addition to this, transfer data after test is complete to Memory M ₁ .													
				(4)				LINE OUT			Input	OVU-20dB (1kHz)		MONITOR "SOURCE"	Assume control data to be M ₁		
				(5)				•Center terminal of RV751 •Center terminal of RV752		Check tape (C-90) Hitachi UD-ER		—	—	MONITOR "TAPE"	Assume reading at that time to be V ₆ (control data: M ₁)		
				(6)								RV751 RV752	=V ₆	MONITOR "TAPE"	Assume Control data to be "MANUAL"		
16	Adjustment of bias meter	—	—	—	—	REC mode	RV503	Indicates 100% of bias meter scale	Refer to Adjustment procedure (20)		Assume Control data to be "MANUAL"						
17	Adjustment of sensitivity meter	—	—	—	—	REC mode	RV508	Indicates 100% of sensitivity meter scale			Assume Control data to be "MANUAL"						

Adjustment procedure

- 1) Perform adjustment after heat run for more than 20 minutes.
- 2) Check and adjust the head using the adjusting jig and then mount the cassette tape provided with a mirror to check tape running. (Refer to the adjusting jig manual.)
- 3) Play back the test tape and adjust to the center of the max. output point of both channels.
- 4) Turn off the power once, then turn it on again while pressing the reset switch at the back of the set.
- 5) Adjust the input so that the output voltage at test point TP2 (REC Dolby output terminal) is 0.775V, and then change over the monitor switch to "SOURCE" and adjust the trimmer so that the output at test point TP4 (PLAY Dolby output terminal) is 0.775V.
- 6) Adjust the input so that the output voltage at test point TP4 (PLAY Dolby output terminal) is 0.775V with the monitor switch set to "SOURCE". Next, adjust the trimmer so that the level meter indicates the Dolby mark (+3VU).
- 7) Play back the test tape and adjust the trimmer so that the output voltage at test point TP4 (PLAY Dolby output terminal) is 0.775V.
- 8) Adjust the input so that the input voltage at test point TP1 (REC Dolby input terminal) is -20dB with the monitor switch set to "SOURCE". Then, turn the Dolby-NR switch ON and adjust the trimmer so that the output voltage at test point TR2 (REC Dolby output terminal) is -15.7dB.
- 9) Change over the monitor switch to "SOURCE" and Dolby-NR switch to ON after the REC Dolby circuit (RT21LR) is adjusted, and adjust the trimmer so that the output voltage at test point TP4 (PLAY Dolby output terminal) is -20dB. Then, check that the output of TP4 does not change when the Dolby-NR switch ON/OFF operation is repeated.
- 10) Adjust the trimmer so that the voltage between the test points (between TP513 and TP515 for R CH, between TP514 and TP515 for L CH) is minimum.
- 11) Change over the monitor switch to "SOURCE" and input a 1 kHz, 0VU -20dB signal. Assume the output voltage at the LINE OUT terminal to V1. Next, change over the monitor switch to "TAPE" and adjust the trimmer so that the PLAY output is maximum.
- 12) After rough adjustment of bias in item 2) is completed, change over the monitor switch alternately to "SOURCE" and "TAPE" and adjust the trimmer so that the PLAY outputs with both switch positions are equal.
- 13) Change over the monitor switch to "SOURCE" and input a 10 kHz, 0VU -20dB signal. Change over the monitor switch to "TAPE" and adjust the trimmer so that the PLAY output at that time is equal to V1. Further, change over the monitor switch to "SOURCE", input a 1 kHz, 0VU -20dB signal and check that the PLAY output is equal to V1 when the monitor switch is changed over to "TAPE" again. When the output levels are not equal, re-adjust starting at the item 12-(1).
- 14) Change over the monitor switch to "SOURCE" and input a 15 kHz, 0VU -20dB signal. Change over the monitor switch to "TAPE" and adjust the trimmer so that the PLAY output at that time is equal to V1.
- 15) Set the Tape selector to "CrO₂", change over the monitor switch to "SOURCE" and input a 1 kHz, 0VU -20dB signal. Assume the LINE OUT output at that time to be V2. Next, input a 10 kHz, 0VU -20dB signal and adjust the trimmer so that the PLAY output is equal to V2 when the monitor switch is changed over to "TAPE" again.
- 16) Set the tape selector to "FeCr", change over the monitor switch to "SOURCE" and input a 1 kHz, 0VU -20dB signal. Assume the LINE OUT output at that time to be V3. Next, input a 10 kHz, 0VU -20dB signal and adjust the trimmer so that the PLAY output is equal to V3 when the monitor switch is changed over to "TAPE" again.
- 17) Ground the bases of Q851 and Q852 to obtain the OFF mode (connect terminals (1), (2) of 4P plug TP852 to terminal (4)) and operate the test signal oscillation circuit. Then, remove connector CN901 shown in Fig. 86 from plug TP901 on the PC Board to change over the oscillation frequency selection from microcomputer control to manual control, and short-circuit (1) or open (2) the patterns corresponding to terminal (2) (red), terminal (4) (orange) and the ground according to the changeover data. Change over the oscillation frequency in the order 1 kHz, 5 kHz, 7 kHz and 14 kHz, and check and adjust the oscillation frequency, waveform and oscillation output at that time.

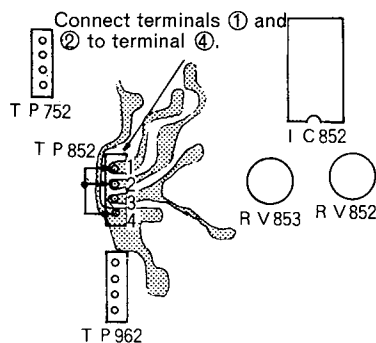
(1) Method of turning Q851, 852 OFF

Fig. 86

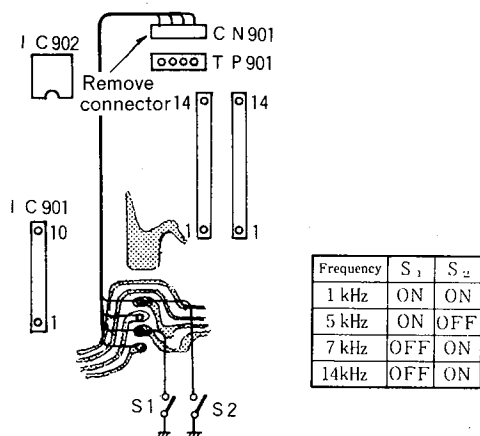
(2) Method of changing over oscillation frequency

Fig. 87

(a) 1 kHz oscillation

Check that the oscillation frequency is 1 kHz \pm 100 Hz and then adjust RV852 so that the peak point of the waveform is not clipped as shown in Fig. 88. Assume the output voltage after adjustment at that time to be V4.

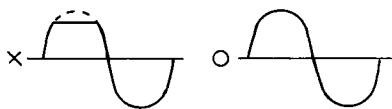


Fig. 88

(b) 5 kHz oscillation

Check that the oscillation frequency is 5 kHz \pm 300 Hz and then check that the output voltage at that time is V4 \pm 1dB.

(c) 7 kHz oscillation

Check that the oscillation frequency is 7 kHz \pm 500 Hz and then check that the output voltage at that time is V4 \pm 0.3dB.

(d) 14 kHz oscillation

Adjust RV851 so that the oscillation frequency is 14 kHz \pm 200 Hz. Check that the oscillation output voltage at that time is V4 \pm 0.5dB. When the oscillation frequency is not as specified above, vary the resistance of the oscillation frequency setting resistance (1 kHz: R551, 5 kHz: R857, 7 kHz: R853). As the resistance is increased the oscillation frequency decreases. Check that the output with each oscillation frequency is within the following values.

Output during 1 kHz oscillation: V4

Output during 5 kHz oscillation: V4 \pm 1dB

Output during 7 kHz oscillation: V4 \pm 0.3dB

Output during 14 kHz oscillation: V4 \pm 0.5dB

When the output is not within the above values, readjust RV852. When this is done, check the oscillation frequency, waveform and output voltage again. Connect connector CN901 to plug TP901 after adjustment is complete.

18) Turn RV751, 752 (setting PLAY gain detector circuit input) fully counterclockwise viewed from the parts side. Use UD-ER (C-90) as the check tape.

Set the deck to the REC mode and input a 1 kHz, 0VU $-$ 20dB signal. Assume the voltage at terminal (2) of IC501 to be V5. Next, adjust RV853 so that the voltage at terminal (2) of IC501 is V5 \pm 1dB when the TEST button is pressed and the deck is in the TEST mode.

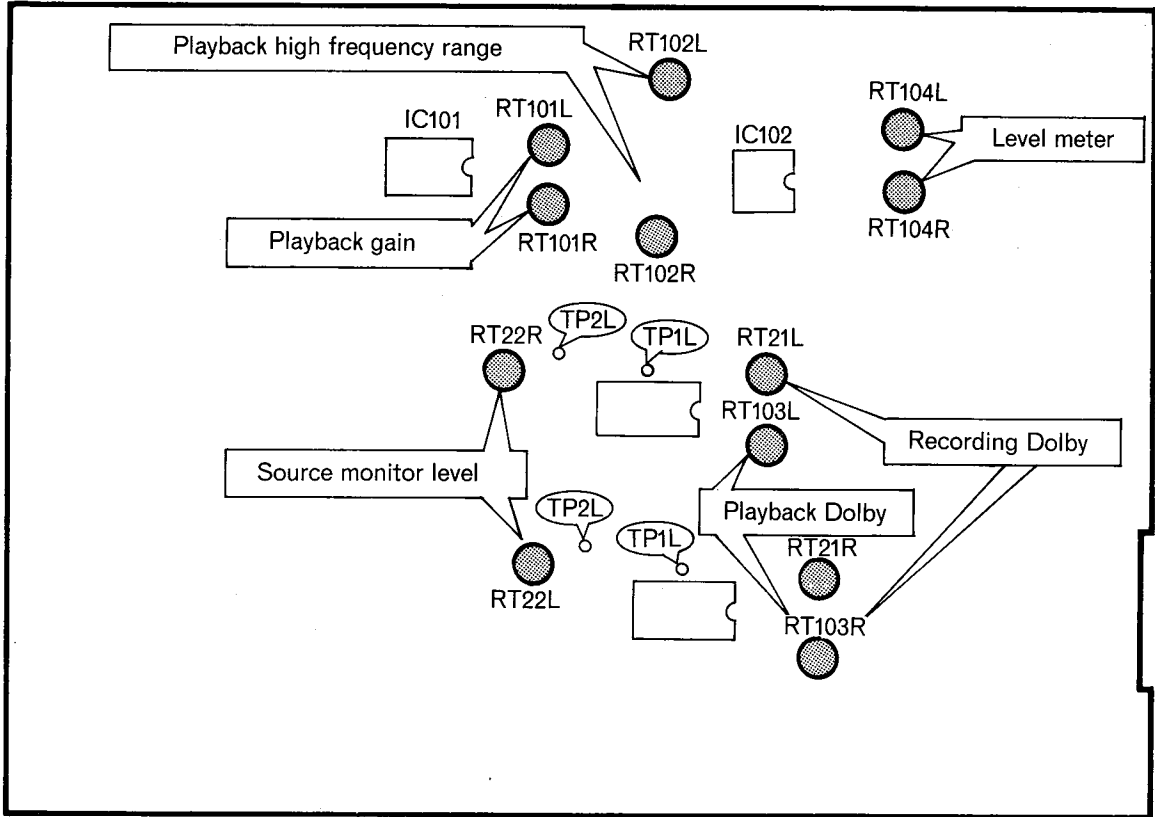
The test mode lasts 20 sec, so complete adjustment during this period.

19) Use the check tape UD-ER (C-90), change over the monitor switch to "SOURCE" and input a 1 kHz, 0VU $-$ 20dB signal. Check that the LINE OUT output at that time and the LINE OUT output when the monitor switch is changed over to "TAPE" are equal. (When they are not equal, adjust RV501 and RV502).

Adjust RV751, 752 (setting the PLAY gain detection input) so that the voltages at the center terminals are $-$ 18.5 dB (RV751) and $-$ 14.5 dB (RV752).

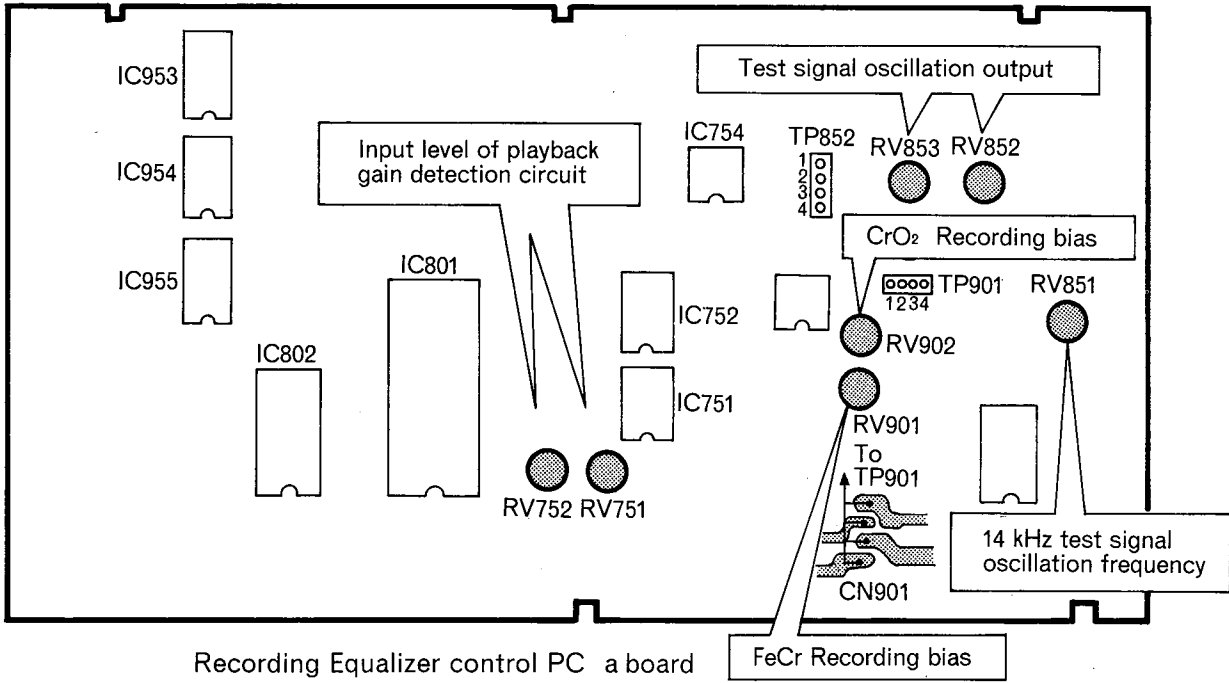
o After checking the above (with the deck is REC mode), press the TEST button to start testing to obtain test data. Transfer the test data after the testing by pressing the TEST button and M1 memory button (press the TEST button before the memory button). Set to the REC mode again (select "MANUAL" for control data at this time), measure voltages at the center terminals of RV751, 752 and assume this voltage to be V6. Then select the M1 control data and adjust RV751 and RV752 so that the voltages at the center terminals of RV751 and RV752 are V6.

20) Select "MANUAL" control data and the "NOR" Tape position and set to the REC mode. Adjust RV503 (bias) and RV508 (sensitivity) so that the bias meter and sensitivity meter indicate "100".



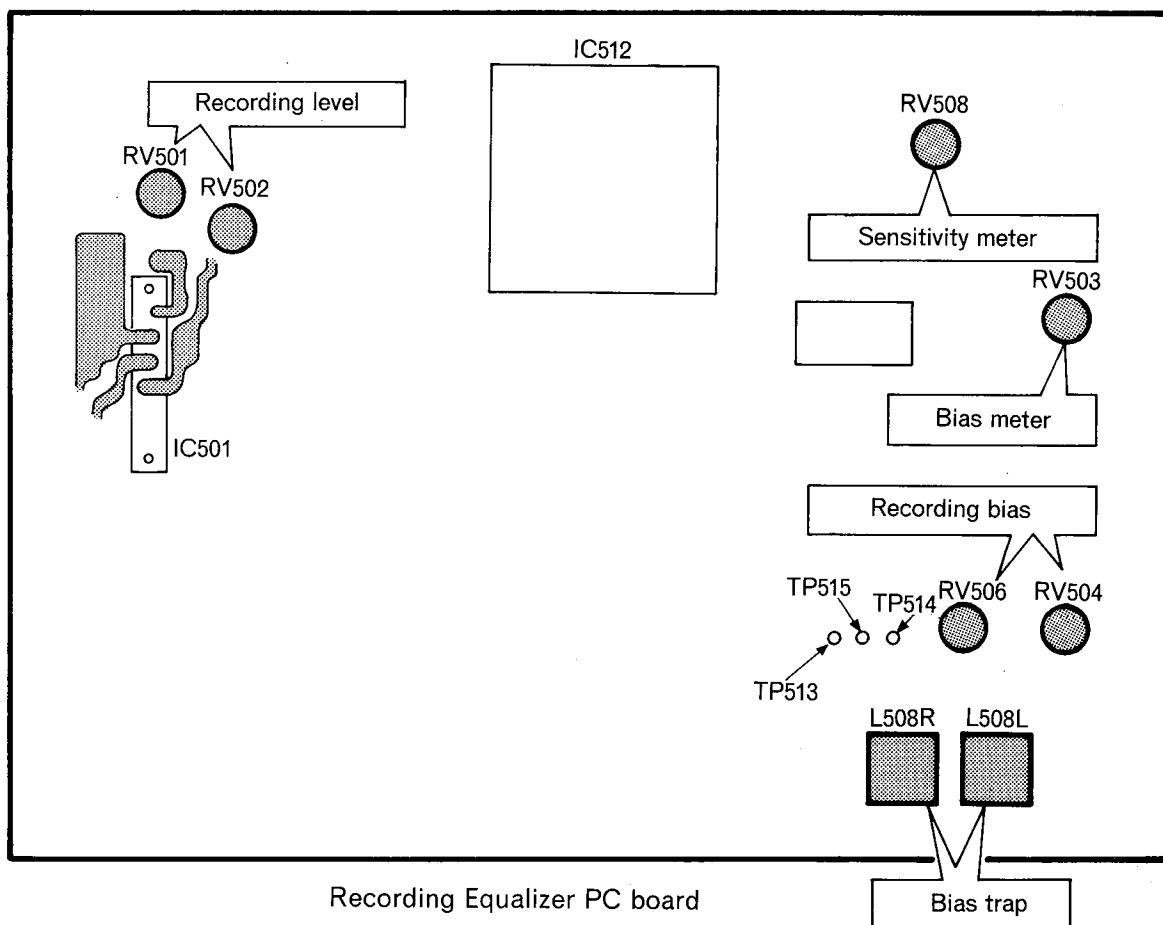
Amplifier PC board

Fig. 89



Recording Equalizer control PC a board

Fig. 90



Recording Equalizer PC board

Fig. 91

Adjustment of Remote Control Section

	Adjustment Item	Measuring instrument		Set's Condition	Adjusted position	Adjustment value	Adjustment procedure
		Measuring instrument used	Connected position				
Transmission unit	① T _A pulse oscillation	Synchroscope	Terminal (3) of IC402	—	RT401	55±2.8ms	
	② T _I pulse oscillation	Synchroscope	Terminal (11) of IC402	—	RT402	2.35±0.12ms	Refer to Adjustment(1)
	③ T _O pulse oscillation	Synchroscope	Terminal (11) of IC403	—	RT403	0.95±0.04ms	
Receiver side	④ Light receiving sensitivity	—	—	Transmission unit: Rated voltage 6V With the REC button pressed	RV451	The REC mode indicator should operate with the transmission unit placed 15-20m away from the reception section. After adjustment is completed, press a button other than the REC button to check that operation is normal.	Refer to Adjustment procedure (2).

Adjustment procedure

1. Set the power voltage of the transmission unit to 6V and keep the operation buttons pressed with the adjustment is completed. Adjust output values of the individual pulse oscillation circuits as specified.

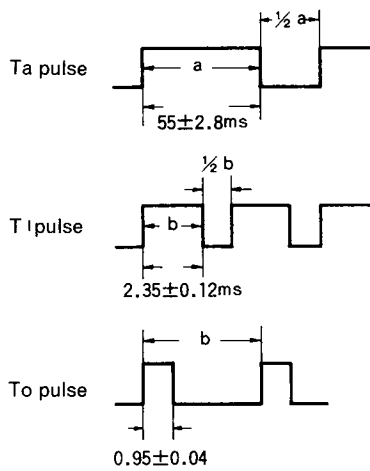


Fig. 92

2. The adjustment of the light receiving sensitivity is to correct for uneven strength of infrared ray reaching the photo-transistor in the receiver from the LED in the transmission unit. It is adjusted using an optical filter in the factory, but the following procedure can be used as a simple method without using jigs.

- (1) Check that the transmission unit is normal.

That is, when the power of the transmission unit is set to 6V and the operation button is pressed, the 4Vp-p pulse should be generated at the collector side of Q403.

- (2) Bring the transmission unit 15 – 20m away from the receiving unit. (More than 10m in specifications)
Set the light receiving section of the deck and the light transmission window to be in a straight line.
The brightness of room illumination is not specified.

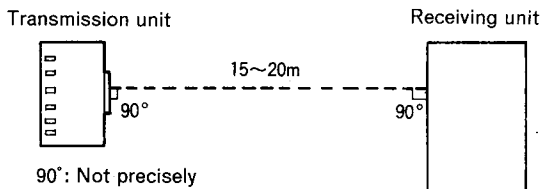


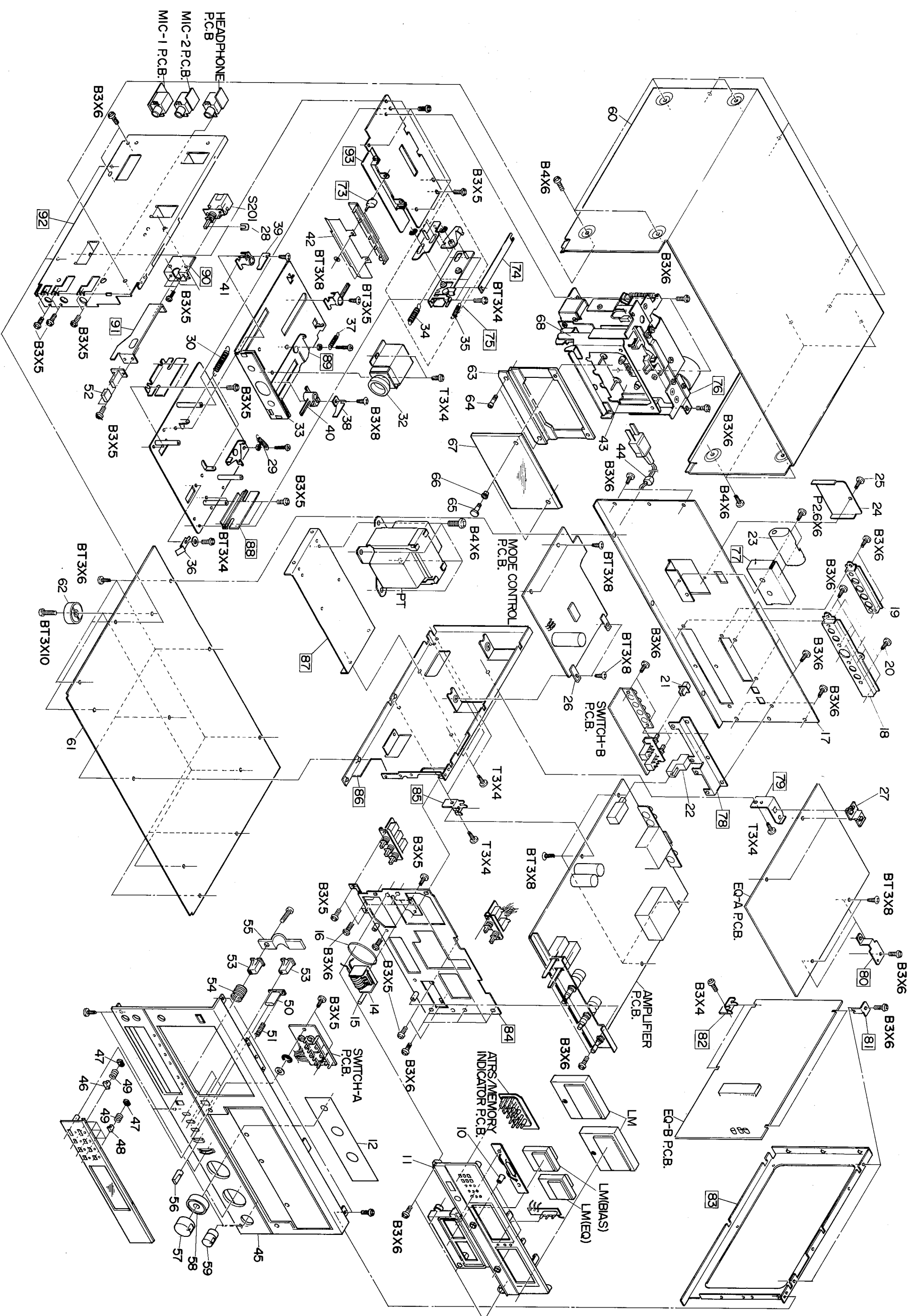
Fig. 93

- (3) Keep the REC operation button of the transmission unit pressed until the adjustment is completed.

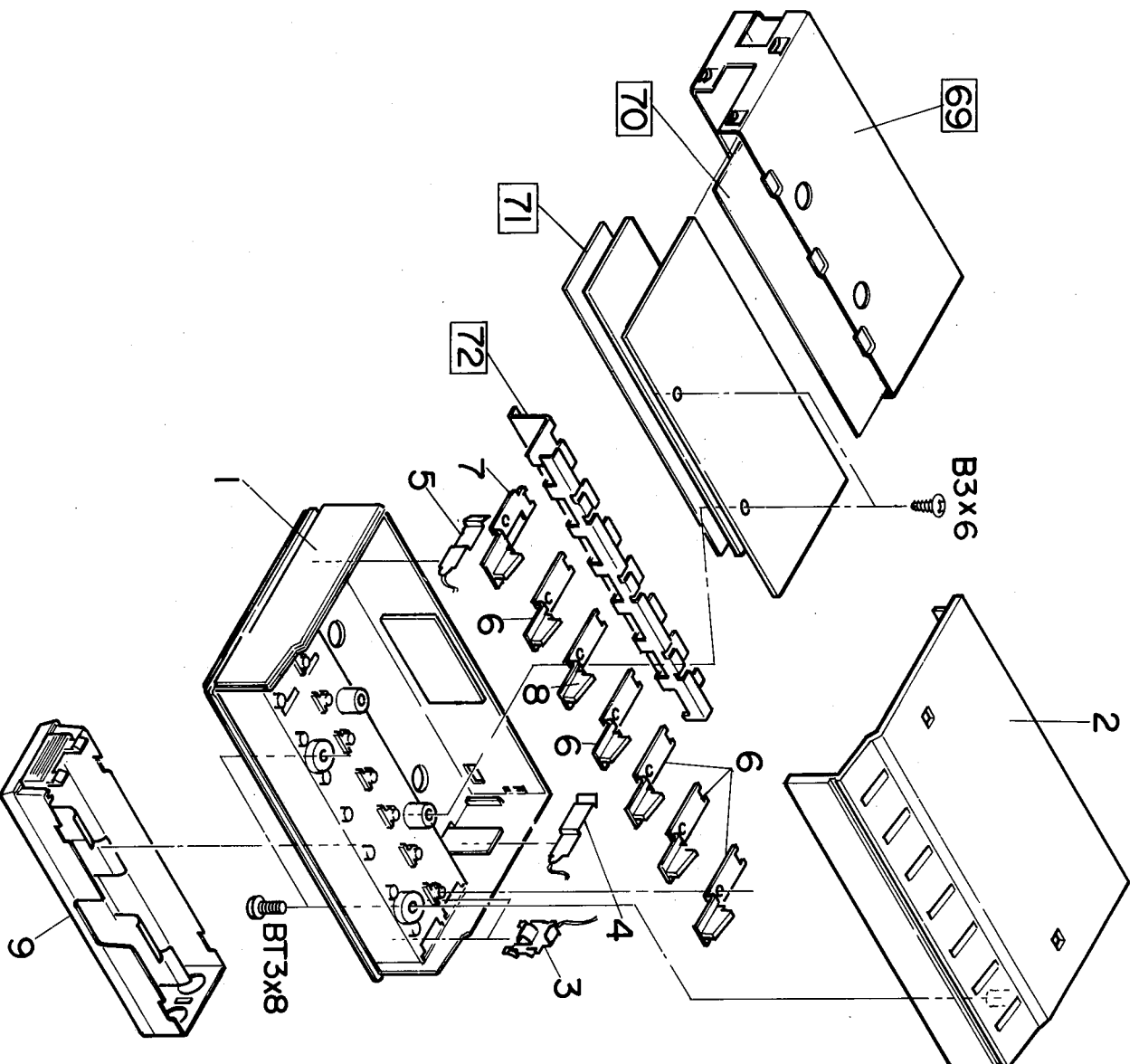
Turn the sensitivity control VR on the receiver side (RV451) gradually clockwise from fully counter-clockwise (viewed from the parts side of the PC Board) to just after the REC mode indicator lamp lights. Press operation buttons other than the REC button of the transmission unit after adjustment is completed to check the corresponding modes operate normally.

(Note)

When the light receiving sensitivity is made larger than required, room illumination and direct light are detected in the normal condition saturating the amplifier circuit, so there is danger that normally receiving signals will become impossible.



EXPLODED VIEW (Remote Control Unit)



Note: Components marked as **number** in this drawing are not specified as replacement parts.

REPLACEMENT PARTS

SYMBOL-NO	P-NO	DESCRIPTION	SYMBOL-NO	P-NO	DESCRIPTION
MISCELLANEOUS					
1	6032112	REMOTE CONTROL CASE ASSEMBLY	6	6051231	PUSH BUTTON ASSEMBLY
2	6671412	REMOTE CONTROL METAL	7	6051232	PUSH BUTTON ASSEMBLY
3	7451001	BATTERY TERMINAL	8	6051233	PUSH BUTTON ASSEMBLY
4	7451011	TERMINAL	9	6488226	BATTERY CASE ASSEMBLY
5	7451012	TERMINAL			

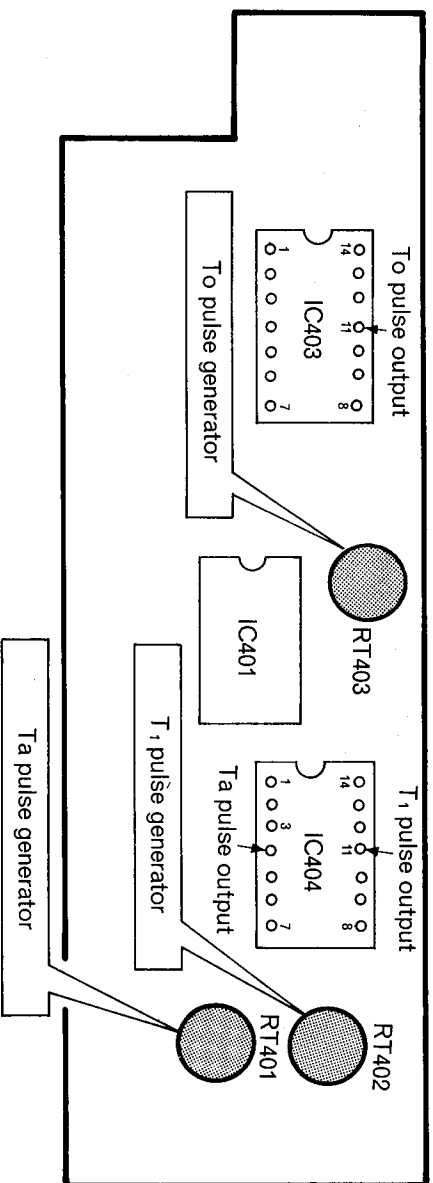


Fig. 94

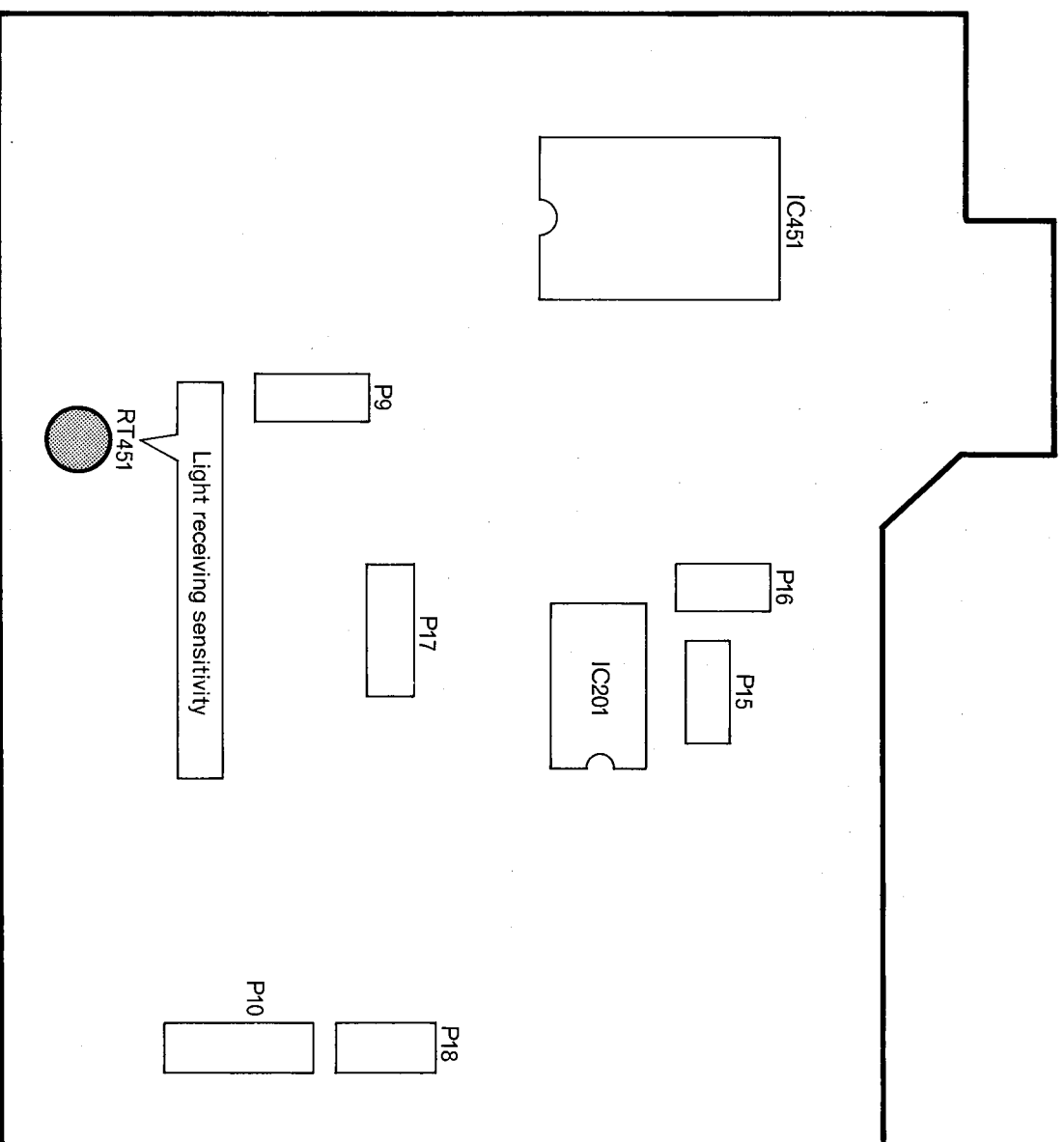


Fig. 95

Mode Control PC board

SYMBOL-NO	P-NO	DESCRIPTION	SYMBOL-NO	P-NO	DESCRIPTION
FOR CASSETTE DECK ASSFMBLY (B)			38	7451021	BATTERY TERMINAL
10	6051211	PUSH BUTTON (METER)	39	7451022	BATTERY TERMINAL
11	6222033	METER FRAME ASSEMBLY	40	6751811	SLIDE GUIDE
12	7769072	KNOB BLIND	41	6751812	SLIDE GUIDE
13	6309991	SPRING FOR METER PANEL	42	6631081	HEAD COVER
14	5552104	COUNTER	43	6630992	CASSETTE METAL ASSEMBLY
15	6669133	COUNTER CAP	44	6711352	BUSHING (BS)
16	6351053	COUNTER BELT		0043793	BUSHING (U,C,W,FS)
17	6040472	BACK COVER (U)	MISCELLANEOUS		
	6040473	BACK COVER (C)	45	6671593	FRONT PANEL ASSEMBLY
	6040475	BACK COVER (FS)	46	6630843	BUTTON (TEST,MANUAL)
	6040476	BACK COVER (W)	47	6751761	SPRING SUPPORT
	6040477	BACK COVER (BS)	48	6630844	BUTTON
18	7309021	MAIN JACK COVER (U,C)	49	6304645	SPRING
	7309022	MAIN JACK COVER (W,FS,BS)	50	6050841	PUSH BUTTON
19	7308901	SUB JACK COVER	51	6304881	BUTTON SPRING
20	6795151	RIVET	52	6051241	PUSH BUTTON ASSEMBLY (POWER)
21	6050592	SHAFT SUPPORT	53	6051221	EJECT BUTTON
22	6050541	KNOB (W,FS,BS)	54	6304452	BUTTON SPRING
23	6488342	BATTERY BOX	55	6532321	BUTTON SPRING
24	6040501	BATTERY COVER	56	6796531	FUNCTION KNOB
25	6360012	SCREW	57	6287541	KNOB ASSEMBLY (RECORD L)
26	6337301	CIRCUIT BOARD HINGE	58	6289161	KNOB ASSEMBLY (RECORD R)
27	6751881	CIRCUIT BOARD SUPPORT	59	6287551	KNOB ASSEMBLY (OUTPUT)
28	7294162	CLIP	60	6040427	UPPER COVER (W,FS,BS)
29	6322501	PRESSURE RETURN SPRING		6040425	UPPER COVER (U,C)
30	6325263	SPRING	61	6040413	BOTTOM COVER
31	6325262	SPRING	62	6796122	FELT LEG
32	6751871	LIGHT DETECTION CAP	63	6671404	CASSETTE DOOR METAL
33	6631771	LIGHT DETECTOR PANEL ASSEMBLY	64	7781395	SPECIAL BOLT
34	6342262	SPRING	65	6690362	SPECIAL SCREW
35	6342221	LEVER RETURN SPRING	66	6587131	RUBBER FOR PANEL
36	6532272	LEAF SPRING	67	6959322	CASSETTE PANEL
37	6320571	CHASSIS LOCK ARM SPRING	68	6560113	CASSETTE HOLDER

SYMBOL-NO	P-NO	DESCRIPTION	SYMBOL-NO	P-NO	DESCRIPTION
CAPACITORS			D103LR	5330572	DIODE SILICON 1S2473HC 100M
C 1	0256570	ELECTROLYTIC 2.2MF 25V	D104LR	5330721	DIODE GERMANIUM 1N34A 10MHZ 50MW
CR	0219902	CR PACK 120 OHM 0.0033MF 450V (U)	D105LR	5330721	DIODE GERMANIUM 1N34A 10MHZ 50MW
CR	0219907	CR PACK (C)	D106LR	5330721	DIODE GERMANIUM 1N34A 10MHZ 50MW
RESISTORS			D107LR	5330721	DIODE GERMANIUM 1N34A 10MHZ 50MW
RT 1	0151885	VARIABLE RESISTOR 4.7KOHM B	D108	5340022	VARISTOR SILICON HV-46 10K
RT 21LR	0151886	VARIABLE RESISTOR 10KOHM B	D109	5340022	VARISTOR SILICON HV-46 10K
RT 22LR	0151886	VARIABLE RESISTOR 10KOHM B	D110	5330721	DIODE GERMANIUM 1N34A 10MHZ 50MW
RT101LR	0151886	VARIABLE RESISTOR 10KOHM B	D111	5330572	DIODE SILICON 1S2473HC 100M
RT102LR	0151887	VARIABLE RESISTOR 22KOHM B	D112	5330341	RECTIFIER SILICON W0-6A 60H
RT103LR	0151886	VARIABLE RESISTOR 10KOHM B	D113	5330131	DIODE 1S2076
RT104LR	0151884	VARIABLE RESISTOR 2.2KOHM B	D201-208	5330101	RECTIFIER SILICON V06C 15K
RT401-403	0151891	SEMI VARIABLE RESISTOR	D209	5330372	RECTIFIER SILICON SV02A 60H
RT451	0151882	VARIABLE RESISTOR 470 OHM	D210	5330371	RECTIFIER SILICON SV01A 60H
RV 21	5000551	VARIABLE 20KOHM(A)	D213	5330572	DIODE SILICON 1S2473HC 100M
RV 22	5000551	VARIABLE 20KOHM(A)	D214	5330101	RECTIFIER SILICON V06C 15K
RV101	5000145	VARIABLE 10KOHM(B)	D215	5330101	RECTIFIER SILICON V06C 15K
RV501	0151885	VARIABLE RESISTOR 4.7KOHM B	D216-225	5330572	DIODE SILICON 1S2473HC 100M
RV502	0151885	VARIABLE RESISTOR 4.7KOHM B	D228	5330572	DIODE SILICON 1S2473HC 100M
RV503	0151890	VARIABLE RESISTOR 220KOHM B	D229	5330572	DIODE SILICON 1S2473HC 100M
RV504	0151889	SEMI VARIABLE RESISTOR 100K OHMB	D230-234	5330572	DIODE SILICON 1S2473HC 100M
RV506	0151889	SEMI VARIABLE RESISTOR 100K OHMB	D235	5330131	DIODE 1S2076
RV508	0151889	SEMI VARIABLE RESISTOR 100K OHMB	D236	5330101	RECTIFIER SILICON V06C 15K
RV751	0151886	VARIABLE RESISTOR 10KOHM B	D237	5330101	RECTIFIER SILICON V06C 15K
RV752	0151886	VARIABLE RESISTOR 10KOHM B	D238	5330131	DIODE 1S2076
RV851	0151880	SEMI VARIABLE RESISTOR 100OHM(B)	D239	5330341	RECTIFIER SILICON W0-6A 60H
RV852	0151889	SEMI VARIABLE RESISTOR 100K OHMB	D240	5330131	DIODE 1S2076
RV853	0151884	VARIABLE RESISTOR 2.2KOHM B	D241	5330131	DIODE 1S2076
RV901	0151886	VARIABLE RESISTOR 10KOHM B	D242	5330131	DIODE 1S2076
RV902	0151886	VARIABLE RESISTOR 10KOHM B	D401-403	5330133	DIODE SILICON 1S2076 100MHZ 250MW
R253	0111301	OXIDE METAL FILM 150OHM+-5%	D405	5380311	LED GL520
R262	0169049	WIRE WOUND 220OHM+-5% 2W	D406	5380311	LED GL520
R263	0111278	OXIDE METAL FILM 120OHM+-5%	D407	5330131	DIODE 1S2076
SEMI-CONDUCTORS			D408	5330131	DIODE 1S2076
D 3-5	5330572	DIODE SILICON 1S2473HC 100M	D451	5380321	DIODE PHDI-PD-46PI
D 6	5330131	DIODE 1S2076	D452-454	5330572	DIODE SILICON 1S2473HC 100M
D 21	5330572	DIODE SILICON 1S2473HC 100M			
D 22	5330572	DIODE SILICON 1S2473HC 100M			
D 23	5340022	VARISTOR SILICON HV-46 10K			
D 24LR	5330721	DIODE GERMANIUM 1N34A 10MHZ 50MW			
D 25LR	5330572	DIODE SILICON 1S2473HC 100M			
D101	5340022	VARISTOR SILICON HV-46 10K			
D102LR	5330721	DIODE GERMANIUM 1N34A 10MHZ 50MW			

SYMBOL-NO	P-NO	DESCRIPTION	SYMBOL-NO	P-NO	DESCRIPTION
SEMI-CONDUCTORS			IC402	5359501	IC MPD4011C
D501-509	5330572	DIODE SILICON 1S2473HC 100M	IC403	5359501	IC MPD4011C
D512	5330572	DIODE SILICON 1S2473HC 100M	IC404	5359611	IC MPD4001C
D513	5330572	DIODE SILICON 1S2473HC 100M	IC451	5359722	IC UPD550-025
D514	0575005	DIODE GERMANIUM 1N60 80M	IC501-506	5356901	IC TA4024
D701	5330572	DIODE SILICON 1S2473HC 100M	IC507-510	5356931	IC TA4027
D702	5330101	RECTIFIER SILICON V06C 15K	IC511	5359561	IC HD74164P
D703	5330101	RECTIFIER SILICON V06C 15K	IC512	5356891	IC TA4023
D704	5330572	DIODE SILICON 1S2473HC 100M	IC701	5356931	IC TA4027
D705-707	5330572	DIODE SILICON 1S2473HC 100M	IC702	5356931	IC TA4027
D710-716	5330572	DIODE SILICON 1S2473HC 100M	IC751	5350301	IC HA-1452
D720	5330721	DIODE GERMANIUM 1N34A 10MHZ 50MW	IC752	5350301	IC HA-1452
D721	5330131	DIODE 1S2076	IC753	5356931	IC TA4027
D722	5330131	DIODE 1S2076	IC754	5350601	IC NJM4558D
D724	5330131	DIODE 1S2076	IC755	5356941	IC TA4028
D726-728	5330131	DIODE 1S2076	IC801	5359771	IC HD38643
D729	0575005	DIODE GERMANIUM 1N60 80M	IC802	5359571	IC HM435101P
D730	5330131	DIODE 1S2076	IC851	5359221	IC HD74145P
D751-757	5330572	DIODE SILICON 1S2473HC 100M	IC852	5350301	IC HA-1452
D801-804	5330131	DIODE 1S2076	IC901	5356941	IC TA4028
D806-809	5330572	DIODE SILICON 1S2473HC 100M	IC902	5350601	IC NJM4558D
D810	5330131	DIODE 1S2076	IC903	5356911	IC TA4025
D811	5330131	DIODE 1S2076	IC904	5356921	IC TA4026
D901	5330572	DIODE SILICON 1S2473HC 100M	IC951	5356931	IC TA4027
D902	5330572	DIODE SILICON 1S2473HC 100M	IC952	5356931	IC TA4027
D903	5330131	DIODE 1S2076	Q 2	5321213	TRANSISTOR 2SD468C 190MHZ 0.9MW
D904	5330572	DIODE SILICON 1S2473HC 100M	Q 3	5321203	TRANSISTOR SILICON 2SB562C 350MHZ .9W
D905	5330572	DIODE SILICON 1S2473HC 100M	Q 4	5321213	TRANSISTOR 2SD468C 190MHZ 0.9MW
D906	0575001	DIODE GERMANIUM 1N34A 10M	Q 5	5321203	TRANSISTOR SILICON 2SB562C 350MHZ .9W
D951-957	5330572	DIODE SILICON 1S2473HC 100M	Q 21	5321295	TRANSISTOR 2SC1740E
IC 1	5359651	IC HA1373	Q 22LR	5320024	TRANSISTOR SILICON 2SC458DLG 230M
IC 21LR	5350251	IC HA1406	Q 23LR	5320024	TRANSISTOR SILICON 2SC458DLG 230M
IC 22LR	5350561	IC HA 11226	Q 24LR	5321194	TRANSISTOR 2SD467BC
IC101	5350301	IC HA-1452	Q 25LR	5320024	TRANSISTOR SILICON 2SC458DLG 230M
IC102	5350601	IC NJM4558D	Q101LR	5321506	TRANSISTOR 2SK68A-N
IC201	5350851	IC HA12001	Q102LR	5321194	TRANSISTOR 2SD467BC
IC401	5359621	IC MPD4014C	Q103LR	5321194	TRANSISTOR 2SD467BC
			Q104LR	5320024	TRANSISTOR SILICON 2SC458DLG 230M
			Q105LR	5321194	TRANSISTOR 2SD467BC
			Q106LR	5320613	TRANSISTOR SILICON 2SC1213C 80M
			Q107LR	5321295	TRANSISTOR 2SC1740E
			Q108LR	5321295	TRANSISTOR 2SC1740E

SYMBOL-NO	P-NO	DESCRIPTION	SYMBOL-NO	P-NO	DESCRIPTION
SEMI-CONDUCTORS			Q457-463	5321295	TRANSISTOR 2SC1740E
IC953	5359221	IC HD74145P	Q464	5320613	TRANSISTOR SILICON 2SC1213C 80M
IC954	5359221	IC HD74145P	Q465	5320024	TRANSISTOR SILICON 2SC458DLG 230M
IC955	5359601	IC HD7420P	Q466	5320024	TRANSISTOR SILICON 2SC458DLG 230M
IC956	5356931	IC TA4027	Q467	5321252	TRANSISTOR ZSA844D
LED 21-29	5380241	LED GL 3PR1	Q468-470	5320024	TRANSISTOR SILICON 2SC458DLG 230M
LED 30-32	5380271	LED GL-9PR2	Q471	5320593	TRANSISTOR SILICON 2SA673C 80M
LED 33-35	5380281	LED GL-9PG2	Q501-505	5321294	TRANSISTOR 2SC 1740S
LED 36	5380241	LED GL 3PR1	Q506	5320593	TRANSISTOR SILICON 2SA673C 80M
LED 37-39	5380242	LED GL 3PG1	Q507	5321294	TRANSISTOR 2SC 1740S
LED 40-42	5380242	LED GL 3PG1	Q508	5321294	TRANSISTOR 2SC 1740S
LED 43	5380241	LED GL 3PR1	Q509	5320593	TRANSISTOR SILICON 2SA673C 80M
LED 44	5380241	LED GL 3PR1	Q510-512	5321294	TRANSISTOR 2SC 1740S
LED101-103	5380241	LED GL 3PR1	Q513	5320593	TRANSISTOR SILICON 2SA673C 80M
LED201-205	5380242	LED GL 3PG1	Q514	5321294	TRANSISTOR 2SC 1740S
LED202	5380241	LED GL 3PR1	Q515	5320643	TRANSISTOR SILICON 2SC1162 150M
LED206	5380241	LED GL 3PR1	Q516-519	5320623	TRANSISTOR SILICON 2SC1213A-C 80MH. 400M
LED407	5380271	LED GL-9PR2	Q701	5321294	TRANSISTOR 2SC 1740S
LED701	5380101	RADIATION DIODE SLP-24B	Q702	5321294	TRANSISTOR 2SC 1740S
LED702	5380101	RADIATION DIODE SLP-24B	Q751-754	5321294	TRANSISTOR 2SC 1740S
Q 1	5320064	TRANSISTOR 2SC458D	Q851-853	5321294	TRANSISTOR 2SC 1740S
Q109LR	5321194	TRANSISTOR 2SD467BC	Q901	5321294	TRANSISTOR 2SC 1740S
Q110-115	5321295	TRANSISTOR 2SC1740E	Q902	5321294	TRANSISTOR 2SC 1740S
Q116LR	5320024	TRANSISTOR SILICON 2SC458DLG 230M	Q951	5321294	TRANSISTOR 2SC 1740S
Q201	5320643	TRANSISTOR SILICON 2SC1162 150M	Q952	5320593	TRANSISTOR SILICON 2SA673C 80M
Q202	5320723	TRANSISTOR 2SA715WT-C	Q953	5321294	TRANSISTOR 2SC 1740S
Q203-205	5320671	TRANSISTOR SILICON 2SC1061B 5M	Q954	5321294	TRANSISTOR 2SC 1740S
Q206	5320643	TRANSISTOR SILICON 2SC1162 150M	Q955	5321294	TRANSISTOR 2SC 1740S
Q207	5320671	TRANSISTOR SILICON 2SC1061B 5M	TH701	5340231	THERMISTER 112302-2
Q208	5320643	TRANSISTOR SILICON 2SC1162 150M	ZD101	5330322	DIODE-ZENER SILICON TR-9S 10K
Q209	5320643	TRANSISTOR SILICON 2SC1162 150M	ZD201	5330392	ZENER DIODE SILICON HZ6B 1MHZ 400M
Q210	5321295	TRANSISTOR 2SC1740E	ZD202	5330311	DIODE SILICON HZ7A 1.0M
Q211	5321295	TRANSISTOR 2SC1740E	ZD203	5330392	ZENER DIODE SILICON HZ6B 1MHZ 400M
Q212-215	5321213	TRANSISTOR 2SD468C 190MHZ 0.9MW	ZD204	5330056	ZENNER DIODE AW01-20
Q216-221	5321295	TRANSISTOR 2SC1740E	ZD205	5330541	ZENER DIODE HZ-15
Q401	5320064	TRANSISTOR 2SC458D	ZD206	5330483	ZENNER DIODE AW01-7
Q402	5320593	TRANSISTOR SILICON 2SA673C 80M	ZD207	5330483	ZENNER DIODE AW01-7
Q403	5321213	TRANSISTOR 2SD468C 190MHZ 0.9MW	ZD208	5330322	DIODE-ZENER SILICON TR-9S 10K
Q404	5321252	TRANSISTOR ZSA844D	ZD451	5330552	ZENNER DIODE HZ11B
Q451	5321501	TRANSISTOR 2SK68			
Q452-455	5320024	TRANSISTOR SILICON 2SC458DLG 230M			
Q456	5321252	TRANSISTOR ZSA844D			

SYMBOL-NO	P-NO	DESCRIPTION	SYMBOL-NO	P-NO	DESCRIPTION
TRANSFORMERS			J 1	5651141	5P DIN SOCKET
PT	5212234	POWER TRANSFORMER (U,C)	J 2LR	5676211	US PIN JACK (2P)
PT	5212501	POWER TRANSFORMER (FS)	J 3LR	5676211	US PIN JACK (2P)
PT	5212502	POWER TRANSFORMER (BS)	J 6LR	5676212	US PIN JACK (4P)
PT	5212503	POWER TRANSFORMER (W)	J 7	5676212	US PIN JACK (4P)
COILS			J 8	5651141	5P DIN SOCKET (W,FS,BS)
L102LR	5120274	CHOKO COIL	LC 21LR	5161662	DOLBY FILTER
L301	0333151	PEAKING COIL 36MH	LC101LR	5161662	DOLBY FILTER
L401	5150821	CHOKO 18MICROH	LM	5554681	LEVEL METER (BIAS)
L451	5260215	TRAP COIL 33HH	LM	5554682	LEVEL METER (EQ)
L501	5260361	CHOKO COIL 33MH	LM	5554691	LEVEL METER
L502	5260361	CHOKO COIL 33MH	PL101	5762036	PILOT LAMP
L503-505	5260215	TRAP COIL 33HH	PL201	5765022	LAMP
L506	5260022	OSCILLATOR COIL	RL21	5641141	LEAD RELAY
L507	5260022	OSCILLATOR COIL	RL701	5641201	RELAY
L508LR	5260215	TRAP COIL 33HH	S 1	5604214	LEVER SWITCH
RL501	5641141	LEAD RELAY	S 2	5604232	LEVER SWITCH
RL502	5641141	LEAD RELAY	S 5-7	5634235	PUSH SWITCH
MISCELLANEOUS			S 13	5634112	PUSH SWITCH
	5391001	HALL ELEMENT	S 14	5633311	PUSH SWITCH (W,FS,BS)
	5674171	MIC JACK	S 15-22	5633351	PUSH SWITCH
	5674181	HEADPHONE JACK	S 23	5634112	PUSH SWITCH
	5746157	POWER CORD (W,FS)	S201	5633271	POWER SWITCH (W,FS,BS)
	5746291	POWER CORD ASS'Y (BS)	S201	5633272	PUSH SWITCH (U,C)
	5746441	POWER CORD (U,C)	S202	5605081	ROTARY SWITCH (W)
CE0451	5780501	CERAMIC OSCILLATOR DEVICE	S401-407	5633351	PUSH SWITCH
F 1	5720173	FUSE 250V 500MAT	S408	5632713	LEAF SWITCH
F 2	5720174	FUSE 630MA	FOR ACCESSORIES		
F 3	5720175	FUSE 0.8A		5662021	SOCKET ADAPTER (W)
F 4	5721042	FUSE (1.25A)		7740321	HEAD CLEANING STICK
F 5	5720175	FUSE 0.8A		5896371	PATCH CORD (U,C,BS)
F 6	5720173	FUSE 250V 500MAT (W,BS)		5744843	DIN CORD (W,FS)



HITACHI SALES CORPORATION OF AMERICA

Eastern Regional Office

1200 Wall Street West, Lyndhurst, New Jersey 07071
Tel. 201-935-8980

Mid-Western Regional Office

1400 Morse Ave., Elk Grove Village, Ill. 60007
Tel. 312-593-1550

Southern Regional Office

510 Plaza Drive College Park, Georgia 30349
Tel. 404-763-0360

Western Regional Office

401 West Artesia Boulevard, Compton, California 90220
Tel. 213-537-8383

HITACHI SALES CORPORATION OF HAWAII, INC

743-G Waiakamilo Rd., Honolulu, Hawaii 96817
Tel. 808-841-0431

HITACHI SALES CORP. OF CANADA Ltd.

3300 Trans Canada Highway Pointe Claire, Quebec, H9R1B1, Canada
Tel. 514-697-9150

HITACHI SALES EUROPA GmbH

2 Hamburg 54, Kleine Bahnstraße 8, West Germany
Tel. 850 60 71-75

HITACHI SALES (U.K.) Ltd.

Hitachi House, Station Road, Hayes, Middlesex UB3 4DR, England
Tel. 01-848-8787 (Service Centre : 01-848-3551)

HITACHI SALES SCANDINAVIA AB

Rissneleden 8, Sundbyberg, Box 7138, S-172-07 Sundbyberg 7,
Sweden
Tel. 08-98 52 80

HITACHI SALES NORWAY A/S

Oerebekk 1620 Gressvik P.O. Box 46 N-1601 Fredrikstad, Norway
Tel. 032-28050

SUOMEN HITACHI OY

Box 151, SF-15100 Lahti 10, Finland
Tel. Lahti 44 241

HITACHI SALES A/S

Kuldysen 13, DK-2630 Taastrup, Denmark
Tel. 02-999200

HITACHI SALES A.G.

5600 Lenzburg, Switzerland
Tel. 064-513621

HITACHI-FRANCE (Radio-Télévision Electro-Ménager) S.A.

9, Boulevard Ney 75018, Paris, France
Tel. 201-25-00

HITACHI SALES WARENHANDELS GMBH

A-1180/Wien, Kreuzgasse 27
Tel. (0043222) 439367/8

HITACHI SALES AUSTRALIA Pty Ltd.

153 Keys Road, Moorabbin, Victoria 3189 Australia
Tel. 95-8722

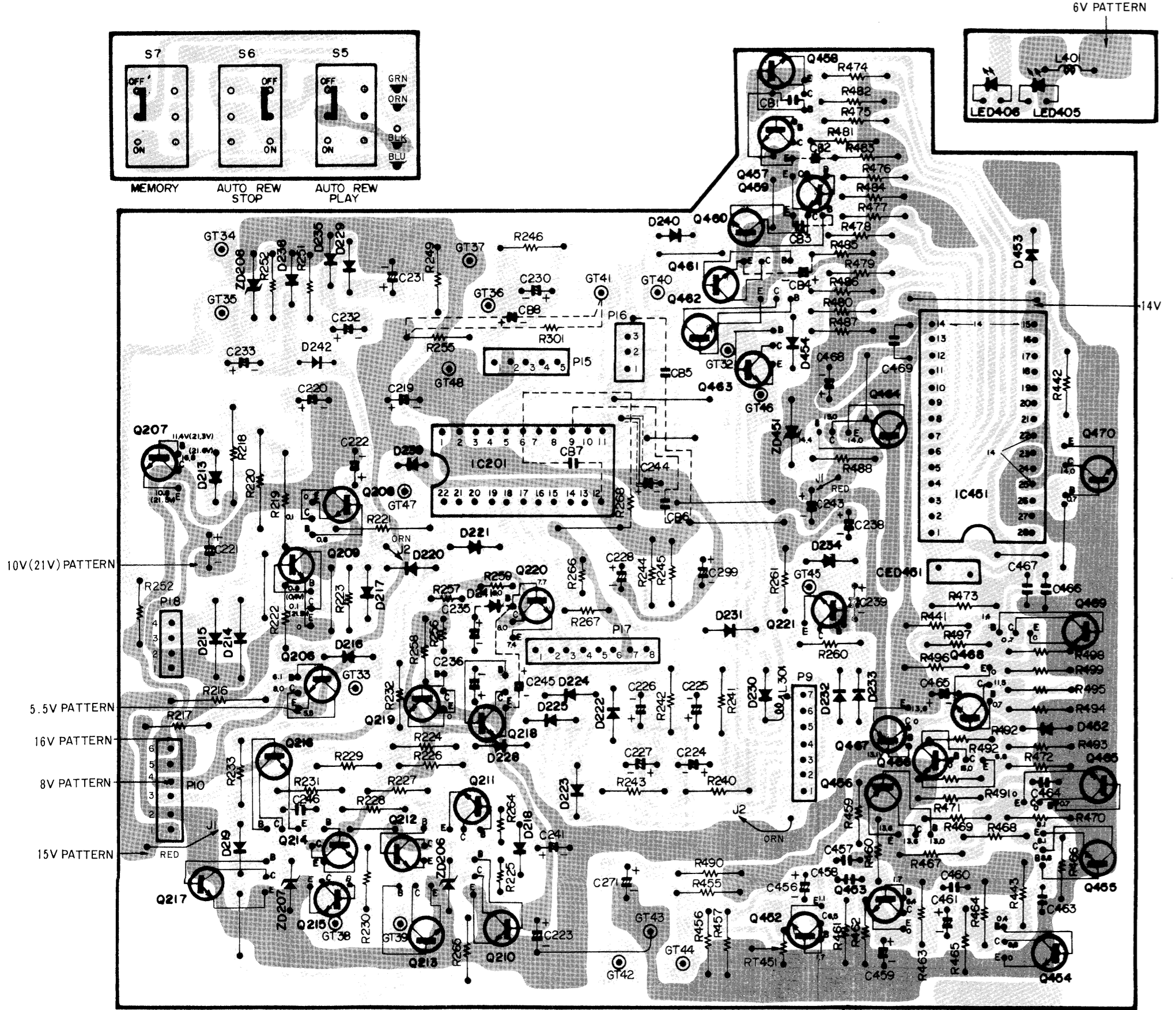
HITACHI Ltd. TOKYO JAPAN

Head Office : 5-1, 1-chome, Marunouchi, Chiyoda-ku, Tokyo
Tel. Tokyo (212) 1111 (80 lines)

Cable Address : "HITACHY" TOKYO

Codes : All Codes Used

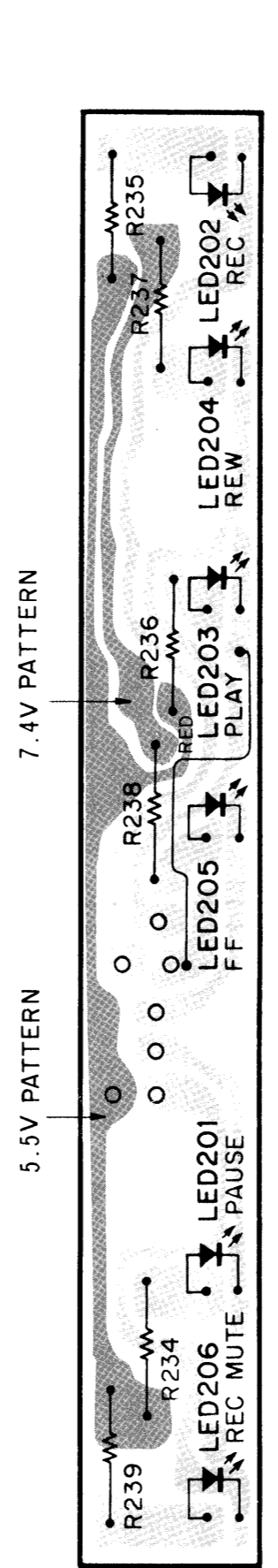
Mode Control P.C.B.



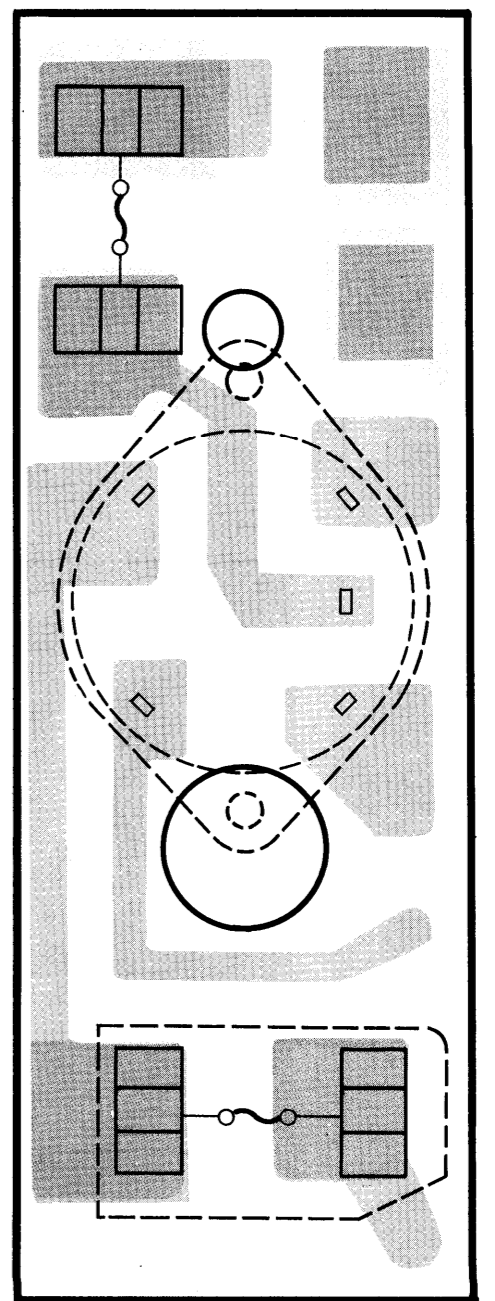
() INDICATE VOLTAGE AT A TIME OF STOP.

CB1 TO CB8 INDICATE CAPACITANCE WITH PATTERN SIDE SOLDERED.

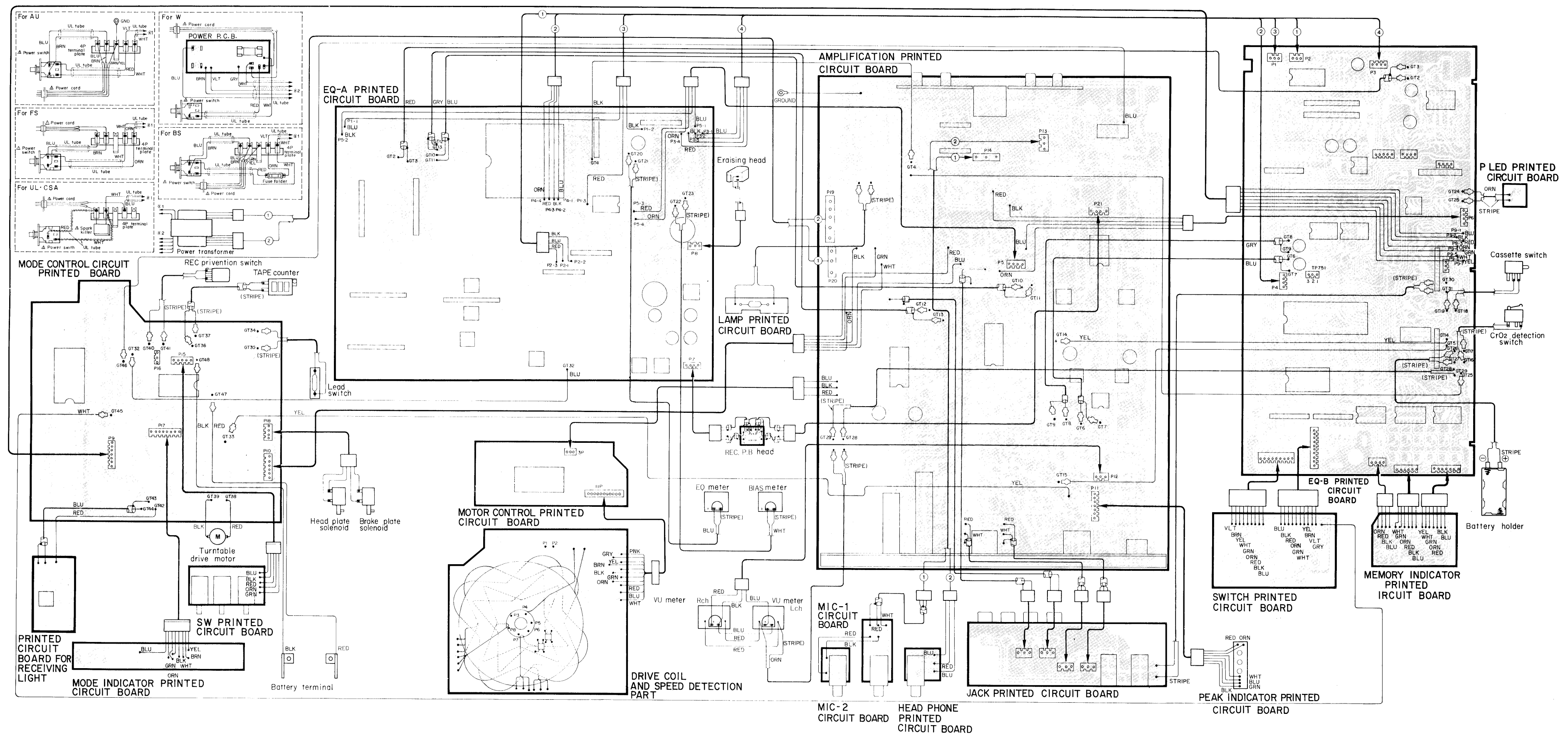
Mode Indicator P.C.B.



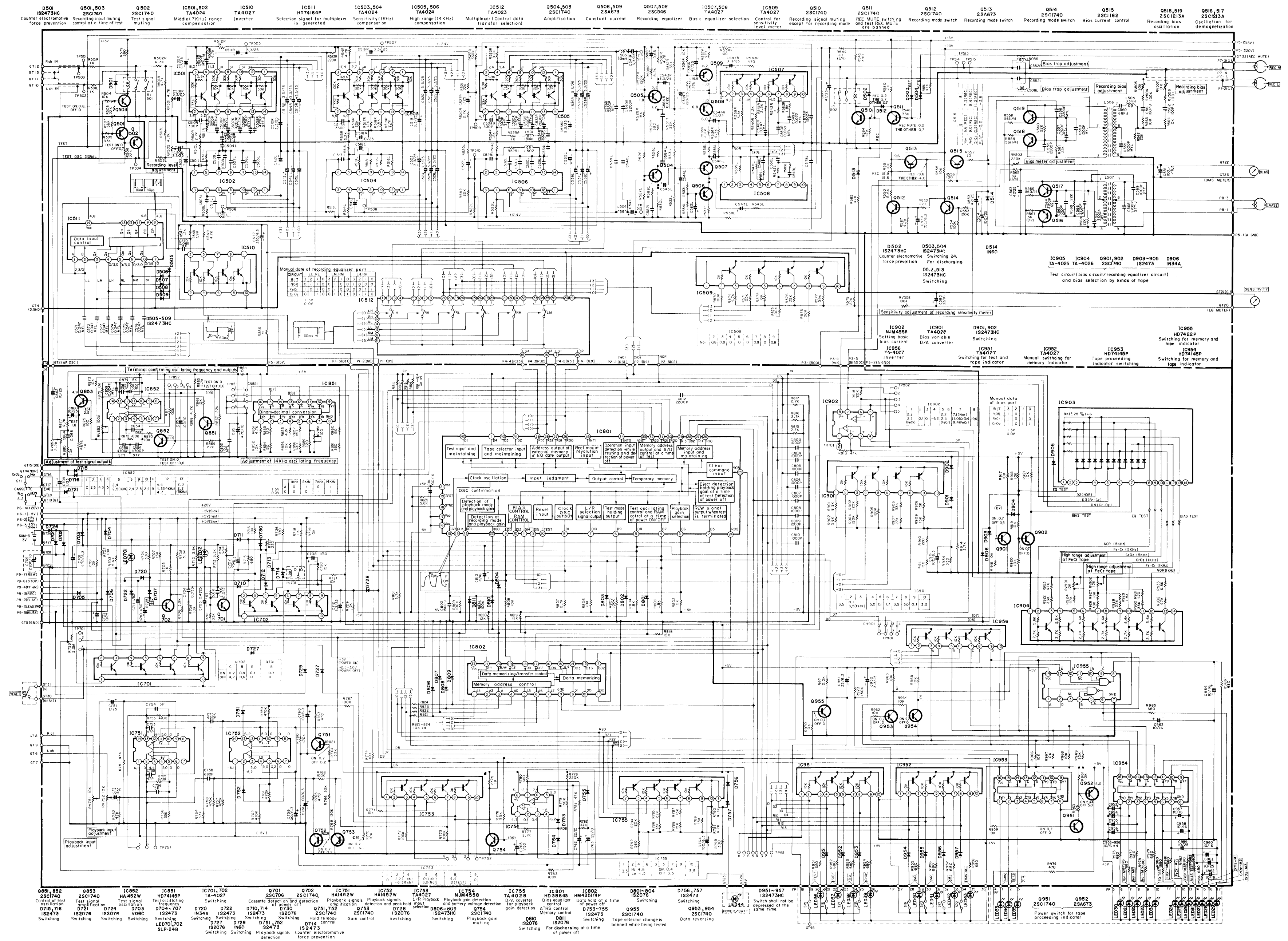
Power P.C.B. (For W)



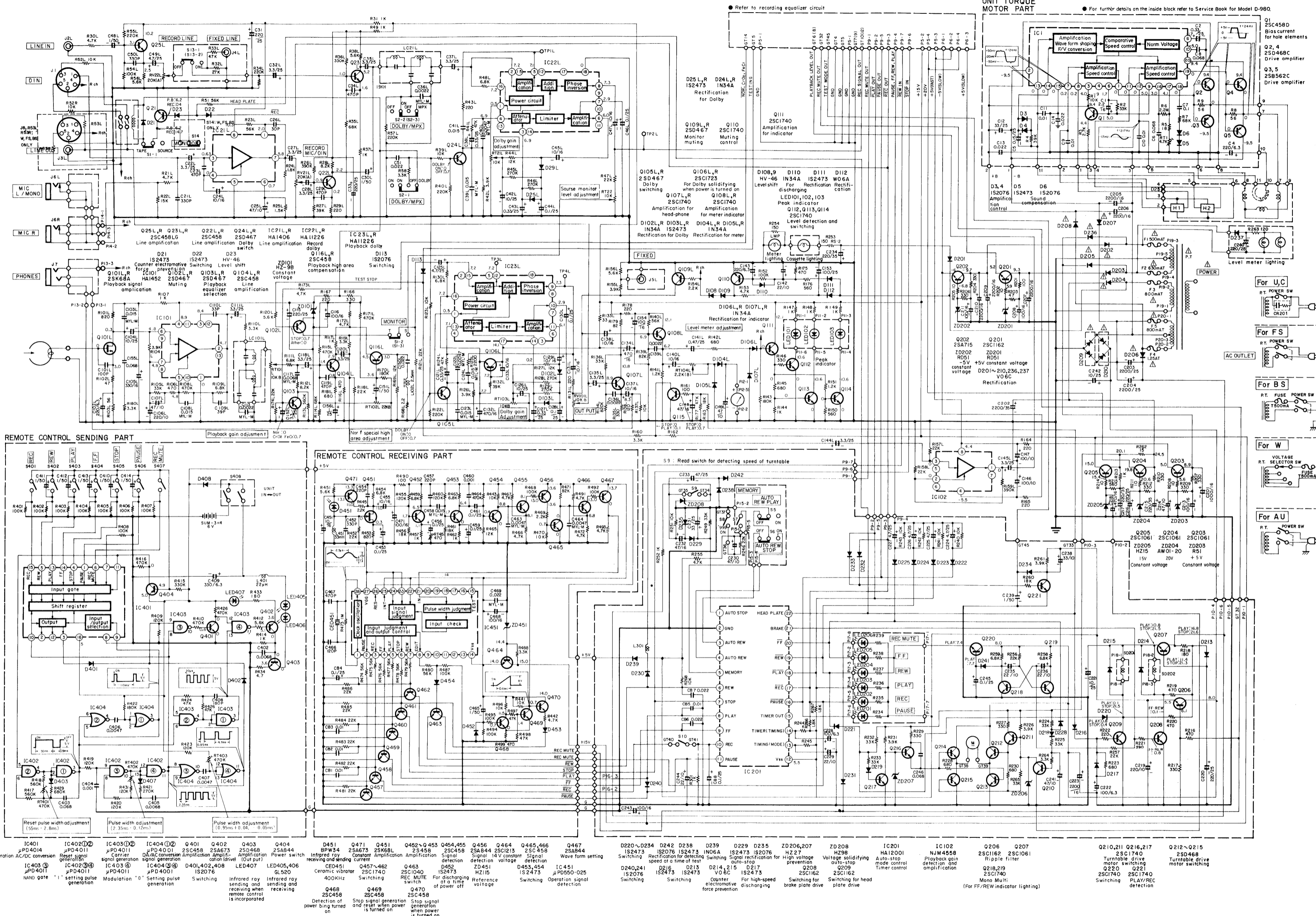
WIRING DIAGRAM



SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



- | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-------|
| IC401 | IC402 | IC403 | IC404 | Q401 | Q402 | Q403 | Q404 | Q405 | Q406 | Q407 | Q408 | Q409 | Q410 | Q411 | Q412 | Q413 | Q414 | Q415 | Q416 | Q417 | Q418 | Q419 | Q420 | Q421 | Q422 | Q423 | Q424 | Q425 | Q426 | Q427 | Q428 | Q429 | Q430 | Q431 | Q432 | Q433 | Q434 | Q435 | Q436 | Q437 | Q438 | Q439 | Q440 | Q441 | Q442 | Q443 | Q444 | Q445 | Q446 | Q447 | Q448 | Q449 | Q450 | Q451 | Q452 | Q453 | Q454 | Q455 | Q456 | Q457 | Q458 | Q459 | Q460 | Q461 | Q462 | Q463 | Q464 | Q465 | Q466 | Q467 | Q468 | Q469 | Q470 | Q471 | Q472 | Q473 | Q474 | Q475 | Q476 | Q477 | Q478 | Q479 | Q480 | Q481 | Q482 | Q483 | Q484 | Q485 | Q486 | Q487 | Q488 | Q489 | Q490 | Q491 | Q492 | Q493 | Q494 | Q495 | Q496 | Q497 | Q498 | Q499 | Q500 | Q501 | Q502 | Q503 | Q504 | Q505 | Q506 | Q507 | Q508 | Q509 | Q510 | Q511 | Q512 | Q513 | Q514 | Q515 | Q516 | Q517 | Q518 | Q519 | Q520 | Q521 | Q522 | Q523 | Q524 | Q525 | Q526 | Q527 | Q528 | Q529 | Q530 | Q531 | Q532 | Q533 | Q534 | Q535 | Q536 | Q537 | Q538 | Q539 | Q540 | Q541 | Q542 | Q543 | Q544 | Q545 | Q546 | Q547 | Q548 | Q549 | Q550 | Q551 | Q552 | Q553 | Q554 | Q555 | Q556 | Q557 | Q558 | Q559 | Q560 | Q561 | Q562 | Q563 | Q564 | Q565 | Q566 | Q567 | Q568 | Q569 | Q570 | Q571 | Q572 | Q573 | Q574 | Q575 | Q576 | Q577 | Q578 | Q579 | Q580 | Q581 | Q582 | Q583 | Q584 | Q585 | Q586 | Q587 | Q588 | Q589 | Q590 | Q591 | Q592 | Q593 | Q594 | Q595 | Q596 | Q597 | Q598 | Q599 | Q600 | Q601 | Q602 | Q603 | Q604 | Q605 | Q606 | Q607 | Q608 | Q609 | Q610 | Q611 | Q612 | Q613 | Q614 | Q615 | Q616 | Q617 | Q618 | Q619 | Q620 | Q621 | Q622 | Q623 | Q624 | Q625 | Q626 | Q627 | Q628 | Q629 | Q630 | Q631 | Q632 | Q633 | Q634 | Q635 | Q636 | Q637 | Q638 | Q639 | Q640 | Q641 | Q642 | Q643 | Q644 | Q645 | Q646 | Q647 | Q648 | Q649 | Q650 | Q651 | Q652 | Q653 | Q654 | Q655 | Q656 | Q657 | Q658 | Q659 | Q660 | Q661 | Q662 | Q663 | Q664 | Q665 | Q666 | Q667 | Q668 | Q669 | Q670 | Q671 | Q672 | Q673 | Q674 | Q675 | Q676 | Q677 | Q678 | Q679 | Q680 | Q681 | Q682 | Q683 | Q684 | Q685 | Q686 | Q687 | Q688 | Q689 | Q690 | Q691 | Q692 | Q693 | Q694 | Q695 | Q696 | Q697 | Q698 | Q699 | Q700 | Q701 | Q702 | Q703 | Q704 | Q705 | Q706 | Q707 | Q708 | Q709 | Q710 | Q711 | Q712 | Q713 | Q714 | Q715 | Q716 | Q717 | Q718 | Q719 | Q720 | Q721 | Q722 | Q723 | Q724 | Q725 | Q726 | Q727 | Q728 | Q729 | Q730 | Q731 | Q732 | Q733 | Q734 | Q735 | Q736 | Q737 | Q738 | Q739 | Q740 | Q741 | Q742 | Q743 | Q744 | Q745 | Q746 | Q747 | Q748 | Q749 | Q750 | Q751 | Q752 | Q753 | Q754 | Q755 | Q756 | Q757 | Q758 | Q759 | Q760 | Q761 | Q762 | Q763 | Q764 | Q765 | Q766 | Q767 | Q768 | Q769 | Q770 | Q771 | Q772 | Q773 | Q774 | Q775 | Q776 | Q777 | Q778 | Q779 | Q780 | Q781 | Q782 | Q783 | Q784 | Q785 | Q786 | Q787 | Q788 | Q789 | Q790 | Q791 | Q792 | Q793 | Q794 | Q795 | Q796 | Q797 | Q798 | Q799 | Q800 | Q801 | Q802 | Q803 | Q804 | Q805 | Q806 | Q807 | Q808 | Q809 | Q810 | Q811 | Q812 | Q813 | Q814 | Q815 | Q816 | Q817 | Q818 | Q819 | Q820 | Q821 | Q822 | Q823 | Q824 | Q825 | Q826 | Q827 | Q828 | Q829 | Q830 | Q831 | Q832 | Q833 | Q834 | Q835 | Q836 | Q837 | Q838 | Q839 | Q840 | Q841 | Q842 | Q843 | Q844 | Q845 | Q846 | Q847 | Q848 | Q849 | Q850 | Q851 | Q852 | Q853 | Q854 | Q855 | Q856 | Q857 | Q858 | Q859 | Q860 | Q861 | Q862 | Q863 | Q864 | Q865 | Q866 | Q867 | Q868 | Q869 | Q870 | Q871 | Q872 | Q873 | Q874 | Q875 | Q876 | Q877 | Q878 | Q879 | Q880 | Q881 | Q882 | Q883 | Q884 | Q885 | Q886 | Q887 | Q888 | Q889 | Q890 | Q891 | Q892 | Q893 | Q894 | Q895 | Q896 | Q897 | Q898 | Q899 | Q900 | Q901 | Q902 | Q903 | Q904 | Q905 | Q906 | Q907 | Q908 | Q909 | Q910 | Q911 | Q912 | Q913 | Q914 | Q915 | Q916 | Q917 | Q918 | Q919 | Q920 | Q921 | Q922 | Q923 | Q924 | Q925 | Q926 | Q927 | Q928 | Q929 | Q930 | Q931 | Q932 | Q933 | Q934 | Q935 | Q936 | Q937 | Q938 | Q939 | Q940 | Q941 | Q942 | Q943 | Q944 | Q945 | Q946 | Q947 | Q948 | Q949 | Q950 | Q951 | Q952 | Q953 | Q954 | Q955 | Q956 | Q957 | Q958 | Q959 | Q960 | Q961 | Q962 | Q963 | Q964 | Q965 | Q966 | Q967 | Q968 | Q969 | Q970 | Q971 | Q972 | Q973 | Q974 | Q975 | Q976 | Q977 | Q978 | Q979 | Q980 | Q981 | Q982 | Q983 | Q984 | Q985 | Q986 | Q987 | Q988 | Q989 | Q990 | Q991 | Q992 | Q993 | Q994 | Q995 | Q996 | Q997 | Q998 | Q999 | Q1000 |
|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-------|