

SERVICE GUIDE

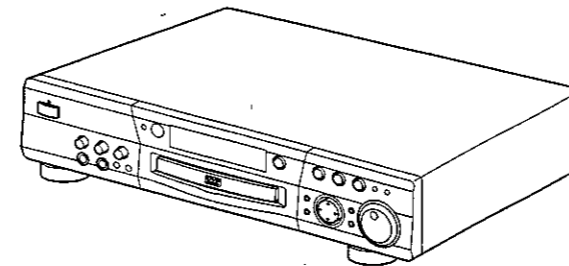
DV-K2

**DVD
PLAYER**

Marketed in July 1998
DVD
No.B002

ADVICE

Please carefully read this guide before using the device. The Hitachi DVD Player has been designed to prevent fire, electrical shock, injury, or harmful radiation. It has been legally fabricated in accordance with the Electrical Appliances Act. Therefore, when using the device, please follow advice in this service guide to keep it safe to use.



1. In brief

DV-K2 is a device for DVD playback.
This device is to be used by connecting it to the video input terminal of a TV set.

2. Features

- ▶ Disc navigation system facilitates program search.
- ▶ Speedy operation by 2x speed drive.
- ▶ Equipped with 2 mike input Karaoke

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Specifications may be changed as improvements are made without advance notice. The marked price does not include consumption tax.

HITACHI





PRECAUTIONS FOR SAFETY (Please follow.)

Before undertaking repair work, please read through this [Precautions for safety].
The following points should be observed in order to prevent accidents from happening and to ensure the safety of the device.

- Degrees of danger or damage that can be caused by faulty operation are indicated by the following marks:

| | |
|--|---|
|  WARNING | Under this mark, there is "Possible death or serious injury". |
|  CAUTION | Under this mark, there is "Possible injury or material damage". |

- The following marks identify actions to be taken:

| | | | |
|---|--|---|---|
|  | This mark indicates items to which 'You should pay attention'. |  | This mark indicates items 'You have to accomplish'. |
|  | This mark indicates: 'You should be cautious of electric shock'. |  | This mark indicates 'Forbidden items'. |

WARNING

You should pay attention.

Where a special attention is required, it is indicated by a label or stamp. For example, on the cabinet, chassis, or parts.
Please respect the indicated items and the 'Precautions for use' of the manual.

You should be cautious against electric shock.

Please be careful during operations because there are high voltage and recharging parts inside. An electric shock or death may happen by touching them.
When disassembling, assembling, or replacing a part, the power plug has to be pulled off.
Touching by error a powered part may cause an electric shock, death, or injury.

Please use designated parts.

Parts are characterized by unflammability and voltage resistance. Therefore, parts having these same characteristics must be used in replacement.
Especially for parts important in insuring safety, identified by Δ in the wiring diagram or parts list, a part with the identical part number shall be used.
If a part with a different part number is used, an electric shock or a fire may occur.

The original part installation and wiring route shall be restored.

For safety, some parts are insulated by a tube or a tape, or installed without contact with substrate. The internal wiring is kept a distance from hot or high voltage parts by clamps or routing. Please restore them as initially done to prevent electric shock or fire from happening.

Please check safety after servicing.

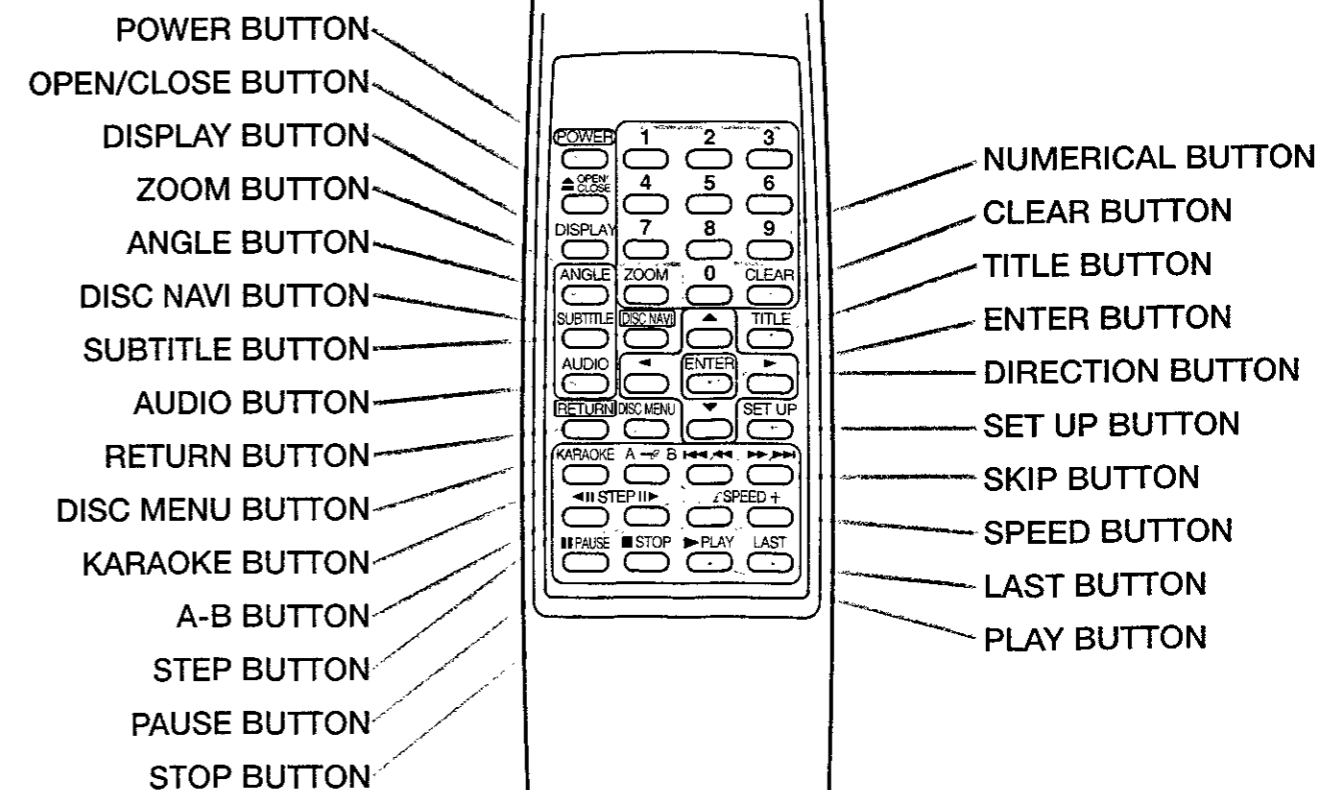
Please check if dismantled screws, parts, and wires are reinstalled as before and if the area surrounding the repair is damaged. Please also measure insulation resistance with a ohmmeter and to confirm that it is more than 1M Ω .
There is risk of electric shock or fire if the insulation resistance is less than 1M Ω .

3. Specification

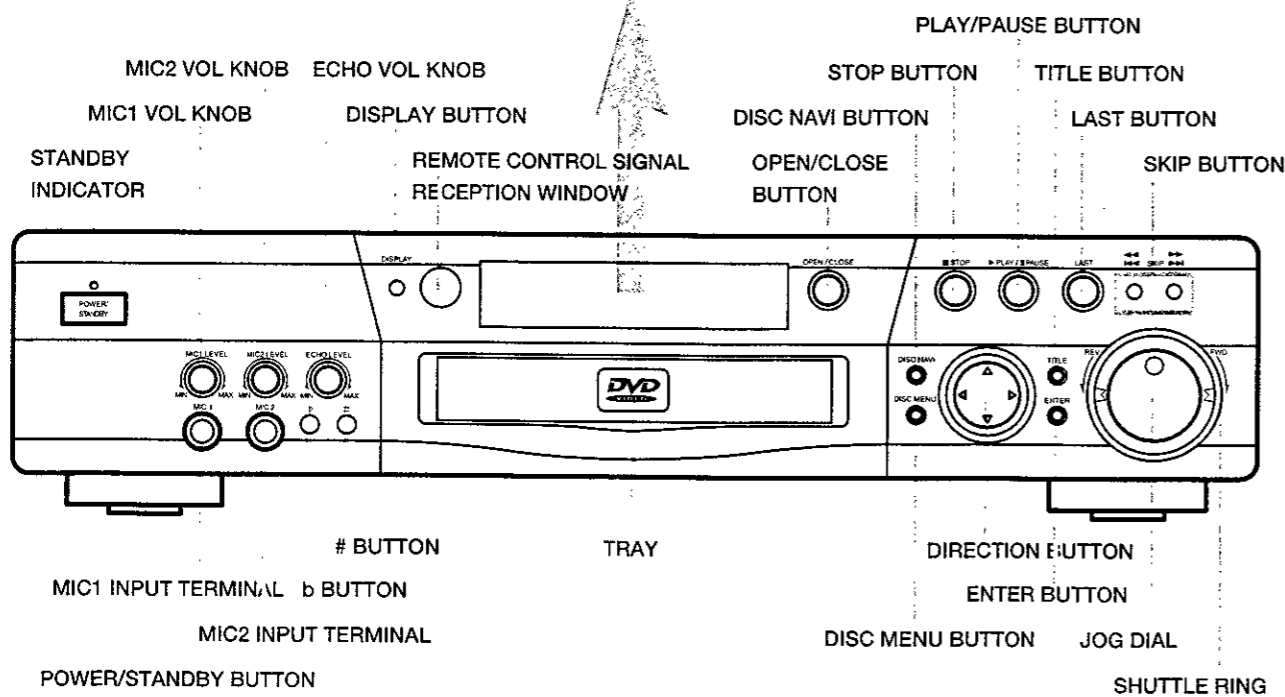
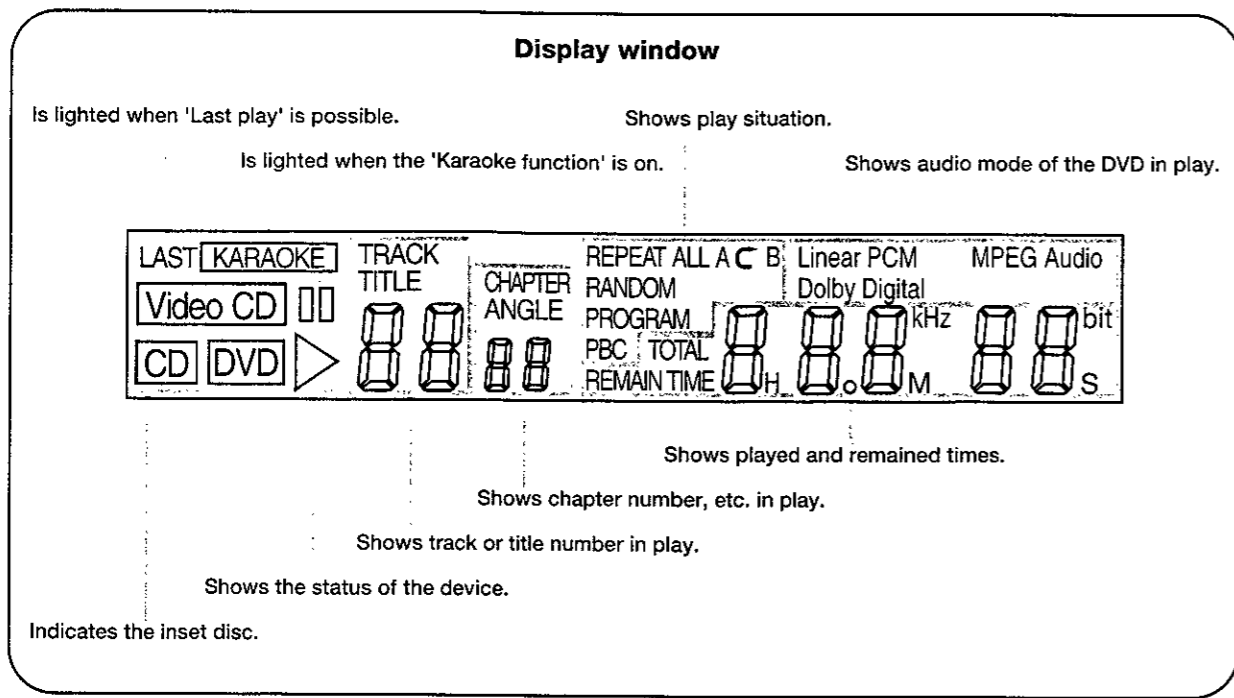
| Common | | | |
|--|--|---------------------------------------|--|
| Model | DV-K2 | Mass | 4.1 kg |
| Laser type | Semiconductor laser | Overall size | 43.4(W)X31.5(D)X9.8(H)cm |
| Electric energy | Wave length:650nm (DVD), 780nm(CD,VCD) | Allowable operating temperature | +5°C~+35°C |
| Power | AC100V,50/60Hz both 22W | Allowable operating humidity | 15%~75%(without condensation) |
| S image output terminal [1 system] (S2 output) | | | |
| Y output level | 1Vp-p (75 Ω) | Output terminal | S terminal |
| C output level | 286mVp-p (75 Ω) | | |
| Image Output terminal [1 system] | | | |
| Output level | 1Vp-p (75 Ω under load, synchronous negative) | Output terminal | Pin jack |
| Audio output terminal [2 systems] | | | |
| Digital audio output level | 200mVrms(1KHz,-20dB) | Frequency characteristics (continued) | DVD:4Hz~44KHz(96K sampling) |
| Channels | 2 channels | SN ratio | 110dB |
| <Digital audio characteristics> | CD:4Hz~20KHz(EIAJ) | Dynamic range | 100dB |
| Frequency characteristics | DVD:4Hz~22KHz(48K sampling) | Total high frequency distortion rate | 0.003% |
| | | Wow flutter | Measuring limits: less than ($\pm 0.001\%$ W.PEAK) (EIAJ) |
| Other terminals | | | |
| Optical digital output: (Dolby Digital <AC-3>/LPCM,LPCM, may be switched to OFF) optical connector | | | |
| Accessories | | | |
| Remote control (DV-RM2) | 1 | AV cord | 1 |
| Single3 type battery (R6P) | 2 | Power cord | 1 |

4. Name of parts

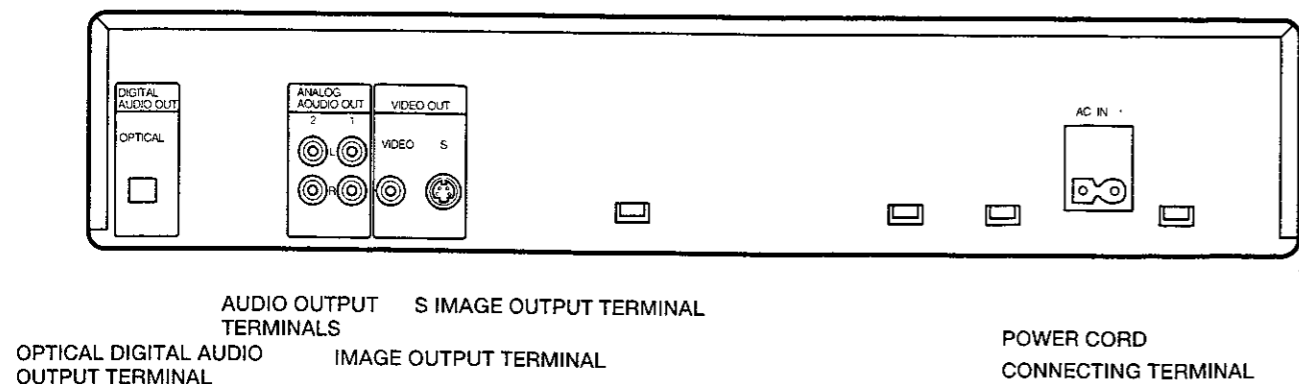
- Remote control set



● Front face



● REAR SIDE



5. Description of adopted new technology

5-1 Digital signal circuit

(1) Data flow

Fig. 5-1 shows the block diagram of digital signal circuit.

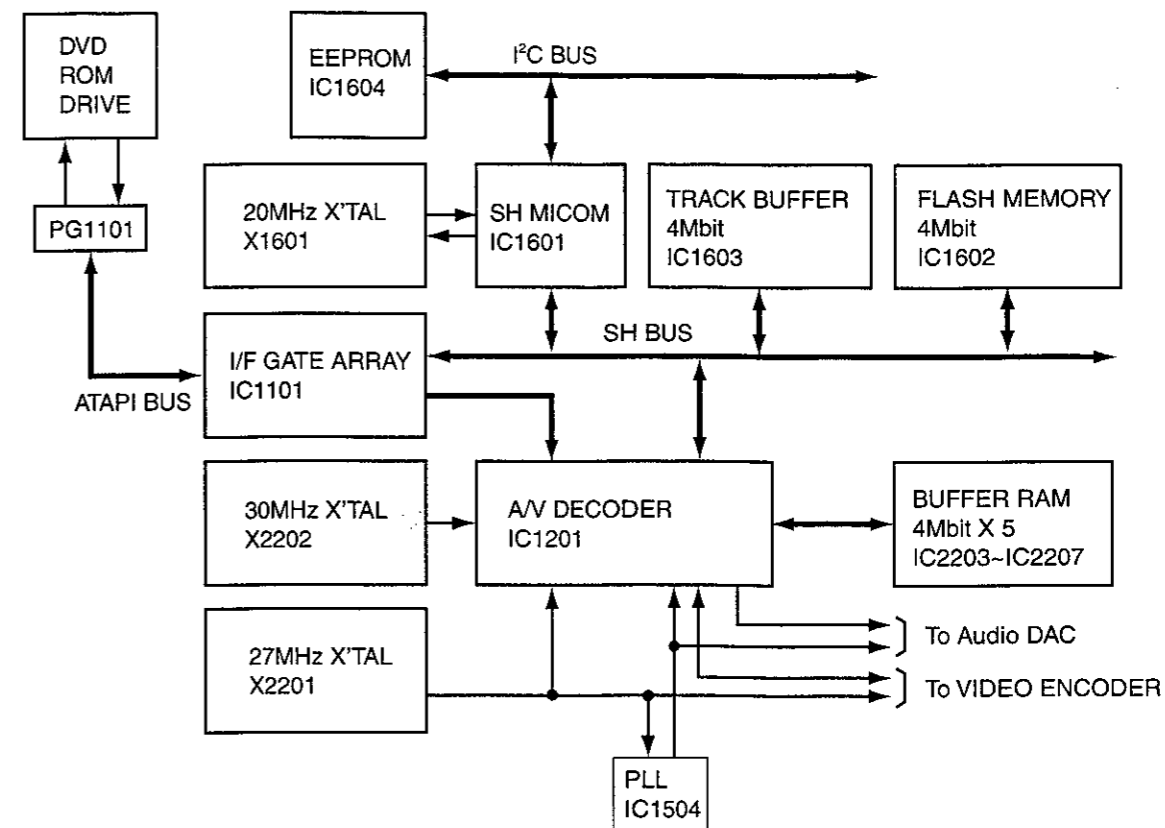


Fig. 5-1 Block diagram of digital signal circuit

DISC data read by DVD ROM DRIVE are stored in TRACK BUFFER (IC1603) by SH MICOM (IC1601) and through I/F GATE ARRAY (IC1101). Then the stored data will be read out from TRACK BUFFER in response to demand by A/V DECODER (IC1201) and input in A/V DECODER through I/F GATE ARRAY. Finally, A/V DECODER will demodulate/decode the data according to their contents and output Audio data to Audio DAC(IC1502), and video data to Video ENCODER(IC2202)

(2) Reference clock of each IC

| IC | Reference Clock |
|-----------------------|--|
| IC1101 I/F GATE ARRAY | 20MHz clock generated by SH MICOM |
| IC1601 SH MICOM | System clock of X1601 20MHz X'TAL, SH |
| IC1602 FLASH MEMORY | Nil (Control signal is generated by SH MICOM) |
| IC1603 TRACK BUFFER | Nil (Control signal is generated by SH MICOM) |
| IC1604 EEPROM | Nil (Control signal is generated by SH MICOM) |
| IC1201A/V DECODER | <ul style="list-style-type: none"> • System clock is input from X2202 30MHz X' TAL. • Video interface clock is input from X2201 27MHz X' TAL. • Audio interface clock is input from IC1504 PLL 16.934 (18.432, 36.864) MHz. |
| IC1504PLL | 16.934 (18.432, 36.864) MHz is generated by X2201, 27MHz X' TAL input. |

(3) Functions of each IC

| | IC | Functions | Operating voltage |
|---|--------------------------|---|-------------------|
| ① | IC1101 I/F GATE ARRAY | Execute data transfer timings from ATAPI to TRACK BUFFER, and from TRACK BUFFER to A/V DECODER. | 5V |
| ② | IC1601 SH MICOM | Execute data transfer, presetting and control of each IC. | 5V |
| ③ | IC1602 FLASH MEMORY | Store memory for SH MICOM software | 5V |
| ④ | IC1603 TRACK BUFFER | Buffer memory for data transfer | 5V |
| ⑤ | IC1604 EEPROM | Storage memory for LAST KEY operation data | 5V |
| ⑥ | IC1201 A/V DECODER | Execute decompression (decoding) of data compressed by MPEG | 3.3V |
| ⑦ | IC2203-IC2207 BUFFER RAM | Memory used for decompression (decoding) of data compressed by MPEG and controlled by A/V DECODER | 5V |
| ⑧ | IC1504 PLL | Generate 16.934 (18.432, 36.864) MHz of audio interface signals from 27MHz clock. | 5V |

The following is the description of the functions of each IC:

① I/F GATE ARRAY (IC1101)

It executes signal timing changes between SH MICOM (IC1601) AND DVD ROM DRIVE I/F (PG1101),A/V DECODER (IC1201). It operates on 20MHz clock output from SH MICOM.

② SH MICOM (IC1601)

It transfers data and executes presetting and control of each IC.

Data transfer from DVD ROM DRIVE I/F is done by setting a register of I/F GATE ARRAY and by intermediary of I/F GATE ARRAY.

In addition, it controls Audio DAC ((IC1502), VIDEO ENCODER (IC2202), AND EEPROM (IC1604), manages TRACK BUFFER (IC1603) AND FLASH MEMORY (IC1602), and communicates with FL MICOM (IC1701).

With 20MHzXTAL(X1601) attached it pulses and is used as a SYSTEM CLOCK.

③ FLASH MEMORY (IC1602)

A 4Mbit FLASH ROM is used. It stores SH MICOM program and its access is controlled by SH MICOM.

④ TRACK BUFFER (IC1603)

A 4Mbit DRAM is used. It stores data read out from DISC. Its control is done by SH MICOM, and its data is read-written via I/F GATE ARRAY. In addition a part of this BUFFER is used as the WORK AREA of SH MICOM.

⑤ EEPROM (IC1604)

It is a 16Kbit EEPROM and stores DISC information by LAST KEY, etc. SH MICOM controls it.

⑥ A/V DECODER (IC1201)

Data input from TRACK BUFFER via I/F GATE ARRAY is separated into Audio data and Video data. MPEG compressed data are decompressed (decoded) and output as DIGITAL Video and DIGITAL audio (AC-3). SH MICOM controls it via I/F GATE ARRAY. SYSTEM CLOCK, CLOCK of VIDEO INTERFACE signals, and CLOCK of AUDIO INTERFACE signals operate by inputting 30MHz, 27MHz, and 16.934(18.432, 36.864)MHz, respectively.

⑦ BUFFER RAM (IC2203-IC2207)

Five 4 Mbit DRAM are used. A/V DECODER controls it and it is used to decompress Audio and Video data compressed by MPEG.

⑧ PLL (IC1504)

PLL generates 16.934(18.432, 36.864)MHz of AUDIO INTERFACE signals clock by inputting 27MHz from VIDEO INTERFACE signals clock. It supplies A/V DECODER and Audio DAC. (See 5-8 clock circuit.)

5-2 Video circuit (DEC substrate)

8bit YCrCb DIGITAL VIDEO STREAM (P) output from A/V DECODER is input in VIDEO ENCODER B1865A (IC2202). VIDEO ENCODER is preset in IC in MASTER MODE that generates reference signals and receives 27MHz from SYSTEM CLOCK and outputs H,V synchronous signals to A/V DECODER.

By presetting of internal register, VIDEO DECODER generates:

① NTSC (North America, Japan, Taiwan)

② PAL (Europe, Asia)

standard analog video signals.

Filter circuit eliminates high frequency components of analog video signals output from VIDEO DECODER. Afterwards in S2 processor circuit DC voltage is superposed on C signals then output 2 types of video signals: COMPOSITE VIDEO SIGNALS and Y/C(S2) VIDEO SIGNALS to RJK substrate via 6P connector (PG2201).

The following is a description of VIDEO CIRCUIT along signal flow:

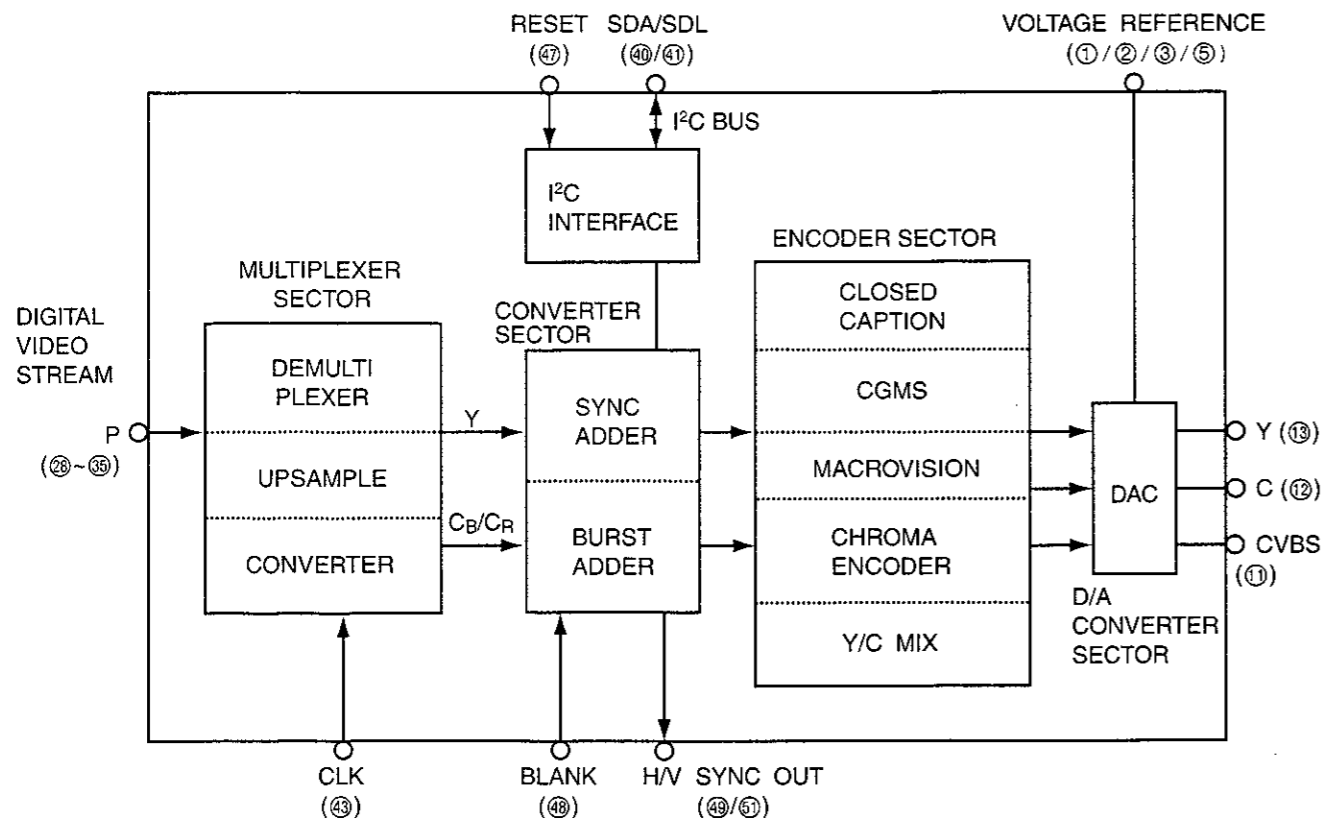


Fig. 5-2-1 Block diagram of VIDEO ENCODER B1865A (IC2202) interior

5-2-1 VIDEO ENCODER B1865A (IC2202)

(1) MULTIPLEXER SECTOR

It transforms input DIGITAL VIDEO STREAM (Input at 26~35 pins) in 8bit parallel data then separates them in Y DATA and C_b/C_r DATA and changes simultaneously the rate (6.75MB/S→13.5MB/S).

(2) CONVERTER SECTOR

It generates various internal timing signals with the synchronous signal as standard by adding synchronous signals generated in IC to Y DATA, according to the conditions set in the internal register or by adding BURST signals to C_b/C_r DATA. At the same time it outputs these synchronous signals to A/V DECODER (Output at 49,50 pins). BLANK signal (Input of L level at 49 pin) is input from SH MICOM when power is turned ON or OFF to prevent screen flickering. In addition, when power is turned ON, RESET signal (Input of L level at 47 pin) is input to reset the register in IC.

Moreover, writing in the internal register (presetting) is done via I²C BUS (40,41 pins).

(3) ENCODER SECTOR

The following ①~③ data are inserted in VIDEO DATA according to preset conditions in the internal register:

① Closed caption

NTSC Mode: 21 lines and 284 lines/ PAL Mode: 22 lines and 335 ines.

② CGMS (Copy Guard Management System)

20 lines and 280 lines of NTSC.

③ Macrovision Copy Prevention System

Finally it generates DIGITAL INTENSITY DATA, DIGITAL CHROMA DATA, and DIGITAL COMPOSITE DATA.

(4) D/A CONVERTER (DAC)SECTOR

Constituted of 10bit DAC, it transforms DIGITAL VIDEO DATA in ANALOG VIDEO DATA for output. Under control of output voltage by DAC pins (①, ②, ③, ⑤pins), it output 3 kinds of ANALOG VIDEO SIGNALS:

① ANALOG COMPOSITE VIDEO SIGNALS (CVBS/⑩ pin), output voltage 1.0Vpp.

② ANALOG INTENSITY SIGNALS (Y/⑬ pin), output voltage1.0Vpp.

③ ANALOG CHROMA SIGNALS (C/⑫ pin), BURST part output voltage 286mVpp.

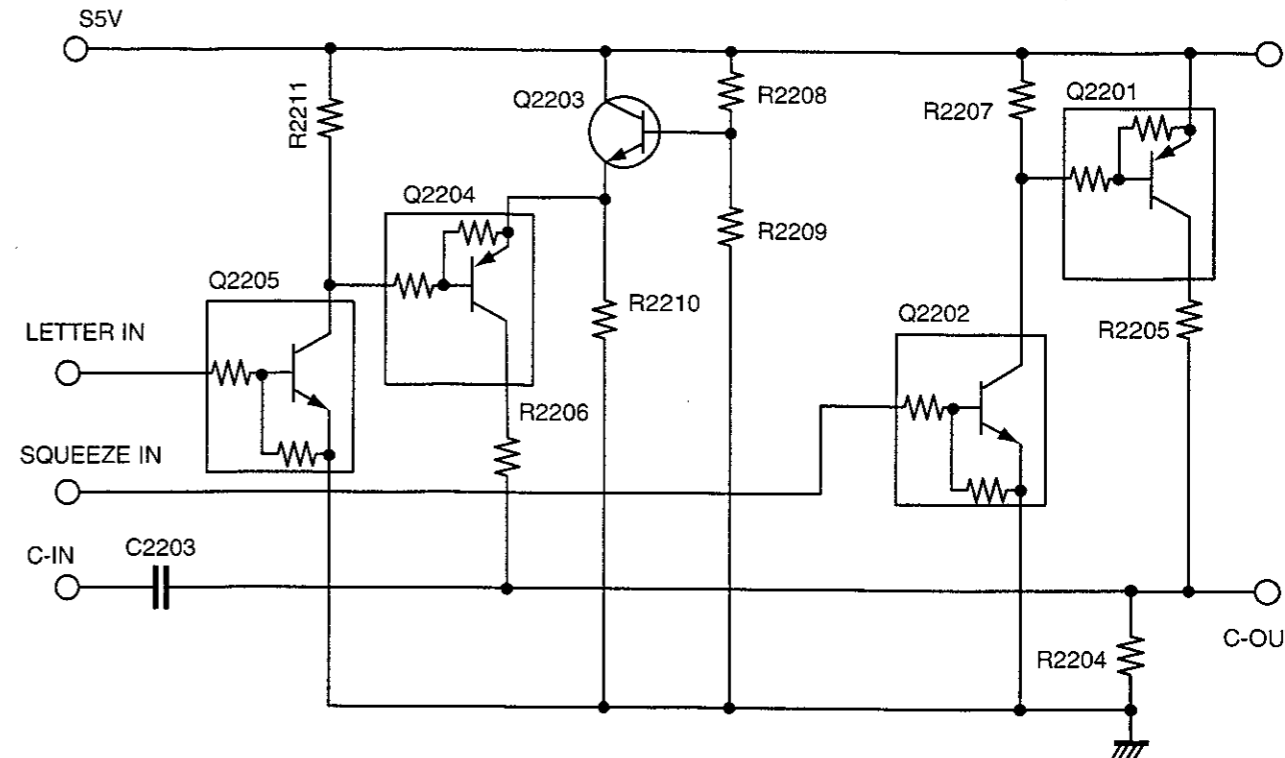


Fig. 5-2-2 S2 Processing Circuit

5-2-2 S2 Processing Circuit

S2 is a standard used in wide television sets possessing screen size switching function in NTSC mode. By inputting VIDEO signals formed by superposing DC voltage on C signal at S input terminal, it switches automatically to TV display size. The DC voltage superposed on C signal varies according to the ASPECT RATIO of VIDEO SIGNALS.

(1) Case of SQUEEZE SIGNAL (*1)

H-level voltage is input in SQUEEZE INPUT; Q2202 and Q2201 are powered and +4V DC voltage is superposed on C signal output line.

(2) Case of LETTER BOX SIGNAL (*2)

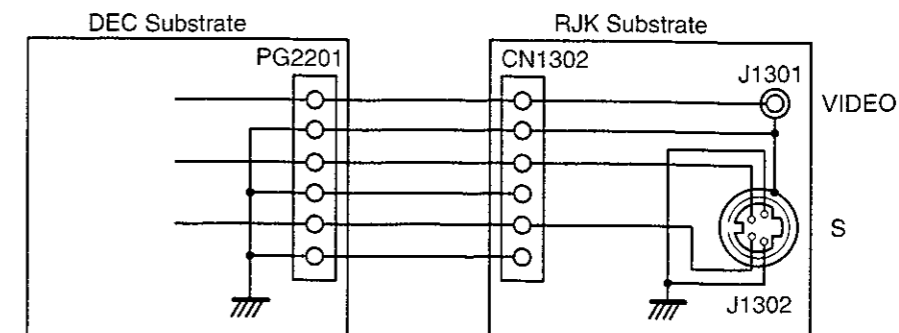
H-level voltage is input in LETTER INPUT; Q2205, Q2204, and Q2203 are powered and +1.8V DC voltage is superposed on C signal output line.

*1: It is a laterally shrunk image information with 525 lines and an aspect ratio of 16:9 carried by the standard TV signal format of 525 lines and an aspect ratio of 4:3. When viewing on a 4:3 TV set, the image appears vertically oblong.

*2: It is a wide screen signal in the standard TV signal format of 525 lines and an aspect ratio of 4:3 with coexistence of upper and lower blank areas of 525 lines and an aspect ratio of 4:3 screen and the principal image area of 4:3 aspect ratio (line 53~232/316~495). When viewing on a 4:3 TV set, one sees black areas at the top and bottom of the screen.

5-3 VIDEO OUTPUT CIRCUIT (RJK substrate)

ANALOG COMPOSITE VIDEO SIGNALS (CVBS), ANALOG INTENSITY SIGNALS (Y), and ANALOG CHROMA SIGNALS (C) are sent from DEC substrate to RJK substrate by passing through 6P connector (PG2201~CN1302). From RJK substrate, CVBS signals are output from output terminal J1301 and Y/C signals are output from output terminal J1302.



5-4 AUDIO CIRCUIT

AUDIO CIRCUIT is shown in Fig. 5-4-1.

AUDIO CIRCUIT is composed of D/A CONVERTER SECTOR (DEC substrate) that transforms digital audio signals output from A/V DECODER (IC1201), ANALOG PROCESSING SECTOR (RJK substrate) that consists of an operational amplifier, and MUTE CIRCUIT (DEC substrate, RJK substrate) for stopping audio output when required.

(1) D/A CONVERTER SECTOR (DEC substrate)

D/A CONVERTER SECTOR is composed of IC1502 that receives and transforms digital audio signals from A/V DECODER in analog signals and IC1504 that generates clock signals corresponding to the sampling frequency of digital audio signals from 27MHz of master clock signals.

IC1502 is a converter corresponding to L and R signals of sampling frequencies 44.1/48/96kHz and data lengths 16/20/24bit, and digital audio signals from A/V DECODER is input at ② pin.

To these digital audio signals are inserted L and R signals in time sharing mode. When they are input in ① pin, they are separated in L and R signals by R clock and after transformation analog L signals are output at ⑩ pin and R signals at ⑪ pin. Moreover, when there are no input signals at ② pin, a signal called ZERO MUTE is output to ⑫ pin to mute useless noises (See paragraph on MUTE CIRCUIT.)

Every functions of IC1502 is preset by MICOM and controlling signals from SH MICOM are input at ⑭⑮⑯ pins.

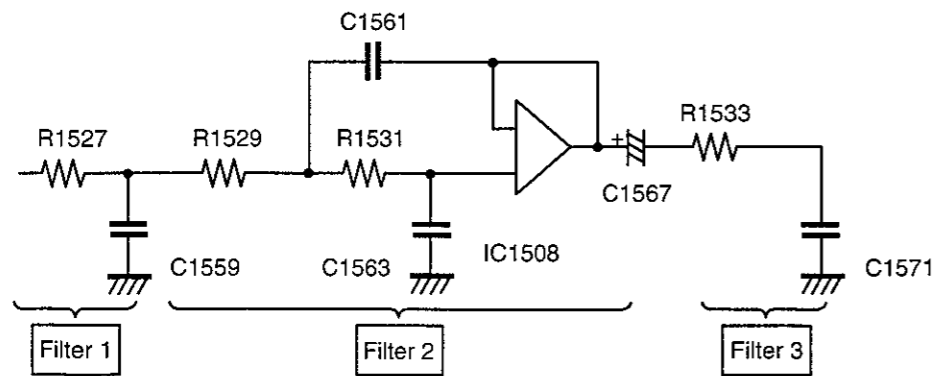
As for presetting items, there are data length, sampling frequency, signal polarity, and de-emphasis.

On the other hand, 27MHz master clock is input at ① pin of IC1504, then passes through the internal PLL circuit and is output from ② pin as a clock signal provided to IC1502.

(2) ANALOG PROCESSING SECTOR (RJK substrate)

ANALOG PROCESSING SECTOR is composed of operational amplifier IC1508 that is a filter and operational amplifier IC1510 that mixes and amplifies audio signals and Karaoke signals.

Filter portion is composed of RC low bass filter and IC1508 formed active low bass filter and there are 3 sections. The diagram below shows its filter portion circuit (for L signals only).



This 3-section filter constitutes a low bass filter of overall cutoff frequency of 44kHz. Audio signals after low bass filter is amplified by IC1510 by about 6dB and output to AUDIO OUT1 AND AUDIO OUT2.

Here, among audio signals, L signals are input at ③ pin of IC1508 and output from ① pin, then input to ② pin of IC1510 then output from ① pin.

R signals are input at ⑥ pin of IC1508 and output from ⑦ pin, then input to ⑥ pin of IC1510 then output from ⑦ pin.

(3) MUTE CIRCUIT (DEC substrate, RJK substrate)

The principal role of MUTE CIRCUIT is the erasing of useless noises occurring when power is turned on.

Mute signal for noise erasing is generated by SH MICOM, reverse-amplified by Q1505 and Q1506. Then by putting Q1510, Q1511, Q1310, and Q1311 'ON', it mutes audio signals.

In addition, if IC1502 detects no-signal, it generate a mute signal called ZERO MUTE. This latter is reverse-amplified by Q1507 and mutes useless audio signals by putting Q1310 and Q1311 'ON'.

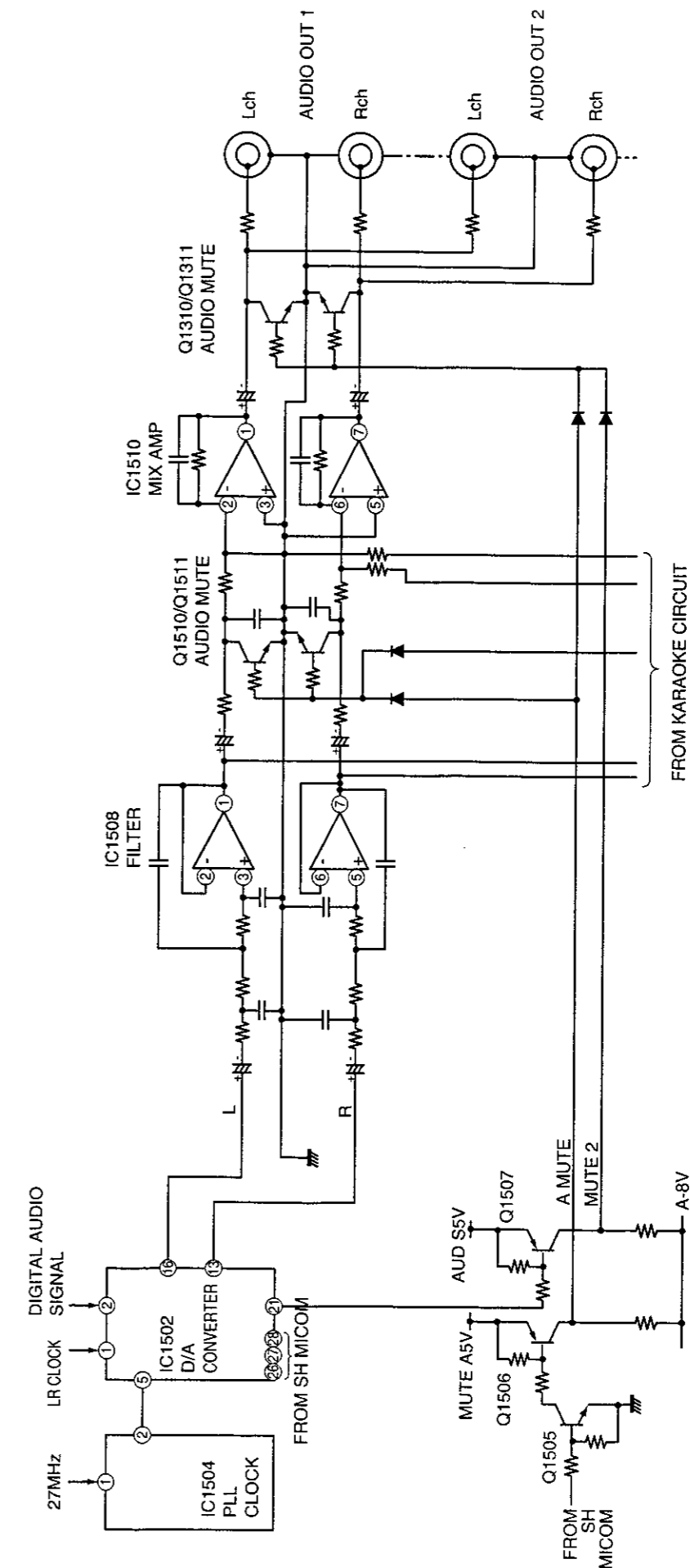


Fig. 5-4-1 Audio circuit

5-5 KARAOKE CIRCUIT (The following descriptions concern Lch signal/Rch signal) When mike is connected to the mike input terminal. "KARAOKE" will be lighted on FL tube and mode will be changed to Karaoke mode. Therefore, karaoke functions of keycon and vocal cancel may be used. When mike is disconnected, karaoke mode is 'OFF'.

(1) MAIN CIRCUIT

L/Rch signals output by audio circuit low bass filter, IC1508 ①, ⑦ pins pass through BUFFER (IC1509, input at ③, ⑤ pins, output at ①, ⑦ pins) and are input to IC1417 at ②⑦, ②⑧. Then they are processed and sorted, by command by SH MICOM (IC1417, input at ③③, ③④ pins), in Lch MONO*¹, Rch MONO*², VOCAL CANCEL*³, L/Rch output as it is, and then output from ②⑨, ②⑩ pins.

Afterwards, L/Rch signals pass through HPF (IC1418, input at ②⑩ pin, output at ①⑨/ IC1419, input at ② pin, output at ① pin), mixed with MIKE ECHO signal and KEYCON signal (IC1418, input at ①⑨ pin, output at ① pin/IC1419, input at ③ pin, output at ⑦ pin), pass switch IC that is used as keycon alternate circuit (IC1421, input at ④, ⑤ pins, output at ③, ⑤ pins), and finally flow back to the audio circuit (IC1510, input at ②, ⑥ pins).

*1 Lch MONO: Lch signals output at L/Rch.

*2 Rch MONO: Rch signals output at L/Rch.

*3 VOCAL CANCEL: Vocal portion situated in the center of vocal source is attenuated.

(2) KEYCON CIRCUIT

L/Rch signals output from IC1417, ②⑨, ②⑩ pins, is mixed with Lch and input to IC1418, ②⑦ pin. After flowing through LPF, they enter KEYCON CIRCUIT to receive KEYCON process according to command from SH MICOM (IC1418, input at ⑦, ⑧, ⑨ pins) and are output at ②⑩ pin.

After that, they flow again through LPF (IC1418, input at ①⑨ pin, output at ①⑦ pin) and are mixed with main L/Rch signals input at IC1418 ①⑨ pin/IC1419 ③ pin.

As described above, signals flowing through LPF are mixed with L/Rch, so that when KEYCON is operating (Otherwise there is alternative circuit.), they become pseudo stereo. LPF makes KEYCON process signals below ~3.3kHz.

(3) KEYCON ALTERNATIVE CIRCUIT

To prevent signals from becoming always pseudo stereo due to KEYCON CIRCUIT, they are arranged to flow in an alternative circuit when the key is natural (When KEYCON is not operating.).

Signals to be output to audio circuit are switched by inputting signals before and after KEYCON process to SWITCH IC, IC1421. Signals before KEYCON process are output at IC1417 ②⑨, ②⑩ pins and input at ①, ① pins. Signals resulting from the mix up of KEYCON signals and MIKE ECHO signals are output at IC1418 ①⑨ pin/IC1419 ⑦ pin and input to IC1421 ④, ⑤ pins.

Control signal, KEYFO (Hi, when key is natural; Lo, otherwise) from SH MICOM is input to Q1423, then flows through Q1424 to reach IC1421 ①③, ①② pins. Finally signals flow through Q1425 from Q1424 and reversed is input to IC1421 at ⑤, ⑥ pins. With this control signal, input at IC1421 ①, ① pins is output at ②, ①⑥ pins; otherwise, input at IC1421 ④, ⑤ pins is output at ③, ⑤ pins. Signals output from IC1421 flow back to AUDIO CIRCUIT and are input at IC1510 ②, ⑥ pins.

When key is natural, signals flow outside MIKE ECHO signal mix circuit, therefore with KEYFO (input at IC1417 ① pin), MIKE ECHO signals are mixed with L/Rch signals in IC1417 and output at IC1417 ②⑨, ②⑩ pins.

(4) MIKE-ECHO CIRCUIT

Signals output from MIC1 are input to IC1417 ① pin, then after passing through MIKE amplifier, output to MIKE VOLUME RV1762 from ④ pin, then input again to IC1417 at ⑥ pin. Similarly, signals output from MIC2 are input to IC1417 ⑥ pin, then after passing through MIKE amplifier, output from ⑨ pin to MIKE VOLUME, then input again to IC1417 at ⑩ pin.

MIC1 and MIC2 are mixed inside IC1417 then output from ① and input at ⑩ pin. After ECHO process they are output from ②④ pin, pass through ECHO VOLUME RV1764, and input again to IC1417 ②⑤ pin. In IC1417, signals input at ②⑤ pin are mixed with the mixed signals, as said above by MIC1 AND MIC2, then output from ③⑥ pin. Afterwards, they are input at IV1418 ①⑥ pin/IC1419 ⑥ pin, and mixed with L/Rch signals.

(5) KARAOKE ALTERNATIVE CIRCUIT

In order to prevent deterioration of common audio sound, it is designed that Karaoke signals pass KARAOKE CIRCUIT only in Karaoke mode (i.e., when mike is connected.)

MIC SW (output from MIC2 jack J1763 ⑤ pin) used as control signal is [Hi] when either of MIC1 or MIC2 is, or both are connected. Otherwise it is [Lo].

After passing through Q1417, MIC SW is connected to Q1419/Q1418. After passing through Q1417, MIC SW passes Q1420 and is connected to Q1511/Q1510. Q1511/Q1510 are connected to output IC1508 ①, ⑦ pins of audio circuit filter. Moreover, after passing through Q1417, MIC SW is connected to Q1422/Q1421. Q1422/Q1421 are connected to output IC1421 ③, ⑤ pins of Karaoke circuit.

In Karaoke mode, signals are output by setting Q1419/Q1418 to 'OFF'.

When Karaoke mode is 'OFF', signals input in Karaoke circuit are muted by setting Q1419/Q1418 'ON'. In addition, output signals of Karaoke circuit are muted by putting Q1511/Q1510 'OFF' and muting audio signals.

(6) VOICE SW

It detects audio input in mike, and is used in AUTO VOCAL CANCEL or to playback mike input without music. Signals having passed are mixed after output from IC1417 ④ pin (MIC1) and ⑥ pin (MIC2). Then, they are input to IC1420 ③ pin, output from ⑦ pin in DC, and finally input to Q1426 base. When sound enters mike, Q1426 is put 'ON' and collector becomes [Lo]. If no sound enters mike, Q1426 is put 'OFF' and collector become [Hi]. This collector output is named VOICE SW. VOICE SW is input to SH MICOM and used for AUTO VOCAL CANCEL control. In addition, it passes through Q1504 and Q1507 of DEC substrate, sets Q1310/Q1311 to 'ON' or 'OFF', and controls muting of audio output. In general, when there is no audio output, there is no noise output, muting is effective on audio output. When there is mike input, it puts Q1310/Q1311 'OFF', lets mike input output without being muted.

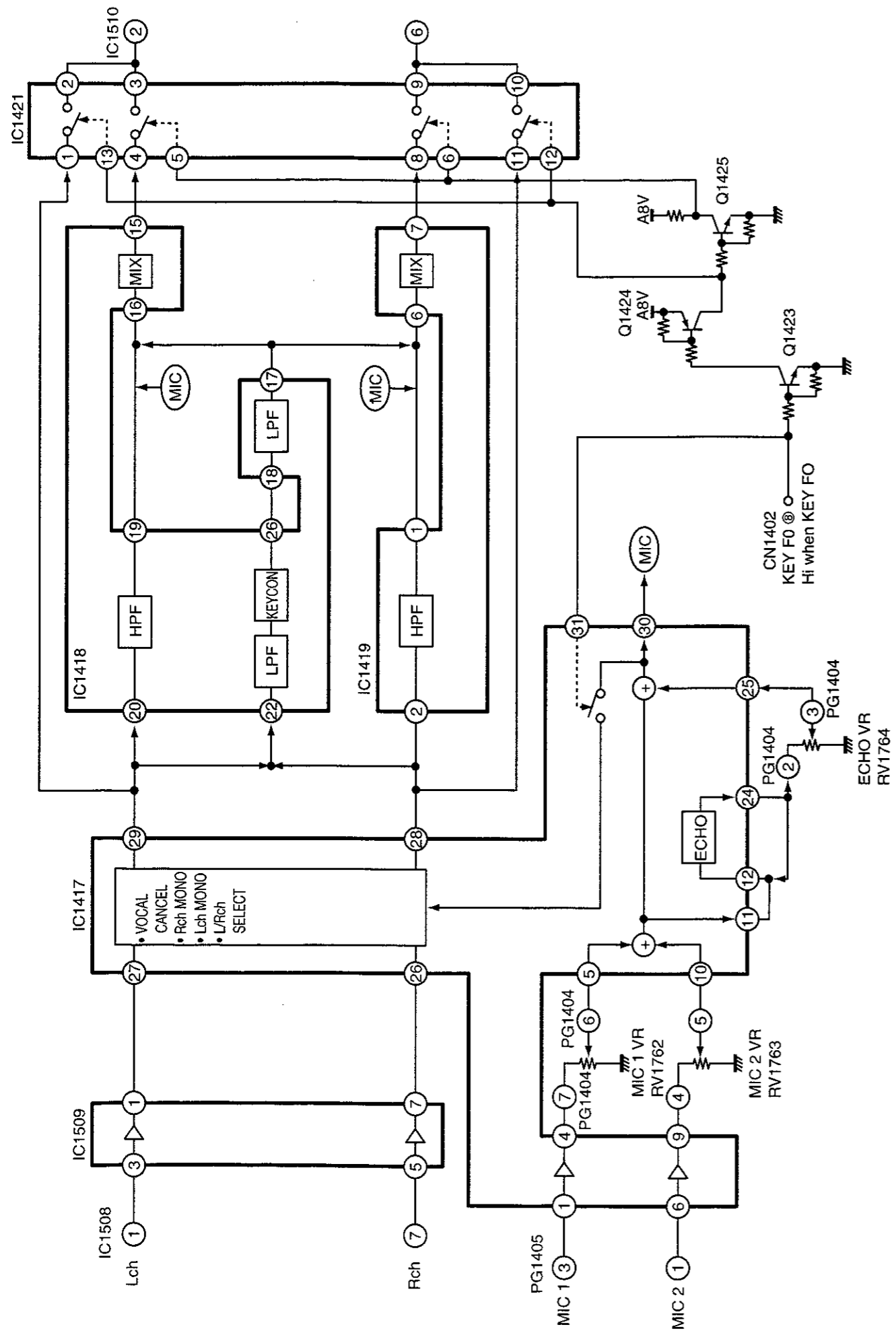


Fig. 5-5-1 KARAOKE CIRCUIT (KEYCON ALTERNATIVE CIRCUIT included.)

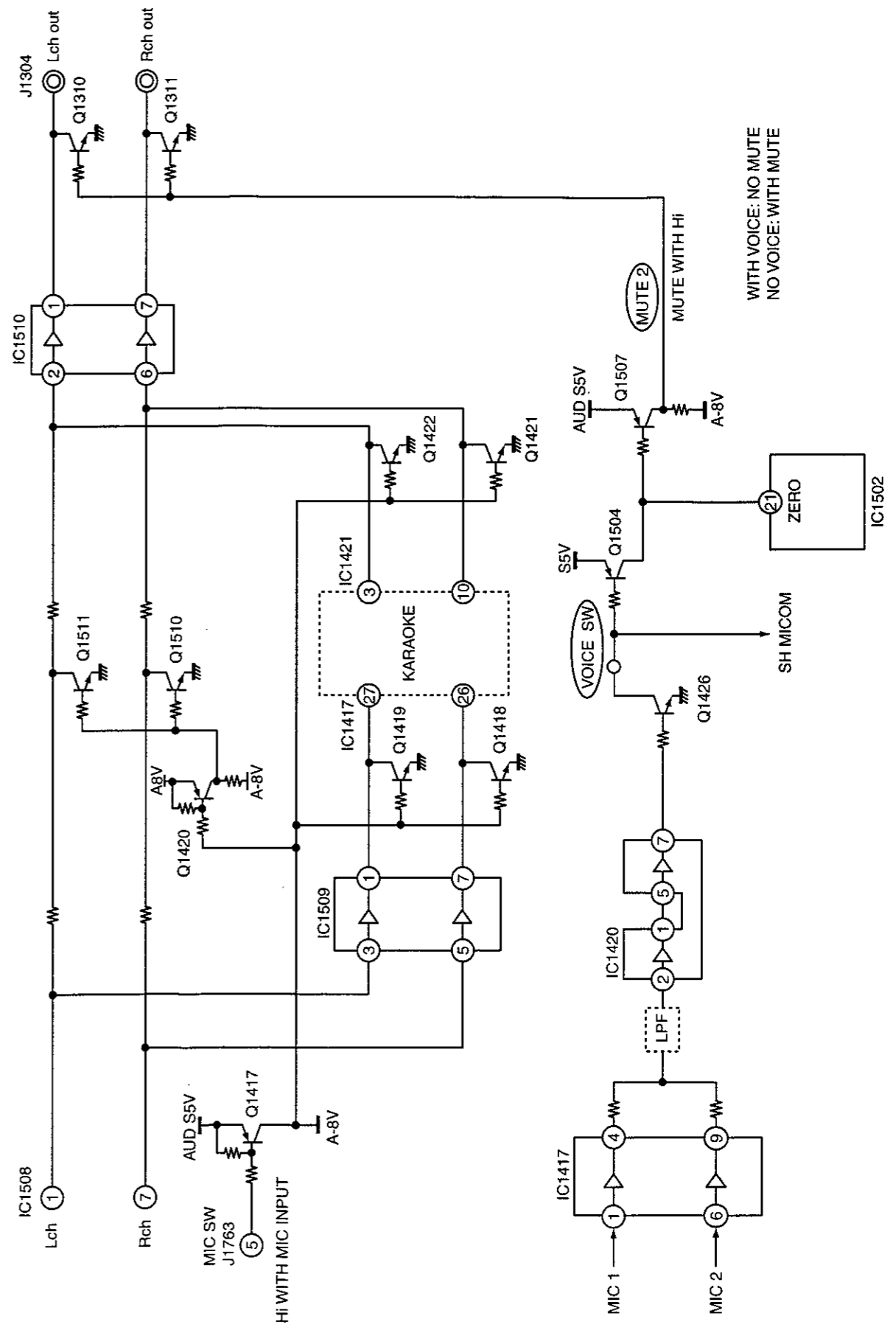


Fig. 5-5-2 KARAOKE CIRCUIT/VOICE SW

5-6 FRONT (FSW) SUBSTRATE CIRCUIT

(1) FL MICOM (IC1701)

It performs communications with SH MICOM (⑥, ⑦, ⑩ ~ ⑬, ⑮, ⑳ pins), including the main frame KEY and remote control operation, FL tube (IC1702) drive, and lighting of power indicator. In addition, it works also in standby mode. When power is 'ON', it outputs control signal at ⑳ pin to start all power sources and voltages and unlock short circuit toward GND of SH MICOM reset IC (IC1605) output.

(2) INCLUSION OF MAIN FRAME KEY AND REMOTE CONTROL OPERATION

Input is done to FL MICOM at ②~④ pins for operation of S1701 ~ S1715 and S1761 ~ S1763 of mainframe KEY. Input is done to FL MICOM at ⑳, ㉑, ㉒~㉔ pins for JOG SHUTTLE SW (S1718) operation.

Remote control signal is received by ultra-red receiver element (IC1703), output at ① pin and input to FL MICOM at ㉕ pin.

(3) FL TUBE DRIVE

Grid voltage of FL TUBE at ⑳~㉓ pins is controlled from FL MICOM ①~⑥ PINS; anode voltage of FL TUBE at ⑤~⑨ pins from FL MICOM ①~⑥ pins. Among which FL MICOM 65~69 pins are connected to A-20V by R1743~R1743 because no pull down resistance is built-in in IC.

Filament voltage (AC4.2V) is supplied from power source to FL TUBE at ①, ②, ④, ⑥ pins.

(4) POWER INDICATOR

Control signal output from FL MICOM ㉖, ㉗ pins puts LED driving transistors Q1703 and Q1704 'ON' or 'OFF' then lights 2-color LED (LED1761) green or red. When power is 'ON', Q1704 is 'ON' and lighted green; when standby, Q1703 is 'ON' and lighted red.

5-7 POWER SUPPLY CIRCUIT

(1) ESSENTIAL OF POWER SUPPLY CIRCUIT OPERATION

Fig 5-7-1 shows the block diagram of the power circuit.

Power supply is RCC switching type. Energy is stored in transformer T1, when FETQ1 is 'ON', by AC100V impressed at AC inlet. After that, when FETQ1 becomes 'OFF', the energy is released to the secondary side.

Power supply to diverse circuits from secondary side includes SW (S5V, S3.3V, S12V) that are put 'ON' by FL MICOM control signal (P. ON/OFF) of PG1901 ① pin and permanently 'ON' supplies (A5V, MUTE A5V, AC4.2V, A-20V, A8V, A-8V).

Detection of secondary side voltage is by A5V. D8, C16, C17 composes its secondary side commutating circuit. It is fed back by photo-coupler PHC1 to primary side and maintains stable output voltage and is supplied to FL MICOM and ultra-red reception element.

MUTE A5V is for AUDIO MUTE and supplied from A5V output.

S5V output is from A5V output and by intermediary of output control circuit Q3.

S3.3V is output from S5V at 3-terminal regulator IC2.

D11 and C24 compose secondary commutating circuit of S12 that is output by 3-terminal regulator IC3 and is for DVD ROM DRIVE use.

D11 and C24 compose secondary commutating circuits of A8V that is output by 3-terminal regulator IC4. For audio circuit proper +5V power supply, AUD S5V is produced from A8V in 5V regulator IC1506 (in DEC substrate).

D13 and C29 compose secondary commutating circuit of A-8V and it output -8V by transistor Q7 and Zener diode D20.

A-20V is negative power supply to FL tube. D14 and C33 compose its secondary commutating circuit and output -20V by transistor Q6 and Zener diode D17.

AC4.2V is for FL tube heater. To prevent fluctuation of output voltage due to that of power source, a self-exciting push-pull circuit is used. It is input from A5V, passes DC/AC inverter composed of transistors Q8, Q9, and transformer T2 and output. It supplies stable voltage without being disturbed by power source fluctuations. It plays an important role in FL tube life maintenance and against brightness decrease

(2) OPERATION OF PROTECTION CIRCUIT

PROTECTION CIRCUITS are different according to different power supplies.

For A5V and S5V, when load current increases and exceeds the control limit of the primary side of the regulator, the over current protection circuit of the primary side operates and regulator output will decrease suddenly. At the same time other outputs stop.

For S12V, S3.3V, and A8V, when load current increases and exceeds the control limit of 3-terminal regulator, the internal over current protection circuit operates and output will decrease suddenly.

Pulling the plug from the wall socket eliminates a short circuit and plugging in again restores the normal state.

When A-8V or A-20V output is short circuited, fuse F2 will open to protect circuit. When AC4.2V output is short circuited, fuse F3 will open to protect the circuit. When this and A5V are short circuited, fuse resistance R26 and R27 will open to protect the circuit.

For over current protection for A5V, destruction of Zener diode by short will stop output. The circuit is protected in this way.

By pulling off plug from wall socket, eliminating short circuit, replace destroyed parts, and plug in again, the normal state will be restored.

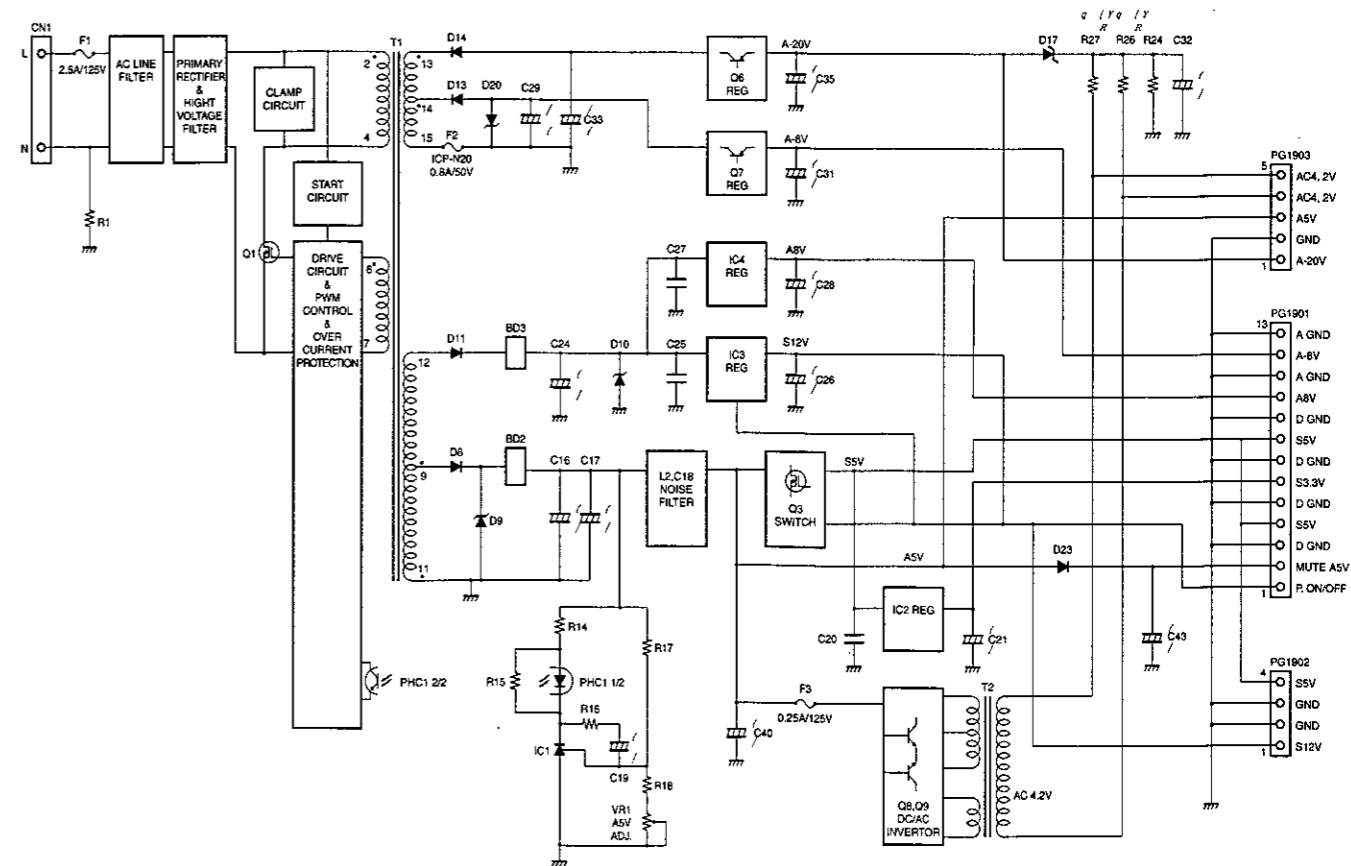


Fig. 5-7-1 BLOCK DIAGRAM OF POWER SUPPLY CIRCUITS

5-8 CLOCK CIRCUITS

5-8-1 27MHzX'TAL (X2201)

Block diagram of 27 MHz clock circuit is shown in Fig. 5-8-1.

When power is supplied to 27 MHz X'TAL, it generates 27MHz clock and input it to A/V DECODER (IC1201, VIDEO ENCODER (IC2202), and PLL (IC1504).

(1) A/V DECODER

At A/V DECODER it is used as CLOCK VCK (input at ⑩ pin) of VIDEO INTERFACE signal and output digital video stream synchronized to VCK from 8bit video data bus VDATA[7:0] (output at ⑩⑧ ~ ⑩⑩, ⑩⑫, ⑩④, ⑩⑥ ~ ⑩⑧ pins)

(2) VIDEO ENCODER

At VIDEO ENCODER it is used as SYSTEM CLOCK CLK (input at ③ pin) and output horizontal synchronous HSYNC (output at ⑨ pin) and vertical synchronous VSYNC (output at ⑥ pin) to A/V DECODER.

(3) PLL

At PLL it is used as reference signal that generates audio external frequency clock signal DA-XCK (output at ② pin). DA-XCK IS supplied to A/V DECODER (input at ⑫ pin) and Audio DAC (input at IC1502 ⑤ pin). The former is used as exterior clock that generates Audio bit clock DA-BCK (output at ⑫ pin) and LR clock DA-LRCK (output at ⑫ pin); the latter is used as System clock.

| | |
|---------|--|
| DA-XCK | Is external clock used for generating DA-BCK and DA-LRCK. DA-XCK takes frequency 384 times the sampling frequency. |
| DA-BCK | Is Audio bit clock obtained by dividing DA-XCK in 8 equal parts. It takes frequency 48 times that of sampling. |
| DA-LRCK | Is clock that identifies channel (Lch or Rch) against all Audio sampling. |

* The Audio Interface Unit inside A/V DECODER corresponds to sampling frequencies (fs) 44.1kHz (CD-DA, Video-CD), 48kHz, 96kHz (DVD).

The frequency of DA-BCK is defined by Formula 5-8-1:

$$f_{DA-BCK} = \text{Audio data bit length} * 2 * fs \dots\dots\dots 5-8-1$$

At A/V DECODER, input to DA-XCK is divided into 8 equal parts and output as DA-BCK (Formula 5-8-2)

$$f_{DA-BCK} = f_{DA-XCK} / 8 \dots\dots\dots 5-8-2$$

Therefore, DA-XCK frequency takes the value 384fs according to formulas 5-8-1 and 5-8-2. Audio data bit length is fixed 24bit. (Formula 5-8-3)

$$f_{DA-XCK} = \text{Audio data bit length} * 2 * fs * 8 = 384fs \dots\dots\dots 5-8-3$$

According to Formulas 5-8-2 and 5-8-3, A/V DECODER drives DA-BCK with frequency 48 times of sampling frequency. (Formula 5-8-4)

$$f_{DA-BCK} = 384fs / 8 = 48fs \dots\dots\dots 5-8-4$$

The relationships between Audio interface signals (DA-XCK, DA-LRCK, DA-BCK) and each sampling frequency are as follows:

◎ Sampling frequency: 44.1 kHz (FOR CD-DA AND Video-CD)

- DA-XCK 384*fs=16.934MHz
- DA-BCK DA-XCK/8=2.1168MHz
- DA-LRCK DA-BCK/48=44.1kHz=fs

◎ Sampling frequency: 48kHz (for DVD)

- DA-XCK 384*fs=18.432MHz
- DA-BCK DA-XCK/8=2.304MHz
- DA-LRCK DA-BCK/48=48kHz=fs

◎ Sampling frequency: 96kHz (for DVD)

- DA-XCK 384*fs=36.864MHz
- DA-BCK DA-XCK/8=4.608MHz
- DA-LRCK DA-BCK/48=96kHz=fs

5-8-2 30MHzX'TAL (X2202)

30 MHzX'TAL (X2202), the same as 27 MHzX'TAL, generates 30 MHz clock by supplying power. It is used as signal for generating A/V DECODER system clock.

From input SYCCLK (IC1201 ⑮ pin) it generates inside the IC an internal 90MHz clock and is used as an interior processor as well as system clock for internal operations.

5-8-3 20MHzX'TAL (X1601)

20MHz clock is generated by attaching 20MHz crystal trembler to SH MICOM (IC1601) and used as the system clock of SH MICOM. This system clock is supplied to I/F GATE ARRAY (input at IC1101 ⑨ pin) and used as clock.

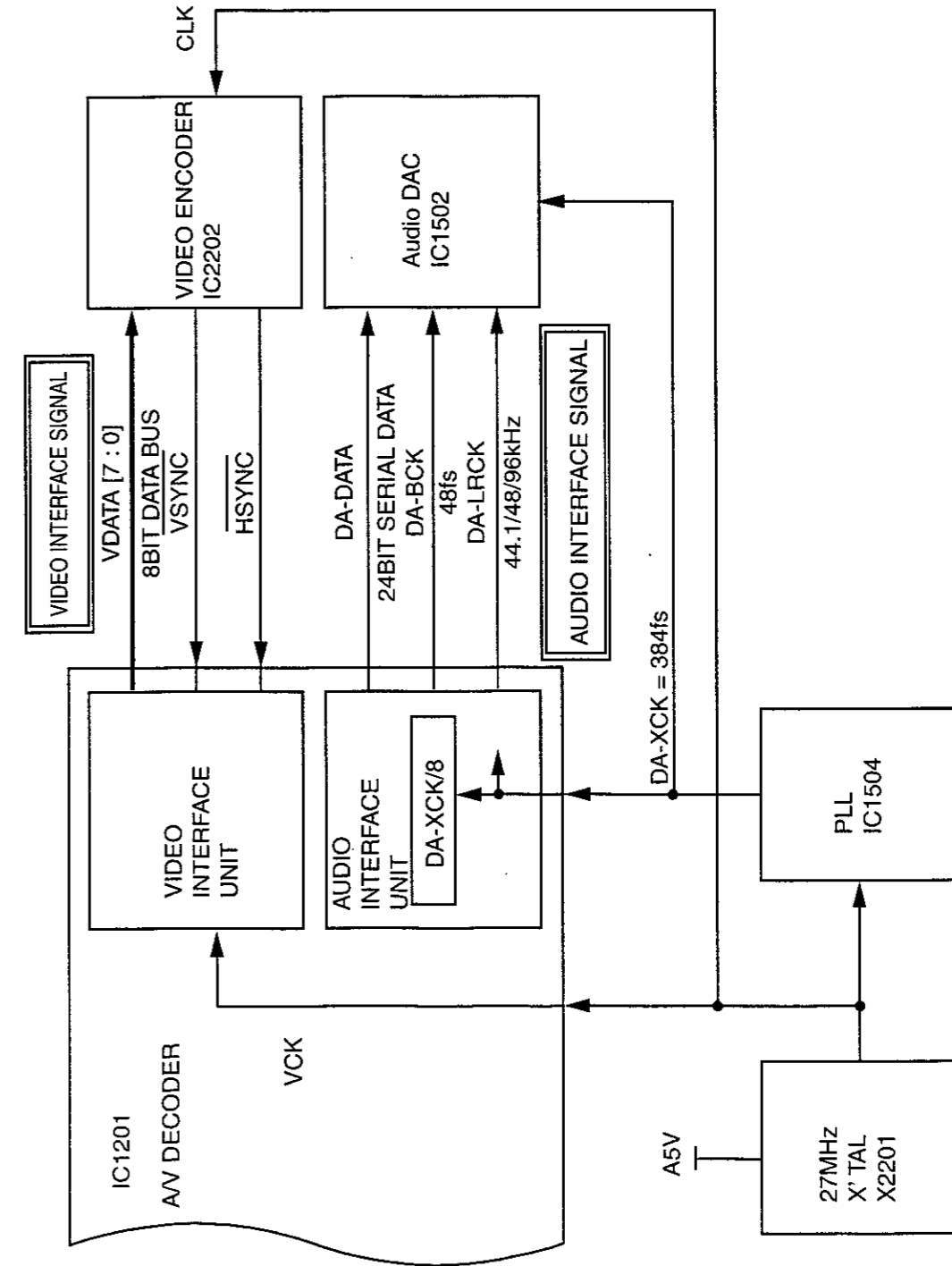


Fig. 5-8-1 BLOCK DIAGRAM OF 27MHz CLOCK CIRCUITS

6. SERVICE POINTS

6-1 TO REMOVE TOP COVER

The top cover is fastened on the front panel with 4 clicks.

- Disengage outside clicks and clicks ① and ④.
 - Lift the rear of the top cover about 15° as shown by Arrows A.
 - Lift both sides of the front of the top cover in the direction shown by Arrows B and disengage clicks ① and ④.
- Disengage inside clicks and clicks ② and ③.
 - After the above operations in 1, lift more and deform both sides of the front of the top cover along Arrows B to disengage clicks ② and ③.
 - To facilitate the operation, you can do it in small steps.

< Caution >

Clicks on the front panel may be damaged if you lift the rear of the top cover by more than 20°.

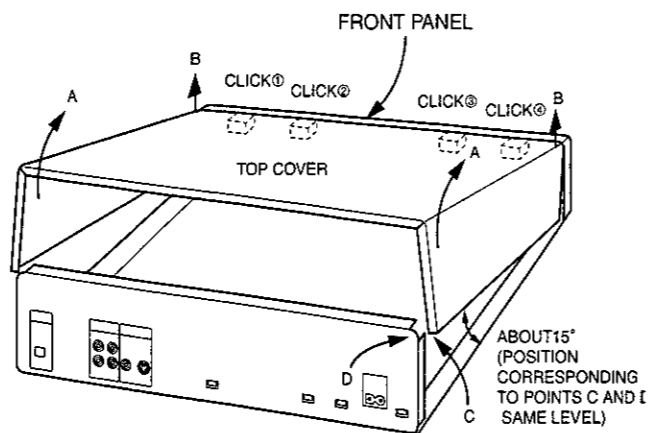


Fig. 6-1 DISASSEMBLING OF TOP COVER

6-2 TO REINSTALL TOP COVER

Keep the top cover at about 15° inclination and engage it to the front panel clicks.

- At this point, lift more and deform both sides of the front of the top cover along Arrows B to engage clicks ② and ③.
- Stop the deformation and engage outside clicks and clicks ① and ④.

< Caution >

The front cover edge may be damaged if you let E of the top cover ride edge F of the front panel while reinstalling the top cover.

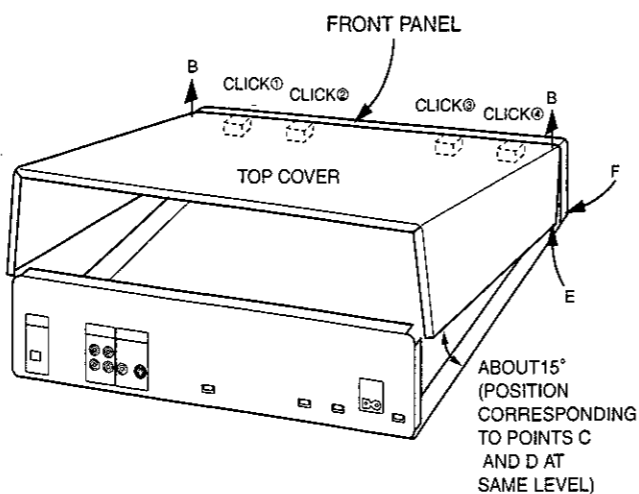
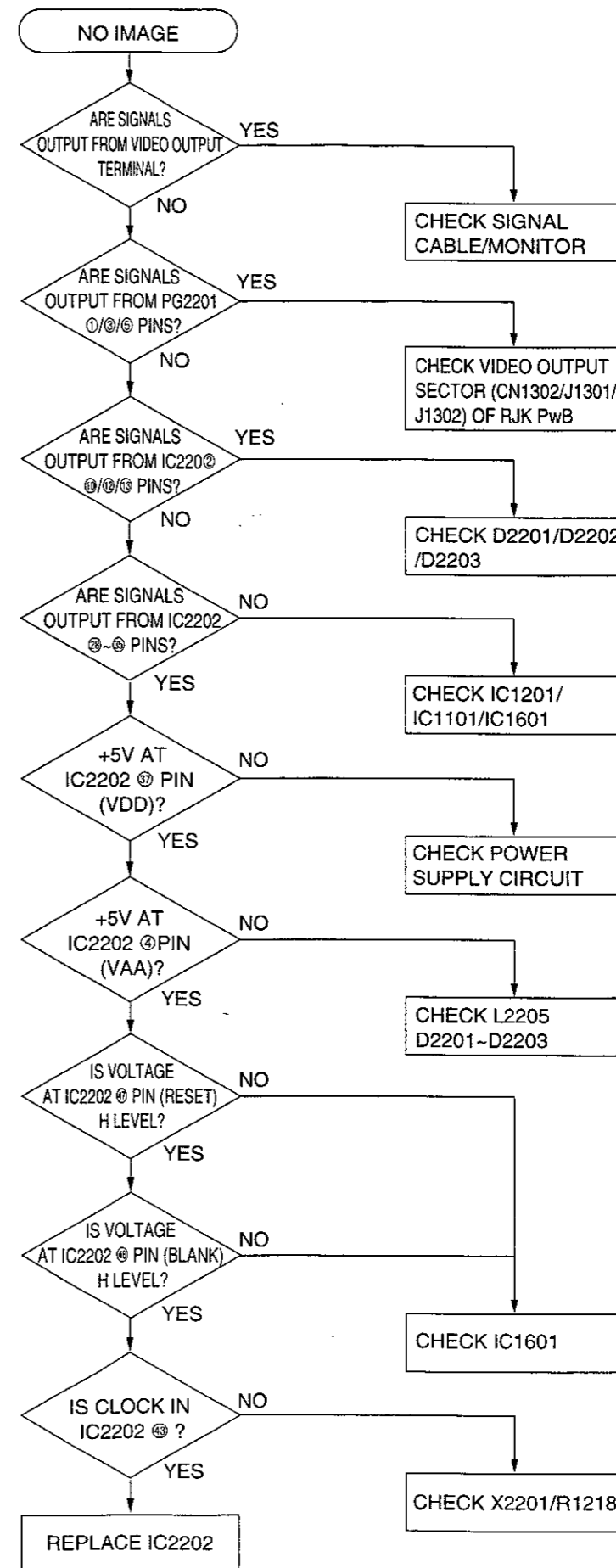


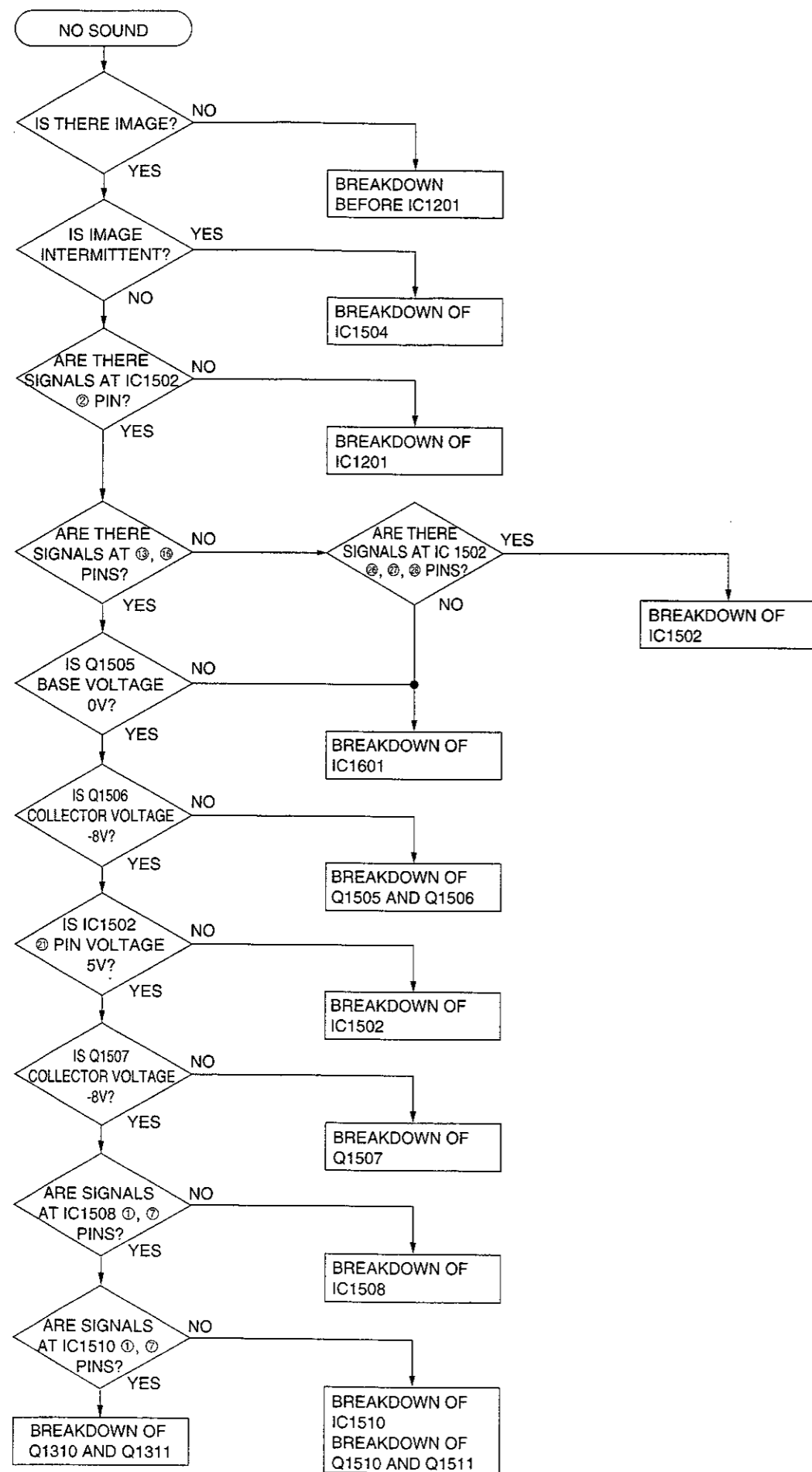
Fig. 6-2 REINSTALLING OF TOP COVER

7. TROUBLE SHOOTING

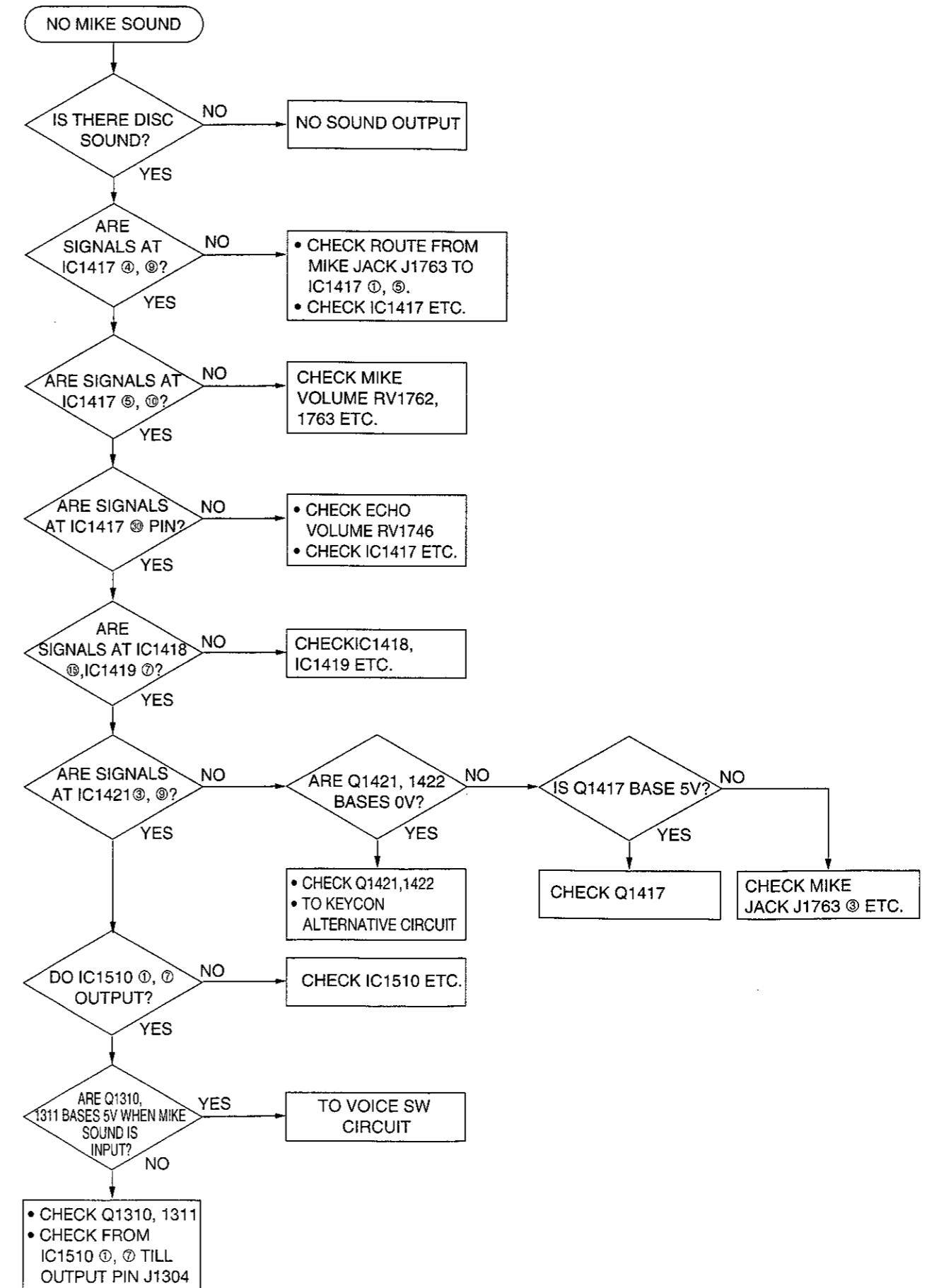
7-1 VIDEO CIRCUIT



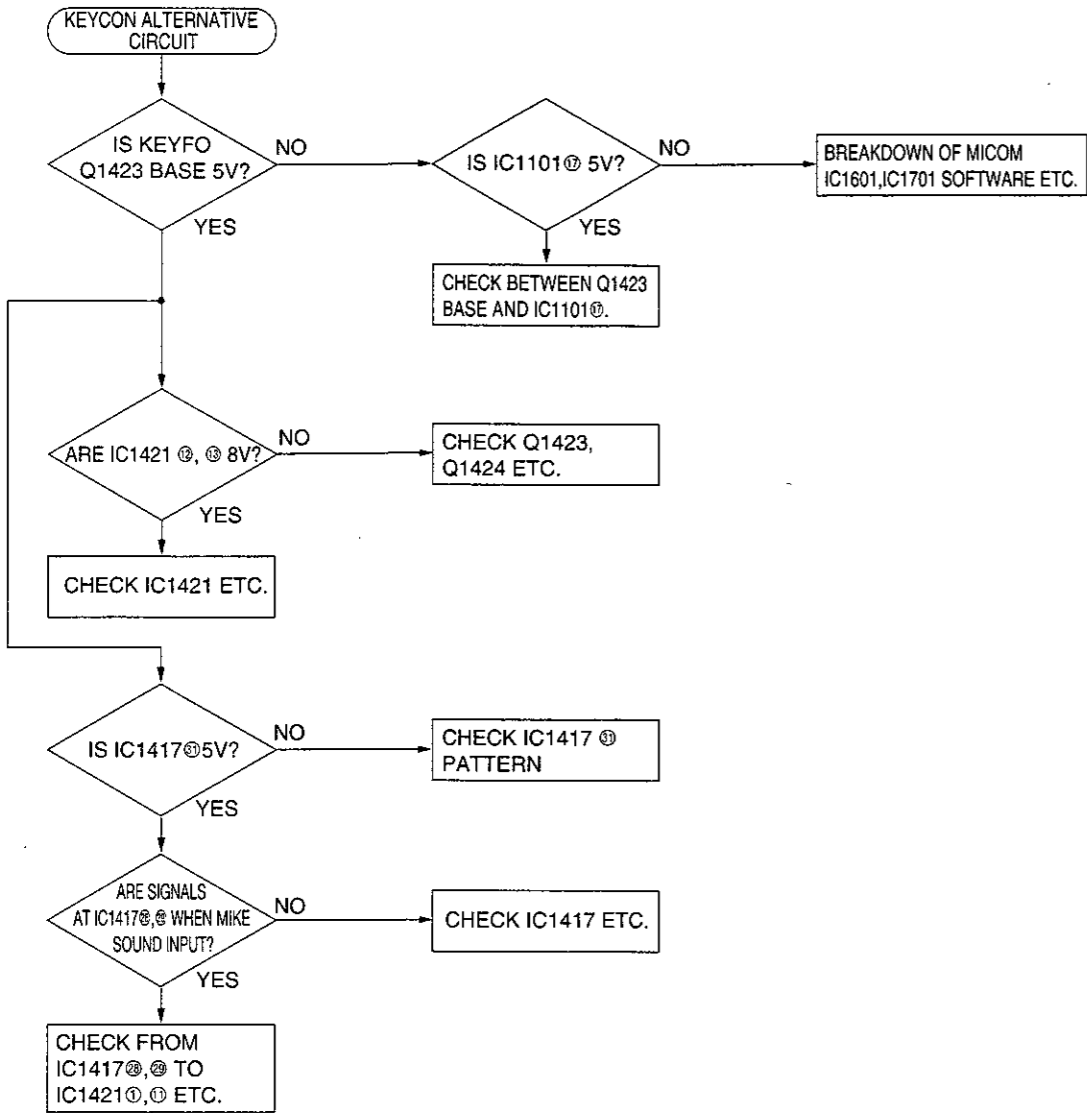
7-2 AUDIO CIRCUIT



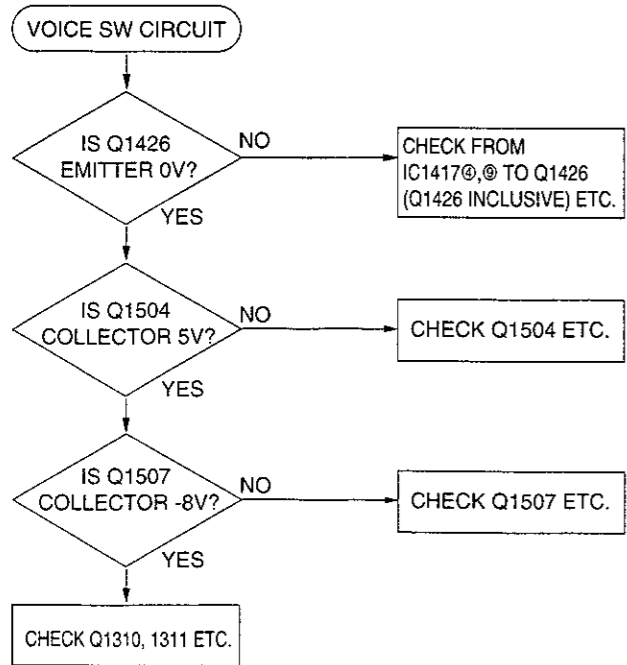
7-3 KARAOKE CIRCUIT



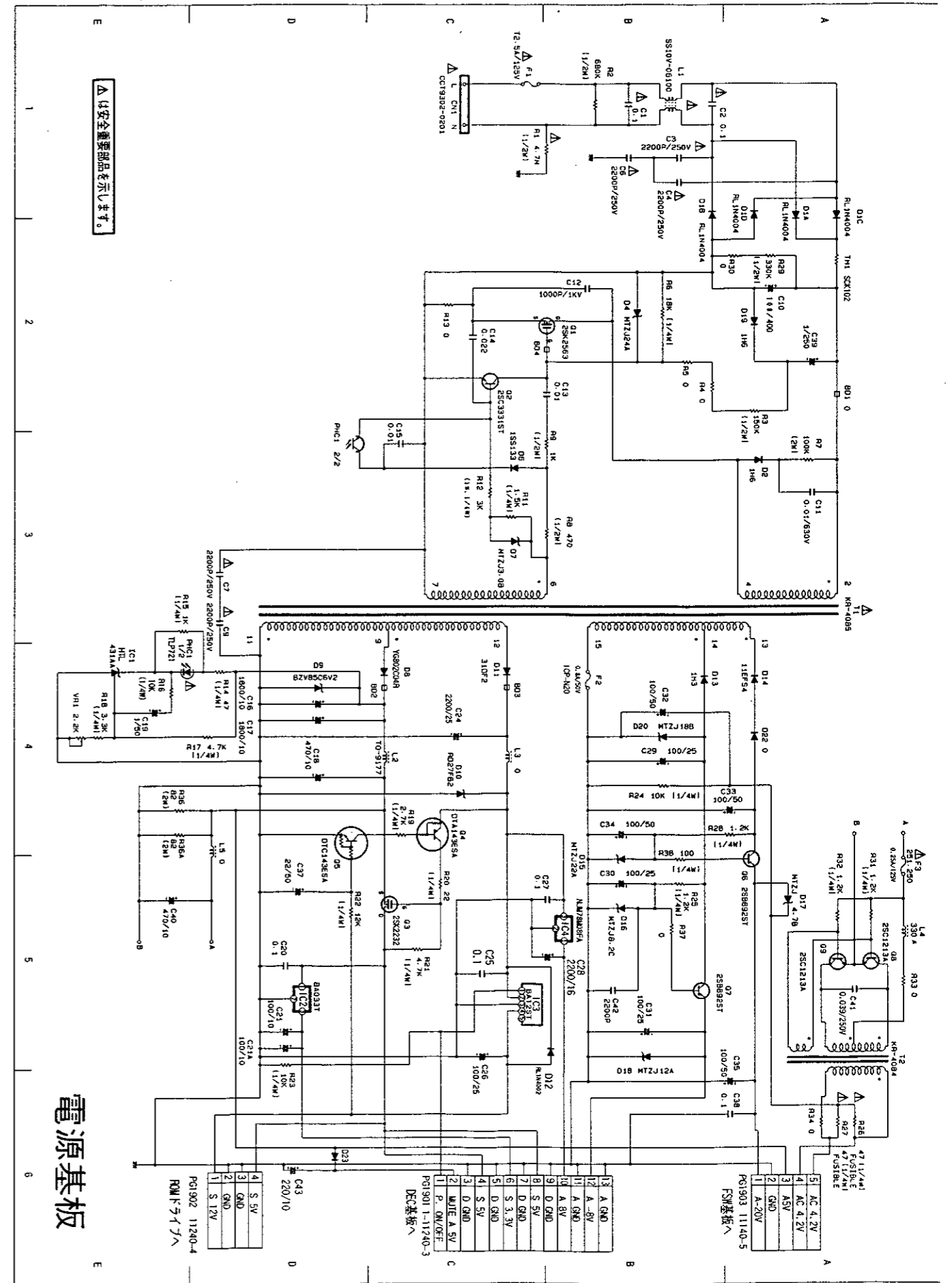
7-4 KEYCON ALTERNATIVE CIRCUIT (KEY CONTROL PRESET AT CENTER)

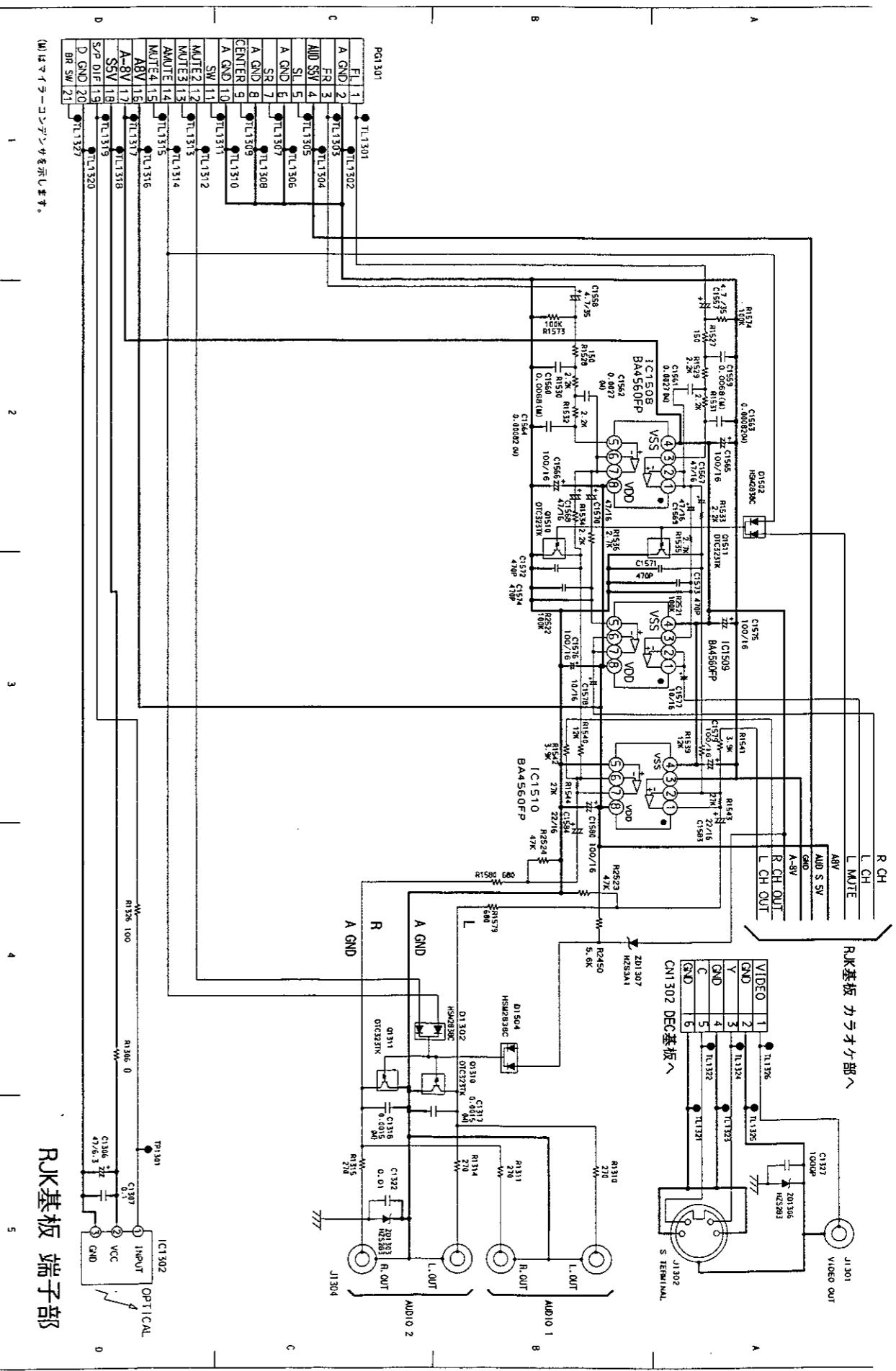


7-5 VOICE SW CIRCUIT The following is in case of mike sound input.



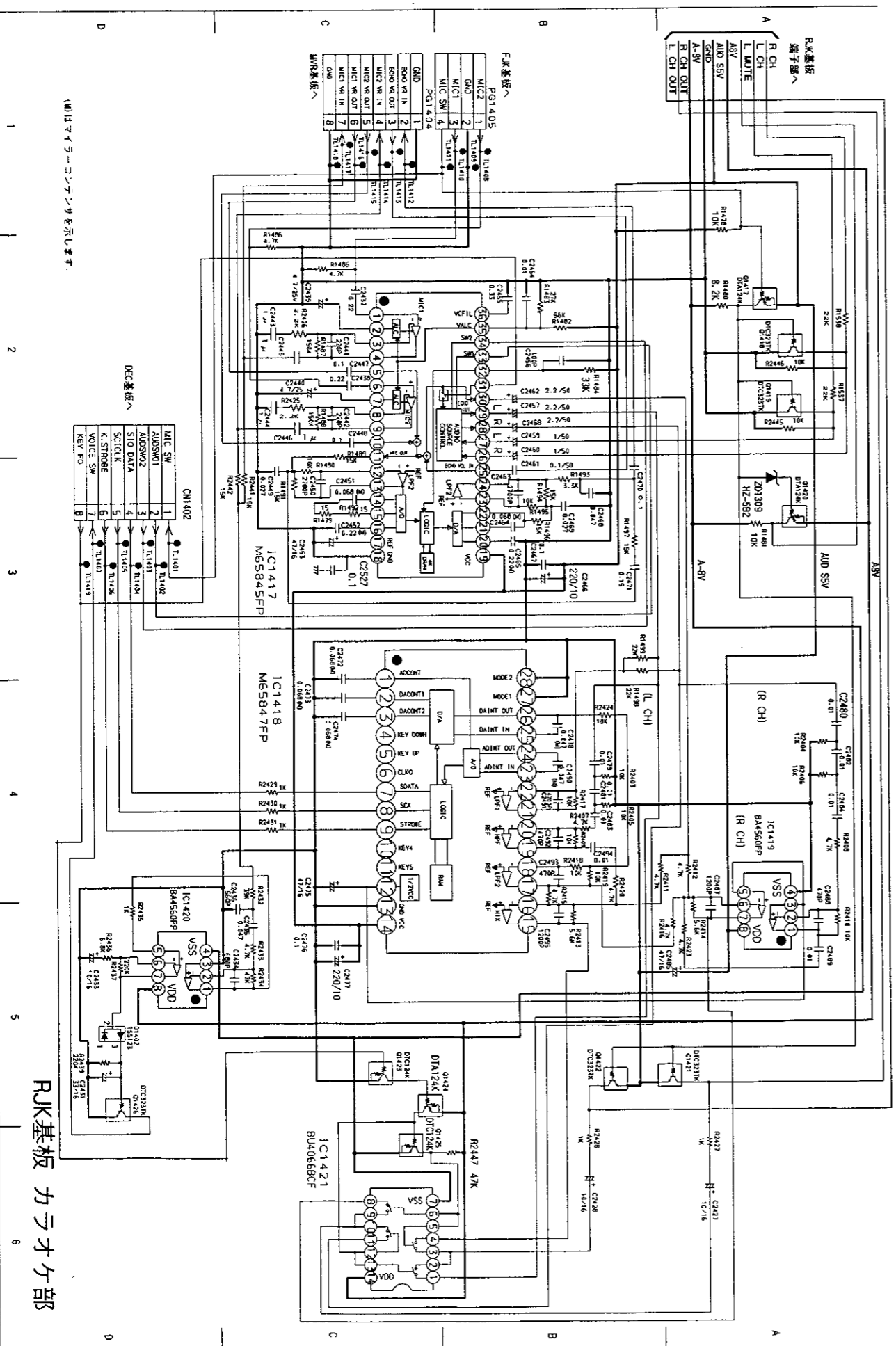
8. 基本回路図





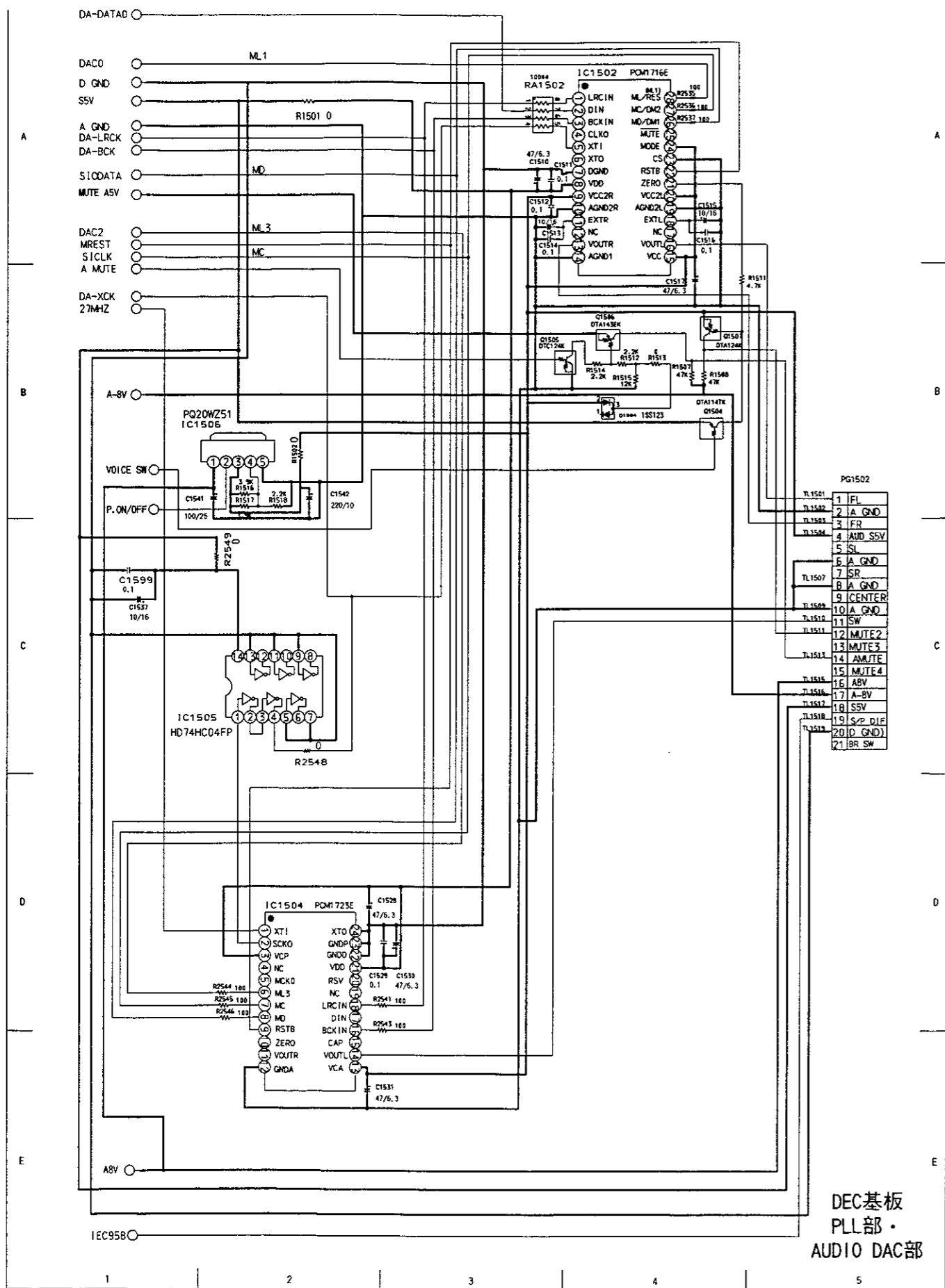
RJK基板 端子部

(例)はマイコンチップを示しています。



RJK基板 カラオケ部

(例)はマイコンチップを示します。

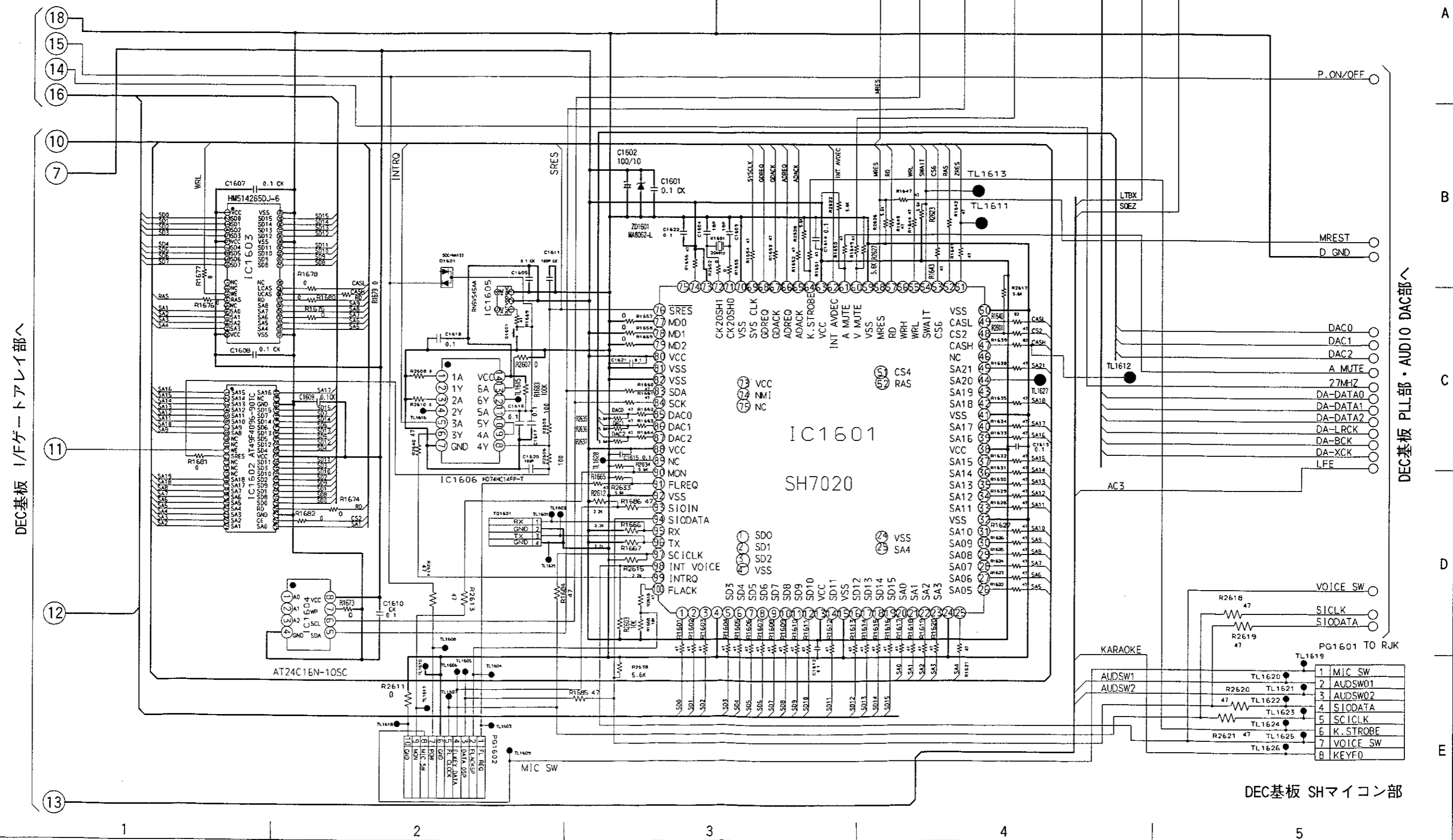


DEC基板
PLL部・
AUDIO DAC部

| PG1502 | |
|--------|------------|
| TL1501 | 1 FL |
| TL1502 | 2 A GND |
| TL1503 | 3 FR |
| TL1504 | 4 AUD SSV |
| | 5 SL |
| | 6 A GND |
| TL1507 | 7 SR |
| | 8 A GND |
| | 9 CENTER |
| TL1509 | 10 A GND |
| TL1510 | 11 SW |
| TL1511 | 12 MUTE2 |
| TL1511 | 13 MUTE3 |
| TL1511 | 14 AMUTE |
| TL1511 | 15 MUTE4 |
| TL1515 | 16 ABV |
| TL1516 | 17 A-BV |
| TL1517 | 18 SSV |
| TL1518 | 19 S/P DIF |
| TL1519 | 20 D GND |
| | 21 BR SW |

DEC基板
AVデコーダ部
ビデオエンコーダ部へ

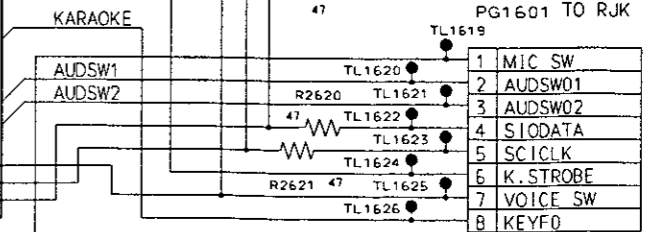
DEC基板 AVデコーダ部・ビデオエンコーダ部へ



DEC基板 I/Fゲートアレイ部へ

DEC基板 PLL部・AUDIO DAC部へ

DEC基板 SHマイコン部



A

B

C

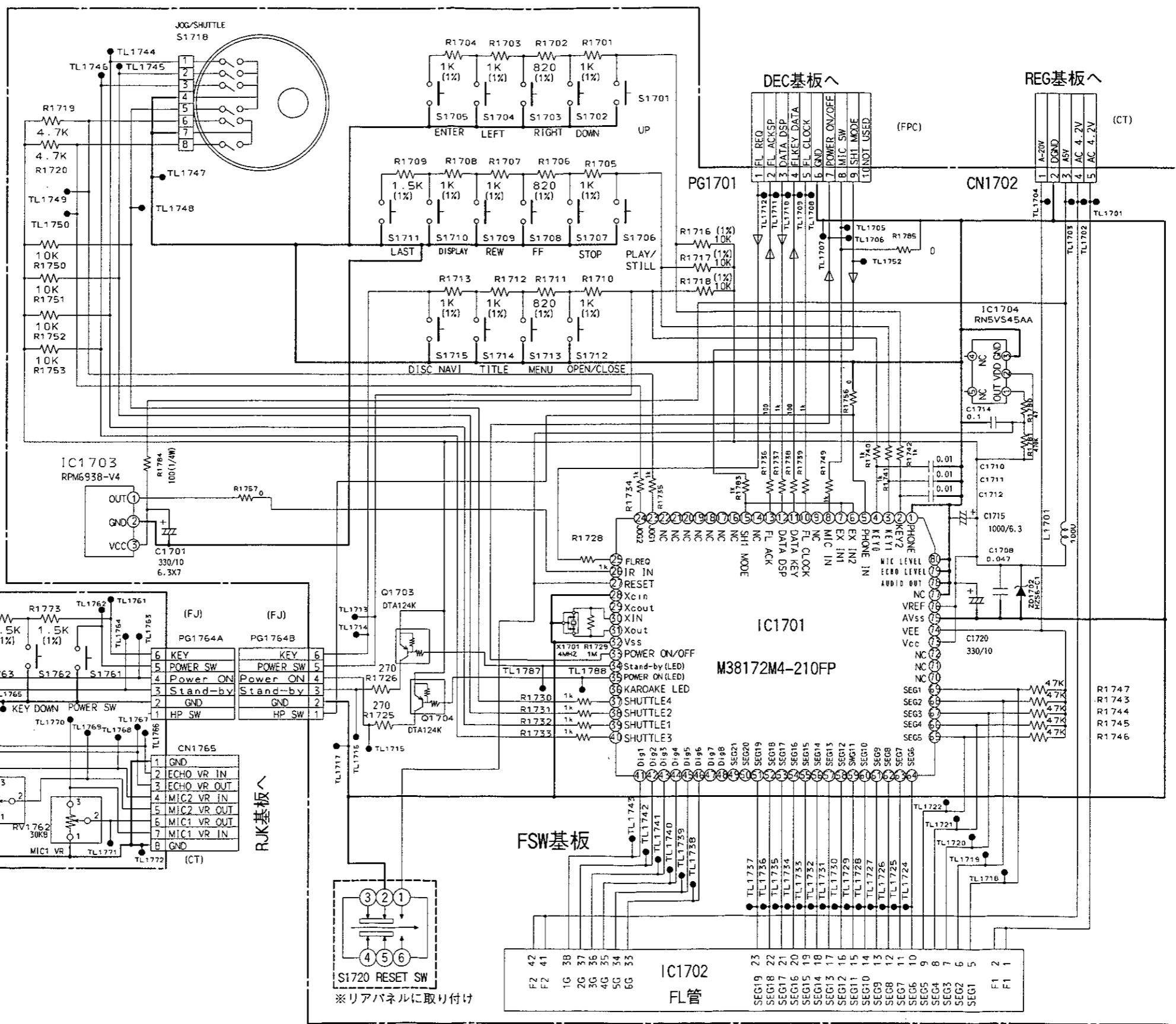
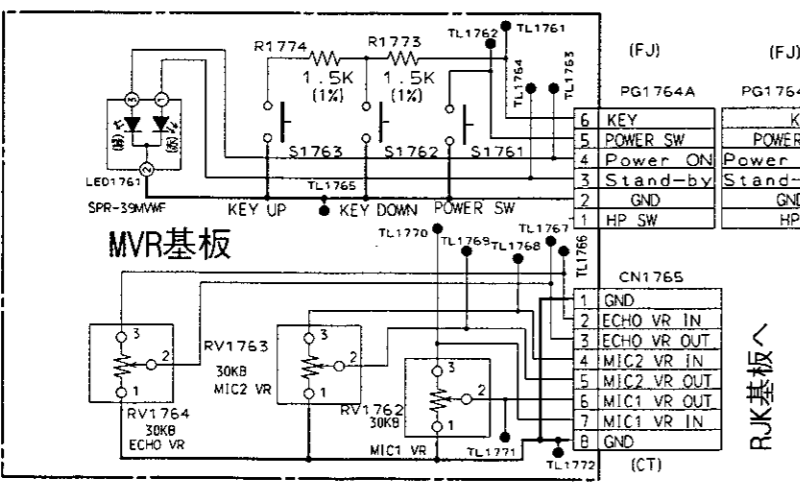
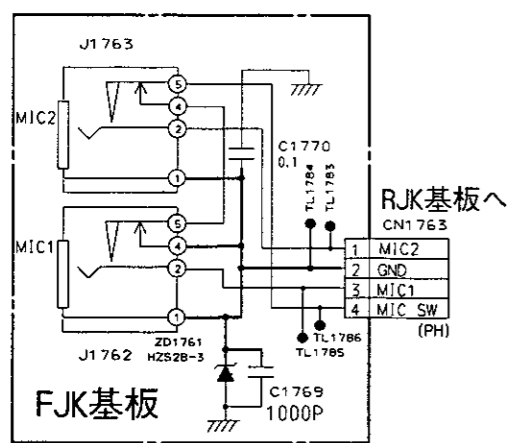
D

A

B

C

D



FSW基板・FJK基板・MVR基板

1

2

3

4

5

DEC基板 SHライコン部へ

| | |
|----|-----------|
| 13 | A GND |
| 12 | A-8V |
| 11 | A GND |
| 10 | A8V |
| 9 | D GND |
| 8 | S5V |
| 7 | D GND |
| 6 | S3.3V |
| 5 | D GND |
| 4 | S5V |
| 3 | D GND |
| 2 | A5V |
| 1 | P. ON/OFF |

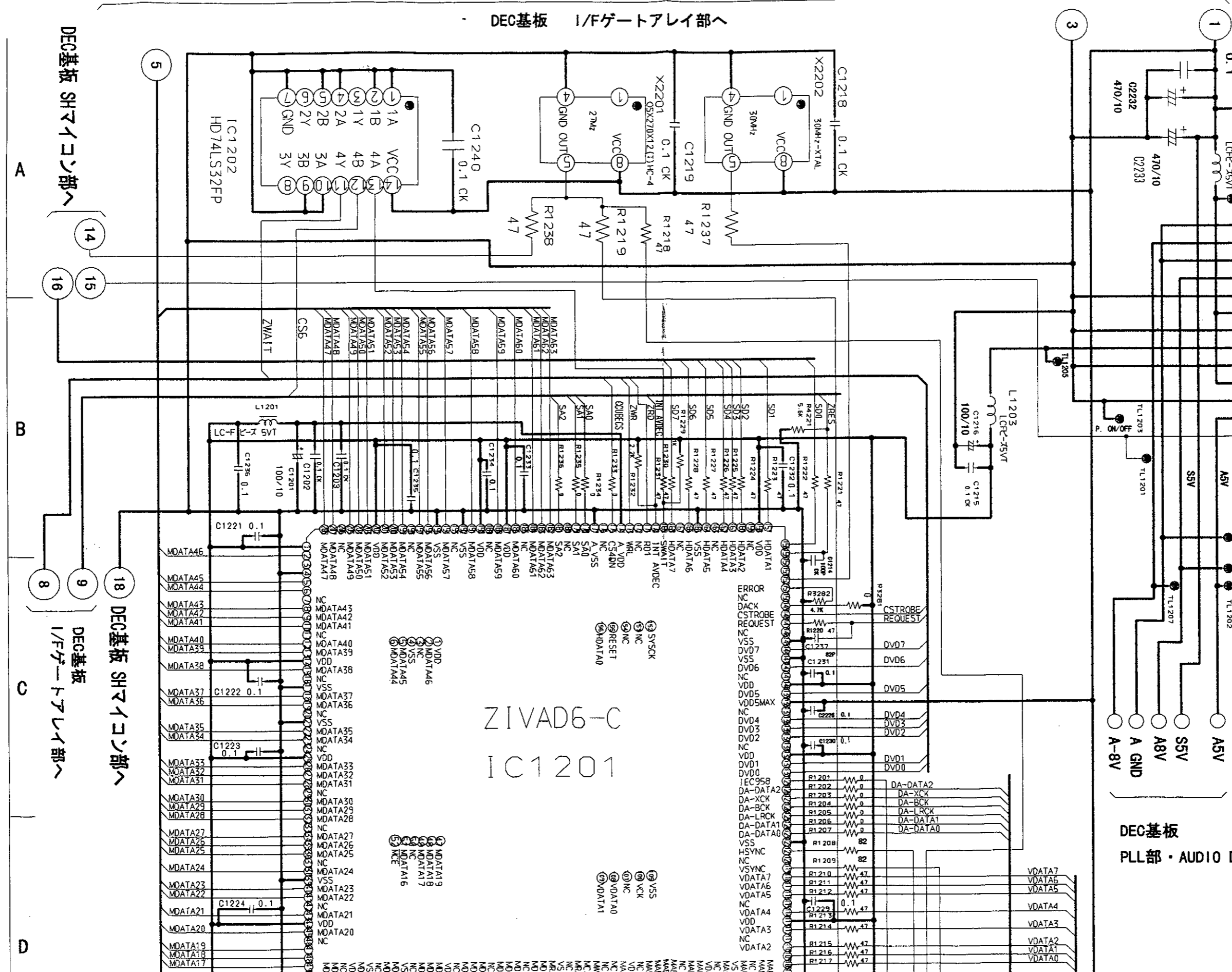
PG1201

DEC基板
PLL部・AUDIO DAC部へ

DEC基板 I/Fゲートアレイ部へ

DEC基板 SHライコン部へ

DEC基板 SHライコン部へ
DEC基板 I/Fゲートアレイ部へ



ZIVAD6-C
IC1201

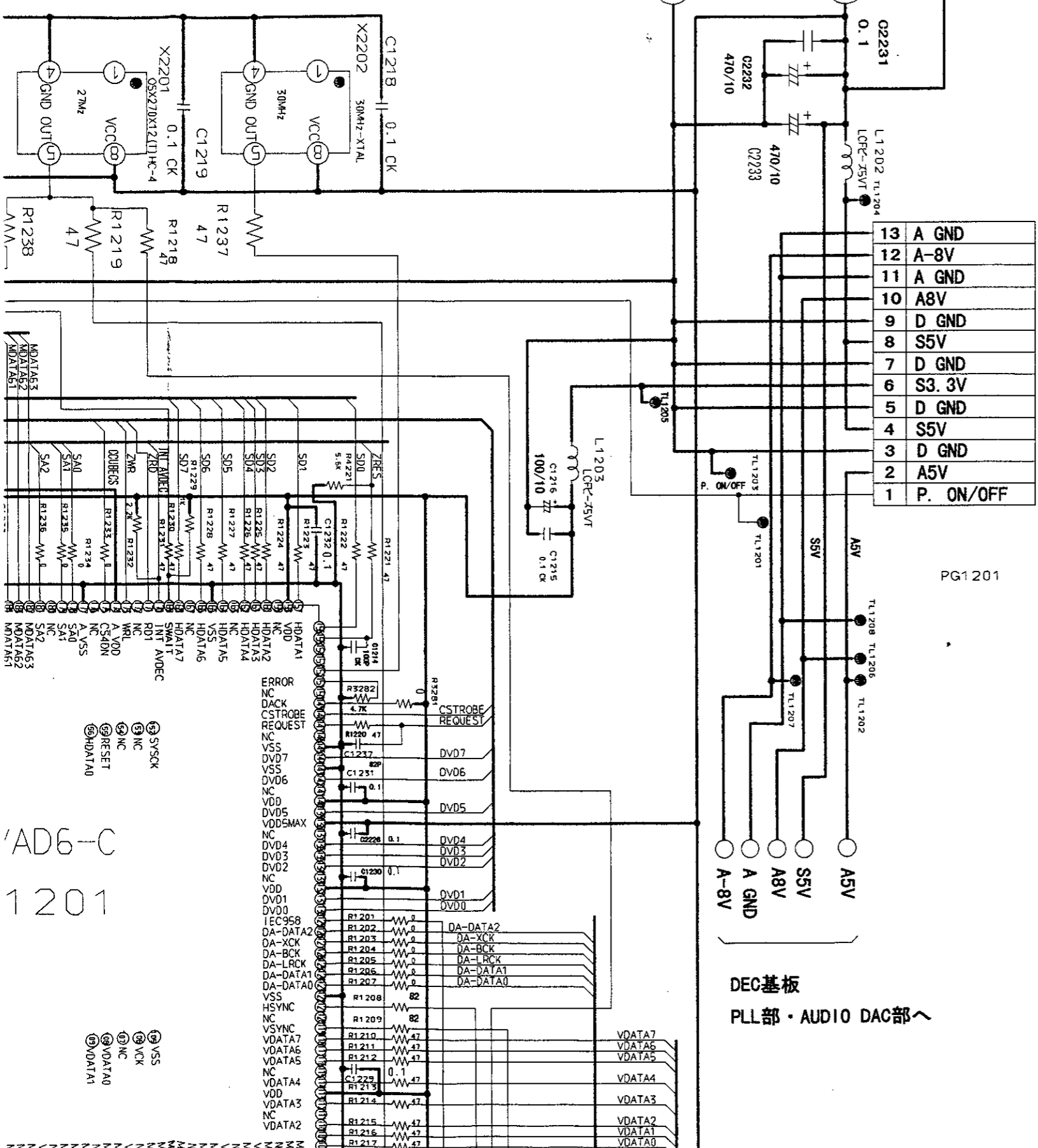
A

B

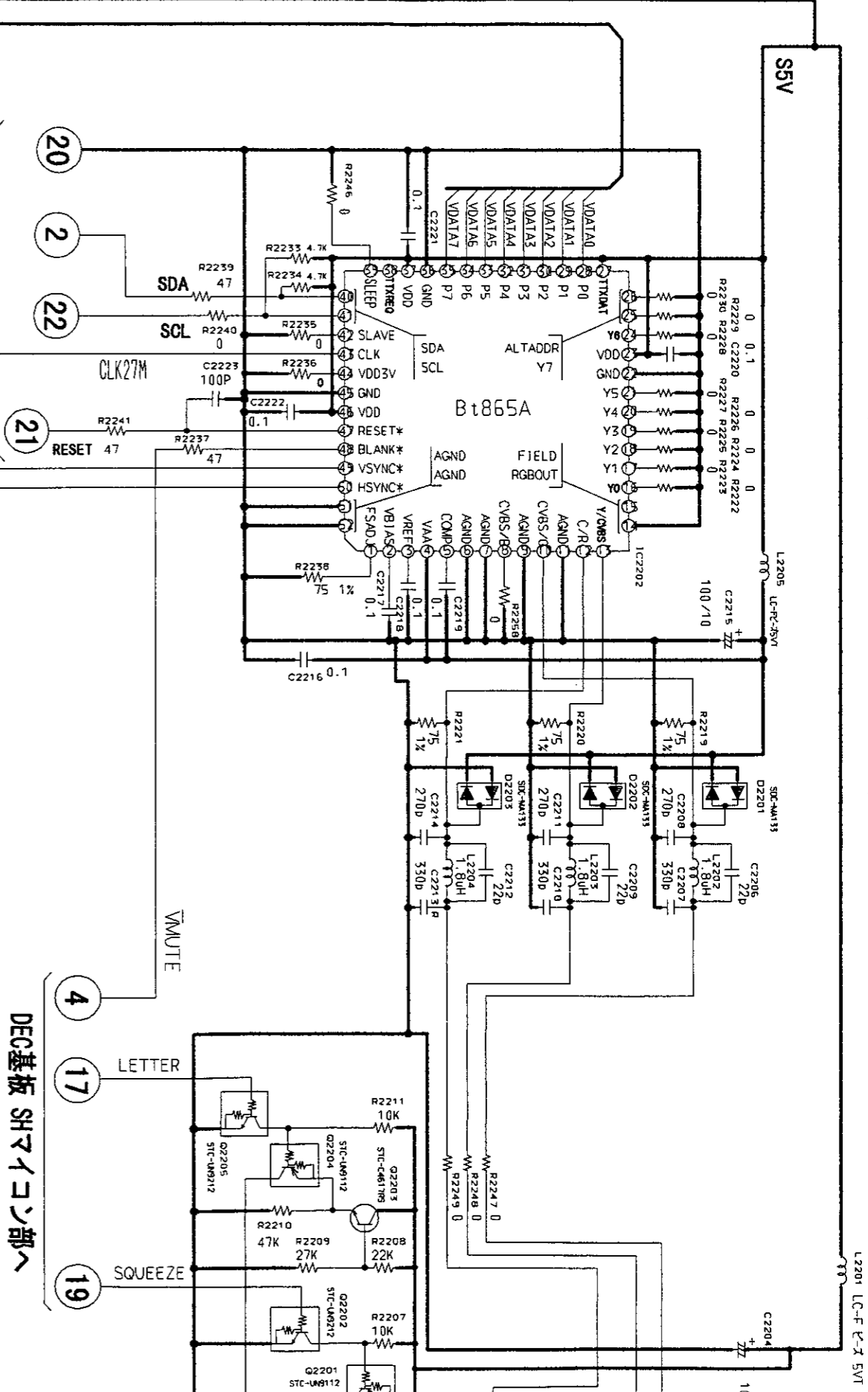
C

D

板 I/Fゲートアレイ部へ



DEC基板 SHマイコン部へ



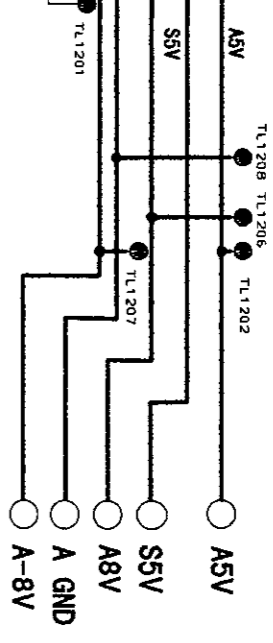
'AD6-C
1201

A
B
C
D

| | |
|---|-----------|
| 7 | D GND |
| 6 | S3.3V |
| 5 | D GND |
| 4 | S5V |
| 3 | D GND |
| 2 | A5V |
| 1 | P. ON/OFF |

PG1201

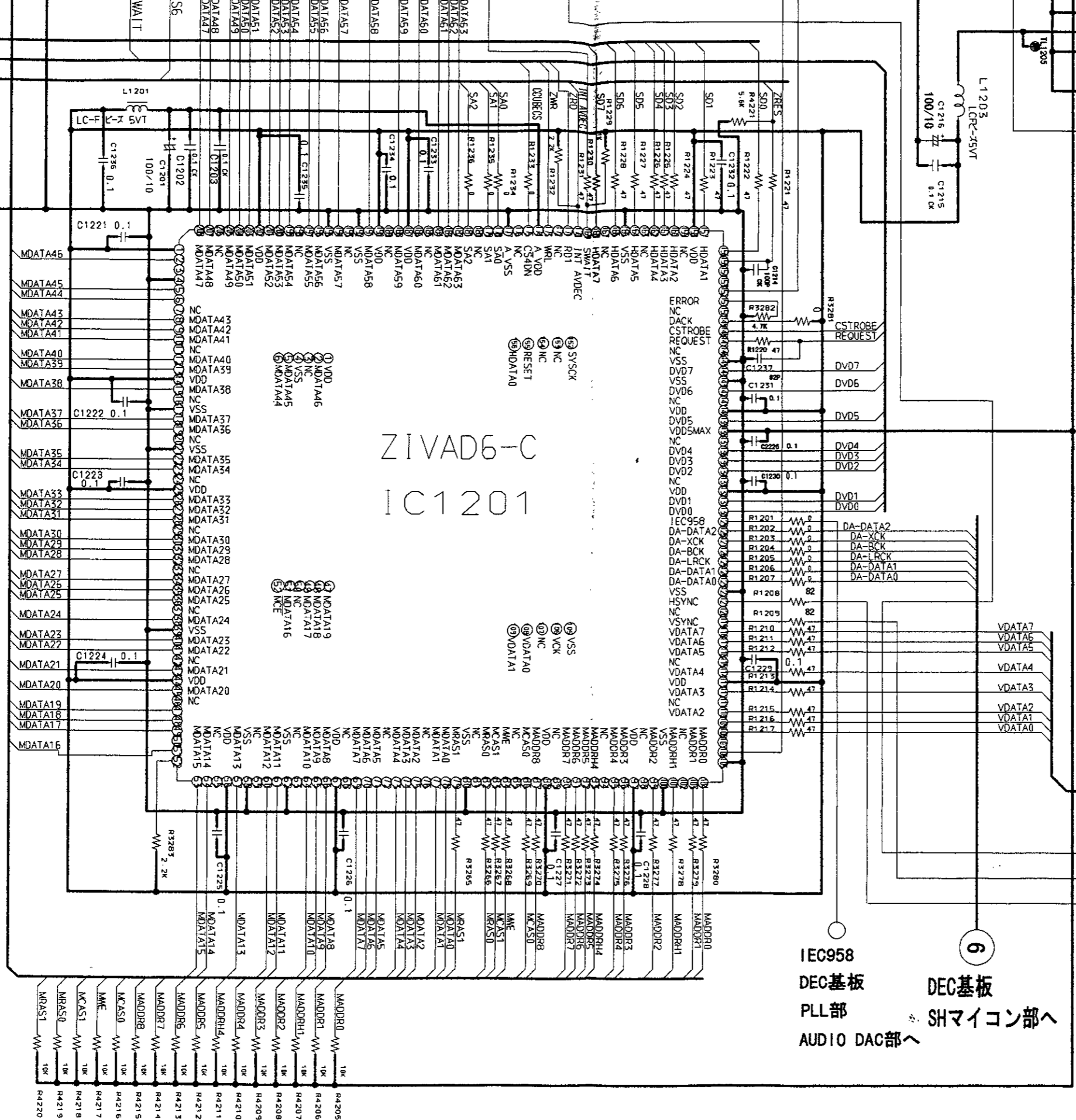
DEC基板 SHマイコン部へ



DEC基板
PLL部・AUDIO DAC部へ

DEC基板
SHマイコン部へ

IEC958
DEC基板
PLL部
AUDIO DAC部へ



DEC基板 SHマイコン部へ
DEC基板
I/Fデータライン部へ

E

D

C

B

1

2

3

4

| | |
|---|-----------|
| 7 | D GND |
| 6 | S3.3V |
| 5 | D GND |
| 4 | S5V |
| 3 | D GND |
| 2 | A5V |
| 1 | P. ON/OFF |

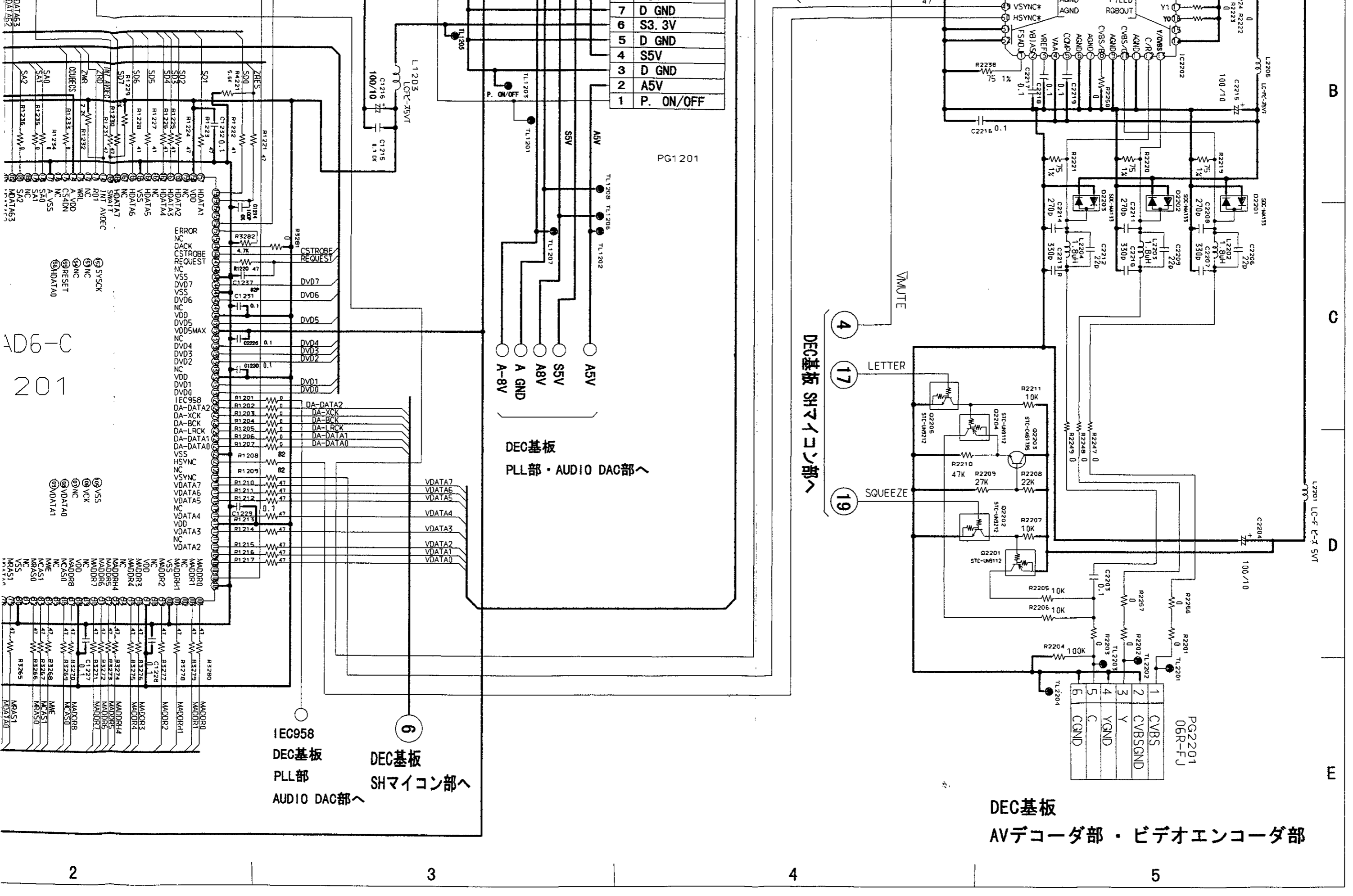
PG1201

DEC基板
PLL部・AUDIO DAC部へ

DEC基板
SHマイコン部へ

DEC基板
PLL部
AUDIO DAC部へ

DEC基板
AVデコーダ部・ビデオエンコーダ部



AD6-C
201

2

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4

5

B

C

D

E

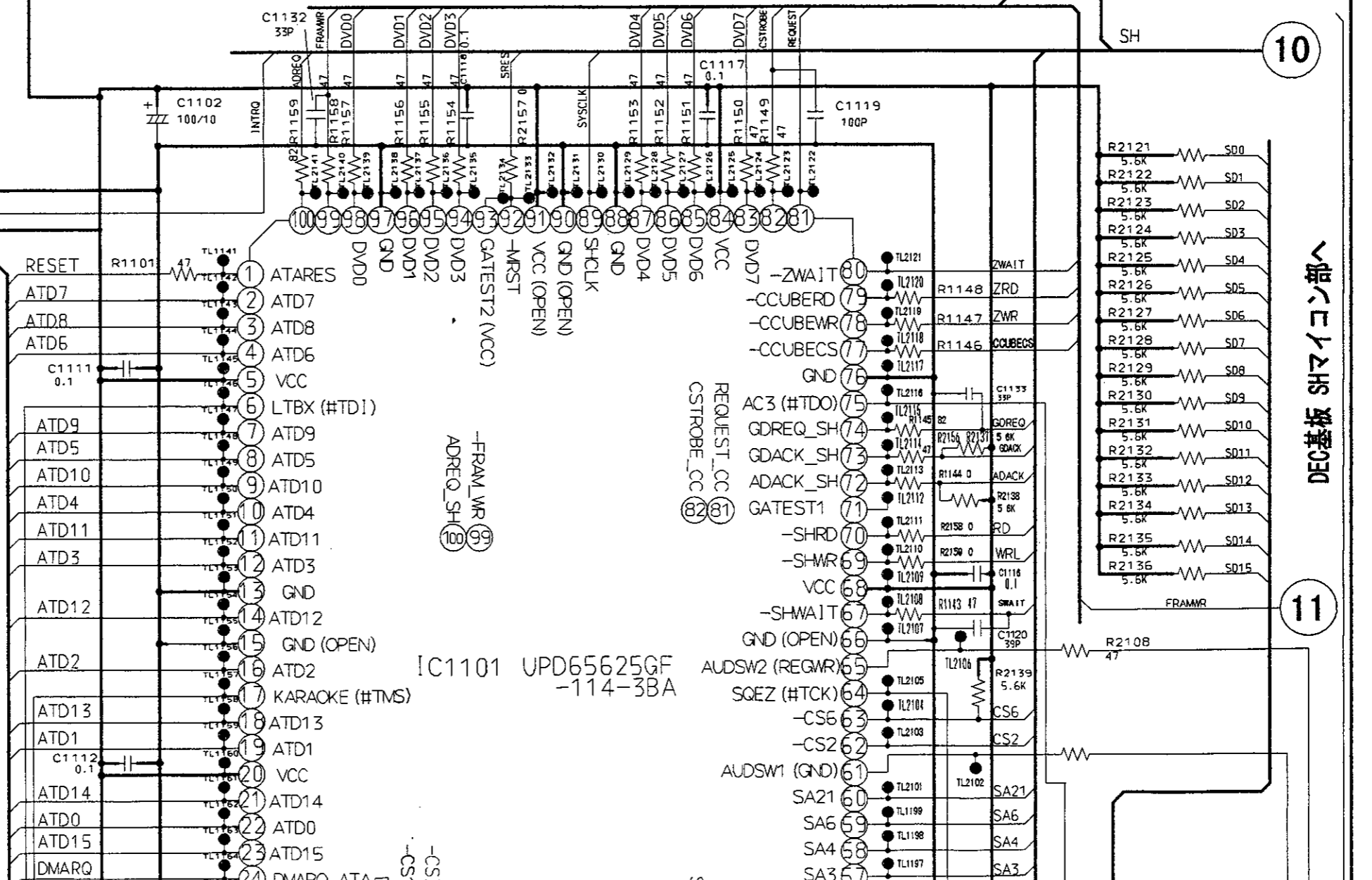
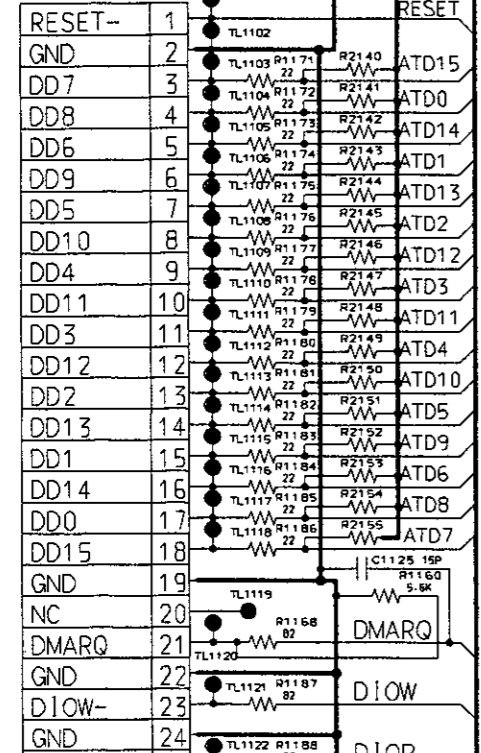
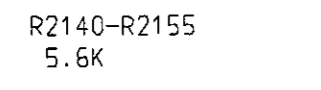
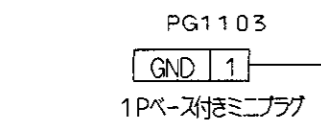
DEC基板
AVデコーダ部
ビデオエンコーダ部へ

A

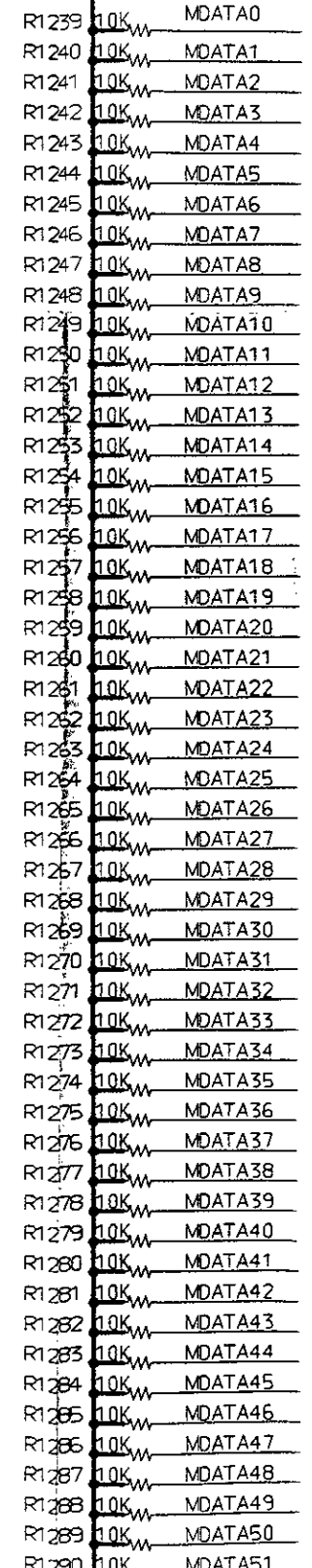
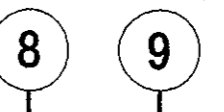
B

C

D

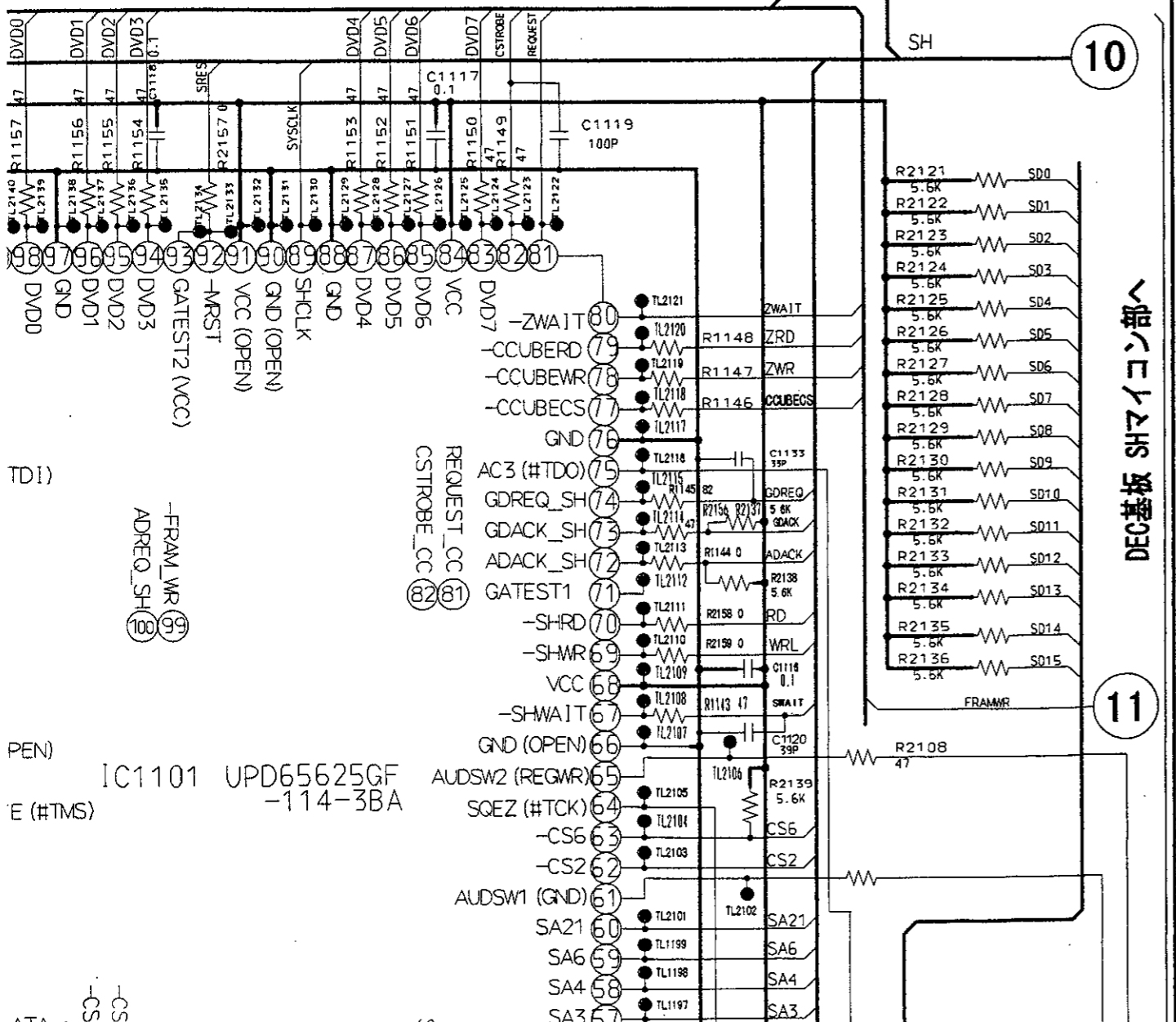


DEC基板 SHマイコン部へ



DEC基板
AVデコーダ部
ビデオエンコーダ部へ

8 9

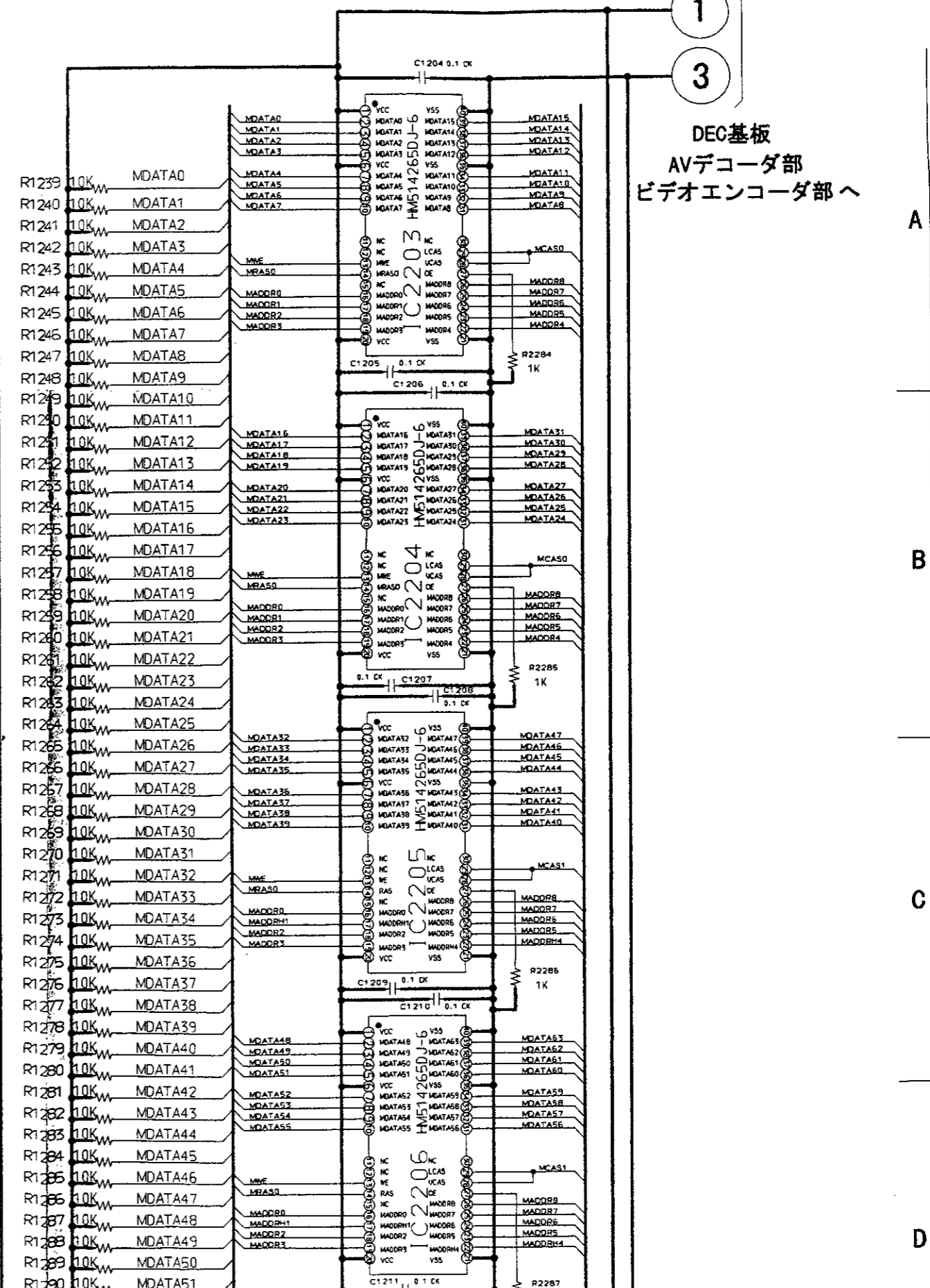


DEC基板 SHマイコン部へ

11

DEC基板
AVデコーダ部
ビデオエンコーダ部へ

1 3

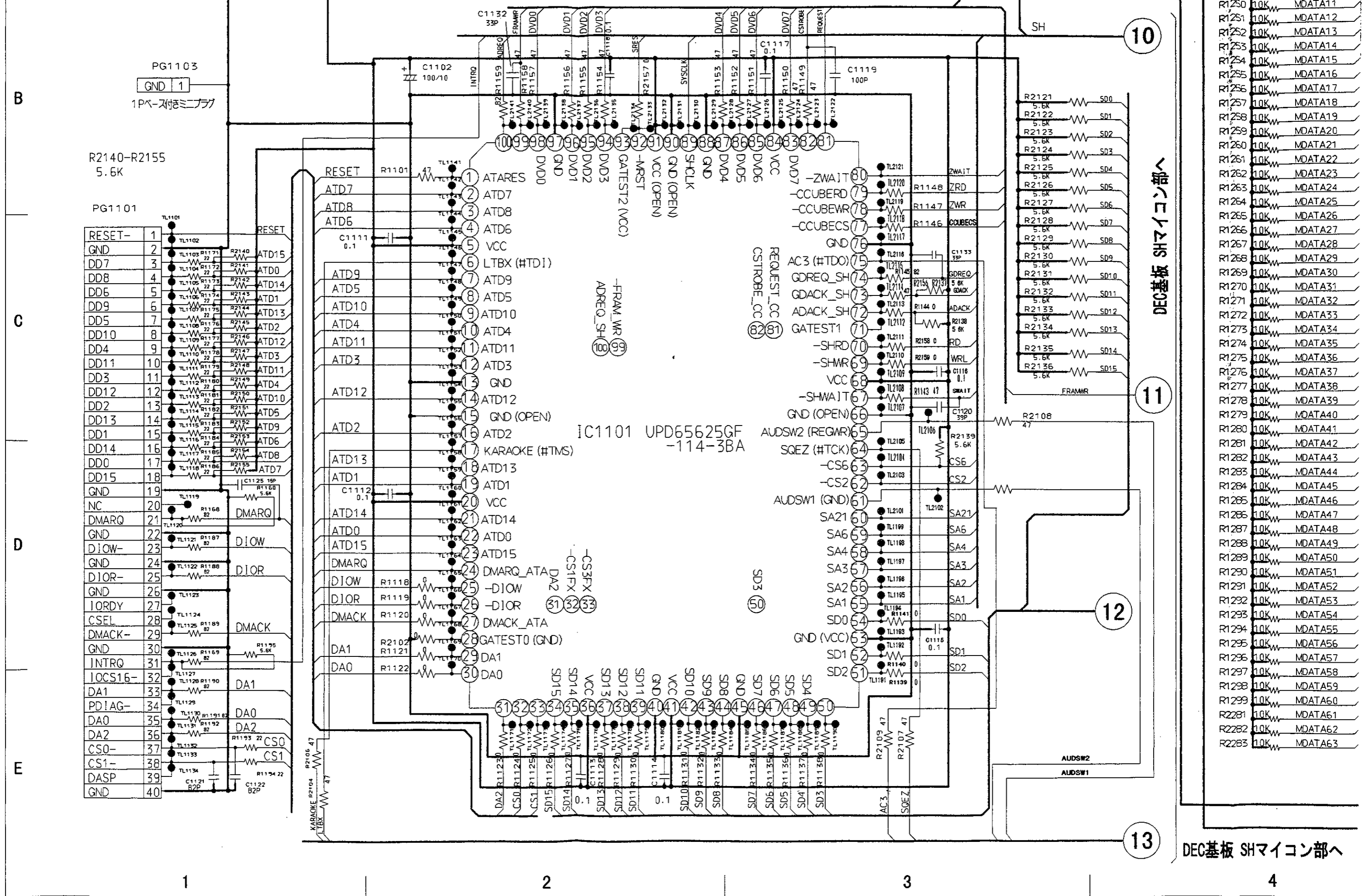


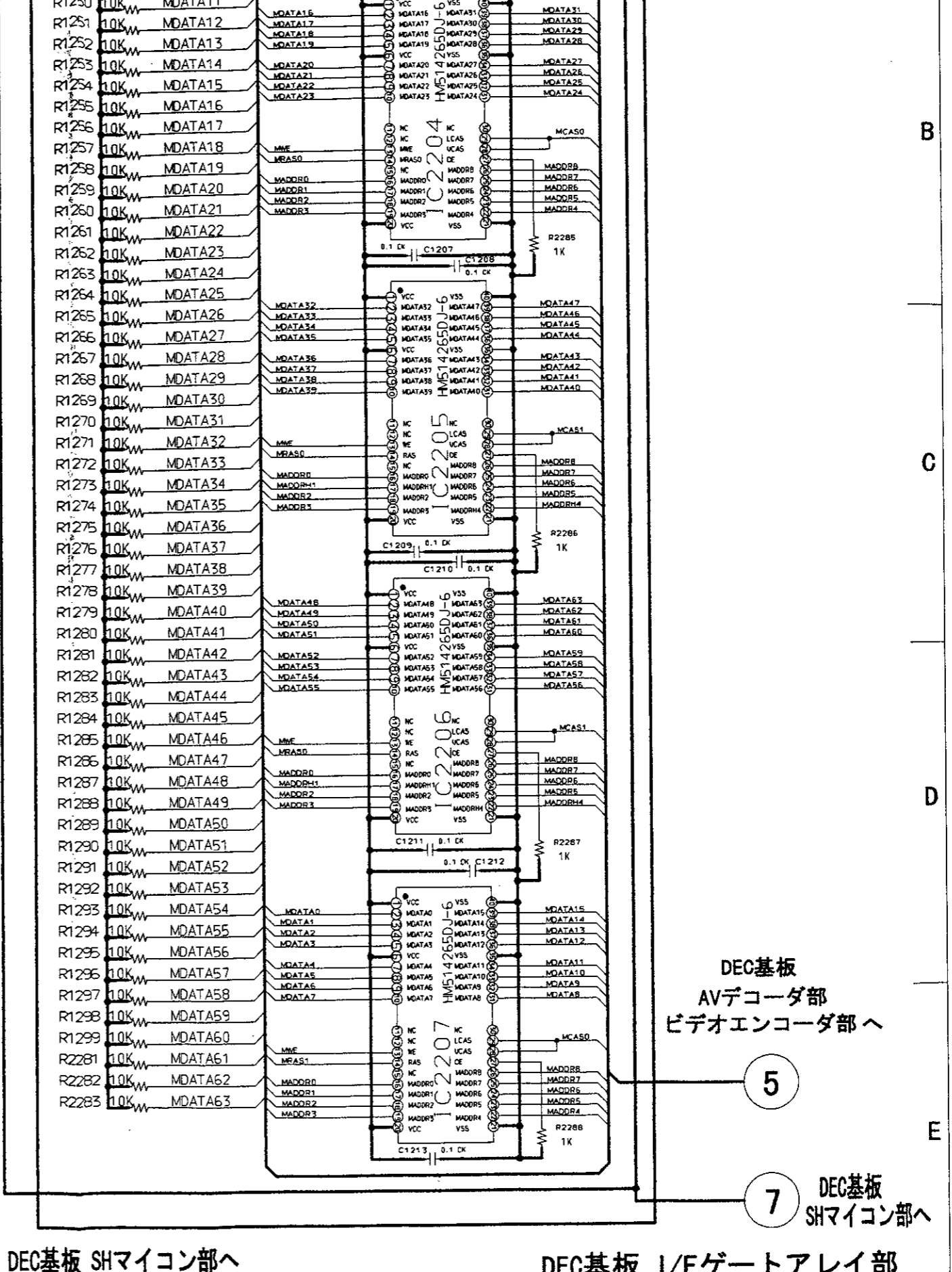
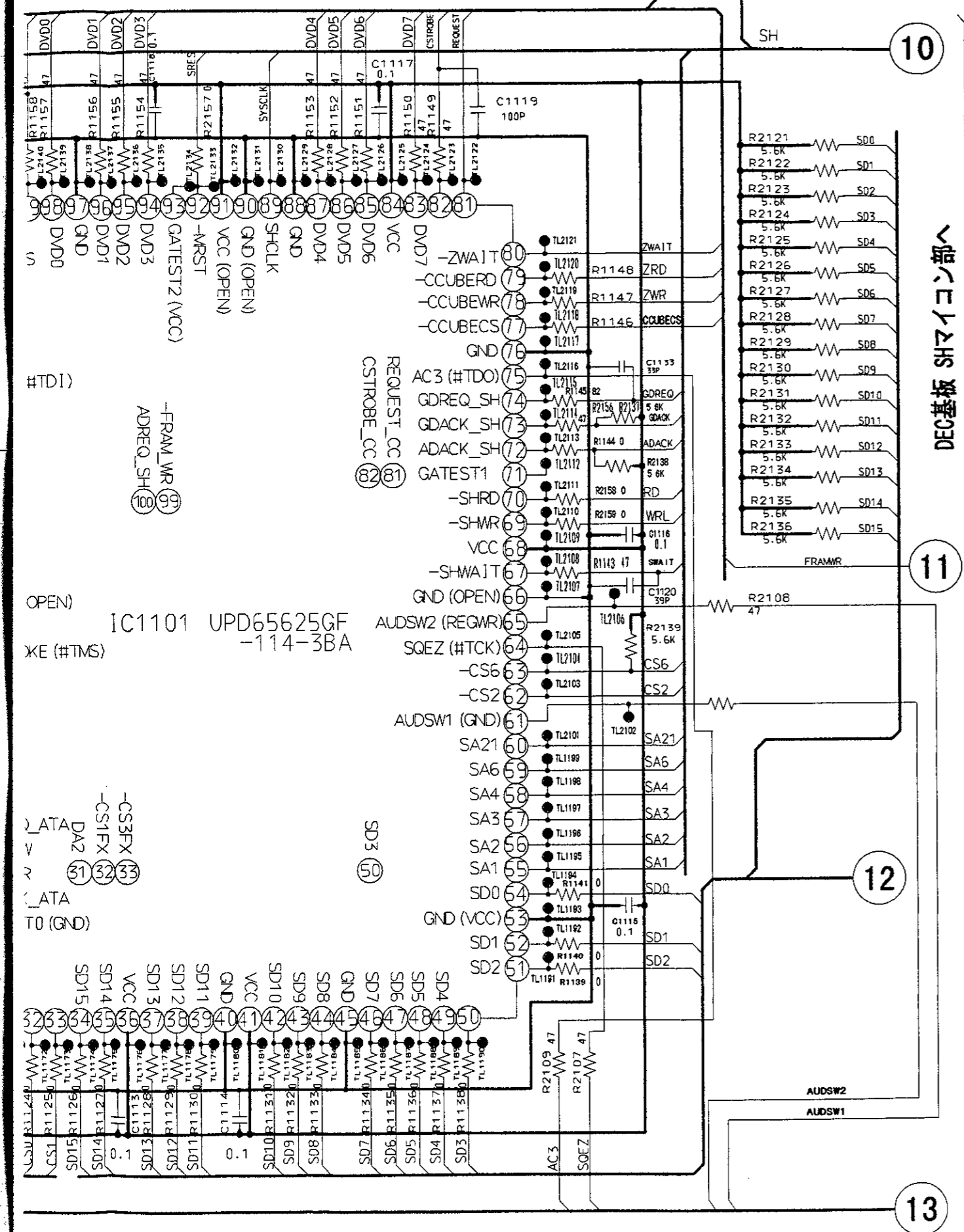
A

B

C

D





DEC基板 SHマイコン部へ

11

12

13

DEC基板 SHマイコン部へ

DEC基板
AVデコーダ部
ビデオエンコーダ部へ

5

7

DEC基板 I/Fゲートアレイ部

2

3

4

5

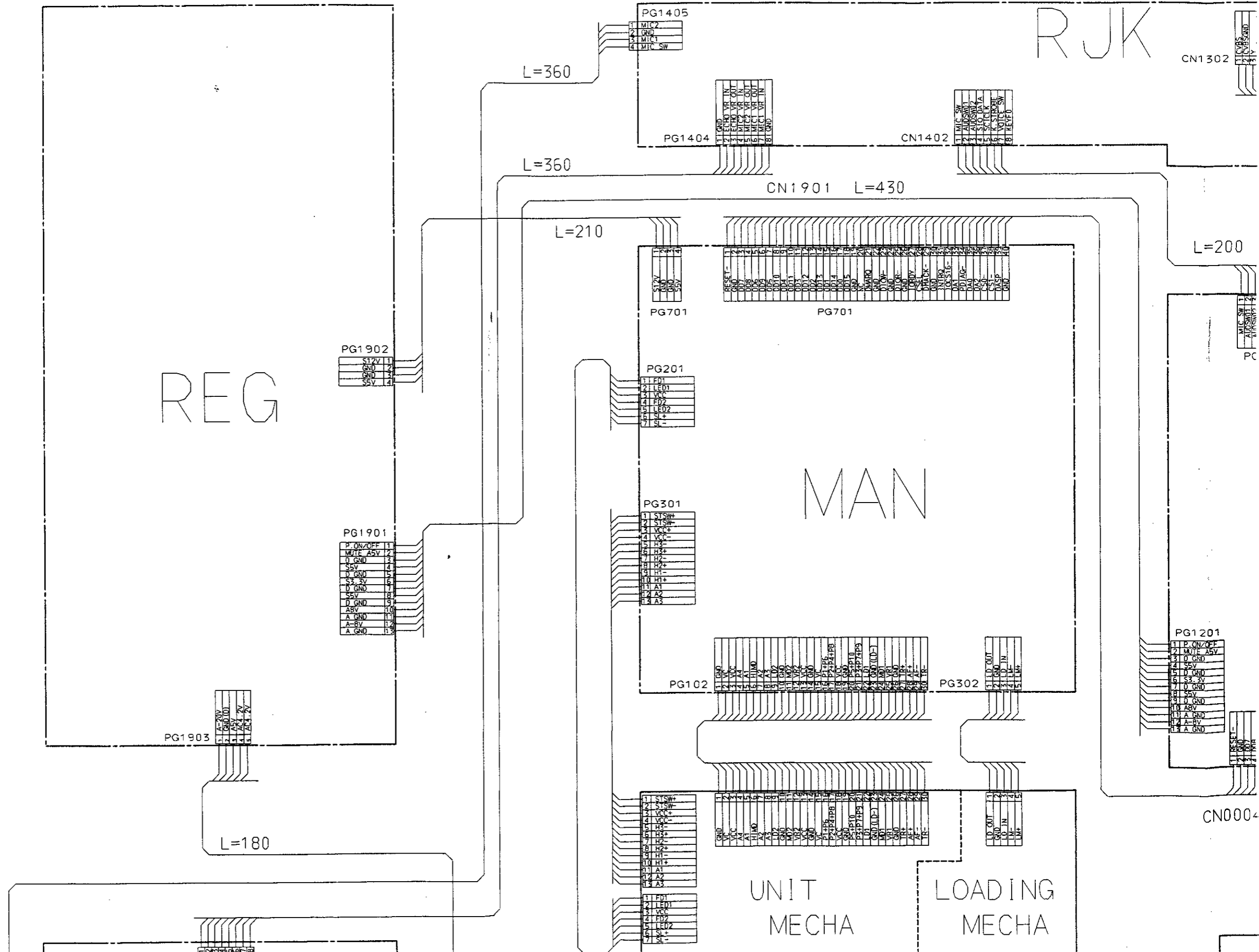
B

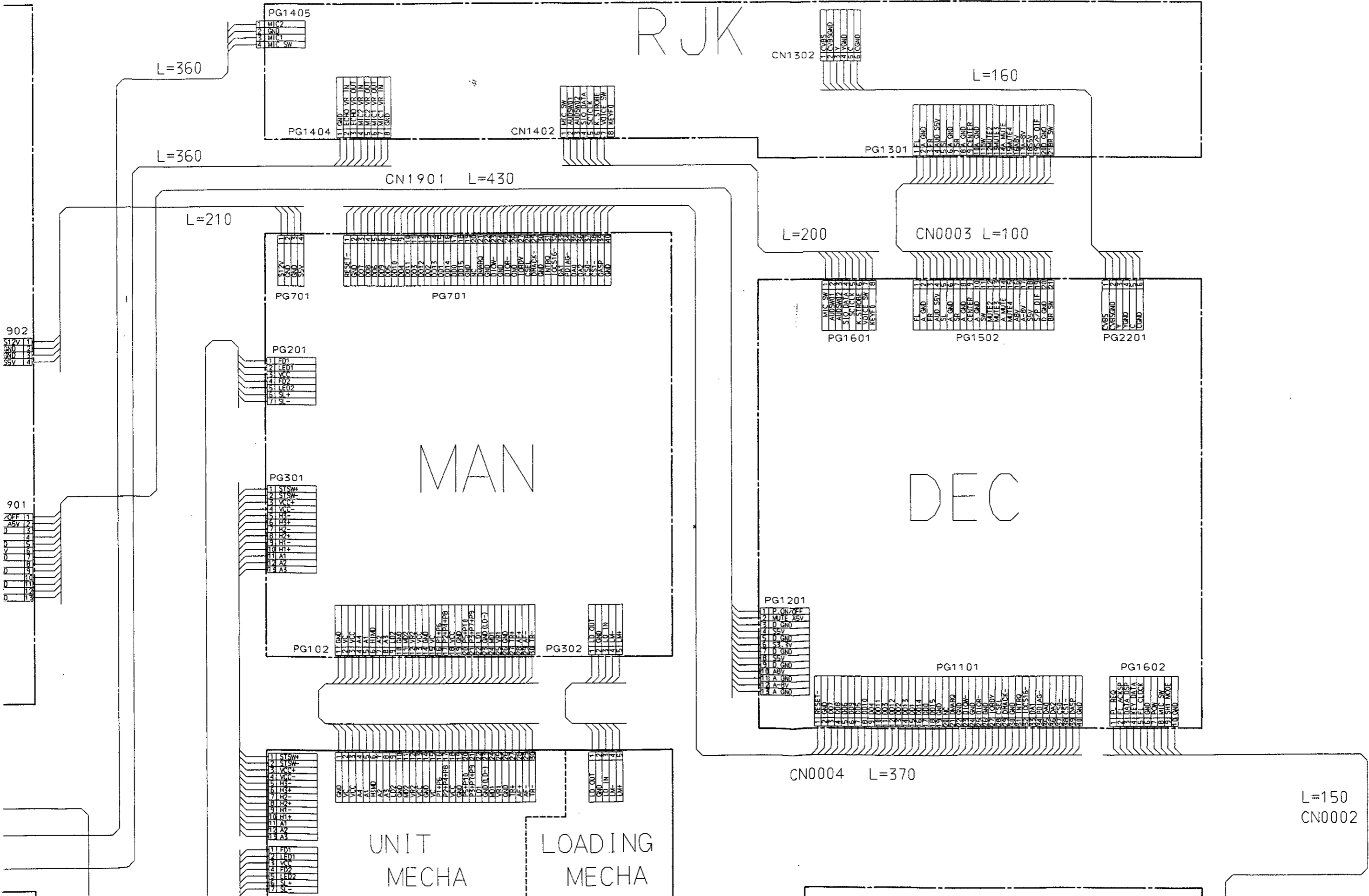
C

D

E

9. コネクタ結線図





REG

MAN

UNIT
MECHA

LOADING
MECHA

MVR

FSW

FJK

PG1902

| | |
|------|---|
| ST2V | 1 |
| GND | 2 |
| GND | 3 |
| SSV | 4 |

PG1901

| | |
|----------|----|
| P.ON/OFF | 1 |
| MUTE ASV | 2 |
| D.GND | 3 |
| SSV | 4 |
| D.GND | 5 |
| SSV | 6 |
| D.GND | 7 |
| SSV | 8 |
| D.GND | 9 |
| AVV | 10 |
| A.GND | 11 |
| A-BV | 12 |
| A.GND | 13 |

PG1903

| | |
|--------|---|
| A-20V | 1 |
| GND(0) | 2 |
| ASV | 3 |
| A-1.2V | 4 |
| A-1.2V | 5 |

L=180

PG201

| |
|--------|
| 1 LED1 |
| 2 LED1 |
| 3 VCC |
| 4 PD2 |
| 5 LED2 |
| 6 SL+ |
| 7 SL- |

PG301

| |
|--------|
| 1 STSW |
| 2 STSW |
| 3 VCC |
| 4 VCC |
| 5 H+ |
| 6 H+ |
| 7 H2- |
| 8 H2+ |
| 9 H+ |
| 10 H+ |
| 11 A1 |
| 12 A2 |
| 13 A3 |

PG102

| | |
|-----|-----|
| GND | 1 |
| VCC | 2 |
| A1 | 3 |
| A2 | 4 |
| A3 | 5 |
| LD2 | 6 |
| LD1 | 7 |
| VCC | 8 |
| VCC | 9 |
| VCC | 10 |
| VCC | 11 |
| VCC | 12 |
| VCC | 13 |
| VCC | 14 |
| VCC | 15 |
| VCC | 16 |
| VCC | 17 |
| VCC | 18 |
| VCC | 19 |
| VCC | 20 |
| VCC | 21 |
| VCC | 22 |
| VCC | 23 |
| VCC | 24 |
| VCC | 25 |
| VCC | 26 |
| VCC | 27 |
| VCC | 28 |
| VCC | 29 |
| VCC | 30 |
| VCC | 31 |
| VCC | 32 |
| VCC | 33 |
| VCC | 34 |
| VCC | 35 |
| VCC | 36 |
| VCC | 37 |
| VCC | 38 |
| VCC | 39 |
| VCC | 40 |
| VCC | 41 |
| VCC | 42 |
| VCC | 43 |
| VCC | 44 |
| VCC | 45 |
| VCC | 46 |
| VCC | 47 |
| VCC | 48 |
| VCC | 49 |
| VCC | 50 |
| VCC | 51 |
| VCC | 52 |
| VCC | 53 |
| VCC | 54 |
| VCC | 55 |
| VCC | 56 |
| VCC | 57 |
| VCC | 58 |
| VCC | 59 |
| VCC | 60 |
| VCC | 61 |
| VCC | 62 |
| VCC | 63 |
| VCC | 64 |
| VCC | 65 |
| VCC | 66 |
| VCC | 67 |
| VCC | 68 |
| VCC | 69 |
| VCC | 70 |
| VCC | 71 |
| VCC | 72 |
| VCC | 73 |
| VCC | 74 |
| VCC | 75 |
| VCC | 76 |
| VCC | 77 |
| VCC | 78 |
| VCC | 79 |
| VCC | 80 |
| VCC | 81 |
| VCC | 82 |
| VCC | 83 |
| VCC | 84 |
| VCC | 85 |
| VCC | 86 |
| VCC | 87 |
| VCC | 88 |
| VCC | 89 |
| VCC | 90 |
| VCC | 91 |
| VCC | 92 |
| VCC | 93 |
| VCC | 94 |
| VCC | 95 |
| VCC | 96 |
| VCC | 97 |
| VCC | 98 |
| VCC | 99 |
| VCC | 100 |

PG302

| | |
|--------|---|
| LD OUT | 1 |
| LD IN | 2 |
| LD IN | 3 |
| LD IN | 4 |
| LD IN | 5 |
| LD IN | 6 |

PG1201

| | |
|----------|----|
| P.ON/OFF | 1 |
| MUTE ASV | 2 |
| D.GND | 3 |
| SSV | 4 |
| D.GND | 5 |
| SSV | 6 |
| D.GND | 7 |
| SSV | 8 |
| D.GND | 9 |
| AVV | 10 |
| A.GND | 11 |
| A-BV | 12 |
| A.GND | 13 |

CN0004

CN1765

| | |
|-------------|---|
| ECRD VR IN | 1 |
| ECRD VR OUT | 2 |
| MIC VR IN | 3 |
| MIC VR OUT | 4 |
| MIC VR IN | 5 |
| MIC VR IN | 6 |
| GND | 7 |

CN1702

| | |
|--------|---|
| A-20V | 1 |
| GND(0) | 2 |
| ASV | 3 |
| A-1.2V | 4 |
| A-1.2V | 5 |

PG1764A

| | |
|----------|---|
| KEY | 1 |
| POWER SW | 2 |
| POWER ON | 3 |
| STAND-BY | 4 |
| GND | 5 |
| HP SW | 6 |

PG1764B

| | |
|----------|---|
| KEY | 1 |
| POWER SW | 2 |
| POWER ON | 3 |
| STAND-BY | 4 |
| GND | 5 |
| HP SW | 6 |

CN1763

| | |
|--------|---|
| MIC | 1 |
| GND | 2 |
| MIC | 3 |
| MIC SW | 4 |

1902
 STV 1
 GND 2
 GND 3
 SV 4

1901
 IN/OFF 1
 IF ASV 2
 GND 3
 GND 4
 GND 5
 GND 6
 GND 7
 GND 8
 GND 9
 GND 10
 GND 11
 GND 12
 GND 13

1764A
 ER SW 6
 ER ON 4
 ND-BY 3
 SW 1

PG201

| | |
|---|-----|
| 1 | ED1 |
| 2 | ED1 |
| 3 | VCC |
| 4 | ED2 |
| 5 | ED2 |
| 6 | ED2 |
| 7 | ED2 |

PG301

| | |
|----|-------|
| 1 | ST SW |
| 2 | ST SW |
| 3 | VCC+ |
| 4 | VCC |
| 5 | HT+ |
| 6 | HT+ |
| 7 | HT+ |
| 8 | HT+ |
| 9 | HT+ |
| 10 | HT+ |
| 11 | HT+ |
| 12 | AT |
| 13 | AZ |
| 14 | AZ |

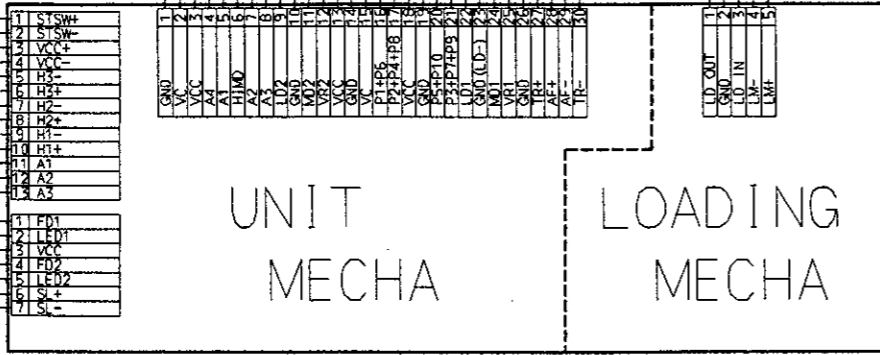
| | |
|----|-------|
| 1 | ST SW |
| 2 | ST SW |
| 3 | VCC+ |
| 4 | VCC |
| 5 | HT+ |
| 6 | HT+ |
| 7 | HT+ |
| 8 | HT+ |
| 9 | HT+ |
| 10 | HT+ |
| 11 | HT+ |
| 12 | AT |
| 13 | AZ |
| 14 | AZ |

PG102

| | |
|-----|------|
| 1 | GND |
| 2 | VCC |
| 3 | VCC |
| 4 | AT |
| 5 | HIND |
| 6 | AZ |
| 7 | AZ |
| 8 | UD |
| 9 | UD |
| 10 | VCC |
| 11 | VCC |
| 12 | GND |
| 13 | VCC |
| 14 | VCC |
| 15 | VCC |
| 16 | VCC |
| 17 | VCC |
| 18 | VCC |
| 19 | VCC |
| 20 | VCC |
| 21 | VCC |
| 22 | VCC |
| 23 | VCC |
| 24 | VCC |
| 25 | VCC |
| 26 | VCC |
| 27 | VCC |
| 28 | VCC |
| 29 | VCC |
| 30 | VCC |
| 31 | VCC |
| 32 | VCC |
| 33 | VCC |
| 34 | VCC |
| 35 | VCC |
| 36 | VCC |
| 37 | VCC |
| 38 | VCC |
| 39 | VCC |
| 40 | VCC |
| 41 | VCC |
| 42 | VCC |
| 43 | VCC |
| 44 | VCC |
| 45 | VCC |
| 46 | VCC |
| 47 | VCC |
| 48 | VCC |
| 49 | VCC |
| 50 | VCC |
| 51 | VCC |
| 52 | VCC |
| 53 | VCC |
| 54 | VCC |
| 55 | VCC |
| 56 | VCC |
| 57 | VCC |
| 58 | VCC |
| 59 | VCC |
| 60 | VCC |
| 61 | VCC |
| 62 | VCC |
| 63 | VCC |
| 64 | VCC |
| 65 | VCC |
| 66 | VCC |
| 67 | VCC |
| 68 | VCC |
| 69 | VCC |
| 70 | VCC |
| 71 | VCC |
| 72 | VCC |
| 73 | VCC |
| 74 | VCC |
| 75 | VCC |
| 76 | VCC |
| 77 | VCC |
| 78 | VCC |
| 79 | VCC |
| 80 | VCC |
| 81 | VCC |
| 82 | VCC |
| 83 | VCC |
| 84 | VCC |
| 85 | VCC |
| 86 | VCC |
| 87 | VCC |
| 88 | VCC |
| 89 | VCC |
| 90 | VCC |
| 91 | VCC |
| 92 | VCC |
| 93 | VCC |
| 94 | VCC |
| 95 | VCC |
| 96 | VCC |
| 97 | VCC |
| 98 | VCC |
| 99 | VCC |
| 100 | VCC |

PG302

| | |
|-----|--------|
| 1 | LD OUT |
| 2 | GND |
| 3 | LD IN |
| 4 | LD IN |
| 5 | LD IN |
| 6 | LD IN |
| 7 | LD IN |
| 8 | LD IN |
| 9 | LD IN |
| 10 | LD IN |
| 11 | LD IN |
| 12 | LD IN |
| 13 | LD IN |
| 14 | LD IN |
| 15 | LD IN |
| 16 | LD IN |
| 17 | LD IN |
| 18 | LD IN |
| 19 | LD IN |
| 20 | LD IN |
| 21 | LD IN |
| 22 | LD IN |
| 23 | LD IN |
| 24 | LD IN |
| 25 | LD IN |
| 26 | LD IN |
| 27 | LD IN |
| 28 | LD IN |
| 29 | LD IN |
| 30 | LD IN |
| 31 | LD IN |
| 32 | LD IN |
| 33 | LD IN |
| 34 | LD IN |
| 35 | LD IN |
| 36 | LD IN |
| 37 | LD IN |
| 38 | LD IN |
| 39 | LD IN |
| 40 | LD IN |
| 41 | LD IN |
| 42 | LD IN |
| 43 | LD IN |
| 44 | LD IN |
| 45 | LD IN |
| 46 | LD IN |
| 47 | LD IN |
| 48 | LD IN |
| 49 | LD IN |
| 50 | LD IN |
| 51 | LD IN |
| 52 | LD IN |
| 53 | LD IN |
| 54 | LD IN |
| 55 | LD IN |
| 56 | LD IN |
| 57 | LD IN |
| 58 | LD IN |
| 59 | LD IN |
| 60 | LD IN |
| 61 | LD IN |
| 62 | LD IN |
| 63 | LD IN |
| 64 | LD IN |
| 65 | LD IN |
| 66 | LD IN |
| 67 | LD IN |
| 68 | LD IN |
| 69 | LD IN |
| 70 | LD IN |
| 71 | LD IN |
| 72 | LD IN |
| 73 | LD IN |
| 74 | LD IN |
| 75 | LD IN |
| 76 | LD IN |
| 77 | LD IN |
| 78 | LD IN |
| 79 | LD IN |
| 80 | LD IN |
| 81 | LD IN |
| 82 | LD IN |
| 83 | LD IN |
| 84 | LD IN |
| 85 | LD IN |
| 86 | LD IN |
| 87 | LD IN |
| 88 | LD IN |
| 89 | LD IN |
| 90 | LD IN |
| 91 | LD IN |
| 92 | LD IN |
| 93 | LD IN |
| 94 | LD IN |
| 95 | LD IN |
| 96 | LD IN |
| 97 | LD IN |
| 98 | LD IN |
| 99 | LD IN |
| 100 | LD IN |



MAN

UNIT MECHA

LOADING MECHA

FSW

PG1601

PG1502

PG2201

PG1201

| | |
|----|----------|
| 1 | P ON/OFF |
| 2 | MODE ASV |
| 3 | GND |
| 4 | SSV |
| 5 | GND |
| 6 | SSV |
| 7 | GND |
| 8 | SSV |
| 9 | GND |
| 10 | ASV |
| 11 | GND |
| 12 | A-BV |
| 13 | A-GND |

PG1101

| | |
|-----|--------|
| 1 | RESET- |
| 2 | LD |
| 3 | LD |
| 4 | LD |
| 5 | LD |
| 6 | LD |
| 7 | LD |
| 8 | LD |
| 9 | LD |
| 10 | LD |
| 11 | LD |
| 12 | LD |
| 13 | LD |
| 14 | LD |
| 15 | LD |
| 16 | LD |
| 17 | LD |
| 18 | LD |
| 19 | LD |
| 20 | LD |
| 21 | LD |
| 22 | LD |
| 23 | LD |
| 24 | LD |
| 25 | LD |
| 26 | LD |
| 27 | LD |
| 28 | LD |
| 29 | LD |
| 30 | LD |
| 31 | LD |
| 32 | LD |
| 33 | LD |
| 34 | LD |
| 35 | LD |
| 36 | LD |
| 37 | LD |
| 38 | LD |
| 39 | LD |
| 40 | LD |
| 41 | LD |
| 42 | LD |
| 43 | LD |
| 44 | LD |
| 45 | LD |
| 46 | LD |
| 47 | LD |
| 48 | LD |
| 49 | LD |
| 50 | LD |
| 51 | LD |
| 52 | LD |
| 53 | LD |
| 54 | LD |
| 55 | LD |
| 56 | LD |
| 57 | LD |
| 58 | LD |
| 59 | LD |
| 60 | LD |
| 61 | LD |
| 62 | LD |
| 63 | LD |
| 64 | LD |
| 65 | LD |
| 66 | LD |
| 67 | LD |
| 68 | LD |
| 69 | LD |
| 70 | LD |
| 71 | LD |
| 72 | LD |
| 73 | LD |
| 74 | LD |
| 75 | LD |
| 76 | LD |
| 77 | LD |
| 78 | LD |
| 79 | LD |
| 80 | LD |
| 81 | LD |
| 82 | LD |
| 83 | LD |
| 84 | LD |
| 85 | LD |
| 86 | LD |
| 87 | LD |
| 88 | LD |
| 89 | LD |
| 90 | LD |
| 91 | LD |
| 92 | LD |
| 93 | LD |
| 94 | LD |
| 95 | LD |
| 96 | LD |
| 97 | LD |
| 98 | LD |
| 99 | LD |
| 100 | LD |

PG1602

| | |
|----|----------|
| 1 | FL REQ |
| 2 | FL ACK |
| 3 | FL DATA |
| 4 | FL DATA |
| 5 | FL CLOCK |
| 6 | GND |
| 7 | POW |
| 8 | MTC SW |
| 9 | SHI MODE |
| 10 | GND |

CN0004 L=370

L=150
 CN0002

PG1701

| | |
|----|----------|
| 1 | FL REQ |
| 2 | FL ACK |
| 3 | FL DATA |
| 4 | FL DATA |
| 5 | FL CLOCK |
| 6 | GND |
| 7 | POW |
| 8 | MTC SW |
| 9 | SHI MODE |
| 10 | GND |

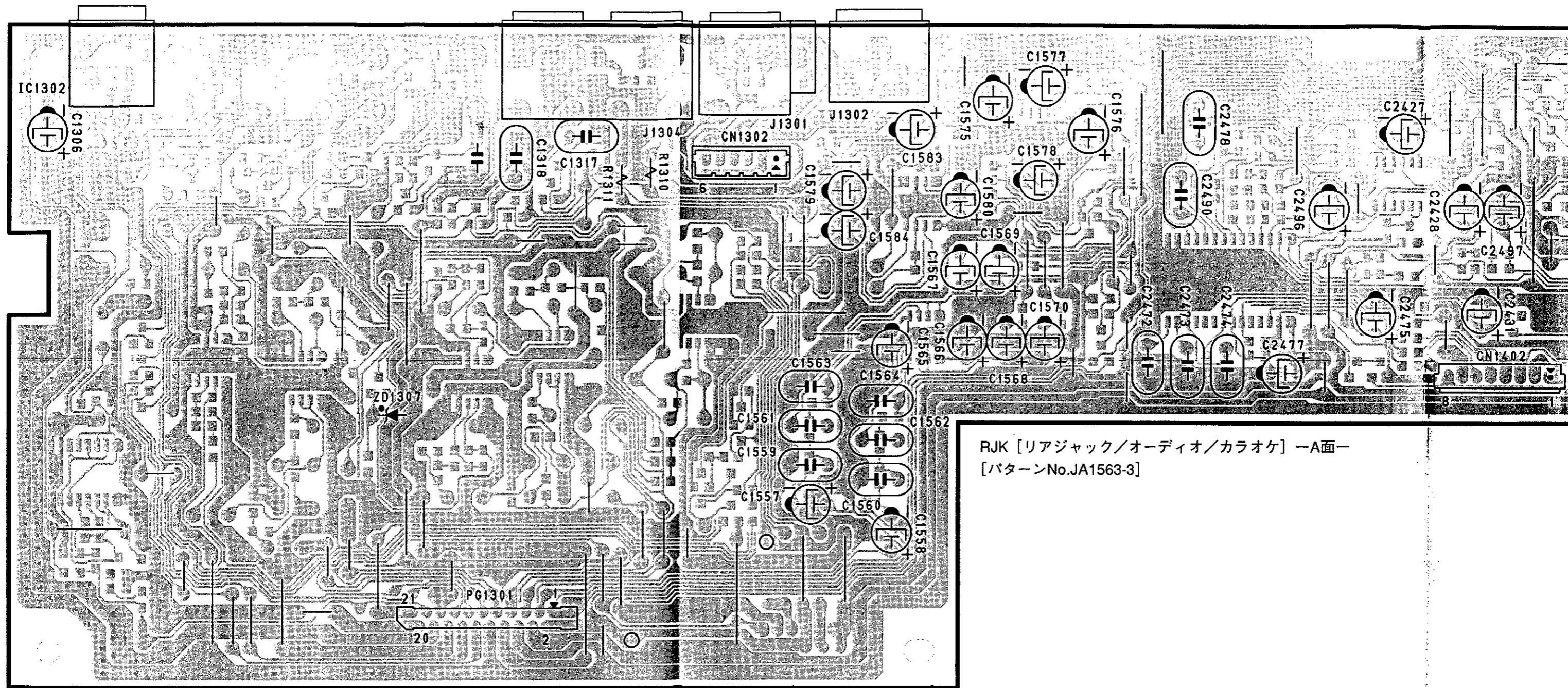
CN1702

| | |
|---|------|
| 1 | A-ZV |
| 2 | GND |
| 3 | ASV |
| 4 | AZV |
| 5 | AZV |
| 6 | AZV |

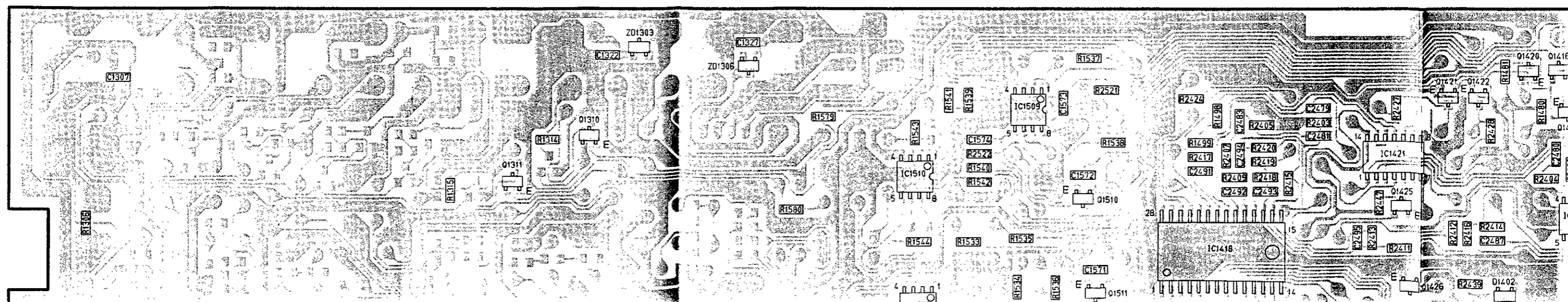
PG1764B

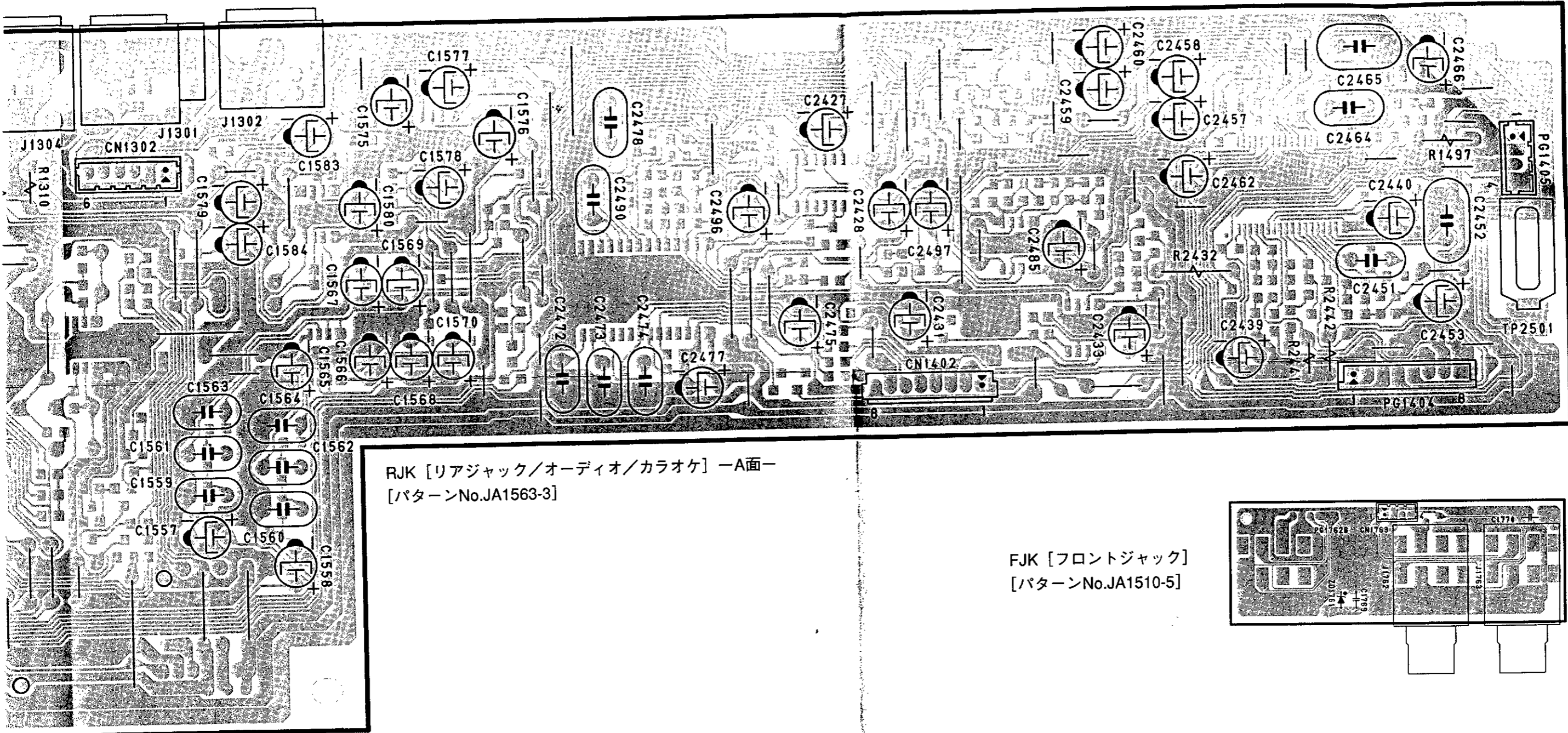
| | |
|---|----------|
| 1 | KEY |
| 2 | POWER SW |
| 3 | POWER ON |
| 4 | STAND-BY |
| 5 | GND |
| 6 | HP SW |

10. 基板図



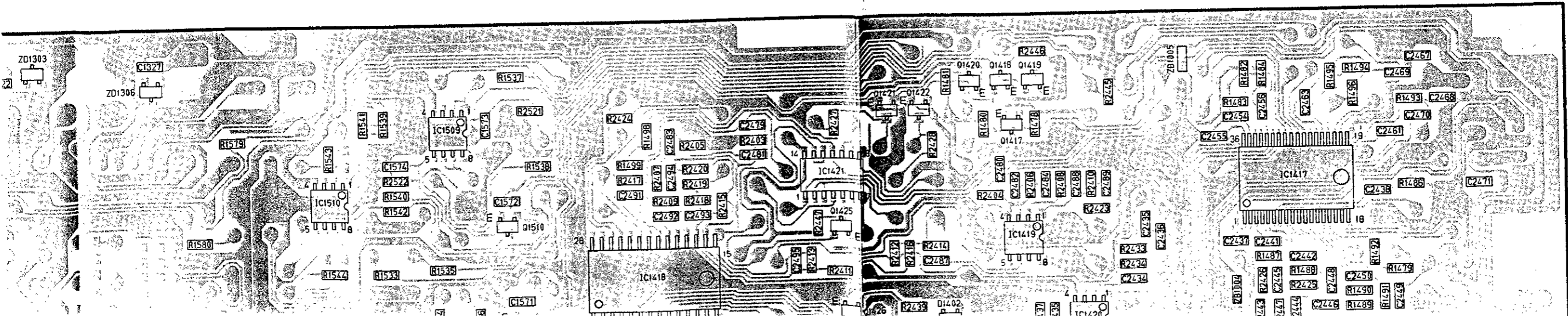
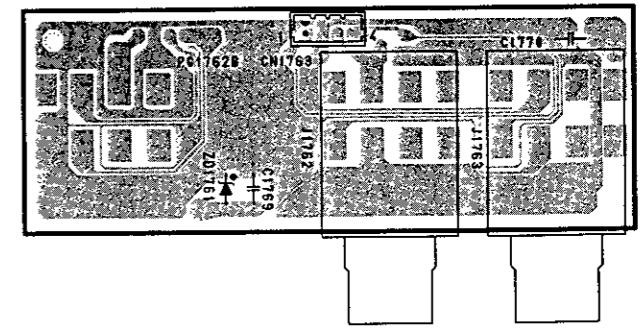
RJK [リアジャック/オーディオ/カラオケ] -A面-
[パターンNo.JA1563-3]

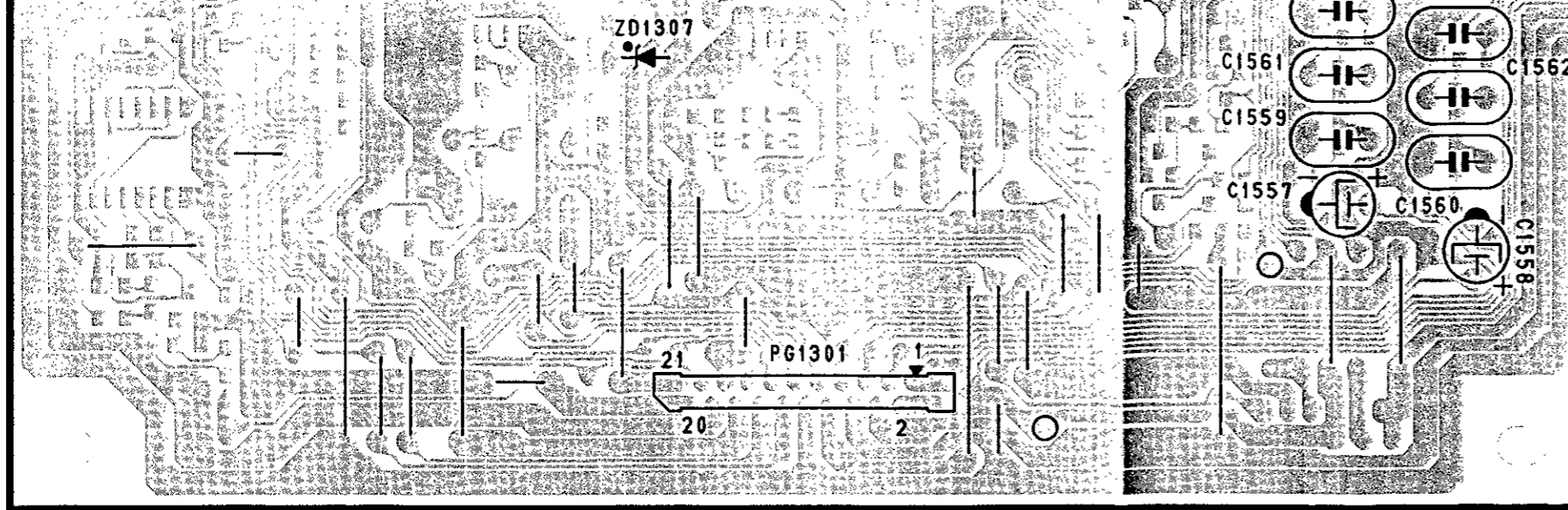




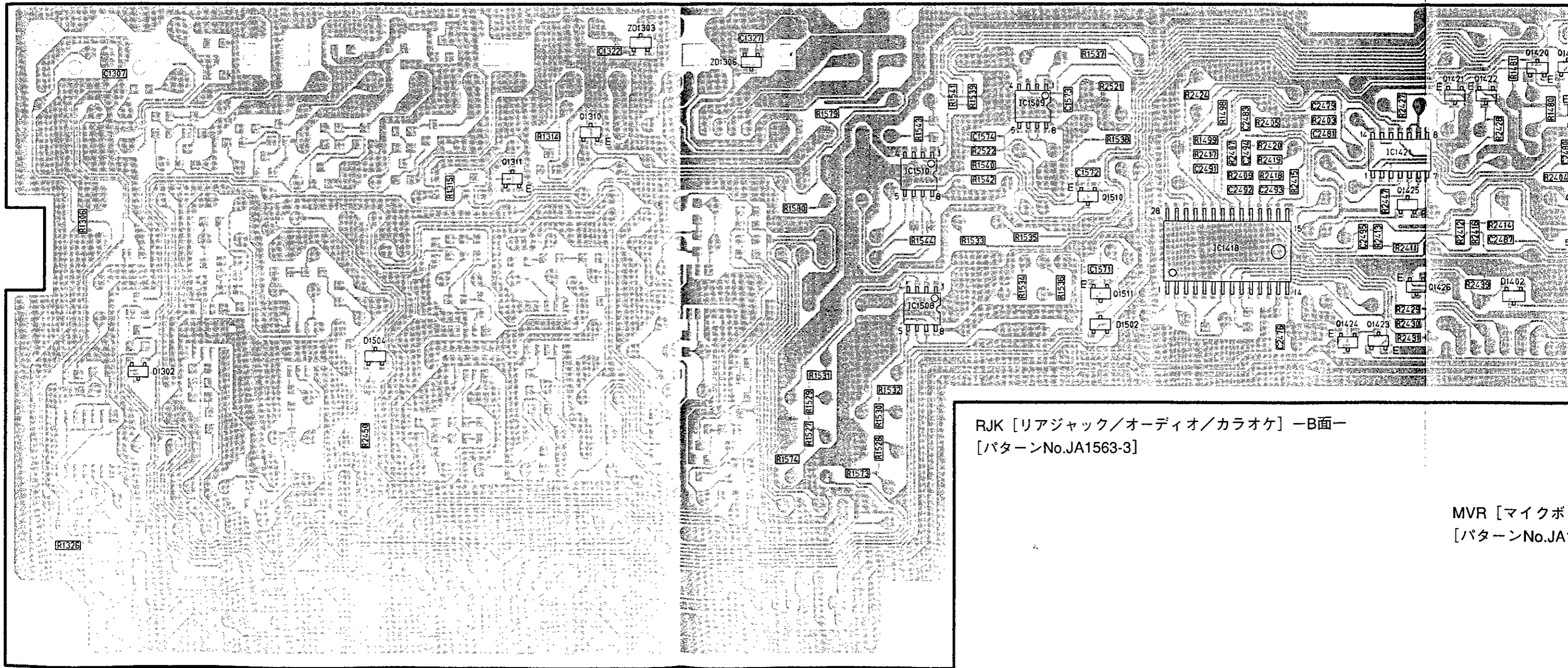
RJK [リアジャック/オーディオ/カラオケ] -A面-
 [パターンNo.JA1563-3]

FJK [フロントジャック]
 [パターンNo.JA1510-5]



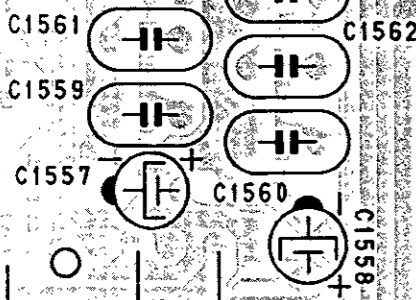


RJK [リアジャック/オーディオ/カラオケ] -A面-
[パターンNo.JA1563-3]



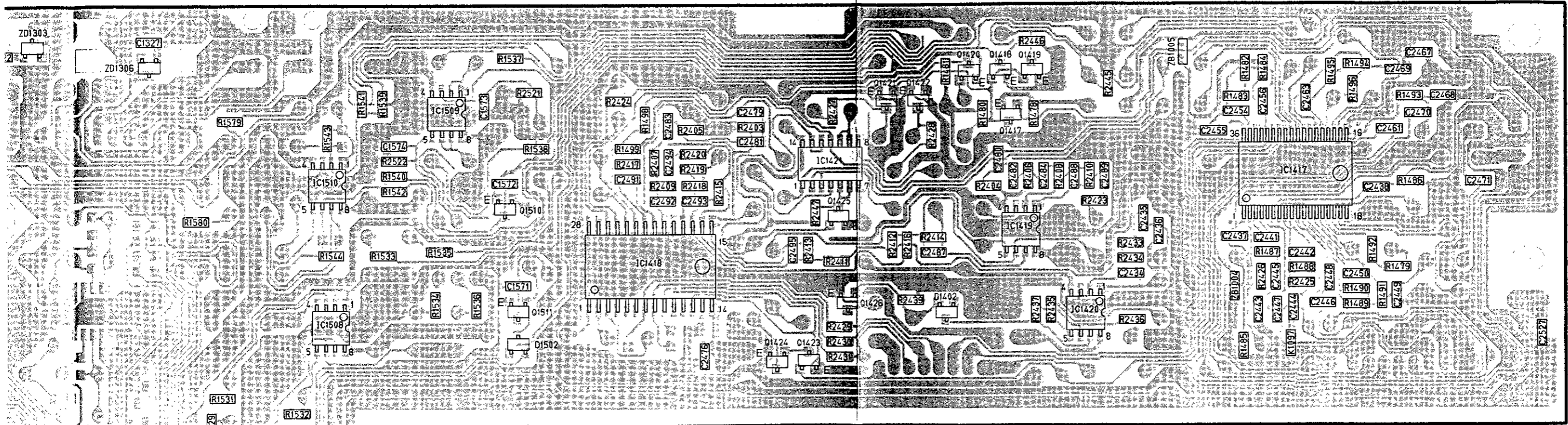
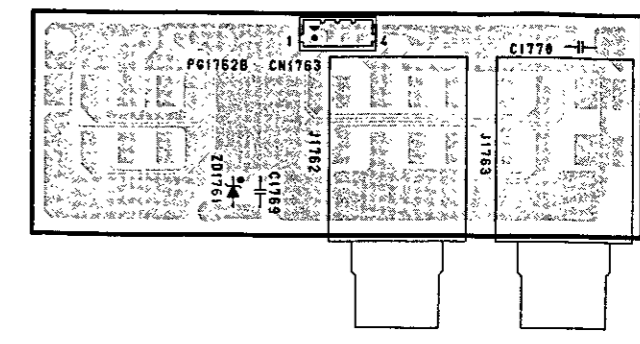
RJK [リアジャック/オーディオ/カラオケ] -B面-
[パターンNo.JA1563-3]

MVR [マイクボリ]
[パターンNo.JA1563-3]



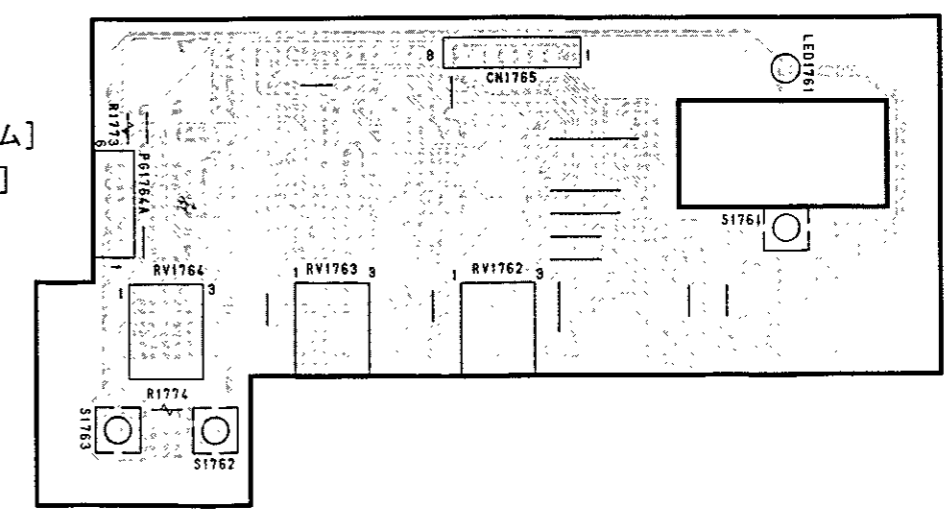
RJK [リアジャック/オーディオ/カラオケ] -A面-
[パターンNo.JA1563-3]

FJK [フロントジャック]
[パターンNo.JA1510-5]



RJK [リアジャック/オーディオ/カラオケ] -B面-
[パターンNo.JA1563-3]

MVR [マイクボリューム]
[パターンNo.JA1510-5]

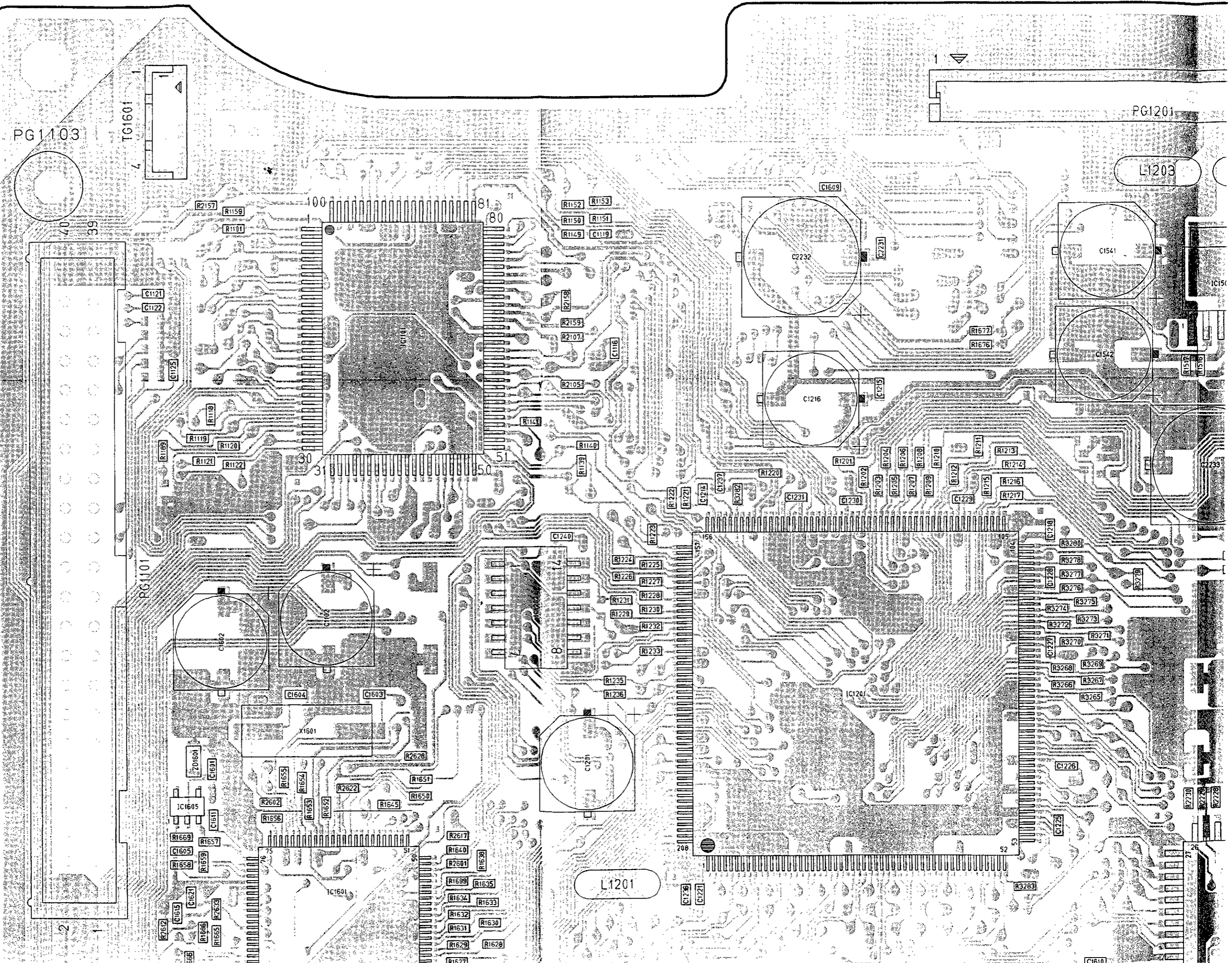


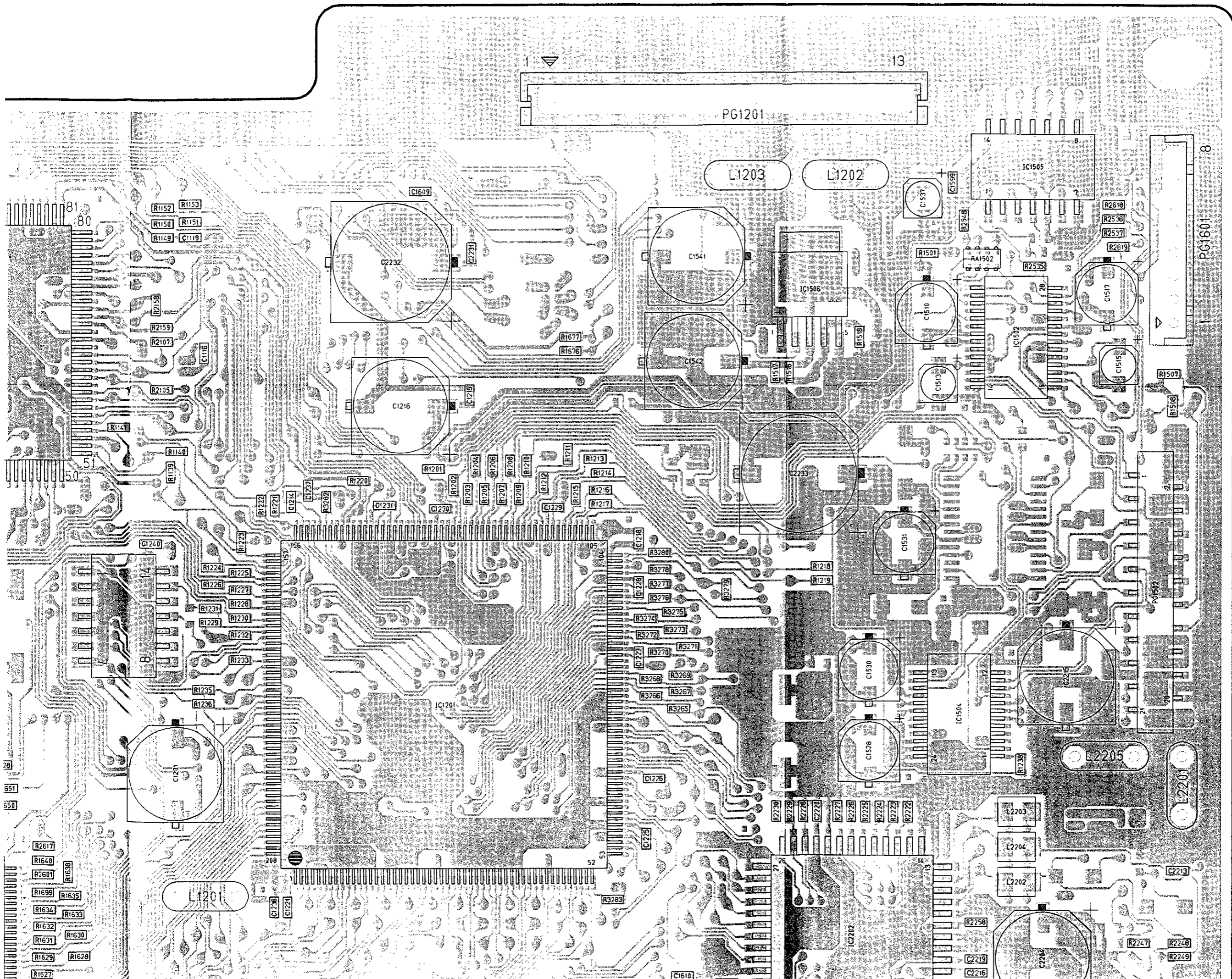
PG1103

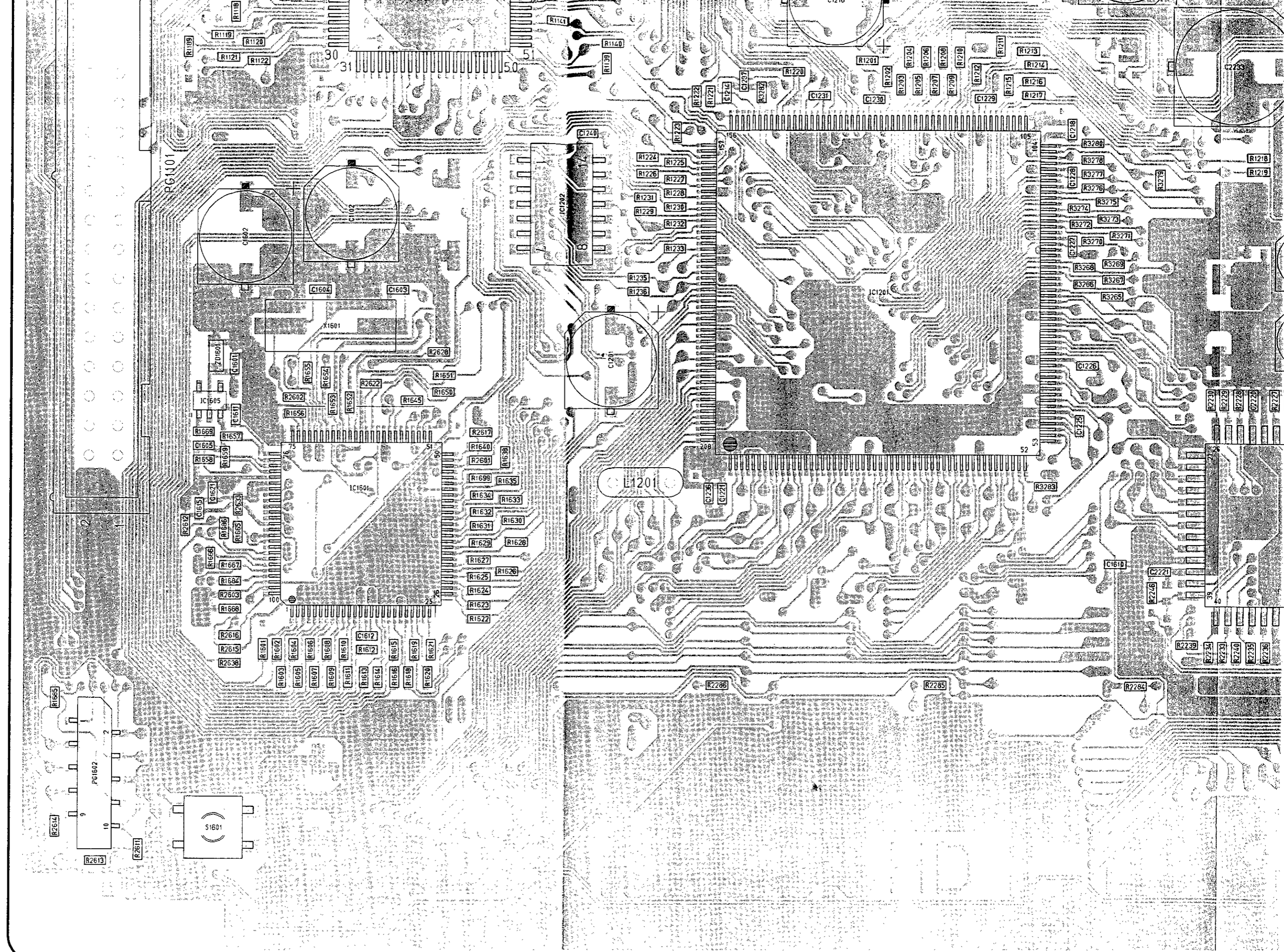
TG1601

PG1201

L1203







RG1101

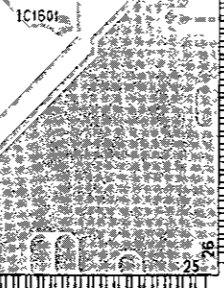
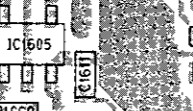
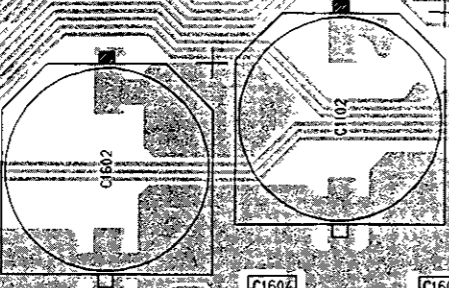
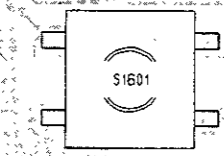
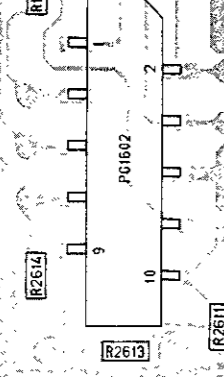
30 31 50 51

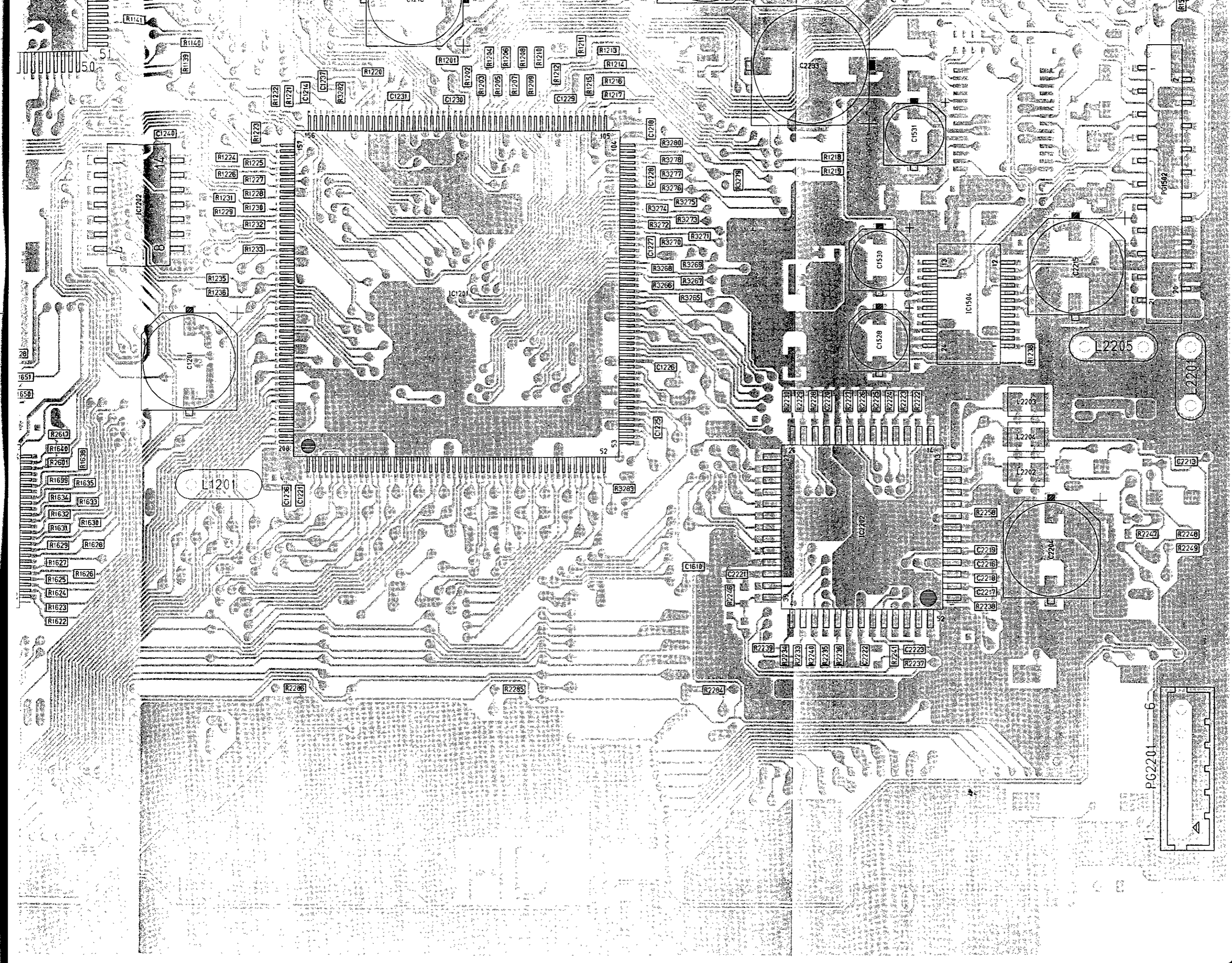
L1201

55

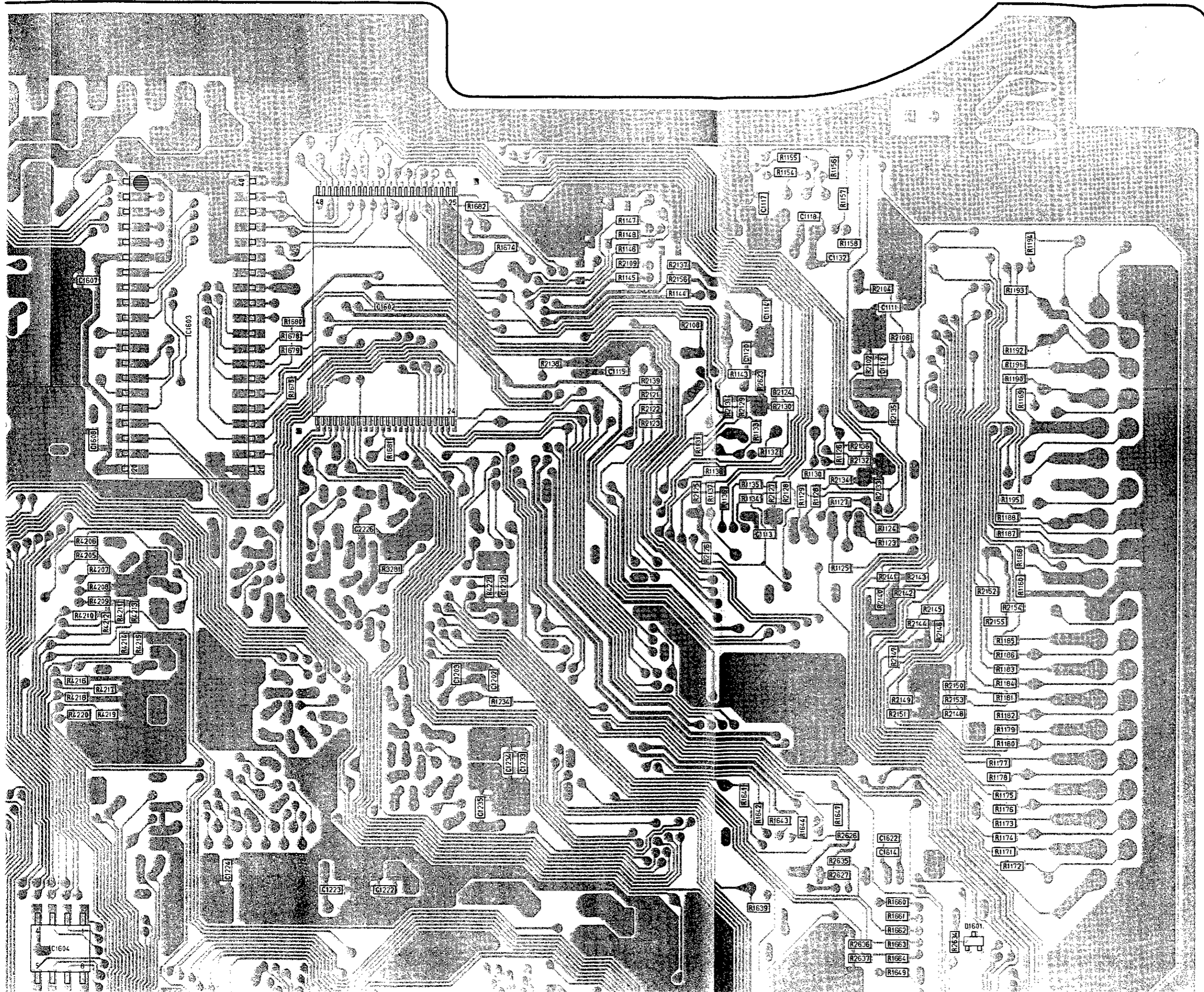
52

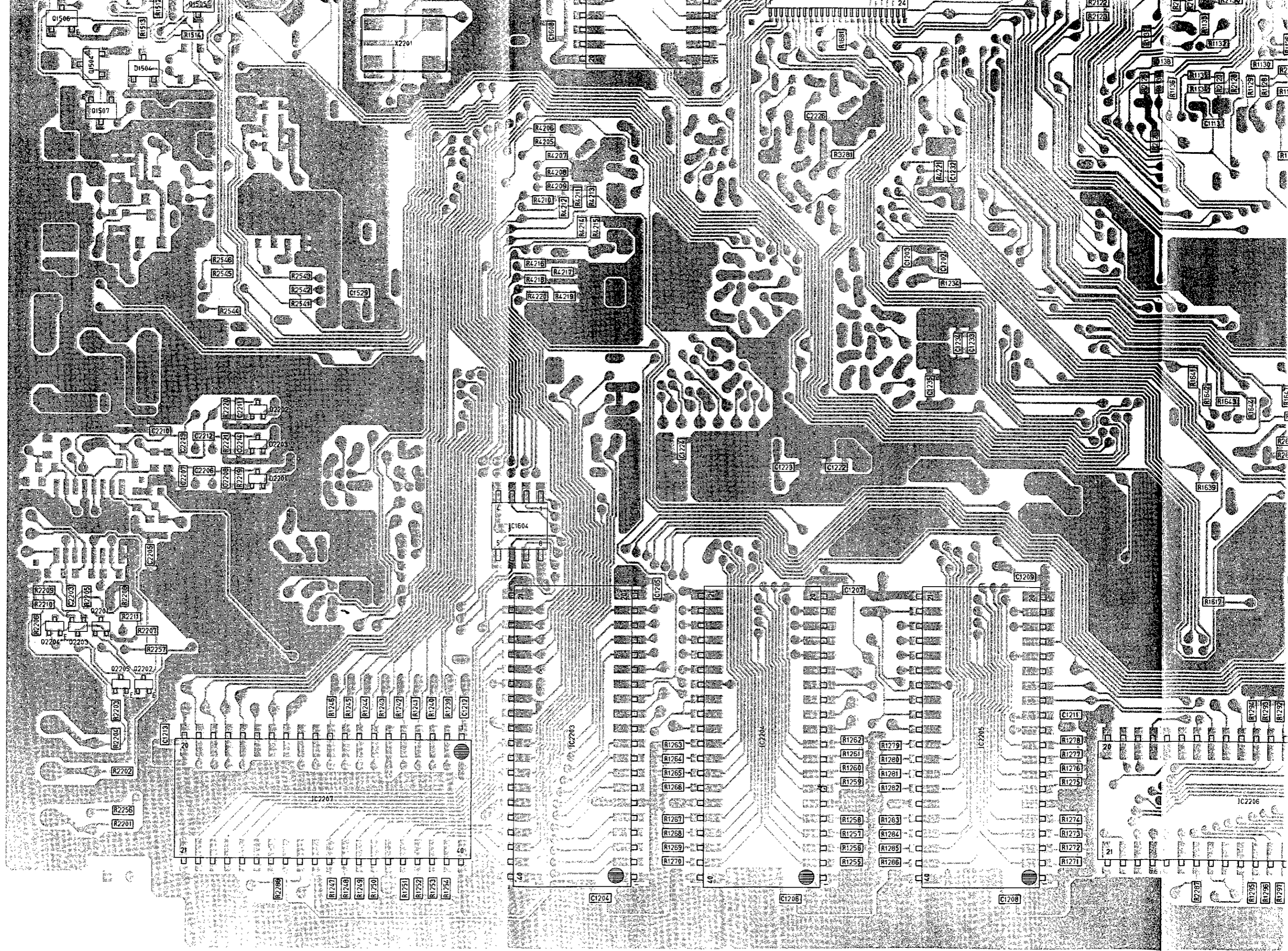
C1610

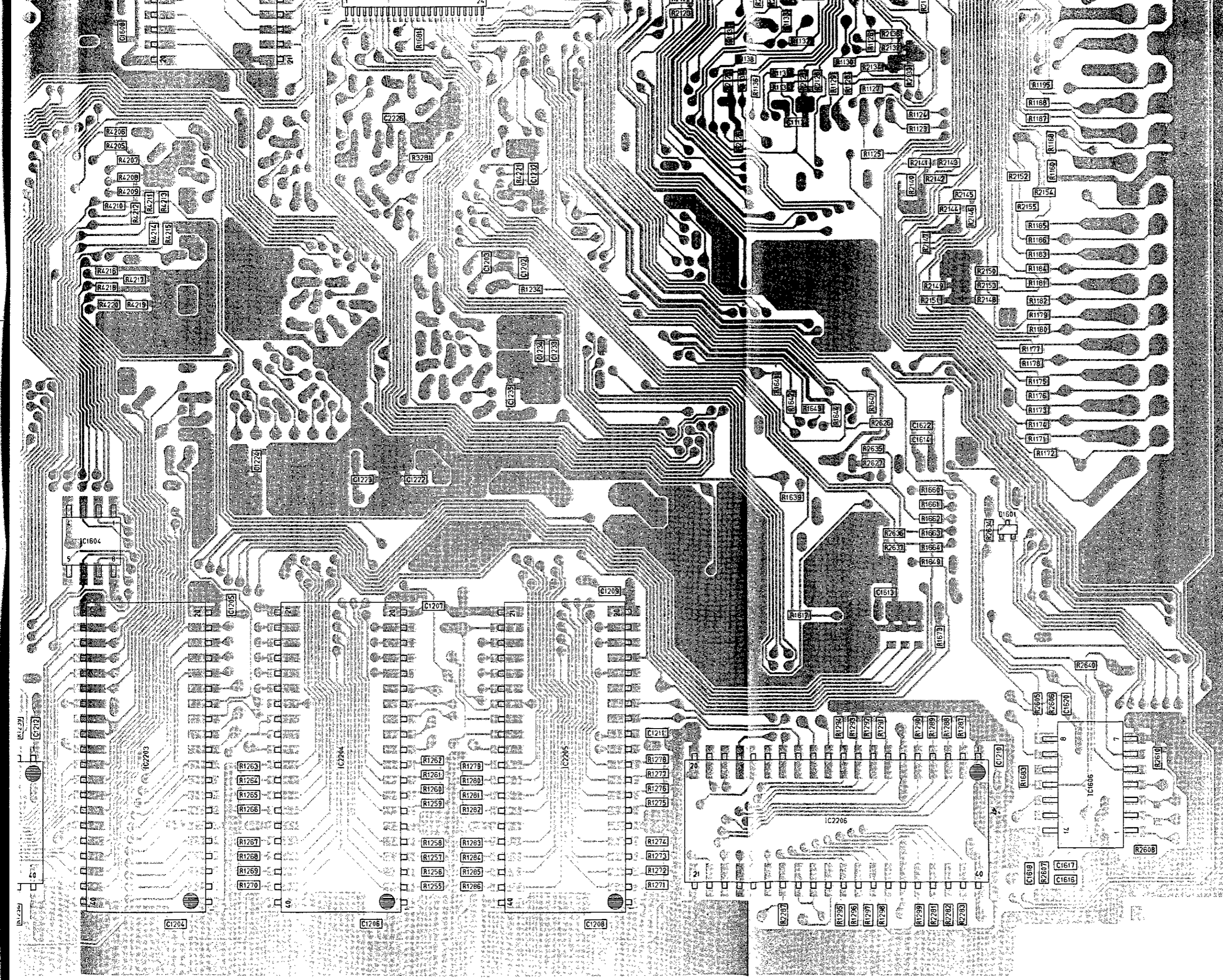




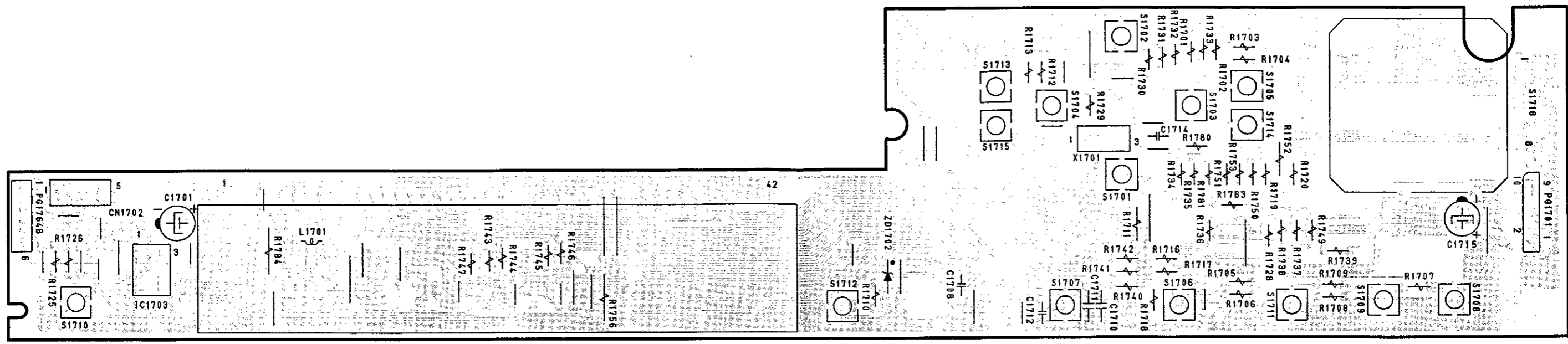
DEC [メイン] -A面-
 [パターンNo.JA1507-5]



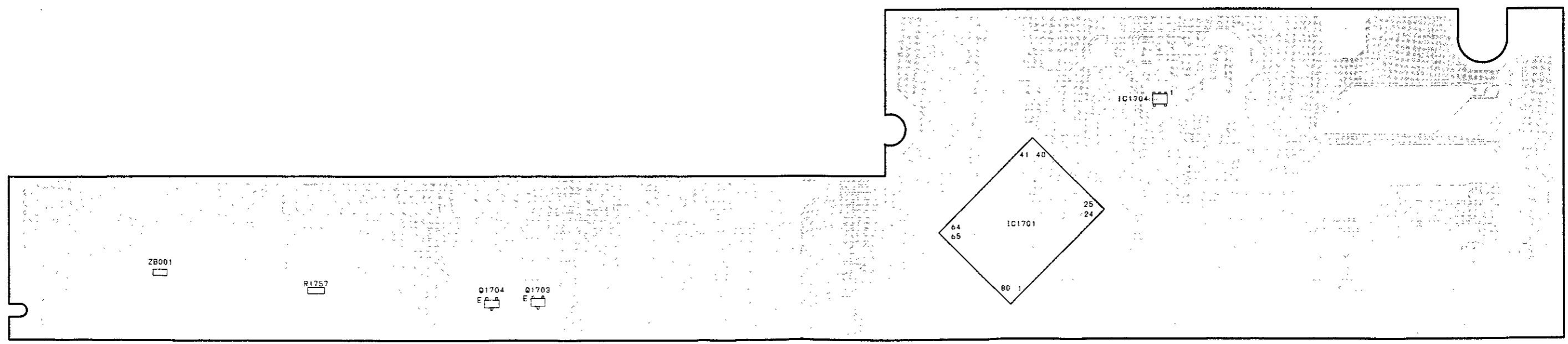




DEC [メイン] -B面-
[パターンNo.JA1507-5]

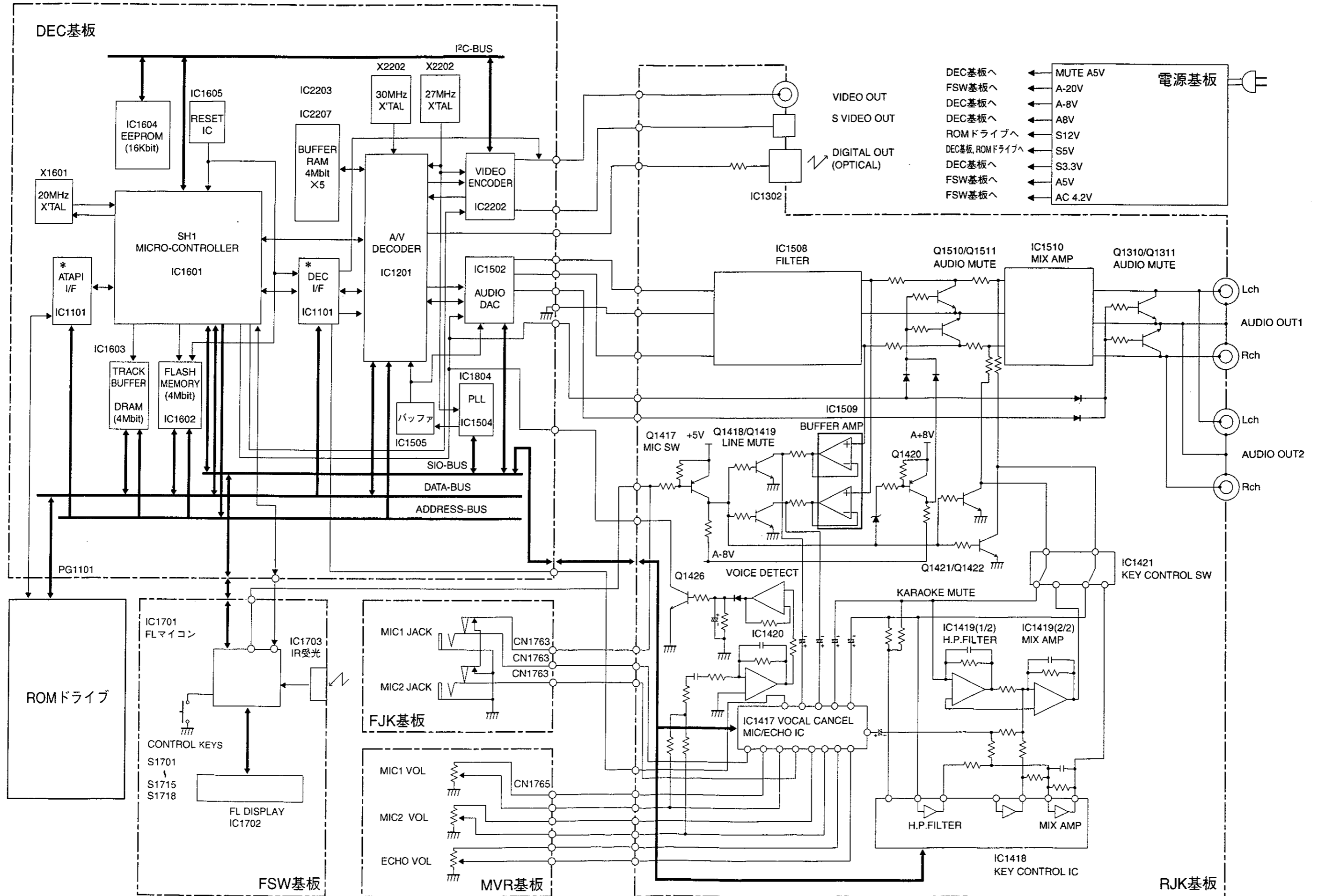


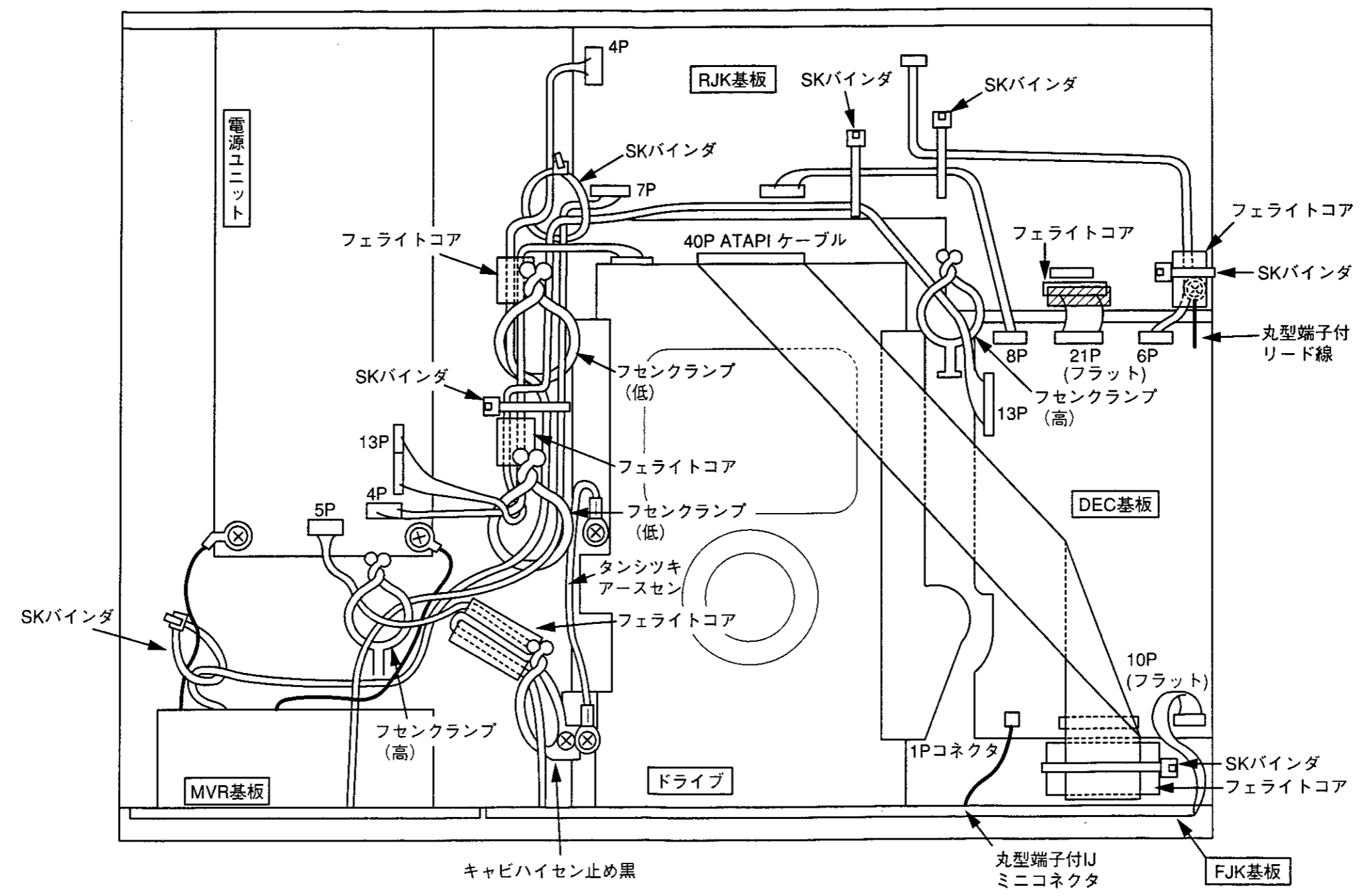
FSW [フロントスイッチ/FL管] -A面-
[パターンNo.JA1563-3]



FSW [フロントスイッチ/FL管] -B面-
[パターンNo.JA1563-3]

11. ブロック図

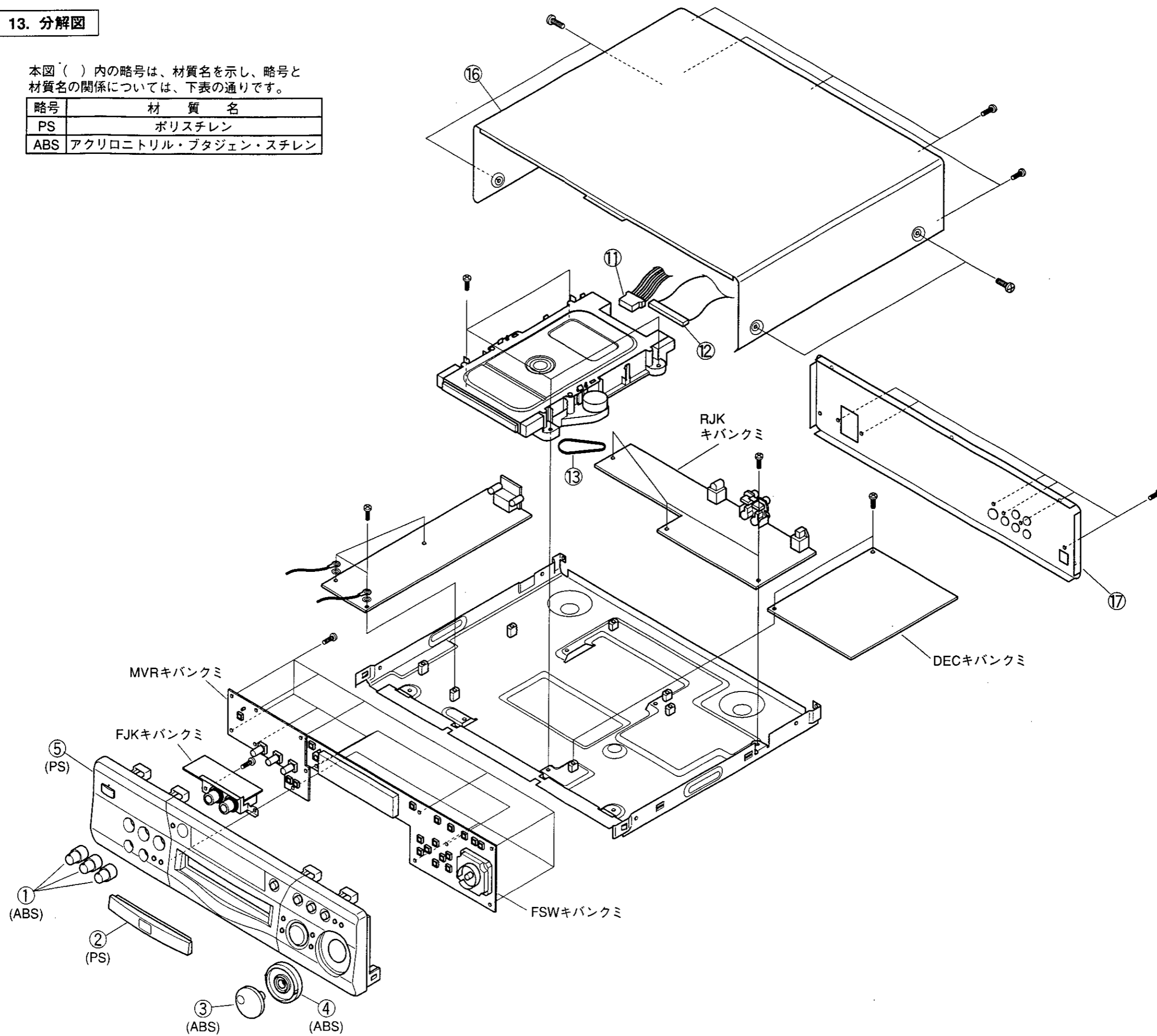




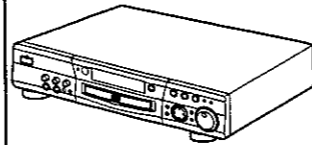
13. 分解図

本図 () 内の略号は、材質名を示し、略号と材質名の関係については、下表の通りです。

| 略号 | 材質名 |
|-----|---------------------|
| PS | ポリスチレン |
| ABS | アクリロニトリル・ブタジェン・スチレン |



14. PARTS LIST

| | | | | |
|---|--------------|------------|-------------------|-----------|
|  | Reserve item | 338-04 | Sale start day | July 1998 |
| | Model | DV-K2 | | |
| | Product name | DVD player | Service guide No. | B002 |

- ※ mark is put for newly adopted part. Prices are those of July 1998.
- △ mark is put for a designated part by safety consideration.

| Distinctive marks | Circuit No. | Part name (specification and usage) | Part No. | Packin g unit | T | ¥ | Remarks |
|-------------------|-------------|-------------------------------------|-----------|---------------|------|------|---------|
| ※ | 1 | Knob | DV-K2 002 | 1 | 210 | 300 | |
| ※ | 2 | Panel tray set | DV-K2 003 | 1 | 560 | 800 | |
| ※ | 3 | Knob (JOG) | DV-K2 004 | 1 | 210 | 300 | |
| ※ | 4 | Knob (SHU) | DV-K2 005 | 1 | 210 | 300 | |
| ※ | 5 | Panel front set | DV-K2 006 | 1 | 2100 | 3000 | |
| ※ | 11 | Connector (4PIN) | DV-K2 009 | 1 | 210 | 300 | |
| ※ | 12 | Connector (40PIN) | DV-K2 010 | 1 | 350 | 500 | |
| ※ | 13 | Rubber belt Cover top | DV-K2 011 | 1 | 210 | 300 | |
| ※ | 16 | Panel rear set | DV-K2 012 | 1 | 1260 | 1800 | |
| ※ | 17 | | DV-K2 013 | 1 | 700 | 1000 | |
| ※ | 801 | Cord (3PIN) | DV-K2 014 | 1 | 700 | 1000 | |
| ※ | 802 | Remote control (DV-RM2) | DV-K2 001 | 1 | 1050 | 1500 | |
| ※△ | 803 | Cord AC | DV-K2 015 | 1 | 700 | 1000 | |

The prices listed above are not including the value added taxes.

**OPTICAL STORAGE DEPARTMENT, IMAGE INFORMATION
MEDIA DIVISION, HITACHI LTD.**

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