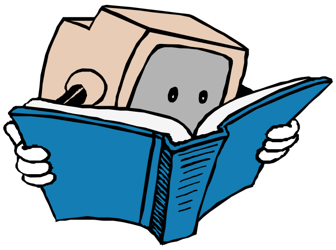
HITACHI

No. 0153

HTDK170E
HTDK170EUK



SERVICE MANUAL
MANUEL D'ENTRETIEN
WARTUNGSHANDBUCH

CAUTION:

Before servicing this chassis, it is important that the service technician read the "Safety Precautions" and "Product Safety Notices" in this service manual.

ATTENTION:

Avant d'effectuer l'entretien du châassis, le technicien doit lire les «Précautions de sécurité» et les «Notices de sécurité du produit» présentés dans le présent manuel.

VORSICHT:

Vor Öffnen des Gehäuses hat der Service-Ingenieur die „Sicherheitshinweise" und „Hinweise zur Produktsicherheit" in diesem Wartungshandbuch zu lesen.

Data contained within this Service manual is subject to alteration for improvement.

Les données fournies dans le présent manuel d'entretien peuvent faire l'objet de modifications en vue de perfectionner le produit.

Die in diesem Wartungshandbuch enthaltenen Spezifikationen können sich zwecks Verbesserungen ändern.

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

DVD DIGITAL THEATRE SYSTEM
July 2003

1. GENERAL DESCRIPTION

1.1 ES60X8

The ES6008/ES6018 Vibratto DVD processor is a single-chip MPEG video decoding chip that integrates audio/video stream data processing, TV encoder, four video DACs with Macrovision. copy protection, DVD system navigation, system control and housekeeping functions.

The Vibratto DVD processor is built on the ESS proprietary dual CPU Programmable Multimedia Processor (PMP) core consists of 32-bit RISC and 64-bit DSP processors and offers the best DVD feature set.

These features can be listed as follows:

General Features:

- Single-chip DVD processor based on ESS proprietary dual CPU PMP core.
- Integrated NTSC/PAL encoder.
- Four integrated 10-bit video DACs.
- DVD-Video, VCD 1.1, 2.0, and SVCD
- Interface for ATAPI devices and A/V DVD loaders.
- Interface for Compact Flash, Memory Stick and SmartMedia cards.
- Direct interface of 8- or 16-bit SDRAM up to 128-Mb capacity.
- Direct interface for up to four banks of 8-/16-bit EPROM or Flash EPROM for up to 16-MB capacity.

Video Related Features:

- Macrovision 7.1 for NTSC/PAL interlaced video.
- Simultaneous composite video and S-video outputs, or composite and YUV outputs, or composite and RGB outputs.
- 8-bit CCIR 601 YUV 4:2:2 output.
- On-Screen Display (OSD) controller with 3-bit blending provides display with 256 colors in 8 degrees of transparency.
- Subpicture Unit (SPU) decoder supports karaoke lyric, subtitles, and EIA-608 compliant Line 21 Captioning.

Audio Related Features:

- Dolby Digital (AC-3) and Dolby Pro Logic.

- High-Definition Compatible Digital. (HDCD) decoding.
- Dolby Digital Class A and HDCD certified.
- CD-DA.
- MP3.

1.2 MEMORY

1.2.1 System SRAM Interface

The system SRAM interface controls access to optional external SRAM, which can be used for RISC code, stack, and data. The SRAM bus supports four independent address spaces, each having programmable bus width and wait states. The interface can support not only SRAM, ROM/EPROM and memory-mapped I/O ports for standalone applications are also supported.

1.2.2 DRAM Memory Interface

The Vibratto provides a glueless 16-bit interface to DRAM memory devices used as video memory for a DVD player. The maximum amount of memory supported is 16 MB of Synchronous DRAM (SDRAM). The memory interface is configurable in depth to support 128-Mb addressing. The memory interface controls access to both external SDRAM or EDO memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers.

1.3 DRIVE INTERFACES

The Vibratto supports the AT Attachment Packet Interface (ATAPI), Integrated Drive Electronics (IDE), and other parallel and serial port interfaces used by many types of DVD loaders. These interfaces meet the specifications of many DVD loader manufacturers. An ATAPI drive is connected via the standard 34 pin dual row PC style IDE header

1.4 FRONT PANEL

The front panel is based around an Futaba VFD and a common NEC front panel controller chip, (uPD16311). The ES6008/ES6018 controls the uPD16311 using several control signals, (clock, data, chip select). The infrared remote control signal is passed directly to the ES60X8 and 8051 for decoding.

1.5 REAR PANEL

Outputs and Inputs at the AV1000 rear panel:

- Left, Right and Subwoofer (active) audio outputs.
- Left, Right and CVBS input.
- Composite, S-Video, and SCART outputs.
- Input SCART
- 5x15W 8ohms (L,R,SL,SR,C) + 1x25W 4ohms Subwoofer outputs.
- AM / FM Tuner Antenna input
- 220-240 V 50Hz AC Power input

The six-video signals used to provide CVBS, S-Video, and RGB are generated by the ES60X8's internal video DAC. The video signals are buffered by external circuitry.

Six channel audio output by the ES6018 in the form of three I^2S (or similar) data streams. The S/PDIF serial stream is also generated by the ES60X8 output by the rear panel. A six channel audio DAC (AK4356) are used for six channel audio output with ES6018, and similarly one AK4362A Audio DAC is used for two channel audio output with ES6008 or ES6018.

2. SYSTEM BLOCK DIAGRAM and ES6008/18 PIN DESCRIPTION

2.1 ES6008/18 PIN DESCRIPTION

<table>
<tr><th>Name</th><th>Pin Numbers</th><th>I/O</th><th>Definition</th></tr>
<tr><td>VEE</td><td>1,18, 27, 59, 68, 75, 92, 99, 104, 130, 148, 157, 159, 164, 183, 193, 201</td><td>I</td><td>I/O power supply.</td></tr>
<tr><td>LA[21:0]</td><td>2:7, 10:16, 19:23, 204:207</td><td>O</td><td>RISC port address bus.</td></tr>
<tr><td>VSS</td><td>8, 17, 26, 34, 43, 52, 60, 67, 76, 84, 91, 98, 103, 112, 120, 129, 138, 147, 156, 163, 171, 177, 184, 192, 200, 208</td><td>I</td><td>Ground.</td></tr>
<tr><td>VCC</td><td>9, 35, 44, 83, 121, 139, 172</td><td>I</td><td>Core power supply.</td></tr>
<tr><td>RESET#</td><td>24</td><td>I</td><td>Reset input, active-low.</td></tr>
<tr><td>TDMDX</td><td rowspan="2">25</td><td>O</td><td>TDM transmit data output.</td></tr>
<tr><td>RSEL</td><td>I</td><td>LCS3 ROM Boot Data Width Select. Strapped to VCC or ground via 4.7-kΩ resistor; read only during reset.
<table>
<tr><th>RSEL</th><th>Selection</th></tr>
<tr><td>0</td><td>16-bit ROM</td></tr>
<tr><td>1</td><td>8-bit ROM</td></tr>
</table>
</td></tr>
<tr><td>TDMDR</td><td>28</td><td>I</td><td>TDM receive data input.</td></tr>
<tr><td>TDMCLK</td><td>29</td><td>I</td><td>TDM clock input.</td></tr>
<tr><td>TDMFS</td><td>30</td><td>I</td><td>TDM frame sync input.</td></tr>
<tr><td>TDMTSC#</td><td>31</td><td>O</td><td>TDM output enable.</td></tr>
<tr><td>TWS</td><td rowspan="2">32</td><td>O</td><td>Audio transmit frame sync output.</td></tr>
<tr><td>SEL_PLL2</td><td>I</td><td>System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available clock frequencies and their respective PLL bit settings. Strapped to VCC or ground via 4.7-kΩ resistor; read only during reset.
<table>
<tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DCLK x 4.25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DCLK</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bypass mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DCLK x 3.75</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>DCLK x 4.5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>DCLK x 3.5</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DCLK x 4</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Name</th><th>Pin Numbers</th><th>I/O</th><th>Definition</th></tr>
<tr><td>TSD0</td><td rowspan="2">33</td><td>O</td><td>Audio transmit serial data port 0.</td></tr>
<tr><td>SEL_PLL0</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 32.</td></tr>
<tr><td>SEL_PLL1</td><td>36</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 32.</td></tr>
<tr><td>NC</td><td>37, 38, 42, 48</td><td>—</td><td>No connect pins. Leave open.</td></tr>
<tr><td>MCLK</td><td>39</td><td>I/O</td><td>Audio master clock for audio DAC.</td></tr>
<tr><td>TBCK</td><td>40</td><td>O</td><td>Audio transmit bit clock.</td></tr>
<tr><td>SPDIF</td><td rowspan="2">41</td><td>O</td><td>S/PDIF output.</td></tr>
<tr><td>SEL_PLL3</td><td>I</td><td>Clock source select.Strapped to VCC or ground via 4.7-kΩ resistor; read only during reset.
<table><tr><th>SEL_PLL3</th><th>Clock Source</th></tr><tr><td>0</td><td>Crystal oscillator</td></tr><tr><td>1</td><td>DCLK input</td></tr></table></td></tr>
<tr><td>RSD</td><td>45</td><td>I</td><td>Audio receive serial data.</td></tr>
<tr><td>RWS</td><td>46</td><td>I</td><td>Audio receive frame sync.</td></tr>
<tr><td>RBCK</td><td>47</td><td>I</td><td>Audio receive bit clock.</td></tr>
<tr><td>XIN</td><td>49</td><td>I</td><td>27-MHz crystal input.</td></tr>
<tr><td>XOUT</td><td>50</td><td>O</td><td>27-MHz crystal output.</td></tr>
<tr><td>AVEE</td><td>51</td><td>I</td><td>Analog power for PLL.</td></tr>
<tr><td>DMA[11:0]</td><td>53:58, 61:66</td><td>O</td><td>DRAM address bus.</td></tr>
<tr><td>DCAS#</td><td>69</td><td>O</td><td>DRAM column address strobe.</td></tr>
<tr><td>DOE#</td><td rowspan="2">70</td><td>O</td><td>DRAM output enable.</td></tr>
<tr><td>DSCK_EN</td><td>O</td><td>DRAM clock enable.</td></tr>
<tr><td>DWE#</td><td>71</td><td>O</td><td>DRAM write enable.</td></tr>
<tr><td>DRAS#</td><td>72</td><td>O</td><td>DRAM row address strobe.</td></tr>
<tr><td>DMBS0</td><td>73</td><td>O</td><td>SDRAM bank select 0.</td></tr>
<tr><td>DMBS1</td><td>74</td><td>O</td><td>SDRAM bank select 1.</td></tr>
<tr><td>DB[15:0]</td><td>77:82, 85:90, 93:96</td><td>I/O</td><td>DRAM data bus.</td></tr>
<tr><td>DCS[1:0]#</td><td>97, 100</td><td>O</td><td>SDRAM chip select.</td></tr>
<tr><td>DQM</td><td>101</td><td>O</td><td>Data input/output mask.</td></tr>
<tr><td>DSCK</td><td>102</td><td>O</td><td>Output clock to SDRAM.</td></tr>
<tr><td>DCLK</td><td>105</td><td>I</td><td>Clock input to PLL.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Pin Numbers</th><th>I/O</th><th>Definition</th></tr>
<tr><td>YUV0</td><td rowspan="3">106</td><td>O</td><td>YUV0 pixel output data.</td></tr>
<tr><td>CAMIN2</td><td>I</td><td>Camera input 2.</td></tr>
<tr><td>UDAC</td><td>O</td><td>DAC Output Configuration Matrix.
<table>
<tr><th>Pin</th><th>114</th><th>113</th><th>108</th><th>106</th></tr>
<tr><th>Value</th><th>DAC V</th><th>DAC Y</th><th>DAC C</th><th>DAC U</th></tr>
<tr><td>0</td><td>CVBS1</td><td>Y</td><td>C</td><td>N/A</td></tr>
<tr><td>1</td><td>CVBS1</td><td>Y</td><td>C</td><td>CVBS2</td></tr>
<tr><td>2</td><td>N/A</td><td>Y</td><td>C</td><td>N/A</td></tr>
<tr><td>3</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>CVBS2</td></tr>
<tr><td>4</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>5</td><td>CVBS1</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>6</td><td>N/A</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>7</td><td>SYNC</td><td>G</td><td>B</td><td>R</td></tr>
<tr><td>8</td><td>CHROMA</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>9</td><td>CVBS1</td><td>G</td><td>B</td><td>R</td></tr>
<tr><td>10</td><td>CVBS1</td><td>G</td><td>R</td><td>B</td></tr>
<tr><td>11</td><td>SYNC</td><td>G</td><td>R</td><td>B</td></tr>
<tr><td>12</td><td>N/A</td><td>Y</td><td>Pr</td><td>Pb</td></tr>
<tr><td>13</td><td>CVBS1</td><td>Y</td><td>Pr</td><td>Pb</td></tr>
</table>
Y: Luma component for YUV and Y/C processing.
C: Chrominance signal for Y/C processing.
U: Chrominance component signal for YUV mode.
V: Chrominance component signal for YUV mode.</td></tr>
<tr><td>YUV1</td><td rowspan="2">107</td><td>O</td><td>YUV1 pixel output data.</td></tr>
<tr><td>VREF</td><td>I</td><td>Internal voltage reference to video DAC. Bypass to ground with 0.1-μF capacitor.</td></tr>
<tr><td>YUV2</td><td rowspan="2">108</td><td>O</td><td>YUV2 pixel output data.</td></tr>
<tr><td>CDAC</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 106.</td></tr>
<tr><td>YUV3</td><td rowspan="2">109</td><td>O</td><td>YUV3 pixel output data.</td></tr>
<tr><td>COMP</td><td>I</td><td>Compensation input. Bypass to ADVEE with 0.1-μF capacitor.</td></tr>
<tr><td>YUV4</td><td rowspan="2">110</td><td>O</td><td>YUV4 pixel output data.</td></tr>
<tr><td>RSET</td><td>I</td><td>DAC current adjustment resistor input.</td></tr>
<tr><td>ADVEE</td><td>111</td><td>I</td><td>Analog power for video DAC.</td></tr>
<tr><td>YUV5</td><td rowspan="2">113</td><td>O</td><td>YUV5 pixel output data.</td></tr>
<tr><td>YDAC</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 106.</td></tr>
</table>

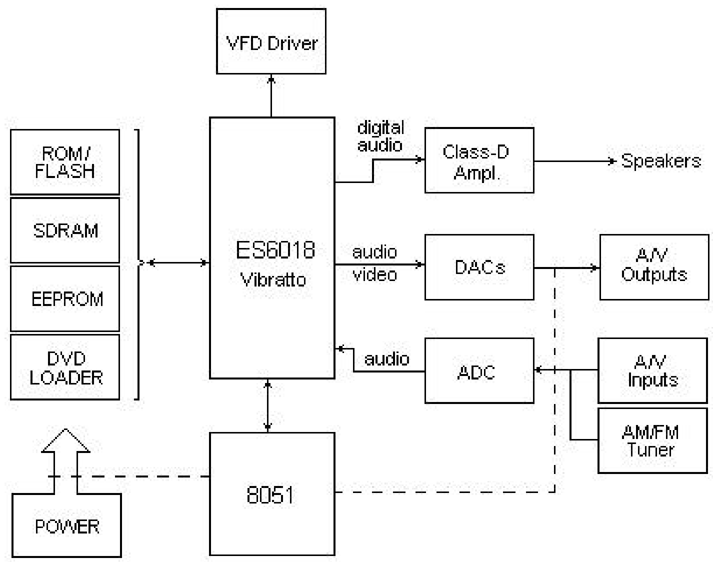
Name	Pin Numbers	I/O	Definition
YUV6	114	O	YUV6 pixel output data.
VDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV7	115	O	YUV7 pixel output data.
CAMIN3		I	Camera YUV 3.
PCLK2XSCN	116	I/O	27-MHz video output pixel clock.
CAMIN4		I	Camera YUV 4.
PCLKQSCN	117	O	13.5-MHz video output pixel clock.
CAMIN5		I	Camera YUV 5.
AUX3[2]		I/O	Aux3 data I/O.
VSYNC#	118	I/O	Vertical sync, active-low.
CAMIN6		I	Camera YUV 6.
AUX3[1]		I/O	Aux3 data I/O.
HSYNC#	119	I/O	Horizontal sync, active-low.
CAMIN7		I	Camera YUV 7.
AUX3[0]		I/O	Aux3 data I/O.
HD[5:0]	122:127	I/O	Host data bus lines 5:0.
DCI[5:0]		I/O	DVD channel data I/O.
AUX1[5:0]		I/O	Aux1 data I/O.
HD[6]	128	I/O	Host data bus line 6.
DCI[6]		I/O	DVD channel data I/O.
AUX1[6]		I/O	Aux1 data I/O.
VFD_DOUT		I	VFD data output.
HD[7]	131	I/O	Host data bus line 7.
DCI[7]		I/O	DVD channel data I/O.
AUX1[7]		I/O	Aux1 data I/O.
VFD_DIN		I	VFD data input.
HD[8]	132	I/O	Host data bus line 8.
DCI_FDS#		I/O	DVD input sector start.
AUX2[0]		I/O	Aux2 data I/O.
VFD_CLK		I	VFD clock input.
HD[9]	133	I/O	Host data bus line 9.
AUX2[1]		I/O	Aux2 data I/O.
SQSQ		I	Subcode-Q data.

Name	Pin Numbers	I/O	Definition
HD[10]	134	I/O	Host data bus line 10.
AUX2[2]		I/O	Aux2 data I/O.
SQSK		I	Subcode-Q clock.
HD[11]	135	I/O	Host data bus line 11.
AUX2[3]		I/O	Aux2 data I/O.
IRQ		O	IRQ.
HD[12]	136	I/O	Host data bus line 12.
AUX2[4]		I/O	Aux2 data I/O.
C2PO		I	C2PO error correction flag from CD-ROM.
HD[13]	137	I/O	Host data bus line 13.
AUX2[5]		I/O	Aux2 data I/O.
SP		I	16550 UART serial port input.
HD[14]	140	I/O	Host data bus line 14.
AUX2[6]		I/O	Aux2 data I/O.
SQSI		I	Subcode-Q sync.
HD[15]	141	I/O	Host data bus line 15.
AUX2[7]		I/O	Aux2 data I/O.
IR		I	IR remote control input.
HWRQ#	142	O	Host write request.
DCI_REQ#		O	DVD control interface request.
AUX4[1]		I/O	Aux4 data I/O.
HRRQ#	143	O	Host read request.
AUX4[0]		I/O	Aux4 data I/O.
HIRQ	144	I/O	Host interrupt.
DCI_ERR#		I/O	DVD channel data error.
AUX4[7]		I/O	Aux4 data I/O.
HRST#	145	O	Host reset.
AUX3[5]		I/O	Aux3 data I/O.
HIORDY	146	I	Host I/O ready.
AUX3[3]		I/O	Aux3 data I/O.
HWR#	149	I/O	Host write.
DCI_CLK		I/O	DVD channel data clock.
AUX4[5]		I/O	Aux4 data I/O.

Name	Pin Numbers	I/O	Definition
HRD#	150	O	Host read.
DCI_ACK#		O	DVD channel data valid.
AUX4[6]		I/O	Aux4 data I/O.
HIOCS16#	151	I	Device 16-bit data transfer.
CAMCLK		I	Camera port pixel clock input.
AUX3[4]		I/O	Aux3 data I/O.
HCS1FX#	152	O	Host select 1.
AUX3[7]		I/O	Aux3 data I/O.
HCS3FX#	153	O	Host select 3.
AUX3[6]		I/O	Aux3 data I/O.
HA[2:0]	154, 155, 158	I/O	Host address bus.
AUX4[4:2]		I/O	Aux4 data I/Os.
AUX[0]	160	I/O	Auxiliary port 0 (open collector).
I2CDATA		I/O	I^2C data I/O.
AUX[1]	161	I/O	Auxiliary port 1 (open collector).
I2C_CLK		I/O	I^2C clock I/O.
AUX[2]	162	I/O	Auxiliary port.
IOW#		O	I/O Write strobe (LCS1).
AUX[3]	165	I/O	Auxiliary port.
IOR#		O	I/O Read strobe (LCS1).
AUX[6:4]	166:168	I/O	Auxiliary ports.
AUX[7]	169	I/O	Auxiliary port.
STALL#		I	STALL# flag input; when set, extends cycle by adding wait states as required.
LOE#	170	O	RISC port output enable.
LCS[3:0]#	173:176	O	RISC port chip select.
LD[15:0]	178:182, 185:191,194:197	I/O	RISC port data bus.
LWRLL#	198	O	RISC port low-byte write enable.
LWRHL#	199	O	RISC port high-byte write enable.
CAMIN0	202	I	Camera YUV 0.
CAMIN1	203	I	Camera YUV 1.

2.1 SYSTEM BLOCK DIAGRAM

System block diagram is shown in the following figure:



3. AUDIO OUTPUT

The ES6008 supports two-channel analog audio output while ES6018 supports six-channel analog audio output. In a system configuration with six analog outputs, the front left and right channels can be configured to provide the stereo (2 channel) outputs and Dolby Surround, or the left and right front channels for a 5.1 channel surround system.

The ES6008 also provides digital output in S/PDIF format. The board supports both optical and coaxial S/PDIF outputs.

AV1000 Has also 5.1 channel Class-D amplifier outputs to 8 ohms satelites and 4 ohms subwoofer.

4 AUDIO DACS

The ES6008/18 supports several variations of an I^2S type bus, varying the order of the data bits (leading or no leading zero bit, left or right alignment within frame, and MSB or LSB first) is possible using the ES6008/18 internal configuration registers. The I^2S format uses four stereo data lines and three clock lines. The I^2S data and clock lines can be connected directly to one or more audio DAC to generate analog audio output.

The two-channel DAC is an AKM AK4382A. The DACs support up to 192kHz sampling rate.

The outputs of the DACs are differential, not single ended so a buffering circuit is required. The buffer circuits use National LM833 op-amps to perform the low-pass filtering and the buffering.

5 VIDEO INTERFACE

5.1 Video Display Output

The video output section controls the transfer of video frames stored in memory to the internal TV encoder of the Vibratto. The output section consists of a programmable CRT controller capable of operating either in Master or Slave mode.

The video output section features internal line buffers which allow the outgoing luminance and chrominance data to match the internal clock rates with external pixel clock rates, easily facilitating YUV4: 2:2 to YUV4: 2:0 component and sample conversion. A polyphase filter achieves arbitrary horizontal decimation and interpolation.

Video Bus

The video bus has 8 YUV data pins that transfer luminance and chrominance (YUV) pixels in CCIR601 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance.

Video Post-Processing

The Vibratto video post-processing circuitry provides support for the color conversion, scaling, and filtering functions through a combination of special hardware and software. Horizontal up-sampling and filtering is done with a programmable, 7-tap polyphase filter bank for accurate non-integer interpolations. Vertical scaling is achieved by repeating and dropping lines in accordance with the applicable scaling ratio.

Video Timing

The video bus can be clocked either by double pixel clock and clock qualifier or by a single pixel clock. The double clock typically is used for TV displays, the single for computer displays.

Video Interface Registers

VID_SCN_HSTART

The write-only Video Screen Horizontal Start Address register contains the 13-bit horizontal pixel starting address of the active video display.

VID_SCN_HEND

The write-only Video Screen Horizontal End Address register contains the 13-bit horizontal pixel ending address of the active video display.

VID_SCN_VSTART

The write-only Video Screen Vertical Start Address register contains the 13-bit vertical scan line starting address of the active video display.

VID_SCN_VEND

The write-only Video Screen Vertical End Address register contains the 13-bit vertical scan line ending address of the active video display.

VID_SCN_VERTIRQ

The write-only Video Screen Vertical Line Interrupt register is selectable by software and contains the line in which a vertical interrupt will occur. Line 0 is the top of the screen, as defined by the leading edge of the VSYNC pin. Typically, an interrupt is set either just before or just after the active video display.

VID_SCN_HBLANK_START

The write-only Video Screen Horizontal Blanking Interval Start Address register contains the 13-bit starting address of the horizontal blanking interval for the active video display.

VID_SCN_HBLANK_STOP
The write-only Video Screen Horizontal Blanking Interval End Address register contains the 13-bit ending address of the horizontal blanking stop interval for the active video display.

VID_SCN_VBLANK_START
The Video Screen Vertical Blanking Interval Start Address register contains the 13-bit starting address of the vertical blanking interval for the active video display.

VID_SCN_VBLANK_STOP
The write-only Video Screen Vertical Blanking Interval Stop Address register contains the 13-bit ending address of the vertical blanking stop interval for the active video display.

VID_SCN_HSYNCWIDTH
The write-only Video Screen Horizontal Sync Width Pulse register contains the 13-bit value of the horizontal sync pulse width for the active video display. This register is needed only if sync direction is output

VID_SCN_HSYNCPERIOD
The write-only Video Screen Horizontal Sync Period register contains the 13-bit value for the period of the horizontal sync pulse used by the active video display. It is needed only if sync direction is output.

VID_SCN_VSYNCPERIOD
The write-only Video Screen Video Sync Period register contains the 13-bit value for the period of the vertical sync pulse used by the active video display. This register is needed only if sync direction is output.

VID_SCN_VSYNCPIXEL
The write-only Video Screen Vertical Sync Pixel register defines which pixel VSYNC will change on for the active video display. The number of pixels delayed from HSYNC that VSYNC will change on either the rising or falling edge of VSYNC. This register is needed only if sync direction is output

VID_SCN_VSYNCWIDTH
The write-only Video Screen Vertical Sync Pulse Width register defines the width of the 6-bit vertical sync pulse. It is needed only if sync direction is output

VID_SCN_VERTCOUNT
The read-only Video Screen Verital Counter register contains the current line of the vertical counter, and starts its counting at VSYNC line 0. This register is typically used for testing only.

VID_SCN_HORIZCOUNT
The read-only Video Screen Horizontal Counter register contains the current pixel of the horizontal counter, and starts its counting at HSYNC pixel 0. This register is typically used for testing only.

VID_SCN_COUNTER_CTL
The write-only Video Screen Counter Control register contains counter control bits for the inverted blank sync, inverted horizontal sync, and inverted vertical sync functions. This register initializes to 0x00 after reset.

VID_SCN_OUTPUTCNTL
The Video Screen Output Control register contains the control logic used to control the clamping and filtering characteristics of the signal being output to the video display.

VID_SCN_ITERFACECNTL
The Video Screen Interface Control register contains the control logic used to determine the signal output characteristics to the video display.

VID_SCN_RESETS
The Video Screen Reset register contains the control logic for reset events, including the reset pan and scan, horizontal filtering and DMA enabling functions. This register is set to 1 on reset.

VID_SCN_STATUS
The Video Screen Status register contains the status bits for the video section.

VID_SCN_OSD_HSTART
The OSD Video Screen Horizontal Start Address register contains the horizontal starting address value for the OSD, as referenced from the active display window.

VID_SCN_OSD_HEND
The OSD Video Screen Horizontal End Address register contains the 13-bit horizontal ending address value for the OSD, as referenced from the active video display.

VID_SCN_OSD_VSTART
The OSD Video Screen Vertical Start Address register contains the 13-bit vertical starting address value for the OSD, as referenced from the active video display.

VID_SCN_OSD_VEND
The OSD Video Screen Vertical End Address register contains the 13-bit vertical ending address value for the OSD, as referenced from the active video display.

VID_SCN_OSD_MISC
The OSD Video Screen Miscellaneous register contains the control logic and status bits for the OSD controller.

VID_SCN_OSD_PALETTE
These 16 registers contain the OSD palette.

6 SDRAM MEMORY

The memory bus interface generates all the control signals to interface with external memory. The Vibratto supports different configurations using the memory configuration bits SDCFG[1:0] (bits 12:11), the SD8BIT bit (bit 14), and SD64M bit (bit 15) in the BUSCON_DRAM_CONTROL register. Configurations can be implemented in many ways. The following table lists the typical SDRAM configurations used by the Vibratto.

Typical SDRAM Configurations:

Size (MB)	Bit Order				Memory Configuration
	SD64M	SD8BIT	SDCFG1	SDCFG0	
2.0	0	0	0	1	1 pc: 512Kx16x2 (16 Mb)
4.0	0	0	0	0	2 pcs: 512Kx16x2 (16 Mb)
4.0	0	1	0	1	2 pcs: 1Mx8x2 (16 Mb)
8.0	0	1	0	0	4 pcs: 1Mx8x2 (16 Mb)
8.0	1	0	X	X	1 pc: 1Mx16x4 (64 Mb)
16.0	1	0	X	X	2 pc: 1Mx16x4 (64 Mb)
16.0	1	1	X	X	2 pc: 2Mx8x4 (64 Mb)
16.0	1	1	X	X	1 pc: 2Mx16x4 (128 Mb)

The memory interface controls access to both external SDRAM or EDO memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers. At high clock speeds, the Vibratto memory bus interface has sufficient bandwidth to support the decoding and displaying of CCIR601 resolution images at full frame rate.

7 FLASH MEMORY

The decoder board supports AMD class Flash memories. Currently 4 configurations are supported:

FLASH_512K_8b
FLASH_1024K_8b
FLASH_512Kx2_8b
FLASH_512Kx2_16b

The Vibratto permits both 8- and 16-bit common memory I/O accesses with a removable storage card via the host interface.

8 SERIAL EEPROM MEMORY

An I2C serial EEPROM is used to store user configuration (i.e. language preferences, speaker setup, etc.) and software configuration.. Industry standard EEPROM range in size from 1kbit to 256kbit and share the same IC footprint and pinout. The default device is 2kbit, 256kx 8, SOIC8 SGS Thomson ST24C02M1 or equivalent.

9 ATA/IDE LOADER INTERFACE

The host interface can directly support ATAPI devices such as DVD drives or I/O controllers. PIO modes 0 through 4 are supported. The ATA/IDE interface can directly control two devices through the use of the HCS1FX# and HCS3FX# signals. The ATA/IDE interface of the Vibratto uses a command execution protocol that allows the operation of audio-CD and DVD loaders to coexist on the same type of interface cable that most computers use for CD loaders and hard disk drives.

Note: The decoder board supports the standard ATAPI electrical connections, but the software protocol within the drive is not always supported according to ATAPI specifications. Custom software may need to be developed and tested to support ATAPI drives from different manufacturers.

10 AUDIO INTERFACE AUDIO SAMPLING RATE AND PLL COMPONENT CONFIGURATION

The ES6008/18 Vibratto audio mode configuration is selectable, allowing it to interface directly with low-cost audio DACs and ADCs. The audio port provides a standard I^2S interface input and output and S/PDIF (IEC958) audio output. Stereo mode is in I^2S format while six channels Dolby Digital (5.1 channel) audio output can be channeled through the S/PDIF. The S/PDIF interface consists of a bi-phase mark encoder, which has low skew. The transmit I^2S interface supports the 128, 192, 256, 384, and 512 sampling frequency formats, where sampling frequency Fs is usually 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, or 192 kHz. The audio samples for the I^2S transmit interface can be 16, 18, 20, 24, and 32-bit samples.

For Linear PCM audio stream format, the Vibratto supports 48 kHz and 96 kHz. Dolby Digital audio only supports 48 kHz. The ES6008/18 Vibratto incorporates a built-in programmable analog PLL in the device architecture in order to generate a master audio clock. The MCLK pin is for the audio DAC clock and can either be an output from or an input to the ES6008/18 Vibratto. Audio data out (TSD) and audio frame sync (TWS) are clocked out of the Vibratto based on the audio transmit bit clock (TBCK). Audio receive bit clock (RBCK) is used to clock in audio data in (RSD) and audio receive frame sync (RWS).

11 FRONT PANEL

11.1 VFD CONTROLLER

The VFD controller is a NEC uPD16311. This controller is not a processor, but does include a simple state machine which scans the VFD and reads the front panel button matrix. The 16311 also includes RAM so it can store the current state of all the VFD icons and segments. Therefore, the 16311 need only be accessed when the VFD status changes and when the button status is read. The ES6008/ES6018 can control this chip directly using PIO pins or can allow the front panel PIC to control the VFD.

12 MISCELLANEOUS FUNCTIONS

12.1 RESET CIRCUITRY

Two different chips are supported to provide the power-on-reset DS1811 or AAT3520.

12.2 VOLTAGE REGULATORS

There are 7812, 7805 and LM317 linear regulator ICs on the power supply to generate +5V, -5V, +12V, -12V and +3.3V for the device. On the standby mode just +12Vst and +5V supplies are generating for standby power consumption.

The ES6008/18 requires 2.5V to operate. This voltage is generated from +5V.

13 CONNECTORS

13.1 ATAPI DRIVE STANDARD CONNECTOR

The I/O connector is a 40-pin connector as shown in figure A.1, with pin assignments as shown in table A.1. The connector shall be keyed to prevent the possibility of installing it upside down. A key is provided by the removal of pin 20. The corresponding pin on the cable connector shall be plugged.

The cable plug, not the receptacle, governs the pin locations. The way in which the receptacle is mounted on the printed circuit board affects the pin positions, and pin 1 shall remain in the same relative position. This means the pin numbers of the receptacle may not reflect the conductor number of the plug. The header receptacle is not polarized, and all the signals are relative to pin 20, which is keyed.

By using the plug positions as primary, a straight cable can connect devices. As shown in figure A.1, conductor 1 on pin 1 of the plug shall be in the same relative position no matter what the receptacle numbering looks like. If receptacle numbering was followed, the cable would have to twist 180 degrees between a device with top-mounted receptacles, and a device with bottom-mounted receptacles.

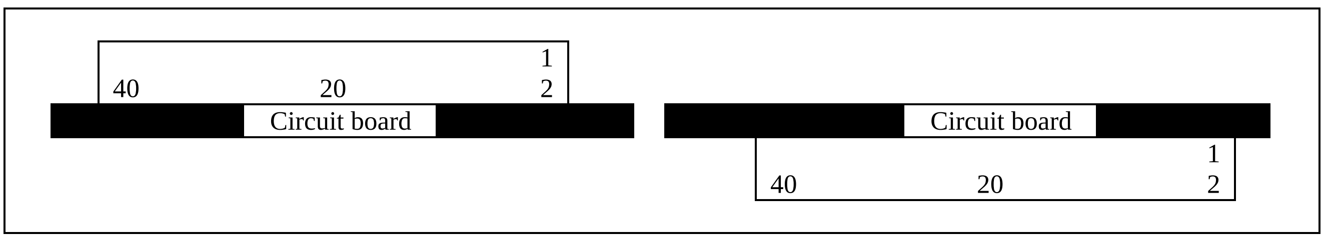


Figure A.1 - 40-pin connector mounting

Table A.1 - 40-pin connector interface signals

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-	23	23	24	24	Ground
DIOR-	25	25	26	26	Ground
IORDY	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground

Recommended part numbers for the mating connector and cable are shown below, but equivalent parts may be used.

Connector (40 pin)	3M 3417-7000 or equivalent
Strain relief	3M 3448-2040 or equivalent

Flat cable (stranded 28 AWG)	3M 3365-40 or equivalent
Flat cable (stranded 28 AWG)	3M 3517-40 (shielded) or equivalent

13.2 SCART CONNECTORS

Pinout of the scart connector:

1 → Audio Right Out
2 → Audio Right In
3 → Audio Left / Monu Out
4 → Audio Gnd
5 → Blue Gnd
6 → Audio Left / Mono In
7 → Blue
8 → Control Voltage
9 → Green Gnd
10 → Comms Data 2

11 → Green
12 → Comms Data 1
13 → Red Gnd
14 → Comms Data Gnd
15 → Red
16 → Fast Blanking
17 → Video Gnd
18 → Fast Blanking Gnd
19 → Composite Video In
20 → Composite Video Out
21 → Shield

Some cheaper SCART cables use unshielded wires, which is just about acceptable for short cable lengths. For longer lengths, shielded co-ax cable become essential.

Scart Signals:

Audio signals
0.5V RMS, <1K output impedance, >10K input impedance.

Red, Green, Blue
0.7Vpp ±2dB, 75R input and output impedance. Note that the Red connection (pin 20) can alternatively carry the S-VHS Chrominance signal, which is 0.3V.

Composite Video / CSync
1Vpp including sync, ±2dB, 75R input and output impedance.Bandwidth = 25Hz to 4.8MHz for normal TV Video de-emphasis to CCIR 405.1 (625-line TV)

Fast Blanking
75R input and output impedance. This control voltage allows devices to over-ride the composite video input with RGB inputs, for example when inserting closed caption text. It is called fast because this can be done at the same speeds as other video signals, which is why it requires the same 75R impedances.

> **0 to 0.4V**: TV is driven by the composite video input signal (pin 19). Left unconnected, it is pulled to 0V by its 75R termination.
>
> **1V to 3V**: the TV is driven by the signals Red, Green, Blue and composite sync. The latter is sent to the TV on pin 19. This signal is useful when using a TV to display the RGB output of devices such as home computers with TV-compatible frame rates. Tying the signal to 5V via 100R forms a potential divider with the 75R termination, holding the signal at around 2V. Alternatively, if a TTL level (0 to 5V) negative sync pulse is available, this will be high during the display periods, so this can drive the blanking signal via a suitable resistor.

Control Voltage
> **0 to 2V** = TV, Normal.
> **5 to 8V** = TV wide screen
> **9.5 to 12V** = AV mode

IC500 8051 Micro Controller's Main Functions:

There are 2 main functions of the IC500 8051 micro controller; signal switching and standby controlls. IC500 communicates with ES80X6 microcontroller by using I^2C bus. (AUX0, AUX1 signals)

Multiplexer (MUX) control signals for signal switching supplied by IC500. These MUX signals are using the select signal sources and input-output signals.

MUX Control Signal list is shown in the following figure:

AV1000 MUX Table for 8051 micro controller

	DVD	AUX1	AUX2 Analog Audio	AUX2 Digital Audio	Tuner	TV	Default Standby	AUX2 Standby
INH_MUX1	0	0	0	0	0	1	1	0
INH_MUX2	0	0	0	0	0	1	1	0
INH_MUX3	0	0	0	0	0	0	1	0
INH_MUX4	0	0	0	0	0	0	1	0
SW_MUX1	1	1	0	0	1	1	1	0
SW_MUX2	1	1	0	0	1	1	1	0
A_MUX3	0	0	1	1	1	0	1	0
B_MUX3	0	0	0	0	1	1	1	0
A_MUX4	1	0	1	1	1	1	1	1
B_MUX4	0	0	0	0	0	0	1	0
C_MUX4	0	0	0	0	0	0	1	0
SW_BM1	0	0	0	1	0	0	1	0
SW_BM2	1	1	1	1	1	1	1	1

14. CIRCUIT DESCRIPTION

14.1 POWER SUPPLY:

- Socket PL800 is the 220VAC input.
- 3.5A fuse F800 is used to protect the device against short circuit and unexpected overloads.
- Line filter and capacitors L800, C800 and C803 are used to block the parasitic coming from the mains. They also prevent the noise, produced in the circuit, from being injected to the line.
- Voltage is rectified by using diodes D805 diode bridge. Using capacitor C815 (220µf) a DC voltage is produced. (310- 320VDC).
- The current in the primary side of the transformer TR800 comes to the SMPS IC (IC800 MC44608). The SMPS IC has a eight-pin DIP-8 package and an external MOSFET with a cooler is mounted on it. It has a built-in oscillator, overcurrent and overvoltage protection circuitry and runs at 100kHz. It starts with the current from the primary side of the transformer and follows the current from the feedback winding.
- Feedback current is deteceted by optocoupler IC803. Depending on the control current coming from the secondary side, SMPS IC keeps the output voltage constant by controlling the duty cycle of the ~30kHz signal (PWM) at the primary side of the transformer.

- Voltages on the secondary side are as follows: +20 Volts at D811, +10 Volts at D808, +14V at D810, -22 Volts at D812, +12Vst at Q804.
- Using the output of the D808, a photo diode inside of the IC803 generates feedback signal bu using optocoupler's photo transistor. This photo transistor adjusts the control voltage at the IC800 pin3. The voltage at this pin effects the pwm output frequency on the IC800 pin5. And finally output voltages reach their correct values by this way.
- Voltage regulator IC805 (LM7805) supplies +5 Volts,

IC807 supplies +5V (off on standby mode),
IC809 supplies +3.3V (by using output of the IC807, off on standby mode),
Q804 supplies +12Vst,
IC806 supplies +12V (off on standby mode),
Q808 supplies -5V,
D812 supplies -22V.
Standby mode controlled by standby control transistors Q805, Q806, Q807. Standby control signal comes from PL805 connector and generated by 8051 micro controllers.

- –22 Volts is used to feed the VFD (Vacuum Fluorescent Display) driver IC on the front panel. Using diode R844, –22V is decreased and connected to the filament winding to produce the DC offset for the filaments.

14.2 FRONT PANEL:

- All the functions on the front panel are controlled by IC1 (ES6008/18) on the mainboard. Key scanning and IR checking operations on the standby mode are controlled by IC500.
- ES60X8 IC sends the commands to IC1 uPD16311 via socket PL1 (pins 2,3 and 4).
- There are 16 keys scanning function, 2 LED outputs, 1 Stand-by output and VFD drivers on IC2.
- Pin 52 is the oscillator pin and is connected via R5 56K.
- LED D5 is bright red in stand-by mode and soft red when the device is on.
- Vacuum fluorescent display MD1 is specially designed for AV1000.
- The scanned keys are transmitted via IC3 to IC1 on the mainboard.
- IR remote control receiver module IC2 (TSOP1836) sends the commands from the remote control directly to IC1 and IC500.
- Socket PL2 carries the VFD filament voltage and –22 Volts.

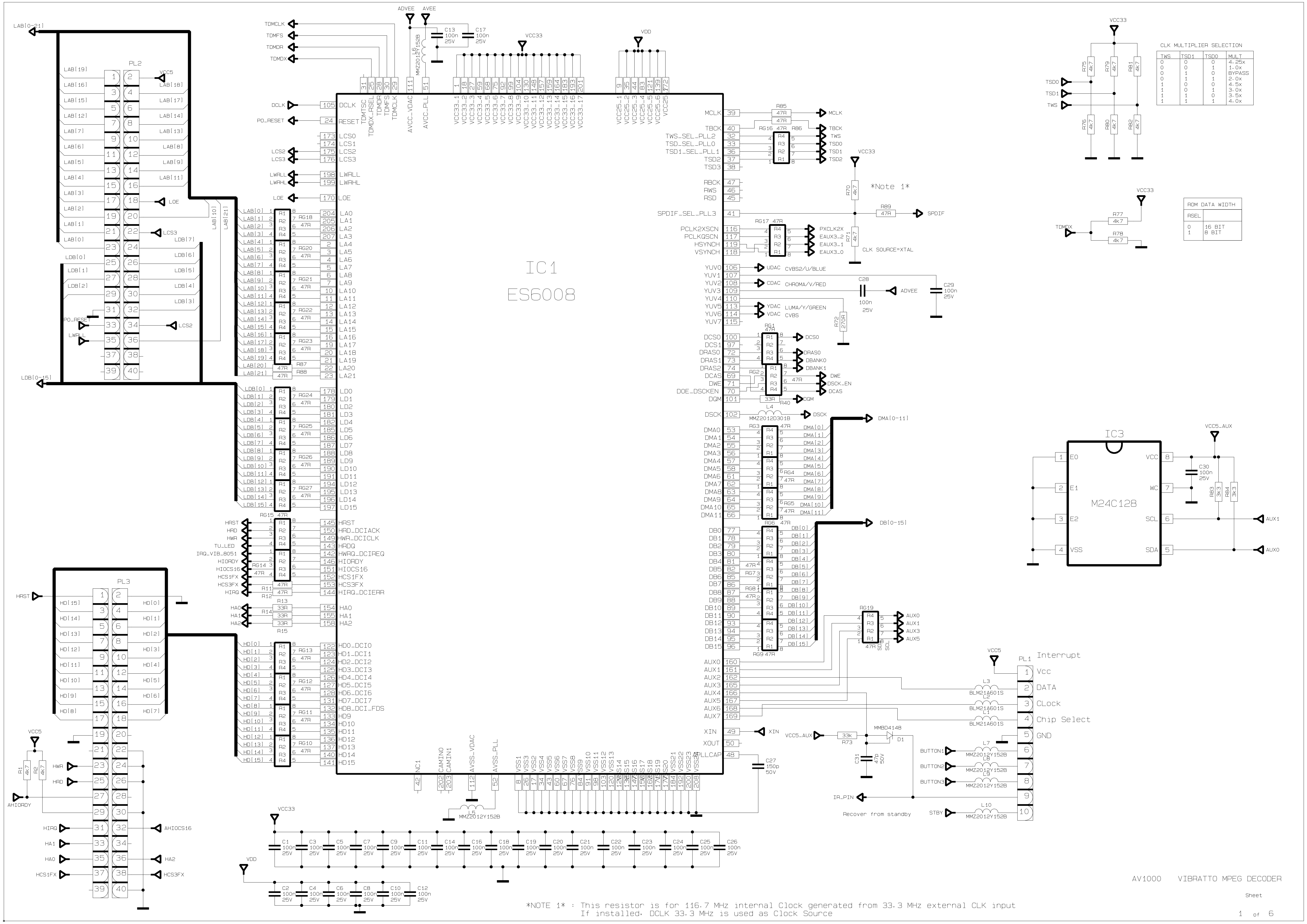
14.3 I/Os and Back Panel:

- PL303 connector on the main board carries digital audio and command signals to Class-D amplifier board (DDX Board). Command signals are carried by an I^2C bus and digital audio signals are carried by I^2S bus interface. After processing and amplification of audio signals amplificated audio signals comes to back panel with this order(left to right): Front Left, Front Right, Rear Right, Center, Rear Left and Subwoofer.

- There are 1 DOUBLE SCART connector PL300 (Scart1 is for input on Scart mode and Scart2 is for TV output), 3 pieces RCA audio jacks (L,R, Active Subwoofer) for audio output, 3 pieces RCA A/V jacks for CVBS,L,R inputs on AV mode, 1 RCA connector for CVBS out, 1 Connector for SVHS output.
- There are two op-amp ICs IC109 and IC110 for L,R and Active Subwoofer output after DAC ICs (IC107 or IC108). IC109 generates L and R audio outputs; IC110 generates Active Subwoofer output. JK302 is the output connector for L,R and Active SW signals.
- JK306 is the CVBS, L and R input connector on the AV mode.
- Radio L,R, RCA Connector L,R, Scart connector input L,R, TV scart L,R input (TV mode, for future use) are selected as analog audio source of the system by IC402 MUX IC. This selected analog audio source comes to the IC412 (LM833 op-amp IC) for amplification. By using ADC IC407 (CS5333) L and R signals becomes digital audio signal and comes to ES60X8 for audio proccessing operations.

14.4 DDX Board (Class-D Amplifier):

- Chipset : 2xDDX-4100 + 3x DDX-2060
- Architecture : Full-Bridge x 6
- Power Supply : + 20V unipolar supply @ 6A max., + 3.3V @ 0.1A typ.
- Audio Input Interface: Serial I2S
- Control Interface: I2C
- Power Interface: + 20V @ 6A Max., + 3.3V@ 0.1A Typ
- Output Interface: Speaker Level
- Speakers: 8 Ohm Satellites + 4 Ohm Subwoofer
- Output Power: 5 x 15 W + 25 W
- DDX Audio proccess ICs are U1 and U2 (DDX-4100A).
- U1 and U2 ICs on the DDX board have digital audio input with I^2S bus.
- I^2S signals are SDI_1, SDI_2, SDI_3 serial data lines U1,U2 pin1,pin2,
  LRCK Left-Right clock signal U1,U2 pin3,
  SCK serial clock signal U1, U2 pin4.
- For mute function U1 and U2 ICs uses EAPD (pin35, External Amplifier Powerdown) signal. This signal comes to the power output ICs U3, U4 and U5 (DDX-2060 ICs Pin25) as power down signal.



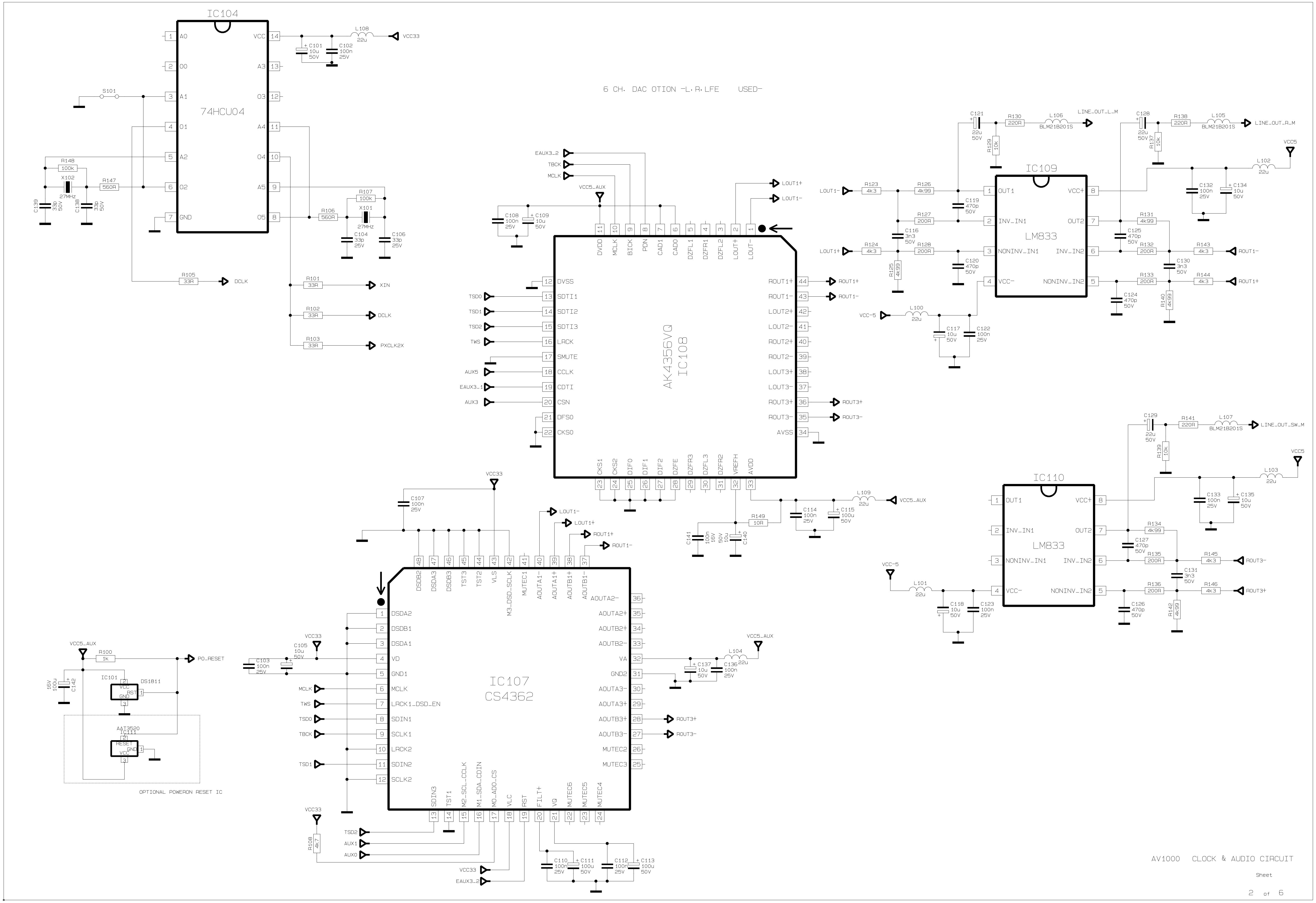
CLK MULTIPLIER SELECTION

TWS	TSD1	TSD0	MULT
0	0	0	4.25x
0	0	1	1.0x
0	1	0	BYPASS
0	1	1	2.0x
1	0	0	4.5x
1	0	1	3.0x
1	1	0	3.5x
1	1	1	4.0x

ROM DATA WIDTH

RSEL	
0	16 BIT
1	8 BIT

NOTE 1 : This resistor is for 116.7 MHz internal Clock generated from 33.3 MHz external CLK input
If installed, DCLK 33.3 MHz is used as Clock Source



AV1000 CLOCK & AUDIO CIRCUIT

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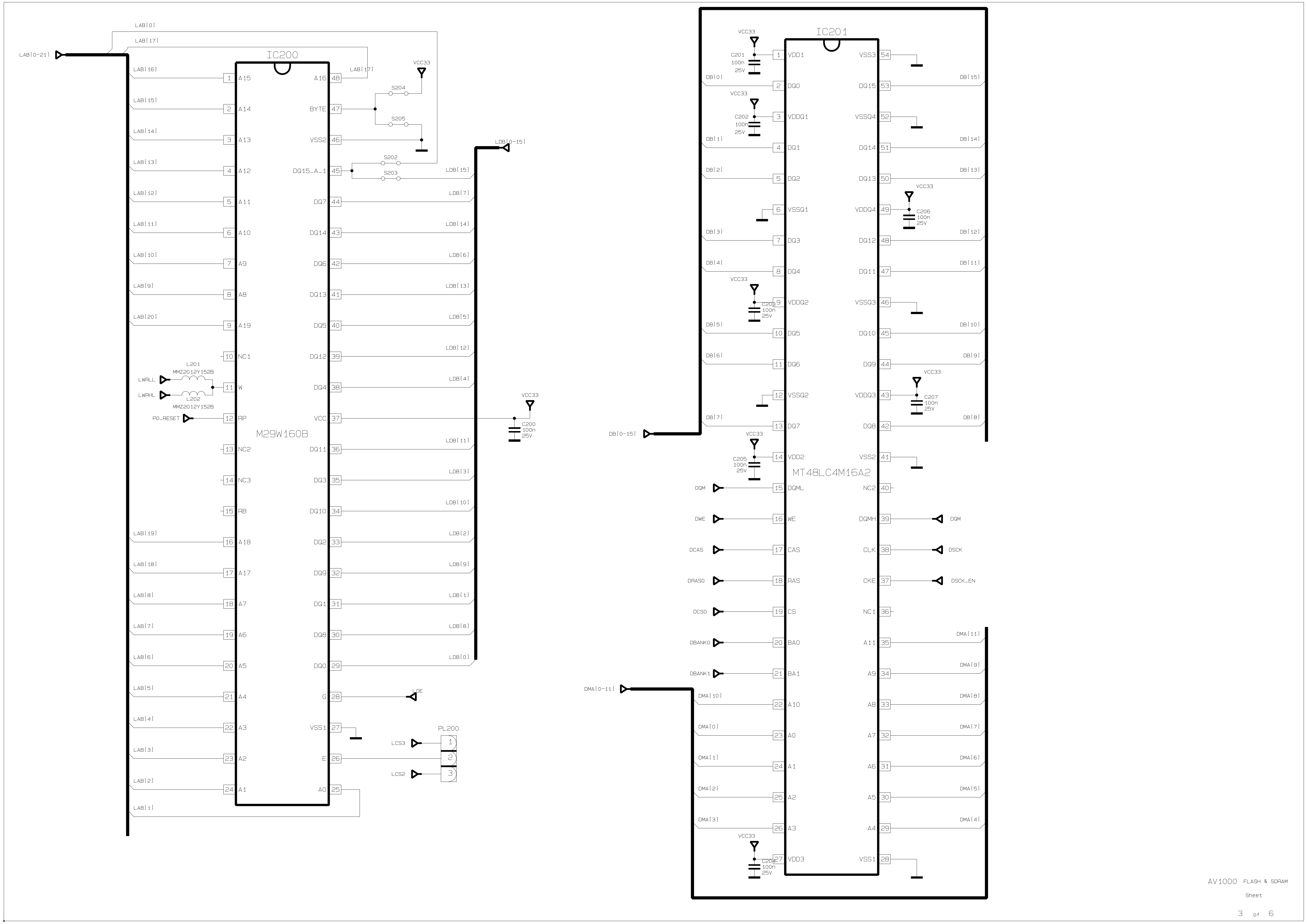

AV1000 FLASH & SDRAM

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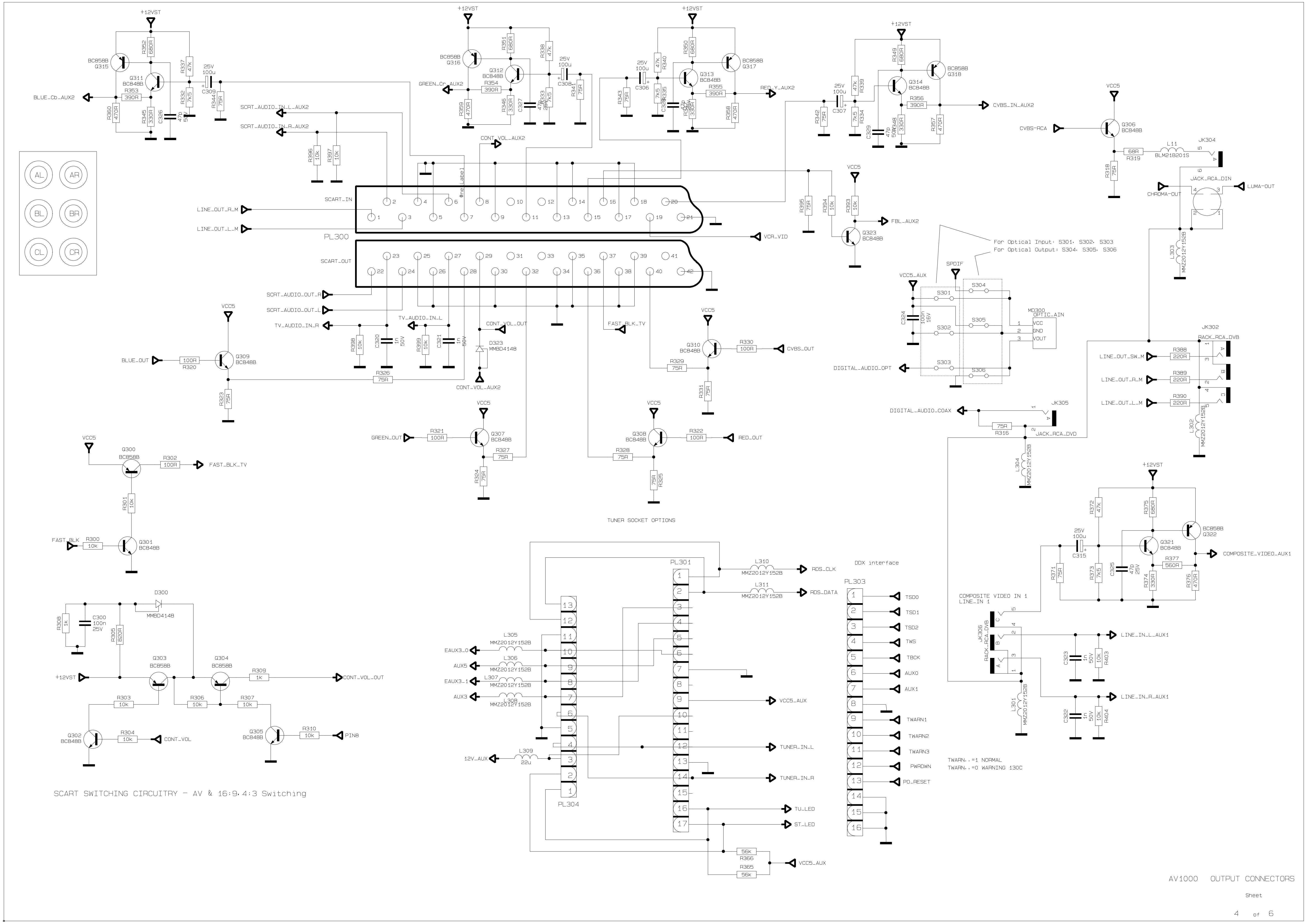

SCART SWITCHING CIRCUITRY - AV & 16:9-4:3 Switching
TUNER SOCKET OPTIONS
DDX interface
For Optical Input: S301, S302, S303
For Optical Output: S304, S305, S306
COMPOSITE VIDEO IN 1
LINE_IN 1
TWARN..=1 NORMAL
TWARN..=0 WARNING 130C
SCART_IN
SCART_OUT
PL300
PL301
PL303
PL304
JK302
JK304
JK305
JK306
MD300
OPTIC_AIN
BLUE_Cb_AUX2
GREEN_Cr_AUX2
RED_Y_AUX2
CVBS_IN_AUX2
CVBS-RCA
SCRT_AUDIO_IN_L_AUX2
SCRT_AUDIO_IN_R_AUX2
CONT_VOL_AUX2
LINE_OUT_R_M
LINE_OUT_L_M
VCR_VID
FBL_AUX2
SCRT_AUDIO_OUT_R
SCRT_AUDIO_OUT_L
TV_AUDIO_IN_R
TV_AUDIO_IN_L
CONT_VOL_OUT
FAST_BLK_TV
CVBS_OUT
BLUE_OUT
GREEN_OUT
RED_OUT
FAST_BLK
CONT_VOL
PIN8
DIGITAL_AUDIO_OPT
DIGITAL_AUDIO_COAX
JACK_RCA_DVD
JACK_RCA_DIN
CHROMA-OUT
LUMA-OUT
RACK_RCA_DVB
LINE_OUT_SW_M
COMPOSITE_VIDEO_AUX1
LINE_IN_L_AUX1
LINE_IN_R_AUX1
RDS_CLK
RDS_DATA
EAUX3_0
AUX5
EAUX3_1
AUX3
12V_AUX
VCC5_AUX
TUNER_IN_L
TUNER_IN_R
TU_LED
ST_LED
TSD0
TSD1
TSD2
TWS
TBCK
AUX0
AUX1
TWARN1
TWARN2
TWARN3
PWRDWN
PO_RESET
AV1000 OUTPUT CONNECTORS
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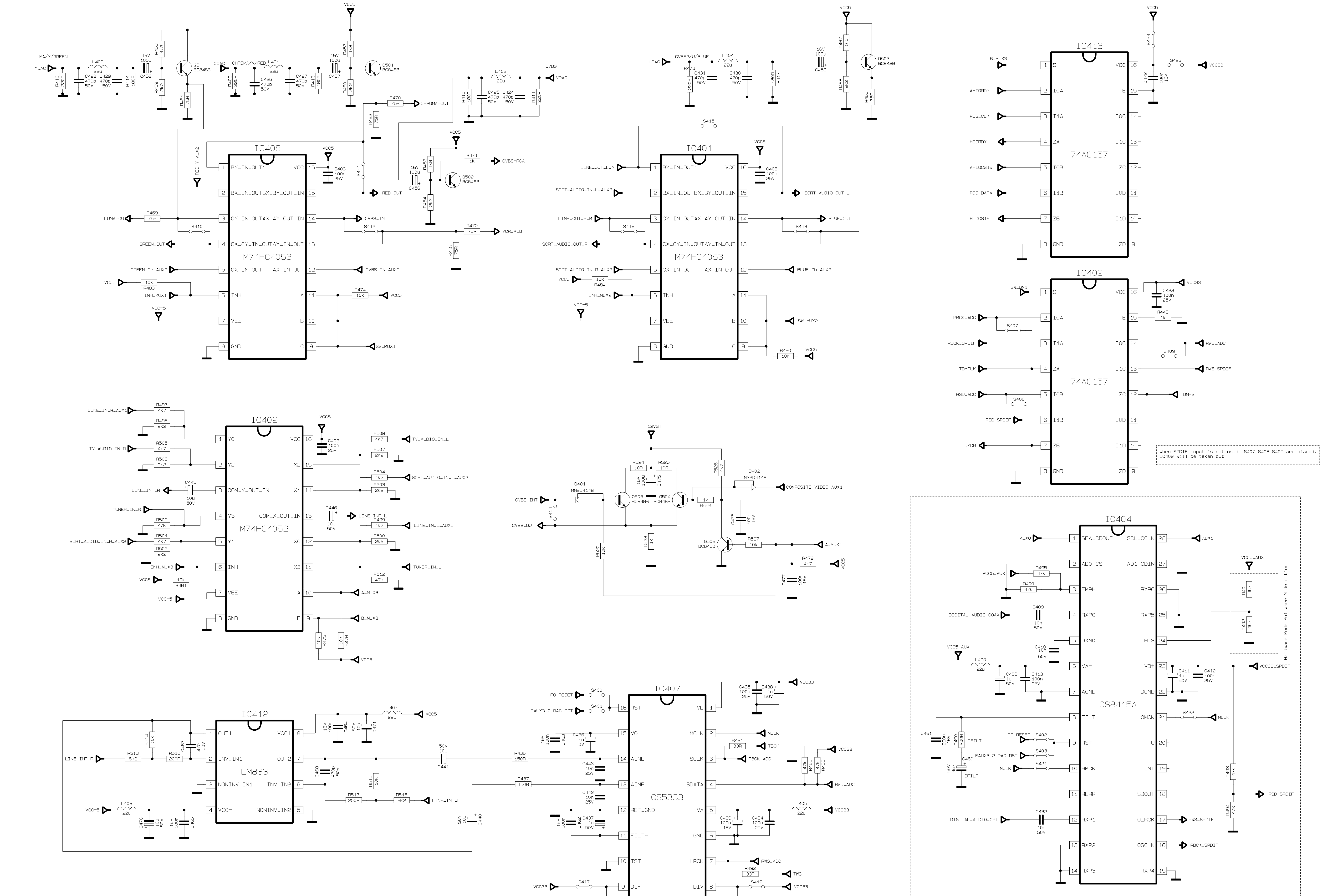
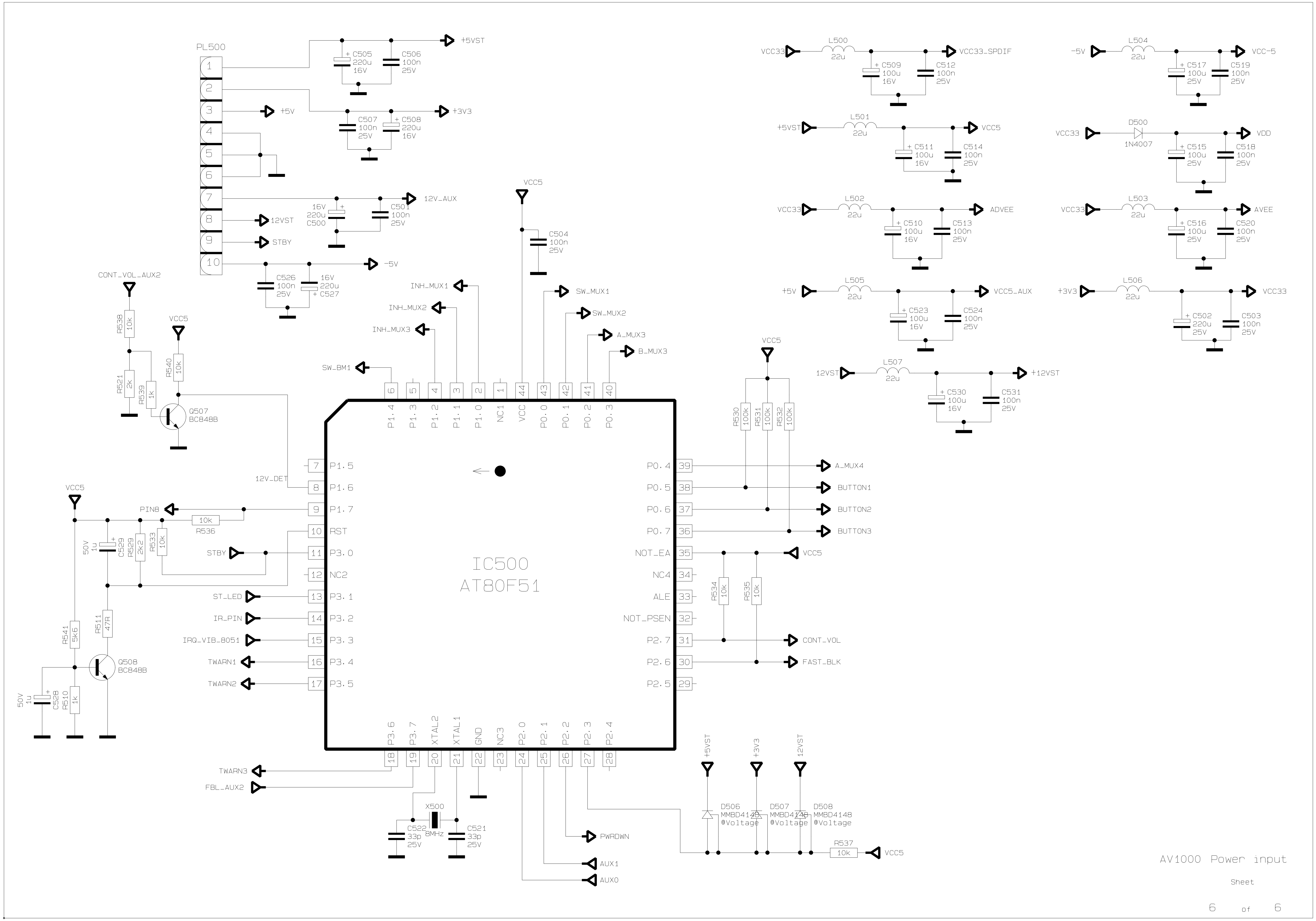


AV1000 ANALOG MUX & SPDIF RECEIVER

Optional SPDIF circuit


PL500
+5VST
+5V
+3V3
12V_AUX
12VST
STBY
-5V
C505 220u 16V
C506 100n 25V
C507 100n 25V
C508 220u 16V
C500 220u 16V
C501 100n 25V
C526 100n 25V
C527 220u 16V
C504 100n 25V
VCC5
CONT_VOL_AUX2
R538 10k
R521 2k
R539 1k
R540 10k
Q507 BC848B
12V_DET
PIN8
R536 10k
C529 1u 50V
R529 2k2
R533 10k
R511 47R
R541 5k6
Q508 BC848B
C528 1u 50V
R510 1k
ST_LED
IR_PIN
IRQ_VIB_8051
TWARN1
TWARN2
TWARN3
FBL_AUX2
INH_MUX1
INH_MUX2
INH_MUX3
SW_BM1
SW_MUX1
SW_MUX2
A_MUX3
B_MUX3
IC500
AT80F51
A_MUX4
BUTTON1
BUTTON2
BUTTON3
R530 100k
R531 100k
R532 100k
R534 10k
R535 10k
CONT_VOL
FAST_BLK
X500 8MHz
C522 33p 25V
C521 33p 25V
PWRDWN
AUX1
AUX0
D506 MMBD4148 @Voltage
D507 MMBD4148 @Voltage
D508 MMBD4148 @Voltage
R537 10k
VCC33
L500 22u
VCC33_SPDIF
C509 100u 16V
C512 100n 25V
L501 22u
VCC5
C511 100u 16V
C514 100n 25V
L502 22u
ADVEE
C510 100u 16V
C513 100n 25V
L505 22u
VCC5_AUX
C523 100u 16V
C524 100n 25V
L507 22u
+12VST
C530 100u 16V
C531 100n 25V
L504 22u
VCC-5
C517 100u 25V
C519 100n 25V
D500 1N4007
VDD
C515 100u 25V
C518 100n 25V
L503 22u
AVEE
C516 100u 25V
C520 100n 25V
L506 22u
C502 220u 25V
C503 100n 25V
AV1000 Power input
Sheet
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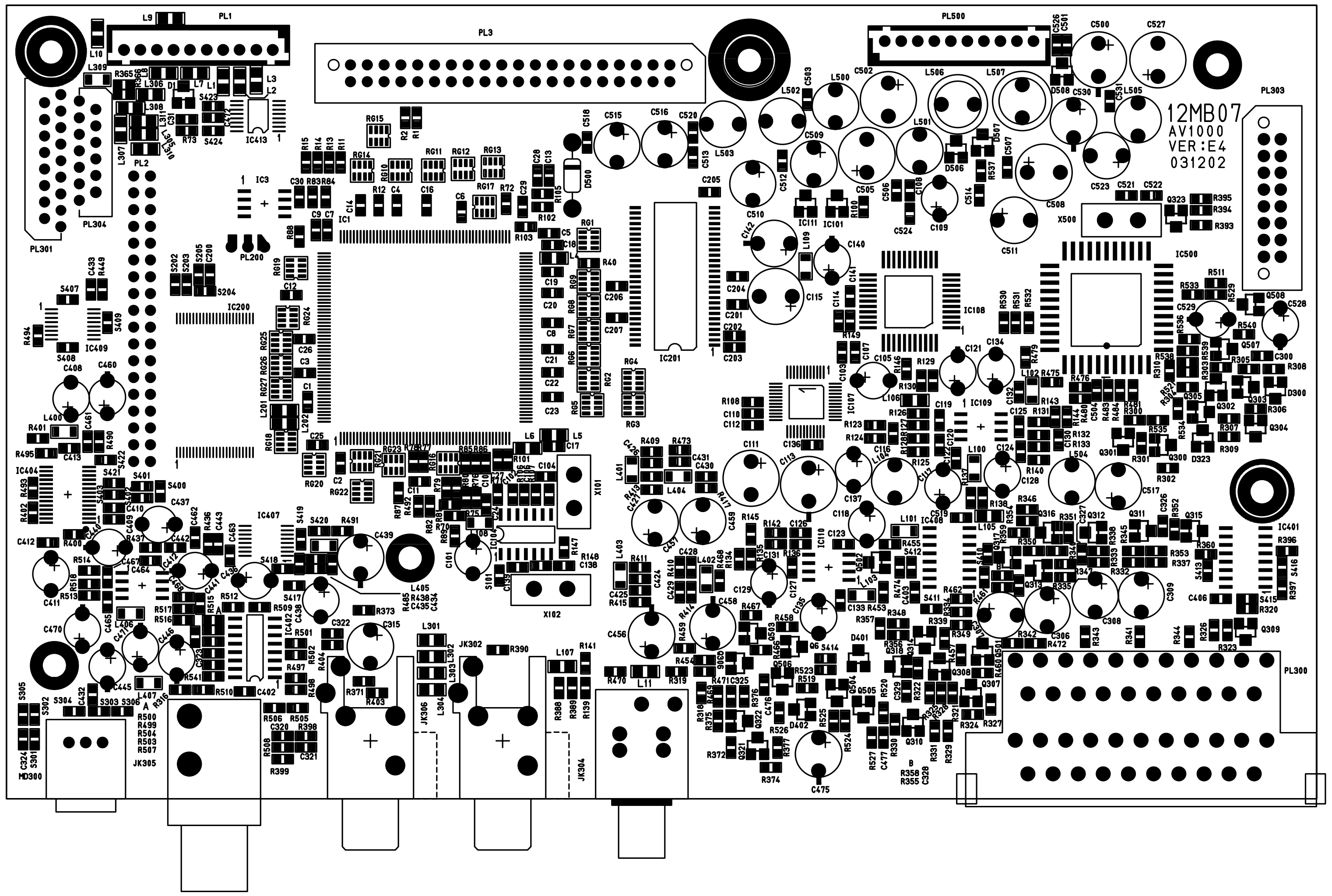
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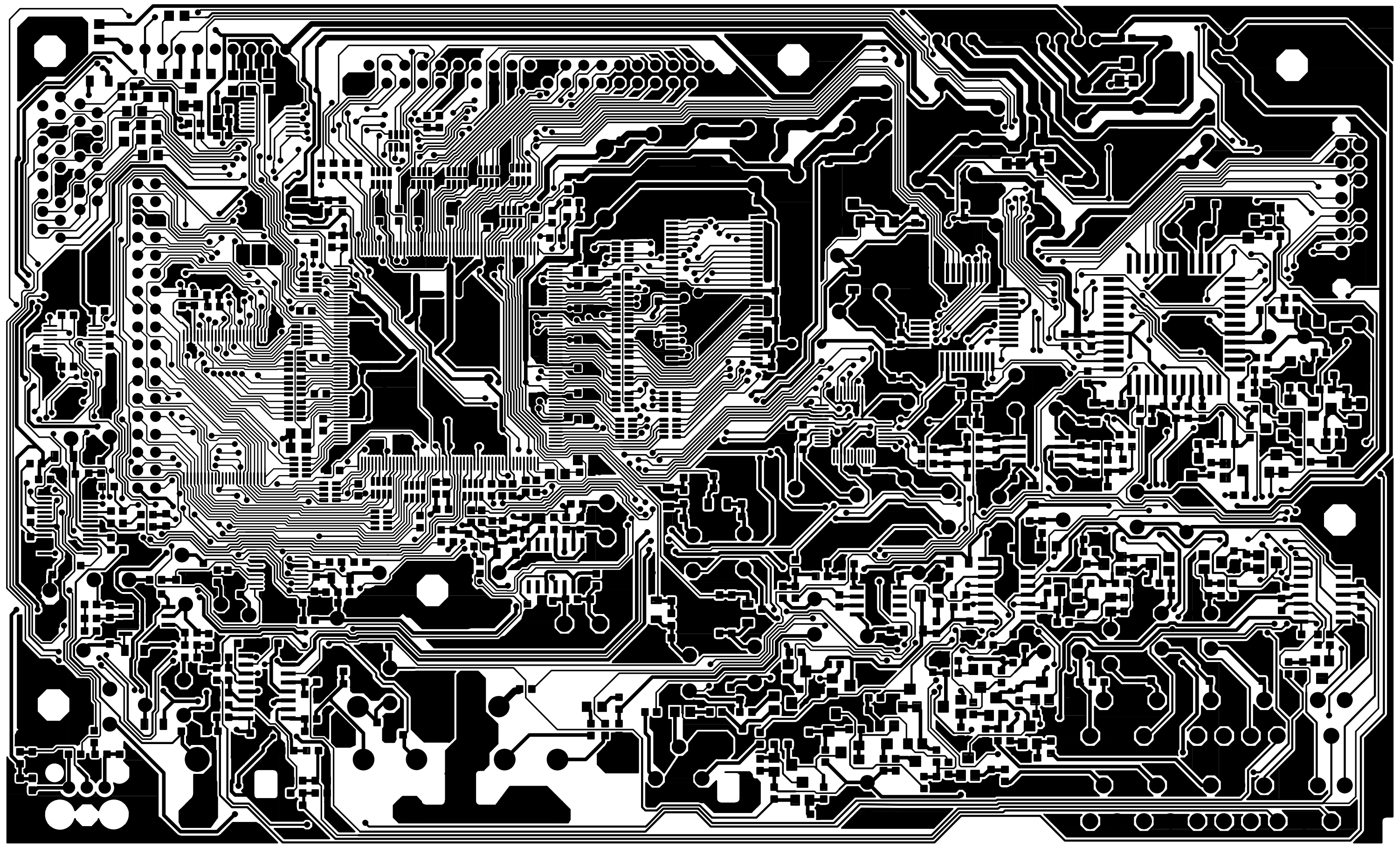

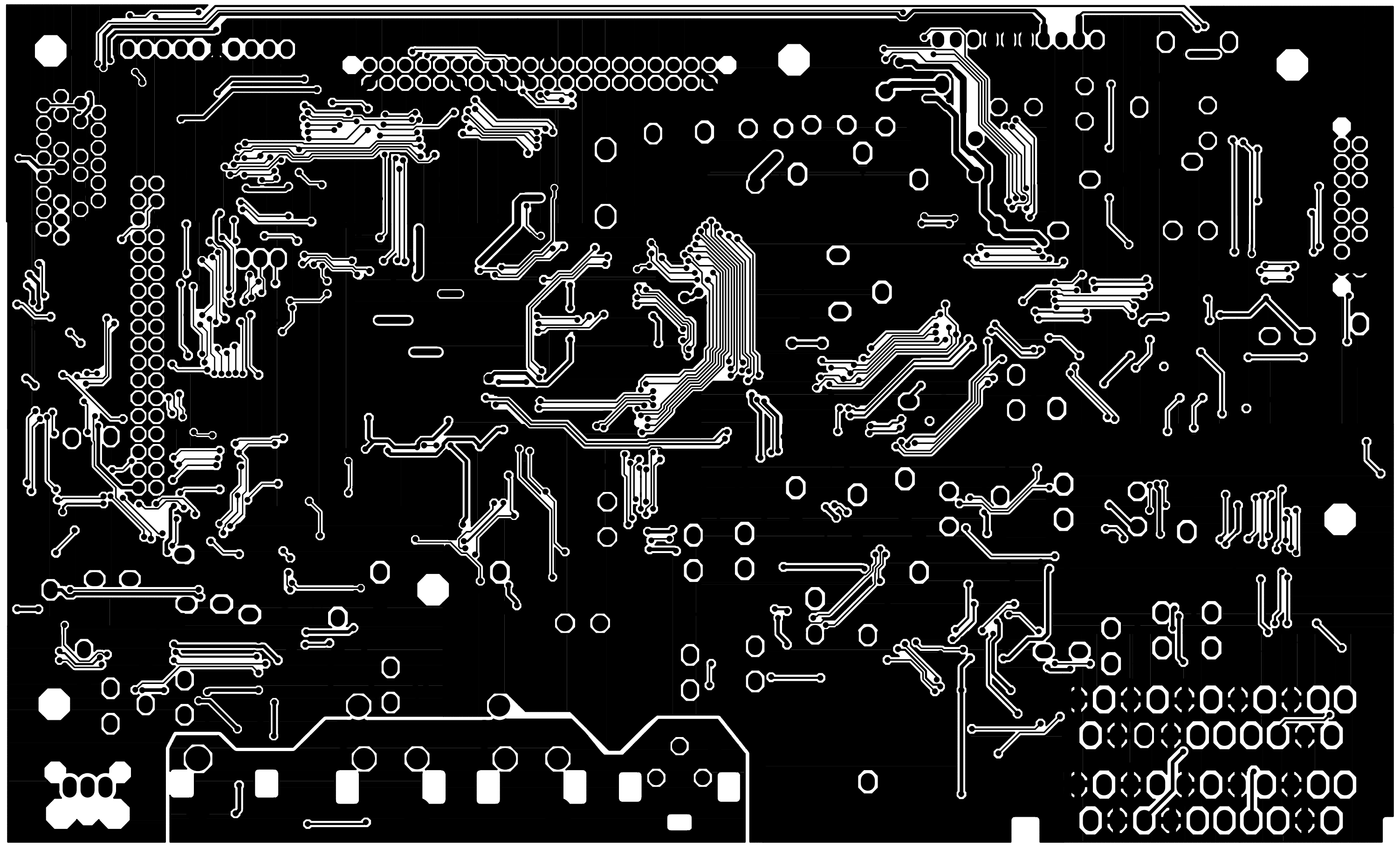

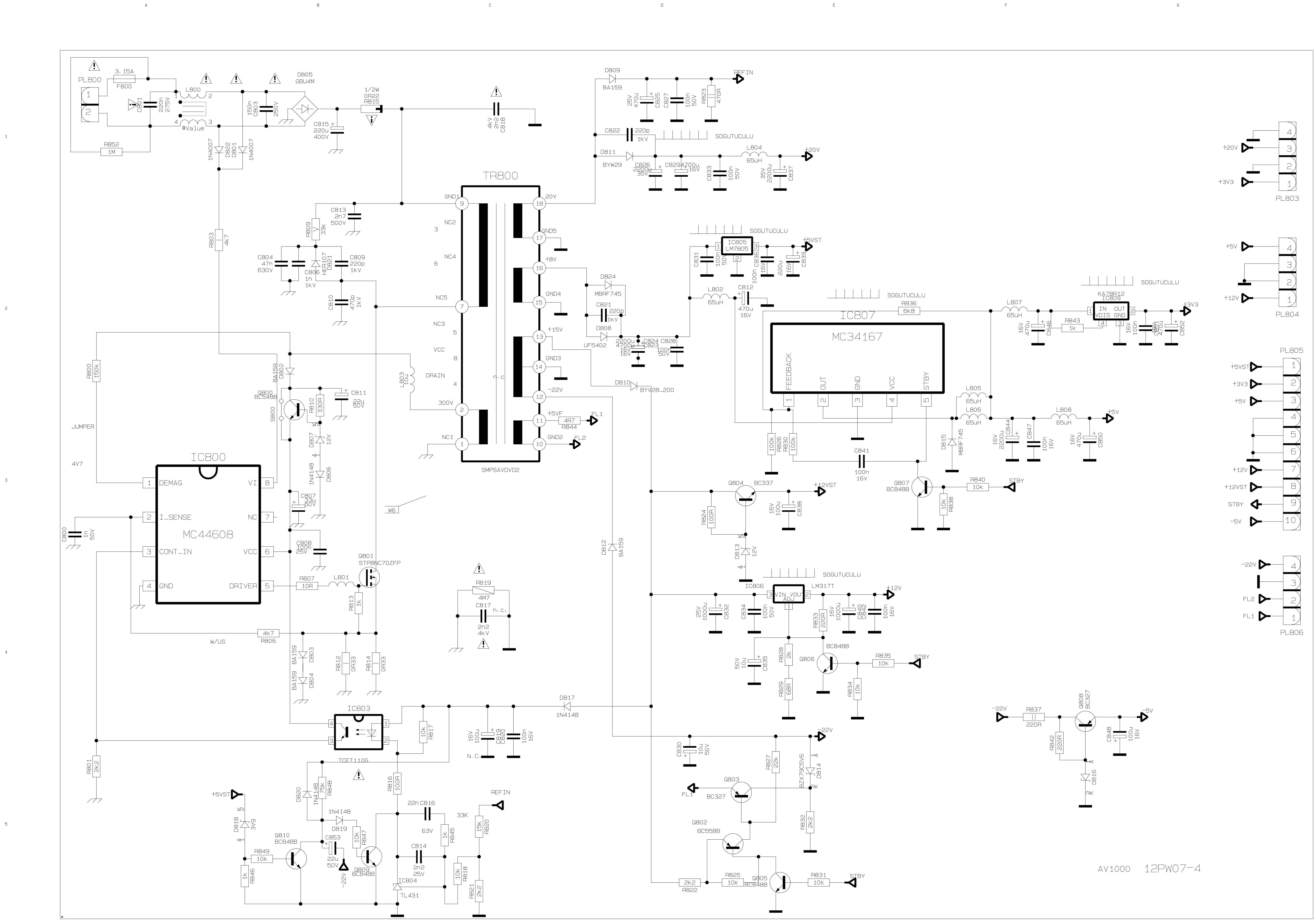

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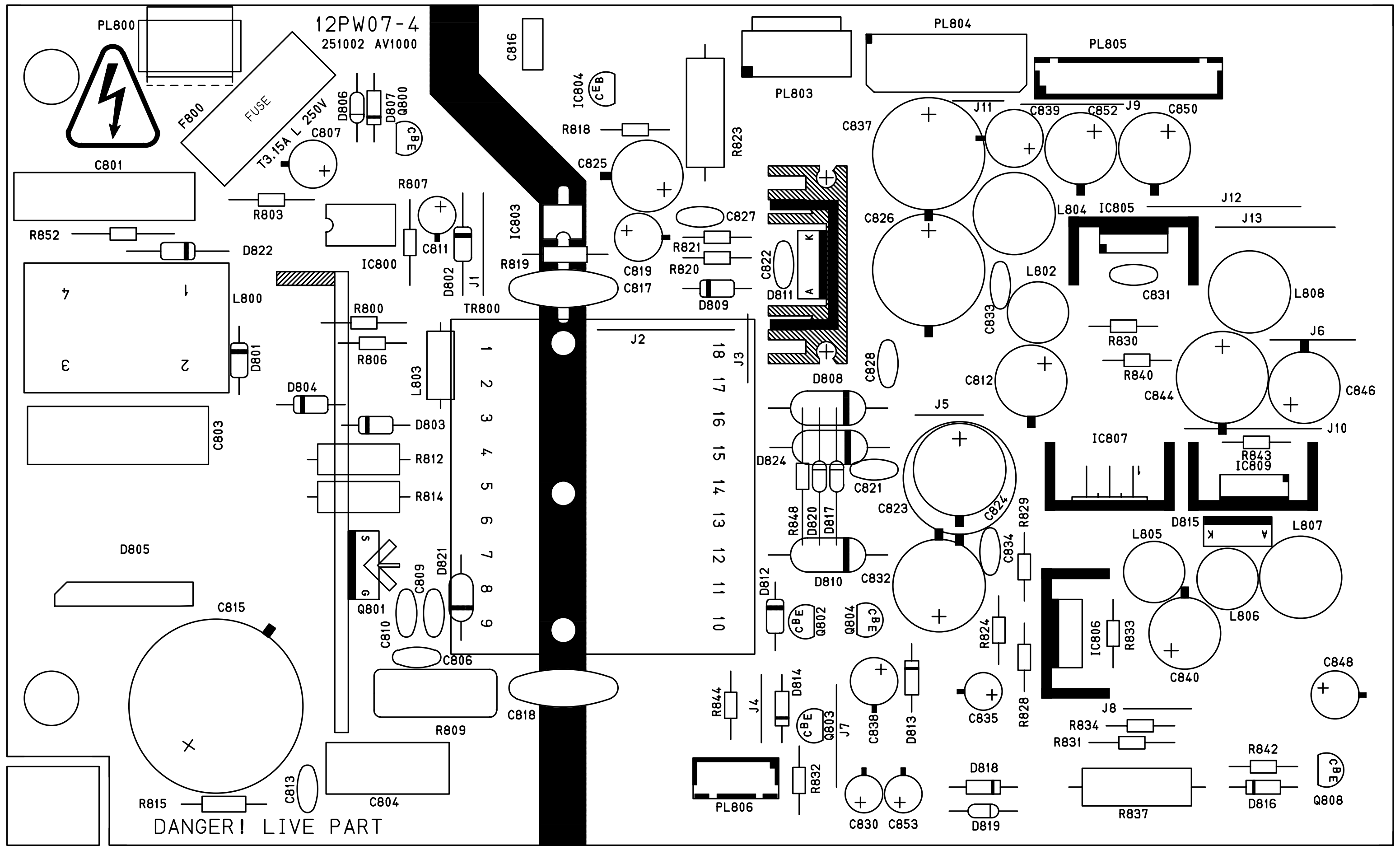
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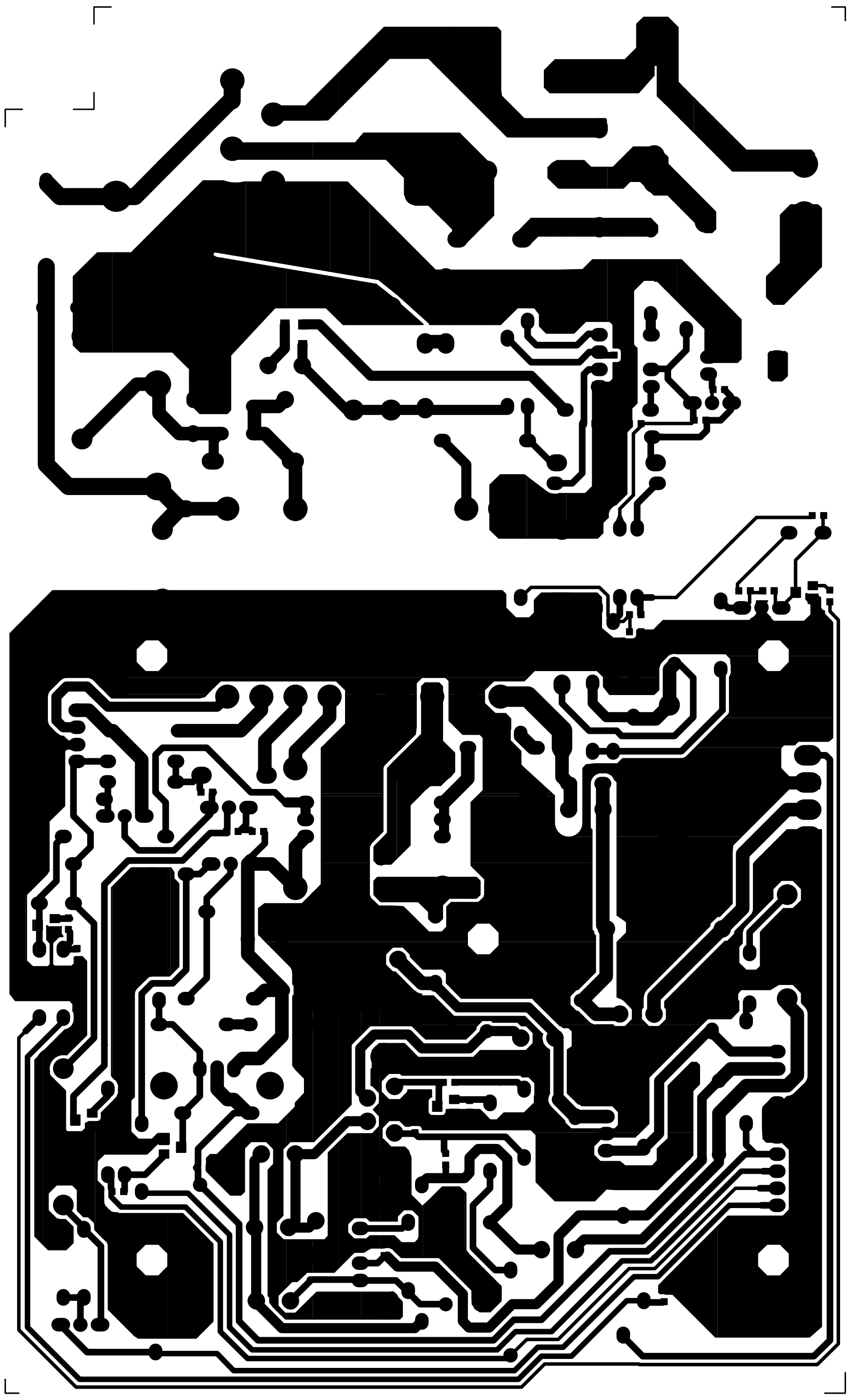

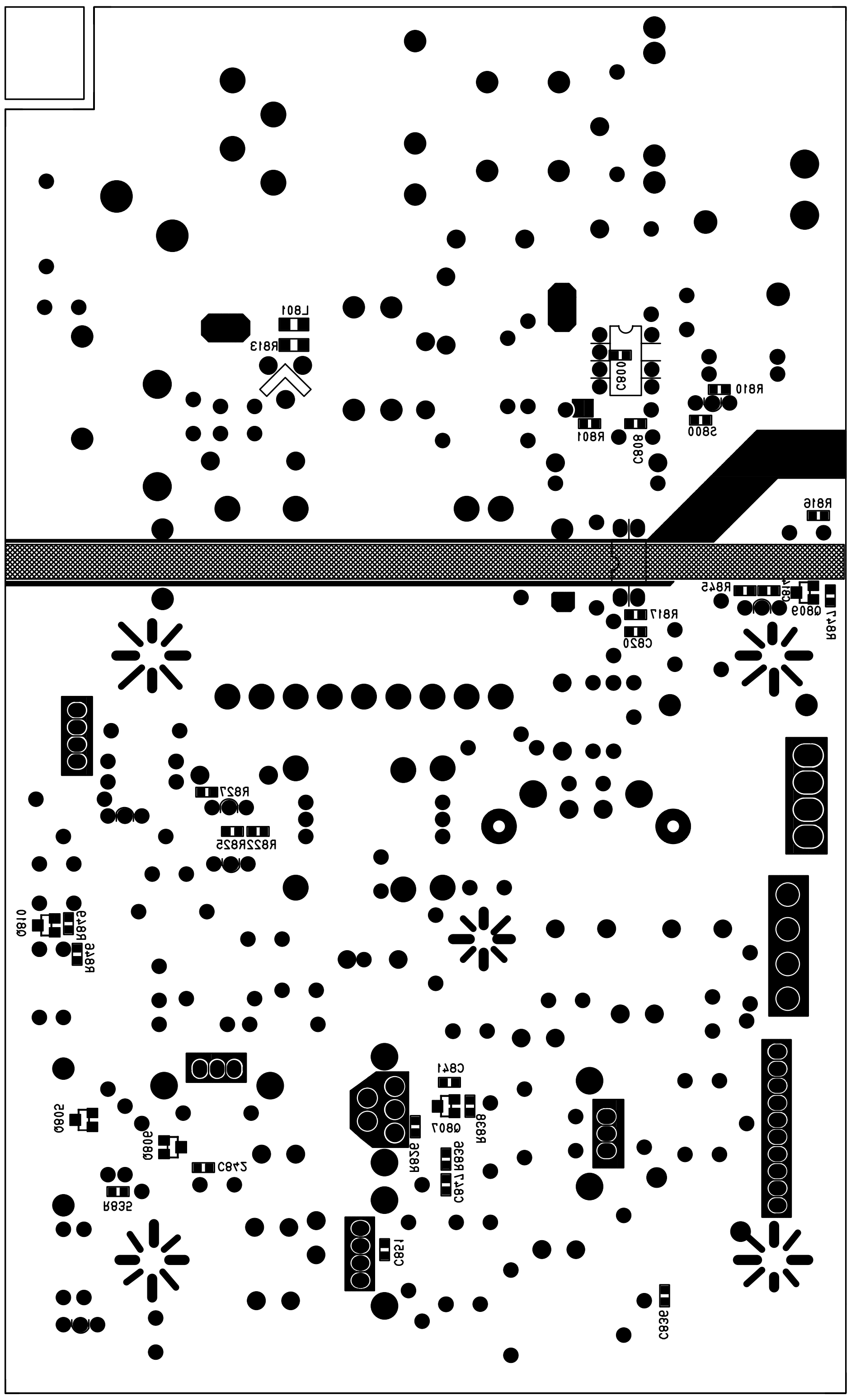

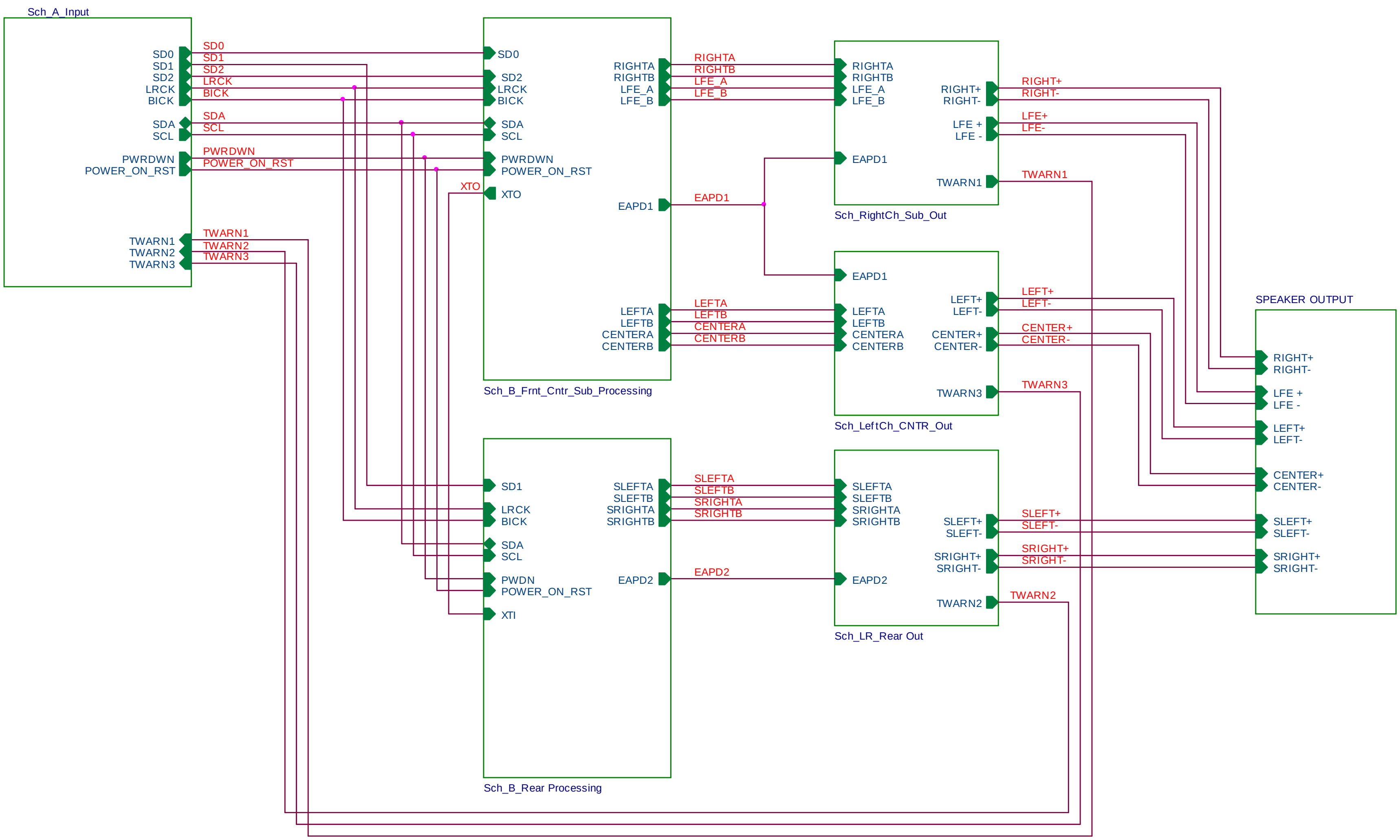

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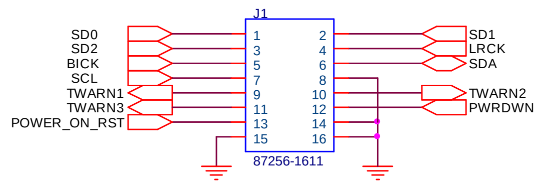
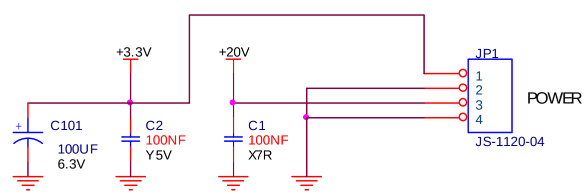
Size B	Document Number 150-0000-001	Rev A
Date: Sunday, March 03, 2002	Sheet 1 of 8	

INPUT CONNECTOR





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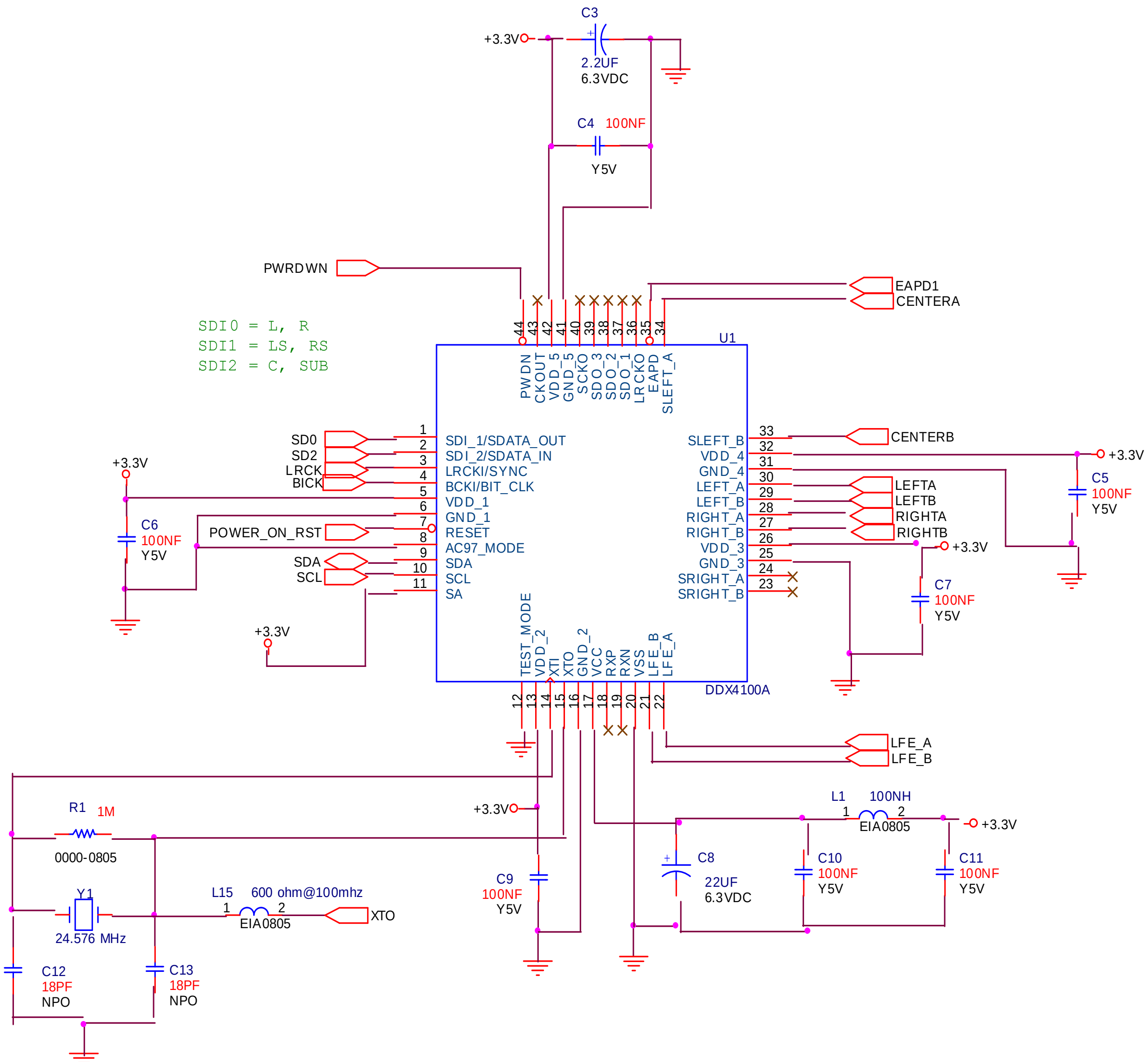
Size A	Document Number 150-0000-001					Rev A
Date:	Thursday , February 14, 2002	Sheet	2	of	8	



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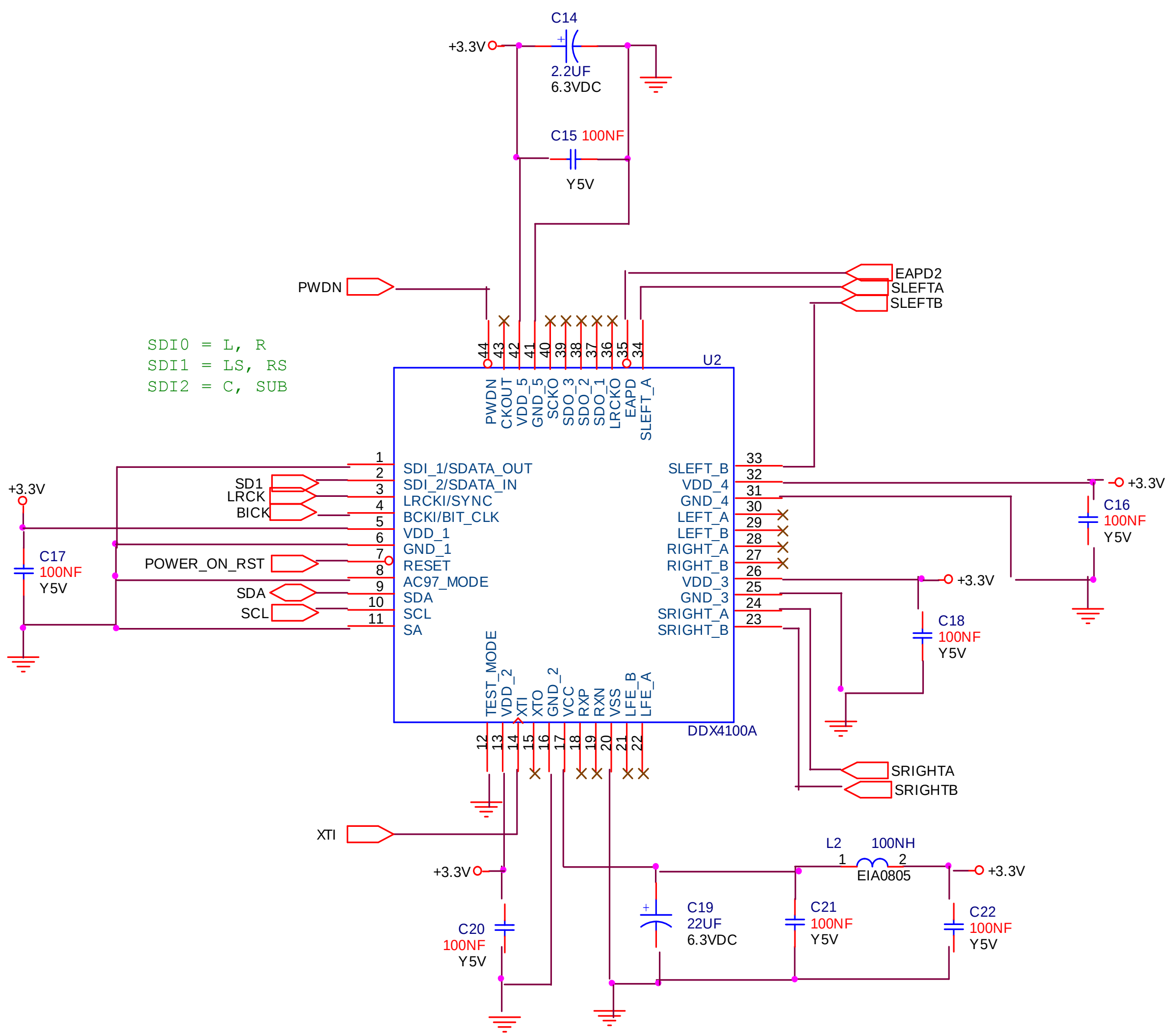
Size B	Document Number 150-0000-001	Rev A
Date: Friday, February 15, 2008	Sheet 3 of 8	



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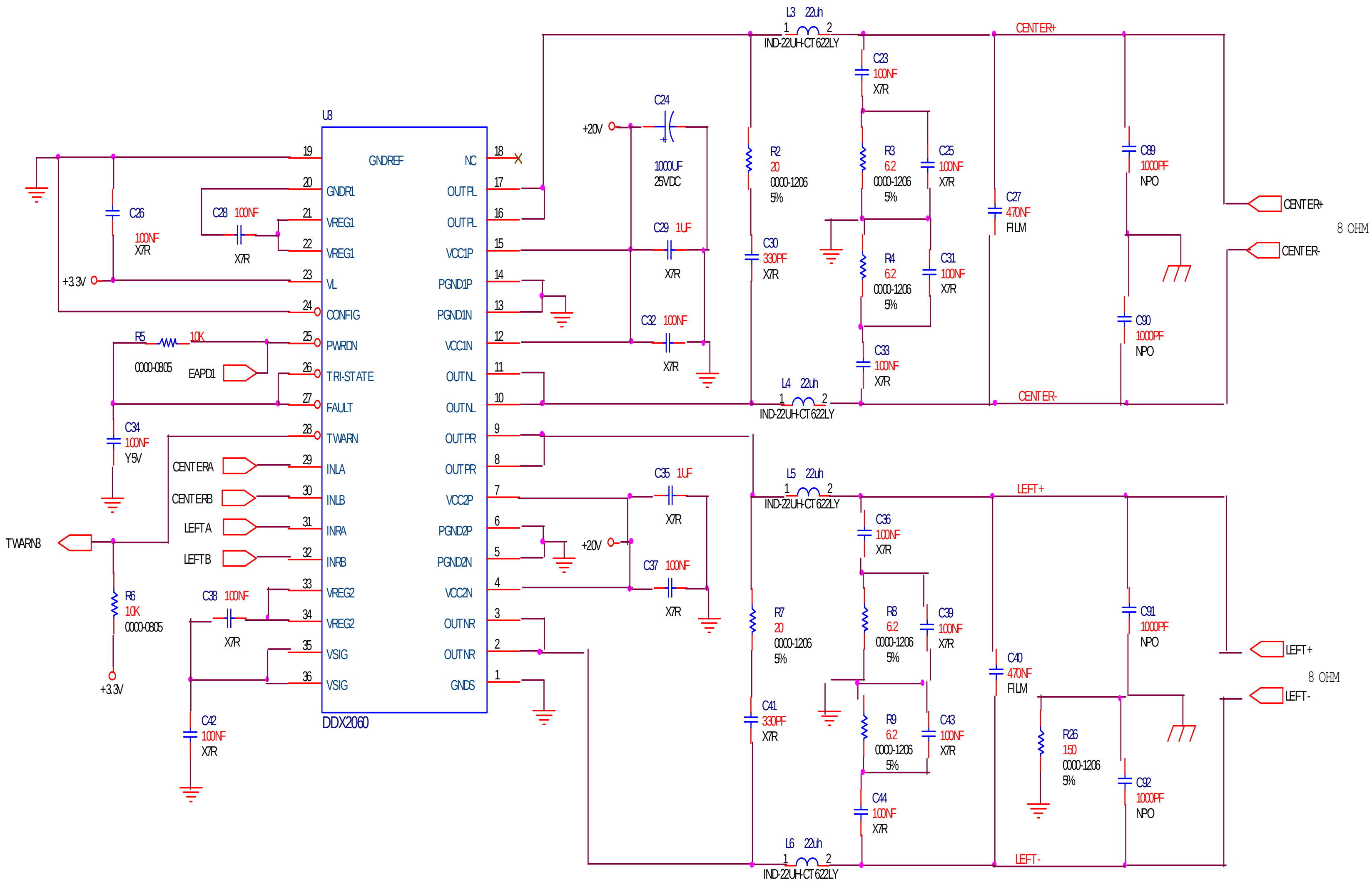
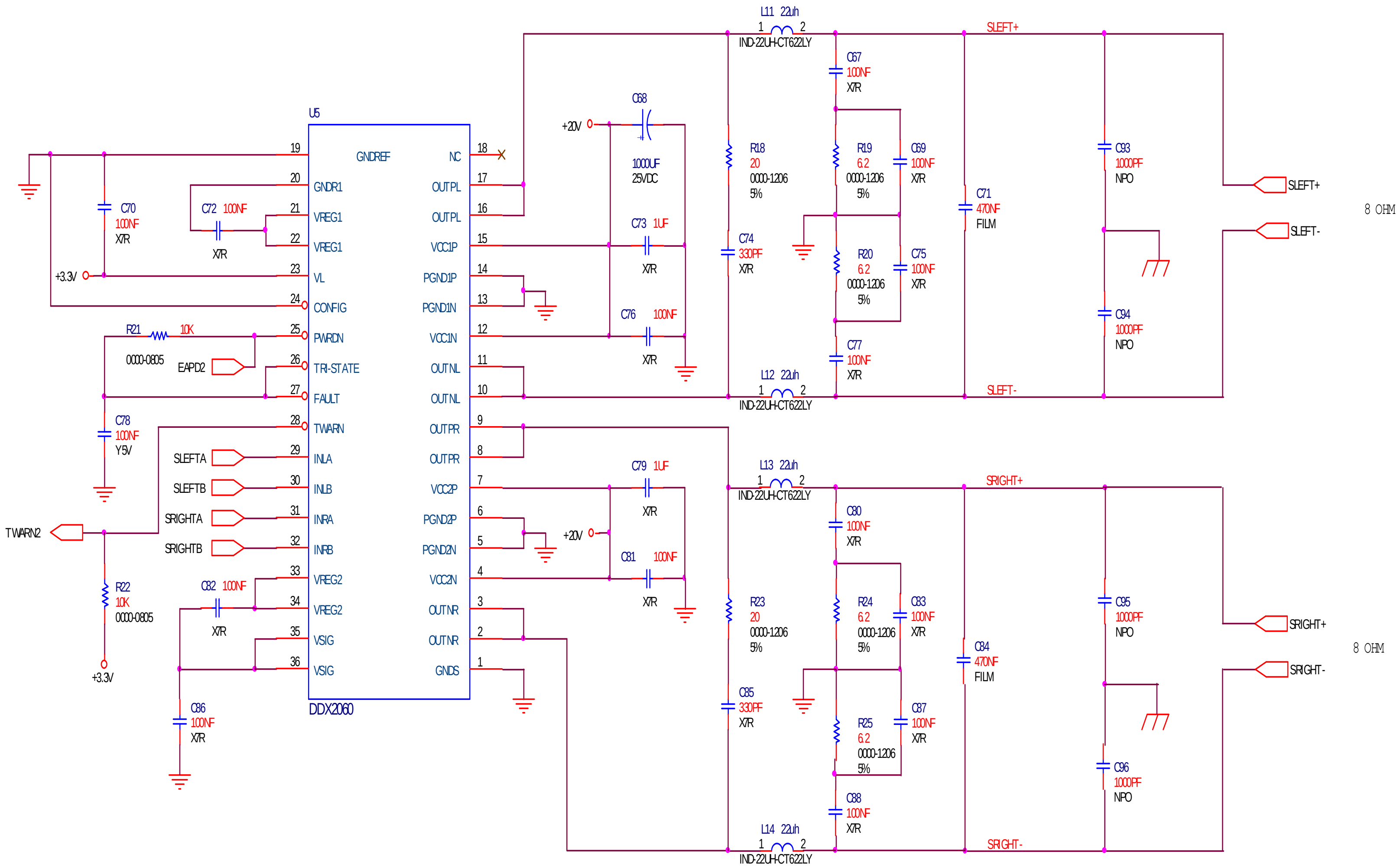
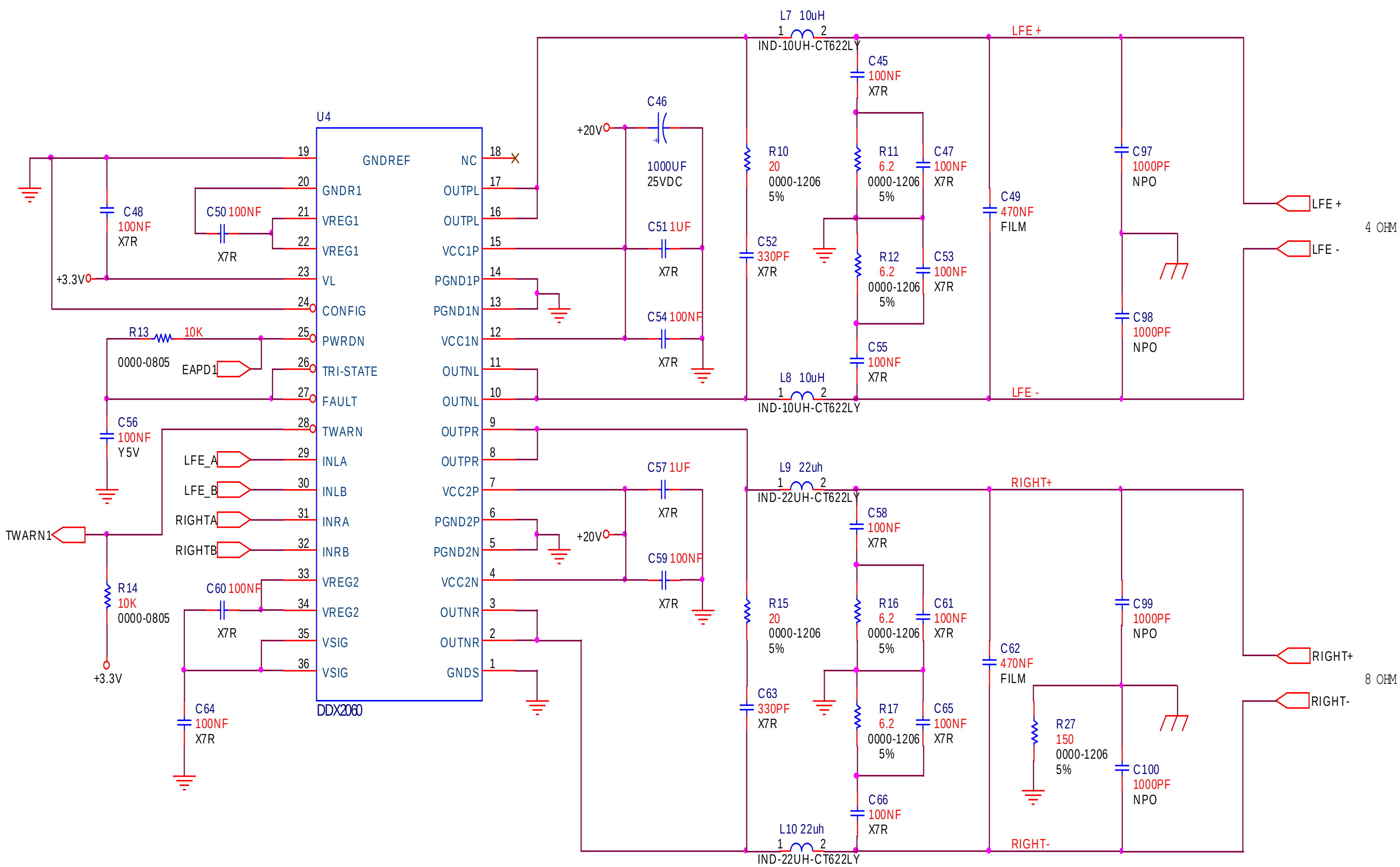
Size B	Document Number 150-0000-001 — Rev A
Date:	Thursday, February 14, 2002 — Sheet 4 of 8



Title: 5.1 CHANNEL SCHEMATIC CENTER, LF CHANNELS AMPLIFIER		
Size: B	Document Number: 150-0000-001	Rev: A
Date: Monday, February 18, 2002	Sheet 5 of 8	



Title	5.1 CHANNEL SCHEMATIC REAR CHANNEL AMPLIFIERS		
Size B	Document Number 150-0000-001	Rev A	
Date:	Thursday, February 14, 2002	Sheet 6	of 8



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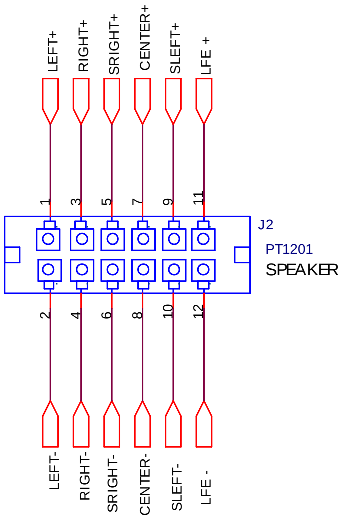
Size B	Document Number 150-0000-001	Rev A
Date: Monday, February 18, 2002	Sheet 7 of 8	



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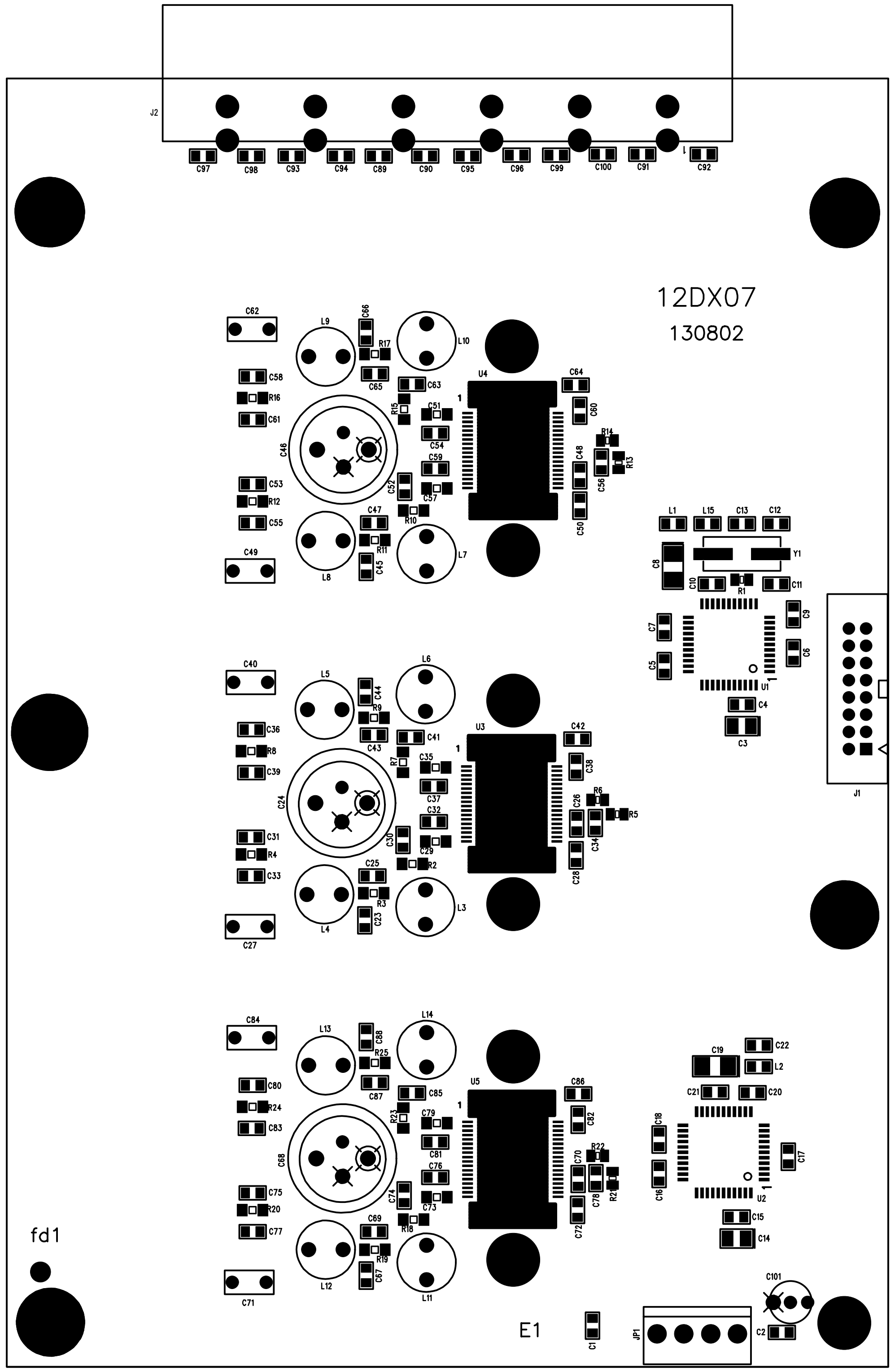
Size A	Document Number 150-0000-001	Rev A
Date:	Friday, February 15, 2002	Sheet 8 of 8



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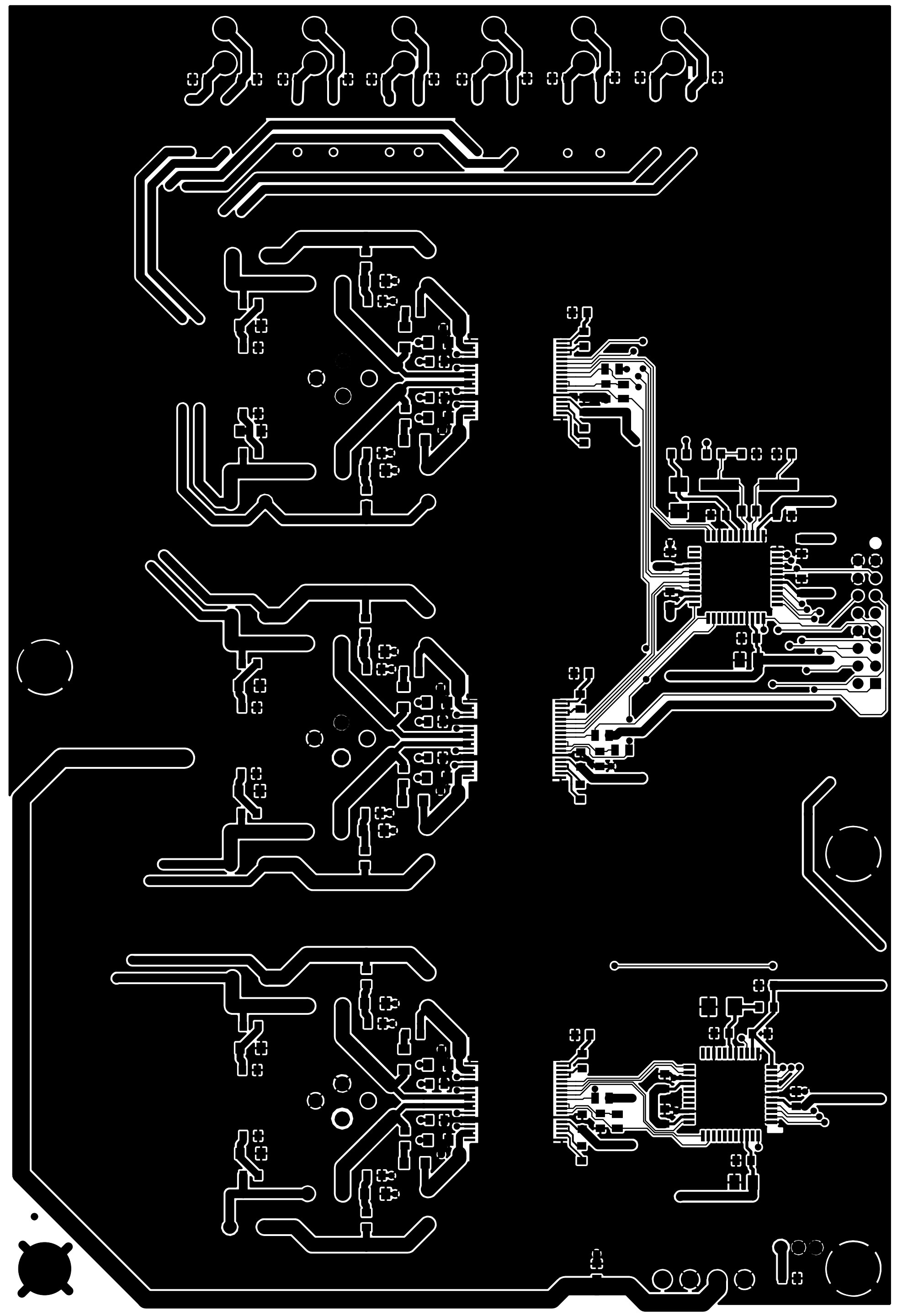
SOLDERMASK TOP



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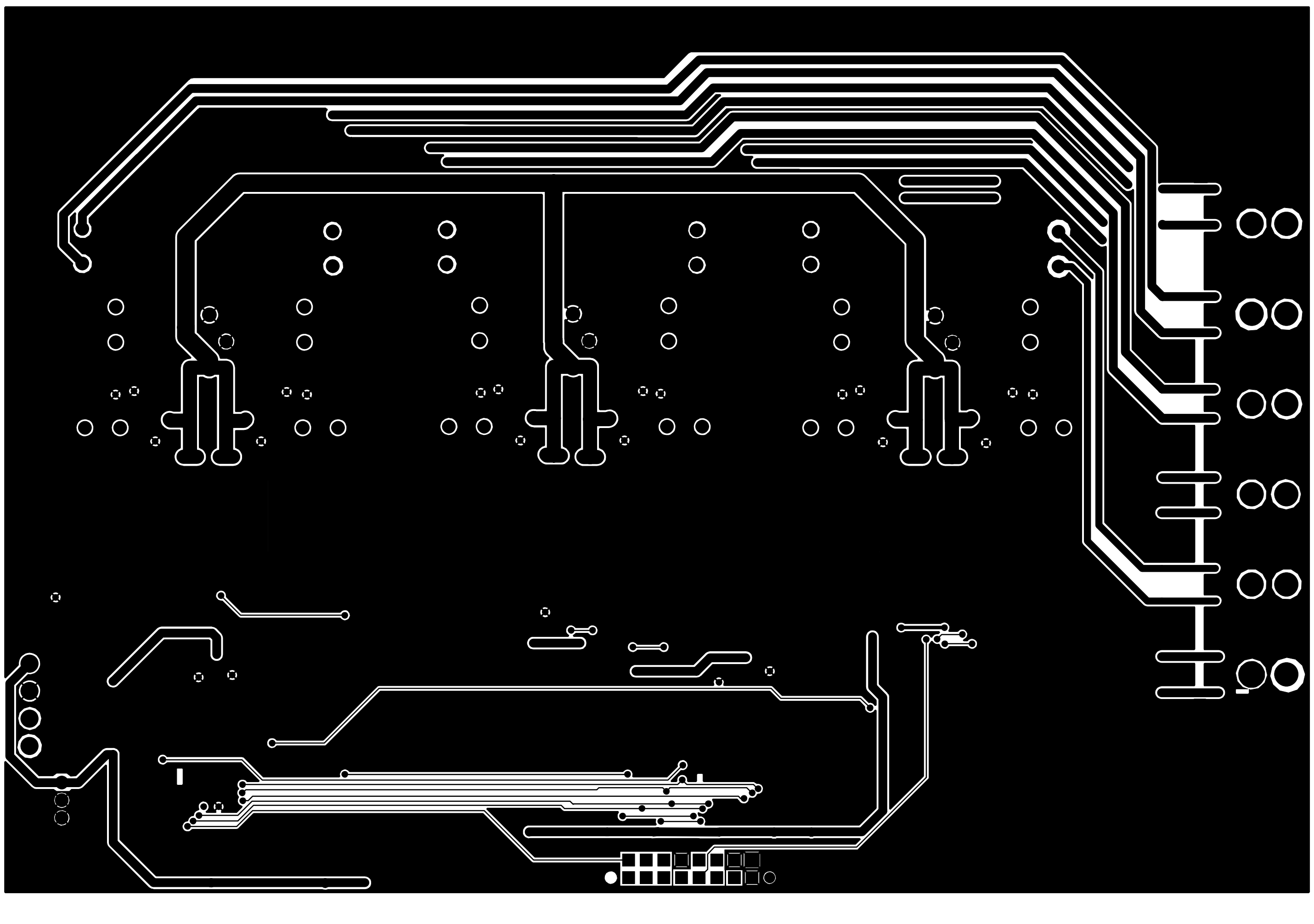

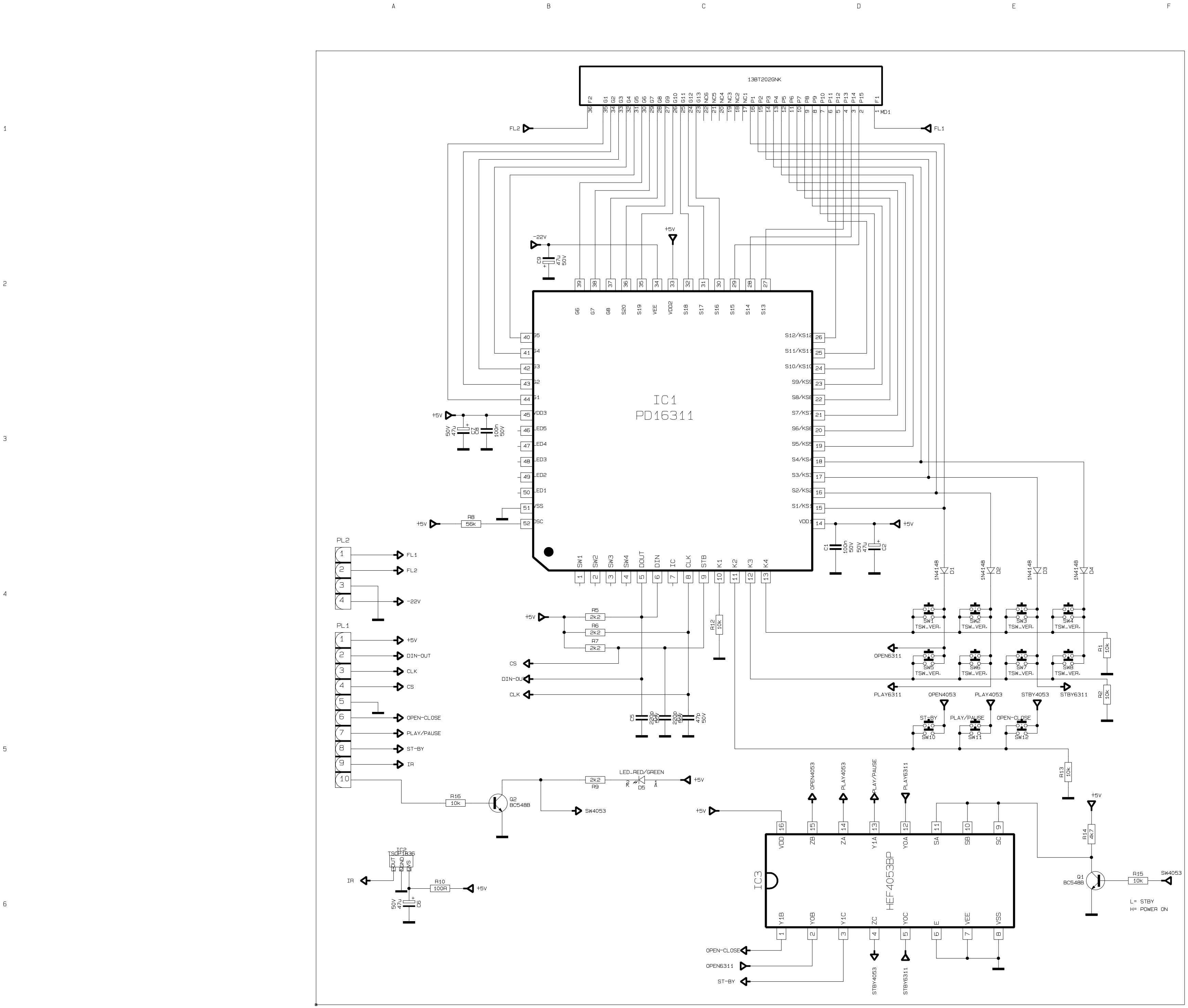

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+5V
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PD16311
VDD1
VDD2
VDD3
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VSS
OSC
DOUT
DIN
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STB
SW1
SW2
SW3
SW4
K1
K2
K3
K4
LED1
LED2
LED3
LED4
LED5
S1/KS1
S2/KS2
S3/KS3
S4/KS4
S5/KS5
S6/KS6
S7/KS7
S8/KS8
S9/KS9
S10/KS10
S11/KS11
S12/KS12
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PL2
DIN-OUT
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OPEN-CLOSE
PLAY/PAUSE
ST-BY
IR
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R6 2k2
R7 2k2
R8 56k
R9 2k2
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R12 10k
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Q2 BC548B
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Y0B
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SB
SC
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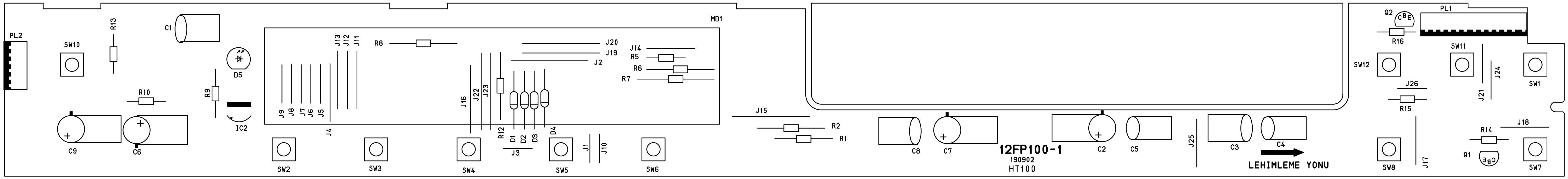
H= POWER ON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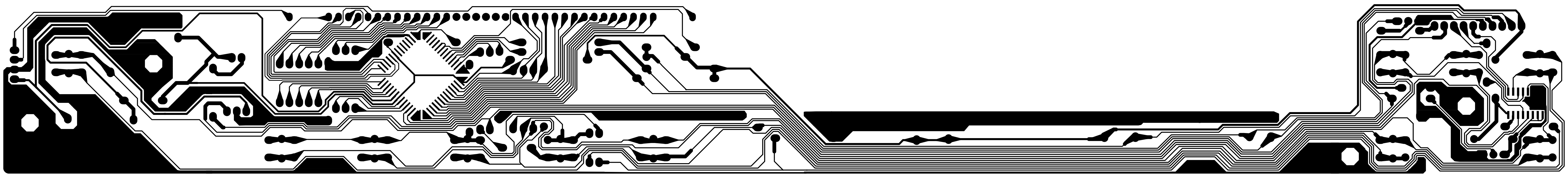

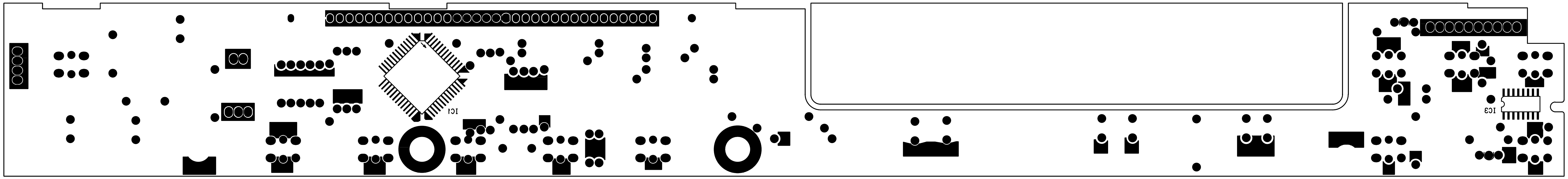
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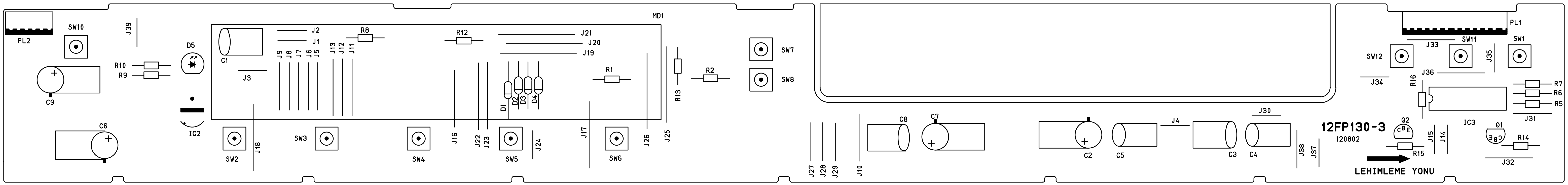

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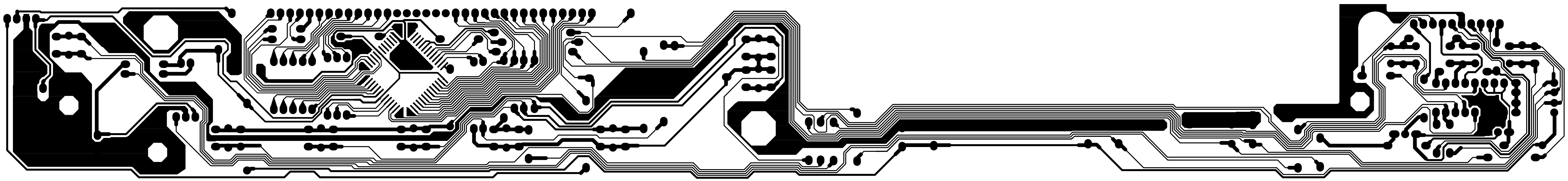

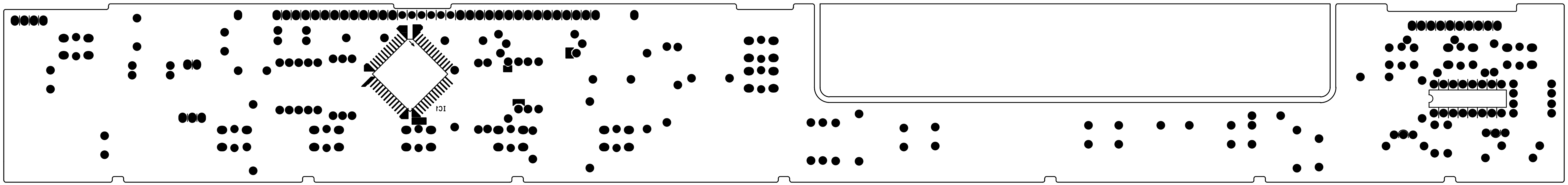

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