HITACHI

SM0154

HTD-K185UK

SERVICE MANUAL
MANUEL D'ENTRETIEN
WARTUNGSHANDBUCH

CAUTION:

Before servicing this chassis, it is important that the service technician read the “Safety Precautions” and “Product Safety Notices” in this service manual.

ATTENTION:

Avant d’effectuer l’entretien du châassis, le technicien doit lire les «Précautions de sécurité» et les «Notices de sécurité du produit» présentés dans le présent manuel.

VORSICHT:

Vor Öffnen des Gehäuses hat der Service-Ingenieur die „Sicherheitshinweise“ und „Hinweise zur Produktsicherheit“ in diesem Wartungshandbuch zu lesen.

Data contained within this Service manual is subject to alteration for improvement.

Les données fournies dans le présent manuel d’entretien peuvent faire l’objet de modifications en vue de perfectionner le produit.

Die in diesem Wartungshandbuch enthaltenen Spezifikationen können sich zwecks Verbesserungen ändern.

SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

DVD AV Receiver and Digital Terrestrial TV Receiver
October 2004

A) HARDWARE

1. GENERAL DESCRIPTION

1.1 MT1379

The MT1379 Progressive Scan DVD-Player Combo Chip is a single-chip MPEG video decoding chip that integrates audio/video stream data processing, TV encoder, four video DACs with Macrovision, copy protection, DVD system navigation, system control and housekeeping functions.

The features of this chip can be listed as follows;

General Features:

*Progressive scan DVD-player combo chip

*Integrated NTSC/PAL encoder,

*Built-in progressive video output

*DVD-Video, VCD 1.1, 2.0, and SVCD,

*Unified track buffer and A/V decoding buffer,

*Direct interface of 32-bit SDRAM,

*Servo controller and data channel processing.

Video Related Features:

*Macrovision 7.1 for NTSC/PAL interlaced video,

*Simultaneous composite video and S-video outputs, or composite and YUV outputs, or composite and RGB outputs.

*8-bit CCIR 601 YUV 4:2:2 output.

* Decodes MPEG video and MPEG2 main profile at main level.

* Maximum input bit rate of 15Mbits/sec.

Audio Related Features:

*Dolby Digital (AC-3) and Dolby Pro Logic

*Dolby Digital S/PDIF digital audio output

*High-Definition Compatible Digital. (HDCD) decoding

*Dolby Digital Class A and HDCD certified

*SRS True Surround

*CD-DA

*MP3

1.2 Memory

SDRAM Memory Interface

The MT1379 provides a glueless 16-bit interface to DRAM memory devices used as OSD, MPEG stream and video buffer memory for a DVD player. The maximum amount of memory support is 16 MB of Synchronous DRAM (SDRAM). The memory interface is configurable in depth to support 128-Mb addressing. The memory interface controls access to both external SDRAM memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers.

1.3 Drive Interfaces

The MT1379 supports the DV34 interface, and other RF and servo interfaces used by many types of DVD loaders. These interfaces meet the specifications of many DVD loader manufacturers.

1.4 Front Panel

The front panel is based around a Futaba VFD and a common NEC front panel controller chip, (uPD16311). The MT1379 controls the uPD16311 using several control signals, (clock, data, chip select). The infrared remote control signal is passed directly to the MT1379 for decoding.

1.5 Rear Panel

A typical rear panel is included in the reference design. This rear panel supports:

- Six channel or two channel audio outputs,
- Optical and coax SPDIF outputs,
- Composite, S-Video, and SCART outputs.

The six-video signals used to provide CVBS, S-Video, and RGB are generated by the MT1379's internal video DAC, The video signals are buffered by external circuitry.

Six channel audio output by the MT1379 in the form of three I2S (or similar) data streams. The S/PDIF serial stream is also generated by the MT1379 output by the rear panel. The six channel audio DACs (AK4356, PCM1606) are used for six channel audio output with MT1379, and similarly AK4382A, CS4392 Audio DACs are used for two channel audio output with MT1379.

12-pin DDX board output jack gives out the amplified audio. Digital Audio is processed in the DDX-8228 IC and then amplified in the DDX-2050 Power Amplifier ICs.

2. SYSTEM BLOCK DIAGRAM AND MT1379 PIN DECRIPTION

2.1 MT1379 Pin Description

Pin Number	Symbol	Type	Description
1	IREF	Analog Input	Current reference input. It generates reference current for data PLL. Connect an external 100K resistor to this pin and PLLVSS.
2	PLLVSS	Ground	Ground pin for data PLL and related analog circuitry
3	LPIOP	Analog Output	Positive output of the low pass filter
4	LPION	Analog Output	Negative output of the low pass filter
5	LPFON	Analog output	Negative output of loop filter amplifier
6	LPFIP	Analog Input	Positive input of loop filter amplifier
7	LPFIN	Analog Input	Negative input of loop filter amplifier
8	LPFOP	Analog Output	Positive output of loop filter amplifier
9	JITFO	Analog Output	RF jitter meter output
10	JITFN	Analog Input	Negative input of the operation amplifier for RF jigger meter
11	PLLVDD3	Power	3.3V power pin for data PLL and related analog circuitry
12	FOO	Analog Output	Focus servo output. PDM output of focus servo compensator
13	TRO	Analog Output	Tracking servo output. PDM output of tracking servo compensator
14	TROPENPWM	Analog Output	Tray open output, controlled by microcontroller. This is PWM output for TRWMEN27hRW2=1 or is digital output for TRWMEN27hRW2=0
15	PWMOUT1	Analog Output	The 1st general PWM output
16	PWMOUT2	Analog Output	The 2nd general PWM output
17	DVDD2	Power	2.5V power pin for internal fully digital circuitry
18	DMO	Analog Output	Disk motor control output. PWM output
19	FMO	Analog Output	Feed motor control. PWM output
20	DVSS	Ground	Ground pin for internal fully digital circuitry
21	FG	Input ^1	Motor Hall sensor input
22	HIGHAO	Inout 2-16 MA, SR PU	Microcontroller address 8
23	HIGHA1	Inout 2-16 MA, SR PU	Microcontroller address 9
24	HIGHA2	Inout 2-1 6MA, SR PU	Microcontroller address 10
25	HIGHA3	Inout 2-16MA, SR PU	Microcontroller address 11
26	HIGHA4	Inout 2-16MA, SR PU	Microcontroller address 12
27	HIGHA5	Inout 2-16MA, SR PU	Microcontroller address 13
28	DVSS	Ground	Ground pin for internal digital circuitry
29	HIGHA6	Inout 2-16MA, SR PU	Microcontroller address 14
30	HIGHA7	Inout 2-16MA, SR PU	Microcontroller address 15

31	AD7	Inout 2-16MA, SR	Microcontroller address/data 7
32	AD6	Inout 2-16MA, SR	Microcontroller address/data 6
33	ADS	Inout 2-16MA, SR	Microcontroller address/data 5
34	AD4	Inout 2-16MA, SR	Microcontroller address/data 4
35	DVDD3	Power	3.3V power pin for internal digital circuitry
36	ADS	Inout 2-16MA, SR	Microcontroller address/data 3
37	AD2	Inout 2-16MA, SR	Microcontroller address/data 2
38	AD1	Inout 2-16MA, SR	Microcontroller address/data 1
39	ADO	Inout 2-16MA, SR	Microcontroller address/data 0
40	IOAO	Inout 2-16MA, SR PU	Microcontroller address 0 / IO
41	IOA1	Inout 2-16MA, SR PU	Microcontroller address 1 / IO
42	DVDD2	Power	2.5V power pin for internal digital circuitry
43	IOA2	Inout 2-16MA, SR PU	Microcontroller address 2 / IO
44		Inout 2-16 MA, SR PU	Microcontroller address 3 / IO
45	IOA4	Inout 2-16MA, SR PU	Microcontroller address 4 / IO
46	IOA5	Inout 2-16MA, SR PU	Microcontroller address 5 / IO
47	IOA6	Inout 2-16MA, SR PU	Microcontroller address 6 / IO
48	IOA7	Inout 2-16MA, SR PU	Microcontroller address 7 / IO
49	A16	Output 2-16MA, SR	Flash address 16
50	A17	Output 2-16MA, SR	Flash address 17
51	IOA18	Inout 2-16MA, SR SMT	Flash address 18 /IO
52	IOA19	Inout 2-16MA, SR SMT	Flash address 19 /IO
53	IOA20	Inout 2-16MA, SR SMT	Flash address 20 / IO OR Video in Data PortB 0
54	APLLVSS	Ground	Ground pin for audio clock circuitry

55	APLLVDD3	Power	3.3V Power pin for audio clock circuitry
56	ALE	Inout 2-16MA, SR PU, SMT	Microcontroller address latch enable
57	IOOE#	Inout 2-16MA, SR SMT	Flash output enable, active low / IO
58	IOWR#	Inout 2-16MA, SR SMT	Flash write enable, active low / IO
59	IOCS#	Inout 2-16MA, SR PU, SMT	Flash chip select, active low / IO
60	DVSS	Ground	Ground pin for internal digital circuitry
61	UP1_2	Inout 4MA, SR PU, SMT	Microcontroller port 1-2
62	UP1_3	Inout 4MA, SR PU, SMT	Microcontroller port 1-3
63	UP1_4	Inout 4MA, SR PU, SMT	Microcontroller port 1-4
64	UP1_5	Inout 4MA, SR PU, SMT	Microcontroller port 1-5
65	UP1_6	Inout 4MA, SR PU, SMT	Microcontroller port 1-6
66	DVDD3	Power	3.3V power pin for internal digital circuitry
67	UP1_7	Inout 4MA, SR PU, SMT	Microcontroller port 1-7
68	UP3_0	Inout 4MA, SR PU, SMT	Microcontroller port 3-0
69	UP3_1	Inout 4MA, SR PU, SMT	Microcontroller port 3-1
70	INTO#	Inout 2-16MA, SR PU, SMT	Microcontroller interrupt 0, active low
71	IR	Input SMT	IR control signal input
72	DVDD2	Power	2.5V power pin for internal digital circuitry
73	UPS 4	Inout	Microcontroller port 3-4
74	UPS 5	Inout	Microcontroller port 3-5
75	UWR#	Inout 2-16MA, SR PU, SMT	Microcontroller write strobe, active low
76	URD#	Inout 2-16MA, SR PU, SMT	Microcontroller read strobe, active low
77	DVSS	Ground	Ground pin for internal digital circuitry
78	RD7	Inout	DRAM data 7
79	RD6	Inout	DRAM data 6
80	RD5	Inout	DRAM data 5
81	RD4	Inout	DRAM data 4
82	DVDD2	Power	2.5V power pin for internal digital circuitry

83	RD3	Inout	DRAM data 3
84	RD2	Inout	DRAM data 2
85	RD1	Inout	DRAM data 1
86	RDO	Inout	DRAM data 0
87	RWE#	Output 2-16MA, SR	DRAM Write enable, active low
88	CAS#	Output 2-16MA, SR	DRAM column address strobe, active low
89	RAS#	Output 2-16MA, SR	DRAM row address strobe, active low
90	RCS#	Output 2-16MA, SR	DRAM chip select, active low
91	BAO	Output 2-1 6MA, SR	DRAM bank address 0
92	DVSS	Ground	Ground pin for internal digital circuitry
93	RD15	Inout 2-16MA, SR PU/PD, SMT	DRAM data 15
94	RD14	Inout 2-16MA, SR PU/PD, SMT	DRAM data 14
95	RD13	Inout 2-16MA, SR PU/PD, SMT	DRAM data 13
96	RD12	Inout 2-16MA, SR PU/PD, SMT	DRAM data 12
97	DVDD3	Power	3.3V power pin for internal digital circuitry
98	RD11	Inout 2-16MA, SR PU/PD, SMT	DRAM data 11
99	RD10	Inout 2-16MA, SR PU/PD, SMT	DRAM data 10
100	RD9	Inout 2-16MA, SR PU/PD, SMT	DRAM data 9
101	RD8	Inout 2-16MA, SR PU/PD, SMT	DRAM data 8
102	DVSS	Ground	Ground pin for internal digital circuitry
103	CLK	Output 2-1 6MA, SR	DRAM clock
104	CLE	Output 2-16MA, SR	DRAM clock enable
105	RA11	Output 2-16MA, SR	DRAM address bit 1 1 or audio serial data 3 (channel 7/8)
106	RA9	Output 2-16MA, SR	DRAM address 9
107	RA8	Output 2-16MA, SR	DRAM address 8
108	DMVDD3	Power	3.3V Power pin for DRAM clock circuitry
109	DMVSS	Ground	Ground pin for DRAM clock circuitry
110	RA7	Output 2-16MA, SR	DRAM address 7
111	DVDD3	Power I %	3.3V power pin for internal digital circuitry

112	RA6	Output 2-16MA, SR	DRAM address 6
113	RA5	Output 2-16MA, SR	DRAM address 5
114	RA4	Output 2-16MA, SR	DRAM address 4
115	DVSS	Ground	Ground pin for internal digital circuitry
116	DQM1	Output 2-16MA, SR	Mask for DRAM input/output byte 1
117	DQMO	Output 2-16MA, SR	Mask for DRAM input/output byte 0
118	BA1	Output 2-16MA, SR	DRAM bank address 0
119	RA10	Output 2-16MA, SR	DRAM address lO
120	DVDD2	Power	2.5V power pin for internal digital circuitry
121	RAO	Output 2-16MA, SR	DRAM address 0
122	RA1	Output 2-16MA, SR	DRAM address 1
123	RA2	Output 2-16MA, SR	DRAM address 2
124	RA3	Output 2-16MA, SR	DRAM address 3
125	DVSS	Ground	Ground pin for internal digital circuitry
126	RD31	Inout 2-16MA, SR PU/PD, SMT	DRAM data 31
127	RD30	Inout 2-16MA, SR PU/PD, SMT	DRAM data 30
128	RD29	Inout 2-16MA, SR PU/PD, SMT	DRAM data 29
129	RD28	Inout 2-16MA, SR PU/PD, SMT	DRAM data 28
130	DVDD3	Power	3.3V power pin for internal digital circuitry
131	RD27	Inout 2-16MA, SR PU/PD, SMT	DRAM data 27
132	RD26	Inout 2-16MA, SR PU/PD, SMT	DRAM data 26
133	RD25	Inout 2-16MA, SR PU/PD, SMT	DRAM data 25
134	RD24	Inout 2-16MA, SR PU/PD, SMT	DRAM data 24
135	DVSS	Ground	Ground pin for internal digital circuitry
136	DQM3	Output 2-1 6MA, SR	Mask for DRAM input/output byte 3
137	DQM2	Output 2-1 6MA, SR	Mask for DRAM input/output byte 2

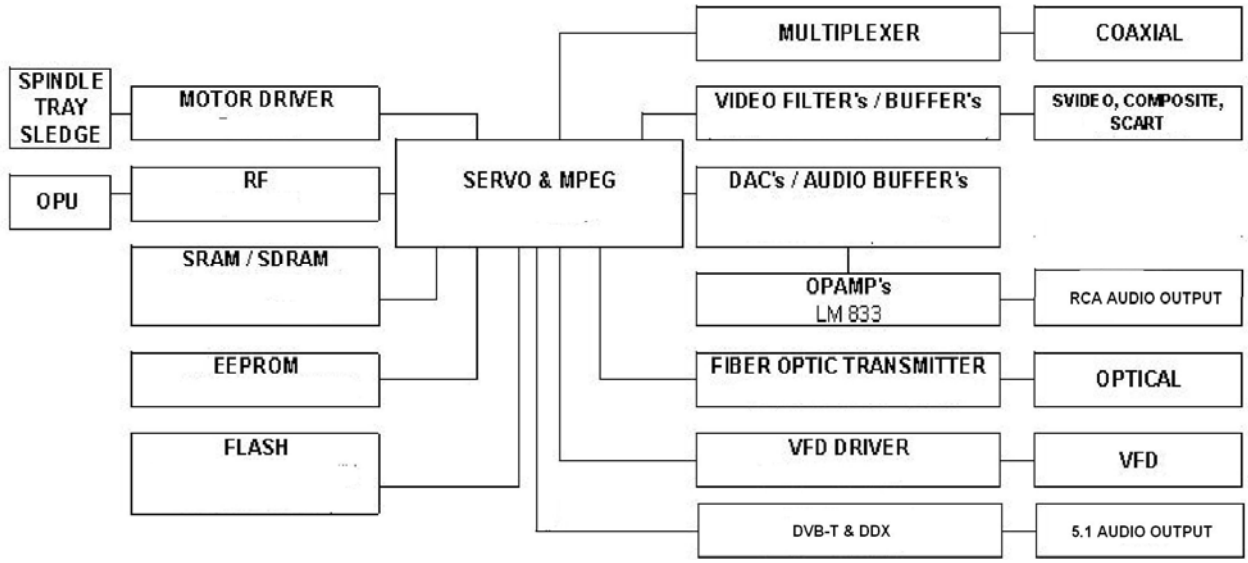
138	RD23	Inout 2-16MA, SR PU/PD, SMT	DRAM data 23 / Videoin Data PortA 7
139	RD22	Inout 2-16MA, SR PU/PD, SMT	DRAM data 22 / Videoin Data PortA 6
140	DVDD2	Power	2.5V power pin for internal digital circuitry
141	RD21	Inout 2-16MA, SR PU/PD, SMT	DRAM data 21 / Videoin Data PortA 5
142	RD20	Inout 2-16MA, SR PU/PD, SMT	DRAM data 20 / Videoin Data PortA 4
143	RD19	Inout 2-16MA, SR PU/PD, SMT	DRAM data 19 / Videoin Data PortA 3
144	RD18	Inout 2-16MA, SR PU/PD, SMT	DRAM data 18 / Videoin Data PortA 2
145	DVSS	Ground	Ground pin for internal digital circuitry
146	RD17	Inout 2-16MA, SR PU/PD, SMT	DRAM data 17 / Videoin Data PortA 1
147	RD16	Inout 2-16MA, SR PU/PD, SMT	DRAM data 16 / Videoin Data PortA 0
148	ABCK	Output 4MA	Audio bit clock
149	ALRCK	Inout 4MA, PD, SMT	(1) Audio left/right channel clock (2) Trap value in power-on reset : 1 : use external 373 0: use internal 373
150	DVDD3	Power	3.3V power pin for internal digital circuitry
151	ACLK	Inout 4MA	Audio DAC master clock (384/256 audio sample frequency)
152	MC DATA	Input	Microphone serial input
153	SPDIF	Output 2-16MA, SR : ON/OFF	SPDIF output
154	ASDATAO	Inout 4MA PDSMT	(1) Audio serial data 0 (left/right channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation
155	ASDATA1	Inout 4MA PD SMT	(1) Audio serial data 1 (surround left/surround right channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation
156	ASDATA2	Inout 4MA PD SMT	(1) Audio serial data 2 (center/left channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation
157	ASDATA3	Inout 4MA PD SMT	(1) Audio serial data 3 (surround left/surround right channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation OR Videoin Data PortB 1
158	ASDATA4	Inout 4MA PD SMT	(1) Audio serial data 4 (center/left channel) (2) Trap value in power-on reset : 1 : manufactory test mode 0 : normal operation OR Videoin Data PortB 2
159	DACVDDC	Power	3.3V power pin for VIDEO DAC circuitry
160	VREF	Analog input	Bandgap reference voltage
161	FS	Analog output	Full scale adjustment

162	YUVO/CIN	Output 4MA, SR	Video data output bit 0 / Compensation capacitor
163	DACVSSC	Ground	Ground pin for VIDEO DAC circuitry
164	YUV1/C	Output 4MA, SR	Video data output bit 1 / Analog chroma output
165	DACVDDB	Power	3.3V power pin for VIDEO DAC circuitry
166	YUV2/Y	Output 4MA, SR	Video data output bit 2 / Analog Y output
167	DACVSSB	Ground	Ground pin for VIDEO DAC circuitry
168	YUV3/CVBS	Output 4MA, SR	Video data output bit 3 / Analog composite output
169	DACVDDA	Power	3.3V power pin for VIDEO DAC circuitry
170	YUV4/G	Output 4MA, SR	Video data output bit 4 / Green or Y
171	DACVSSA	Ground	Ground pin for VIDEO DAC circuitry
172	YUV5/B	Output 4MA, SR	Video data output bit 5 / Blue or CB
173	YUV6/R	Output 4MA, SR	Video data output bit 6 / Red or CR
174	ICE	Input PD, SMT	Microcontroller ICE mode enable
175	BLANK#	Inout 4MA, SR SMT	Video blank area, active low / Videoin Field_601
176	VSYN	Inout 4MA, SR SMT	Vertical sync / Videoin Vsync_601
177	YUV7	Inout 4MA, SR SMT	Video data output bit 7 / Videoin Data PortB 3
178	DVSS	Ground	Ground pin for internal digital circuitry
179	HSYN	Inout I4MA, SR SMT	Horizontal sync / Videoin Hsync_601
180	SPMCLK	Input	Audio DAC master clock of SPDIF input / Videoin Data PortB 4
181	SPDATA	Input	Audio data of SPDIF input / Videoin Data PortB 5
182	DVDD2	Power	2.5V power pin for internal digital circuitry
183	SPLRCK	Input	Audio left/right channel clock of SPDIF input / Videoin Data PortB 6
184	SPBCK	Input	Audio bit clock of SPDIF input / Videoin Data PortB 7
185	DVDD3	Power	3.3V power pin for internal digital circuitry
186	XTALO	Output	Crystal output
187	XTALI	Input	Crystal input
188	PRST	Input PD, SMT	Power on reset input, active high
189	DVSS	Ground	Ground pin for internal digital circuitry
190	VFO13	Output	The 1st, 3rd header VFO pulse output
191	IDGATE	Output	Header detect signal output
192	DVDD3	Power	3.3V power pin for internal digital circuitry
193	UDGATE	Output	DVD_RAM recording data gate signal output
194	WOBSI	Input	Wobble signal input
195	SDATA	Output	RF serial data output
196	SDEN	Output	RF serial data latch enable
197	SLCK	Output	RF serial clock output
198	EDO	Input	Flag of defect data input status
199	ADCVSS	Ground	Ground pin for ADC circuitry

200	ADIN	Analog Input	General A/D input
201	RFSUBI	Analog Input	RF subtraction signal input terminal
202	TEZISLV	Analog Input	Tracking error zero crossing low pass input
203	TEI	Analog Input	Tracking error input
204	CSO	Analog Input	Central servo input
205	FEI	Analog Input	Focus error input
206	RFLEVEL	Analog Input	Sub beam add input or RFRP low pass input
207	RFRP DC	A Input	RF ripple detect input
208	RFRP AC	Analog Input	RF ripple detect input (through AC coupling)
209	HRFZC	Analog Input	High frequency RF ripple zero crossing
210	PWMVREF	A Input	A reference voltage input for PWM circuitry. A typical value of 4.0 v
211	PWM2VREF	A Input	A reference voltage input for PWM circuitry. A typical value of 2.0 v
212	ADCVDD3	Power	3.3V power pin for ADC circuitry
213	RFDTSLVP	Analog Output	Positive RF data slicer level output
214	RFDTSLVN	Analog Output	Negative RF data slicer level output
215	RFIN	Analog Input	Negative input of RF differential signal
216	RFIP	Analog Input	Positive input of RF differential signal

2.2 System Block Diagram

A sample system block diagram for AV1100 board design is shown in the following figure:



3. AUDIO OUTPUT

The MT1379 supports two-channel and six-channel analog audio output. In a system configuration with six analog outputs, the front left and right channels can be configured to provide the stereo (2 channel) outputs and Dolby Surround, or the left and right front channels for a 5.1 channel surround system.

The MT1379 also provides digital output in SPDIF format. The board supports both optical and coaxial SPDIF outputs,

4. AUDIO DACS

The MT1379 supports several variations of an PS type bus, varying the order of the data bits (leading or no leading zero bit, left or right alignment within frame, and MSB or

LSB first) is possible using the MT1379 internal configuration registers. The I2S format uses four stereo data lines and three clock lines. The PS data and clock lines can be connected directly to one or more audio DAC to generate analog audio output.

The two-channel DAC is a CS4392, The DACs support up to 192kHz sampling rate.

The outputs of the DACs are differential, not single ended so a buffering circuit is required. The buffer circuits use National LM833 op-amps to perform the low-pass filtering and the buffering,

5 VIDEO INTERFACE

5.1 Video Display Output

The video output section controls the transfer of video frames stored in memory to the internal TV encoder of the MT1379, The output section consists of a programmable CRT controller capable of operating either in Master or Slave mode.

The video output section features internal line buffers which allow the outgoing luminance and chrominance data to match the internal clock rates with external pixel clock rates, easily facilitating YUV 4:2:2 to YUV 4:2:0 component and sample conversion, A polyphase filter achieves arbitrary horizontal decimation and interpolation.

Video Bus

The video bus has 8 YUV data pins that transfer luminance and chrominance (YUV) pixels in CCIR601 pixel format (4:2:2), In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance,

Video Post-Processing

The MT1379 video post-processing circuitry provides support for the color conversion, scaling, and filtering functions through a combination of special hardware and software. Horizontal up-sampling and filtering is done with a programmable, 7-tap polyphase filter bank for accurate non-integer interpolations. Vertical scaling is achieved by repeating and dropping lines in accordance with the applicable scaling ratio.

Video Timing

The video bus can be clocked either by double pixel clock, and clock qualifier or by a single pixel clock. The double clock typically is used for TV displays, the single for computer displays.

6 FLASH MEMORY

The decoder board supports 70ns Flash memories. Currently 4 configurations are supported:

- FLASH_512K_8b
- FLASH_1024K_8b
- FLASH_512Kx2_8b
- FLASH_512Kx2_16b

The MT1379 permits both 3- and 16-bit common memory I/O accesses with a removable storage card via the host interface.

7 SERIAL EEPROM MEMORY

An I2G serial EEPROM is used to store user configuration (i,e, language preferences, speaker setup, etc.) and software configuration. Industry standard EEPROM range in size from 1kbit to 253kbit and share the same IC footprint and pinout. The default device is 2kbit, 256kx 8, SOIC8 SGS Thomson ST24C02M1 or equivalent.

8 AUDIO INTERFACE AUDIO SAMPLING RATE AND PLL COMPONENT CONFIGURATION

The MT1379 audio mode configuration is selectable, allowing it to interface directly with low-cost audio DACs and ADCs. The audio port provides a standard PS interface input and output and S/PDIF (IEC958) audio output. Stereo mode is in PS format while six channels Dolby Digital (5,1 channel) audio output can be channeled through the S/PDIF. The S/PDIF interface consists of a bi-phase mark encoder, which has low skew. The transmit I2S interface supports the 112, 128, 192, 256, 384, and 512 sampling frequency formats, where sampling frequency Fs is usually 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, or 192 kHz, The audio samples for the PS transmit interface can be 16, 18, 20, 24, and 32-bit samples.

For Linear PCM audio stream format, the MT1379 supports 48 kHz and 96 kHz. Dolby Digital audio only supports 48 kHz. The MT1379 incorporates a built-in programmable analog PLL in the device architecture in order to generate a master audio clock, The MCLK pin is for the audio DAC clock and can either be an output from or an input to the MT1379. Audio data out (TSD) and audio frame sync (TWS) are clocked out of the MT1379 based on the audio transmit bit clock (TBCK), Audio receive bit clock (RBCK) is used to clock in audio data in (RSD) and audio receive frame sync (RWS),

9 FRONT PANEL

9.1 VFD CONTROLLER

The VFD controller is a NEC uPD 16311. This controller is not a processor, but does include a simple state machine which scans the VFD and reads the front panel button matrix. The 16311 also includes RAM so it can store the current state of all the VFD icons and segments. Therefore, the 16311 need only be accessed when the VFD status changes and when the button status is read. The MT1379 can control this chip directly using PIO pins or can allow the front panel PIC to control the VFD,

10 CONNECTORS

10.1 Scart Connectors

Cable between VCR and TV (Scart)			
TV		**VCR**	
Audio Right Out	1	2	Audio Right In
Audio Right In	2	1	Audio Right Out
Audio Left Out	3	6	Audio Left In
Audio Left In	6	3	Audio Left Out
Audio Ground	4	4	Audio Ground
Red	15	15	Red
Red Ground	13	13	Red Ground
Green	11	11	Green
Green Ground	9	9	Green Ground
Blue	7	7	Blue
Blue Ground	5	5	Blue Ground
Status / 16:9	8	8	Status / 16:9
Reserved	10	10	Reserved
Reserved	12	12	Reserved
Fast Blanking Ground	14	14	Fast Blanking Ground
Fast Blanking	16	16	Fast Blanking
Video Out Ground	17	18	Video In Ground
Video In Ground	18	17	Video Out Ground
Video Out	19	20	Video In
Video In	20	19	Video Out
Ground	21	21	Ground

Some cheaper SCART cables use unshielded wires, which is just about acceptable for short cable lengths. For longer lengths, shielded co-ax cable become essential,

Scart Signals:

- Audio signals

0.5V RMS, <1K output impedance, >10K input impedance.

- Red, Green, Blue

O.7 Vpp ±2dB, 75R input and output impedance. Note that the Red connection (pin20) can alternatively carry the S-Video Chrominance signal, which is 0.3V.

- Composite Video / CSync

1 Vpp including sync, ±2dB, 75R input and output impedance. Bandwidth = 25Hz to 4.8MHz for normal TV Video de-emphasis to CCIR405.1 (625-line TV)

Fast Blanking

75R input and output impedance. This control voltage allows devices to over-ride the composite video input with RGB inputs, for example when inserting closed caption text. It is called fast because this can be done at the same speeds as other video signals, which is why it requires the same 75R impedances.

- 0 to 0.4V: TV is driven by the composite video input signal (pin 19). Left unconnected, it *s* pulled to 0V by its 75R termination.
- 1V to 3V: the TV is driven by the signals Red, Green, Blue and composite sync. The latter is sent to the TV on pin 19. This signal is useful when using a TV to display the RGB output of devices such as home computers with TV-compatible frame rates. Tying the signal to 5V via 1 DDR forms a potential divider with the 75R termination, holding the signal at around 2V. Alternatively, if a TTL level (0 to 5V) negative sync pulse is available, this will be high during the display periods, so this can drive the blanking signal via a suitable resistor.

Control Voltage

0 to 2V = TV, Normal.

5 to 8V = TV wide screen

9.5 to 12V = AV mode

11. CIRCUIT DESCRIPTION

11.1 POWER SUPPLY:

• Socket PL800 is the220VAC input.

• 3.15A fuse F1 is used to protect the device against short circuit.

•Voltage is rectified by using diode D805 and capacitor C815 (330uF) a DC voltage is produced. (310-320V DC).

•IC800 (MC44608) is a SMPS IC. The switching frequency of this IC is constant. Only the duty cycle determines the voltage on the secondary side of the transformer and the duty cycle depends on the feedback current injected into pin 3 (from the secondary side of the SMPS via the opto-coupler IC803)

•VI pin of IC800 transfers the voltage across C854 to VCC pin internally. This voltage is used during the start up process. As soon as the IC starts up, this property is disabled.

•IC804 TL431 is a constant current regulator. TL431 watches the 30V output of the transformer and supplies the required current to opto-coupler (IC803). The LED inside the IC803 transmits the value of the current from IC804 to phototransistor. Depending on the current gain of the phototransistor IC800 keeps the voltage on the 30V winding constant.

•MC34167 (IC807) is a power switching regulator and it is used to step down 8V to 5V. When the device enters stand by mode, transistor Q807 starts to conduct and pulls pin 5 (stby pin) of this IC to ground and this cuts off 5V and 3.3V output of this board.

11.2 FRONT PANEL:

•The VFD controller is a NEC uPD 16311 (IC1). This controller is not a processor, but does include a simple state machine which scans the VFD and reads the front panel button matrix.

•The pressed key information is send to MT1379 from pin 5 and pin 6 of IC1.

•IR remote control receiver module IC2 (TSOP1836) sends the commands from the remote control directly to IC300 MT1379.

•The 16311 also includes RAM so it can store the current state of all the VFD icons and segments. Therefore, the 16311 need only be accessed when the VFD status changes and when the button status is read. The MT1379 can control this chip directly using PIO pins. It sends the commands to IC1 UPD16311 via socket PL301 (on the mainboard).

•Socket PL2 carries the VFD filament voltages (FL1, FL2) and -22 Volts. These three voltages are sent from the power board (socket PL806).

11.3 I/Os and Back Panel:

•There are

- 2 SCART (input and output) connectors,
- 2 RCA audio jacks for audio output,
- 3 RCA jacks for av input.
- 1 coaxial digital audio output,

- 1 laser digital audio output
- Also there are antenna inputs for AM/FM tuner, antenna in and tv out for dvb-t receiver.

•TOTX176 is used for laser output.

•For coaxial audio output SPDIF is used.

•SCART pin 8 controls 16:9 and 4:3 mode using Q617 and Q619.

•When the pin 8 output of the scart becomes 12 Volts, 4:3 mode is selected and 16:9 mode is selected when this output becomes 5.

• S-video output is active only in dvd mode.

• RGB outputs of output scart is active only in DVD and Scart Mode. It is not used in RGB mode. Becouse of this in AV mode, the voltage level at pin 16 of the output scart is below 1 V.

11.4 DVB-T & DDX Board (Class-D Amplifier):

11.4.1 DDX Part

- Chipset: lxDDX-8228 + 2x DDX-2050
- Architecture : Full-Bridge x 2, Half-Bridge x4
- Power Supply : + 20V unipolar supply @ 6A max., + 3.3V @ 0.1A typ.
- Audio Input Interface: Serial I2S
- Control Interface: I2C
- Power Interface: + 20V @ 6A Max., + 3.3V@ 0.1A Typ
- Output Interface: Speaker Level
- Speakers: 8 Ohm Satellites + 4 Ohm Subwoofer
- Output Power: 5 x 15 W +25 W
- DDX Audio proccess IC is U2 (DDX-8228).
- U2 IC on the DDX board has digital audio input with I2S bus.
- I2S signals are SDI12, SDI34, SDI56 serial data lines U2 pin9, pin8, pin7 LRCKI Left-Right clock signal U2 pin 10, BICKI serial clock signal U2 pin 11.
- For mute function U2 IC uses EAPD (pin51, External Amplifier Powerdown) signal. This signal comes to the power output ICs U3 and U4 (DDX-2050 ICs Pin25) as power down signal.

11.4.2 DVB-T Part

The IF output of the tuner (TU401) is converted to Transport Stream signals (multiplexed video, audio and data information) after some filtering, and COFDM (coded orthogonal demodulation).

The digital demodulator (IC401) output is transported to the STI5518 MPEG–2 decoder (IC100) with cm_clk (clock signal to decoder), cm_valid (indicates valid data bits of transport stream (TS) and cm_sync (indicates start of a TS).

TU401 is controlled by demodulator (IC401) via sclk and sdata. Demodulator is controlled via I^2C by STI5518 decoder.

The CPU (ST20) inside STI5518 controls all processes. Demultiplexer of the CPU provides the transmission of the desired channel's information from TS (Transport Stream) to MPEG Decoder section.

The program that runs on STI5518 is in Flash memory (IC302). 64Mbits SDRAMs (IC300 and IC301) are used for data memory of this program. IC300 is SMI SDRAM and decoded data is stored here. It has a clock input of 121.5Mhz. Software is mostly run over IC301 EMI SDRAM. Some program and status information is stored in EEPROM (IC304).

The CPU (ST20) inside STI5518 uses 32- bit data and 22- bit address buses for access to flash, DRAM and MPEG decoder. It uses RAS, CAS etc. (read, write, enable) signals to activate related IC while accessing them.

The main clock (which is needed by STI 5518), is generated at power on mode and at STBY by 27MHz crystal (X112) and IC102 (74HCU04). The output of PWM outputs of STI 5518 is filtered to have a DC level via R128 and C133. At the output of IC103, the 27MHz clock can be adjusted according to capacity of pins of 27MHz crystal to ground. This capacity is related with DC value on D100 and D101 (BB133) at pins of crystal. This operation maintains synchronization between audio-video that are coming from MPEG transport stream and PCR clock.

MPEG decoder in STI5518, is responsible for decoding of MPEG video and audio signals. The video, which is compressed using MPEG2 and audio, which is compressed using MPEG1 Layer 1-2, are processed here. After decoding, CCIR 601 formatted 8-bit video and PCM formatted audio, are generated by mpeg decoder.

B) SOFTWARE

1. AV RECEIVER

1.1 UNIVERSAL SERVICE PASSWORD

Universal Password for Parental level is 1369

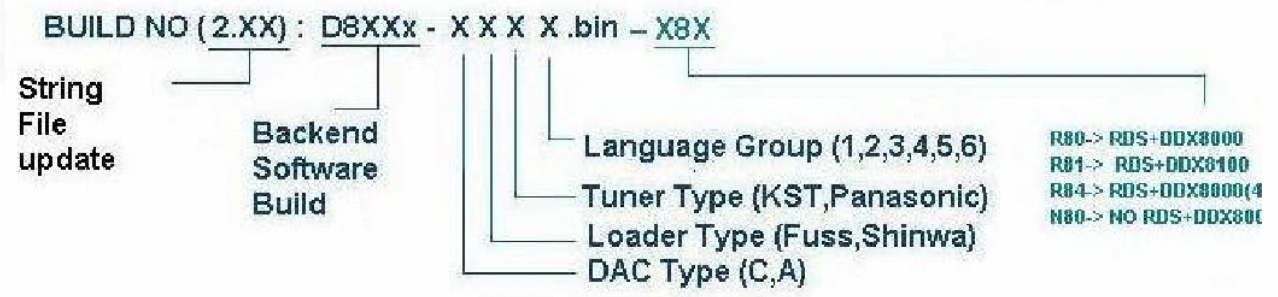
1.2 VERSION PAGE (Hidden Menu)

To see Version Page:

- Press DISPLAY button from remote for Setup Menu
- Press "1"- "3 "- "5 "- "7 " at Setup Menu
- Setup Menu screen refresh and "Version" selection can be seen under "Preferences Setup"
- Select "Version" for version Page
- BUILD NO contains version and Hardware options other information for development only.

Details of Build No as follows:

Tracking Build number and Hardware options from Version Page:



Language Groups for AV1XXX

	Group 1	Group 2	Group 3	Group 4	Group 5	Group 6
1	English	English	English	English	English	English
2	French	Italian	Danish	Czech	Slovenian	German
3	German	Portugues	Swedish	Polish	Romanian	Dutch
4	Dutch	Spanish	Finnish	Hungarian	Crotarian	Turkish

Press "DISPLAY" button on remote control to exit menu.

1.3 VFD Full Segment Test Mode

During Pressing STOP button on Front Panel if you press Standby button all segments of VFD are highlighted.

1.4 REGION MANAGEMENT

At Version page by using arrow keys Region can be changed.

1.5 UPDATE FILE NAME

Proper Update file name can be learned from Version Page as follows:

First Characters of DAC, LOADER, TUNER and LANGUAGE group gives proper update file name.

Example: CFKI.bin

1.6 CD UPDATE PROCEDURE:

1) Player can be updated automatically with Update CD which contains proper file. Check hidden menu for update file name.

2) Burn CD* within proper update file

3) There should be no Volume Name for CD

Open Tray and place update CD

4) You can see "Upgrade File Detected. Press Play to start" OSD message

5) Press Play button to start upgrade

6) You can see "File copying" OSD message for a few second

7) Tray is open automatically

8) No need for CD in tray; Take it from tray.

9) During upgrade procedure "CD upgrade start, Please wait.." indicator at OSD, and "UPG" indicator at VFD

10) Upgrade procedure takes about a few minutes, please wait if tray is open.

11) When CD update is finished tray is closed, screen is refreshed, update is finished.

NOTE: * For "NERO Burning Rom" program

ideal configuration;

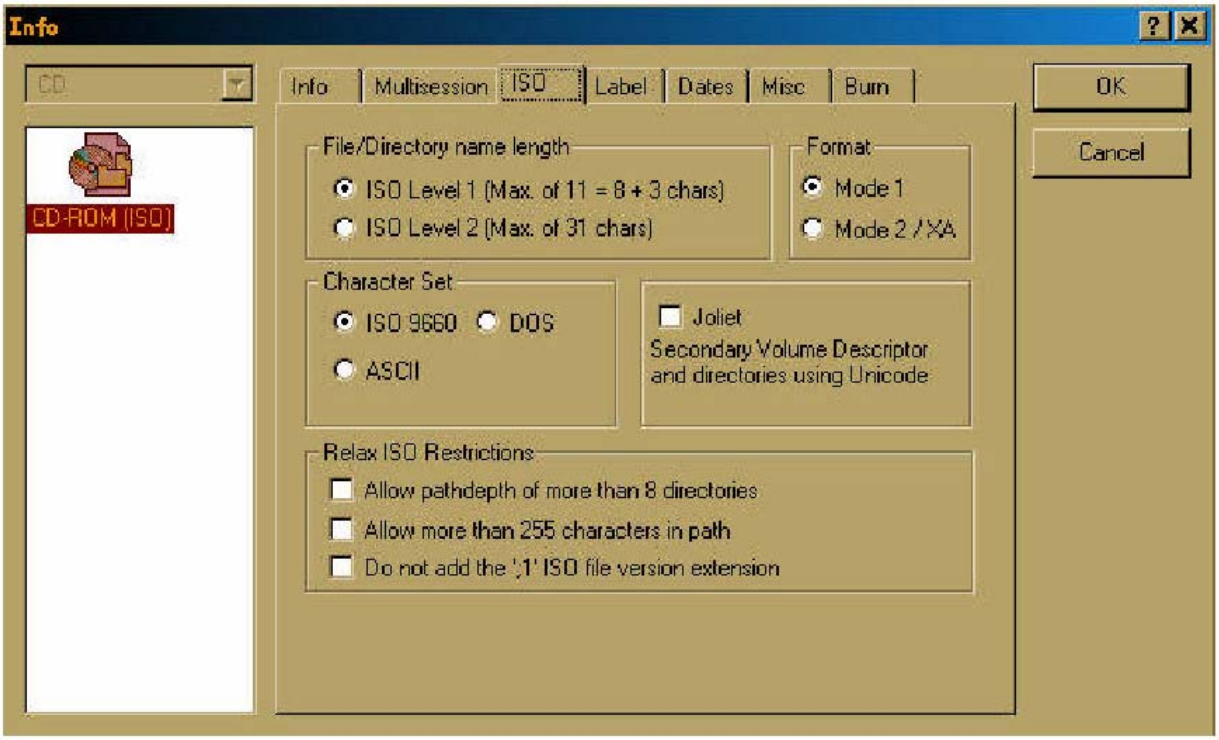
Multisession selection should be "No Multisession"

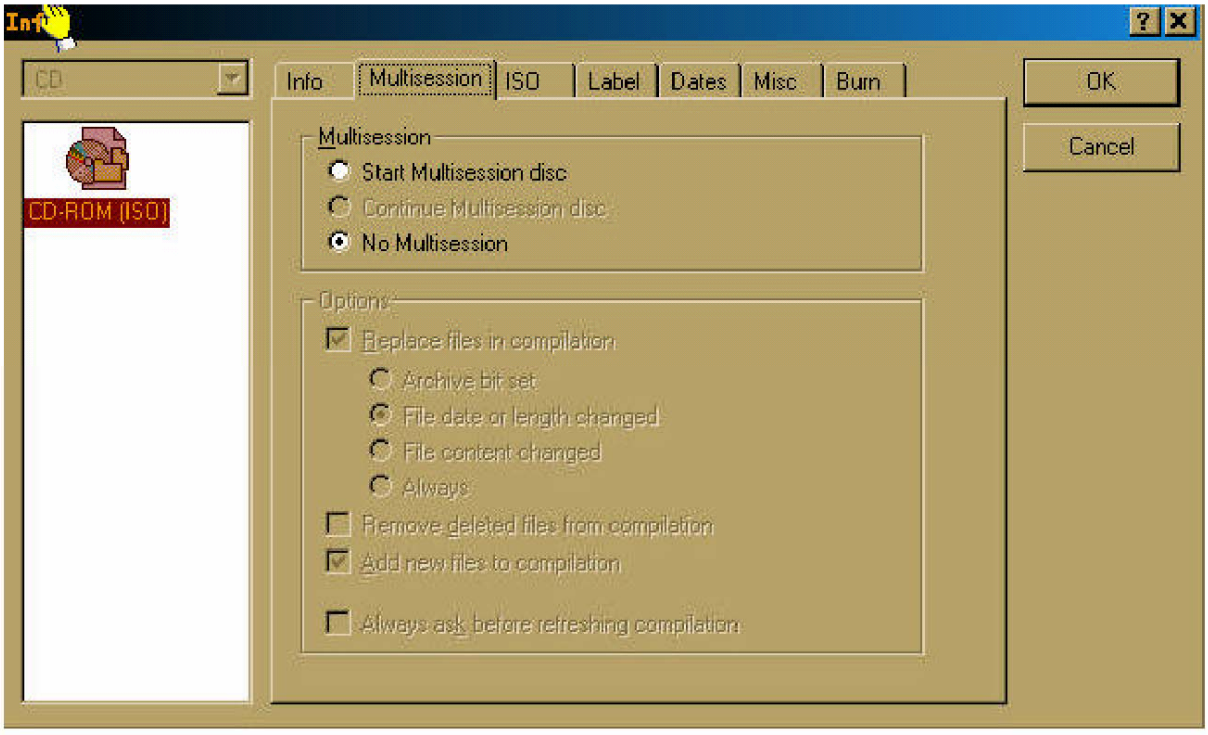
File format should be "IS09660" .Do not use "Joliet"

It is better to erase with "Quick Erase" if you use CD-RW before burning.

There should be no Volume label.

It may be better to put some dummy files in Cd with update file.





2. DVB

FIRST TIME INSTALLATION

In Installation menu first time installation sub-menu exists. If you choose YES by pressing SELECT button on the remote control, EEPROM and database is erased.

SOFTWARE DOWNLOAD FROM COM PORT

RS232 TEST

The list of the necessary equipment is as follows:

PC with “Hyper Terminal” function,
RS232 serial communication cable
RS232 software download kit

Steps to be followed by the user are given below:

1. Connect the serial communication cable between the TVSCART of the receiver and the serial communication port (COM1 or COM2) of the PC.

2. Make sure that the PC is on and the receiver is powered off.

3. Run “Hyper Terminal” program of the PC from Start / Programs / Accessories / Communications / Hyper Terminal menu.

4. For a new connection, run Hypertrm.exe file.

5. Give a name and choose an icon for the connection. (You do not need to make a new connection every time. You can use this name for the future connections.)

6. Choose communication port in the new coming window (COM1 or COM2) whichever you have used in Step 1.

7. Port settings should be as follows:

Bits per second: 38400
Data Bits : 8
Parity : None
Stop bits : 1
Flow control : Hardware

8. Now Hyper Terminal connection is established. When you power on the stb you will see that stb is going to stby state .Then you can activate the stb by remote control and see every result of command from the remote control

If your system passes this test, you can start software download.

Steps to be followed by the user are given below:

1. Connect the serial communication cable between the RS232 outport of the receiver and the serial communication port (COM1 or COM2) of the PC.

2. Make sure that the PC is on and the receiver is in Power on mode.

3. Run “Hyper Terminal” program of the PC from Start / Programs / Accessories / Communications / Hyper Terminal menu.

4. For a new connection, run Hypertrm.exe file.

5. Give a name and choose an icon for the connection. (You do not need to make a new connection every time. You can use this name for the future connections.)

6. Choose communication port in the new coming window (COM1 or COM2) whichever you have used in Step 1.

7. Port settings should be as follows:

Bits per second	:	115200
Data Bits	:	8
Parity	:	None
Stop bits	:	1
Flow control	:	None

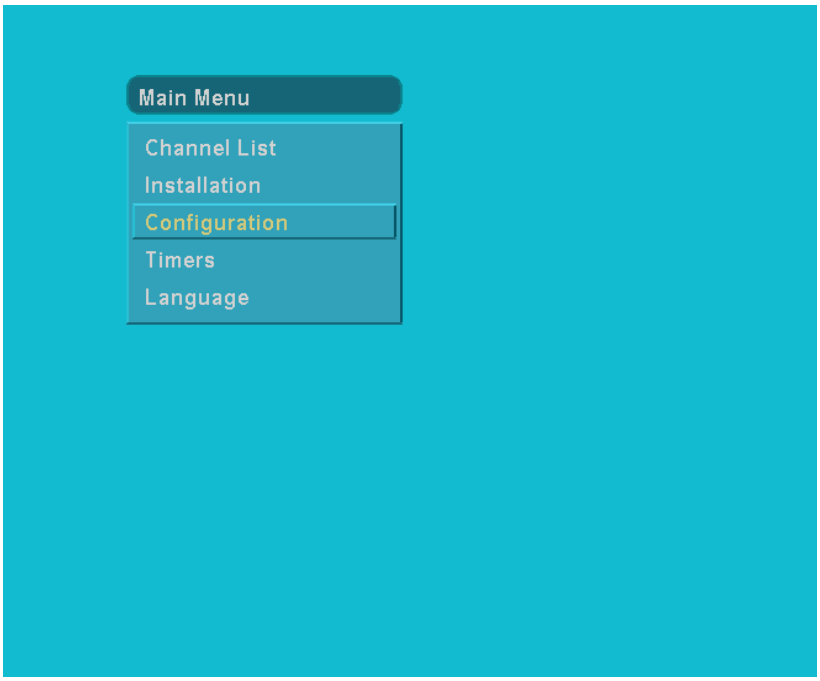
8. Now Hyper Terminal connection is established.

9. Go to Transfer>Send file menu. Press “Browse” button and by using “up one level” button find the directory where you had stored the new software in your PC. Then select the new software name by pressing “open“. Software name and its path is written in SEND FILE “file Name“ bar. Also check that 1K Xmodem option is selected in the “ protocol” menu. Then press ”send” button of SEND FILE menu. You will see that file is started to be transferred. If there is no transfer process that is; counter is not active then please turn off and on the stb through main power chord. During software transfer process software will be transferred with 9k packages and ACTIVE led at the front panel of the stb will be flashing red, later it will turn off for some time. PLEASE WAIT FOR UNTIL ACTIVE LED IS FLASHING RED FOR A FEW TIMES AGAIN AND SOME DIFFERENT CHARACTERS IN THE HYPER TERMINAL SCREEN IS SEEN. During this waiting time new software is written into the flash memory and writing into the flash is not a quick process. Also waiting time increases as the software size increases. This waiting time may be about 3 minutes.

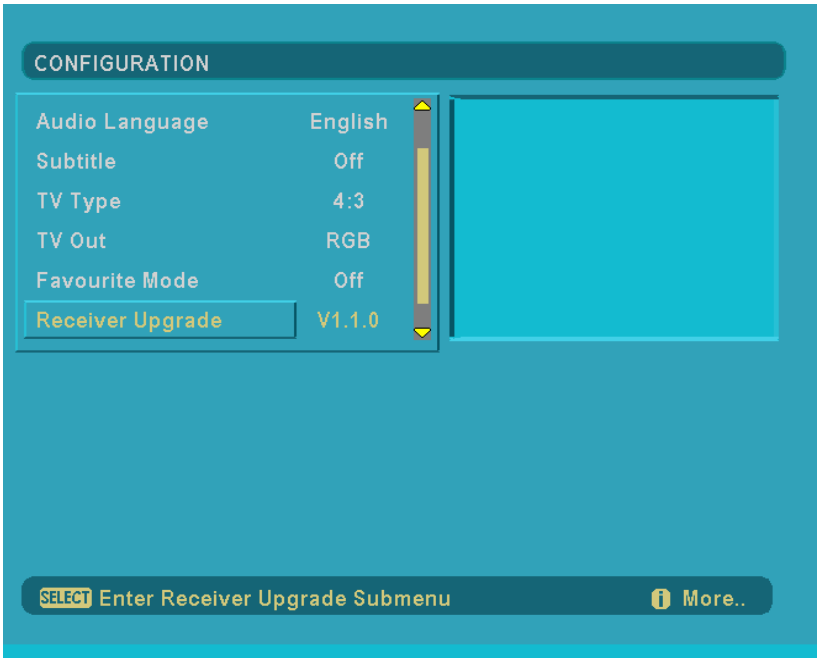
Then activate the STB and do “first time installation” for the new software to run properly. Then you can tune to a channel and test that the new software is functioning properly.

RECEIVER UPGRADE OVER THE AIR

The STB can be upgraded via the configuration menu, entered from the main menu.



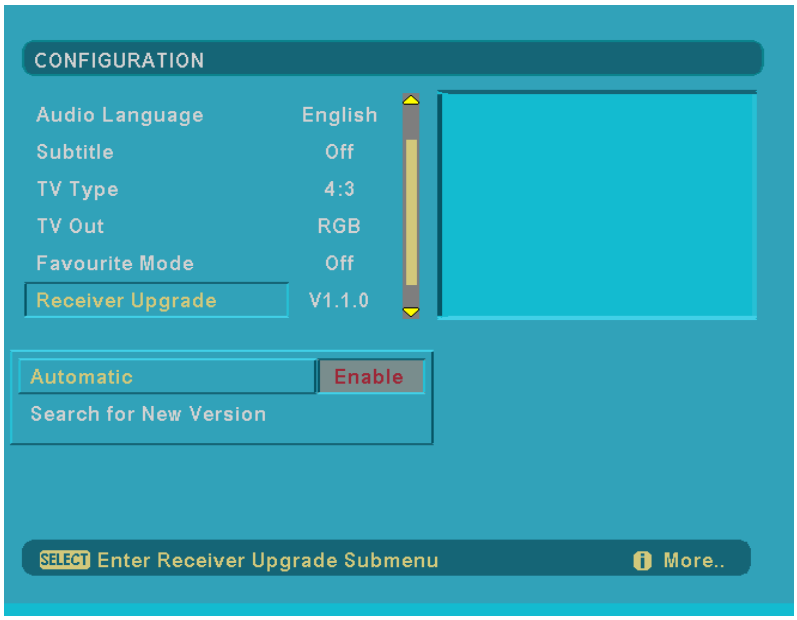
In the configuration menu, there is the “Receiver Upgrade” button. Upgrade process can be started by pressing this button.



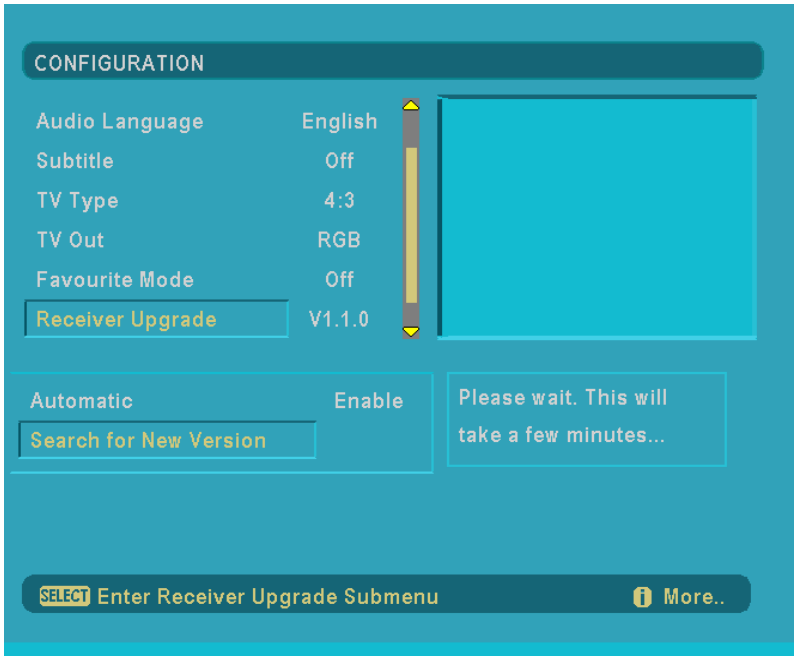
There are two possibilities for receiver software to be upgraded: automatic and manual. Automatic upgrade can be enabled or disabled by pressing Left/Right buttons. If it is enabled, then there are two ways for automatic upgrade. The first one is checking the

existence of a new software every time the STB goes to standby. The second one is waking up at 04:00 a.m. every night, provided that the STB is left in standby mode. Both automatic upgrade methods result in standby mode either upgraded or not. If the automatic upgrade is set to ‘Disable’ then this function will not work.

Manual upgrade starts if the ‘Search for New Version’ button is pressed.



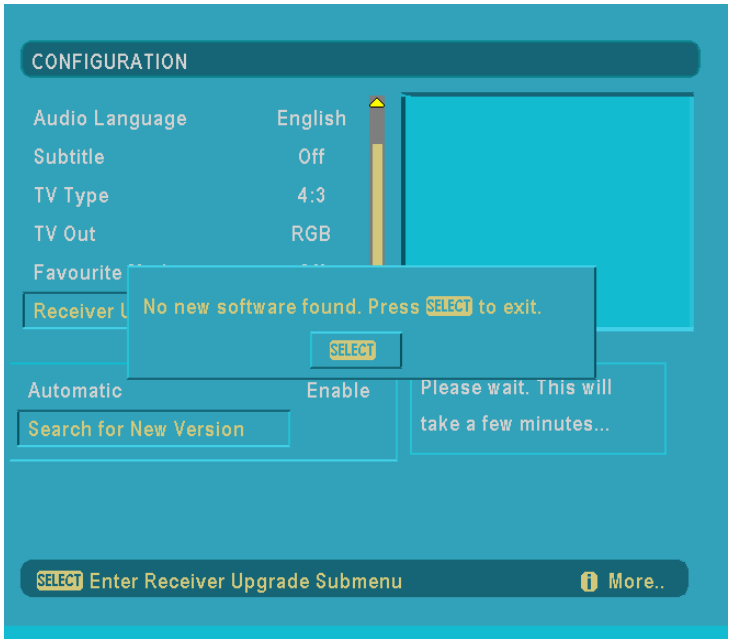
After pressing the ‘Search for New Version’ button, the STB tunes to each frequency that have been stored in its database and looks for the new software. Since this process takes some time, a warning message is displayed.



Depending on the existence of a new software, two different messages can appear on the screen: ‘No new software found. Press SELECT to exit.’ or ‘New software found!

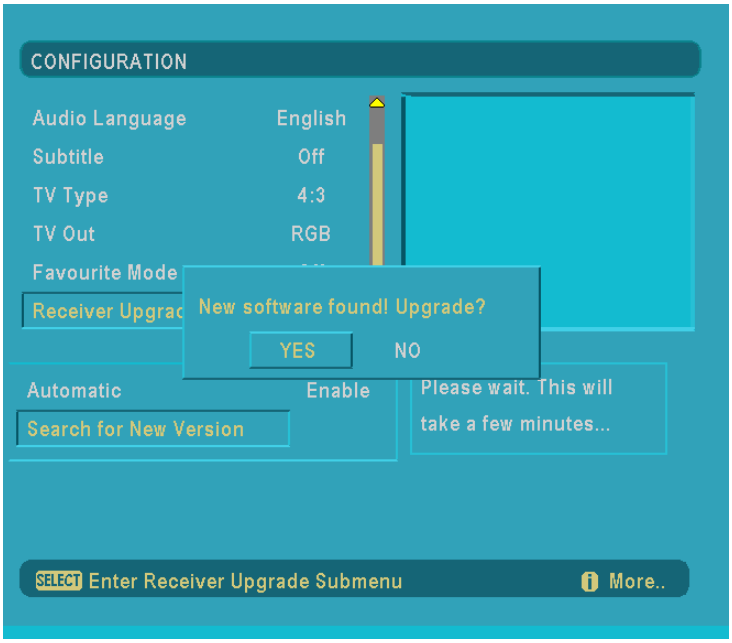
Upgrade?’

If there is no new software, pressing SELECT button returns the STB to the configuration menu.



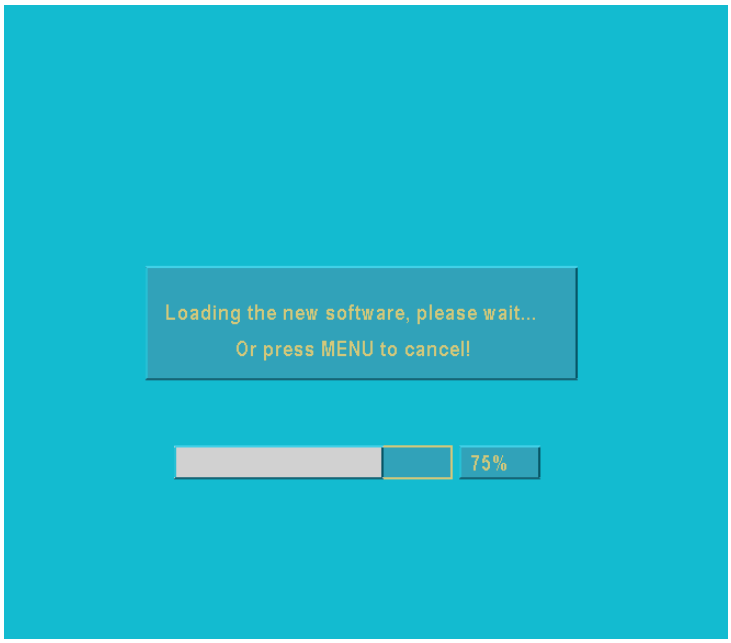
If there is a new software, pressing “Yes” will cause upgrading to be started.

By, pressing “No” user can return to the configuration menu.

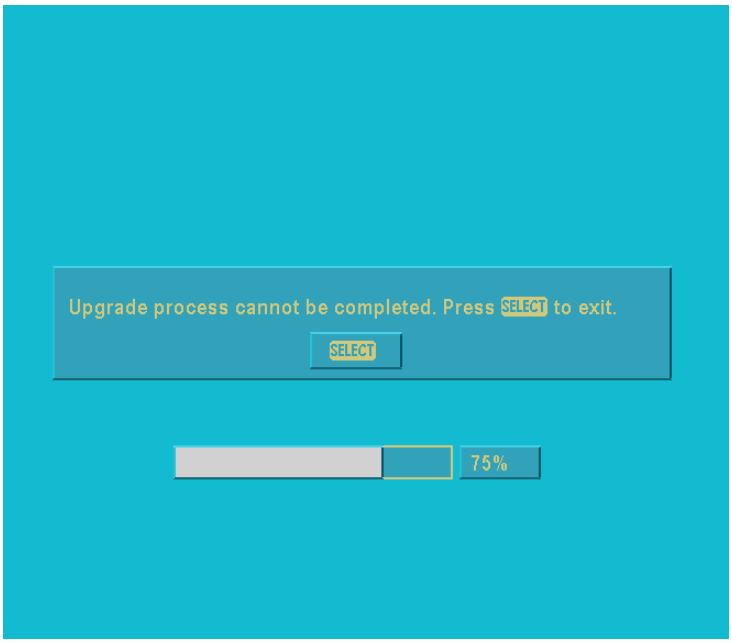


Loading will be displayed on the screen by a message and a progress bar, together with a percentage button will indicate the status.

User can cancel the upgrade any time by pressing the MENU button.

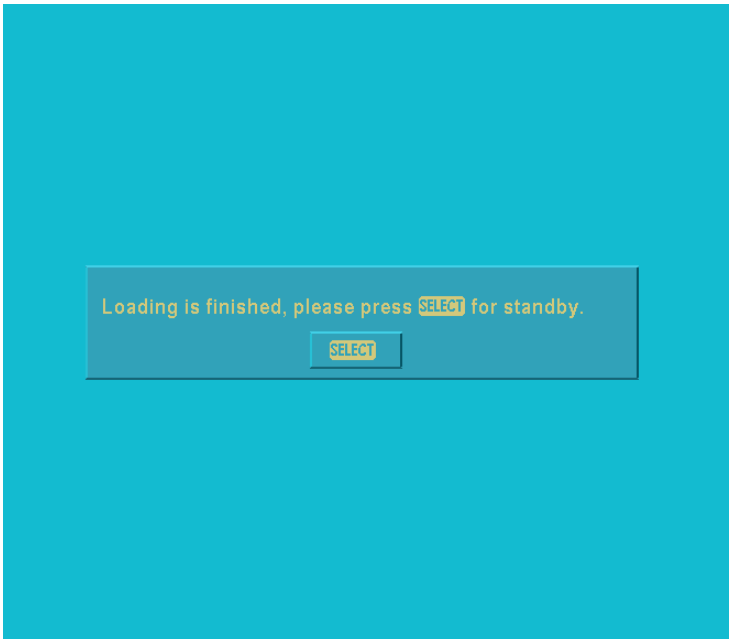


If the upgrade is cancelled or any error is occurred during the loading process, a warning message is displayed and user is asked to press the SELECT button for returning the last watched channel.



After loading the software into memory (SDRAM), it will be written permanent memory (flash).If the STB power is down while new software is being written into the flash memory then new software will not run and old software will be cleaned also. The restoring code is G-O-L-F (3-5-4-2).To restore the receiver software please power off the stb from mains. When you power on the stb again you will recognize that the led at the front panel is first green for some time and then it is turning into red colour. To open the zipped software which is stored in the factory you should at least press the G button of the remote control

while the led is green during start up and pressing O-L-F buttons consecutively. For the back up software to run properly do First Time Installation.

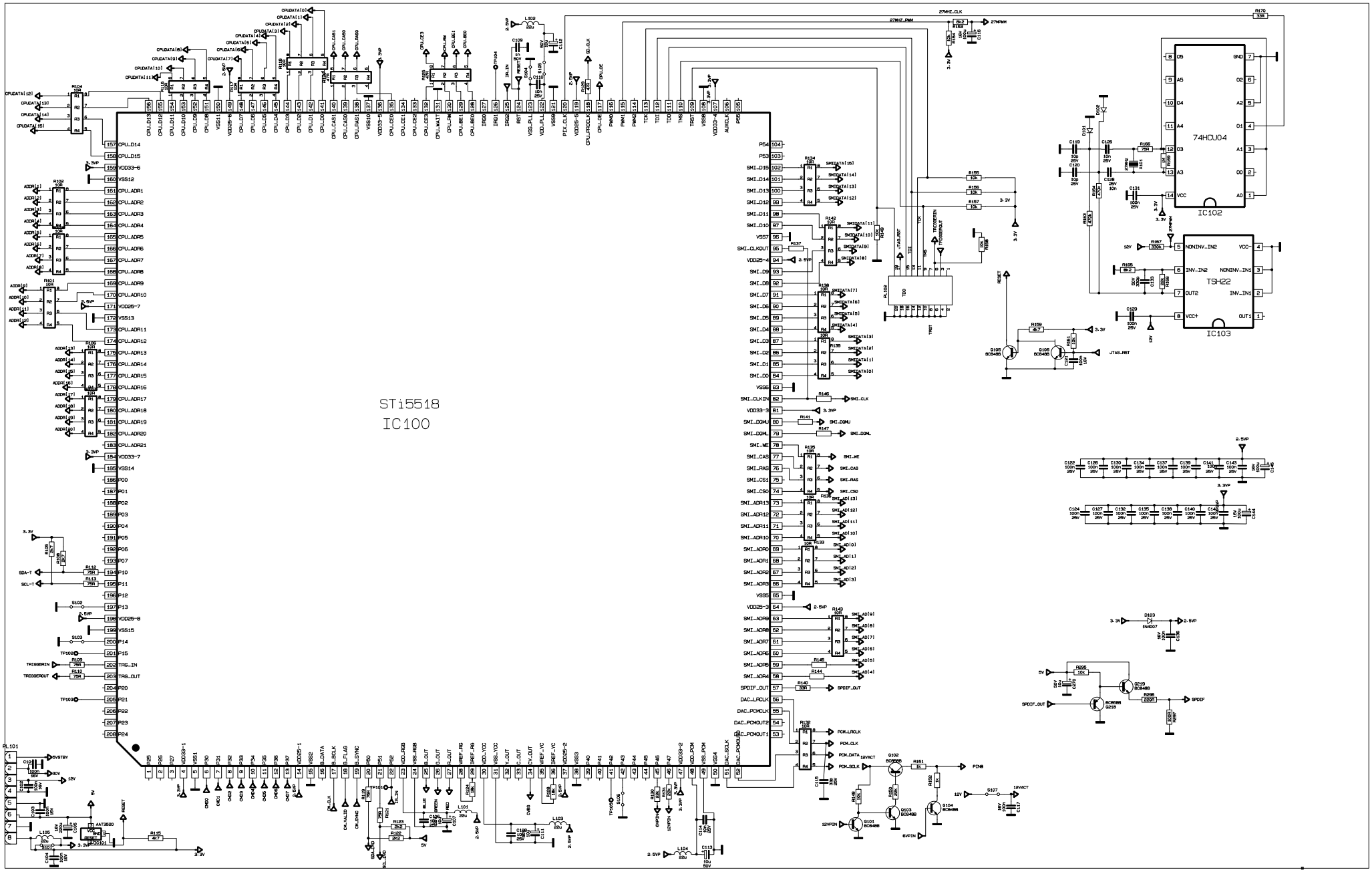


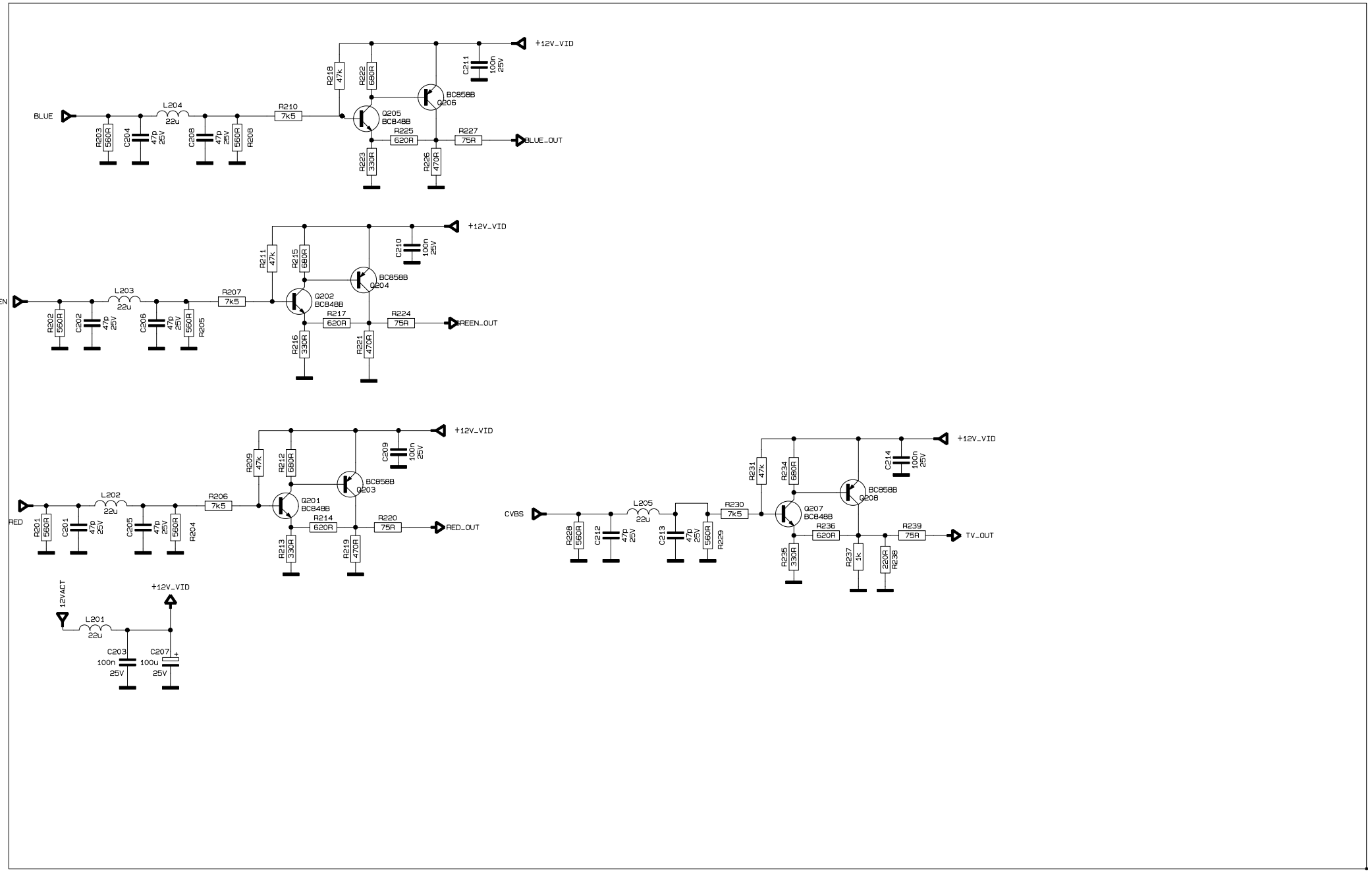
If there is no problem during software download through the air process then the above message indicating a successful upgrade will be shown and the STB should go into standby mode in order the changes to take place.

THE UPDATED PARTS LIST

FOR THIS MODEL IS

AVAILABLE ON ESTA


STi5518
IC100
74HCU04
IC102
TSH22
IC103


A
B
C
D
E
F
1
2
3
4
BLUE
L204
22u
R203
560R
C204
470
25V
C208
470
25V
R208
560R
R210
7k5
R218
47k
R222
680R
C211
100n
25V
+12V_VID
BC858B
Q206
Q205
BC848B
R225
620R
R227
75R
BLUE_OUT
R223
330R
R226
470R
GREEN
L203
22u
R202
560R
C202
470
25V
C206
470
25V
R205
560R
R207
7k5
R211
47k
R215
680R
C210
100n
25V
+12V_VID
BC858B
Q204
Q202
BC848B
R217
620R
R224
75R
GREEN_OUT
R216
330R
R221
470R
RED
L202
22u
R201
560R
C201
470
25V
C205
470
25V
R204
560R
R206
7k5
R209
47k
R212
680R
C209
100n
25V
+12V_VID
BC858B
Q203
Q201
BC848B
R214
620R
R220
75R
RED_OUT
R213
330R
R219
470R
12VACT
L201
22u
C203
100n
25V
C207
100u
25V
+12V_VID
CVBS
L205
22u
R228
560R
C212
470
25V
C213
470
25V
R229
560R
R230
7k5
R231
47k
R234
680R
C214
100n
25V
+12V_VID
BC858B
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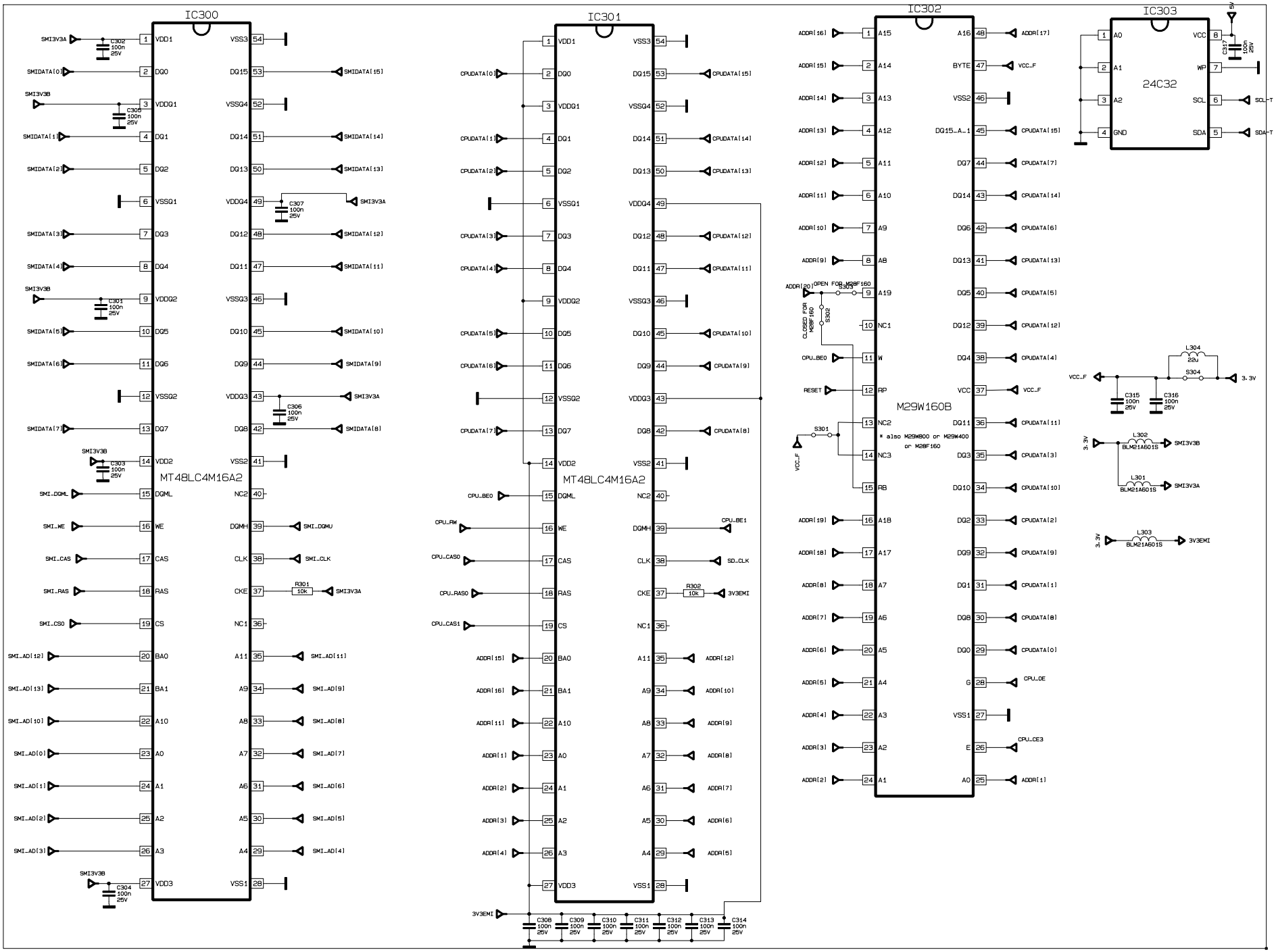
75R
TV_OUT
R235
330R
R237
1K
R238
220R


IC300
MT48LC4M16A2
SMI3V3A
SMI3V3B
C302 100n 25V
C305 100n 25V
C301 100n 25V
C303 100n 25V
C304 100n 25V
C307 100n 25V
C306 100n 25V
R301 10k
SMIDATA[0]
SMIDATA[1]
SMIDATA[2]
SMIDATA[3]
SMIDATA[4]
SMIDATA[5]
SMIDATA[6]
SMIDATA[7]
SMIDATA[8]
SMIDATA[9]
SMIDATA[10]
SMIDATA[11]
SMIDATA[12]
SMIDATA[13]
SMIDATA[14]
SMIDATA[15]
SMI_DQML
SMI_WE
SMI_CAS
SMI_RAS
SMI_CS0
SMI_DQMU
SMI_CLK
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SMI_AD[6]
SMI_AD[5]
SMI_AD[4]
IC301
MT48LC4M16A2
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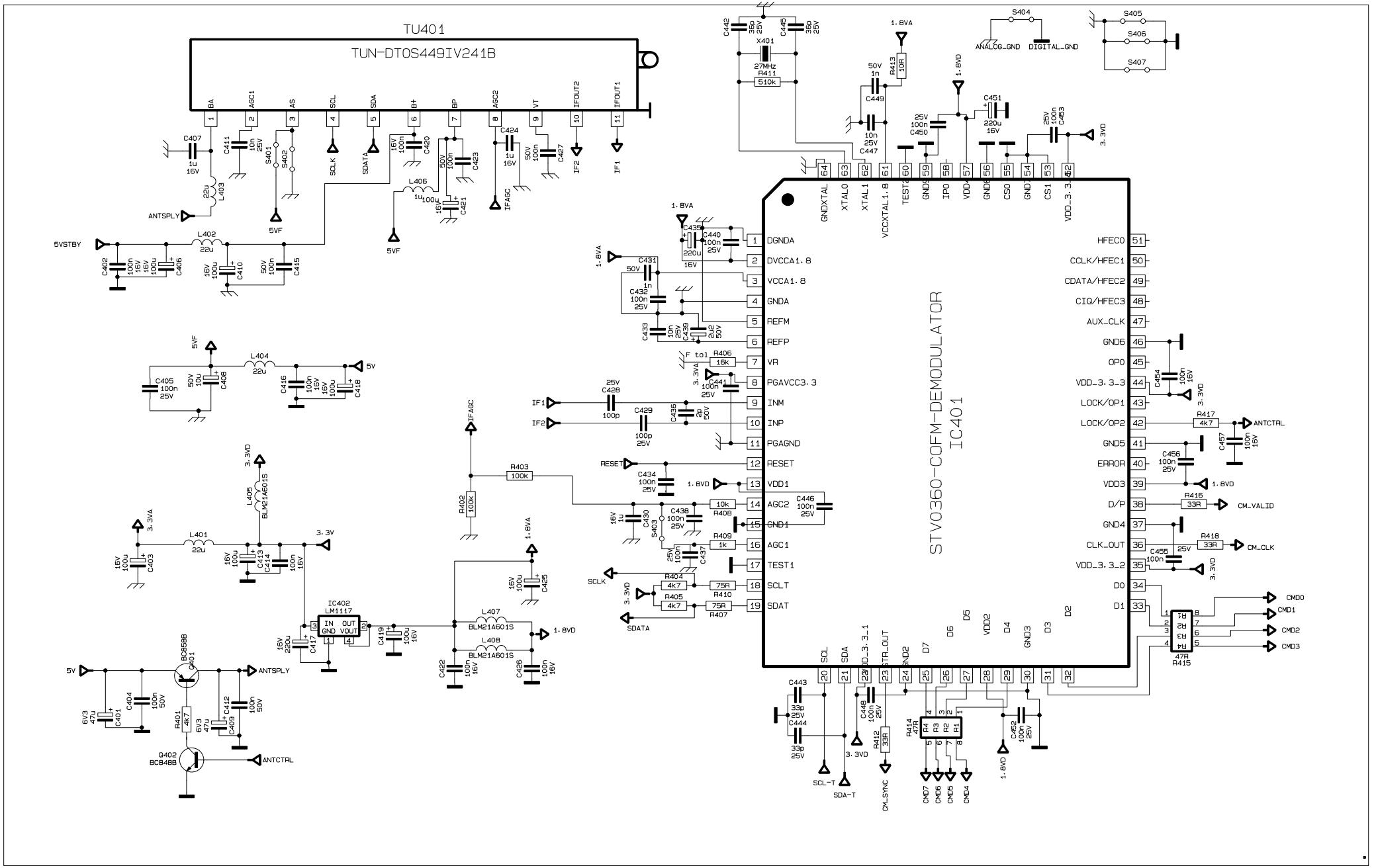
CPUDATA[1]
CPUDATA[2]
CPUDATA[3]
CPUDATA[4]
CPUDATA[5]
CPUDATA[6]
CPUDATA[7]
CPUDATA[8]
CPUDATA[9]
CPUDATA[10]
CPUDATA[11]
CPUDATA[12]
CPUDATA[13]
CPUDATA[14]
CPUDATA[15]
CPU_BE0
CPU_RW
CPU_CAS0
CPU_RAS0
CPU_CAS1
CPU_BE1
SD_CLK
3V3EMI
R302 10k
ADDR[15]
ADDR[16]
ADDR[11]
ADDR[1]
ADDR[2]
ADDR[3]
ADDR[4]
ADDR[12]
ADDR[10]
ADDR[9]
ADDR[8]
ADDR[7]
ADDR[6]
ADDR[5]
C308 100n 25V
C309 100n 25V
C310 100n 25V
C311 100n 25V
C312 100n 25V
C313 100n 25V
C314 100n 25V
IC302
M29W160B
* also M29W800 or M29W400 or M28F160
ADDR[16]
ADDR[15]
ADDR[14]
ADDR[13]
ADDR[12]
ADDR[11]
ADDR[10]
ADDR[9]
ADDR[20]
CPU_BE0
RESET
S301
VCC_F
ADDR[19]
ADDR[18]
ADDR[8]
ADDR[7]
ADDR[6]
ADDR[5]
ADDR[4]
ADDR[3]
ADDR[2]
ADDR[17]
VCC_F
CPUDATA[15]
CPUDATA[7]
CPUDATA[14]
CPUDATA[6]
CPUDATA[13]
CPUDATA[5]
CPUDATA[12]
CPUDATA[4]
CPUDATA[11]
CPUDATA[3]
CPUDATA[10]
CPUDATA[2]
CPUDATA[9]
CPUDATA[1]
CPUDATA[8]
CPUDATA[0]
CPU_OE
CPU_CE3
ADDR[1]
OPEN FOR M28F160
S303
S302
CLOSED FOR M28F160
IC303
24C32
C317 100n 25V
SCL-T
SDA-T
L304 22U
S304
3.3V
C315 100n 25V
C316 100n 25V
L302 BLM21A601S
SMI3V3B
L301 BLM21A601S
SMI3V3A
L303 BLM21A601S
3V3EMI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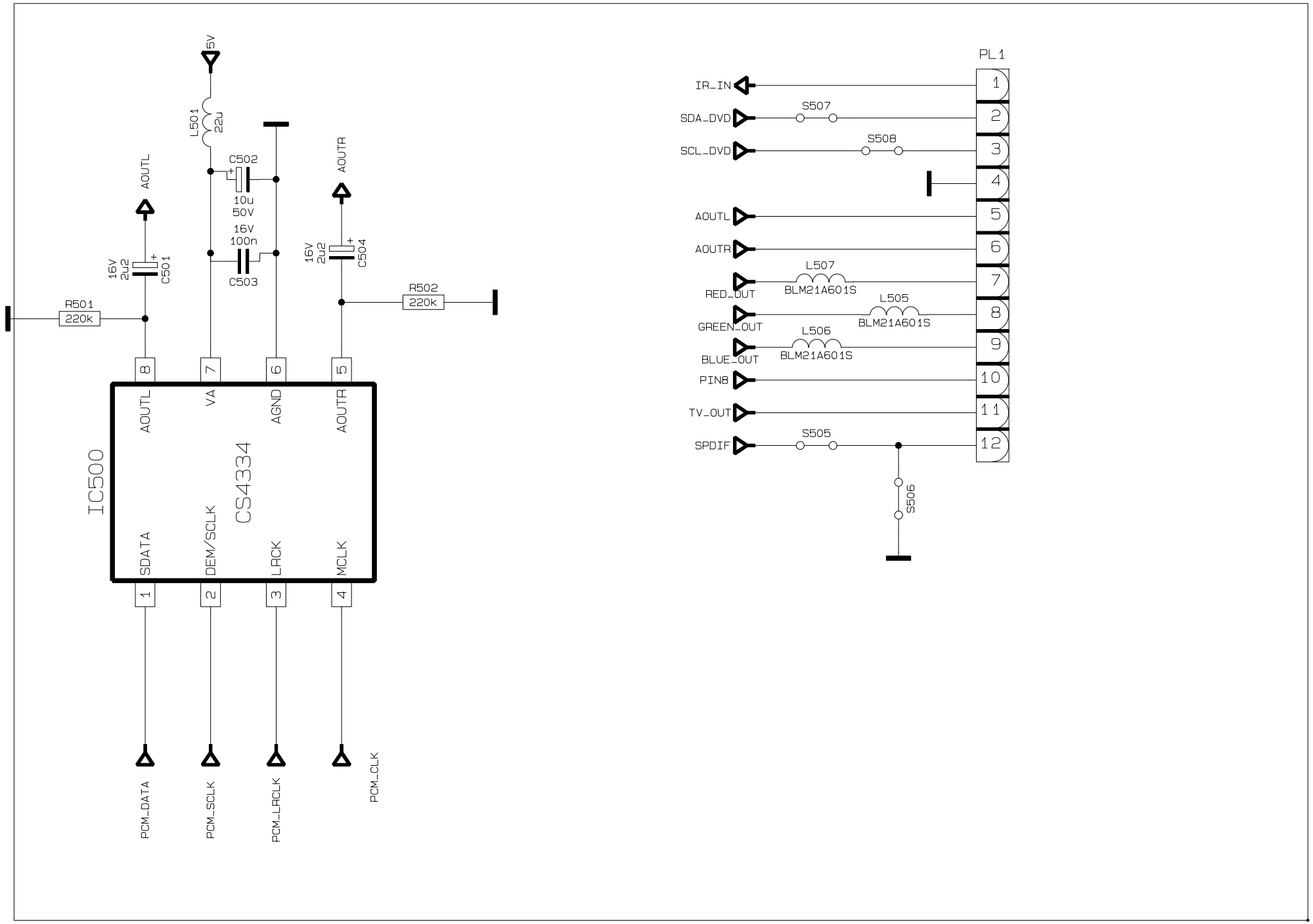
TUN-DT0S449IV241B
STV0360-COFM-DEMODULATOR
IC401
IC402
LM1117
Q401
BC858B
Q402
BC848B
ANTSPLY
5VSTBY
5VF
5V
3.3V
3.3VA
1.8VD
1.8VA
ANTCTRL
IFAGC
SCLK
SDATA
SCL-T
SDA-T
CM_SYNC
CM_VALID
CM_CLK
CMD0
CMD1
CMD2
CMD3
CMD4
CMD5
CMD6
CMD7
ANALOG_GND
DIGITAL_GND
27MHz


5V
L501
22u
C502
10u
50V
16V
100n
C503
AOUTL
16V
2u2
C501
R501
220k
AOUTR
16V
2u2
C504
R502
220k
IC500
CS4334
8
7
6
5
AOUTL
VA
AGND
AOUTR
SDATA
DEM/SCLK
LRCK
MCLK
1
2
3
4
PCM_DATA
PCM_SCLK
PCM_LRCLK
PCM_CLK
PL1
IR_IN
SDA_DVD
S507
SCL_DVD
S508
AOUTL
AOUTR
RED_OUT
L507
BLM21A601S
GREEN_OUT
L505
BLM21A601S
BLUE_OUT
L506
BLM21A601S
PIN8
TV_OUT
SPDIF
S505
S506
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2
3
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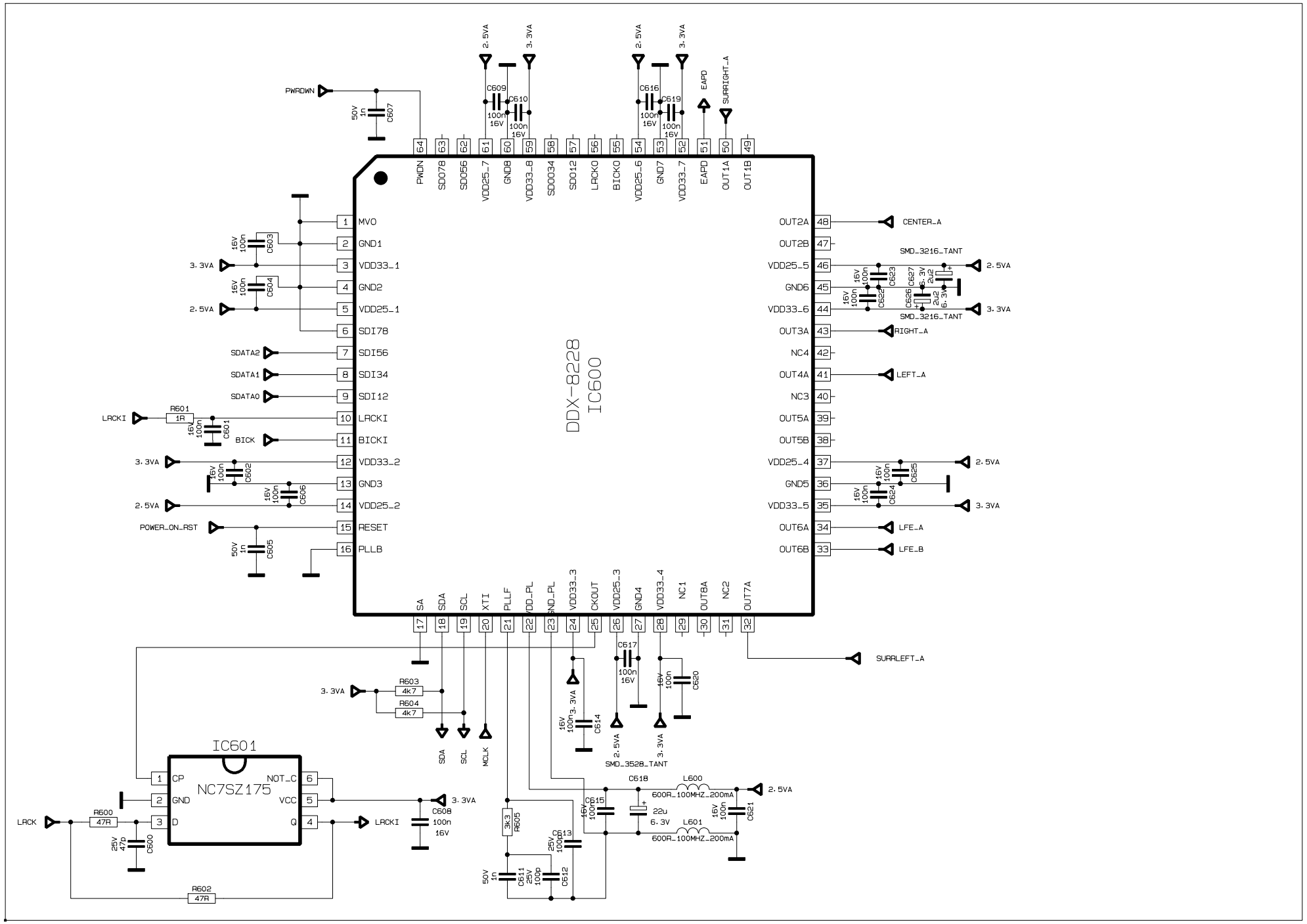
7
8
9
10
11
12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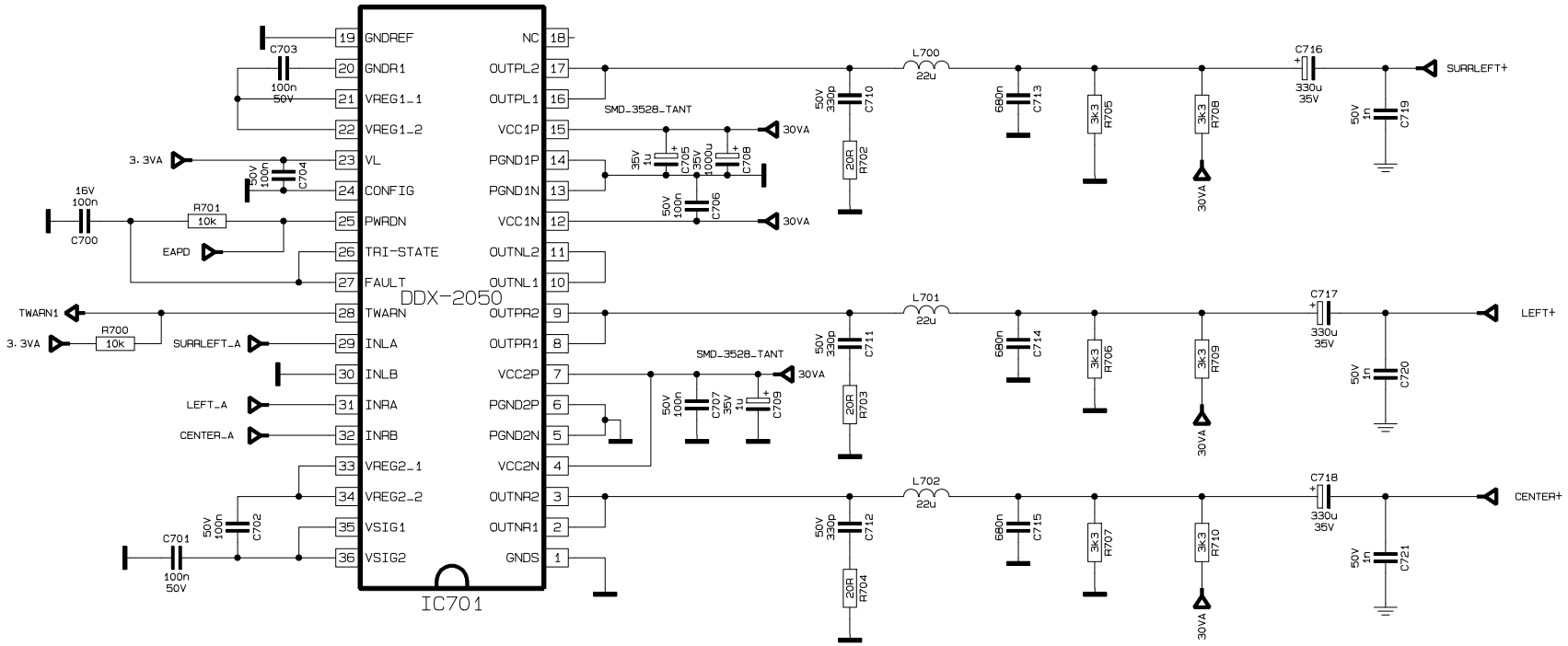
IC600
IC601
NC7SZ175
PWRDWN
LACKI
BICK
SDATA2
SDATA1
SDATA0
POWER_ON_RST
SDA
SCL
MCLK
LACK
CENTER_A
RIGHT_A
LEFT_A
LFE_A
LFE_B
SURRLEFT_A
SURRIGHT_A
EAPD
2.5VA
3.3VA
SMD_3216_TANT
SMD_3528_TANT
600R_100MHZ_200mA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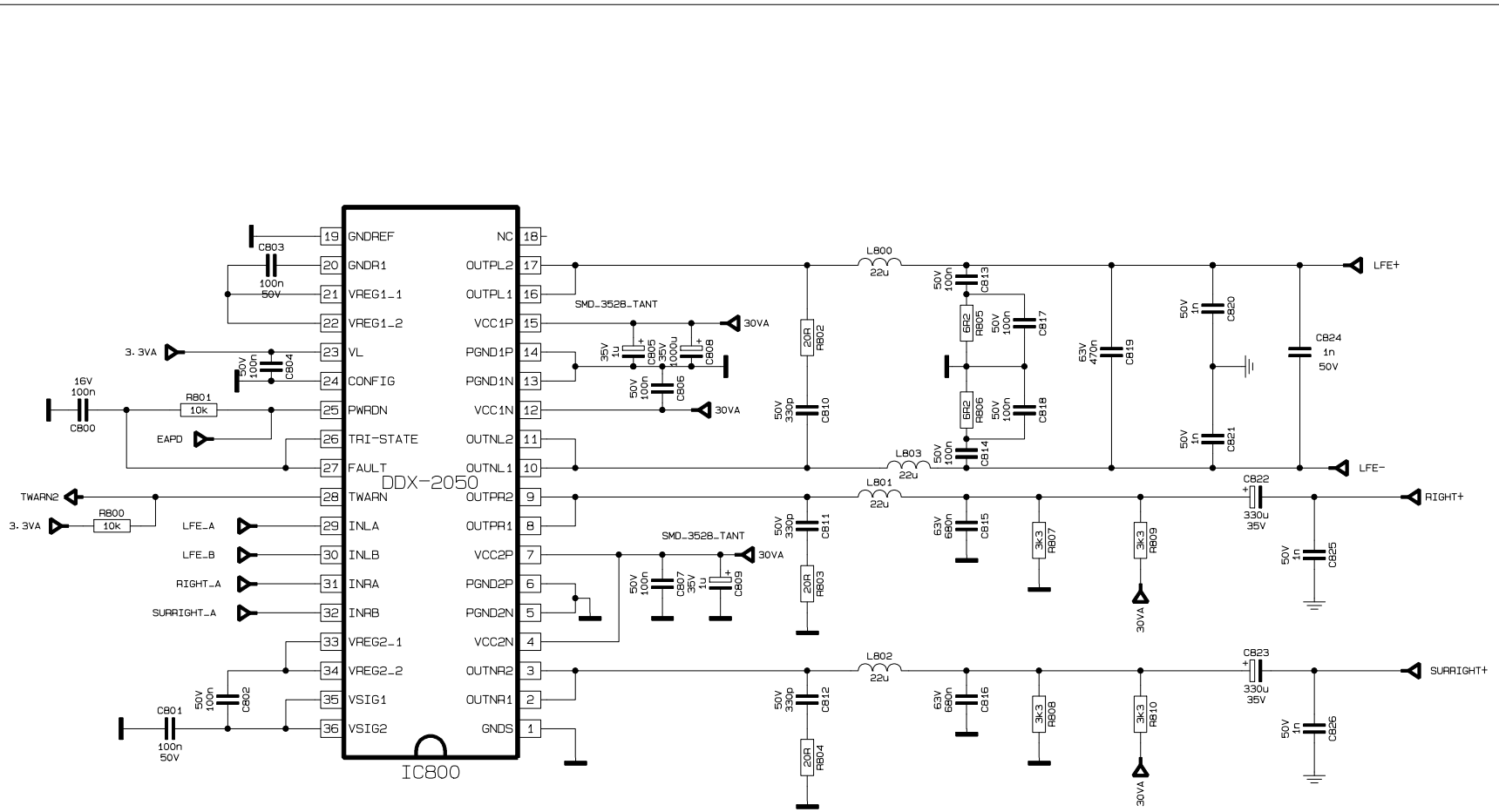
DDX-2050
GNDREF
GNDR1
VREG1_1
VREG1_2
VL
CONFIG
PWRDN
TRI-STATE
FAULT
TWARN
INLA
INLB
INRA
INRB
VREG2_1
VREG2_2
VSIG1
VSIG2
NC
OUTPL2
OUTPL1
VCC1P
PGND1P
PGND1N
VCC1N
OUTNL2
OUTNL1
OUTPR2
OUTPR1
VCC2P
PGND2P
PGND2N
VCC2N
OUTNR2
OUTNR1
GNDS
3.3VA
EAPD
TWARN1
SURLEFT_A
LEFT_A
CENTER_A
30VA
SMD_3528_TANT
L700
L701
L702
SURLEFT+
LEFT+
CENTER+


DDX-2050
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GNDREF
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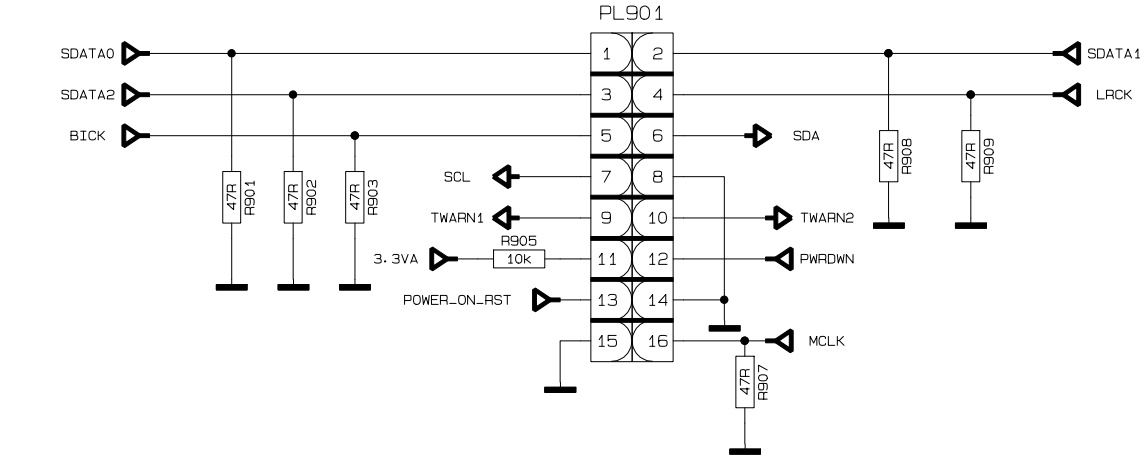
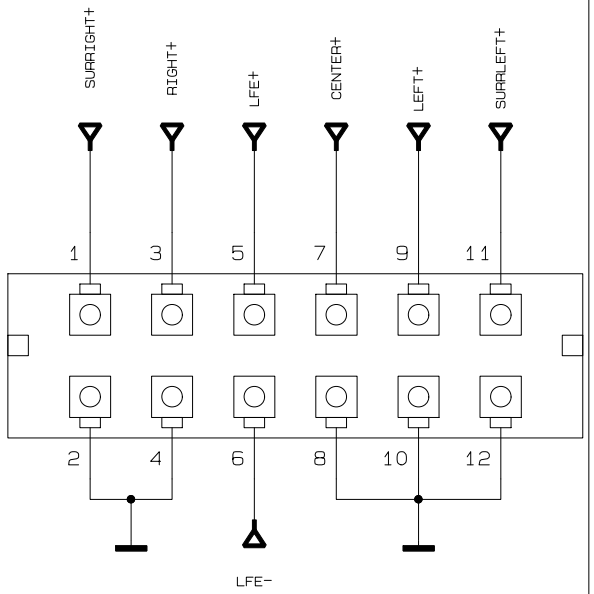
VREG1_1
VREG1_2
VL
CONFIG
PWRDN
TRI-STATE
FAULT
TWARN
INLA
INLB
INRA
INRB
VREG2_1
VREG2_2
VSIG1
VSIG2
NC
OUTPL2
OUTPL1
VCC1P
PGND1P
PGND1N
VCC1N
OUTNL2
OUTNL1
OUTPR2
OUTPR1
VCC2P
PGND2P
PGND2N
VCC2N
OUTNR2
OUTNR1
GNDS
C803
C804
C800
R801
EAPD
R800
C802
C801
SMD_3528_TANT
C805
C808
C806
C807
C809
30VA
3. 3VA
TWARN2
LFE_A
LFE_B
RIGHT_A
SURRIGHT_A
L800
L803
L801
L802
C813
C817
C820
C824
C819
C821
C818
C814
C822
C825
C811
C815
C807
C812
C816
C823
C826
R802
R805
R806
R803
R807
R809
R804
R808
R810
LFE+
LFE-
RIGHT+
SURRIGHT+


PL901
SDATA0
SDATA2
BICK
SCL
TWARN1
3.3VA
POWER_ON_RST
SDATA1
LRCK
SDA
TWARN2
PWRDWN
MCLK
R905
10k
47R R901
47R R902
47R R903
47R R907
47R R908
47R R909


SURRIGHT+
RIGHT+
LFE+
CENTER+
LEFT+
SURRLEFT+
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3
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2
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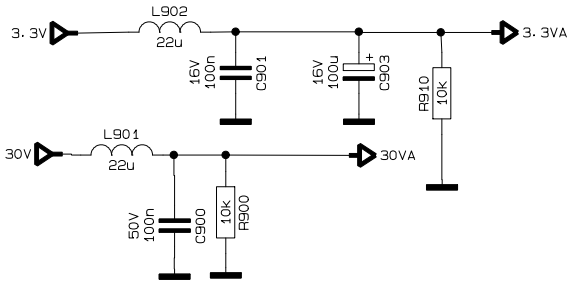
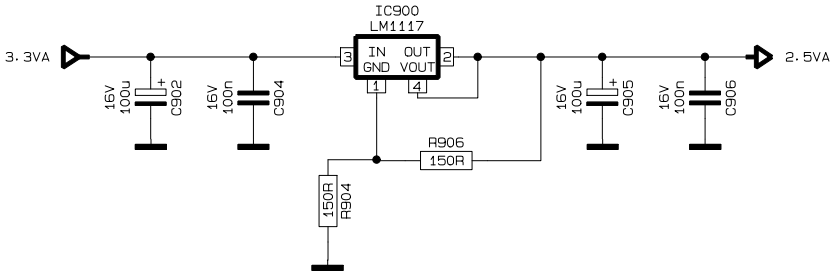
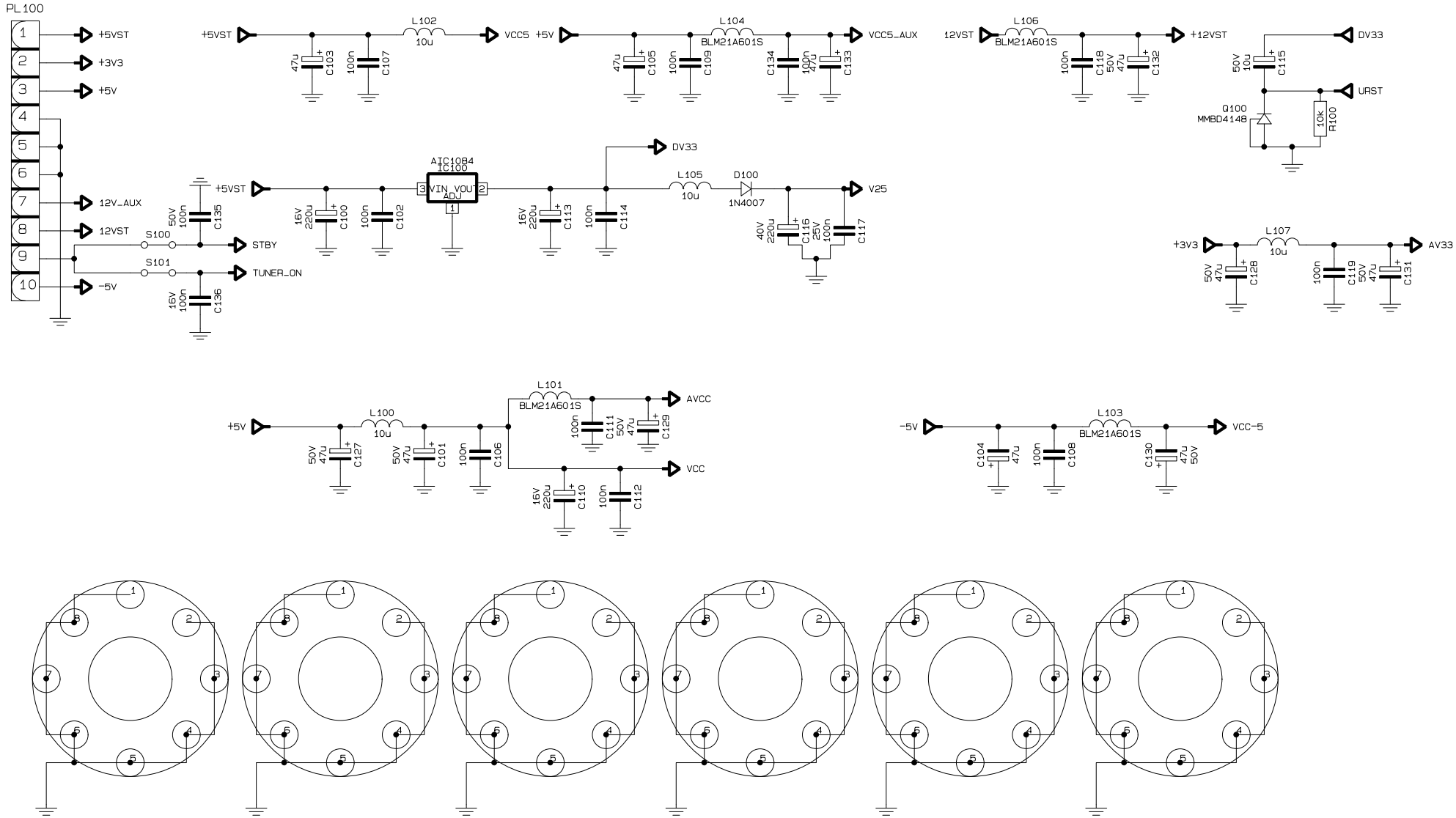
6
8
10
12
LFE-


3.3V
L902
22u
3.3VA
16V 100n C901
16V 100u C903
R910 10k
30V
L901
22u
30VA
50V 100n C900
10k R900


IC900
LM1117
IN
GND
OUT
VOUT
3.3VA
2.5VA
16V 100u C902
16V 100n C904
16V 100u C905
16V 100n C906
R906
150R
150R R904



AV 1300 MAIN BOARD SHEET 1
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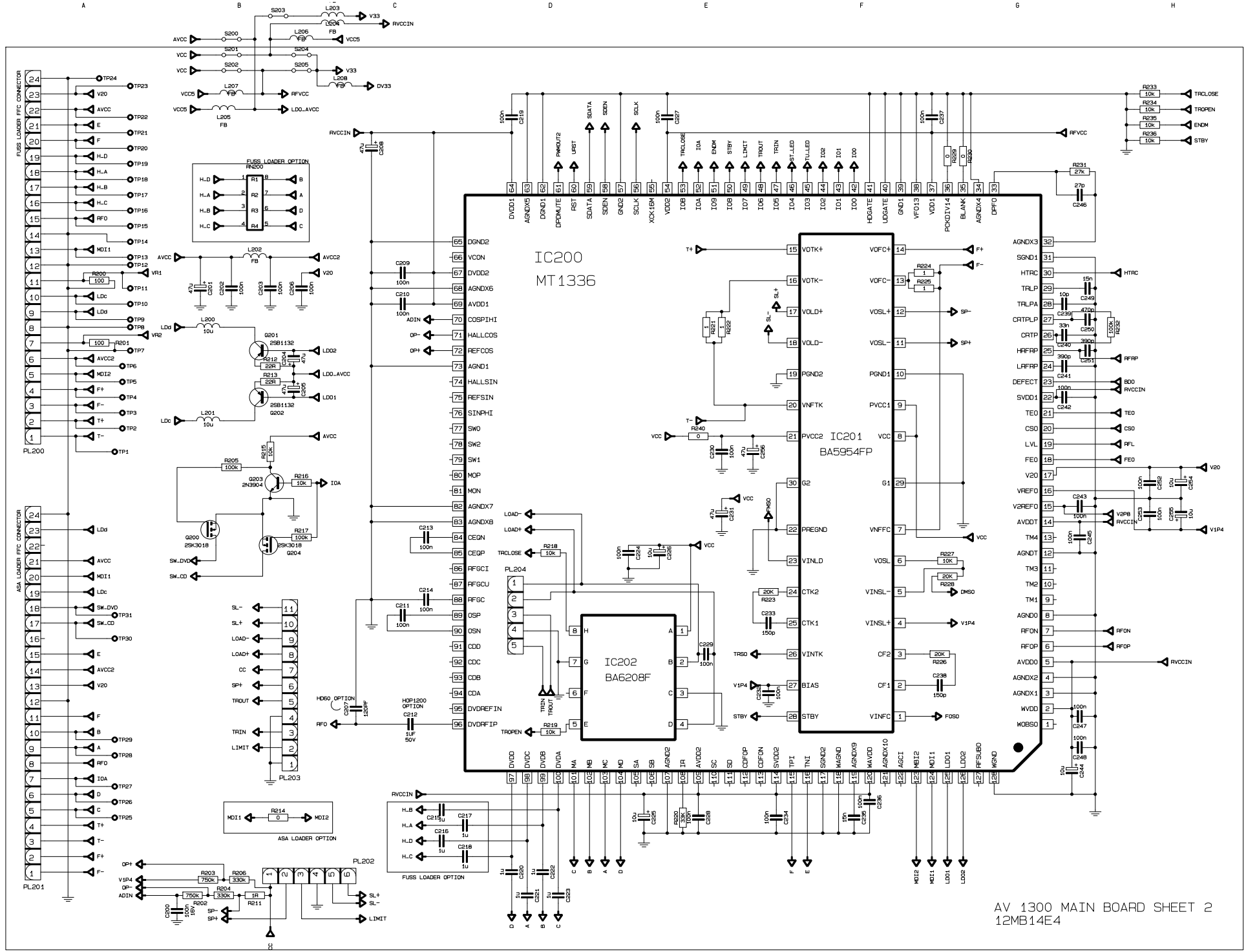
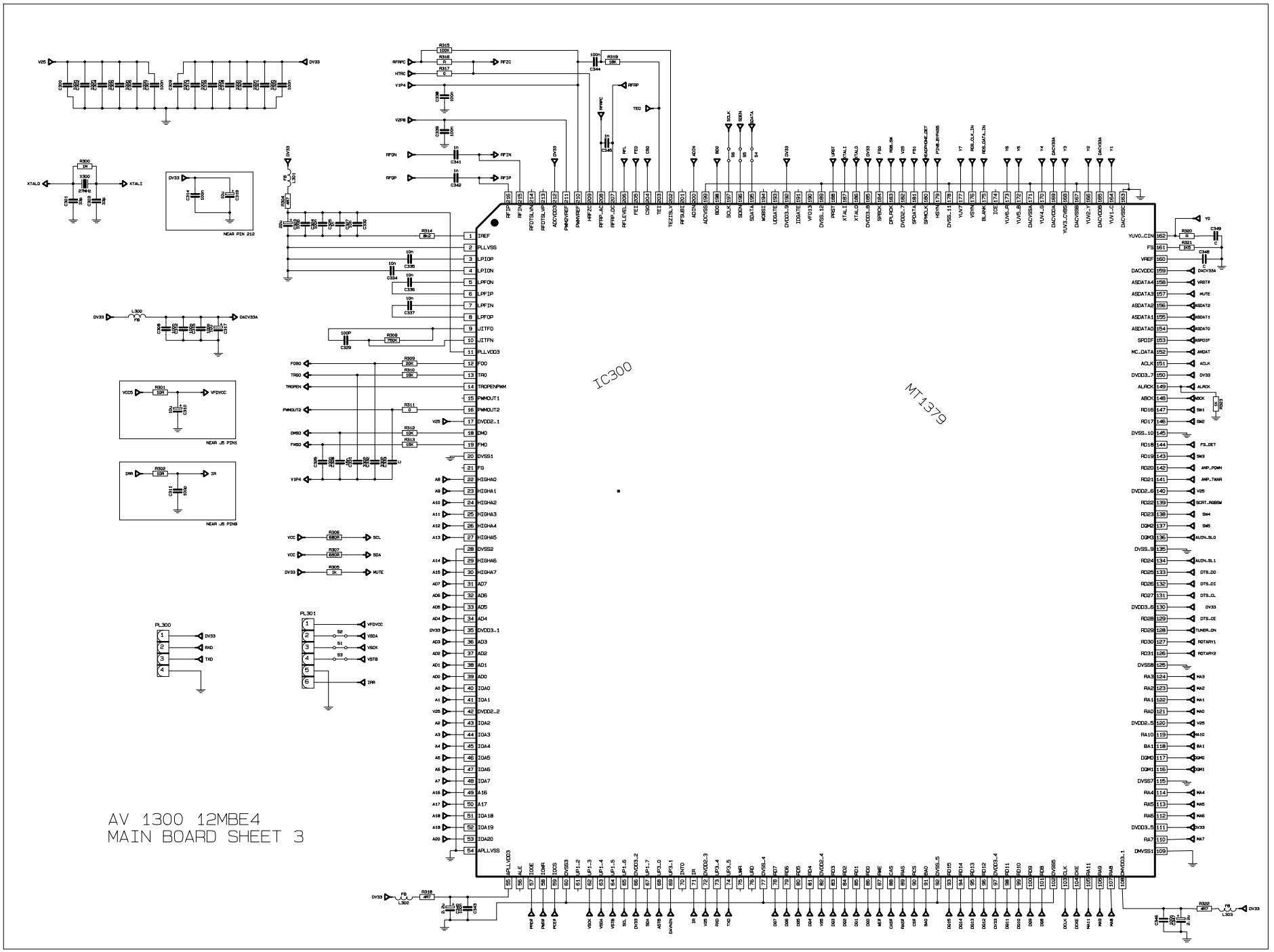
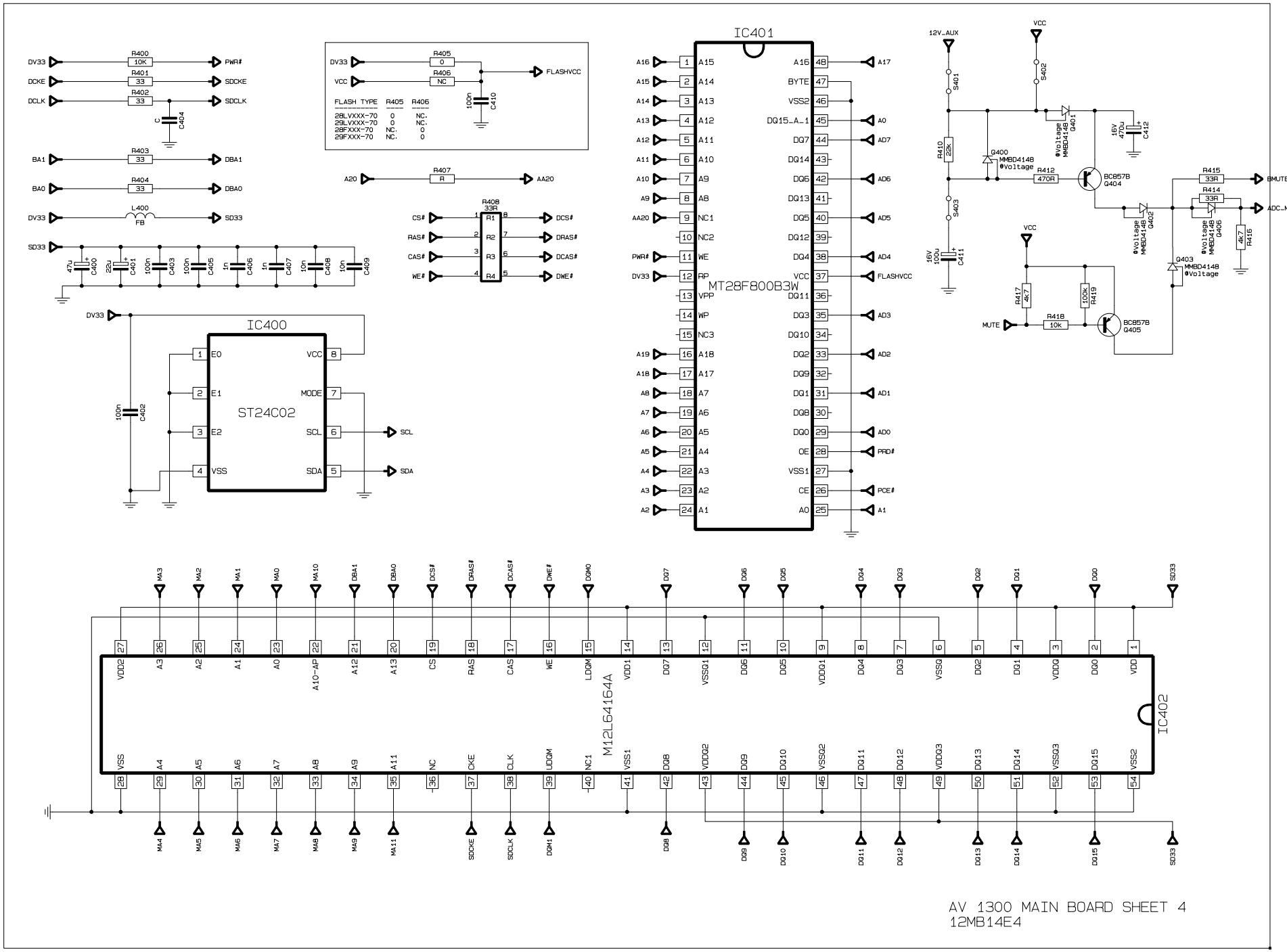

IC200
MT1336
IC201
BA5954FP
IC202
BA6208F
FUSS LOADER FFC CONNECTOR
ASA LOADER FFC CONNECTOR
PL200
PL201
PL202
PL203
PL204
FUSS LOADER OPTION
ASA LOADER OPTION
HD60 OPTION
HDP1200 OPTION
AV 1300 MAIN BOARD SHEET 2
12MB14E4


IC300
MT1379
AV 1300 12MBE4
MAIN BOARD SHEET 3



AV 1300 MAIN BOARD SHEET 4
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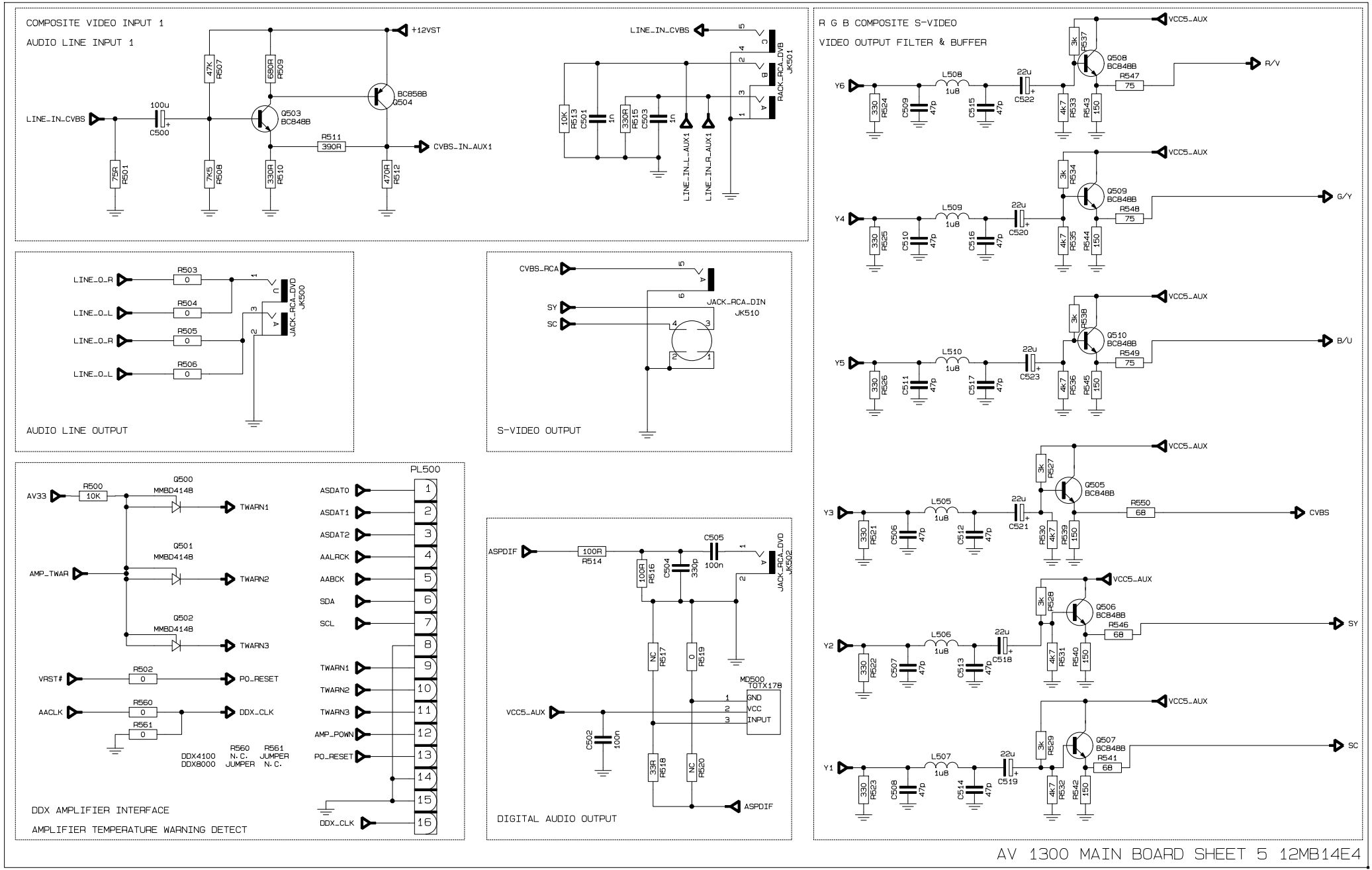
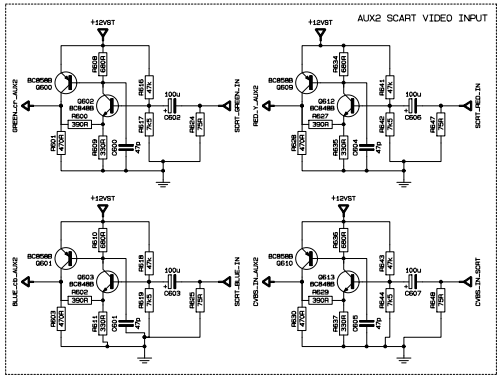
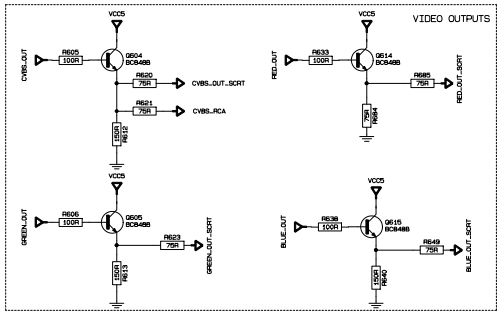
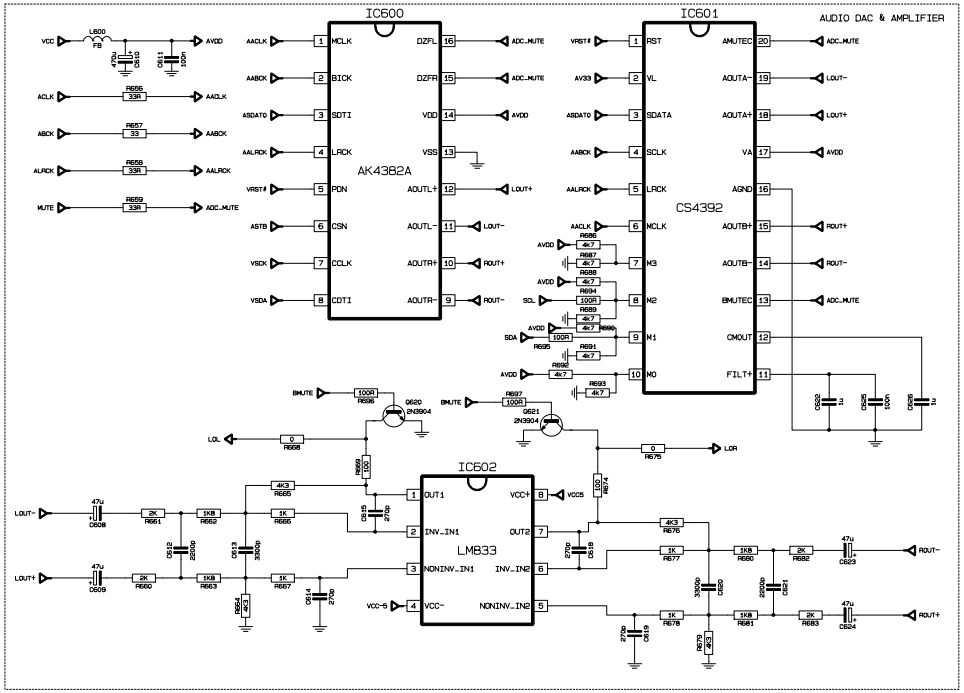
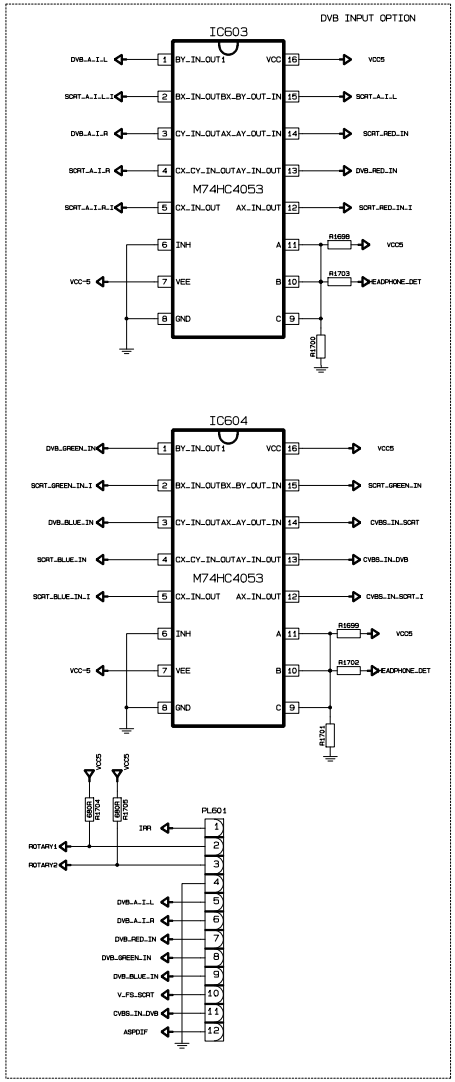


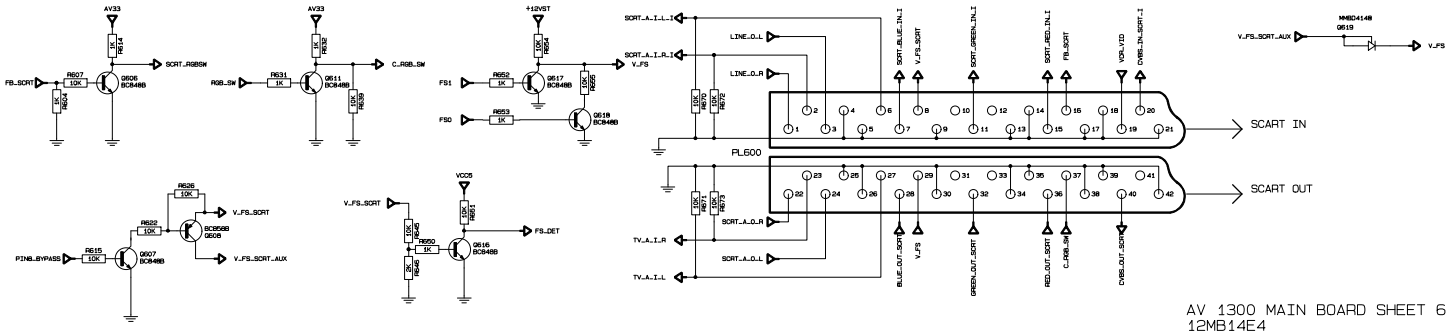
AV 1300 MAIN BOARD SHEET 5 12MB14E4











AV 1300 MAIN BOARD SHEET 6
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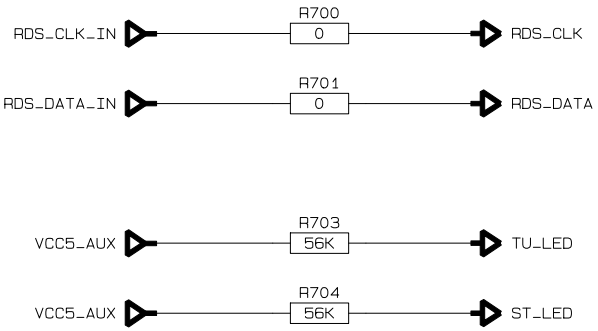
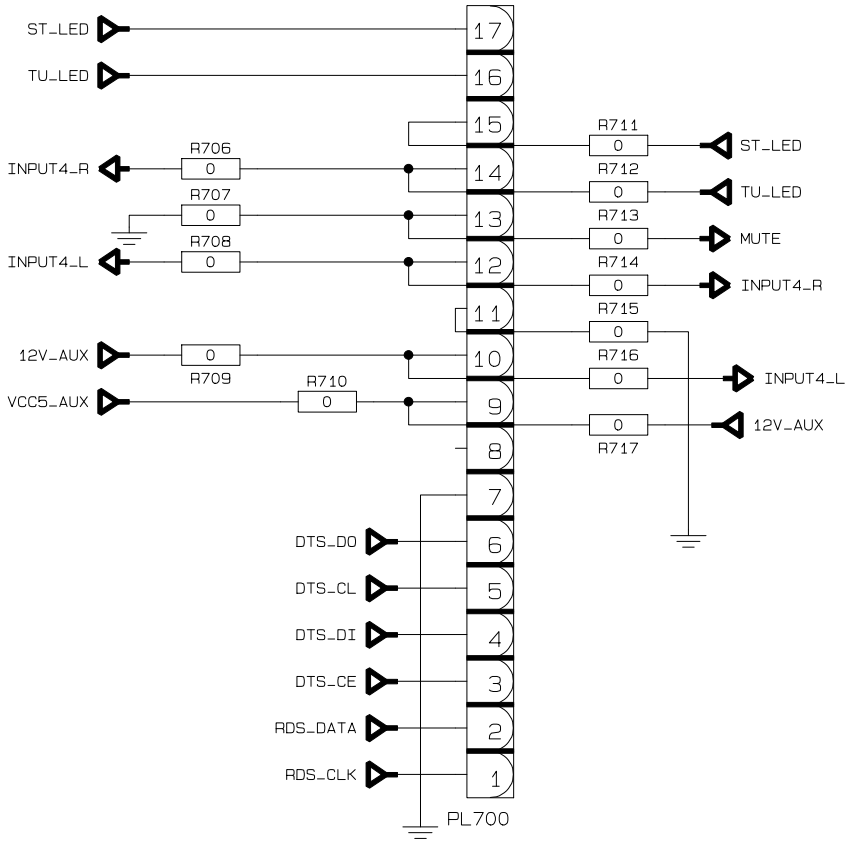
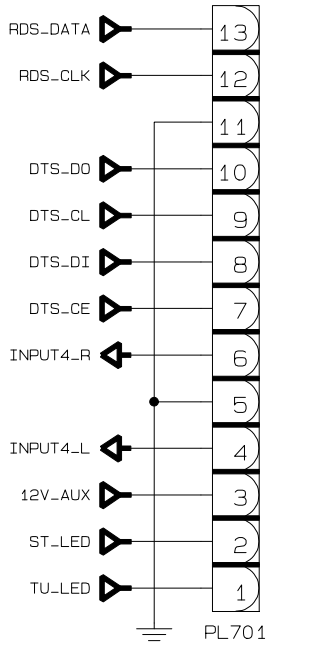




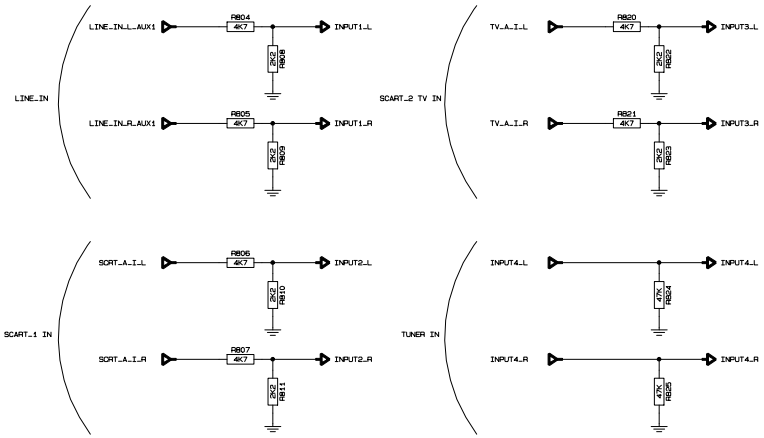
TBHK / PANASONIC TUNER OPTION

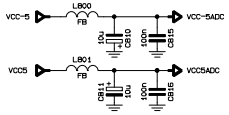


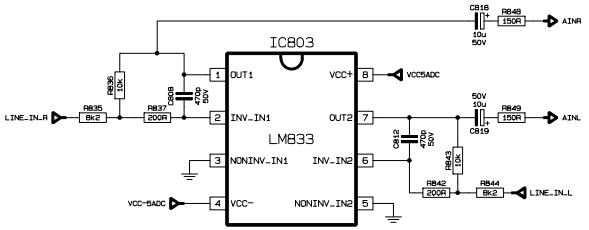
KST TUNER OPTION

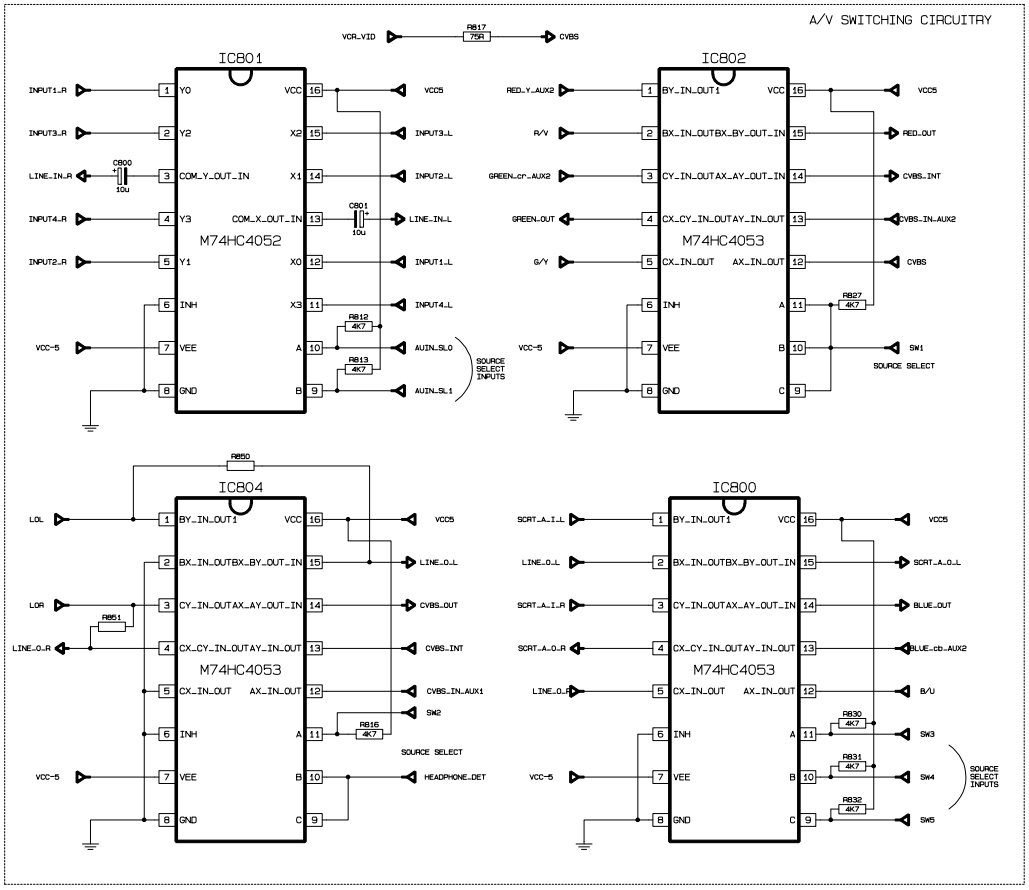
RESISTOR	PANASONIC	TBHK
R706	N. C.	JUMPER
R707	N. C.	JUMPER
R708	N. C.	JUMPER
R709	N. C.	JUMPER
R710	N. C.	JUMPER
R711	JUMPER	N. C.
R712	JUMPER	N. C.
R713	JUMPER	N. C.
R714	JUMPER	N. C.
R715	JUMPER	N. C.
R716	JUMPER	N. C.
R717	JUMPER	N. C.

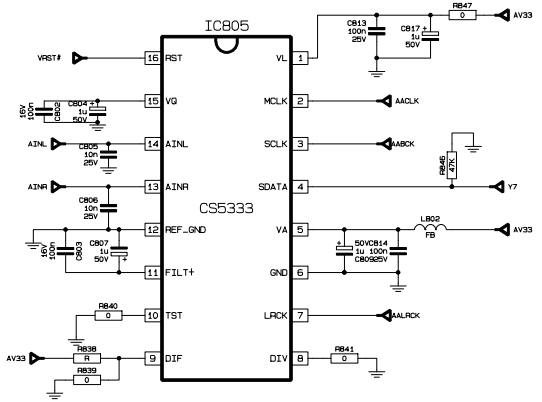
AV1300 MAIN BOARD SHEET 7
12MB14E4











AV 1300 MAIN BOARD SHEET 8
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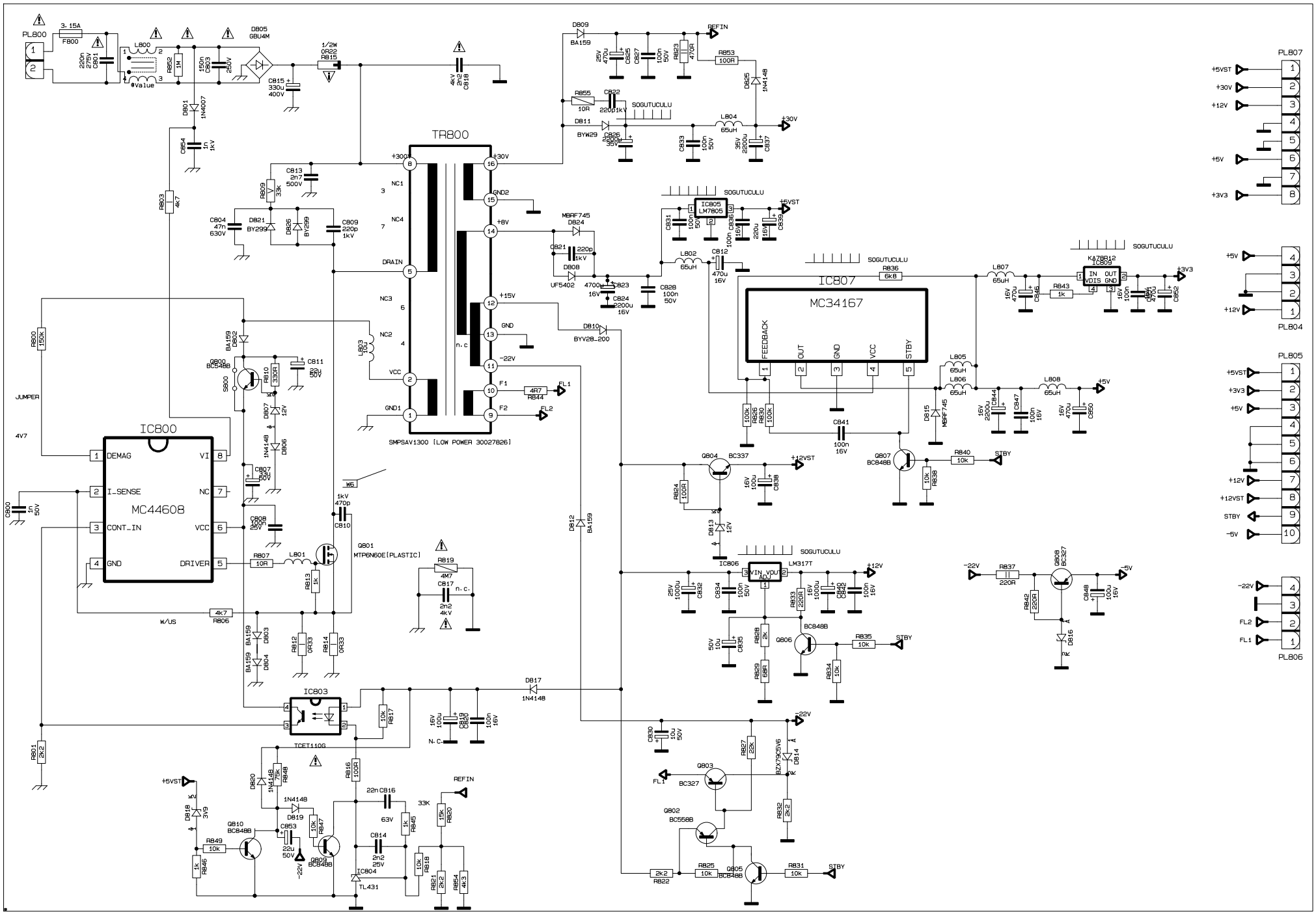
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L800
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D805
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C815
330u
400V
D801
1N4007
TR800
SMPSAV1300 [LOW POWER 30027826]
IC800
MC44608
DEMAG
I_SENSE
CONT_IN
GND
VI
NC
VCC
DRIVER
Q801
MTP6N60E[PLASTIC]
IC803
TCET110G
IC804
TL431
IC807
MC34167
FEEDBACK
OUT
GND
VCC
STBY
IC805
LM7805
IC806
LM317T
IC809
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BC337
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BA159
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D808
UF5402
D815
MBRF745
D816
1N4148
REFIN
SOGUTUCULU
JUMPER
W/US
W5
FL1
FL2
STBY
PL807
PL804
PL805
PL806
+5VST
+30V
+12V
+5V
+3V3
+12VST
-5V
-22V

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