JVC

SERVICE MANUAL

DVD DIGITAL THEATER SYSTEM

TH-A10

SP-PWA10

XV-THA10

SP-XSA10   SP-XCA10   SP-XSA10
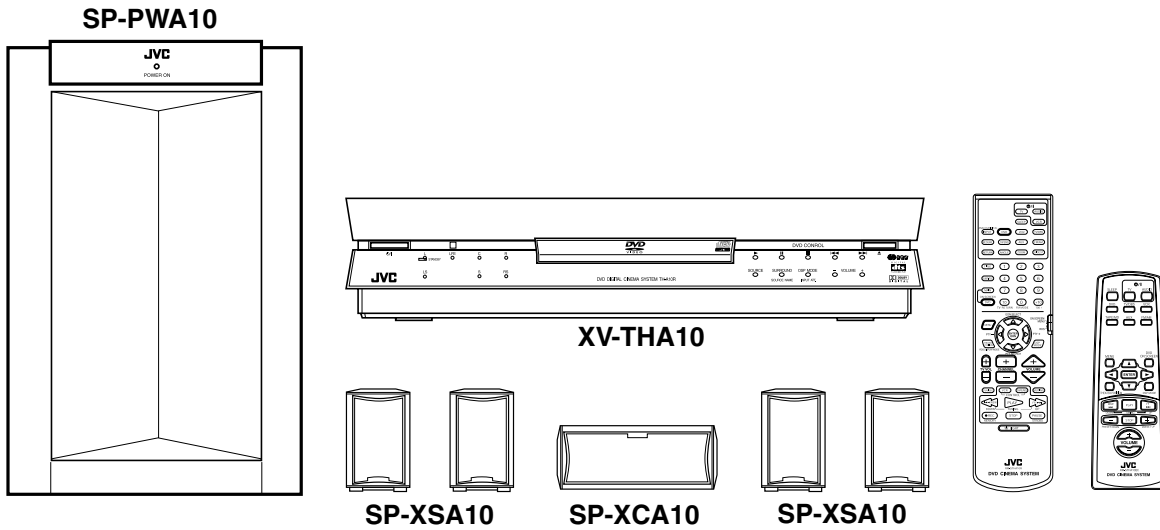
**Area Suffix
TH-A10**

3U ---- Maiaysia, Thailand,
Philippines
4U ---- Brazil, Mexico, Peru

TH-A10	(DVD player)/XV-TH-A10	
	SP-THA10 (Speaker section)	SP-PWA10 (Powered subwoofer)
		SP-XCA10 (Center speaker)
		SP-XSA10 (Satellite speaker) x 4

Contents

No.20890
JAN. 2001

Safety precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.

2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer`s warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.

3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.

4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.

5. Leakage currnet check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
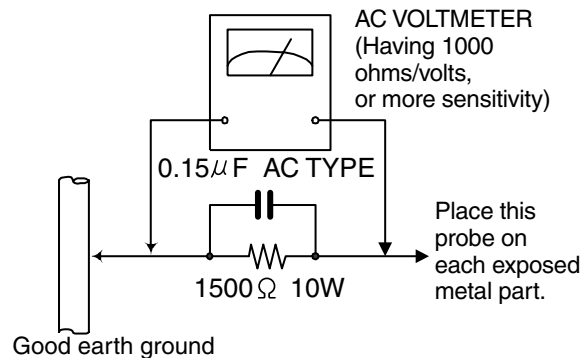   Do not use a line isolation transformer during this check.

   ● Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet , particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.)

   ● Alternate check method
   Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
   Measure the AC voltage across the resistor with the AC voltmeter.
   Move the resistor connection to eachexposed metal part, particularly any exposed metal part having a return path to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).

   AC VOLTMETER
   (Having 1000 ohms/volts, or more sensitivity)

   0.15μF AC TYPE

   1500Ω 10W

   Place this probe on each exposed metal part.

   Good earth ground

Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ *CAUTION* **Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.**

Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

## 1.1. Grounding to prevent damage by static electricity
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

1.1.1. Ground the workbench
1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

1.1.2. Ground yourself
1. Use an anti-static wrist strap to release any static electricity built up in your body.

(caption)
Anti-static wrist strap

1MΩ

Conductive material
(conductive sheet) or iron plate
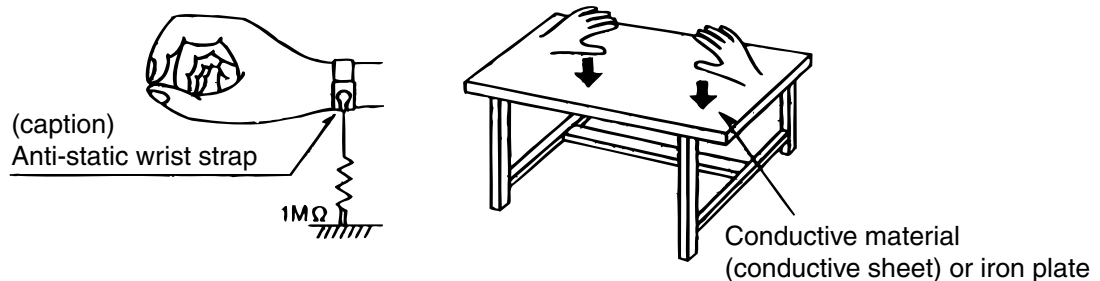
1.1.3. Handling the optical pickup
1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)

2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

1.2. Handling the traverse unit (optical pickup)
1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.

2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.

3. Handle the flexible cable carefully as it may break when subjected to strong force.

4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Dismantling and assembling the traverse unit

1. Notice regarding replacement of optical pickup

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs to the optical pickup or connected devices.

(Refer to the section regarding anti-static measures.)

1. Do not touch the area around the laser diode and actuator.

2. Do not check the laser diode using a tester, as the diode may easily be destroyed.

3. It is recommended that you use a grounded soldering iron when shorting or removing the laser diode.
   Recommended soldering iron: HAKKO ESD-compatible product

4. Solder the land on the optical pickup's flexible cable.
 ▪ Note : Short the land after shorting the terminal on the flexible cable using a clip, etc., when using an ungrounded soldering iron.
 ▪ Note : After shorting the laser diode according to the procedure above, remove the solder according to the text explanation.

Laser pick-up unit

Flexible cable

Short circuit land

Shorting

Shot with the rclip
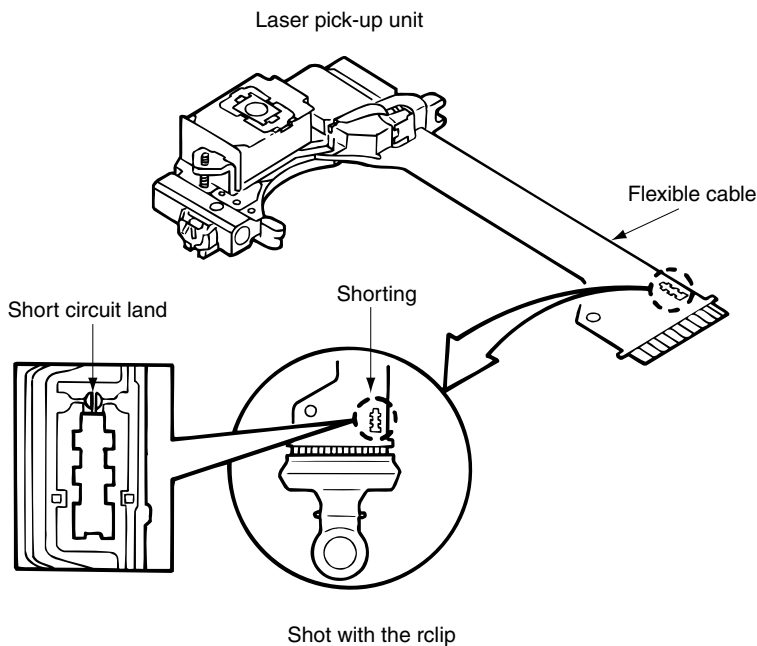
Disassembly method

<Main body>

■Removing the top cover
(See Fig.1 and 2)

1. Remove the four screws A attaching the top cover (Use an Allen wrench).

2. Lift up the front part of the top cover to release the two joints a and remove the top cover toward the front.

A   Top cover

A

Joints a
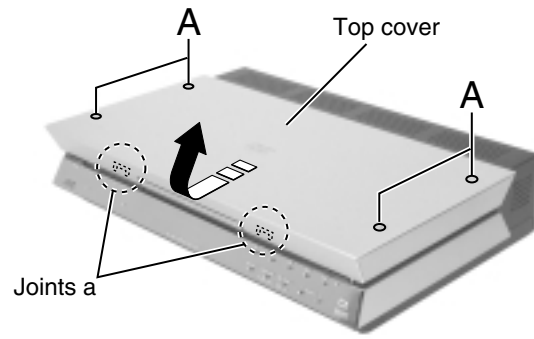
Fig.1

■Removing the rear cover (See Fig. 3)

・ Prior to performing the following procedure, remove the top cover.

1. Remove the four screws B attaching the rear cover on the back of the body. Pull out the rear cover backward.

Top cover

Joint a

Fig.2

■Removing the right and left side covers
(See Fig. 4 and 5)

・ Prior to performing the following procedure, remove the top cover and the rear cover.

1. Move the left side cover backward to release the five joint hooks b and remove the left side cover outward.

2. Remove the right side cover in the same way.

B   Rear cover   B

B   B

Fig.3

Right side cover

Joints b

Fig.5

Left side cover

Joints b
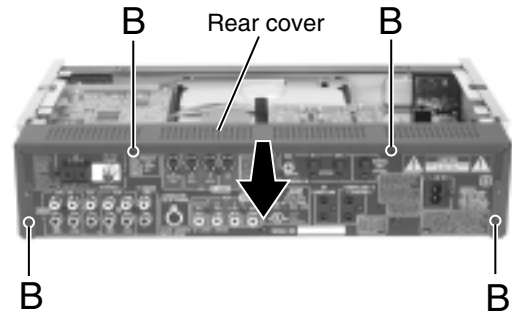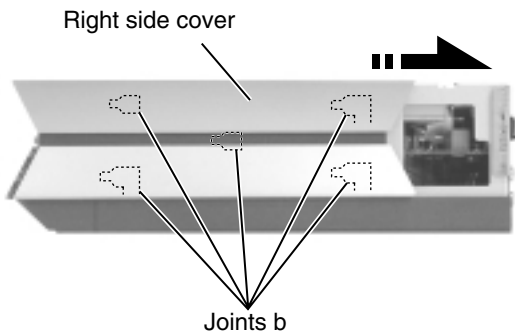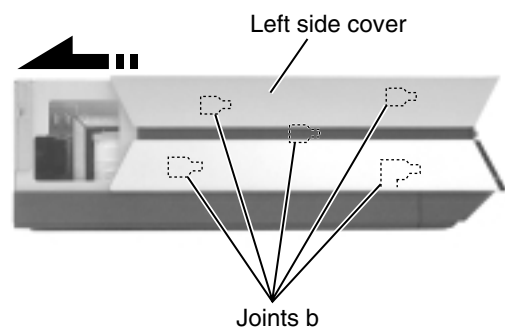
Fig.4

■Removing the front panel assembly
(See Fig. 6 to 9)

・ Prior to performing the following procedure, remove the top cover, the rear cover and the side covers.

1. Disconnect the harness from connector CN802 on the main board on the upper side of the body.

2. Remove the two screws C on the upper side of the body.

3. Remove the three screws D on the bottom of the body.

4. Release the five joints c and detach the front panel assembly toward the front.

C
Joint c
Joint c
CN802
C
Front panel assembly

Fig.6

D
Front panel assembly
Joint c
D

Fig.7

Joint c

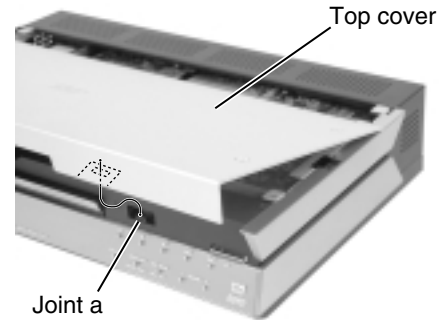Front panel assembly

Fig.9

Joint c
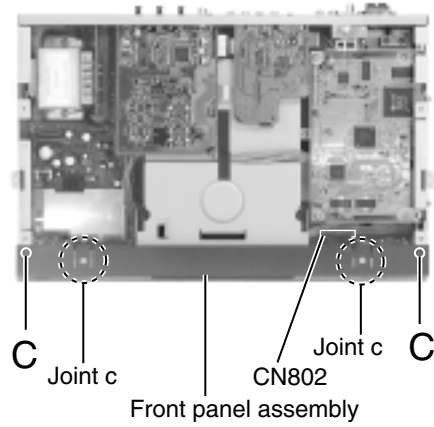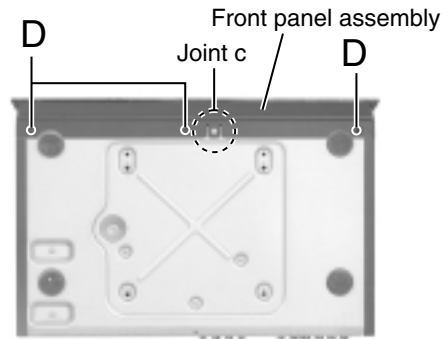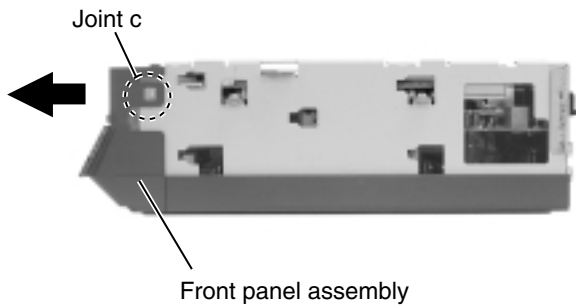
Front panel assembly
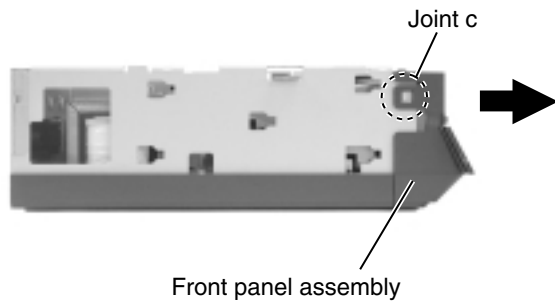
Fig.8

■Removing the right and left corner covers (See Fig.10 and 11)

・Prior to performing the following procedure, remove the top cover, the rear cover, the side covers and the front panel assembly.

・It is not necessary to remove the front panel assembly.

1. Move the left corner cover backward to release the three joint hooks d.

2. Remove the right corner cover in the same way.

Joint d   Left corner cover   Joints d
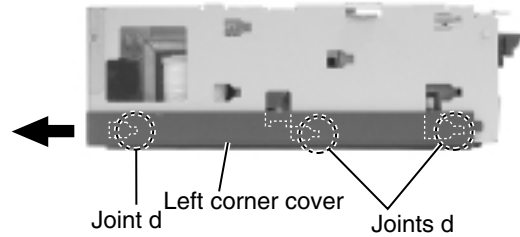
Fig.10

■Removing the rear panel
(See Fig.12 to 14)

・Prior to performing the following procedure, remove the top cover and the rear cover.

1. Remove the eighteen screws E and the one screw F attaching the rear panel.

2. Release the two joints e on both sides of the body.

Joints d   Joint d
Right corner cover

Fig.11

E   E   E   Rear panel   E

E   F   E   E

Fig.12

Joint e

Rear panel

Fig.12

Joint e

Rear panel
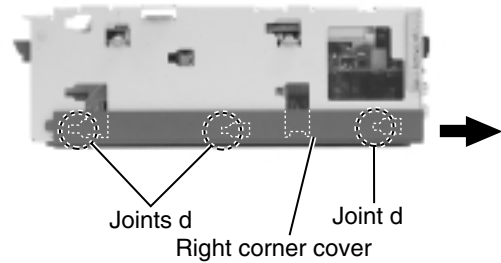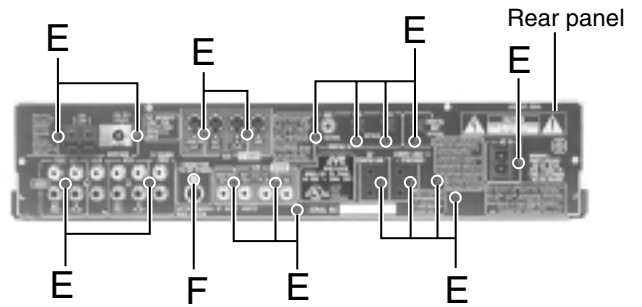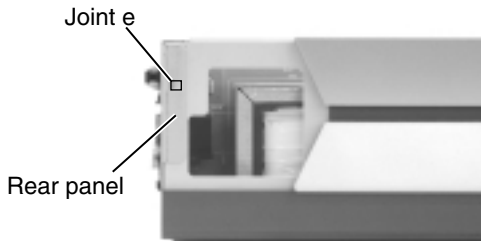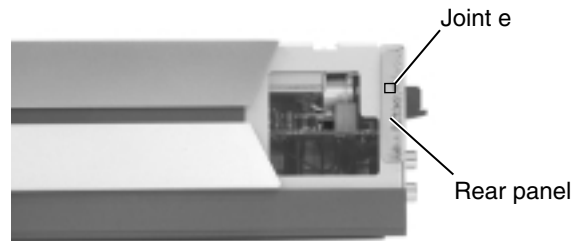
Fig.12

■Removing the DVD servo control board (See Fig.15 to 17)

・Prior to performing the following procedure, remcover and the right side cover.ove the top cover, the rear

1. Remove the three screws G and pull the DVD servo control board case upward.

2. Disconnect the harness from connector CN501 and CN503, and the card wire from CN101, CN103 and CN502 of the DVD servo control board on the underside of the DVD servo control board case.

3. Remove the four screws H attaching the DVD servo control board.

Digital I / O board

CN681

Analog I / O board

CN201

G

CN687   DVD servo control board (case)

Fig.15

CN501   CN503   CN502

DVD servo control board case   CN103   CN101

Fig.16

H   H

DVD servo control board

H

DVD servo control board case   H

Fig.17
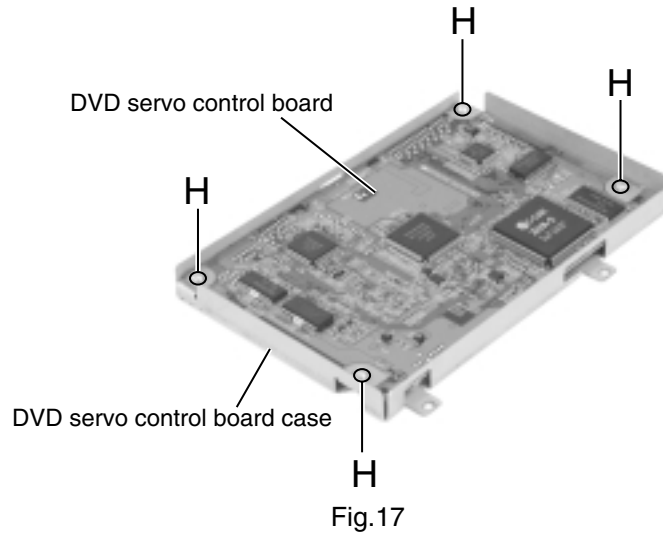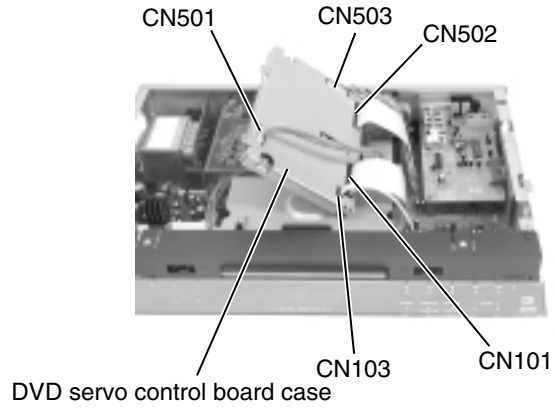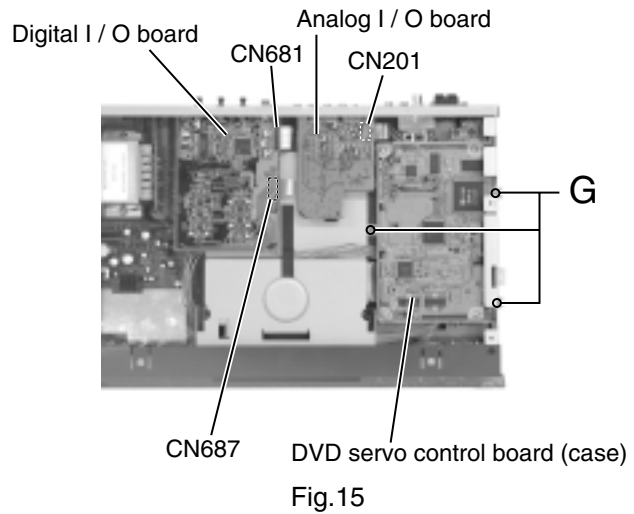
■Removing the analog I / O board / the digital I / O board (See Fig.18 and 19)

・ Prior to performing the following procedure, remove the top cover and the rear cover.

1. Remove the two screws E attaching the analog I / O board on the back of the body.

2. Disconnect the card wire from connector CN201 on the analog I / O board.

3. Remove the four screws E attaching the digital I / O board on the back of the body.

4. Disconnect the card wire from connector CN681 and CN687 on the digital I / O board.
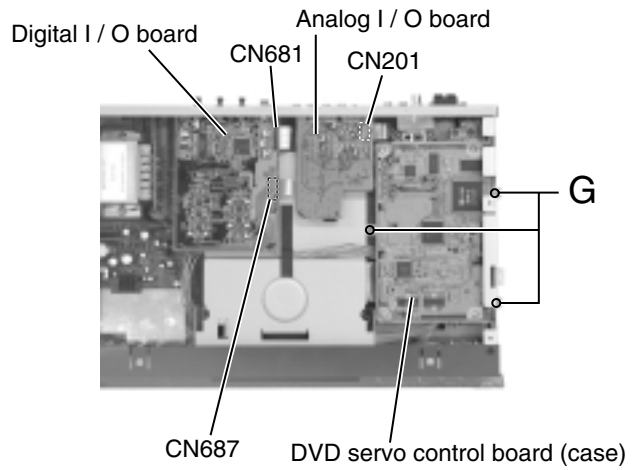
Fig.18

■Removing the tuner board / the sub board (See Fig.20 and 21)

・ Prior to performing the following procedure, remove the top cover, the rear cover and the DVD servo control board case.

1. Remove the two screws E attaching the tuner board on the back of the body.

2. Disconnect connector CN111 on the tuner board from the sub board.

3. Disconnect connector CN131 on the sub board from the main board.
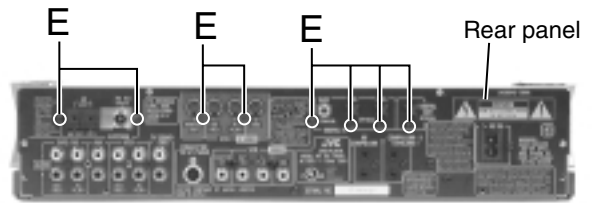
Fig.19
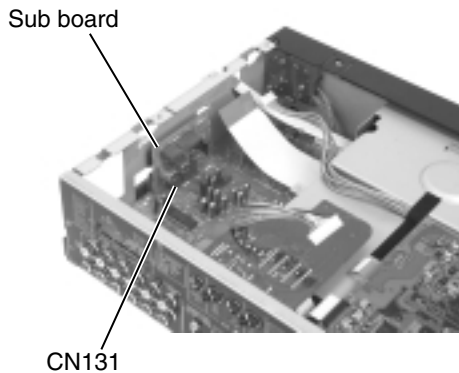
Fig.21
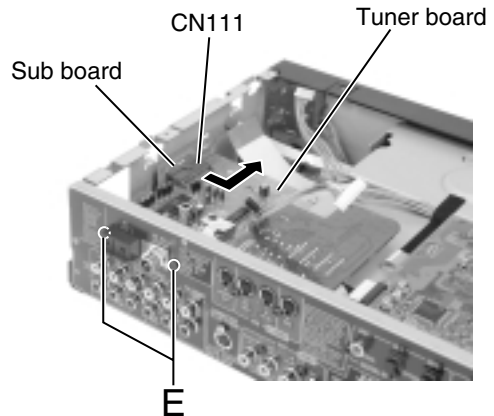
Fig.20

■Removing the DVD mechanism assembly
(See Fig.22 and 23)

・ Prior to performing the following procedure, remove the top cover, the rear cover, the front panel assembly, the DVD servo control board case, the analog I / O board, the digital I / O board and the tuner board.

1. Disconnect the harnesses from the spacer on the upper side of the DVD mechanism cover.

2. Remove the two screws I and the one screw J attaching the DVD mechanism cover.

3. Remove the two screws K attaching the DVD mechanism assembly.

4. Remove the DVD mechanism assembly upward while pulling it backward.

DVD mechanism cover

K   J   K

I   Spacer   I

Fig.22

DVD mechanism assembly
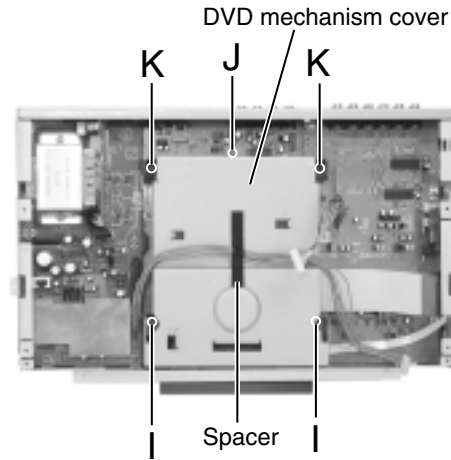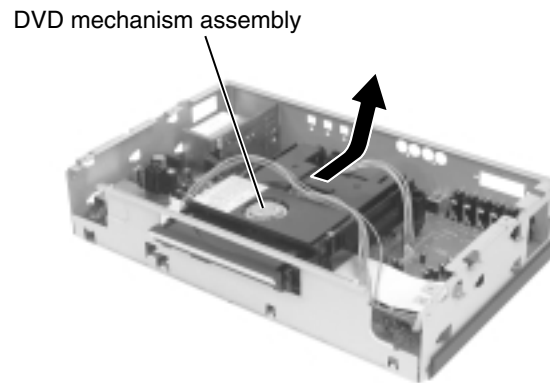
Fig.23

■Removing the power board
(See Fig.24 and 25)

・ Prior to performing the following procedure, remove the top cover, the rear cover, the front panel assembly, the DVD servo control board case and the digital I / O board.

1. Disconnect the harness from the spacer on the upper side of the DVD mechanism cover.

2. Remove the two screws E attaching the power board on the back of the body.

3. Disconnect the harness from connector CN911 and CN912 on the power board.

4. Remove the four screws L attaching the power board.

5. Disconnect connector CN913 and CN914 of the power board from the main board by pulling out them respectively.

Rear panel

E   E

Fig.24

Power transformer assembly

CN911,CN912

L

M

L

Power board

CN914   CN913   Spacer

L
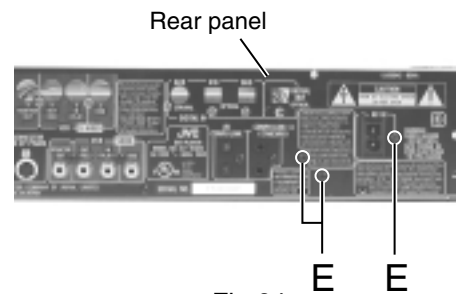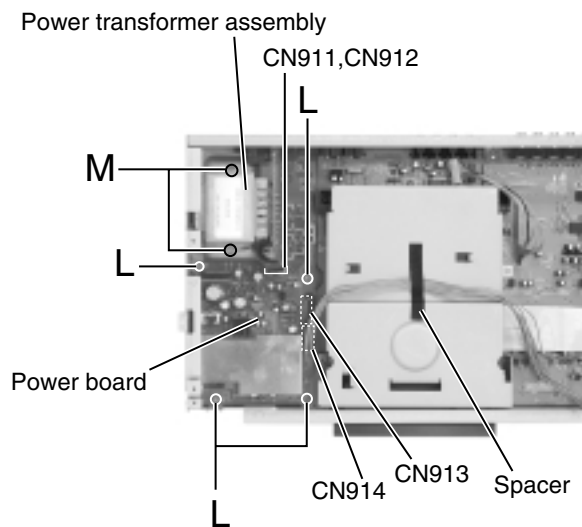
Fig.25

■Removing the power transformer assembly (See Fig.24 and 25)

・ Prior to performing the following procedures, remove the top cover and the rear cover.

1. Disconnect the harnesses from connector CN911 and CN912 on the power board.

2. Remove the two screws M attaching the power transformer assembly.

3. Remove the screw E attaching the power transformer assembly on the back of the body.
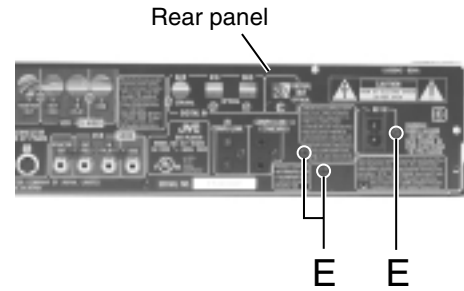
■Removing the main board (See Fig.26)

・ Prior to performing the following procedure, remove the top cover, the rear cover, the front panel assembly, the rear panel, the DVD mechanism assembly, the power board and the sub board.

1. Remove the four DVD spacers on the upper side of the main board.

2. Remove the five screws N attaching the main board.
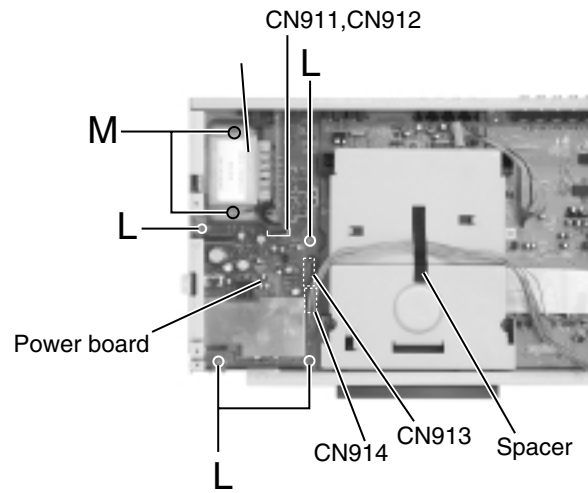
<Front panel assembly>

・ Prior to performing the following procedure, remove the top cover, the rear cover, the side covers and the front panel assembly.

■Removing the power switch board (See Fig.27)

1. Dithe harness from connector CN705 on the power switch board.sconnect

2. Remove the three screws O attaching the power switch board.

Rear panel

Fig.24

CN911,CN912

M

L

L

Power board

CN914 CN913 Spacer

Fig.25

Mainboard

N

N

N

N

Fig.26

IC board R CN706 Power switch board

O

O

S LED board
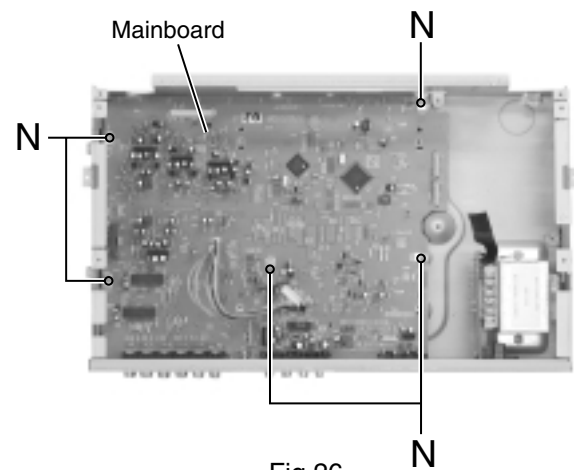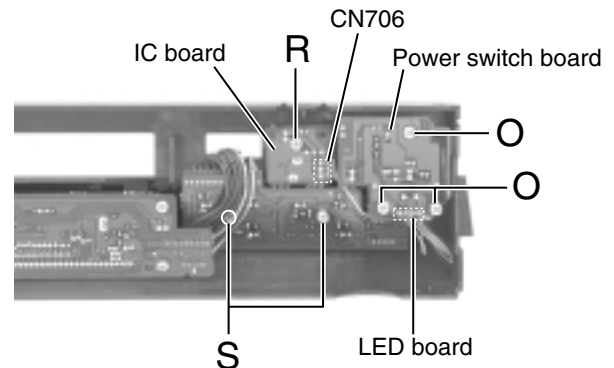
Fig.27

■Removing the eject board (See Fig.28)

1. Disconnect the harness from connector CN702 on the eject board.

2. Remove the three screws P attaching the eject board.

Eject board   Switch board

P

CN702

T
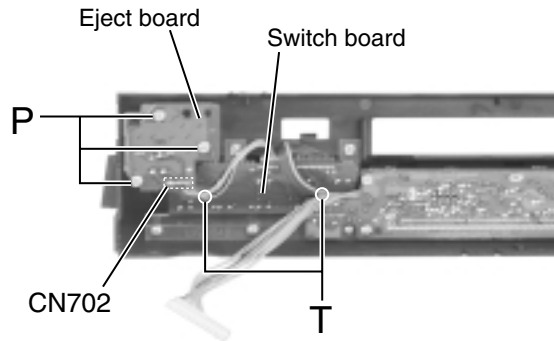
Fig.28

■Removing the LCD board (See Fig.29)

1. Remove the four screws Q attaching the LCD board.

2. Unsolder WA701, WA703 and WA704 on the LCD board.
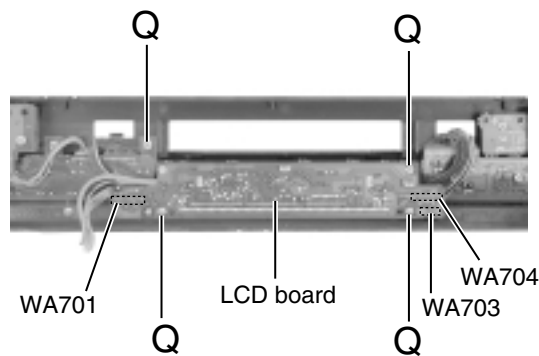
■Removing the IC board (See Fig.27)

1. Remove the screw R attaching the IC board.

2. Disconnect the harness from connector CN706 on the IC board.

Q   Q

WA701   LCD board   WA704
                        WA703
Q   Q

Fig.29

■Removing the LED board (See Fig.27)

· Prior to performing the following procedure, remove the LCD board and the IC board.

1. Disconnect the harness from connector CN705 on the power switch board.

2. Remove the two screws S attaching the LED board.

CN706
IC board   R   Power switch board
                              O
                              O

S   LED board
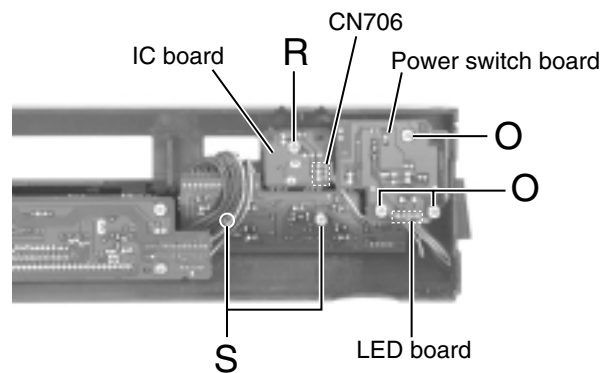
Fig.27

■Removing the switch board (See Fig.28)

· Prior to performing the following procedure, remove the LCD board.

1. Disconnect the harness from connector CN702 on the eject board.

2. Remove the two screws T attaching the switch board.

<Removing DVD mechanism unit>

■ **Removing the clamper base** (refer to Figure 1)

 o Remove the top cover.

 o Remove the DVD mechanism unit.

1. Remove the two screws at A fixing the clamper base.
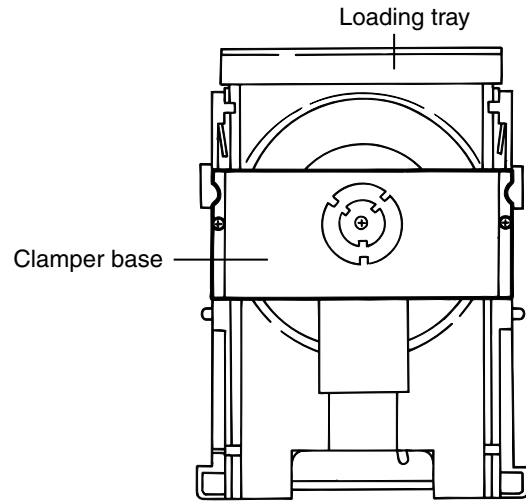
■ **Removing the loading tray** (refer to Figures 2 - 4)

 o Remove the clamper base.

1. Turn the up-down cam lever clockwise (in the direction of the arrow in Figure 2) to lower the position of the mechanism.

2. Manually set the loading tray to the fully-open position.

3. Stretch the tray stoppers on both sides of the loading base outward and pull out the tray.

Loading tray

Clamper base

Figure 1

Loading tray (front side)

Loading base

Up-down cam

Lever

Figure 2

Tray stopper

Loading tray

Loading base

Tray stopper

Figure 4

Loading tray

Push

Push
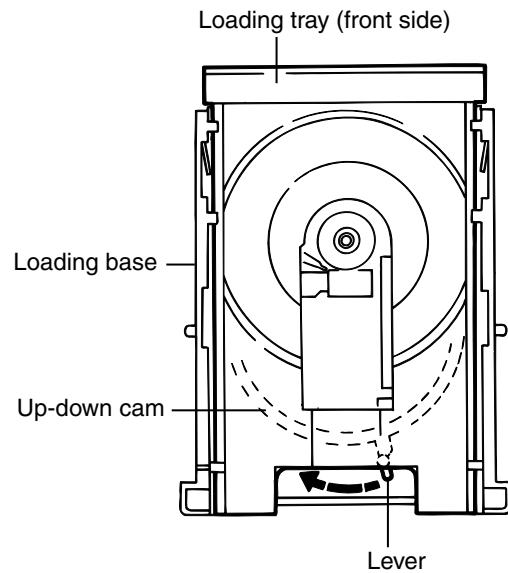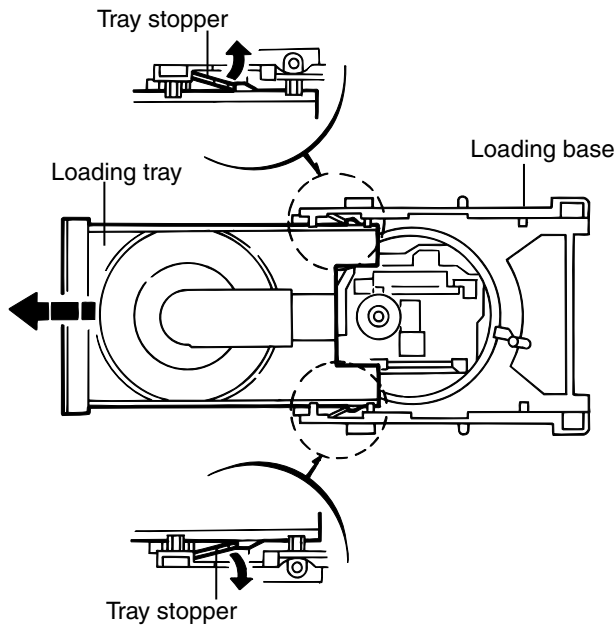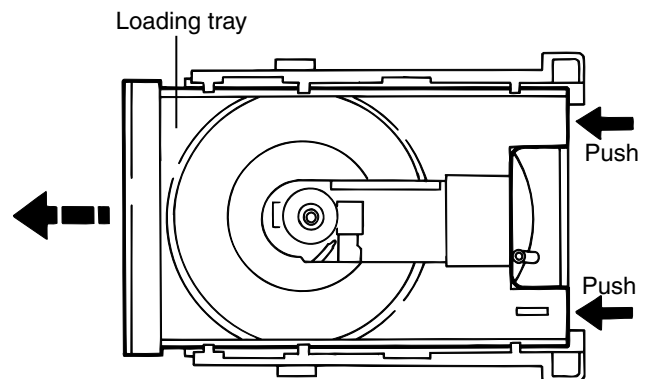
Figure 3

■ **Removing the traverse mechanism unit** (refer to Figure 5)

o Remove the loading tray.

1. Remove the three screws at B fixing the traverse mechanism unit.

■ **Protecting the optical pickup**

o Solder the flexible ground point on the optical pickup when replacing the pickup or before detaching the mechanism control board. When assembling the unit, remove the solder last.

■ **Removing the mechanism control board**
 (refer to Figures 6 - 7)

o Remove the traverse unit. (Can be detached without detaching the T-mechanism unit.)

1. Remove the two screws at C fixing the mechanism control base from the bottom of the traverse unit.
2. Pull out the CN12 connector and detach the mechanism control board.
3. Remove the card wire from the CN13 connector on the mechanism control board.
4. Pull out the FPC holder from the CN12 connector on the reverse side of the mechanism control board and remove the flexible harness, referring to Figure 7.

Traverse mechanism unit

B

B

B

Figure 5

Traverse mechanism unit

CN12

Enlargement

C

CN13

Connection area
(Solder the flexible
ground point)

Mechanism control board

Figure 6

Flexible harness

3

Flexible harness

Enlargement

FPC holder

2

1

CN12
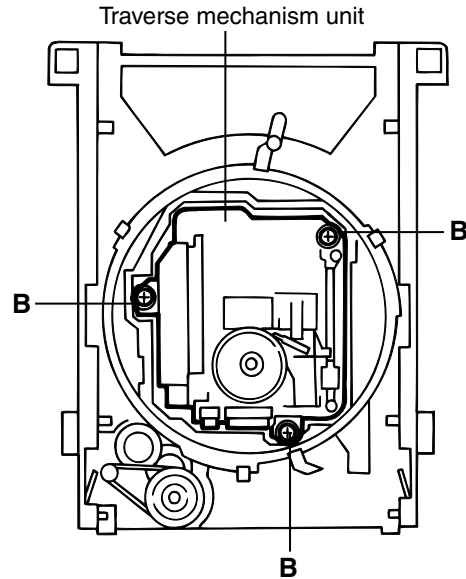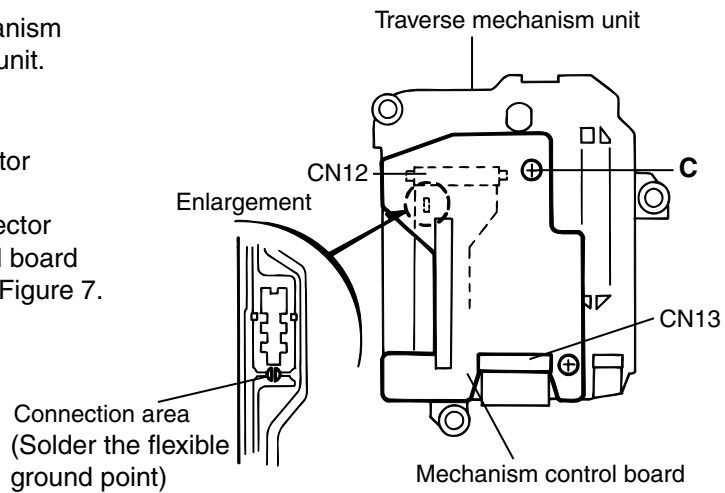
Figure 7
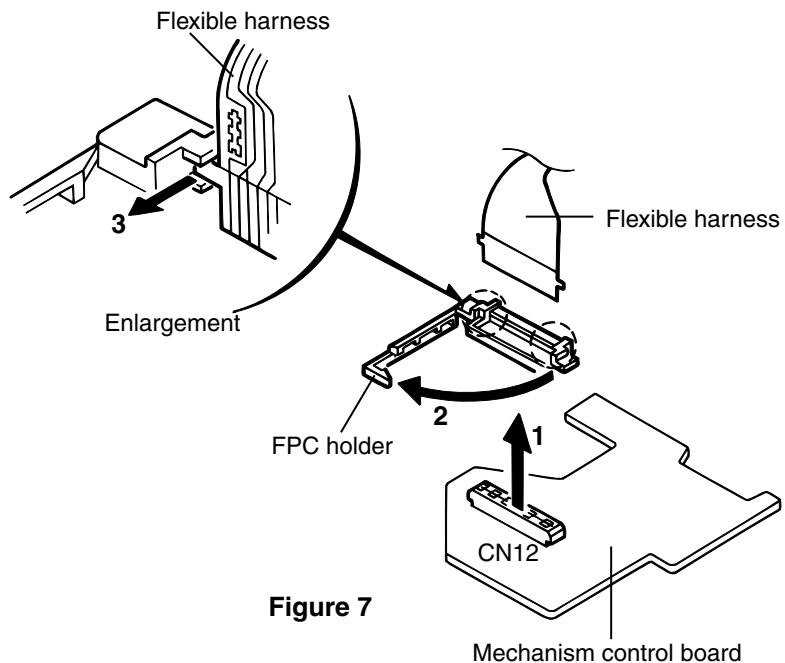
Mechanism control board

■ **Removeing the turntable and spindle motor assemby**
(refer to Figures 8 - 9)

o Remove the traverse mechanism unit.

o Solder the flexible ground point on the optical pickup.
(Figure 6)

o Remove the mechanism control board.

1. Remove the flexible harness from the feed motor
connector on the spindle motor board assembly.
2. Remove the three screws at D fixing the spindle motor
from the bottom of the traverse chassis.
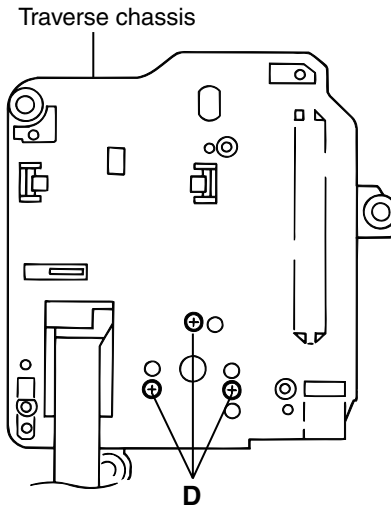
■ **Removing the feed motor unit** (refer to Figure 9)

o Remove the traverse mechanism unit.

o Remove the mechanism control board.

1. Remove the FPC from the feed motor connector
on the turntable spindle motor board.
2. Remove the two screws at E fixing the feed motor unit.

■ **Removing the optical pickup unit** (refer to Figure 9)

o Remove the traverse mechanism unit.

o Remove the mechanism control board.

o Remove the feed motor unit.

1. Remove the screw at F fixing the guide shaft holder at B,
then simultaneously remove the guide shaft at B and the
optical pickup unit. While doing so, slide the unit
horizontally away from the guide shaft at A.

Traverse chassis

D

Figure 8

Traverse mechanism unit

F

Guide shaft B

Pick-up assembly

E

Guide shaft A

E

Feed motor assembly

Flexible harness

Turn table spindle motor unit

Feed motor connector
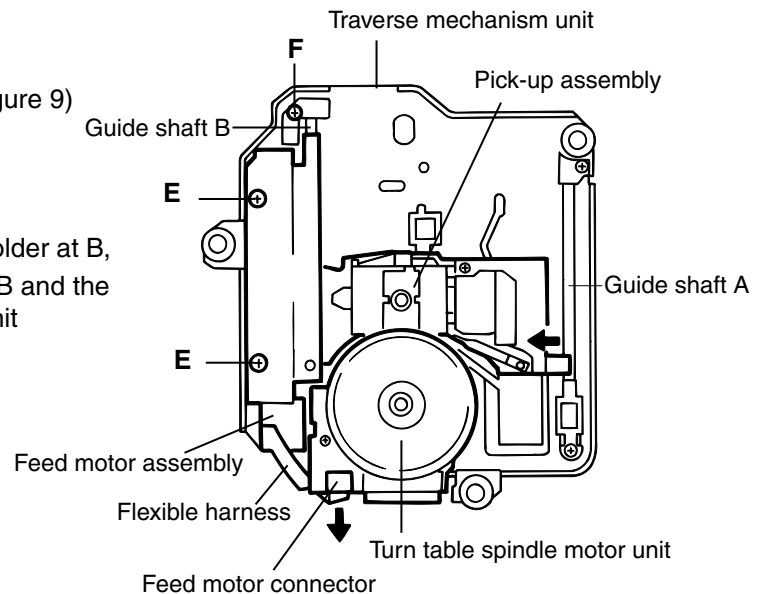
Figure 9

■ **Removeing the loading mechanism parts**
(refer to Figures 10 - 11)

o Remove the clamper base.

o Remove the disk tray.

1. Turn the lever counterclockwise until it stops (position 1), while pushing the switch lever in the direction of the arrow and pushing up the pawl at A using a screwdriver.
2. Stretch the two pawls at B outward using a screwdriver and remove the chassis.
3. Turn the lever clockwise (position 2) to remove the up-down cam.
4. Remove the pulley gear and the pulley gear belt after removing the screw at G fixing the pulley gear.
5. Pull out drive gear 2 then drive gear 1.
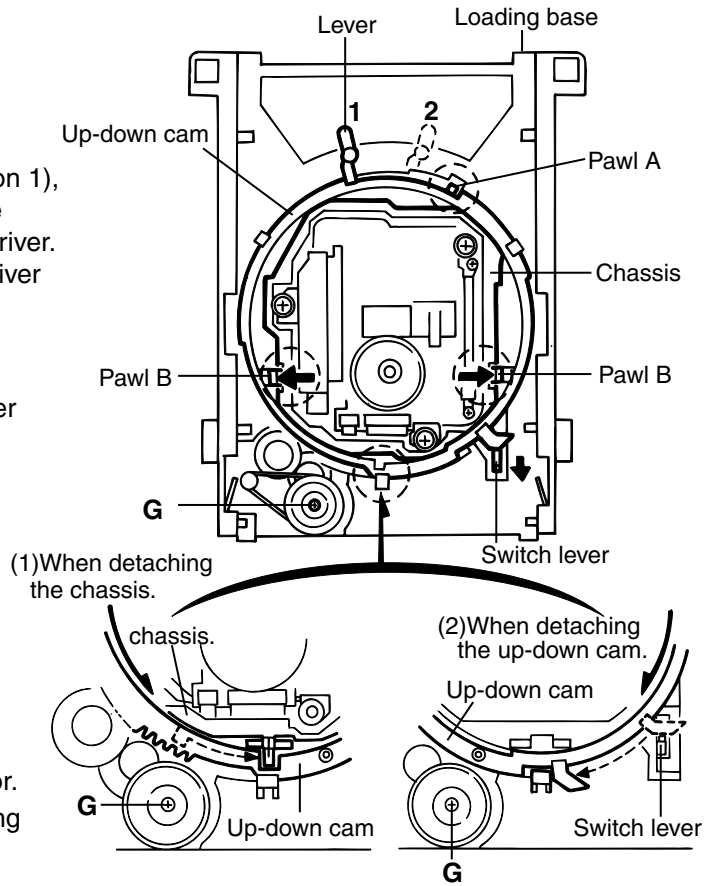
■ **Removing the loading motor board**
(refer to Figures 11 - 12)

o Remove the clamper base.

o Remove the disk tray.

1. Remove the loading belt.
2. Remove the two screws at H fixing the loading motor.
3. Remove the screw at I and the three pawls at C fixing the loading motor base from the reverse side of the loading base.

Lever Loading base

Up-down cam

1 **2**

Pawl A

Chassis

Pawl B Pawl B

G

Switch lever

(1)When detaching the chassis.

chassis.

(2)When detaching the up-down cam.

Up-down cam

G Up-down cam

Switch lever

G

Figure 10

Drive gear 1

Drive gear 2

H

Loading motor unit

H

G

Loading base Loading belt Pulley gear

Figure 11

Loading base Loading motor board

I

Pawl C
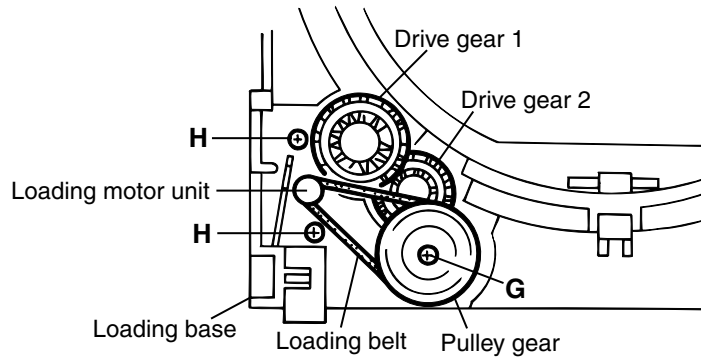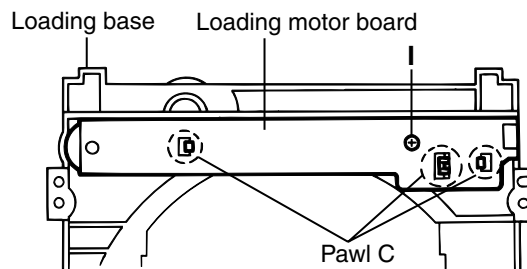
Figure 12

Disassembly method

<Speaker>

■Removing the amplifier assembly
(See Fig.1)

1. Remove the twelve screws A attaching the amplifier assembly on the back of the body.

2. Move the amplifier assembly backward and disconnect the harness from connector CN109 in the lower part of the amplifier assembly.
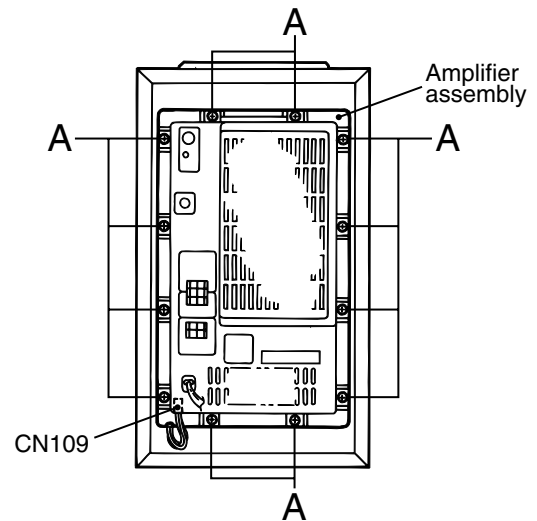
Fig.1

■Removing the heat sink cover and the amplifier cover (See Fig.2 and 3)

・ Prior to performing the following procedure, remove the amplifier assembly.

1. Pull out the volume knob.

2. Remove the four screws B attaching the heat sink cover.

3. Remove the twenty screws C and the one screw D attaching the amplifier cover.
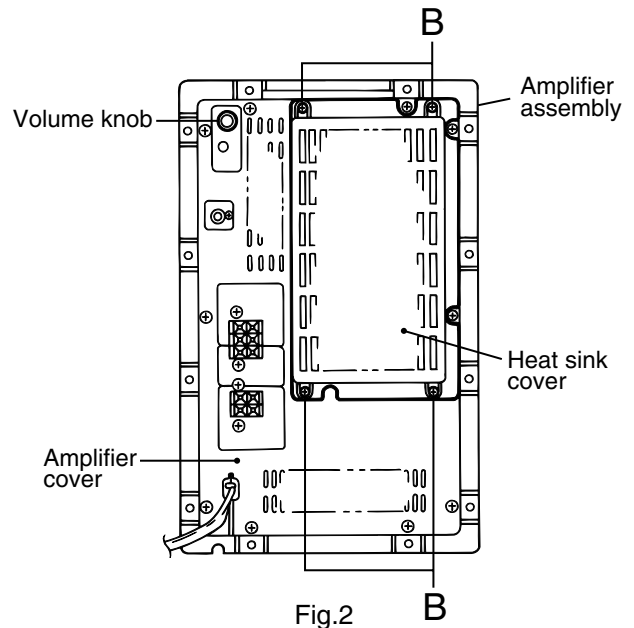
Fig.2
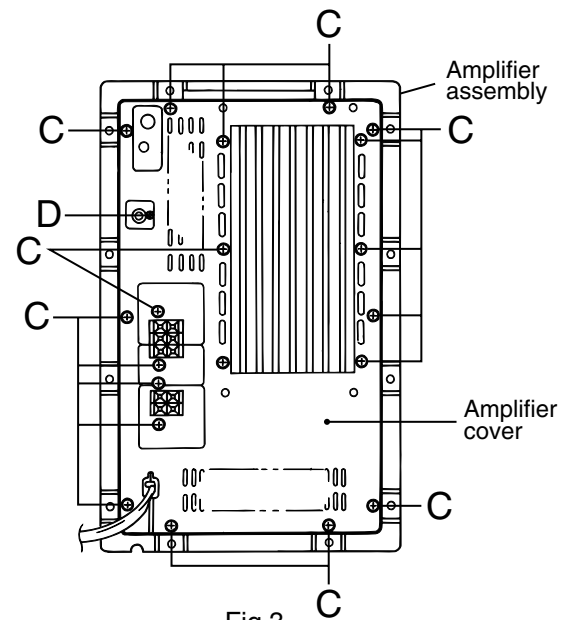
Fig.3

■Removing the preamplifier board (See Fig.4 to 6)

・ Prior to performing the following procedure, remove the heat sink cover and the amplifier cover.

1. Remove the two screws E attaching the preamplifier board to the bracket.

2. Disconnect connector CN201 on the preamplifier board from the main amplifier board.

3. Pull out the switch knob.

4. Remove the nut and the two screws F attaching the bracket.
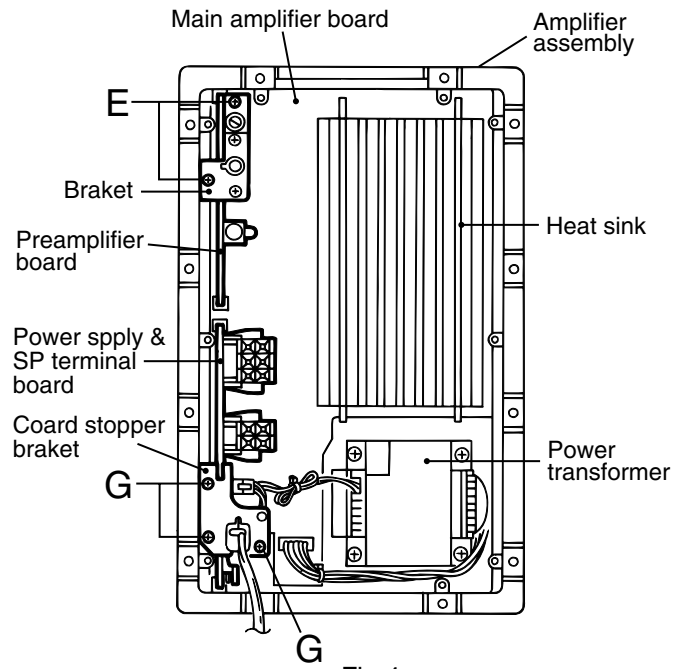
Fig.4

■Removing the power spply & SP terminal board (See Fig.4and 5)

・ Prior to performing the following procedure, remove the heat sink cover and the amplifier cover.

1. Remove the three screws G attaching the coard stopper braket.

2. Disconnect connector CN210 and CN211 on the power spply & SP terminal board from the main amplifier board.

3. Disconnect the power cord from connector CN108 on the power spply & SP terminal board and the harness from CN107.
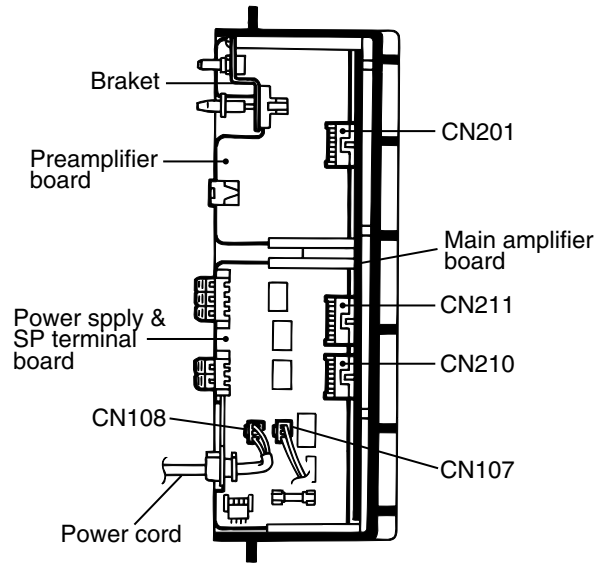
Fig.5
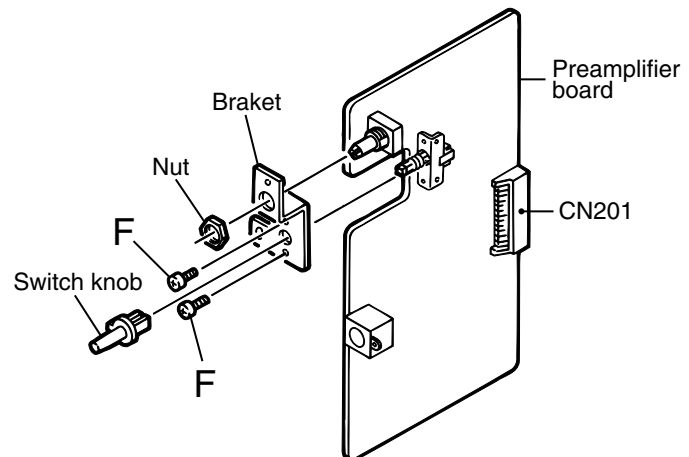
Fig.6

■Removing the Power Amplifier Board(See Fig.7 and 8)

・ Prior to performing the following procedure, remove the heat sink cover, the amplifier cover, the preamplifier board and the power spply & SP terminal board.

1. Disconnect the harness from connector CN104 on the power amplifier board.

2. Remove the six screws H and the power amplifier board with the heat sink.

3. Remove the two screws I attaching the power amplifier board (A) and the two screws J attaching the power amplifier board (B) on the underside of the power amplifier board.

4. Disconnect connector CN102 and CN103 on the power amplifier board (A) and CN105 and CN106 on the power amplifier board (B) from the power amplifier board respectively.
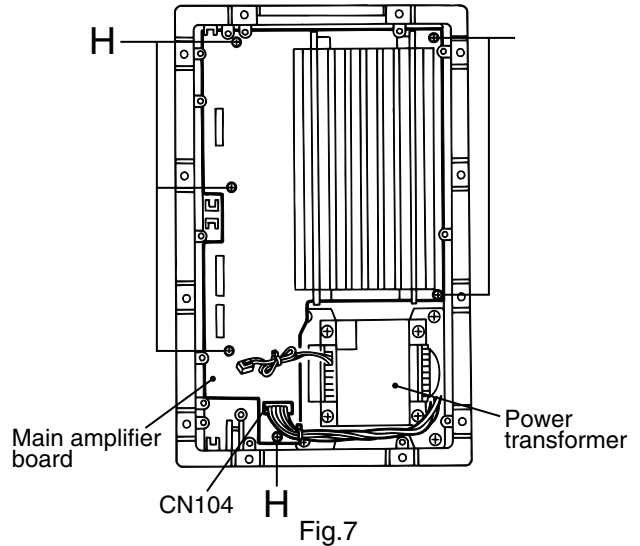
■Removing the power amplifier board (A) (See Fig.9 and 10)

・ Prior to performing the following procedure, remove the heat sink cover, the amplifier cover, the preamplifier board, the power spply & SP terminal board and the power amplifier board.

1. Remove the four screws K attaching the power amplifier board (A) to the heat sink.

2. Release the four joint hooks a bent and attached to the outside of the power amplifier board (A).

3. Move the power amplifier board (A) in the direction of the arrow to release joint b and remove the power amplifier board (A) from the bracket (A).

Fig.7

Fig.8

Fig.9

Fig.10
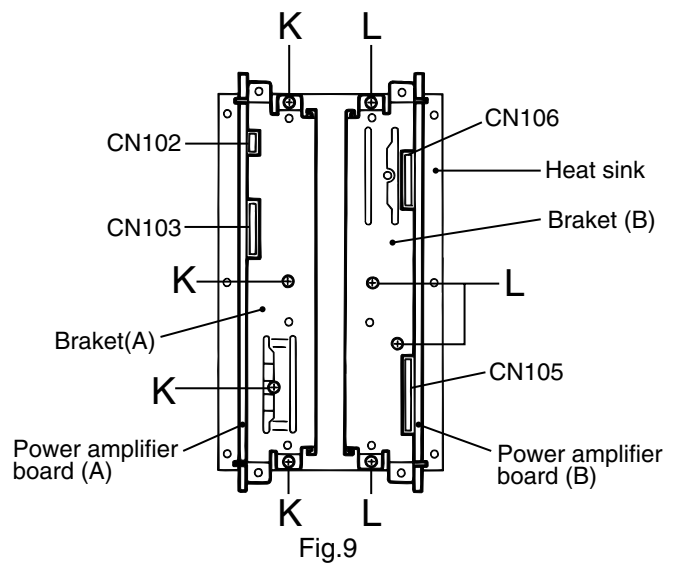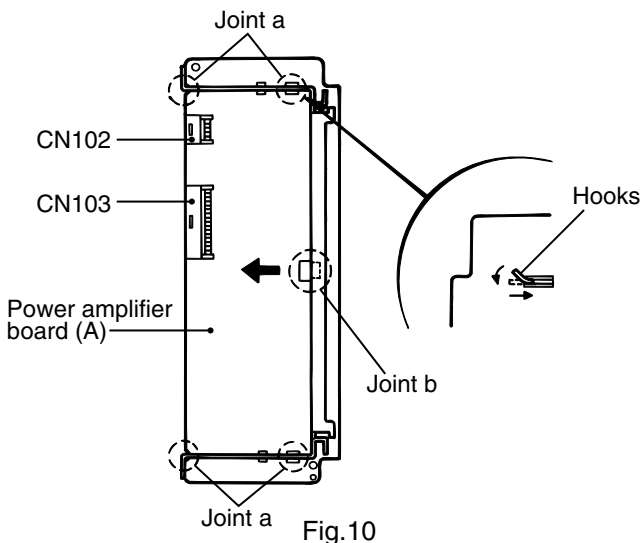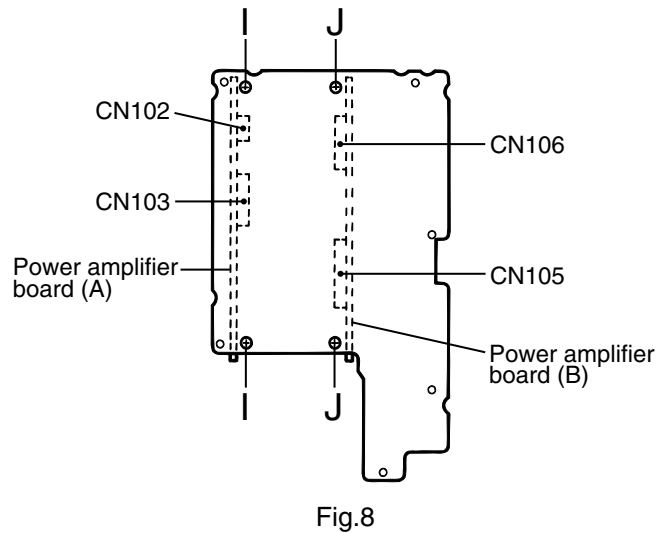
■Removing the power amplifier board (B) (See Fig.9 and 11)

・ Prior to performing the following procedure, remove the heat sink cover, the amplifier cover, the preamplifier board, the power spply & SP terminal board and the main amplifier board.

1. Remove the four screws L attaching the power amplifier board (B) to the heat sink.

2. Release the four joint hooks c bent and attached to the outside of the power amplifier board (B).

3. Move the power amplifier board (B) in the direction of the arrow to release joint d and remove the power amplifier board (B) from the bracket (B).
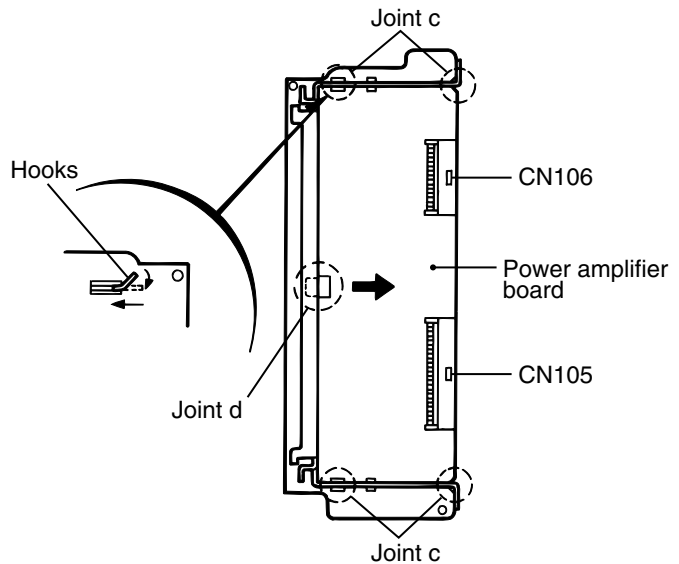
Fig.11

■Removing the power transformer (See Fig.12 and 13)

・ Prior to performing the following procedure, remove the amplifier cover.

1. Disconnect the harness from connector CN104 on the main amplifier board.

2. Disconnect the harness from connector CN107 on the power spply & SP terminal board.

3. Remove the four screws M attaching the power transformer.
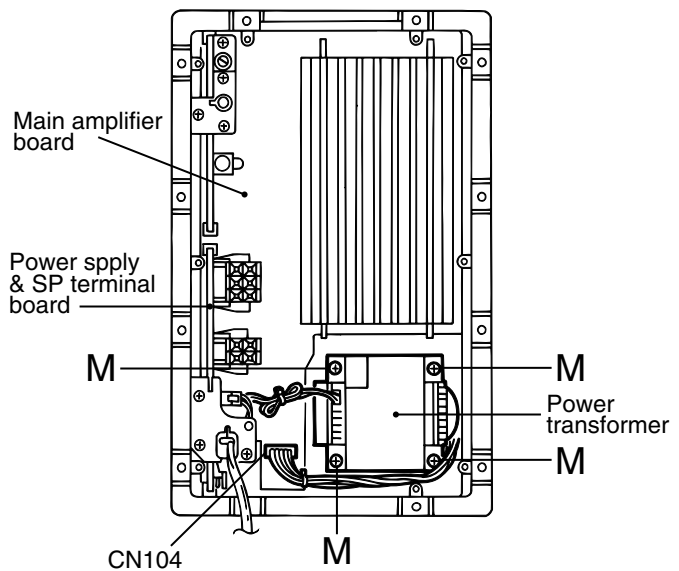
Fig.12
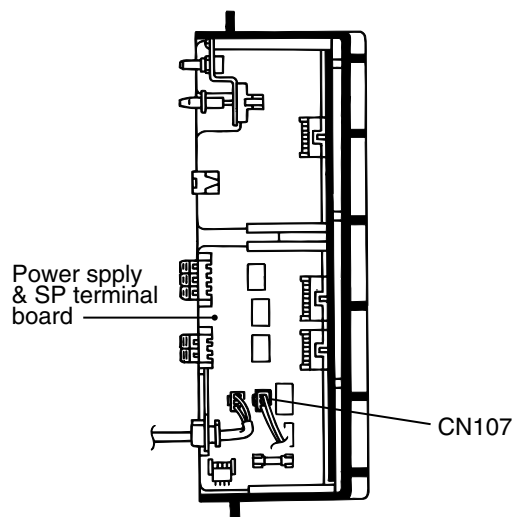
Fig.13

Main adjustment

Adjustment and confirmation matter

(1) Auto adjustment method

If microprocessor (IC401, IC402, IC714, IC716) or DVD Prek-up is replaced, initialize the DVD player in the following matter:

1. Initialize the DVD player in the following matter:

   1) Make sure that no disc is on the tray.
   2) Insert the power pulag to the outret while pressing "PLAY" and "OPEN/CLOSE" button at the same time.
      FL Display indicate ¥ ; Region cord.
   3) Press Enter button. And EEPROM initialize start.
   4) When indicate "96kHz EEPROM" on the display , initialize finished.

   Note : During the EEPROM initialization the keys may not be operated.
   Press the "POWER" key to initiate the STAND-BY mode and the test mode will then
   be cancelled.

(2) Confirmation of DVD RF level

1. The oscilloscope is connected between P1 and GND.

2. Reproduction of the test disc (VT-501) made by JVC.

3. It is confirmed that RF LEVEL is 350mVp-p ± 150mVp-p.

4. When there is disorder in the waveform road cuts etc, test disk is exchanged and measured.

P12 and GND   P1 and GND

(3) Confirmation of CD jitter level and RF level

1. The CD jitter meter is connected between GND and P12.
   The RF level is observed at the same time.
2. The first test disk(CTS-1000) made of JVC is reproduced.

3. It is confirmed that RF LEVEL is 360 ± 100mVp-p.

5. When there is disorder in the waveform road cuts etc, test disk is exchanged and measured.

DVD SERVO CONTROL PWB
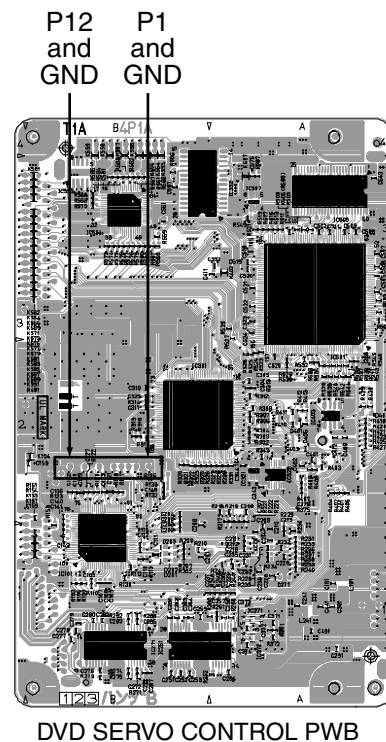
FRONT SIDE

(4) Flap adjustment of the Pick-up guide shaft

1) Make sure that there is no disc on the tray.

2) Press both the "PLAY" and "OPEN/CLOSE" keys of the main unit to activate the primary power and ∗∗¥(∗∗ ; Version3, ¥; Region cord) will be displayed on the FL indicator.

   Note: If the FL indicator display stops and remains at "TEST 0", unplug the power cord from the outlet and after waiting at least 1 second, plug it in again. After the tray open/close procedure has completed, unplug it again and then perform the initialization procedure again.

3) Press the "OPEN/CLOSE" key of the main unit to draw the tray out.
   *Place the test disk (VT-501) on the tray and then press the "OPEN/CLOSE" key.
   (Note: Pushing the tray to close it is not possible.)

4) Press the "PLAY" key of the main unit.

5) The "JIT 0000" is displayed on the FL indicator.
   Set the FL indicator figure value to its minimum by adjusting the pickup guide shaft flap.
   * The test mode is cancelled when the power is turned off.

Measurement	Adjustment point	Mode	Disc
—	Refer to Fig.2	Reproduction part	VT-501
Measurement machine	connections	Extension cord No.	
No need	Refer to Fig.1	QUQ110-3740AM	
General tool : Hex-head wrench (1.27 mm)			

"Flap adjustment" of the Pick-up guide shaft adjusts
"Tangential adjustment machine screw" A and
"Tilt adjustment machine screw" B from the
DVD Mechanism A'ssy bottom.

1. The part at the center on the DVD test disc is reproduced.
2. The flap adjustment screws is turned alternately and adjusted like clearly seeing the waveform of CN104"1" to the way.

Note
1. The tangential adjustment is done finish and, then, tilt is adjusted.
2. The repeat the adjustment 2-3 times,for best result.
3. The final adjustment should be tilt adjustment.
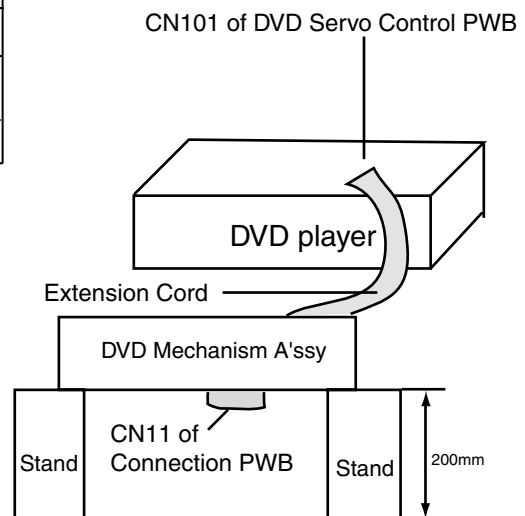
Fig.1
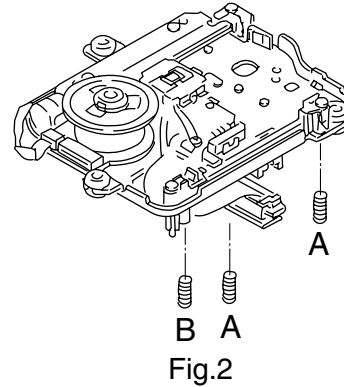
Confirmation after adjustment.

Confirm to reproduce video CD and CD after
the DVD test disc is adjusted and to find abnormality.

B   A
Fig.2

(5) About keeping the disc
As for the DVD test disc, plane accuracy is demanded.Please note the keeping place on the disc.
   1. Please do not put the disc directly on the work desk etc. after uses .
   2. To keep the planarity of the disc, politely handle ,and please put in a special case and keep
      the disc vertically after uses .
      Please keep keeping the disc in a cool place where direct sunshine and the air-conditioning
      wind do not drive.
   3. When the disc curves,an accurate adjustment cannot be done.
      Please exchange for a new test disc and adjust optics.
   4. Other discs might not be able to be reproduced when adjusting on a curved disc.

 Point of adjustment
  * Please execute the static electricity protection measures before starting the adjustment.
  * When the following parts are exchanged,optical adjustment "Adjust the flap of the disc motor"
   is necessary.
      1.The disc motor was exchanged.
      2.The laser pick up was exchanged.
      3.The traverse motor unit was exchanged.
 Note
      **Additionally, please adjust the flap of the disc motor when the picture quality
      deterioration is seen .The basic adjustment though, is unnecessary for part exchange
      in the traverse.
      An optical adjustment in the laser pick up cannot be done.
      Please adjust the flap of the disc motor after exchanging the laser pick up.**

  * When the traverse unit is exchanged, the adjustment is basically unnecessary.

Precautions for Service

Handling of Traverse Unit and Laser Pickup

1. Do not touch any peripheral element of the pickup or the actuator.
2. The traverse unit and the pickup are precision devices and therefore must not be subjected to strong shock.
3. Do not use a tester to examine the laser diode. (The diode can easily be destroyed by the internal power supply of the tester.)
4. To replace the traverse unit, pull out the metal short pin for protection from charging.
5. When replacing the pickup, after mounting a new pickup, remove the solder on the short land which is provided at the center of the flexible wire to open the circuit.
6. Half-fixed resistors for laser power adjustment are adjusted in pairs at shipment to match the characteristics of the optical block.
   Do not change the setting of these half-fixed resistors for laser power adjustment.

Destruction of Traverse Unit and Laser Pickup by Static Electricity

Laser diodes are easily destroyed by static electricity charged on clothing or the human body. Before repairing peripheral elements of the traverse unit or pickup, be sure to take the following electrostatic protection:

1. Wear an antistatic wrist wrap.
2. With a conductive sheet or a steel plate on the workbench on which the traverse unit or the pick up is to be repaired, ground the sheet or the plate.
3. After removing the flexible wire from the connector (CN101), short-circuit the flexible wire by the metal clip.
4. Short-circuit the laser diode by soldering the land which is provided at the center of the flexible wire for the pickup.
   After completing the repair, remove the solder to open the circuit.

Short-circuit
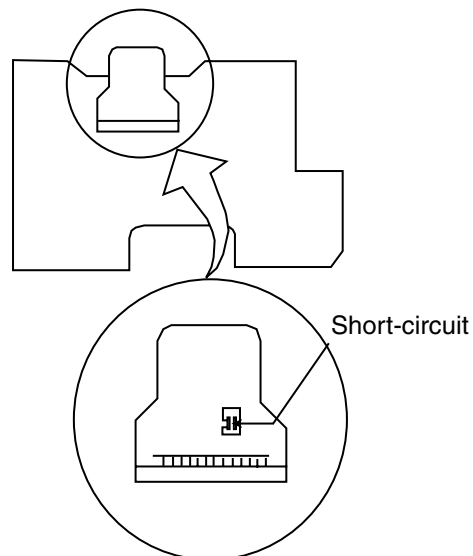
Discription of major IC's

■ AK5330 (IC701) : A/D Converter

1. Terminal layout

AINR	1 ●	24 DIF2
ZEROR	2	23 DIF1
AINL	3	22 DIF0
ZEROL	4	21 SDT0
VREFR	5	20 L/R
VREFL	6	19 SCLK
VCOM	7	18 MCLK
AGND	8	17 PD
VA	9	16 CMODE
VB	10	15 TST1
TST2	11	14 DGND
TST3	12	13 VD

Top View

2. Block diagram

VA AGND   VD   VB   DGND   MCLK CMODE

AINL → Δ Σ Modulator → Decimation Filter
ZEROL

AINR → Δ Σ Modulator → Decimation Filter
ZEROR

VCOM ← Voltage Reference
VREFL ←
VREFR ←

Clock Divider

Serial I/O Interface → SDT0

L/R
SCLK

TST1
TST2
TST3

PD   DIF0   DIF1   DIF2

3. Pin function

No.	Pin Name	I/O	Function
1	AINR	I	Rch Analog Input Pin
2	ZEROR	I	Rch Zero Input Pin
3	AINL	I	Lch Analog Input Pin
4	ZEROL	I	Lch Zero Input Pin
5	VREFR	O	Rch Vopltage Reference Output Pin. 2.5V Normally connected to AGND with a 0.1uF ceramic capacitor in parallel with an electrolytic capacitor less than 10uF.
6	VREFL	O	Lch Vopltage Reference Output Pin. 2.5V Normally connected to AGND with a 0.1uF ceramic capacitor in parallel with an electrolytic capacitor less than 10uF.
7	VCOM	O	Voltage Common Output Pin. 2.5V Normally connected to AGND with a 0.1uF ceramic capacitor in parallel with an electrolytic capacitor less than 10uF.
8	AGND	-	Analog Ground Pin
9	VA	-	Analog Supply Pin, +5V
10	VB	-	Substrate Voltage Supply Pin, +5V
11	TST2	I/O	Test Pins (Pull-down pin)
12	TST3	I/O	Must be left floating.
13	VD	-	Digital power Supply Pin, +5V
14	DGND	-	Digital Ground Pin
15	TST1	I	Test Pin (Pull-down pin) Must be left floating or connected to DGND.
16	CMODE	I	Master Clock Select Pin "L" : MCLK=256fs, "H" : MCLK=384fs
17	PD	I	Power-Down Pin When "H", the circuit is in power-down mode,Upon returning to "L", the AK5330 starts an offset calibration cycle.A calibration cycle should always be initiated after power-up.
18	MCLK	I	Master Clock Input Pin
19	SCLK	I	Serial Data Clock Pin Output data is clocked out on the falling edge of SCLK. Input data is clocked in on the rising edge of SCLK. SCLK requires a continuously supplied clock at any frequency from 32fs to 64fs.
20	L/R	I	Left/Right Channel Select Pin The fs clock is input to this pin. "H" : Lch, "L" : Rch
21	SDT0	O	Serial Data Output Pin Data bits are presented MSB first, in 2's complement format. This pin is "L" in the power-down mode.
22	DIF0	I	Serial Interface Format Pin
23	DIF1	I	Correspond to 8 modes.
24	DIF2	I	

■ AK93C65AF-X (IC590) : EEPROM

1.Pin layout

```
        ┌─────────────┐
 PE ──[ ]│ 1         8 │[ ]── NC
        │             │
VCC ──[ ]│ 2         7 │[ ]── GND
        │             │
 CS ──[ ]│ 3         6 │[ ]── DO
        │             │
 SK ──[ ]│ 4         5 │[ ]── DI
        └─────────────┘
          8 PIN SOP
```
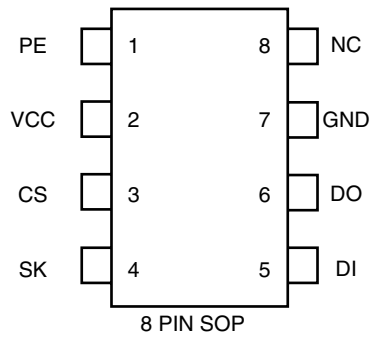
2.Block diagram
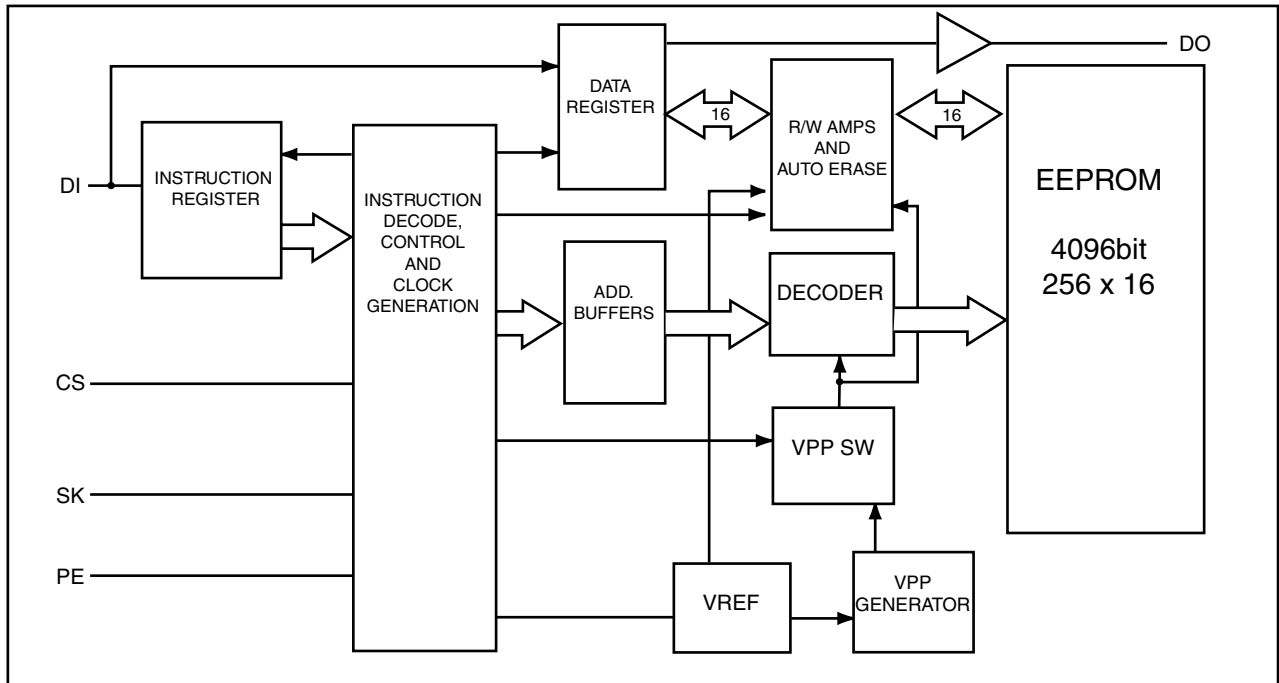
3.Pin function

Pin no.	Symbol	Function
1	PE	Program enable (With built-in pull-up resistor)
2	VCC	Power supply
3	CS	Chip selection
4	SK	Cereal clock input
5	DI	Cereal data input
6	DO	Cereal data output
7	GND	Ground
8	NC	No connection

NOTE : The pull-up resistor of the PE pin is about 2.5M Ω (VCC=5V)

■ AN8706FHQ (IC101) : Front end processor

1.Pin layout

Pin layout diagram for AN8706FHQ:

Top pins (75 to 51):
75 CBDOSL
74 CSAG
73 DCAGC
72 AGCG
71 PEAK
70 BOTTOM
69 RFENV
68 FC
67 BOOST
66 OFTR
65 BDO
64 JITOUT
63 GND3
62 FUPDN
61 ITDLI
60 VCOIN
59 PLFLT
58 PLFLT2
57 FCPO
56 PCPO
55 VCC3
54 CAPA
53 DTRD
52 IDGT
51 VCC5

Left pins (76 to 100):
CBDOFS 76
RBCA 77
TESTSG 78
RFINP 79
RFINN 80
VCC2 81
GND2 82
VREF2 83
COFTFS 84
COFTSL 85
RFON 86
RFOP 87
TS 88
DCRF 89
FS 90
VIN6 91
VIN5 92
VCC1 93
VIN1 94
VIN2 95
VIN3 96
VIN4 97
VREF4 98
DIFP 99
DIFN 100

Right pins (50 to 26):
50 RDCKP
49 RDCKN
48 RDTP
47 RDTN
46 GND5
45 GND4
44 VCC4
43 DTMONN
42 DTMONP
41 DSLFLT
40 DSLO
39 FLTOUT
38 DCFLT
37 VREF3
36 VPWBDO
35 VPWOFT
34 IDDLY
33 DBAL
32 GND1
31 VREF1
30 TKCNT
29 TKCFLT
28 TEOUT
27 TEI
26 RSCL

Bottom pins (1 to 25):
1 LDONB
2 LDONA
3 LPCOA
4 LPC1
5 VHARF
6 TGBAL
7 POFLT
8 PTH
9 TBAL
10 TG
11 FGCTL
12 FBAL
13 FEOUT
14 FEN
15 VREFL
16 VREFC
17 VREFH
18 PULIN
19 SEN
20 SCK
21 STDI
22 STNBY
23 XTRON
24 MTRON
25 ROMRAM

Center label: AN8706FHQ

2.Block diagram

3.Pin function

Pin No.	Symbol	I/O	Functions
1	LDONB	I	Laser ON (CD Head) terminal
2	LDONA	I	Laser ON (DVD Head) terminal
3	LPCOA	O	Laser drive output terminal
4	LPC1	I	Laser PIN input terminal
5	VHARF	O	VHALF voltage output terminal
6	TGBAL	I	Tangential phase balance control terminal
7	POFLT	O	Track detection Threshold value level terminal
8	PTH	I	Track detection Threshold value level terminal
9	TBAL	I	Tracking balance control terminal
10	TG	O	Tangential phase error signal output terminal
11	FGCTL	I	Focus amplifier Gain control terminal
12	FBAL	I	Focus balance control terminal
13	FEOUT	O	Focus error signal output terminal
14	FEN	I	Focus error output amplifier reversing input terminal
15	VREFL	O	VREFL voltage output terminal
16	VREFC	O	VREFC voltage output terminal
17	VREFH	O	VREFH voltage output terminal
18	PULIN	I	DSL,PLL drawing mode switch terminal
19	SEN	I	SEN(Cereal data input terminal)
20	SCK	I	SCK(Cereal data input terminal)
21	STDI	I	STDI(Cereal data input terminal)
22	STNBY	I	Standby mode control terminal
23	XTRON	I	Tracking OFF holding input terminal
24	MTRON	I	Monitor output ON/OFF switch terminal
25	ROMRAM	I	ROM · RAM switch terminal
26	RSCL	O	Standard current source terminal
27	TEI	I	Tracking error output Amp reversing input terminal
28	TEOUT	O	Tracking error signal output terminal
29	TKCFLT	O	Track count detection filter terminal
30	TKCNT	O	Track count output terminal
31	VREF1	O	VREF1 voltage output terminal
32	GND1	O	Earth terminal 1
33	DBAL	I	Data slice offset adjustment terminal
34	IDDLY	I	Data slice delay adjustment terminal
35	VPWOFT	I	OFTR detection level setting terminal
36	VPWBDO	I	BDO detection level setting terminal
37	VREF3	O	VREF3 voltage output terminal
38	DCFLT	O	Capacity connection terminal for data slice input filter
39	FLTOUT	O	Filter amplifier output terminal
40	DSLO	O	Data slice single data output terminal
41	DSLFLT	O	Constant filter terminal when data is sliceddelly
42	DTMONP	O	PLL differential motion 2 making to value edge signal moniter output (+)
43	DTMONN	O	PLL differential motion 2 making to value edge signal moniter output (-)
44	VCC4	I	Power terminal 4 (5V)
45	GND4	O	Earth terminal 4
46	GND5	O	Earth terminal 5
47	RDTN	O	PLL differential motion making to synchronization RF signal reversing output
48	RDTP	O	PLL differential motion making to synchronization RF signal rotation output
49	RDCKN	O	PLL differential motion making synchronization clock reversing output
50	RDCKP	O	PLL differential motion making synchronization clock rotation output

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Pin No.	Symbol	I/O	Functions
51	VCC5	I	Power terminal 5 (3.3V)
52	IDGT	I	Data slice part address part gate signal input terminal (For RAM)
53	DTRD	I	Data slice data read signal input terminal(For RAM)
54	CAPA	I	Data slice CAPA(Address)signal input terminal (For RAM)
55	VCC3	I	Power terminal 3 (5V)
56	PCPO	O	PLL phase gain set terminal
57	FCPO	O	PLL frequency gain set terminal
58	PLFLT2	O	PLL low region filter terminal
59	PLFLT	O	PLL high region filter terminal
60	VCOIN	I	PLL VCO input terminal
61	ITDLI	O	PLL jitter free current ripple removal filter terminal
62	FUPDN	I	PLL frequency control input terminal
63	GND3	O	Earth terminal 3
64	JITOUT	O	Detection signal output of jitter
65	BDO	O	BDO output terminal
66	OFTR	O	OFTR output terminal
67	BOOST	I	Booth control terminal for filter
68	FC	I	FC control terminal for filter
69	RFENV	O	RF enve output terminal
70	BOTTOM	O	Bottom enve detection filter terminal
71	PEAK	O	Peak enve detection filter terminal
72	AGCG	O	AGC amplifier gain control terminal
73	DCAGC	O	AGC amp filter terminal
74	CSAG	O	Sag cancellation circuit filter terminal
75	CBDOSL	O	BDO detection capacitor terminal
76	CBDOFS	O	BDO detection capacitor terminal
77	RBCA	O	BCA detection level setting terminal
78	TESTSG	I	TEST signal input terminal
79	RFINP	I	RF signal positive moving input terminal
80	RFINN	I	RF signal reversing input terminal
81	VCC2	I	Power terminal 2 (5V)
82	GND2	O	Earth terminal 2
83	VREF2	O	VREF2 voltage output terminal
84	COFTFS	O	OFTR detection capacitor terminal
85	COFTFL	O	OFTR detection capacitor terminal
86	RFON	O	RF signal output terminal P
87	RFOP	O	RF signal output terminal N
88	TS	O	All addition amplifier (DVD) output terminal
89	DCRF	O	All addition amplifier capacitor terminal
90	FS	O	All addition amplifier (CD) output terminal
91	VIN6	I	Focus input of external division into two terminal
92	VIN5	I	Focus input of external division into two terminal
93	VCC1	I	Power terminal 1 (5V)
94	VIN1	I	External division into four (DVD/CD) RF input terminal 1
95	VIN2	I	External division into four (DVD/CD) RF input terminal 2
96	VIN3	I	External division into four (DVD/CD) RF input terminal 3
97	VIN4	I	External division into four (DVD/CD) RF input terminal 4
98	VREF4	O	VREF4 voltage output terminal
99	DIFP	O	RF signal (RAM) output terminal P
100	DIFN	O	RF signal (RAM) output terminal N

■ BA15218N (IC32 / IC35) : Dual Ope. Amp.

OUT1 +IN1 +IN1 GND +IN2 -IN2 OUT2 Vcc

■ MC33269D-X (IC555) : Regurator

GND/ADJ 1   8 NC
Vout {   2   7 } Vout
         3   6
Vin   4   5 NC
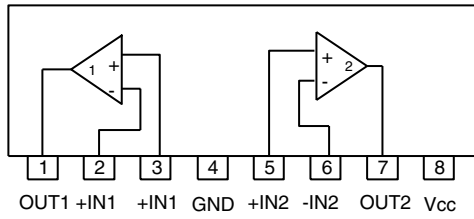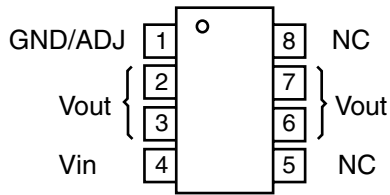
■ RN5RZ20BA-X(IC102) : High cycle module

1.Terminal layout   2.Block diagram
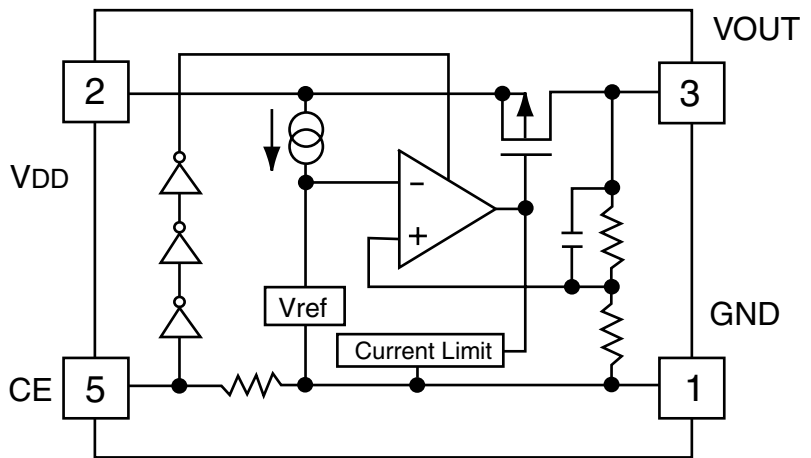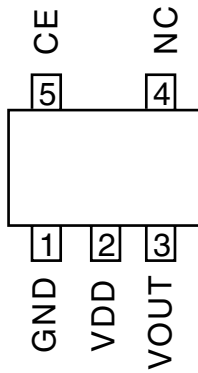
3.Pin function

Pin No.	Pin name	Function
1	GND	Ground terminal
2	VDD	Input terminal
3	VOUT	Output terminal
4	NC	No connection
5	CE	Chip enable terminal

■ BA5983FM (IC271) : 4CH DRIVER

1.Block Diagram
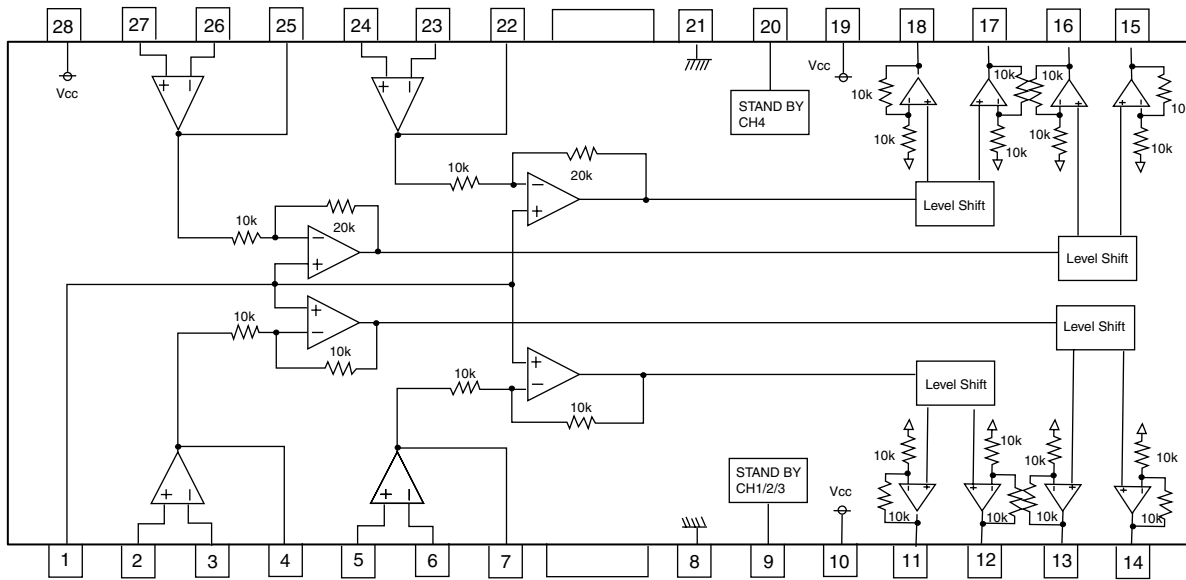
2.Pin Function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	BLAS IN	I	Input for Bias-amplifier	15	VO4(+)	O	Non inverted output of CH4
2	OPIN1(+)	I	Non inverting input for CH1 OP-AMP	16	VO4(-)	O	Inverted output of CH4
3	OPIN1(-)	I	Inverting input for CH1 OP-AMP	17	VO3(+)	O	Non inverted output of CH3
4	OPOUT1	O	Output for CH1 OP-AMP	18	VO3(-)	O	Inverted output of CH3
5	OPIN2(+)	I	Non inverting input for CH2 OP-AMP	19	PowVcc2	-	Vcc for CH3/4 power block
6	OPIN2(-)	I	Inverting input for CH2 OP-AMP	20	STBY2	I	Input for Ch4 stand by control
7	OPOUT2	O	Output for CH2 OP-AMP	21	GND	-	Substrate ground
8	GND	-	Substrate ground	22	OPOUT3	O	Output for CH3 OP-AMP
9	STBY1	I	Input for CH1/2/3 stand by control	23	OPIN3(-)	I	Inverting input for CH3 OP-AMP
10	PowVcc1	-	Vcc for CH1/2 power block	24	OPIN3(+)	I	Non inverting input for CH3 OP-AMP
11	VO2(-)	O	Inverted output of CH2	25	OPOUT4	O	Output for CH4 OP-AMP
12	VO2(+)	O	Non inverted outpur of CH2	26	OPIN4(-)	I	Inverting input for CH4 OP-AMP
13	VO1(-)	O	Inverted output of CH1	27	OPIN4(+)	I	Non inverting input for CH4 OP-AMP
14	VO1(+)	O	Non inverted outpur of CH1	28	PreVcc	-	Vcc for pre block

■ HY57V161610DTC8 or KM416S1120DT-G8 (IC504,IC505) : 16MB SDRAM

1.Block diagram
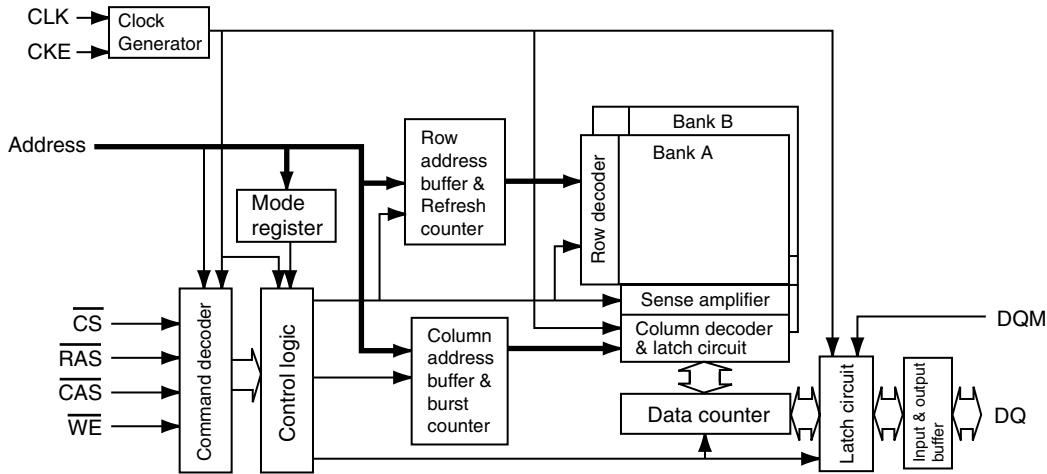
2.Pin function

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	VCC	Power supply	26	VSS	Connect to GND
2,3	DQ0,1	Data input/output	27~32	A4~9	Address inputs
4	VSS	Connect to GND	33	NC	Non connect
5,6	DQ2,3	Data input/output	34	CKE	Clock enable
7	VDD	Power supply	35	CLK	System clock input
8,9	DQ4,5	Data input/output	36	UDQM	Upper DQ mask enable
10	VSS	Connect to GND	37	NC	Non connect
11,12	DQ6,7	Data input/output	38	VCC	Power supply
13	VCC	Power supply	39,40	DQ8,9	Data input/output
14	LDQM	Lower DQ mask enable	41	VSS	Connect to GND
15	$\overline{WE}$	Write enable	42,43	DQ10,11	Data input/output
16	$\overline{CAS}$	Column address strobe	44	VDD	Power supply
17	$\overline{RAS}$	Row address strobe	45,46	DQ12,13	Data input/output
18	$\overline{CS}$	Chip enable	47	VSS	Connect to GND
19,20	A11,10	Address inputs	48,49	DQ14,15	Data input/output
21~24	A0~3	Address inputs	50	VSS	Connect to GND
25	VCC	Power supply			

■ JCE8011(IC551):GRAPHIC CONTROLLER

Pin No.	Symbol	I/O	Function
1~8	VD0~7	I	DVD Image signal input (Multi plex data Y,Cr,Cb)
9	VCLKI	I	Dot clock signal input (27MHz)
10	HSYNCI	I	The horizontal synchronous signal input
11	VSYNCI	I	Vertical synchronous signal input
12	VCC	-	Power supply
13	VCLKD	O	Dot clock signal output (27MHz)
14	HSYNCO	O	'H' blanking output
15	VSYNCO	O	'V' blanking output
16~23	DOUT0~7	O	Digital data output
24	TEST	-	Test terminal (Uses as GND usually)
25	RESETB	I	System reset signal
26	GND	-	Connect to GND
27	NTB	I	Mode switching NTSC(low) / PAL(high)
28	DTSF0	I	Taking timing shift of VD input
29	DTSFI	I	Taking timing shift of VD input
30	VIDEG	I	Taking edge specification of VD input (0:up , 1:down)
31	DOSF0	I	Timing shift input of output data
32	DOSF1	I	Timing shift input of output data
33	XVRST	O	Non connect
34	F1	O	Field Identification signal output
35	HBL	O	'H' blanking output
36	VBL	O	'V' blanking output
37	VOEDG	I	Output timing setting of DOUT (0:up , 1:down)
38	VCC	-	Power supply
39~46	FRD7~0	I	Field memory read data input
47	GND	-	Connect to GND
48	FRCK	O	Field memory read clock
49	FWCK	O	Field memory write clock
50	FREB	O	Field memory read enable
51	FWEB	O	Field memory write enable
52	FRRSTB	O	Field memory read address reset
53	FWRSTB	O	Field memory write address reset
54~61	FWD7~0	O	Field memory write data output
62	VCC	-	Power supply
63~70	CHD7~0	I	Character ROM data
71	GND	-	Connect to GND
72	CHOEB	O	Character ROM output enable
73~82	CHA19~10	O	Character ROM address output
83	VCC	-	Power supply
84~93	CHA9~0	O	Character ROM address output
94	GND	-	Connect to GND
95	ACK	O	
96	CS1B	I	Serial data chip select for graphic control
97	CS2B	I	Serial data chip select for encoder control
98	SCK	I	Serial clock input
99	RXD	I	Serial input data
100	TXD	O	Serial output data

■ MC44724AVFU (IC554) : VIDEO ENCODER

1.Terminal layout
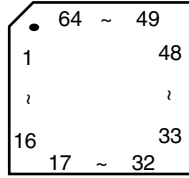
2.Block diagrams
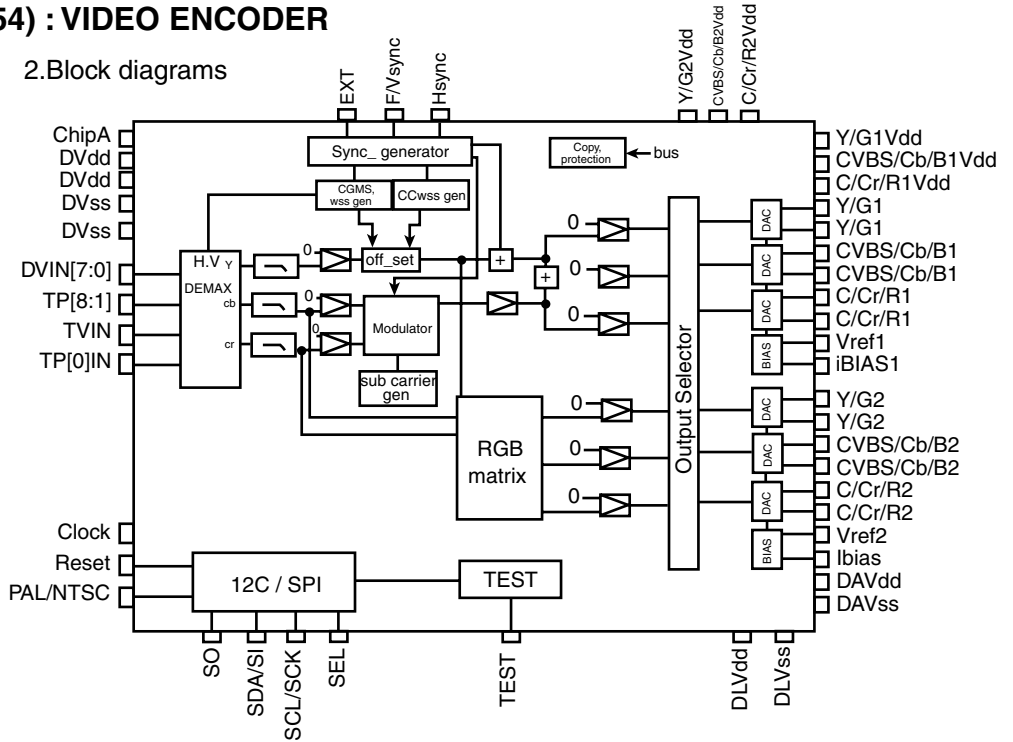
3.Pin function

No.	Symbol	I/O	Function	No.	Symbol	I/O	Function
1	CVBS/Cb/B1	O	Analog composite drive signal (+)	33	SO	-	Non connect
2	$\overline{\text{CVBS/Cb/B1}}$	O	Analog composite drive signal (-)	34	SDA/SI	I	SPI Mode : Serial data input
3	CVBS/Cb/B1Vdd	-	Power supply for CVBS/Cb/B DAC1	35	SCL/SCK	I	Serial clock input
4	Y/G1	O	Analog brightness signal/G drive signal (+)	36	SEL	I	Power supply for serial data,chip select,digital
5	$\overline{\text{Y/G1}}$	O	Analog brightness signal/G drive signal (-)	37	DVdd	--	Power supply for digital circuit
6	Y/G1/Vdd	-	Power supply for Y/G DAC	38	DVss	--	Digital ground
7	C/Cr/R1	O	Analog chroma signal (+)	39	DVIN7	I/O	Y data input / test data I/O
8	$\overline{\text{C/Cr/R1}}$	O	Analog chroma signal (-)	40	DVIN6	I/O	Y data input / test data I/O
9	C/Cr/R1Vdd	-	Power supply for C/Cr/RDAC	41	DVIN5	I/O	Y data input / test data I/O
10	DAVss	-	Connect to ground for DAC	42	DVIN4	I/O	Y data input / test data I/O
11	TBIAS1	O	Standard BIAS for DAC1	43	DVIN3	I/O	Y data input / test data I/O
12	Vref1	-	Standard voltage for DAC1	44	DVIN2	I/O	Y data input / test data I/O
13	DAVdd	-	Power supply for DAC	45	DVIN1	I/O	Y data input / test data I/O
14	Vref2	-	Standard voltage for DAC2	46	DVIN0	I/O	Y data input / test data I/O
15	TBIAS2	O	Standard BIAS for DAC2	47	TVIN	I	VIDEO mute on Reset(0:nomal, 1:mute)
16	NC	-	Non connect	48	EXT	I/O	Frame output / VBI information input
17	CVBS/Cb/B2	O	Analog composite drive signal (+)	49	F/Vsyac	I/O	Frame / Vertical, synchronous I/O
18	CVBS/Cb/B2	O	Analog composite drive signal (-)	50	Chsyac	I/O	The horizontal, synchronous I/O
19	CVBS/Cb/B2Vdd	-	Power supply for CVBS/Cb/B DAC2	51	DATST	I	Data input
20	Y/G2	O	Analog brightness signal/G drive signal (+)	52	TP-8	I/O	Multiplex data input
21	$\overline{\text{Y/G2}}$	O	Analog brightness signal/G drive signal (-)	53	TP7	I/O	Multiplex data input
22	Y/GVdd	-	Power supply for Y/G DAC	54	TP6	I/O	Multiplex data input
23	C/Cr/R2	O	Analog chroma signal (+)	55	TP5	I/O	Multiplex data input
24	$\overline{\text{C/Cr/R2}}$	O	Analog chroma signal (-)	56	DVss	-	Ground for digital circuit
25	C/Cr/R2Vdd	-	Power supply for C/Cr/RDAC2	57	DVdd	-	Power supply for digital circuit
26	ChipA	-	Chip address selection	58	TP4	I/O	Data input / Test data I/O
27	TEST	I	Connect to test pin	59	TP3	I/O	Data input / Test data I/O
28	DVdd	-	Digital ground	60	TP2	I/O	Data input / Test data I/O
29	CLOCK	I	Clock signal input (27MHz)	61	TP1	I/O	Data input / Test data I/O
30	DVss	-	Power supply for digital circuit	62	TP0	I/O	Data input / Test data I/O
31	Reset	I	Reset signal input L:ON	63	DLVdd	-	Power supply for D/A converter
32	PAL/NTSC	I	Selection NTSC/PAL NTSC:L PAL:H	64	DLVss	-	Ground for D/A converter

■ MN102LP25G-01(IC401):UNIT CPU

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	WAIT	I	Micon wait signal input	51	SWCLOSE	I	Detection switch of tray close
2	RE	O	Read enable	52	SWOPEN	I	Detection switch of tray open
3	MUTE	O	Driver mute	53	ADSCEN	O	Serial enable signal for ADSC
4	WEM	O	Write enable	54	VDD	-	Non connect
5	CS0	O	Non connect	55	EFPEN	O	Serial enable signal for FEP
6	CS1	O	Chip select for ODC	56	SLEEP	O	Standby signal for FEP
7	CS2	O	Chip select for ZIVA	57	BUSY	I	Communication busy
8	CS3	O	Chip select for outer ROM	58	REQ	O	Communication Request
9	TCLOSE	O	Tray close signal output	59	WEROM	O	Non connect
10	TOPEN	O	Tray open signal output	60	WPROM	O	Non connect
11	LSIRST	I	LSI reset	61	VSS	-	Power supply
12	WORD	O	Bus selection input	62	EECS	O	Chip select signal for EEPROM
13	A0	O	Address bus 0 for CPU	63	EECK	O	Clock signal for EEPROM
14	A1	O	Address bus 1 for CPU	64	EEDI	I	Input data for EEPROM
15	A2	O	Address bus 2 for CPU	65	EEDO	O	Output data for EEPROM
16	A3	O	Address bus 3 for CPU	66	VDD	-	Power supply
17	VDD	-	Power supply	67	SCLK0	I	Communication clock
18	SYSCLK	O	System clock signal output	68	S2UDT	I	Communication input data
19	VSS	-	Power supply	69	S2SDT	O	Communication output data
20	XI	-	Non connect	70	CPSCK	O	Clock for ADSC serial
21	XO	-	Non connect	71	SDIN	I	ADSC serial data input
22	VDD	-	Power supply	72	SDOUT	O	ADSC serial data output
23	OSCI	I	Clock signal input(13.5MHz)	73	-	-	Non connect
24	OSCO	-	Non connect	74	-	-	Non connect
25	MODE	I	CPU Mode selection input	75	NMI	-	Non connect
26	A4	O	Address bus 4 for CPU	76	ADSCIRQ	I	Interrupt input of ADSC
27	A5	O	Address bus 5 for CPU	77	ODCIRQ	I	Interrupt input of ODC
28	A6	O	Address bus 6 for CPU	78	DECIRQ	I	Interrupt input of ZIVA
29	A7	O	Address bus 7 for CPU	79	WAKEUP	O	Non connect
30	A8	O	Address bus 8 for CPU	80	ODCIRQ2	I	Non connect
31	A9	O	Address bus 9 for CPU	81	ADSEP	I	Address data selection input
32	A10	O	Address bus 10 for CPU	82	RST	I	Reset input
33	A11	O	Address bus 11 for CPU	83	VDD	-	Power supply
34	VDD	-	Power supply	84	TEST1	I	Test signal 1 input
35	A12	O	Address bus 12 for CPU	85	TEST2	I	Test signal 2 input
36	A13	O	Address bus 13 for CPU	86	TEST3	I	Test signal 3 input
37	A14	O	Address bus 14 for CPU	87	TEST4	I	Test signal 4 input
38	A15	O	Address bus 15 for CPU	88	TEST5	I	Test signal 5 input
39	A16	O	Address bus 16 for CPU	89	TEST6	I	Test signal 6 input
40	A17	O	Address bus 17 for CPU	90	TEST7	I	Test signal 7 input
41	A18	O	Address bus 18 for CPU	91	TEST8	I	Test signal 8 input
42	A19	O	Address bus 19 for CPU	92	VSS	-	Power supply
43	VSS	-	Power supply	93	D0	I/O	Data bus 0 of CPU
44	A20	O	Address bus 20 for CPU	94	D1	I/O	Data bus 1 of CPU
45	-	-	Non connect	95	D2	I/O	Data bus 2 of CPU
46	STOP	-	Non connect	96	D3	I/O	Data bus 3 of CPU
47	ADPD	-	Non connect	97	D4	I/O	Data bus 4 of CPU
48	-	-	Non connect	98	D5	I/O	Data bus 5 of CPU
49	-	-	Non connect	99	D6	I/O	Data bus 6 of CPU
50	TRVSW	I	Detection switch of traverse inside	100	D7	I/O	Data bus 7 of CPU

■ MN103007BGA (IC301) : Optical disc controller

1. Terminal layout

Top pins (left to right): DMARQ 144, NIOWR 143, VSS 142, NIORD 141, IORDY 140, NDMACK 139, 5VDD 138, INTRQ 137, IOCS16 136, DA1 135, VSS 134, NPDIAG 133, DA0 132, DA2 131, VDD 130, NCS1FX 129, NCS3FX 128, NDASP 127, NTRYCL 126, 5VDD 125, NEJECT 124, VSS 123, MONI0 122, MONI1 121, MONI2 120, MONI3 119, SDATA 118, SCLOCK 117, VDD 116, FAT0 115, DAT1 114, DAT2 113, DAT3 112, CHCK4 111, XCLDCK 110, SUBC 109

Left pins (top to bottom):
Pin	Signal
1	HDD15
2	HDD0
3	HDD14
4	5VDD
5	HDD1
6	HDD13
7	HDD2
8	VSS
9	HDD12
10	VDD
11	HDD3
12	HDD11
13	HDD4
14	HDD10
15	5VDD
16	HDD5
17	HDD9
18	VSS
19	HDD6
20	HDD8
21	HDD7
22	5VDD
23	NRESET
24	MASTER
25	NINT0
26	NINT1
27	WAITOOC
28	NMRST
29	DASPST
30	VDD
31	OSCO2
32	OSCI2
33	UATASEL
34	VSS
35	PVSSDRAM
36	PVDDDAM

MN103007BGA

Right pins (top to bottom):
Pin	Signal
108	SBCK
107	VSS
106	P0
105	P1
104	PVDD
103	PVSS
102	VDD
101	OSC01
100	OSCI1
99	VSS
98	LRCK
97	BLKCK
96	IPFLAG
95	DACCLK
94	DACLRCK
93	DACDATA
92	NTRON
91	LG
90	JMPINH
89	IDDHOLD
88	PLLOK
87	CLKOUT2
86	VDD
85	NRST
84	MMOD
83	VSS
82	CPDET1
81	CPDET2
80	BDO
79	IDGT
78	DTRO
77	TEHLD
76	VDD
75	CLKOUT1
74	CPUDT0
73	CPUDT1

Bottom pins (left to right): CPUNDA17 37, CPUADR16 38, VSS 39, CPUASR15 40, CPUADR14 41, CPUADR13 42, CPUADR12 43, VDD 44, CPUADR11 45, CPUADR10 46, CPUADR9 47, CPUADR8 48, CPUADR7 49, CPUADR6 50, CPUADR5 51, CPUADR4 52, CPUADR3 53, CPUADR2 54, CPUADR1 55, VSS 56, CPUADR0 57, NCS 58, NWR 59, NRD 60, VDD 61, CPUDT17 62, CPUDT16 63, PVPODRAM 64, PTESTORAM 65, OVDDDRAM 66, PVSSDRAM 67, CPUDT15 68, CPUDT14 69, CPUDT13 70, VSS 71, CPUDT2 72

2. Block diagram

TH-A10

3.Function

Pin NO.	Symbol	I/O	Function	Pin NO.	Symbol	I/O	Function
1	HDD15	I/O	ATAPI data	48	CPUADR8	I	System control address
2	HDD0	I/O	ATAPI data	49	CPUADR7	I	System control address
3	HDD14	I/O	ATAPI data	50	CPUADR6	I	System control address
4	5VDD			51	CPUADR5	I	System control address
5	HDD1	I/O	ATAPI data	52	CPUADR4	I	System control address
6	HDD13	I/O	ATAPI data	53	CPUADR3	I	System control address
7	HDD2	I/O	ATAPI data	54	CPUADR2	I	System control address
8	VSS			55	CPUADR1	I	System control address
9	HDD12	I/O	ATAPI data	56	VSS		GND
10	VDD			57	CPUADR0	I	System control address
11	HDD3	I/O	ATAPI data	58	NCS	I	System control chip selection
12	HDD11	I/O	ATAPI data	59	NWR	I	System control wright
13	HDD4	I/O	ATAPI data	60	NRD	I	System control lead
14	HDD10	I/O	ATAPI data	61	VDD		Apply 3V
15	5VDD			62	CPUDT7		System control data
16	HDD5	I/O	ATAPI data	63	CPUDT6		System control data
17	HDD9	I/O	ATAPI data	64	PVPPDRAM	O	C=10000PF is connected
18	VSS						between VSS
19	HDD6	I/O	ATAPI data	65	PTESTDRAM	I	VSS connected
20	HDD8	I/O	ATAPI data	66	OVDDDRAM		
21	HDD7	I/O	ATAPI data	67	PVSSDRAM		
22	5VDD			68	CPUDT5		System control data
23	NRESET	I	ATAPI reset	69	CPUDT4		System control data
24	MASTER	I/O	ATAPI master / slave selection	70	CPUDT3		System control data
25	NINT0	O	System control interruption 0	71	VSS		GND
26	NINT1	O	System control interruption 1	72	CPUDT2		System control data
27	WAITODC	O	System control weight control	73	CPUDT1	I/O	System control data
28	NMRST	O	System control reset	74	CPUDT0	I/O	System control data
29	DASPST	I	DASP signal initializing	75	CLKOUT1	O	16.9/11.2/8.45MHz clock
30	VDD			76	VDD	-	Apply 3V
31	OSCO2	I,O	VSS connection,OPEN	77	TEHLD	O	Mirror gate
32	OSCI2	I,O	VSS connection, OPEN	78	DTRO	O	Data part frequency control
33	UATASEL	I	VSS connection				switch
34	VSS			79	IDGT	O	Part CAPA switch
35	PVSSDRAM			80	BDO	I	RF dropout / BCA data of
36	PVDODRAM						making to binary
37	CPUADR17	I	System control address	81	CPDET2	I	Outer side CAPA detection
38	CPUADR18	I	System control address	82	CPDET1	I	Side of surroundings on inside
39	VSS			83	VSS		GND
40	CPUADR15	I	System control address	84	MMOD	I	VSS connected
41	CPUADR14	I	System control address	85	NRST	I	System reset
42	CPUADR13	I	System control address	86	VDD	-	Apply 3V
43	CPUADR12	I	System control address	87	CLKOUT2	O	16.9MHz clock
44	VDD		System control address	88	PLLOK	O	Frame mark detection
45	CPUADR11	I	System control address	89	IDOHOLD	O	ID gate for tracking holding
46	CPUADR10	I	System control address	90	JMPINH	O	Jump prohibition
47	CPUADR9	I	System control address				

Pin NO.	Symbol	I/O	Function	Pin NO.	Symbol	I/O	Function
91	LG	O	Land / group switch	133	NPDIAG	I/O	ATAPI slave master diagnosis input
92	NTRON	I	Tracking ON	134	VSS		
93	DACDATA	O	Cereal output	135	DA1	I/O	ATAPI host address
94	DACLRCK	O	L and R identification output	136	IOCS16	O	ATAPI output of selection of width
95	DACCLK	I	Clock for cereal output				of host data bus
96	IPFLAG	I	Interpolation flag input	137	INTRQ	O	ATAPI host interruption output
97	BLKCK	I	Sub-code,Block clock input	138	5VDD		
98	LRCK	I	L and R identification signal output	139	NDMACK	I	ATAPI host DMA response
99	VSS			140	IORDY	O	ATAPI host ready output
100	OSCI1	I,O	16.9MHz oscillation	141	NIORD	I	ATAPI host read
101	OSCO1	I,O	16.9MHz oscillation	142	VSS		
102	VDD			143	NIOWR	I/O	ATAPI host writes
103	PVSS			144	DMARQ	O	ATAPI host DMA demand
104	PVDD						
105	P1	I/O	Terminal MASTER polarity switch input				
106	P0	I/O	CIRC-RAM OVER/UNDER Interruption signal input				
107	VSS						
108	SBCK	O	Sub-code, Clock output for serial input				
109	SUBC	I	Sub-code, Cereal input				
110	XCLDCK	I	Sub-code, Frame clock input				
111	CHCK4	I	Read clock to DAT3~0(Output of dividing frequency four from ADSC)				
112	DAT3	I	Read data from DISC				
113	DAT2	I	(PAralle output from ADSC)				
114	DAT1	I					
115	DAT0	I					
116	VDD						
117	SCLOCK	I/O	Debugging cereal clock (270 Ω pull up)				
118	SDATA	I/O	Debugging cereal data (270 Ω pull up)				
119~122	MONI3~0	O	Internal goods title monitor				
123	VSS						
124	NEJECT	I	Eject detection				
125	5VDD						
126	NTRYCL	I	Tray close detection				
127	NDASP	I/O	ATAPI Drive active/ Sulave connection I/O				
128	NCS3FX	I	ATAPI host chip selection				
129	NCS1FX	I	ATAPI host chip selection				
130	VDD						
131	DA2	I/O	ATAPI host address				
132	DA0	I/O	ATAPI host address				

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Pin NO.	Symbol	I/O	Function
91	LG	O	Land / group switch
92	NTRON	I	Tracking ON
93	DACDATA	O	Cereal output
94	DACLRCK	O	L and R identification output
95	DACCLK	I	Clock for cereal output
96	IPFLAG	I	Interpolation flag input
97	BLKCK	I	Sub-code,Block clock input
98	LRCK	I	L and R identification signal output
99	VSS		
100	OSCI1	I,O	16.9MHz oscillation
101	OSCO1	I,O	16.9MHz oscillation
102	VDD		
103	PVSS		
104	PVDD		
105	P1	I/O	Terminal MASTER polarity switch input
106	P0	I/O	CIRC-RAM OVER/UNDER Interruption signal input
107	VSS		
108	SBCK	O	Sub-code, Clock output for serial input
109	SUBC	I	Sub-code, Cereal input
110	XCLDCK	I	Sub-code, Frame clock input
111	CHCK4	I	Read clock to DAT3~0 (Output of dividing frequency four from ADSC)
112	DAT3	I	Read data from DISC
113	DAT2	I	(PAralle output from ADSC)
114	DAT1	I	
115	DAT0		
116	VDD		
117	SCLOCK	I/O	Debugging cereal clock (270Ω pull up)
118	SDATA	I/O	Debugging cereal data (270Ω pull up)
119	MONI3	O	Internal goods title monitor
120	MONI2	O	
121	MONI1	O	
122	MONI0	O	
123	VSS		
124	NEJECT	I	Eject detection
125	5VDD		
126	NTRYCL	I	Tray close detection
127	NDASP	I/O	ATAPI Drive active/ Sulave connection I/O
128	NCS3FX	I	ATAPI host chip selection
129	NCS1FX	I	ATAPI host chip selection
130	VDD		
131	DA2	I/O	ATAPI host address
132	DA0	I/O	ATAPI host address

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Pin NO.	Symbol	I/O	Function
133	NPDIAG	I/O	ATAPI slave master diagnosis input
134	VSS		
135	DA1	I/O	ATAPI host address
136	IOCS16	O	ATAPI output of selection of width of host data bus
137	INTRQ	O	ATAPI host interruption output
138	5VDD		
139	NDMACK	I	ATAPI host DMA response
140	IORDY	O	ATAPI host ready output
141	NIORD	I	ATAPI host read
142	VSS		
143	NIOWR	I/O	ATAPI host writes
144	DMARQ	O	ATAPI host DMA demand

■ MN67705EA (IC201) : Digital servo controller

1.Terminal layout

Top side pins (left to right, 128 down to 97):

128 FEPNTRON
127 N.C.
126 N.C.
125 CDDVD
124 N.C.
123 N.C.
122 N.C.
121 ECR(PWM3B)
120 EC(PWM3A)
119 DVSS
118 SYSCLK
117 VCOF1
116 IREF1
115 XRESET
114 TEST
113 MINTEST
112 FG
111 DSLO
110 TKCRS2
109 TKCRS1
108 OFTR
107 DVDD
106 TRSDRVB(DA8)
105 TRSDRVA(DA7)
104 TRDRV(DA6)
103 FODRV(DA5)
102 DBAL(DA4)
101 BOOST(DA3)
100 FC(DA2)
99 FBAL(DA1)
98 AVDD
97

Left side pins:

FGC	1
LDONA	2
LDONB	3
PULIN	4
SRF	5
DVSS	6
TRAYSET1	7
TRAYSET2	8
DRVMUTE	9
DVDD	10
TRVSW	11
TRAY-CLOSE	12
TRAY-OPEN	13
ST/SP	14
HFMON	15
BRK	16
DVSS	17
PLLOK	18
N.C.	19
TBAL(PWMDA1)	20
GBAL(PWMDA2)	21
BDOLVL(PWMDA3)	22
OFTLVL(PWMDA4)	23
N.C.	24
N.C.	25
N.C.	26
DVSS	27
DVDD	28
TSTSG	29
FUPDN	30
MONA	31
MONB	32

Center: MN67705

Right side pins:

96	AVSS
95	TS(AD1)
94	FS(AD2)
93	FE(AD3)
92	TROFS(AD4)
91	TE(AD5)
90	VREFLDA
89	VREFMDA
88	VREFHDA
87	TG(AD6)
86	N.C.(AD7)
85	N.C.(AD8)
84	RFENV(AD9)
83	VREFOP
82	LDCUR(AD10)
81	JITOUT(AD11)
80	VREFC
79	AVDD(AD12)
78	VREFHAD
77	VREFMAD
76	VREFLAD
75	AVSS
74	DVDD
73	DVSS
72	TX
71	MOND
70	IPFLAG
69	CIRCIRQ
68	N.C.
67	N.C.
66	N.C
65	DVSS

Bottom side pins (left to right, 33 to 64):

33 CPSEN
34 CPCEN
35 CPUIRQ
36 CPUCLK
37 CPUDTIN
38 CPUDTOUT
39 CHK4I
40 SCLK+
41 SCLK-
42 SDAT+
43 SDAT-
44 BDO
45 SBCK
46 N.C.
47 N.C.
48 N.C.
49 DVSS
50 N.C.
51 DVSS
52 DVDD
53 SUBC
54 BLKCLK
55 MONC
56 NCLDCK
57 LRCK
58 NTRON
59 DVSS
60 DAT0
61 DAT1
62 DAT2
63 DAT3
64 CHCK4

2.Block diagram

The signal of the error of the servo input from FEP. → A/Dconverter → Focus servo / Tracking servo → A/D converter (Analog control) → Focus tracking driving value output

Track crossing counter → Traverse servo → PWM → Spindre / traverse driving value output

Phese comparison → Spindle servo

Line speed detection → SERVO DSP core ← Standard clock generation (PLL) ← Crystal 33.8MHz

Driver → Detection at FG cycle

Serial port CPU I/F

CIRC core (PLL) → ODC

FEP I/F (PLL) ← FEP

CPU

└ ─ ┘ ADSC function block of the second generation.

3.Pin function

Pin No.	Symbol	I/O	Function
1	FGC	O	H fixation
2	LDONA	O	Laser drive controlA (ON / OFF)
3	LDONB	O	Laser drive controlB (ON / OFF)
4	PULIN	O	DSL and PLL high boost signal (FEP)
5	SRF	O	Head amplifier gain H/L selection
6	DVSS	—	Ground for digital circuit
7	TRAYSET1	O	Tray drive ON/OFF and direction control
8	TRAYSET2	O	Tray drive ON/OFF and direction control
9	DRVMUTE	O	Drive IC mute control
10	DVDD	—	Power supply for digital circuit
11	TRVSW	I	Surroundings position detection in traverse
12	TRAY-CLOSE	I	Tray close detection SW
13	TRAY-OPEN	I	Tray opening detection SW
14	ST/SP	O	Spindle motor drive switch (START /STOP)
15	HFMON	O	High cycle module control
16	BRK	O	Spindle motor IC short brake control
17	DVSS	—	Ground for digital circuit
18	PLLOK	I	SYNC detection (DVD : 18T / CD : 22T)
19	N.C.	O	
20	TBAL(PWMDA1)	O	Tracking balance (FEP)
21	GBAL(PWMDA2)	O	Tangential balance (FEP)
22	BDOLVL(PWMDA3)	O	BDO slice level (FEP)
23	OFTLVL(PWMDA4)	O	Off-track error slice level (FEP)
24	N.C.	O	
25	N.C.	O	
26	N.C.	O	
27	DVSS	—	Ground for digital circuit
28	DVDD	—	Power supply for digital circuit
29	TSTSG	O	Self calibration signal (FEP)
30	FUPDN	O	Signal of frequency UP/DOWN of PLL (FEP)
31	MONA	O	Monitor terminal A
32	MONB	O	Monitor terminal B
33	CPSEN	I	Servo DSP cereal I/F chip selection (SYSCOM)
34	CPCEN	I	CIRC cereal I/F chip selection (SYSCOM)
35	CPUIRQ	O	Interrupt request to silicon (SYSCOM)
36	CPUCLK	I	Silicon cereal I/F clock (SYSCOM)
37	CPUDTIN	I	Silicon cereal I/F data input (SYSCOM)
38	CPUDTOUT	O	Silicon cereal I/F data output (SYSCOM)
39	CHK4I	I	Connects with unused DVSS
40	SCLK+	I	Lead channel clock differential motion signal (positive)
41	SCLK-	I	Lead channel clock differential motion signal (negative)
42	SDAT+	I	Lead channel data differential motion signal (positive)
43	SDAT-	I	Lead channel data differential motion signal (negative)
44	BDO	I	BDO + BCA (FEP)
45	SBCK	I	CD sub-code data shift clock (ODC)
46	IREF2	—	Connects with unused DVSS

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Pin No.	Symbol	I/O	Function
47	IREF3	—	Connects with unused DVSS
48	VCOF2	—	Connects with unused DVSS
49	DVSS	—	Ground for digital circuit
50	VCOE3	—	Connects with unused DVSS
51	DVSS	—	Ground for digital cirucuit
52	DVDD	—	Power supply for digital cirucuit
53	SUBC	O	CD sub-code (ODC)
54	BLKCLK	O	CD sub-code synchronous signal (ODC)/Jump output of one at DVD
55	MONC	O	Monitor terminal C
56	NCLDCK	O	Sub-code data freme clock (ODC)
57	LRCK	O	LR channnel data strove circCIRC(ODC)
58	NTRON	O	L: Tracking ON (ODC)
59	DVSS	—	Ground for digital cirucuit
60	DAT0	O	CIRC / Binary making DVD data output
61	DAT1	O	CIRC / Binary making DVD data output
62	DAT2	O	CIRC / Binary making DVD data output
63	DAT3	O	CIRC / Binary making DVD data output
64	CHCK4	O	Synchronous clock of DAT0～3
65	DVSS	—	Ground for digital circuit
66	DACCLK	O	
67	DACLRCK	I	Connects with unused DVSS
68	DACDATA	I	Connects with unused DVSS
69	CIRCIRQ	O	RAM with built-in CIRC exceeds / Underflow interrupt
70	IPFLAG	O	CIRC error flag
71	MOND	O	Monitor terminal D
72	TX	O	Digital audio interface
73	DVSS	—	Ground for digital cirucuit
74	DVDD	—	Power supply for digital cirucuit
75	AVSS	—	Ground for analog cirucuit
76	VREFLAD	—	AD subordinate position standard voltage (0.6±0.1v)
77	VREFMAD	—	It is a place standard voltage in AD (1.4±0.1V)
78	VREFHAD	—	High-ranking AD standard voltage (2.2±0.1V)
79	AVDD	—	Power supply for analog circuit
80	VREFC(AD12)	I	
81	JIOUT(AD11)	I	Jitter signal(FEP)
82	LDCUR(AD10)	I	Laser drive current signal
83	VREFOP	—	Operation amplifier standard voltage(VREFC)
84	RFENV(AD9)	I	RFENV(FEP)
85	N.C.(AD8)	I	Connects with VREFC
86	N.C.(AD7)	I	Connects with VREFC
87	TG(AD6)	I	Tangential Phase difference (FEP)
88	VREFHDA	—	High-ranking AD standard voltage (2.2±0.1V)
89	VREFMDA	—	It is a place standard voltage in AD (1.4±0.1V)
90	VREFLDA	—	AD subordinate position standard voltage (0.6±0.1v)
91	TE(AD5)	I	Tracking error (FEP)
92	TROFS(AD4)	I	Tracking drive IC input offset
93	FE(AD3)	I	Focus error (FEP)

Pin No.	Symbol	I/O	Function
94	FS(AD2)	I	FS (FEP)
95	TS(AD1)	I	TS (FEP)
96	AVSS	—	Ground for analog cirucuit
97	AVDD	—	Power supply for analog circuit
98	FBAL(DA1)	O	Focus balance(FEP)
99	FC(DA2)	O	Cutting off frequency (FEP)
100	BOOST(DA3)	O	Amount of boost (FEP)
101	TBAL(DA4)	O	DSL offset balance (FEP)
102	FODRV(DA5)	O	Focus drive
103	TRDRV(DA6)	O	Tracking drive
104	TRSDRVA(DA7)	O	Traverse drive A aspect
105	TRSDRVB(DA8)	O	Traverse drive B aspect
106	DVDD	—	Power supply for digital cirucuit
107	OFTR	I	Off-track error signal (FEP)
108	TKCRS1	I	Track crossing signal 1 (FEP)
109	TKCRS2	I	Track crossing signal 2 (FEP)
110	DSLO	I	Binary making data slice signal (FEP)
111	FG	I	FG signal input (spindle motor driver)
112	MINTEST	—	Connects with DVSS
113	TEST	—	Connects with DVSS
114	XRESET	I	Reset L : Reset
115	IREF1	—	VCO reference current 1(for SYSCLK)
116	DVSS	—	Ground for digital circuit)
117	VCOF1	—	VCO control voltage 1 (for SYSCLK)
118	SYSCLK	I	33.8MHz system clock input
119	DVSS	—	Ground for digital circuit
120	EC(PWM3A)	O	Spindle motor drive
121	ECR(PWM3B)	O	
122	N.C.(PWM3A)	O	
123	N.C.(PWM2B)	O	
124	N.C.(PWM1A)	O	
125	CDDVD	O	CD/DVD control signal (FEP) CD : H DVD : L
126	N.C.(PWM0A)	O	
127	N.C.(PWM0B)	O	
128	FEPNTRON	O	Tracking ON (FEP)

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■STK402-030 (IC301) :

1.Pin layout
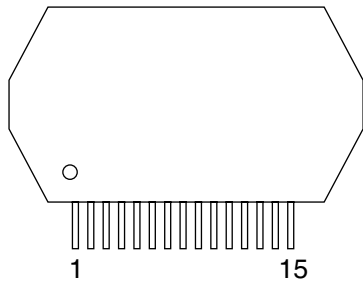
2.Block diagram
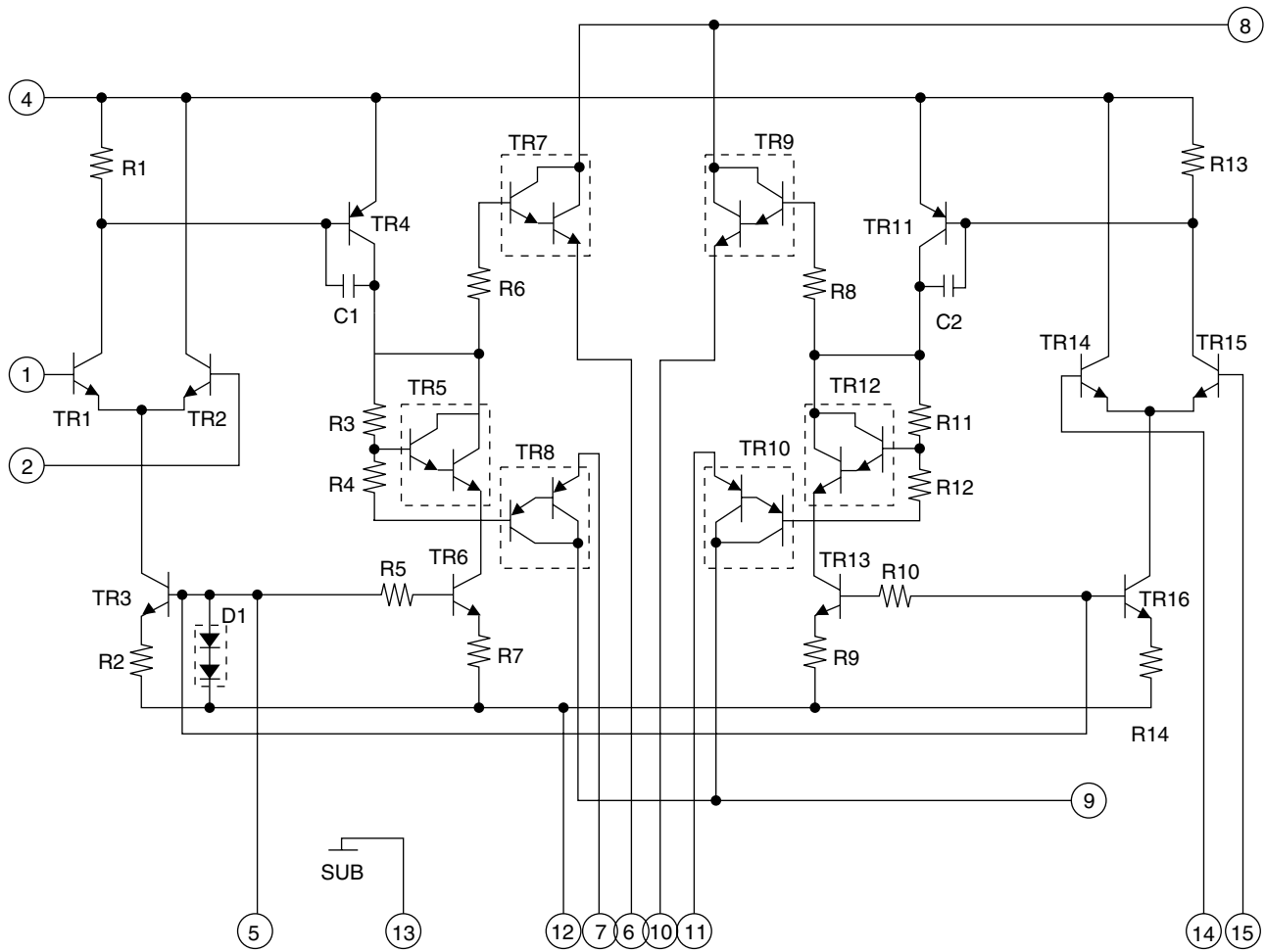
■ TC74VHC00FT-X (IC503) : Wright timing control

1.Terminal layout / Block diagram

Vcc 4B 4A 4Y 3B 3A 3Y
14 13 12 11 10 9 8

1 2 3 4 5 6 7
1A 1B 1Y 2A 2B 2Y GND
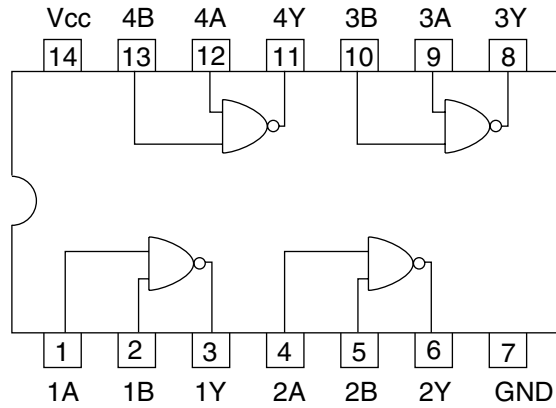
■ TC74VHC08FT-X (IC420) : NAND gate

1. Pin layout & Block diagram

1A 1   14 Vcc
1B 2   13 4B
1I 3   12 4A
2A 4   11 4Y
2B 5   10 3B
2Y 6   9 3A
GND 7   8 3Y
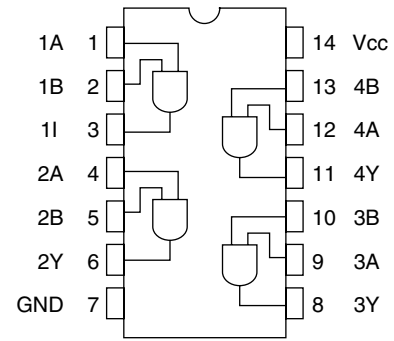
■ TC7SH32FU-X (IC312) : Timing control

1.Terminal layout

IN B 1   5 VCC
IN A 2
GND 3   4 OUT Y
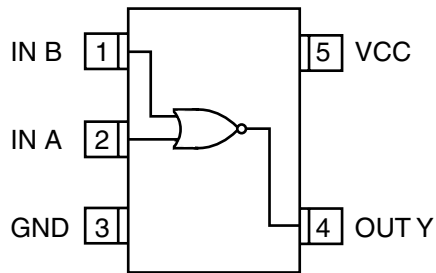
■ TC7SHU04FU-X (IC371,IC372): Clock generator

1. Terminal layout

IN B 1   5 VCC
IN A 2
GND 3   4 OUT Y
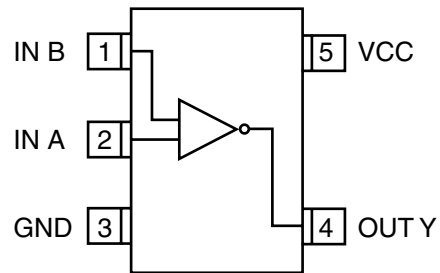
■ TC7SH08FU-X(IC311) : Timing control

1.Terminal layout

IN B 1   5 VCC
IN A 2
GND 3   4 OUT Y
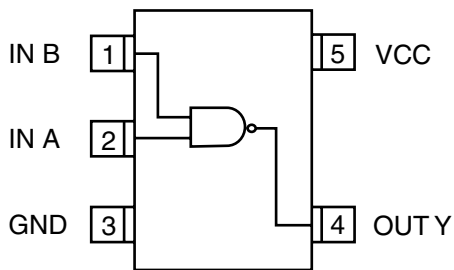
■ TC7W125FU-X (IC452) : Buffer

1. Terminal layout

2. Block diagram

Pin	Signal
$\overline{G1}$ 1	
A1 2	
Y2 3	
GND 4	

Pin	Signal
8	Vcc
7	$\overline{C2}$
6	Y1
5	A2
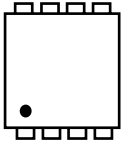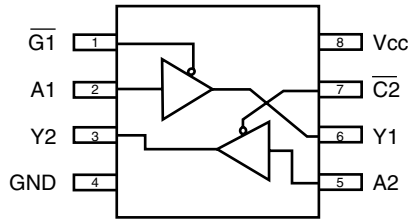
■ TC7WH74FU-X (IC374) : Clock buffer

1. Terminal layout

2. Block diagram

CK	1	8	VCC
D	2	7	$\overline{PR}$
$\overline{Q}$	3	6	$\overline{CLR}$
GND	4	5	Q
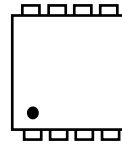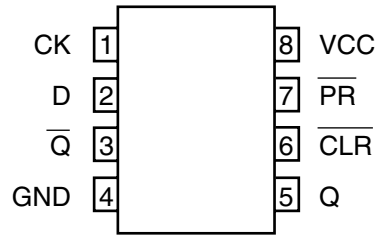
■ UPD42280GU-30-X (IC552) : 2M FRAM

1.Terminal Layout

```
         UPD42280GU-XX
DI0   ┤1            28├  DO0
DI1   ┤2            27├  DO1
DI2   ┤3            26├  DO2
DI3   ┤4            25├  DO3
WE    ┤5            24├  RE
GND   ┤6            23├  GND
TEST  ┤7            22├  OE
WRST  ┤8            21├  RRST
WCK   ┤9            20├  RCK
VDD   ┤10           19├  VDD
DI4   ┤11           18├  DO4
DI5   ┤12           17├  DO5
DI6   ┤13           16├  DO6
DI7   ┤14           15├  DO7
```
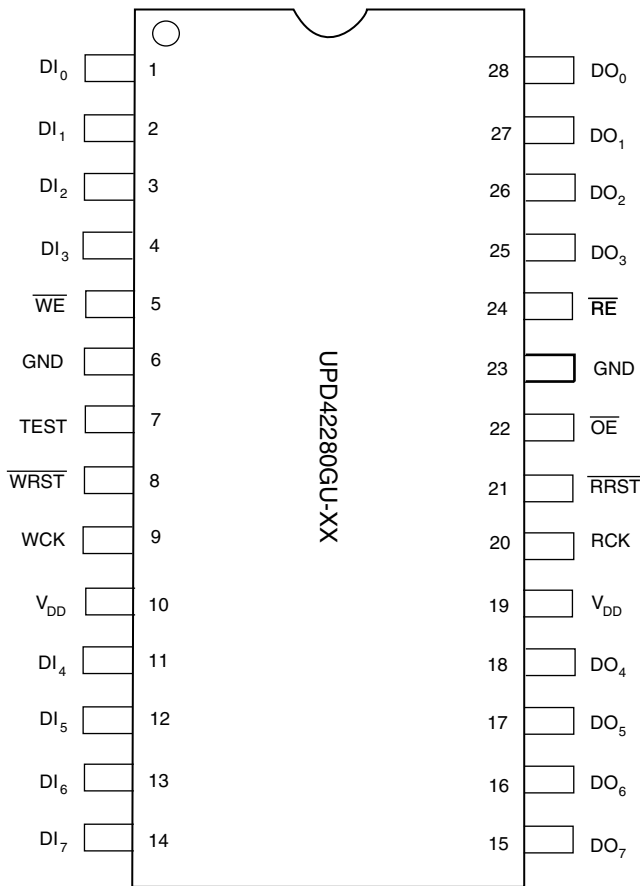
2.Pin Function

Pin No.	Symbol	I/O	Function
1~4	DI0~DI3	I	Data input
5	$\overline{WE}$	I	Write enable input
6	GND	-	Connect to GND
7	TEST	-	Connect to GND
8	$\overline{WRST}$	I	Write reset input
9	WCK	I	Write clock input
10	V_{DD}	-	Powre supply +5V
11~14	DI4~DI7	I	Data input
15~18	DO7~DO4	O	Data output
19	V_{DD}	-	Power supply +5V
20	RCK	I	Read clock input
21	$\overline{RRST}$	I	Read reset input
22	$\overline{OE}$	I	Output enable input
23	GND	-	Connect to GND
24	$\overline{RE}$	I	Read enable input
25~28	DO3~DO1	O	Data output

3.Block diagram

TH-A10
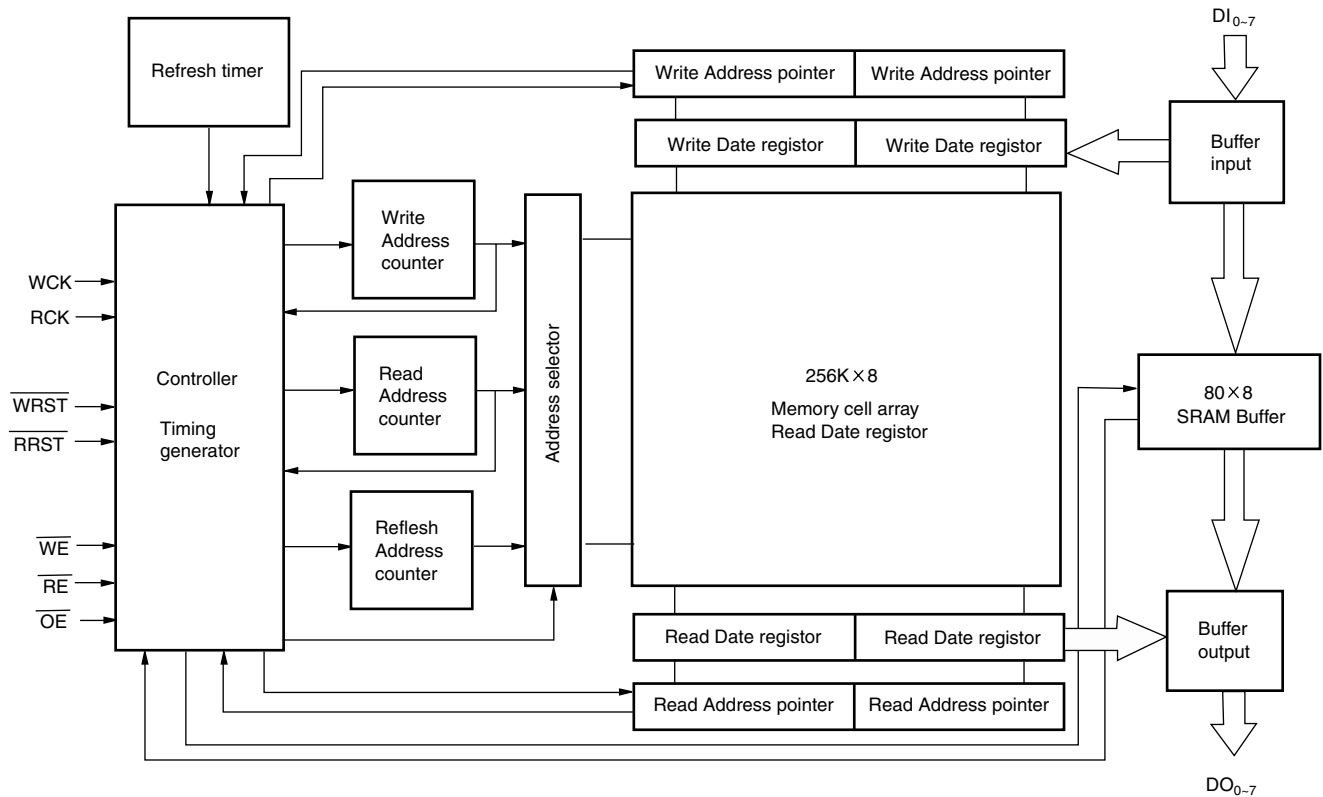
3.Function

MN103007BGA(1/2)

Pin NO.	Symbol	I/O	Function	Pin NO.	Symbol	I/O	Function
1	HDD15	I/O	ATAPI data	48	CPUADR8	I	System control address
2	HDD0	I/O	ATAPI data	49	CPUADR7	I	System control address
3	HDD14	I/O	ATAPI data	50	CPUADR6	I	System control address
4	5VDD			51	CPUADR5	I	System control address
5	HDD1	I/O	ATAPI data	52	CPUADR4	I	System control address
6	HDD13	I/O	ATAPI data	53	CPUADR3	I	System control address
7	HDD2	I/O	ATAPI data	54	CPUADR2	I	System control address
8	VSS			55	CPUADR1	I	System control address
9	HDD12	I/O	ATAPI data	56	VSS		GND
10	VDD			57	CPUADR0	I	System control address
11	HDD3	I/O	ATAPI data	58	NCS	I	System control chip selection
12	HDD11	I/O	ATAPI data	59	NWR	I	System control wright
13	HDD4	I/O	ATAPI data	60	NRD	I	System control lead
14	HDD10	I/O	ATAPI data	61	VDD		Apply 3V
15	5VDD			62	CPUDT7		System control data
16	HDD5	I/O	ATAPI data	63	CPUDT6		System control data
17	HDD9	I/O	ATAPI data	64	PVPPDRAM	O	C=10000PF is connected
18	VSS						between VSS
19	HDD6	I/O	ATAPI data	65	PTESTDRAM	I	VSS connected
20	HDD8	I/O	ATAPI data	66	OVDDDRAM		
21	HDD7	I/O	ATAPI data	67	PVSSDRAM		
22	5VDD			68	CPUDT5		System control data
23	NRESET	I	ATAPI reset	69	CPUDT4		System control data
24	MASTER	I/O	ATAPI master / slave selection	70	CPUDT3		System control data
25	NINT0	O	System control interruption 0	71	VSS		GND
26	NINT1	O	System control interruption 1	72	CPUDT2		System control data
27	WAITODC	O	System control weight control	73	CPUDT1	I/O	System control data
28	NMRST	O	System control reset	74	CPUDT0	I/O	System control data
29	DASPST	I	DASP signal initializing	75	CLKOUT1	O	16.9/11.2/8.45MHz clock
30	VDD			76	VDD	-	Apply 3V
31	OSCO2	I,O	VSS connection,OPEN	77	TEHLD	O	Mirror gate
32	OSCI2	I,O	VSS connection, OPEN	78	DTRO	O	Data part frequency control
33	UATASEL	I	VSS connection				switch
34	VSS			79	IDGT	O	Part CAPA switch
35	PVSSDRAM			80	BDO	I	RF dropout / BCA data of
36	PVDODRAM						making to binary
37	CPUADR17	I	System control address	81	CPDET2	I	Outer side CAPA detection
38	CPUADR18	I	System control address	82	CPDET1	I	Side of surroundings on inside
39	VSS			83	VSS		GND
40	CPUADR15	I	System control address	84	MMOD	I	VSS connected
41	CPUADR14	I	System control address	85	NRST	I	System reset
42	CPUADR13	I	System control address	86	VDD	-	Apply 3V
43	CPUADR12	I	System control address	87	CLKOUT2	O	16.9MHz clock
44	VDD		System control address	88	PLLOK	O	Frame mark detection
45	CPUADR11	I	System control address	89	IDOHOLD	O	ID gate for tracking holding
46	CPUADR10	I	System control address	90	JMPINH	O	Jump prohibition
47	CPUADR9	I	System control address				

Pin Function (2/3)

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
51	ARAM-ADDR14	-	Connect to TP564	97	E-VSS	-	Connect to GND
52	TEST-PIN1	-	Test pin	98	M-ADDR11	O	Address output to IC508,504
53	M-DATA15	I/O	Data bus I/O to IC508,IC504	99	M-ADDR8	O	Address output to IC508,504
54	M-DATA0	I/O	Data bus I/O to IC508,IC504	100	M-ADDR10	O	Address output to IC508,504
55	E-VDD	-	Power supply	101	E-VDD	-	Power supply
56	M-DATA14	I/O	Data bus I/O to IC508,IC504	102	M-ADDR7	O	Address output to IC508,504
57	E-VSS	-	Connect to GND	103	E-VSS	-	Connect to GND
58	M-DATA1	I/O	Data bus I/O to IC508,IC504	104	M-ADDR0	O	Address output to IC508,504
59	M-DATA13	I/O	Data bus I/O to IC508,IC504	105	M-ADDR6	O	Address output to IC508,504
60	M-DATA2	I/O	Data bus I/O to IC508,IC504	106	M-ADDR1	O	Address output to IC508,504
61	E-VDD	-	Power supply	107	E-VDD	-	Power supply
62	M-DATA12	I/O	Data bus I/O to IC508,IC504	108	M-ADDR5	O	Address output to IC508,504
63	E-VSS	-	Connect to GND	109	E-VSS	-	Connect to GND
64	M-DATA3	I/O	Data bus I/O to IC508,IC504	110	M-ADDR2	O	Address output to IC508,504
65	I-VDD	-	Power supply	111	M-ADDR4	O	Address output to IC508,504
66	M-DATA11	I/O	Data bus I/O to IC508,IC504	112	M-ADDR3	O	Address output to IC508,504
67	I-VSS	-	Connect to GND	113	E-VDD	-	Power supply
68	M-DATA14	I/O	Data bus I/O to IC508,IC504	114	M-ADDR12	-	Connect to TP513
69	E-VDD	-	Power supply	115	E-VSS	-	Connect to GND
70	M-DATA10	I/O	Data bus I/O to IC508,IC504	116	M-ADDR13	-	Connect to TP514
71	E-VSS	-	Connect to GND	117	I-VDD	-	Power supply
72	M-DATA5	I/O	Data bus I/O to IC508,IC504	118	M-ADDR14	-	Connect to TP515
73	M-DATA9	I/O	Data bus I/O to IC508,IC504	119	I-VSS	-	Connect to GND
74	M-DATA6	I/O	Data bus I/O to IC508,IC504	120	M-ADDR15	-	Connect to TP516
75	E-VDD	-	Power supply	121	M-ADDR16	-	Connect to TP517
76	M-DATA8	I/O	Data bus I/O to IC508,IC504	122	M-ADDR17	-	Connect to TP518
77	E-VSS	-	Connect to GND	123	E-VDD	-	Power supply
78	M-DATA7	I/O	Data bus I/O to IC508,IC504	124	M-ADDR18	-	Connect to TP519
79	LDQM	O	Lower DQ mask enable	125	E-VSS	-	Connect to GND
80	UDQM	O	Upper DQ mask enable	126	M-ADDR19	-	Connect to TP520
81	E-VDD	-	Power supply	127	M-ADDR20	-	Connect to TP521
82	$\overline{\text{MWE}}$	O	Write enable	128	$\overline{\text{ROM-CS}}$	-	Connect to TP522
83	E-VSS	-	Connect to GND	129	TEST-PIN2	-	Test pin
84	SD-CLK	O	System clock signal output	130	OSD-CLK	-	Connect to TP523
85	$\overline{\text{SD-CAS}}$	O	column address strobe	131	OSD-DATA0	-	Connect to TP525
86	$\overline{\text{SD-RAS}}$	O	Row address strobe	132	OSD-DATA1	-	Connect to TP526
87	E-VDD	-	Power supply	133	TEST-PIN3	-	Test pin
88	$\overline{\text{SD-CS1}}$	O	Chip select output to IC508	134	E-VDD	-	Power supply
89	E-VSS	-	Connect to GND	135	OSD-DATA2	-	Connect to TP528
90	$\overline{\text{SD-CSO}}$	O	Chip select output to IC504	136	E-VSS	-	Connect to GND
91	I-VDD	-	Power supply	137	OSD-DATA3	-	Connect to TP529
92	$\overline{\text{EDO-CAS}}$	-	Connect to TP511	138	TEST-PIN4	-	Test pin
93	I-VSS	-	Connect to GND	139	OSD-BLK1	-	Connect to TP531
94	$\overline{\text{EDO-RAS}}$	-	Connect to TP512	140	OSDVC1	-	Connect to TP532
95	E-VDD	-	Power supply	141	TEST-PIN5	-	Test pin
96	M-ADDR9	O	Address output to IC508,504	142	VDATA0	O	DVD image signal output

Pin Function (3/3)

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
143	VDATA1	O	DVD image signal output	176	A-VDD	-	Connect to TP507
144	I-VDD	-	Power supply	177	VCLK	I/O	Dot clock signal output (27MHz)
145	VDATA2	O	DVD image signal output	178	SYSCLK	-	Connect to TP505
146	I-VSS	-	Connect to GND	179	A-VSS	-	Connect to GND
147	TEST-PIN6	-	Test pin	180	DVD-DATA0	I	ATAPI data I/O to IC301
148	VDATA3	O	DVD image signal output	181	E-VDD	-	Power supply
149	E-VDD	-	Power supply	182	DVD-DATA1	I	ATAPI data I/O to IC301
150	VDATA4	O	DVD image signal output	183	E-VSS	-	Connect to GND
151	E-VSS	-	Connect to GND	184	DVD-DATA2	I	ATAPI data I/O to IC301
152	VDATA5	O	DVD image signal output	185	DVD-DATA3	I	ATAPI data I/O to IC301
153	TEST-PIN7	-	Test pin	186	DVD-DATA4	I	ATAPI data I/O to IC301
154	VDATA6	O	DVD image signal output	187	DVD-DATA5	I	ATAPI data I/O to IC301
155	VDATA7	O	DVD image signal output	188	DVD-DATA6	I	ATAPI data I/O to IC301
156	TEST-PIN8	-	Test pin	189	DVD-DATA7	I/O	ATAPI data I/O to IC301
157	$\overline{\text{HSYNC}}$	I/O	Horizontal synchronous signal output	190	TEST-PIN10	-	Test pin
158	$\overline{\text{VSYNC}}$	I/O	Vertical synchronous signal output	191	V-REQUEST	O	Master/Sleave Selection for ATAPI
159	IEC-958	O	Digital audio data output	192	V-STROBE	I	Host address for ATAPI
160	E-VDD	-	Power supply	193	I-VDD	-	Power supply
161	DA-DATA0	O	Data output to IC702	194	A-REQUEST	-	Connect to TP539
162	E-VSS	-	Connect to GND	195	I-VSS	-	Connect to GND
163	DA-DATA1	O	Data output to IC702	196	V-DACK	I	Host interrupt input for ATAPI
164	DA-DATA2	O	Data output to IC702	197	E-VDD	-	Power supply
165	DA-DATA3	O	Data output to IC702	198	SECT-SYNC	I	Host write for ATAPI
166	DA-LRCK	O	L/R clock output to IC702	199	E-VSS	-	Connect to GND
167	DA-BCK	O	Bit clock output to IC702	200	ERROR	-	Connect to GND
168	I-VDD	-	Power supply	201	HOST-SEL	-	Connect to GND
169	DA-XCK	-	Non connect	202	HADDR0	I	System control address input
170	I-VSS	-	Connect to GND	203	HADDR1	I	System control address input
171	DAI-DATA	-	Connect to TP501	204	HADDR2	I	System control address input
172	DAI-LRCK	I	L/R clock input from IC702	205	DTACK-SEL	-	Connect to GND
173	DAI-BCK	I	Bit clock input from IC702	206	$\overline{\text{CS}}$	I	Chip select for ZIVA
174	TEST-PIN9	-	Test pin	207	$\overline{\text{R/W}}$	I	Write enable
175	CLK-SEL	-	Connect to GND	208	$\overline{\text{RD}}$	I	Read enable

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