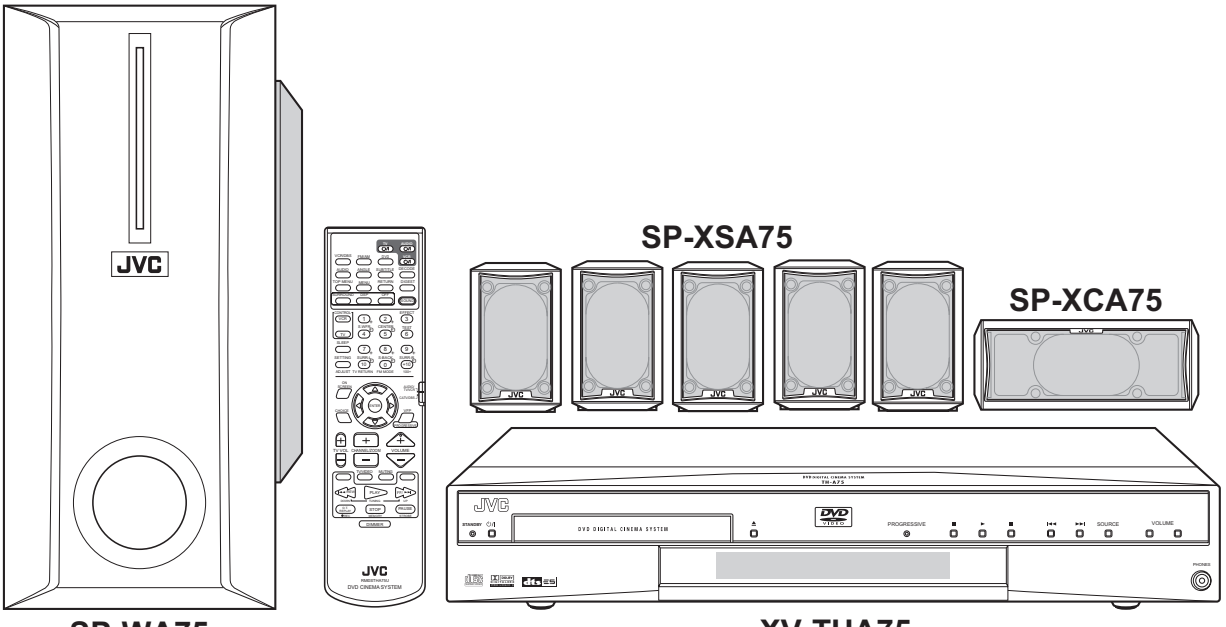
JVC

SERVICE MANUAL

DVD DIGITAL CINEMA SYSTEM

TH-A75



Area Suffix	
US	Singapore
UP	Korea
UT	Taiwan
UX	Saudi Arabia

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No.22009
2003/02

SECTION 1
Important Safety Precautions

1.1 Safety Precautions

(1) This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.

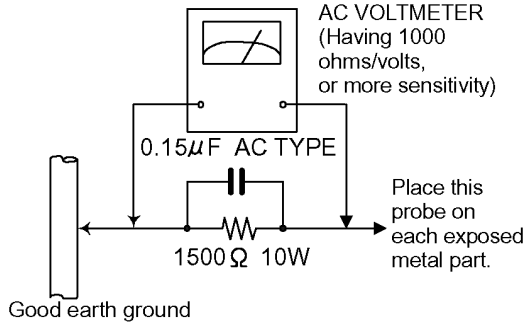
(2) Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturers warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.

(3) Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.

(4) The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after reassembling.

(5) Leakage shock hazard testing)
After reassembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
Do not use a line isolation transformer during this check.

- Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.).
- Alternate check method
  Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500 ohm 10W resistor paralleled by a 0.15 µF AC-type capacitor between an exposed metal part and a known good earth ground.
  Measure the AC voltage across the resistor with the AC voltmeter.
  Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and measure the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. Voltage measured any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



1.2 Warning

(1) This equipment has been designed and manufactured to meet international safety standards.

(2) It is the legal responsibility of the repairer to ensure that these safety standards are maintained.

(3) Repairs must be made in accordance with the relevant safety standards.

(4) It is essential that safety critical components are replaced by approved parts.

(5) If mains voltage selector is provided, check setting for local voltage.

1.3 Caution

Burrs formed during molding may be left over on some parts of the chassis.
Therefore, pay attention to such burrs in the case of preforming repair of this system.

1.4 Critical parts for safety

In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (▬), diode (▮) and ICP (●) or identified by the " ⚠ " mark nearby are critical for safety.
When replacing them, be sure to use the parts of the same type and rating as specified by the manufacturer. (Except the JC version)

1.5 Preventing static electricity

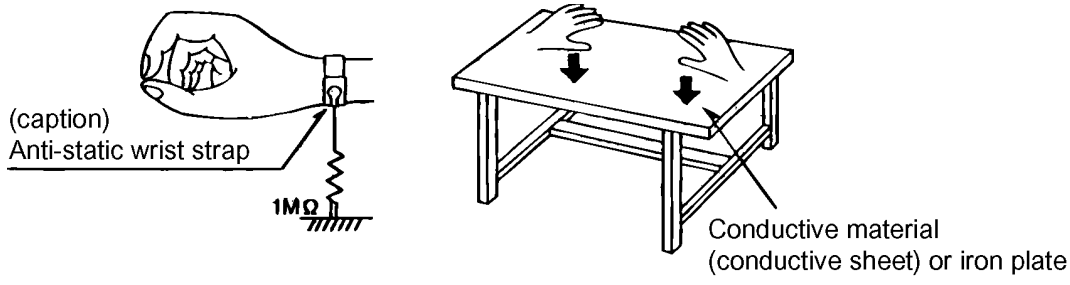
Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

1.5.1 Grounding to prevent damage by static electricity

Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

(1) Ground the workbench
Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

(2) Ground yourself
Use an anti-static wrist strap to release any static electricity built up in your body.



(3) Handling the optical pickup
- In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)
- Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

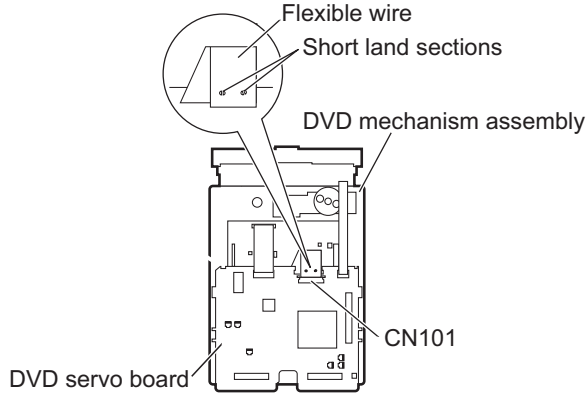
1.6 Handling the traverse unit (optical pickup)

(1) Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.
(2) Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.
(3) Handle the flexible cable carefully as it may break when subjected to strong force.
(4) I t is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it.

1.7 Attention when traverse unit is decomposed

***Please refer to "Disassembly method" in the text for the DVD pickup unit.**

- Apply solder to the short land sections before the flexible wire is disconnected from the connector CN101 on the DVD servo board. (If the flexible wire is disconnected without applying solder, the DVD pickup may be destroyed by static electricity.)
- In the assembly, be sure to remove solder from the short land sections after connecting the flexible wire.



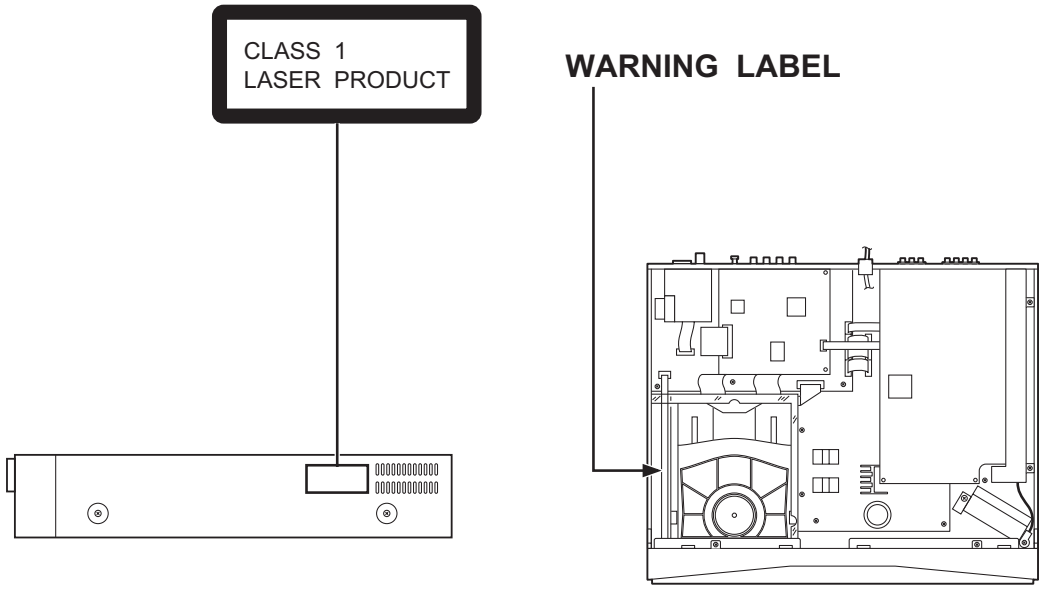
1.8 Important for laser products

(1) **CLASS 1 LASER PRODUCT**
(2) **DANGER :** Invisible laser radiation when open and inter lock failed or defeated. Avoid direct exposure to beam.
(3) **CAUTION :** There are no serviceable parts inside the Laser Unit. Do not disassemble the Laser Unit. Replace the complete Laser Unit if it malfunctions.
(4) **CAUTION :** The compact disc player uses invisible laser radiation and is equipped with safety switches which prevent emission of radiation when the drawer is open and the safety interlocks have failed or are de feated.
It is dangerous to defeat the safety switches.
(5) **CAUTION :** If safety switches malfunction, the laser is able to function.
(6) **CAUTION :** Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

⚠CAUTION
Please use enough caution not to see the beam directly or touch it in case of anadjustment or operation check.

VARNING Osynlig laserstrålning är denna del är öppnad och spårren är urkopplad. Betrakta ej strålen.	**ADVARSEL** Usynlig laserstråling ved åbning, når sikkerhedsafbrydere er ude af funktion. Undgå udsasttelse for stråling.
VARO Avattaessa ja suojalukitus ohitettaessa olet alttiina näkymättömälle lasersäteilylle. Älä katso säteeseen.	**ADVARSEL** Usynlig laserstråling ved åpning, når sikkerhetsbryteren er avslott. unngå utsettelse for stråling.

REPRODUCTION AND POSITION OF LABELS



SECTION 2
Disassembly method

2.1 Main body section

2.1.1 Removing the top cover (See Figs.1 to 4.)

(1) From the right and left sides of the main body, remove the four screws A attaching the top cover. (See Figs.1 and 2.)
(2) From the back side of the main body, remove the two screws B attaching the top cover. (See Fig.3.)
(3) Lift the rear section of the top cover, slide the top cover slightly in the direction of the arrow. (See Fig.4.)
(4) Disengage the engagement sections a of the top cover from the main body. (See Fig.4.)

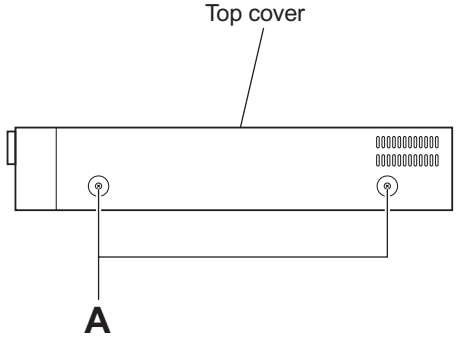


Fig.1

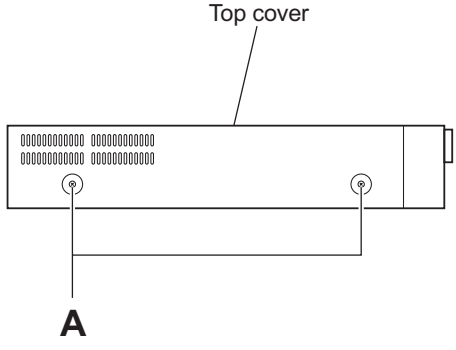


Fig.2

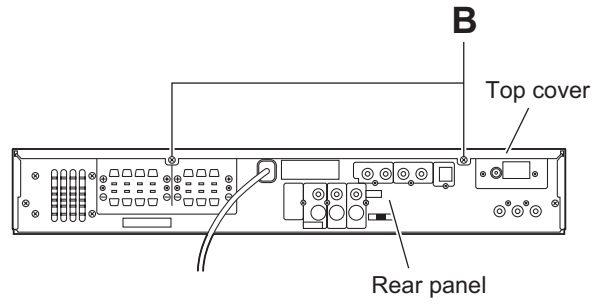


Fig.3

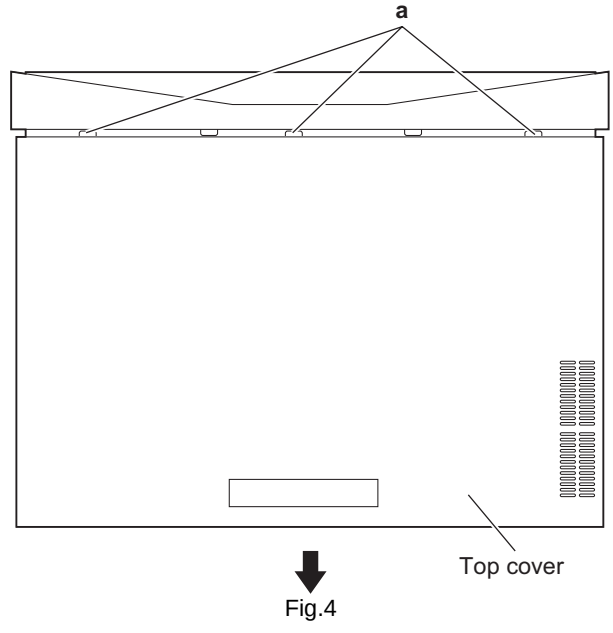


Fig.4

2.1.2 Removing the front panel assembly (See Figs.5 to 8.)

- Remove the top cover.
  (1) From the left side of the main body, push the section b of the slide cam using the screw driver, etc. (See Fig.5.)
  (2) Pull out the tray. (See Fig.5.)
  (3) Push the tray fitting assembly of the tray in the direction of the arrow and then remove the tray fitting assembly. (See Fig.6.)
  (4) Return the tray into the DVD mechanism assembly.
  (5) From the bottom side of the main body, remove the four screws C attaching the front panel assembly. (See Fig.7.)
  (6) From the top side of the main body, remove the two screws D attaching the front panel assembly. (See Fig.8.)
  (7) Disconnect the card wires from the connectors CN206 and CN207 on the main board. (See Fig.8.)
  (8) Remove the screw E attaching the lug wire. (See Fig.8.)
  (9) While opening the hooks c to the right and left sides of the front panel assembly in the direction of the arrow 1, remove the front panel assembly in the direction of the arrow 2. (See Fig.8.)

  Reference:

  In the assembly, through the card wire in the barrier and then hold the card wire to the sections d of the barrier. (See Fig.8.)

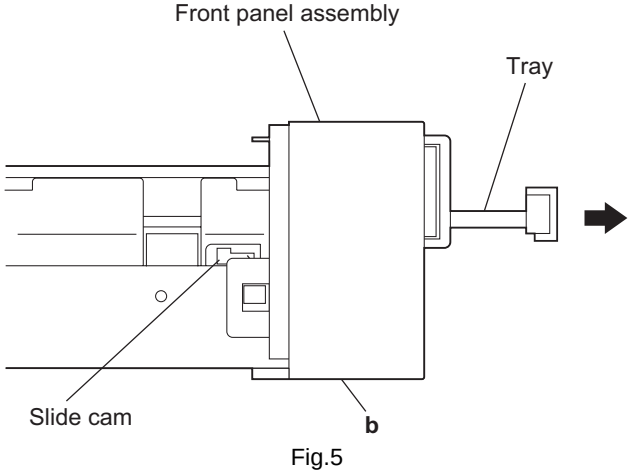


Fig.5

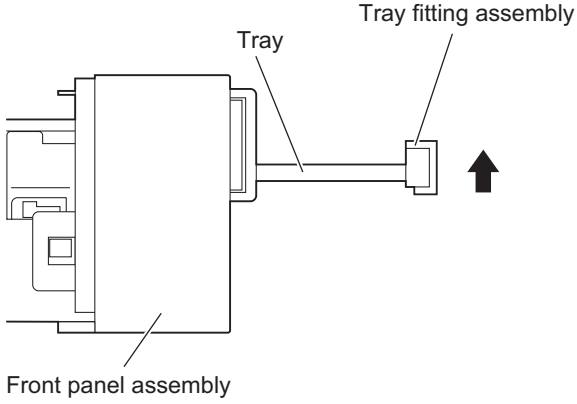


Fig.6

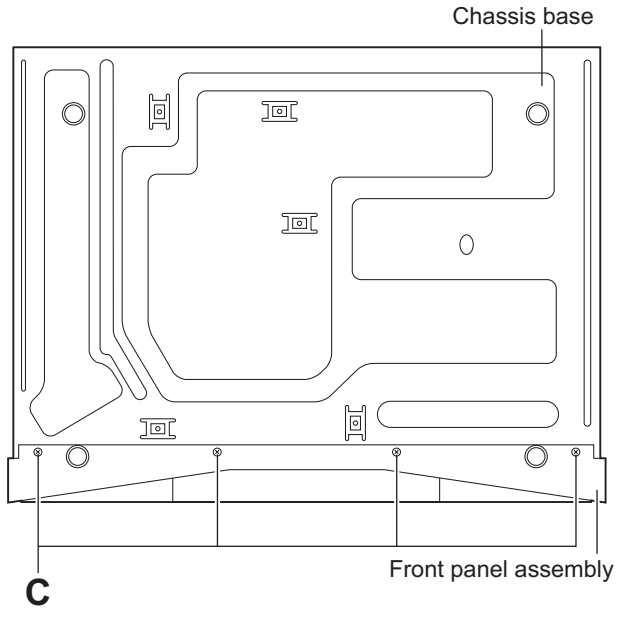


Fig.7

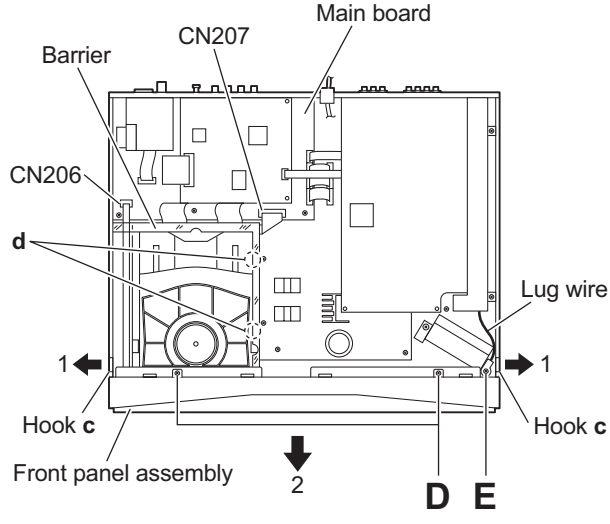


Fig.8

2.1.3 Removing the DVD mechanism assembly (See Fig.9.)

- Remove the top cover.
- Remove the front panel assembly.
  (1) From the top side of the main body, remove the barrier.
  (2) Disconnect the card wires from the connectors CN208 and CN209 on the main board.
  (3) Remove the three screws F attaching the DVD mechanism assembly.
  (4) Take out the DVD mechanism assembly from the chassis base.

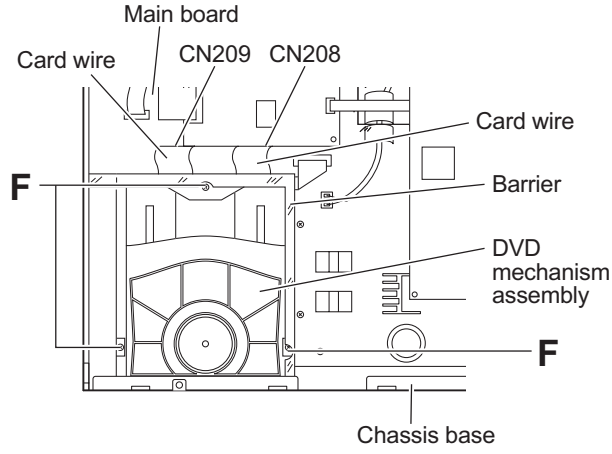


Fig.9

2.1.4 Removing the DSP board (See Figs.10 and 11.)

- Remove the top cover.
  (1) From the top side of the main body, disconnect the card wires from the connectors CN591 and CN592 on the DSP board. (See Fig.10.)
  (2) From the back side of the main body, remove the three screws G attaching the DSP board. (See Fig.11.)
  (3) Remove the DSP board from the section e of the barrier, take out the DSP board. (See Fig.10.)

  Reference:

  When attaching the DSP board, hang the DSP board to the section e of the barrier. (See Fig.10.)

2.1.5 Removing the tuner (See Figs.10 and 11.)

- Remove the top cover.
  (1) From the top side of the main body, disconnect the card wire from the connector CN1 on the tuner. (See Fig.10.)
  (2) From the back side of the main body, remove the two screws H attaching the tuner. (See Fig.11.)

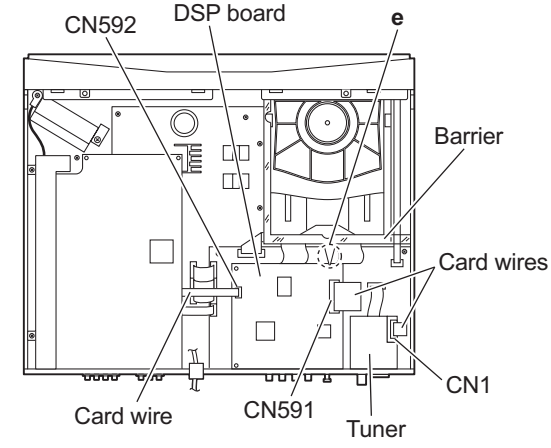


Fig.10

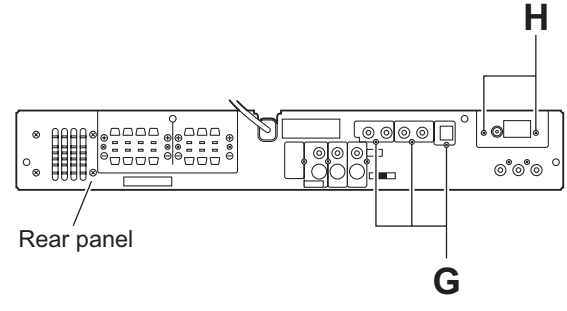


Fig.11

2.1.6 Removing the main board (See Figs.12 and 13.)

- Remove the top cover.
- Remove the DSP board.
- Remove the tuner.

(1) From the top side of the main body, disconnect the card wires from the connectors (CN201, CN202, CN204, CN206-CN209) on the main board. (See Fig.12.)
(2) Remove the screw J and two screws K attaching the main board. (See Fig.12.)
(3) From the back side of the main body, remove the five screws L attaching the main board. (See Fig.13.)

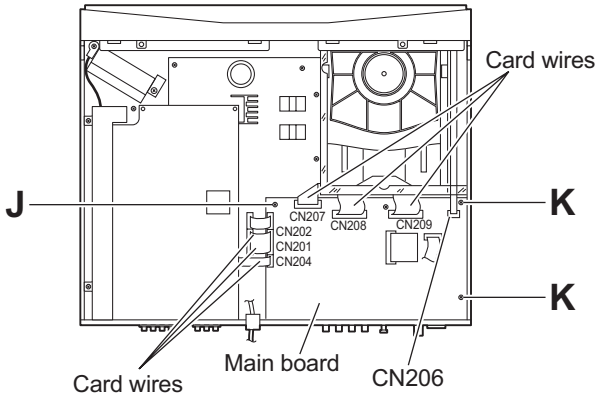


Fig.12

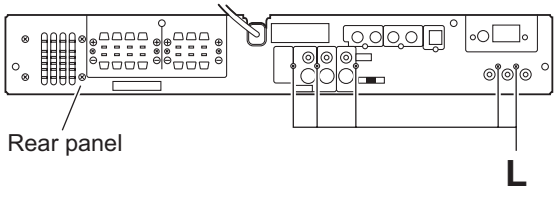


Fig.13

2.1.7 Removing the amplifier board (See Figs.14 to 16.)

- Remove the top cover.

(1) From the top side of the main body, disconnect the card wires from the connectors CN701 and CN702 on the amplifier board (See Fig.14.)
(2) Remove the three screws M attaching the amplifier board. (See Fig.14.)
(3) From the back side of the main body, remove the four screws N attaching the amplifier board. (See Fig.15.)
(4) Disconnect the connector CN703 on the amplifier board, take out the amplifier board. (See Fig.14.)
(5) Remove the six screws P attaching the heat sink to the amplifier board. (See Fig.16.)

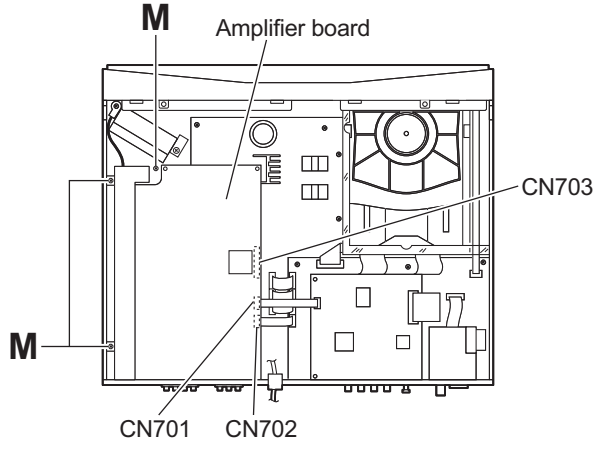


Fig.14

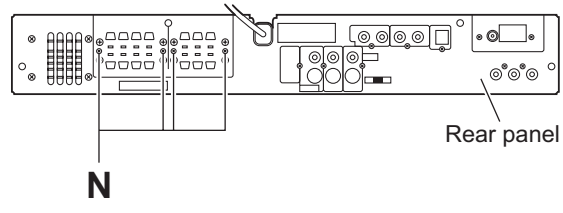


Fig.15

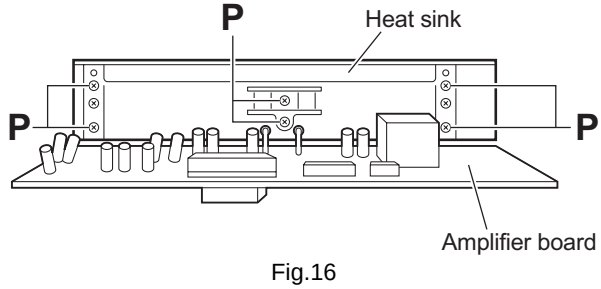


Fig.16

2.1.8 Removing the fan motor (See Figs.17 and 18.)

- Remove the top cover.
- Remove the amplifier board.

(1) From the top side of the main body, remove the fan cover. (See Fig.17.)
(2) Remove the tie band banding the fan motor wire and then disconnect the fan motor wire from the connector CN174 on the power board. (See Fig.17.)
(3) Remove the screw Q and screw R attaching the fan bracket. (See Fig.17.)
(4) Remove the two screws S attaching the fan motor to the fan bracket. (See Fig.18.)

Reference:

When attaching the screw Q, attach the lug wire of the front panel assembly at the same time.

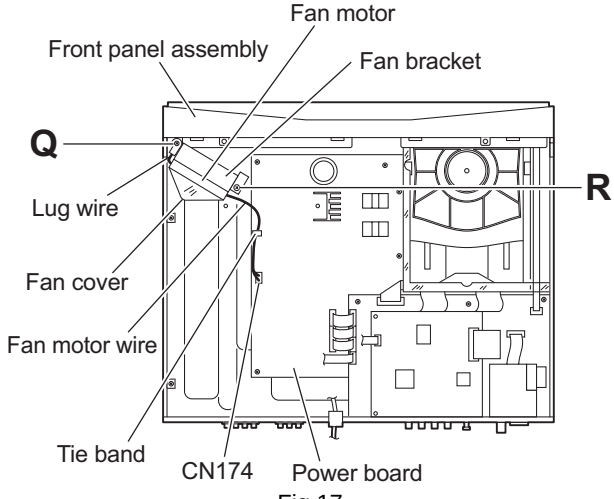


Fig.17

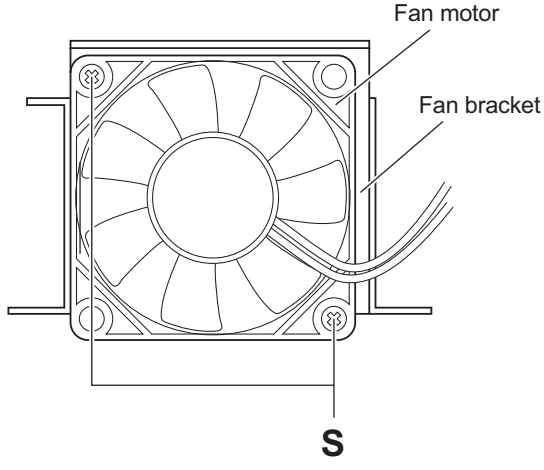


Fig.18

2.1.9 Removing the power board (See Fig.19.)

- Remove the top cover.
- Remove the amplifier board.

(1) From the top side of the main body, disconnect the card wires from the connectors CN172 and CN173 on the power board.
(2) Remove the tie band banding the fan motor wire and then disconnect the fan motor wire from the connector CN174 on the power board.
(3) Disconnect the power cord from the connector CN101 on the power board.
(4) Remove the screw T and three screws U attaching the power board.

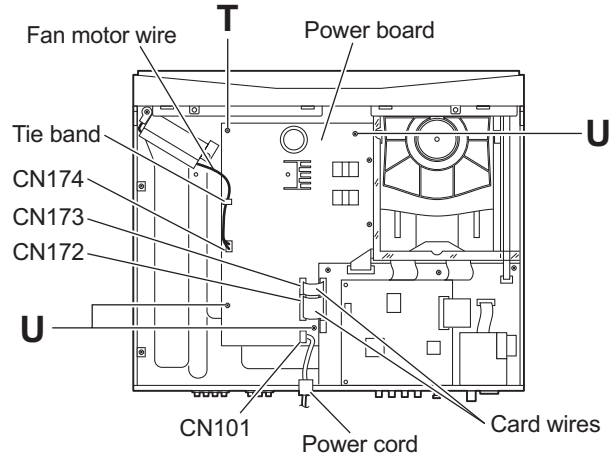


Fig.19

2.2 Front panel assembly section

- Remove the top cover.
- Remove the front panel assembly.

2.2.1 Removing the jack board (See Fig.1.)

(1) From the inside of the front panel assembly, disconnect the wire from the connector CN403 on the switch board.
(2) Remove the two screws V attaching the jack holder, take out the jack board together the jack holder.

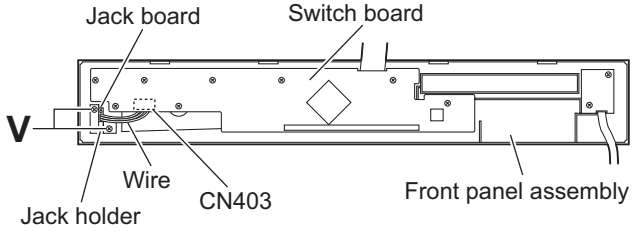


Fig.1

2.2.2 Removing the switch board (See Figs.2 and 3.)

(1) From the inside of the front panel assembly, disconnect the wire from the connector CN403 on the switch board. (See Fig.2.)
(2) Remove the eight screws W attaching the switch board, take out the switch board. (See Fig.2.)

Reference:

In the assembly, attach the switch board after attaching the push buttons and light lens as before. (See Fig.3.)

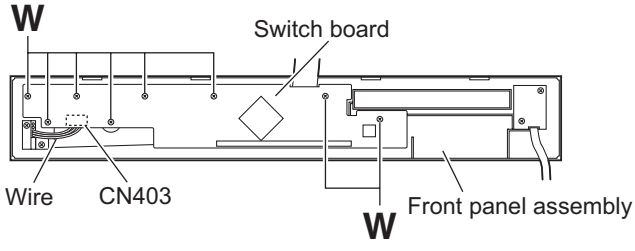


Fig.2

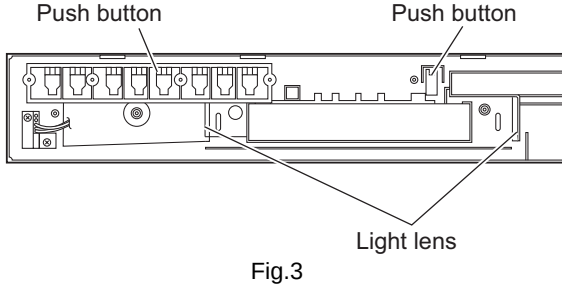


Fig.3

2.2.3 Removing the standby board (See Fig.4.)

From the inside of the front panel assembly, remove the two screws X attaching the standby board.

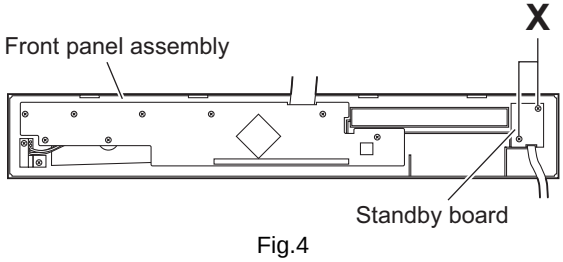


Fig.4

2.3 DVD mechanism section

- Remove the top cover.
- Remove the DVD mechanism assembly.

2.3.1 Removing the tray (See Figs.1 and 2.)

(1) From the left side of the DVD mechanism assembly, push the slide cam in the direction of the arrow 1 and then pull out the tray in the direction of the arrow 2. (See Fig.1.)
(2) Push the tray stoppers a in the direction of the arrow 3, pull out the tray in the direction of the arrow 4. (See Fig.2.)

2.3.2 Attaching the tray (See Fig.2.)

When attaching the tray, insert the tray to the rail of the DVD mechanism assembly and then push the tray in the DVD mechanism assembly.

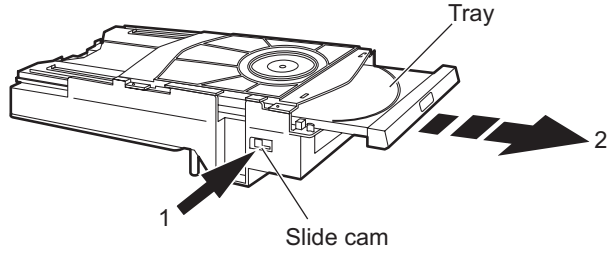


Fig.1

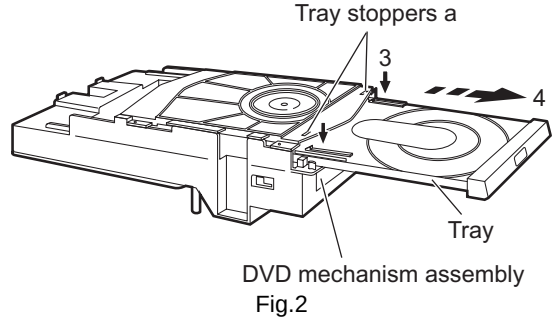


Fig.2

2.3.3 Removing the tray (See Fig.3.)

(1) From the bottom side of the DVD mechanism assembly, disconnect the card wires from the connectors CN201 and CN202 on the DVD servo board.

Caution:

Be sure to solder the short land sections b on the flexible wire before disconnecting the flexible wire from connector CN101 on the DVD servo board.

If the flexible wire is disconnected without attaching solder, the DVD pickup unit may be destroyed by static electricity.

(2) Release the locks of the connector CN101 (in the direction of the arrow 1) on the DVD servo board, disconnect the flexible wire.

(3) Release the locks of the connector CN101 on the DVD servo board in the direction of the arrow 1, disconnect the flexible wire.

Caution:

In the assembly, be sure to remove solders from the short land sections b after connecting the flexible wire to the connector CN101 on the DVD servo board.

(4) While pushing the claw c of the DVD mechanism assembly in the direction of the arrow 2, remove the DVD servo board in an upward direction.

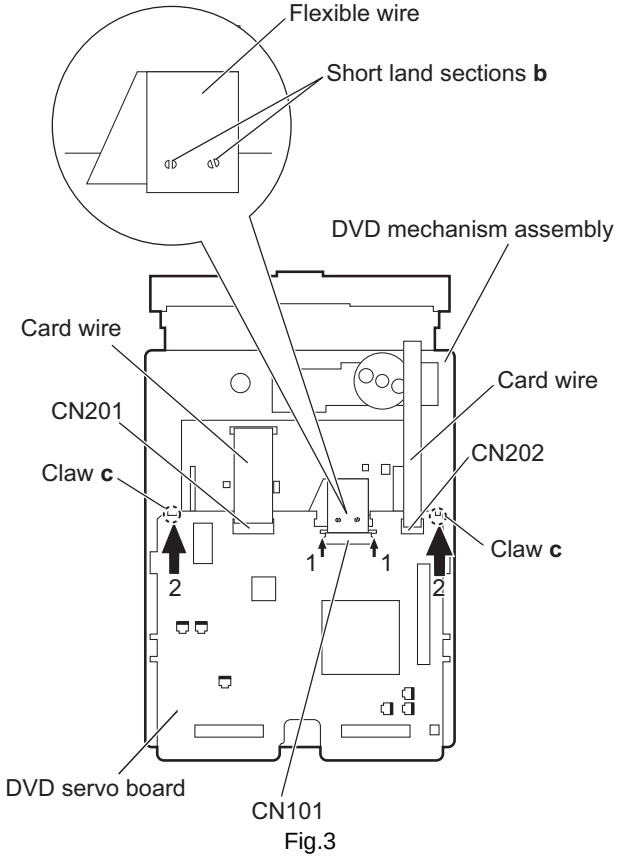


Fig.3

2.3.4 Removing the clamper base (See Fig.4.)

(1) From the top side of the DVD mechanism assembly, remove the four screws A attaching the clamper base.

(2) Remove the clamper base from the bosses d of the loading base in an upward direction, remove the clamper base from the sections e while sliding it in the direction of the arrow.

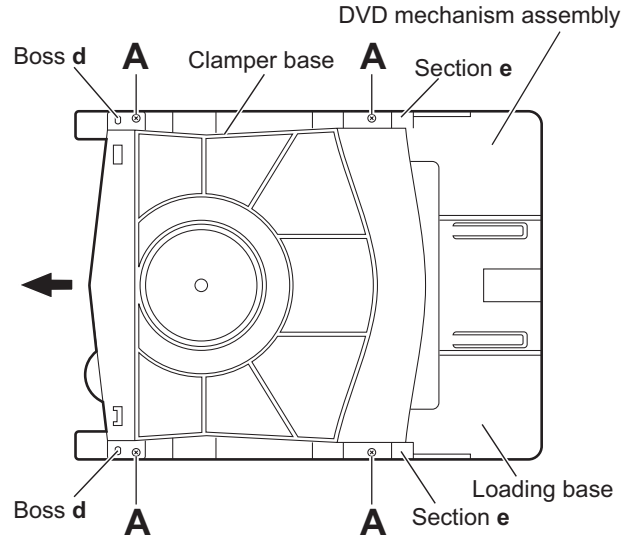


Fig.4

2.3.5 Removing the tray drive board (See Fig.5.)

- Remove the clamper base.

(1) From the bottom side of the DVD mechanism assembly, remove the solders from the soldered sections f on the tray drive board.

(2) Remove the screw B attaching the tray drive board to the DVD mechanism assembly.

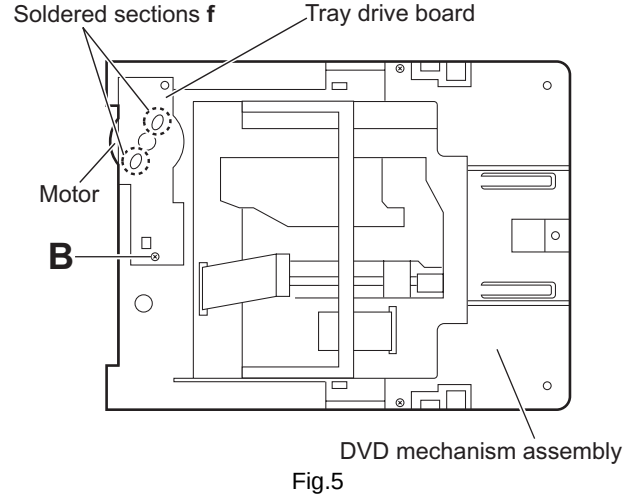


Fig.5

2.3.6 Removing the motor (See Fig.6.)

- Remove the clamper base.
- Remove the tray drive board.

(1) From the top side of the DVD mechanism assembly, remove the belt of the pulley gear.

Note:

Take care not to attach grease on the belt.

(2) Remove the screw C attaching the motor to the DVD mechanism assembly.

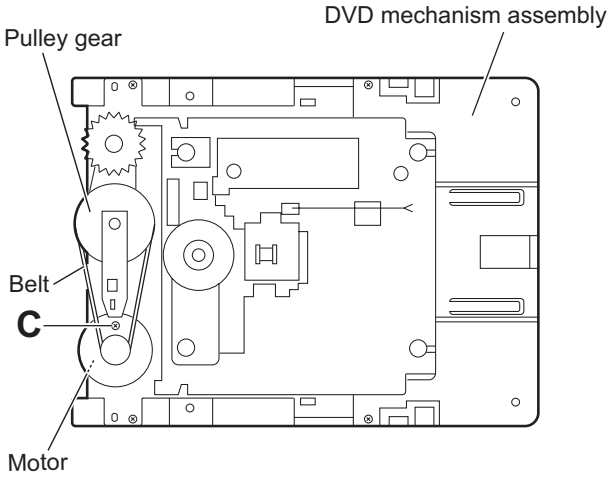


Fig.6

2.3.7 Removing the DVD traverse mechanism assembly (See Figs.7.)

- Remove the DVD servo board.
- Remove the clamper base.

(1) From the top side of the DVD mechanism assembly, remove the four screws D attaching the DVD traverse mechanism assembly to the loading base.

(2) Take out the DVD traverse mechanism assembly from the loading base.

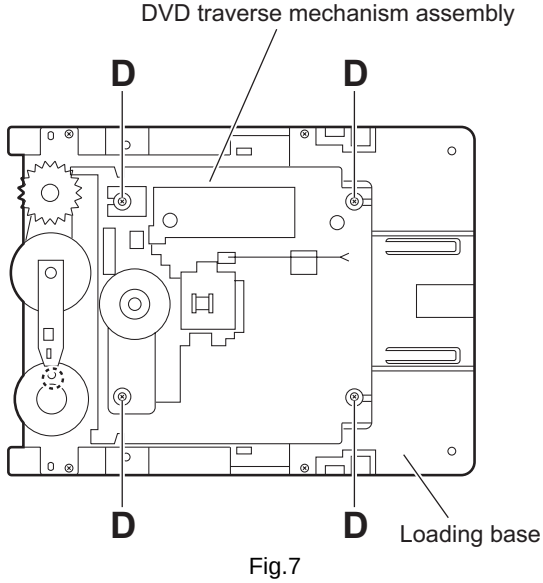


Fig.7

2.3.8 Removing the DVD pickup unit (See Figs.8 to 10.)

- Remove the DVD servo board.
- Remove the clamper base.
- Remove the DVD traverse mechanism assembly.

(1) From the top side of the DVD traverse mechanism assembly, remove the screw E attaching the plate and torsion spring. (See Fig.8.)

(2) Remove the shaft from the section g and then remove the shaft from the section h. (See Fig.9.)

(3) Disengage the section i of the DVD pickup unit and then remove the DVD pickup unit with the shaft.

(4) Pull the shaft out of the DVD pickup unit.

(5) Remove the two screws F attaching the SW. actuator.

2.3.9 Attaching the DVD pickup unit (See Figs.8,10 to 12)

Reference:

Refer to the explanation of "Removing the DVD pickup unit" on the preceding page.

(1) Attach the SW. actuator and shaft to the DVD pickup unit. (See Fig.10.)

(2) Engage the section i of the DVD pickup unit to the shaft of the DVD traverse mechanism assembly first, and set the both ends of the shaft of the DVD pickup unit in the sections g and h of the DVD traverse mechanism assembly. (See Fig.11.)

(3) Slide the DVD pickup unit all the way in the direction of the arrow. (See Fig.12.)

(4) Mesh the lead screw to the section j of DVD pickup unit and then set the end of the lead screw to the section k. (See Fig.12.)

(5) Attach the torsion spring. (See Fig.8.)

(6) Attach the plate. (See Fig.8.)

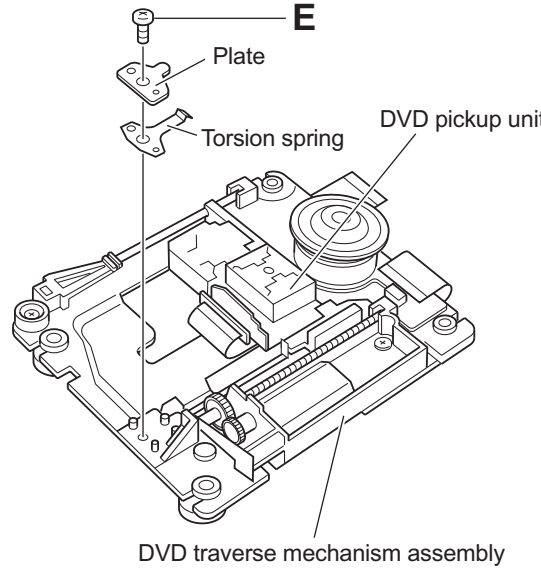


Fig.8

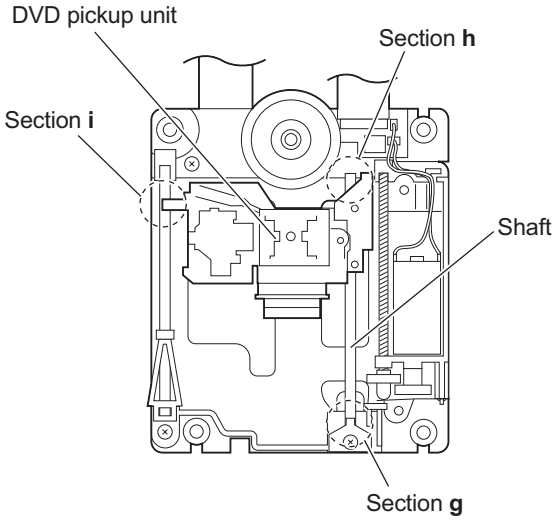


Fig.9

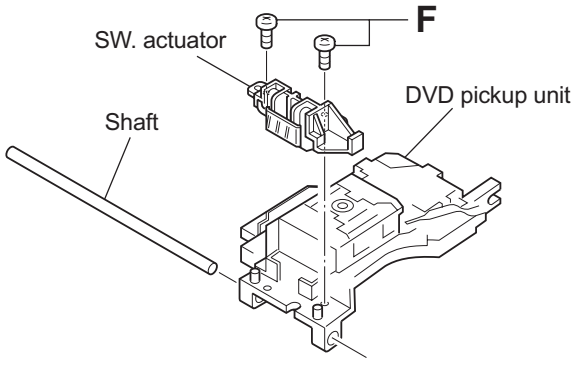


Fig.10

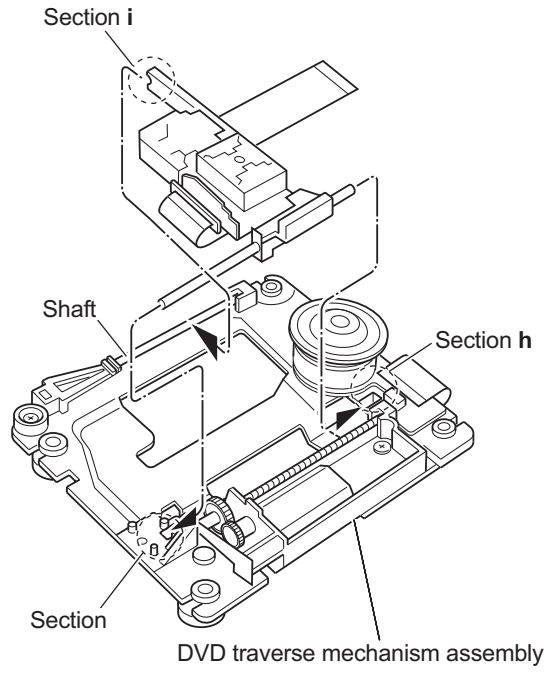


Fig.11

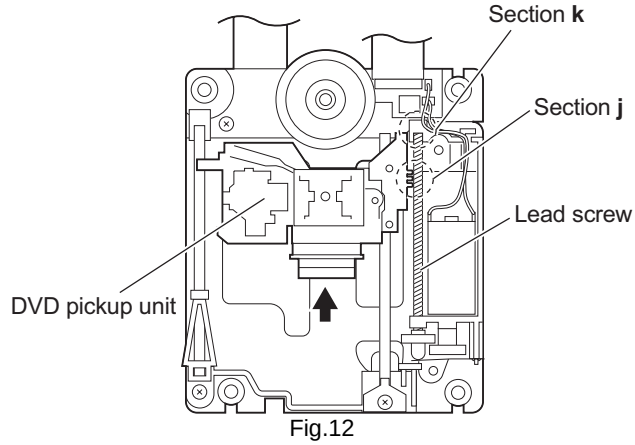


Fig.12

2.3.10 Removing the spindle motor board (See Figs.13 and 14.)

- Remove the DVD servo board.
- Remove the clamper base.
- Remove the DVD traverse mechanism assembly.

(1) From the top side of the DVD traverse mechanism assembly, remove the feed motor wire that is soldered to the spindle motor board. (See Fig.13.)

(2) From the bottom side of the DVD traverse mechanism assembly, remove the three screws G attaching the spindle motor board. (See Fig.14.)

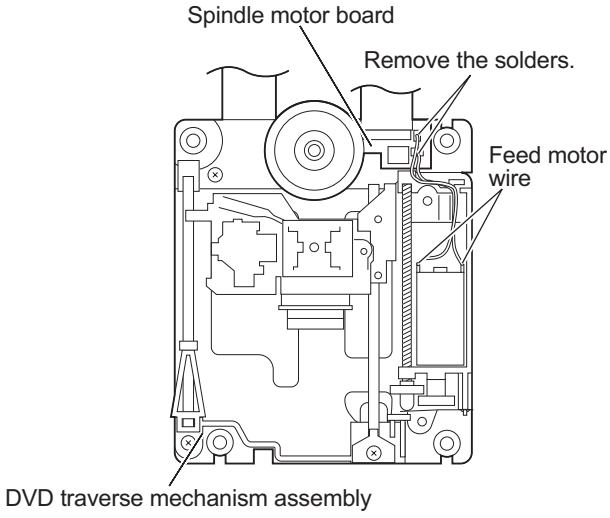


Fig.13

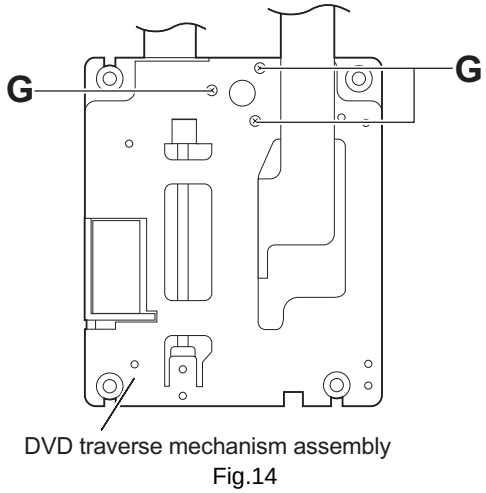


Fig.14

2.3.11 Removing the feed motor (See Figs.15 to 17.)

- Remove the DVD servo board.
- Remove the clamper base.
- Remove the DVD traverse mechanism assembly.

(1) From the top side of the DVD traverse mechanism assembly, remove the feed motor wire that is soldered to the spindle motor board. (See Fig.15.)

(2) Remove the screws H attaching the feed holder assembly and then take out the feed holder assembly. (See Fig.15.)

(3) Remove the screw J attaching the thrust spring. (See Fig.16.)

(4) Remove the feed gear and lead screw in the direction of the arrow. (See Fig.16.)

(5) Remove the two screws K attaching the feed motor. (See Fig.17.)

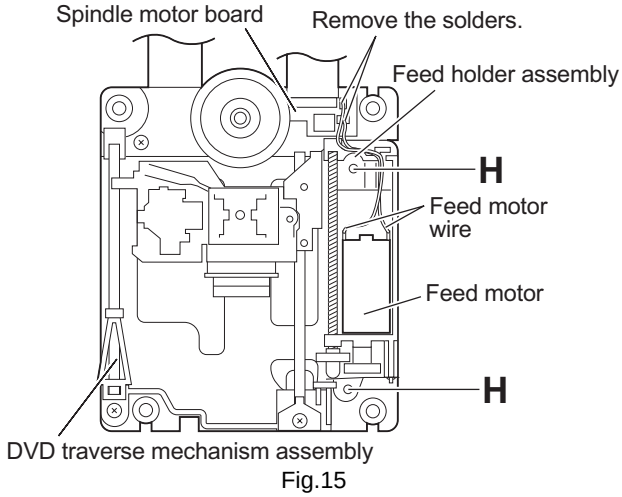


Fig.15

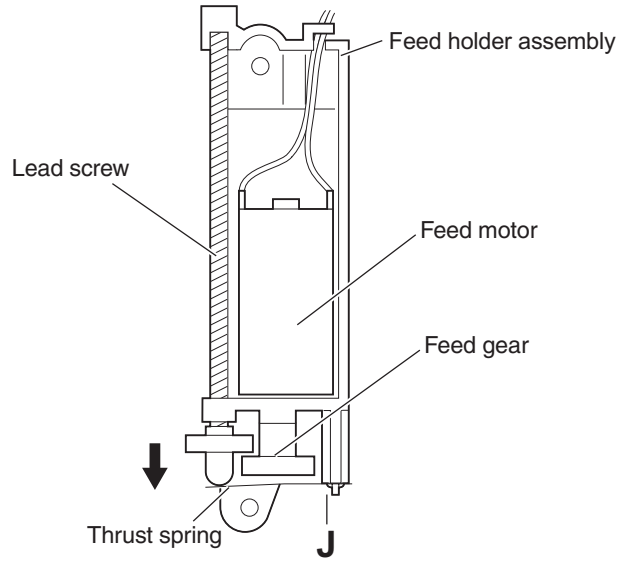


Fig.16

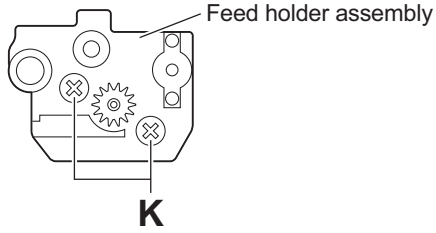


Fig.17

SECTION 3
Adjustment

3.1 Test mode

(1) The AC cord is connected after pushing the STOP key and the EJECT key of a main body.
(2) Change to test mode, FL indicate "TEST ??". (?? is version)
At this time, TV monitor indicate the firm number " ∗ ∗ ∗ ".
(3) Press PAUSE key of the main body, EEPROM initialize is start.
FL indicate "RDS", EEPROM initialize is complete.
(4) Release the test mode by power to off.

3.2 Up grade

3.2.1 How to UPGRADE

(1) Power to on then mode to DVD.
(2) Set the recorded disc.
(Down loaded the up grade program "TH-A75 -Firmware Update Procedure" from Audio Products DIV. Technological Material of JS-Net .)
(3) FL indicate "UPGRADE", press cursol ↑ key of the remote controller.
(4) TV monitor indication the UPGRADE condition.
(5) Upgrade is complete, disc is automatically eject then finish the upgrade.

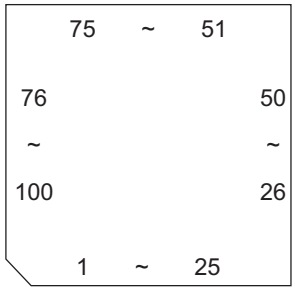
3.2.2 After UPGRADE

After upgrade, it is should done the EEPROM initialize and confirm the firm number.
(1) Tray close then release the AC cord.
(2) The AC cord is connected after pushing the STOP key and the EJECT key of a main body.
(3) Change to test mode, FL indicate "TEST ??". (?? is version)
In this time, confrim the TV monitor indicate the firm number "114".
(4) EEPROM initialize start by press the PAUSE key of main body.
FL indicate "RDS", EEPROM initialize is complete.
(5) Release the test mode by power to off.

SECTION 4
Description of major ICs

4.1 UPD784215AGC194 (IC531) : CPU

- Pin layout



- Pin function

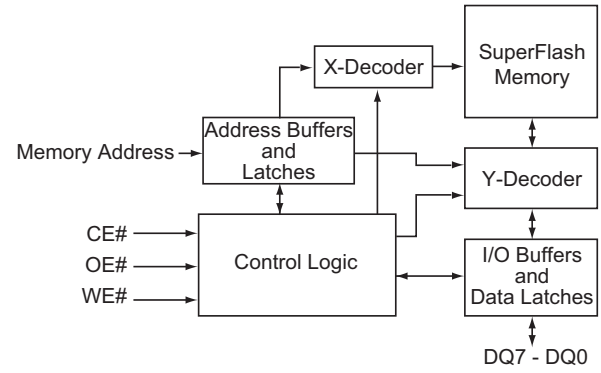
Pin No.	Symbol	I/O	Function
1~8	-	-	Not use
9	VDD	-	+3.0V
10	X2	I	Main system clock input
11	X1	I	Main system clock input
12	VSS	-	GND
13	XT2	-	OPEN
14	XT1	I	Connect to VSS
15	RESET	I	Reset for Flash write
16	-	-	Not use
17	INT0	I	Error input0 (detect UNLOCK)
18	INT1	I	Error input1 (detect Non Audio)
19	DZF	I	GND
20~22	-	-	Not use
23	AVDD	-	The same potential as VDD
24	AV REF0	-	The same potential as VSS
25	-	-	Not use
26	CS1	I	Chip select input port
27	CS2	I	Chip select input port
28	CS3	I	Chip select input port
29	CS4	I	Chip select input port
30~32	-	-	Not use
33	AVSS	-	The same potential as VSS
34, 35	-	-	Not use
36	AV REF1	-	The same potential as VDD
37	RX	O	For flash write
38	TX	O	For flash write
39	-	-	Not use
40	DSP_COM	I	Command (serial 1)
41	DSP_STS	O	Status (Serial 1)
42	DSP_CLK	I	Clock (Serial 1)
43	DSP_RDY	I	Ready
44	-	-	Not use
45	MIDIO_IN	I	Data in (Serial 0)
46	MIDIO_OUT	O	Data out (Serial 0)
47	MICK	O	Clock (Serial 0)

Pin No.	Symbol	I/O	Function
48	HREQ	I	HREQ
49	SS	O	Slave select
50,51	-	-	Not use
52	DSP_RST	O	DSP RESET
53	-	-	Not use
54	DA_CS	O	Chip select output
55	-	-	Not use
56	PD/DA	O	Power down output (RESET)
57	PD	O	Power down output (RESET)
58~63	-	-	Not use
64	CODEC_D-OUT	O	Data out
65	CODEC_D-IN	I	Data in
66	CODEC_CLK	O	Clock
67	CODEC_CS	O	Chip select output
68	DEBUG1	O	Debug out port
69	DEBUG2	O	Debug out port
70	DEBUG3	O	Debug out port
71	GEBUG4	O	Debug out port
72	GND	-	GND
73~75	-	-	Not use
76	EQ	O	EQ
77	CTR_TONE	O	Center tone
78	3D	O	3D-Phonic
79, 80	-	-	Not use
81	VDD	-	+3.0V
82, 83	-	-	Not use
84	ANA/T.TUNE	O	ANALOG./T.TONE
85	LFE.MIX	O	LFE MIX CONTROL
86	LEF_OUT	O	LFE OUT CONTROL
87	-	-	Not use
88	S.MUTE	O	S.MUTE
89~93	-	-	Not use
94	TEST	O	Usual "VSS"
95~100	-	-	Not use

4.2 39VF0207CWHQ01 (IC524) : 2 Mbit multi-purpose flash memory

- Pin layout

- Block diagram

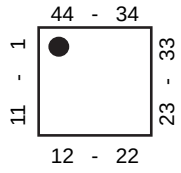


- Pin function

Pin No.	Symbol	Function
1 - 6	A11,A9,A8 A13,A14,A17	Address inputs
7	WE#	Write enable
8	VDD	Power supply
9	NC	Not connect
10 - 20	A16,A15,A12 A7 - A0	Address inputs
21 - 23	DQ0 - DQ2	Data inputs/outputs
24	VSS	Ground
25 - 29	DQ3 - DQ7	Data inputs/outputs
30	CE#	Chip enable
31	A10	Address input
32	OE#	Output enable

4.3 AK4586VQ (IC511) : A/D, D/A Converter

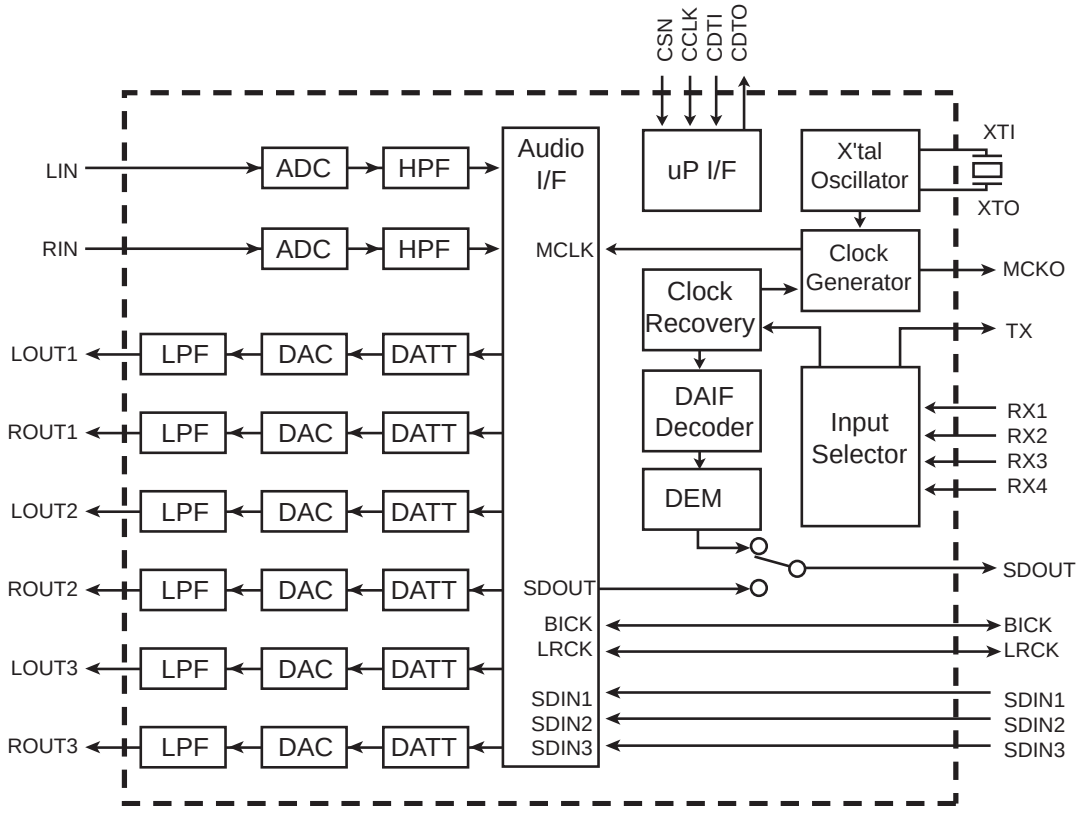
• Pin layout



• Pin function

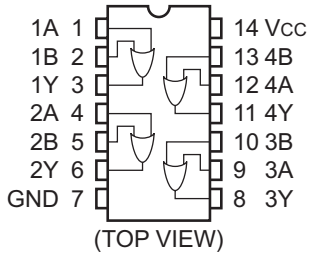
Pin No.	Symbol	I/O	Function
1	XTO	O	X'tal output pin
2	XTI	I	X'tal input pin
	EXTCLK	I	External master clock input pin
3	TVDD	-	Output buffer power supply pin, 2.7V~5.5V
4	VDSS	-	Digital Ground pin, 0V
5	DVDD	-	Digital power supply pin, 4.5V~5.5V
6	TX	O	Transmit channel (through data) output pin
7	MCKO	O	Master clock output pin
8	LRCK	I/O	Input/Output channel clock pin
9	BICK	I/O	Audio serial data clock pin
10	SDTO	O	Audio serial data output pin
11	SDTI1	I	DAC1 audio serial data input pin
12	SDTI2	I	DAC2 audio serial data input pin
13	SDTI3	I	DAC3 audio serial data input pin
14	INT0	O	Interrupt 0 pin
15	INT2	O	Interrupt 1 pin
16	CDTO	O	Control data output pin in 4-wire serial control mode
	CAD1	I	Chip address 1 pin in I2C bus control mode
17	CDTI	I	Control data input pin in 4-wire serial control mode
	SDA	I/O	Control data input/output pin in I2C bus control mode
18	CCLK	I	Control data clock pin in 4-wire serial control mode
	SCL	I	Control data clock pin in I2C bus control mode
19	CSN	I	Chip select pin in 4-wire serial control mode
	CAD0	I	Chip address 0 pin in I2C bus control mode
20	DZF2	O	Zero input detect 2 pin
	OVF	O	Analog input overflow detect pin
21	AVSS	-	Analog ground pin, 0V
22	AVDD	-	Analog power supply pin, 4.5V~5.5V
23	VREFH	I	Positive voltage reference input pin, AVDD
24	VCOM	O	Common voltage output pin, AVDD/2
25	DZF1	O	Zero input detect 1 pin
26	LOUT3	O	DAC3 Lch analog output pin
27	ROUT3	O	DAC3 Rch analog output pin
28	LOUT2	O	DAC2 Lch analog output
29	ROUT2	O	DAC2 Rch analog output pin
30	LOUT1	O	DAC1 Lch analog output pin
31	ROUT1	O	DAC1 Rch analog output pin
32	LIN	I	Lch analog input pin
33	RIN	I	Rch analog input pin
34	PCDD	-	PLL power supply pin, 4.5V~5.5V
35	R	-	External resistor pin
36	PVSS	-	Pll ground pin, 0V
37	RX4	I	Receiver channel 4 pin (internal biased pin)
38	SLAVE	I	Slave mode pin
39	RX3	I	Receiver channel 3 pin (internal biased pin)
40	TST	I	Test pin
41	RX2	I	Receiver channel 2 pin (internal biased pin)
42	I2C	I	Control mode select pin
43	RX1	I	Receiver channel 1 pin (internal biased pin)
44	PDN	I	Power-Down & Reset pin

- Block diagram



4.4 MM74HCT32MTC-X (IC521) : Quad 2 input OR gate

• Pin layout & Block diagram



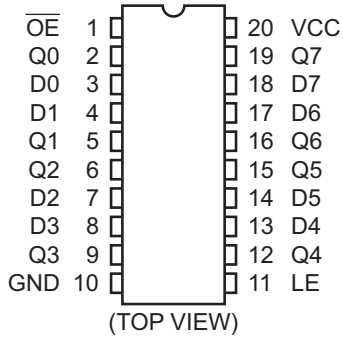
(TOP VIEW)

• Truth table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

4.5 74LCX373MTC-X (IC512,IC513) : Octal D-type latch

• Pin layout



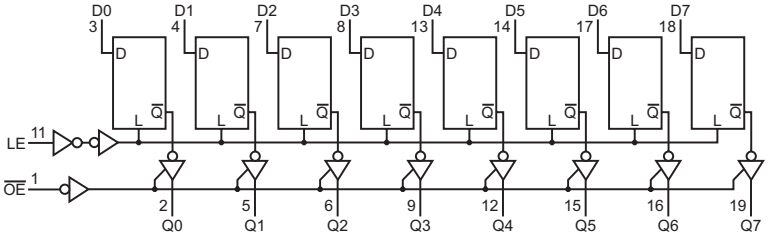
(TOP VIEW)

• Truth table

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Y
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

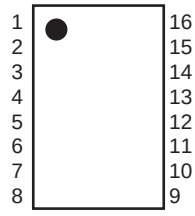
X: Don't care
Z: High impedance
Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

• Block diagram

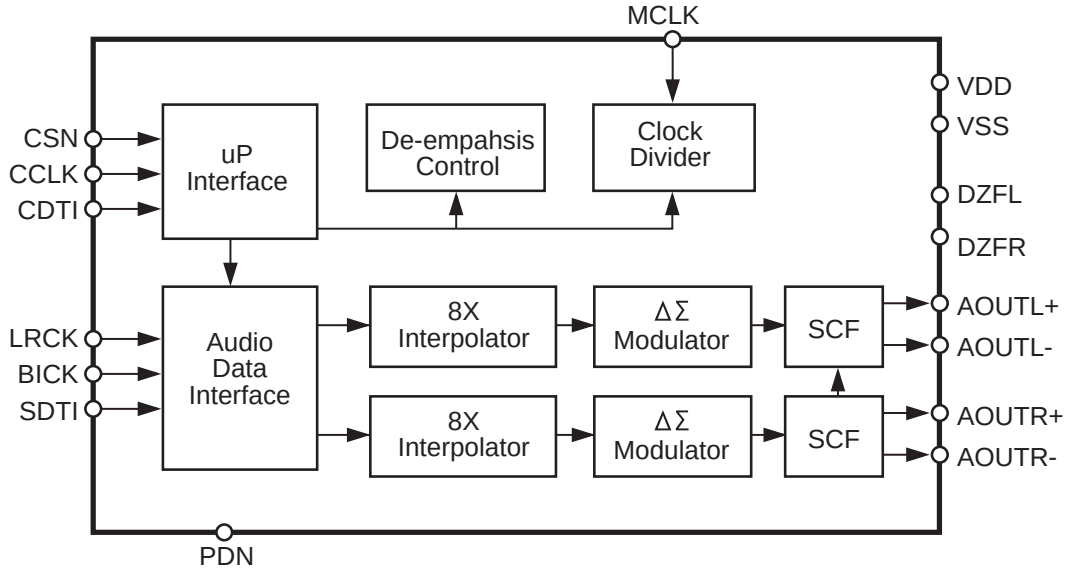


4.6 AK4382AVT-X (IC512) : D/A Converter

- Pin layout



- Block diagram

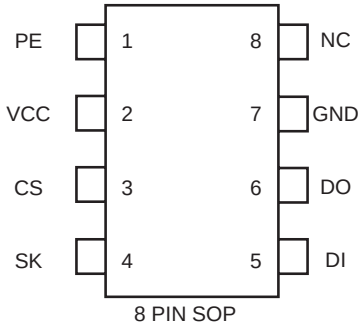


- Pin function

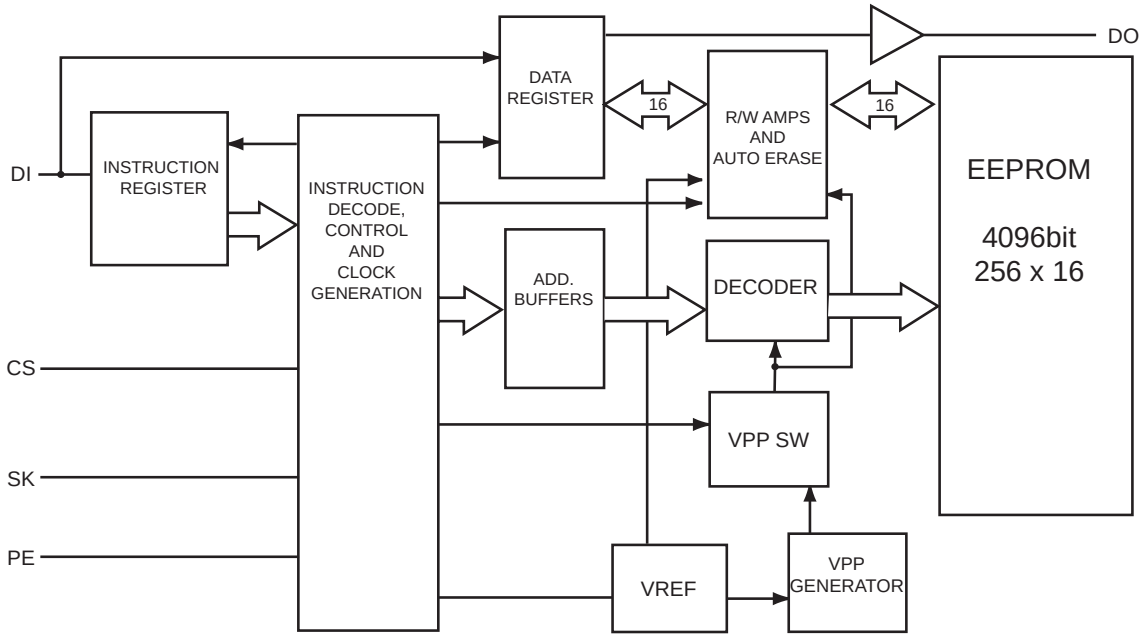
Pin No.	Symbol	I/O	Function
1	MCLK	I	Master Clock Input Pin
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin
5	PDN	I	Power-Down Mode Pin
6	CSN	I	Chip Select Pin
7	CCLK	I	Control Data Input Pin
8	CDTI	I	Control Data Input Pin
9	AOUTR-	O	Rch Negative Analog Output Pin
10	AOUTR+	O	Rch Positive Analog Output Pin
11	AOUTL-	O	Lch Negative Analog Output Pin
12	AOUTL+	O	Lch Positive Analog Output Pin
13	VSS	-	Ground Pin
14	VDD	-	Power Supply Pin
15	DZFR	O	Rch Data Zero Input Detect Pin
16	DZFL	O	Lch Data Zero Input Detect Pin

4.7 AK93C65AF-X (IC510) : EEPROM

- Pin layout



- Block diagram



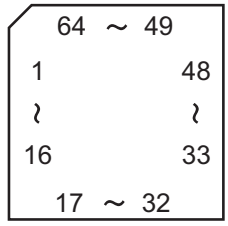
- Pin function

Pin no.	Symbol	Function
1	PE	Program enable (With built-in pull-up resistor)
2	VCC	Power supply
3	CS	Chip selection
4	SK	Cereal clock input
5	DI	Cereal data input
6	DO	Cereal data output
7	GND	Ground
8	NC	No connection

NOTE :
The pull-up resistor of the PE pin is about 2.5Mohm (VCC=5V)

4.8 AN8703FH-V (IC101) : Frontend processor for DVD

- Pin layout



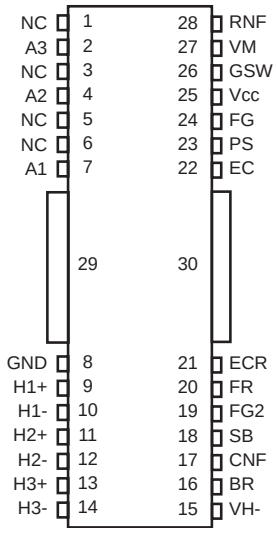
- Pin function

Pin No.	Symbol	I/O	Description
1	LPC1	I	Laser input terminal (DVD)
2	LPC01	O	Laser drive signal output terminal (DVD)
3	LPC2	I	Laser input terminal (CD)
4	LPC02	O	Laser drive signal output terminal (CD)
5	VFOSHORT	I	VFOSHORT control terminal
6	TBAL	I	Tracking balance control terminal
7	FBAL	I	Focus balance control terminal
8	POFLT	O	Track detection threshold level terminal
9	DTRD	I	Data slice part data read signal input terminal(For RAM)
10	IDGT	I	Data slice part address part gate signal input terminal(For RAM)
11	STANDBY	I	Standby mode control terminal
12	SEN	I	SEN(Serial data input terminal)
13	SCK	I	SCK(Serial data input terminal)
14	STDI	I	STDI(Serial data input terminal)
15	RSCL	I	Standard electric current terminal
16	JLINE	I	Electric current setting terminal of JLine
17	TEN	I	Reversing input terminal of tracking error output AMP.
18	TEOUT	O	Tracking error signal output terminal
19	AGCBAL	I	Offset adjusting terminal 1
20	ASOUT	O	Full adder signal output terminal
21	FEN	I	Focus error output amplifier reversing input terminal
22	FEOUT	O	Focus error signal output terminal
23	AGCOFST	I	Offset adjusting terminal 2
24	MON	-	Non connect
25	AGCLVL	O	Output amplitude adjustment for DRC
26	GND2	-	Connect to GND
27	VREF2	O	VREF2 voltage output terminal
28	VCC2	-	Power supply terminal 5V
29	VHALF	O	VHALF voltage output terminal
30	DFLTON	O	Reversing output terminal of filter AMP.
31	DFLTOP	O	Filter AMP. output terminal
32	DCFLT	I	Capacity connection terminal for filter output

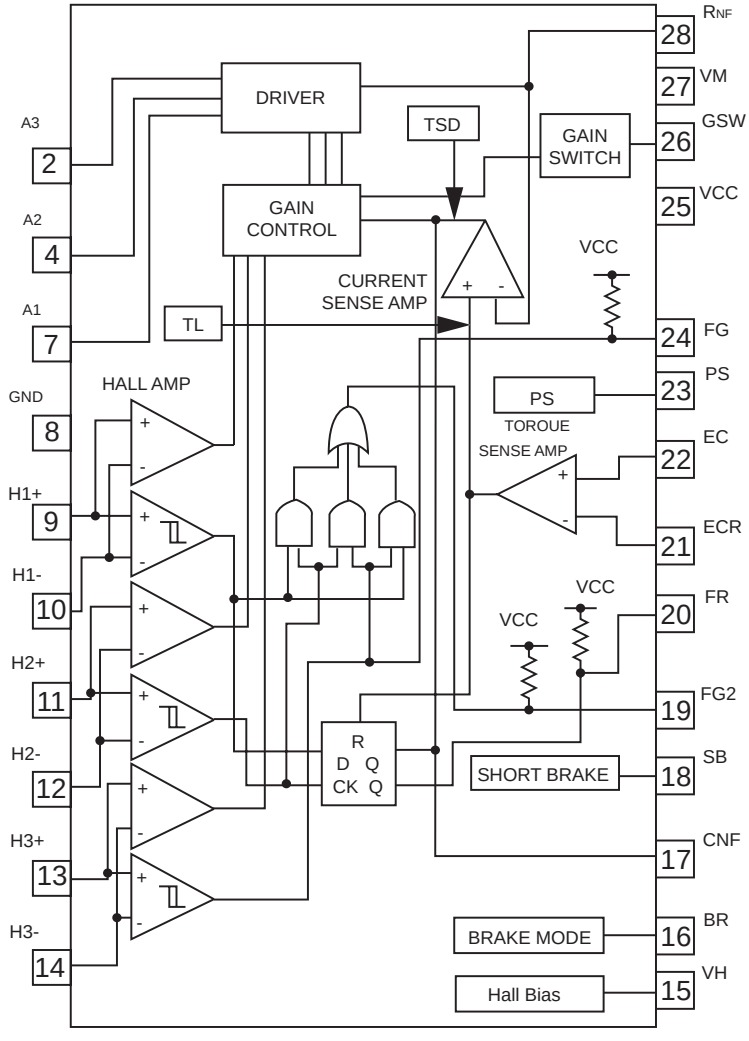
Pin No.	Symbol	I/O	Description
33	GND3	-	Connect to GND
34	RFDIFO	-	Non connect
35	RFOUT	-	Connect to TP103
36	VCC3	-	Power supply terminal 3.3V
37	RFC	O	Filter for RF delay correction AMP.
38	DCRF	O	All addition amplifier capacitor terminal
39	OFTR	O	OFTR output terminal
40	BDO	O	BDO output terminal
41	RFENV	O	RF envelope output terminal
42	BOTTOM	O	Bottom envelope detection filter terminal
43	PEAK	O	Peak envelope detection filter terminal
44	AGCG	O	AGC amplifier gain control terminal
45	AGCO	O	AGC amplifier level control terminal
46	TESTSG	I	TEST signal input terminal
47	RFINP	I	RF signal positive input terminal
48	RFINN	I	RF signal negative input terminal
49	VIN5	I	Internal four-partition (CD) RF input 1
50	VIN6	I	Internal four-partition (CD) RF input 2
51	VIN7	-	Internal four-partition (CD) RF input 3
52	VIN8	-	Internal four-partition (CD) RF input 4
53	VIN9	I	External two-partition (DVD) RF input 2
54	VIN10	I	External two-partition (DVD) RF input 1
55	VCC1	-	Power supply terminal 5V
56	VREF1	O	VREF1 voltage output terminal
57	VIN1	I	Internal four-partition (DVD) RF input 1
58	VIN2	I	Internal four-partition (DVD) RF input 2
59	VIN3	I	Internal four-partition (DVD) RF input 3
60	VIN4	I	Internal four-partition (DVD) RF input 4
61	GND1	-	Connect to GND
62	VIN11	I	3 beam sub input terminal 2 (CD)
63	VIN12	I	3 beam sub input terminal 1 (CD)
64	HDTYPE	O	HD Type selection

4.9 BA6664FM-X (IC251) : Motor driver

- Pin layout



- Block diagram

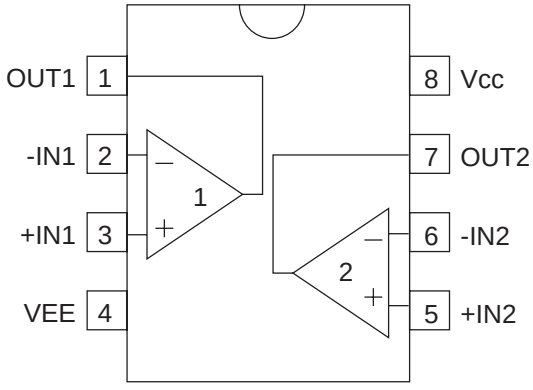


• Pin function

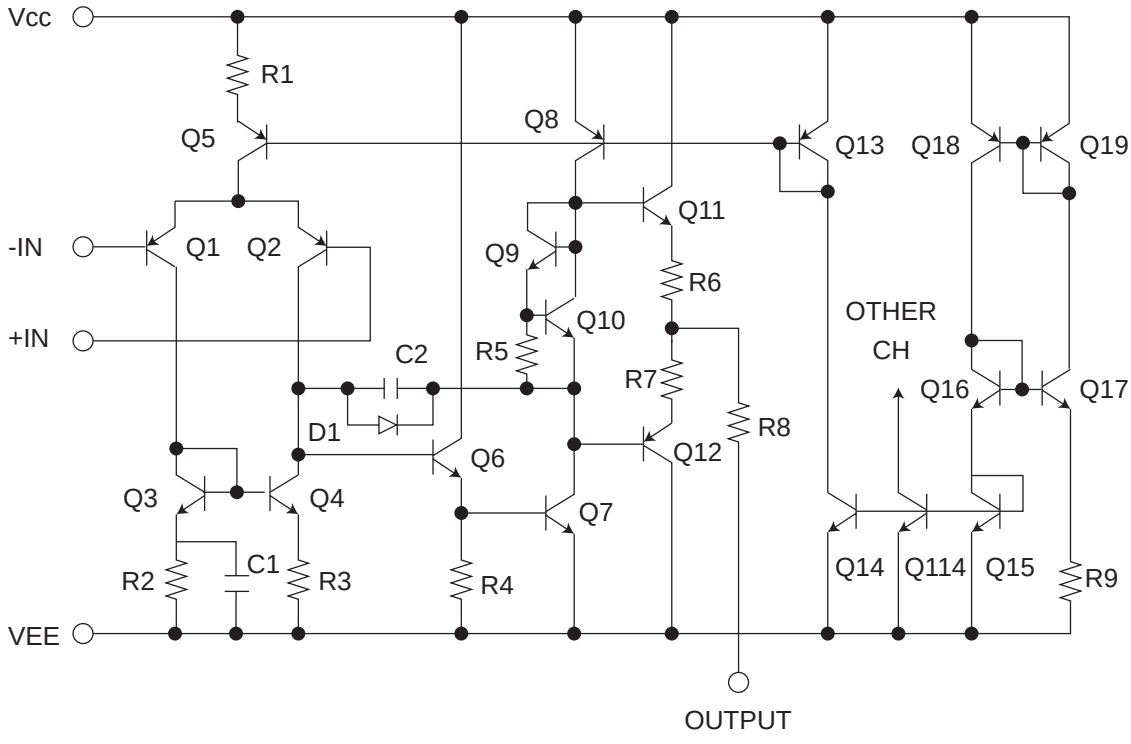
Pin No.	Symbol	I/O	Description
1	NC	-	Non connect
2	A3	O	Output 3 for spindle motor
3	NC	-	Non connect
4	A2	O	Output 2 for spindle motor
5	NC	-	Non connect
6	NC	-	Non connect
7	A1	O	Output 1 for spindle motor
8	GND	-	Connect to ground
9	H1+	I	Positive input for hall input AMP 1
10	H1-	I	Negative input for hall input AMP 1
11	H2+	I	Positive input for hall input AMP 2
12	H2-	I	Negative input for hall input AMP 2
13	H3+	I	Positive input for hall input AMP 3
14	H3-	I	Negative input for hall input AMP 3
15	VH	I	Hall bias terminal
16	BR	-	Non connect
17	CNF	-	Capacitor connection pin for phase compensation
18	SB	I	Short brake terminal
19	FG2	-	Non connect
20	FR	-	Non connect
21	ECR	I	Torque control standard voltage input terminal
22	EC	I	Torque control voltage input terminal
23	PS	O	Start/stop switch (power save terminal)
24	FG	O	FG signal output terminal
25	VCC	-	Power supply for signal division
26	GSW	O	Gain switch
27	VM	-	Power supply for driver division
28	RNF	O	Resistance connection pin for output current sense
29		-	Connect to ground
30		-	Connect to ground

4.10 BA15218F-XE (IC251/IC540/IC544/IC546/IC548/IC557/IC560/IC562/IC564/IC566/IC711/IC712) : Dual operational amplifier

- Pin layout

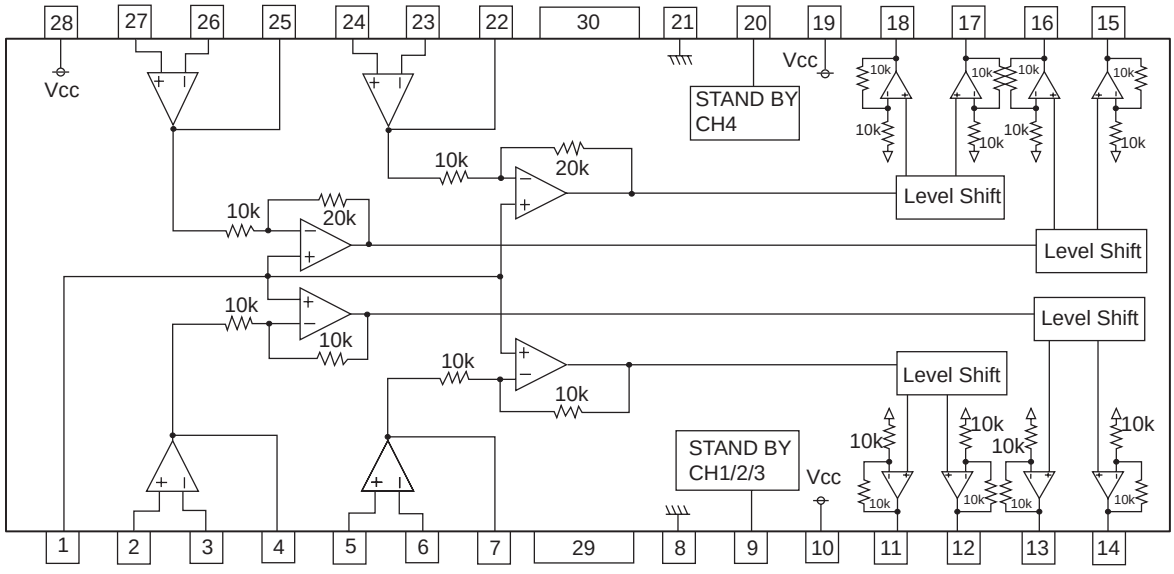


- Block diagram



4.11 BA5983FM-X (IC201) : 4-channel driver

- Block diagram



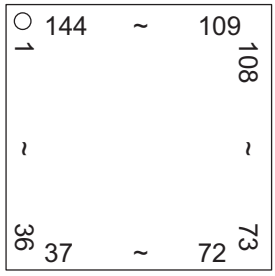
- Pin function

Pin No.	Symbol	I/O	Description
1	BIAS IN	I	Input for Bias-amplifier
2	OPIN1(+)	I	Non inverting input for CH1 OP-AMP
3	OPIN1(-)	I	Inverting input for CH1 OP-AMP
4	OPOUT1	O	Output for CH1 OP-AMP
5	OPIN2(+)	I	Non inverting input for CH2 OP-AMP
6	OPIN2(-)	I	Inverting input for CH2 OP-AMP
7	OPOUT2	O	Output for CH2 OP-AMP
8	GND	-	Substrate ground
9	STBY1	I	Input for CH1/2/3 stand by control
10	PowVcc1	-	Vcc for CH1/2 power block
11	VO2(-)	O	Inverted output of CH2
12	VO2(+)	O	Non inverted output of CH2
13	VO1(-)	O	Inverted output of CH1
14	VO1(+)	O	Non inverted output of CH1
15	VO4(+)	O	Non inverted output of CH4

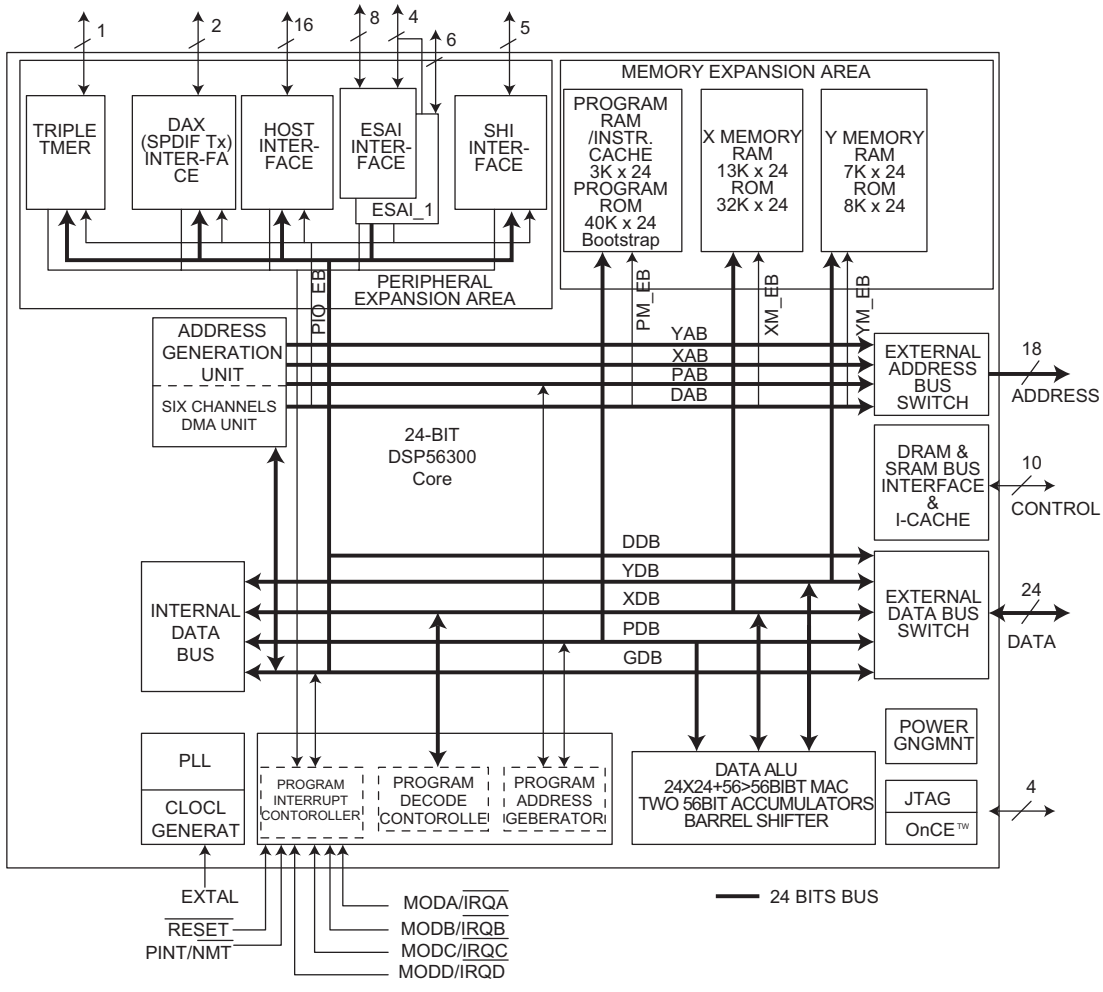
Pin No.	Symbol	I/O	Description
16	VO4(-)	O	Inverted output of CH4
17	VO3(+)	O	Non inverted output of CH3
18	VO3(-)	O	Inverted output of CH3
19	PowVcc2	-	Vcc for CH3/4 power block
20	STBY2	I	Input for Ch4 stand by control
21	GND	-	Substrate ground
22	OPOUT3	O	Output for CH3 OP-AMP
23	OPIN3(-)	I	Inverting input for CH3 OP-AMP
24	OPIN3(+)	I	Non inverting input for CH3 OP-AMP
25	OPOUT4	O	Output for CH4 OP-AMP
26	OPIN4(-)	I	Inverting input for CH4 OP-AMP
27	OPIN4(+)	I	Non inverting input for CH4 OP-AMP
28	PreVcc	-	Vcc for pre block
29		-	Connect to ground
30		-	Connect to ground

4.12 DSPC56367PV150 (IC521) : DSP

- Pin layout



- Block diagram



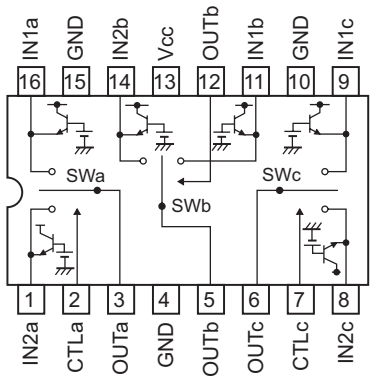
• Pin function

Pin No	Symbol	I/O	Function
1	SCK/SCL	I/O	SPI serial clock / I2C serial clock
2	$\overline{SS}$/HA2	I	SPI slave select / I2C slave address 2
3	$\overline{HREQ}$	I/O	Host request
4	SDO0/SDO0_1	O	Serial data output 0
5	SDO1/SDO1_1	O	Serial data output 1
6	SDO2/SDI3/SDO2_1/SDI3_1	O	Serial data output 2 / Serial data input 3
7	SDO3/SDI2/SDO3_1/SDI2_1	O	Serial data output 3 / Serial data input 2
8	VCCS	-	SHI,ESAI,ESAI_1,DAX and Timer power
9	GNDS	-	SHI,ESAI,ESAI_1,DAX and Timer ground
10	SDO4/SDI1	O	Serial data output 4 / Serial data input 1
11	SDO5/SDI0	O	Serial data output 5 / Serial data input 0
12	FST	I/O	Frame sync for transmitter
13	FSR	I/O	Frame sync for receiver
14	SCKT	I/O	Transmitter serial clock
15	SCKR	I/O	Receiver serial clock
16	HCKT	I/O	High frequency clock for transmitter
17	HCKR	I/O	High frequency clock for receiver
18	VCCQL	-	Quite core (Low) power
19	GNDQ	-	Quite ground
20	VCCQH	-	Quite external (High) power
21	HDS/HWR	I	Host data strobe / Host write data
22	HRW/HRD	I	Host read write / Host read data
23	HACK/HRRQ	I	Host acknowledge / Receive host request
24	HOREQ/HTRQ	O	Host request / Transmit host request
25	VCCS	-	SHI,ESAI,ESAI_1,DAX and Timer power
26	GNDS	-	SHI,ESAI,ESAI_1,DAX and Timer ground
27	ADO	O	Digital audio data output
28	ACI	I	Audio clock input
29	TIO0	I/O	Timer 0 schmitt-trigger input/output
30	HCS/HA10	I	Host chip select / Host address 10
31	HA9/HA2	I	Host address 9 / Host address input 2
32	HA8/HA1	I	Host address 8 / Host address input 1
33	HAS/HA0	I	Host address strobe / Host address input 0
34~37	HAD7~HAD4	I/O	Host address/Data
38	VCCH	-	Host power
39	GNDH	-	Host ground
40~43	HAD3~HAD0	I/O	Host address/Data
44	$\overline{RESET}$	I	Reset
45	VCCP	-	PLL power
46	PCAP	I	PLL capacitor
47	GNDP	-	PLL ground
48	SDO5_1/SDI0_1	I/O	Serial data output 5_1 / Serial data input 0_1
49	VCCQH	-	Quite external (High) power
50	FST_1	I/O	Frame sync for transmitter
51	AA2	O	Address attribute or Row address strobe
52	$\overline{CAS}$	O	Column address strobe
53	SCKT_1	I/O	Transmitter serial clock_1
54	GNDQ	-	Quite ground
55	EXTAL	I	External clock input
56	VCCQL	-	Quite core (Low) power
57	VCCC	-	Bus control power
58	GNDC	-	Bus control ground

Pin No	Symbol	I/O	Function
59	FSR_1	I/O	Frame sync for receiver
60	SCKR_1	I/O	Receiver serial clock_1
61	PINIT/NMI	I	PLL initial / Nonmaskable interrupt
62	$\overline{TA}$	I	Transfer acknowledge
63	$\overline{BR}$	O	Bus request
64	$\overline{BB}$	I/O	Bus busy
65	VCCC	-	Bus control power
66	GNDC	-	Bus control ground
67	$\overline{WR}$	O	Write enable
68	$\overline{RD}$	O	Read enable
69,70	AA1,AA0	O	Address attribute or row address strobe
71	$\overline{BG}$	I	Bus grant
72,73	A0,A1	O	Data bus
74	VCCA	-	Address bus power
75	GNDA	-	Address bus ground
76~79	A2~A5	O	Data bus
80	VCCA	-	Address bus power
81	GNDA	-	Address bus ground
82~85	A6~A9	O	Data bus
86	VCCA	-	Address bus power
87	GNDA	-	Address bus ground
88,89	A10,A11	O	Data bus
90	GNDQ	-	Quite ground
91	VCCQL	-	Quite core (Low) power
92~94	A12~A14	O	Data bus
95	VCCQH	-	Quite core (High) power
96	GNDA	-	Address bus ground
97~99	A15~A17	O	Data bus
100~102	D0~D2	I/O	Data bus
103	VCCD	-	Data bus power
104	GNDD	-	Data bus ground
105~110	D3,D8	I/O	Data bus
111	VCCD	-	Data bus power
112	GNDD	-	Data bus ground
113~118	D9~D14	I/O	Data bus
119	VCCD	-	Data bus power
120	GNDD	-	Data bus ground
121~125	D15~D19	I/O	Data bus
126	VCCQL	-	Quite core (Low) power
127	GNDQL	-	Quite core (Low) ground
128	D20	I/O	Data bus
129	VCCD	-	Data bus power
130	GNDD	-	Data bus ground
131~133	D21~D23	I/O	Data bus
134	MODD/$\overline{IRQD}$	I	Mode select D / External interrupt request D
135	MODC/$\overline{IRQC}$	I	Mode select C / External interrupt request C
136	MODB/$\overline{IRQB}$	I	Mode select B / External interrupt request B
137	MODA/IRQA	I	Mode select A / External interrupt request A
138	SDO4_1/SDI1_1	I/O	Serial data output 4_1 / Serial data input 1_1
139~142	TDO,TDI,TCK,TMS	O/I	Test data output,Test data input,Test clock,Test mode select
143	MOSI/HA0	I/O	SPI master-out-sleve-in / I2C slave address 0
144	MISO/SDA	I/O	SPI master-in-slave-out / I2C data and acknowkedge

4.13 BA7603F-X (IC211/IC221) : Video signal switcher

- Pin layout & Block diagram

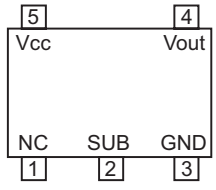


CTL	OUTPUT
H	IN2
L	IN1

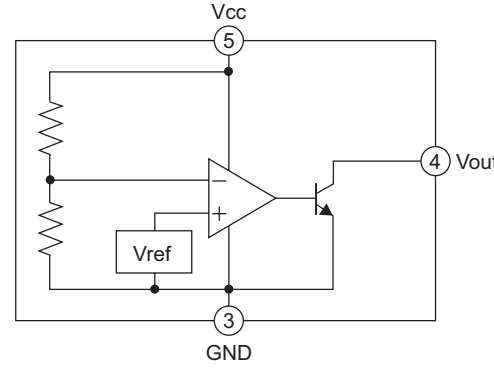
SWa,SWb,SWc: Clamp inputs

4.14 BD4740G-W (IC272) : Reset

- Pin layout

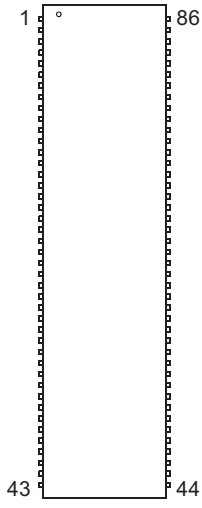


- Block diagram

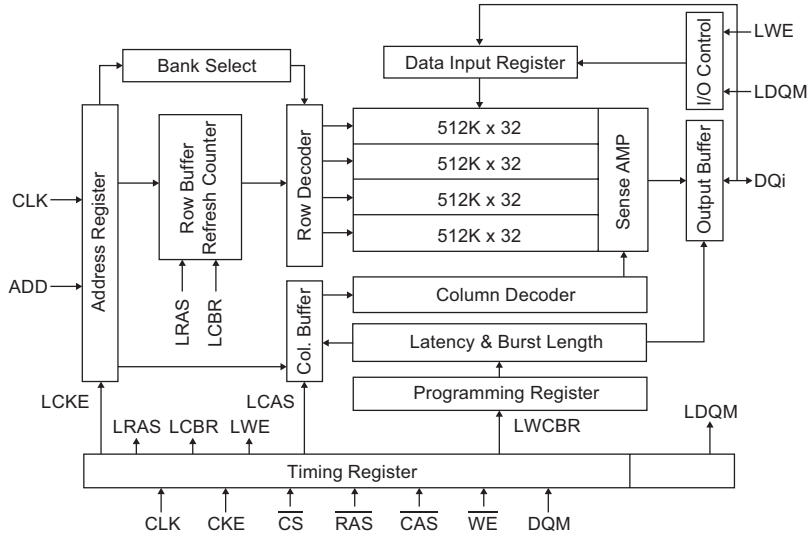


4.15 K4S643232E-TC60 (IC505) : 512K x 32 bit x 4 banks synchronous DRAM

- Pin layout



- Block diagram



• Pin function

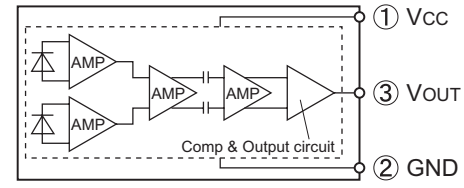
Pin No.	Symbol	Function
1	VDD	Power for the input buffers and core logic.
2	DQ0	Data input/output are multiplexed on the same pin.
3	VDDQ	Isolated power supply for the output buffers to provide improved noise immunity.
4,5	DQ1,DQ2	Data inputs/outputs are multiplexed on the same pins.
6	VSSQ	Isolated ground for the output buffers to provide improved noise immunity.
7,8	DQ3,DQ4	Data inputs/outputs are multiplexed on the same pins.
9	VDDQ	Isolated power supply for the output buffers to provide improved noise immunity.
10,11	DQ5,DQ6	Data inputs/outputs are multiplexed on the same pins.
12	VSSQ	Isolated ground for the output buffers to provide improved noise immunity.
13	DQ7	Data input/output are multiplexed on the same pin.
14	N.C	This pin is recommended to be left no connection on the device.
15	VDD	Power for the input buffers and core logic.
16	DQM0	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
17	$\overline{WE}$	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
18	$\overline{CAS}$	Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access.
19	$\overline{RAS}$	Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
20	$\overline{CS}$	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
21	N.C	This pin is recommended to be left no connection on the device.
22,23	BA0,BA1	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
24,25~27	A10,A0 - A2	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, Column address : CA0 ~ CA7
28	DQM2	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
29	VDD	Power for the input buffers and core logic.
30	N.C	This pin is recommended to be left no connection on the device.
31	DQ16	Data input/output are multiplexed on the same pin.
32	VSSQ	Isolated ground for the output buffers to provide improved noise immunity.
33,34	DQ17,DQ18	Data inputs/outputs are multiplexed on the same pins.
35	VDDQ	Isolated power supply for the output buffers to provide improved noise immunity.
36,37	DQ19,DQ20	Data inputs/outputs are multiplexed on the same pins.
38	VSSQ	Isolated ground for the output buffers to provide improved noise immunity.
39,40	DQ21,DQ22	Data inputs/outputs are multiplexed on the same pins.
41	VDDQ	Isolated power supply for the output buffers to provide improved noise immunity.
42	DQ23	Data input/output are multiplexed on the same pin.
43	VDD	Power for the input buffers and core logic.
44	VSS	Ground for the input buffers and core logic.
45	DQ24	Data input/output are multiplexed on the same pin.
46	VSSQ	Isolated ground for the output buffers to provide improved noise immunity.
47,48	DQ25,DQ26	Data inputs/outputs are multiplexed on the same pins.
49	VDDQ	Isolated power supply for the output buffers to provide improved noise immunity.
50,51	DQ27,DQ28	Data inputs/outputs are multiplexed on the same pins.
52	VSSQ	Isolated ground for the output buffers to provide improved noise immunity.

Pin No.	Symbol	Function
53,54	DQ29,DQ30	Data inputs/outputs are multiplexed on the same pins.
55	VDDQ	Isolated power supply for the output buffers to provide improved noise immunity.
56	DQ31	Data input/output are multiplexed on the same pin.
57	N.C	This pin is recommended to be left no connection on the device.
58	VSS	Ground for the input buffers and core logic.
59	DQM3	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
60~66	A3 - A9	Row/column addresses are multiplexed on the same pins. Row address : RA0 - RA10, Column address : CA0 - CA7
67	CKE	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down mode.
68	CLK	Active on the positive going edge to sample all inputs.
69,70	N.C	This pin is recommended to be left no connection on the device.
71	DQM1	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
72	VSS	Ground for the input buffers and core logic.
73	N.C	This pin is recommended to be left no connection on the device.
74	DQ8	Data input/output are multiplexed on the same pin.
75	VDDQ	Isolated power supply for the output buffers to provide improved noise immunity.
76,77	DQ9,DQ10	Data inputs/outputs are multiplexed on the same pins.
78	VSSQ	Isolated ground for the output buffers to provide improved noise immunity.
79,80	DQ11,DQ12	Data inputs/outputs are multiplexed on the same pins.
81	VDDQ	Isolated power supply for the output buffers to provide improved noise immunity.
82,83	DQ13,DQ14	Data inputs/outputs are multiplexed on the same pins.
84	VSSQ	Isolated ground for the output buffers to provide improved noise immunity.
85	DQ15	Data input/output are multiplexed on the same pin.
86	VSS	Ground for the input buffers and core logic.

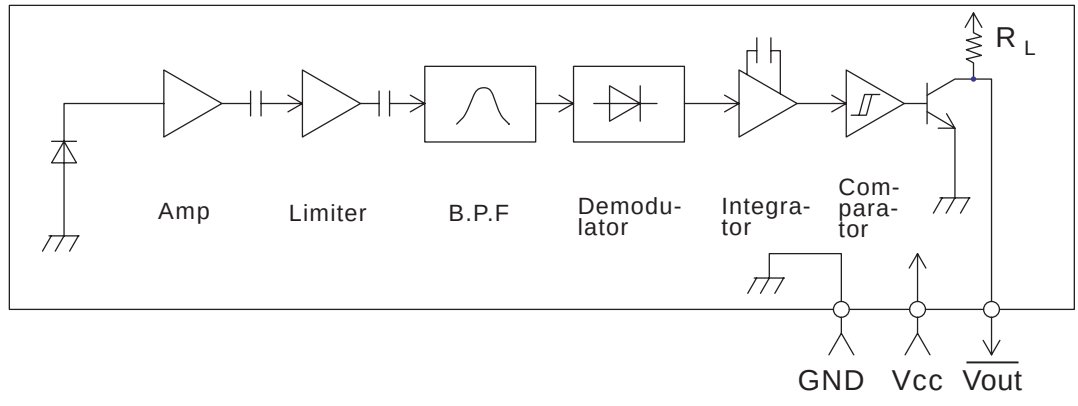
4.16 GP1FA351RZ (J5521) : Fiber optic receiver

- Pin layout

- Block diagram

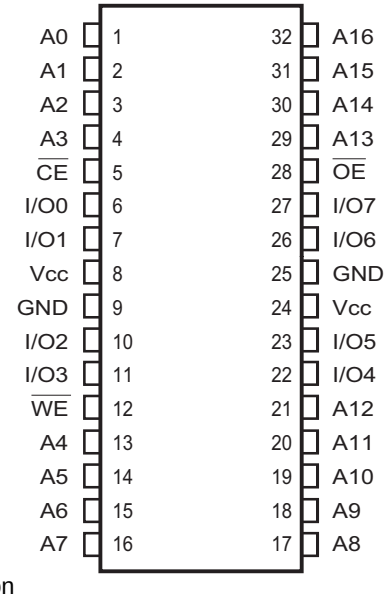


4.17 GP1UM271XK (IC402) : IR detecting unit for remote control

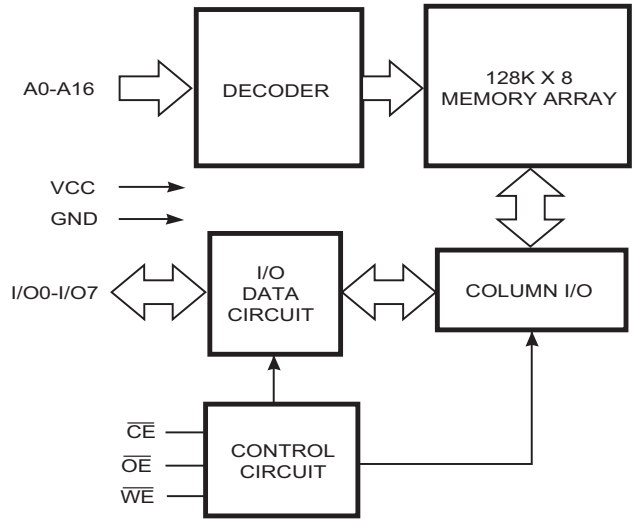


4.18 IS63LV102410K-X (IC525/IC526/IC527) : SRAM

- Pin layout



- Block diagram



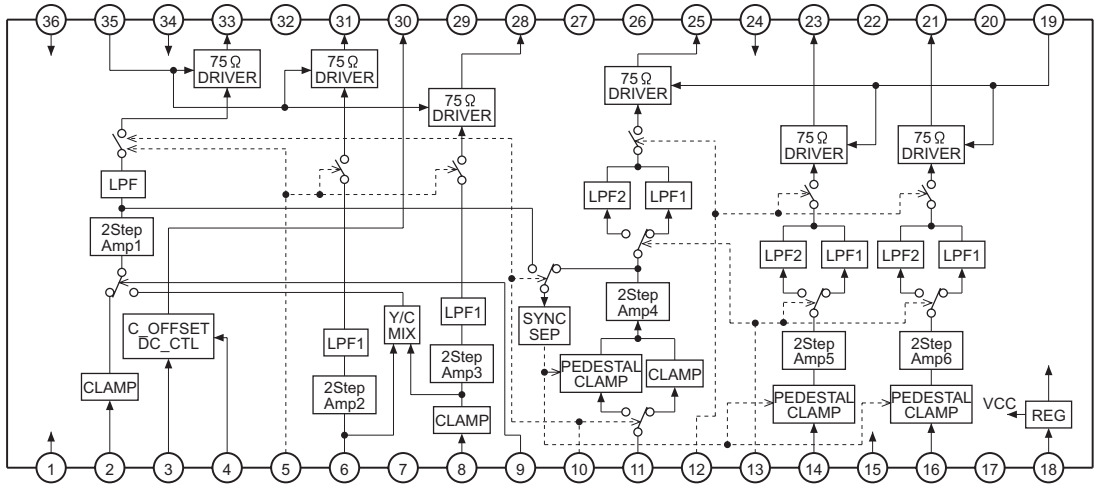
- Pin function

Pin No.	Symbol	I/O	Function
1-4	A0-A3	I	Address inputs
5	$\overline{CE}$	I	Chip enable input
6,7	I/O0,I/O1	I/O	Bidirectional ports
8	Vcc	-	Power
9	GND	-	Ground
10,11	I/O2,I/O3	I/O	Bidirectional ports
12	$\overline{WE}$	I	Write enable input

Pin No.	Symbol	I/O	Function
13-21	A4-A12	I	Address inputs
22,23	I/O4,I/O5	I/O	Bidirectional ports
24	Vcc	-	Power
25	GND	-	Ground
26,27	I/O6,I/O7	I/O	Bidirectional ports
28	$\overline{OE}$	I	Output enable input
29-32	A13-A16	I	Address inputs

4.19 LA73054-X (IC231) : Video driver

- Pin layout & Block diagram

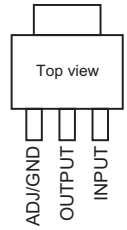


- Pin function

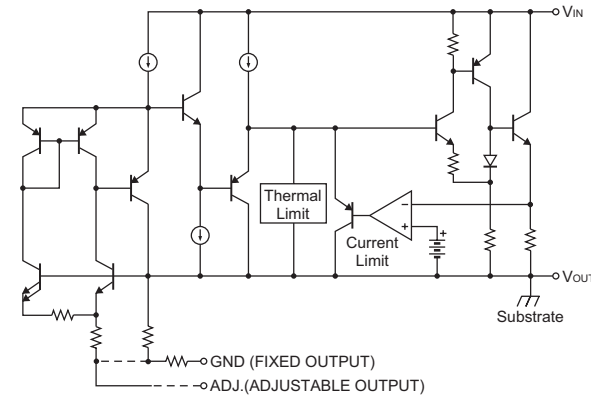
Pin No.	Symbol	I/O	Function
1	VCC1	-	VCC except for 75ohm driver
2	COMPOSITE.IN	I	Input composite
3	SQUEEZE.SW	I	Selecting squeeze mode
4	LETTER-BOX.SW	I	Selecting letter-box mode
5	MUTE-SW-1	I	Composite/S signal mute selection
6	C-IN	I	Input Chroma signal
7	GND11	-	Composite/S GND except for 75ohm driver
8	Y-IN-1	I	Input Y signal
9	YC-MIX.SW	I	Selecting of doing Y/C-MIX or not
10	SIGNAL-IN.SW	I	Selection of a kind of signal
11	Y-IN-2	I	Input component Y or baseband signal
12	MUTE-SW-2	I	Component signal mute selection
13	LPF.SW	I	Selection of a kind of component LPF
14	CB.IN	I	Input component or baseband signal
15	AMP.SW-2	I	Selecting amplifier gain for component signal
16	CR.IN	I	Input component or baseband signal
17	GND12	-	Component GND except for 75ohm driver
18	REG	O	Capacitor terminal for regulator
19	DRIVE.SW-2	I	2drive/1drive select for component signal
20	GND26	-	CR-GND for 75ohm driver
21	CR.OUT	O	75ohm driver output of pin16 input
22	GND25	-	CB-OUT for 75ohm driver
23	CB.OUT	O	75ohm driver output of pin14 input
24	VCC22	-	Component Vcc for 75ohm driver
25	Y-OUT-2	O	75ohm driver output of pin11 input
26	GND24	-	Component Y out for 75ohm driver
27	GND23	-	Y out for 75ohm driver
28	Y-OUT-1	O	75ohm driver output of pin8 input
29	GND22	-	Chroma out for 75ohm driver
30	C-DC.OUT	O	DC voltage output for S1,S2
31	C-OUT	O	75ohm driver output of pin6 input
32	GND21	-	Composite out for 75ohm driver
33	COMPOSITE-OUT	O	75ohm driver output of pin2 input
34	VCC21	-	Composite/S Vcc for 75ohm driver
35	DRIVE.SW-1	I	2drive/1drive select for composite/S signal
36	AMP.SW-1	I	Selecting amplifier gain for composite/S signal

4.20 LM1117MP1.8-X (IC511) : Regulator

- Pin layout

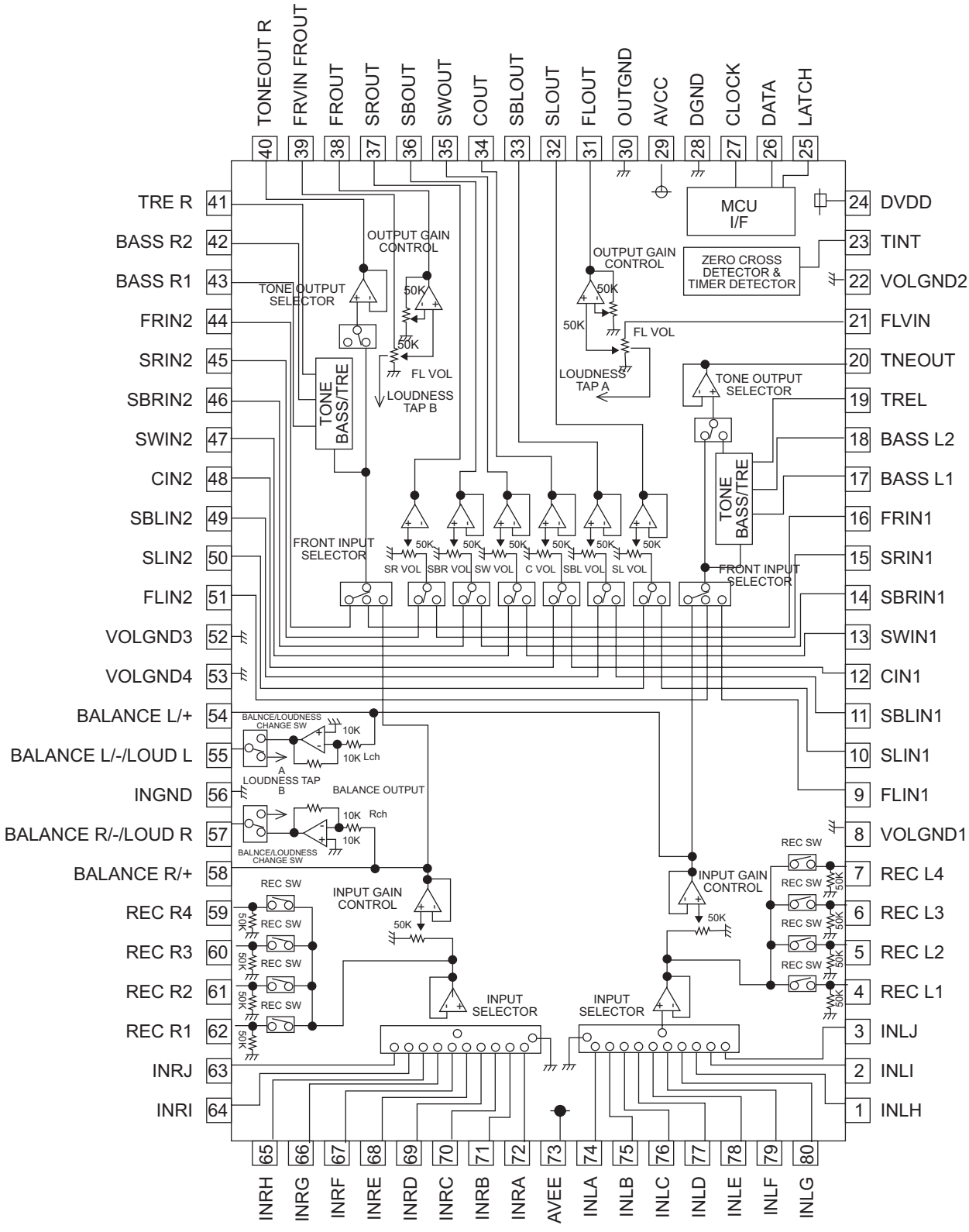


- Block diagram



4.21 M61516FP (IC551) : Sound controller

- Pin layout & Block diagram

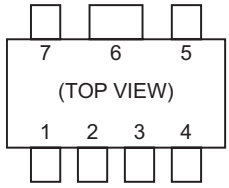


• Pin function

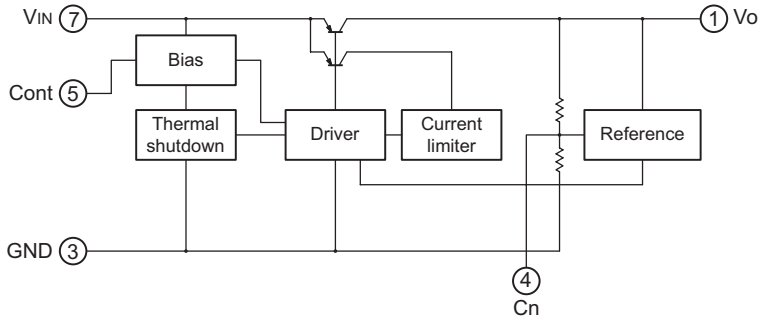
Pin No.	Symbol	Function
1~3	INLH,INLI,INLJ	Lch input
4~7	REC L1,REC L2,REC L3,REC L4	REC output
8	VOLGND1	Analog GND for vol.
9~12	FLIN1,SLIN1,SBLIN1,CIN1	FLch,SLch,SBLch,Cch input
13~16	SWIN1,SBRIN1,SRIN1,FRIN1	SWch,SBRch,SRch,FRch input
17,18	BASS L1,BASS L2	Tone path frequency characteristic setup
19	TRE L	Treble frequency characteristic setup
20	TONEOUT L	Tone output
21	FLVIN	FL vol. input
22	VOLGND2	Analog GND for vol.
23	TIM1	Timer setup
24	DVDD	Internal logic circuit Power supply terminal
25,26,27	LATCH,DATA,CLOCK	Latch,Data,Clock input for serial data transmission
28	DGND	Internal logic circuit GND terminal
29	AVCC	Internal analog cicuit power supply terminal (+)
30	OUTGND	analog GND
31~34	FLOUT,SLOUT,SBLOUT,COUT	FLch,SLch,SBLch,Cch output
35~38	SWOUT,SBROUT,SROUT,FROUT	SWch,SBRch,SRch,FRch output
39	FRVIN	FR vol.input
40	TONEOUT R	Tone output
41	TRE R	Treble frequency characteristic setup
42,43	BASS R1,BASS R2	Tone path frequency characteristic setup
44~47	FRIN2,SRIN2,SBRIN2,SWIN2	FRch,SRch,SBRch,SWch input
48~51	CIN2,SBLIN2,SLIN2,FLIN2	Cch,SBLch,SLch,FLch input
52,53	VOLGND3,VOLGND4	Analog GND for vol.
54	BALANCE L/+	Lch balance output for ADC
55	BALANCE L/- LOUD L	Lch loudness frequency setup
56	INGND	Analog GND
57	BALANCE R/+	Rch balance output for ADC
58	BALANCE R/- LOUD R	Rch loudness frequency setup
59~62	REC R1,REC R2,REC R3,REC R4	REC input
63~66	INRJ,INRI,INRH,INRG	Rch input
67~70	INRF,INRE,INRD,INRC	Rch input
71,72	INRB,INRA	Rch input
73	AVEE	Internal analog circuit power supply terminal (-)
74~77	INLA,INLB,INLC,INLD	Lch input
78~80	INLE,INLF,INLG	Lch input

4.22 MM1561KF-X (IC593) : Regulator

• Pin layout



• Block diagram

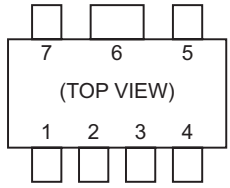


• Pin function

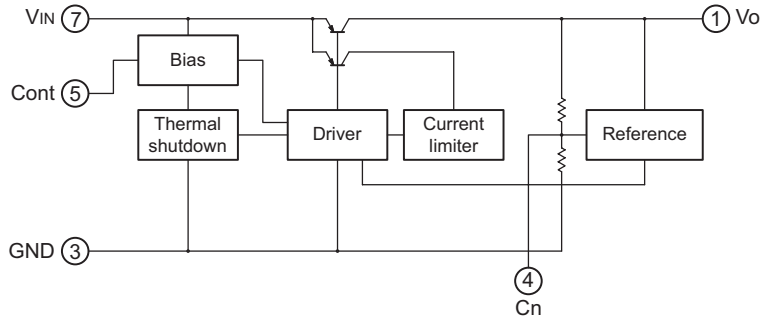
Pin No.	Symbol	Function
1	Vo	Output pin
2	NC	Not connect
3	GND	Ground
4	Cn	Noise decrease pin
5	CONT	Control pin CONT: H → Output: ON; CONT: L → Output: OFF
6	Sub	Substrate pin, The 6pin must be connected to GND.
7	VIN	Input pin

4.23 MM1563DF-X (IC592) : Regulator

- Pin layout



- Block diagram

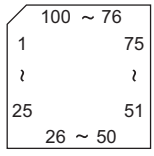


- Pin function

Pin No.	Symbol	Function
1	Vo	Output pin
2	NC	Not connect
3	GND	Ground
4	Cn	Noise decrease pin
5	CONT	Control pin CONT: H → Output: ON; CONT: L → Output: OFF
6	Sub	Substrate pin, The 6pin must be connected to GND.
7	VIN	Input pin

4.24 MN101C49GKR (IC271) : System micom

• Pin layout



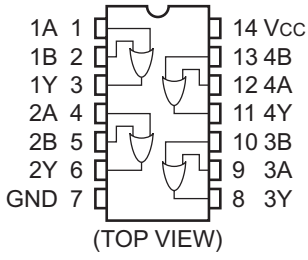
• Pin function

Pin No.	Symbol	I/O	Function
1	VREF-	-	Connect to ground
2	NTSEL(RGB--SEL)	I	NTSC/PAL discrimination (RGB/YC switching discrimination) signal
3	VCR-S/C	I	VCR S/Composite detection signal
4	DBS-S/C	I	DBS S/Composite detection signal
5	TH-DET	I	Heat sink temp. detection
6	SAFETY1	I	Short detection signal
7	VERSION	I	Version select switch signal
8	KEY-IN1	I	Key input1 (AD)
9	KEY-IN2	I	Key input2 (AD)
10	VREF+	-	Reference power supply
11	VDD	-	Power supply
12	OSC2	O	Oscillator output (8MHz)
13	OSC1	I	Oscillator input (8MHz)
14	GND	-	Ground
15,16	NC	-	Not used
17	GND	-	Ground
18	DI-DO	O	Panel serial communication data output
19	NC	-	Not used
20	DI-CK	O	Panel serial communication clock output
21	S2UDT/TX (DATA OUT)	O	Serial communication data output for PANTERA
22	S2UDT/RX (DATA IN)	I	Serial communication data input for PANTERA
23	SCLK/CLK	I	Serial communication clock for PANTERA
24	INTP	O	Transmit request for PANTERA communication
25	CPU-RESET	O	Reset signal for PANTERA
26	CS	I	Receive request for PANTERA communication (Interruption)
27	REMOCON	I	Remote control signal input (interruption)
28	PROTECT	I	Speaker protect detection
29	RDS ST	I	RDS communication strobe (Interruption)
30	NC	-	Not used
31	GND	-	Ground
32	VDD2/FLASH-VDD	-	VDD for Flash write
33	RESET-IN/RST	I	System control micom reset input
34	DSP-RST	O	DSP micom reset signal output
35	DSP-RDY	O	DSP micom ready signal
36	AVC-OUT	O	AV compulink signal output
37	AVC-IN	I	AV compulink signal input
38~40	NC	-	Not used
41	VPP/FLASH-VSS	-	VPP for Flash write
42	DSP-COM	O	DSP serial communication data output
43	DSP-STAT	I	DSP serial communication data input
44	DSP-CLK	O	DSP serial communication clock
45	VOL-DATA	O	VOLUME serial communication data output
46	VOL-LATCH	O	VOLUME serial communication strobe
47	VOL-CLK	O	VOLUME serial communication clock

Pin No.	Symbol	I/O	Function
48	NC	-	Not used
49	INT/PROG	O	Video driver filter select
50	RELAT-CTL	O	Speaker control
51	BASS	O	Bass boost control
52,53	NC	-	Not used
54	VIDEO-MUTE1	O	Video driver mute1 control
55	VIDEO-MUTE2	O	Video driver mute2 control
56	VIDEO-YCMIX	O	Video driver YCMIX control
57	VIDEO-RGB	O	Video driver RGB control
58	NC	-	Not used
59	INH	I	AC cut of detection
60	NC	-	Not used
61	HP	I	Headphone input detection
62	S-PON	O	System power supply control
63	AMP-PON	O	Power amp. power supply control
64	DVD-PON	O	DVD power supply control
65	TU-PON	O	TUNER power supply control
66	-	-	Not used
67	RDS-DATA	O	RDS communication data
68	RDS-CLK	O	RDS communication clock
69	NC	-	Not use
70	TU-DI	I	TUNER serial communication data input
71	NC	-	Not use
72	TU-DO	O	TUNER serial communication data output
73	TU-CLK	O	TUNER serial communication clock
74	TU-CE	O	TUNER serial communication CE
75	AM-BEAT	O	AM beat cut switching
76	S-MUTE	O	System mute
77,78	VS1,VS3	O	E version SLOW switch control
79	FAN-ON/OFF	O	Fan ON/OFF control
80	FAN-CTL	O	Fan speed control
81	STBY-LED	O	STANDBY LED control
82	DISC-SET	O	Read start signal output for Frontend
83	DISC-STOP	I	Receive eject permission signal from Frontend
84	SAFETY2	I	Short detection2
85,86	NC	-	Not used
87	VIDEO-SW1	O	Video select output1
88	VIDEO-SW2	O	Video select output2
89	VIDEO-SW3	O	Video select output3
90	BLANK-CTL	O	E version BLANKING select
91	DI-RST	O	Panel micom reset output
92	DI-CS	O	Panel micom serial communication chip select
93	NC	-	Not used
94	TOPEN	O	Mechanism open output
95	DAVSS	-	Ground
96	TCLOSE	O	Mechanism close output
97	LMMUTE	O	Loader mute output
98	SWOPEN	I	Mechanism switch open detection
99	SWUPDN	I	Mechanism switch close detection
100	DAVDD	-	Power supply

4.25 74LCX32MTC-X (IC522) : Quad 2 input OR gate

• Pin layout & Block diagram



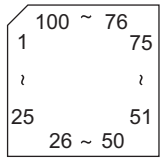
(TOP VIEW)

• Truth table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

4.26 MN101C35DKW (IC401) : FL driver microcomputer

• Pin layout

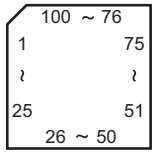


• Pin function

Pin No.	Symbol	I/O	Function
1	NC	-	Not connect
2	DATAIN	I	FL driver communication data input
3	CLOCK	I	FL driver communication clock input
4	NC	-	Not connect
5	INITIAL	I	FL driver communication CS(INITIAL)
6,7	NC	-	Not connect
8	B5V	-	VDD(B5V)
9	OSC2	O	8MHz main clock output
10	OSC1	I	8MHz main clock input
11,12	GND	-	Ground
13	NC	-	Not connect
14~23	GND	-	Ground
24	VREF+	-	Reference voltage
25	NC	-	Not connect
26	RESET	I	FL reset input
27	PROG_LED	O	PROGRAM LED switching signal
28	NC	O	Not connect
29	ILUMI_LED	O	Illumi LED switching signal
30~32	NC	-	Not connect
33~38	GND	-	Ground
39	PROG_DM	O	Program LED dimmer select
40	ILUMI_DIM	O	Illumi LED dimmer select
41~46	NC	-	Not connect
47	G1	O	Grid signal outputs
48~59	G2~G13	O	Grid signal outputs
60	G14	O	Grid signal outputs
61~64	NC	-	Not connect
65~99	S1~S35	O	Segment signal outputs
100	-VPP	-	VPP

4.27 MN102L62GLF3 (IC401) : Unit CPU

- Pin layout



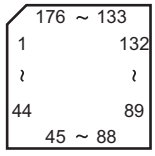
- Pin function

Pin No.	Symbol	I/O	Function
1	WAIT	I	Micro computer wait signal input
2	RE	O	Read enable
3	/SPMUTE	O	Spindle muting output to IC251
4	WEN	O	Write enable
5	/LMMUTE	-	Not connect
6	CS1	O	Chip select for ODC
7	CS2	-	Chip select for ZIVA (Not connect.)
8	HDTYPE	O	HD TYPE selection
9	/DRVMUTE	O	Driver mute
10	SBRK	O	SP motor brake control
11	LSIRST	O	LSI reset
12	WOR0	O	Bus selection input
13-16	A0-A3	O	Address bus (0-3) for CPU
17	VDD	-	Power supply
18	SYSCLK	-	System clock signal output (Not connect.)
19	VSS	-	Ground
20	XI	-	Not use (Connect to VSS)
21	XO	-	Not connect
22	VDD	-	Power supply
23	OSCI	I	Clock signal input (13.5MHz)
24	OSCO	O	Clock signal output (13.5MHz) (Not connect.)
25	MODE	I	CPU mode selection input
26-33	A4-A11	O	Address bus (4-11) for CPU
34	VDD	-	Power supply
35-40	A12-A17	O	Address bus (12-17) for CPU
41	A18	-	Address bus 18 for CPU (Not connect.)
42	A19	-	Address bus 19 for CPU (Not connect.)
43	VSS	-	Ground
44	A20	-	Address bus 20 for CPU (Not connect.)
45	DISCSTP	O	DISC STOP control
46	HAGUP	O	H/A gain control
47	TCLOSE	-	Not connect.
48	WOBBLEFIL	-	Not connect.
49	/HFMON	I	HF monitor
50	TRVSW	I	Detection switch of traverse inside

Pin No.	Symbol	I/O	Function
51	SWUPDN	-	Not connect.
52	MECHA_H/V	I	Disc detection
53	DISCSET	O	Serial enable signal for ADSC
54	VDD	-	Power supply
55	FEPEN	O	Serial enable signal for FEP
56	SLEEP	O	Standby signal for FEP
57	BUSY	-	Not connect.
58	REQ	O	Communication request
59		-	Connect to TP405 (REQ)
60		-	Not connect.
61	VSS	-	Ground
62	EPCS	O	EEPROM chip select
63	EPSK	O	EEPROM clock
64	EPDI	I	EEPROM data input
65	EPDO	O	EEPROM data output
66	VDD	-	Power supply
67	SCLKO	I	Communication clock
68	S2UTD	I	Communication input data
69	U2SDT	O	Communication output data
70	CPSCK	O	Clock for ADSC serial
71	P74/SBI1	-	Connect to VSS
72	SDOUT	O	ADSC serial data output
73		-	Not use. (Pull-up to power supply)
74		-	Not use. (Pull-up to power supply)
75	NMI	-	Not use. (Pull-up to power supply)
76	ADSCIRQ	I	Interrupt input of ADSC
77	ODCIRQ	I	Interrupt input of ODC
78	DECIRQ	I	Interrupt input of ZIVA
79	CSSIRQ	I	Interrupt input of SODC
80	ODCIRQ2	I	Interruption of system control
81	ADSEP	I	Address data selection input (Pull-up to power supply)
82	RST	I	Reset input
83	VDD	-	Power supply
84-91	TEST1-TEST 8	I	Test signal (1-8) input (Not connect.)
92	VSS	-	Ground
93-100	D0-7	I/O	Data bus (0-7) of CPU

4.28 MN103S26EGA (IC301) : Optical disc controller

• Pin layout



• Pin function

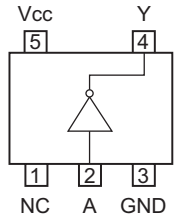
Pin No.	Symbol	I/O	Function
1	NINT0	O	System control interruption 0
2	NINT1	O	System control interruption 1
3	VDD3	-	Power supply (3.3V)
4	VSS	-	Ground
5	NINT2	O	System control interruption 2
6	WAITODC	O	System control wait control
7	NMRST	-	System control reset (Not connect.)
8	DASPST	-	DASP signal initializing
9~17	CPUADR17 - 9	I	System control address
18	VDD18	-	Power supply (1.8V)
19	VSS	-	Ground
20	DRAMVDD18	-	Connect to VDD18
21	DRAMVSS	-	Connect to VSS
22~30	CPUADR8 - 0	I	System control address
31	VDD3	-	Power supply (3.3V)
32	VSS	-	Ground
33	DRAMVDD3	-	Connect to VDD3
34	NCS	I	System control chip select
35	NWR	I	System control write
36	NRD	I	System control read
37~44	CPUDT7 - 0	I/O	System control data
45	CLKOUT1	-	Not connect.
46	MMOD	I	Connect to VSS
47	NRST	I	System reset
48	MSTPOL	I	Master terminal polarity switch input (Connect to VSS.)
49	SCLOCK	-	Not connect.
50	SDATA	-	Not connect.
51	OFTR	I	Off track signal input
52	BDO	I	RF dropout/BCA data of making to binary
53~56	PWM1 - 4	-	Not connect.
57	VDD3	-	Power supply (3.3V)
58	DRAMVDD18	-	Connect to VDD18
59	DRAMVSS	-	Connect to VSS
60	VSS	-	Ground
61~64	PWM5 - 8	-	Not connect.
65	TBAL	O	Tracking balance adjustment output
66	FBAL	O	Focus balance adjustment output
67	TRSDRV	O	Traverse drive output
68	SPDRV	O	Spindle drive output
69	FG	I	Motor FG input
70	TILTP	-	Not connect.

Pin No.	Symbol	I/O	Function
71	TILT	-	Not connect.
72	TILTN	-	Not connect.
73	TX	-	Not connect.
74	DTRD	-	Not connect.
75	IDGT	-	Not connect.
76	VDD18	-	Power supply (1.8V)
77	VSS	-	Ground
78	VDD3	-	Power supply (1.8V)
79	OSCI1	I	16.9MHz clock input
80	OSCO1	-	Not connect.
81	VSS	-	Ground
82	TSTSG	O	Calibration signal
83	VFOSHORT	O	VFO short output
84	JLINE	O	J-line setting output
85	AVSS	-	Analog ground
86	ROUT	-	Not connect.
87	LOUT	-	Not connect.
88	AVDD	-	Analog power supply
89	VCOF	I	JFVCO control voltage
90	TRCRS	I	Input signal for track cross formation
91	CMPIN	-	Not connect.
92	LPFOUT	-	Not connect.
93	LPFIN	I	Pull-up to VHALF
94	AVSS	-	Analog ground
95	HPFOUT	-	Not connect.
96	HPFIN	I	HPF input
97	CSLFLT	I	Pull-up to VHALF
98	RFOIF	-	Not connect.
99	AVDD	-	Analog power supply
100	PLFLT2	I	Connect to capacitor 2 for PLL
101	PLFLT1	I	Connect to capacitor 1 for PLL
102	AVSS	-	Analog ground
103	RVI	I	Connect to resistor for VREF reference current source
104	VREFH	I	Reference voltage input (2.2V)
105	PLPG	-	Not connect.
106	VHALF	I	Reference voltage input (1.65V)
107	DSLF2	I	Connect to capacitor 2 for DSL
108	DSLF1	I	Connect to capacitor 1 for DSL
109	AVDD	-	Analog power supply
110	NARF	I	Equivalence RF-
111	ARF	I	Equivalence RF+
112	JITOUT	O	Output for jitter signal monitor
113	AVSS	-	Analog ground
114	DAC0	O	Tracking drive output
115	DAC1	O	Focus drive output
116	AVDD	-	Analog power supply
117	AD0	I	Focus error input
118	AD1	I	Phase difference/3 beams tracking error

Pin No.	Symbol	I/O	Function
119	AD2	I	AS: Full adder signal
120	AD3	I	RF envelope input
121	AD4	I	DVD laser current control terminal
122	AD5	I	Tracking drive IC input offset
123	AD6	I	CD laser current control terminal
124	TECAPA	-	Not connect.
125	VDD3	-	Power supply (3.3V)
126	VSS	-	Ground
127~130	MONI0 - 3	O	Internal goods title monitor (Connect to TP306 - TP309)
131	NEJECT	I	Eject detection
132	NTRYCTL	I	Tray close detection
133	NDASP	I/O	ATAPI drive active / Slave connection I/O
134	NCS3FX	I	ATAPI host chip select (Not connect.)
135	NCS1FX	I	ATAPI host chip select (Not connect.)
136	DA2	I/O	ATAPI host address
137	DA0	I/O	ATAPI host address (Not connect.)
138	NPDIAG	I/O	ATAPI slave master diagnosis input
139	DA1	I/O	ATAPI host address (Not connect.)
140	NIOCS16	-	ATAPI output of selection of host data bus width (Not connect.)
141	INTRQ	O	ATAPI host interruption output
142	NDMACK	I	ATAPI host DMA response (Not connect.)
143	VDD3	-	Power supply (3.3V)
144	VSS	-	Ground
145	IORDI	-	ATAPI host ready output (Not connect.)
146	NIORD	I	ATAPI host read (Not connect.)
147	NIOWR	I/O	ATAPI host write
148	DMARQ	-	ATAPI host DMA request (Not connect.)
149~151	HDD15,HDD0,HDD14	I/O	ATAPI host data 15,0,14
152	VDD18	-	Power supply (1.8V)
153	PO	-	Connect to ground
154	UATASEL	I	Connect to VSS
155	VSS	-	Ground
156	VDD3	-	Power supply (3.3V)
157~159	HDD1,HDD13,HDD2	I/O	ATAPI data 1,13,2
160161	HDD12,HDD3	I/O	ATAPI data 12,3
162	VDD3	-	Power supply (3.3V)
163	VSS	-	Ground
164~166	HDD11,HDD4,HDD10	I/O	ATAPI data 11,4,10
167168	HDD5,HDD9	I/O	ATAPI data 5,9
169	VDD3	-	Power supply (3.3V)
170	VSS	-	Ground
171~173	HDD6,HDD8,HDD7	I/O	ATAPI data 6,8,7
174	VDDH	-	Reference power supply for ATAPI (5.0V)
175	NRESET	I	ATAPI host reset
176	MASTER	I/O	ATAPI master / Slave selection

4.29 NC7S04P5-X (IC533) : Invereter

• Pin layout & Block diagram



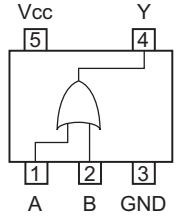
• Truth table

INPUT	OUTPUT
A	Y
L	H
H	L

H : HIGH logic level
L : LOW logic level

4.30 NC7ST32P5-X (IC532) : 2-Input OR Gate

• Pin layout & Block diagram



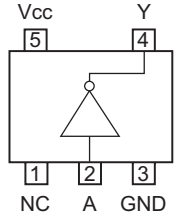
• Truth table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H : HIGH logic level
L : LOW logic level

4.31 NC7SU04P5-X (IC522) : Invereter

• Pin layout & Block diagram



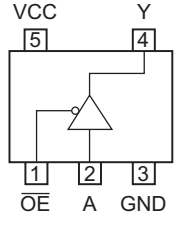
• Truth table

INPUT	OUTPUT
A	Y
L	H
H	L

H : HIGH logic level
L : LOW logic level

4.32 NC7SZ125P5-X (IC523) : Bus buffer gate with 3-state output

• Pin layout & Block diagram



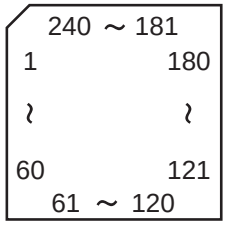
• Truth table

INPUTS		OUTPUT
$\overline{OE}$	B	Y
L	H	H
L	L	L
H	X	Z

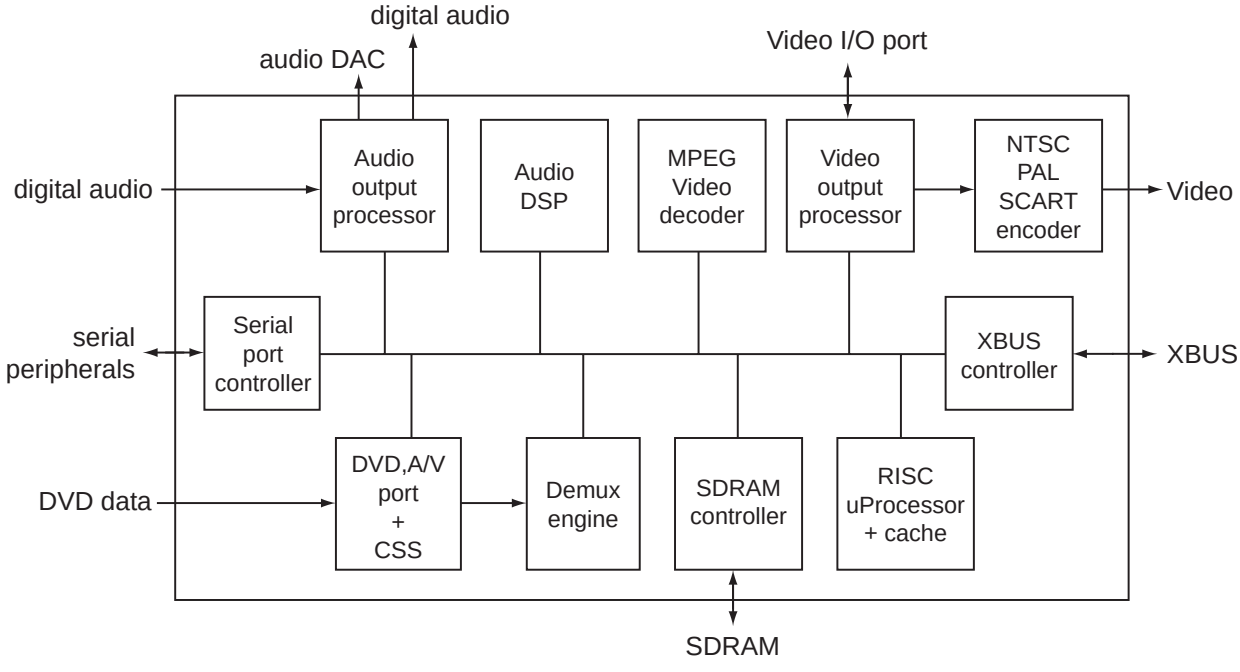
X: Don't care
Z: High impedance

4.33 NDV8601VWA-BE (IC501) : DVD on a chip processor

- Pin layout



- Block diagram



- Pin function

Pin No.	Symbol		Description
1	VDDio	-	Power supply terminal 3.3V
2,3	MD10,11	I/O	SDRAM Data bus terminal
4	VDD	-	Power supply terminal 1.8V
5	MD12	I/O	SDRAM Data bus terminal
6	VSSio	-	Connect to ground
7~9	MD13~15	I/O	SDRAM Data bus terminal
10	VDDio	-	Power supply terminal 3.3V
11	DQM1	O	SDRAM Data byte enable
12,13	MA9,8	O	SDRAM Address bus terminal
14	VSSio	-	Connect to ground
15,16	MA7,6	O	SDRAM Address bus terminal
17	VSS	-	Connect to ground
18	MA5	O	SDRAM Address bus terminal
19	VDDio	-	Power supply terminal 3.3V
20,21	MA4,3	O	SDRAM Address bus terminal
22	MCLK	O	SDRAM Clock output
23	VSSio	-	Connect to ground
24	CKE	O	SDRAM Clock enable output

Pin No.	Symbol		Description
25,26	MA2,1	O	SDRAM Address bus terminal
27	VDDio	-	Power supply terminal 3.3V
28	MA0	O	SDRAM Address bus terminal
29	MA10	O	SDRAM Address bus terminal
30	MA11	-	Non connect
31	VSSio	-	Connect to ground
32,33	MA12,13	O	SDRAM Address bus, reserved for terminal compatibility with 64Mb SDRAM
34	VDD	-	Power supply terminal 1.8V
35	CS0	O	SDRAM Primary bank chip select
36	VDDio	-	Power supply terminal 3.3V
37	RAS	O	SDRAM Command bit
38	CAS	O	SDRAM Command bit
39	WE	O	SDRAM Command bit
40	VSSio	-	Connect to ground
41	DQM0	O	SDRAM Data byte enable
42	DQM2	O	SDRAM Data byte enable
43	MD16	I/O	SDRAM Data bus terminal
44	VDDio	-	Power supply terminal 3.3V
45,46	MD17,18	I/O	SDRAM Data bus terminal
47	VSS	-	Connect to ground
48	MD19	I/O	SDRAM Data bus terminal
49	VSSio	-	Connect to ground
50~52	MD20~22	I/O	SDRAM Data bus terminal
53	VDDio	-	Power supply terminal 3.3V
54~56	MD23~25	I/O	SDRAM Data bus terminal
57	VSSio	-	Connect to ground
58~61	MD26~29	I/O	SDRAM Data bus terminal
62	VDDio	-	Power supply terminal 3.3V
63,64	MD30,31	I/O	SDRAM Data bus terminal
65	DQM3	O	SDRAM Data byte enable
66	CS1	O	SDRAM Extension bank chip select
67	VSSD	-	Connect to ground
68	SPDIF	O	S/PDIF Digital audio output terminal
69	VSSio	-	Connect to ground
70	AIN	I	Digital audio input for digital micro; can be used as GPIO
71	AOUT3	O	Serial audio output data to audio DAC for left and right channels for down-mix
72	AOUT2	O	Serial audio output data to audio DAC for surround left and right channels
73	AOUT1	O	Serial audio output data to audio DAC for center and LFE channels
74	AOUT0	O	Serial audio output data to audio DAC for left and right channels
75	VDDio	-	Power supply terminal 3.3V
76	PCMCLK	O	Audio DAC PCM sampling clock frequency, common clock for DACs and ADC
77	VDD	-	Power supply terminal 1.8V
78	ACLK	O	Audio interface serial data clock, common clock for DACs and AD converter
79	LRCLK	O	Left / right channel clock, common clock for DACs and ADC
80	SRST	O	Active low RESET signal for peripheral reset
81	RSTP	I	RESET_Power : from system, used to reset frequency synthesizer and rest of chip

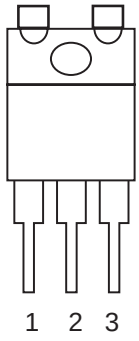
Pin No.	Symbol		Description
82	VSSio	-	Connect to ground
83	RXD1	I	UART1 Serial data input from external serial device, used for IR receiver
84	SSPIN1	I/O	SSP1 Data in or 16X clock for USART function in UART1
85	VSS	-	Connect to ground
86	SSPOUT1	I/O	SSP1 Data out or UART1 data-terminal-ready signal
87	SSPCLK1	I/O	SSP1 Clock or UART1 clear-to -send signal
88	SSPCLK0	I/O	SSP0 Clock or request-to-send function in UART1
89	VDD	-	Power supply terminal 1.8V
90	SSPIN0	I/O	SSP0 Data in or 16X clock for USART function in UART0
91	VDDio	-	Power supply terminal 3.3V
92	SSPOUT0	I/O	SSP0 Data out or UART0 data-terminal-ready signal
93	TXD0	I/O	UART0 Serial data output to an external serial device
94	RXD0	I	UART0 Serial data input from external serial device
95	CTS0	I/O	UART0 Clear-to-send signal
96	RTS0	I/O	UART0 Request-to-send signal
97	VSSio	-	Connect to ground
98	CXI	I	Crystal input terminal for on-chip oscillator or system input clock
99	CXO	O	Crystal output terminal for on-chip oscillator
100	OSCVSS	-	Connect to ground for oscillator
101	OSCVDD	-	Power supply terminal for oscillator 1.8V
102	MVCKVDD	-	Power supply terminal for main and video clock PLL 3.3V
103	SCEN	I	Scan chain test enable
104	MVCKVSS	-	Connect to ground for main and video clock PLL
105	ACLKVSS	-	Connect to ground for audio clock PLL
106	SCMD	I	Scan chain test mode
107	ACLKVDD	-	Power supply terminal for audio clock PLL 3.3V
108	VDDDAK	-	Power supply terminal for DAC digital 1.8V
109	VSSDAC	-	Connect to ground for DAC digital
110	Cr/R	O	Video signal output (Cr output : composite/component Red output)
111	IOM	O	Cascaded DAC differential output used to dump current into external resistor for power
112	C/Cb/B	O	Video signal output (Chrominance output for NTSC/PAL S-Video
113	VAA3	-	Cb output for component Blue output)
114	Y/G	O	Power supply terminal for DAC analog 3.3V
115	VSSA	-	Video signal output (Luminance for S-Video and component Green output)
116	VREF	-	Connect to ground for DAC analog
117	VAA	-	Non connect
118	CVBS/C	O	Video signal output (Composite video Chrominance output for S-Video)
119	RSET	O	Current setting resistor of output DACs
120	COMP	O	Compensation capacitor connection
121	VSS	-	Connect to ground
122	VCLK	-	Non connect
123	VSYNC	-	Non connect
124	HSYNC	-	Non connect
125	VDDio	-	Power supply terminal 3.3V
126~131	VI07~02	-	Non connect
132	VSSio	-	Connect to ground

Pin No.	Symbol		Description
133,134	VI01,00	-	Non connect
135	VDD	-	Power supply terminal 1.8V
136~139	AD31~28	I/O	Multiplexed address / data bus terminal
140	VDDio	-	Power supply terminal
141~144	AD27~24	I/O	Multiplexed address / data bus terminal
145	PWE3	I/O	Byte write enable for FLASH,EEPROM,SRAM or peripherals terminal
146	AD23	I/O	Multiplexed address / data bus terminal
147	VSSio	-	Connect to ground
148~153	AD22~17	I/O	Multiplexed address / data bus terminal
154	VDDio	-	Power supply terminal 3.3V
155	AD16	I/O	Multiplexed address / data bus terminal
156	PWE2	I/O	Byte write enable for FLASH,EEPROM,SRAM or peripherals terminal
157,158	AD15,14	I/O	Multiplexed address / data bus terminal
159	VDD	-	Power supply terminal 1.8V
160	SCLK	O	External bus clock used for programmable host peripherals
161	ACK	I/O	Programmable WAIT/ACK/RDY control
162	VSSio	-	Connect to ground
163~168	AD13~8	I/O	Multiplexed address / data bus terminal
169	VDDio	-	Power supply terminal 3.3V
170	PWE1	I/O	Byte write enable for FLASH,EEPROM,SRAM or peripherals terminal
171	VSS	-	Connect to ground
172~176	AD7~3	I/O	Multiplexed address / data bus terminal
177	VSSio	-	Connect to ground
178~180	AD2~0	I/O	Multiplexed address / data bus terminal
181	VDDio	-	Power supply terminal 3.3V
182	PWE0	I/O	Byte write enable for FLASH,EEPROM,SRAM or peripherals terminal
183	ALE	I/O	Address latch enable
184~187	LA0~3	I/O	Latched address 0~3
188	VSSio	-	Connect to ground
189	RD	I/O	Read terminal
190	LHLDA	O	Bus hold acknowledge in slave mode
191	LHLD	I	Bus hold request from external master in slave mode
192	VDD	-	Power supply terminal 1.8V
193	PCS0	O	Peripheral chip select 0, generally used for enabling the program store ROM/FLASH
194,195	XI01,02	I/O	Programmable general purpose external input/output
196	VDDio	-	Power supply terminal 3.3V
197~200	XI03~06	I/O	Programmable general purpose external input/output
201	VSS	-	Connect to ground
202,203	XI07,08	I/O	Programmable general purpose external input/output
204	VSSio	-	Connect to ground
205	XI09	I/O	Programmable general purpose external input/output
206~209	XID10~13	I/O	Programmable general purpose external input/output
210	VDDio	-	Power supply terminal 3.3V
211	XID14	I/O	Programmable general purpose external input/output
212	VDD	-	Power supply terminal 1.8V
213	DSYNC	I	DVD Parallel mode sector sync

Pin No.	Symbol		Description
214	DREQ	O	DVD Parallel mode data request
215	DCLK	I	Data sampling clock
216	DSTB	I	Parallel mode data valid, serial mode left/right clock
217	DVD0	I	DVD Drive parallel data port
218	VSSio	-	Connect to ground
219~223	DVD1~5	I	DVD Drive parallel data port
224	VDDio	-	Power supply terminal 3.3V
225,226	DVD6,7	I	DVD Drive parallel data port
227	MD0	I/O	SDRAM Data bus terminal
228	VSSio	-	Connect to ground
229	MD1	I/O	SDRAM Data bus terminal
230	VSS	-	Connect to ground
231,232	MD2,3	I/O	SDRAM Data bus terminal
233	VDDio	-	Power supply terminal 3.3V
234~236	MD4~6	I/O	SDRAM Data bus terminal
237	VSSio	-	Connect to ground
238~240	MD7~9	I/O	SDRAM Data bus terminal

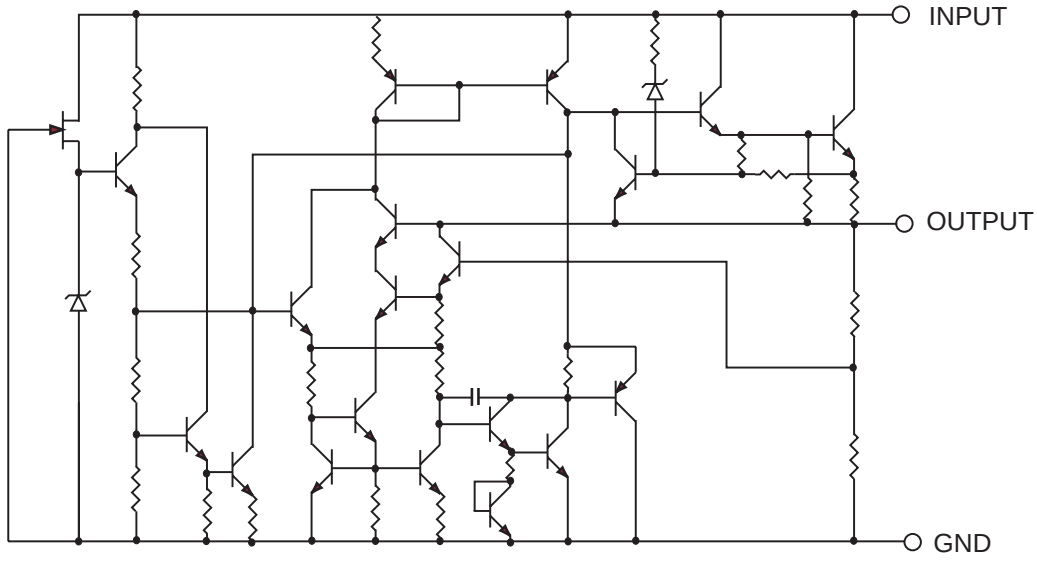
4.34 NJM78M05FA (IC291) : Regulator

- Terminal layout



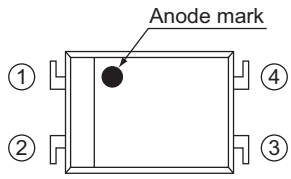
1.INPUT
2.GND
3.OUTPUT

- Block diagram

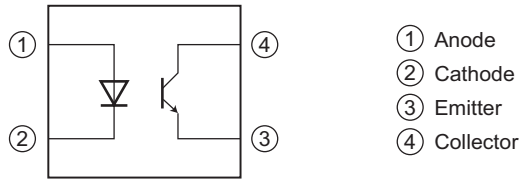


4.35 PC123Y02 (IC102/IC103/IC104/IC122/IC123) : Photocoupler

• Pin layout

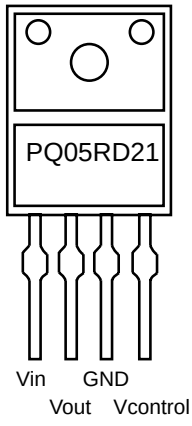


• Block diagram

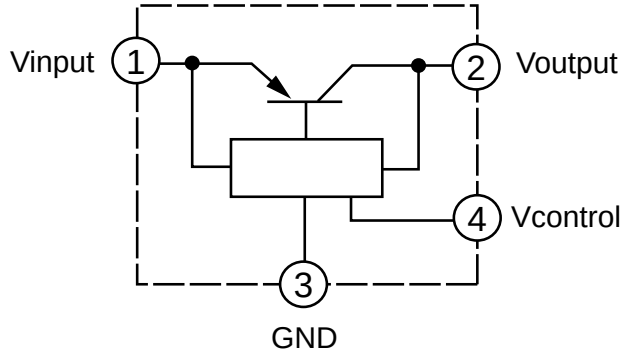


4.36 PQ05RD21 (IC171) : Regulator

• Terminal layout

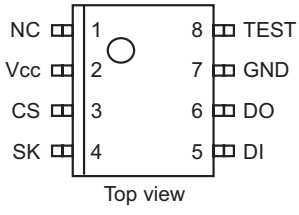


• Block diagram

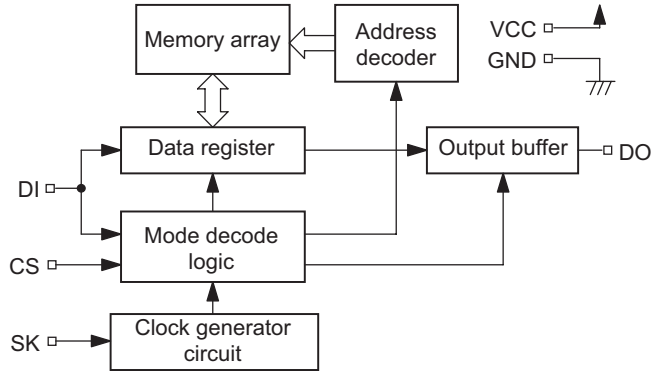


4.37 S-93C66AFJ-X (IC451) : Serial EEPROM

• Pin layout



• Block diagram

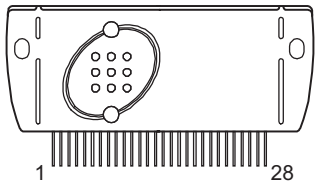


• Pin function

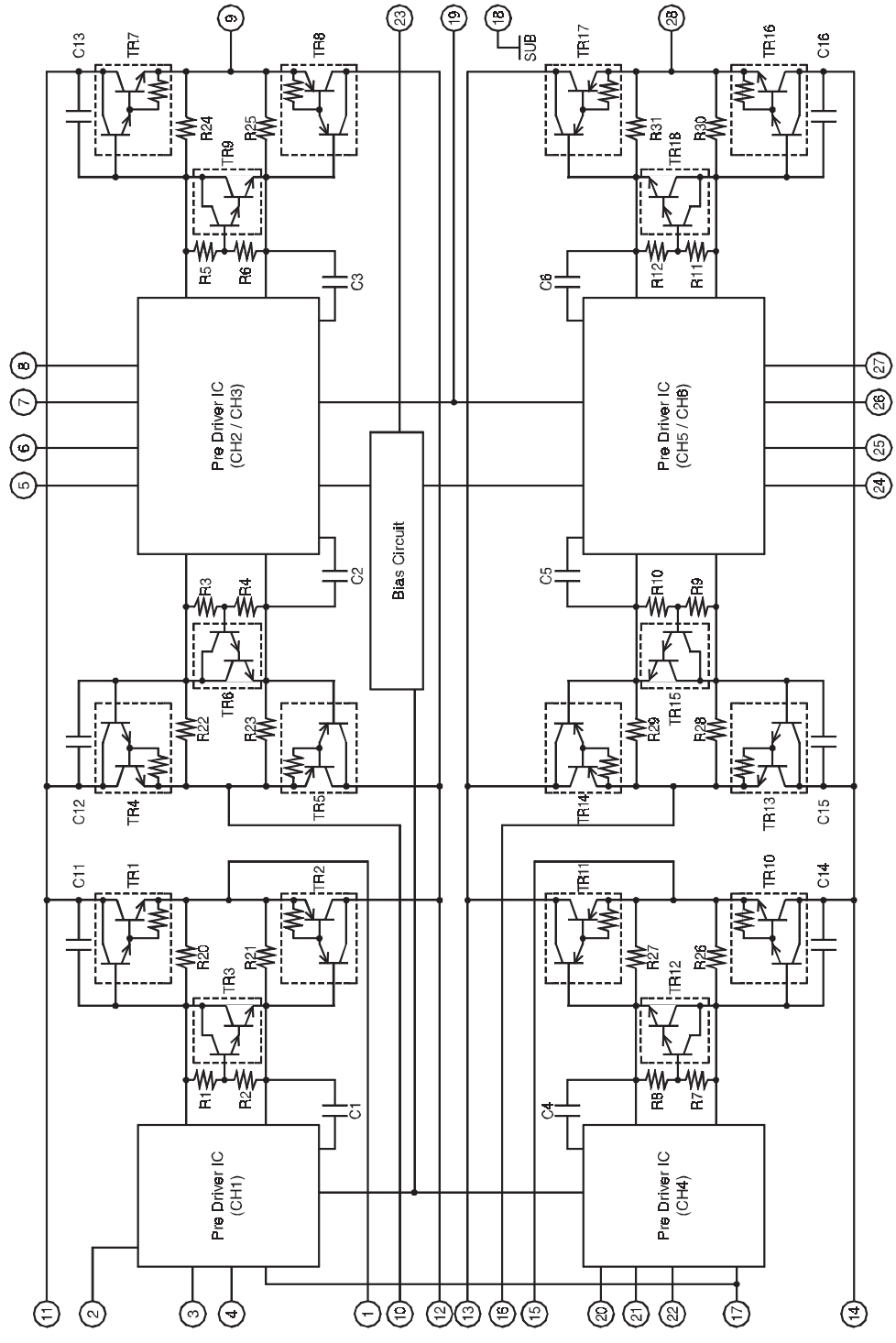
Pin No.	Symbol	Function
1	NC	Not connect
2	Vcc	Power supply
3	CS	Chip select input
4	SK	Serial clock input
5	DI	Serial data input
6	DO	Serial data output
7	GND	Ground
8	TEST	TEST pin:Open

4.38 STK403-430 (IC721) : Power amplifier

- Pin layout

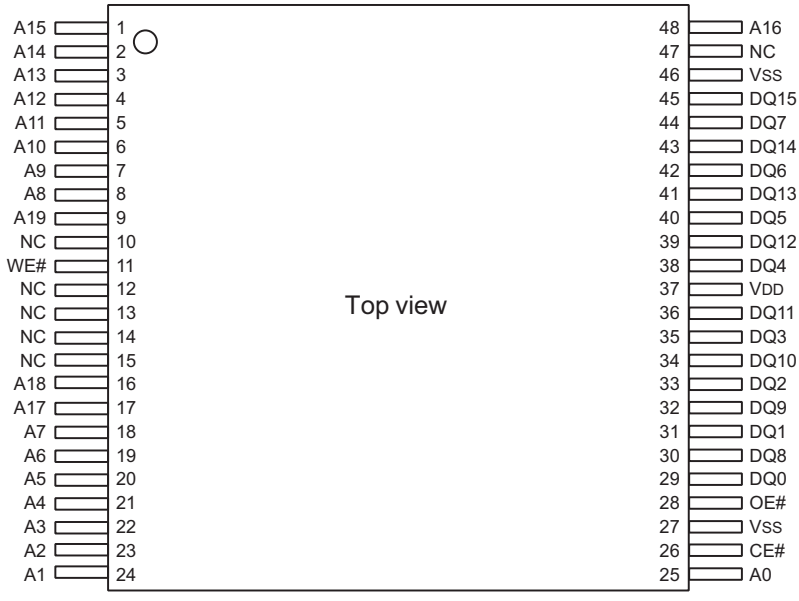


- Block diagram

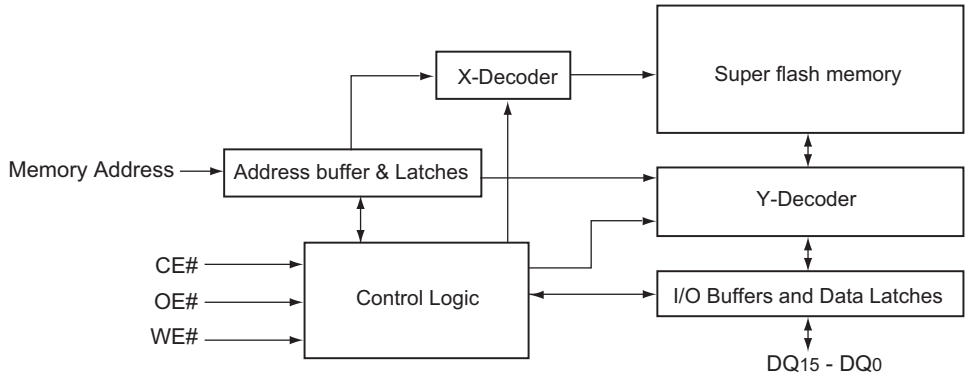


4.39 SST39VF160-7CEK (IC509) : 16 Mbit multi-purpose flash memory

- Pin layout



- Block diagram

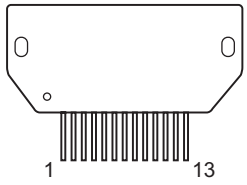


• Pin function

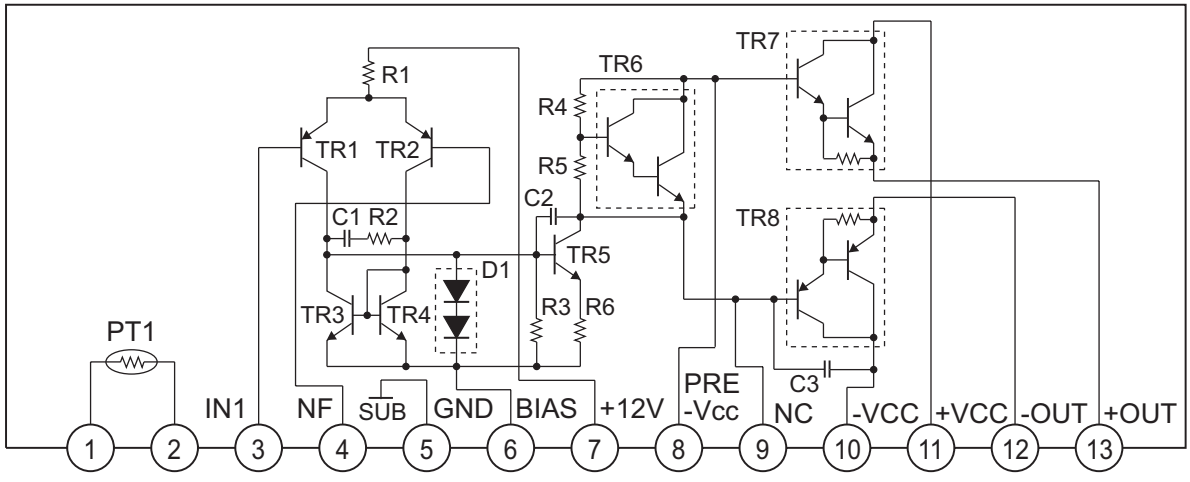
Pin No.	Symbol	I/O	Function
1-9	A15-A8,A19	I	Address inputs : To provide memory addresses. During Sector-Erase A19-A11 address lines will select the sector. During Block-Erase, A19-A15 address line will select the block.
10	NC	-	No connection : Unconnected pins
11	WE#	I	Write Enable : To control the Write operations
12-15	NC	-	No connection : Unconnected pins
16-25	A18,A17,A7-A0	I	Address inputs : To provide memory addresses. During Sector-Erase A19-A11 address lines will select the sector. During Block-Erase, A19-A15 address line will select the block.
26	CE#	I	Chip Enable : To activate the device when CE# is low.
27	VSS	-	Ground
28	OE#	I	Output Enable : To gate the data output buffers
29-36	DQ0,DQ8,DQ1 DQ9,DQ2,DQ10 DQ3,DQ11	I/O	Data input/output : To output data during Read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
37	VDD	-	Power supply : To provide power supply voltage (2.7-3.6V)
38-45	DQ4,DQ12,DQ5 DQ13,DQ6,DQ14 DQ7,DQ15	I/O	Data input/output : To output data during Read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
46	VSS	-	Ground
47	NC	-	No connection : Unconnected pins
48	A16	I	Address input : To provide memory address. During Sector-Erase A19-A11 address lines will select the sector. During Block-Erase, A19-A15 address line will select the block.

4.40 STK404-130 (IC701) : Power amplifier

- Pin layout

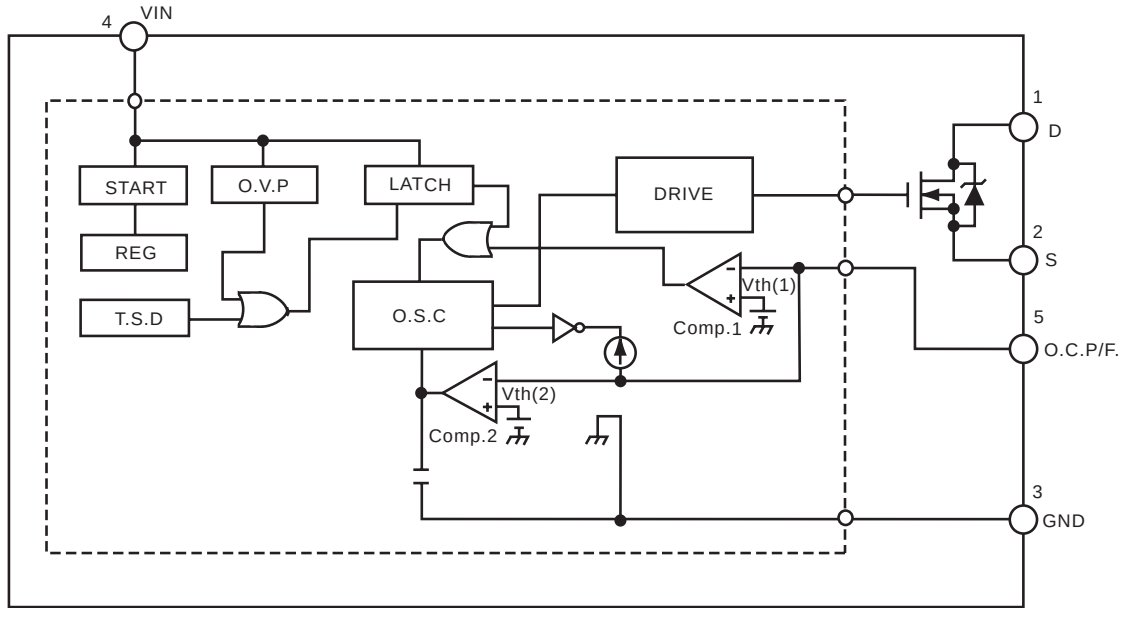


- Block diagram



4.41 STR-G6651 (IC121) : Switching regulator

- Block diagram

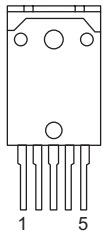


- Pin function

Pin No.	Symbol	Description	Function
1	D	Drain terminal	MOS FET drain
2	S	Source terminal	MOS FET source
3	GND	Ground terminal	Ground
4	Vin	Power supply terminal	Input of power supply for control circuit
5	O.C.P/F.B	Over current / Feedback terminal	Input of over current detection signal and constant voltage control signal

4.42STR-F6667B (IC101) : Switching regulator

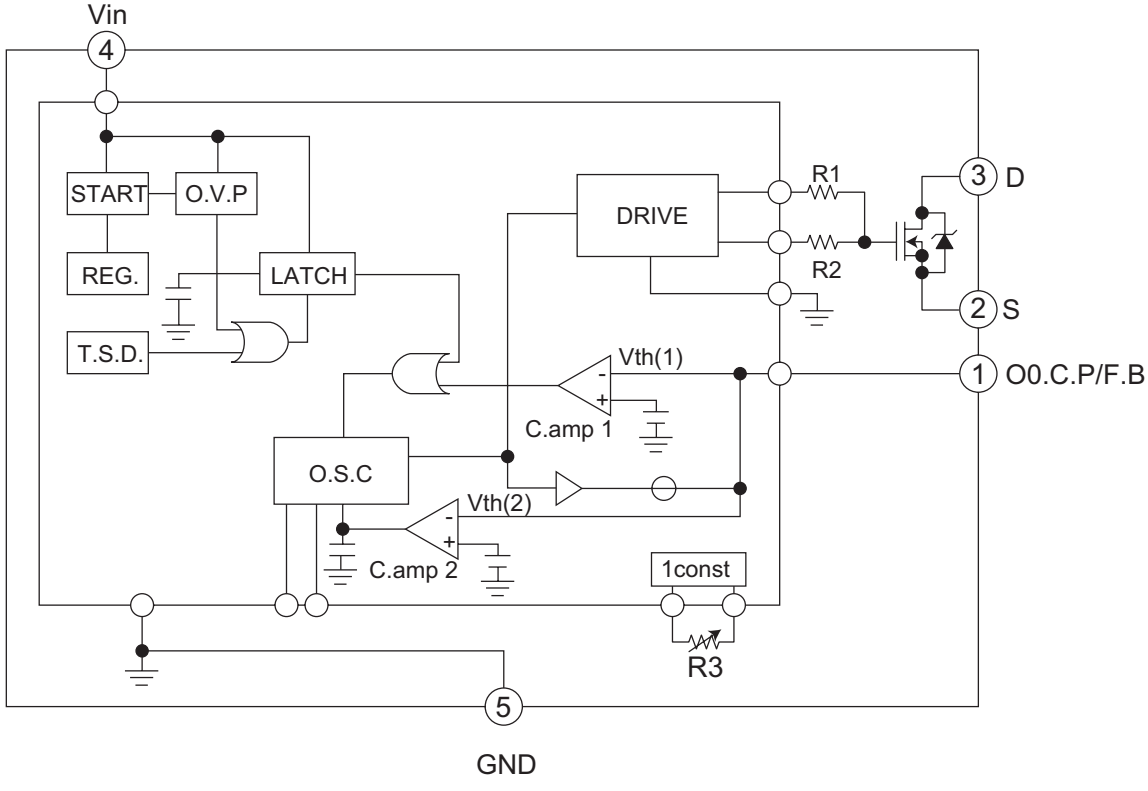
- Pin layout



- Pin function

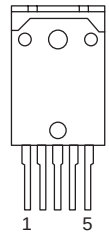
Pin No	Symbol	Function
1	O.C.P/F.B	Over current/Feedback terminal
2	S	Source terminal
3	D	Drain terminal
4	VIN	Power supply terminal
5	GND	Ground terminal
-	O.V.P	Overvoltage protection circuit
-	T.S.D	Thermal shutdown circuit

- Block diagram



4.43 STR-F6668B (IC101) : Switching regulator

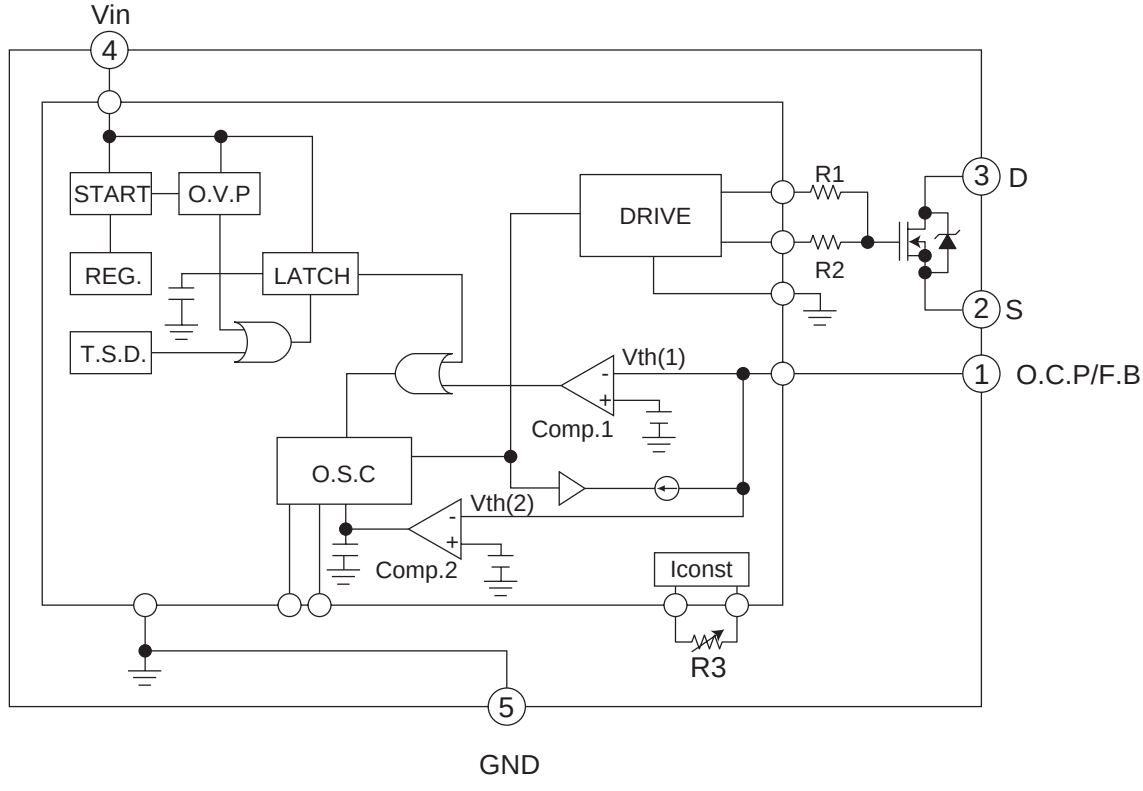
- Pin layout



- Pin function

Pin No	Symbol	Function
1	O.C.P/F.B	Over current/Feedback terminal
2	S	Source terminal
3	D	Drain terminal
4	VIN	Power supply terminal
5	GND	Ground terminal
-	O.V.P	Overvoltage protection circuit
-	T.S.D	Thermal shutdown circuit

- Block diagram



JVC

VICTOR COMPANY OF JAPAN, LIMITED
AV & MULTIMEDIA COMPANY 10-1,1chome,Ohwatari-machi,Maebashi-city,371-8543,Japan

(No.22009)

Printed in Japan
200302WPC

JVC

SCHEMATIC DIAGRAMS

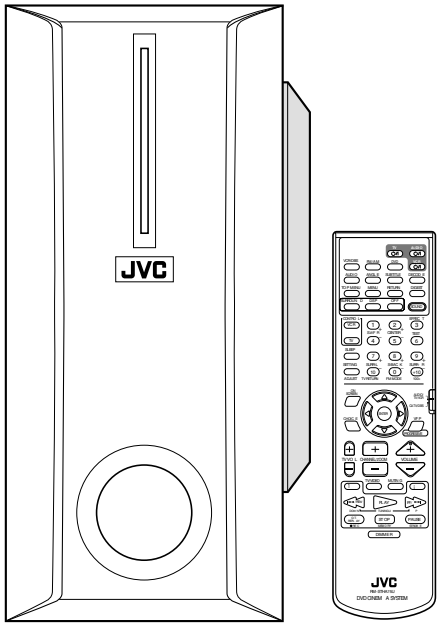
DVD DIGITAL CINEMA SYSTEM

TH-A75

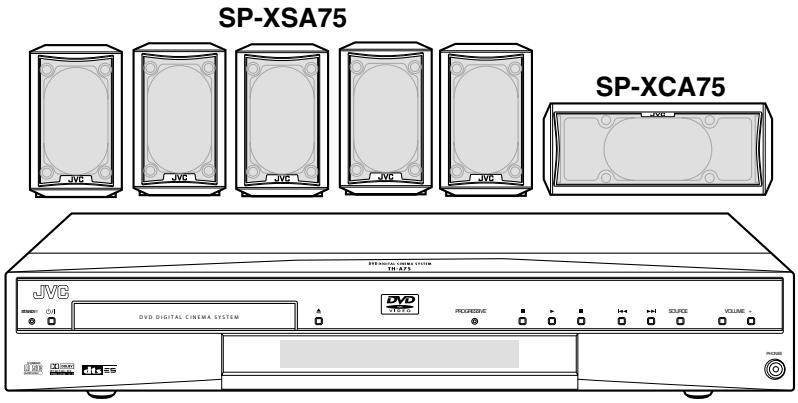
CD-ROM No.SML200302

Area suffix

US ---------- Singapore
UP ---------- Korea
UT ---------- Taiwan
UX ---------- Saudi Arabia



SP-WA75



SP-XSA75

SP-XCA75

XV-THA75

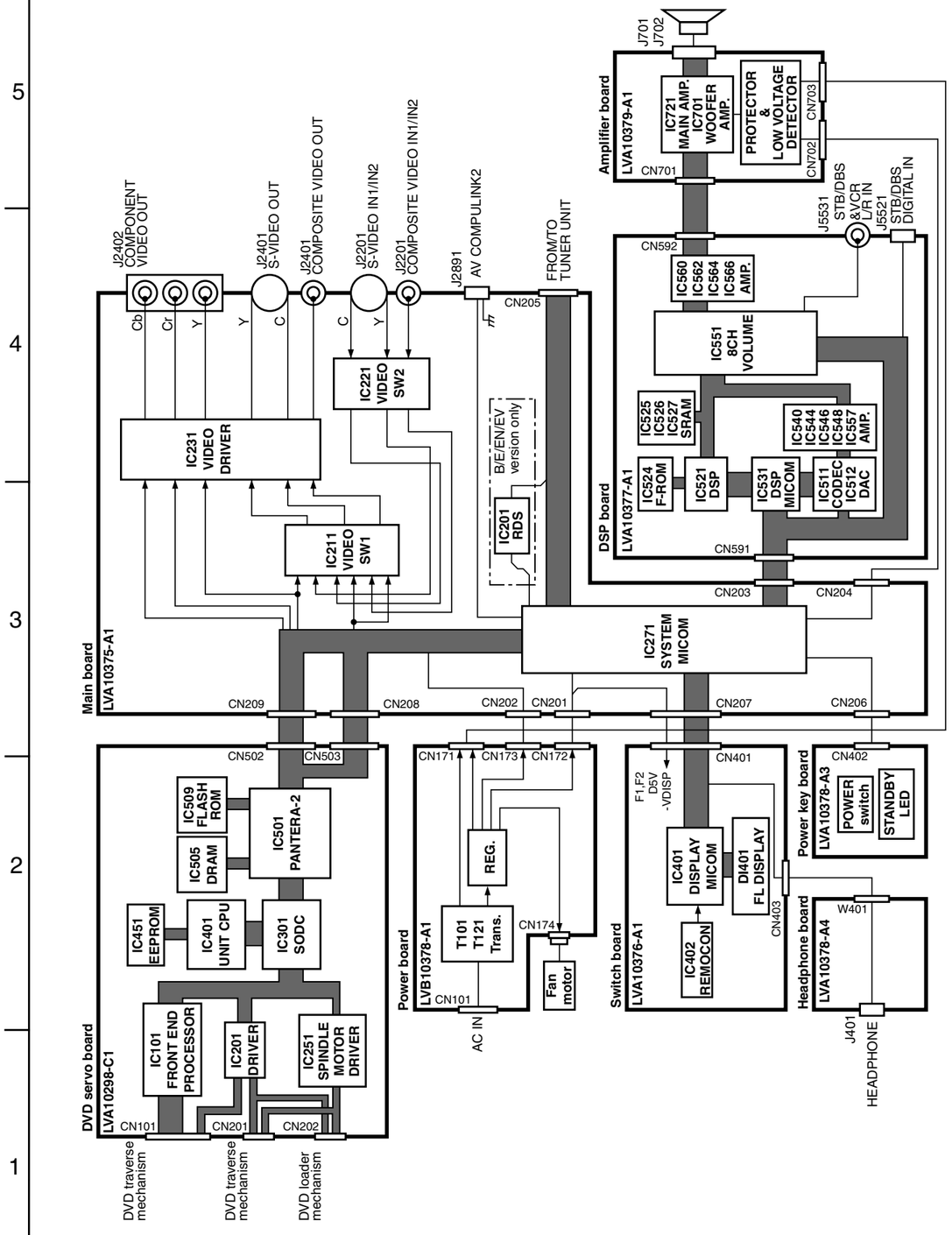
Contents

No.22009SCH
2003/02

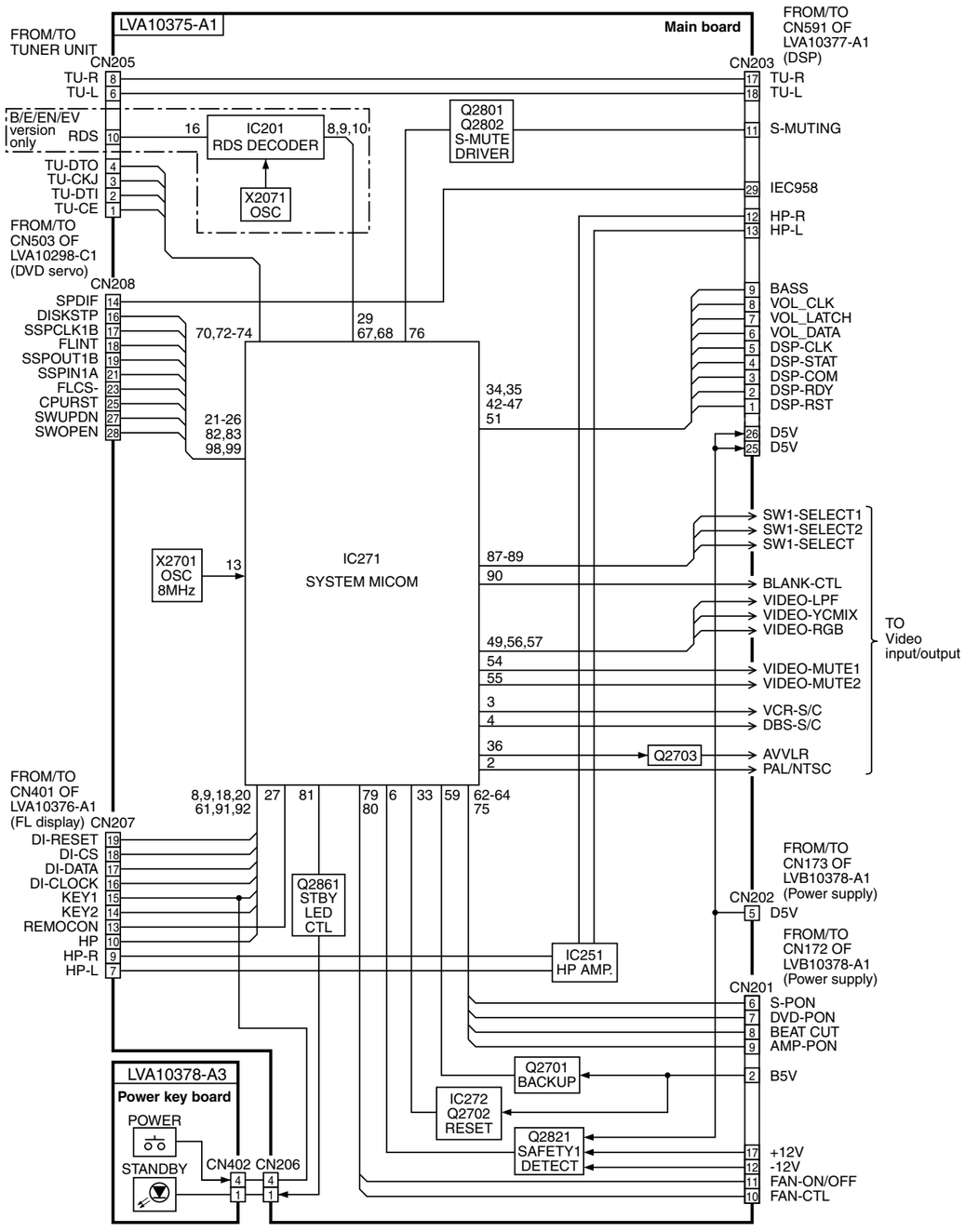
In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (▬), diode (▬|▬) and ICP (⬤) or identified by the "⚠" mark nearby are critical for safety.
(This regulation does not correspond to J and C version.)

Block diagrams

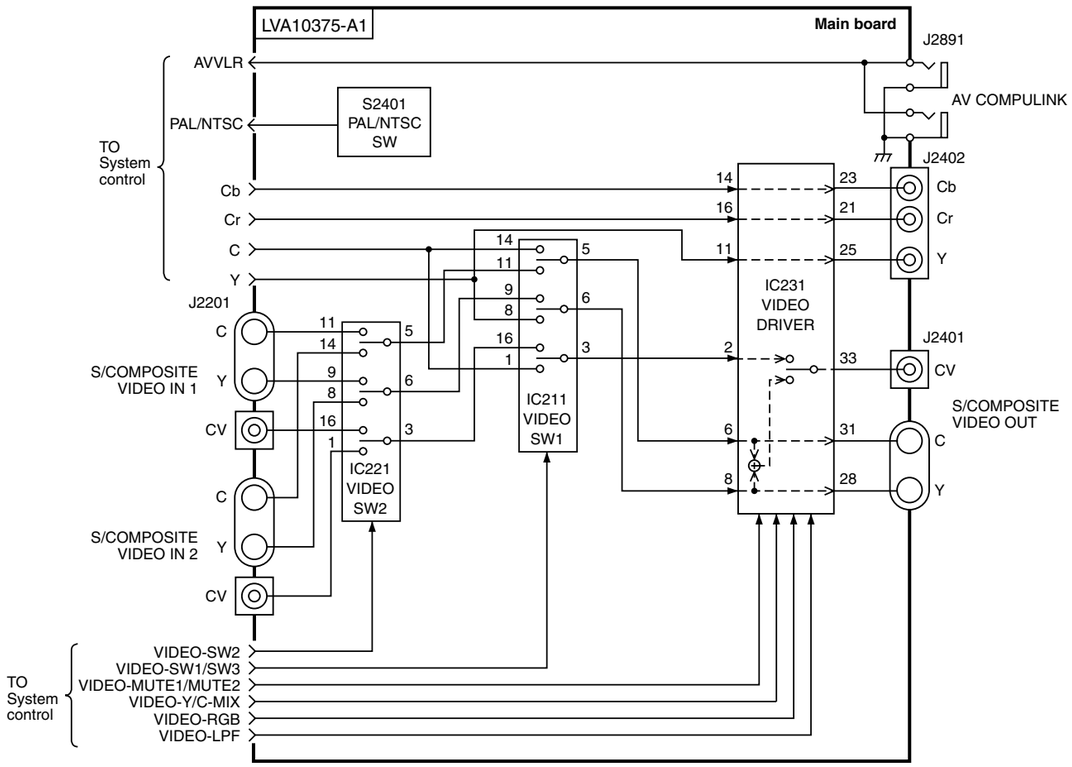
■ Overall block diagram



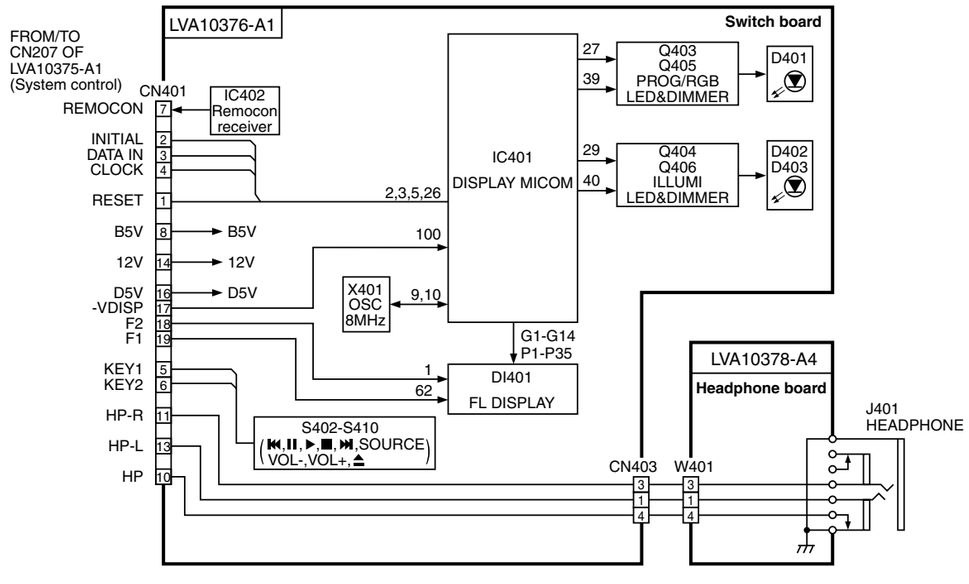
■ System control section



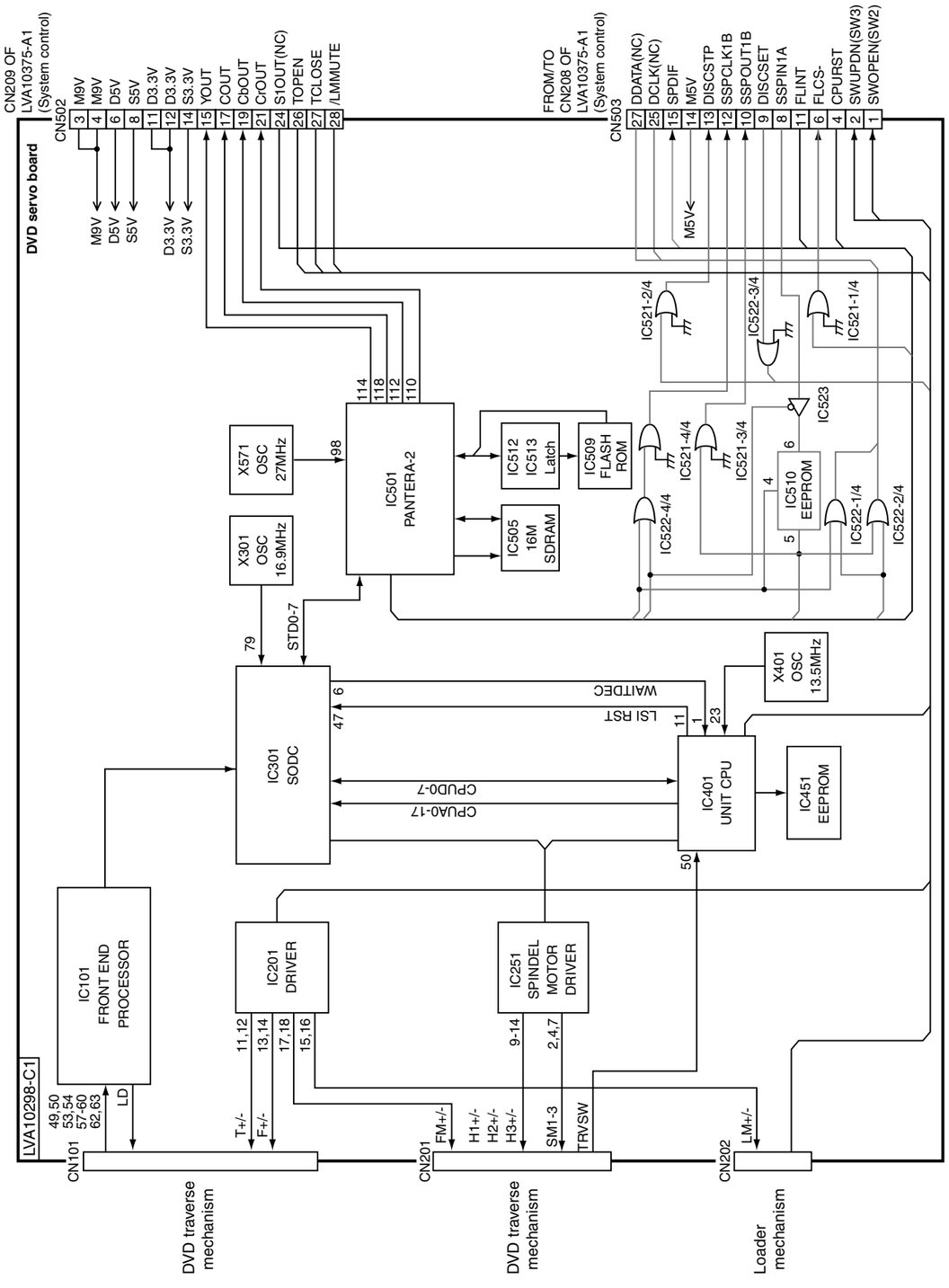
■ Video input/output section



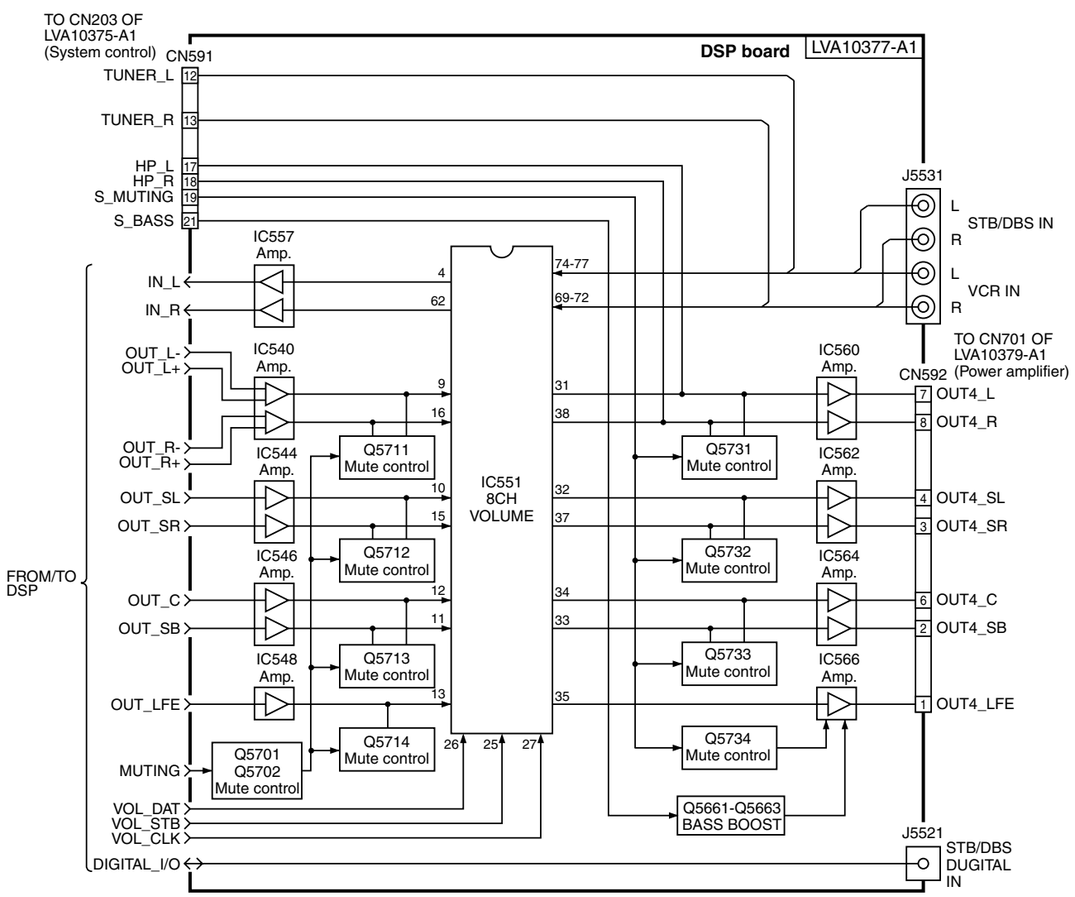
■ FL display section



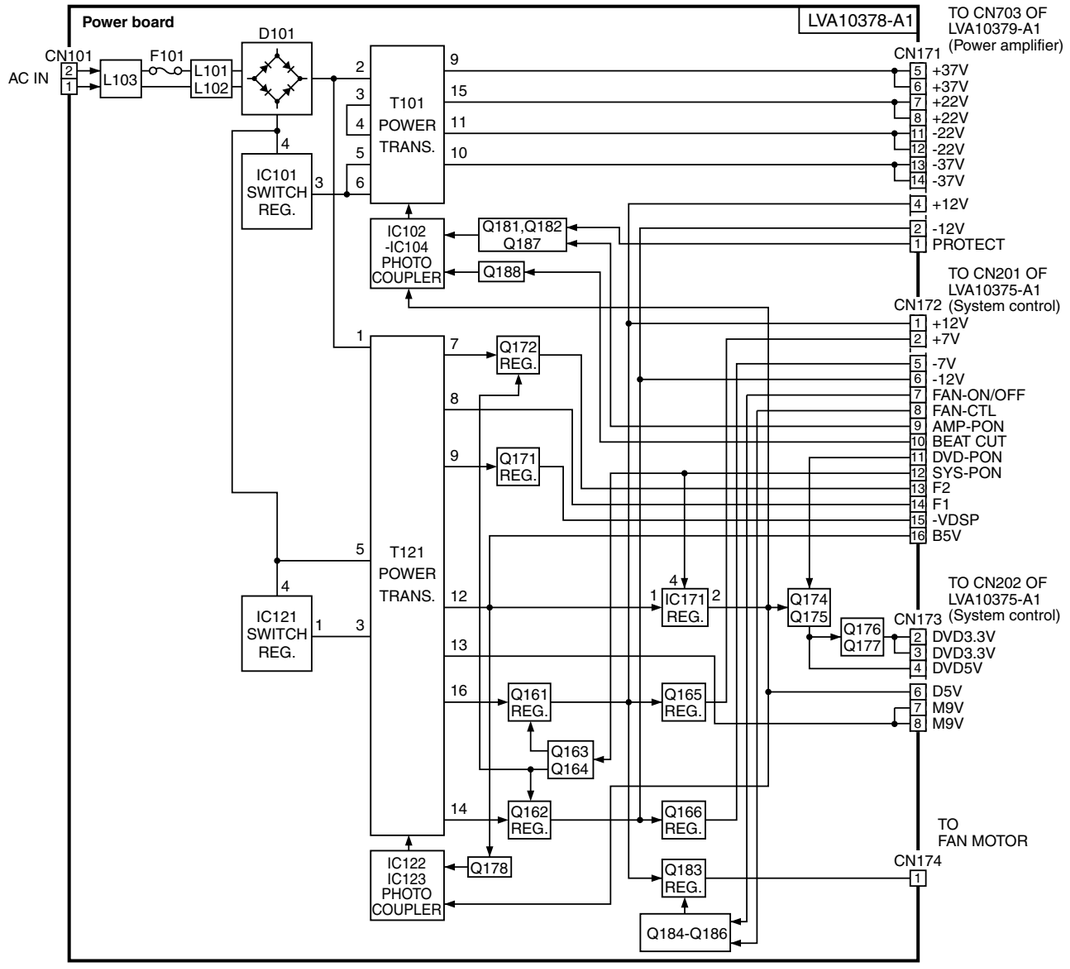
■ DVD servo section



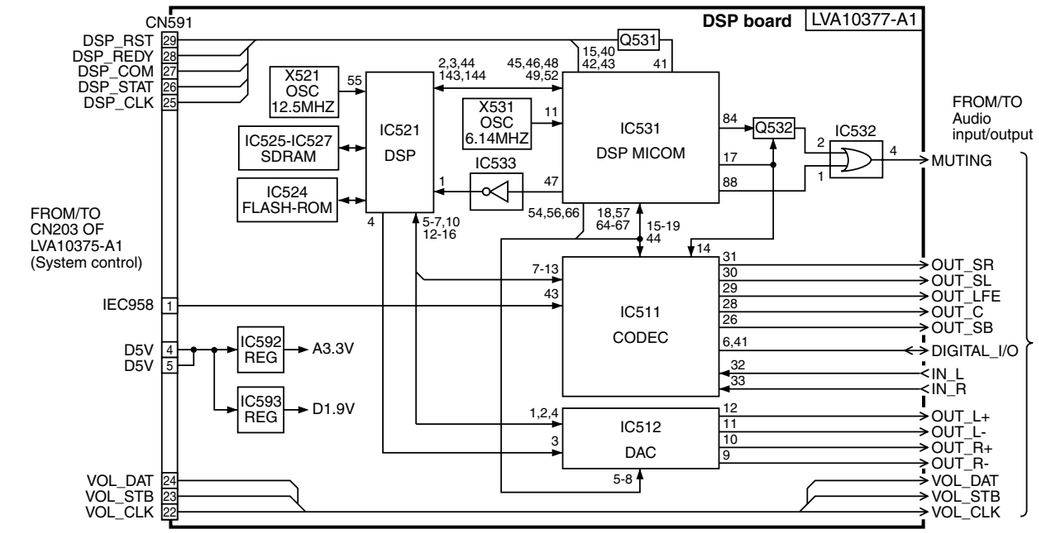
■ Audio input/output section



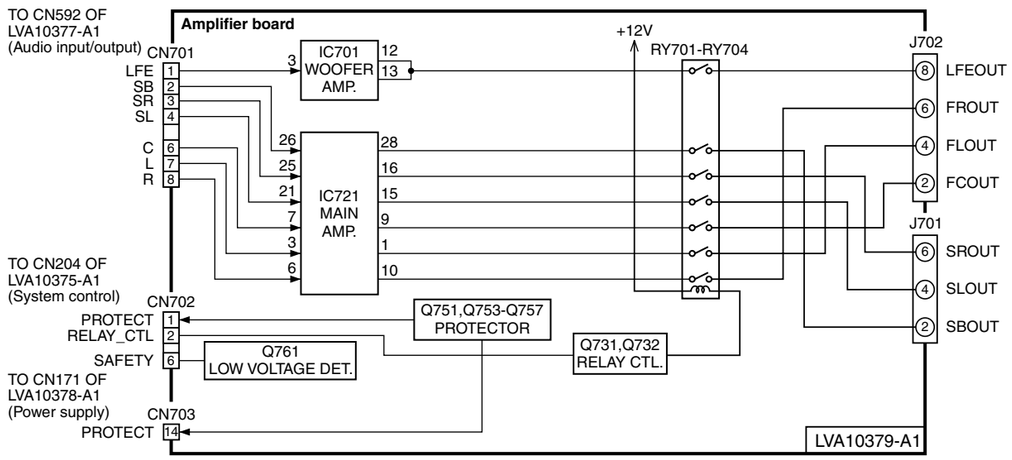
■ Power supply section



■ DSP section

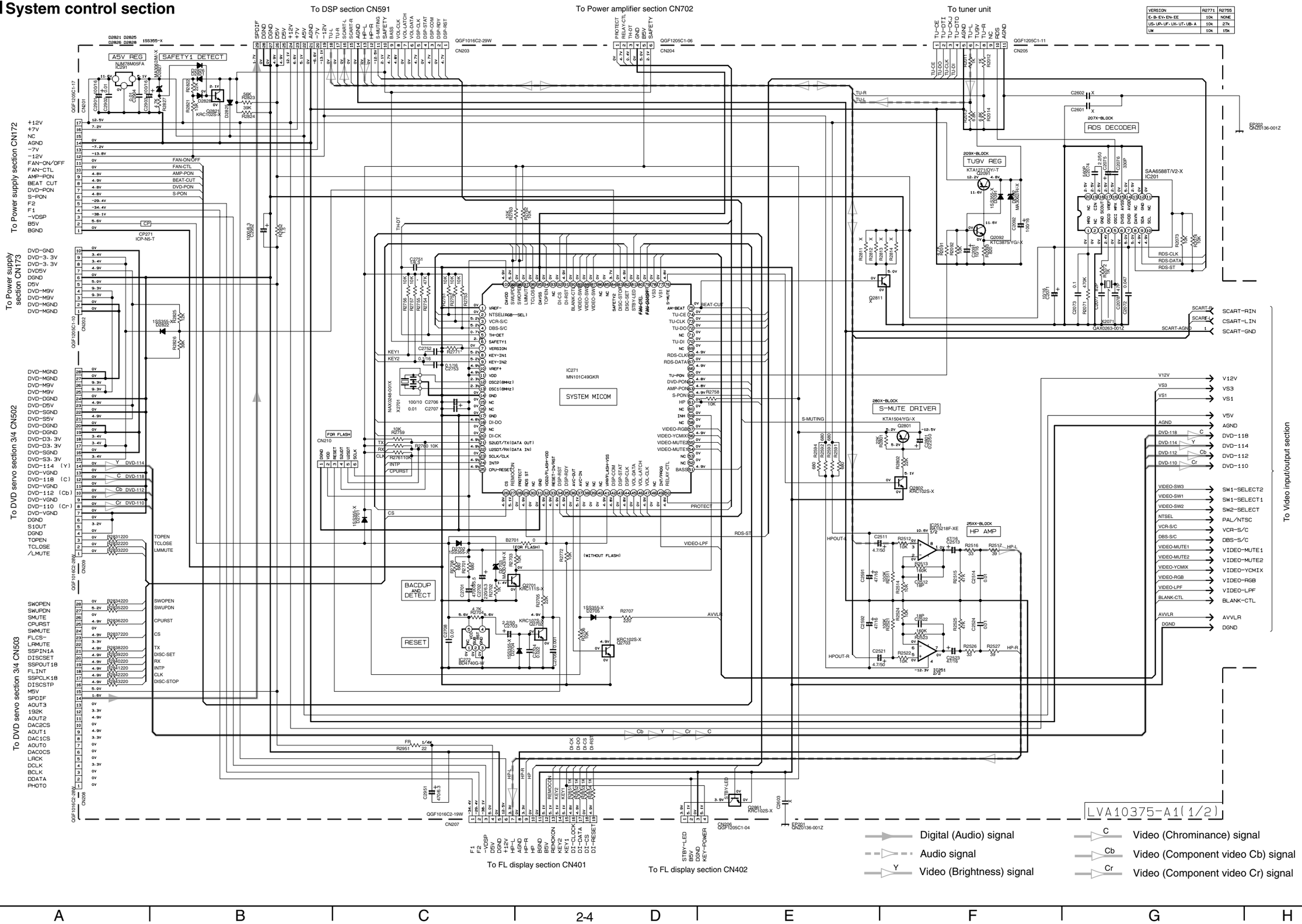


■ Power amplifier section



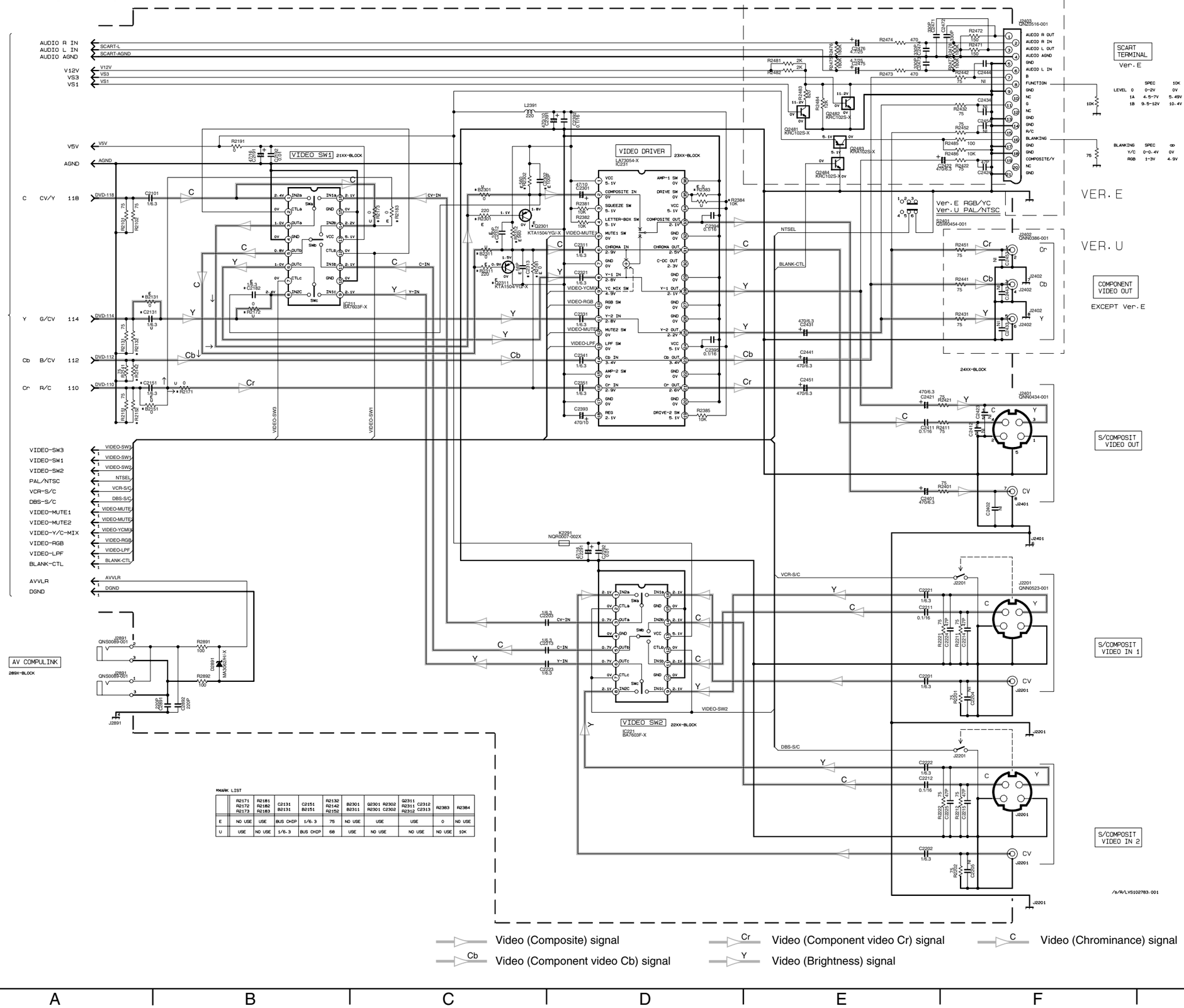
Standard schematic diagrams

■ System control section



VERSION	R2771	R2755
E-, B-, EV-, EN-, EE	10K	NONE
US-, UP-, UF-, UX-, UT-, UB-, A	10K	27K
UN	10K	15K

■ Video input/output section

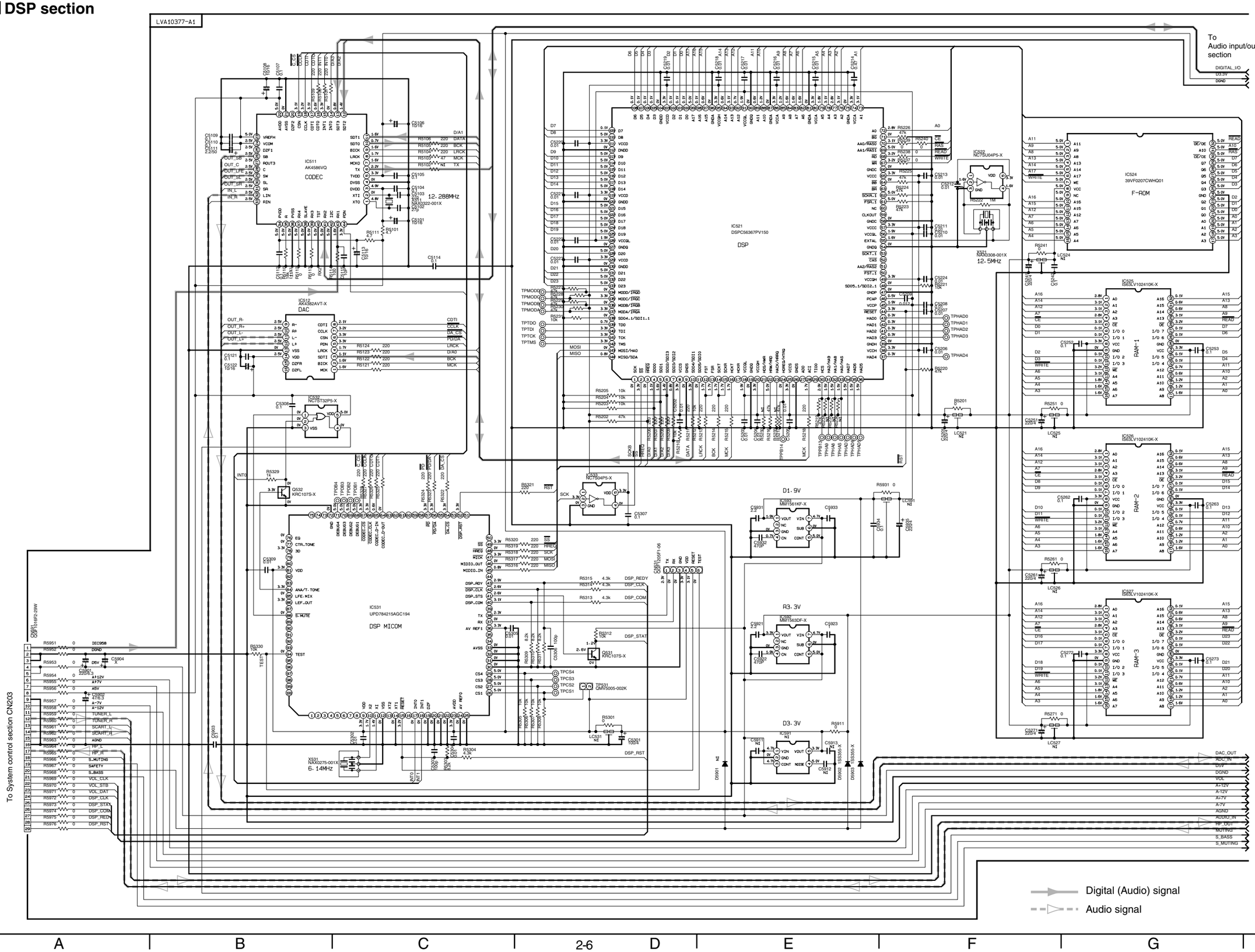


*MARK LIST

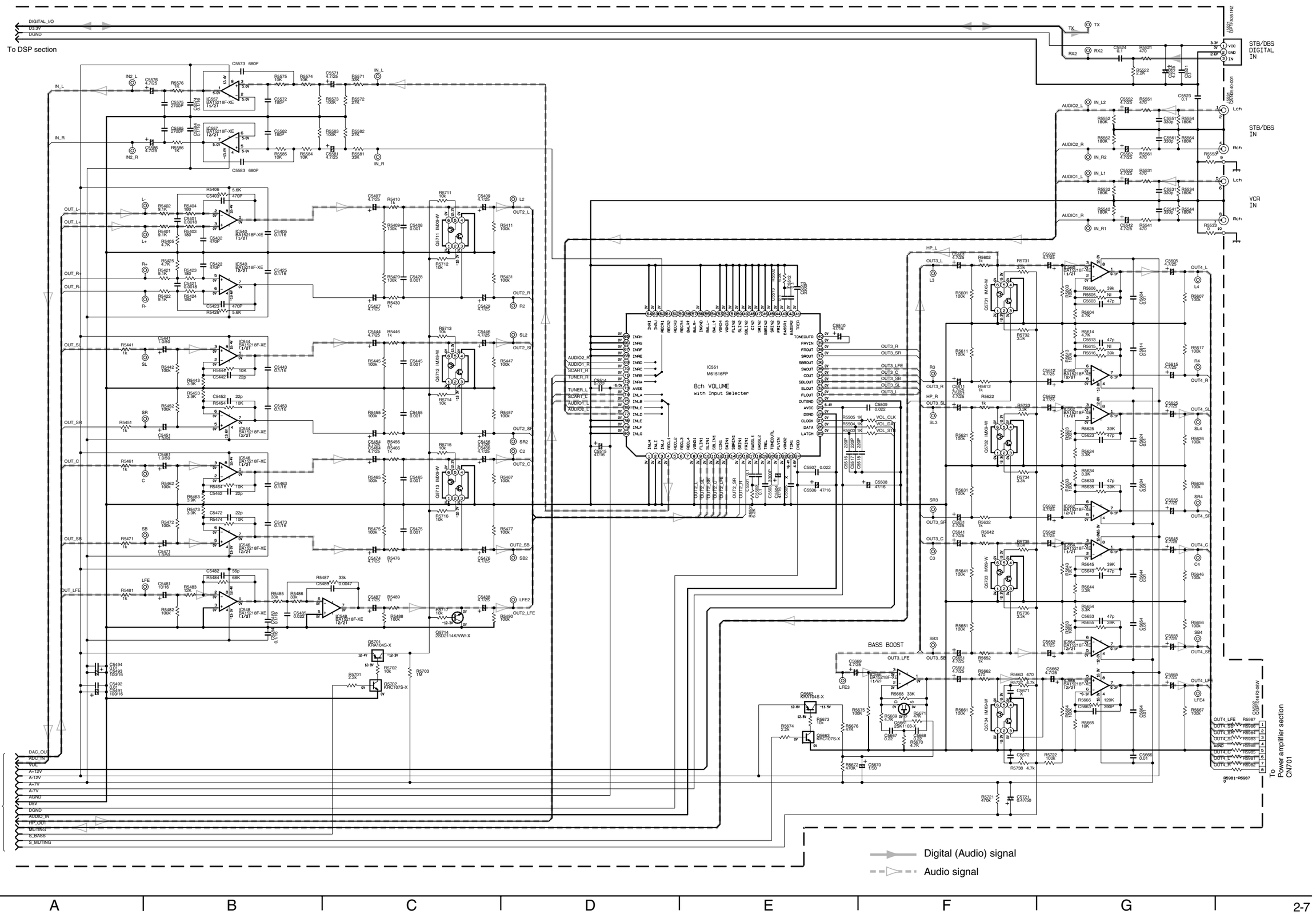
	R2171 R2172 R2173	R2181 R2182 R2183	C2131 B2131	C2151 B2151	R2132 R2142 R2152	B2301 B2311	Q2301 R2302 Q2311 R2301 C2302	Q2311 R2311 C2312 R2312 C2313	R2383	R2384
E	NO USE	USE	BUS CHIP	1/6.3	75	NO USE	USE	USE	0	NO USE
U	USE	NO USE	1/6.3	BUS CHIP	68	USE	NO USE	NO USE	NO USE	10K

Video (Composite) signal
Video (Component video Cb) signal
Cr Video (Component video Cr) signal
Y Video (Brightness) signal
C Video (Chrominance) signal

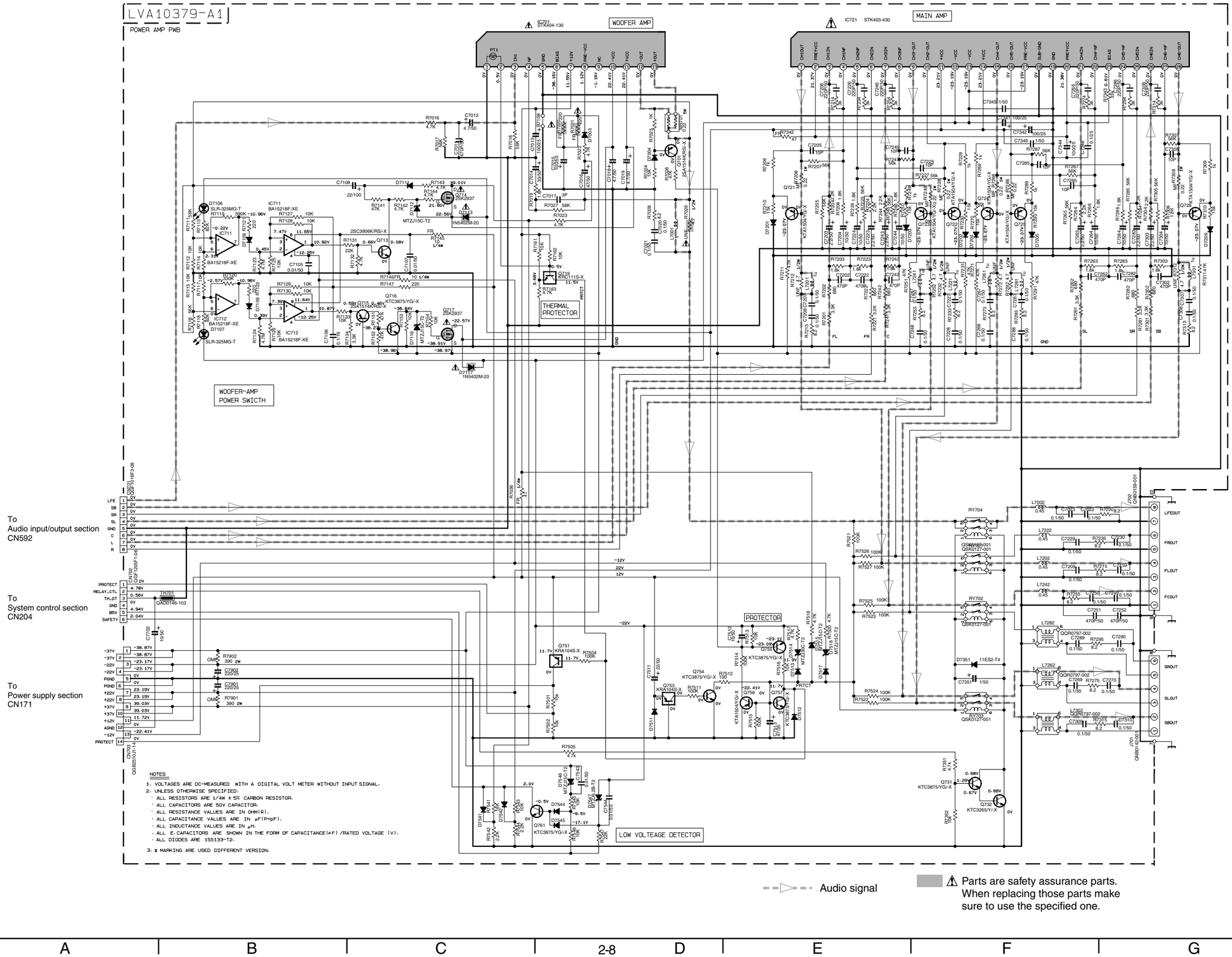
■ DSP section


LVA10377-A1
To Audio input/output section
DIGITAL_I/O
D3.3V
DGND
IC521
DSPC56367PV150
DSP
IC531
UPD784215AGC194
DSP MICOM
IC512
AK4382AVT-X
DAC
ICS11
AK4586VQ
CODEC
IC522
NC7SU04P5-X
IC524
39VF0207CWHQ01
F-ROM
IC525
IC526
IC527
S63LV102410K-X
RAM-1
RAM-2
RAM-3
IC532
NC7ST32P5-X
IC533
NC7S04P5-X
IC591
MM1561KF-X
IC592
MM1563DF-X
Q532
KRC107S-X
Q531
KRC107S-X
X521
NAX0308-001X
12.5MHz
X531
NAX0275-001X
6.14MHz
X501
NAX0322-001X
12.288MHz
D1.9V
R3.3V
D3.3V
To System control section CN203
Digital (Audio) signal
Audio signal

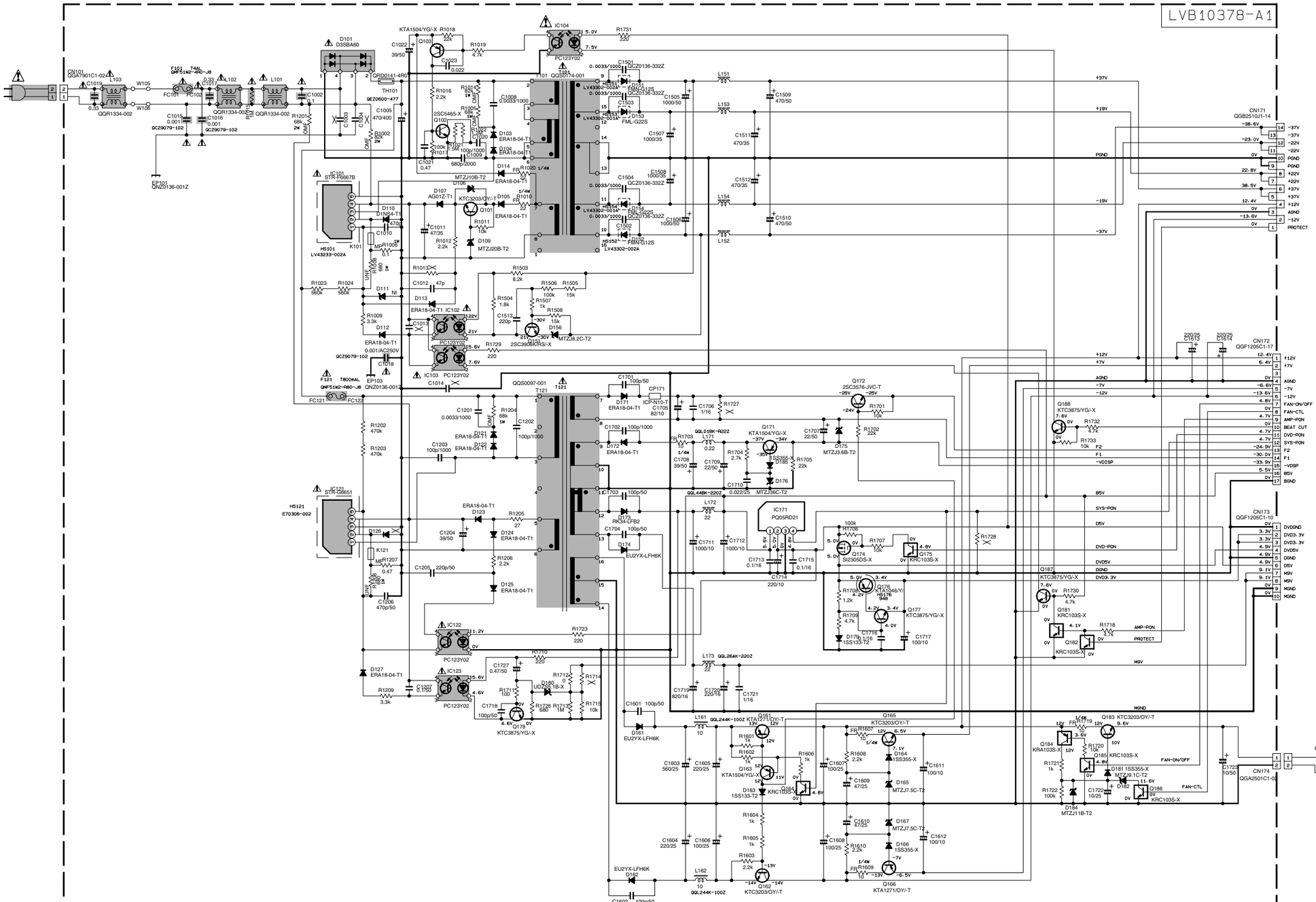
■ Audio input/output section



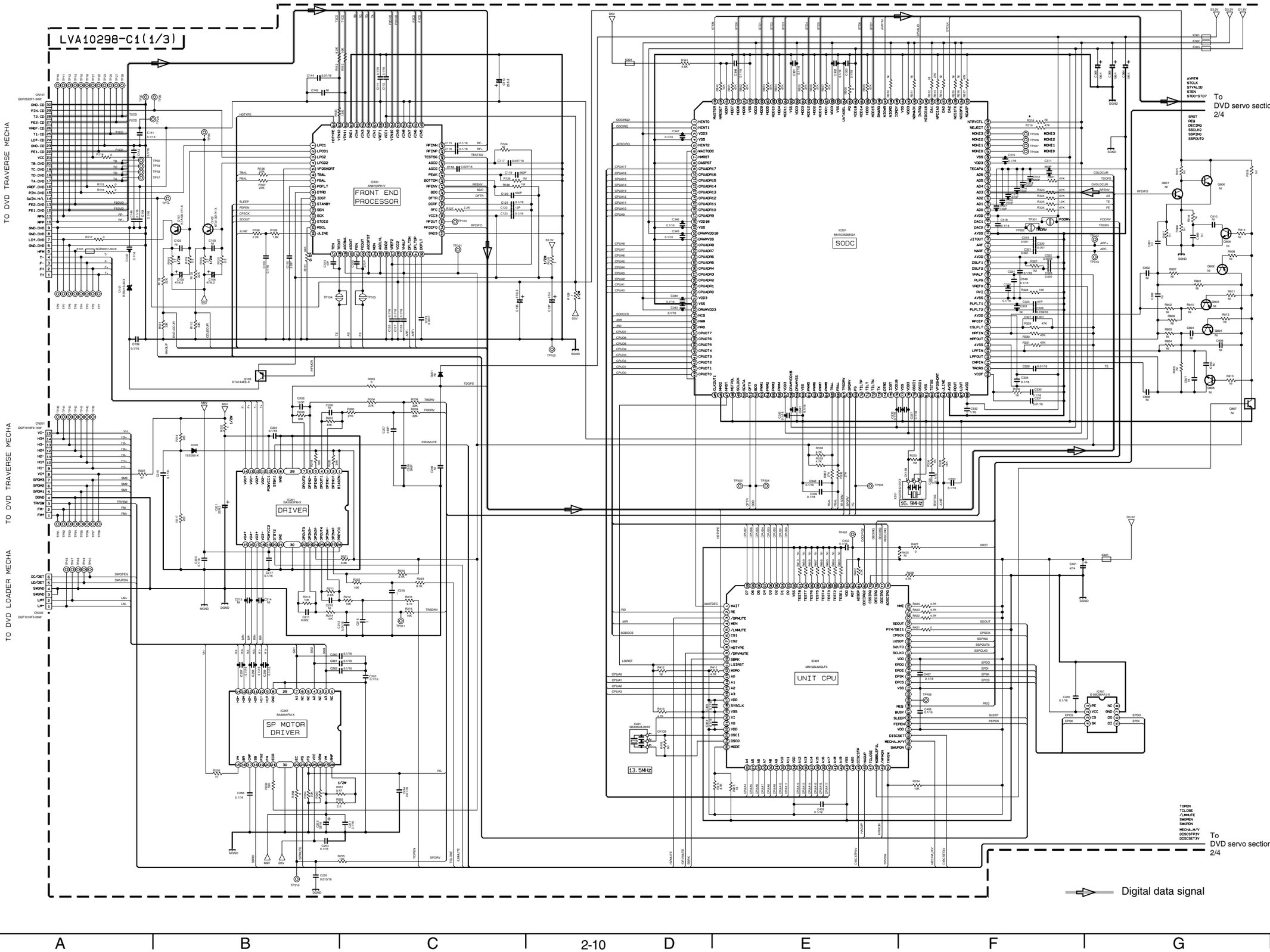
■ Power amplifier section



■ Power supply section



■ DVD servo section 1/4



■ DVD servo section 2/4

LVA10298-C1(2/3)

To DVD servo section 1/4

SRST
REQ
DECSRQ
SSCLKO
SSPSYNO
SSPOUTO

AVRTN
STCLK
STVALID
STEN
STD0~STD7

To DVD servo section 3/4

FLCS3V
RCK
DACOCS
DAC1CS
DAC2CS
XS
RGB
NTB
DACDENA
CPURST
SRST
FL1NT
BUSY
SMMUTE

PANTERA-2

To DVD servo section 3/4

PCS0
LHLD
LHLD4
LAO~LA3
ALE
RD~
AOK
SCLK
PWE0~PWE3
AD0~AD31

To DVD servo section 3/4

CrOUT
CbOUT
YOUT
COUT

Cb Y Cr C

To DVD servo section 3/4

192K
SMUTE
LMMUTE
S1OUT
SSPCLK1
SSPOUT1
SSPIN1
LRCLK
BCK
AOUT0~AOUT3
SPDIF

To DVD servo section 3/4

DISCSTP3V
DISCSET3V
MECHA_HV
TOPEN
TCLOSE
/LMMUTE
SWOPEN
SWUPEN

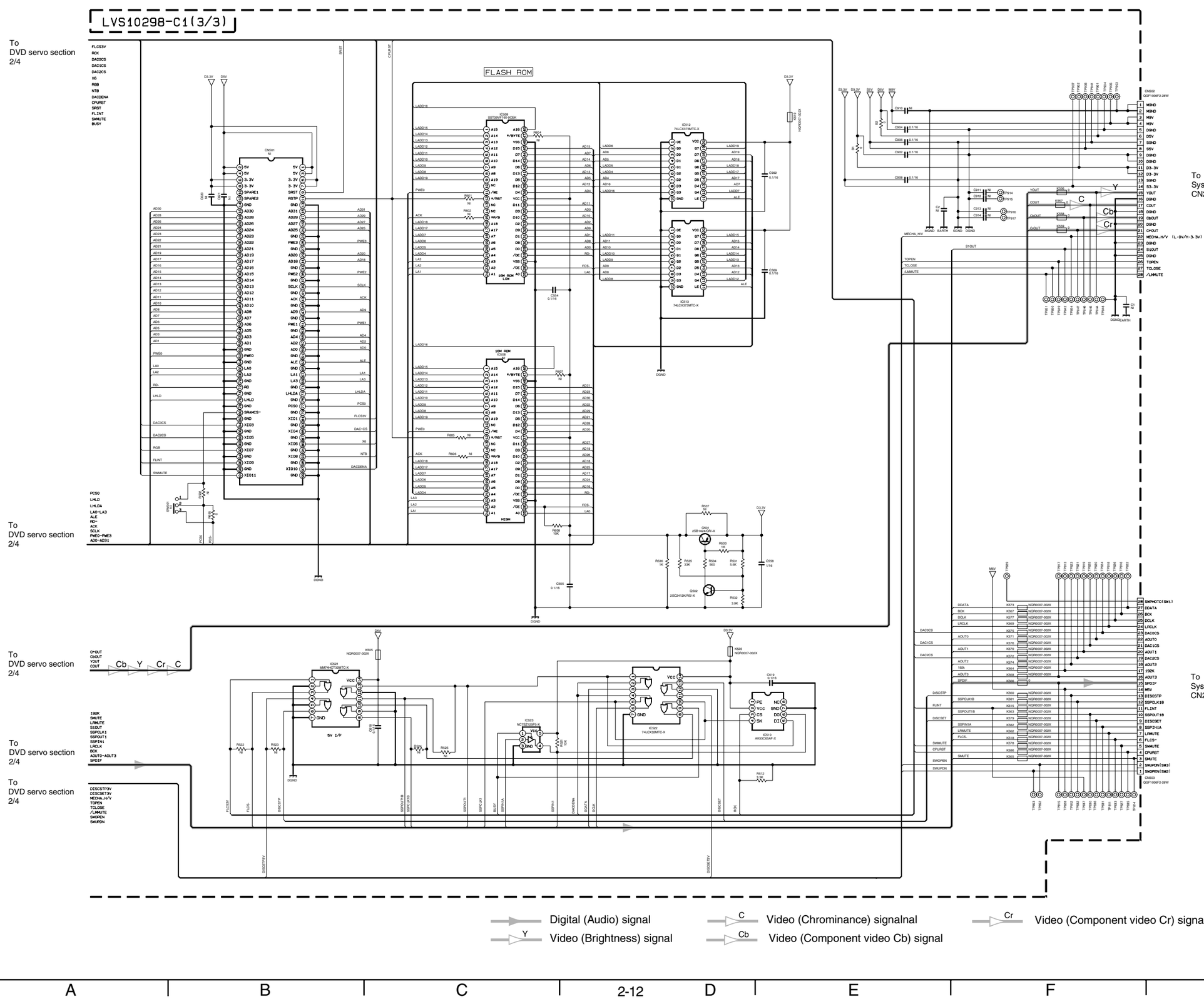
To DVD servo section 3/4

TOPEN
TCLOSE
/LMMUTE
SWOPEN
SWUPEN
MECHA_HV
DISCSTP3V
DISCSET3V

To DVD servo section 1/4

Digital data signal
Digital (Audio) signal
Y Video (Brightness) signal
C Video (Chrominance) signal
Cb Video (Component video Cb) signal
Cr Video (Component video Cr) signal

■ DVD servo section 3/4



■ DVD servo section 4/4 (Voltage value)

IC101

NO	DC(V)	NO	DC(V)
1	0V	51	2.1V
2	4.4V	52	2.1V
3	3.7V	53	2.1V
4	4.4V	54	2.1V
5	0V	55	4.9V
6	1.7V	56	2.1V
7	1.7V	57	2.1V
8	1.9V	58	2.1V
9	3.3V	59	2.1V
10	0V	60	2.1V
11	3.3V	61	0V
12	3.3V	62	2.1V
13	3.3V	63	2.1V
14	3.3V	64	0V
15	0V		
16	1.7V		
17	1.5V		
18	1.7V		
19	1.7V		
20	0V		
21	1.7V		
22	0V		
23	1.7V		
24	0.9V		
25	1.7V		
26	0V		
27	0V		
28	4.9V		
29	1.7V		
30	0V		
31	0V		
32	0V		
33	0V		
34	0V		
35	0.9V		
36	3.3V		
37	1.3V		
38	0.9V		
39	3.3V		
40	3.3V		
41	1.7V		
42	1.7V		
43	1.7V		
44	1.0V		
45	1.7V		
46	2.1V		
47	2.1V		
48	2.1V		
49	2.1V		
50	2.1V		

IC201

NO	DC(V)
1	1.7V
2	1.7V
3	1.7V
4	1.7V
5	1.7V
6	1.7V
7	1.7V
8	0V
9	3.2V
10	5.0V
11	2.5V
12	2.5V
13	2.5V
14	2.5V
15	4.3V
16	4.3V
17	4.3V
18	4.3V
19	9.2V
20	0V
21	0V
22	1.7V
23	1.7V
24	1.7V
25	0V
26	0V
27	1.7V
28	9.2V
29	1.7V
30	9.2V

IC251

NO	DC(V)
1	0.8V
2	0.8V
3	0.8V
4	0.8V
5	0V
6	0V
7	0.8V
8	0V
9	5.0V
10	5.0V
11	5.0V
12	5.0V
13	5.0V
14	5.0V
15	0V
16	0V
17	0V
18	0V
19	5.0V
20	5.0V
21	1.67V
22	1.67V
23	0V
24	3.3V
25	5.0V
26	0V
27	9.2V
28	9.2V
29	0V
30	0V

IC301

NO	DC(V)	NO	DC(V)	NO	DC(V)	NO	DC(V)
1	0V	51	3.3V	101	0.7V	151	0V
2	2.9V	52	3.3V	102	0V	152	1.7V
3	3.3V	53	——	103	1.4V	153	0V
4	0V	54	——	104	2.1V	154	1.7V
5	3.3V	55	——	105	——	155	0V
6	3.3V	56	——	106	1.7V	156	3.3V
7	——	57	3.3V	107	0.7V	157	0V
8	0V	58	1.7V	108	0.7V	158	0V
9	0V	59	0V	109	3.3V	159	0V
10	0V	60	0V	110	1.7V	160	0V
11	3.3V	61	——	111	1.7V	161	0V
12	3.3V	62	——	112	0V	162	3.3V
13	3.3V	63	——	113	0V	163	0V
14	0V	64	——	114	1.7V	164	0V
15	1.4V	65	1.7V	115	1.7V	165	0V
16	0.3V	66	1.7V	116	3.3V	166	0V
17	1.4V	67	1.7V	117	1.7V	167	0V
18	1.7V	68	1.7V	118	1.7V	168	0V
19	0V	69	3.3V	119	1.7V	169	3.3V
20	1.7V	70	——	120	1.7V	170	0V
21	0V	71	——	121	2.1V	171	0V
22	2.2V	72	——	122	1.7V	172	3.3V
23	2.2V	73	——	123	2.1V	173	0V
24	1.7V	74	——	124	——	174	4.9V
25	1.5V	75	——	125	3.3V	175	4.9V
26	1.5V	76	1.7V	126	0V	176	3.3V
27	1.5V	77	0V	127	0V		
28	1.5V	78	3.3V	128	0V		
29	1.5V	79	1.7V	129	0V		
30	0.5V	80	——	130	0V		
31	3.3V	81	0V	131	3.3V		
32	0V	82	0.8V	132	0V		
33	3.3V	83	2.1V	133	0V		
34	3.3V	84	1.7V	134	0V		
35	3.3V	85	0V	135	0V		
36	3.3V	86	——	136	1.7V		
37	0V	87	——	137	3.3V		
38	0V	88	3.3V	138	0V		
39	0V	89	0V	139	3.3V		
40	0V	90	1.7V	140	0V		
41	0V	91	——	141	0V		
42	0V	92	——	142	0V		
43	1.0V	93	1.7V	143	3.3V		
44	0V	94	0V	144	0V		
45	——	95	——	145	——		
46	0V	96	1.7V	146	1.7V		
47	3.3V	97	1.7V	147	3.3V		
48	0V	98	——	148	——		
49	——	99	3.3V	149	0V		
50	——	100	0.7V	150	0V		

IC401

NO	DC(V)	NO	DC(V)
1	3.3V	51	——
2	3.3V	52	0V
3	0V	53	3.3V
4	3.3V	54	3.3V
5	——	55	3.3V
6	3.3V	56	3.3V
7	——	57	——
8	0V	58	3.3V
9	3.3V	59	0V
10	0V	60	——
11	3.3V	61	0V
12	3.3V	62	0V
13	1.5V	63	0V
14	1.5V	64	0V
15	1.5V	65	0V
16	1.5V	66	3.3V
17	3.3V	67	3.3V
18	——	68	0V
19	0V	69	3.3V
20	0V	70	3.3V
21	——	71	0V
22	3.3V	72	3.3V
23	1.7V	73	3.3V
24	1.7V	74	3.3V
25	5.0V	75	3.3V
26	3.3V	76	3.3V
27	0V	77	0V
28	3.3V	78	0V
29	3.3V	79	0V
30	3.3V	80	0V
31	3.3V	81	3.3V
32	0V	82	3.3V
33	3.3V	83	3.3V
34	3.3V	84	3.3V
35	0V	85	3.3V
36	3.3V	86	3.3V
37	3.3V	87	3.3V
38	3.3V	88	3.3V
39	0V	89	3.3V
40	0V	90	3.3V
41	——	91	3.3V
42	——	92	0V
43	0V	93	0V
44	——	94	0V
45	3.3V	95	0V
46	0V	96	0V
47	0V	97	0V
48	3.3V	98	0V
49	3.3V	99	0V
50	3.3V	100	0V

IC451

NO	DC(V)
1	0V
2	3.2V
3	0V
4	0V
5	0V
6	0V
7	0V
8	0V

IC501

NO	DC(V)	NO	DC(V)	NO	DC(V)	NO	DC(V)	NO	DC(V)
1	3.2V	53	3.2V	105	0V	157	0V	209	0V
2	0.5V	54	0.4V	106	0V	158	0V	210	3.2V
3	0.4V	55	0.4V	107	3.2V	159	1.7V	211	0V
4	1.8V	56	0.4V	108	1.7V	160	1.7V	212	1.7V
5	0.4V	57	0V	109	0V	161	3.2V	213	3.2V
6	0V	58	0.4V	110	0V	162	0V	214	3.2V
7	0.4V	59	0.4V	111	1.0V	163	0V	215	0V
8	0.4V	60	0.4V	112	1.0V	164	0V	216	0V
9	0V	61	0.5V	113	3.1V	165	0V	217	3.2V
10	3.2V	62	3.2V	114	0.4V	166	0V	218	0V
11	0V	63	0.5V	115	0.4V	167	0V	219	3.2V
12	0V	64	3.2V	116	——	168	0V	220	3.2V
13	0V	65	1.0V	117	3.1V	169	3.2V	221	0V
14	0V	66	——	118	0.8V	170	3.2V	222	3.2V
15	2.0V	67	0V	119	1.3V	171	0V	223	3.2V
16	1.3V	68	1.7V	120	1.8V	172	0V	224	3.2V
17	0V	69	0V	121	0V	173	0V	225	0V
18	0.4V	70	3.2V	122	0V	174	0V	226	0V
19	3.2V	71	0V	123	0V	175	0V	227	0.8V
20	1.4V	72	0V	124	0V	176	0V	228	0V
21	1.7V	73	0V	125	3.2V	177	0V	229	0.8V
22	1.7V	74	0V	126	0V	178	0V	230	0V
23	0V	75	3.2V	127	0V	179	0V	231	0.8V
24	3.2V	76	——	128	0V	180	0V	232	0.6V
25	0.5V	77	1.7V	129	0V	181	3.2V	233	3.2V
26	2.5V	78	1.7V	130	0V	182	3.2V	234	0.6V
27	3.2V	79	1.7V	131	0V	183	0V	235	0.8V
28	1.2V	80	0V	132	0V	184	0V	236	1.0V
29	0V	81	0V	133	0V	185	3.2V	237	0V
30	0V	82	0V	134	0V	186	0V	238	0.4V
31	0V	83	3.2V	135	1.8V	187	0V	239	0.8V
32	2.0V	84	0.4V	136	0V	188	0V	240	0.8V
33	1.3V	85	0V	137	0V	189	3.2V		
34	1.7V	86	3.2V	138	0V	190	0V		
35	2.2V	87	0V	139	0V	191	0V		
36	3.1V	88	1.7V	140	3.2V	192	1.7V		
37	3.2V	89	0V	141	0V	193	3.2V		
38	0V	90	0V	142	0V	194	3.2V		
39	3.2V	91	1.2V	143	0V	195	0V		
40	0V	92	0V	144	0V	196	3.2V		
41	0V	93	0V	145	3.2V	197	3.2V		
42	0V	94	0.6V	146	0V	198	3.2V		
43	0.7V	95	0V	147	0V	199	3.2V		
44	3.2V	96	0V	148	0V	200	3.2V		
45	0.7V	97	0V	149	0V	201	0V		
46	0.5V	98	1.7V	150	0V	202	3.2V		
47	0V	99	——	151	0V	203	3.2V		
48	0.5V	100	——	152	0V	204	0V		
49	0V	101	1.7V	153	0V	205	4.9V		
50	0.4V	102	3.2V	154	3.2V	206	3.2V		
51	0.4V	103	0V	155	0V	207	0V		
52	0.4V	104	0V	156	3.2V	208	3.2V		

IC502

NO	DC(V)
1	1.5V
2	3.3V
3	1.7V
4	0V
5	1.7V
6	1.7V
7	1.7V
8	1.7V

IC505

NO	DC(V)	NO	DC(V)
1	3.2V	51	0.5V
2	0.8V	52	0V
3	3.2V	53	0.5V
4	0.8V	54	0.7V
5	0.8V	55	3.2V
6	0V	56	0.7V
7	0.6V	57	0.6V
8	0.6V	58	0V
9	3.2V	59	0V
10	0.8V	60	1.7V
11	1.0V	61	1.4V
12	0V	62	0.4V
13	0.4V	63	1.3V
14	——	64	1.3V
15	3.2V	65	2.0V
16	0V	66	0V
17	3.2V	67	3.2V
18	0V	68	1.7V
19	3.2V	69	——
20	2.2V	70	——
21	——	71	0V
22	2.0V	72	0V
23	1.3V	73	——
24	0V	74	0V
25	1.2V	75	3.2V
26	2.5V	76	0.4V
27	0.5V	77	0.4V
28	1.0V	78	0V
29	3.2V	79	0V
30	——	80	0.4V
31	0.4V	81	3.2V
32	0V	82	0.5V
33	0.4V	83	0.8V
34	0.4V	84	0V
35	3.2V	85	0.8V
36	0.4V	86	0V
37	0.4V	87	
38	0V	88	
39	0.5V	89	
40	0.5V	90	
41	3.2V	91	
42	3.2V	92	
43	3.2V	93	
44	0V	94	
45	0.4V	95	
46	0V	96	
47	0.4V	97	
48	0.4V	98	
49	3.2V	99	
50	0.4V	100	

IC509

NO	DC(V)
1	0V
2	0V
3	0V
4	0V
5	0V
6	0V
7	0V
8	0V
9	0V
10	——
11	3.2V
12	0V
13	——
14	——
15	0V
16	0V
17	0V
18	0V
19	0V
20	0V
21	0V
22	0V
23	0V
24	3.2V
25	0V
26	3.2V
27	0V
28	3.2V
29	0V
30	0V
31	0V
32	0V
33	0V
34	0V
35	0V
36	0V
37	3.2V
38	0V
39	0V
40	0V
41	0V
42	0V
43	0V
44	0V
45	0V
46	0V
47	0V
48	0V

IC510

NO	DC(V)
1	0V
2	3.2V
3	0V
4	3.2V
5	3.2V
6	3.2V
7	0V
8	0V

IC511

NO	DC(V)
1	0V
2	1.8V
3	3.2V

IC512

NO	DC(V)
1	0V
2	0V
3	0V
4	0V
5	0V
6	0V
7	0V
8	0V
9	0V
10	0V
11	0V
12	0V
13	0V
14	0V
15	0V
16	0V
17	0V
18	0V
19	0V
20	3.2V

IC513

NO	DC(V)
1	0V
2	0V
3	0V
4	0V
5	0V
6	0V
7	0V
8	0V
9	0V
10	0V
11	0V
12	0V
13	0V
14	0V
15	0V
16	0V
17	0V
18	0V
19	0V
20	3.2V

IC521

NO	DC(V)
1	3.2V
2	0V
3	5.0V
4	3.2V
5	0V
6	5.0V
7	0V
8	5.0V
9	0V
10	3.2V
11	5.0V
12	0V
13	3.2V
14	5.0V

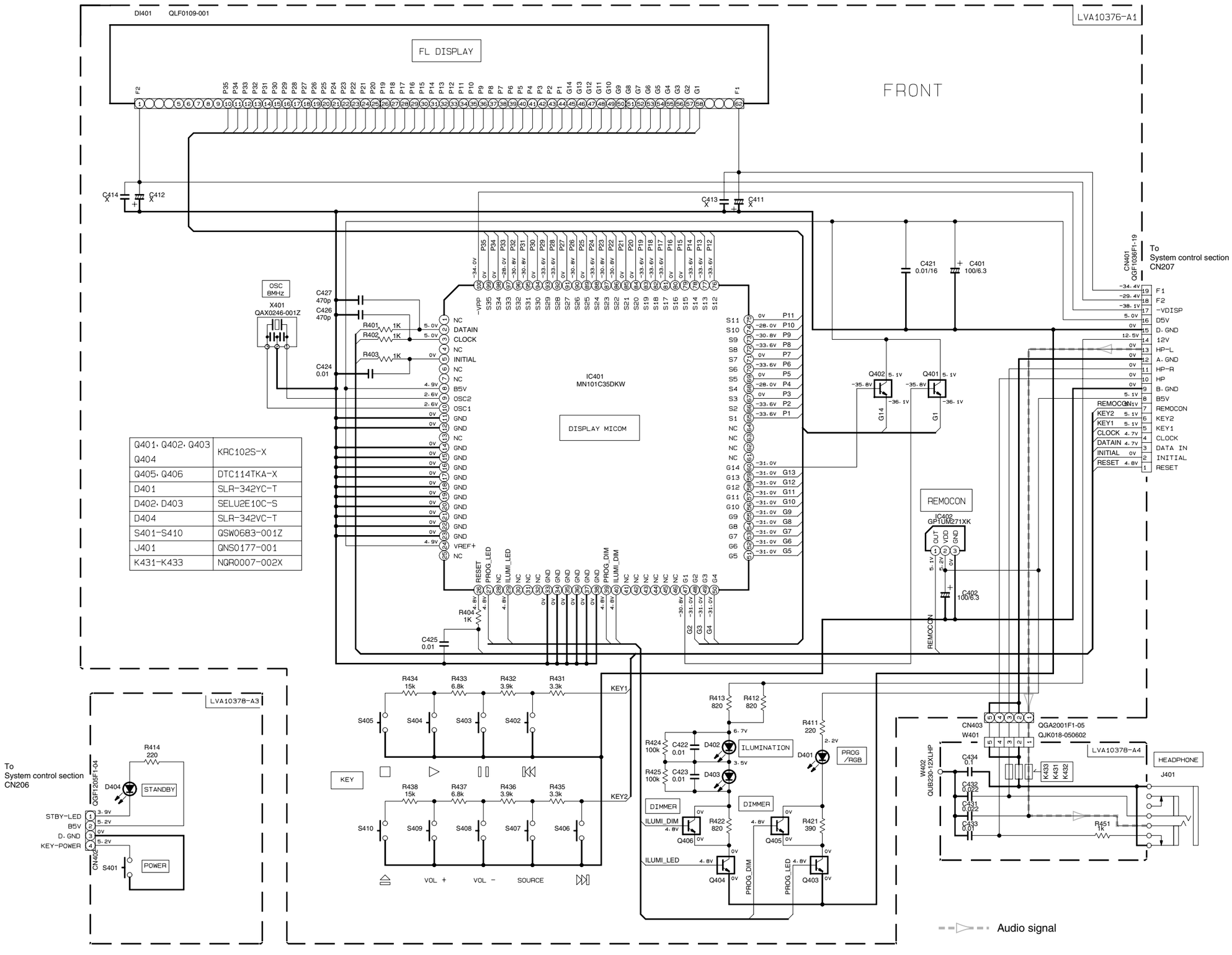
IC522

NO	DC(V)
1	3.2V
2	3.2V
3	3.2V
4	3.2V
5	3.2V
6	3.2V
7	0V
8	0V
9	3.2V
10	3.2V
11	3.2V
12	0V
13	5.0V
14	3.2V

NOTES

1. VOLTAGES ARE DC-MEASURED WITH A DIGITAL VOLT METER WITHOUT INPUT SIGNAL.
CONDITION --- POWER ON DVD STOP

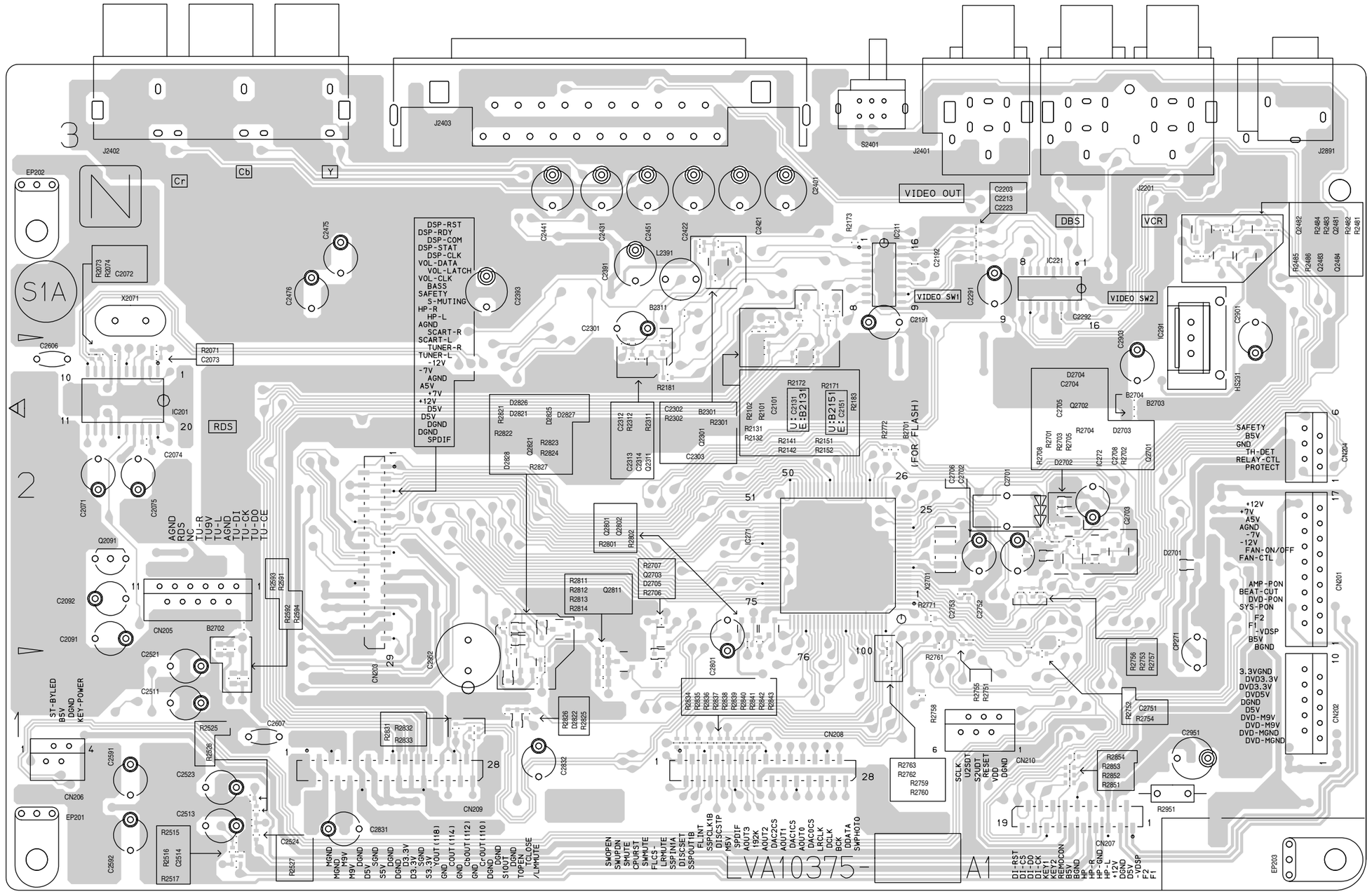
■ FL display section



Printed circuit boards

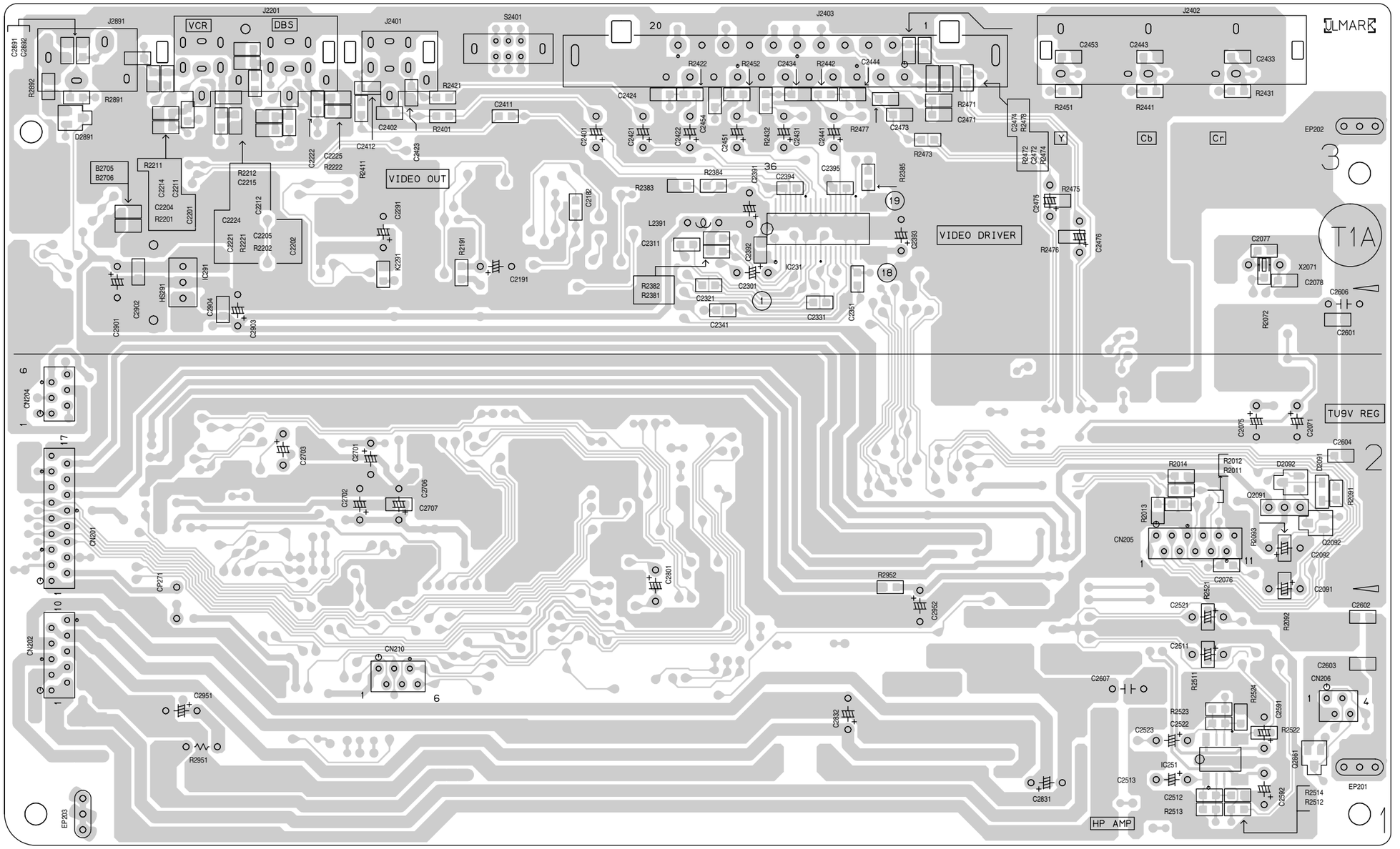
■ Main board

Forward side



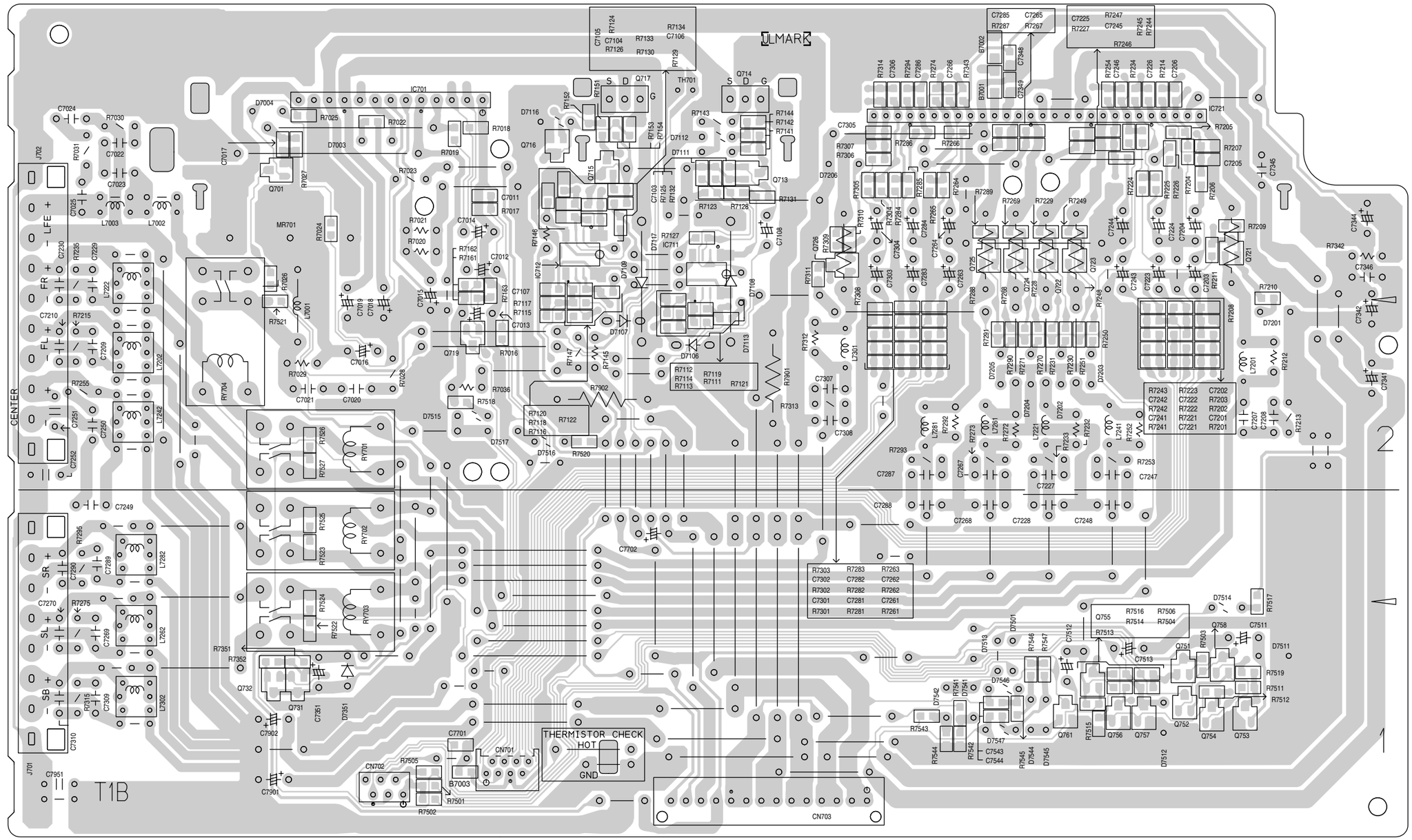
■ Main board

Reverse side



■ Amplifier board

Reverse side



■ Power board

Reverse side

(Suport board 1)

(Jack board)

(Connection board)

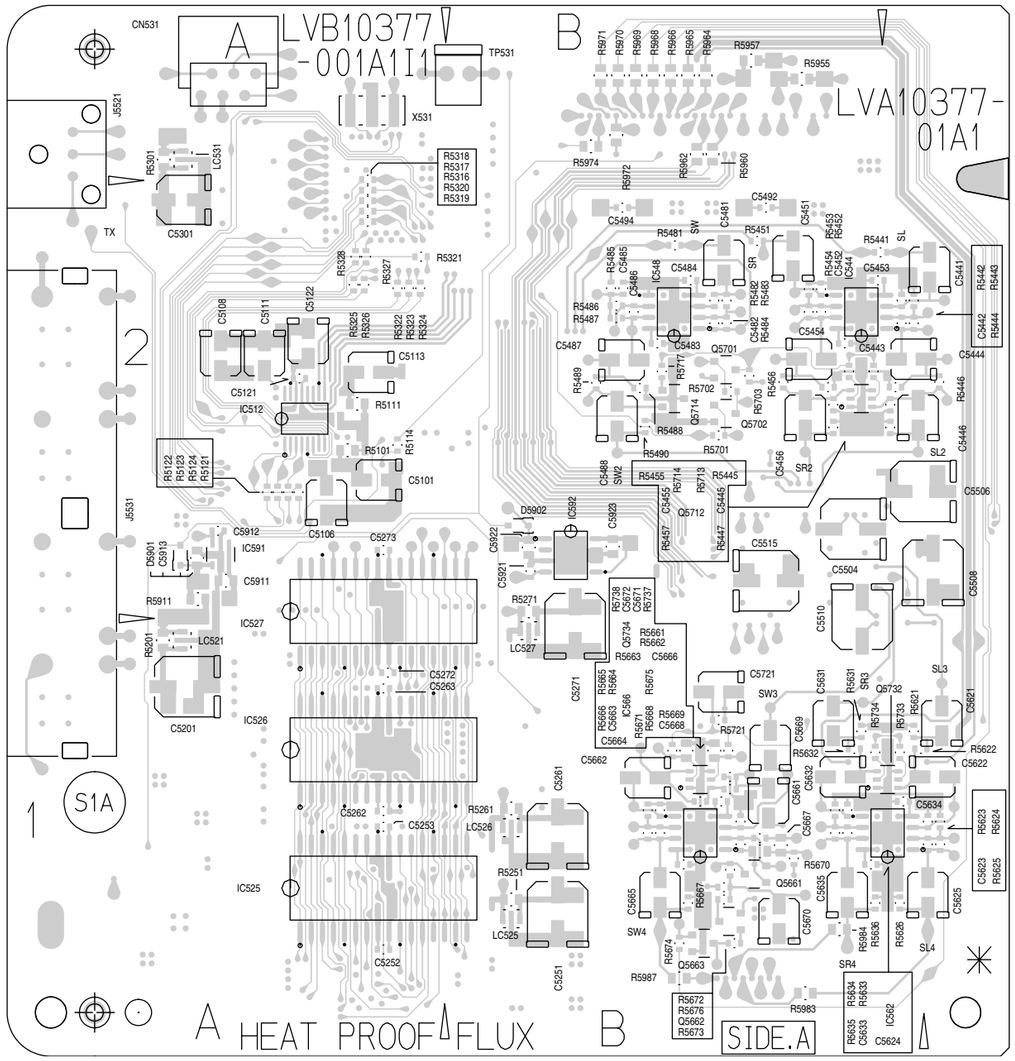
(Standby board)

(Suport board 2)

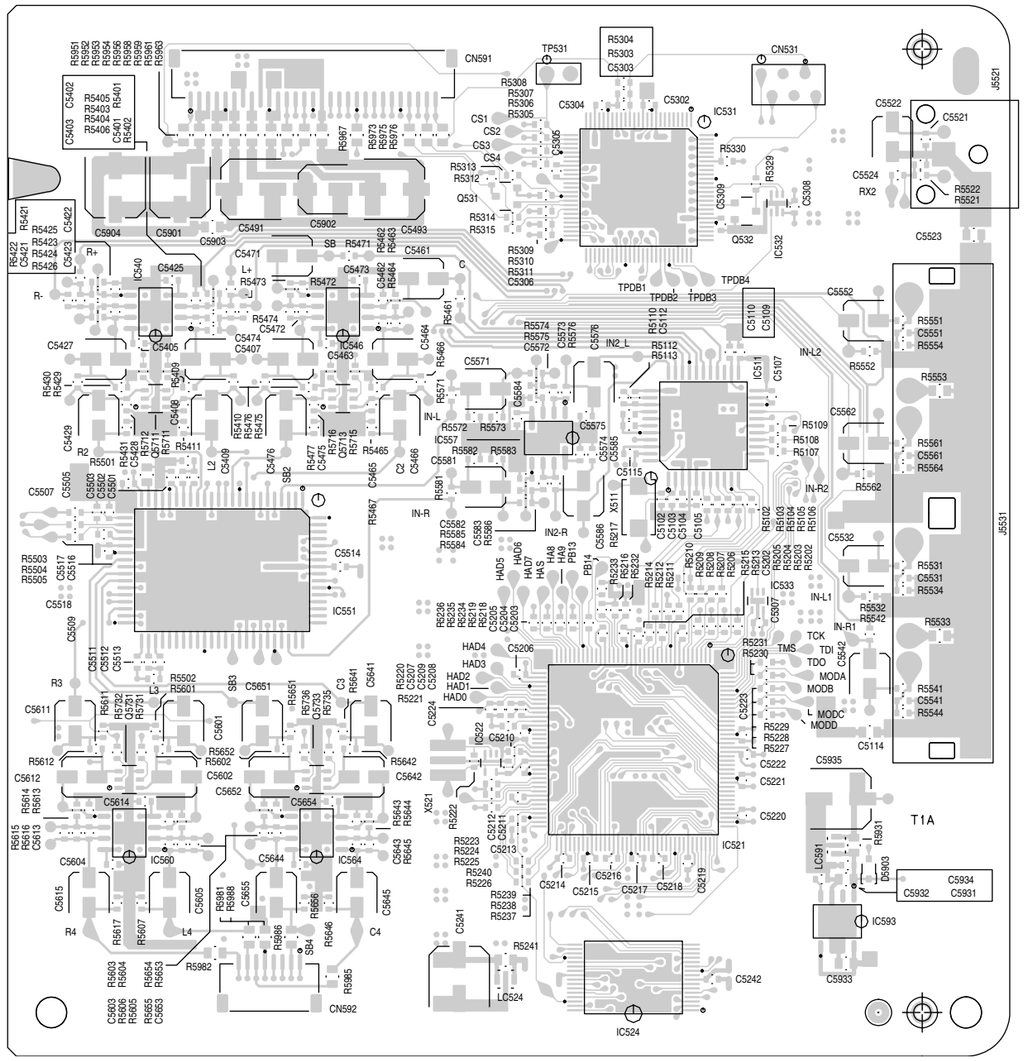
(Power board)

■ DSP board

Forward side

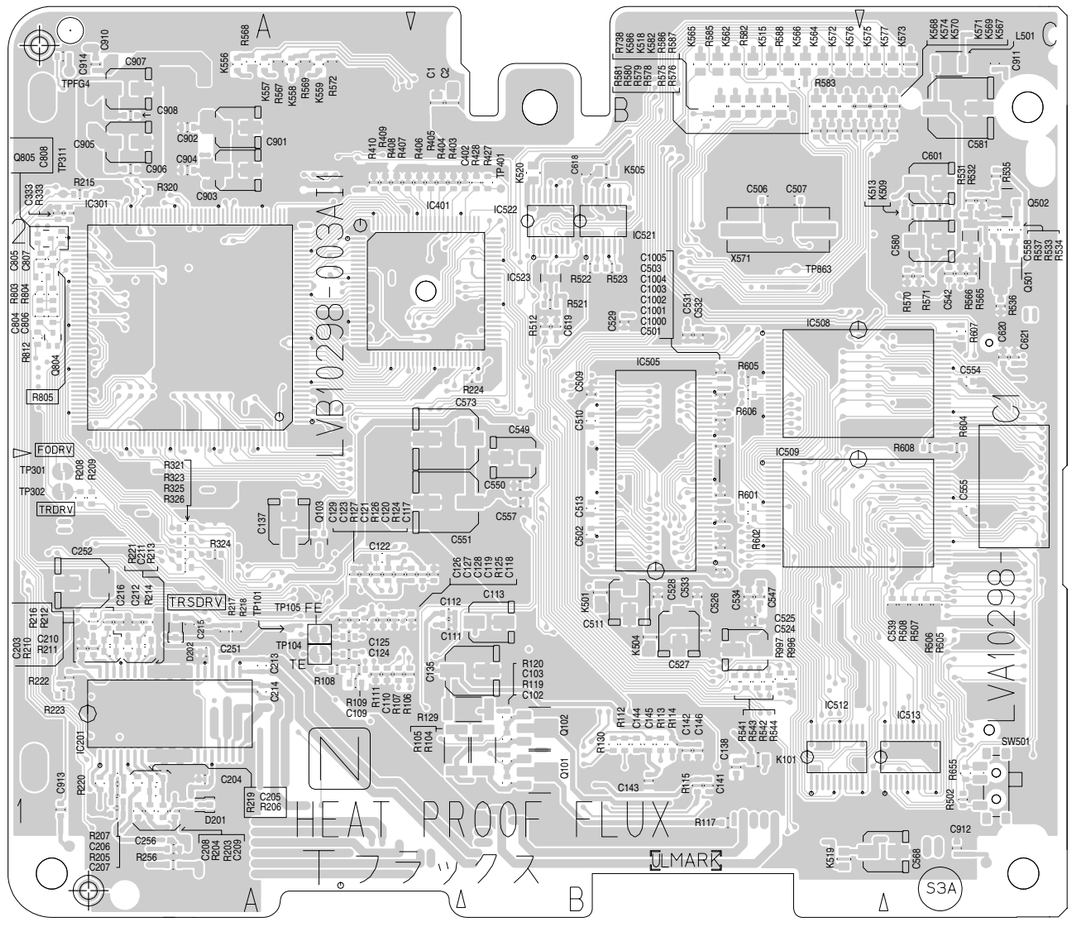


Reverse side

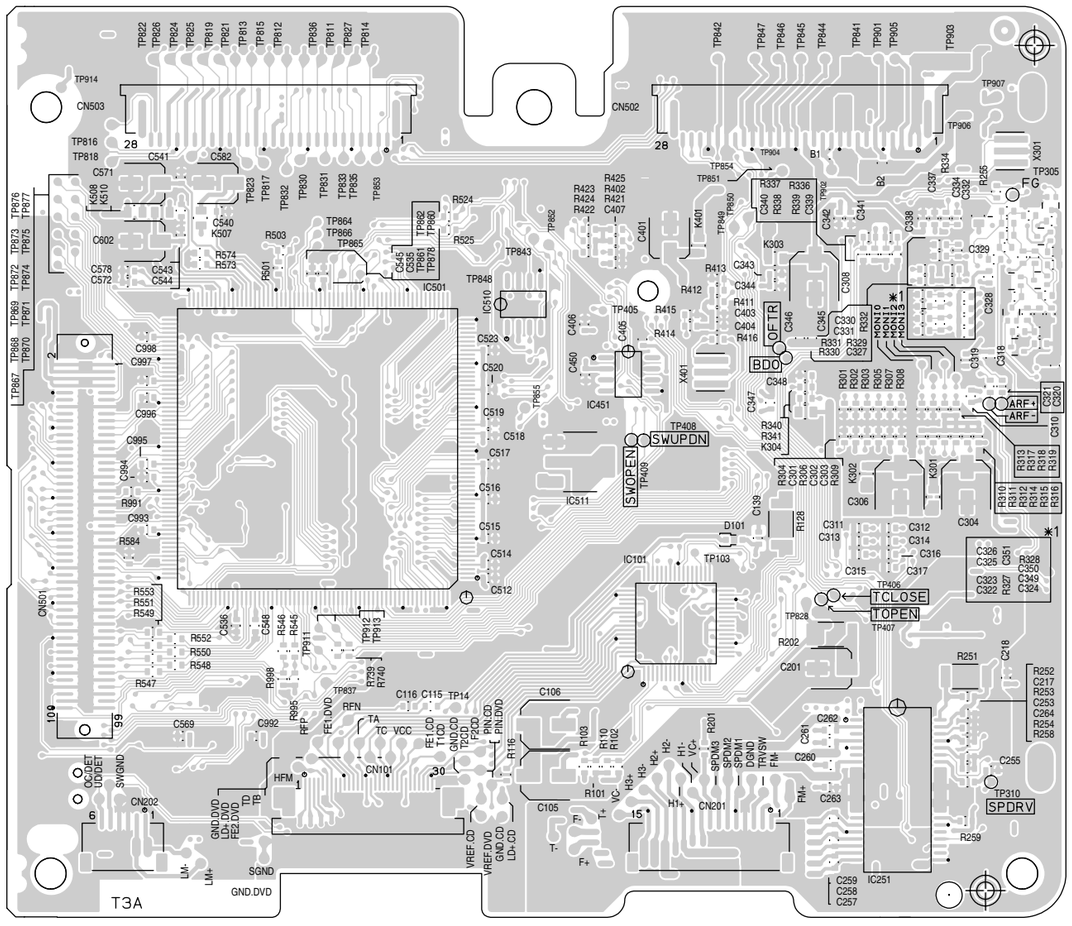


■ DVD servo board

Forward side

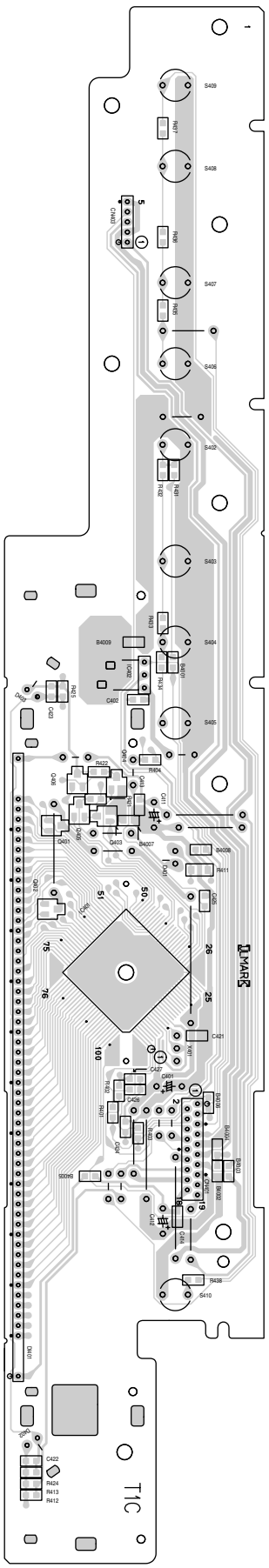


Reverse side



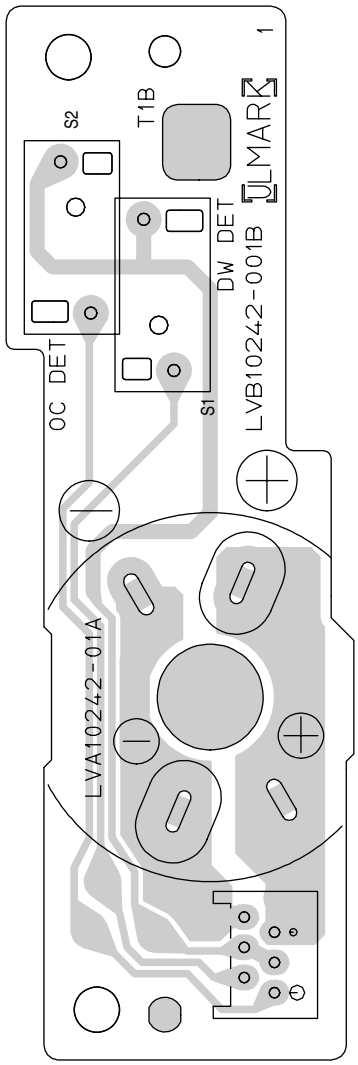
■ Switch board

Reverse side



■ Spindle motor board

Reverse side



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