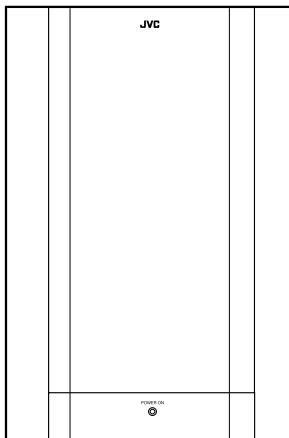# JVC

SERVICE MANUAL

DVD DIGITAL THEATER SYSTEM

TH-A9
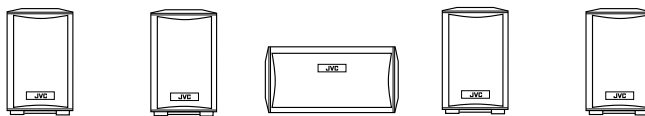
SP-XSA9   **SP-XCA9**   **SP-XSA9**

SP-PWA9   **XV-THA9**

Contents

Safety Precautions

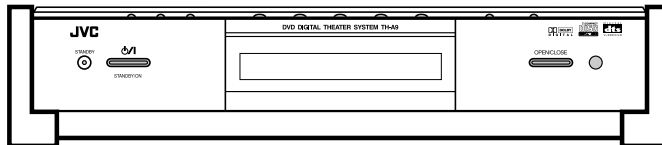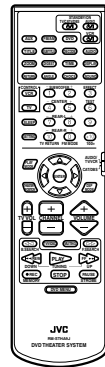1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.

2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer`s warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.

3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.

4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.

5. Leakage currnet check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.

   ● Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet , particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.)

   ● Alternate check method
   Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
   Measure the AC voltage across the resistor with the AC voltmeter.
   Move the resistor connection to eachexposed metal part, particularly any exposed metal part having a return path to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).

AC VOLTMETER
(Having 1000
ohms/volts,
or more sensitivity)

0.15μF AC TYPE

1500Ω 10W

Place this
probe on
each exposed
metal part.

Good earth ground
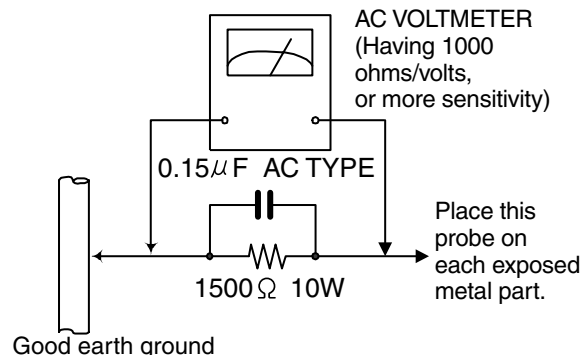
Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ *CAUTION* **Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.**

Important for Laser Products

1.CLASS IIa LASER PRODUCT

2.DANGER : Invisible laser radiation when open and inter lock failed or defeated. Avoid direct exposure to beam.

3.CAUTION : There are no serviceable parts inside the Laser Unit. Do not disassemble the Laser Unit. Replace the complete Laser Unit if it malfunctions.

4.CAUTION : The compact disc player uses invisible laserradiation and is equipped with safety switches whichprevent emission of radiation when the drawer is open and the safety interlocks have failed or are de feated. It is dangerous to defeat the safety switches.

5.CAUTION : If safety switches malfunction, the laser is able to function.

6.CAUTION : Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

⚠ *CAUTION* **Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.**

Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

## 1.1. Grounding to prevent damage by static electricity
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

1.1.1. Ground the workbench
1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

1.1.2. Ground yourself
1. Use an anti-static wrist strap to release any static electricity built up in your body.

(caption)
Anti-static wrist strap

1MΩ

Conductive material
(conductive sheet) or iron plate
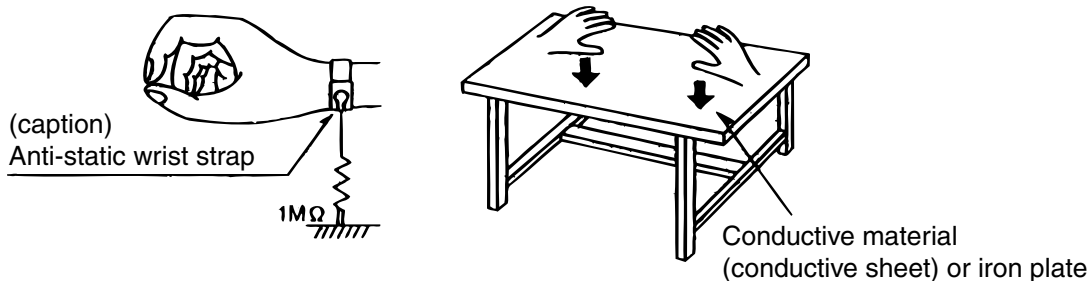
1.1.3. Handling the optical pickup
1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)

2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

1.2. Handling the traverse unit (optical pickup)
1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.

2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.

3. Handle the flexible cable carefully as it may break when subjected to strong force.

4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Dismantling and assembling the traverse unit

1. Notice regarding replacement of optical pickup

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs to the optical pickup or connected devices.

(Refer to the section regarding anti-static measures.)

1. Do not touch the area around the laser diode and actuator.

2. Do not check the laser diode using a tester, as the diode may easily be destroyed.

3. It is recommended that you use a grounded soldering iron when shorting or removing the laser diode.
   Recommended soldering iron: HAKKO ESD-compatible product

4. Solder the land on the optical pickup's flexible cable.
   ・Note : Short the land after shorting the terminal on the flexible cable using a clip, etc., when using an ungrounded soldering iron.
   ・Note : After shorting the laser diode according to the procedure above, remove the solder according to the text explanation.

Shorting

Shorting
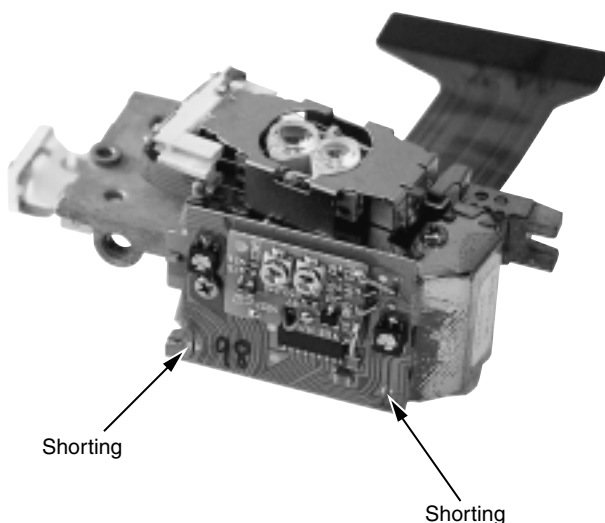
■ Importance Admistering point on the Safety (XV-THA9)
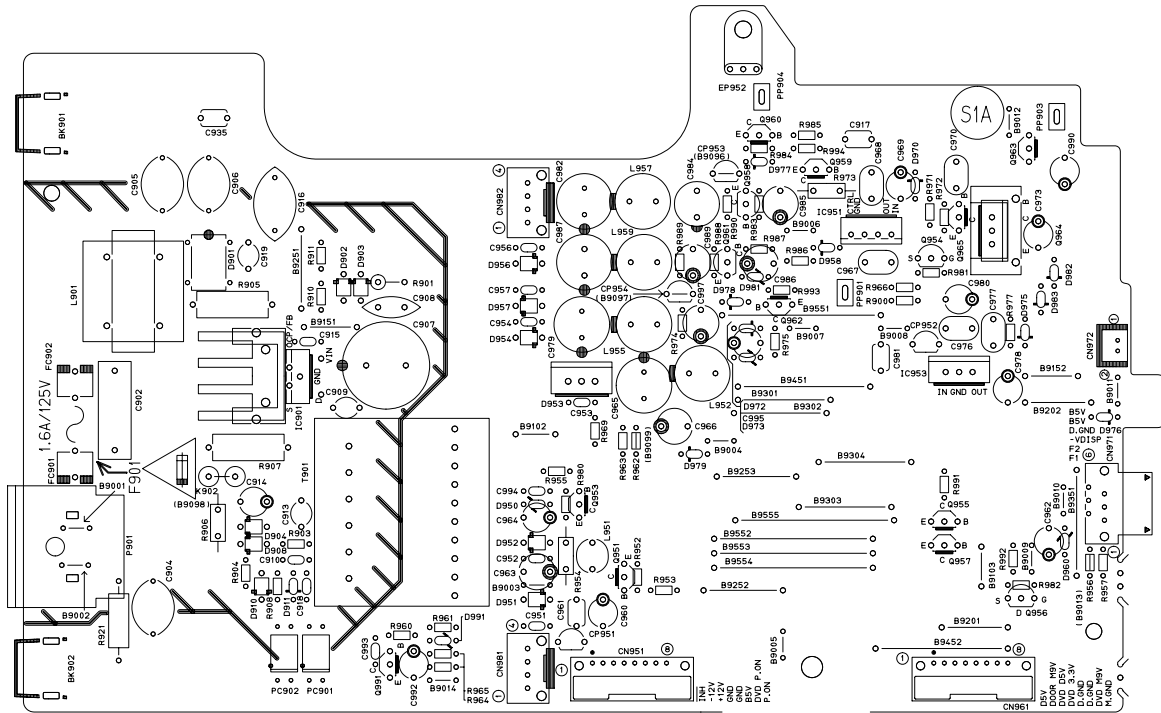
Note : It's means "J" for U.S.A. market model and "C" for canada market model.

| XV-THA9 C/J ONLY	XV-THA9 C/J SEULEMENT
Full Fuse Replacement Marking	**Marquage Pour Le Remplacement Complet De Fusible**
Graphic symbol mark (This symbol means fast blow type fuse.)	Le symbole graphique (Ce symbole signifie fusible de type á fusion rapide.)
should be read as follows ;	doit être interprété comme suit ;
FUSE CAUTION	**PRECAUTIONS SUR LES FUSIBLES**
FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE AND RATING OF FUSES ;	POUR UNE PROTECTION CONTINUE CONTRE DES RISQUES D'INCENDIE, REMPLACER SEULEMENT PAR UN FUSIBLE DU MEME TYPE ;
F901 : 1.6 A / 125 V	**F901 : 1.6 A / 125 V**

■ Importance Admistering point on the Safety (SP-PWA9)
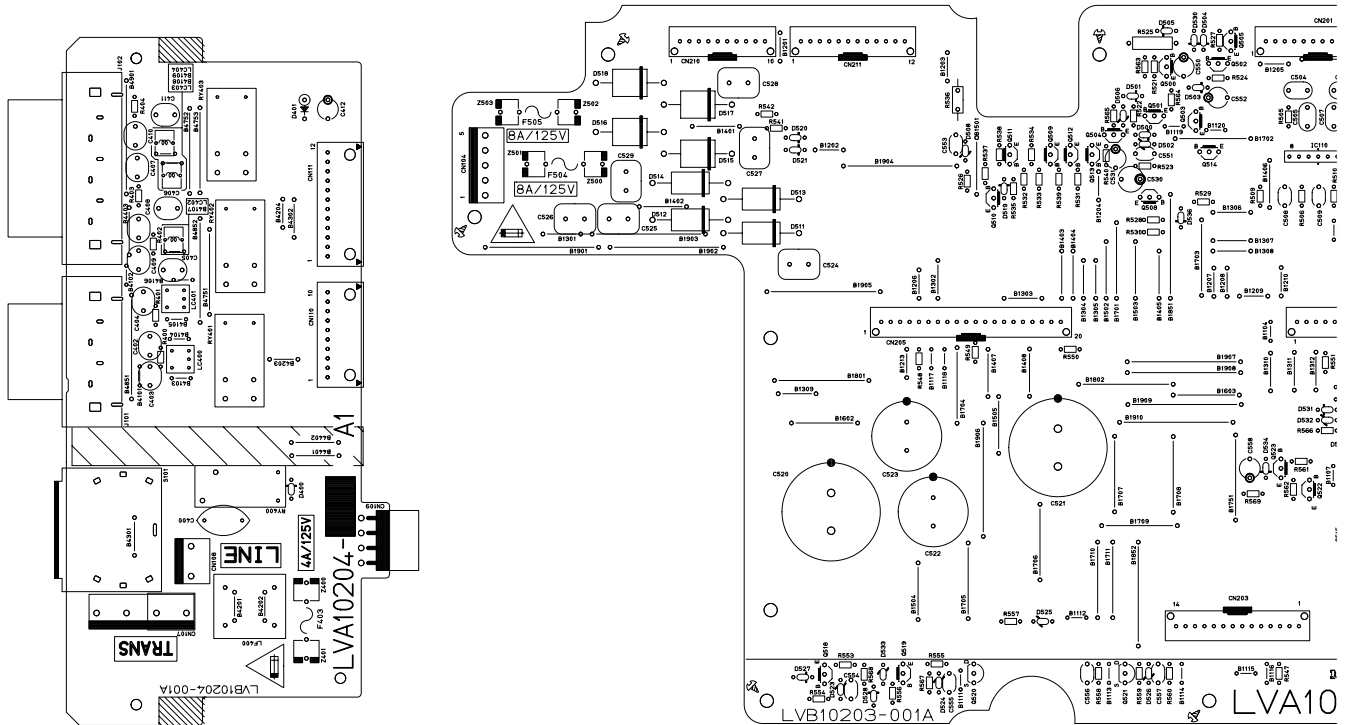
Note : It's means "J" for U.S.A. market model and "C" for canada market model.

SP-PWA9 C/J ONLY	SP-PWA9 C/J SEULEMENT
Full Fuse Replacement Marking	**Marquage Pour Le Remplacement Complet De Fusible**
Graphic symbol mark (This symbol means fast blow type fuse.)	Le symbole graphique (Ce symbole signifie fusible de type á fusion rapide.)
should be read as follows ;	doit être interprété comme suit ;
FUSE CAUTION	**PRECAUTIONS SUR LES FUSIBLES**
FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE AND RATING OF FUSES ; F401 : 4A / 125 V F504 : 8A / 125 V F505 : 8A / 125 V	POUR UNE PROTECTION CONTINUE CONTRE DES RISQUES D'INCENDIE, REMPLACER SEULEMENT PAR UN FUSIBLE DU MEME TYPE ; F401 : 4A / 125 V F504 : 8A / 125 V F505 : 8A / 125 V

Disassembly method

<Main unit>

■Removing the DVD door (See Fig.1)

1. Remove the four screws A that retain the DVD door from the top of the unit.
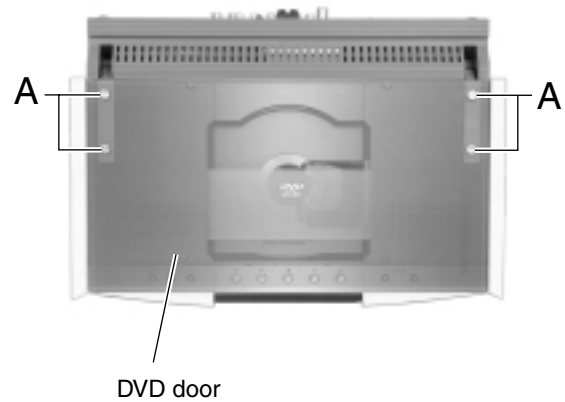
DVD door

Fig.1

■Removing the right and left side covers (See Fig.2)

· Prior to performing the following procedure, remove the DVD door.

1. Remove the four screws (B) that attach the left and right side covers of the unit, from the bottom panel.

2. Remove the left and right side covers by moving each of them in the direction of the corresponding arrow.

Right side cover

B

B

Bottom panel

Left side cover

Fig.2

■Removing the front panel assembly and the DVD mechanism base

(See Figs.3 to 7)

・ Prior to performing the following procedure, remove the left and right side covers.
・ Also remove the DVD door.

(Note) Remove the front panel assembly and the DVD mechanism together, just as they were assembled.

・ The mechanism slide switch for pickup protection should be set to the SHORTED position.

1. Remove the three screws (C) that retain the front panel assembly, from the bottom panel of the unit.

2. Remove four screws (D) that retain the DVD mechanism base, from the top of the unit.

3. Remove the three screws (E) from the rear panel of the unit that retain the DVD mechanism base.

4. Remove the DVD mechanism together with the front panel assembly by lifting them upward from the main unit and moving them toward the front.

5. Disconnect the card wire of the DVD mechanism from the connector CN101 on the DVD servo board.

Disconnect the wire of the LED board from the connector CN812 on the analog input/output board.

Fig.3

Fig.4
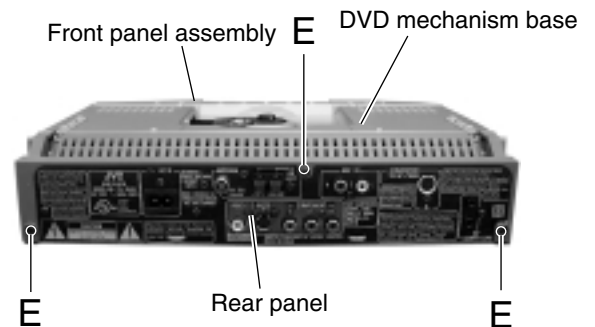
Fig.5
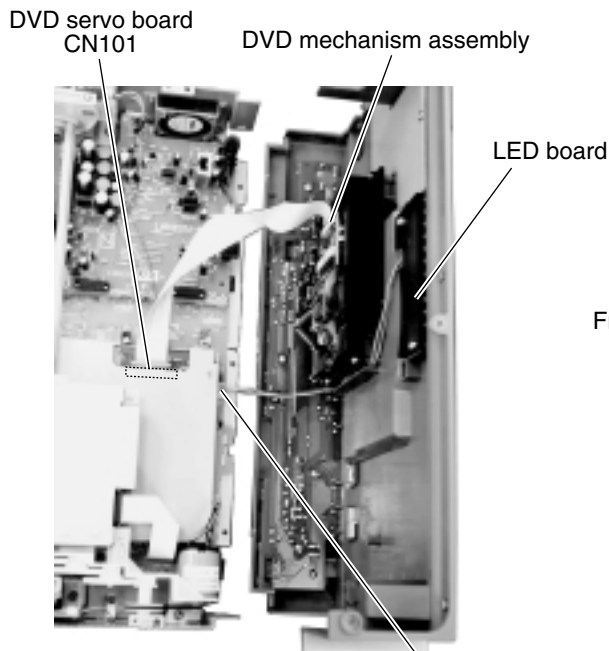
Fig.7
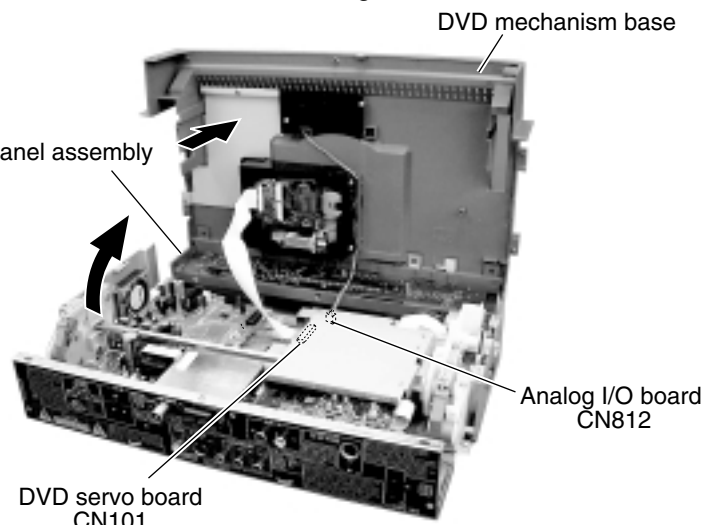
Fig.6

■Separating the front panel assembly and the DVD mechanism base (See Fig.8)

・Prior to performing the following procedure, remove the left and right side covers.
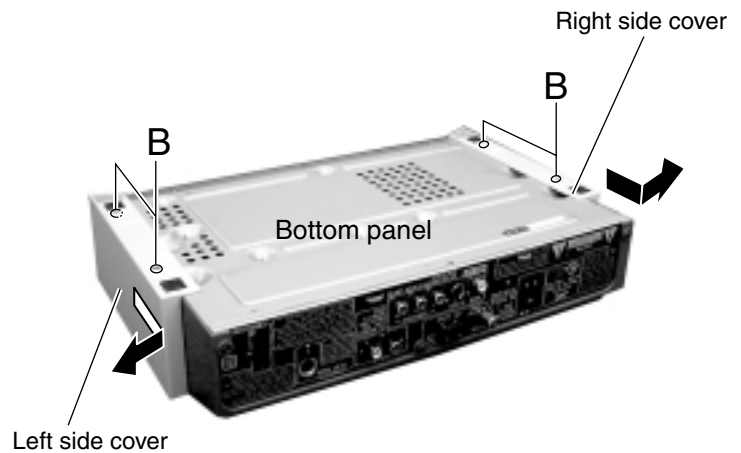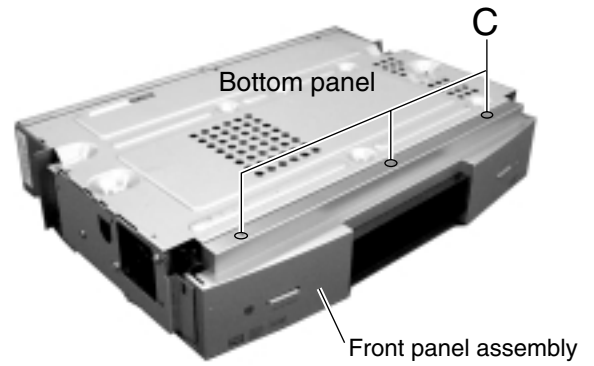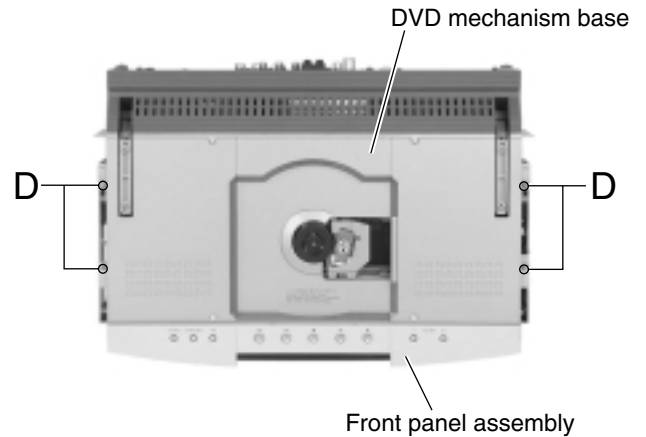・Also remove the DVD door.

1. Remove the front panel assembly and the DVD mechanism base together from the main unit. (See Figs. 3 to 7.)

2. On the back of the DVD mechanism base, disengage the four claws at the engaging points (a) that attach the front panel assembly to the DVD mechanism base, and then pull out the front panel assembly in the direction of the arrow to separate it from the DVD mechanism base.

(Note) It is at this stage that the front panel assembly and the DVD mechanism base are separated from each other.
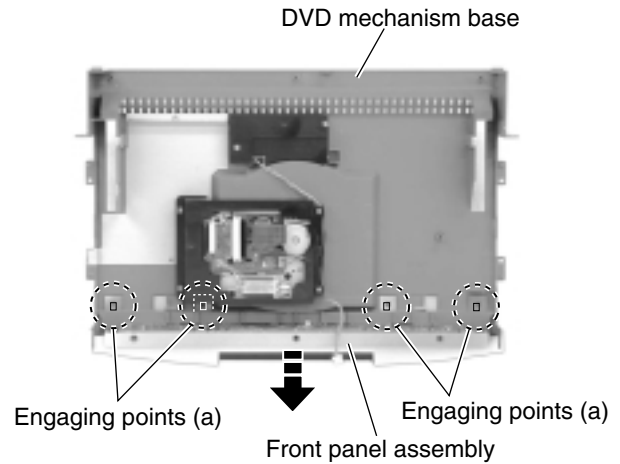
■Removing the display board (See Fig.9)

・Prior to performing the following procedure, remove the left and right side covers.
・Also remove the DVD door.
・Also separate the front panel assembly from the DVD mechanism base.

1. Remove the five screws (F) that retain the display board.

■Removing the DVD mechanism assembly (See Figs.10 and 11)

・Prior to performing the following procedure, remove the left and right side covers.
・Also remove the DVD door.

(Note) This work is possible even when the front panel assembly is attached to the DVD mechanism base.

1. Remove the four screws (G) from the back of the DVD mechanism base that retain the DVD mechanism cover.

2. Remove the DVD mechanism assembly from the DVD mechanism base.
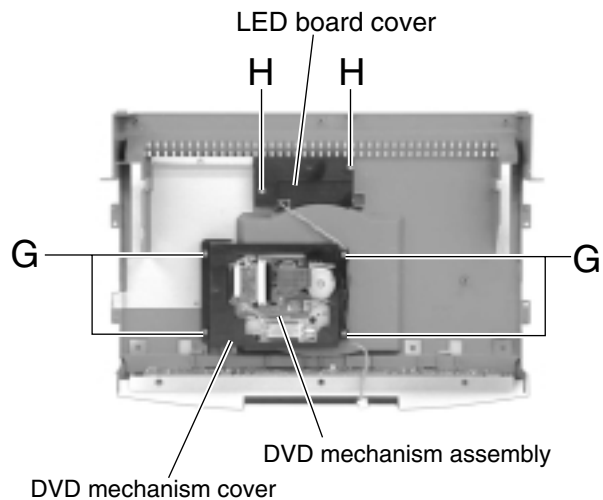
■Removing the LED board (See Figs.10 and 11)

・Prior to performing the following procedure, remove the left and right side covers.
・Also remove the DVD door.

(Note) This work is possible even when the front panel assembly is attached to the DVD mechanism base.

1. Remove two screws (H) that retain the LED board cover, from the back of the DVD mechanism base.

2. Remove the LED board by pulling it away from the DVD mechanism base.

DVD mechanism base

Engaging points (a)   Engaging points (a)
Front panel assembly

Fig.8

F   Display board

Front panel assembly

F

Fig.9

LED board cover
H   H

G   G

DVD mechanism assembly
DVD mechanism cover

Fig.10

DVD mechanism assembly

LED board
Fig.11

■Removing the analog board
(See Figs.12 to 14)

・ Prior to performing the following procedure, remove the left and right side covers.
・ Also remove the DVD door.
・ Also remove the front panel assembly and DVD mechanism base.

1. Disconnect the card wires from the connectors CN401 and CN402 on the analog board.

2. Remove the screw (I) that retains the analog board bracket from the top of the unit.

3. Remove the screw (J) and the screw (K) that retain the analog board from the rear panel of the unit.

4. Disengage the analog board bracket and the gear motor assembly by moving the engaged part (b) upward. Then move the analog board in the direction of the arrow, and remove it as if pulling it out of the rear panel.

5. Remove two screws (L) that attach the analog board to the analog board bracket.
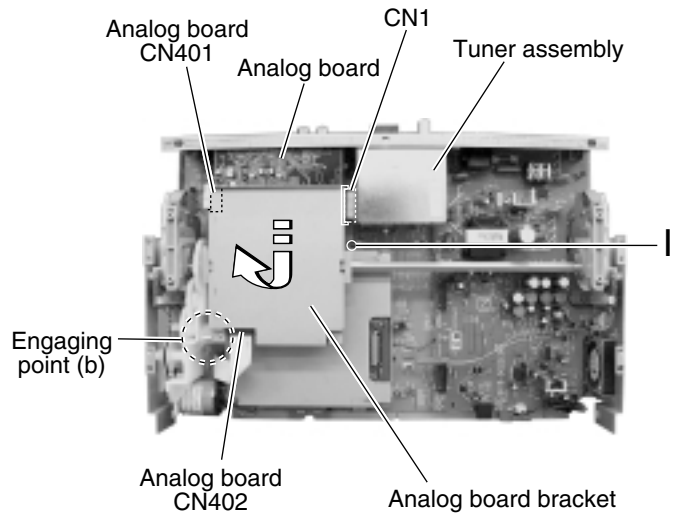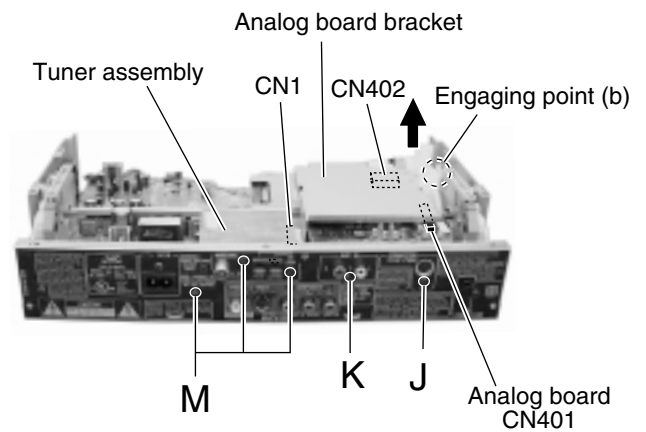
■Removing the tuner assembly
(See Figs.12 and 13)

・ Prior to performing the following procedure, remove the left and right side covers.
・ Also remove the DVD door.
・ Also remove the front panel assembly and the DVD mechanism base.

1. Remove the three screws (M) that retain the tuner assembly, from the rear panel of the unit.

2. Disconnect the card wire from the connector CN1 on the tuner assembly.

Fig.12

Fig.13
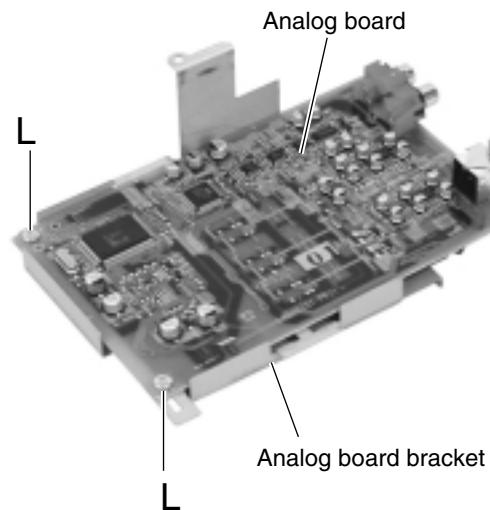
Fig.14

■Removing the fan motor assembly (See Figs.15 and 16)

・ Prior to performing the following procedure, remove the left and right side covers.
・ Also remove the DVD door.
・ Also remove the front panel assembly and the DVD mechanism base.

1. Disconnect the wire from the connector CN972 on the power supply board.

2. Remove the two screws N that retain the fan motor assembly, from the right side of the unit.

3. Remove the two screws (O) that attach the fan motor assembly to the fan bracket.
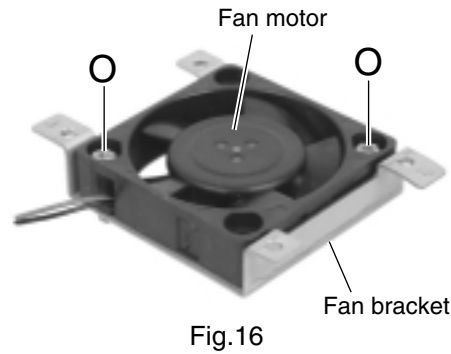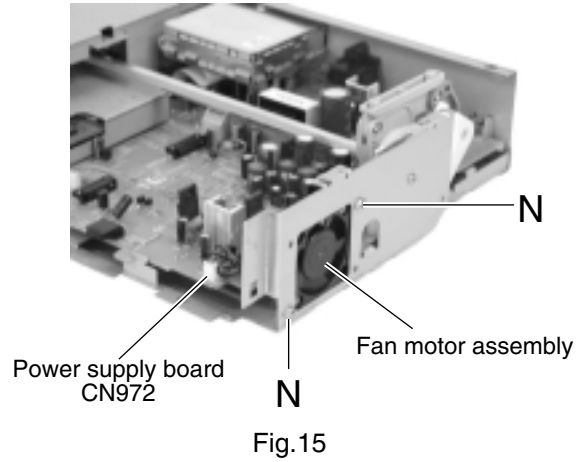
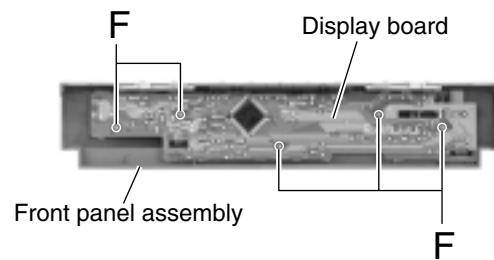## ■Removing the gear motor assembly (See Figs.17 to 19)

・ Prior to performing the following procedure, remove the left and right side covers.
・ Also remove the DVD door.
・ Also remove the front panel assembly and the DVD mechanism base.
・ Also remove the analog board.

1. Disconnect the wire from the connector CN106 on the analog input/output board.

2. Remove the two screws (P) that retain the gear motor assembly and remove the assembly in the direction of the arrow.

(Note) When reassembling, check that the gear motor assembly is engaged properly with the door arm assembly at the engaging points (c) and (d).

3. Remove the belt from the gear motor assembly.

4. Remove two screws Q that retain the gear motor.

Power supply board CN972   N   Fan motor assembly

Fig.15

Fan motor

O   O

Fan bracket

Fig.16

Gear motor assembly

P   Analog I/O board CN106

Fig.17

Gear motor

Belt

Q

Fig.19

Engaging point (c)

Engaging point (d)

P

P

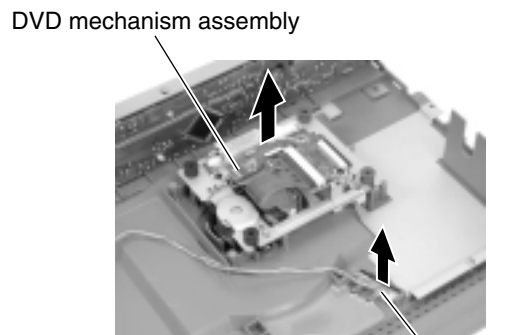Gear motor assembly   Analog I/O board CN106

Fig.18
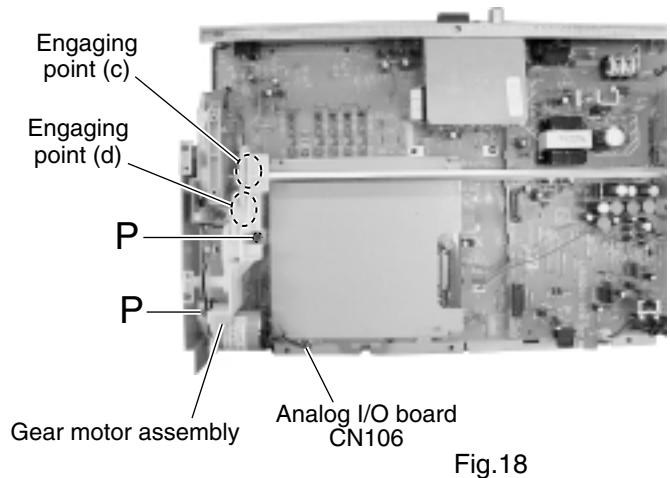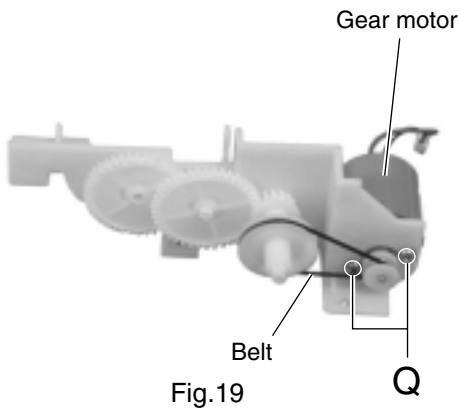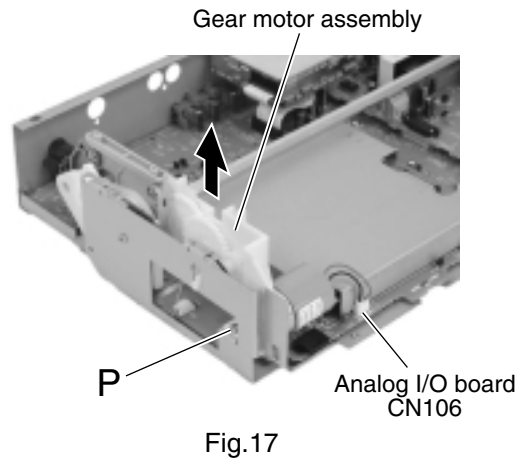
■Removing the door arm assembly
(See Figs.20 to 23)

・ Prior to performing the following procedure, remove the left and right side covers.
・ Also remove the DVD door.
・ Also remove the front panel assembly and the DVD mechanism base.
・ Also remove the analog board.
・ Also remove the gear motor assembly.

1. Disconnect the wires from the connectors CN810 and CN811 on the analog input/output board.

2. Remove the four screws (R) that retain the door arm assembly, from the top of the unit.

3. Remove the two screws (S) that retain the door arm assembly, from the left and right sides of the unit.

Door arm assembly

Analog I/O board
CN811

R

Fig.20

Door arm assembly

R

Analog I/O board
CN810

Power supply
board

Fig.21

Analog I/O board
CN810

Door arm assembly

S

R

Fig.23

Door arm assembly

S

R
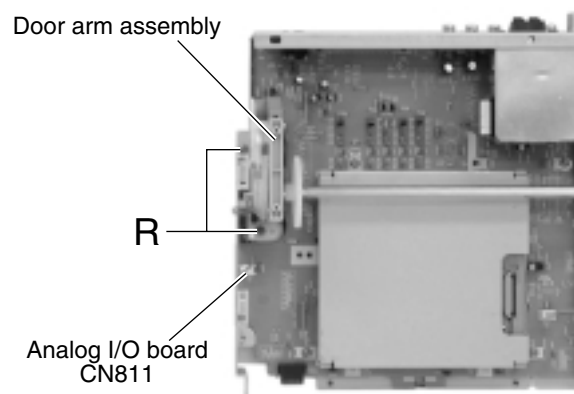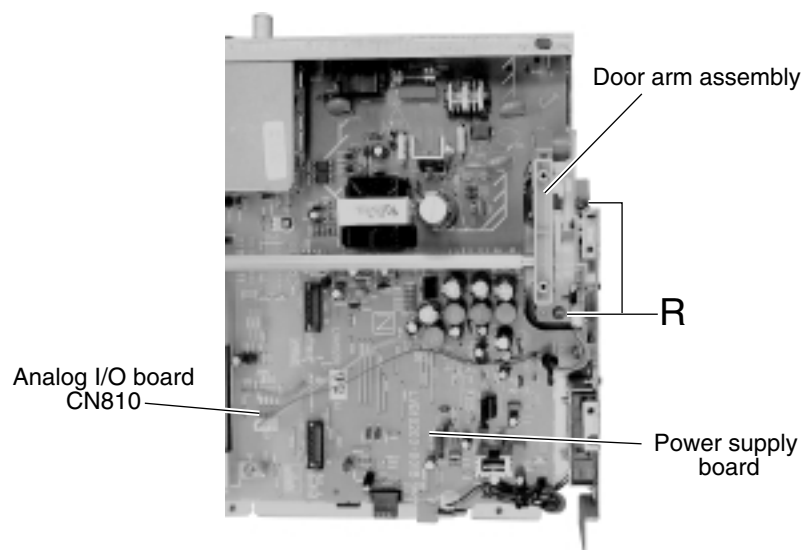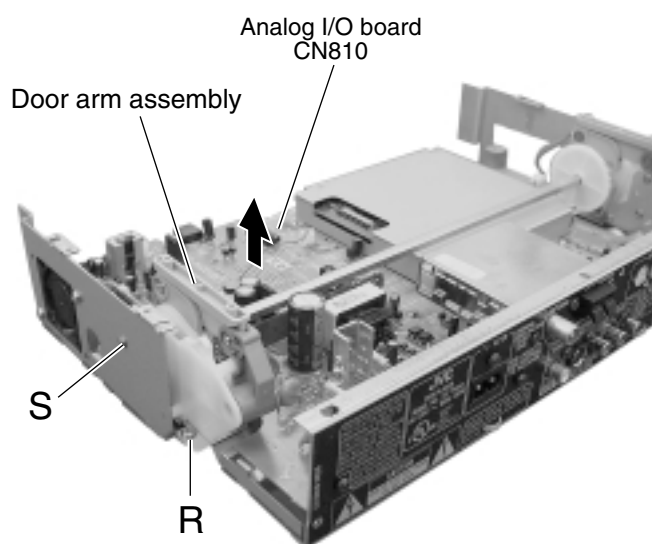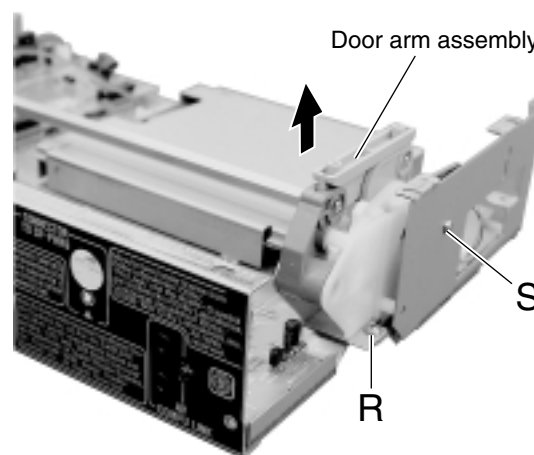
Fig.22

■Removing the door arm boards (L) and (R) (See Figs.24 and 25)

・ Prior to performing the following procedure, remove the left and right side covers.
・ Also remove the DVD door.
・ Also remove the front panel assembly and the DVD mechanism base.
・ Also remove the analog board.
・ Also remove the gear motor assembly.
・ Also remove the door arm assembly.

1. Remove the two screws (U) that retain the door arm board (L).

2. Remove two screws (U) that retain the door arm board (R).

Door arm board (L)

Fig.24

Door arm board (R)
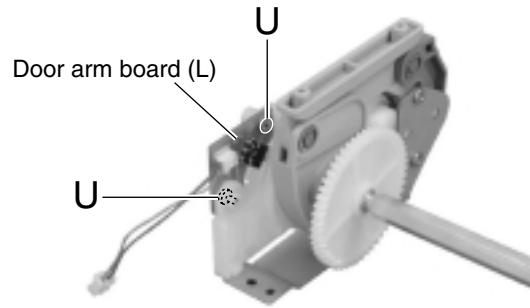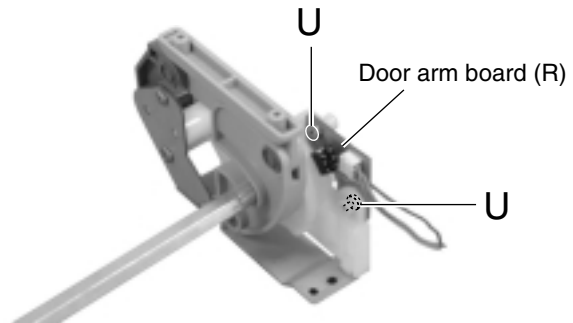
Fig.25

■Removing the power supply board (See Figs.26 and 27)

・ Prior to performing the following procedure, remove the left and right side covers.
・ Also remove the DVD door.
・ Also remove the front panel assembly and the DVD mechanism base.
・ Also remove the analog board.
・ Also remove the gear motor assembly.
   Also remove the door arm assembly.

1. Remove the screw (V) that retains the power supply board, from the top of the unit.

2. Remove three screws (W) that retain the power supply board, from the rear panel of the unit.

3. Pull out the power supply board from clamp a.

4. Disconnect the wire from the connector CN972 on the power supply board, and then remove the power supply board in the direction of the arrow while unplugging the connectors CN951 and CN952 from the analog input/output board.

Analog I/O board   Power supply board

Clamp a

CN951   CN952   Power supply board CN972

Fig.26

Power supply board

Rear panel   CN952   Clamp a

CN951
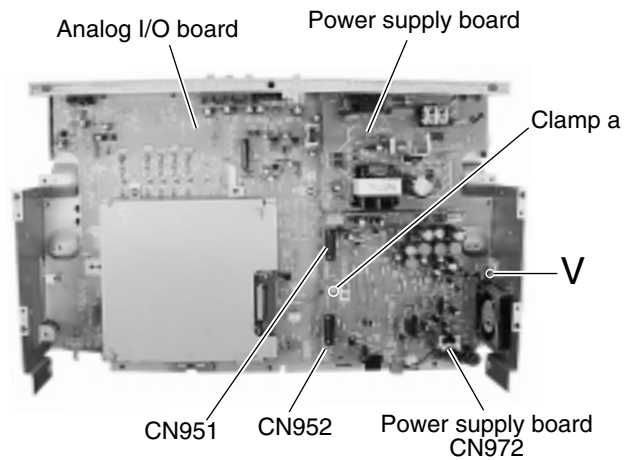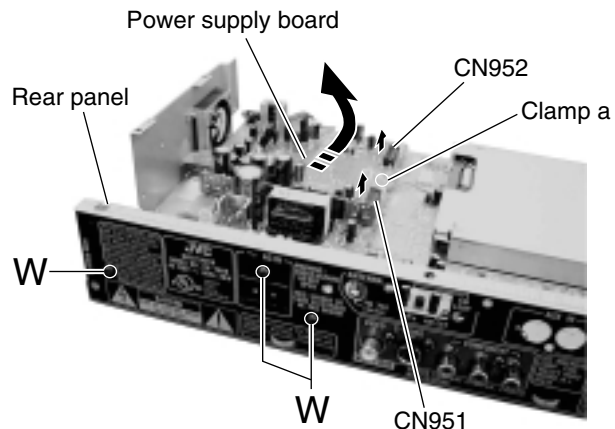
Fig.27

■Removing the AV decoder board and analog input/output board

(See Figs.28 to 30)

・ Prior to performing the following procedure, remove the left and right side covers.
・ Also remove the DVD door.
・ Also remove the front panel assembly and DVD mechanism base.
・ Also remove the analog board.
・ Also remove the gear motor assembly.
・ Also remove the door arm assembly.

1. Remove the three screws (X) that retain the AV decoder board cover, from the top of the unit and remove the screw (X) that retains the analog input/output board.

2. IF it is required to separate the AV decoder board from the analog input/output board, unplug the connectors CN501, CN502 and CN503 on the AV decoder board from the analog input/output board.

   (Note) The analog input/output board can be removed even when it is engaged with the AV decoder board.

3. Remove the four screws (Y) that retain the analog input/output board, from the rear panel of the unit. This procedure also detaches the rear panel.
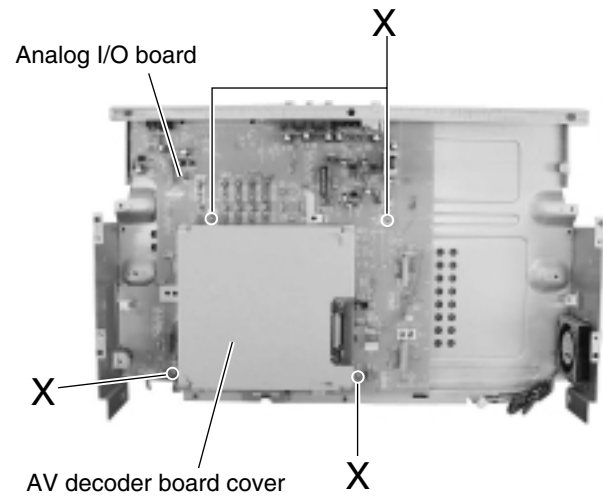
Fig.28
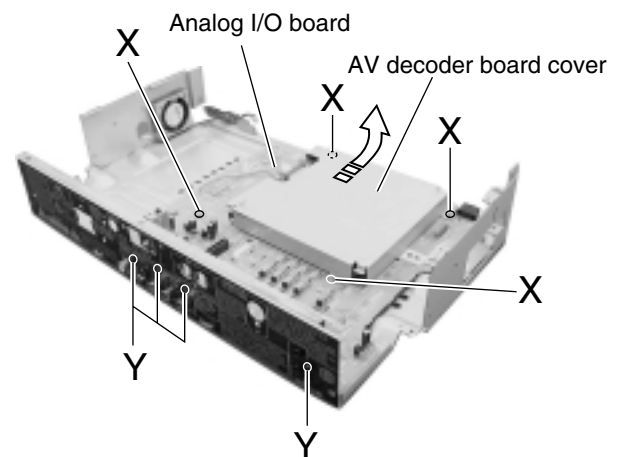
Fig.29
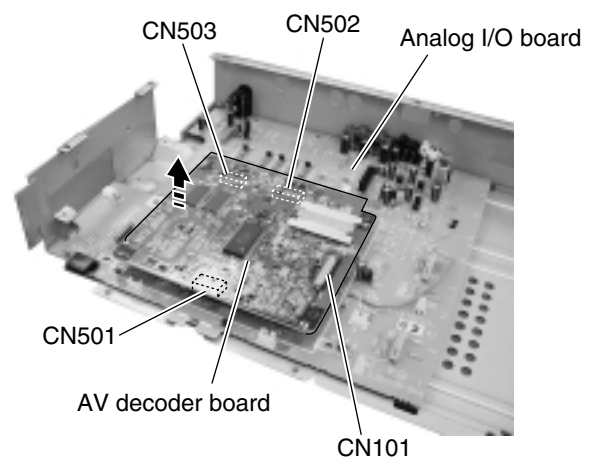
Fig.30

Disassembly method

<Speaker>

■Removing the heat sink cover (See Fig.1)

1. Remove the four screws A attaching the heat sink cover.

■Removing the amplifier assembly and the amplifier cover (See Figs.2 and 3)

・ Prior to performing the following procedure, remove the heat sink.

1. Remove the eigth screws B attaching the amplifier assembly on the back of the body.

2. Move the amplifier assembly backward and disconnect the harness from connector CN109 in the lower part of the amplifier assembly.

3. Pull out the volume knob.

4. Remove the ten screws C attaching the heat sink cover.

5. Remove the ten screws D and the one screw E attaching the amplifier cover.
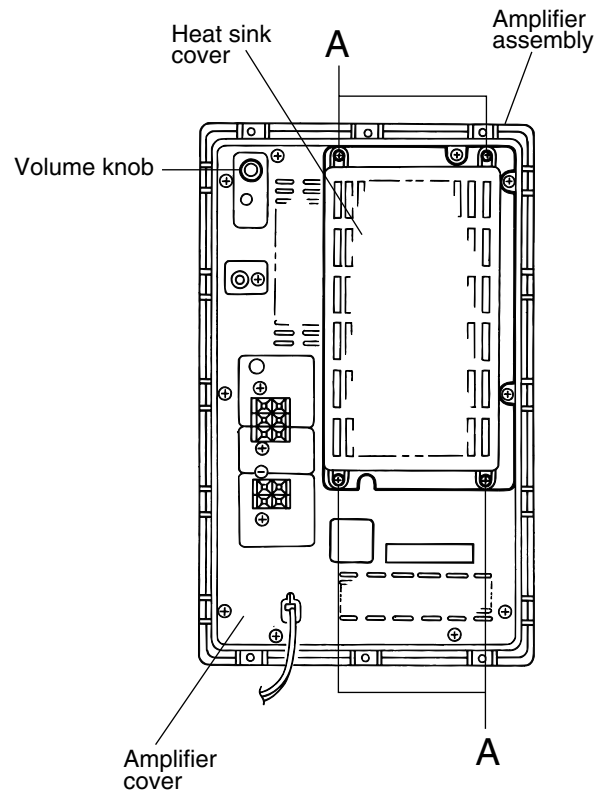
Fig.1
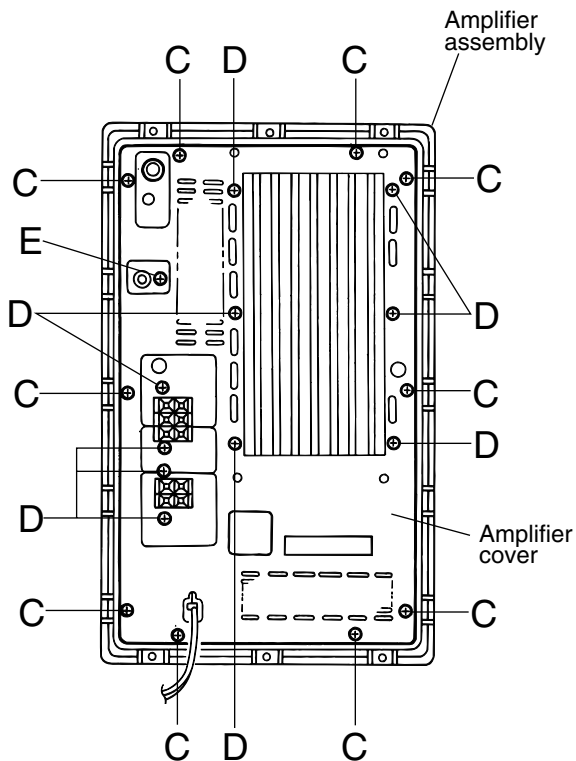
Fig.3
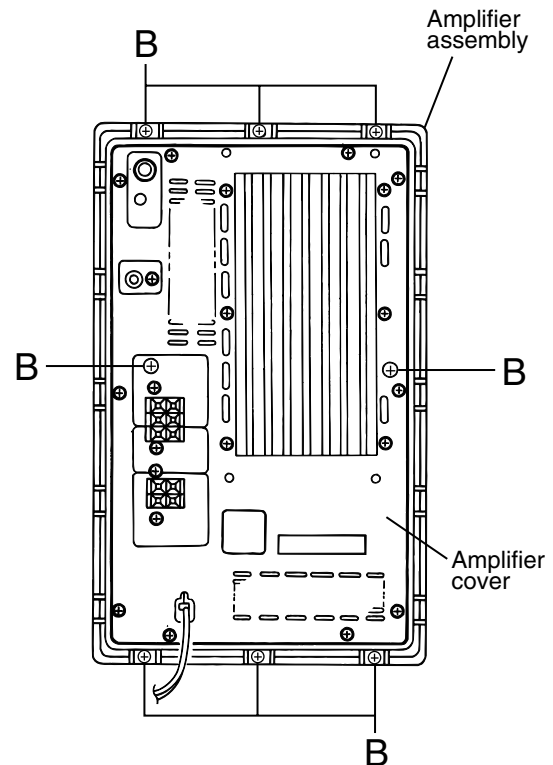
Fig.2

■Removing the preamplifier board
(See Figs.4 to 6)

・ Prior to performing the following procedure, remove the heat sink cover, the amplifier assembly and the amplifier cover.

1. Remove the two screws F attaching the preamplifier board to the bracket.

2. Disconnect connector CN101 on the preamplifier board from the main amplifier board.

3. Pull out the switch knob.

4. Remove the nut and the two screws G attaching the bracket.
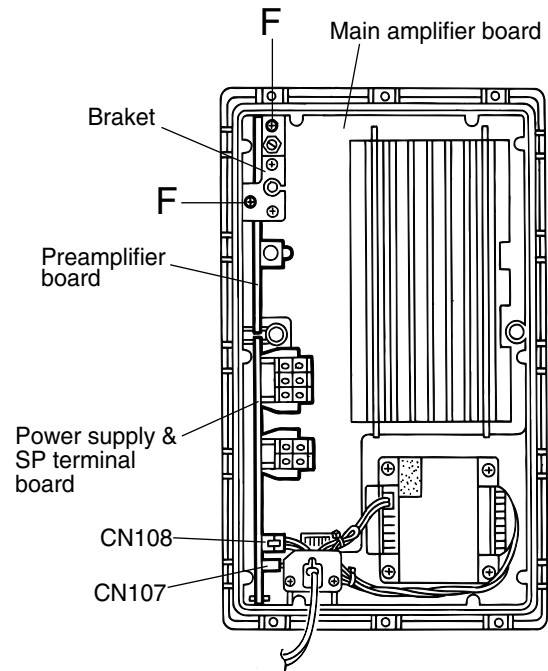
■Removing the power supply & SP terminal board (See Figs.4 and 5)

・ Prior to performing the following procedure, remove the heat sink cover, amplifier assembly and the amplifier cover.

1. Disconnect the wire from the connectors CN107 and CN108 on the power supply & SP terminal board.

2. Unplug the connectors CN110 and CN111 on the power supply & SP terminal board from the main amplifier board.

Fig.4

Fig.5

Fig.6

TH-A9
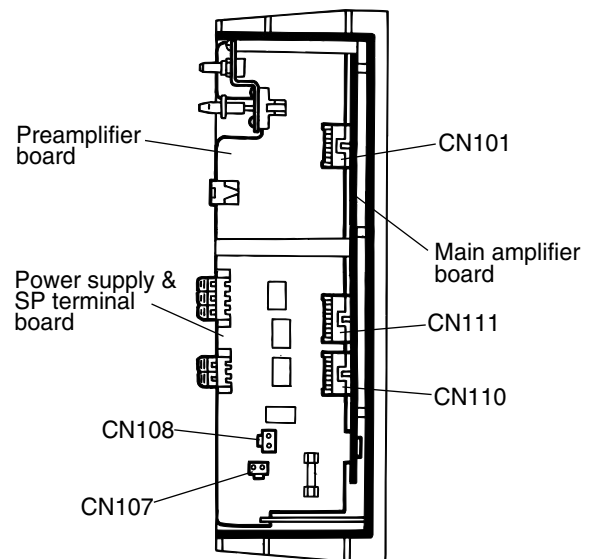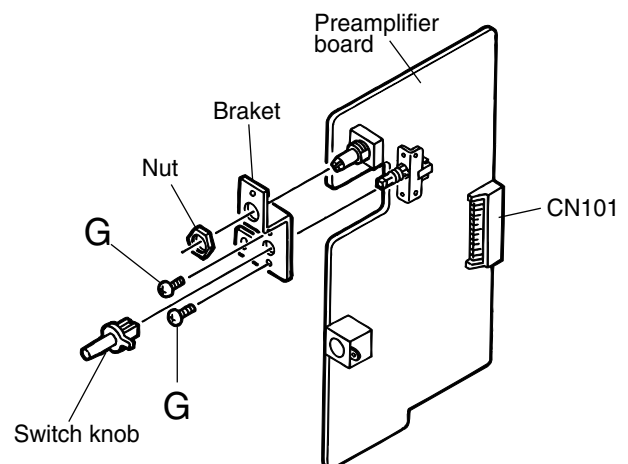
■Removing the Main amplifier Board
(See Figs.7 and 8)

・ Prior to performing the following procedure, remove the heat sink cover, the amplifier board, the amplifier cover, the preamplifier board and the power supply & SP terminal board.

1. Disconnect the harness from connector CN104 on the main amplifier board.

2. Remove the seven screws H and the main amplifier board with the heat sink.

3. Remove the two screws I attaching the power amplifier board (A) and the two screws J attaching the power amplifier board (B) on the underside of the main amplifier board.

4. Disconnect connector CN102 and CN103 on the power amplifier board (A) and CN105 and CN106 on the power amplifier board (B) from the main amplifier board respectively.
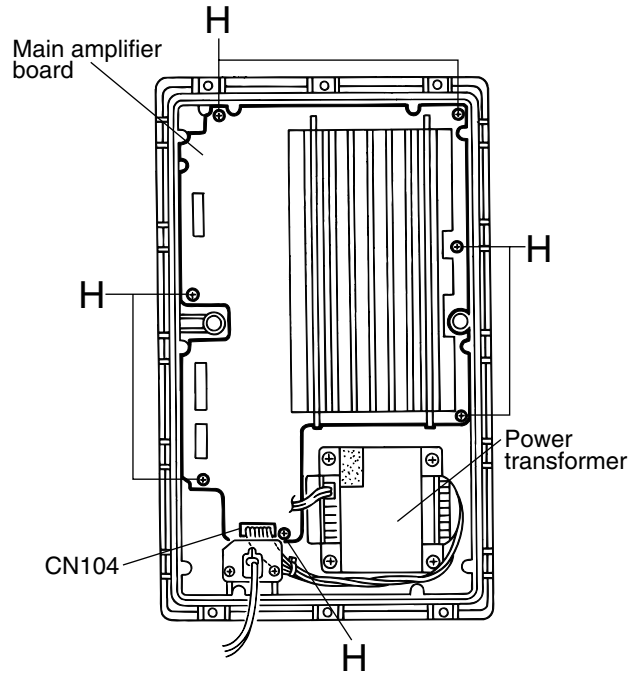
■Removing the power amplifier board (A)
(See Figs.9 and 10)

・ Prior to performing the following procedure, remove the heat sink cover, amplifier assembly, the amplifier cover, the preamplifier board, the power supply & SP terminal board, the main amplifier board.

1. Remove the four screws K attaching the power amplifier board (A) to the heat sink.

2. Release the four joint hooks a bent and attached to the outside of the power amplifier board (A).

3. Move the power amplifier board (A) in the direction of the arrow to release joint b and remove the power amplifier board (A) from the bracket (A).

Fig.7

Fig.8

Fig.10

Fig.9

1-18
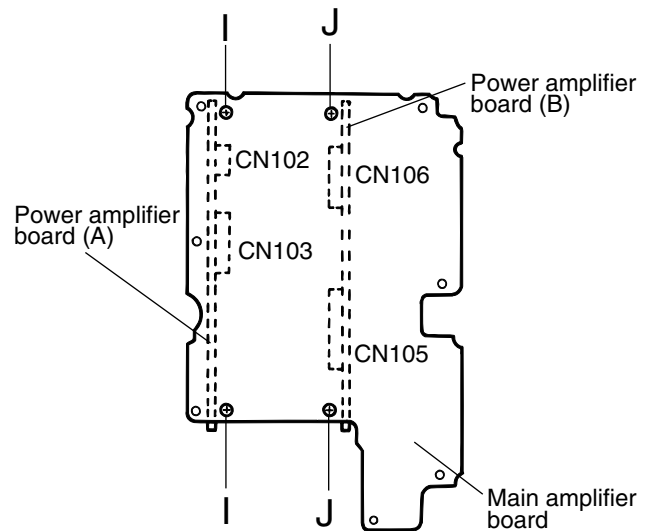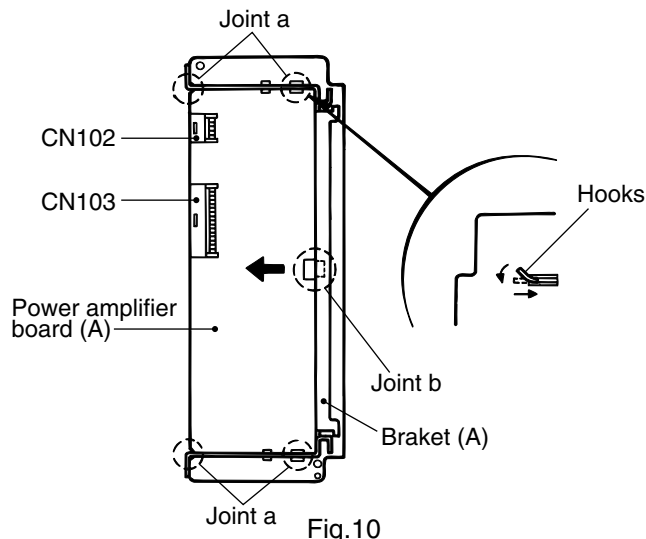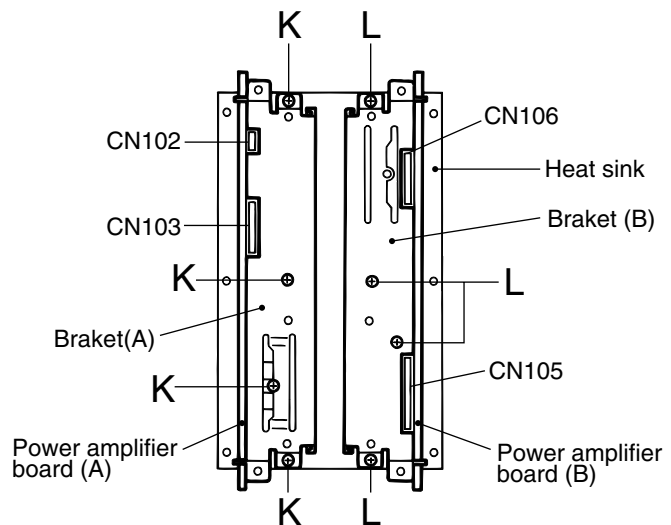
■Removing the power amplifier board (B) (See Figs.9 and 11)

・ Prior to performing the following procedure, remove the heat sink cover, the amplifier assembly, the amplifier cover, the preamplifier board, the power supply & SP terminal board, the main amplifier board and power amplifier board (A).

1. Remove the four screws L attaching the power amplifier board (B) to the heat sink.

2. Release the four joint hooks c bent and attached to the outside of the power amplifier board (B).

3. Move the power amplifier board (B) in the direction of the arrow to release joint d and remove the power amplifier board (B) from the bracket (B).
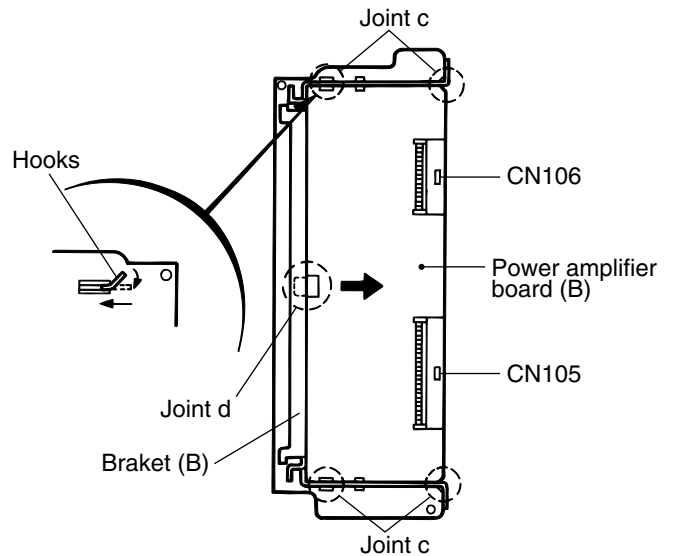
Fig.11

■Removing the power transformer (See Figs.12 and 13)

・ Prior to performing the following procedure, remove the heat sink cover, the amplifier assembly, the amplifier cover, the preamplifier board, the power supply & SP terminal board, the main amplifier board, the power amplifier board (A) and power amplifier board (B).

1. Disconnect the harness from connector CN104 on the main amplifier board.

2. Disconnect the wire from connector CN107 on the power supply & SP terminal board.

3. Remove the four screws M attaching the power transformer.
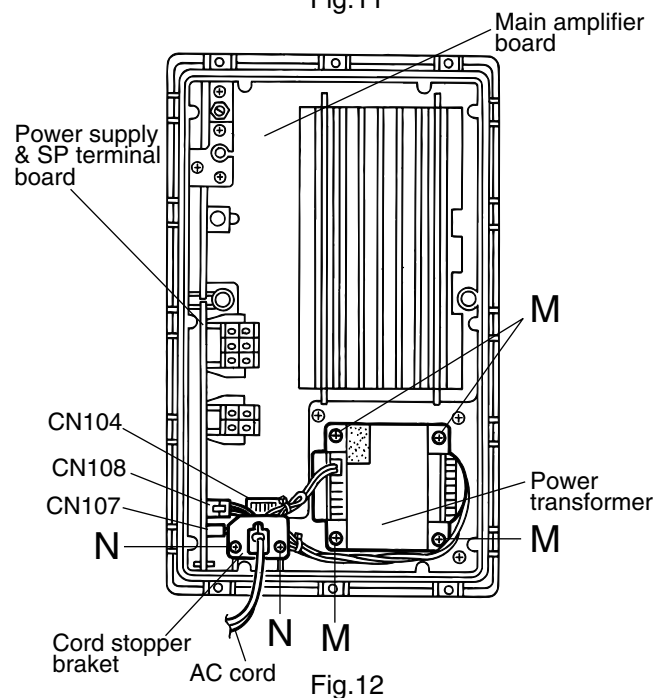
Fig.12

■Removing the AC power cord (See Fig.12)

・ Prior to performing the following procedure, remove the heat sink cover, the amplifier assembly, the amplifier cover, the preamplifier board, the power supply & SP terminal board, the main amplidier board, the power amplifier board (A), the power amplifier board (B) and power transformer.

1. Disconnect the wire from connector CN108 on the power supply & SP terminal board.

2. Remove the two screws N attaching the AC power cord.
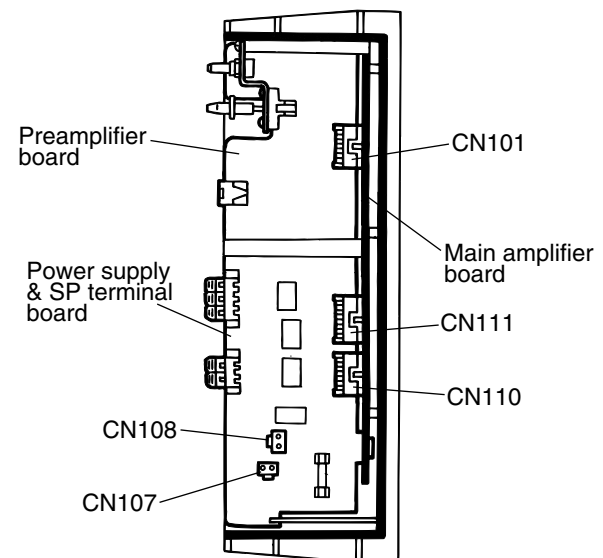
Fig.13

■Initialization of EEPROM

1. Make sure that no disc is present on the tray.

2. At first push the power switch to be on. Then the door slides to the position to be able to push the stop button. After that pull AC plug out.

3. While holding the STOP and OPEN/CLOSE keys on the main unit depressed, turn on the primary power supply.

4. The FL display should show "TEST JC 1".

5. Press the ENTER key on the remote controller.
   Initialization of the EEPROM starts (and lasts for about 3 seconds). The initialization has completed when the FL display shows "EEPROM" at the center.

6. Now the EEPROM initialization is complete.
   No key is accepted during the EEPROM initialization.
   To exit from the test mode, press the POWER key to enter the STAND-BY mode.

■Display of the laser current value

1. While holding the STOP and OPEN/CLOSE keys on the main unit depressed, plug the AC power cord into the power outlet.

2. The FL display should show "TEST".
   Note: When the power is in the STAND-BY mode or OFF, the stop key is hidden behind the door.
          Therefore, to facilitate the entry in the test mode, slide the door in advance so that the STOP key can be pressed even when the AC power is turned off by unplugging the AC power cord.

3. Press the "5" key on the remote controller in the test mode. The DVD laser will turn on and the FL display will show a message such as "03EXXXX". As the FL display shows a hexadecimal value, check the actual current value by referring to the conversion table to see if it is OK or not. (The actual laser current value is calculated by subtracting 15 mA from the value obtained with the conversion table.)

4. To exit from the test mode, press the POWER key to enter the STAND-BY (power off) mode.

FL Display conversion table

1.Current

FL Display	Current(mA)	Evalution	FL Display	Current(mA)	Evalution	FL Display	Current(mA)	Evalution
001c,001b	25	OK	03E5	59	OK	03AF,03AE	93	NG
001A	26	OK	03E4,03E3	60	OK	03Ad	94	NG
0019,0018	27	OK	03E2	61	OK	03Ac,03Ab	95	NG
0017	28	OK	03E1,03E0	62	OK	03AA,03A9	96	NG
0016,0015	29	OK	03dF,03dE,	63	OK	03A8	97	NG
0014,0013	30	OK	03dd	64	OK	03A7,03A6	98	NG
0012	31	OK	03dc,03db	65	NG	03A5	99	NG
0011,0010	32	OK	03dA	66	NG	03A4,03A3	100	NG
000f	33	OK	03d9,03d8	67	NG	03A2,03A1	101	NG
000e,000d	34	OK	03d7,03d6	68	NG	03A0	102	NG
000c,000b	35	OK	03d5	69	NG	039F,039E	103	NG
000A	36	OK	03d4,03d3	70	NG	039d,039c	104	NG
0009,0008	37	OK	03d2	71	NG	039b	105	NG
0007	38	OK	03d1,03d0	72	NG	039A,0399	106	NG
0006,0005	39	OK	03cF,03cE	73	NG	0398	107	NG
0004,0003	40	OK	03cd	74	NG	0397	108	NG
0002	41	OK	03cc,03cb	75	NG			
0001,0000	42	OK	03cA,03c9	76	NG			
03FF	43	OK	03c8	77	NG			
03FE,03Fd	44	OK	03c7,03c6	78	NG			
03Fc,03Fb	45	OK	03c5	79	NG			
03FA	46	OK	03c4,03c3	80	NG			
03F9,03F8	47	OK	03c2,03c1	81	NG			
03F7	48	OK	03c0	82	NG			
03F6,03F5	49	OK	03bF,03bE	83	NG			
03F4,03F3	50	OK	03bd	84	NG			
03F2	51	OK	03bc,03bb	85	NG			
03F1,03F0	52	OK	03bA,03b9	86	NG			
03EF,03EE	53	OK	03b8	87	NG			
03Ed	54	OK	03b7,03b6	88	NG			
03Ec,03Eb	55	OK	03b5	89	NG			
03EA	56	OK	03b4,03b3	90	NG			
03E9,03E8	57	OK	03b2,03b1	91	NG			
03E7,03E6	58	OK	03b0	92	NG			

Discription of major IC's

■AK93C65AF-X(IC403) : EEPROM

1.Terminal layout

```
        ┌──────────┐
PE  ──┤ 1      8 ├── NC
        │          │
VCC ──┤ 2      7 ├── GND
        │          │
CS  ──┤ 3      6 ├── DO
        │          │
SK  ──┤ 4      5 ├── DI
        └──────────┘
          8 pin SOP
```
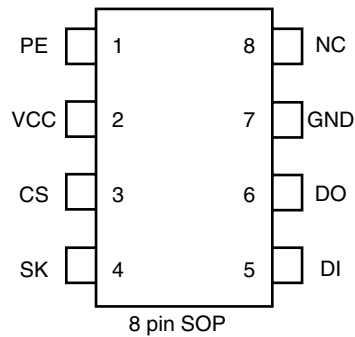
2.Block diagram
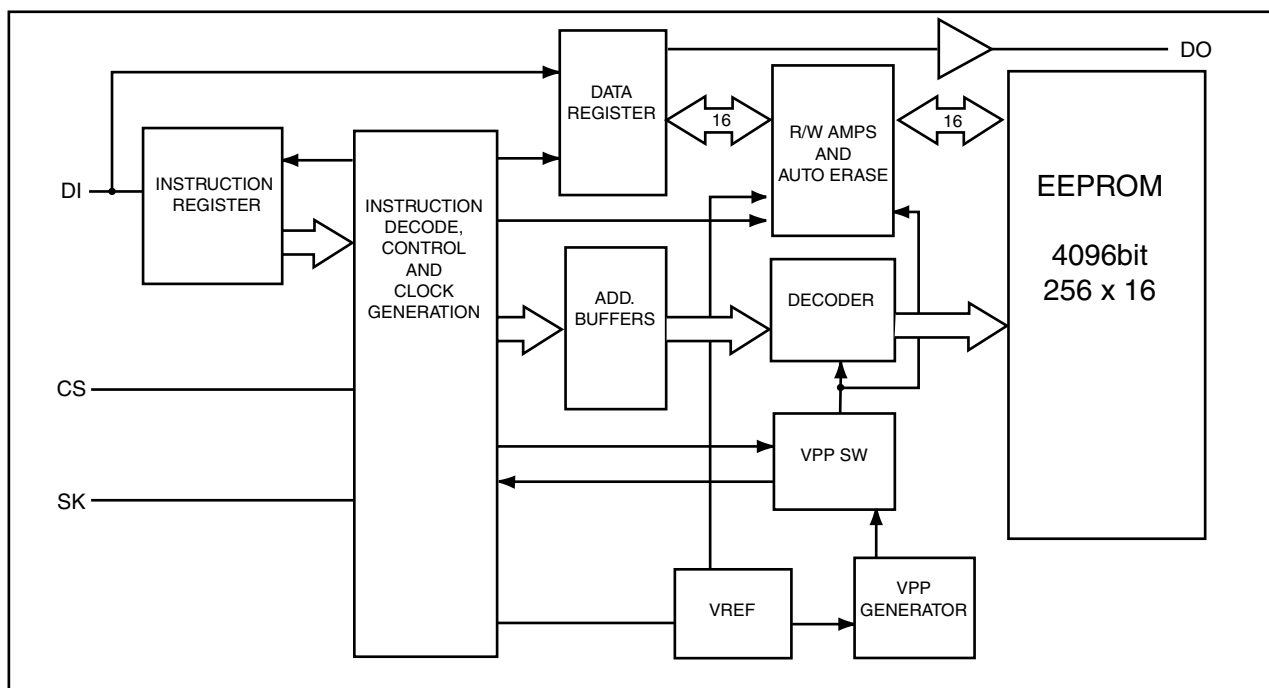
3.Pin function

Pin No.	Symbol	Function
1	PE	Program enable (With built-in pull up resistor)
2	VCC	Power supply
3	CS	Chip selection
4	SK	Serial clock input
5	DI	Serial data input
6	DO	Serial data output
7	GND	Ground
8	NC	No connection

Note : The pull-up resistor of the PE pin is about 2.5 M Ω (VCC=5V)

■ AN8702FH (IC101) : Frontend processor

1.Pin layout

Top pins (left to right): 64 HDTYPE, 63 VIN12, 62 VIN11, 61 GND1, 60 VIN4, 59 VIN3, 58 VIN2, 57 VIN1, 56 VREF1, 55 VCC1, 54 VIN10, 53 VIN9, 52 VIN8, 51 VIN7, 50 VIN6, 49 VIN5

Left pins (top to bottom): 1 PC1, 2 PC01, 3 PC2, 4 PC02, 5 TGBAL, 6 TBAL, 7 FBAL, 8 POFLT, 9 DTRD, 10 IDGT, 11 STANDBY, 12 SEN, 13 SCK, 14 STDI, 15 RSEL, 16 JLINE

AN8702FH

Right pins (top to bottom): 48 RFINN, 47 RFINP, 46 TESTSG, 45 AGCO, 44 AGCG, 43 PEAK, 42 BOTTOM, 41 RFENV, 40 BDO, 39 OFTR, 38 DCRF, 37 RFC, 36 VCC3, 35 RFOUT, 34 RFDIFO, 33 GND3

Bottom pins (left to right): 17 TEN, 18 TEOUT, 19 ASN, 20 ASOUT, 21 FEN, 22 FEOUT, 23 VSS, 24 TG, 25 VDD, 26 GND2, 27 VREF2, 28 VCC2, 29 VHALF, 30 DFLTON, 31 DFLTOP, 32 DSFLT

2. Pin function

AN8702FH

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	PC1			33	GND3	-	Earth terminal 3
2	PC01			34	RFDIFO		
3	PC2			35	RFOUT		
4	PC02			36	VCC3	-	Power terminal 3 (5V)
5	TGBAL	I	Tangential phase balance control terminal	37	RFC		
6	TBAL	I	Tracking balance control terminal	38	DCRF	O	BDO output terminal
7	FBAL	I	Focus balance control terminal	39	OFTR	O	OFTR output terminal
8	POFLT	O	Track detection threshold value level terminal	40	BDO	O	BDO output terminal
9	DTRD	I	Data slice data read signal input terminal (For RAM)	41	RFENV	O	RF enve output terminal
10	IDGT	I	Data slice part address part gate signal input terminal (For RAM)	42	BOTTOM	O	Bottom enve detection filter terminal
11	STANDBY	I	Standby mode control terminal	43	PEAK	O	Peak enve detection filter terminal
12	SEN	I	SEN(Sereal data input terminal)	44	AGCG	O	AGC amplifier gain control terminal
13	SCK	I	SCK(Sereal data input terminal)	45	AGCO		
14	STDI	I	STDI(Sereal data input terminal)	46	TESTSG	I	TEST signal input terminal
15	RSEL			47	RFINP	I	RF signal positive moving input terminal
16	JLINE			48	RFINN	I	RF signal reversing input terminal
17	TEN			49	VIN5	I	Focus input of external division into two terminal
18	TEOUT	O	Tracking error signal output terminal	50	VIN6	I	Focus input of external division into two terminal
19	ASN			51	VIN7	I	
20	ASOUT			52	VIN8	I	
21	FEN	I	Focus error output amplifier reversing input terminal	53	VIN9	I	
22	FEOUT	O	Focus error signal output terminal	54	VIN10	I	
23	VSS	-	Earth terminal	55	VCC1	-	Power terminal 1
24	TG	O	Tangential phase error signal output terminal	56	VREF1	O	VREF1 voltage output terminal
25	VDD	-	Power terminal (3V)	57	VIN1	I	External division into four (DVD/CD) RF input terminal 1
26	GND2	-	Earth terminal 2	58	VIN2	I	External division into four (DVD/CD) RF input terminal 2
27	VREF2	O	VREF2 voltage output terminal	59	VIN3	I	External division into four (DVD/CD) RF input terminal 3
28	VCC2	-	Power terminal (5V)	60	VIN4	I	External division into four (DVD/CD) RF input terminal 4
29	VHALF	O	VHALF voltage output terminal	61	GND1	-	Earth terminal 1
30	DFLTON			62	VIN11	I	
31	DFLTOP			63	VIN12	I	
32	DSFLT			64	HDTYPE		

■ HY57V161610DTC8 or KM416S1120DT-G8 (IC504,IC505) : 16MB SDRAM

1.Block diagram
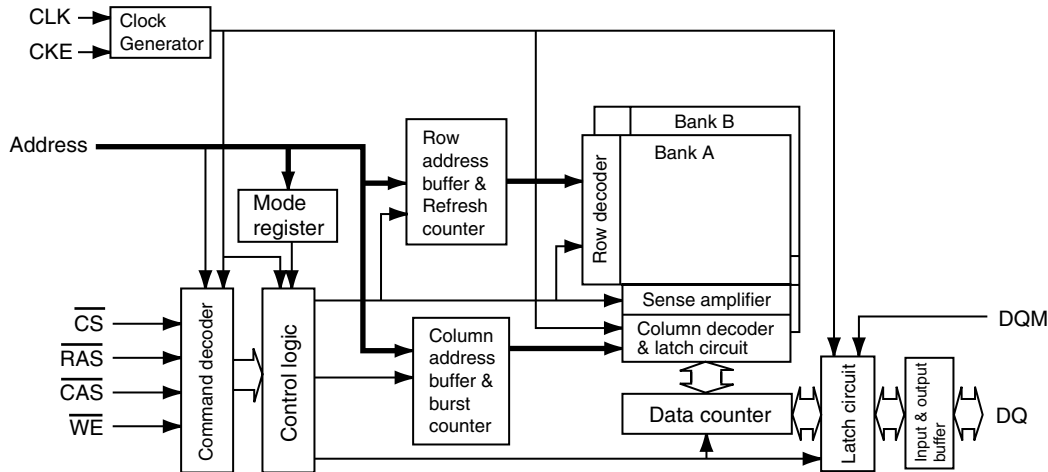
2.Pin function

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	VCC	Power supply	26	VSS	Connect to GND
2,3	DQ0,1	Data input/output	27~32	A4~9	Address inputs
4	VSS	Connect to GND	33	NC	Non connect
5,6	DQ2,3	Data input/output	34	CKE	Clock enable
7	VDD	Power supply	35	CLK	System clock input
8,9	DQ4,5	Data input/output	36	UDQM	Upper DQ mask enable
10	VSS	Connect to GND	37	NC	Non connect
11,12	DQ6,7	Data input/output	38	VCC	Power supply
13	VCC	Power supply	39,40	DQ8,9	Data input/output
14	LDQM	Lower DQ mask enable	41	VSS	Connect to GND
15	$\overline{WE}$	Write enable	42,43	DQ10,11	Data input/output
16	$\overline{CAS}$	Column address strobe	44	VDD	Power supply
17	$\overline{RAS}$	Row address strobe	45,46	DQ12,13	Data input/output
18	$\overline{CS}$	Chip enable	47	VSS	Connect to GND
19,20	A11,10	Address inputs	48,49	DQ14,15	Data input/output
21~24	A0~3	Address inputs	50	VSS	Connect to GND
25	VCC	Power supply			

■ M56788FP-W(IC271) : Traverse mechanism driver

1.Pin layout

CH3IN	1		42	REG+
OUT3	2		41	REGB
IN3-	3		40	IN1+
VBS2	4		39	VBS1
Vm2	5		38	Vm1
N.C	6		37	IN1-
GND	7		36	OUT1
IN3+	8		35	VM1-
VM3-	9		34	VM1+
VM3+	10		33	GND
GND	11		32	VM2+
VM4+	12		31	VM2-
VM4-	13		30	OUT2
VM5+	14		29	GND
VM5-	15		28	IN2-
OUT5	16		27	IN2+
IN5-	17		26	MUTE1
IN5+	18		25	MUTE2
IN4+	19		24	SS.GND
IN4-	20		23	VREF
OUT4	21		22	VERFO
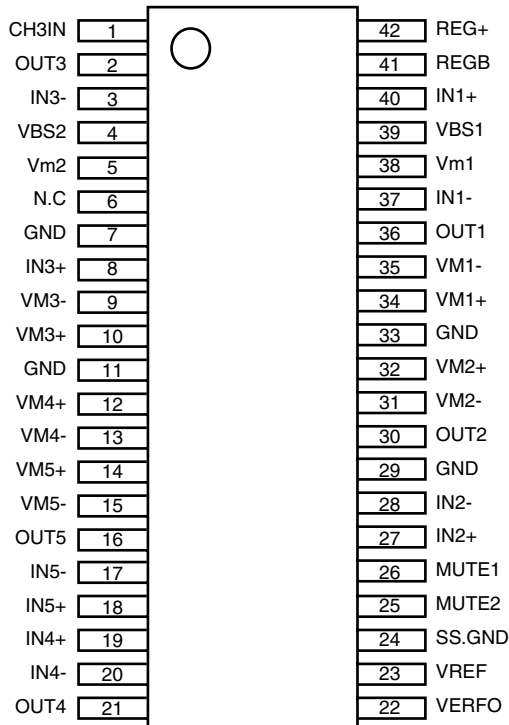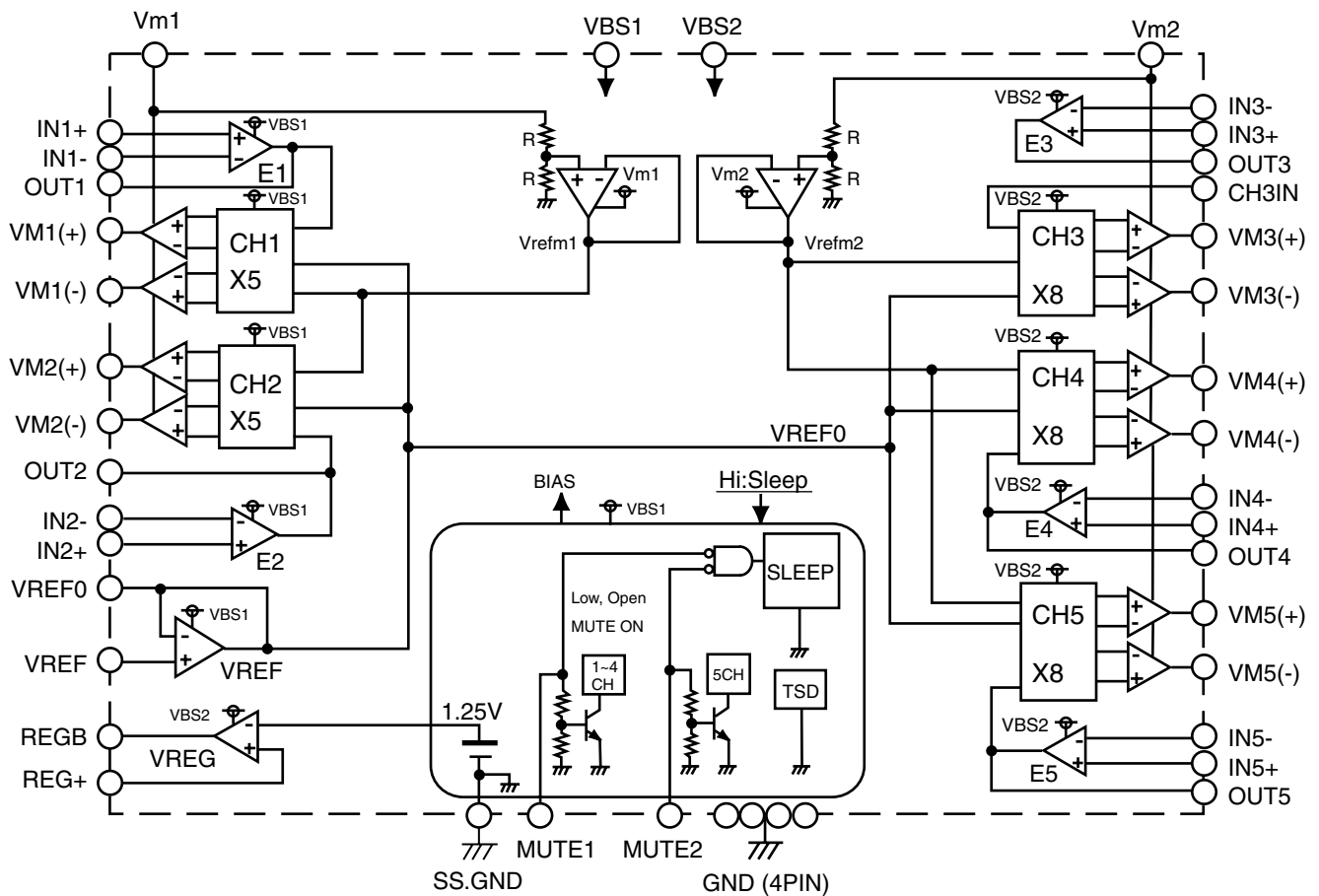
2.Block diagram

■ MC44724AVFU (IC554) : VIDEO ENCODER

1.Terminal layout
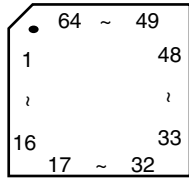
2.Block diagrams
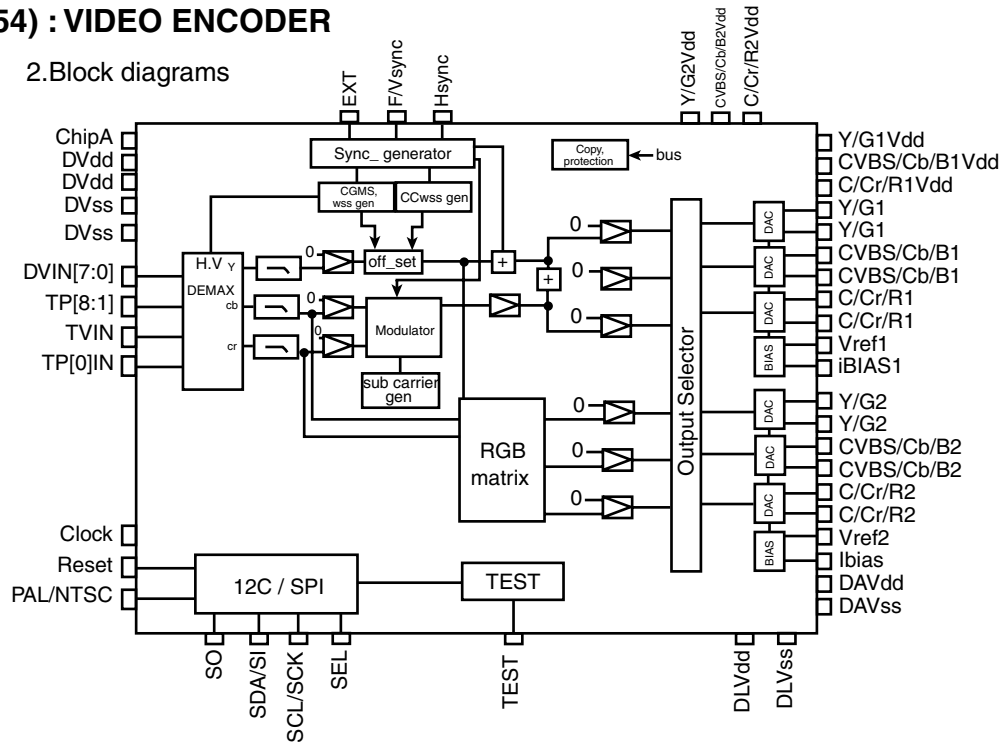
3.Pin function

No.	Symbol	I/O	Function	No.	Symbol	I/O	Function
1	CVBS/Cb/B1	O	Analog composite drive signal (+)	33	SO	-	Non connect
2	CVBS/Cb/B1	O	Analog composite drive signal (-)	34	SDA/SI	I	SPI Mode : Serial data input
3	CVBS/Cb/B1Vdd	-	Power supply for CVBS/Cb/B DAC1	35	SCL/SCK	I	Serial clock input
4	Y/G1	O	Analog brightness signal/G drive signal (+)	36	SEL	I	Power supply for serial data,chip select,digital
5	Y/G1	O	Analog brightness signal/G drive signal (-)	37	DVdd	--	Power supply for digital circuit
6	Y/G1/Vdd	-	Power supply for Y/G DAC	38	DVss	--	Digital ground
7	C/Cr/R1	O	Analog chroma signal (+)	39	DVIN7	I/O	Y data input / test data I/O
8	C/Cr/R1	O	Analog chroma signal (-)	40	DVIN6	I/O	Y data input / test data I/O
9	C/Cr/R1Vdd	-	Power supply for C/Cr/RDAC	41	DVIN5	I/O	Y data input / test data I/O
10	DAVss	-	Connect to ground for DAC	42	DVIN4	I/O	Y data input / test data I/O
11	TBIAS1	O	Standard BIAS for DAC1	43	DVIN3	I/O	Y data input / test data I/O
12	Vref1	-	Standard voltage for DAC1	44	DVIN2	I/O	Y data input / test data I/O
13	DAVdd	-	Power supply for DAC	45	DVIN1	I/O	Y data input / test data I/O
14	Vref2	-	Standard voltage for DAC2	46	DVIN0	I/O	Y data input / test data I/O
15	TBIAS2	O	Standard BIAS for DAC2	47	TVIN	I	VIDEO mute on Reset(0:nomal, 1:mute)
16	NC	-	Non connect	48	EXT	I/O	Frame output / VBI information input
17	CVBS/Cb/B2	O	Analog composite drive signal (+)	49	F/Vsyac	I/O	Frame / Vertical, synchronous I/O
18	CVBS/Cb/B2	O	Analog composite drive signal (-)	50	Chsyac	I/O	The horizontal, synchronous I/O
19	CVBS/Cb/B2Vdd	-	Power supply for CVBS/Cb/B DAC2	51	DATST	I	Data input
20	Y/G2	O	Analog brightness signal/G drive signal (+)	52	TP-8	I/O	Multiplex data input
21	Y/G2	O	Analog brightness signal/G drive signal (-)	53	TP7	I/O	Multiplex data input
22	Y/GVdd	-	Power supply for Y/G DAC	54	TP6	I/O	Multiplex data input
23	C/Cr/R2	O	Analog chroma signal (+)	55	TP5	I/O	Multiplex data input
24	C/Cr/R2	O	Analog chroma signal (-)	56	DVss	-	Ground for digital circuit
25	C/Cr/R2Vdd	-	Power supply for C/Cr/RDAC2	57	DVdd	-	Power supply for digital circuit
26	ChipA	-	Chip address selection	58	TP4	I/O	Data input / Test data I/O
27	TEST	I	Connect to test pin	59	TP3	I/O	Data input / Test data I/O
28	DVdd	-	Digital ground	60	TP2	I/O	Data input / Test data I/O
29	CLOCK	I	Clock signal input (27MHz)	61	TP1	I/O	Data input / Test data I/O
30	DVss	-	Power supply for digital circuit	62	TP0	I/O	Data input / Test data I/O
31	Reset	I	Reset signal input L:ON	63	DLVdd	-	Power supply for D/A converter
32	PAL/NTSC	I	Selection NTSC/PAL NTSC:L PAL:H	64	DLVss	-	Ground for D/A converter

■ MN102L25GHW(IC401) : UNIT CPU

1. Pin layout

MN102L25GHW
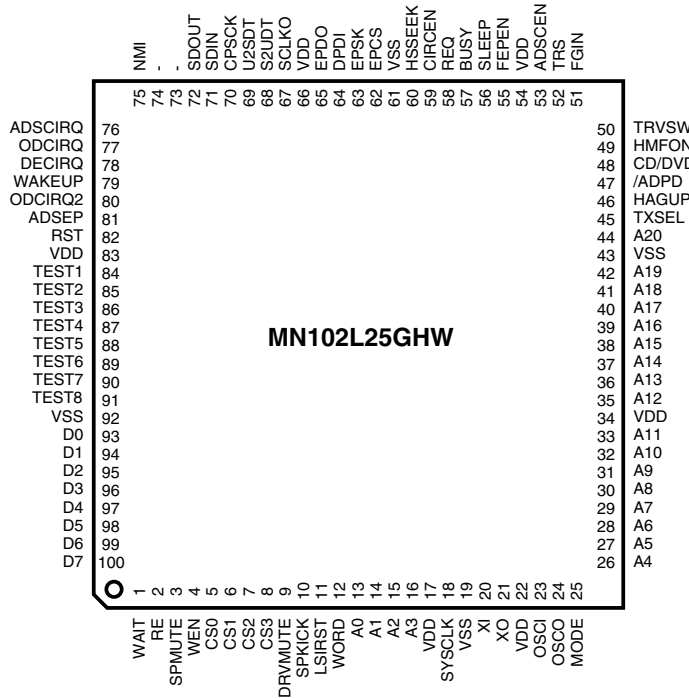
2.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	WAIT	I	Micon wait signal input	51	FGIN	I	Photo input
2	RE	O	Read enable	52	TRS		
3	SPMUTE	O		53	ADSCEN	O	Serial enable signal for ADSC
4	WEN	O	Write enable	54	VDD	-	Power supply
5	CS0	O	Non connect	55	FEPEN	O	Serial enable signal for FEP
6	CS1	O	Chip select for ODC	56	SLEEP	O	Standby signal for FEP
7	CS2	O	Chip select for ZIVA	57	BUSY	I	Communication busy
8	CS3	O	Chip select for outer ROM	58	REQ	O	Communication request
9	DRVMUTE	O	Driver mute	59	CIRCEN	O	CIRC command select
10	SPKICK	O	Non connect (Spin kick output)	60	HSSEEK	O	Seek select
11	LSIRST	O	LSI reset	61	VSS	-	GND
12	WORD	O	Bus selection input	62	EPCS	O	Chip select signal for EEPROM
13	A0	O	Address bus 0 for CPU	63	EPSK	O	Clock signal for EEPROM
14	A1	O	Address bus 1 for CPU	64	DPDI	I	Input data for EEPROM
15	A2	O	Address bus 2 for CPU	65	EPDO	O	Output data for EEPROM
16	A3	O	Address bus 3 for CPU	66	VDD	-	Power supply
17	VDD	-	Power supply	67	SCLKO	I	Communication clock
18	SYSCLK	O	System clock signal output	68	S2UDT	I	Communication input data
19	VSS	-	GND	69	U2SDT	O	Communication output data
20	XI	-	Non connect (Connect to VSS)	70	CPSCK	O	Clock for ADSC serial
21	XO	-	Non connect	71	SDIN	I	ADSC serial data input
22	VDD	-	Power supply	72	SDOUT	O	ADSC serial data output
23	OSCI	I	Clock signal input (13.5MHz)	73	-	-	Non connect
24	OSCO	O	Clock signal output (13.5MHz)	74	-	-	Non connect
25	MODE	I	CPU Mode selection input	75	NMI	-	Non connect
26	A4	O	Address bus 4 for CPU	76	ADSCIRQ	I	Interrupt input of ADSC
27	A5	O	Address bus 5 for CPU	77	ODCIRQ	I	Interrupt input of ODC
28	A6	O	Address bus 6 for CPU	78	DECIRQ	I	Interrupt input of ZIVA
29	A7	O	Address bus 7 for CPU	79	WAKEUP	O	Non connect
30	A8	O	Address bus 8 for CPU	80	ODCIRQ2	I	
31	A9	O	Address bus 9 for CPU	81	ADSEP	I	Address data selection input
32	A10	O	Address bus 10 for CPU	82	RST	I	Reset input
33	A11	O	Address bus 11 for CPU	83	VDD	-	Power supply
34	VDD	-	Power supply	84	TEST1	I	Test signal 1 input
35	A12	O	Address bus 12 for CPU	85	TEST2	I	Test signal 2 input
36	A13	O	Address bus 13 for CPU	86	TEST3	I	Test signal 3 input
37	A14	O	Address bus 14 for CPU	87	TEST4	I	Test signal 4 input
38	A15	O	Address bus 15 for CPU	88	TEST5	I	Test signal 5 input
39	A16	O	Address bus 16 for CPU	89	TEST6	I	Test signal 6 input
40	A17	O	Address bus 17 for CPU	90	TEST7	I	Test signal 7 input
41	A18	O	Address bus 18 for CPU	91	TEST8	I	Test signal 8 input
42	A19	O	Address bus 19 for CPU	92	VSS	-	GND
43	VSS	-	GND	93	D0	I/O	Data bus 0 of CPU
44	A20	O	Address bus 20 for CPU	94	D1	I/O	Data bus 1 of CPU
45	TXSEL	O	TX select	95	D2	I/O	Data bus 2 of CPU
46	HAGUP	O		96	D3	I/O	Data bus 3 of CPU
47	/ADPD			97	D4	I/O	Data bus 4 of CPU
48	CD/DVD	O		98	D5	I/O	Data bus 5 of CPU
49	HMFON			99	D6	I/O	Data bus 6 of CPU
50	TRVSW	I	Detection switch of traverse inside	100	D7	I/O	Data bus 7 of CPU

■ MN103S13BDA(IC301) : Optical disc controller

1. Pin layout

Top pins (left to right, 144–109):
DMARQ, NIOWR, VSS, NIORD, IORDY, NDMACK, VDD, INTRQ, NIOCS16, DA1, VSS, NPDIAG, DA0, DA2, VDD, NCS1FX, NCS3FX, NDASP, NTRYCL, VDD, NEJECT, VSS, MONI0, MONI1, MONI2, MONI3, SDATA, SCLOCK, VDD, DAT0, DAT1, DAT2, DAT3, CHCK40, NCLDCK, SUBC

Left pins (1–36):
1 HDD15
2 HDD0
3 HDD14
4 VDD
5 HDD1
6 HDD13
7 HDD2
8 VSS
9 HDD12
10 VDD
11 HDD3
12 HDD11
13 HDD4
14 HDD10
15 VDD
16 HDD5
17 HDD9
18 VSS
19 HDD6
20 HDD8
21 HDD7
22 VDDH
23 NRESET
24 MASTER
25 NINT0
26 NINT1
27 WAITDOC
28 NMRST
29 DASPST
30 VDD
31 OSCO2
32 OSCI2
33 UATASEL
34 VSS
35 PVSSDRAM
36 PVDDDRAM

MN103S13BDA

Right pins (108–73):
108 SBCK
107 VSS
106 P0
105 P1
104 PVDD
103 PVSS
102 VDD
101 OSCO1
100 OSCI1
99 VSS
98 LRCK
97 BLKCK
96 IPFLAG
95 DACCLK
94 DACLRCK
93 DACDATA
92 NTRON
91 LG
90 JMPINH
89 IDHOLD
88 SBCK/PLLOK
87 CLKOUT2
86 VDD
85 NRST
84 MMOD
83 VSS
82 CPDET1
81 CPDET2
80 BDO
79 IDGT
78 DTRD
77 TEHLD
76 VDD
75 CLKOUT1
74 CPUDT0
73 CPUDT1

Bottom pins (37–72, left to right):
CPUADR17, CPUADR16, VSS, CPUADR15, CPUADR14, CPUADR13, CPUADR12, VDD, CPUADR11, CPUADR10, CPUADR9, CPUADR8, CPUADR7, CPUADR6, CPUADR5, CPUADR4, CPUADR3, CPUADR2, CPUADR1, VSS, CPUADR0, NCS, NWR, NRD, VDD, CPUDT7, CPUDT6, PVPPDRAM, PTESTDRAM, PVDDDRAM, PVSSDRAM, CPUDT5, CPUDT4, CPUDT3, VSS, CPUDT2

2. Block diagram

DVD-ROM Formatter, CD-PRE, Formatter i/t, ECC, Host i/f MPEG i/t, ATAPI

High speed IO bus

CGEN, Instruction memory (40KB), 32 bit CPU core, DMA, BCU, DRAMC, 4Mbit DRAM

MODE, DATA MEMORY (6KB), GCAL

General purpose IO bus

WDT, 16 bit timer x 2, SYSTEM i/f, INTC

3.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	HDD15	I/O	ATAPI data	73	CPUDT1	I/O	System control data
2	HDD0	I/O	ATAPI data	74	CPUDT0	I/O	System control data
3	HDD14	I/O	ATAPI data	75	CLKOUT1	O	16.9/11.2/8.45MHz clock
4	VDD	-	Power supply (3V)	76	VDD	-	Power supply (3V)
5	HDD1	I/O	ATAPI data	77	TEHLD	O	Mirror gate (Connect with TP141)
6	HDD13	I/O	ATAPI data	78	DTRD	O	Frequency control switch for data (Connect with TP304)
7	HDD2	I/O	ATAPI data	79	IDGT	O	Part CAPA switch
8	VSS	-	GND	80	BDO	I	RF dropout / BCA data
9	HDD12	I/O	ATAPI data	81	CPDET2	I	Outer side CAPA detection
10	VDD	-	Power supply (2.7V)	82	CPDET1	I	Inner side CAPA detection
11	HDD3	I/O	ATAPI data	83	VSS	-	GND
12	HDD11	I/O	ATAPI data	84	MMOD	I	Connect with VSS
13	HDD4	I/O	ATAPI data	85	NRST	I	System reset
14	HDD10	I/O	ATAPI data	86	VDD	-	Power supply (3V)
15	VDD	-	Power supply (3V)	87	CLKOUT2	O	16.9MHz clock
16	HDD5	I/O	ATAPI data	88	SBCK/PLLOK	O	Frame mark detection
17	HDD9	I/O	ATAPI data	89	IDOHOLD	O	ID gate for holding tracking
18	VSS	-	GND	90	JMPINH	O	Jump prohibition
19	HDD6	I/O	ATAPI data	91	LG	O	Land / group switch
20	HDD8	I/O	ATAPI data	92	NTRON	I	Tracking ON
21	HDD7	I/O	ATAPI data	93	DACDATA	O	Serial output
22	VDDH			94	DACLRCK	O	L and R identification output
23	NRESET	I	ATAPI reset	95	DACCLK	I	Clock for serial output
24	MASTER	I/O	ATAPI master / slave selection	96	IPFLAG	I	IP flag input
25	NINT0	O	System control interruption 0	97	BLKCK	I	Clock for sub-code and block input
26	NINT1	O	System control interruption 1	98	LRCK	I	L and R identification signal output
27	WAITDOC	O	System control wait control	99	VSS	-	GND
28	NMRST	O	System control reset (Connect with TP302)	100	OSCI1	I	16.9MHz oscillation
29	DASPST	I	DASP signal initializing	101	OSCO1	O	16.9MHz oscillation
30	VDD	-	Power supply (3V)	102	VDD	-	Power supply (3V)
31	OSCO2	O	Not used (Connect with TP140)	103	PVSS	-	GND
32	OSCI2	I	Not used (Connect with TP303)	104	PVDD	-	Power supply (3V)
33	UATASEL	I	VSS connection	105	P1	I/O	Terminal MASTER polarity switch input
34	VSS	-	GND	106	P0	I/O	CIRC-RAM OVER/UNDER Interruption signal input
35	PVSSDRAM		VSS connection	107	VSS	-	GND
36	PVDDDRAM		Connect with 2.7V VDD	108	SBCK	O	Sub-code and Clock output for serial input
37	CPUADR17	I	System control address	109	SUBC	I	Sub-code and serial input
38	CPUADR18	I	System control address	110	NCLDCK	I	Sub-code and Frame clock input
39	VSS	-	GND	111	CHCK40	I	Read clock to DAT3~0 (Output of dividing frequency four from ADSC)
40	CPUADR15	I	System control address	112	DAT3	I	Read data from DISC (Parallel output from ADSC)
41	CPUADR14	I	System control address	113	DAT2	I	Read data from DISC (Parallel output from ADSC)
42	CPUADR13	I	System control address	114	DAT1	I	Read data from DISC (Parallel output from ADSC)
43	CPUADR12	I	System control address	115	DAT0	I	Read data from DISC (Parallel output from ADSC)
44	VDD	-	Power supply (2.7V)	116	VDD	-	Power supply (3V)
45	CPUADR11	I	System control address	117	SCLOCK	I/O	Debugging serial clock (270 Ω pull up)
46	CPUADR10	I	System control address	118	SDATA	I/O	Debugging serial data (270 Ω pull up)
47	CPUADR9	I	System control address	119	MONI3	O	Internal goods title monitor (Connect to TP150)
48	CPUADR8	I	System control address	120	MONI2	O	Internal goods title monitor (Connect to TP151)
49	CPUADR7	I	System control address	121	MONI1	O	Internal goods title monitor (Connect to TP152)
50	CPUADR6	I	System control address	122	MONI0	O	Internal goods title monitor (Connect to TP153)
51	CPUADR5	I	System control address	123	VSS	-	GND
52	CPUADR4	I	System control address	124	NEJECT	I	Eject detection
53	CPUADR3	I	System control address	125	VDD	-	Power supply (2.7V)
54	CPUADR2	I	System control address	126	NTRYCL	I	Tray close detection
55	CPUADR1	I	System control address	127	NDASP	I/O	ATAPI Drive active/Slave connection I/O
56	VSS	-	GND	128	NCS3FX	I	Not used (ATAPI host chip selection)
57	CPUADR0	I	System control address	129	NCS1FX	I	Not used (ATAPI host chip selection)
58	NCS	I	System control chip selection	130	VDD	-	Power supply (3V)
59	NWR	I	System control write	131	DA2	I/O	ATAPI host address
60	NRD	I	System control read	132	DA0	I/O	Not used (ATAPI host address)
61	VDD	-	Power supply (3V)	133	NPDIAG	I/O	ATAPI slave/master diagnosis input
62	CPUDT7	I/O	System control data	134	VSS	-	GND
63	CPUDT6	I/O	System control data	135	DA1	I/O	Not used (ATAPI host address)
64	PVPPDRAM	O	Connect with VSS	136	NIOCS16	O	ATAPI output for selecting width of host data bus
65	PTESTDRAM	I	Connect with VSS	137	INTRQ	O	ATAPI host interruption output
66	PVDDDRAM		Connect with VDD (2.7V)	138	VDD	-	Power supply (3V)
67	PVSSDRAM		Connect with VSS	139	NDMACK	I	Not used (ATAPI host DMA response)
68	CPUDT5	I/O	System control data	140	IORDY	O	ATAPI host ready output (Connect to TP157)
69	CPUDT4	I/O	System control data	141	NIORD	I	Not used (ATAPI host read)
70	CPUDT3	I/O	System control data	142	VSS	-	GND
71	VSS	-	GND	143	NIOWR	I/O	ATAPI host writes
72	CPUDT2	I/O	System control data	144	DMARQ	O	ATAPI host DMA demand (Connect to TP159)

■ MN67706ZY(IC201) : ADSC

1.Pin layout

MN67706ZY
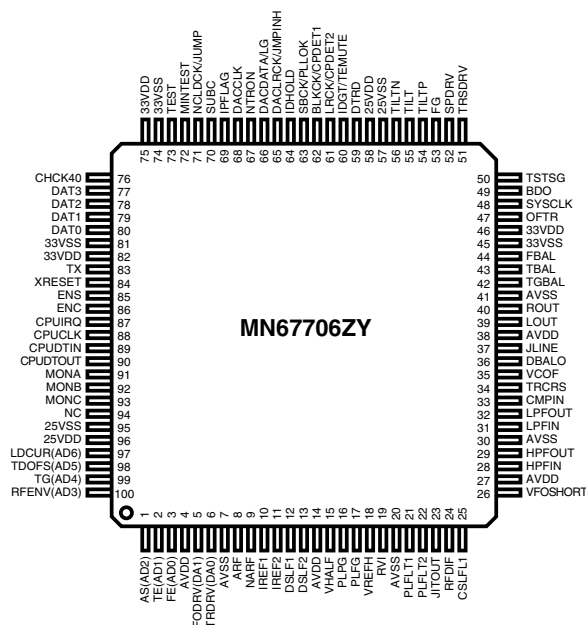
2.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	AS(AD2)	I	AS : All added signal (FEP)	51	TRSDRV	O	Traverse drive (DRVIC)
2	TE(AD1)	I	Tracking error (FEP)	52	SPDRV	O	Spindle drive output (DRVIC)
3	FE(AD0)	I	Focus error (FEP)	53	FG	I	FG signal input (spindle motor driver)
4	AVDD	-	Power supply for analog circuit (3.3V)	54	TILTP	O	Connect with TP205
5	FODRV(DA1)	O	Focus drive (DRVIC)	55	TILT	O	Connect with TP206
6	TRDRV(DA0)	O	Tracking drive (DRVIC)	56	TILTN	O	Connect with TP207
7	AVSS	-	Ground for analog circuit	57	25VSS	-	For internal core GND
8	ARF	I	Equalized RF+(FEP)	58	25VDD	-	Power supply for internal core (2.5V)
9	NARF	I	Equalized RF–(FEP)	59	DTRD	I	Data read control signal (ODC)
10	IREF1	I	Reference power supply 1 for DBAL	60	IDGT/TEMUTE	I	Pull down for GND
11	IREF2	I	Reference power supply 2 for DBAL	61	LRCK/CPDET2	O	LR channel data strobe (ODC)/
12	DSLF1	I/O	Capacitor 1 for DSL	62	BLKCK/CPDET1	O	CD sub code synchronize signal (ODC)/
13	DSLF2	I/O	Capacitor 2 for DSL	63	SBCK/PLLOK	I	CD sub-code data shift clock (ODC)/SYNC detection
14	AVDD	-	Power supply for analog circuit (3.3V)	64	IDHOLD	I	Pull down for GND
15	VHALF	I	Reference voltage 1.65±0.1V(FEP)	65	DACLRCK/JMPINH	I	1 bit DAC-LR channel data strobe (ODC)/
16	PLPG	-	Not used	66	DACDATA/LG	I	CD1 bit DAC channel data (ODC)
17	PLFG	-	Not used	67	NTRON	O	L:tracking ON (ODC)
18	VREFH	I	Reference voltage 2.2V±0.1V(FEP)	68	DACCLK	O	1 bit DAC channel data shift clock (ODC)
19	RVI	I/O	VREFH reference power supply for resistor	69	IPFLAG	O	CIRC error flag (ODC)
20	AVSS	-	Ground for analog circuit	70	SUBC	O	CD sub code (ODC)
21	PLFLT1	O	Capacitor 1 for PLL	71	NCLDCK/JUMP	O	CD sub code data frame clock (ODC)/DVD JUMP signal (ODC)
22	PLFLT2	O	Capacitor 2 for PLL	72	MINTEST	I	Connects with DVSS (for MINTEST)
23	JITOUT	I/O	Detection signal output of jitter	73	TEST	I	Connects with DVSS (for TEST)
24	RFDIF	I	Not used	74	33VSS	-	For I/O GND
25	CSLFL1	I/O	Pull up for VHALF	75	33VDD	-	Power supply for I/O (3.3V)
26	VFOSHORT	O	VFO short output	76	CHCK40	O	For SRDATA clock (ODC)
27	AVDD	-	Power supply for analog circuit (3.3V)	77	DAT3	O	SRDATA3(ODC)
28	HPFIN	I	Pull up for VHALF	78	DAT2	O	SRDATA2(ODC)
29	HPFOUT	O	Connect woth TP208	79	DAT1	O	SRDATA1(ODC)
30	AVSS	-	Ground for analog circuit	80	DAT0	O	SRDATA0(ODC)
31	LPFIN	I	Pull up for VHALF	81	33VSS	-	For I/O GND
32	LPFOUT	O	Not used	82	33VDD	-	Power supply for I/O (3.3V)
33	CMPIN	I	Connect with TP210	83	TX	O	Digital audio interface
34	TRCRS	I	Track crossing signal (FEP)	84	XRESET	I	Reset L : Reset
35	VCOF	I/O	JFVCO control voltage	85	ENS	I	Servo DSC sereal I/F chip select (SYSCON)
36	DBALO	O	DSL balance adjustment output	86	ENC	I	CIRC sereal I/F chip select (SYSCON)
37	JLINE	O	J-line preset output (FEP)	87	CPUIRQ	O	Interrupt request to silicon (SYSCON)
38	AVDD	-	Power supply for analog circuit (3.3V)	88	CPUCLK	I	Silicon cereal I/F clock (SYSCON)
39	LOUT	O	Connect with TP203 (analog audio L out)	89	CPUDTIN	I	Silicon cereal I/F data input (SYSCON)
40	ROUT	O	Connect with TP204 (analog audio R out)	90	CPUDTOUT	O	Silicon cereal I/F data output (SYSCON)
41	AVSS	-	Ground for analog circuit	91	MONA	O	Monitor terminal A (connect with TP226)
42	TGBAL	O	Tangential balance (FEP)	92	MONB	O	Monitor terminal B (connect with TP225)
43	TBAL	O	Tracking balance (FEP)	93	MONC	O	Monitor terminal C (connect with TP224)
44	FBAL	O	Focus balance (FEP)	94	NC	O	Not used (connect with TP211)
45	33VSS	-	For I/O GND	95	25VSS	-	For internal core GND
46	33VDD	-	Power supply for I/O (3.3V)	96	25VDD	-	Power supply for internal core (2.5V)
47	OFTR	I	Off-track error signal (FEP)	97	LDCUR(AD6)	I	
48	SYSCLK	I	16.9344MHz system clock input (ODC)	98	TDOFS(AD5)	I	
49	BDO	I	BDO + BCA (FEP)	99	TG(AD4)	I	Tangential Phase difference (FEP)
50	TSTSG	O	Self calibration signal (FEP)	100	RFENV(AD3)	I	RFENV (FEP)

■ MSM531622F91G-X(IC402) : 1M x 16Bit/2M x 8Bit change enable ROM

1.Pin layout

```
           NC  1        44  NC
          A18  2        43  A19
          A17  3        42  A8
           A7  4        41  A9
           A6  5        40  A10
           A5  6        39  A11
           A4  7        38  A12
           A3  8        37  A13
           A2  9        36  A14
           A1 10        35  A15
           A0 11        34  A16
           CE 12        33  BYTE
          Vss 13        32  Vss
           OE 14        31  D15/A-1
           D0 15        30  D7
           D8 16        29  D14
           D1 17        28  D6
           D9 18        27  D13
           D2 19        26  D5
          D10 20        25  D12
           D3 21        24  D4
          D11 22        23  Vcc
```
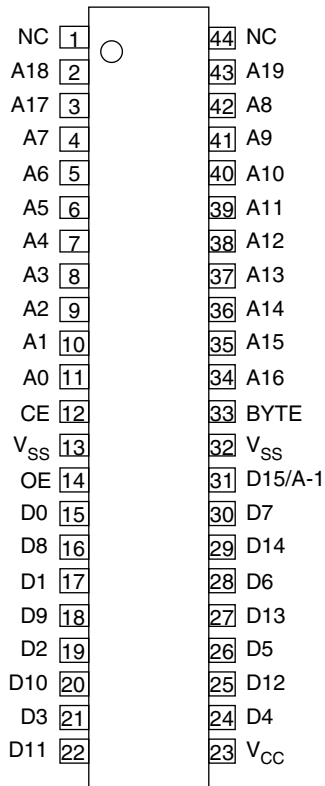
44 pin SOP

3.Pin function

Symbol	Function
D15/A-1	Address input (For 8bit output)
A0~A19	Address input
D0~D15	Data output
$\overline{CE}$	Chip enable
$\overline{OE}$	Chip enable
$\overline{BYTE}$	Output 16/8bit select L : 8bit output + H : 16bit output
V_{CC}, V_{SS}	Power supply
NC	No connection

2.Block diagram
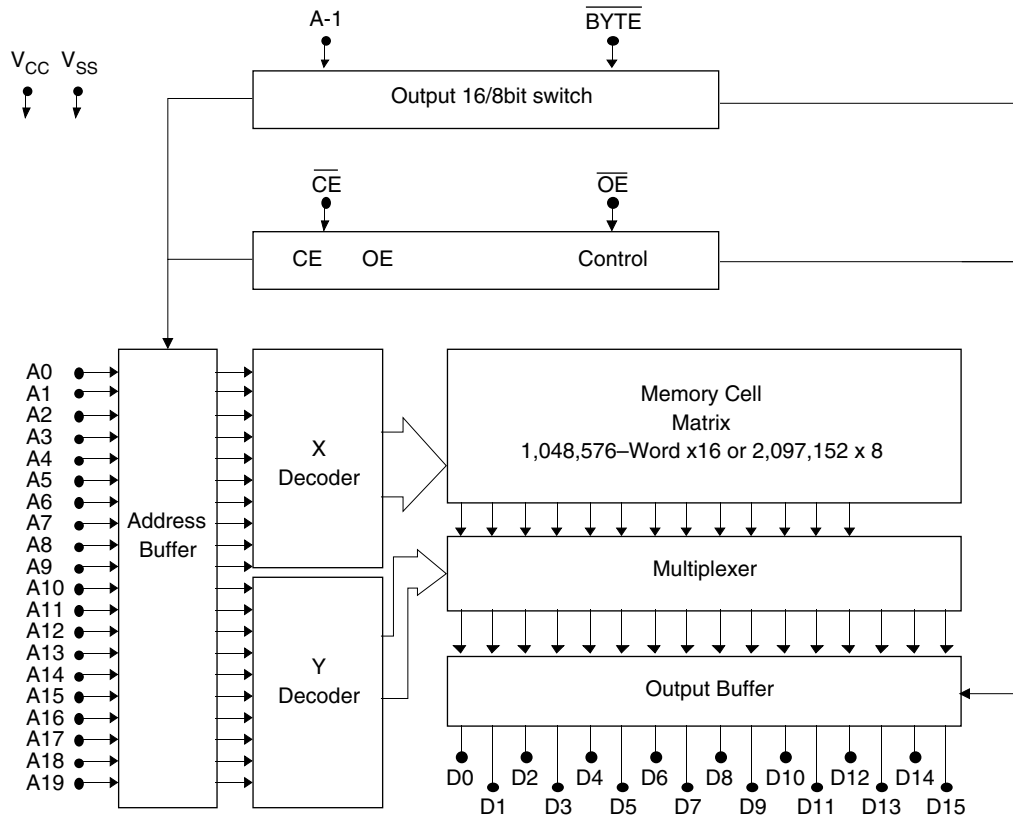
■ RN5RZ33BA-X(IC1, IC102) : High cycle module

1.Terminal layout

```
   CE        NC
   ┌5┐      ┌4┐
  ┌─────────────┐
  │             │
  └─────────────┘
   └1┘ └2┘ └3┘
  GND VDD VOUT
```
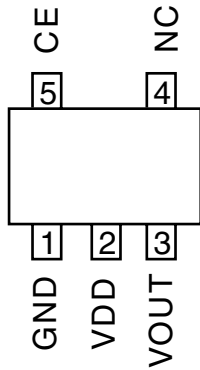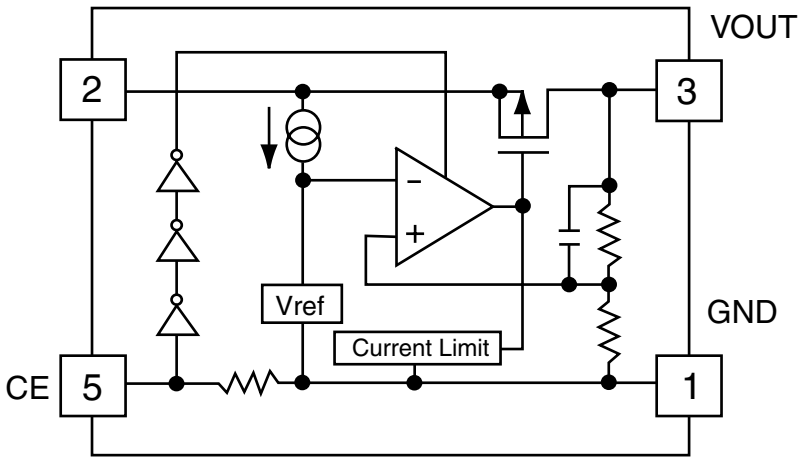
2.Block diagram

3.Pin function

Pin No.	Pin name	Function
1	GND	Ground terminal
2	VDD	Input terminal
3	VOUT	Output terminal
4	NC	No connection
5	CE	Chip enable terminal

■ STK404-130(IC105) : Power amp

1.Terminal layout
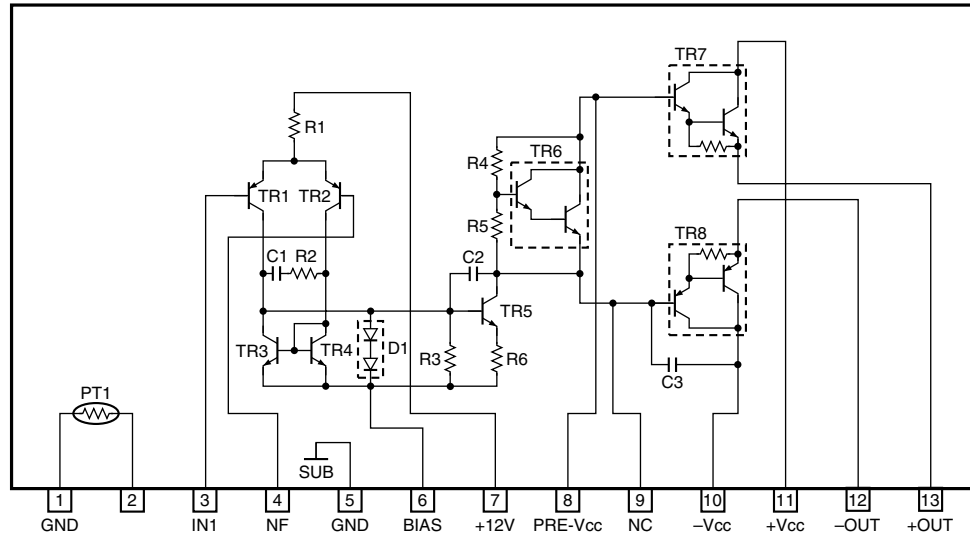
2.Block diagram

■ STK402-230(IC107) : Power amp

1. Terminal layout
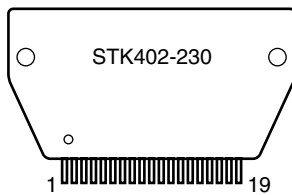
2.Block daiagram
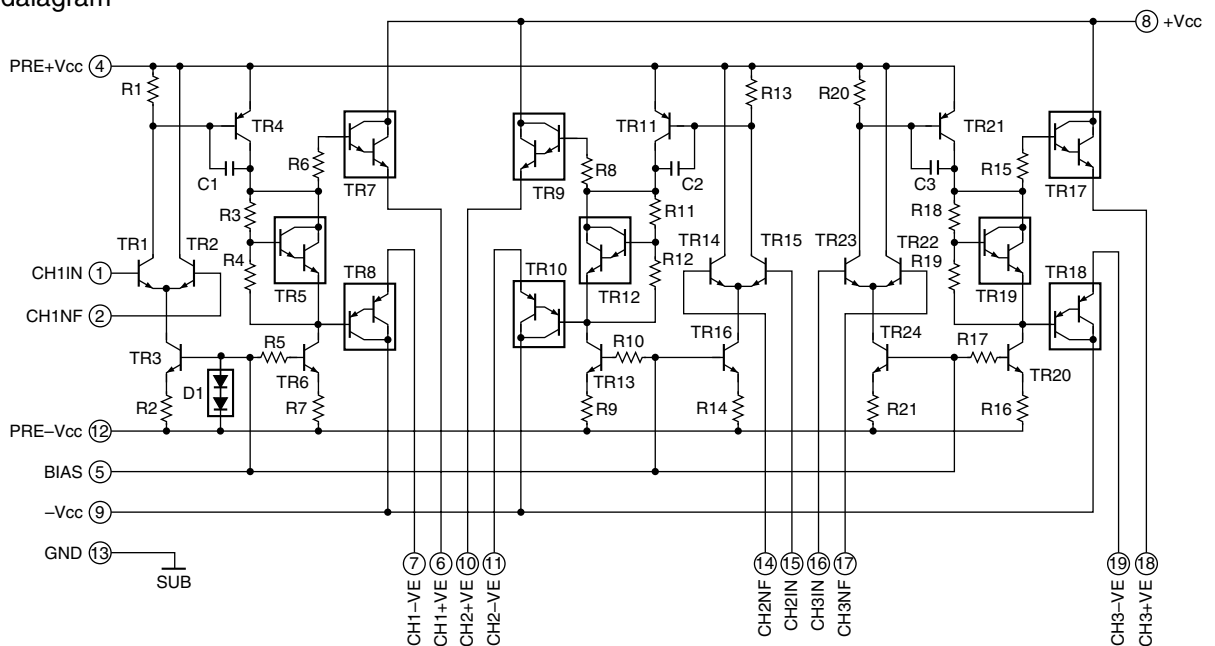
■ TC74VHC00FT-X(IC322,IC503)
: Write timing control

1.Pin layout /Block diagram

Vcc	4B	4A	4Y	3B	3A	3Y
14	13	12	11	10	9	8

1	2	3	4	5	6	7
1A	1B	1Y	2A	2B	2Y	GND
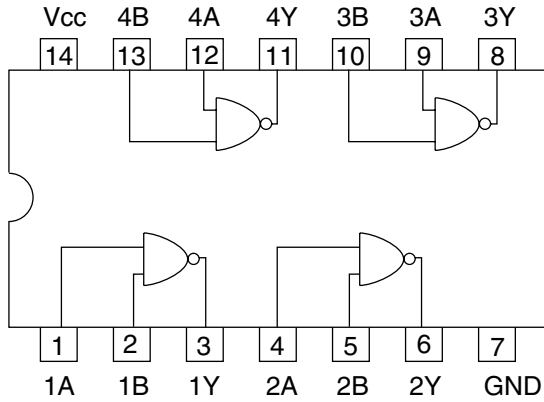
■ TC7WH74FU-X(IC321) : Clock buffer

1.Terminal layout

CK	1	8	VCC
D	2	7	$\overline{PR}$
$\overline{Q}$	3	6	$\overline{CLR}$
GND	4	5	Q
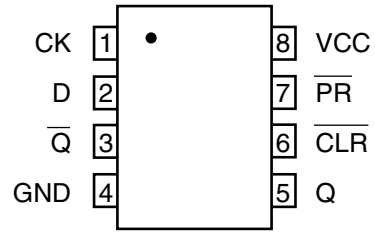
■ TC7SH32FU-X(IC312)
: Timing control

1.Terminal layout

IN B	1	5	VCC
IN A	2		
GND	3	4	OUT Y
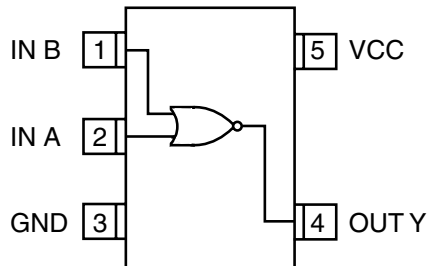
■ TC7SH08FU-X(IC311) : Timing control

1.Terminal layout

IN B	1	5	VCC
IN A	2		
GND	3	4	OUT Y
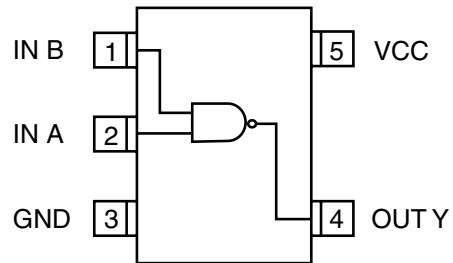
■ TC7W125FU-X(IC202) : Buffer

1.Terminal layout
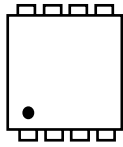
2.Block diagram

■ BA15218N(IC104,IC108,IC109,IC110) : OP AMP

1.Pin layout / Block diagram

■ ZIVA3-PE0 (IC501) : AV Decoder

1. Terminal Description

ZIVA3-PEO (1/5)

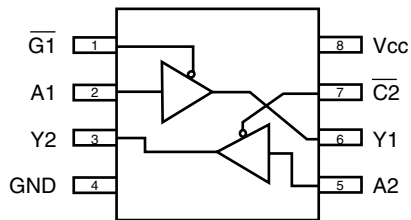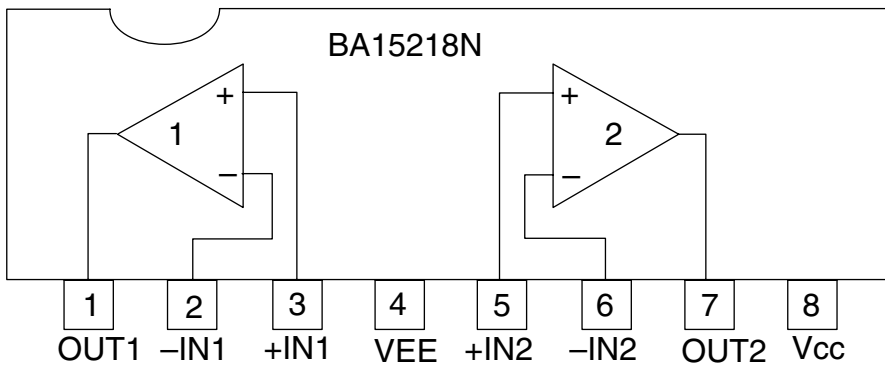| Pin No.	Symbol	I/O	Function
1	PIO0	I/O	Programmable I/O pin, which enters input mode after resetting.
2	HDATA0		8-bit, bi-directional host data bus. Write data in decoder Code FIFO via HDATA.
3	HDATA1	I/O	The 32-bit word MSB is written first. The host reads and writes the internal register of
4	HDATA2		the decoder and local SRAM via HDATA.
5	VDD-3.3	-	3.3 V supply voltage for I/O signals.
6	HDATA3	I/O	8-bit, bi-directional host data bus. Writes data in decoder Code FIFO via HDATA. The 32-bit word MSB is written first. The host reads and writes the internal register of the decoder and local SRAM via HDATA.
7	VSS	-	Core logic and I/O signal grounding.
8	HDATA4		8-bit, bi-directional host data bus. Write data in decoder Code FIFO via HDATA.
9	HDATA5		The 32-bit word MSB is written first. The host reads and writes the internal register of
10	HDATA6	I/O	the decoder and local SRAM via HDATA.
11	HDATA7		
12	VDD-2.5	-	2.5 V supply voltage for the core logic.
13	$\overline{\text{RESET}}$	I	Hardware reset. An external device expresses $\overline{\text{RESET}}$ (Active Low) to execute hardware resetting of the decoder. RESET is expressed for at least 20 ms to guarantee optimum initialization to occur after power has stabilized.
14	VSS	-	Core logic and I/O signal grounding.
15	$\overline{\text{WAIT}}/\overline{\text{DTACK}}$	O	Transfer incomplete/data acknowledgement, which is an Active Low signal indicating that transfer started by the host is not completed. $\overline{\text{WAIT}}$ is expressed after negative going edge of $\overline{\text{CS}}$, and expressed again when the decoder is ready for completing the transfer cycle. As the signal for opening the drain should be pulled up from 1 V to 3.3 V, it is driven at high speed for 10 ns before the tri-state condition is entered.
16	$\overline{\text{INT}}$	O	Host interrupt. As the signal for opening the drain should be pulled up from 4.7 V to 3.3 V, it is driven at high speed for 10 ns before the tri-state condition is entered.
17	VDD-3.3	-	3.3 V supply voltage for I/O signals.
18	NC	O	No connection.
19	VSS	-	Core logic and I/O signal grounding.
20	NC	O	No connection.
21	PIO11		
22	PIO12		
23	PIO13		
24	PIO14	I/O	Programmable I/O pins, which enter input mode. after resetting.
25	PIO15		
26	PIO16		
27	VDD-3.3	-	3.3 V supply voltage for I/O signals.
28	PIO17	I/O	Programmable I/O pin, which enters input mode after resetting.
29	VSS	-	Core logic and I/O signal grounding.
30	PIO18	I/O	Programmable I/O pin, which enters input mode after
31	PIO19		
32	PIO20		
33	PIO21	I/O	Programmable I/O pins, which enter output mode after resetting.
34	PIO22		
35	PIO23		
36	VDD-3.3	-	3.3 V supply voltage for I/O signals.
37	PIO24	I/O	Programmable I/O pin, which enters output mode after resetting.
38	VSS	-	Core logic and I/O signal grounding.
39	PIO25	I/O	Programmable I/O pin, which enters output mode after resetting.
40	VDD-2.5	-	2.5 V supply voltage for the core logic.
41	PIO26	I/O	Programmable I/O pin, which enters output mode after resetting.
42	VSS	-	Core logic and I/O signal grounding.

Pin No.	Symbol	I/O	Function
44	PIO28		
45	PIO29	I/O	Programmable I/O pins, which enter output mode after resetting.
46	PIO30		
47	VDD-3.3	-	3.3 V supply voltage for I/O signals.
48	PIO31	I/O	Programmable I/O pin, which enters output mode after resetting.
49	VSS	-	Core logic and I/O signal grounding.
50	NC	O	No connection.
51			
52	PIO1	I/O	Programmable I/O pin, which enters input mode after resetting.
53	MDATA15	I/O	Memory data.
54	MDATA0	I/O	Memory data.
55	VDD-3.3	-	3.3 V supply voltage for I/O signals.
56	MDATA14	I/O	Memory data.
57	VSS	-	Core logic and I/O signal grounding.
58	MDATA1		
59	MDATA13	I/O	Memory data.
60	MDATA2		
61	VDD-3.3	-	3.3 V supply voltage for I/O signals.
62	MDATA12	I/O	Memory data.
63	VSS	-	Core logic and I/O signal grounding.
64	MDATA3	I/O	Memory data.
65	VDD-2.5	-	2.5 V supply voltage for the core logic.
66	MDATA11	I/O	Memory data.
67	VSS	-	Core logic and I/O signal grounding
68	MDATA4	I/O	Memory data.
69	VDD-3.3	-	3.3 V supply voltage for I/O signals.
70	MDATA10	I/O	Memory data.
71	VSS	-	Core logic and I/O signal grounding.
72	MDATA5		
73	MDATA9	I/O	Memory data.
74	MDATA6		
75	VDD-3.3	-	3.3 V supply voltage for I/O signals.
76	MDATA8	I/O	Memory data.
77	VSS	-	Core logic and I/O signal grounding.
78	MDATA7	I/O	Memory data.
79	LDQM	O	SDRAM LDQM.
80	UDQM	O	SDRAM UDQM.
81	VDD-3.3	-	3.3 V supply voltage for I/O signals.
82	$\overline{\text{MWE}}$	O	SDRAM write enable. The decoder expresses Active Low to request write operation of the SDRAM array.
83	VSS	-	Core logic and I/O signal grounding.
84	SD-CLK	O	SDRAM system clock.
85	$\overline{\text{SD-CAS}}$	O	Active Low, SDRAM column address.
86	$\overline{\text{SD-RAS}}$	O	Active Low, SDRAM row address.
87	VDD-3.3	-	3.3 V supply voltage for I/O signals.
88	$\overline{\text{SD-CS1}}$	O	Active Low SDRAM bank selection.
89	VSS	-	Core logic and I/O signal grounding.
90	SD-CS0	O	Active Low SDRAM bank selection.
91	VDD-2.5	-	2.5 V supply voltage for the core logic.
92	NC	O	No connection.
93	VSS	-	Core logic and I/O signal grounding.
94	NC	O	No connection.
95	VDD-3.3	-	3.3 V supply voltage for I/O signals.
96	MADDR9	O	Memory address.
97	VSS	-	Core logic and I/O signal grounding.
98	MADDR11	O	Memory address.

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Pin No.	Symbol	I/O	Function
99	MADDR8	O	Memory address.
100	MADDR10		
101	VDD-3.3	-	3.3 V supply voltage for I/O signals.
102	MADDR7	O	Memory address.
103	VSS	-	Core logic and I/O signal grounding.
104	MADDR0		
105	MADDR6	O	Memory address.
106	MADDR1		
107	VDD-3.3	-	3.3 V supply voltage for I/O signals.
108	MADDR5	O	Memory address.
109	VSS	-	Core logic and I/O signal grounding.
110	MADDR2		
111	MADDR4	O	Memory address.
112	MADDR3		
113	VDD-3.3	-	3.3 V supply voltage for I/O signals.
114	NC	O	No connection.
115	VSS	-	Core logic and I/O signal grounding.
116	NC	O	No connection.
117	VDD-2.5	-	2.5 V supply voltage for the core logic.
118	NC	O	No connection.
119	VSS	-	Core logic and I/O signal grounding.
120			
121	NC	O	No connection.
122			
123	VDD-3.3	-	3.3 V supply voltage for I/O signals.
124	NC	O	No connection.
125	VSS	-	Core logic and I/O signal grounding.
126	NC	O	No connection.
127			
128	RESERVED	O	The signal for opening the drain should be pulled up from 4.7 V to 3.3 V.
129	PIO2	I/O	Programmable I/O pin. Enters input mode after resetting.
130	NC	O	No connection.
131	RESERVED	I	Coupled with VSS or VDD-3.3.
132			
133	PIO3	I/O	Programmable I/O pin, which enters input mode after resetting
134	VDD-3.3	-	3.3 V supply voltage for I/O signals.
135	RESERVED	I	Coupled with VSS or VDD-3.3.
136	VSS	-	Core logic and I/O signal grounding.
137	RESERVED	I	Coupled with VSS or VDD-3.3.
138	PIO4	I/O	Programmable I/O pin, which enters input mode after resetting.
139	RESERVED	I	Coupled with VSS or VDD-3.3.
140			
141	PIO5	I/O	Programmable I/O pin, which enters input mode after resetting.
142	VDATA0	O	Video data bus for byte-serial CbYCrY data in sync with VCLK. In power up, the decoder
143	VDATA1		does not drive VDATA. In boot-up, the decoder uses the configuration parameters for drive or tri-state VDATA.
144	VDD-2.5	-	2.5 V supply voltage for the core logic.
145	VDATA2	O	Video data bus for byte-serial CbYCrY data in sync with VCLK. In power up, the decoder does not drive VDATA. In boot-up, the decoder uses the configuration parameters for drive or tri-state VDATA.
146	VSS	-	Core logic and I/O signal grounding.
147	PIO6	I/O	Programmable I/O pin, which enters input mode after resetting.
148	VDATA3	O	Video data bus for byte-serial CbYCrY data in sync with VCLK. In power up, the decoder does not drive VDATA. In boot-up, the decoder uses the configuration parameters for drive or tri-state VDATA.

Pin No.	Symbol	I/O	Function
149	VDD-3.3	-	3.3 V supply voltage for I/O signals.
150	VDATA4	O	Video data bus for byte-serial CbYCrY data. In power up, the decoder does not drive VDATA. In boot-up, the decoder uses the operation configuration parameters or tri-state VDATA.
151	VSS	-	Core logic and I/O signal grounding.
152	VDATA5	O	Video data bus for byte-serial CbYCrY data. In power up, the decoder does not drive VDATA. In boot-up, the decoder uses the operation configuration parameters or tri-state VDATA.
153	PIO7	I/O	Programmable I/O pin, which enters input mode after resetting.
154	VDATA6	O	Video data bus for byte-serial CbYCrY data.
155	VDATA7		In power up, the decoder does not drive VDATA. In boot-up, the decoder uses the operation configuration parameters or tri-state VDATA.
156	PIO8	I/O	Programmable I/O pin, which enters input mode after resetting.
157	$\overline{HSYNC}$	I/O	Horizontal sync. After the negative-going edge of $\overline{VSYNC}$, the decoder starts pixel data output for the new horizontal line.
158	$\overline{VSYNC}$	I/O	Vertical sync, which is bi-directional. After the negative-going edge of $\overline{VSYNC}$, the decoder outputs the highest border of the new field for the first $\overline{SYNC}$. $\overline{VSYNC}$ can receive either V sync or upper/lower field notification from an external source.
159	DA-IEC	O	ICE-1937 bitstream output or IEO-958 format PCM data output.
160	VDD-3.3	-	3.3 V supply voltage for I/O signals.
161	DA-DATA0	O	PCM data output in 8 channels. Serial audio sample relative to the DA-BCK clock.
162	VSS	-	Core logic and I/O signal grounding.
163	DA-DATA1	O	PCM data output in 8 channels.
164	DA-DATA2		Serial audio sample relative to the DA-BCK clock.
165	DA-DATA3		
166	DA-LRCK	O	PCM left/right clock. Identifies the channel for each audio sample. The polarity is programmable.
167	DA-BCK	O	PCM bit clock. Obtained by dividing DA-XCK by 8. DA-BCK takes a value of 48 or 32 times the sampling clock.
168	VDD-2.5	-	2.5 V supply voltage for the core logic.
169	DA-XCK	I/O	Audio master frequency clock, which is used to generate DA-BCK and DALRCK. DA-XCK takes a value of 384 or 256 times the sampling frequency.
170	VSS	-	Core logic and I/O signal grounding.
171	DAI-DATA	I	PCM input data with 2 channels. Serial audio sample relative to the DA-BCK clock.
172	DAI-LRCK	I	PCM input left/right clock.
173	DAI-BCK	I	PCM input bit clock.
174	PIO9	I/O	Programmable I/O pin, which enters input mode after resetting.
175	CLKSEL	I	Input selection: Internal = VDD. External = VSS.
176	A-VDD	-	3.3 V analog supply voltage.
177	VCLK	I	Video clock. Data is recorded at input.
178	SYSCLK	I	System clock. The decoder requires an external 27 MHz TTL oscillator. Same drive frequency as the VCK of 27 MHz.
179	A-VSS	-	Analog grounding of the PLL.
180	DVD-DATA0 /CD-DATA	I	Serial CD data. This pin is also used as a DVD compression data pin DVD-DATA0.
181	VDD-3.3	-	3.3 V supply voltage for I/O signals.
182	DVD-DATA1 /CD-LRCK	I	16-bit word sync with programmable polarity for the decoder (right channel High). This pin is also used as a DVD compression data pin DVD-DATA1.
183	VSS	-	Core logic and I/O signal grounding.
184	DVD-DATA2 /CD-BCK	I	CD bit clock. The decoder accepts multiple BCK rates. This pin is also used as a DVD compression data pin DVD-DATA2.
185	DVD-DATA3 /CD-C2PO	I	Performs High expression by indicating the damaged byte. The decoder holds the effective pixels in the last image until the next effective image is decoded. DVD compression data pin DVD-DATA3.

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Pin No.	Symbol	I/O	Function
186	DVD-DATA7	I	DVD parallel compression data from the DVD DSP. When the DVD DSP transmits a 32-bit
187	/CDG-SCLK		word, it should first describe the WSB.
188	DVD-DATA6		CDG-SDTA: CD+G (subcode) data, which indicates a serial subcode data input.
189	/CDG-SOS1		CDG-VSFY: CD+G (subcode) frame sync, which indicates the start of a frame or a
	DVD-DATA5		composite sync input.
	/CDG-VFSY		CDG-SOS1: CD+G (subcode) block sync, which indicates a block start sync input.
	DVD-DATA4		CDG-SCLK: CD+G (subcode) clock, which indicates the input or output of the subcode
	/CDG-SDATA		data clock.
190	PIO10	I/O	Programmable I/O pin, which enters the input mode after resetting.
191	VREQUEST	O	Video request. The decoder expresses VREQUEST to indicate that the video input buffer has available space. The polarity is programmable.
192	VSTROBE	I	Video strobe, which is a programmable, dual-mode pulse and either async or sync. In the async mode, the external source sends VSTROBE to indicate that it is ready for data transfer. In the sync mode, the signal becomes the VSTROBE clock data.
193	VDD-3.3	-	3.3 V supply voltage for I/O signals.
194	NC	O	No connection.
195	VSS	-	Core logic and I/O signal grounding.
196	V-DACK	I	Video data acknowledgement in the case of the sync mode. Expressed when the DVD data is valid. The polarity is programmable.
197	VDD-2.5	-	2.5 V supply voltage for the core logic.
198	RESERVED	I	Coupled with VSS or VDD-3.3.
199	VSS	-	Core logic and I/O signal grounding.
200	ERROR	I	Input data error. If the ERROR signal from the DSP is unusable, grounding should be performed.
201	HOST8SEL	I	Permanently coupled with VDD-3.3.
202	HADDR0		Host address bus. This 3-bit address bus selects one of the six hosts interface registers.
203	HADDR1	I	
204	HADDR2		
205	DTACKSEL	I	Coupled with High to select the $\overline{\text{WAIT}}$ signal or with Low to select the $\overline{\text{DTACK}}$ signal. (Motorola 68K mode)
206	$\overline{\text{CS}}$	I	Host chip selection. The host expresses CS to select the decoder for use in read/write. The read or write operation starts at the negative-going edge of this signal.
207	R/$\overline{\text{W}}$	I	Performs strobe read/write in the M mode and strobe write in the I mode. The host expresses R/$\overline{\text{W}}$ LOW to select write or LOW to select read.
208	$\overline{\text{RD}}$	I	Performs strobe read in the I mode. Should be kept HIGH in the M mode.

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