COMPACT DISC PLAYER

DP-48

SERVICE MANUAL

KENWOOD

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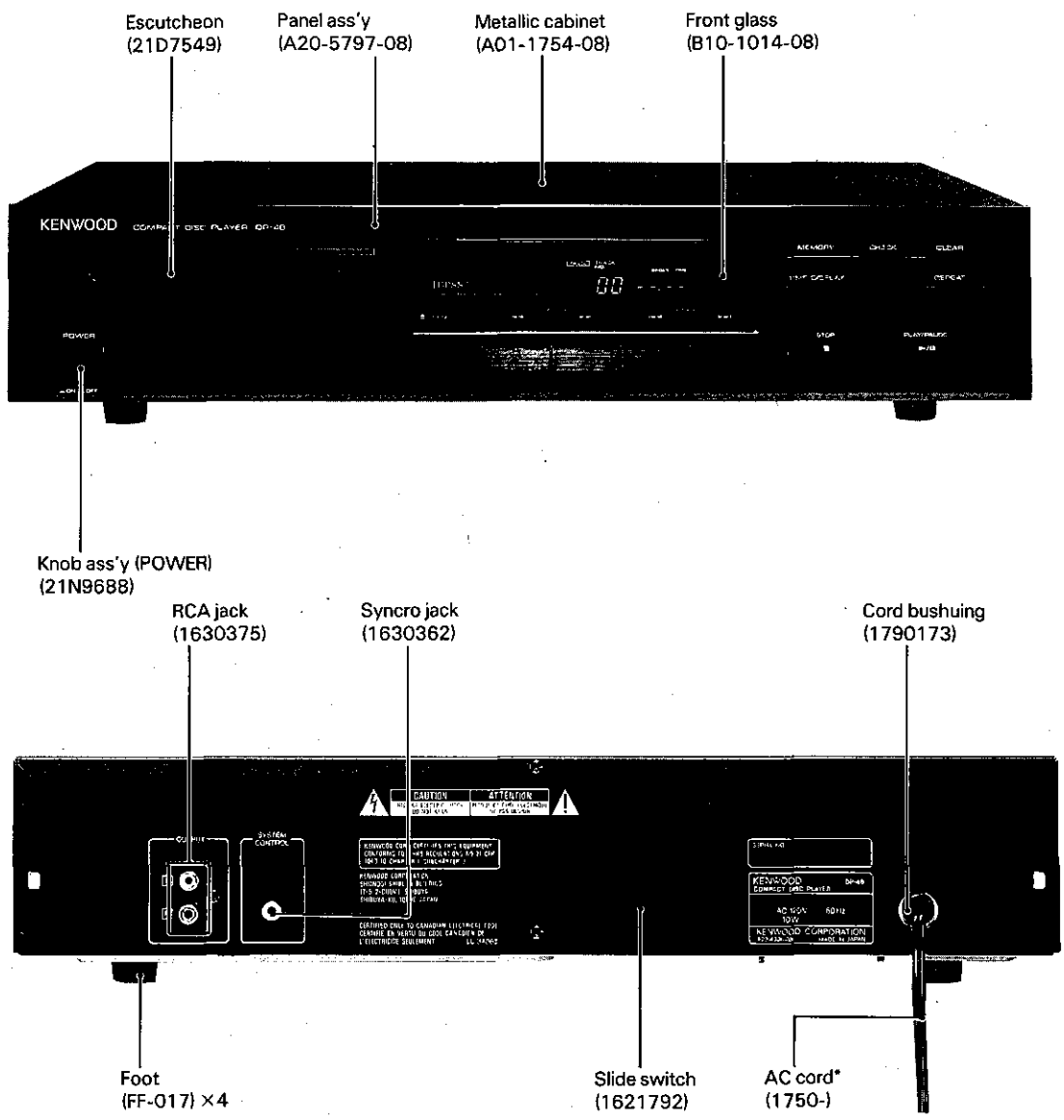

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DANGER: Laser radiation when open and interlock defeated.
AVOID DIRECT EXPOSURE TO BEAM.

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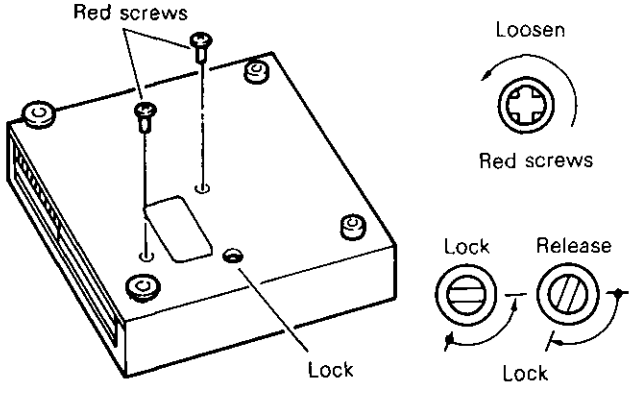
TRANSPORTATION SCREW

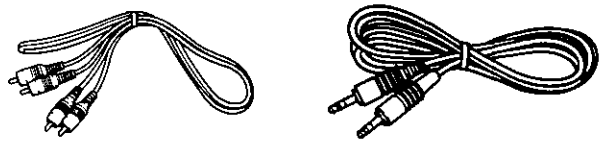
(1) Release the transportation lock as shown in the diagram.
(2) Remove the two red transportation screws.



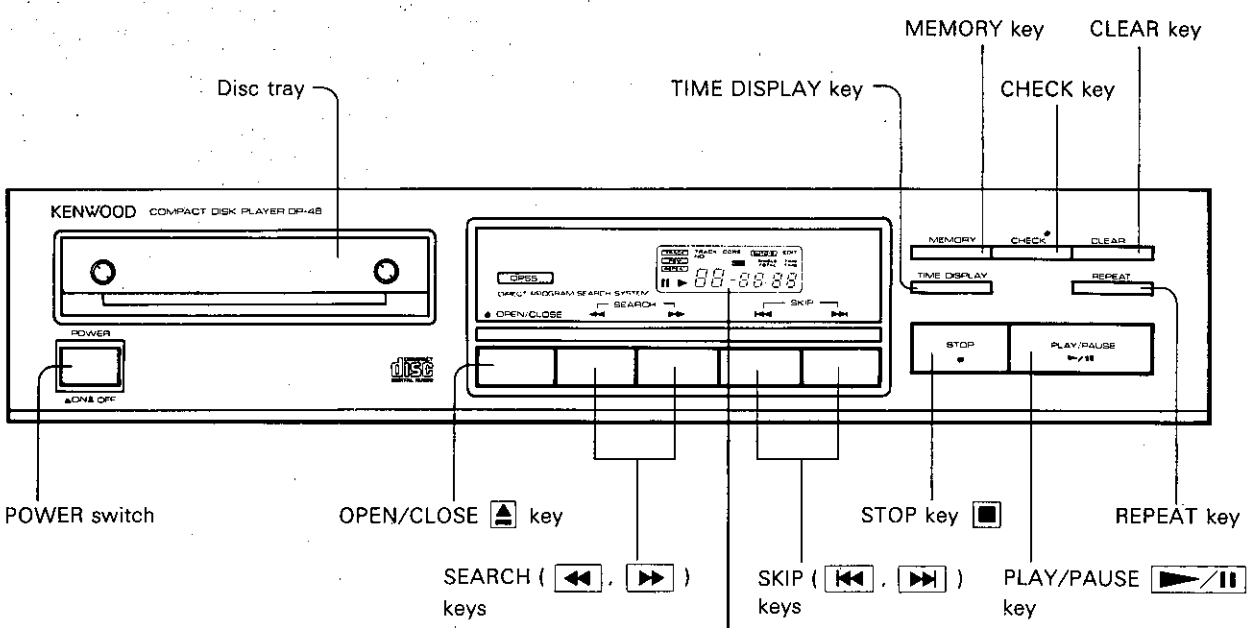
Before using the CD player, release the lock on the bottom of the unit and remove the two red screws used for transporting it from the factory with a screwdriver, coin or similar. Retain the screws and be sure to replace them when the unit is to be transported again.

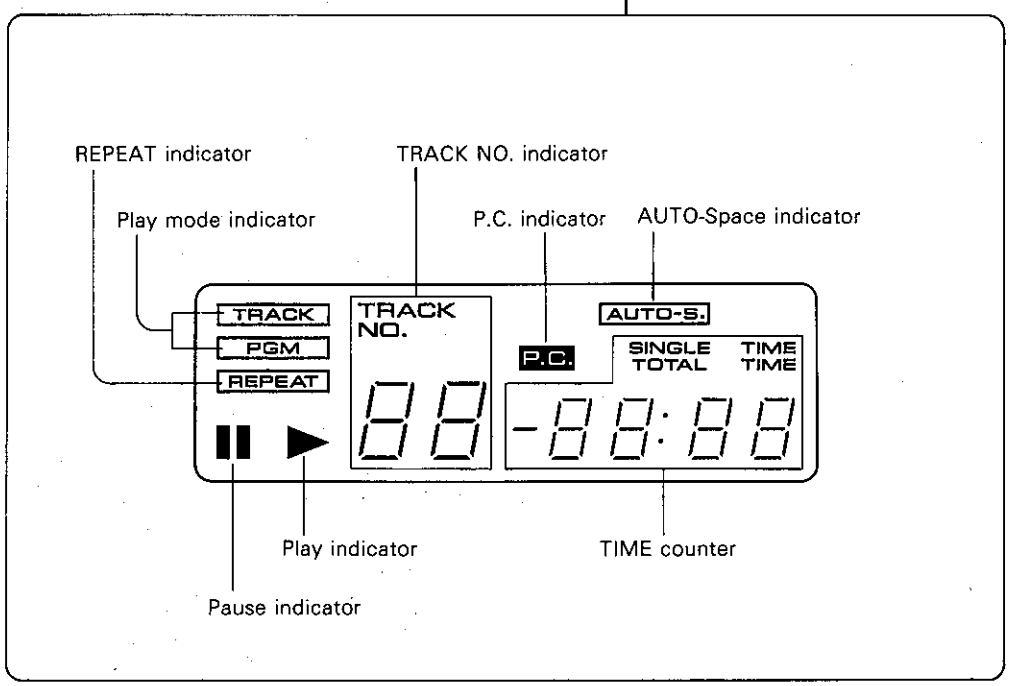
Accessories

- Audio cord 1
- System control cord ..... 1 (Except for some areas.)



CONTROLS AND INDICATORS

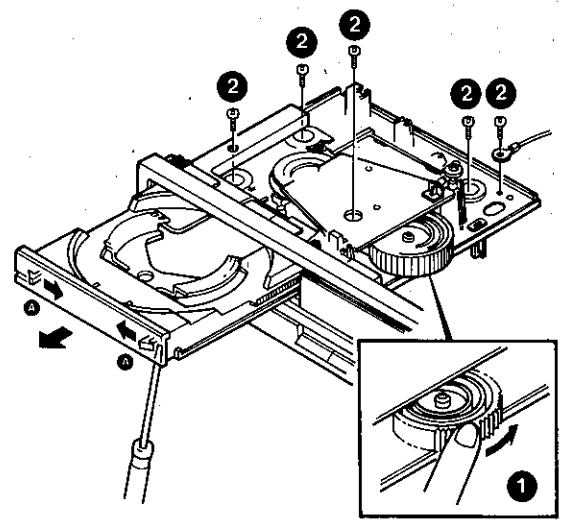




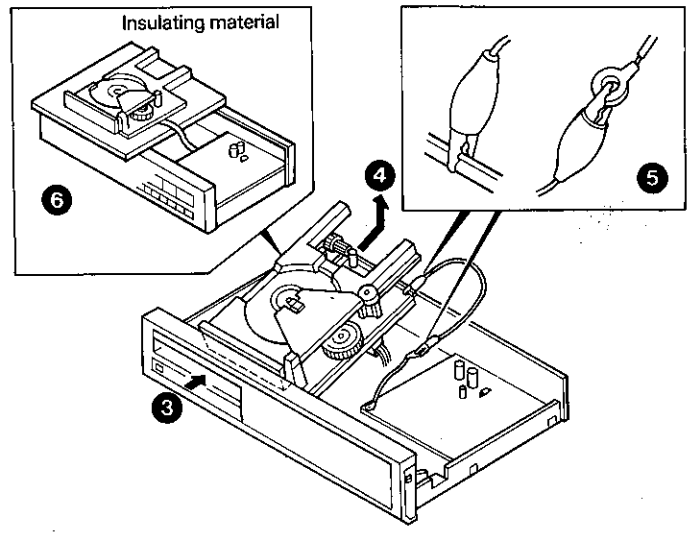
DISASSEMBLY FOR REPAIR

1. Removing and checking the mechanism

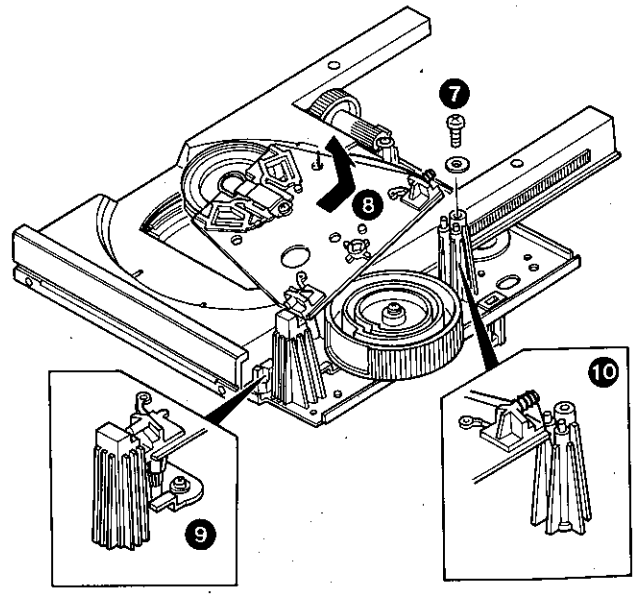
1. Turn the white gear slightly and slide the tray (❶).
2. Remove the tray panel (Ⓐ).
3. Remove the four screws retaining the Mechanism. Also remove the two screws located on the front side by inserting a screwdriver through the opening on the tray and clamper. Also remove the screw retaining the grounding wire (❷).



4. Return the opened tray (❸).
5. Take out the Mechanism in the direction of the arrow (❹).
6. Connect the grounding wire, removed in 2., again using a cable with clips (❺).
7. Place a plate made of insulating material, then place the Mechanism on it making it ready for adjustment (❻).



8. Remove the screw fixing the clamper (❼).
9. Remove the clamper in the direction of the arrow (❽).
10. When returning the clamper to the original position, first engage the stick projecting from the clamper with the metal (❾).
11. Then insert the spring attached on the clamper in between the pillars (❿) and return the clamper.

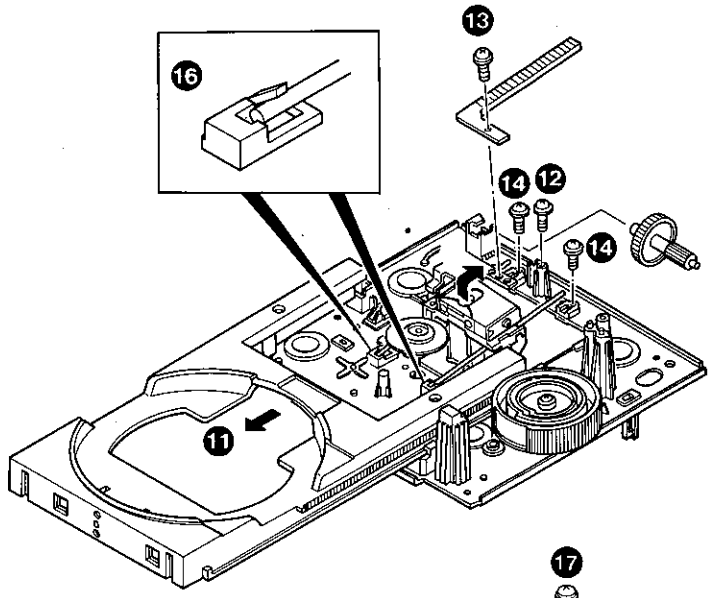


DISASSEMBLY FOR REPAIR

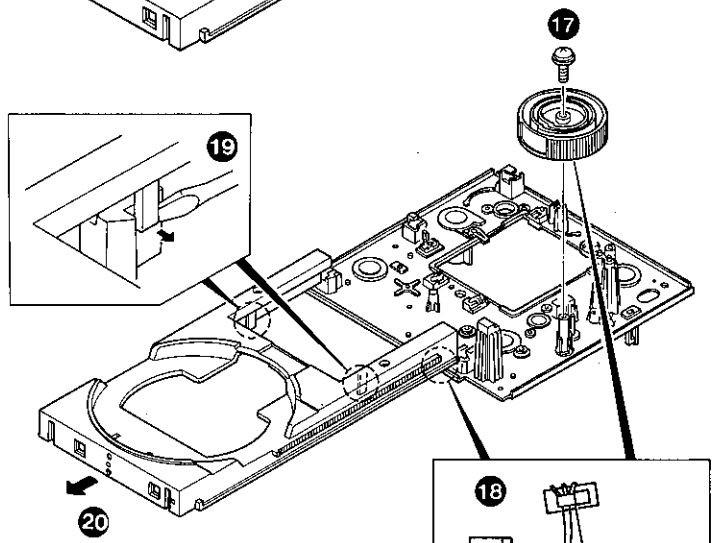
2. Removing the pickup

(Note) The pickup is sensitive to electrostatic destruction. Therefore, do not disassemble unless necessary. When replacing the pickup, take precaution against bodily static electricity by using a static arresting wrist band, etc.

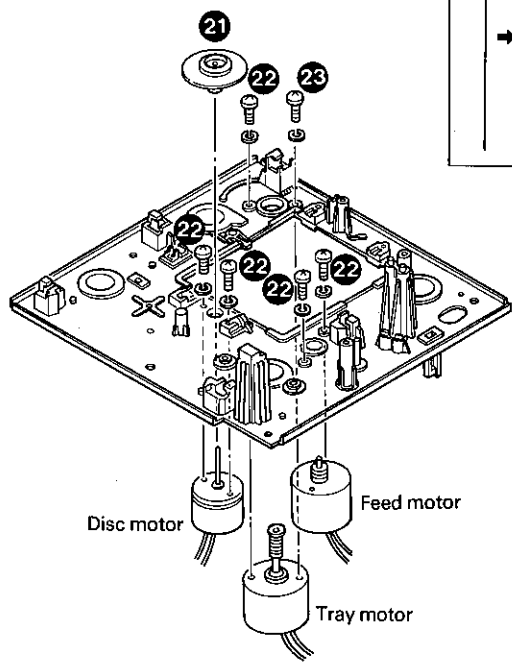
11. Pull out the tray (⓫).
12. Remove the screw, then the worm wheel (⓬).
13. Remove the screw, then the gear (⓭).
14. Remove the two screws fixing the shaft (⓮).
15. Remove the pickup block in the direction of the arrow (⓯).
16. When attaching the pickup, first insert the shaft into the groove on the chassis (⓰).



17. Remove the screw retaining the white gear, and remove it (⓱).
18. When assembling the pickup block to its original position, pull out the tray fully, and align the tray's gear with the first tooth of the white gear as shown in the illustration (⓲).
19. While disengaging the stoppers on the left and right of the tray (⓳), remove the tray in the direction of the arrow (⓴).



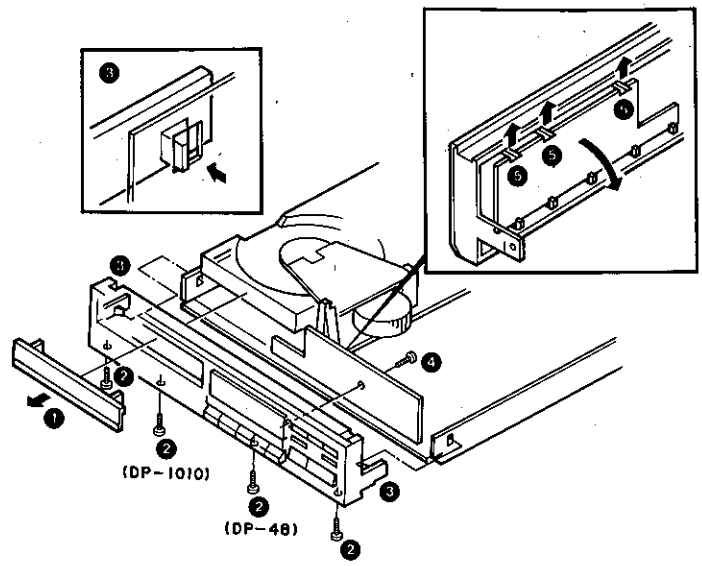
20. Remove the disc table (㉑).
21. Each motor is attached using two screws (㉒)



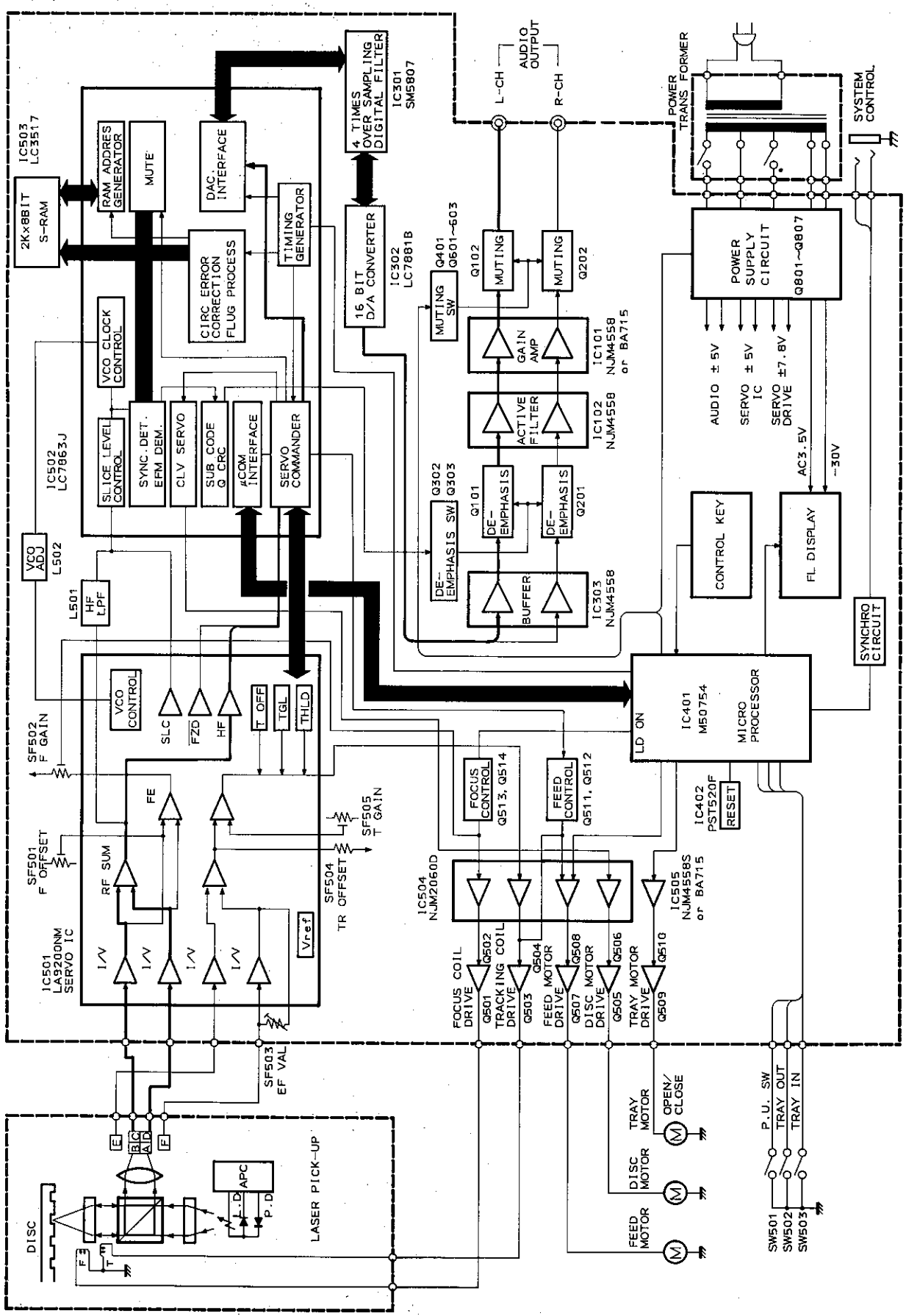
DISASSEMBLY FOR REPAIR

3. Removing and checking the PC board

1. Remove the tray panel (❶).
2. Remove the three screws from the front panel (❷).
3. Undo the two catches (❸) in the inside.
4. Remove the screw fixing the PC board to the front panel (❹).
5. Remove the claws retaining the PC board to the front panel in the sequence of ❺ , and remove the PC board in the direction of arrow.



BLOCK DIAGRAM



CIRCUIT DESCRIPTION

Component Functions
Board name: Main board

Component	Use/Function	Operation/Condition/Interchangeability
IC101 NJM4558S	Operation amplifier	Buffer amplifier
IC102 NJM4558S	Operation amplifier	Secondary active filter
IC103 NJM4556S	Operation amplifier	Headphone amplifier
IC301 SM5807	Digital filter	4 oversampling digital filter
IC302 LC7881B	D/A converter	16-bit D/A converter
IC303 NJM4558	Operation amplifier	D/A converter's buffer amplifier
IC401 M50754-112SP	Microprocessor	Display, each key input process, and servo IC control
IC402 PST-520F	Reset IC	Microprocessor IC reset
IC501 LA9200NM	Analog signal processing LSI	Tracking/focus error amplifier, VCO control, and LD control
IC502 LC7863J	Digital signal processing LSI	EFM signal demodulation, error detection/correction and servo control
IC503 LC3517A	S-RAM	Signal processing RAM (16 K)
IC504 NJM2060D	Operation amplifier	Focus/tracking/disc/feed servo preamplifier
IC505 NJM4558S	Operation amplifier	Loading motor predriver
Q101, Q201 2SC1740	Transistors	Emphasis switching
Q102, Q202 2SC2878	Transistors	Audio muting
Q301 2SC3811	Transistor	LR clock pulse inversion
Q302 2SC1740	Transistor	Emphasis transistor driver
Q303 2SA933	Transistor	Emphasis transistor driver
Q401 2SC1740	Transistor	Microprocessor output muting circuit driver
Q402 2SC1740	Transistor	Microprocessor output RESET signal inversion (supplied to IC502)
Q501 2SD1380	Transistor	Focus coil driver
Q502 2SB1009	Transistor	Focus coil driver
Q503 2SD1380	Transistor	Tracking coil driver
Q504 2SB1009	Transistor	Tracking coil driver
Q505 2SD1380	Transistor	Disc motor driver
Q506 2SB1009	Transistor	Disc motor driver
Q507 2SD1380	Transistor	Feed motor driver
Q508 2SB1009	Transistor	Feed motor driver

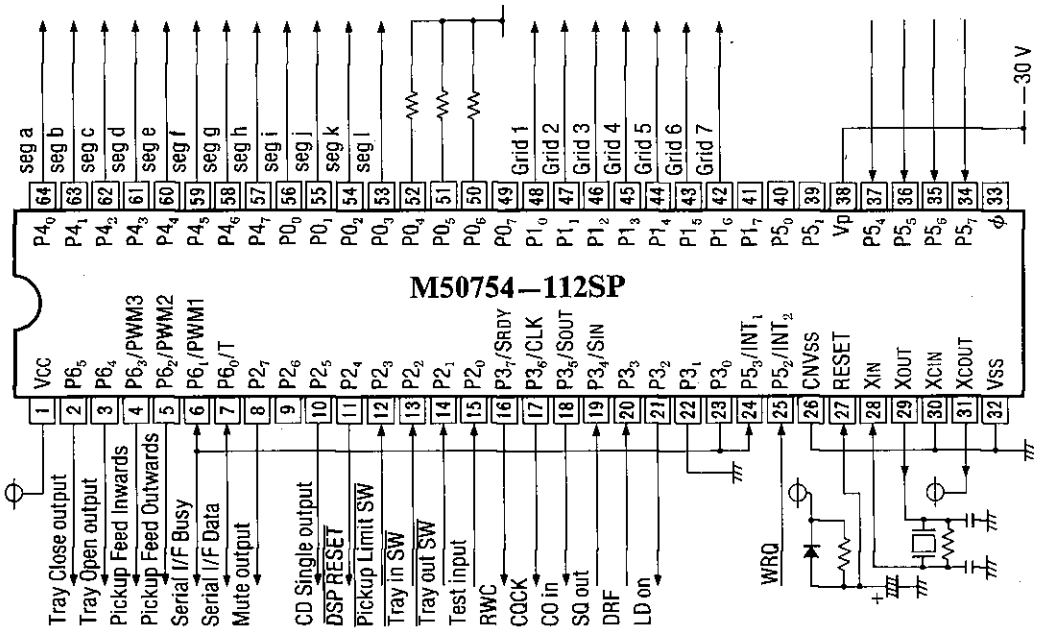
CIRCUIT DESCRIPTION

Component	Use/Function	Operation/Condition/Interchangeability
Q509 2SD1227	Transistor	Loading motor driver
Q510 2SB911	Transistor	Loading motor driver
Q511 2SC1740	Transistor	Control of feed servo signal by error flag
Q512 2SC1740	Transistor	Control of Q511 by tracking hold signal
Q513 2SA933	Transistor	Q514 inversion driver
Q514 2SC1740	Transistor	Focus servo cut-off at LD OFF
Q601 2SC1740	Transistor	Muting constant-voltage circuit
Q602 2SA933	Transistor	Microprocessor control muting driver
Q603 2SA933	Transistor	Power ON/OFF muting driver
Q801 2SD1380	Transistor	System +5 V constant-voltage circuit ripple filter
Q802 2SB1009	Transistor	System —5 V constant-voltage circuit ripple filter
Q803 2SC2060	Transistor	Audio +5 V constant-voltage circuit ripple filter
Q804 2SA934	Transistor	APC circuit laser drive
Q806 2SA934	Transistor	Audio —5 V constant-voltage circuit ripple filter
Q807 DTC124XS	Digital transistor	Q804 (laser drive) control

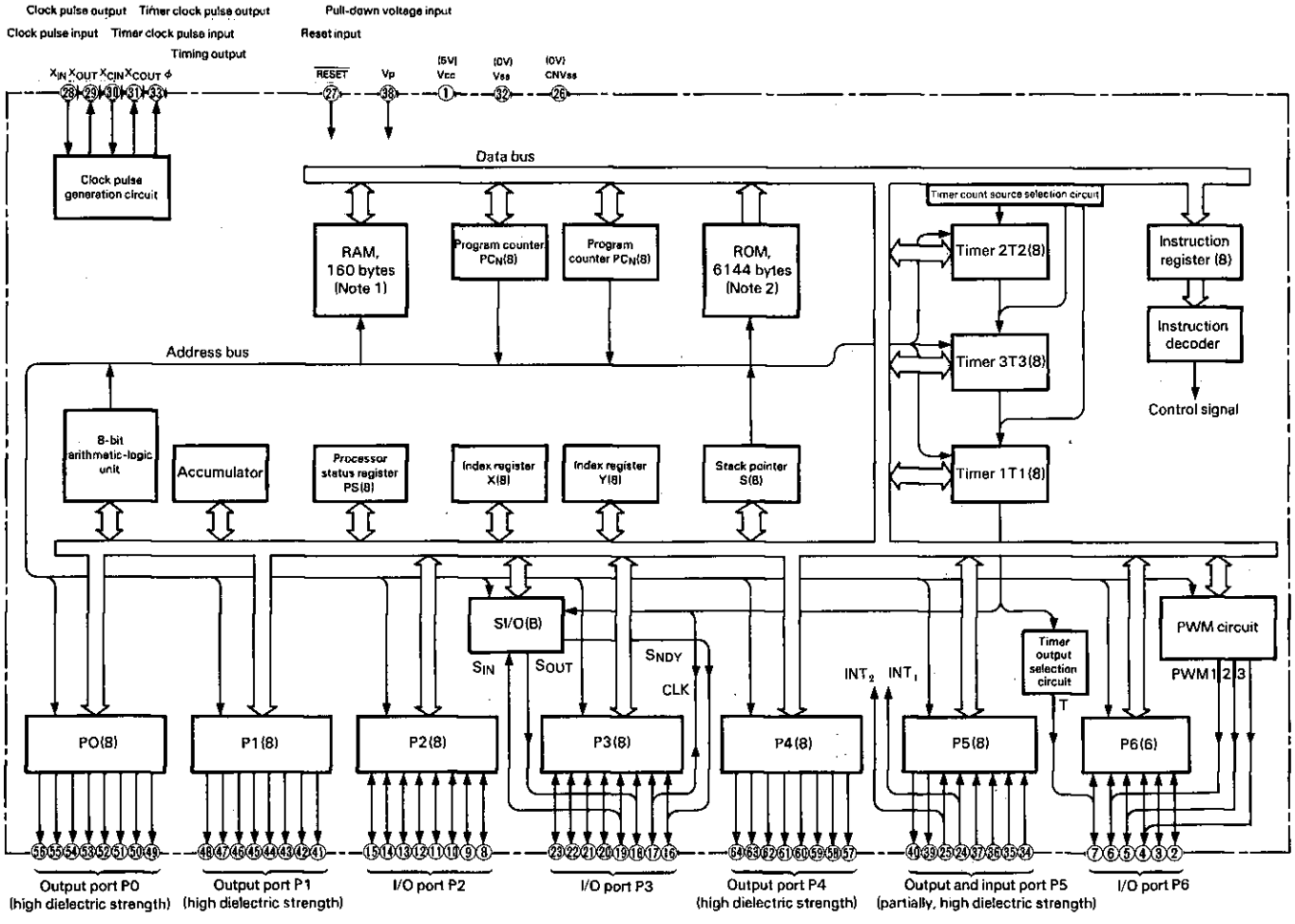
CIRCUIT DESCRIPTION

Microprocessor (M50754-112SP)

Circuit Diagram



Block Diagram of M50754-112SP



Notes: 1. 192 bytes for M50954-XXXSP and M50955-XXXSP
2. 8,192 bytes for M50954-XXXSP and 10,240 bytes for M50955-XXXSP

CIRCUIT DESCRIPTION

M50754-112SP Pin Assignment Table 1

Pin No.	Port	Name	I/O	Function
1	Vcc	—	—	Power supply pin
2	$P6_5$	T CLOSE	O	Tray Close signal Tray close: "H"
3	$P6_4$	T OPEN	O	Tray Open signal Tray open: "H"
4	$P6_3$/PWM3	P FEED I	O	Pickup Inwards Feed output Inwards feed: "H"
5	$P6_2$/PWM2	P FEED O	O	Pickup Outwards Feed output Outwards feed: "H"
6	$P6_1$/PWM1	SIF BUSY	I/O	Serial Interface Busy signal
7	$P6_0$/T	SIF DATA	I/O	Serial Interface Busy signal
8	$P2_7$	MUTE	O	Audio Mute output Mute: "H"
10	$P2_5$	SNGL OUT	O	CD Single output CD single: "H"
11	$P2_4$	$\overline{\text{DSP RST}}$	O	LSI Reset signal
12	$P2_3$	$\overline{\text{PU LIMIT}}$	I	Pickup Position Inner Limit SW input SW ON: "L"
13	$P2_2$	$\overline{\text{TRAY IN}}$	I	Tray Close Detection SW input SW ON: "L"
14	$P2_1$	TRAY OUT	I	Tray Open Detection SW input SW ON: "L"
15	$P2_0$	TEST	I	Test input pin Test mode: "L"
16	$P3_7$/SRDY	RWC	O	LC7863 RWC pin
17	$P3_6$/CLK	CQCK	O	LC7863 CQCK pin
18	$P3_5$/SOUT	COIN	O	LC7863 COIN pin
19	$P3_4$/SIN	SQOUT	I	LC7863 SQOUT pin
20	$P3_3$	DRF	I	LA9200 DRF pin
21	$P3_2$	LD ON	O	Laser Diode ON output Laser ON: "H"
22	$P3_1$	—	—	—
23	$P3_0$	—	—	—
24	$P5_3$/INT_1	SIF BUSY	I	Serial Interface Busy signal
25	$P5_2$/INT_2	WRQ	I	LC7863 WRQ pin
26	CNVss	—	—	Ground
27	RESET	—	—	Reset input
28	XIN	—	—	Oscillation input (4 MHz)
29	XOUT	—	—	Oscillation output
30	XCIN	—	—	Low-speed oscillation input
31	XCOUT	—	—	Low-speed oscillation ontput
32	Vss	—	—	Ground
33	ϕ	—	—	Timing output
34	$P5_7$	—	I	Key input
35	$P5_6$	—	I	Key input
36	$P5_5$	—	I	Key input
37	$P5_4$	—	I	Key input
38	Vp	—	—	Pull-down voltage input
42	$P1_6$	GRID 7	O	FLD grid signal
43	$P1_5$	GRID 6	O	FLD grid signal
44	$P1_4$	GRID 5	O	FLD grid signal
45	$P1_3$	GRID 4	O	FLD grid signal/key scan line
46	$P1_2$	GRID 3	O	FLD grid signal/key scan line
47	$P1_1$	GRID 2	O	FLD grid signal/key scan line

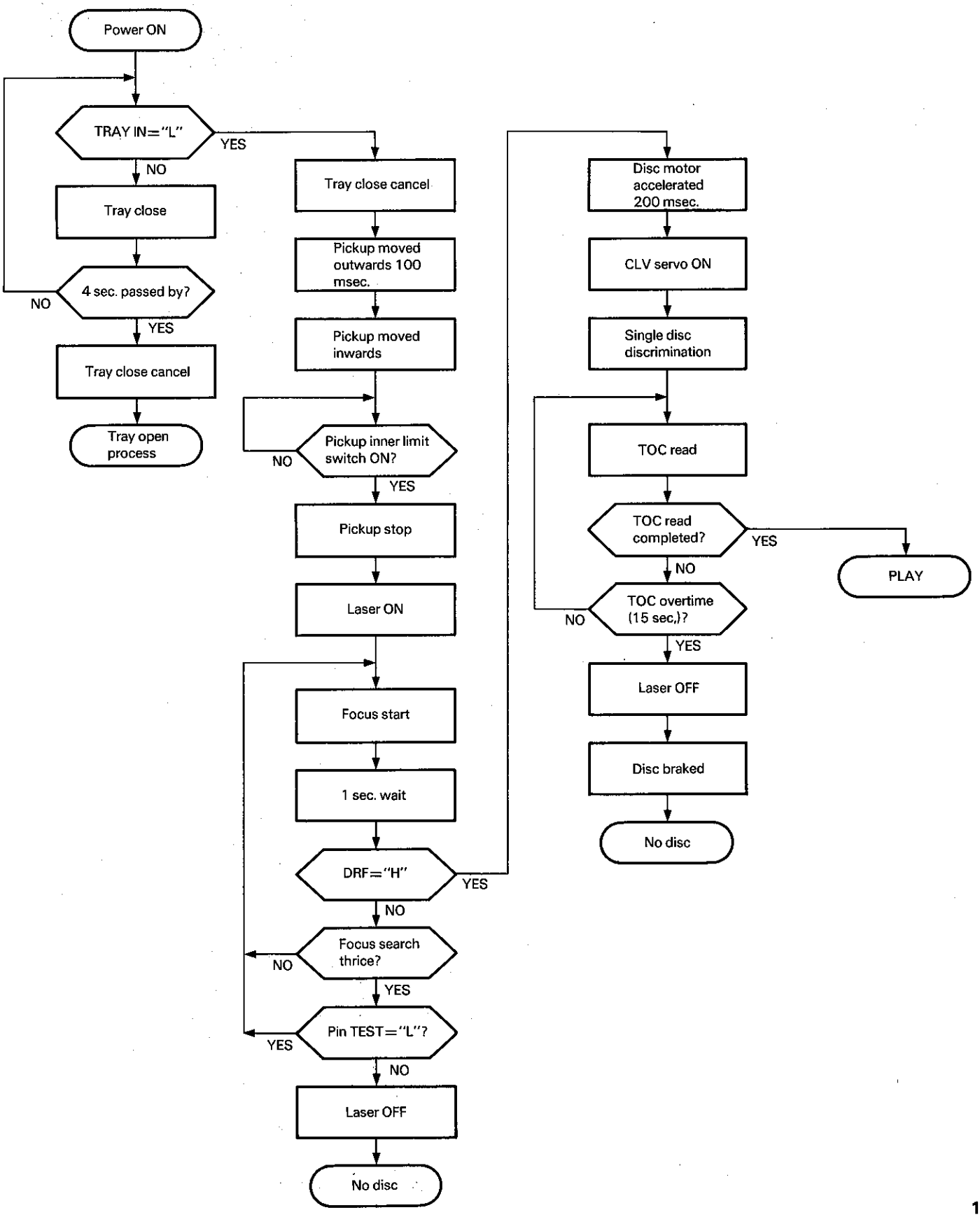
CIRCUIT DESCRIPTION

M50954-112SP Pin Assignment Table 2

Pin No.	Port	Name	I/O	Function
48	$P1_0$	GRID 1	O	FLD grid signal/key scan line
53	$P0_3$	SEG L	O	FLD segment signal
54	$P0_2$	SEG K	O	FLD segment signal
55	$P0_1$	SEG J	O	FLD segment signal
56	$P0_0$	SEG I	O	FLD segment signal
57	$P4_7$	SEG H	O	FLD segment signal
58	$P4_6$	SEG G	O	FLD segment signal
59	$P4_5$	SEG F	O	FLD segment signal
60	$P4_4$	SEG E	O	FLD segment signal
61	$P4_3$	SEG D	O	FLD segment signal
62	$P4_2$	SEG C	O	FLD segment signal
63	$P4_1$	SEG B	O	FLD segment signal
64	$P4_0$	SEG A	O	FLD segment signal

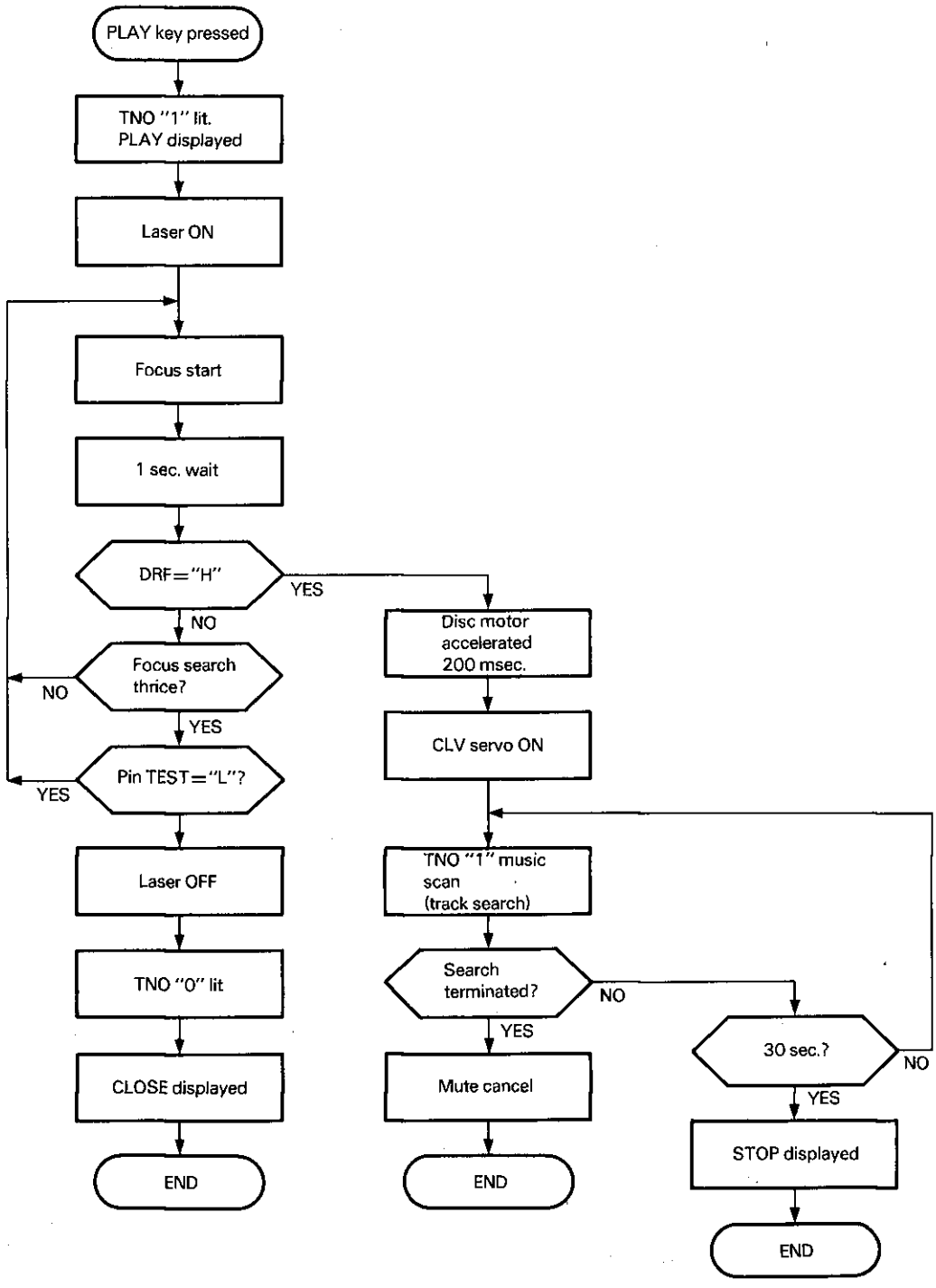
CIRCUIT DESCRIPTION

Operational flowchart after power ON from the state that the tray is open



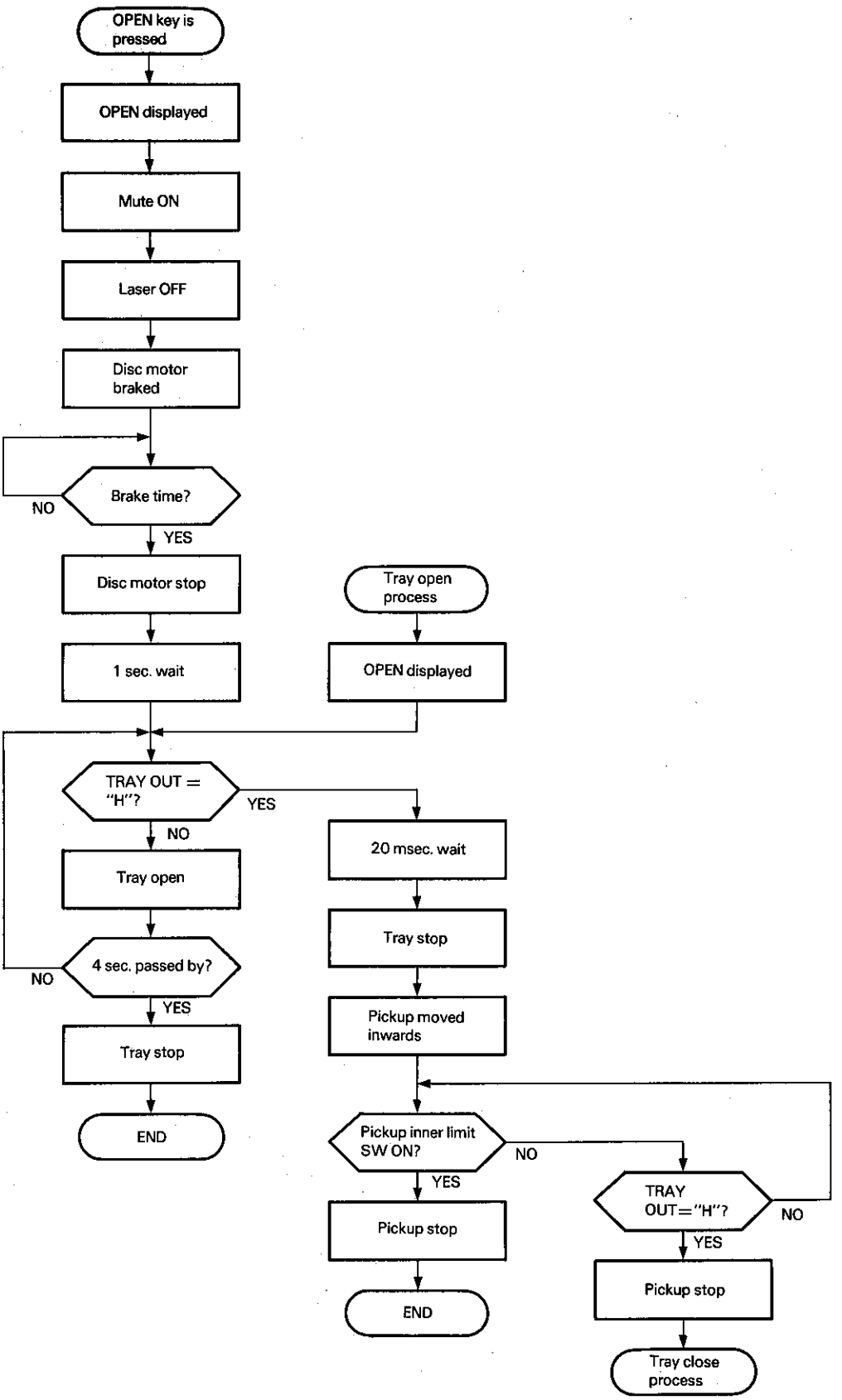
CIRCUIT DESCRIPTION

Operational flowchart when PLAY key is pressed (after TOC read)



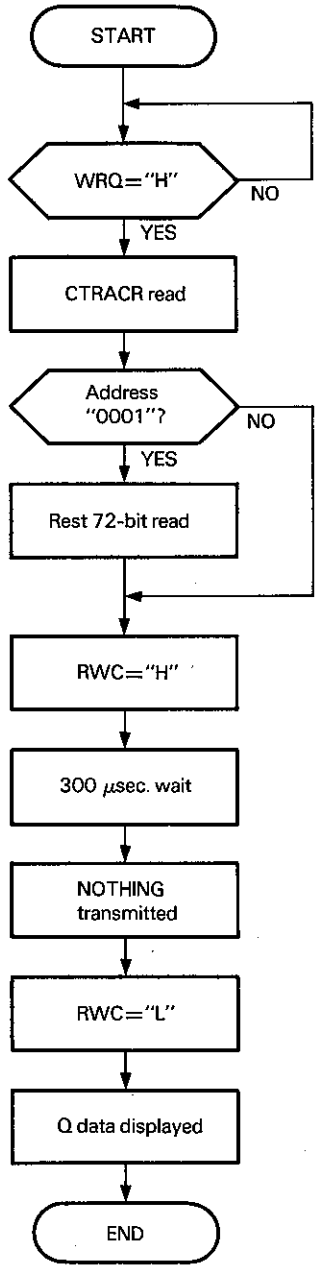
CIRCUIT DESCRIPTION

Operational flowchart when OPEN key is pressed (after play of track No. 1)



CIRCUIT DESCRIPTION

Operational flowchart from Q data read-in until display



CIRCUIT DESCRIPTION

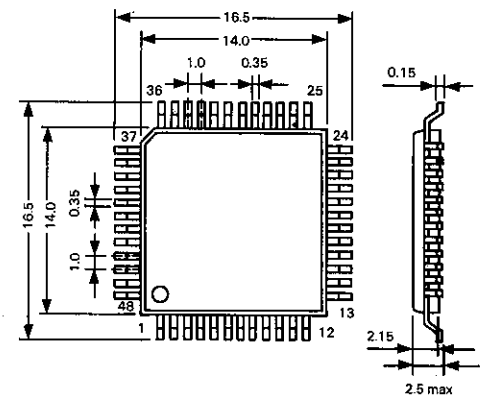
ASP for CD Player (LA9200NM)

The LA9200NM is a 3-beam bi-polar IC for analog signal processing and servo control in a compact disc player. This is capable of constituting a compact disc player system in combination with LC786ON, 7863 (DSP) and 7881 (DAC) with a lesser number of components.

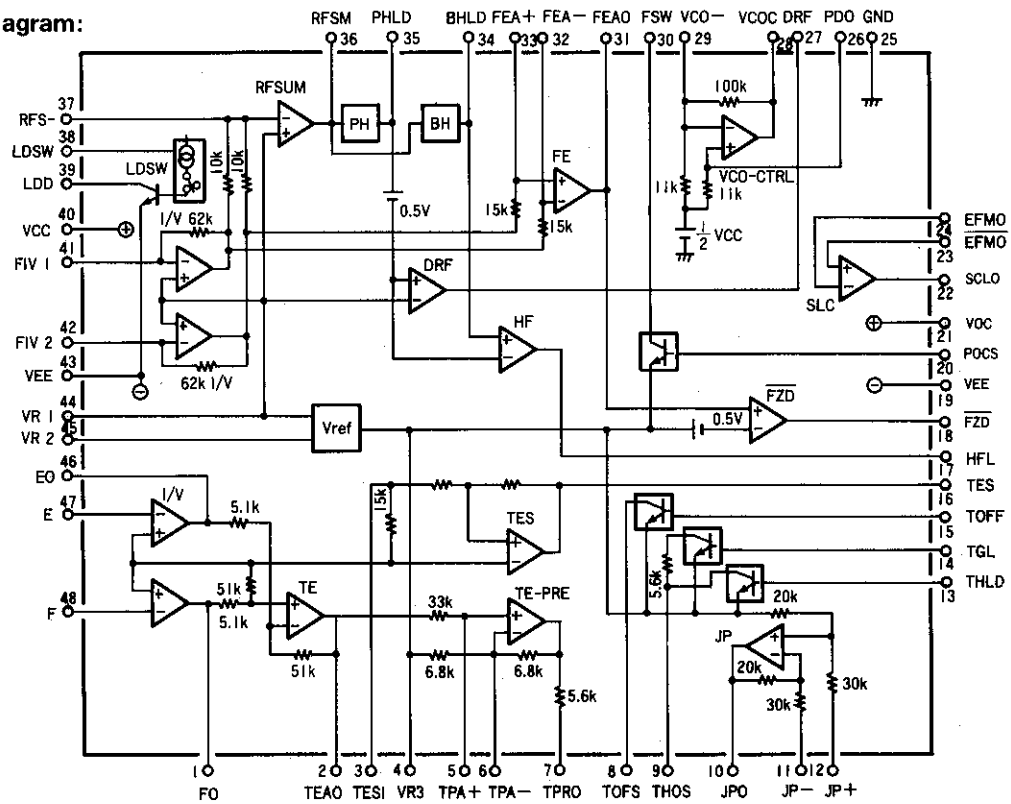
Functions:

- RF amplifier
- Focus servo
- Tracking servo
- VCO control
- Slice level control (SLC)
- Laser ON/OFF switch
- DRF, HF, FZD, TES, JP
- Switch: Focus (FOCS), THLD, TOFF, TGL

Outline dimensioned drawing 3102-Q48DIC (unit: mm)



Block Diagram:



CIRCUIT DESCRIPTION

Operation Principle

1. RF amplifier (eyepattern output)

Output currents (A+C) and (B+D) of the photo diode of the optical pickup are input to pins 41 and 42, respectively, after which they are in turn subject to I-V conversion and are output to pin 36 of the RF amplifier. Output (A+C)+(B+D) of pin 36 is input to a filter, whose output becomes the HF signal (eyepattern).

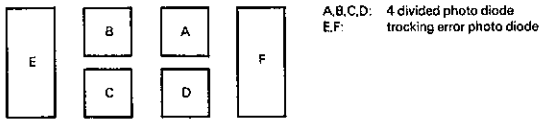


Figure 1. Photo diode

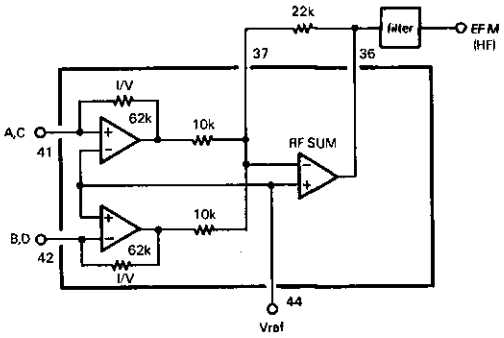


Figure 2. RF amplifier

2. Focus servo

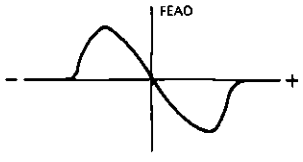
Some focusing methods are available.

Here, by detecting the difference in light amount between (A+C) and (B+D) by the FE amplifier), it is possible to determine whether the focal point on the disc surface is passed or not yet reached. Thus, the focus lens can always be just focused by virtue of driving the focus coil by the difference signal between (A+C) and (B+D).

2-1 FE amplifier

Outputs (A+C) and (B+D) of the optical pickup are input to pins 41 and 42, respectively. Of (A+C) and (B+D) subjected to I-V conversion, the difference (B+D)—(A+C) is output to pin 31 of the EF amplifier.

a. Disc displacement



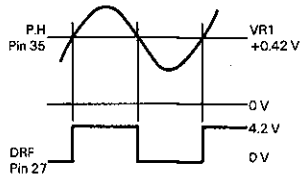
2-2 DRF, FZD, FOCS

These circuits are to start the focus servo.

2-2-1 DRF

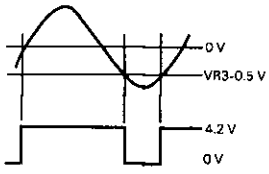
When the laser beam is just focused on the disc surface, this becomes "H".

P.H (pin 35)		DRF (pin 27)
VR1 (pin 44)	+0.42 V or more	H
VR1	less than 0.42 V	L



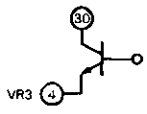
2-2-2 FZD

This circuit is to detect the S curve of the focus error detection signal (FE amplifier output). When the focal point on the disc surface is near, although the S curve is detected, this signal falls when it is less than —0.5 V.



2-2-3 FOCS

When pin 20 is made "H", pin 30 becomes "L". This is used to stop the FE amplifier output.



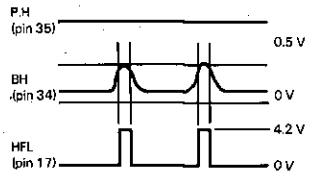
2-2-4 Focusing

Explanation is made on the focusing taking an example of an amplification circuit. When the focus start instruction is issued, FST of LC7860N becomes "L" to draw down the objective lens, which is then drawn up gradualy along the charging by FOCS. When the focal point on the disc surface nears, the S curve of the focus error detection signal appears in the FE amplifier output. Thus, when this output becomes less than —0.5 , FZD falls. Concurrently with its fall, FOCS is reset to open pin 30 to turn ON the focus servo. At this time, when DRF is "H", the focus servo continues operation as it is.

CIRCUIT DESCRIPTION

3. HFL

This is to detect track jump. This, together with TES, transmits the brake timing data to DSP (e.g. LC7863A).



4. TES

TES falls when the S curve of the tracking error detection signal (TE output) falls. The TES circuit, which is a Schmitt circuit, permits lesser faulty operation due to noises put on the TE output. TES, together with HFL, transmits the brake timing data to DSP (e.g. LC7863A).

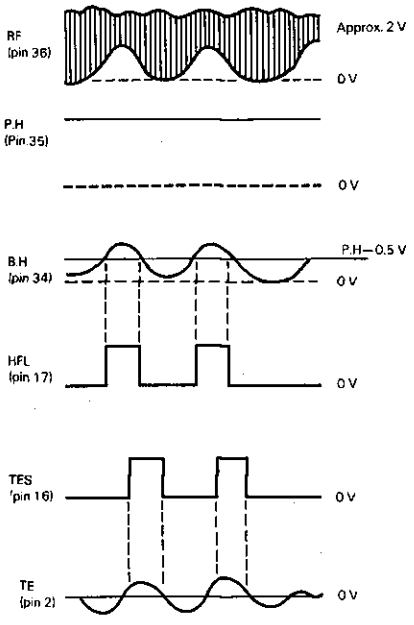


Figure 3. Timing chart

5. Tracking servo

This circuit, which is suited to the 3-beam method, is to let the light beam follow exactly on the track. With the 3-beam method, one main beam and two sub beams are used in track detection.

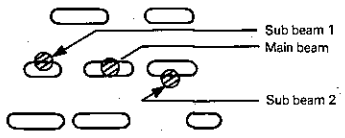


Figure 4. Track detection

The reflections of sub beams 1 and 2 are received by photo diodes E and F.

In case of upwards deviation

Reflection of sub beam 1 > reflection of sub beam 2

In case of downwards deviation

Reflection of sub beam 1 < reflection of sub beam 2

Making use of this difference in reflection, the tracking servo is driven.

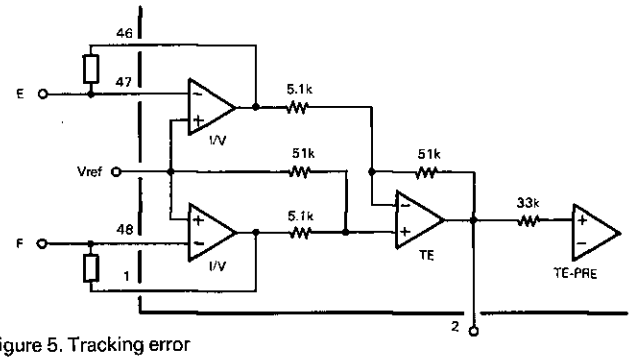


Figure 5. Tracking error

5-1 TE amplifier

Photo diode output currents E and F of the optical pickup are input to pins 47 and 48, respectively. After that they are in turn subject to I-V conversion, and their difference is taken by the TE amplifier and is output as F-E to pin 2.

5-2 TE-PRE amplifier

This amplifier is to compensate for low-frequency and high-frequency ranges of the TE amplifier output.

5-3 JP (jump pulse) amplifier

This amplifier is for track jump. This is also used in tracking brake to move the beam to the target track quickly to follow on the track.

5-4 TOFF

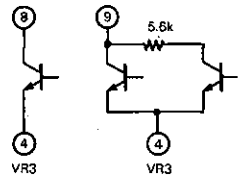
When pin 15 is made "H", pin 8 becomes "L" to turn OFF the tracking servo.

5-5 TGL

When pin 14 is made "H", pin 9 becomes "L" through a resistance of 5.6 k to lower the tracking gain.

5-6 THLD

When pin 13 is made "H", pin 9 becomes "L" to hold the tracking servo output voltage to that voltage at THLD ON.



CIRCUIT DESCRIPTION

6. VCO-CTRL

The CVO-CTRL amplifier is to supply the control voltage to the varicap by making use of the PDO output of the DSP (e.g. LC7863A) side in the PLL circuit which generates a clock pulse synchronized with the EFM signal (4.3218 MHz). In the VCO-CTRL amplifier, when an input is applied to pin 26 (non-inverting input), it is compared with the reference voltage (approx. 2.5 V) at pin 29 (inverting input), after which it is output to pin 28.

7. SLC (slice level control)

The SLC amplifier is to fix the duty ratio of the HF signal (eyepattern) to 50% at all times. When the HF signal of DSP (e.g. LC7863A) is input to EFMIN, an inphase signal passed through an amplitude limiter is output to EFMO and a anti-signal is output to EFMO. These EFMO and EFMO are input respectively to pins 24 (EFMO) and 23 (EFMO) of LA9200NM. Therewith, when the SCLO output of pin 22 is fed back to EFMIN, the slice level is automatically corrected to ensure the duty ratio of the EFM signal 50%.

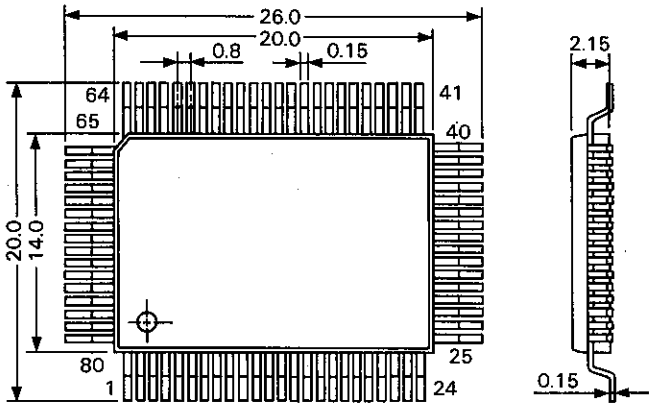
8. LDSW

This is the current source to make the laser of the laser pickup emit light. LDD (pin 39) is turned ON/OFF by applying 0 V or 5 V to LDSW (pin 38).

Digital Signal Processing (for CDP) (LC7860N/LC7863-)

LC7860N/LC7863 is a CMOS LSI by which in a compact disc or laser disc player the signals in the digital audio section are processed and the system is servo-controlled. This LSI also deals with EFM signal demodulation, deinterleaving, error signal detection/correction, sound quality improvement, and signals of a digital filter, etc. useful for player cost reduction, and different commands to the servo system from the microprocessor. This LSI permits direct interface with LC7880 (made by our company) DAC exclusive for serial input. Points of difference between LC7860N and LC7863 lie in sub-code Q reading conditions, track jump and LRCLK timings, etc.

Outlined dimensioned drawing
3044B-QBOAIC (unit: mm)

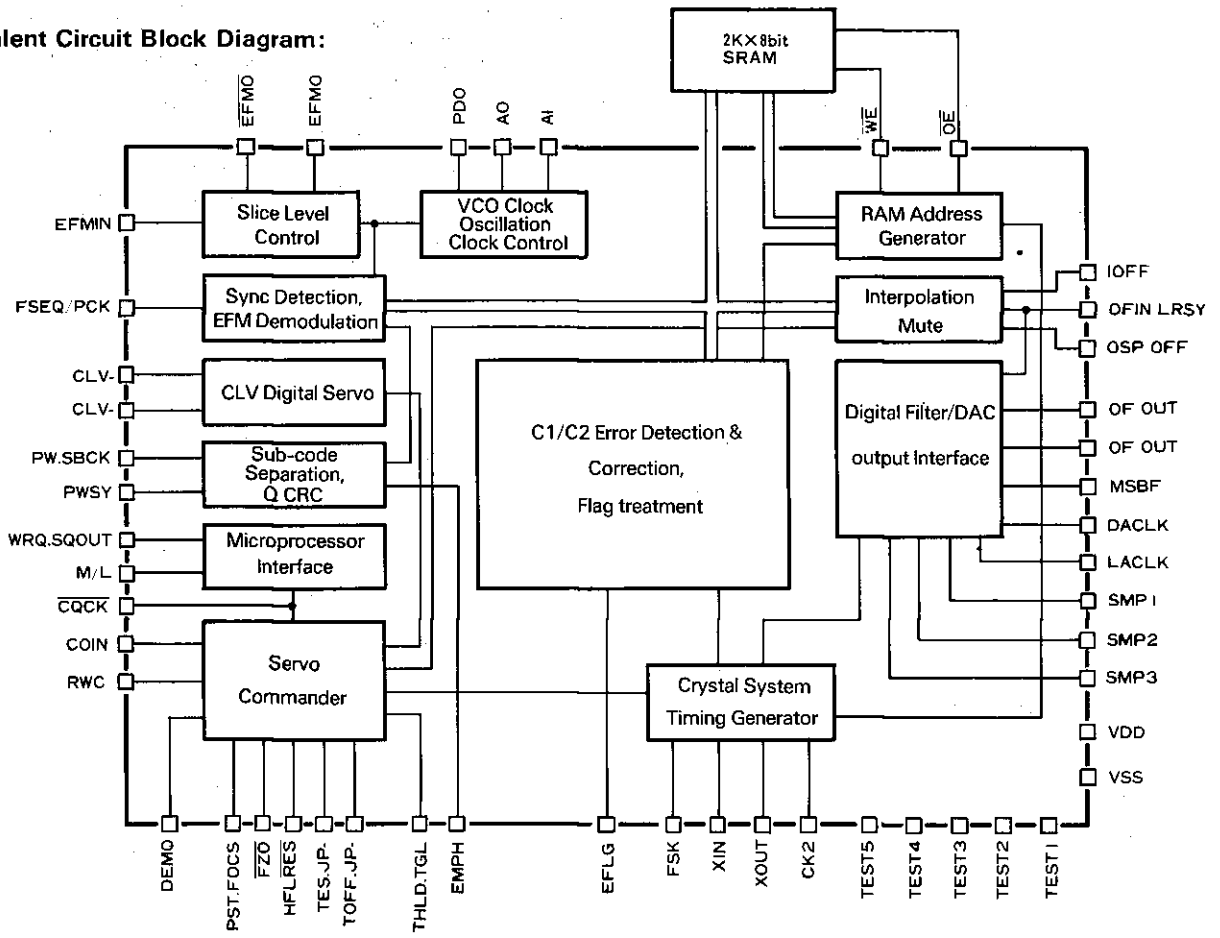


Functions:

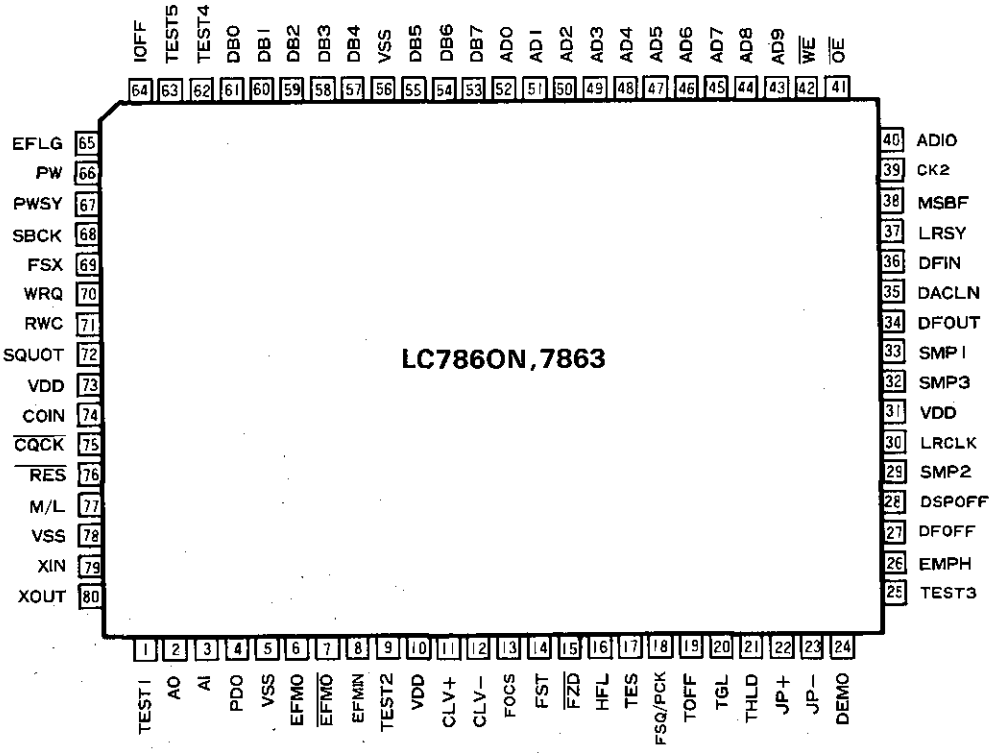
- When the HF signal is input, the HF signal is sliced at an accurate level and converted to an EFM signal, which is then phase-compared with VCO to regenerate the PLL clock pulse of average 4.3218 MHz.
- With a crystal oscillator externally connected, various timings necessary inside are precisely generated, including generating the standard clock pulse of 4.3218 MHz.
- The rotating speed of the disc motor is controlled by the frame phase difference signal made up by the playback clock pulse and the standard clock pulse.
- The frame sync signal detection, protection and interpolation are performed to ensure stable reading of data.
- The EFM signal is demodulated and converted to 8-bit symbol data.
- Subcode is separated from the EFM demodulation signal and output to the external microprocessor.
- Subcode Q signal, after CRC check, is output to the microprocessor through a serial I/O. (LSB first-out selectable)
- The EFM demodulation signal is subject to buffering by signal exchange with the external RAM to absorb jitters of up to +/—4 frames due to the change in disc rotation.
- The EFM demodulation signal is subject to unscrambling and deinterleaving into a prescribed order of data.
- Error signal detection, correction and flag treatment are performed. (C1, dual C2, dual correction method)
- With reference to C1 flag and C2 check result, C2 flag is set. By C2 flag, signal interpolation and previous value holding are made.

CIRCUIT DESCRIPTION

Equivalent Circuit Block Diagram:



Pin Layout:



CIRCUIT DESCRIPTION

Pin functions

Pin No.	Pin Name	I/O		Function
1	TEST1	I	—	LSI testing. Normally unconnected.
2	AO	O	—	VCO is formed with an LC resonance circuit connected between AI and AO. PDO (8.6436 MHz) is an output in phase with the EFM signal and its setting is so made as to raise the VCO frequency when PDO varies to "+".
3	AI	O	—	
4	PDO	O	—	
5	Vss	—	—	Grounding
6	$\overline{\text{EFMO}}$	O	—	HF signal of 1 to 2 Vp-p is input to EFMIN. EFM signals in anti-phase with each other passed through amplitude limiter from EFMO and EFMO are output, thereby providing slice level control.
7	EFMO	O	—	
8	EFMIN	I	—	
9	TEST2	I	—	LSI testing. Normally unconnected.
10	V_{DD}	—	—	+5 V.
11	CLV+	O	—	Disc motor control output.
12	CLV—	O	—	
13	FOCS	O	—	Focus servo is turned OFF when FOCS is "H". The objective lens is drawn down when FST is "L", while when FST is "H", it is drawn up gradually. When FZD appears, FOCS is reset. For focus draw-in.
14	FST	O	—	
15	$\overline{\text{FZD}}$	I	—	
16	HFL	I	*1	*1. Kick pulse JP+ or JP— is generated according to the track jump command. Jump is made over the specified number of tracks (1, 4, 16, 64). *2. 4.3218 MHz PCK monitor pin. When DEMO is "H", this pin becomes "H" with a coincidence between the sync signal detected from the EFM signal and the sync signal of the counter.
17	TES	I	*1	
18	FSEQ/PCK	O	*2	
19	TOFF	O	*1	
20	TGL	O	*1	
21	THLD	O	*1	
22	JP+	O	*1	
23	JP—	O	*1	
24	DEMO	I	—	Sound emission for unit adjustment.
25	TEST3	I	—	LSI testing. Normally unconnected.
26	EMPH	O	—	At "H", deemphasis is necessary.
27	DFOFF	I	—	Digital filter ON/OFF SW. At "H", filter OFF.
28	DSPOFF	I	—	LSI testing. Normally "L".
29	SMP2	O	*3	*3. Signal output to DAC. L/R selection. Sample-hold signal. *4. +5 V. *5. For CDROM compatible signal output. *6. CDROM sync signal.
30	LRCLK	O	*3	
31	V_{DD}	—	*4	
32	SMP3	O	*3	
33	SMP1	O	*3	
34	DFOUT	O	*3	
35	DACLK	O	*3	
36	DFIN	I/O	*5	
37	LRSY	O	*6	
38	MSBF	I	*3	
39	CK2	O	—	2.1609 MHz
40	AD10	O	*7	*7. RAM address output. *8. Output mode at WE="L" and input mode at WE="H".
41	$\overline{\text{OE}}$	O	*8	
42	$\overline{\text{WE}}$	O	*8	
43	AD9	O	*7	
44	AD8	O	*7	
45	AD7	O	*7	
46	AD6	O	*7	
47	AD5	O	*7	
48	AD4	O	*7	

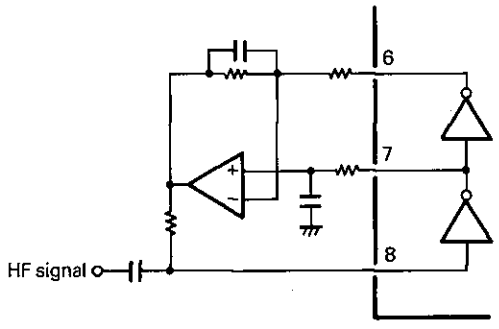
CIRCUIT DESCRIPTION

Pin No.	Pin Name	I/O		Function
49	AD3	O	*7	*7. RAM address output. *8. Output mode at WE="L" and input mode at WE="H".
50	AD2	O	*7	
51	AD1	O	*7	
52	AD0	O	*7	
53	DB7	I/O	*9	*9. DB7-DB0: Connected to RAM data pins. *10. Grounding.
54	DB6	I/O	*9	
55	DB5	I/O	*9	
56	Vss	—	*10	
57	DB4	I/O	*9	
58	DB3	I/O	*9	
59	DB2	I/O	*9	
60	DB1	I/O	*9	
61	DB0	I/O	*9	
62	TEST4	I	—	LSI testing. Normally unconnected.
63	TEST5	I	—	
64	IOFF	I	—	CDROM compatible. At "H", interpolation and previous value holding are not performed.
65	EFLG	O	—	For C1, C2, single or dual correction monitor.
66	PW	O	—	PWSY is a sub/main combined sync signal. Its change from "H" to "L" is caught outside to send eight clock pulses to SBCK to read out sub-codes P, Q, R, S, T, U, V and W.
67	PWSY	O	—	
68	SBCK	I	—	
69	FSX	O	—	7.35 kHz sync signal output
70	WRQ	O	*11	*11. WRQ becomes "H" when sub-code Q data passes CRC check. This "H" is caught outside, and CQCK is sent correspondingly, and thereby data is read out from SQOUT. When data is needed in the LSB First mode, M/L is set down to "L". After setting RWC to "H" by microprocessor, command is given by sending out CQCK, command and data synchronously. *12. Once set to "L" at power ON.
71	RWC	I	*11	
72	SQOUT	O	*11	
73	VDD	—	*11	
74	COIN	I	*11	
75	CQCK	I	*11	
76	RES	I	*12	
77	M/L	I	*11	
78	Vss	—	—	GND
79	XIN	I	—	Pins to connect 8.6436 crystal oscillator.
80	XOUT	O	—	

CIRCUIT DESCRIPTION

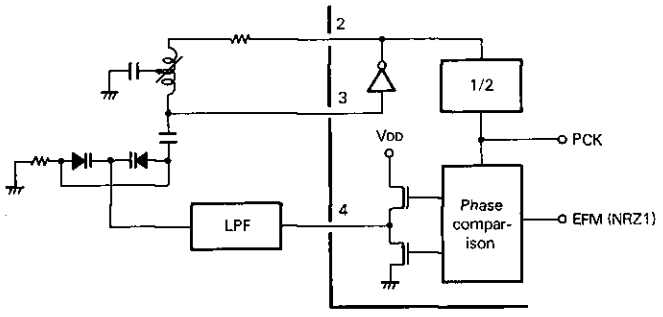
Pin Applications:

1) HF signal input circuit: pin 8 (EFMIN), pin 7 (EFMO), pin 6 (EFMO)



- When HF signal is input to EFMIN, the EFM signal (NRZ) subjected to slicing at an optimum level is obtained.

2) PLL clock pulse regeneration circuit: pin 4 (PDO), pin 3 (AI), pin 2 (AO)



The VCO is formed with an LC resonance circuit connected between AO and AI. When the VCO phase delays, the output of PDO swings up in the direction of "+". At this time, therefore, a control voltage is supplied to the varicap to raise the VCO frequency.

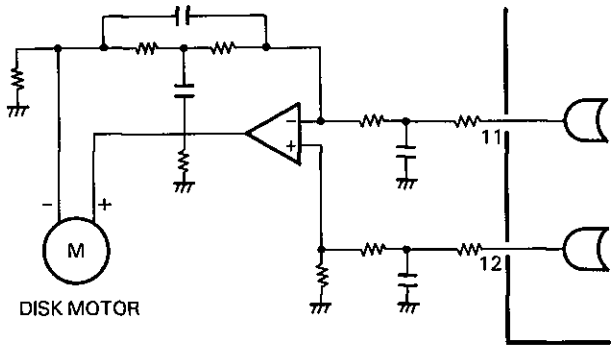
3) Sync detection monitor: pin 18 (FSEQ/PCK)
When DEMO (pin 24) is "L", this acts to monitor PCK of average 4.3218 MHz resultant from dividing VCO by 2. while when DEMO is "H", this becomes "H" with a coincidence between the frame sync signal separated from the EFM signal by use of PCK and the timing pulse generated in the counter, at which time this acts as a sync detection monitor.

4) CLV servo circuit: pin 11 (CLV+), pin 12 (CLV—)
CLV+ is to accelerate the disc in the forward direction and CLV— is to decelerate. According to the command from the microprocessor, one is selected from four modes, acceleration, deceleration, CLV and stop. The following table shows the H/L states of outputs CLV+ and CLV— in each mode.

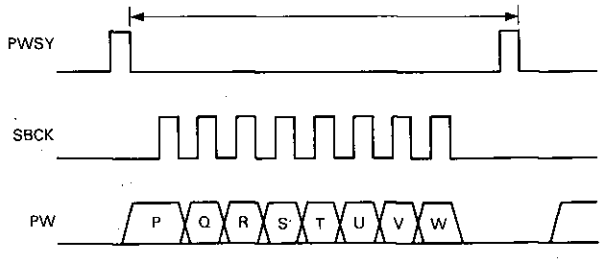
MODE	CLV+	CLV—
Acceleration	H	L
Deceleration	L	H
CLV	*	*
STOP	L	L

*: In the CLV mode, the disc rotation is detected from the HF signal to change the internal mode of DSP to perform each control so that the disc is put to the regularized linear velocity rotation. The frequency of PWM is 7.35 kHz and the period of 1/64 DUTY is 1.114 sec.

Internal mode	CLV+	CLV—
Rough servo (when rotation speed is judged low)	H	L
Rough servo (when rotation speed is judged high)	L	H
Phase control (with PCK locked)	PWM	PWM
Low-speed rotation (with no HF signal)	1/64 DUTY	L



5) Subcodes P, Q, R, S, T, U, V and W output circuit: pin 67 (PWSY), pin 66 (PW), pin 68 (SBCK)
PW is the pin to output the subcode signal. By sending eight clock pulses to SBCK within 136 μsec from the fall of PWSY, it is possible to read out all subcodes P, Q, R, S, T, U, V and W. The signal appearing at PW changes at the fall of RCK. When no clock pulses are sent to SBCK, only subcode P is output from PW.
a. 1 frame (approx. 136 μsec.)

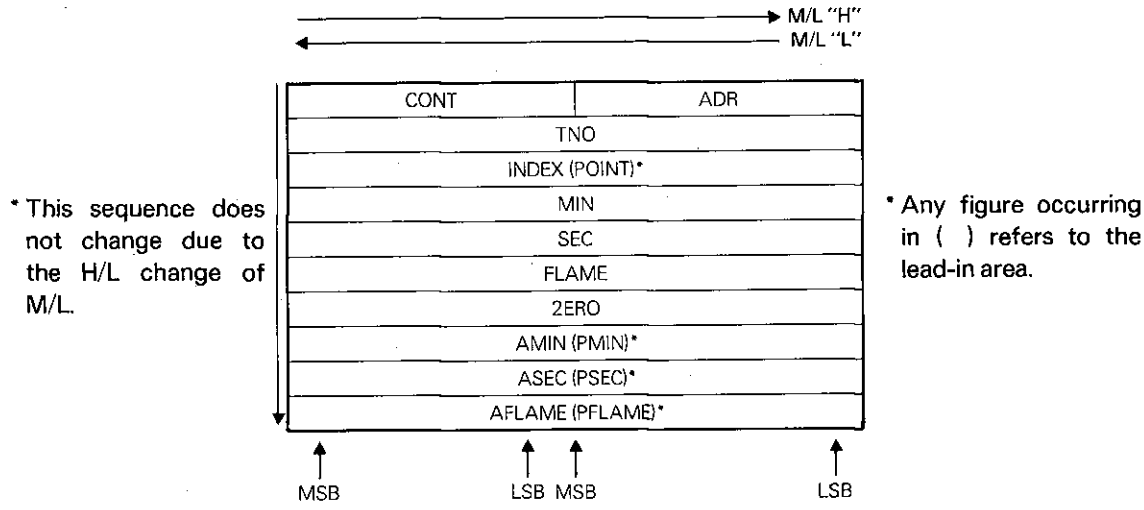


In a frame with subcode sync S0 and S1, PWSY does not fall down to "L" and keeps "H".

CIRCUIT DESCRIPTION

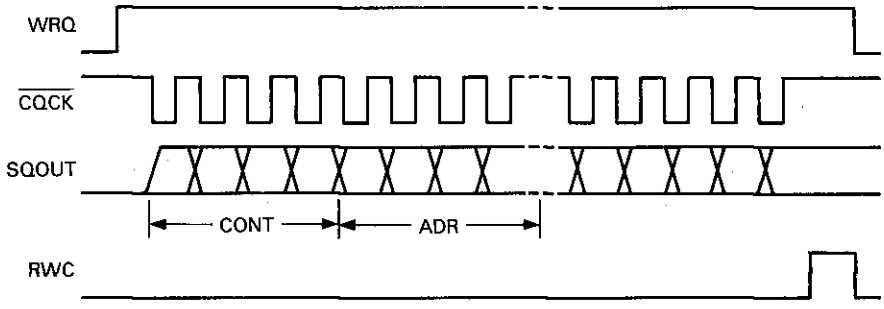
6) Subcode Q output circuit: pin 70 (WRQ), pin 71 (RWC), pin 72 (SQOUT), pin 75 (CQCK), pin 77 (M/L)Subcode Q is necessary for tune access, display, etc. Only when this subcode passes CRC check and then address 1 (Note 1) is engaged, WRQ becomes "H". Upon the start of CQCk sending, the data in a register is inhibited from updating. The microprocessor, after completion of reading, makes RWC "H" once to permit data updating. At this time, WRQ goes down to "L". WRQ at "H" goes down to "L" after 11.2 msec. Accordingly, CQCK starts to be sent while WRQ is "H". By setting M/L to "L", it is possible to read out data in the LSB First mode.

Note 1: LC7863 is provided with no condition for address 1.



* This sequence does not change due to the H/L change of M/L.

* Any figure occurring in ( ) refers to the lead-in area.



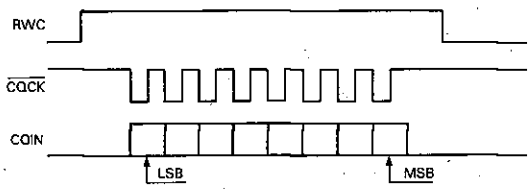
7) Servo commander function: pin 71 (RWC), pin 74 (COIN), pin 75 (CQCK)

By setting RWC to "H" and sending 8-bit 1-word commands synchronized with clock pulse CQCK from COIN, it is possible to input four instructions of FOCUS START, DISC MOTOR, TRACK JUMP and MUTE.

#1: JP pulse width 233 μsec+233 μsec

#2: Change from acceleration pulse to deceleration pulse is made upon the detection of an intermediate point of the track.

Note 2: For LC7863, this command provides 32 TRACK JUMP.



MSB CODE LSB	COMMAND				
00000000			NOTHING		
00010001	1	TRACK	JUMP	IN	#1
00010010	1	TRACK	JUMP	IN	#2
00010011	4	TRACK	JUMP	IN	
00010100	16	TRACK	JUMP	IN	
00010101 (Note. 2)	64	TRACK	JUMP	IN	
00011001	1	TRACK	JUMP	OUT	#1
00011010	1	TRACK	JUMP	OUT	#2
00011011	4	TRACK	JUMP	OUT	
00011100	16	TRACK	JUMP	OUT	
00011101 (Note. 2)	64	TRACK	JUMP	OUT	
00010110	256	TRACK	CHECK		
00000001	MUTE			0 dB	
00000010	MUTE			−12 dB	
00000011	MUTE			−∞ dB	
00000100	DISK	MOTOR		START	
00000101	DISK	MOTOR		CLV	
00000110	DISK	MOTOR		BRAKE	
00000111	DISK	MOTOR		STOP	
00001000	FOCUS		START		

LSB First out

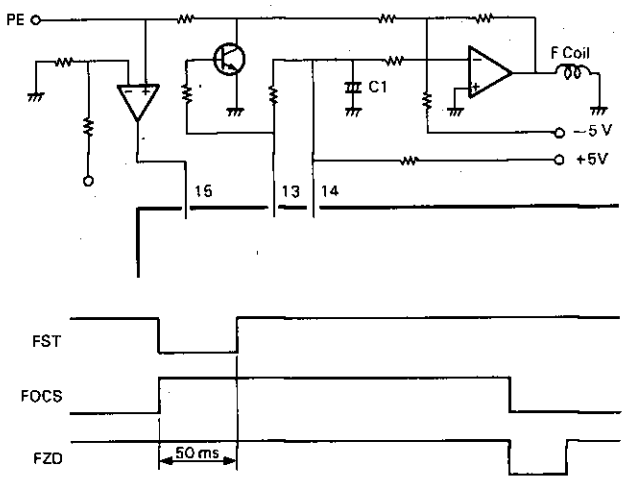
CIRCUIT DESCRIPTION

Each command is executed at the fall of RWC. A MUTE or DISC MOTOR command, latched in register, can be replaced with another command of its own group. When reset by RES, MUTE $-\infty$ DB is engaged for mute and DISC MOTOR STOP for disc motor.

It takes around 25 msec for the execution of a TRACK JUMP command. Even during its execution, a next TRACK JUMP command can be provided. It takes more time for the execution of the FOCUS START command. During this time, any other command cannot be input. Therefore, when inputting a plurality of commands, a MUTE or DISC MOTOR command is input first, and next the FOCUS START command or a TRACK JUMP command is input.

8) Focus servo circuit: pin 13 (FOCS), pin 14 (FST), pin 15 (FZD)

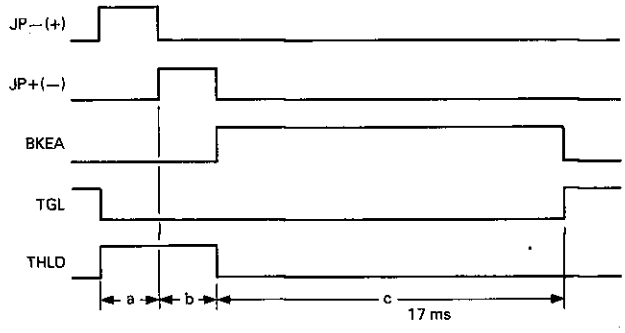
When an instruction of FOCUS START is input to the servo commander, the charge in C1 is at first discharged by FST to draw down the object lens (when the disc is above), and in the next, discharged by FOCS to draw it up gradually. When the laser beam is just focused on the disc surface, FOCS is reset concurrently with the fall of FZD to turn ON the focus servo.



processor sends out an instruction of FOCUS START once again to repeat the focus servo operation.

9) Track jump circuit: pin 16 (HFL), pin 17 (TETS), pin 19 (TOFF), pin 20 (TGL), pin 21 (THLD), pin 22 (JP+), pin 23 (JP−)

The microprocessor, after sending out the command, checks DRF to confirm that the laser beam is just focused on the disc surface, then proceeds to the subsequent flow. Even upon the exhaustion of the charge in C1, when the laser beam is not focused on, the micro-

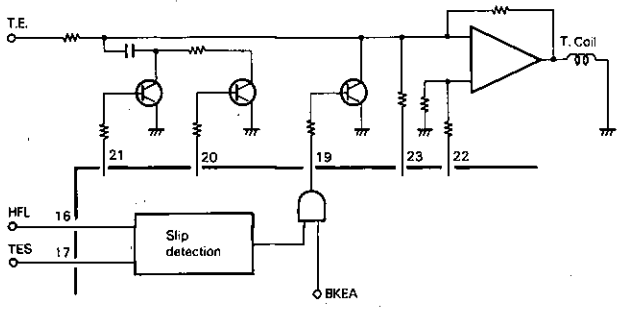


COMMAND	a	b	c
1 TRADK JUMP IN (OUT) #1	233 μs	233 μs	17 ms
1 TRACK JUMP IN (OUT) #2	0.5 TRACK JUMP period	233 μs	17 ms
4 TRACK JUMP IN (OUT)	2 TRACK JUMP period	466 μs	17 ms
16 TRACK JUMP IN (OUT)	9 TRACK JUMP period	7 TRACK JUMP period	17 ms
64 TRACK JUMP IN (OUT)	36 TRACK JUMP period	28 TRACK JUMP period	17 ms
256 TRACK CHECK	Only THLD is "H" while 256 tracks pass by.		

When an instruction of TRACK JUMP is input to the servo commander, an acceleration pulse appears, then successively a deceleration pulse appears, and thus a specified track jump is completed by way of a braking period.

In the braking period, the beam slip direction is detected by inputs TES and HFL, that portion of the TE signal which causes further slippage, and the servo gain is raised by TGL to grasp the track to which the pickup jumps.

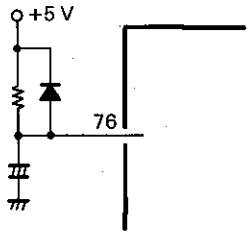
The TOFF pin becomes "H" when the STOP command is engaged for CLV servo.



CIRCUIT DESCRIPTION

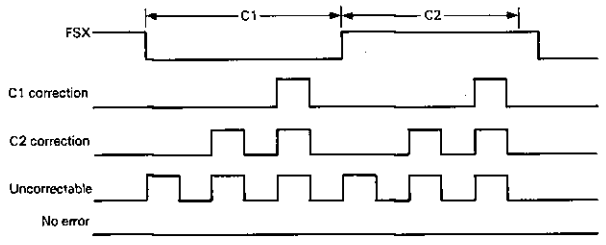
10) Sound emission for adjustment process: pin 24 (DEMO)
Even when no command is sent from the microprocessor, with this pin set to "H", MUTE 0 DB is engaged for muting and DISC MOTOR CLV for disc motor, an therewith the focus start operation is performed. In addition, this pin works to select between functions of pin 18 (FSEQ/PCK).

11) Reset circuit: pin 76 (RES)
At power ON, this pin is made once "L" and then "H". MUTE $-\infty$ DB is engaged for muting and DISC MOTOR STOP for disc motor.



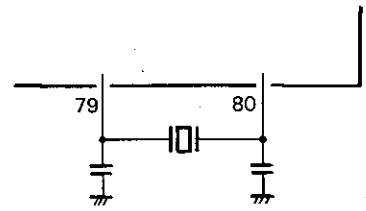
12) Deemphasis ON/OFF: pin 26 (EMPH)
The preemphasis ON/OFF bit of the subcode Q control data is output from the EMPH pin. When this pin is "H", deemphasis is performed.

13) Error flag output: pin 65 (EFLG), pin 69 (FSX)



FSX, which is obtained from the dividing of the crystal clock signal, is a 7.35 kHz frame sync signal. The error correction status in each frame is output to EFLG. From the "H" quantity occurring herein, the playback quality can be easily known.

14) Crystal clock oscillation: pin 79 (Xin), pin 80 (Xout)
A crystal oscillator of 8.6436 MHz, connected between these pins, oscillates to generate a clock pulse which acts as the time base.

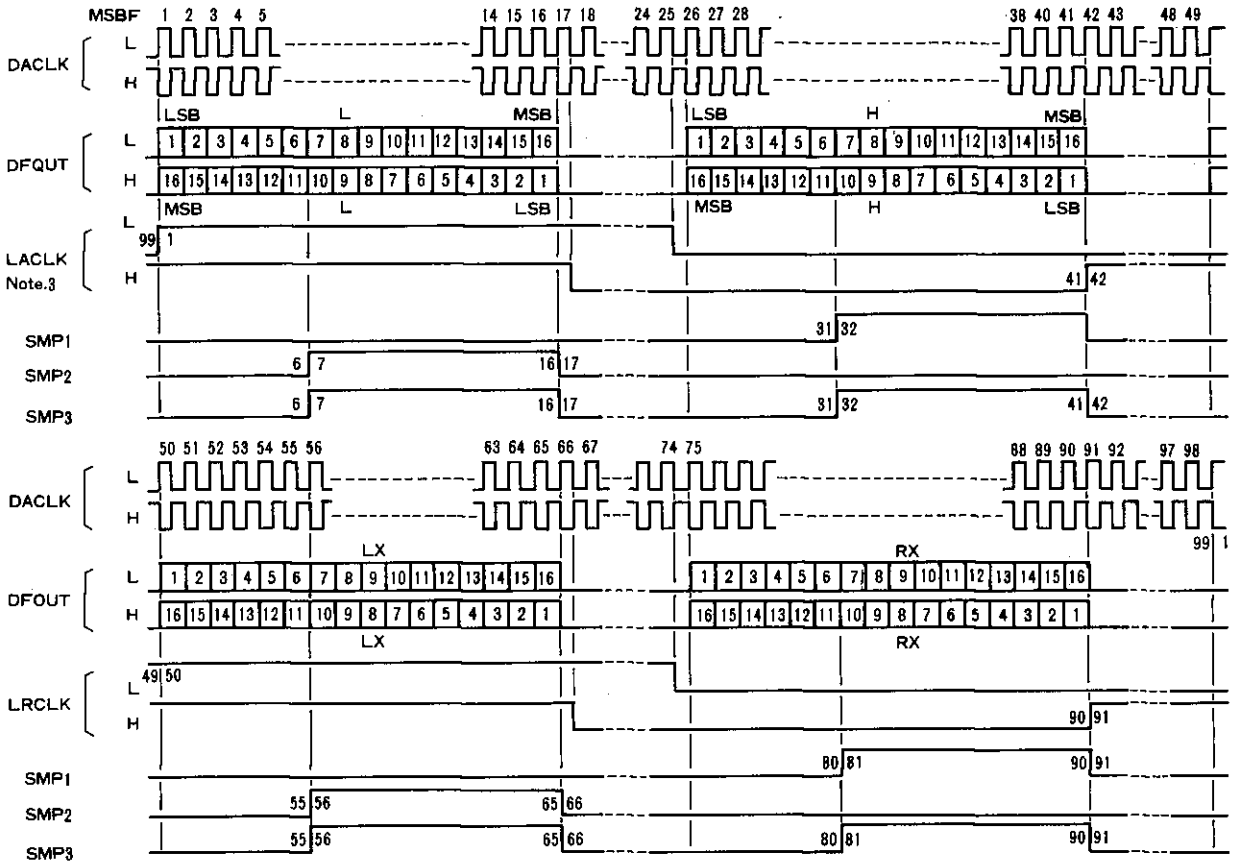


15) DAC interface: pin 27 (DFOFF), pin 29 (SMP2), pin 30 (LRCLK), pin 32 (SMP3), pin 33 (SMP1), pin 34 (DFOUT), pin 35 (DACLK), pin 38 (MSBF)
When MSBF is "L", the DAC data is output in synchronization with the rise of DACLK in the LSB First Out mode. While when MSBF is "H", the DAC data is output in sychronization with the fall of DACLK in the MSB First Out mode.

CIRCUIT DESCRIPTION

LC7860N Digital Filter Output Data Format (DFOFF="L")

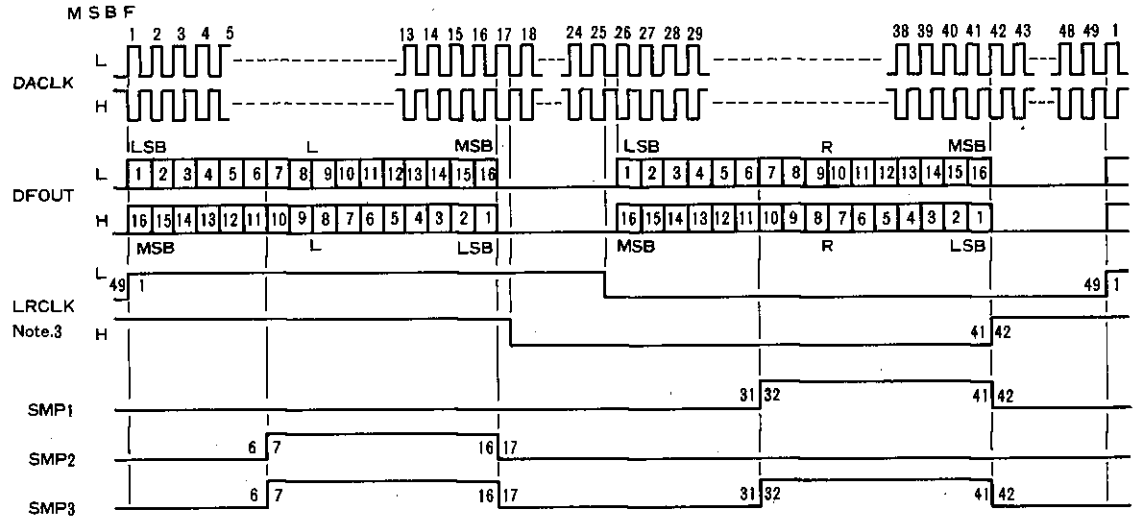
* The DACLK clock rate is the same as CK4 (4.3218 MHz).



LC7860N Digital Filter Output Data Format (DFOFF="H")

* In this format, input data is output without any processing. However, the DAC timing signal and the MSB First Out mode are effective.

* The DACLK clock rate is the same as CK2 (2.1609 MHz).

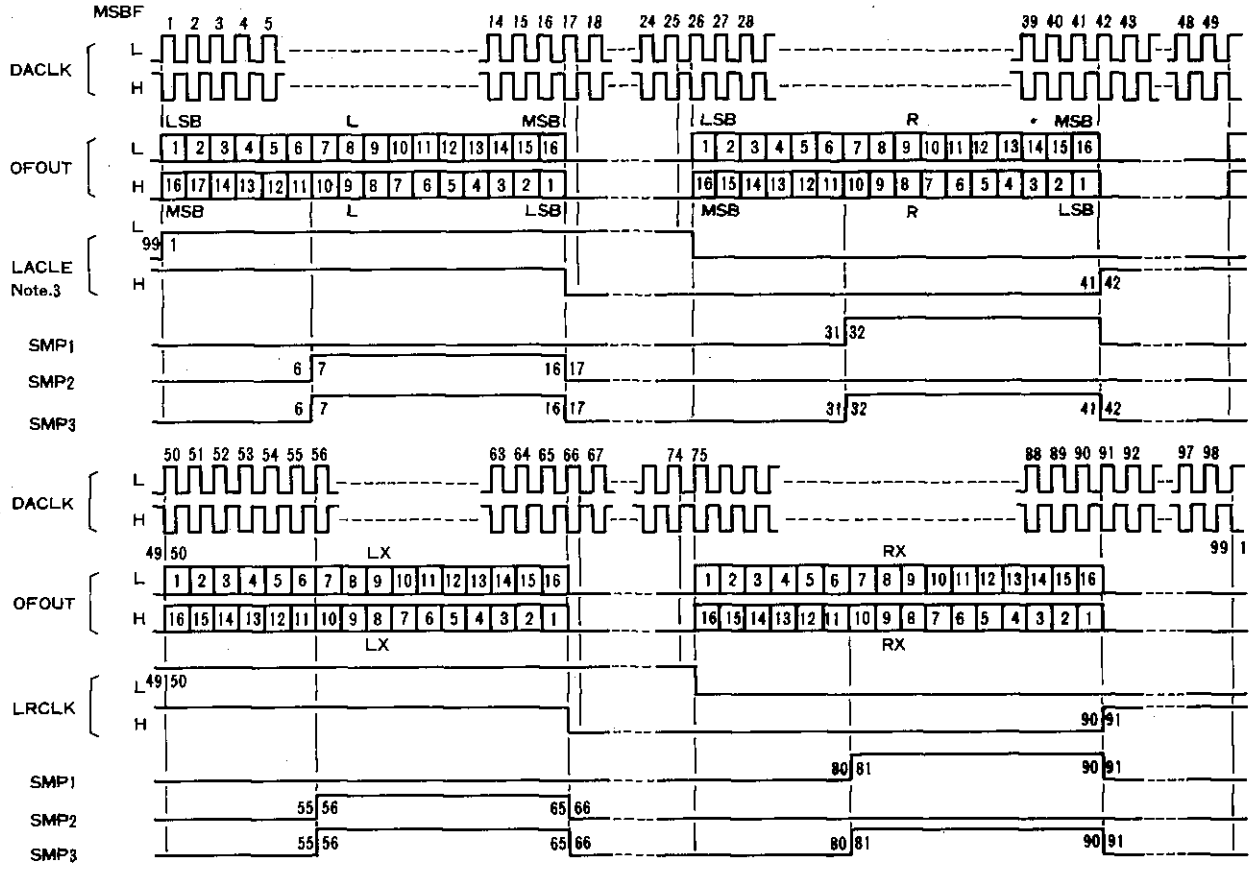


Note 3: LC7860N and LC7863 are different in the timing of LRCLK from each other.

CIRCUIT DESCRIPTION

LC7863 Digital Filter Output Data Format (DFOFF="L")

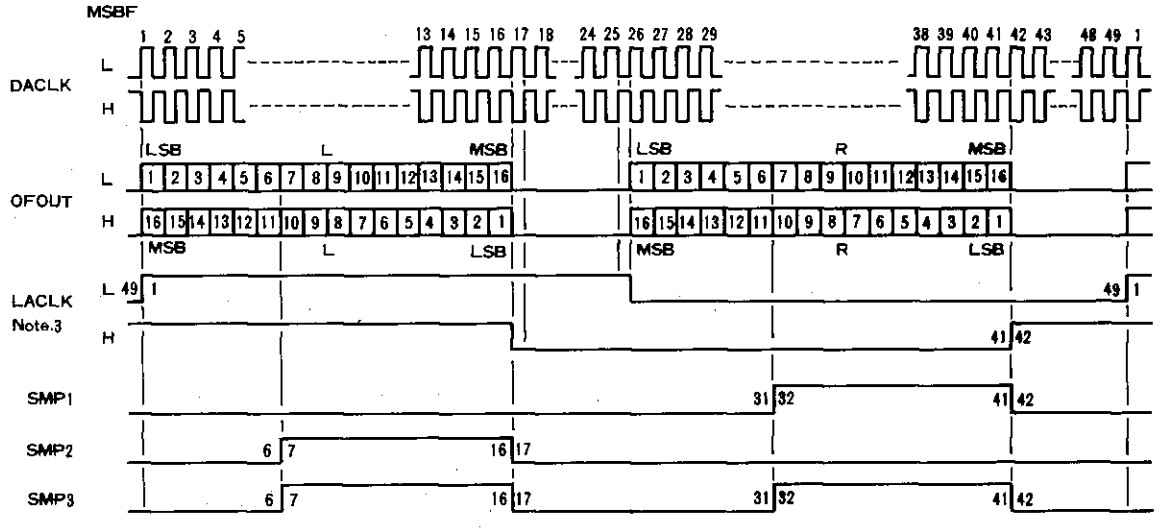
* The DACLK clock rate is the same as CK4 (4.3218 MHz).



LC7863 Digital Filter Output Data Format (DFOFF="H")

* In this format, input data is output without any processing. However, the DAC timing signal and the MSB First Out mode are effective.

* The DACLK clock rate is the same as CK2 (2.1609 MHz).

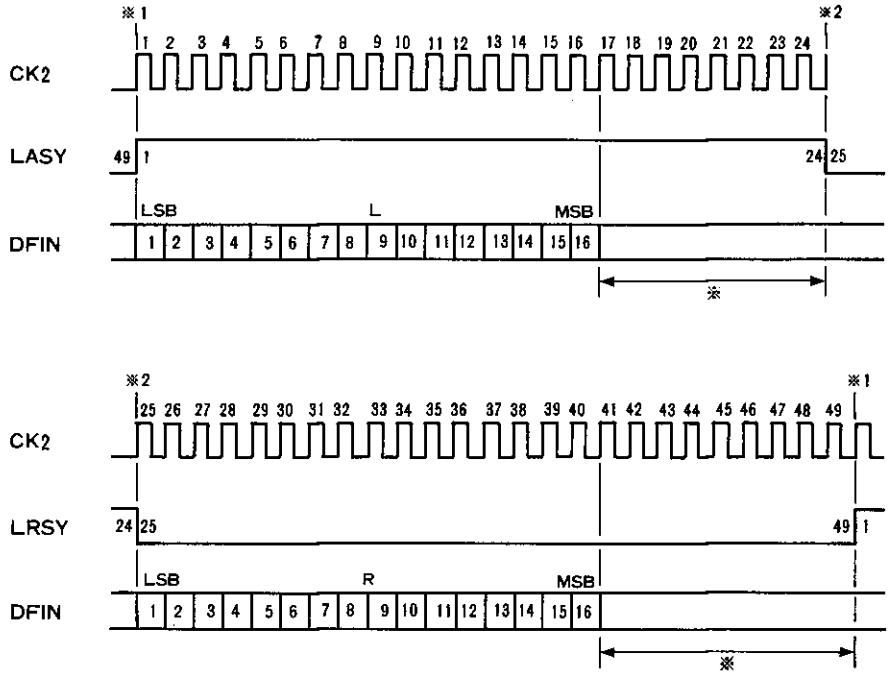


Note 3: LC7860N and LC7863 are different in the timing of LRCLK from each other.

CIRCUIT DESCRIPTION

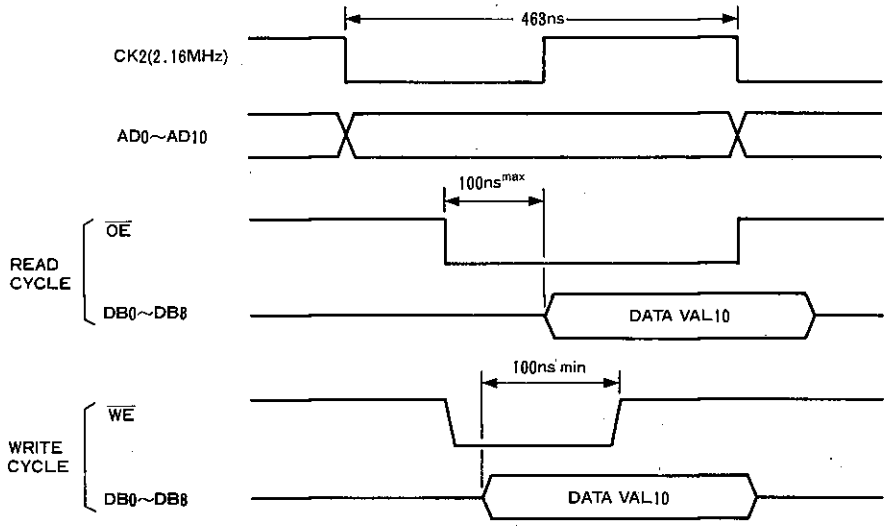
16) CDROM compatible output: pin 39 (CK2), pin 37 (LRSY), pin 36 (DFIN), pin 28 (DSPOFF), pin 64 (IOFF)
When DSPOFF is "L", the input signal to the digital filter from DFIN can be extracted. As regards data, the Lch data is obtained in synchronization with CK2 at the rise of LRSY in the LSB First Out mode, and the Rch data is also obtained in synchronization with CK2 at the rise of LRSY in the LSB First Out mode.
CK2 is a clock pulse of 2.1609 MHz. When DSPOFF is "H", it is feasible to input external signal from DFIN to the digital filter section. Mainly, this is for LSI testing.

LC7860N/LC7863 Digital Filter Input Data Format



*: When DSPOFF="L", the DSP signal is output, at which time the data for that marked period is the same as MSB.
When external signal is applied at DSPOFF="H", care is unnecessary for the data for that marked period.
When IOFF is made "H", it is feasible to stop interpolation and previous-value holding.

17) RAM interface: pin 41 (OE), pin 42 (WE), pins 40—52 (AD10—AD0), pins 53—61 (DB7—DB0)



Address signal, data signal and control signal to be connected with 2-Kbyte RAM

CIRCUIT DESCRIPTION

Block Operation

1) RAM address control

LC7860N or LC7863 deinterleaves the EFM demodulation data by means of address control over an external RAM of 8 bits ×2 Kwords. Its ability to absorb jitters from the input data covers +/—4 frames owing to its buffer memory capacity. In addition, this buffer memory is always checked for its marginal capacity. In this way, by the fine adjustment in the division ratio of the PCK side of the CLV servo circuit, it is so controlled that the data written address refers to the center of the buffer memory. Furthermore, in excess of the buffer memory capacity of +/—4 frames, the data written address is compulsorily set to +/—0, and since any error caused thereby cannot be treated with a flag, muting is applied for a period of 128 frames.

Position	Division ratio or treatment	
—4 or less	Compulsorily moved to +/—0	
—3	589	
—2	589	Advance division
—1	589	
±0	588	Standard division
+1	587	
+2	587	Recede division
+3	587	
+4 or more	Compulsorily moved to +/—0	

2) C1/C2 correction

The EFM demodulation data is written in an external RAM, then subjected to jitter absorption, and undergoes the following process at the fixed timing given by a clock pulse generated by a crystal oscillator. At first, performed in the C1 block are error check and correction, C1 flag determination and its writing to C1 flag register. In the next, performed in the C2 block are error check and correction, C2 flag determination and its writing to external RAM.

C1 check	Correction and flag treatment
No error	Correction unneeded, flag reset
1 error	Correction made, flag reset
2 errors	Correction made, flag set
3 or more errors	Uncorrectable, flag set

C2 check	Correction and flag treatment
No error	Correction unneeded, flag reset
1 error	Correction made, flag reset
2 errors	C1 flag is referred to. *1
3 or more errors	C1 flag is referred to. *2

*1:When the error position(s) determined in the C2 check are in agreement with the C1 flag(s), correction is performed and then flag resetting is performed. However, when the number of C1 flags is 3 or more, since faulty correction may be performed, no correction is made, and the C1 flags are taken as C2 flags as they are.

When one of the error positions is in agreement but not the other one, correction is not feasible. More, when the number of C1 flag(s) is 5 or less, since the results of the C1 check can be thought to be reliable, flag setting is made.

When the number of C1 flag is 6 or more, the error correction is taken impossible in the same manner as with "uncorrectable", and the C1 flags are taken as C2 flags as they are.

When none of the error positions is in agreement, correction is impossible as a matter of course. When the number of C1 flags is 2 or less, since even the data taken OK the C1 check can be assumed to be erroneous, flag setting is made.

Otherwise, C1 flag are taken as C2 flags.

*2:When correction is judged impossible with 3 or more errors, correction is not feasiable as a matter of course. When the number of C1 flag(s) is 2 or less, even the data taken OK in the C1 check can be assumed to be erroneous, flag setting is made.

3) Playback flag determination and interpolation

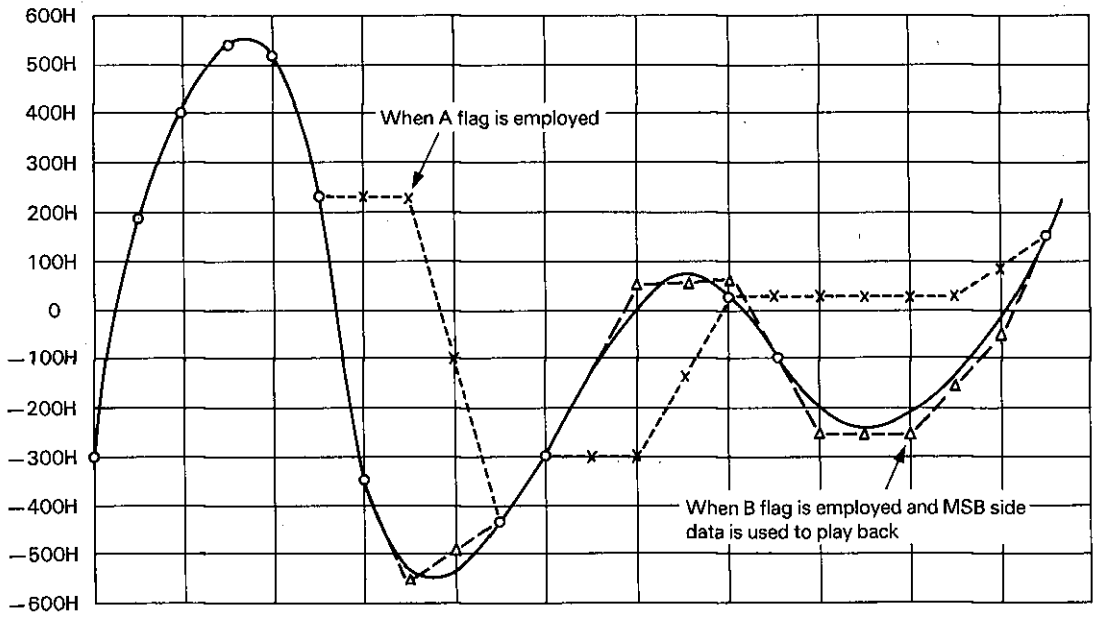
C2 flag		Playback flag
High-order	Low-order	
0	0	Reset
0	1	*
1	0	Set
1	1	Set

* When there is amplitude of more than 200H for preceding 8 samples, it is reset, while when there is not, it is set.

Until the C2 block, data is handled as symbols, each consisting of 8 bits. One sample consists of 16 bits, 8 bits of a high-order symbol and the rest 8 bits of a low-order symbol. Therefore, one sample is provided with two C2 flags. To perform data treatment such as by average value interpolation, previous value holding, etc., a value as close as possible to the true value is estimated from the preceding and following samples and is substituted into the erroneous sample. In this case, the error between the true value and the substitute value is small for small signal level and large for large signal level.

As to a sample of which the high-order symbol is not erroneous and only the low-order symbol is erroneous, 80H is substituted into the low-order symbol. In this case, the error is max. 80H, that it relatively small. Accordingly, in such occasions, when amplitude of more than 200H exists in the preceding 8 samples, the playback flag is reset. When only one sample is erroneous, average value interpolation is applied, while when two or more samples are erroneous continuously, previous value holding is applied.

CIRCUIT DESCRIPTION



A	0	0	0	0	0	1	1	1	0	0	1	1	1	0	1	1	1	1	1	1	0
B	0	0	0	0	0	0	0	1	0	0	1	0	1	0	1	0	1	0	1	0	0

A: When C2 flags of high- and low-order symbols are ORed to take the playback flag

B: When C2 flag of high-order symbol is taken as the playback flag as it is (LC7860N, LC7863)

4) Mute

Mute is feasible in −12 dB or −∞ dB. In either way, mute shifts in 4 steps gradually so as to reduce ON/OFF pop noises.

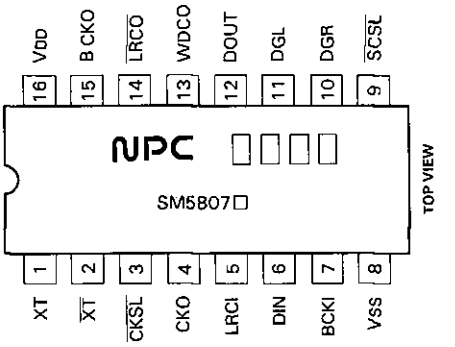
	0	1	2	3
−∞ dB	1	3/4	1/4	0
−12 dB	1	3/4	2/4	1/4

CIRCUIT DESCRIPTION

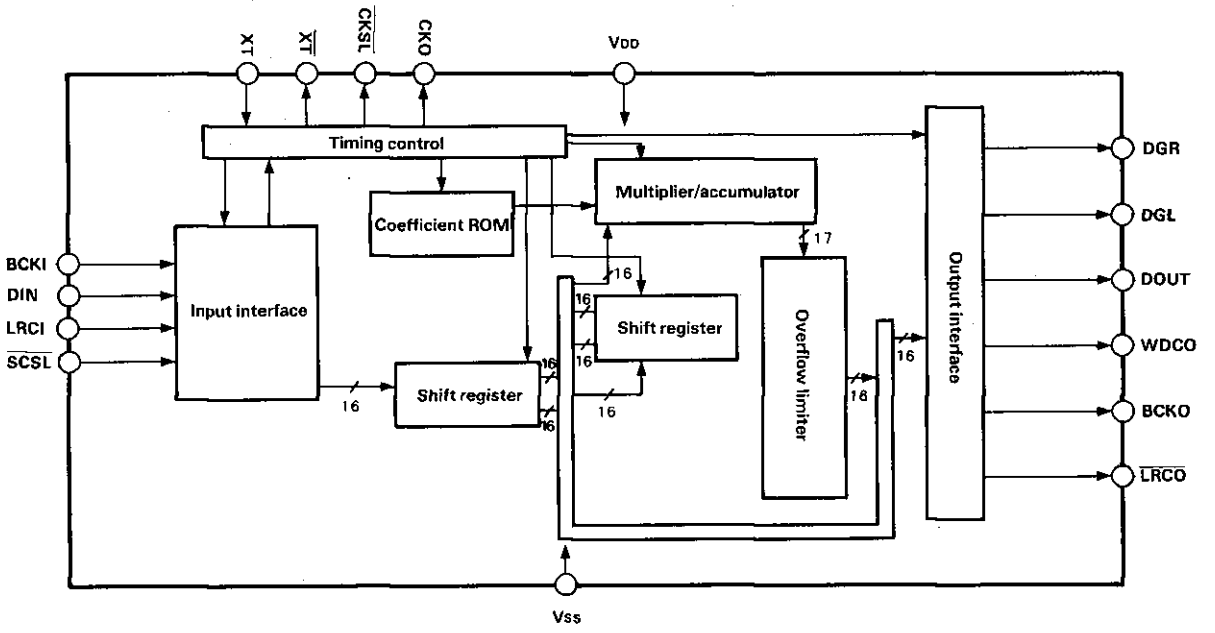
Oversampling digital filter (SM5807DP/EP)

The SM5807DP/EP is a 4x oversampling digital filter LSI for CD players which makes use of a molybdeum gate CMOS technology. In this LSI are incorporated digital filters for two channels. The 4x oversampling output can be obtained for each channel. By virtue of this, the analog filter configuration in the latter stage can be simplified.

Pin layout



Block diagram



Pin functions

Note: I: Input pin (Ip: pull-up resistance built-in)
O: Output pin

Pin No.	Pin Name	I/O	Function
1	XT	I	Oscillation section input pin
2	XT	O	Oscillation section output pin
3	CKSL	Ip	CKSL=H: X'tal OSC 16.9344 MHz or 17.2872 MHz or external input to XT CKSL=L: X'tal OSC 8.4672 MHz or 8.6436 MHz or external input to XT
4	CKO	O	Clock pulse output
5	LRCI	Ip	44.1 kHz sync clock pulse input
6	DIN	Ip	Serial data input
7	BCKI	Ip	Serial input bit clock pulse input
8	Vss		GND pin (0 V)
9	SCSL	Ip	SCSL=H: System clock pulse=192fs (fs: sampling frequency) SCSL=L: System clock pulse=196fs (fs: sampling frequency)
10	DGR	O	Rch deglitch signal (176.4 kHz)
11	DGL	O	Lch deglitch signal (176.4 kHz)
12	DOUT	O	Serial data output
13	WDCO	O	Output control clock pulse (352.8 kHz)
14	LRCO	O	Output control clock pulse (176.4 kHz)
15	BCKO	O	Serial output bit clock pulse (8.4672 MHz or 8.6436 MHz)
16	VDD		Power supply pin (5 V)

CIRCUIT DESCRIPTION

1. SM5807DP filter characteristic

(@ frequency 0 to 88.2 kHz)

Characteristic item	Performance
Pass band	0 ~ 20 kHz
Reject band	More than 24.1 kHz
Pass band ripple	Within +/−0.05 dB
Reject band attenuation (24.1 ~ 40 kHz) (40.0 kHz)	 More than 45 dB More than 50 dB

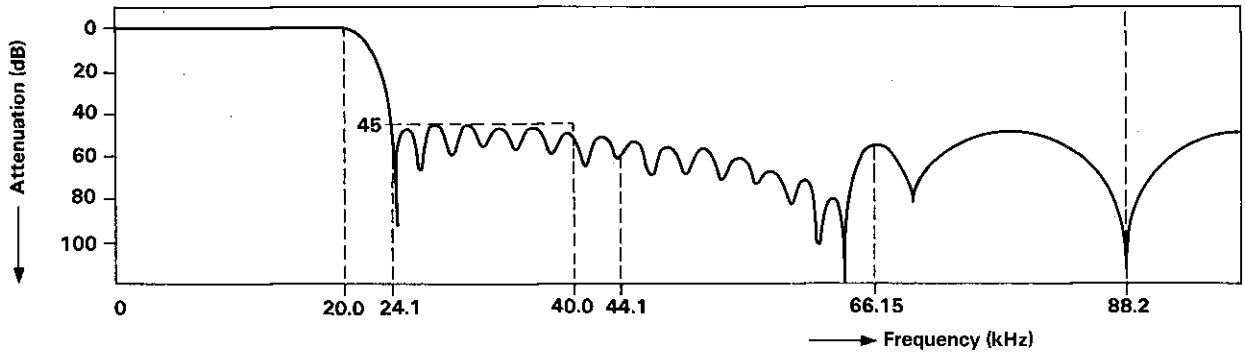


Figure 3-4 SM5807EP Frequency Characteristic

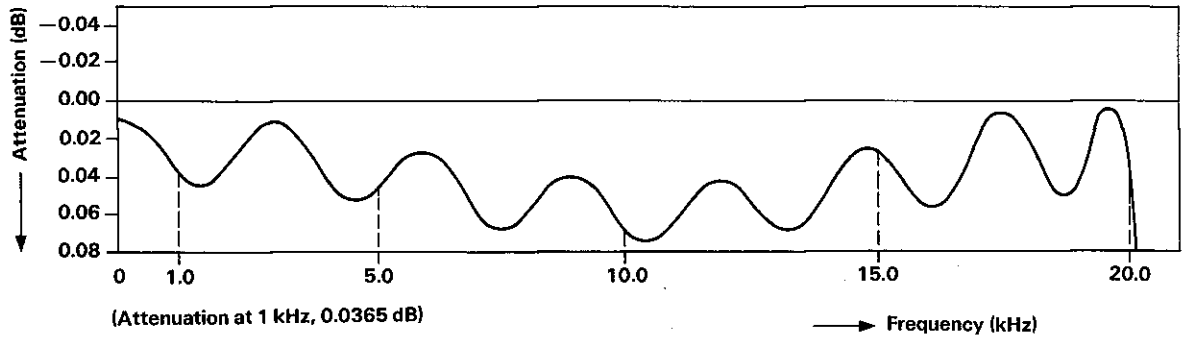


Figure 3-5 SM5807EP Pass Band Characteristic

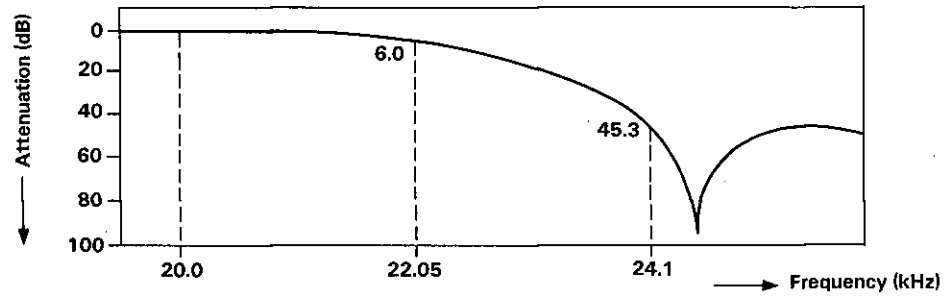


Figure 3-6 SM5807EP Transit Band Characteristic

CIRCUIT DESCRIPTION

2. SM5807EP filter characteristic

(@ frequency 0 to 88.2 kHz)

Characteristic item	Performance
Pass band	0 ~ 20 kHz
Reject band	More than 24.1 kHz
Pass band ripple	Within +/—0.05 dB
Reject band attenuation (more than 24.1 kHz)	More than 50 dB

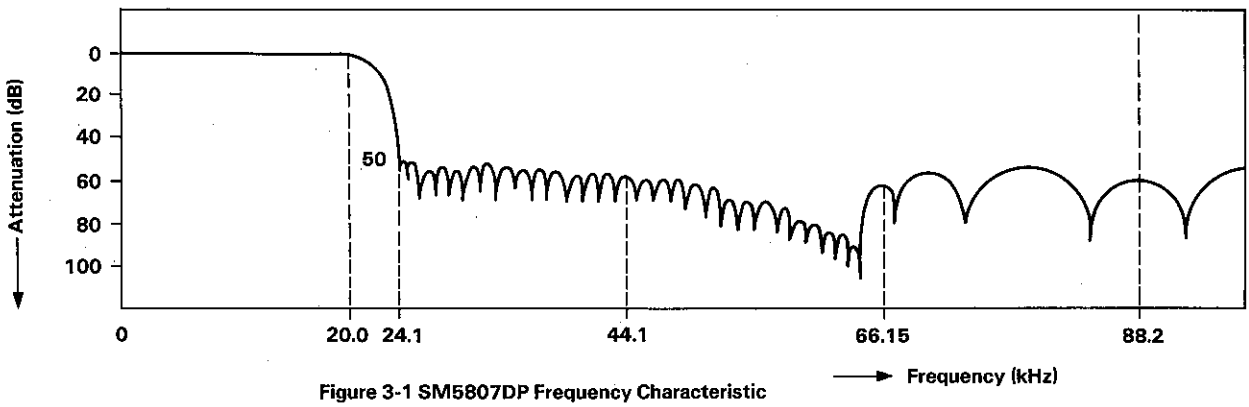


Figure 3-1 SM5807DP Frequency Characteristic

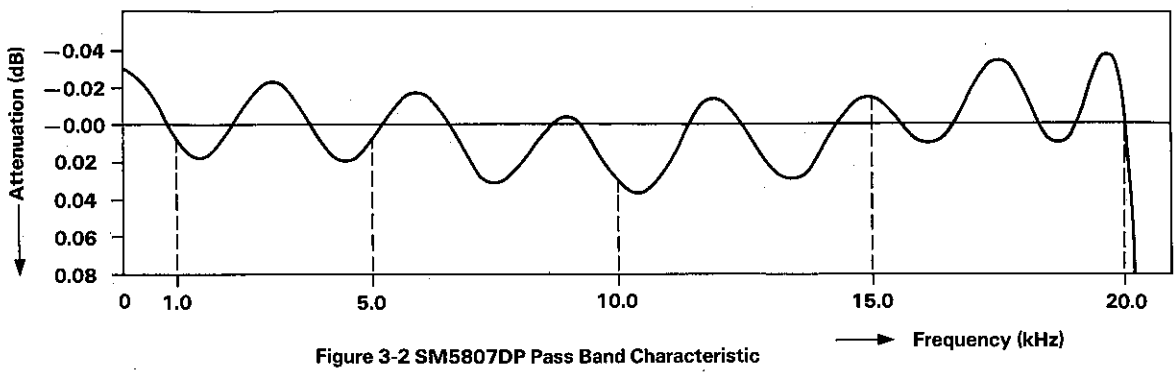


Figure 3-2 SM5807DP Pass Band Characteristic

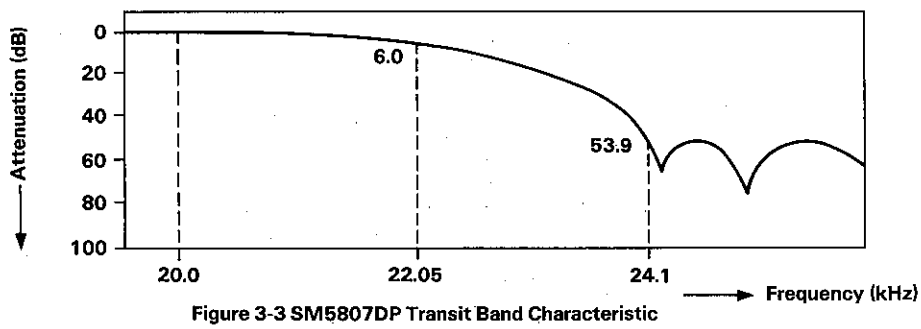


Figure 3-3 SM5807DP Transit Band Characteristic

CIRCUIT DESCRIPTION

Functions

4x oversampling

In this LSI are built digital filters for 2 channels. A 4x oversampling output can be thus obtained for each channel.
In this LSI, linear phase FIR filters, each of which provides 2x oversampling action, are cascade connected in two stages. That basic configuration is as shown in Figure 9-1.
The input signal sampled at 44.1 kHz is converted into a signal sampled at 88.2 kHz by the 2x oversampling action of the 61-ary first digital filter. In the 13-ary second digital filter, the input signal sampled at 88.2 kHz is also further subject to 2x oversampling and is output as a signal sampled at 176.4 kHz, four times the input of the first digital filter.

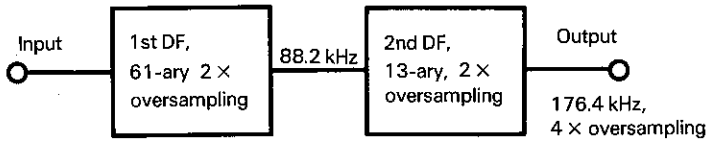


Figure 9-1 4 × Oversampling Process

System clock pulse

Of this LSI, the system clock pulse is available in 192fs=8.4672 MHz or 196fs=8.6436 MHz, from which one is selected by the SCSL pin. (fs=44.1 kHz)

SCSL=H (or open) —192fs (compatible with 96fs system clock pulse)
SCSL=L —196fs (compatible with 98fs system clock pulse)

Clock pulse generation method

$\overline{SCSL}$	H (or open)		L	
$\overline{CKSL}$	H (or open)	L	H (or open)	L
Clock pulse generation method	X'tal OSC/ external input	X'tal OSC/ external input	X'tal OSC/ external input	X'tal OSC/ external input
XT/$\overline{XT}$ input frequency	384fs=16.9344 MHz	192fs=8.4672 MHz	392fs=17.2872 MHz	196fs=8.6436 MHz
Clock pulse output ($CK\overline{O}$)	↑	↑	↑	↑
System clock pulse (internal)	192fs=8.4672 MHz	↑	196fs=8.6436 MHz	↑

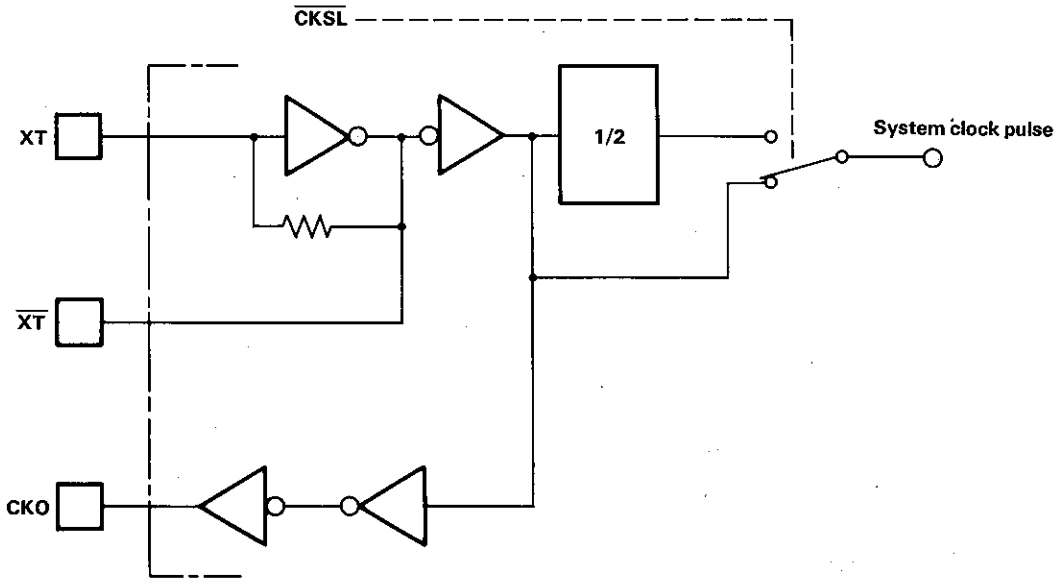
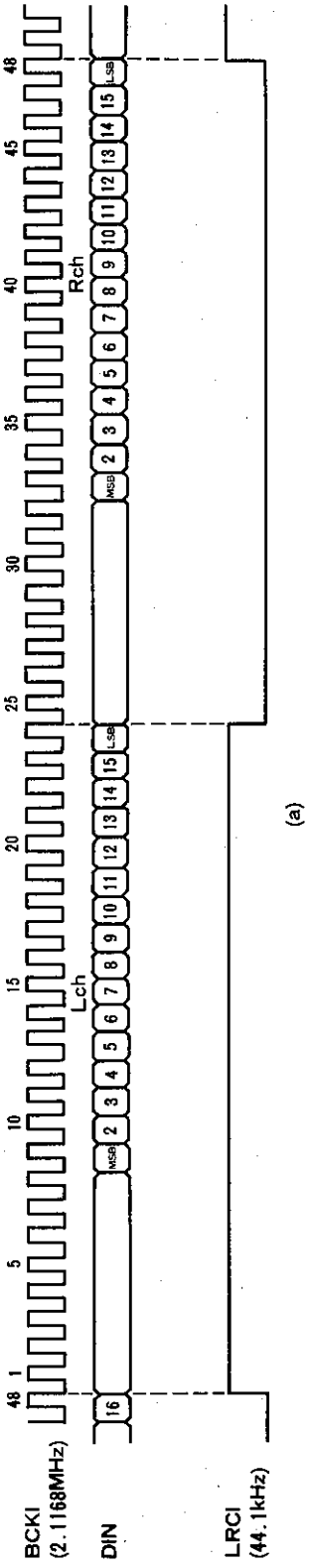


Figure 9-2 Clock Pulse Generation Circuit

CIRCUIT DESCRIPTION

10. Timing charts



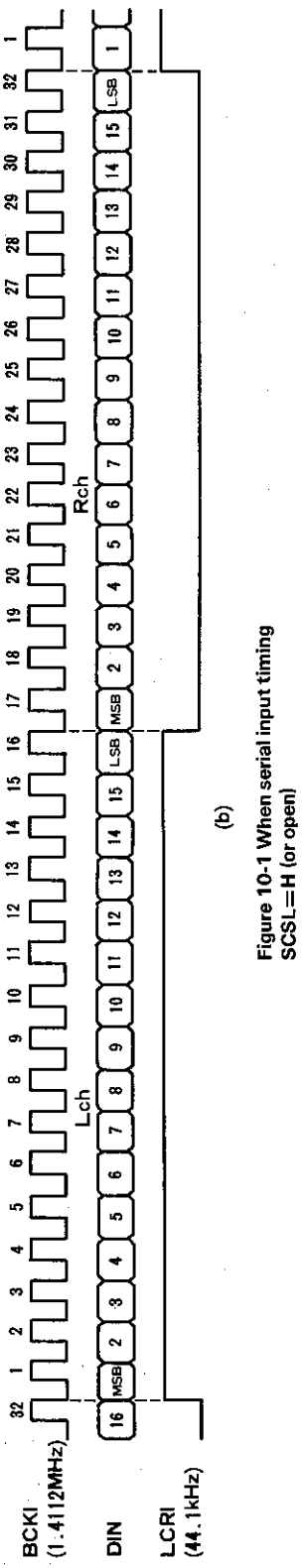


Figure 10-1 When serial input timing
SCSL=H (or open)

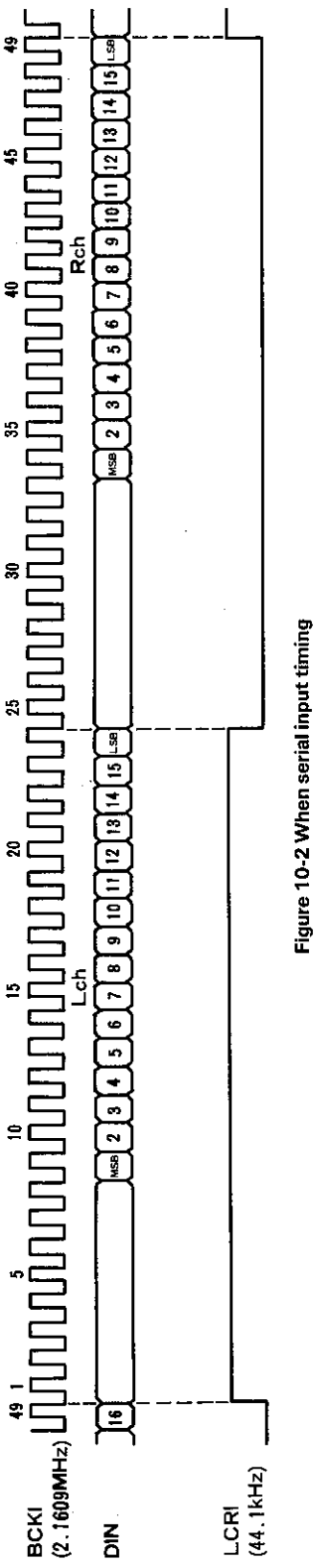


Figure 10-2 When serial input timing
SCSL=L

CIRCUIT DESCRIPTION

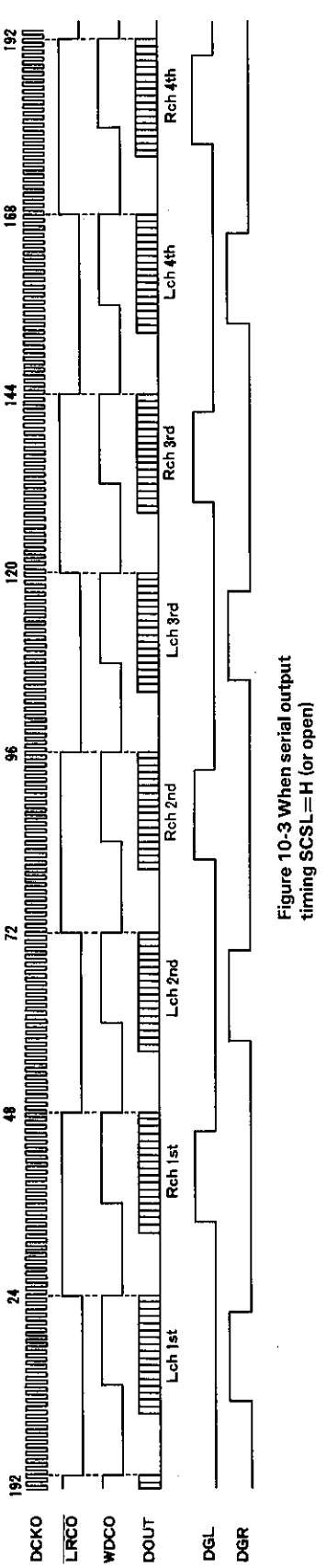


Figure 10-3 When serial output timing SCSL=H (or open)

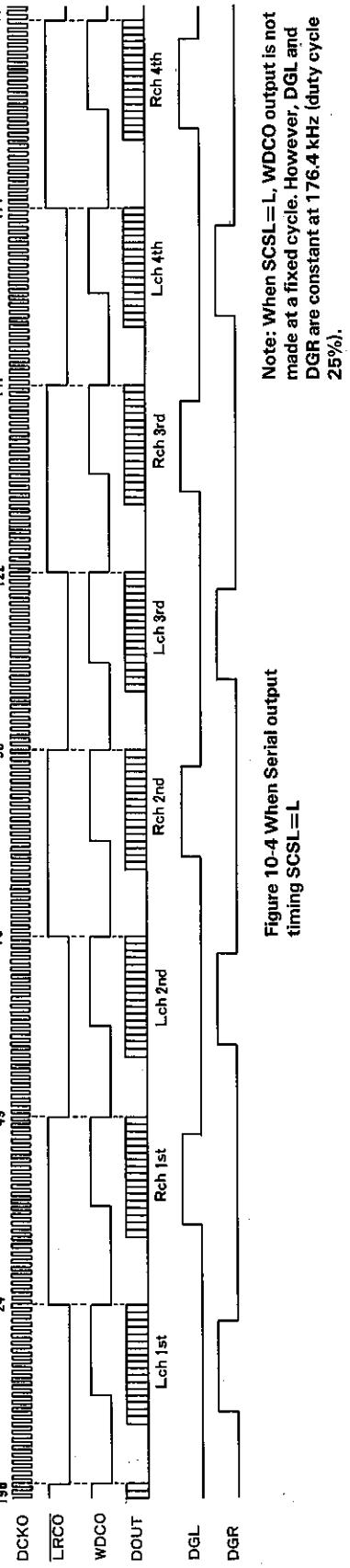


Figure 10-4 When Serial output timing SCSL=L

Note: When SCSL=L, WDCO output is not made at a fixed cycle. However, DGL and DGR are constant at 176.4 kHz (duty cycle 25%).

CIRCUIT DESCRIPTION

Serial input (data and bit clock pulse)

The serial input data is input at the rise of serial input bit clock pulse BCKI. Thus, the data should be changed at the fall of BCKI. The data is latched in internal registers due to sync clock pulse LRCI after input of 16 bits. The data shall be input in the 2's complement and MSB First mode.

Operation start

The operation is started at the rise of sync clock LRCI.

Serial output (data and bit clock pulse)

The Lch/Rch serial data are output alternately from DOUT. By virtue of this, the use of one D/A converter suffices for D/A conversion. In addition, at this point, the use of a few externally connected circuits (two gates) enables the in-phase conversion using two D/A converters. The data is output in the 2's complement and MSB First mode.

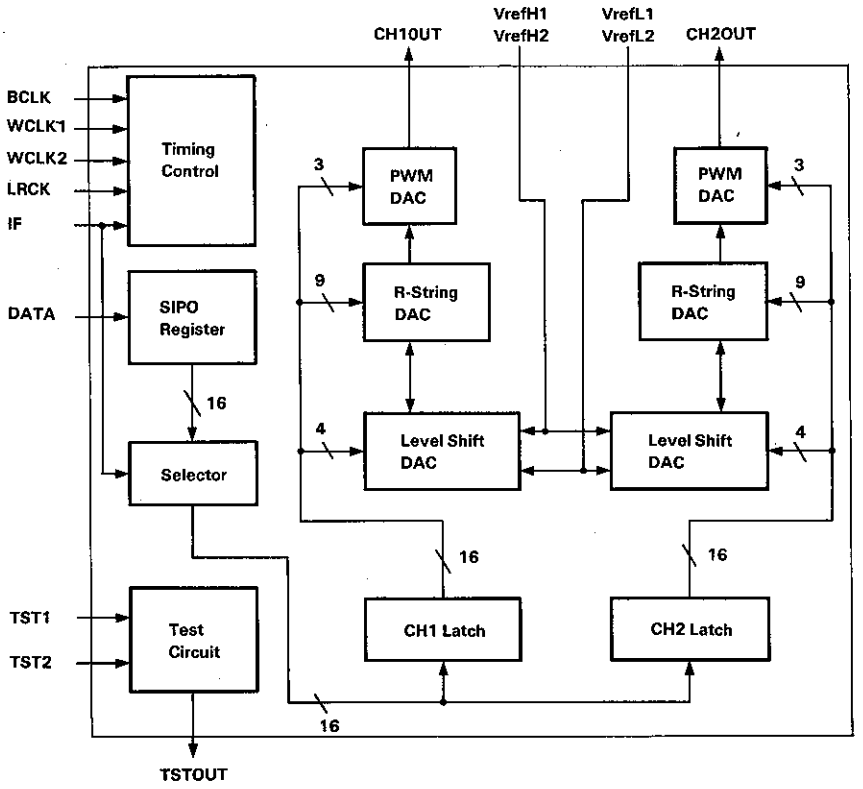
The serial output bit clock pulse is output from the BCKO pin. Since the data changes in synchronization with the rise of this bit clock pulse, the data can be input to a D/A converter at the rise of the bit clock pulse.

BCKO=8.4672 MHz—
(SCSL=H or open—System clock pulse=192fs)
BCKO=8.6436 MHz—
(SCSL=L —System clock pulse=196fs)

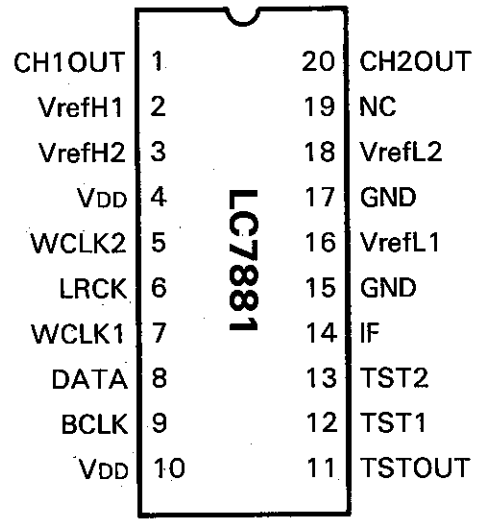
Deglitch signals

DGL—Lch deglitch signal, 176.4 kHz (duty cycle 25%)
DGR—Rch deglitch signal, 176.4 kHz (duty cycle 25%)

Block diagram



Pin layout



DP-48

Pin functions

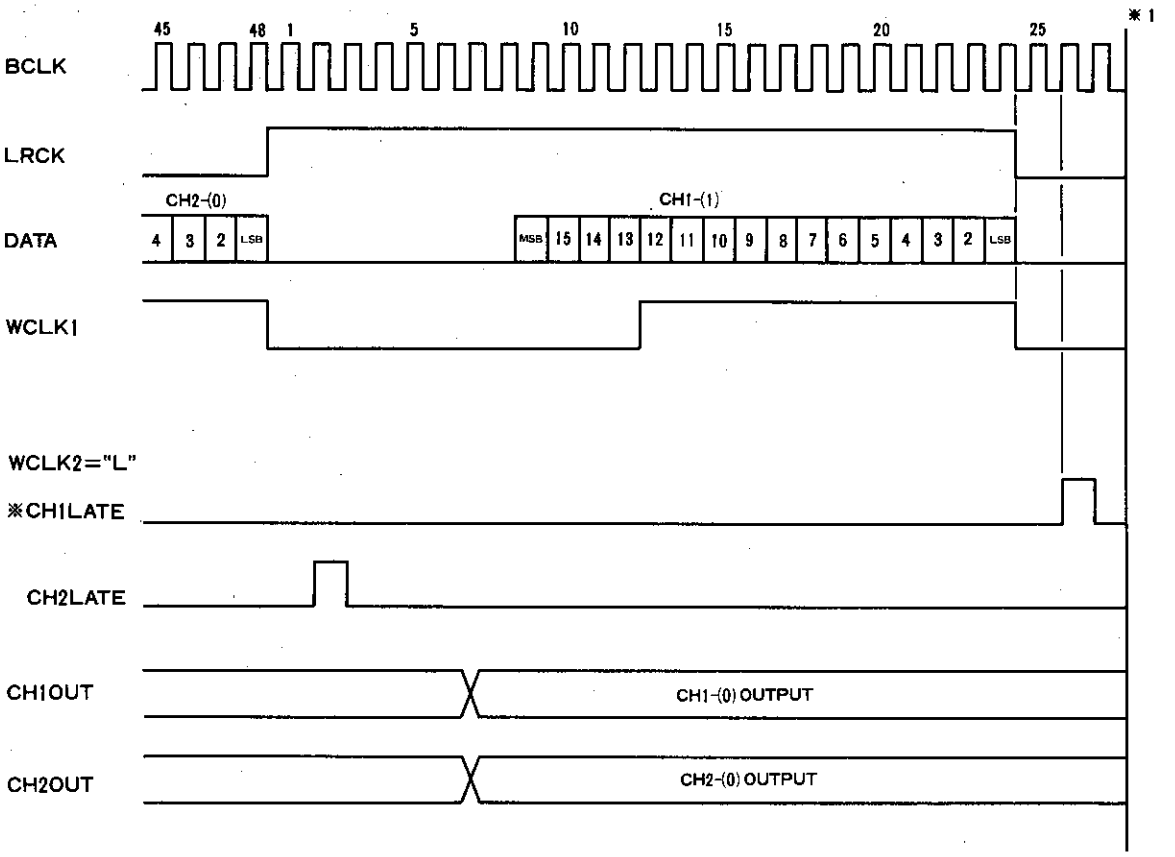
Pin No.	Pin Name	Function
1	CH1OUT	CH1 output pin
2	VrefH1	Reference voltage "H" input pin 1
3	VrefH2	Reference voltage "H" input pin 2
4	VDD	Supply voltage pin +5 V
5	WCLK2	Word clock pulse 2 input pin At IF="H", WCLK2 needs to be made "L". At IF="L", an internal signal by which the digital audio data of CH1 is latched is generated using the fall of WCLK2.
6	LRCK	LR clock pulse input This pin serves to indicate which channel of input digital audio data is engaged, CH1 or CH2. At LRCK="H", CH1 is engaged. At LRCK="L", CH2 is engaged.
7	WCLK1	Word clock pulse 1 input pin At IF="H", an internal signal by which the data of both channels CH1 and CH2 is latched is generated using the fall of WCLK1. At IF="L", an internal signal by which the digital audio data of CH2 is latched is generated using the fall of WCLK1.
8	DATA	Digital audio data input pin At IF="H", data is input in the bit serial mode from the MSB side. AT IF="L", data is input in the bit serial mode from the LSB side.
9	BCLK	Bit clock pulse pin Clock pulse by which digital audio data is input in the LSI in the bit serial mode. And, clock pulse for PWMDAC
10	VDD	Supply voltage pin +5 V
11	TSTOUT	Test output pin. Normally open.
12	TST1	Test input pin. Normally connected to GND.
13	TST2	
14	IF	Interface select pin At IF="H", digital audio data is input in the MSB First mode. At IF="L", digital audio data is input in the LSB first mode.
15	GND	GND pin
16	VrefL1	Reference voltage "L" input pin 1
17	GND	GND pin
18	VrefL2	Reference voltage "L" input pin 2
19	NC	NO CONNECTION
20	CH2OUT	CH2 output pin

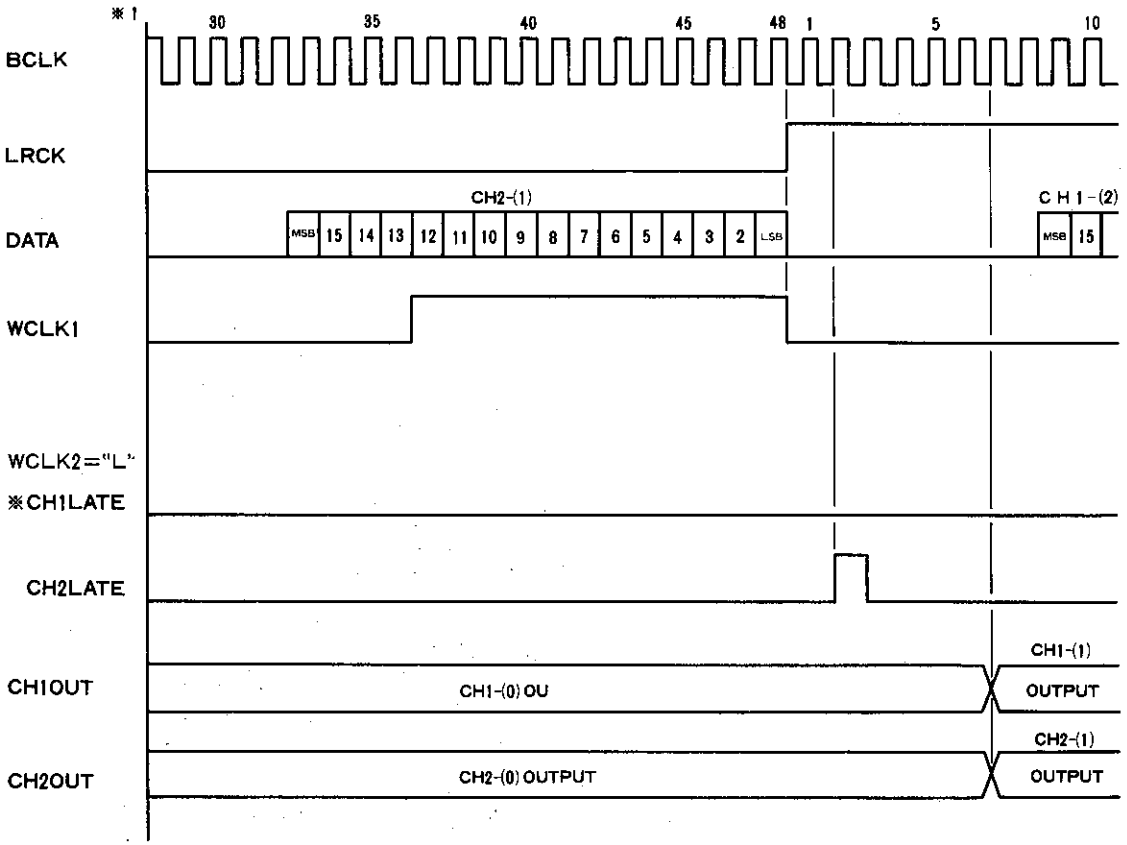
CIRCUIT DESCRIPTION

Timing diagram

At IF="H"

* CH1LATE and CH2LATE are internal signals.

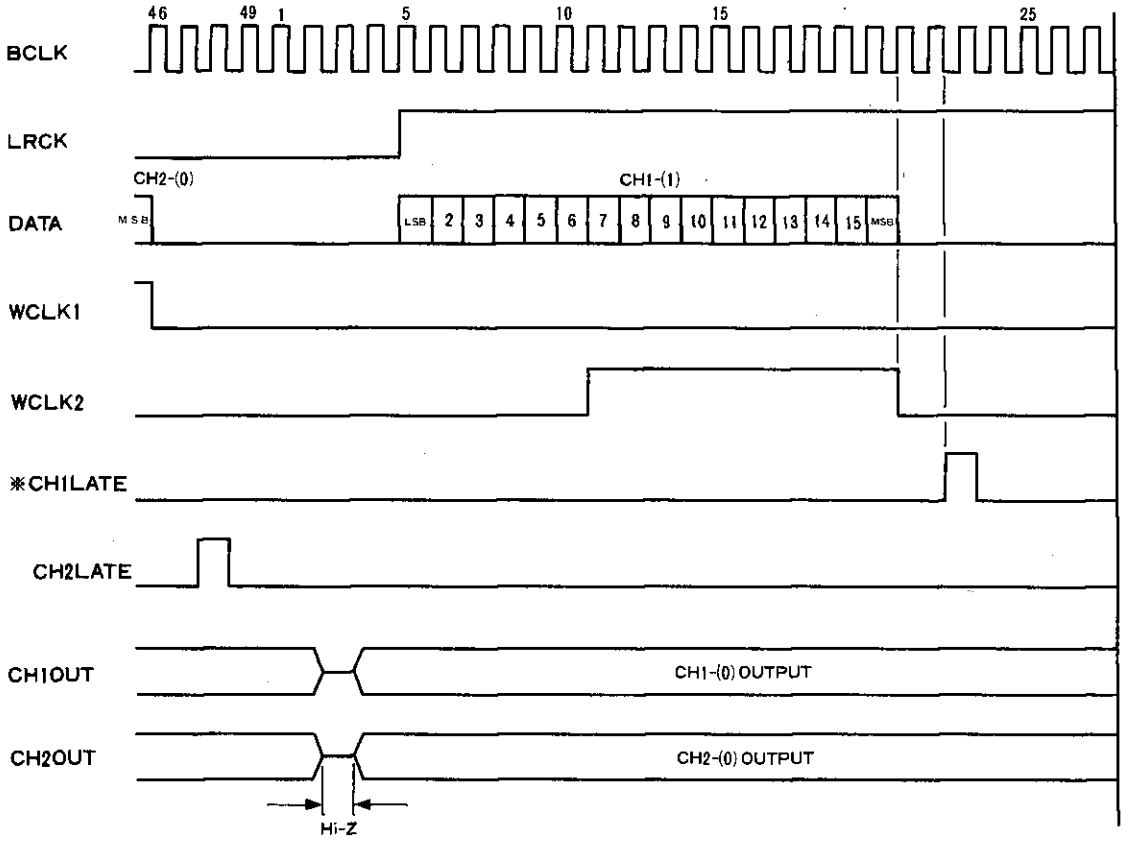


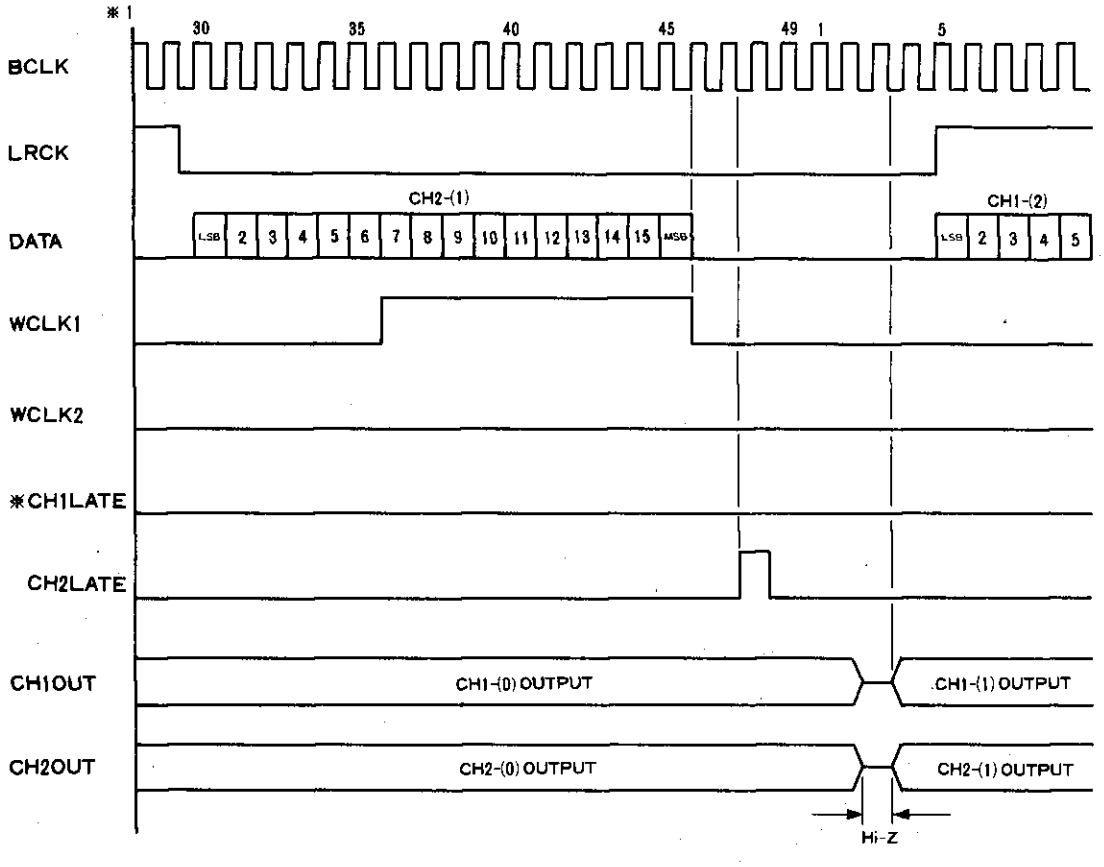


CIRCUIT DESCRIPTION

At IF="L"

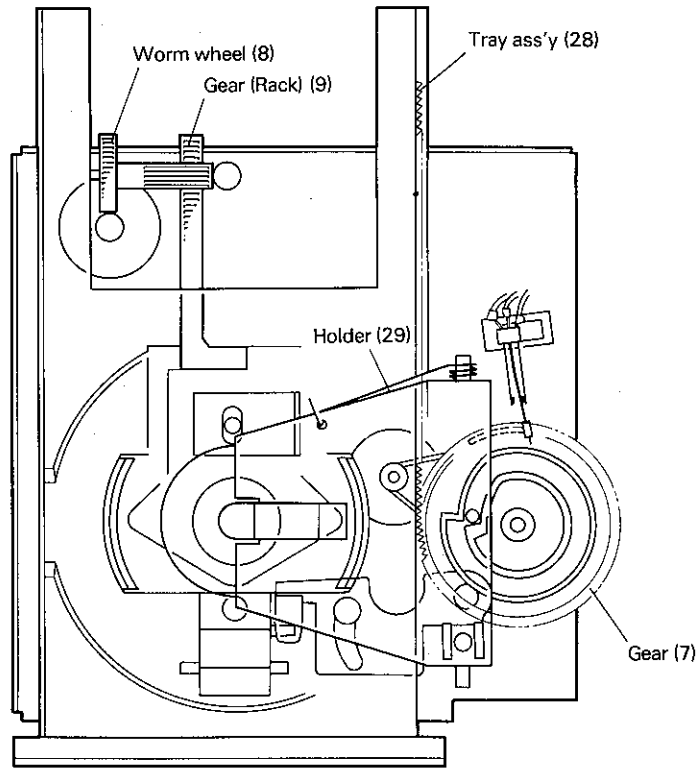
* CH1LATE and CH2LATE are internal signals.





MECHANISM DESCRIPTION

The figure on the upper right side shows the positional relationship of the mechanism in the STOP mode.



Stop Mode

In the disc loading and unloading operations, the tray is opened and closed as described below.

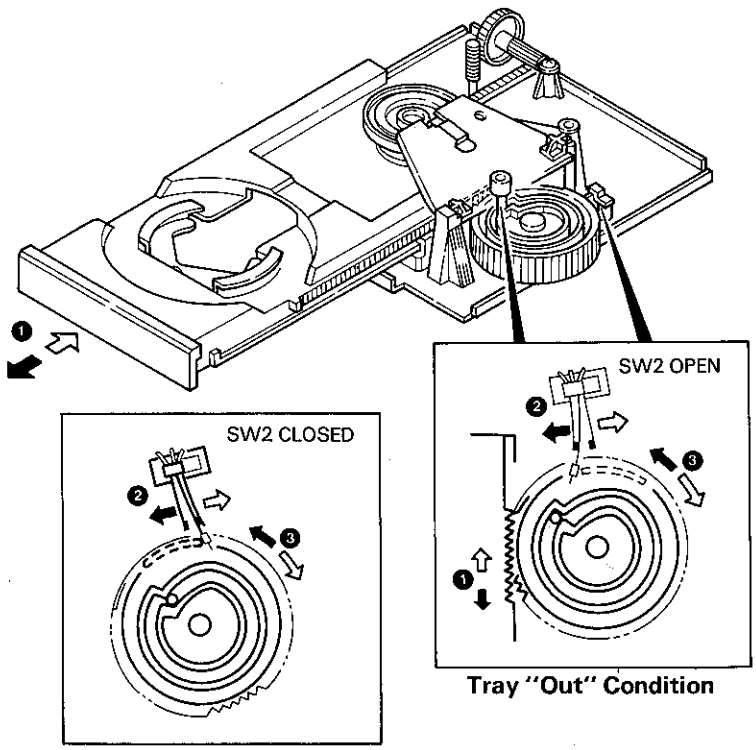
Note: The diagrams accompanying the following operation description include black and white arrows.
Black arrow: indicates the direction in which the tray opens.
White arrow: indicates the direction in which the tray is closed.

The numbers inside ( ) put after the parts names in the following description indicate the reference Nos. in the enlarged view diagram shown in the Service Manual.

When the tray is closed, the OPEN/CLOSE detector leaf switch on the chassis (SW2) is depressed rightward.

When the OPEN/CLOSE switch on the front panel is pressed, the loading motor (M3) starts rotation in the counterclockwise direction, and the rotation is transmitted via the belt to the geared pulley (10). The rotation force is then transmitted to the large-sized white gear (7), which pushes the tray out. When the OPEN/CLOSE or PLAY switch is pressed, the same loading motor (M3) as used in the opening operation rotates again (in the clockwise direction) to pull in the tray.

If an opened tray is pushed in forcibly, the detector leaf switch (SW2) is pressed rightward, the same loading (M3) as used in the opening operation rotates (in the clockwise direction) to pull in the tray.



Tray "Out" Condition

Tray "In" Condition

CLOSE ⇦ ➡ OPEN

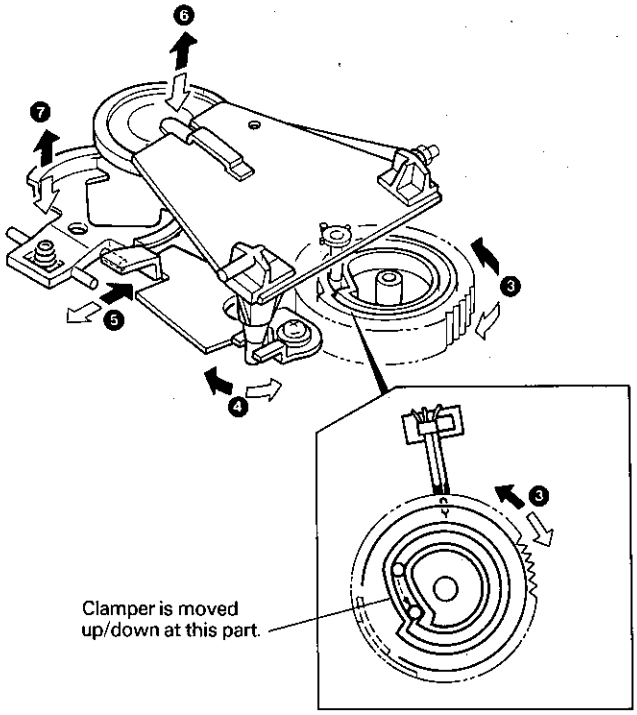
MECHANISM DESCRIPTION

Tray opening operation

The large white gear (10) rotates counterclockwise, and the clamper (29) is moved upward by the engagement of the gear (10) with the clamper's projecting part. (As the groove of the white pulley is not round, the clamper's projecting part is first pulled toward the outside then pushed toward the center. The clamper (29) is moved upward when the projecting part is pushed toward the center.)
At this time, the projection at the extremity of the clamper releases the holder (25), moving the disc upward.

Tray closing operation

The large white gear (10) rotates clockwise. When the clamper's projecting part approaches the end of the groove, it is pulled toward the center of the white gear and the clamper (29) is moved downward.
When the clamper (29) starts to move downward, the projection at the extremity of the clamper (29) moves the holder (25) downward via the arm.



ADJUSTMENT

No.	ITEM	INPUT SETTINGS	OUTPUT SETTINGS	CD PLAYER SETTINGS	ALIGNMENT POINTS	ALIGN FOR	FIG.
1	LASER POWER	–	Set the sensor of the laser power meter on the pickup lens.	Measure after setting the Power switch to ON. Be quick for the laser power is switched OFF in a few seconds. Repeat this measurement a few times.	–	0.15 to 0.25mW(The pickup is OK if, with the power within this range, the RF level is 1.5Vp-p or more, TE(Servo Open) is 2.0Vp-p or more, and the diffraction grating is correct is aligned.)	(a)
2	VCO	–	Connect a frequency counter to TP4(VCO).	STOP	L502	4.32MHz	(b)
3	TRACKING DC OFFSET	–	Connect an oscilloscope to TP3-2.	STOP (Short-circuit TP7 and GND. After the adjustment, release the shorting pin.)	SF504	0V	(c)
4	FOCUS DC OFFSET	Test disc Type 4	Connect an oscilloscope to TP4(HF).	STOP	SF501	Optimum eye pattern.	(d)
5	TRACKING ERROR BALANCE	Test disc Type 4	Connect an oscilloscope (or DC voltmeter) to TP1(TE).	PLAY Short-circuit TP8 with GND. Be quick, for the servo loop Open condition is released in about 5 seconds after shorting TP8. After the adjustment, release the shorting pin.	SF503	Symmetry between upper and lower patterns, or DC=0±0.05V	(e)
6	TRACKING GAIN	Test disc Type 4 Oscillator (1kHz, 0.5Vp-p)	Connect an oscillator and VTVM to TP3-1 and TP3-2.	PLAY	SF505	Two VTVM should read the same value.	(f)
7	FOCUS GAIN	Test disc Type 4 Oscillator (1kHz, 0.5Vp-p)	Connect an oscillator and VTVM to TP2-1 and TP2-2.	PLAY	SF502	Two VTVM should read the same value.	(f)

(Note) Type 4 disc: SONY YEDS-18 Test Disc or equivalent.

REGLAGE

N°	ITEM	REGLAGE D'ENTREE	REGLAGE DE SORTIE	REGLAGE DE LA LECTURE	POINT DE L'ALIGNEMENT	ALIGNER POUR	FIG
1	ALIMENTATION LASER	–	Placer le détecteur du compteur de puissance laser sur le capteur.	Mesurer après avoir réglé l'interrupteur d'alimentation sur ON. Etre rapide car l'alimentation au laser est coupée en quelques secondes. Répéter cette mesure plusieurs fois.	–	0,15 à 0,25mW(le capteur est correct si, avec l'alimentation dans cette gamme, le niveau RF est de 1,5 Vc-c ou plus, TE servo ouvert) est de 2Vc-c ou plus et le réseau de diffraction correct aligné.)	(a)
2	VCO	–	Raccorder le compteur de fréquence à TP4(VCO).	STOP	L502	4.32MHz	(b)
3	DECALAGE CC D'ALIGNEMENT	–	Raccorder un oscilloscope à TP3-2.	STOP (Court-circuiter TP7 et GND. Aprés l'ajustement, relâcher la broche court-circuit.)	SF504	0V	(c)
4	DÉCALAGE CC DE MISE AU POINT	Disqur test Type 4	Raccorder un oscilloscope à TP4(HF).	STOP	SF501	Forme optimum	(d)
5	EQUILIBRE D'ERREUR D'ALIGNEMENT	Disque test Type 4	Raccorder un oscilloscope (ou un voltmètre CC) à TP1(TE).	PLAY Court-circuiter TP8 avec GND. Etre rapide car la condition d'ouverture de la boucle servo est relâchée environ dans les 5 secondes qui suivent le court-circuit de TP8. Après l'ajustement, relâcher la broche court-circuit.	SF503	Symétrie entre les formes supérieure et inférieure ou DC=0±0,05V	(e)
6	GAIN D'ALIGNEMENT	Disque test Type 4 Oscillateur (1kHz, 0,5Vc-c)	Raccorder un oscillateur et un voltmètre électronique à TP3-1 et TP3-2.	PLAY	SF505	Deux voltmètres électroniques doivent donner la même valeur.	(f)
7	GAIN DE MESE AU POINT	Disque test Type 4 Oscillateur (1kHz, 0,5Vc-c)	Raccorder un oscillateur et un voltmètre électronique à TP2-1 et TP2-2.	PLAY	SF502	Deux voltmètres électroniques doivent donner la même valeur.	(f)

(Remarque) Disque de type 4:Disque test SONY YEDS-18 ou équivalent.

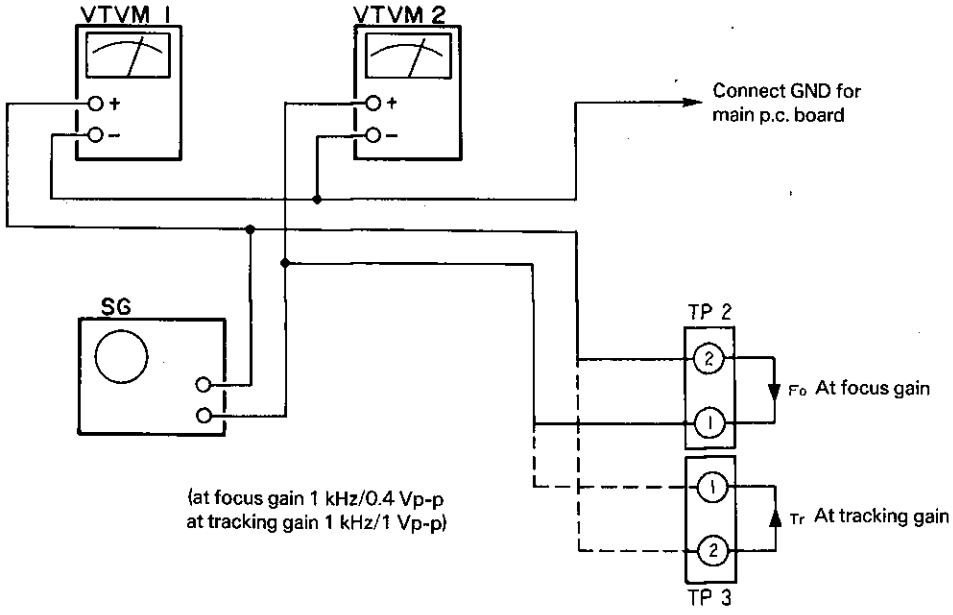
ABGLEICH

NR.	GEGENSTAND	EINGANGS-EINSTELLUNG	AUSGANGS-EINSTELLUNG	SPIELER-EINSTELLUNG	ABGLEICH-PUNKTE	ABGLEICHEN FÜR	ABB.
1	LASERLEISTUNG	–	Den Sensor des Laserleistungs-meters auf den Tonabnehmer setzen.	Nach Einschalten des Netzschalters messen. Schnell messen, weil der Laser innerhalb weniger Sekunden ausgeschaltet wird. Diese Messung mehrmals wiederholen.	–	0,15 bis 0,25mW(Die Abtast-teinheit ist einwandfrei, wenn die Werte innerhalb dieses Bereiches liegen und der HF-Pegel 1,5Vs-s oder größer ist, TE(Servo Open) 2,0Vs-s oder größer ist und das Diff-raktionsgitter korrekt ausgerichtet ist.)	(a)
2	VCO	–	Einen Frequenzmesser an TP4(VCO) anschließen.	STOP	L502	4,32MHz	(b)
3	SPURHALTE-DC-VERSATZ	–	Ein Oszilloskop an TP3-2 anschließen.	STOP (TP7 und GND Kurzschließen. Nach erfolgter Einstellung den Kurzschlußstift freigegen.)	SF504	0V	(c)
4	FOKUS-DC-VERSATZ	Testdisc Typ 4	Ein Oszilloskop an TP4(HF) anschließen.	STOP	SF501	Optimales Augenmusten	(d)
5	SPURHALTE-FEHLERBALANCE	Testdisc Typ 4	Ein Oszilloskop (oder Gleichstrom-Voltmeter) an TP1(TE) anschließen.	PLAY TP8 an Masse Kurz-schließen. Keine Zeit verlieren, weil der Offen-Zustand der Servo-schleife ca.5 Sekunden nach Kurzscließen von TP8 freigegeben wird. Nach erfolgter Einstellung den Kurz-schlußstift freigegen.	SF503	Symmetrie zwischen oberen und umteren Mustern oder Gleichstrom DC=0±0,05V	(e)
6	SPURHALTE-VERSTÄRKUNG	Testdisc Typ 4 Oszillator (1kHz, 0,5Vs-s)	Einen Oszillator und ein Röhrenvolt-meter an TP3-1 und TP3-2 anschließen.	PLAY	SF505	Die beiden Röhrenvolt-meter müssen den gleichen Wert anzeigen.	(f)
7	FOKUS-VERSTÄRKUNG	Testdisc Typ 4 Oszillator (1kHz, 0,5Vs-s)	Einen Oszillator und ein Röhrenvolt-meter an TP2-1 und TP2-2 anschließen.	PLAY	SF502	Die beiden Röhrenvolt-meter müssen den gleichen Wert anzeigen.	(f)

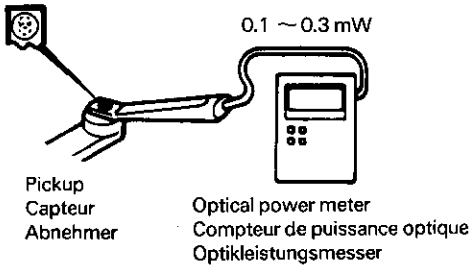
(Hinweis) Typ 4 Disc: SONY YEDS-18 Testdisc oder Äquivalent.

ADJUSTMENT/REGLAGE/ABGLEICH

(f) Focus Gain and Tracking Gain

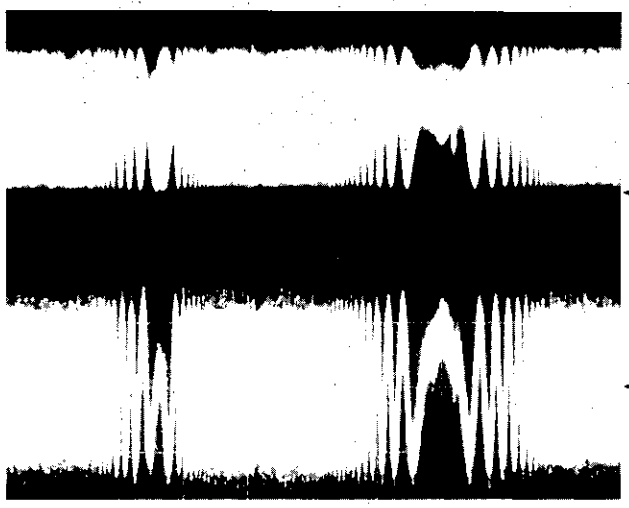


(a) Laser Power



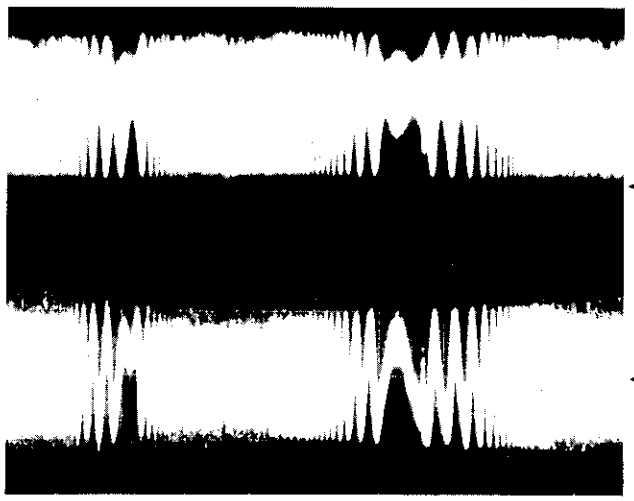
ADJUSTMENT/REGLAGE/ABGLEICH

DIFFRACTION GRID ADJUSTMENT/REGLAGE DU RESEAU DE DIFFRACTION/BEUGUNGSGITTER-EINSTELLUNG



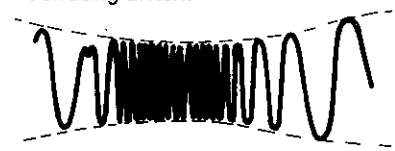
(Photo. 1)
(Photo. 1)
(Foto. 1)

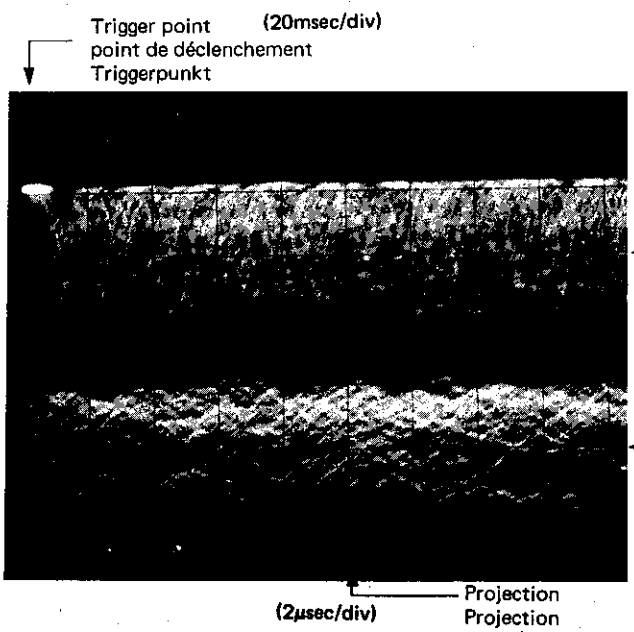
- RF signal and T.Error signal after diffraction grating adjustment.
- Signal RF et signal T.Error aprés ajustement de réseau de diffraction.
- RF-Signal und T.Error-Signal nach Diffraktions-gitter-Einstellung.



(Photo. 2)
(Photo. 2)
(Foto. 2)

- RF signal and T.Error signal when there is small diffraction grating position error.
- The T.Error signal level is small, and the envelope is as shown in the diagram below.
- Signal RF et signal T.Error quand il y a une petite erreur de position du réseau de diffraction.
- Le niveau de signal T.Error est petit et l'envelope est telle qu'indiquée dans le diagramme ci-dessous.
- RF-Signal und T.Error-Signal bei kleinem Diffraktions-gitter-Positionierungsfehler.
- Der T.Error-Signalpegel ist klein, und die Hüll-kurve ist wie in der Abbildung unten.

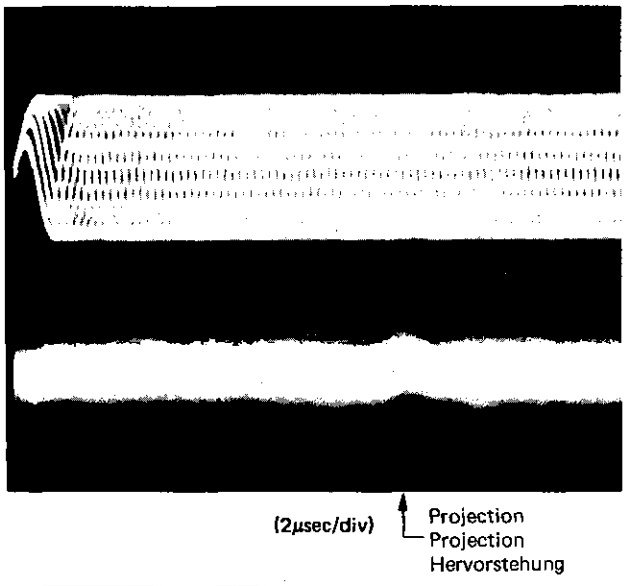




(Photo. 3)
(Photo. 3)
(Foto. 3)

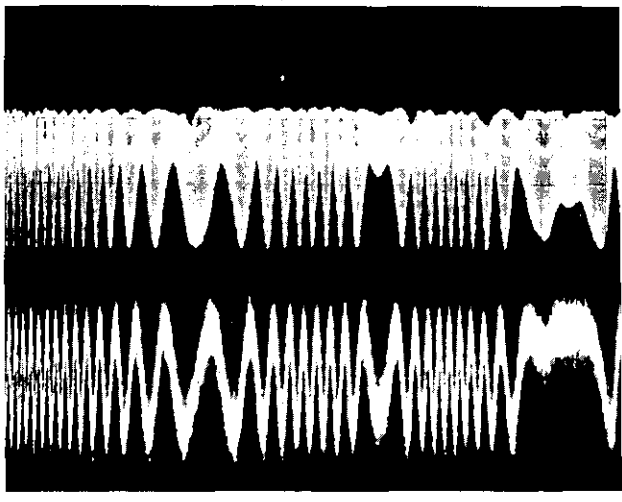
- RF signal and T.Error signal in test mode (with focusing ON).
- When the sub-beam traces the same bit series as the main beam during diffraction grating adjustment, bringing the RF trigger point to the position shown in the Photo causes a "projection" to be observies in the T.Error waveform.
- Le signal RF et le signal T.Error en mode de test (avec la mise au point sur ON).
- Quand un faisceau auxiliaire tracela même série de bits que le faisceau principal pendant l'ajustement de réseau de diffraction, l'apport du point de déclenchement RF à la position indiquée dans la photo provoque une "projection" qui s'observe dans la forme d'onde d' T.Error.
- RF-Signal und T.Error-Signal im Testmodus (bei eingeschalteter Fokussierung).
- Wenn der Nebenstrahl die gleiche Bitreihe wie der Hauptstrahl während der Diffraktionsgitter-Einstellung verfolgt und den RF-Triggerpunkt auf die im Foto gezeigte Position bringt, wird eine "Hervorstehung" verursacht, die in der T.Error-Wellenform beobachtet werden kann.

ADJUSTMENT/REGLAGE/ABGLEICH



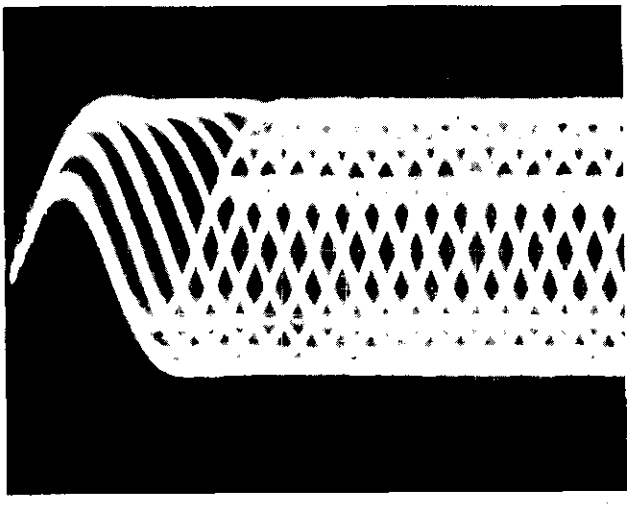
(Photo. 4)
(Photo. 4)
(Foto. 4)

- RF signal and E.Spot signal in test mode (PLAY).
- If the diffraction grating has been adjusted properly, the influence of triggering is observed on the E.Spot waveform of approx. 12μs after RF signal, in the form of a projection.
- Signal RF et signal E.Spot en mode de test (PLAY).
- Si le réseau de diffraction a été ajusté correctement, l'influence du déclenchement s'observe sur la forme d'onde E.Spot d'environ 12μs après le signal RF, sous la forme d'une projection.
- RF-Signal und E.Spot-Signal im Testmodus (PLAY).
- Wenn das Diffraktionsgitter richtig eingestellt wurde, wird der Einfluß des Triggers in der E.Spot-Wellenform etwa 12μs nach dem RF-Signal in der Form einer Hervorstehung beobachtet.



(Photo. 5)
(Photo. 5)
(Foto. 5)

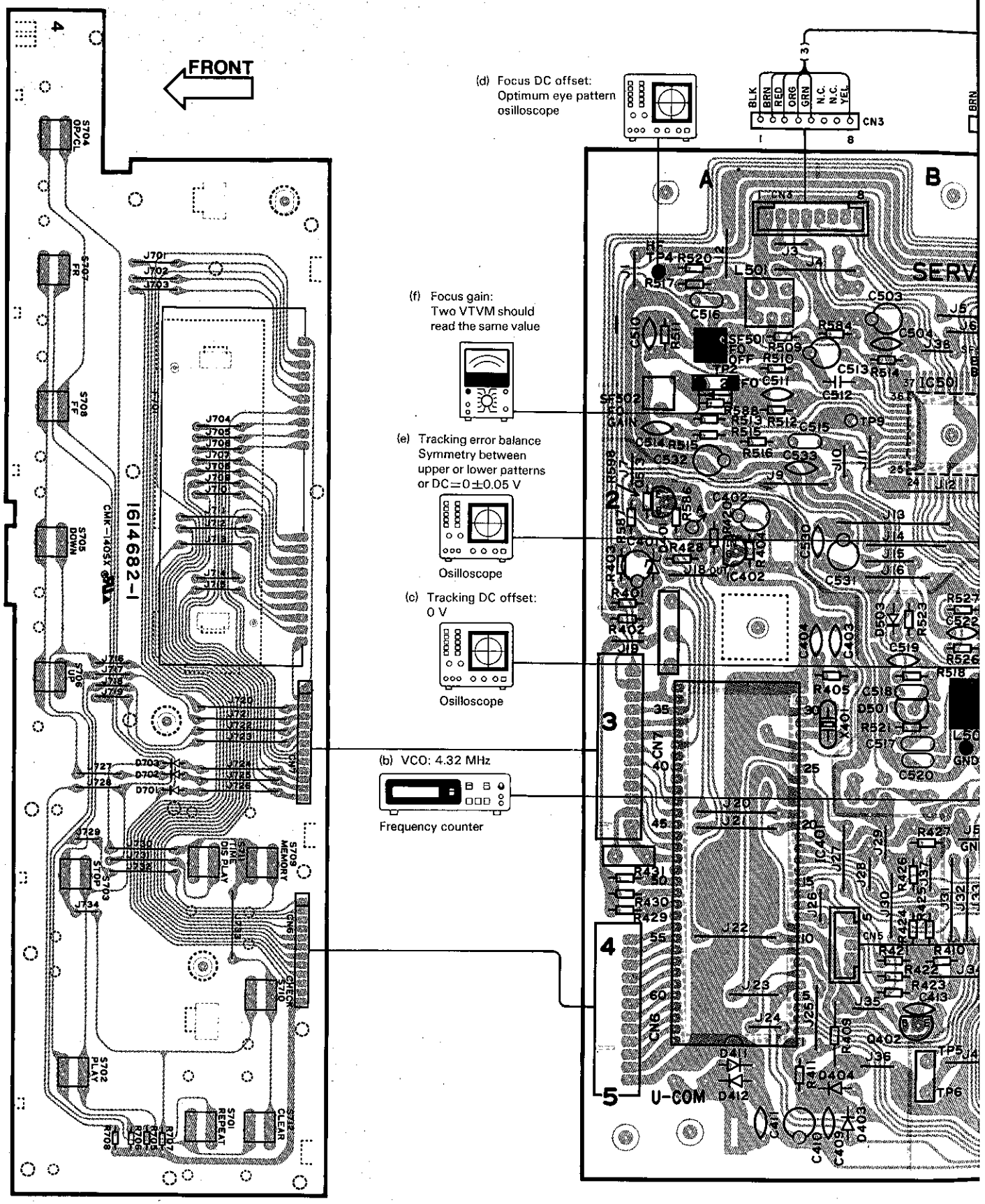
- RF signal and T.Error signal; in test mode (Focusing ON). (Disc type 4)
- Adjust T.Error so that the waveform is symmetrical above and below 0V.
- Signal RF et signal T.Error; en mode test (mise au point ON). (Disque de type 4)
- Ajuster T.Error pour que la forme d'onde soit symétrique en-dessus et au-dessous de 0V.
- RF-Signal und T.Error-Signal; im Testmodus (Fokussierung eingeschaltet). (Disc-Typ 4)
- T.Error so einstellen, daß die Wellenform über und unter 0V symmetrisch ist.

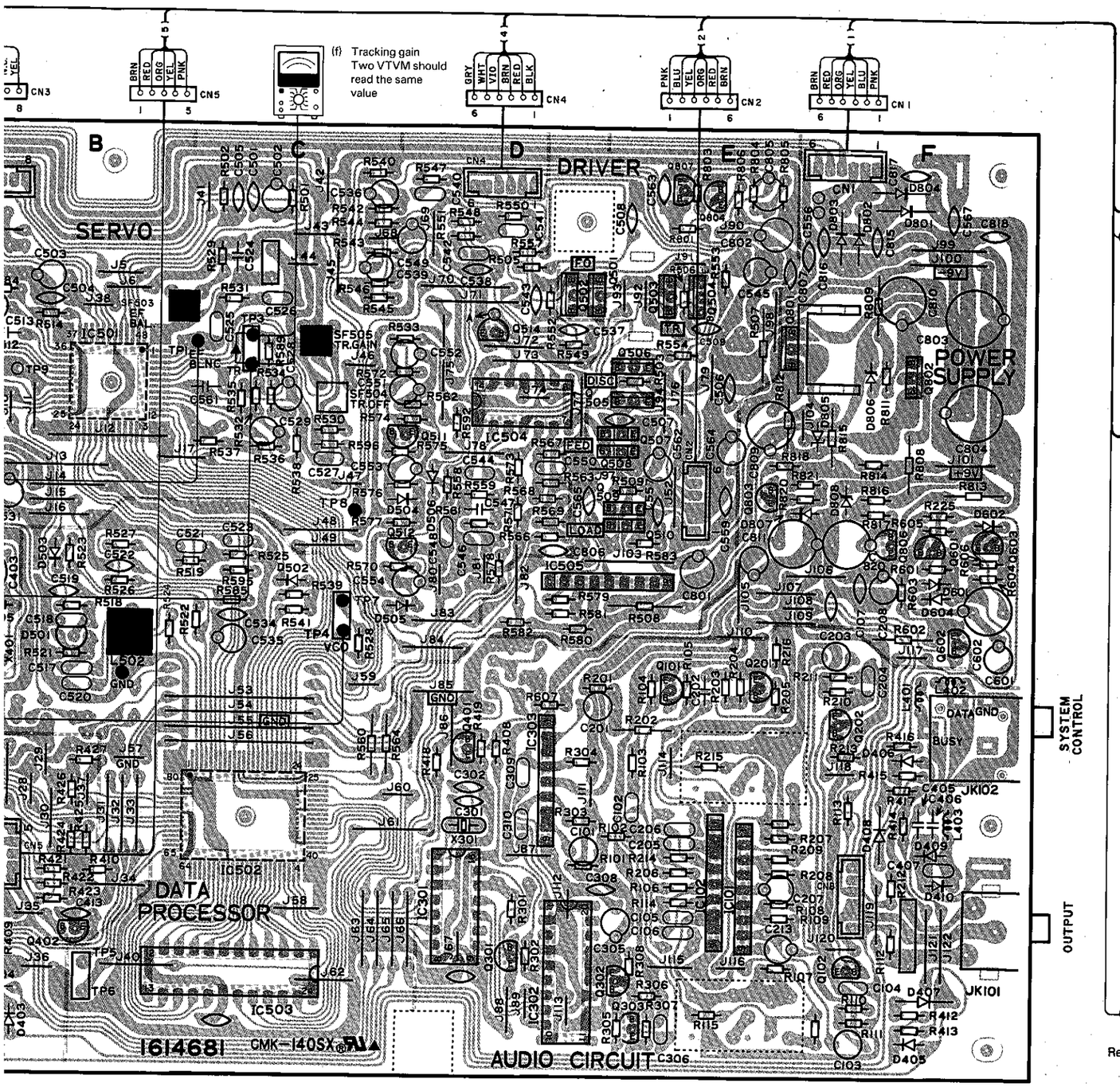


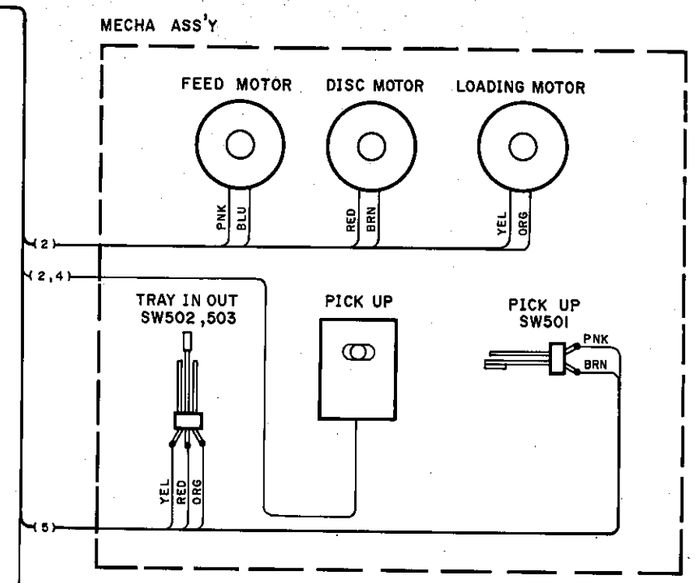
(Photo. 6)
(Photo. 6)
(Foto. 6)

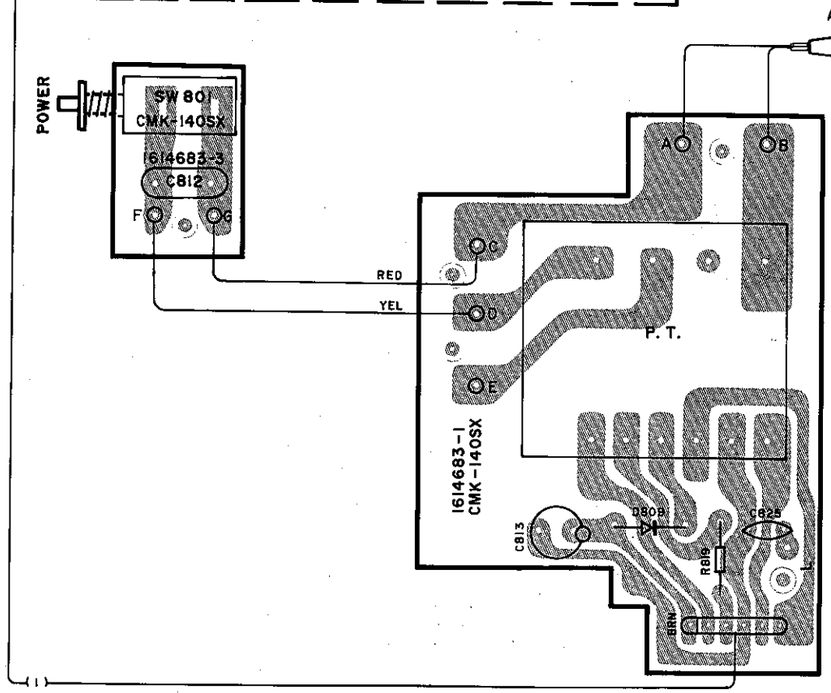
- RF signal in test mode (PLAY).
- Perform the tangential and focusing offset adjustments so that each of the center cross points are focused into one point on the display. The crossing points above and below the center shall also be displayed clearly.
- Signal RF en mode de test (PLAY).
- Effectuer les ajustements d'offset tangentiel et de mise au point pour que chacun des points de croisement central soit mis au point sur un point de l'affichage. Les points de croisement au-dessus et en-dessous du centre doivent aussi être affichés clairement.
- RF-Signal im Testmodus (PLAY).
- Die Tangential- und Fokusversatz-Einstellungen so durchführen, daß jeder der mittleren Kreuzungspunkte in einem Punkt auf dem Display fokussiert wird. Auch die Kreuzungspunkte über und unter der Mitte müssen klar angezeigt werden.

PC BOARD (COMPONENT SIDE VIEW)







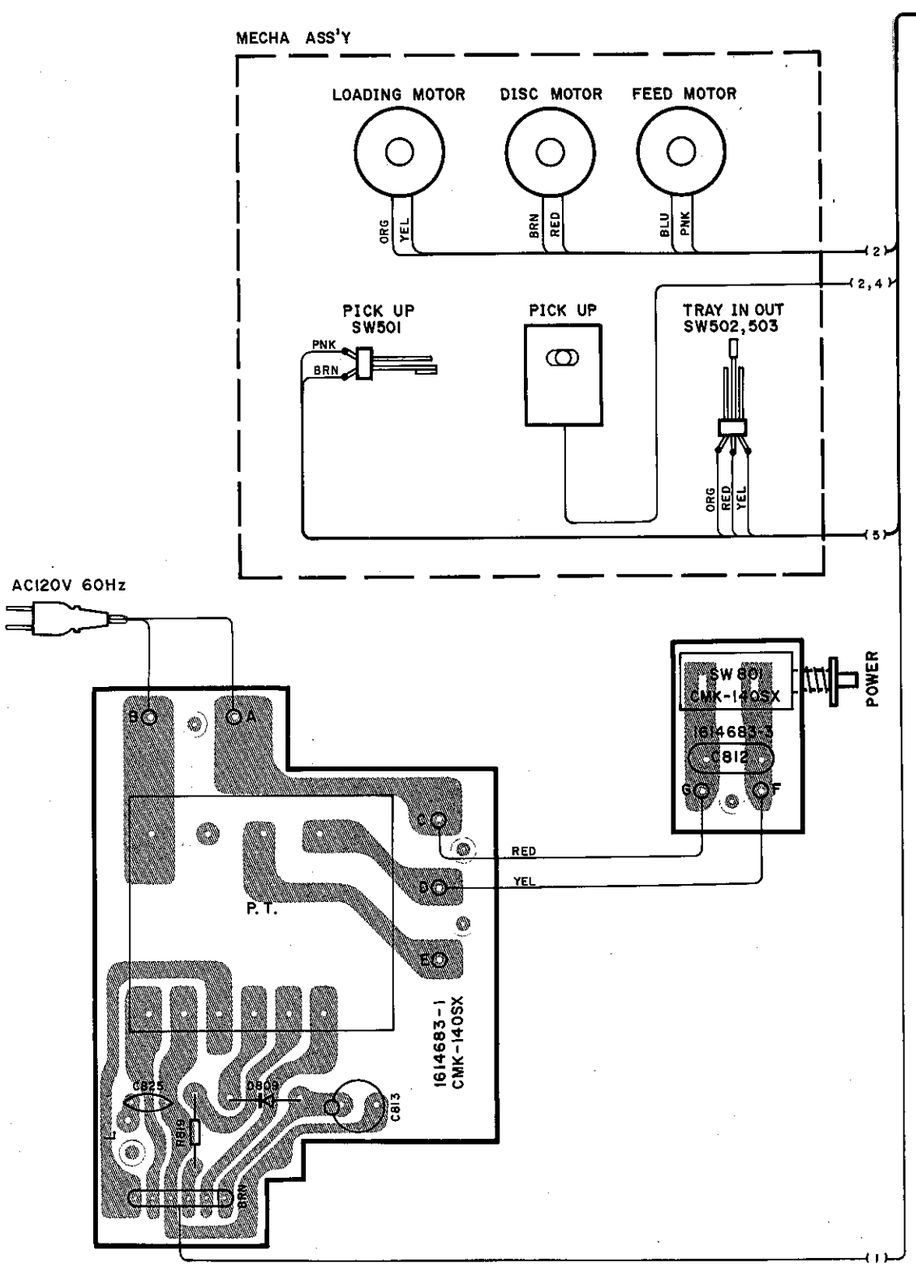


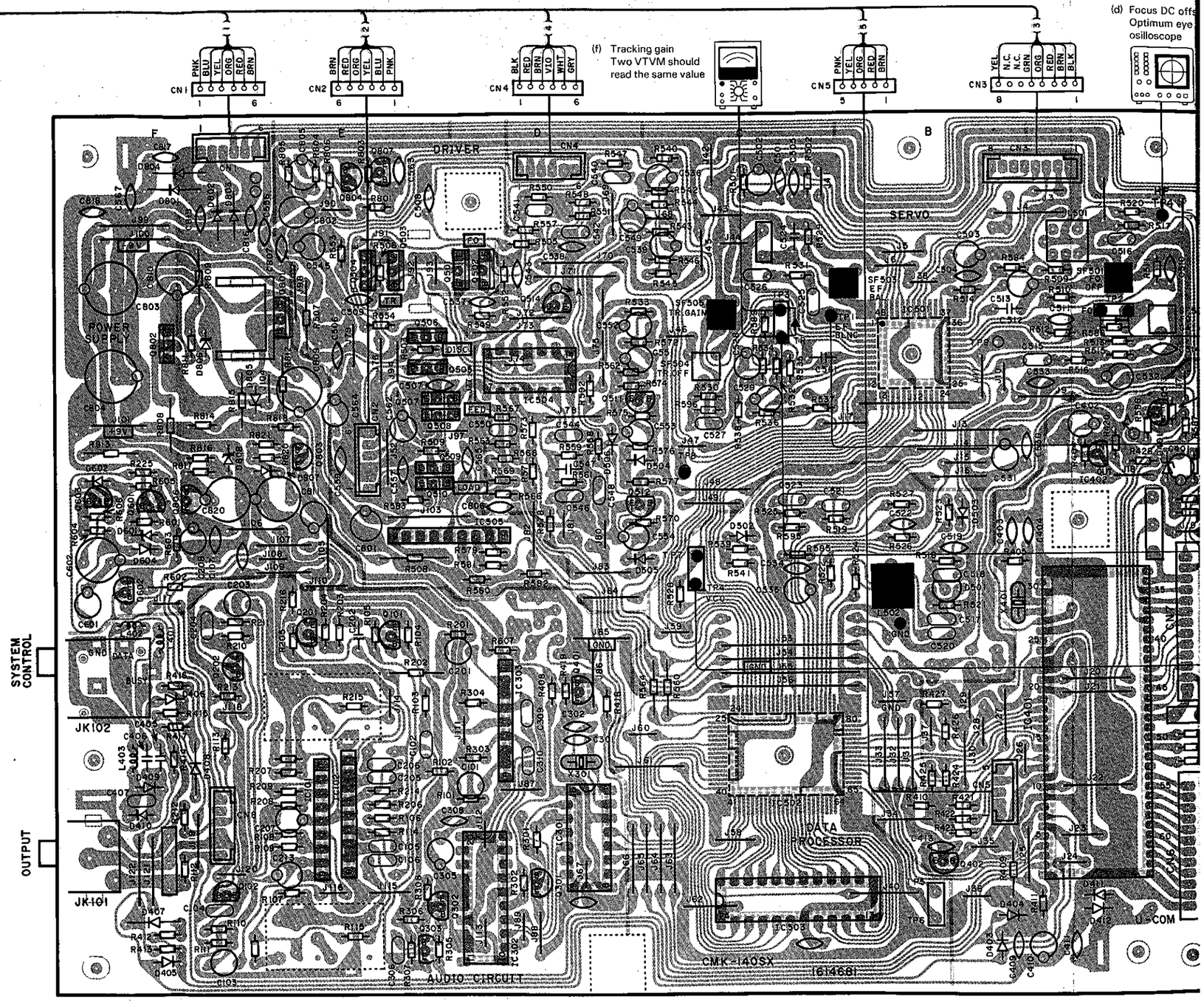
Ref. No. IC	Ref. No. Q	Address	Ref. No. IC	Ref. No. Q	Address
	101	4 I		601	4 J
	102	6 I		602	4 J
	201	4 I		603	4 J
	202	5 I		801	3 I
	301	6 H		802	3 J
	302	6 H		804	2 H
	303	6 H		806	4 J
	401	5 G		807	2 H
	402	6 E	101		6 I
	501	2 H	102		6 I
	502	2 H	103		
	503	2 H	301		6 F
	504	2 I	302		6 H
	505	3 H	303		5 H
	506	3 H	401		5 D
	507	3 H	402		4 D
	508	3 H	501		3 E
	509	4 H	502		5 F
	510	4 H	503		6 F
	511	3 G	504		3 H
	512	4 G	505		4 H
	513	3 D			
	514	3 G			

Refer to the schematic diagram for the values of resistors and capacitors.

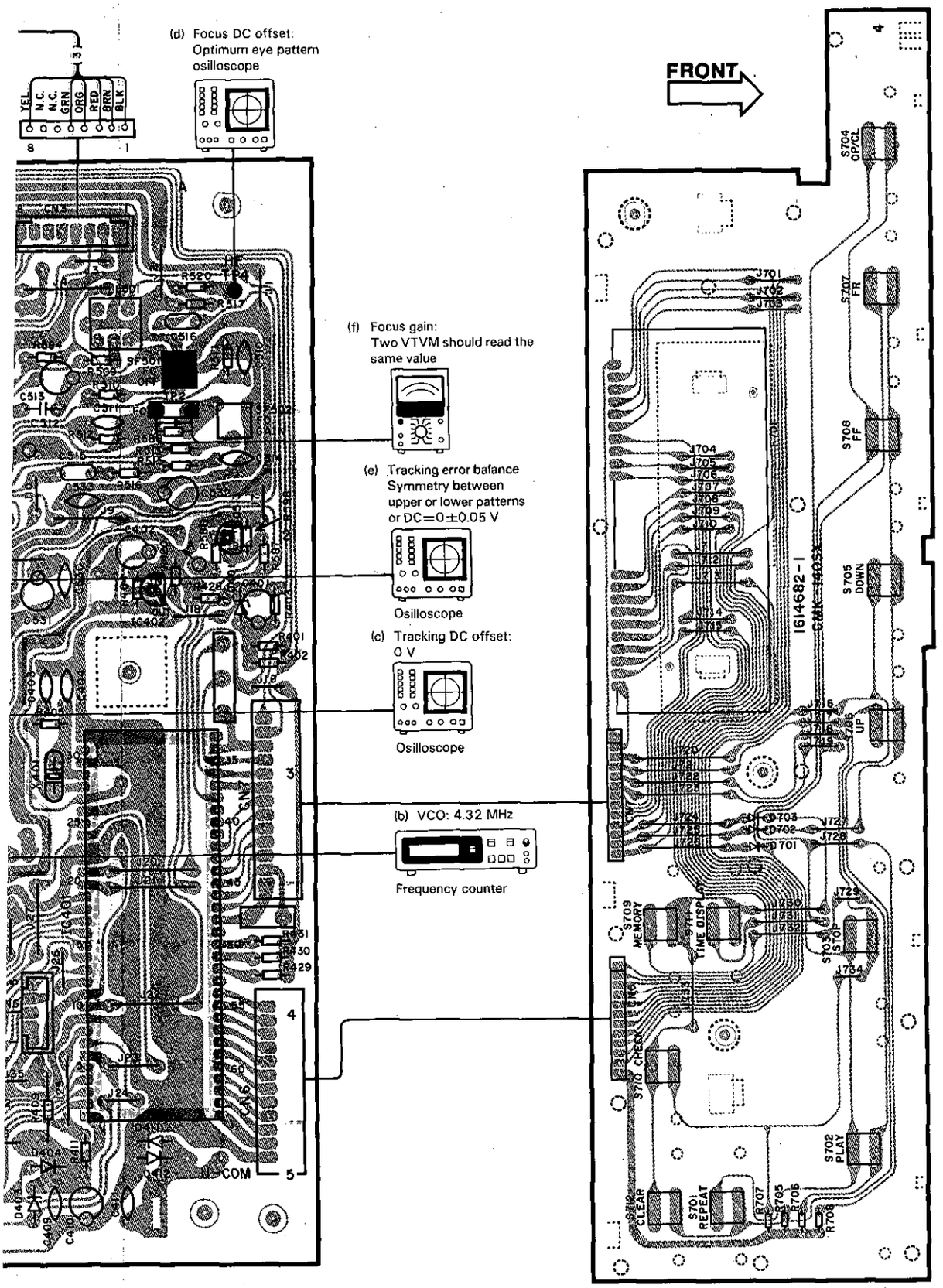
DP-48(K)

PC BOARD (FOIL SIDE VIEW)



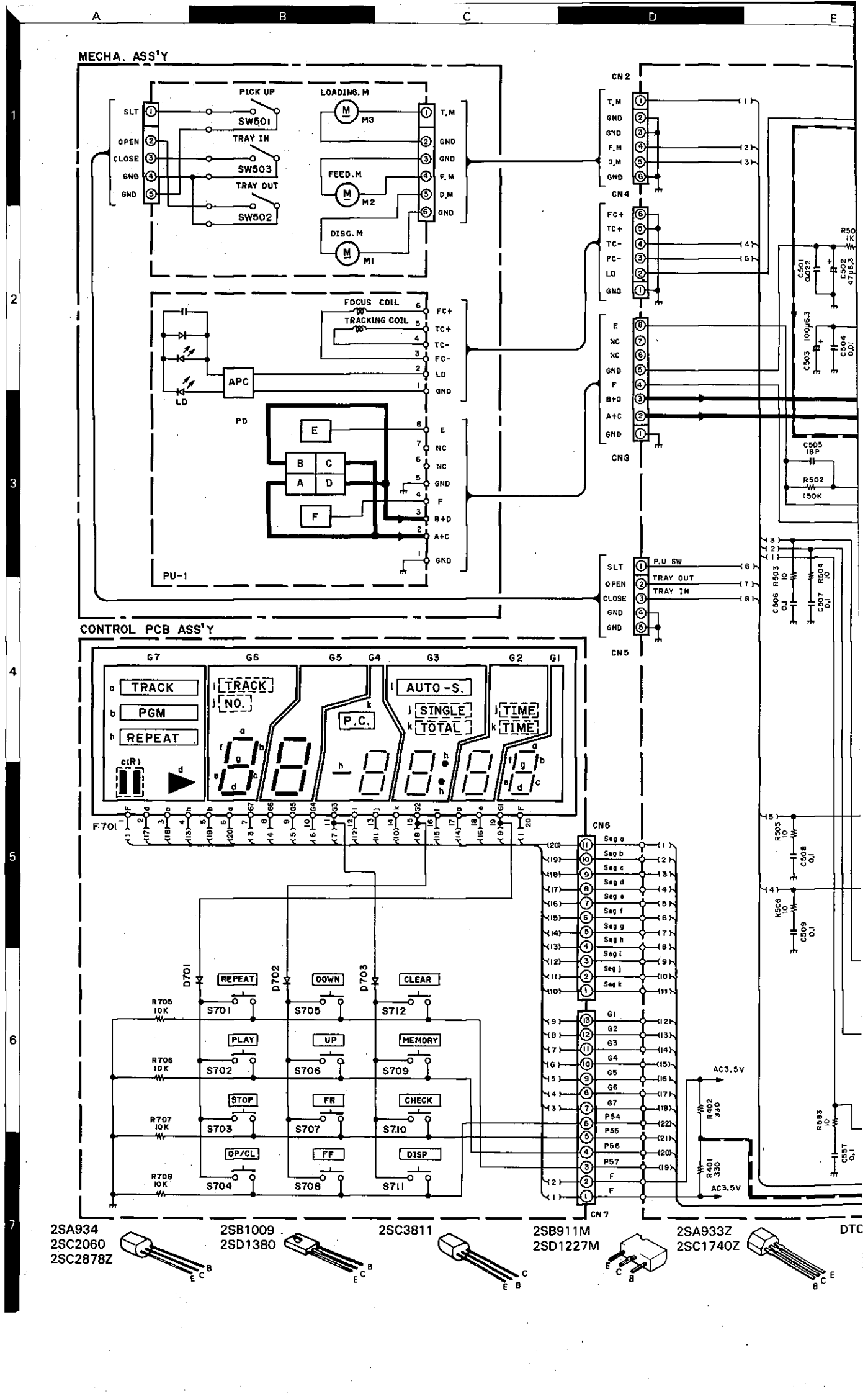


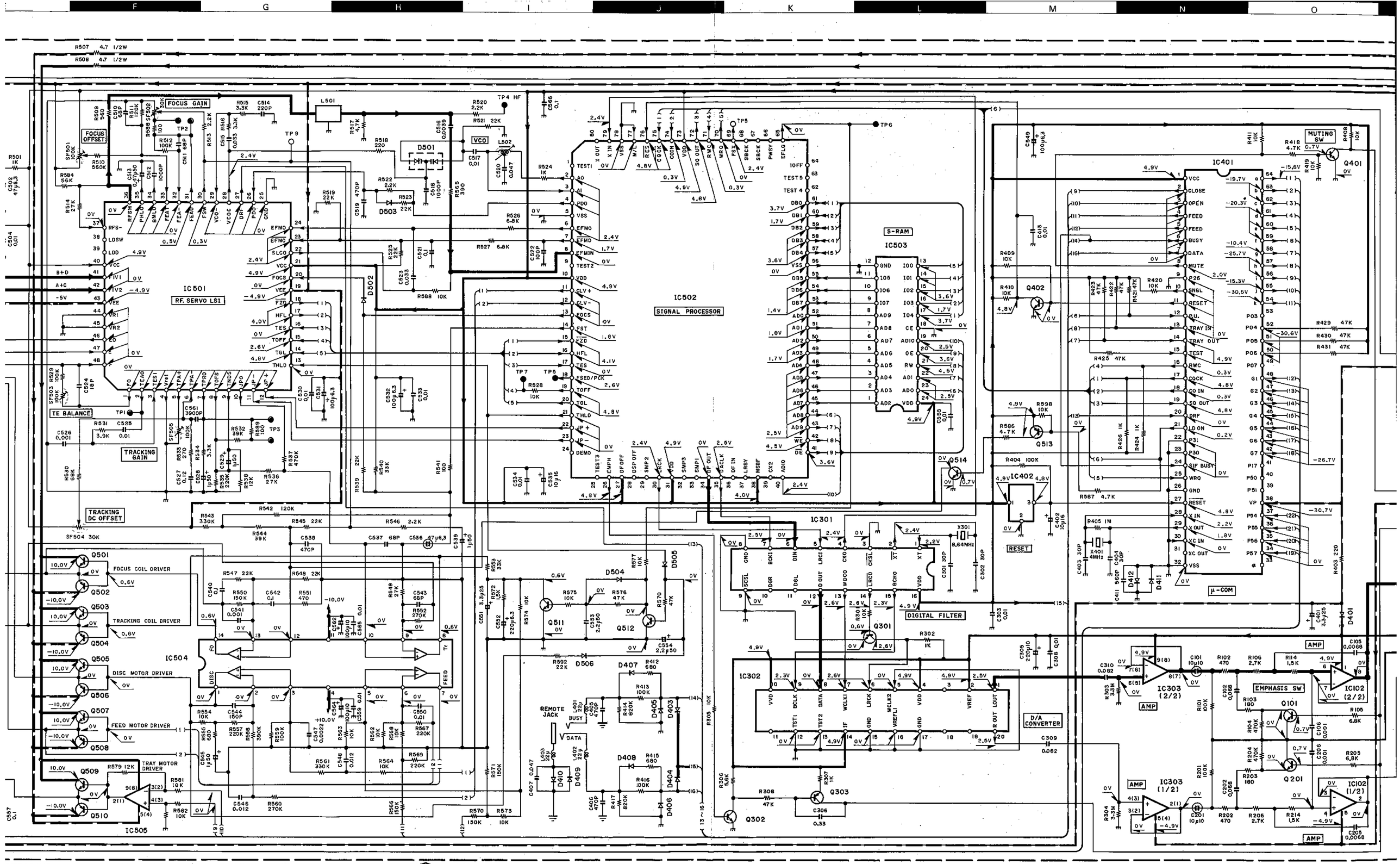
Refer to th



Ref. No.		Address
IC	Q	
	101	4 V
	102	6 U
	201	4 U
	202	5 U
	301	6 W
	302	6 V
	303	6 V
	401	5 W
	402	6 Y
	501	2 V
	502	2 V
	503	2 V
	504	2 V
	505	3 V
	506	3 V
	507	3 V
	508	3 V
	509	4 V
	510	4 V
	511	3 W
	512	4 W
	513	3 Z
	514	3 W
	601	4 T
	602	4 T
	603	4 T
	801	3 U
	802	3 T
	804	2 U
	806	4 T
	807	2 V
101		5 U
102		5 U
103		
301		6 W
302		6 V
303		5 V
401		5 Y
402		4 Z
501		3 Y
502		5 X
503		6 X
504		3 V
505		4 V

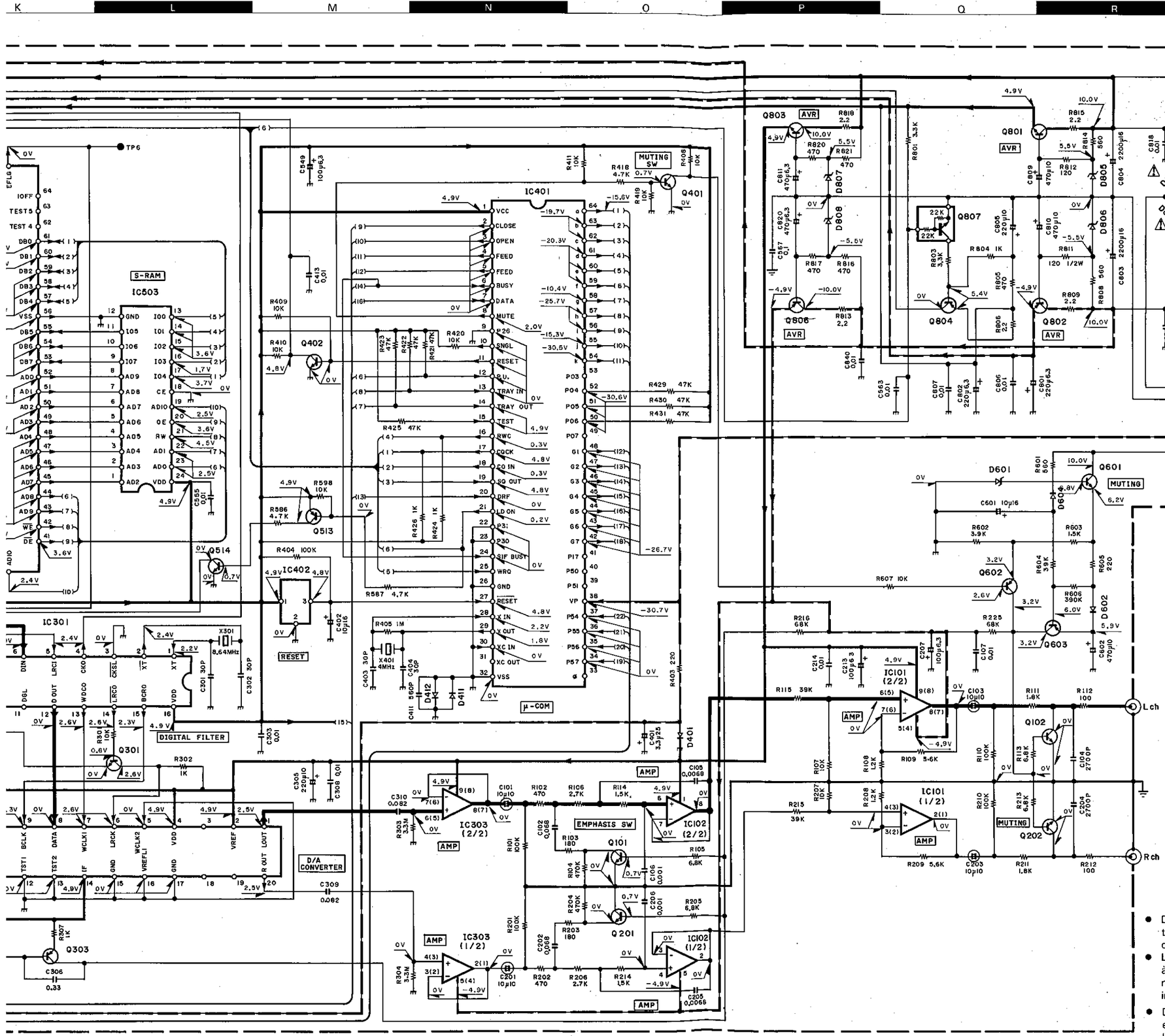
Refer to the schematic diagram for the values of resistors and capacitors.


MECHA. ASS'Y
PICK UP
LOADING. M
SW501
TRAY IN
SW503
TRAY OUT
SW502
FEED.M
DISC.M
M3
M2
M1
SLT
OPEN
CLOSE
GND
T.M
F.M
D.M
FOCUS COIL
TRACKING COIL
APC
LD
PD
E
NC
B+D
A+C
PU-1
CN2
CN4
CN3
CN5
P.U SW
TRAY OUT
TRAY IN
CONTROL PCB ASS'Y
TRACK
PGM
REPEAT
NO.
P.C.
AUTO-S.
SINGLE
TOTAL
TIME
F701
CN6
CN7
REPEAT
DOWN
CLEAR
PLAY
UP
MEMORY
STOP
FR
CHECK
OP/CL
FF
DISP
AC3.5V
2SA934
2SC2060
2SC2878Z
2SB1009
2SD1380
2SC3811
2SB911M
2SD1227M
2SA933Z
2SC1740Z
DTC



DTC124XS SM5807EP NJM4558L NJM4558L-D NJM4560S PST520F BA4558N BA4558NDX LC7863 LA9200NM

CAUTION: For continued safety, replace safety c
nents only with manufacturer's recommended p
parts list). ⚠ Indicates safety critical components.
risk of electric shock, leakage-current or resistance r



IC101	:	NJM4558LD or BA4558NDX
IC102, 303, 505	:	NJM4558L or BA4558N
IC301	:	SM5807
IC302	:	LC7881B
IC401	:	~~M50734~~ M50974-113SP
IC402	:	14D0249
IC501	:	LA9200NM
IC502	:	LC7863
IC503	:	LC35178S-15
IC504	:	NJM2060D

Q101, 201, 302, 401, 402, 511, 512, 514, 601	:	2SCI740Z
Q102, 202	:	2SC2878Z
Q301	:	2SC3811
Q303, 513, 602, 603	:	2SA933Z
Q501, 503, 505, 801	:	2SDI380
Q502, 504, 506, 802	:	2SBI009
Q507, 509	:	2SDI227M or 2SD1862Z
Q508, 510	:	2SB911M or 2SBI240Z
Q803	:	2SC2060
Q804, 806	:	2SA934
Q807	:	DTCI24XS

D401	:	MTZ-30BT
D403~406, 409~412, 502~506, 701~703	:	ISSI33T
D407, 408	:	0A90A-RT
D501	:	SVC211SPC
D601	:	MTZJ-6.8CT
D801~804	:	ISRI39-100T or ISR35-100AT
D805~808	:	MTZ-5.6BT
D809	:	ISR35-100 or ISRI39-100

- DC voltages are measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
- Les tensions c.c. doivent être measurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.
- Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Voltmeter gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u. U. geringfügig.

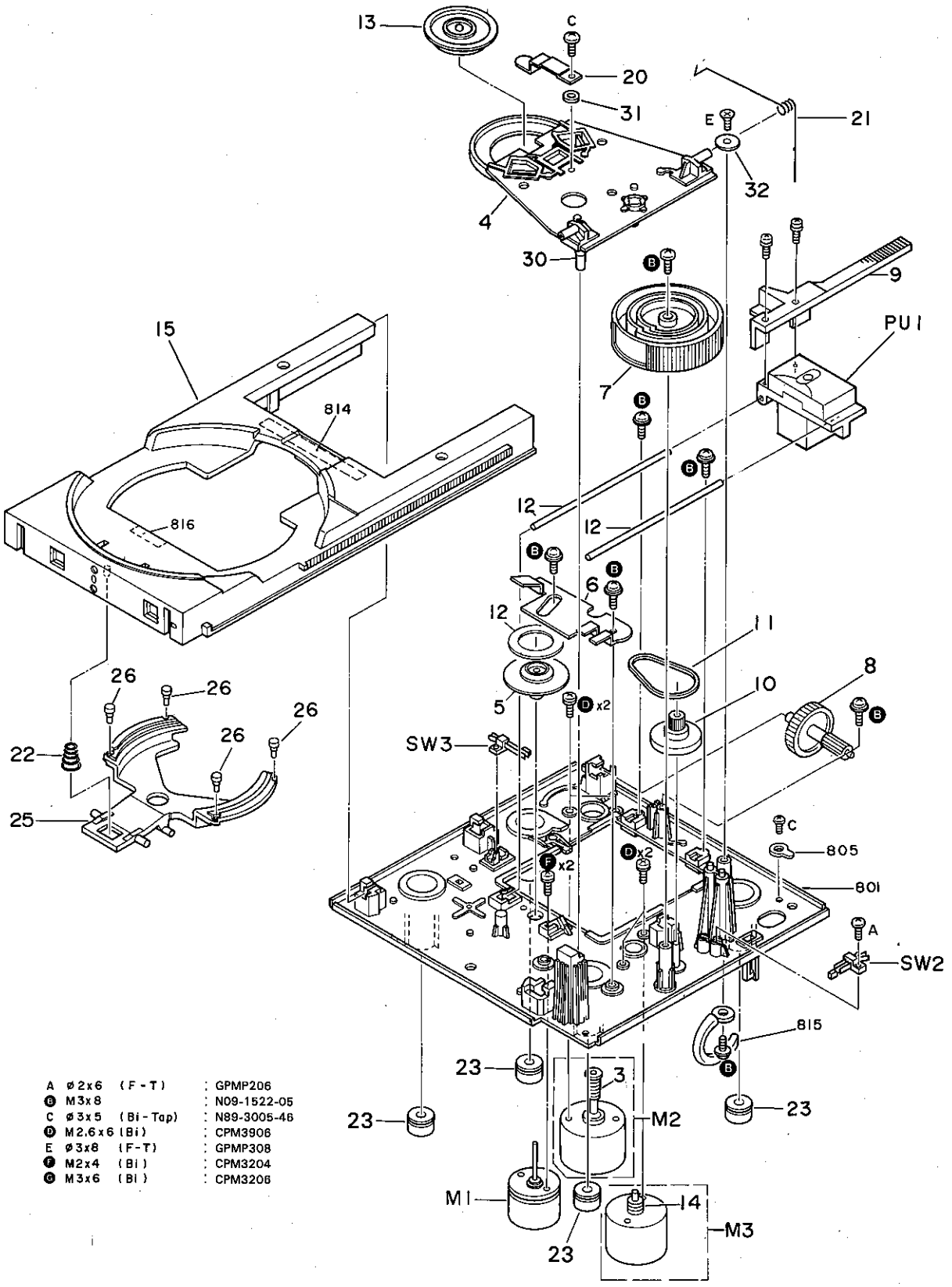
CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

Y22-1690-10

DP-48

KENWOOD

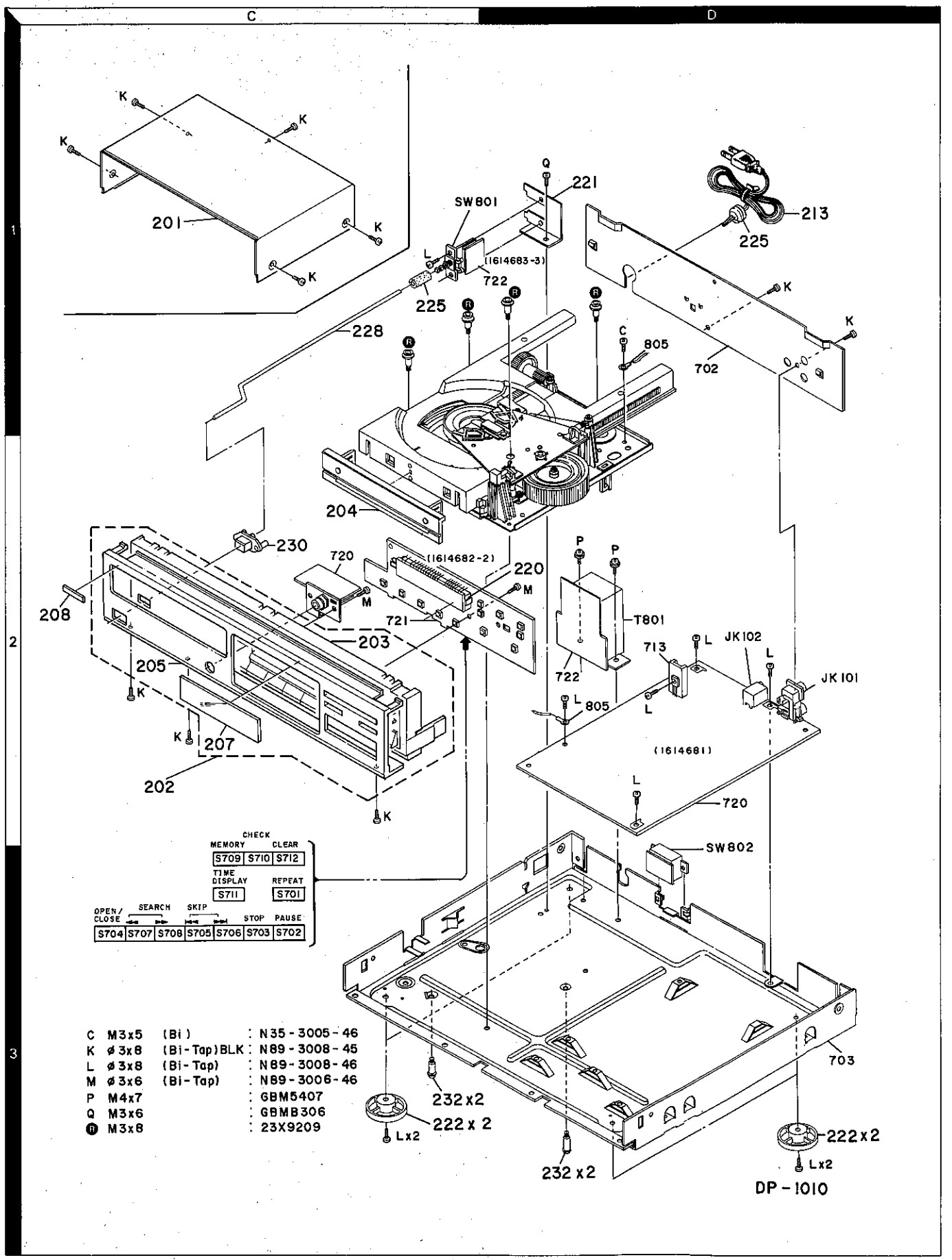
EXPLODED VIEW (MECHANISM)



A	ø2x6	(F-T)	: GPMP206
B	M3x8		: N09-1522-05
C	ø3x5	(Bi-Tap)	: N89-3005-46
D	M2.6x6	(Bi)	: CPM3906
E	ø3x8	(F-T)	: GPMP308
F	M2x4	(Bi)	: CPM3204
G	M3x6	(Bi)	: CPM3206

Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)



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			DP-48			
201	1C	*	A01-1754-08	METALLIC CABINET		
202	2C	*	A20-5797-08	PANEL ASSY		
203	2C	*	27F7053	ESCUTCHEON ASSY		
204	2C	*	21D7549	ESCUTCHEON		
205	2C	*	21F7734	ESCUTCHEON		
207	2C	*	B10-1014-08	FRONT GLASS		
208	2C		B43-0287-04	BADGE		
-			B46-0092-03	WARRANTY CARD	K	
-			B46-0096-13	WARRANTY CARD	X	
-			B46-0121-03	WARRANTY CARD	P	
-			B46-0122-13	WARRANTY CARD	E	
-		*	B50-9524-08	INSTRUCTION MANUAL (ENGLISH)	EKPX	
-		*	B50-9525-08	INSTRUCTION MANUAL (FRENCH)	EP	
-		*	B50-9526-08	INSTRUCTION MANUAL (G,I)	E	
-			B58-0223-04	CAUTION CARD		
-			B58-0513-04	CAUTION CARD		
-			B58-0893-08	CAUTION LABEL		
-		*	B58-0901-08	CAUTION LABEL		
-		*	B58-0909-08	CAUTION LABEL		
-			24L8446	CAUYION LABEL		
-			24L9042	CAUTION LABEL (CHASSIS)		
209	1C		5750342	RCA PACH CORD		
210	1C	*	5750346	SYNCRS CORD		
213	1D	*	1750585	AC CORD	E	
213	1D	*	1750829	AC CORD	KP	
213	1D	*	1750839	AC CORD	X	
228	1C	*	26W8097	LEVER ARM		
		*	H01-8471-08	ITEM CARTON BOX		
		*	H10-3812-08	POLYSTYRENE FOAMED FIXTURE		
			H25-0106-08	PROTECTION BAG		
		*	Z25550P	PROTECTION BAG		
			32E7036	TURNTABLE SHEET		
			32W7009	SPACER		
220	2D	*	21W8242	HOLDER (FL TUBE)		
221	1D	*	23X9504	HOLDER (SWITCHE)		
222	3C,3D	*	FF-017	FOOT		
223	1D		1790173	CORD BUSHUING		
225	1C		J19-3031-08	SHAFT COUPLING		
230	2C	*	21N9668	KNOB ASSY (POWER)		
232	3C,3D		N19-1084-08	FLAT WASHER		
K	1C,1D		N89-3008-45	BINDING HEAD TAPTITE SCREW		
L	1C,2D		N89-3008-46	BINDING HEAD TAPTITE SCREW		
M	2C,2D		N89-3006-46	BINDING HEAD TAPTITE SCREW		
P	2D	*	GBM5407	SCREW M4X7		
Q	1D	*	GBMB306	SCREW M3X6		
R	1C,1D		23X9209	SCREW		
T801	2D	*	1150852	POWER TRANS	E	
T801	2D	*	1150853	POWER TRANS	X	
T801	2D	*	1150855	POWER TRANS	KP	

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ELECTRIC CIRCUIT MODULE								
C101			C90-1353-05	NP-ELEC	10UF	25WV		
C102			CF92FV1H683J	MF	0.068UF	J		
C103			C90-1353-05	NP-ELEC	10UF	25WV		
C104			CF92FV1H272J	MF	2700PF	J		
C105			CF92FV1H682J	MF	6800PF	J		
C106			CF92FV1H102J	MF	1000PF	J		
C107			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C108,109			CE04KW1A221M	ELECTRO	220UF	10WV		
C110			CE04KW1C100M	ELECTRO	10UF	16WV		
C111			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C201			C90-1353-05	NP-ELEC	10UF	25WV		
C202			CF92FV1H683J	MF	0.068UF	J		
C203			C90-1353-05	NP-ELEC	10UF	25WV		
C204			CF92FV1H272J	MF	2700PF	J		
C205			CF92FV1H682J	MF	6800PF	J		
C206			CF92FV1H102J	MF	1000PF	J		
C207,208			CE04KW0J101M	ELECTRO	100UF	6.3WV		
C210			CE04KW1C100M	ELECTRO	10UF	16WV		
C213			CE04KW0J101M	ELECTRO	100UF	6.3WV		
C214			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C301,302			CC45CH1H300J	CERAMIC	30PF	J		
C303			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C305			CE04KW0J221M	ELECTRO	220UF	6.3WV		
C306			CF92FV1H334J	MF	0.33UF	J		
C308			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C309,310			CF92FV1H823J	MF	0.082UF	J		
C401			CE04KW1E3R3M	ELECTRO	3.3UF	25WV		
C402			CE04KW1C100M	ELECTRO	10UF	16WV		
C403,404			CC45CH1H300J	CERAMIC	30PF	J		
C405,406			CK45FF1H471J	CERAMIC	470PF	J		
C407			CK45FF1H473K	CERAMIC	0.047UF	K		
C409			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C410			CE04KW1A470M	ELECTRO	47UF	10WV		
C411			CK45FB1H561K	CERAMIC	560PF	K		
C413			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C501			CK45FF1H223Z	CERAMIC	0.022UF	Z		
C502			CE04KW1A470M	ELECTRO	47UF	10WV		
C503			CE04KW0J101M	ELECTRO	100UF	6.3WV		
C504			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C505			CC45FCH1H180J	CERAMIC	18PF	J		
C506-509			CK45FB1H104K	CERAMIC	0.10UF	K		
C510,511			CC45SL1H680J	CERAMIC	68PF	J		
C512			CF92FV1H102J	MF	1000PF	J		
C513			CE04KW1HR47M	ELECTRO	0.47UF	50WV		
C514			CK45FB1H221K	CERAMIC	220PF	K		
C515			CF92FV1H333J	MF	0.033UF	J		
C516			CF92FV1H392J	MF	3900PF	J		
C517			CF92FV1H103J	MF	0.010UF	J		
C518			CF92FV1H102J	MF	1000PF	J		
C519			CC45FCH1H471J	CERAMIC	470PF	J		
C520			CC45SL1H473J	CERAMIC	0.047UF	J		
C521			CF92FV1H104J	MF	0.10UF	J		
C522			CK45FB1H101K	CERAMIC	100PF	K		

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C523			CF92FV1H333J	MF	0.033UF	J		
C524			CC45CH1H180J	CERAMIC	18PF	J		
C525			CF92FV1H103J	MF	0.010UF	J		
C526			CF92FV1H102J	MF	1000PF	J		
C527			CF92FV1H124J	MF	0.12UF	J		
C528			CE04KW1H010M	ELECTRO	1.0UF	50WV		
C530			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C531,532			CE04KW0J101M	ELECTRO	100UF	6.3WV		
C533,534			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C535			CE04KW1C100M	ELECTRO	10UF	16WV		
C536			C90-1352-05	NP-ELEC	4.7UF	25WV		
C537			CC45CH1H680J	CERAMIC	68PF	J		
C538			CC45CH1H471J	CERAMIC	470PF	J		
C539			CE04KW1H010M	ELECTRO	1.0UF	50WV		
C540			CF92FV1H104J	MF	0.10UF	J		
C541			CF92FV1H102J	MF	1000PF	J		
C542			CF92FV1H104J	MF	0.10UF	J		
C543			CC45SL1H050C	CERAMIC	5.0PF	C		
C544			CK45FF1H151Z	CERAMIC	150PF	Z		
C545			CE04KW1H010M	ELECTRO	1.0UF	50WV		
C546			CF92FV1H123J	MF	0.012UF	J		
C547			CF92FV1H222J	MF	2200PF	J		
C548			CF92FV1H123J	MF	0.012UF	J		
C549			CE04KW0J101M	ELECTRO	100UF	6.3WV		
C550			CF92FV1H103J	MF	0.010UF	J		
C551			CE04KW1E3R3M	ELECTRO	3.3UF	25WV		
C552			CE04KW0J221M	ELECTRO	220UF	6.3WV		
C553,554			CE04KW1H2R2M	ELECTRO	2.2UF	50WV		
C555			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C557			CK45FB1H104K	CERAMIC	0.10UF	K		
C559			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C561			CF92FV1H392J	MF	3900PF	J		
C562			CE04KW1A101M	ELECTRO	100UF	10WV		
C563			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C564			CE04KW1A101M	ELECTRO	100UF	10WV		
C565			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C566,567			CK45FB1H104K	CERAMIC	0.10UF	K		
C601			CE04KW1C100M	ELECTRO	10UF	16WV		
C602			CE04KW1A471M	ELECTRO	470UF	10WV		
C801,802			CE04KW0J221M	ELECTRO	220UF	6.3WV		
C803,804			CE04KW1C222M	ELECTRO	2200UF	16WV		
C805			CE04KW1A221M	ELECTRO	220UF	10WV		
C806,807			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C809,810			CE04KW1A471M	ELECTRO	470UF	10WV		
C811			CE04KW0J471M	ELECTRO	470UF	6.3WV		
C815-818			CK45FF1H103Z	CERAMIC	0.010UF	Z		
C820			CE04KW0J471M	ELECTRO	470UF	6.3WV		
C840			CK45FF1H103Z	CERAMIC	0.010UF	Z		
		*	1630370	PHONE JACK				
			1730828	CONNECTING WIRE(6P)				
		*	1730830	CONNECTING WIRE(8P)				
			1740265	PLUG				
			1740767	CONNECTING WIRE(5P)				
			1740768	CONNECTING WIRE(6P)				

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		*	1770028	MINI TERMINAL BOARD(2P)		
		*	1770029	MINI TERMINAL BOARD(3P)		
		*	1770951	CONNECTING WIRE(12P)		
		*	1770952	CONNECTING WIRE(13P)		
JK101			1630375	RCA JACK		
JK102			1630362	SYNCHRO JACK		
L401-403		*	2165220T	FIXD INDUCTOR 22UH		
L501		*	1813010	LPF		
L502		*	1170659	VCO COIL		
X301		*	1811341	CERAMIC OSCILLATOR 8.64MHZ		
X401		*	1812387	CERAMIC OSCILLATOR 4MHZ		
R507,508			5362479	FUSE R 4.7 J 1/2W		
SF501		*	138N785	POTENTIOMETER(100KB)		
SF502		*	138N783	POTENTIOMETER(30KB)		
SF503		*	138N785	POTENTIOMETER(100KB)		
SF504		*	138N783	POTENTIOMETER(30KB)		
SF505		*	138N785	POTENTIOMETER(100KB)		
D401		*	MTZ-30BT	ZENER DIODE		
D403-406			1SS133T	DIODE		
D407,408		*	0A90A-RT	DIODE		
D409-412			1SS133T	DIODE		
D501		*	SVC211SPC	VARISTOR		
D502-506			1SS133T	DIODE		
D601			MTZJ6.8CT	ZENER DIODE		
D801-804		*	1SR139-100T	DIODE		
D801-804			1SR35-100AT	DIODE		
D805-808			MTZ5.6BT	ZENER DIODE		
IC101			BA4558NDX	IC(OP AMP X2)		
IC101			NJM4558L-D	IC(OP AMP X2)		
IC102			BA4558N	IC(OP AMP X2)		
IC102			NJM4558L	IC(OP AMP X2)		
IC301		*	SM5807SP	IC(DIGITAL FILTER FOR CD)		
IC302		*	LC7881B	IC(DAC)		
IC303			BA4558N	IC(OP AMP X2)		
IC303			NJM4558L	IC(OP AMP X2)		
IC401		*	~~M50754-112SP~~	IC(CPU) M50954-113SP		
IC402			PST520F	IC(LOW POWER RESET)		
IC501			LA9200NM	IC(ANALOGUE SIGNAL PROCESSOR)		
IC502		*	LC7863	IC(SIGNAL PROCESSOR)OCESSOR)		
IC503		*	LC35173S-15	IC(16KX8 RAM)		
IC504		*	NJM2060D	IC(OP AMP)		
IC505			BA4558N	IC(OP AMP X2)		
IC505			NJM4558L-D	IC(OP AMP X2)		
Q101			2SC1740Z	TRANSISTOR		
Q102			2SC2878Z	TRANSISTOR		
Q201			2SC1740Z	TRANSISTOR		
Q202			2SC2878Z	TRANSISTOR		
Q301			2SC3811	TRANSISTOR		
Q302			2SC1740Z	TRANSISTOR		
Q303			2SA933Z	TRANSISTOR		
Q401,402			2SC1740Z	TRANSISTOR		
Q501			2SD1380	TRANSISTOR		
Q502			2SB1009	TRANSISTOR		

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Q503			2SD1380	TRANSISTOR		
Q504			2SB1009	TRANSISTOR		
Q505			2SD1380	TRANSISTOR		
Q506			2SB1009	TRANSISTOR		
Q507			2SD1227M	TRANSISTOR		
Q507			2SD1862Z	TRANSISTOR		
Q508			2SB1240Z	TRANSISTOR		
Q508			2SB911M	TRANSISTOR		
Q509			2SD1227M	TRANSISTOR		
Q509			2SD1862Z	TRANSISTOR		
Q510		*	2SB1240Z	TRANSISTOR		
Q510			2SB911M	TRANSISTOR		
Q511,512			2SC1740Z	TRANSISTOR		
Q513			2SA933Z	TRANSISTOR		
Q514			2SC1740Z	TRANSISTOR		
Q601			2SC1740Z	TRANSISTOR		
Q602,603			2SA933Z	TRANSISTOR		
Q801			2SD1380	TRANSISTOR		
Q802			2SB1009	TRANSISTOR		
Q804			2SA934	TRANSISTOR		
Q804		*	2SA934T103	TRANSISTOR		
Q805			2SC2060	TRANSISTOR		
Q805		*	2SC2060T103	TRANSISTOR		
Q806			2SA934	TRANSISTOR		
Q806		*	2SA934T103	TRANSISTOR		
Q807			DTC124XS	TRANSISTOR		
S701-712			5622157	TACT SW		
D701-703			1SS133T	DIODE		
F701		*	1833094	FL TUBE		
IC103			NJM4560S	IC(OP AMP X2)		
C812			1220817	SPARK KILLER		
C813			CE04KW1V101M	ELECTRO 100UF 35WV		
C825			CK45B1H104K	CERAMIC 0.10UF K		
SW801		*	1622845	PUSH SWITCH		
SW802			1621792	SLIDE SWITCH		
D809			1SR139-100	DIODE		
D809			1SR35-100	DIODE		
MECHANISM ASS'Y						
		*	24LP508	PLANT NAME LABEL	KP	
		*	24L8110	LL NO LABEL	P	
		*	24L8354	DANGER LABEL	KP	
3	3B		21W8074	WORM GEAR		
4	1A	*	21W8256	LEVER ARM		
5	2B	*	21W8176B	TURNTABLE PLATTER (B)		
6	2B	*	23X9518	LEVER ARM (B)		
7	1B		21W8077B	GEAR		
8	2B		21W8238	WORM WHEEL		
9	1B		21W8237	GEAR (S)		
10	2B		21W8079	PULLEY		

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11	2B		21V7131	SQUARE BELT (8.2CM URETHANE)		
12	2B		25W8945	GUIDE SHAFT (B)		
13	1A		21W8144I	RORATION PARTS		
14	3B		21W8027	PULLY		
15	1A		21W8234B	RAIL		
			D3706-01	FINISHED WIRE SET		
20	1B		23X9366A	SPRING		
21	1B		26W8037A	SPRING		
22	2A		26W8023D	SPRING		
23	3A,3B		21W8039	FORMED PLATE		
30	1B	*	G0M4010	SPACER		
25	2A	*	21W8254	HOLDER		
26	2A		21W8207	BUSHING		
PU1	1B	*	1540022	PICK UP		
31	1B		WPM3085	FLAT WASHER		
32	1B		WPM4151	FLAT WASHER		
A	3B		GPMP206	SCREW M2X6		
B	1B,2B		N09-1522-05	SCREW M3X8		
C	2B		N89-3005-46	SCREW M3X5		
D	2B		CPM3906	SCREW M2.6X6		
E	1B		GDMP308	SCREW M3X8		
F	3B		CPM3204	SCREW M2X4		
G	1B		CPM3206	SCREW M2X6		
SW2	3B		1624150	LEAF SWCTCH		
SW3	2B		1624118	LEAF SWITCH		
M1	3B		1640274	DC MOTOR ASSY(DISC)		
M2	3B		1640233	DC MOTOR ASSY(FEED)		
M3	3B		1640353	DC MOTOR ASSY(LOADING)		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

DP-48

SPECIFICATIONS

[Format]

Type: ..... Compact disc player
Read system: ..... Non-contact optical pickup
Rotational speed: ..... About 200 to 500 rpm

[Audio]

Frequency response: ..... 20Hz ~ 20kHz
Signal-to-noise ratio: ..... more than 92dB
Total harmonic distortion: ..... 0.05% at 1kHz
Wow flutter: ..... Below measurable limit
Output level/ impedance: ..... 1.6V/3.3 kΩ

[General]

Power consumption: 10W
Dimensions: ..... W: 440mm (17-5/16")
H: 98mm (3-7/8")
D: 261mm (10-1/4")
Weight: ..... 3.6kg (7.9 lb)

Note:
KENWOOD follows a policy of continuous development. For this reason specifications may be changed without notice.

Note:
Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on the U.S.A. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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