

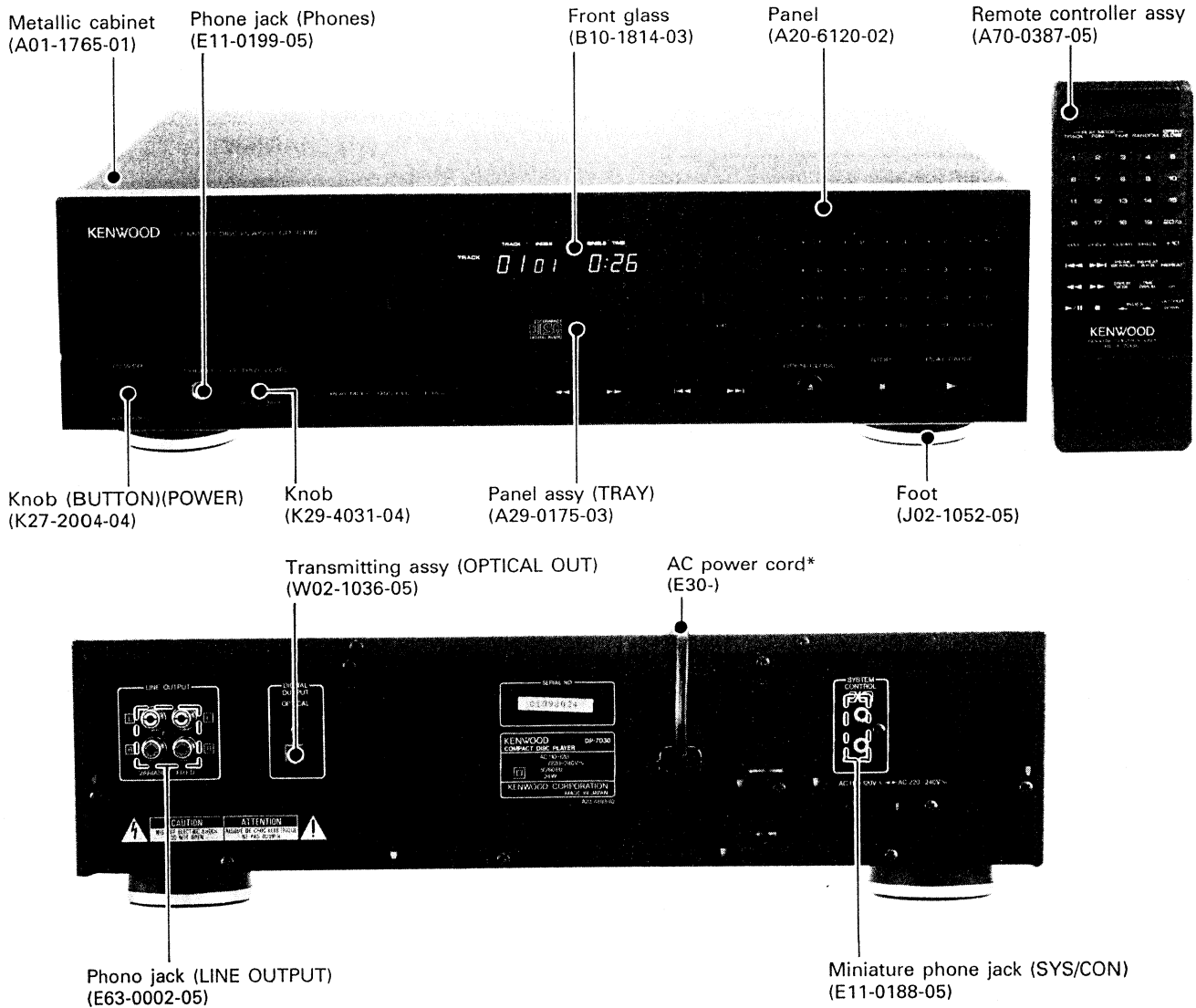
COMPACT DISC PLAYER

DP-7030

SERVICE MANUAL

KENWOOD

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B51-4244-00 (O) 2140



***Refer to parts list on page 49.**

In compliance with Federal Regulations, following are reproductions of labels on, or inside the product relating to laser product safety.

KENWOOD-Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040. 10, Chapter 1, Subchapter J.

**DANGER : Laser radiation when open and interlock defeated.
AVOID DIRECT EXPOSURE TO BEAM.**

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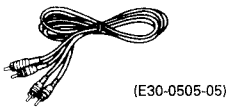
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SPECIFICATIONS BACK COVER

Accessories

- Audio cord 1



- Remote control unit 1



- System control cord 1
(Except for the U.K. and Europe)

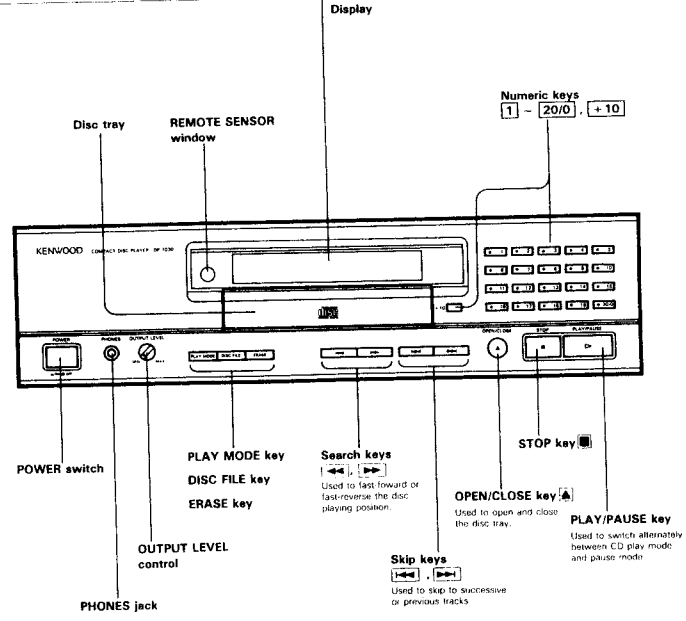
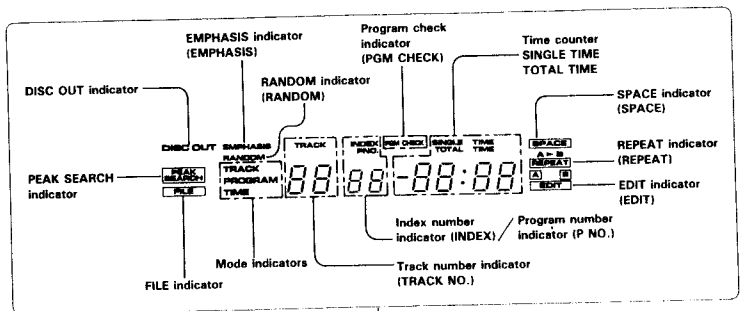


- Battery ("AA" or "R06") 2



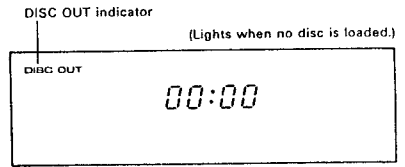
CONTROLS / CAUTION

Controls



Caution

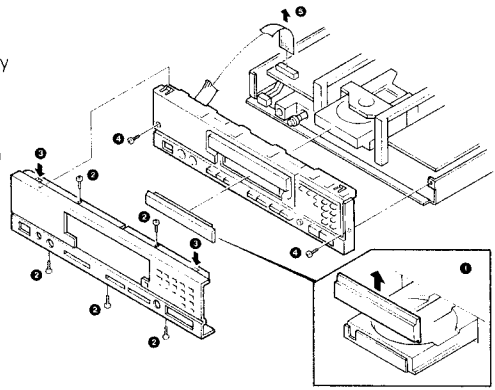
- **Note related to transportation and movement**
Carry out the operations listed before transporting or moving this unit.
- 1. After making sure that there is no compact disc loaded in the unit, turn the POWER switch ON.
- 2. Wait for several seconds to verify that the DISC OUT indicator (OUT) lights on the display, and then turn the POWER switch back OFF.



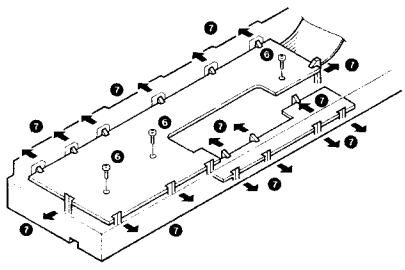
DISASSEMBLY FOR REPAIR

1. HOW TO DISASSEMBLE

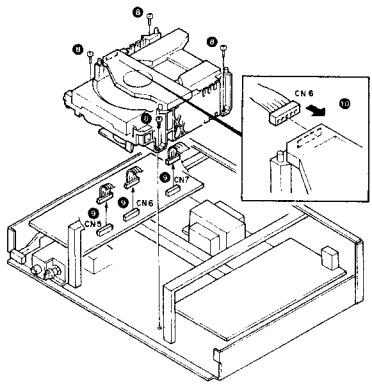
1. After sliding out the tray, turn off the power switch.
2. Remove the tray panel and push the tray backward by hand (1).
3. Remove 5 screws (2) and 2 catches (3). And then remove the panel.
4. Remove 2 screws (4) and connector (5). And then remove the sub panel.



5. Remove 5 screws (6).
6. Remove 17 catches (7) and pc board.



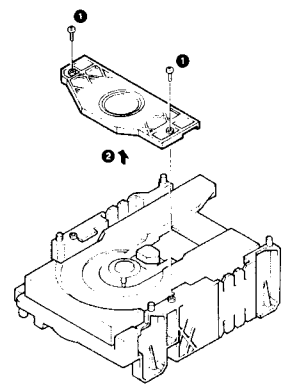
7. Remove 4 screws (8).
8. Remove 3 connectors (9) and mechanism ass'y.
9. Inert the connector CN6 to LD short pin (10).



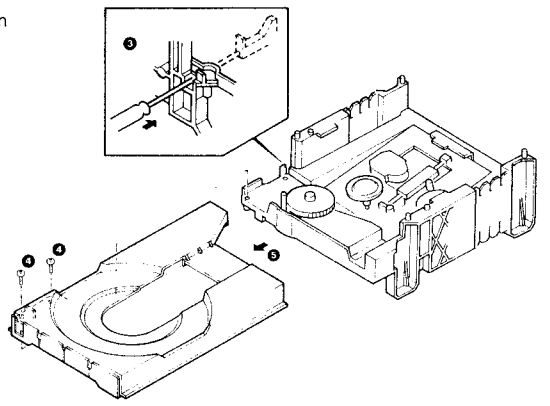
DISASSEMBLY FOR REPAIR

2. HOW TO REMOVE TRAY

1. Remove 2 screws (1).
2. Remove clamber ass'y (2).

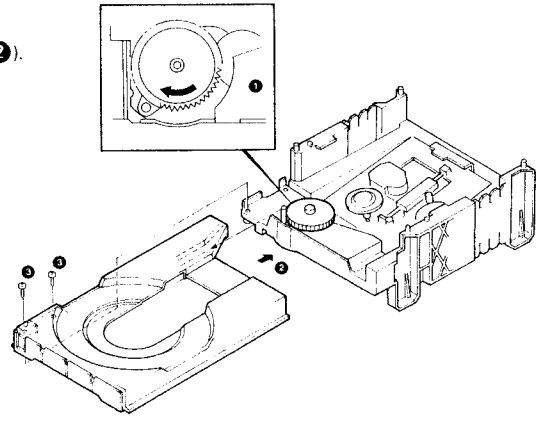


3. Insert the driver to left-side hole of mechanism ass'y and push the slider (3).
4. Remove 2 screws (4).
5. Tray can be pulled out (5).



3. HOW TO MOUNT TRAY

1. Set the pole to fully clockwise (1).
2. Insert the tray to both-side guide on chassis (2).
3. Fix 2 screws (3).

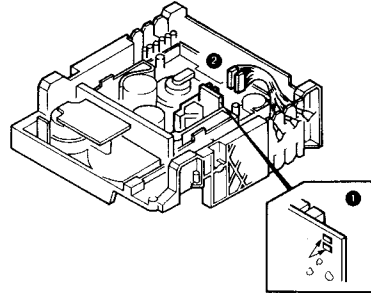


DISASSEMBLY FOR REPAIR

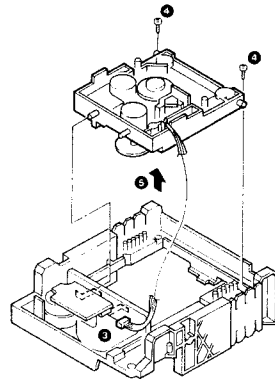
4. HOW TO REPLACE THE PICKUP.

Short the short-land of the pickup before the following procedures (1).

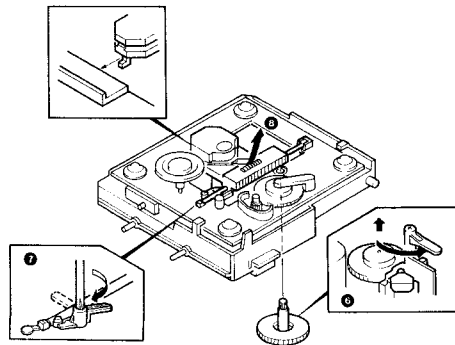
1. Remove 2 connectors (2).



2. Remove the connector (3).
3. Remove 2 screws (4).
4. Remove the mechanism drive (MD) ass'y (5).

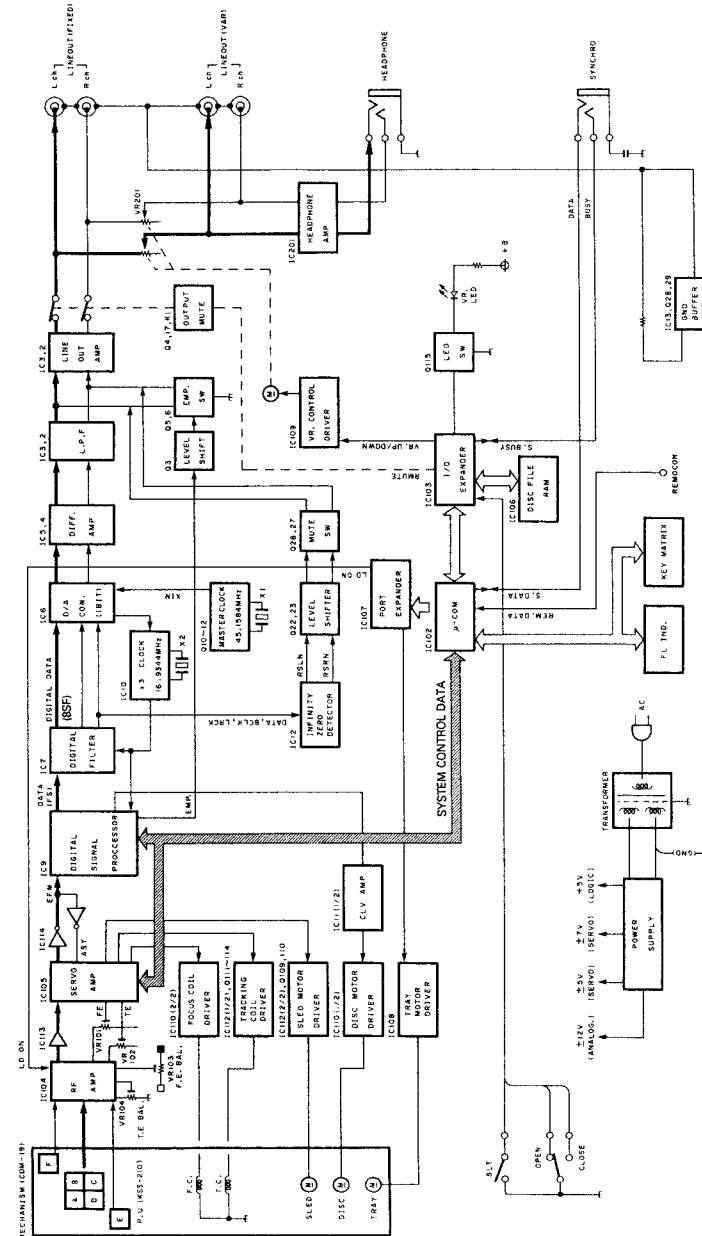


5. Remove stopper and gear (6).
6. Remove rod stopper (7).
7. Remove the pickup ass'y (8).



Note : When mounting the pickup, in the reverse order of disassembly. Unsolder the short land after connecting the flexible wire.

BLOCK DIAGRAM

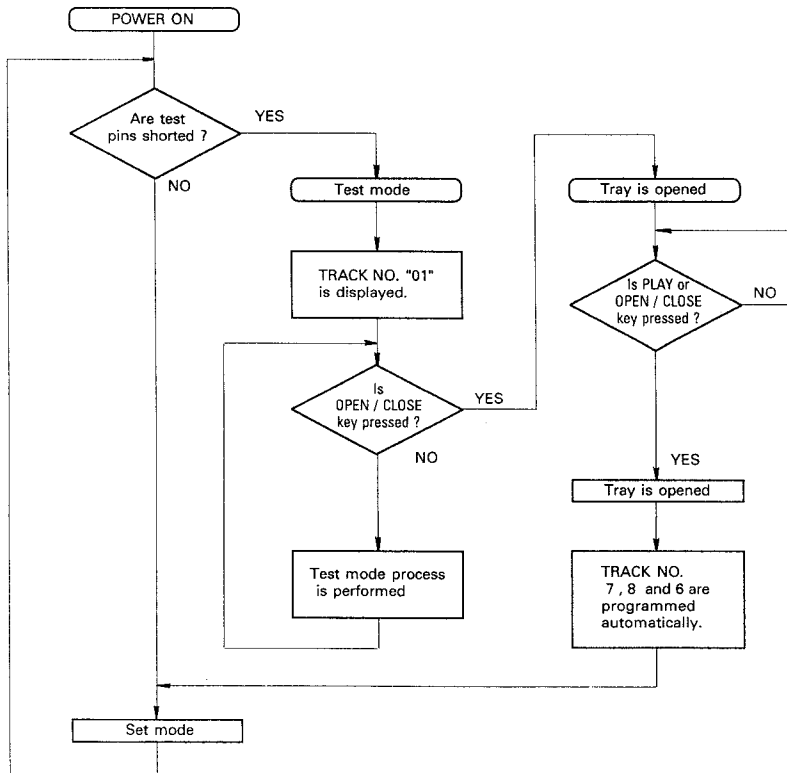


CIRCUIT DESCRIPTION

1. Test Mode

1-1. Setting the test mode

This microprocessor built in this unit (X32-1790-00, X32-1802-70) can be put to TEST MODE by just short-circuiting the test pins (#2 and 3).



CIRCUIT DESCRIPTION

2-2. Key and functions valid in test mode

No.	Input key	Function	Track No. display
1	PLAY	(1) Focusing servo ON (2) Tracking servo ON (3) Feed servo ON	TRACK NO. 05 ↓ Displayed for a few seconds after completion (1), (2) and (3). ↓ Disc Track No. is displayed.
2	+10	(1) Focusing servo ON (2) Tracking servo OFF (3) Feed servo OFF	TRACK NO. 03
3	STOP	(1) Focusing servo OFF (2) Tracking servo OFF (3) Feed servo OFF	TRACK NO. 01
4	UP (▶▶)	Turns all FL display lamps ON.	TRACK NO. 88
5	DOWN (◀◀)	Turns all FL display lamps OFF. "TRACK NO." is lighted.	TRACK NO. 88
6	P. MODE	Track No. 7,8, and 6 are programmed and playback from Track No.7. The test mode is canceled.	-
7	OPEN/CLOSE (▲)	When the tray is opened then closed. Track No. 7, 8, and 6, are programmed and set is in STOP mode. The test mode is canceled.	TRACK NO. 00
8	ERASE	In the STOP mode, moves the pickup toward the outer position of disc. And laser diode is lighted when push OPEN / CLOSE key, set into STOP mode.	TRACK NO. 02

CIRCUIT DESCRIPTION

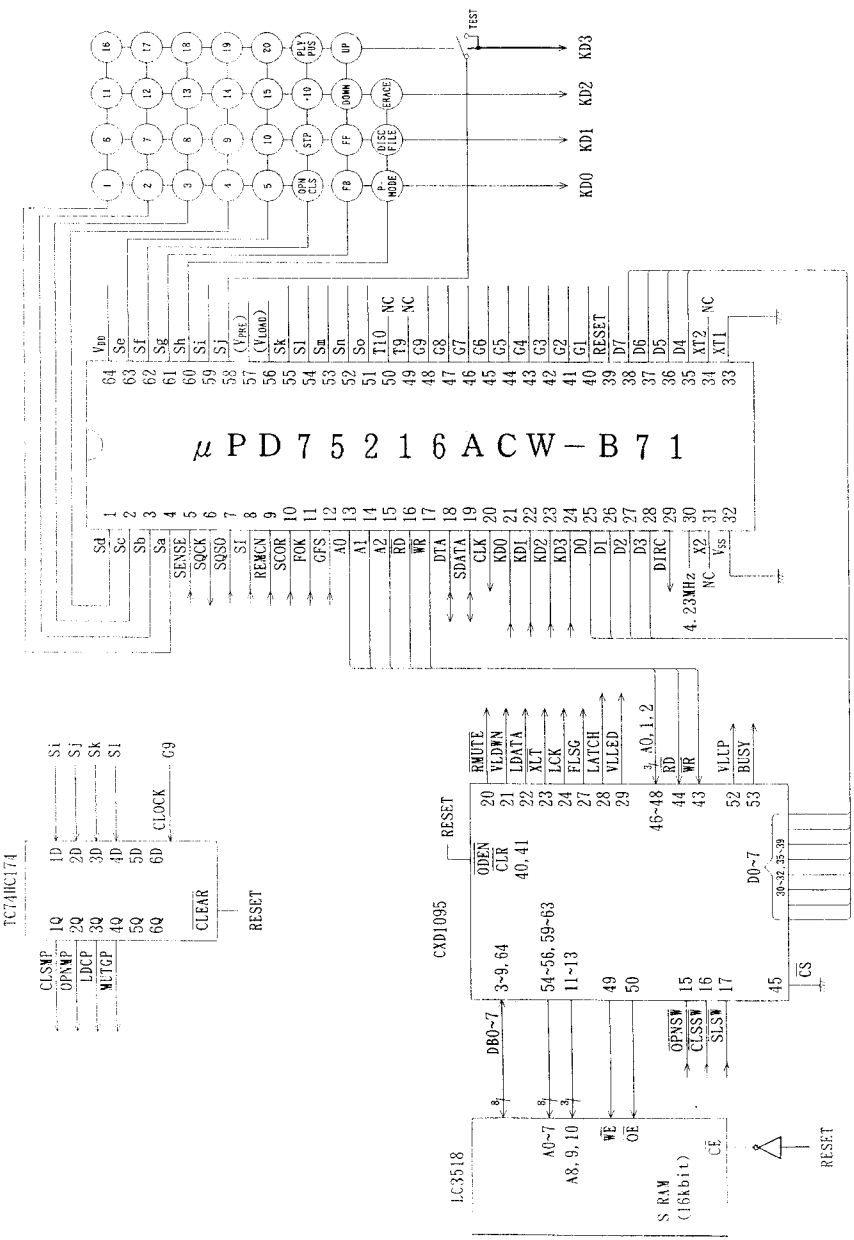
CIRCUIT DESCRIPTION

2. Microprocessor : μ PD75216ACW-B71 (IC102)

2-2. Pin functions : μ PD75216ACW-B71 (IC102)

2-1. Terminal connection diagram

Pin No.	Pin name	I/O	Function
1-4	Sd-Sa	O	FL segment control terminals (also used for key scan signal)
5	SENSE	O	Signal detection terminal for SENSE signal from processor and servo ICs.
6	SQCK	O	Q data read clock output terminal.
7	SQSO	O	Q data input terminal.
8	SI	-	N.C.
9	REMCN	I	Remote control input terminal
10	SCOR	I	Sub-code frame sync detection signal input terminal.
11	FOKP	I	Input terminal for FOK signal from RF amp. (focus OK : 'H')
12	GFS	I	Frame sync signal input terminal. ('H' : frame sync)
13-15	A0-2	O	Control address for control register of CXD1095.
16	RD	O	Read control signal for CXD1095.
17	WR	-	Write control signal for CXD1095.
18	DTA	O	Control serial data to CXD2500 and CXA1372.
19	SDATA	I/O	Serial data signal input / output terminal.
20	CLK	O	Clock for serial data to CXD2550 and CXA1372.
21-24	KD0-3	I	Input terminal for key return signal from key matrix.
25-28	D0-3	I/O	Data bus to CXD1095. (LSB 4-bits)
29	DIRC	O	DIRC signal output to CXA1372.
30	X1	I	Input terminal of system clock. (4.23MHz)
31	X2	-	Not used.
32	Vss	-	GND.
33	XT1	-	GND.
34	XT2	-	N.C.
35-38	D4-7	-	Data bus to CXD1095.(MSB 4-bits)
39	RESET	I	Reset input terminal. (active 'L')
40-48	G1-9	O	FL digit control terminals.
49,50	T9,10	-	N.C.
51-55	So-k	O	FL segments control terminals. (also used for key scan signal)
56	VLOAD	I	FL driver negative power supply. (-30V)
57	VPRE	I	FL pre-driver negative power supply. (-5V)
58-63	Sj-e	O	FL segment control terminals. (also used for key scan signals)
64	VDD	I	Power supply. (+5V)



CIRCUIT DESCRIPTION

2-3. Pin functions : CXD1095 (IC103)

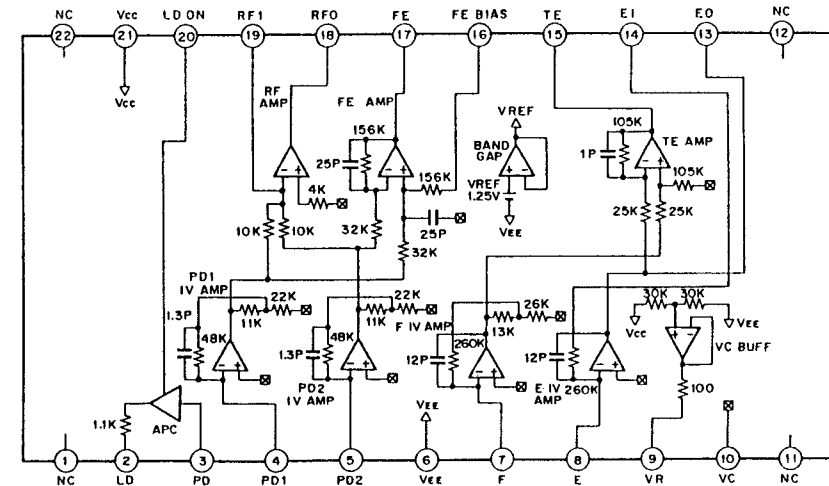
Pin No.	Pin name	I/O	Functions
1,2	N.C.	I	
3-9	DB1-7	I/O	Data input/output terminals for RAM (LC3518). (MSB 7-bits).
10	Vss	-	GND.
11-13	A8-10	O	Access address to LC3518.
14	-	-	Not used.
15	OPNSW	I	Tray open switch. (Open : 'L')
16	CLSSW	I	Tray close switch. (Close : 'L')
17	SLSW	I	Sled limit switch. (SW ON : 'L')
18	PC7	-	Not used.
19	N.C.	-	
20	RMUTE	O	Relay mute. (Active 'L')
21	VLDWN	O	Motor driven volume to counter clock wise. (Active 'H')
22	LDATA	O	20-LEDs control data.
23	XLT	O	Latch signal of ending data output to LSI.
24	CLK	O	Clock signal for 20-LEDs control
25	Vss	-	GND.
26	Vdd	-	Power supply. (+5V)
27	FLSG	O	Display off : 'H'.
28	LATCH	O	Latch signal of ending data output of 20-LEDs.
29	VLLED	O	LED indicator of motor driven volume. (In turning volume knob, LED blinks)
30-32	D0-2	I/O	Data bus to microprocessor. (LSB 3-bits)
33,34	N.C.	-	
35-39	D3-7	I/O	Data bus to microprocessor. (MSB 5-bits)
40	CLR	I	Connect to RESET circuit.
41	OPEN	I	Connect to RESET circuit.
42	Vss	-	GND
43	WR	I	Write strobe signal to write data from microprocessor to CXD1095.
44	RD	I	Read strobe signal to read data from CXD1095 to microprocessor.
45	CS	I	Connect to GND.
46-48	A0-2	O	Address for ports and control register.
49	WE	O	Write enable to write data to LC3518. (Write : 'L')
50	OE	O	Connect to 'H' level.
51	N.C.	-	
52	VLUP	O	Motor driven volume to clockwise. (Active 'H')
53	BUSY	I/O	Serial busy signal input / output terminal.
54-56	PA0-2	O	Address port to LC3518. (LSB 3-bits)
57	Vss	-	GND.
58	Vdd	-	Power supply (+5V).
59-63	PA3-7	O	Address port to LC3518. (center 5-bits)
64	DB0	I/O	Data input / output terminal to LC3518. (LSB)

CIRCUIT DESCRIPTION

3. RF amplifier : CXA1471S (IC104)

CXA1471 is an IC developed for compact disc players. It contains an RF amplifier for 3 spot optical pickup, focus error amplifier, tracking error amplifier, and APC circuit.

3-1. Block diagram



3-2. Pin functions

Pin No.	Pin name	I/O	Function
2	LD	O	APC LD amplifier output pin.
3	PD	I	APC LD amplifier input pin.
4	PD1	I	RF I-V amplifier inverted input pin. Current input by connecting to the photo diode A+C terminals.
5	PD1	I	RF I-V amplifier inverted input pin. Current input by connecting to the photo diode B+D terminals.
7	F	I	F I-V amplifier inverted input pin. Current input by connecting to the photo diode F terminal.
8	E	I	E I-V amplifier inverted input pin. Current input by connecting to the photo diode E terminal.
9	VR	O	CD voltage output pin of (Vcc+Vee) / 2.
10	VC	I	Connected GND when using dual power supply (±). Connected to VR (pin 9) when using a single power supply.
13	EO	O	E output of I-V amplifier.
14	EI	-	E I-V amplifier feedback input pin. For E I-V amplifier gain adjustment.
15	TE	O	Tracking error amplifier output pin.
16	FE-BIAS	I	Bias pin on the focus error amplifier non-inverted side.
17	FE	O	Focus error amplifier output pin.
18	RFO	O	RF summing amplifier output pin.
19	RFI	I	Inverted input pin of RF amplifier. Gain of amplifier is fixed by resistor between RFO and RFI.
20	LD-ON	I	LD ON / OFF select pin. (Vcc : ON)

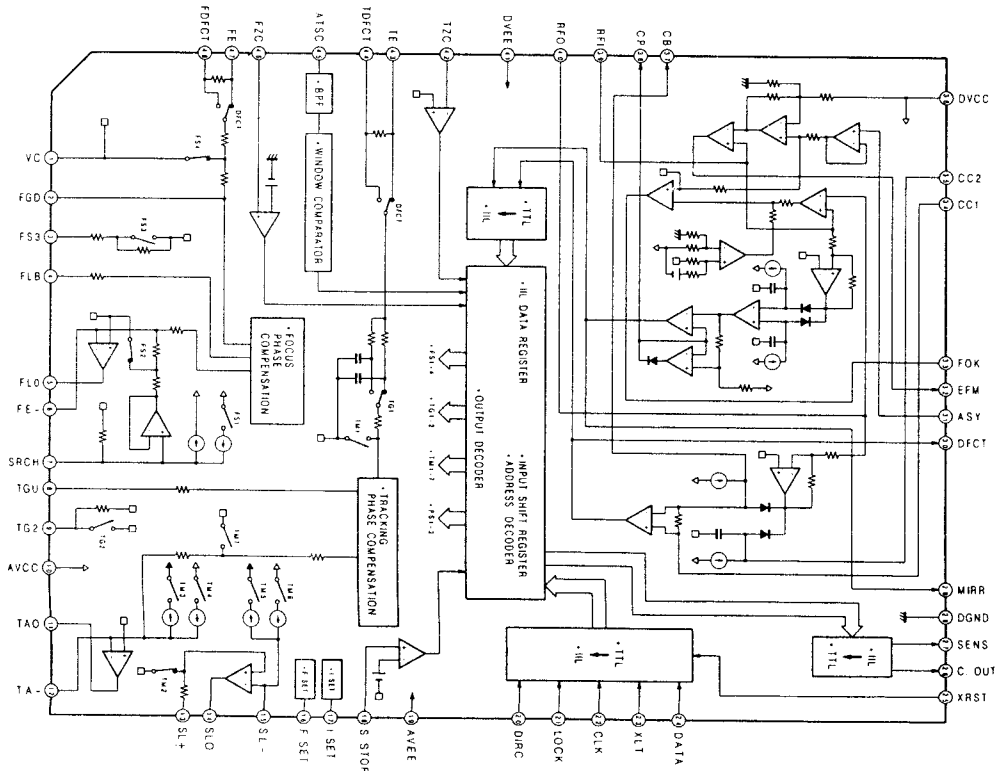
CIRCUIT DESCRIPTION

4. Servo Signal Processor : CXA1372Q (IC105)

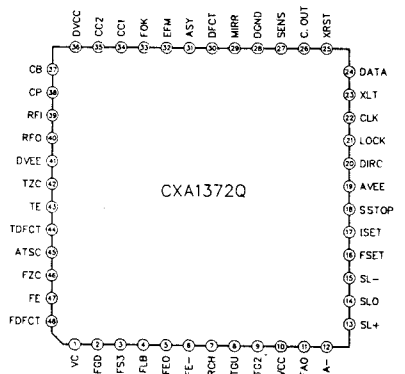
Outline
 CXA1372Q is a bipolar IC developed to be used for processing of the RF signal (Focus OK, mirror, defect, comparator of EFM) and servo control.

- Functions**
- Auto asymmetry control
 - Focus OK detection circuit
 - Mirror detection circuit
 - Defect detection and countermeasure circuit
 - EFM comparator
 - Focus servo control
 - Tracking servo control
 - Thread servo control

4-2. Block diagram



4-1. Pin connection



CIRCUIT DESCRIPTION

4-3. Pin functions

Pin No.	Pin name	I/O	Function
1	VC	I	Middle-point voltage input terminal. When two power sources are used : GND, when single power source is used : (Vcc+GND)/2.
2	FGD	I	When lowering the high-band gain of the focus servo, insert a capacitor between this terminal and terminal No. 3.
3	FS3	I	Change the high-band gain of the focus servo by turning FS3 on and off.
4	FLB	I	Outside terminal of time constant for raising the low-band of the focus servo.
5	FEO	O	Focus drive output.
6	FE-	I	Inverted input terminal of focus amplifier.
7	SRCH	I	Outside terminal of time constant for making focus search waveform.
8	TGU	I	Outside terminal of time constant for changing high-band gain of tracking.
9	TG2	I	Outside terminal of time constant for changing high-band gain of tracking.
10	AVCC		
11	TAO	O	Tracking drive output.
12	TA-	I	Inverted input terminal of tracking amplifier.
13	SL+	I	Non-inverted input terminal of thread amplifier.
14	SLO	O	Thread drive output.
15	SL-	I	Inverted input terminal of thread amplifier.
16	FSET	I	Terminal for setting the peak for phase compensation of focus tracking.
17	ISET	I	Current for determining the height of the focus search track jump thread kick is applied.
18	SSTOP	I	Terminal for ON/OFF detecting signal of limit switch for detecting the most inside line of disc.
19	AVEE		
20	DIRC	I	Used to jump over one track. 47kΩ pull-up resistor is inserted.
21	LOCK	I	When "L", thread runaway-preventive circuit operates. 47kΩ pull-up resistor is inserted.
22	CLK	I	Clock input for transferring the serial data from CPU (having no pull-up resistors).
23	XLT	I	Latch input from CPU (having no pull-up resistors).
24	DATA	I	Serial data input from CPU (having no pull-up resistors).
25	XRST	I	Reset when reset input terminal is at "L" (having no pull-up resistors).
26	SENS	O	Outputs FZC, AS, TZC, SSTOP, etc. on receipt of command from CPU.
27	C. OUT	O	Signal output for counting tracks.
28	DGND		
29	MIRR	O	Output terminal of MIRR comparator. (DC voltage : Load of 10kΩ connected)
30	DFCT	O	Output terminal of DEFECT comparator. (DC voltage : Load of 10kΩ connected)
31	ASY	I	Input terminal of auto asymmetry control.
32	EFM	O	Output terminal of EFM comparator. (DC voltage : Load of 10kΩ connected)
33	FOK	O	Output terminal of focus OK comparator. (DC voltage : Load of 10kΩ connected)
34	CC1	I	DEFECT bottom hold output terminal.
35	CC2	O	Terminal in which DEFECT bottom hold output is input after capacitive coupling.
36	DVCC		
37	CB	I	Terminal to which DEFECT bottom hold capacitor is connected.
38	CP	I	Terminal for connecting MIRR hold comparator. Non-inverted input terminal of MIRR comparator.
39	RFI	I	Terminal in which output of RF summing amplifier is input after capacitive coupling.
40	RFO	O	Output terminal of RF summing amplifier. Check point of eye pattern.
41	DVEE		
42	TZC	I	Input terminal of tracking zero cross comparator.
43	TE	I	Input terminal of tracking error.
44	TDFCT	I	Terminal for connecting the capacitor for time constant in case of defect.
45	ATSC	I	Input terminal of window comparator for detecting ATSC.
46	FZC	I	Terminal for inputting the focus zero cross comparator.
47	FE	I	Input terminal of focus error.
48	FDFCT	I	Terminal for connecting capacitor for time constant in case of defect.

CIRCUIT DESCRIPTION

5. Digital Signal Processor : CXD2500Q (IC9)

Outline

The CXD2500Q is a digital signal processing LSI for a compact disc player, which has the following functions.

- A wide frame jitter margin realized by 32-KRAM (±28 frames)
- Bit clocks for strobing EFM signal are generated by the digital PLL, and the capture range is ±150kHz minimum
- Demodulation of EFM data
- Protection and reinforcement of EFM frame sync signal
- Strong error correction by refined super strategy. C1 : Double correction, C2 : Quadruple correction
- Double-speed replay and variable pitch replay
- Reduction of noise generation at track jumps
- Auto zero cross muting
- Demodulation of sub-code and detection of errors in sub-code Q data

- Digital spindle servo (Having over-sampling filter)
- 16-bit traverse counter
- CPU interface by serial bus
- A built-in servo auto sequencer
- Output for digital audio interface
- Built-in digital level meter and peak meter
- Applicable to bilingual system

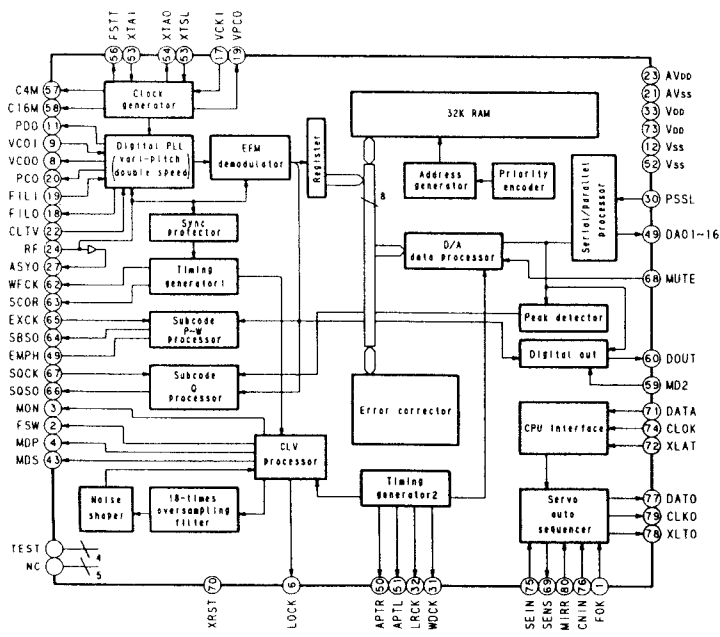
Features

- One chip of this LSI can process all the digital signals used for replay
- Integration level can be heightened because of the built-in RAM

Structure

Silicon gate CMOS

5-1. Block diagram



CIRCUIT DESCRIPTION

5-2. Pin functions

Pin No.	Pin name	I/O	Function
1	FOK	I	Focus OK input terminal. Used for SENS output and servo auto sequencer.
2	FSW	O	Output for changing output filter of spindle motor.
3	MON	O	ON/OFF control output of spindle motor.
4	MDP	O	Servo control of spindle motor.
5	MDS	O	Servo control of spindle motor.
6	LOCK	O	Outputs "H", when GFS is sampled at 460Hz and it is "H". Output "L", if "L" is detected eight times continuously.
7	NC	-	Not used.
8	VCOO	O	Oscillation circuit output for analog EFM PLL.
9	VCOI	I	Oscillation circuit input for analog EFM PLL. f _{lock} = 8.6436MHz
10	TEST	I	Test terminal, normally grounded.
11	PDO	O	Charge pump output for analog EFM PLL.
12	Vss	-	GND.
13-15	NC	-	Not used.
16	VPCO	O	PLL charge pump output for variable pitch.
17	VCKI	I	Clock input f _{center} = 16.9344MHz from outside VCO for variable pitch.
18	FILO	O	Filter output for master PLL (Slave = Digital PLL).
19	FILI	I	Filter input for master PLL.
20	PCO	O	Charge pump output for master PLL.
21	AVss	-	Analog GND.
22	CLTV	I	VCO control voltage input for master.
23	AVDD	-	Analog power source (+5V).
24	RF	I	EFM signal input.
25	TEST2	I	Used for grounding.
26	TEST3	I	Used for grounding.
27	ASYO	O	EFM full swing output ("L" = Vss, "H" = VDD).
28	TEST4	I	Used for grounding.
29	NC	-	Not used.
30	PSSL	I	Audio data output mode changing input. Set to "L" for serial output and "H" for parallel output.
31	WDCK	O	D/A interface for 48-bit slot. Word clock f = 2 Fs
32	LRCK	O	D/A interface for 48-bit slot. LR clock f = Fs
33	VDD	-	Source voltage (+5V).
34	DA16	O	Outputs DA16 (MSB) when PSSL = 1. Outputs serial data of 48-bit slot when PSSL = 0. (2s' COMP, MSB first)
35	DA15	O	Outputs DA15 when PSSL = 1. Outputs bit clock of 48-bit slot when PSSL = 0.
36	DA14	O	Outputs DA14 when PSSL = 1. Outputs serial data of 64-bit slot when PSSL = 0. (2s' COMP, LSB first)
37	DA13	O	Outputs DA13 when PSSL = 1. Outputs bit clock of 64-bit slot when PSSL = 0.
38	DA12	O	Outputs DA12 when PSSL = 1. Outputs LR clock of 64-bit slot when PSSL = 0.
39	DA11	O	Outputs DA11 when PSSL = 1. Outputs GTOP when PSSL = 0.
40	DA10	O	Outputs DA10 when PSSL = 1. Outputs XUGF when PSSL = 0.
41	DA09	O	Outputs DA09 when PSSL = 1. Outputs XPLCK when PSSL = 0.
42	DA08	O	Outputs DA08 when PSSL = 1. Outputs GFS when PSSL = 0.
43	DA07	O	Outputs DA07 when PSSL = 1. Outputs RFCK when PSSL = 0.
44	DA06	O	Outputs DA06 when PSSL = 1. Outputs C2PO when PSSL = 0.
45	DA05	O	Outputs DA05 when PSSL = 1. Outputs XRAOF when PSSL = 0.
46	DA04	O	Outputs DA04 when PSSL = 1. Outputs MNT3 when PSSL = 0.
47	DA03	O	Outputs DA03 when PSSL = 1. Outputs MNT2 when PSSL = 0.
48	DA02	O	Outputs DA02 when PSSL = 1. Outputs MNT1 when PSSL = 0.
49	DA01	O	Outputs DA01 when PSSL = 1. Outputs MNT0 when PSSL = 0.

CIRCUIT DESCRIPTION

Pin functions

Pin No.	Pin name	I/O	Function
50	APTR	O	Control output for correcting aperture. Set to "H" when Rch.
51	APTL	O	Control output for correcting aperture. Set to "H" when Lch.
52	Vss	-	GND.
53	XTAI	I	X'tal oscillation circuit input of 16.9344MHz, or input of 33.8688MHz.
54	XTAO	O	X'tal oscillation circuit output of 16.9344MHz.
55	XTSL	I	X'tal selection input terminal. Set to "L" when x'tal is 16.9344MHz, and to "H" when 33.8688MHz.
56	FSTT	O	2/3 division output of terminals 53 and 54. Does not vary as pitch varies.
57	C4M	O	4.2336MHz output. Varies as pitch varies.
58	C16M	O	16.9344MHz output. Varies as pitch varies.
59	MD2	I	Digital-out ON/OFF control. Turns on when "H", and off when "L".
60	DOUT	O	Digital-out output terminal.
61	EMPH	O	Outputs "H" when playing disc has emphasis, and "L" when the latter does not.
62	WFCK	O	WFCK (Write Frame Clock) output.
63	SCOR	O	Outputs "H" when sub-code sync S0 or S1 is detected.
64	SBSO	O	Serial output of Sub P - W.
65	EXCK	I	Clock input for SBSO read out.
66	SQSO	O	Sub Q 80-bit and PCM peak, and level data 16-bit output.
67	SQCK	I	Clock input for SQSO read out.
68	MUTE	I	Mutes when "H", and resets when "L".
69	SENS	-	Outputs SENS to CPU.
70	XRST	I	Resets system when "L".
71	DATA	I	Inputs serial data from CPU.
72	XLAT	I	Latches serial data when latch input from CPU falls.
73	Vdd	-	Power supply (+5V).
74	CLOCK	I	Serial data transfer clock input from CPU.
75	SEIN	I	Input SENS from SSP.
76	CNIN	I	Inputs signals for counting number of track jumps.
77	DATO	O	Outputs serial data to SSP.
78	XLTO	O	Outputs serial data latch to SSP, and latches at fall.
79	CKO	O	Outputs serial data transfer clock to SSP.
80	MIRR	I	Inputs mirror signal. Auto sequencer uses this for jumping 128 or more tracks.

Notes

- The 64-bit slot is 2's compliment output of LSB first, and the 48-bit slot is 2's compliment output of MSB first.
- GTOP is used to monitor the protective condition of the frame sync. ("H" : Sync protective window is released.)
- XUGF is the frame sync obtained from the EFM signal, which is a negative pulse. This is the signal before the protection of sync.
- XPLCK is the inverted clock of EFM PLL. PLL is so made that the falling edge will be matched to the change point of the EFM signal.
- The GFS becomes "H" when the frame sync is matched to the internal protection timing.
- RFCK is a signal having the period of 136μ obtained by the accuracy of X'tal.
- C2P0 is a signal indicating the error condition of data.
- XRAOF is a signal generated when 32 KRAM exceeds the jitter margin of ±28F.

CIRCUIT DESCRIPTION

6. Digital Filter : SM5840CP (IC7)

Outline

This LSI is a digital filter for 8 times over-sampling (interpolation) for a digital audio playback device. This is LSI accepts not only 16 bit signals but also 18 bit signals, and outputs 16, 18 or 20 bit signals. Accordingly, this LSI can be a wide interface.

In addition, this LSI has the digital de-emphasis function matched to 3fs, the noise shaping function to reduce re-quantized noises, etc.

Features and functions

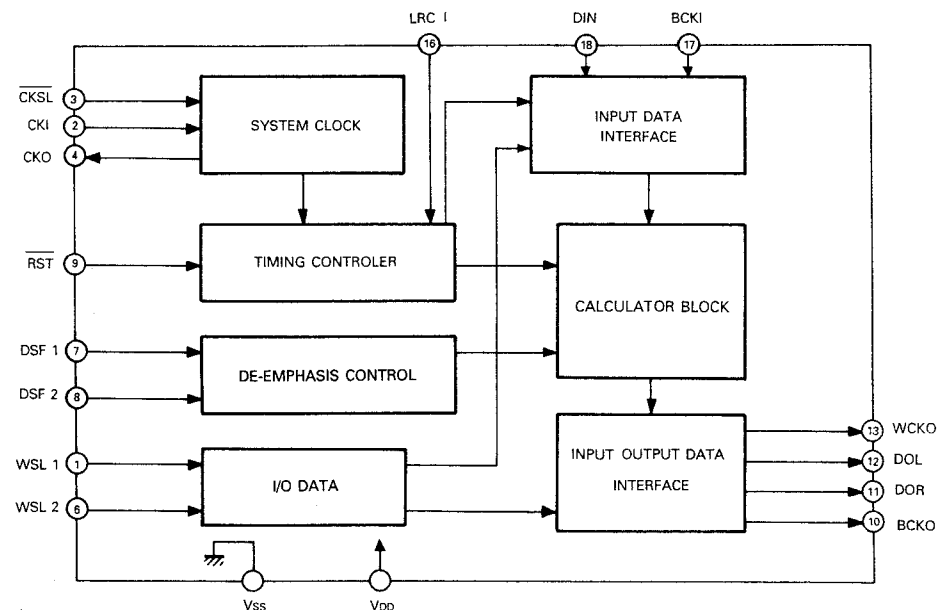
- 2 channel processing
- 8 times over-sampling (interpolation) (Hereinafter referred to as 8fs)
- Digital de-emphasis (Matched to 3fs of 48kHz, 44.1kHz and 32kHz)
- Serial input data
Complementary number of 2, MSB first, selection of 16 or 18 bit signal
- Serial output data
MSB first, complementary number of 2, selection of 16 or 18 bit signal

- Primary noise shaper (Turned on only when 16 or 18 bit signal is output)
- Selection of system clock of 256fs or 384fs
- Input / Output TTL compatible
- Signal power source of 5V (Standard)
- Can be operated with low voltage (3.2V)
- 18 pin plastic DIP

Composition of filter

- Interpolation of filter (Straight line phase FIR filters of 3 stages)
1st stage (fs → 2fs) : Degree 69
2nd stage (2fs → 4fs) : Degree 13
3rd stage (4fs → 8fs) : Degree 9
- De-emphasis filter
Accurate gain and phase characteristics are obtained by the composition of IIR filter
- Highly accurate calculation with (19 × 14) bit parallel multiplier and 24 bit accumulator
- Built in overflow limiter

6-1. Block diagram



CIRCUIT DESCRIPTION

6-2. Pin connections

(TOP VIEW)

WSL1	1	18	DIN
CKI	2	17	BCKI
CKSL	3	16	LRCI
CKO	4	15	(NC)
VSS	5	14	VDD
WSL2	6	13	WCKO
DSF1	7	12	DOL
DSF2	8	11	DOR
RST	9	10	BCKO

6-3. Explanation of terminals

("fs" in the following explanation represents the sampling frequency of the data.)

Pin No.	Pin name	I/O	Function				
			Setting of terminal		Noise shaper	I/O data word length	
1	WSL1	Ip	Input / Output data word length.			OFF	Number of bits of Input/Number of bits of output
			WSL1	WSL2	18bit		20bit
			H	L	18bit		20bit
			L	H	16bit		18bit
			L	L	16bit	16bit	
2	CKI	I	Input terminal of system clock.				
3	CKSL	I	System clock selection terminal (384fs when CKSL is 'H'), (256fs when CKSL is 'L').				
4	CKO	O	System clock output terminal (CKI clock is buffered, then output).				
5	Vss	-	GND.				
6	WSL2	Ip	Input / Output data word length selection terminal 2.				
7	DSF1	Ip	De-emphasis selection terminal 1.		ON /OFF	De-emphasis fs	
			DSF1	DSF2		44.1kHz	
			L	L		48.0kHz	
			H	H		32.0kHz	
8	DSF2	Ip	De-emphasis selection terminal 2.		OFF	-	
			L	L			
			H	H			
			H	L			
9	RST	Ip	System resetting (Resets and initializes when RST is 'L'.)				
10	BCKO	O	Output bit clock.				
11	DOR	O	Rch 8fs data output.				
12	DOL	O	Lch 8fs data output.				
13	WCKO	O	Output word clock.				
14	Vdp	-	Power source terminal (Standard 5V).				
15	(NC)	-	(Terminal not connected.)				
16	LRCI	Ip	Sample rate (fs) clock of input data .				
17	BCKI	Ip	Input bit clock.				
18	DIN	Ip	Input data.				

CIRCUIT DESCRIPTION

7. Zero Cross Data Selector : SM5827CP (IC12)

Outline

This IC observes and detects infinity 0 of the 2 channel serial audio signals output from the signal processing LSI of CD etc., and generates and outputs reset signals for 1 bit DAC etc.

Functions

- Observes and detects infinity 0 of the serial audio signals of L and R channels independent from each other.

Bit clock frequency	Infinity 0 lasting time (fs=44.1kHz)
32fs	0.372sec
48fs	0.248sec

When infinity 0 lasts for the above time, the following reset signals are output.

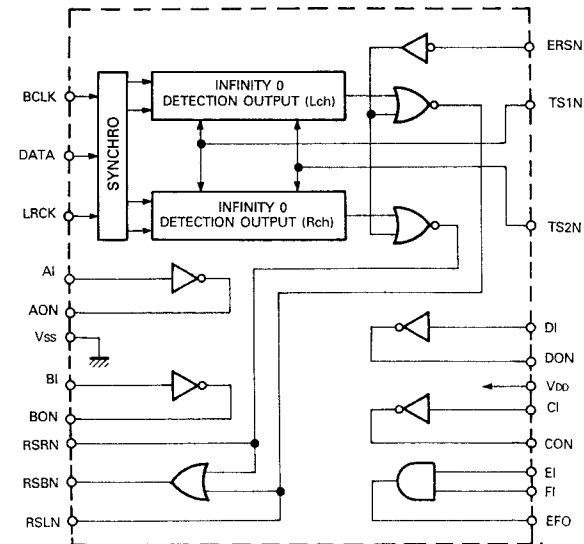
- Outputs the reset signal of 1 bit DAC of the following 3 types. Lch reset output, Rch reset output, and (Lch and Rch) reset output.
- Contains 4 inverters for generating complementary data signal.
- Contains a 2 input and elements.

7-1. Pin connections

(TOP VIEW)

(NC)	1	30	(NC)
(NC)	2	29	(NC)
BCLK	3	28	ERSN
DATA	4	27	TS1N
LRCI	5	26	TS2N
AI	6	25	DI
AON	7	24	DON
VSS	8	23	VDD
BI	9	22	CI
BON	10	21	CON
RSRN	11	20	EI
RSBN	12	19	FI
RSLN	13	18	EFO
(NC)	14	17	(NC)
(NC)	15	16	(NC)

7-2. Block diagram



CIRCUIT DESCRIPTION

7-3. Function of terminals (30 pin shrink DIP)

Pin No.	Pin name	I/O	Functions
1	(NC)	-	
2	(NC)	-	
3	BCLK	Ip	Bit clock input (Ordinary frequency : 32fs or 48fs).
4	DATA	Ip	DATA input (16 bit / serial / LR alternate).
5	LRCK	Ip	LR clock input (fs rate / Duty : 50%), (H / L = Lch Rch).
6	AI	I	A signal input.
7	AON	O	A signal inverted output.
8	Vss	-	GND power supply (0V)
9	BI	I	B signal input.
10	BON	O	B signal inverted output.
11	RSRN	O	Rch infinity 0 detection output (L : Active).
12	RSBN	O	Lch / Rch infinity 0 detection output (L : Active).
13	RSLN	O	Lch infinity 0 detection output (L : Active).
14	(NC)	-	
15	(NC)	-	
16	(NC)	-	
17	(NC)	-	
18	EFO	O	E · F (Logical multiplication) output.
19	FI	I	F signal input.
20	EI	I	E signal input.
21	CON	O	C signal inverted output.
22	CI	I	C signal input.
23	VDD	-	+ Power supply (Type. 5V).
24	DON	O	D signal inverted output.
25	DI	I	D signal input.
26	TS2N	I	Test terminal 2 (H / L = Ordinary / Test).
27	TS1N	I	Test terminal 1 (H / L = Ordinary / Test).
28	ERSN	I	Outside reset input (Microcomputer reset signal) : (L : Active)
29	(NC)	-	
30	(NC)	-	

- Note : 1) 'fs' represents the sampling frequency of the audio signal, which is 44.1kHz for CD.
 2) The input terminal Ip is equipped with a pull-up resistors.
 3) (NC) must not be connected to any thing. Do not use it.

CIRCUIT DESCRIPTION

Function of detect infinity 0

• This function is used to observe infinity 0 of the serial audio (PCM) signals output from the signal processing LSI of etc. If infinity 0 lasts for a certain time, the detection signal is output.

The state of "Infinity 0" in this case means that all bit data of complementary of 2 are 0 and does not mean that the polarity of all data is inverted and they are set to 1. The method to detect infinity 0 in this IC becomes effective when the following inputs are applied.

- (a) 3 wire serial input of BCLK (Bit clock), DATA (Serial data) and LRCK (LR clock).
- (b) If the number of clock of BCLK is larger than the number of bits of DATA, DATA signal must be set to L level in case other than the effective data of DATA (16 bits in ordinary case).

(c) L level of LRCK corresponds the L/R channel as follows; H level = L channel and L level = R channel. Accordingly, if the polarity of LRCK is inverted, the output terminal of the detected signal is inverted.

For the above, see the timing chart in sub-section 7-4.

• The time of infinity 0 is counted by BCLK clock during the period in which the L/R channel data of DATA signals become 0 (L level) respectively. If this counter counts the above condition by 2^{20} times, it outputs a carry output as an infinity 0 detection output. The following 3 detection outputs are used.

- (a) RSLN : Detection of infinity 0 of L channel (L level : Active)
- (b) RSRN : Detection of infinity 0 of R channel (L level : Active)
- (c) RSBN : Detection of infinity 0 of both L and R channels (L level : Active)

RSBN is output when infinity 0 is detected in both L and R channels. These outputs are turned off and the counter is reset at the moment when 1 (H level) is input to the corresponding data.

The relationship between the lasting time of infinity 0 and bit clock necessary to make the detected output active is as follows in case of any output.

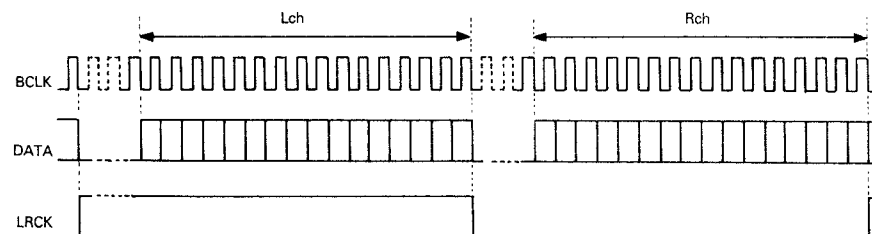
$$TZ = 2^{20} / (NB * fs)$$

At this time, NB is set to the number of pulses (e.g. 32 or 48) in the period of LRCK (fs rate). A concrete example of this calculation is shown below.

Bit clock frequency	Infinity 0 lasting time :TZ (fs=44.1kHz)
32fs	0.372sec
48fs	0.248sec

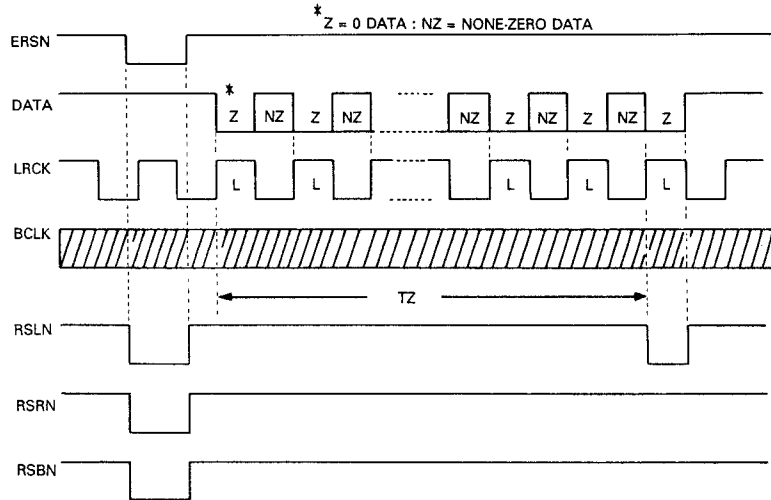
7-4. Timing chart

• Serial input



CIRCUIT DESCRIPTION

• Infinity 0 detection output

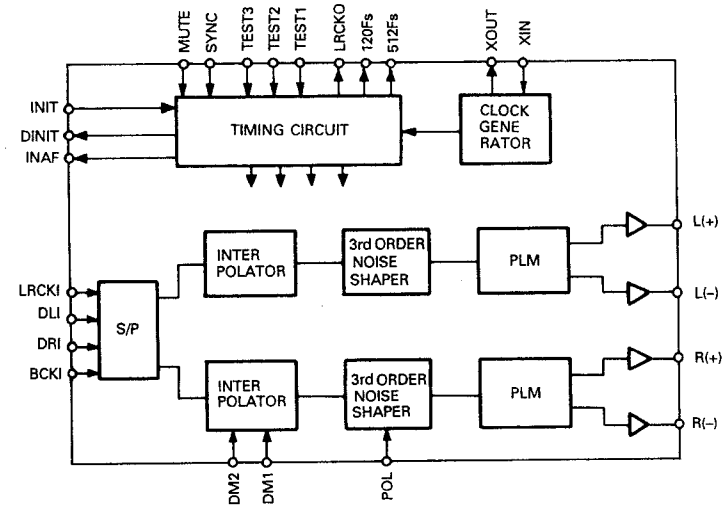


CIRCUIT DESCRIPTION

8. D/A Converter : CXD2552Q (IC6)

CXD2552Q is a pulse D/A converter developed for digital audio devices such as CD players.

8-1. Block diagram



8-2. Pin functions

Pin No.	Pin name	I/O	Functions
1	VDD2	-	Analog power supply.
2	VSS	-	Analog GND.
3	R (-)	O	Rch PLM output (Inverted).
4	VDD	-	Analog power supply.
5	VSS2	-	Analog GND.
6	VSUB	-	Sub straight. Connected to GND.
7	LRCKO	O	LRCK output.
8	DM2	I	Polarity of diza.
9	DM1	I	Appointment of diza.
10	POL	I	Polarity of PLM output. (L : Normal phase, H : Inverted phase)
11	DVDD	-	Digital power supply.
12	TEST3	I	Test terminal. Normally fixed to L level.
13	MUTE	I	Converts INTERPOLATER output into \emptyset data. Effective at H
14	LRCK	I	LRCK input.
15	DRI	I	Rch data input.
16	DLI	I	Lch data input.
17	BCKI	I	BCK input.
18	TEST1	I	Test terminal. Normally fixed to L level.
19	TEST2	I	Test terminal. Normally fixed to L level.
20	SYNC	I	Synchronization control terminal.

CIRCUIT DESCRIPTION

8-2. Pin functions

Pin No.	Pin name	I/O	Functions
21	INIT	I	Re-synchronization at rising edge of this signal.
22	128Fs	O	128Fs output
23	Vsub	-	Sub straight. Connected to GND.
24	512Fs	O	512Fs output.
25	DINIT	O	Delay INIT signal output.
26	INAF	O	Output " H " when input / output are out of synchronization.
27	DVss	-	Digital GND.
28	Vsub	-	Sub straight. Connected to GND.
29	Vss2	-	Analog GND.
30	VDD	-	Analog power supply.
31	L (-)	O	Lch PLM output (Normal phase).
32	Vss	-	Analog GND.
33	VDD2	-	Analog power supply.
34	Vss	-	Analog GND.
35	L (+)	O	Lch PLM output (Normal phase).
36	VDD	-	Analog power supply.
37	Vsub	-	Sub straight. Connected to GND.
38	XVss	-	Clock GND.
39	XIN	I	input terminal of crystal oscillator (1024Fs).
40	XOUT	O	Output terminal of crystal oscillator (1024Fs).
41	XVDD	-	Clock power supply.
42	VDD	-	Analog power supply.
43	R (+)	O	Rch PLM output (Normal phase).
44	Vss	-	Analog GND.

MECHANISM OPERATION DESCRIPTION

Mechanism Operation Description

Fig. 1 shows the relationship of mechanisms in the STOP mode. The OPEN/CLOSE operation of the mechanism and the UP/DOWN operation of the pickup chassis when loading the disc are description below.

Note 1 : The black arrow (OPEN) and the while arrow (CLOSE) in the operation description have the following meanings :

Black arrow (OPEN) : Tray opening direction (Tray OPEN)

White arrow (CLOSE): Tray closing direction (Tray CLOSE)

Note 2 : Figures in the bracket () in the operation description or accompanied with the part name in the diagra show the reference numbers in the Exploded View.

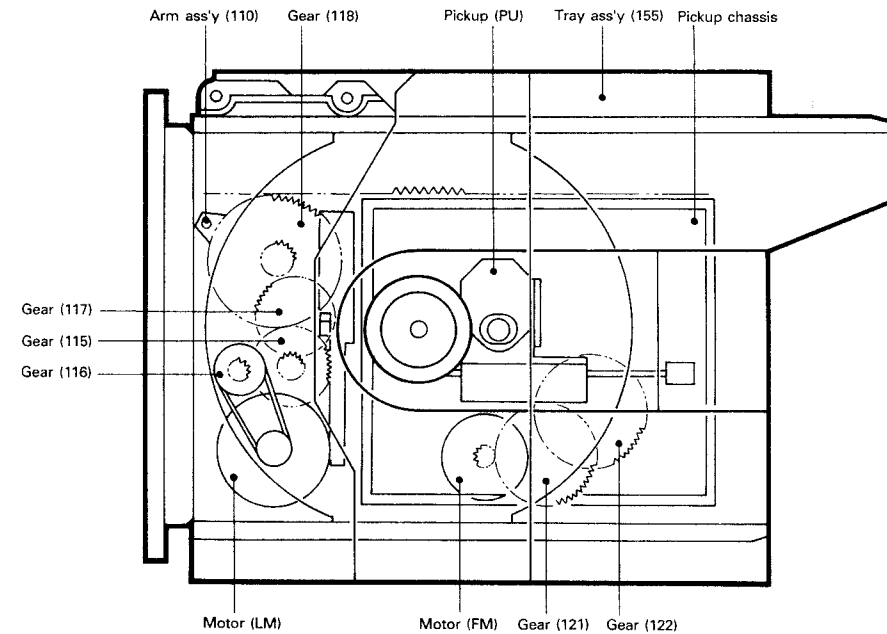


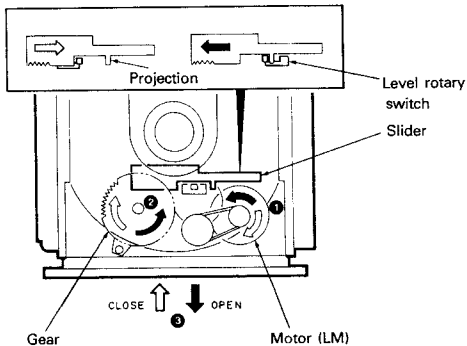
Fig.1

MECHANISM OPERATION DESCRIPTION

MECHANISM OPERATION

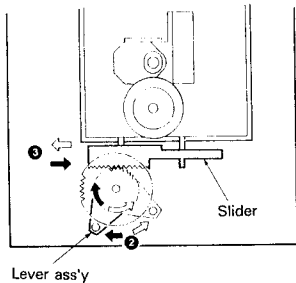
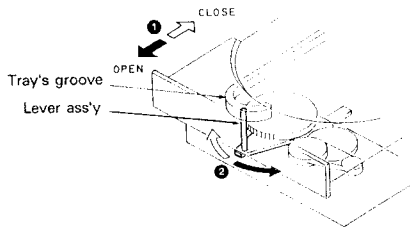
1. OPEN/CLOSE FUNCTION

By the rotation of the loading motor (1), Gear (2) is rotated and the tray starts OPEN/CLOSE operation (3). The OPEN/CLOSE operation stops when the projection of the slider comes in contact with the detection switch (4).

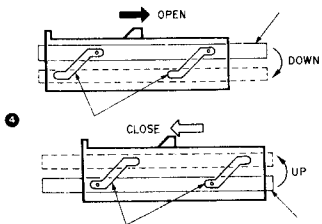


2. PICKUP CHASSIS TRAVELING

According to tray's OPEN/CLOSE operation (1), the shaft of lever moves (2). And then slider travels by the lever with gear (3).



Along with the grooves in the lever, the pickup chassis moves up and down (4).

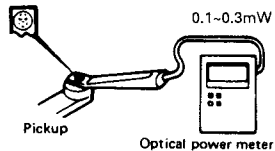


ADJUSTMENT

No.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG
1	LASER POWER		Set the sensor section of the optical power meter on the pickup lens.	Short-circuit pins TEST and turn the power on to enter the test mode. Press the "+10" key to check that the display is "03".		On the power from 0.1 to 0.3mW, when the diffraction grating is correctly aligned with the RF level of 1.0Vp-p or more.	(a)
2	TRACKING ERROR	Test disc Type 4	Connect an oscilloscope as follows. CH1: RF (CN4-1) CH2: TE (CN4-6)	Press the "+10" key. Confirm that the display is "03".	TE BALANCE VR104	Symmetry between upper and lower or DC 0:0.05V	(c)
3	FOCUS ERROR	Test disc Type 4	Connect an oscilloscope as follows. CH1: RF(CN4-1) CH2: TE(CN4-6)	Press the PLAY key. Confirm that the display is "05".	FE BALANCE VR103	Optimum eye pattern	(d)
4	FOCUS GAIN	Test disc Type 4 Apply signal of 1.0kHz, 100mVrms to CN4 pin 2-3.	Connect a LPF to CN4 pin 2-3 to which connect an oscilloscope or AC voltmeters.	Press the PLAY key. Confirm that the display is "05".	FOCUS GAIN VR101	Two VTVMs should read the same value.	(e)
5	TRACKING GAIN	Test disc Type 4 Apply signal of 1.2kHz, 100mVrms to CN4 pin 5-6.	Connect a LPF to CN4 pin 5-6 to which connect an oscilloscope or AC voltmeters.	Press the PLAY key. Confirm that the display is "05".	TRACKING GAIN VR102	Two VTVMs should read the same value.	(e)

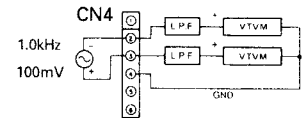
(Note) Type 4 disc: SONY YDS 18 Test Disc or equivalent.
LPF: Around 47kohms+390pF or so.
Step 1-5 are in Test Mode.

(a) Laser Power

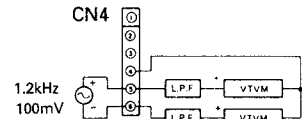


(e) Focus Gain and Tracking Gain Adj.

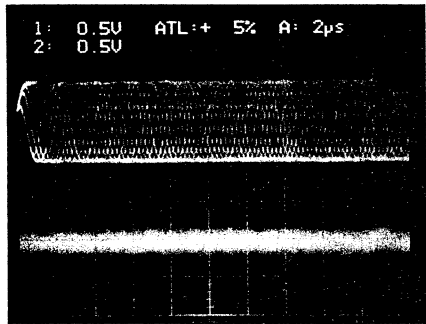
Focus gain Adj.



Tracking gain Adj.



ADJUSTMENT

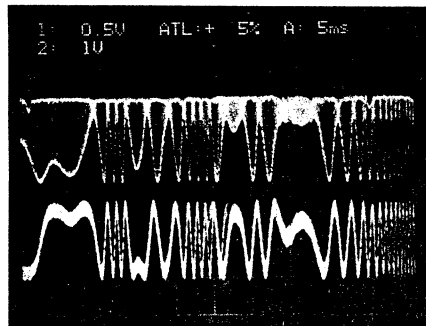


18μs

- RF signal and E.Spot signal in test mode (PLAY).
- If the diffraction grating has been adjusted properly, the influence of triggering is observed on the E.Spot waveform of approx. 18μs after RF signal, in the form of a projection.

CH1 : AC couple
RF signal

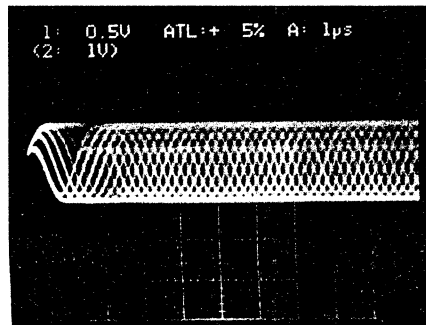
← 0(V)
CH2 : DC couple
TE signal



- RF signal and T.Error signal, in test mode (Focusing ON). (Disc type 4)
- Adjust T.Error so that the waveform is symmetrical above and below 0V. (VR104)

CH1 : AC couple
RF signal

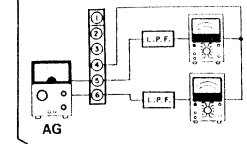
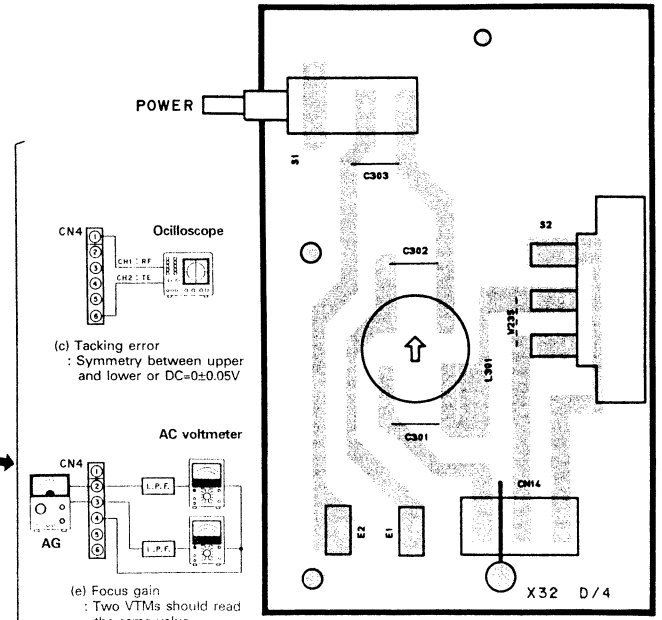
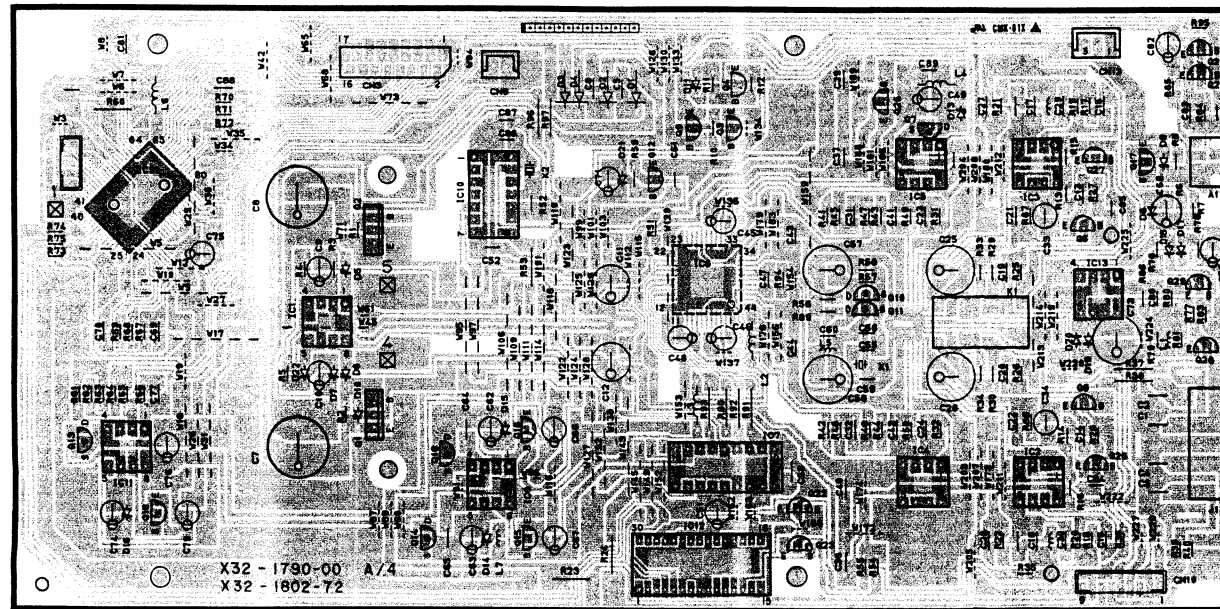
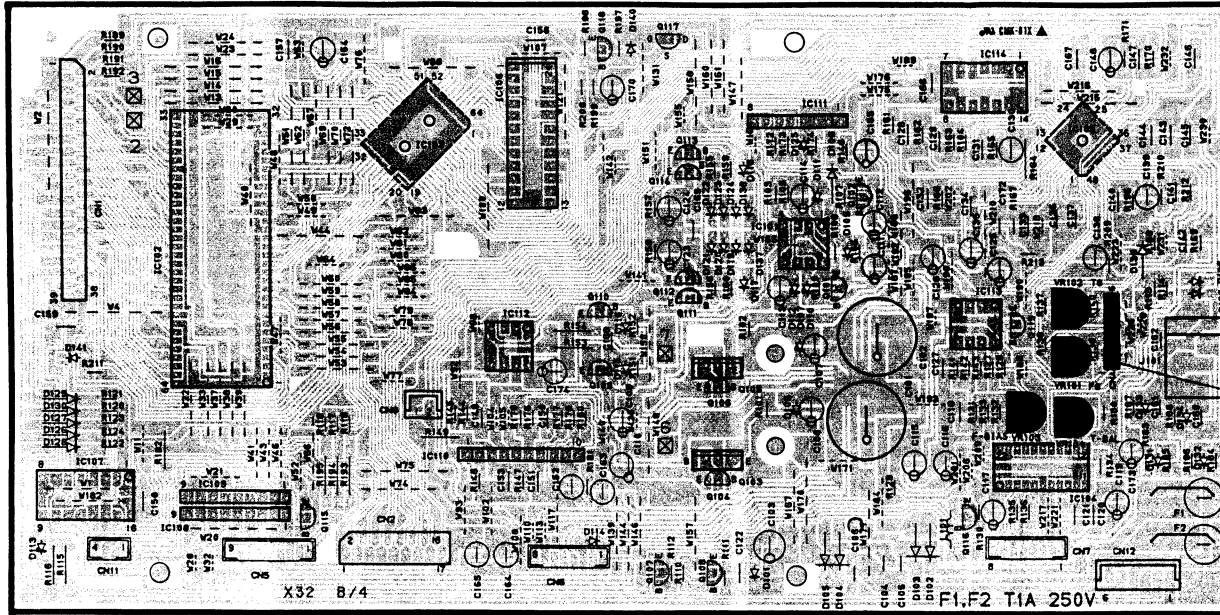
← 0(V)
CH2 : DC couple
TE signal



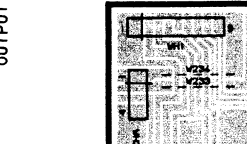
- RF signal in test mode (PLAY).
- Perform the tangential and focusing offset adjustments so that each of the center cross points are focused into one point on the display. The crossing points above and below the center shall also be displayed clearly.

RF signal
AC couple

PC BOARD (COMPONENT SIDE VIEW)



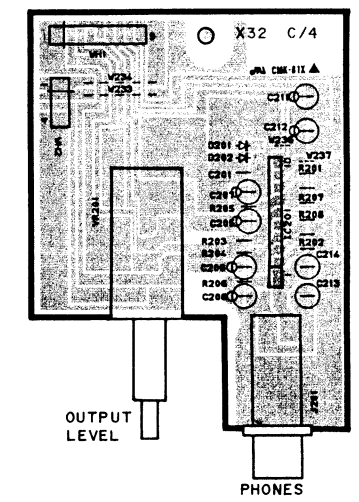
(c) Tracking error
: Symmetry between upper and lower or DC=0±0.05V



(e) Focus gain
: Two VTMs should read the same value.

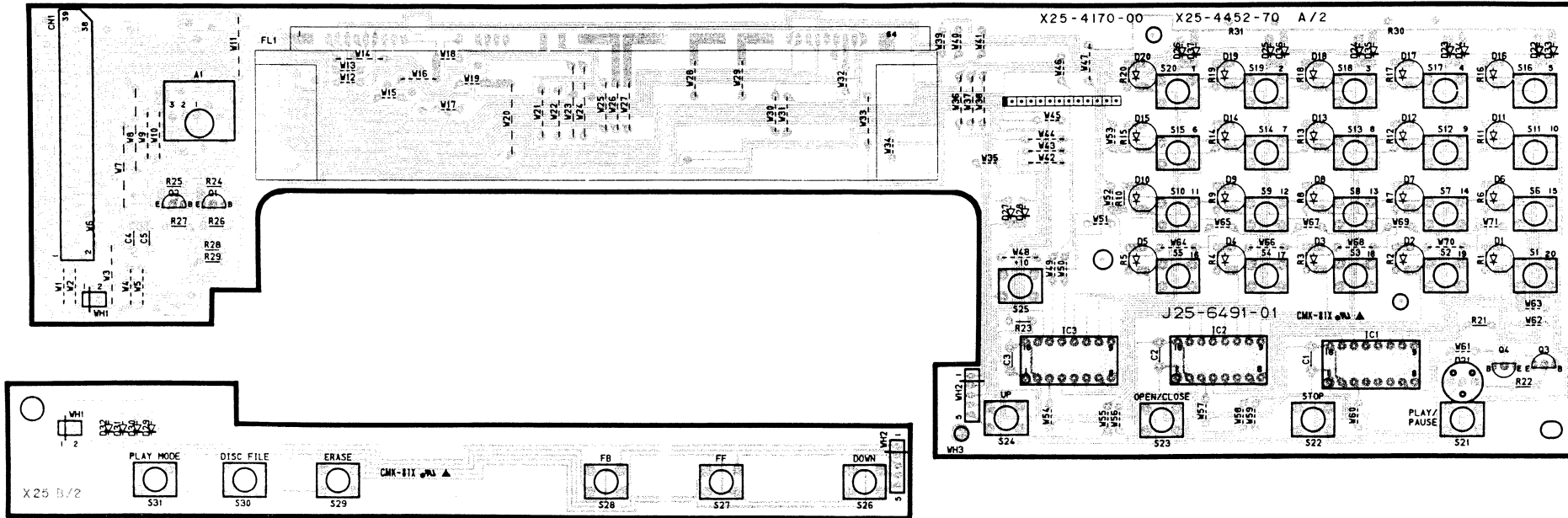


(e) Tracking gain
: Two VTMs should read the same value.



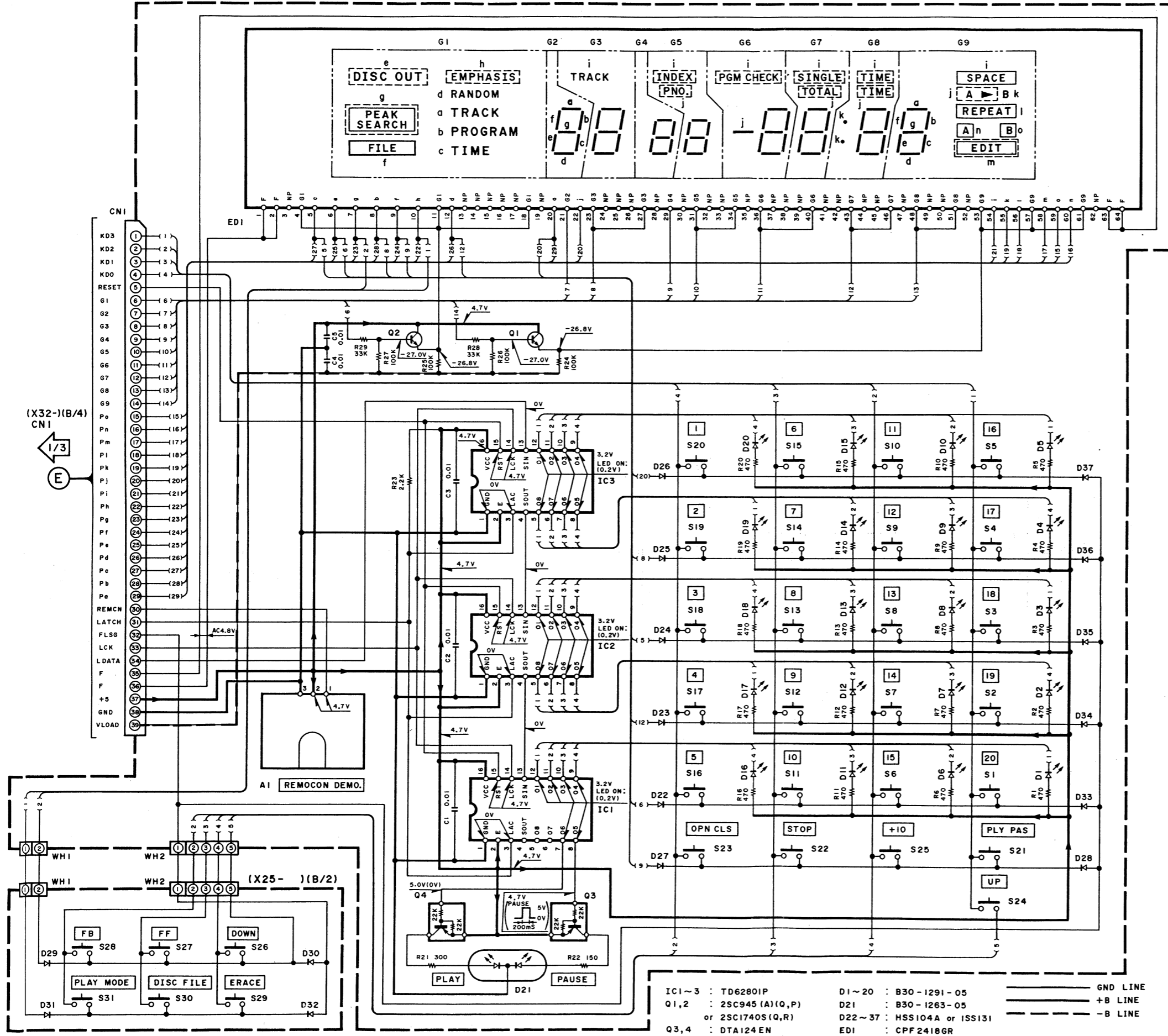
Refer to the schematic diagram for the values of resistors and capacitors.

PC BOARD (COMPONENT SIDE VIEW)



Refer to the schematic diagram for the values of resistors and capacitors.

(X25-4170-00)(A/2) JAPAN MADE (X25-4452-70)(A/2) SINGAPORE MADE

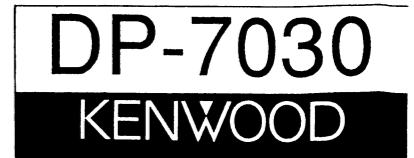


- | | |
|--------------|-----------------|
| 2SK163 | 2SK161 |
| SM5840CP | BA10393N |
| LC3518BSL-15 | SM5827CP |
| CXD1095Q | CXA1372Q |
| CXD2552Q | UPD75216ACW-B71 |
| CXD2500Q | CXA1471S |

CAUTION : For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). Δ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

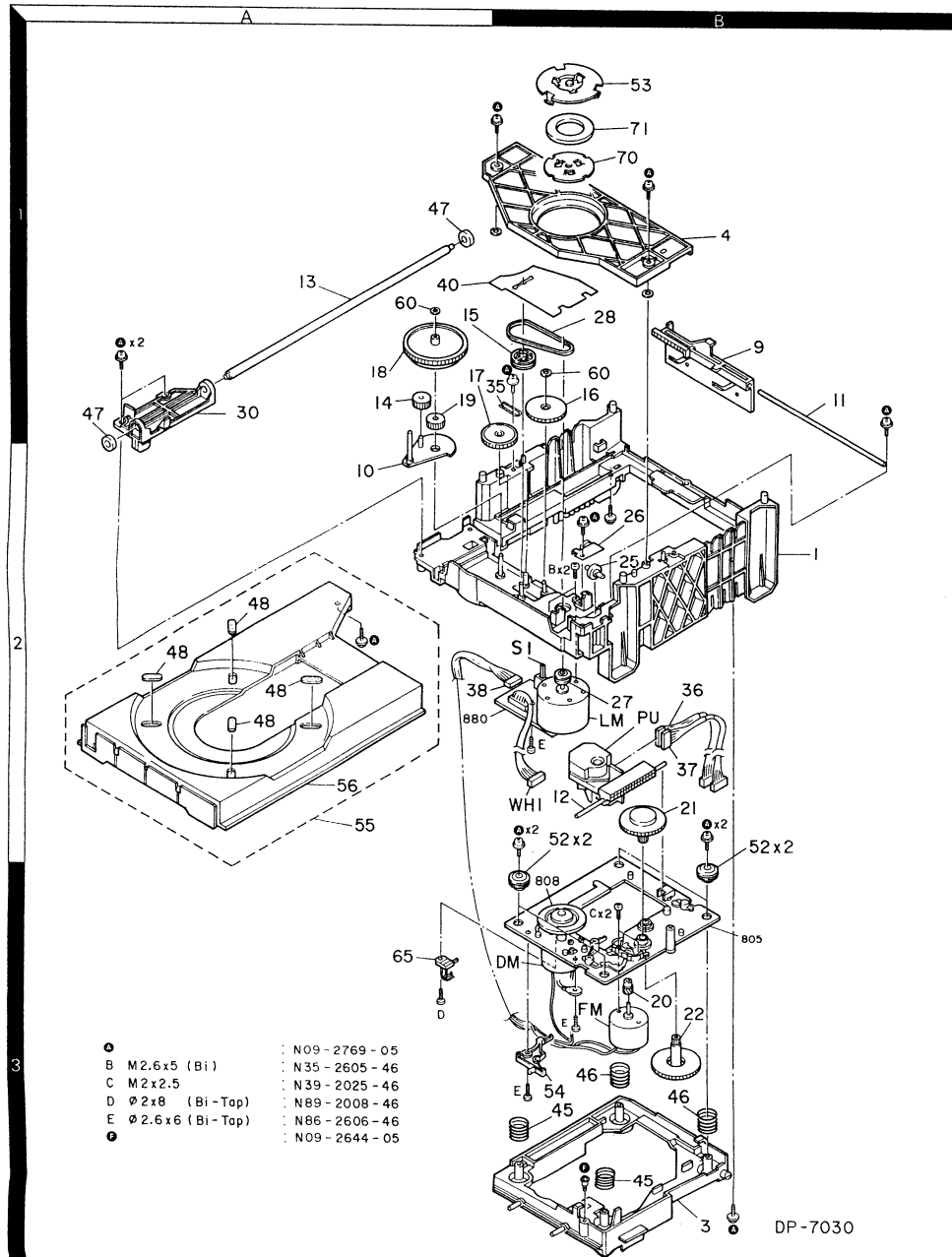
• DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

- | | | |
|------------------------|------------------------------|------------|
| IC1 ~ 3 : TD62801P | D1 ~ 20 : B30-1291-05 | — GND LINE |
| Q1,2 : 2SC945 (A)(Q,P) | D21 : B30-1263-05 | — +B LINE |
| or 2SC1740S (Q,R) | D22 ~ 37 : HSS104A or ISS131 | — -B LINE |
| Q3,4 : DTA124 EN | ED1 : CPF2418GR | |



DP-7030

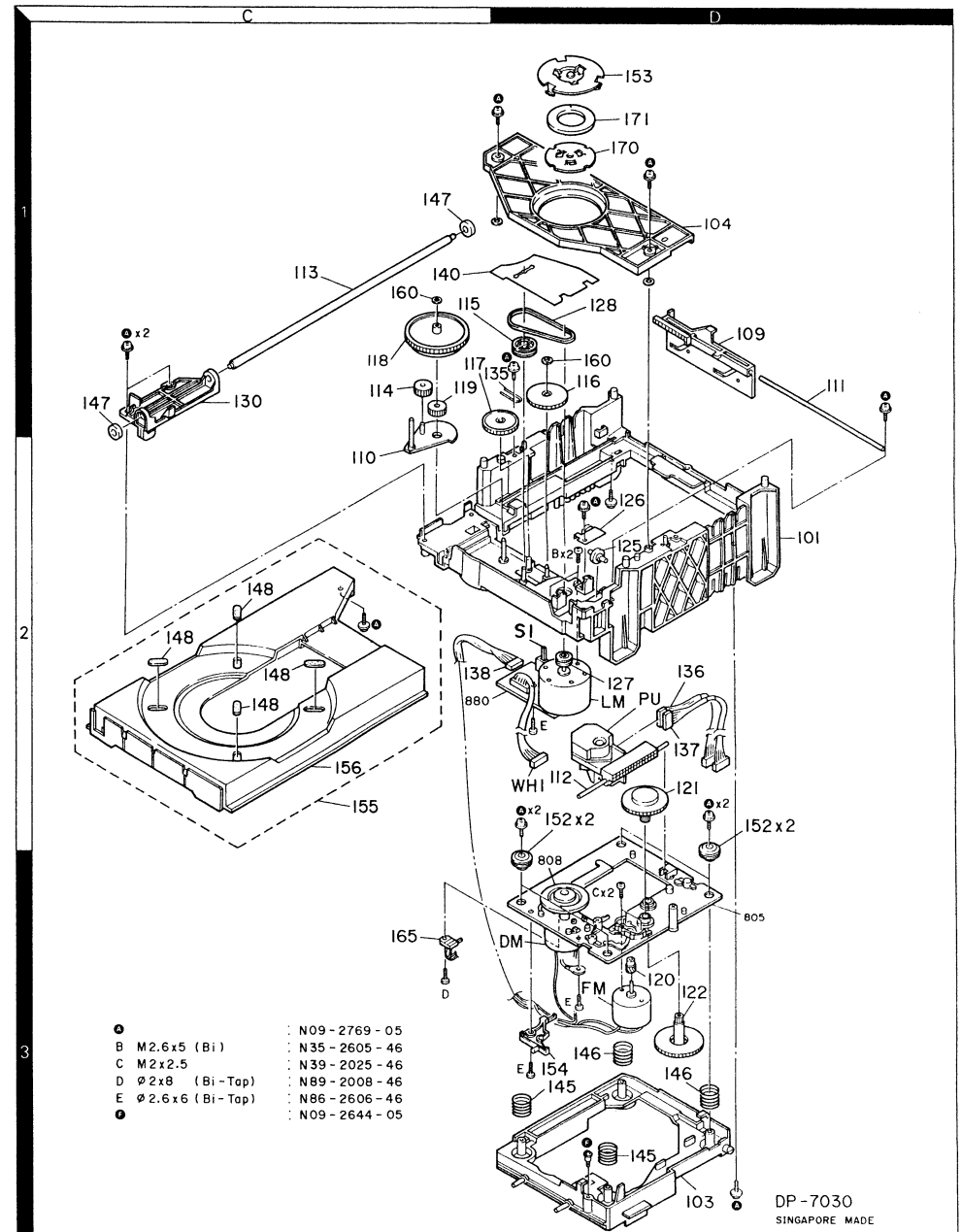
EXPLODED VIEW (MECHANISM) : JAPAN MADE



Parts with the exploded numbers larger than 700 are not supplied.

DP-7030

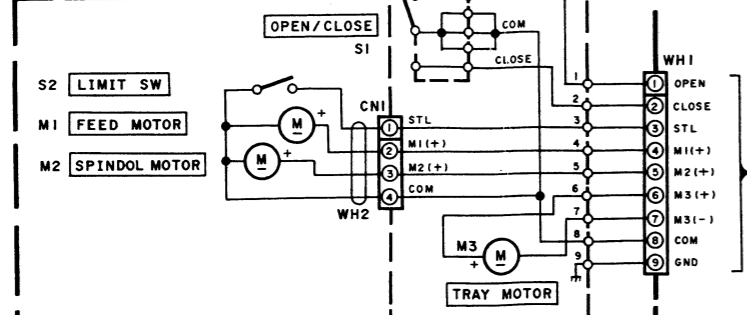
EXPLODED VIEW (MECHANISM) : SINGAPORE MADE



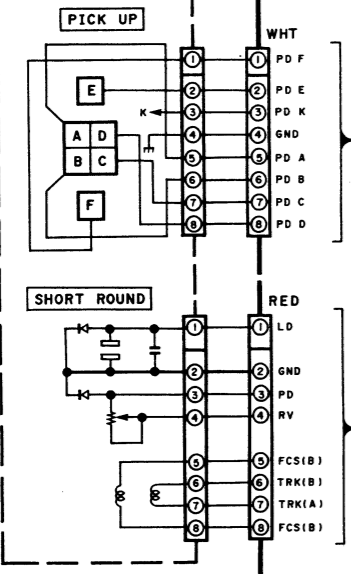
Parts with the exploded numbers larger than 700 are not supplied.

(X92-1570-20) JAPAN MADE
(X92-1600-21) SINGAPORE MADE

(X25-4150-XX)



KSS-210A

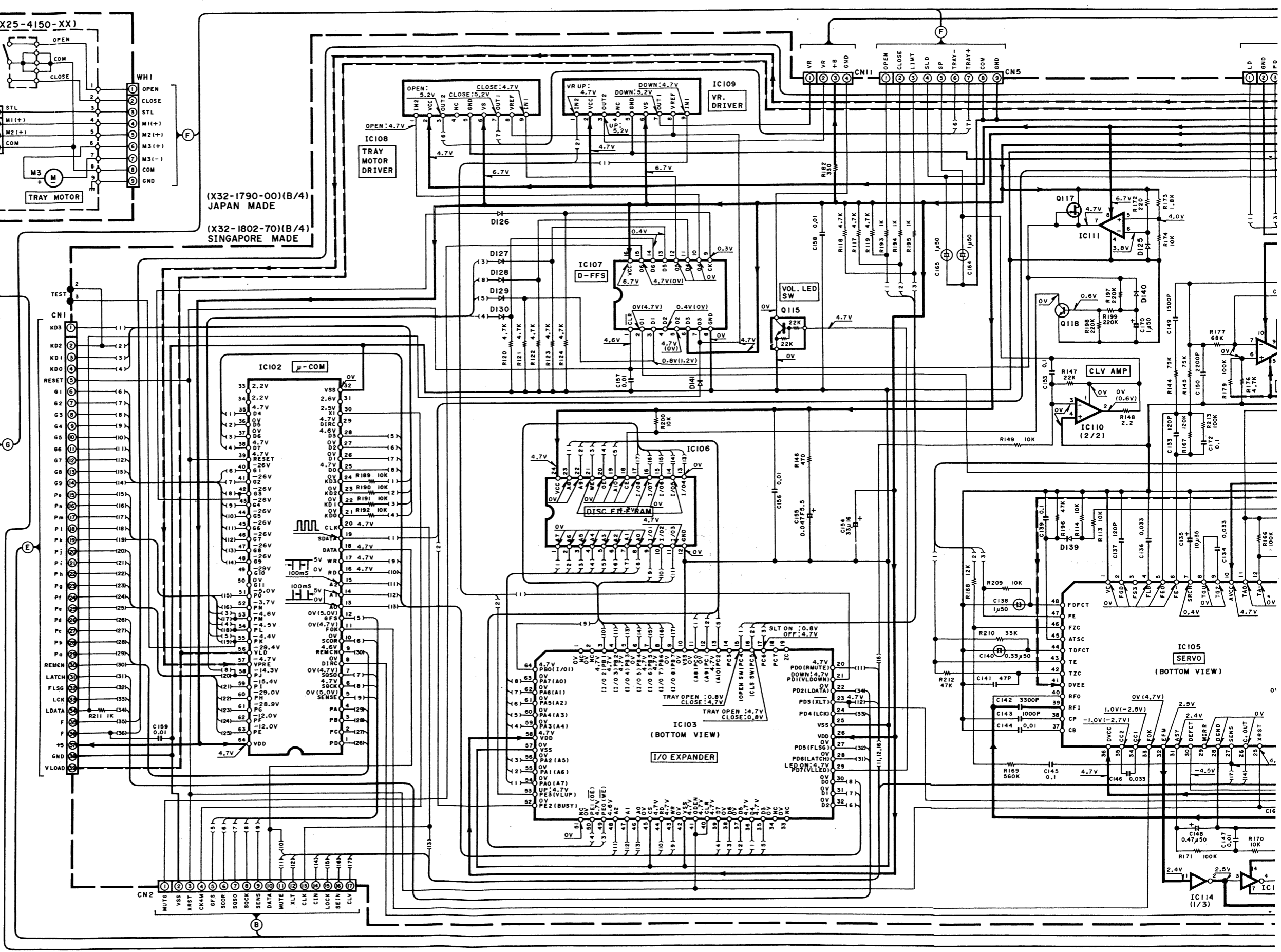


(X32-1790-00)(B/4) JAPAN MADE
(X32-1802-70)(B/4) SINGAPORE MADE

- IC101, 112 : NJM4558D
- IC102 : μ PD75216ACW-B71
- IC103 : CXD10950
- IC104 : CXA1471S
- IC105 : CXA13720
- IC106 : LC3518BSL-15
- IC107 : TC74HC174AP
- IC108, 109 : TA8409S
- IC110, 201 : TA8410AK or LA6510
- IC111 : BA10393N
- IC113 : M523BP
- IC114 : TC74HC04AP or MN74HC04

- D101, 126-130 : HSS104A or ISS133
- D102-105 : S5566B
- D106, 107, 113 : RD7.5JS(B) or HZS7.5S(B)
- D108, 109, 114-124, 131-141, 201, 202 : HSS104 or ISS133
- D110-112 : RD5.1ES(B2) or HZS5.1N(B2)
- D125 : RD3.9ES(B2) or HZS3.9N(B2)

PRODUCT P.	DESTINATION COUNTRY	ABB.	UNIT NAME
JAPAN MADE	JAPAN	J	X32-1790-00
	GENERAL MARKET	M	X92-1570-20
	PX	Y	X25-4170-00
SINGAPORE MADE	AUSTRALIA	X	X32-1790-71
	ENGLAND EUROPE	T E	X32-1802-70 X92-1600-21 X25-4452-70



2

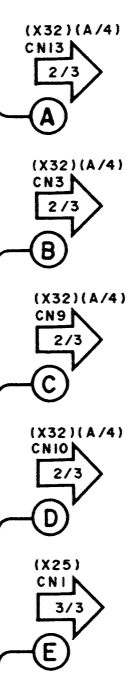
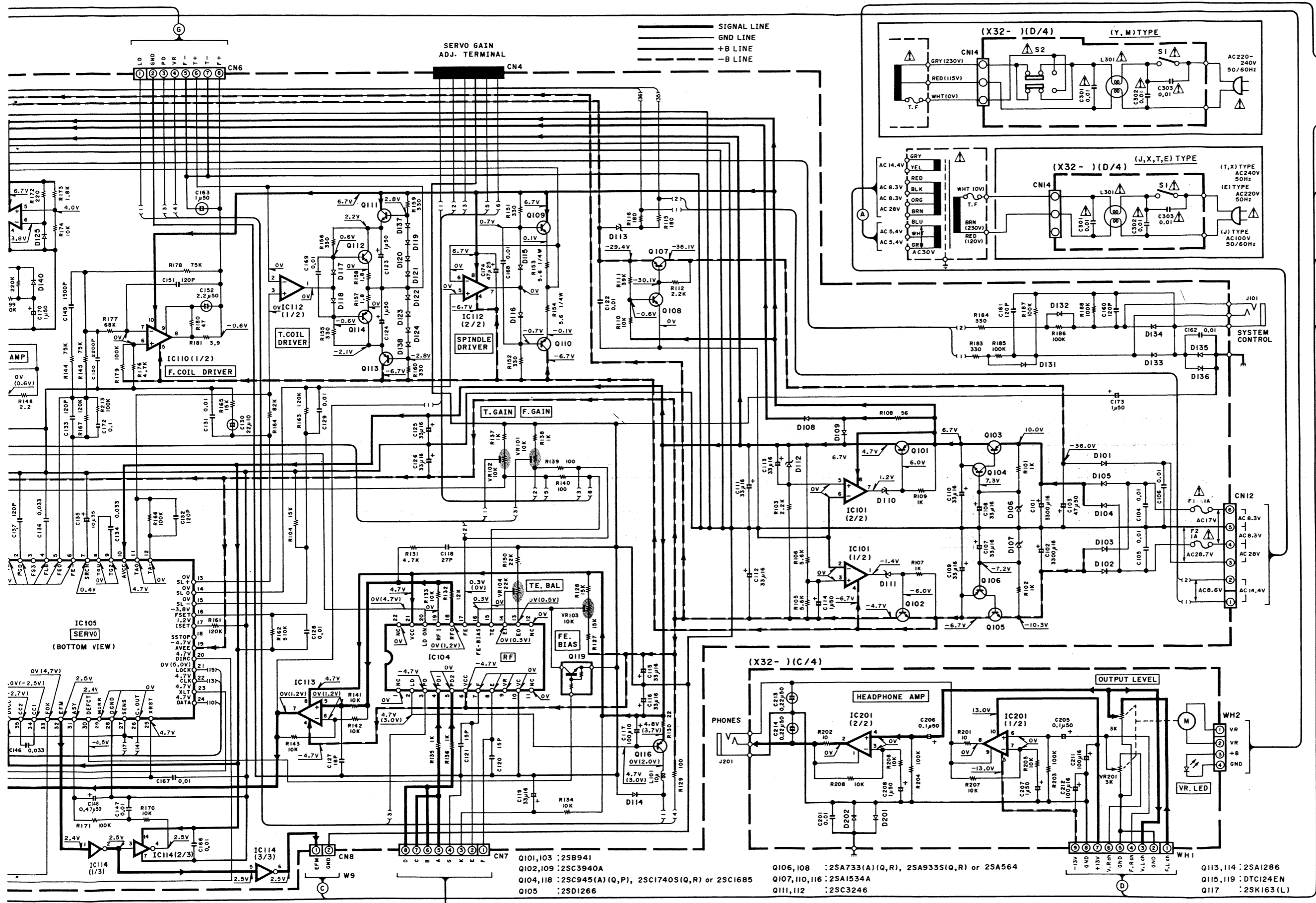
3

4

5

6

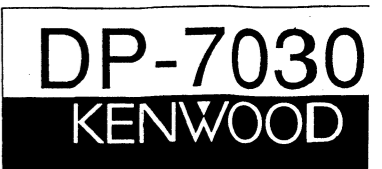
7



- | | | |
|---|---|---------------------|
| Q101,103 : 2S8941 | Q106,108 : 2SA733(A)(Q,R), 2SA933S(Q,R) or 2SA564 | Q113,114 : 2SA1286 |
| Q102,109 : 2SC3940A | Q107,110,116 : 2SA1534A | Q115,119 : DTC124EN |
| Q104,118 : 2SC945(A)(Q,P), 2SC1740S(Q,R) or 2SC1685 | Q111,112 : 2SC3246 | Q117 : 2SK163(L) |
| Q105 : 2SD1266 | | |

CAUTION : For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). Δ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

• DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.



POWER TRANSFORMER

(X32)(B/4) 1/3 A

(X32)(B/4) 1/3 B

(X32)(B/4) 1/3 C

(X32)(B/4) 1/3 D

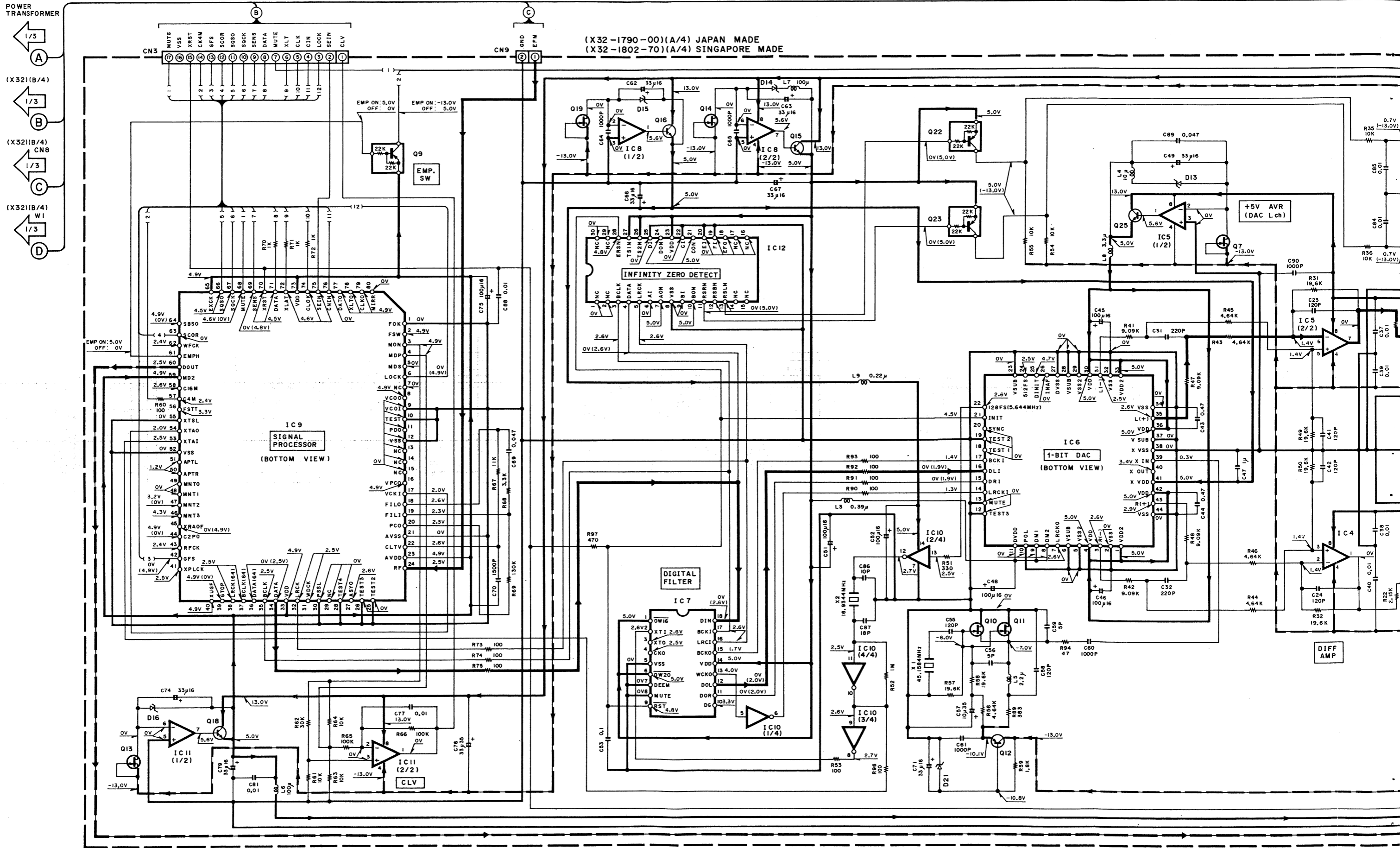
3

4

5

6

7



(X32-1790-00)(A/4) JAPAN MADE
(X32-1802-70)(A/4) SINGAPORE MADE

IC9
SIGNAL PROCESSOR
(BOTTOM VIEW)

DIGITAL FILTER
IC7

1-BIT DAC
IC6
(BOTTOM VIEW)

DIFF AMP
IC4

+5V AVR
(DAC Lch)

INFINITY ZERO DETECT
IC12

IC11 (1/2)

IC11 (2/2)

IC10 (1/4)

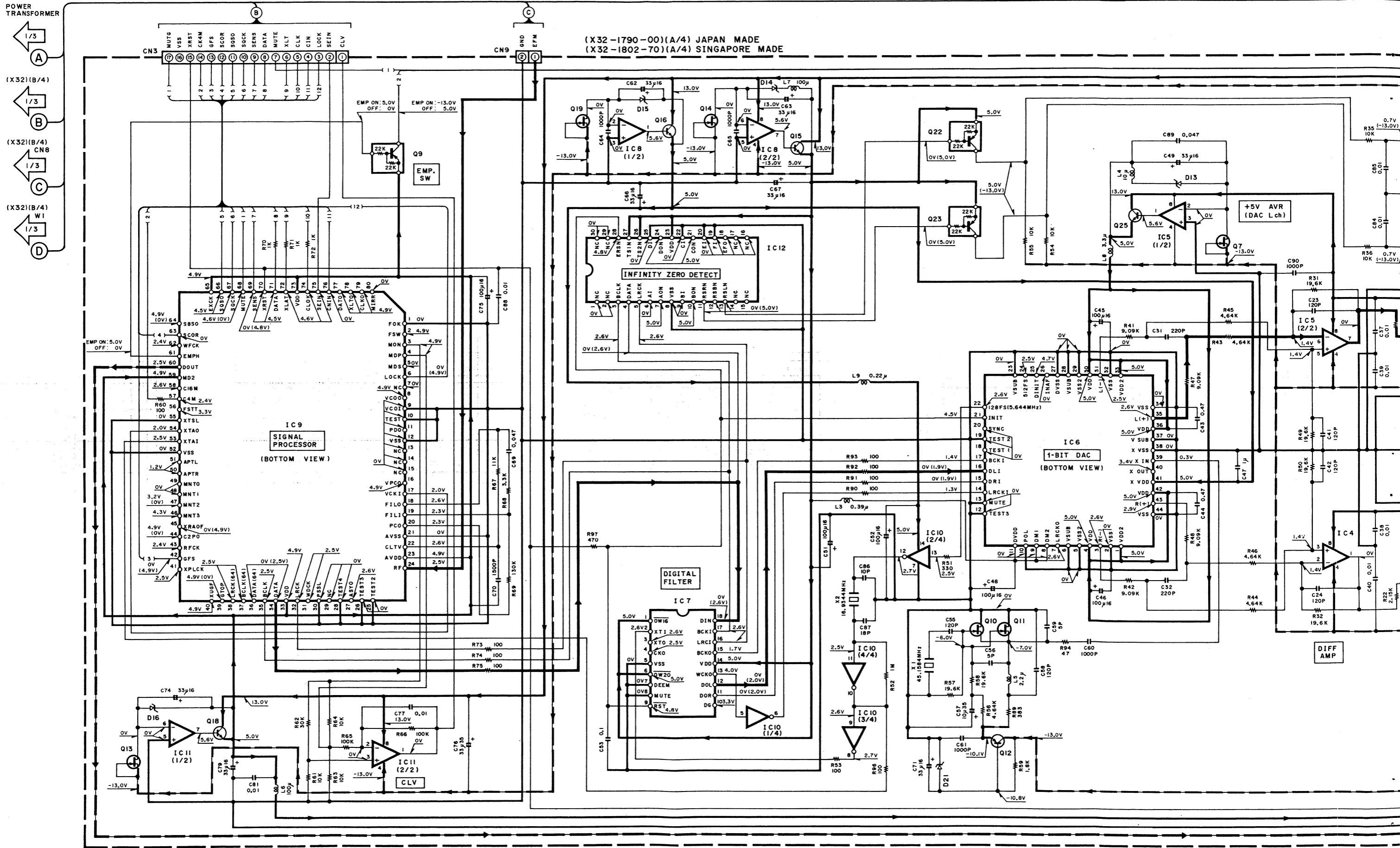
IC10 (2/4)

IC10 (3/4)

IC10 (4/4)

IC5 (1/2)

IC5 (2/2)



(X32-1790-00)(A/4) JAPAN MADE
(X32-1802-70)(A/4) SINGAPORE MADE

IC9
SIGNAL PROCESSOR
(BOTTOM VIEW)

DIGITAL FILTER
IC7

1-BIT DAC
IC6
(BOTTOM VIEW)

DIFF AMP
IC4

+5V AVR
(DAC Lch)

INFINITY ZERO DETECT
IC12

IC11 (1/2)

IC11 (2/2)

IC10 (1/4)

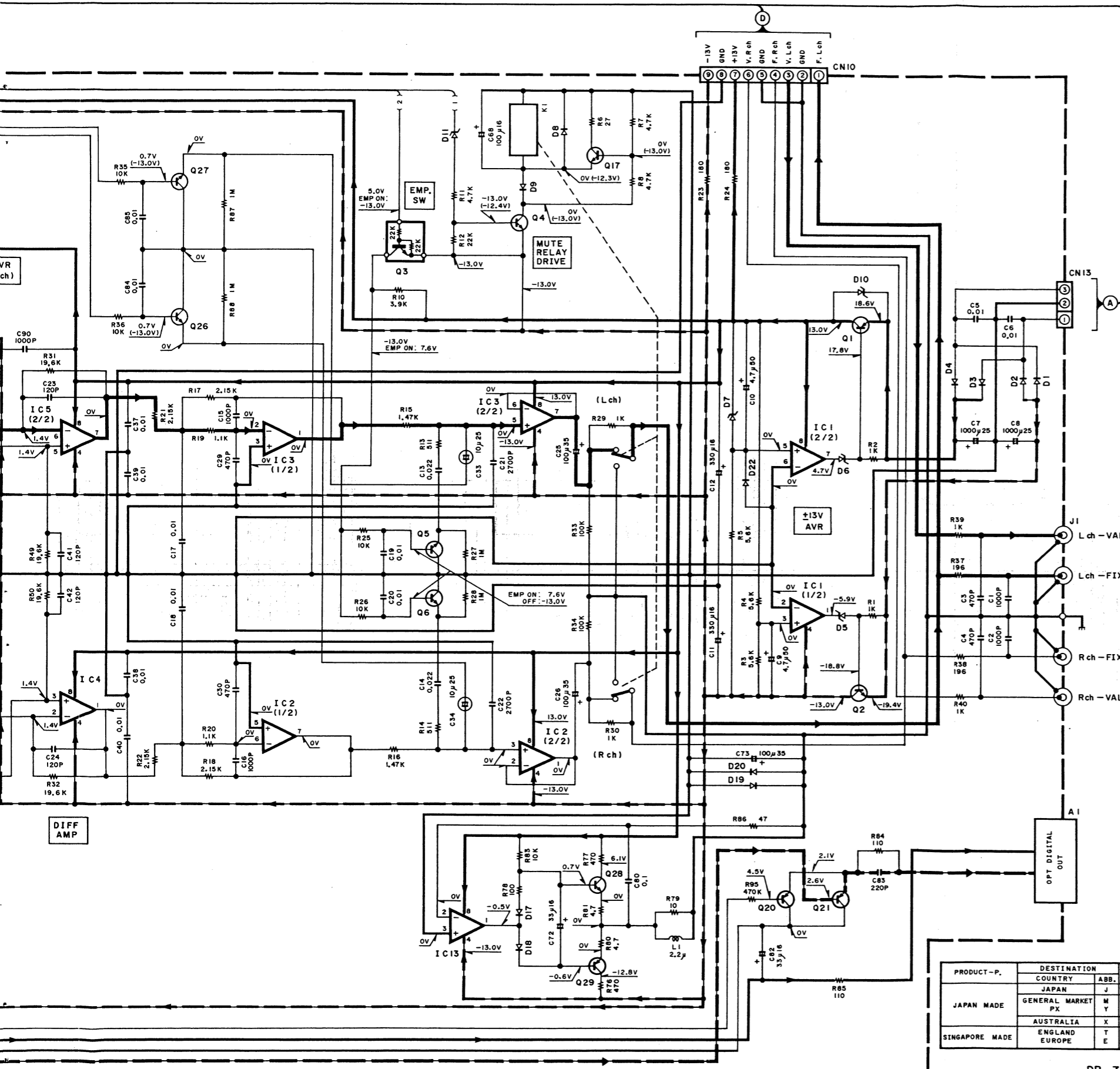
IC10 (2/4)

IC10 (3/4)

IC10 (4/4)

IC5 (1/2)

IC5 (2/2)



- IC 1, 8, 11 : NJM4558D
 IC 2~5, 13 : NJM4565D
 IC 6 : CXD25520
 IC 7 : SM5840CP
 IC 9 : CXD2500Q
 IC 10 : TC74HCU04AP or MN74HCU04
 IC 12 : SM5827CP
- Q 1 : 2SB941
 Q 2 : 2SD1266
 Q 3 : DTC124EN
 Q 4, 25, 28 : 2SC945 (A)(Q,P)
 or 2SC1740S(Q,R) or 2SC1685
 Q 5, 6, 26, 27 : 2SC2878 (B) or 2SD1302(S,T)
 Q 7, 13, 14, 19 : 2SK246 (Y,GR)
 Q 9, 22, 23 : DTA124EN
 Q 10, 11 : 2SK161 (GR)
 Q 12, 20, 21, 29 : 2SA733(A)(Q,P)
 or 2SA933S(Q,R) or 2SA564
 Q 15, 16, 18 : 2SC3940A
 Q 17 : 2SC3246
- D 1~4 : S5566B
 D 5~7, 10 : RD13ES (B2)
 or HZS13N (B2)
 D 8, 9, 17~20, 22 : ISS133
 or HSS104
 D 11 : RD15ES (B2)
 or HZS15N (B2)
 D 13~16 : RD5.1ES (B2)
 or HZS5.1N (B2)
 D 21 : RD11ES (B2)
 or HZS11N (B2)

- DTA124EN

 DTC124EN

 2SA1286
 2SA1534A
 2SA733(A)
 2SA564
 2SC1685
 2SC2878
 2SC3940A
 2SD1302
 2SC3246
 2SC945(A)

- 2SD1266

 2SA933S
 2SC1740S

- 2SB941

 NJM4558D
 NJM4565D

- MN74HCU04
 TC74HCU04AP

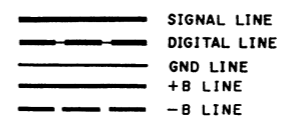
 TC74HC174AP

- TA8409S

 M5238P

- LA6510
 TA8410AK

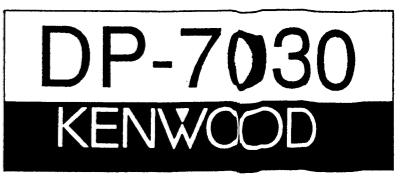
 2SK246



PRODUCT-P.	DESTINATION	UNIT NAME
JAPAN MADE	JAPAN	X32-1790-00
	GENERAL MARKET	X32-1790-21
SINGAPORE MADE	AUSTRALIA	X32-1790-71
	ENGLAND EUROPE	X32-1802-70

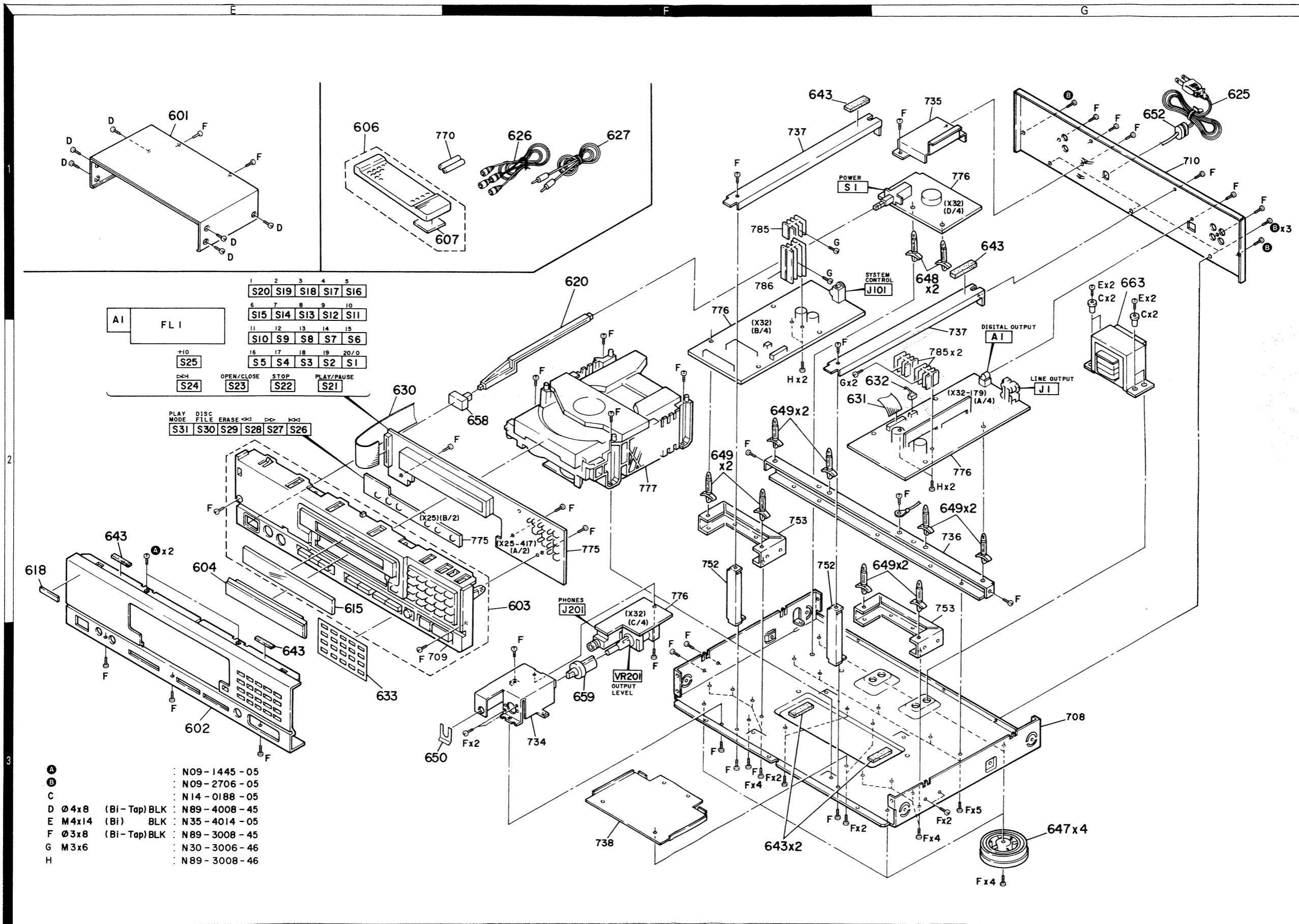
DP-7030(2/3)
 • DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

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DP-7030 DP-7030

EXPLODED VIEW (UNIT)



Parts with the exploded numbers larger than 700 are not supplied.

* New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnés dans le Parts No. ne sont pas fournis.
Teile ohne Parts No. werden nicht geliefert.

Table with columns: Ref. No., Address, New Parts, Parts No., Description, Destination, Remarks. Includes sub-sections for DP-7030 (JAPAN MADE) and DP-7030 (SINGAPORE MADE).

E: Scandinavia & Europe K: USA P: Canada W: Europe

V: PK (Far East, Hawaii) T: England M: Other Areas

Y: AAFES (Europe) X: Australia

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PARTS LIST

DP-7030

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Ref. No.	Address	New Parts	Parts No.	Description	Desti- nation	Re- marks
参照番号	位置	新	部品番号	部品名 / 規格	仕	備考
C148			CE04KW1H147M	ELECTRO 0.47UF 50WV		
C149			CF92FV1H152J	MF 1500PF J		
C150			CF92FV1H222J	MF 2200PF J		
C151			CF92FV1H121K	MF 120PF K		
C152			C90-1350-05	NP-ELEC 2.2UF 50WV		
C153			CF92FV1H104J	MF 0.10UF J		
C154			CE04KW1C330M	ELECTRO 33UF 16WV		
C155			C90-1826-05	NP-ELEC 0.047F 5.5WV		
C156-159			CF92FV1H103J	MF 0.010UF J		
C160,161			CF92FV1H121K	MF 120PF K		
C162			CF92FV1H103J	MF 0.010UF J		
C163-165			C90-1349-05	NP-ELEC 1UF 50WV		
C166-169			CF92FV1H103J	MF 0.010UF J		
C170			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C172			CF92FV1H104J	MF 0.10UF J		
C173			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C174			C90-1922-05	ELECTRO 47UF 25WV		
C201			CF92FV1H103J	MF 0.010UF J		
C205,206			CE04KW1H010M	ELECTRO 0.1UF 50WV		
C207,208			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C211,212			CE04KW1C101M	ELECTRO 100UF 16WV		
C213,214			C90-1456-05	NP-ELEC 0.22UF 50WV		
C301-303			C91-0971-05	FILM 0.01UF 250WV		
J1	1H		E63-0002-05	PHONE JACK(LINE OUTPUT)		
J101	1G		E11-0108-05	MINIATURE PHONE JACK(SYS/CON)		
J201	2F		E11-0199-05	PHONE JACK(PHONES)		
F1 ,2			F53-0006-05	FUSE		YMX
F1 ,2			F53-0018-05	FUSE		
-			J11-0098-05	WIRE CLAMPER		
L1			L40-2291-17	SMALL FIXED INDUCTOR		
L3			L40-3981-17	SMALL FIXED INDUCTOR		
L4			L40-1011-17	SMALL FIXED INDUCTOR		
L5			L40-2291-17	SMALL FIXED INDUCTOR		
L6 ,7			L40-1011-17	SMALL FIXED INDUCTOR		
L8			L40-3391-17	SMALL FIXED INDUCTOR		
L9			L40-2281-17	SMALL FIXED INDUCTOR		
L101			L40-1001-17	SMALL FIXED INDUCTOR		
L301			L79-0733-05	LINE FILTER		
X1			L77-1190-05	CRYSTAL RESONATOR (45.158MHz)		
X2			L77-1187-05	CRYSTAL RESONATOR (16.9344MHz)		
G			N30-3006-46	PAN HEAD MACHINE SCREW		
H			N89-3008-46	BINDING HEAD TAPTITE SCREW		
R13 ,14			RN14BK2C5110F	RN 511.0 F 1/6W		
R15 ,16			RN14BK2C1471F	RN 1.47K F 1/6W		
R17 ,18			RN14BK2C2151F	RN 2.15K F 1/6W		
R19 ,20			RN14BK2C1101F	RN 1.10K F 1/6W		
R21 ,22			RN14BK2C2151F	RN 2.15K F 1/6W		
R29 ,30			RN14BK2C1001F	RN 1.00K F 1/6W		
R31 ,32			RN14BK2C1962F	RN 19.6K F 1/6W		
R33 ,34			RN14BK2C1003F	RN 100K F 1/6W		
R37 ,38			RN14BK2C1960F	RN 196.0 F 1/6W		
R39 ,40			RN14BK2C1001F	RN 1.00K F 1/6W		

Ref. No.	Address	New Parts	Parts No.	Description	Desti- nation	Re- marks
参照番号	位置	新	部品番号	部品名 / 規格	仕	備考
R41 ,42			RN14BK2C9091F	RN 9.09K F 1/6W		
R43 -46			RN14BK2C4641F	RN 4.64K F 1/6W		
R47 ,48			RN14BK2C9091F	RN 9.09K F 1/6W		
R49 ,50			RN14BK2C1962F	RN 19.6K F 1/6W		
R56			RN14BK2C4641F	RN 4.64K F 1/6W		
R57 ,58			RN14BK2C1962F	RN 19.6K F 1/6W		
R89			RN14BK2C3830F	RN 383.0 F 1/6W		
R153,154			RD14GB2E5R6J	PL-PROOF RD 5.6 J 1/4W		
VR101-103			R12-3126-05	TRIM POT. 10K (P/B)		
VR104			R12-3128-05	TRIMMING POT.(22K)		
VR201	3F		R29-1005-05	POTENTIOMETER(3KX2)OUT/LEVEL		
K1			S51-2089-05	MAGNETIC RELAY		
S1			S40-1103-05	PUSH SWITCH (POWER TYPE)		YM
S2			S31-2131-05	SLIDE SWITCH (POWER TYPE)		
D1 -4			S5566B	DIODE		
D5 -7			HZS13N(B2)	ZENER DIODE		
D5 -7			RD13ES(B2)	ZENER DIODE		
D8 ,9			HSS104	DIODE		
D8 ,9			ISS133	DIODE		
D10			HZS13N(B2)	ZENER DIODE		
D10			RD13ES(B2)	ZENER DIODE		
D11			HZS15N(B2)	ZENER DIODE		
D11			RD15ES(B2)	ZENER DIODE		
D13 -16			HZS5.1N(B2)	ZENER DIODE		
D13 -16			RD5.1ES(B2)	ZENER DIODE		
D17 -20			HSS104	DIODE		
D17 -20			ISS133	DIODE		
D21			HZS11N(B2)	ZENER DIODE		
D21			RD11ES(B2)	ZENER DIODE		
D22			HSS104	DIODE		
D22			ISS133	DIODE		
D101			HSS104A	DIODE		
D101			ISS131	DIODE		
D102-105			S5566B	DIODE		
D106,107			HZS7.5S(B)	ZENER DIODE		
D106,107			RD7.5JS(B)	ZENER DIODE		
D108,109			HSS104	DIODE		
D108,109			ISS133	DIODE		
D110-112			HZS5.1N(B2)	ZENER DIODE		
D110-112			RD5.1ES(B2)	ZENER DIODE		
D113			HZS7.5S(B)	ZENER DIODE		
D113			RD7.5JS(B)	ZENER DIODE		
D114-124			HSS104	DIODE		
D114-124			ISS133	DIODE		
D125			HZS3.9N(B2)	ZENER DIODE		
D125			RD3.9ES(B2)	ZENER DIODE		
D126-130			ISS133	DIODE		
D126-130			HSS104A	DIODE		
D126-130			ISS131	DIODE		
D131-141			HSS104	DIODE		
D131-141			ISS133	DIODE		
D201,202			HSS104	DIODE		
D201,202			ISS133	DIODE		
D201,202			ISS133	DIODE		
IC1			NJM4558D	IC(OP AMP X2)		
IC2 -5			NJM4565D	IC(OP AMP X2)		

PARTS LIST

DP-7030

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 Y: PK(Far East, Hawaii) T: England M: Other Areas
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▲ indicates safety critical components.

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Table with columns: Ref. No., Address, New Parts, Parts No., Description, Destination, Remarks. Includes parts like CXD2552Q, SM5840CP, NJM4558D, etc.

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A: Indicates safety critical components.

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Y: PK/Far East (Hawaii) T: England M: Other Areas X: Australia
A: Indicates safety critical components.

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Table with columns: Ref. No., Address, New Parts, Parts No., Description, Destination, Remarks. Includes parts like E31-7891-05, E31-7892-05, F19-1027-04, etc.

E: Scandinavia & Europe K: USA P: Canada W: Europe S: SINGAPORE MADE J: JAPAN MADE
Y: PK/Far East (Hawaii) T: England M: Other Areas X: Australia
A: Indicates safety critical components.

DP-7030

PARTS LIST

PARTS LIST

DP-7030

DP-7030

SPECIFICATIONS

[Format]

Type Compact disc player
Read system Non-contact optical pick-up
Rotational speed About 200 to 500 rpm

[Audio]

Frequency response 2Hz ~ 20kHz \pm 0.5dB
Signal to noise ratio More than 113dB
Total harmonic distortion 0.0013% at 1kHz
Channel separation More than 110dB at 1kHz
Wow & Flutter Below measurable limit

Output

LINE (Fixed) 2.0V
(Variable) 0 ~ 2.0V
DIGITAL (OPTICAL) -15dBm ~ -21dBm
Headphone jack 20mW (8 Ω)

[General]

Power consumption 25W
Dimensions W : 440mm
H : 132mm
D : 381mm
Weight 10.1kg

Note:

KENWOOD follows a policy of continuous advancements in development. For this reason specifications may be changed without notice.

Note :

Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the Canada (P) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

KENWOOD CORPORATION

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P.O. BOX 1075, 959 Gana Court, Mississauga, Ontario, Canada L4T 4C2

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KENWOOD HOUSE, Dwight Road, Watford, Herts, WD1 8EB United Kingdom

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KENWOOD ELECTRONICS DEUTSCHLAND GMBH

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TRIO-KENWOOD FRANCE S.A.

13 Boulevard Ney, 75018 Paris, France

KENWOOD LINEAR S.p.A.

20125, MILANO-VIA ARBE, 50, ITALY

KENWOOD ELECTRONICS AUSTRALIA PTY. LTD. (INCORPORATED IN N.S.W.)

P.O. BOX 504, 8 FIGTREE DRIVE, AUSTRALIA CENTRE, HOMEBUSH, N.S.W. 2140, AUSTRALIA

KENWOOD & LEE ELECTRONICS, LTD.

Wang Kee Building, 4th Floor, 34-37, Connaught Road, Central, Hong Kong