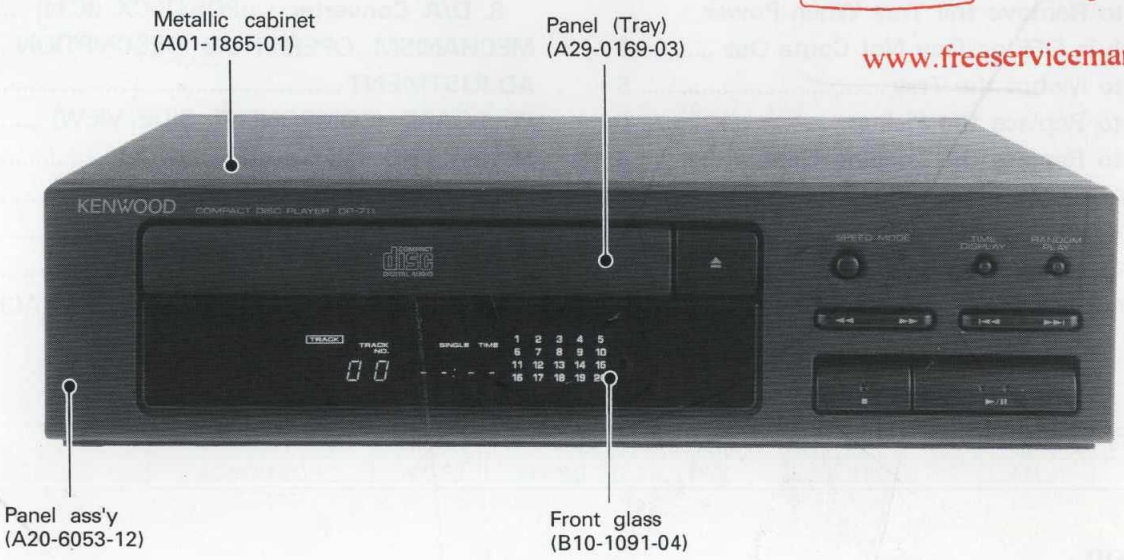
COMPACT DISC PLAYER

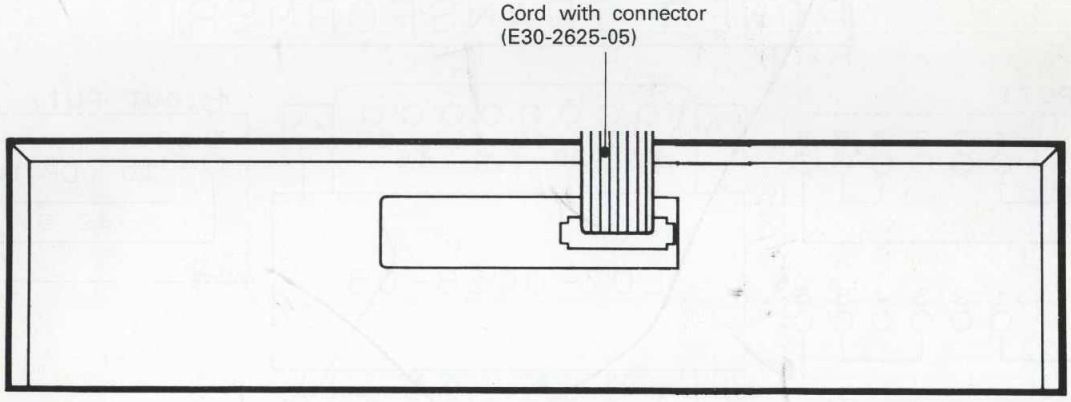
DP-711

SERVICE MANUAL

KENWOOD

B51-4167-00 (O) 3048





CAUTION

When doing repair of DP-711, be sure to have the customer bring the A-711, or supply to 9V AC to terminal Nos 12 and 13 (CN8) on the X32-1700 PC board ass'y.
If not get 9V AC, please order the A-848's power transformer (parts No. L-07-0038-05 / 120V / 220V / 240V).
Don't use the "RHEOSTAT".
Pattern of flexible cable (exploded view No. 31) is weak. Handle with care.

In complicance with Federal Regulations, following are reproductions of labels on, or inside the product relating to laser product safety.

KENWOOD-Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040. 10, Chapter 1, Subchapter J.

DANGER : Laser radiation when open and interlock defeated. AVOID DIRECT EXPOSURE TO BEAM.

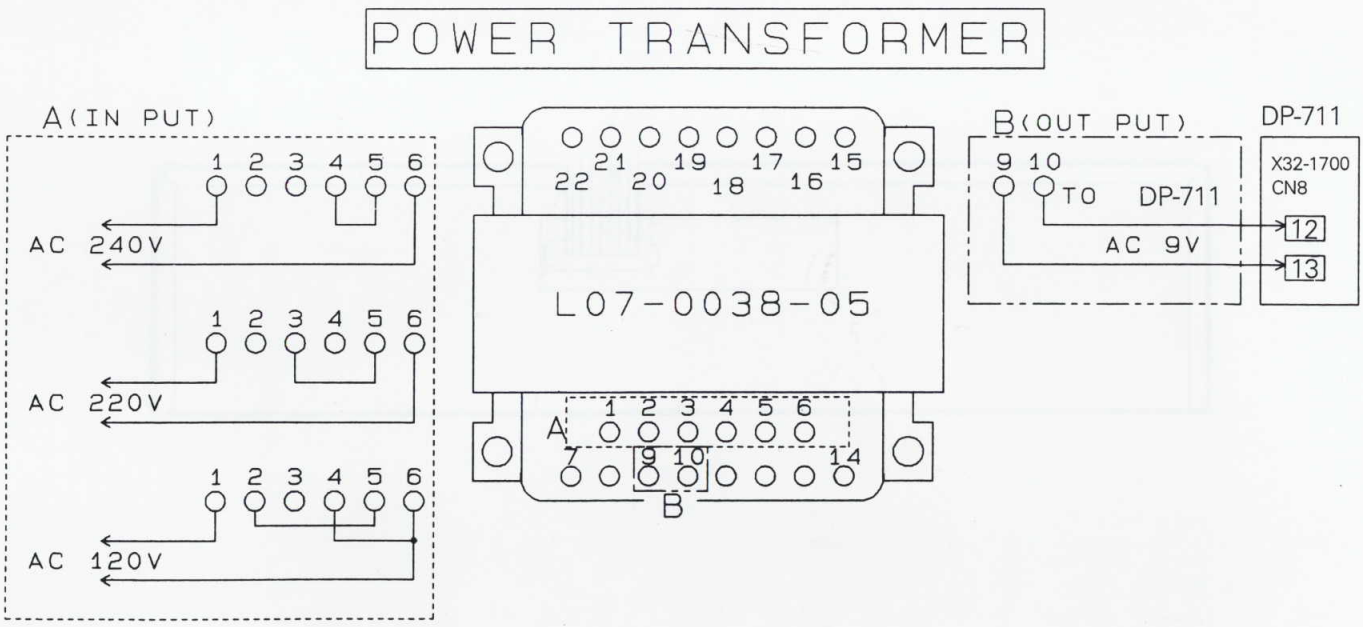
DP-711

CONTENTS / CONNECTION

Contents

System mane	Receiver	Graphic equalizer	Cassette deck	CD player	Speaker	Outer packing case
UD7	A-711	GE-711	X-711	DP-711	LS-711	H03-1576-04

Connection



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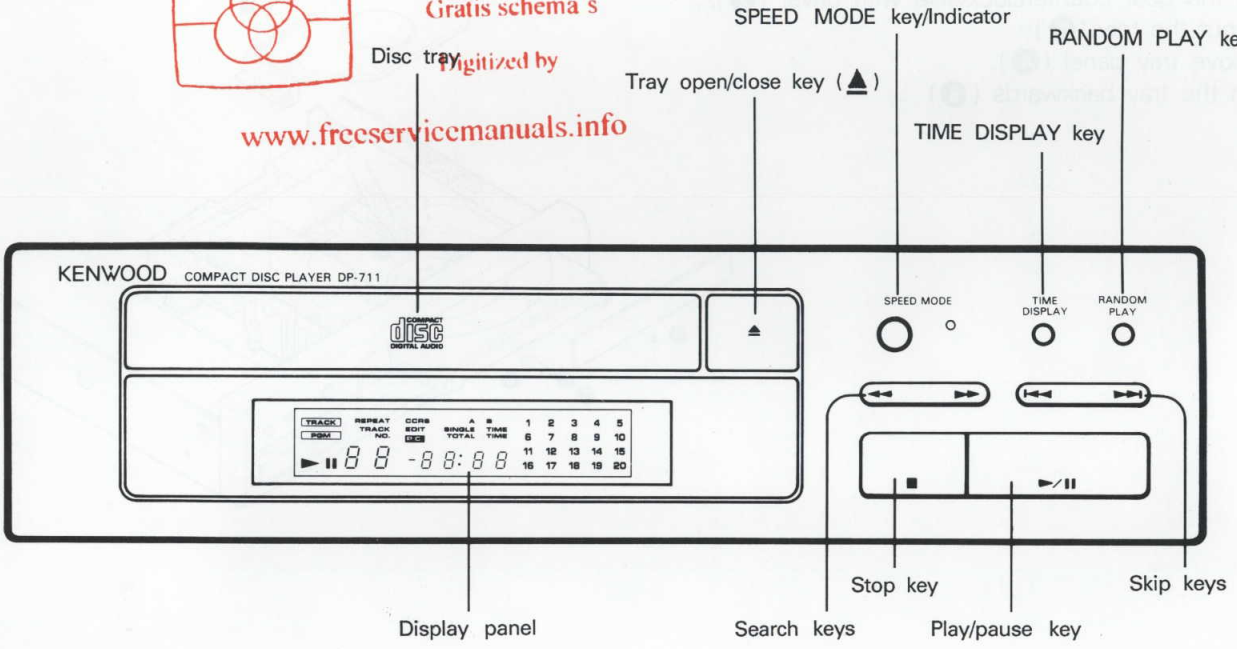
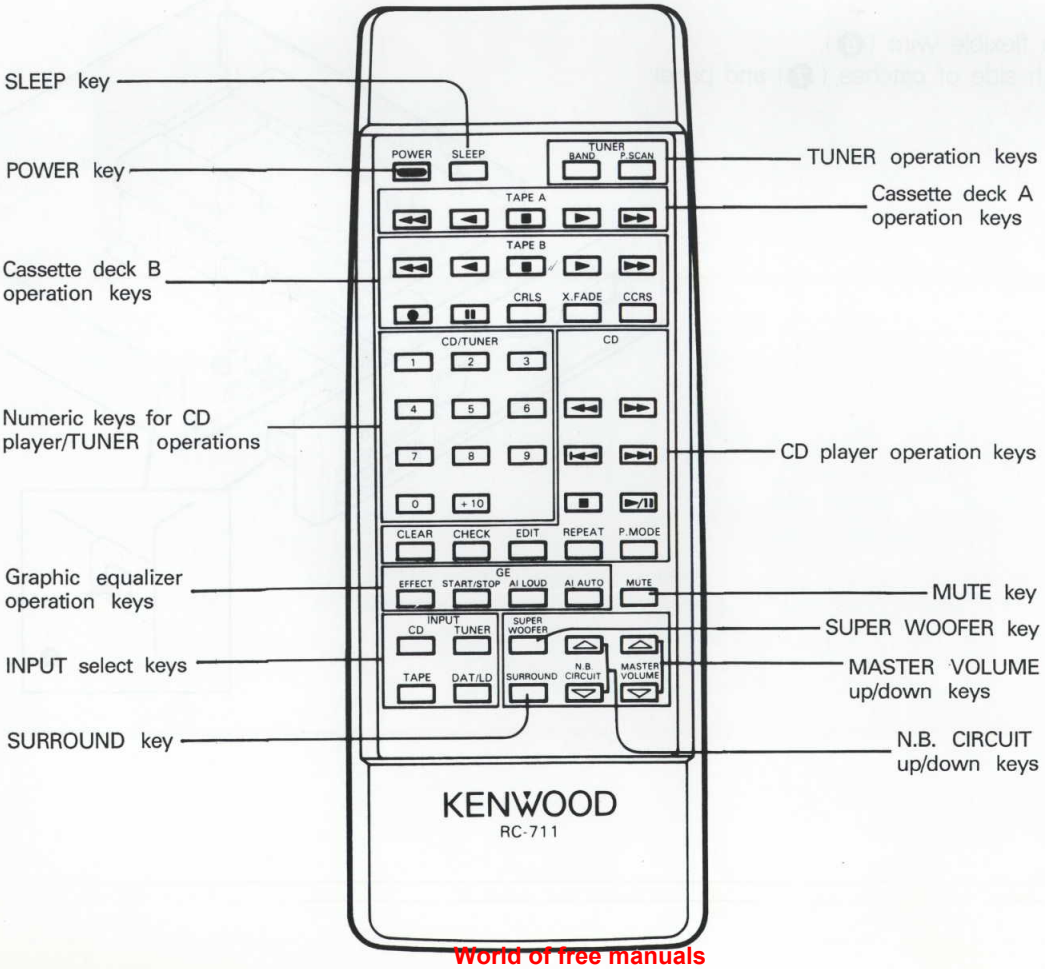
CONTROLS

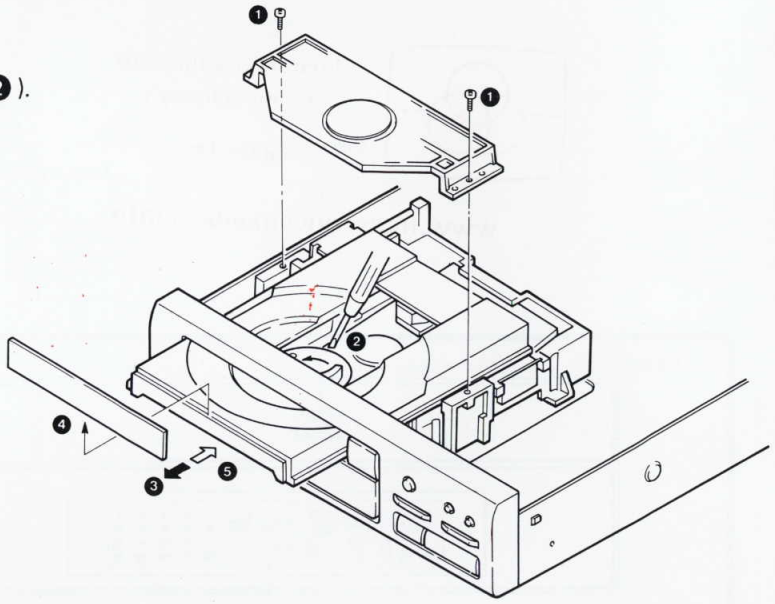




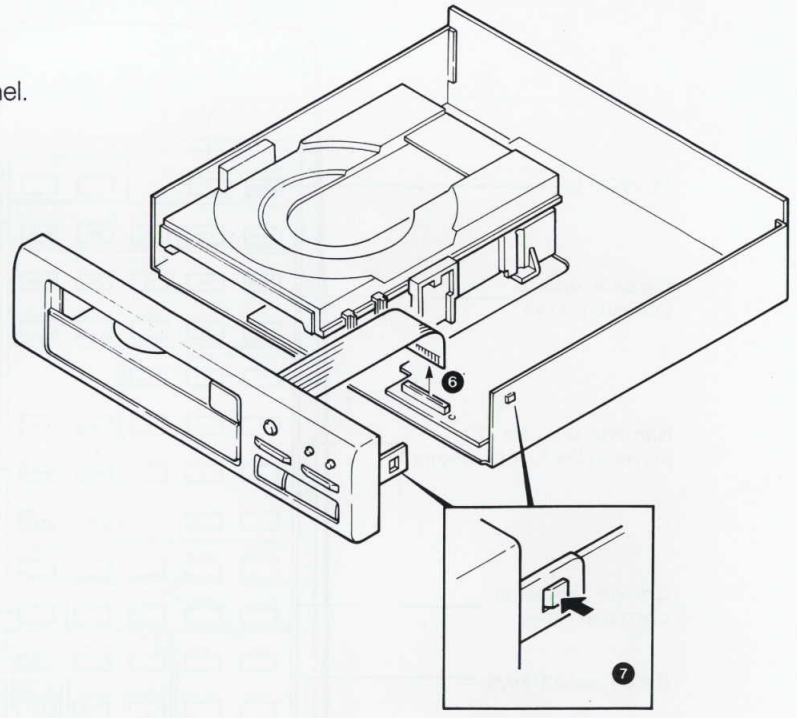
DISASSEMBLY FOR REPAIR

1. How to Disassembly

1. Remove the screws (❶), and clamper ass'y.
2. Turn the gear counterclockwise with driver (❷).
3. Pull out the tray (❸).
4. Remove tray panel (❹).
5. Push the tray backwards (❺).



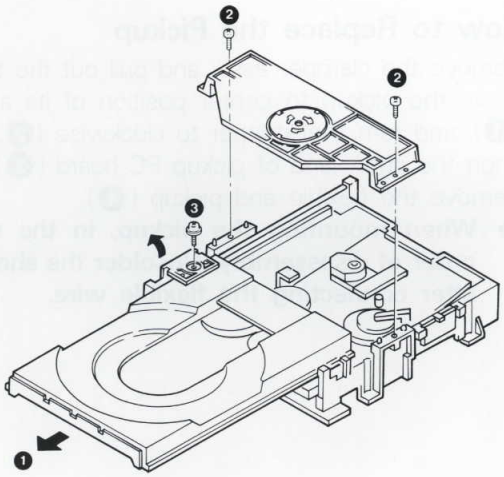
6. Remove the flexible wire (❻).
7. Remove both side of catches (❼) and panel.



DISASSEMBLY FOR REPAIR

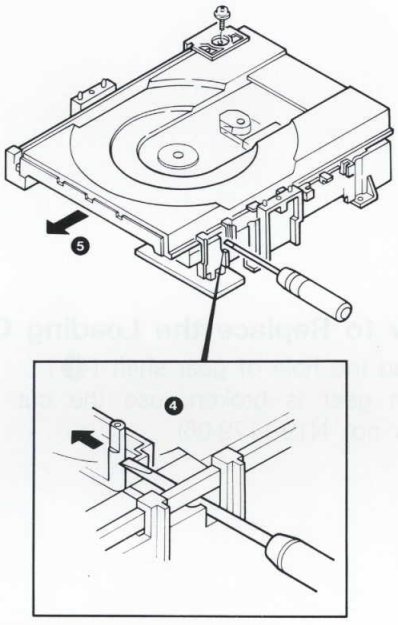
2. How to Remove Tray

1. Turn the power switch to OFF when the tray is open condition (❶).
2. Remove the screws (❷) and clamper ass'y.
3. Remove the screw (❸) and guide. And then remove the tray.



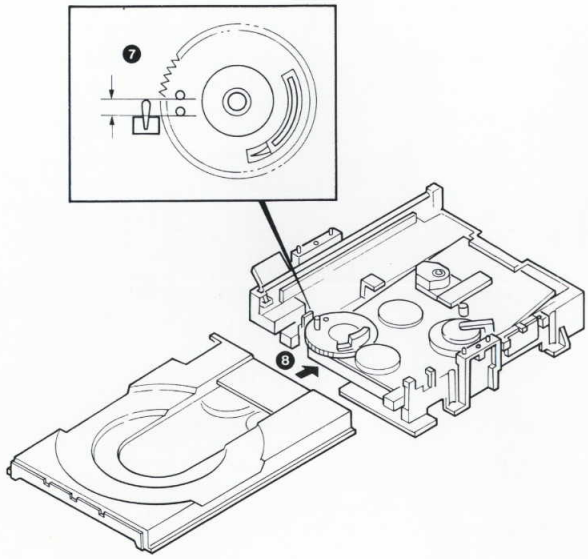
3. How to Remove the Tray When Power Switch is OFF or Tray Not Come Out

1. Insert the driver to the right-side hole of mechanism ass'y (❹).
2. Tray can be pulled out (❺).



4. How to Mount the Tray

1. Meet the mark on the gear with that of mechanism chassis (❼).
2. Insert the tray to both-side guide on chassis (❽).
3. Mount the guide on the chassis with screw (❸).

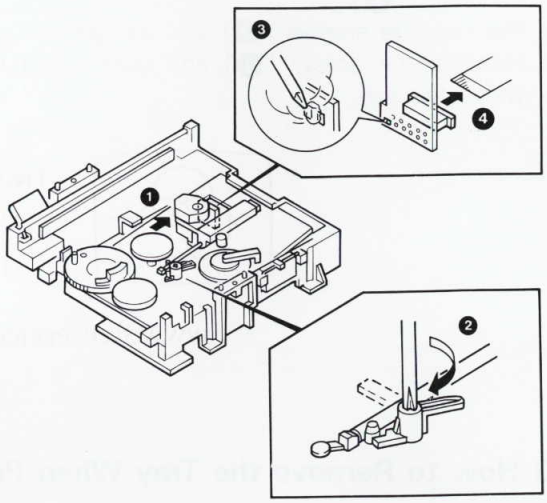


DISASSEMBLY FOR REPAIR

5. How to Replace the Pickup

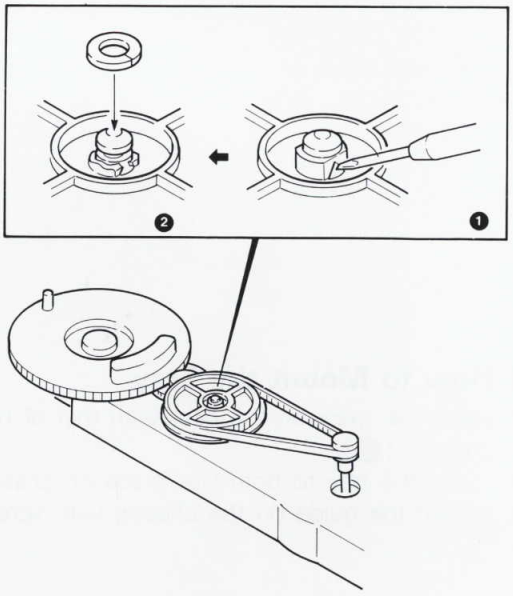
1. Remove the clamper ass'y and pull out the tray.
2. Move the pickup to center position of its all travel (❶), and turn the stopper to clockwise (❷).
3. Short the short land of pickup PC board (❸).
4. Remove the flexible and pickup (❹).

Note : When mounting the pickup, in the reverse order of disassembly. Unsolder the short land after connecting the flexible wire.

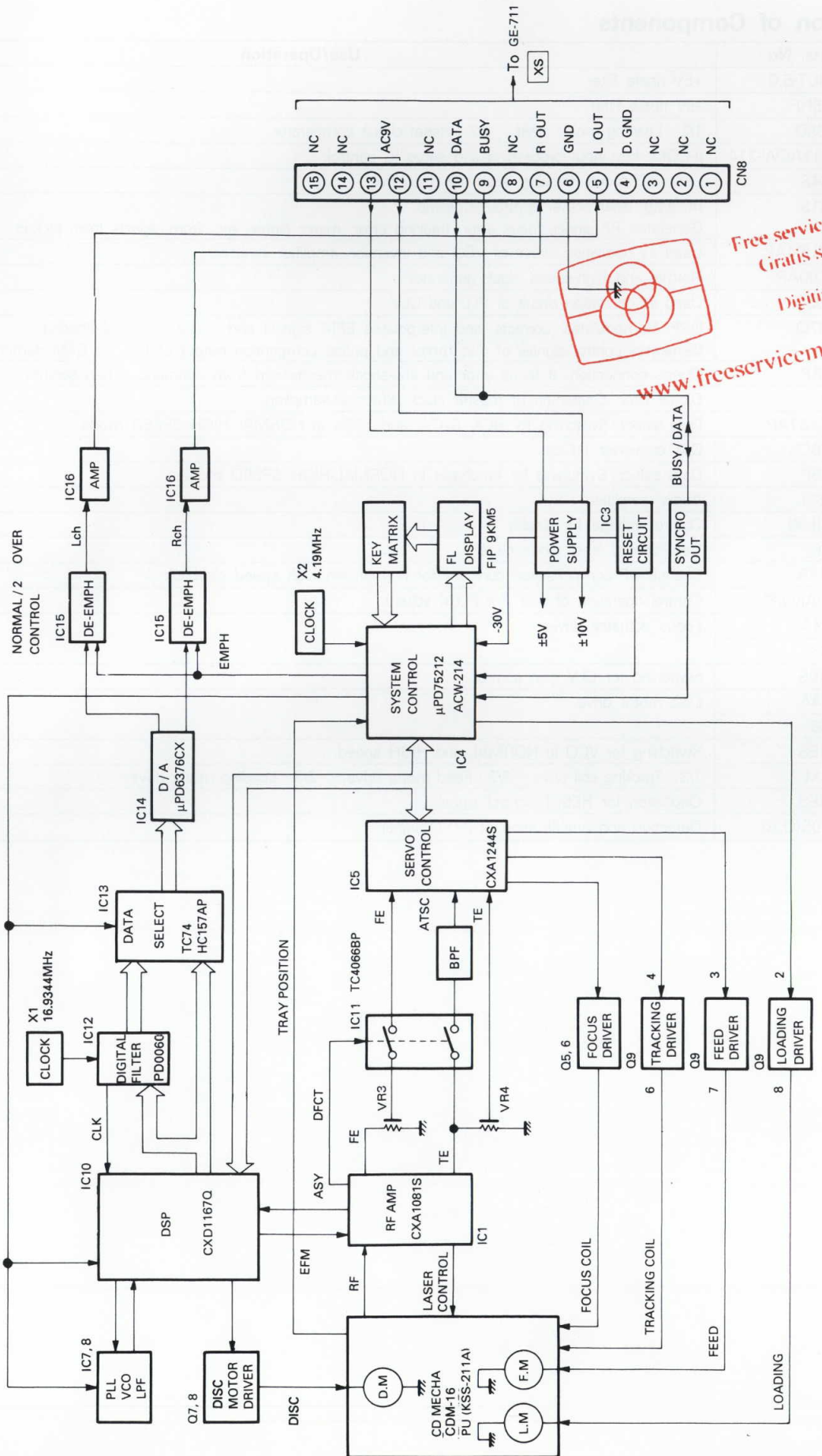


6. How to Replace the Loading Gear

1. Spread the hole of gear shaft (❶).
2. When gear is broken, use the cut washer (❷) (parts no. N19-1179-05)



BLOCK DIAGRAM



CIRCUIT DESCRIPTION

1. Description of Components

Ref. No	Parts. No	Use/Operation
IC1	LM2940CT-5.0	+5V ripple filter.
IC2	µPC7905HF	–5V ripple filter.
IC3	NJM4565D	1/2 : Loading motor drive. 2/2 : Reset circuit comparator.
IC4	µPD75212ACW-214	µ-COM, key input processing and servo IC control.
IC5	CXA1244S	Servo IC, focus, tracking, feed servo control.
IC6	CXA1081S	RF amp, laser power control of pickup. Generates RF signal, focus error, tracking error, mirror signal, etc. from signals from pickup.
IC7	TC74HCU04AP	Used as oscillation circuit of VCO and inversion amplifier inverter.
IC8	TC74HC00AP	Normal and high-speed clock generator.
IC9	NJM4565D	Used as oscillation circuit of PLL and CLV.
IC10	CXD1167Q	DSP. Demodulates, corrects, and interpolates EFM signals and performs digital filtering. Generates control signals of disc motor and phase comparison output of PLL for EFM demodulation.
IC11	TC4066BP	Opens connection of focus error and anti-shock mechanism from operating, when scratch is made.
IC12	PD0060	Digital filter. Oscillation of master clock. 8fs over-sampling.
IC13	TC74HC157AP	Data select. Switching for BCK, DATA, and LRCK in NORMAL-HIGH SPEED mode.
IC14	µPD6376CX	D/A converter (16-bit).
IC15	TC4052BP	Data select. Switching for emphasis in NORMAL-HIGH SPEED mode.
IC16	NJM4565L	Audio amplifier.
Q1	2SA954(L,K)	Control voltage for display.
Q2	2SA1426	Detection of laser diode current.
Q3	DTC124ES	Change RF compensation constant for normal and high speed playback.
Q4	2SA733(A)(Q,P)	Control operation of ASY (for PLCK adjust).
Q5	2SA1534A	Focus actuator driver.
Q12	2SD1266	
Q6	DTC124ES	Switching for CLV gain control.
Q7	2SA1534A	Disc motor drive.
Q13	2SD1266	
Q8	DTA124ES	Switching for VCO in NORMAL and HIGH speed.
Q9	STA341M	1/3 : Tracking coil drive. 2/3 : Feed motor drive. 3/3 : Loading motor drive.
Q10	DTC124ES	Oscillation for RESET control signal.
Q11	2SC1740S(Q,R)	Detection and amplification of ATSC signal.

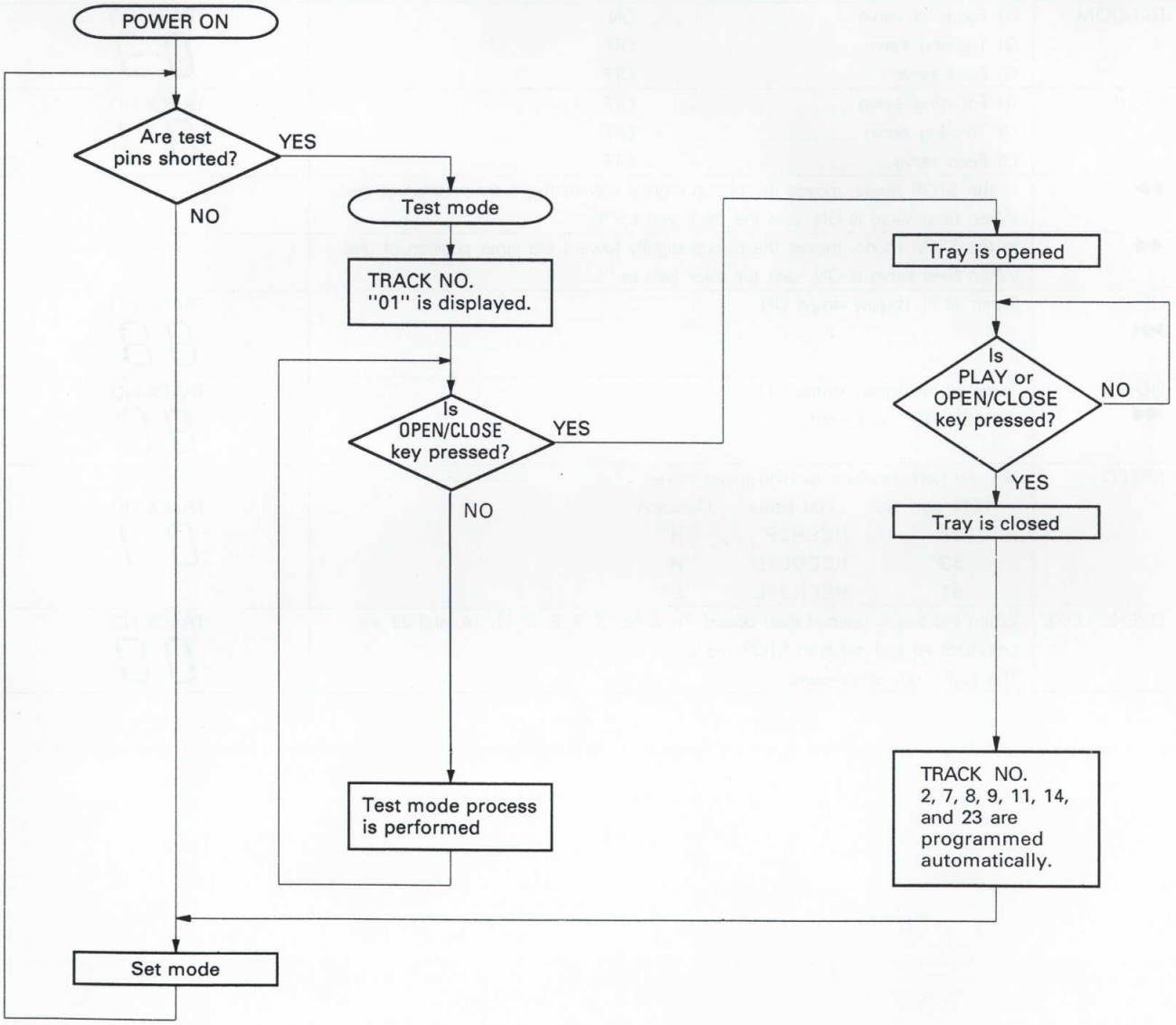
CIRCUIT DESCRIPTION

2. Test Mode

2-1. Setting the test mode

This microprocessor built in this unit can be put to TEST MODE by just short-circuiting the test pins (#7 and 8).

The TEST MODE can be also initiated with short-circuiting the test pins when tray is open. If unit is in test mode, TRACK NO. displays "05".



CIRCUIT DESCRIPTION

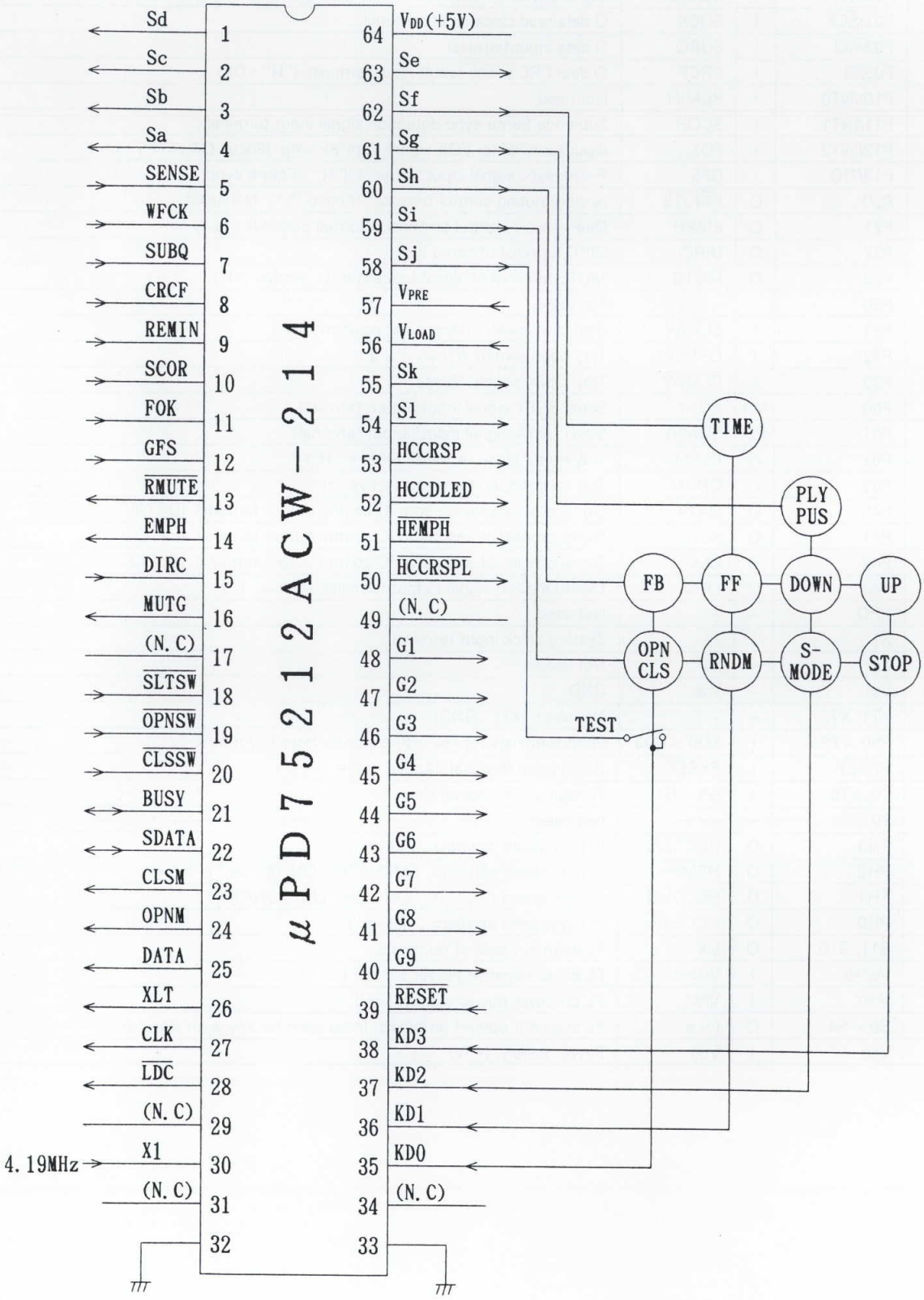
2-2. Key and functions valid in test mode

No.	Input key	Function	Track No. display
1	PLAY	(1) Focusing servo ..... ON (2) Tracking servo ..... ON (3) Feed servo ..... ON	TRACK NO. 05 ↓ Display for a few seconds after completion (1), (2) and (3). ↓ Disc Track No. is displayed.
2	RANDOM	(1) Focusing servo ..... ON (2) Tracking servo ..... OFF (3) Feed servo ..... OFF	TRACK NO. 03
3	STOP	(1) Focusing servo ..... OFF (2) Tracking servo ..... OFF (3) Feed servo ..... OFF	TRACK NO. 01
4	▶▶	In the STOP mode, moves the pickup slightly toward the outer position of disc. When feed servo is ON, sets the track gain to "H".	–
5	◀◀	In the STOP mode, moves the pickup slightly toward the inner position of disc. When feed servo is ON, sets the track gain to "L".	–
6	UP ▶▶|	Turns all FL display lamps ON.	TRACK NO. 88
7	DOWN |◀◀	Turns all FL display lamps OFF. "TRACK NO." is lighted.	TRACK NO. 88
8	SPEED	Set the port condition to High-speed mode. IC14 port No. Port name Condition 54 HCCRSP "H" 53 HCCDLED "H" 51 HCCRSPL "L"	TRACK NO. 01
9	OPEN/CLOSE	When the tray is opened then closed. Track No. 2, 7, 8, 9, 11, 14, and 23 are programmed and set is in STOP mode. The test mode is canceled.	TRACK NO. 00

CIRCUIT DESCRIPTION

3. Microprocessor : μPD75212ACW-214 (IC4)

3-1. Terminal connection diagram



CIRCUIT DESCRIPTION

3-2. EXplanation of terminals

Terminal No.	Terminal Name	I/O	Function Name	Function
1 ~ 4	S3 ~ S0	O	d~a	FL segment control terminals (also used for key scan signals).
5	P00/INT4	I	SENSE	Signal detection terminal for SENSE signal from signal processor and servo ICs.
6	P01/$\overline{SCK}$	I	SQCK	Q data read clock input terminal.
7	P02/SO	I	SUBQ	Q data input terminal.
8	P03/SI	I	CRCF	Q data CRC check result input terminal. ("H" : OK)
9	P10/INT0	I	REMIN	Not used.
10	P11/INT1	I	SCOR	Sub-code frame sync detection signal input terminal.
11	P12/INT2	I	FOK	Input terminal for FOK signal from RF amp. (Focus OK : "H")
12	P13/TIO	I	GFS	Frame sync signal input terminal. ("H" : Frame sync)
13	P20	O	$\overline{RMUTE}$	Analog muting control terminal. (Active "L") Not used.
14	P21	O	EMPH	Deemphasis control terminal. (Normal playback : "L")
15	P22	O	DIRC	DIRC terminal of servo IC.
16	P23	O	MUTG	MUTE terminal of signal processor IC. (Active "H")
17	P30	–	–	Not used.
18	P31	I	$\overline{SLTSW}$	Sled limit switch. (Innermost position : "L")
19	P32	I	$\overline{OPNSW}$	Tray open switch. (Open : "L")
20	P33	I	$\overline{CLSSW}$	Tray close switch. (Close : "L")
21	P60	I/O	BUSY	Serial BUSY signal input/output terminal.
22	P61	I/O	SDATA	Serial DATA signal input/output terminal.
23	P62	O	CLSM	Tray motor close terminal. (Active "H")
24	P63	O	OPNM	Tray motor open terminal. (Active "H")
25	P40	O	DATA	Signal processor and servo IC control output terminal. (DATA)
26	P41	O	XLT	Signal processor and servo IC control output terminal. (LATCH)
27	P42	O	CLK	Signal processor and servo IC control output terminal. (CLOCK)
28	P43	O	LDC	Laser ON/OFF signal output terminal. (Active "L")
29	PPO	–	–	Not used.
30	X1	I	X1	System clock input terminal.
31	X2	–	X2	Not used.
32	Vss	–	Vss	GND.
33, 34	XT1, XT2	–	–	Not used. (XT1 : GND)
35 ~ 38	P50 ~ P53	I	KD0 ~ KD3	Input terminals for key return signals from key matrix.
39	RESET	I	$\overline{RESET}$	Reset input terminal. (Active "L")
40 ~ 48	T0 ~ T8	I	G9 ~ G1	FL digit control terminals.
49	T9	–	–	Not used.
50	PH3	O	$\overline{HCCRSPL}$	In high-speed playback : Active "L"
51	PH2	O	$\overline{HEMPH}$	In high-speed playback, EMPHASIS : ON. (Active "L")
52	PH1	O	HCCDLED	In high-speed playback, EDIT-CCRS LED : ON/OFF.
53	PH0	O	HCCRSP	In high-speed playback : Active "H".
54, 55	S11, S10	O	l, k	FL segment control terminals.
56	VLOAD	I	VLOAD	FL driver negative power supply. (–30V)
57	VPRE	I	VPRE	FL predriver power supply. (–5V)
58 ~ 63	S9 ~ S4	O	j ~ e	FL segment control terminals. (Also used for key-scan signals)
64	VDD	I	VDD	Power supply. (+5V)

CIRCUIT DESCRIPTION

4. RF amplifier : CXA1081S (IC6)

General

The CXA1081S is an IC developed for use in Compact Disc players. It incorporates a 3-spot optical pickup RF output amplifier, a focusing error amplifier, a tracking error amplifier, and other signal processing circuitry, such as focus OK, mirror, detect, and EFM comparator circuits, as well as a laser diode APC (Automatic Power Control) circuit.

Features

- Operates on a signal +5V power supply, as well as on a ±5V dual-voltage power supply.
- Low power consumption (100mW with ±5V, 50mW with +5V).
- An APC circuit which accepts either a P-sub or N-sub laser diode.
- A minimum of external parts required.
- A disc defect detector circuit for improved playability.

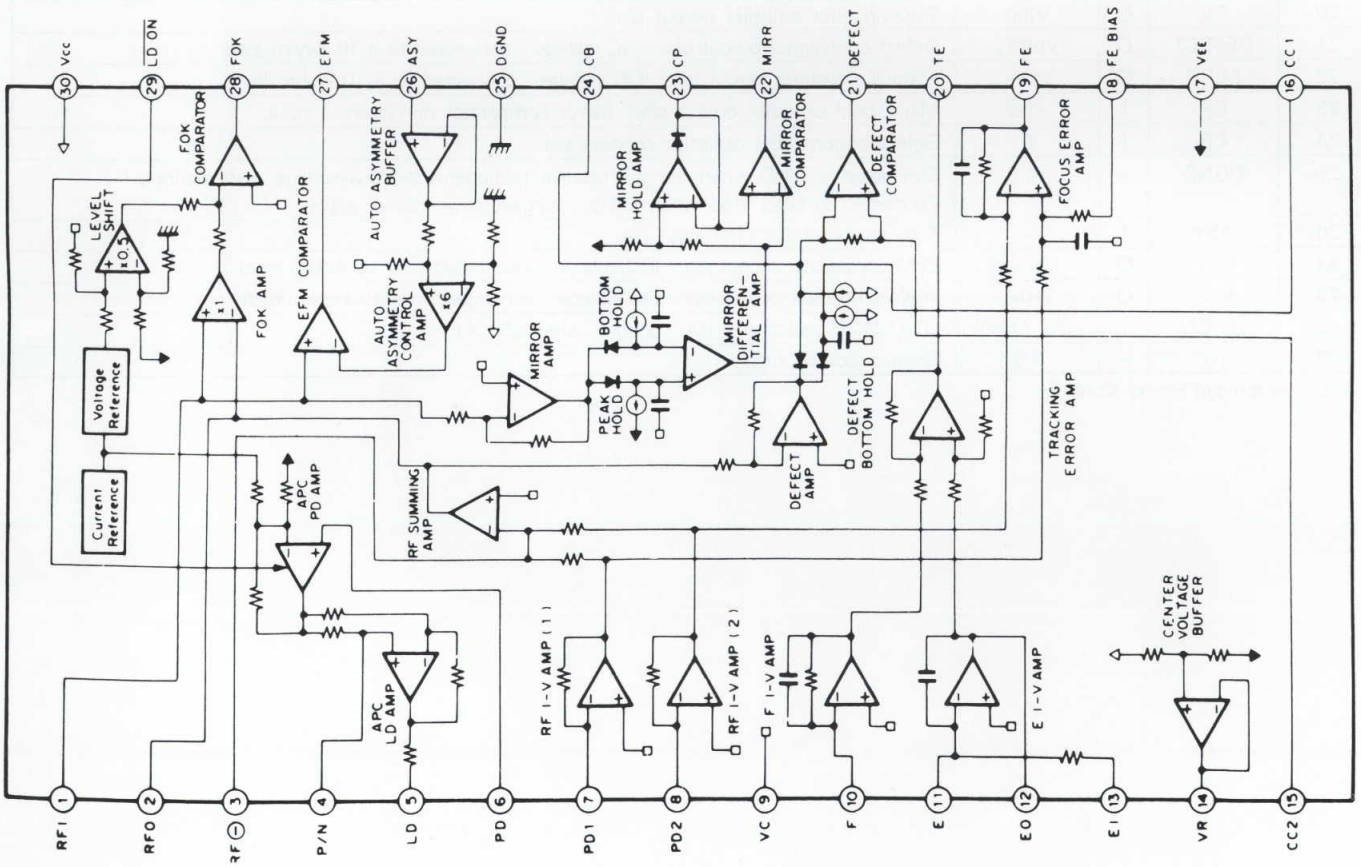
Structure

Bipolar silicon monolithic IC.

Functions

- RF amplifier
- Focus OK detector circuit
- Mirror detector circuit
- Tracking error amplifier
- Defect detector circuit
- APC circuit
- EFM comparator
- Auto asymmetry control amplifier

4-1. Block diagram



CIRCUIT DESCRIPTION

4-2. Terminal functions (V_{CC} = 2.5V, V_{EE} = D_{GND} = –2.5V, VC = GND)

Pin No.	Pin name	I/O	DC voltage (V)	Function
1	RFI	I	0	Input pin for the C-coupled signal output from the RF summing amplifier.
2	RFO	O	V_{RFO}	RF summing amplifier output pin. Used as the check point for the eye pattern.
3	RF⊖	I	0	RF summing amplifier feedback input pin.
4	P/N	I	0 (VC)	P-sub/N-sub select pin for the LD (Laser Diode). (DC voltage : in N-sub mode)
5	LD	O	–1.8	* APC LD amplifier output pin. (DC voltage : PD open in N-sub mode)
6	PD	I	0	* APC LD amplifier input pin. (DC voltage : open)
7	PD1	I	0	RF I-V amplifier (1) inverted input pin. Current input by connecting to the photodiode A + C terminal.
8	PD2	I	0	RF I-V amplifier (2) inverted input pin. Current input by connecting to the photodiode B + D terminal.
9	VC	–	0	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply. Connected to VR (pin 14) when using a single-voltage power supply.
10	F	I	0	F I-V amplifier inverted input pin. Current input by connecting to the photodiode F terminal.
11	E	I	0	E I-V amplifier inverted input pin. Current input by connecting to the photodiode E terminal.
12	EO	O	0	E I-V amplifier output pin.
13	EI	I	0	E I-V amplifier feedback input pin. For E I-V amplifier gain adjustment.
14	VR	O	V_{CVO}	DC voltage output pin of (V_{CC} + V_{EE})/2.
15	CC2	I	1.0	Input pin for the C-coupled signal output from the defect bottom hold.
16	CC1	O	1.2	Defect bottom hold output pin.
17	V_{EE}	–	–2.5	Connected to the negative power supply when using a positive (+)/negative (–) dual-voltage power supply. Connected to GND when using a single-voltage power supply.
18	FF BIAS	I	0	Bias pin on the focus error amplifier non-inverted side. For CMR adjustment of the focus error amplifier.
19	FE	O	V_{FEO}	Focus error amplifier output pin.
20	TE	O	V_{TEO}	Tracking error amplifier output pin.
21	DEFECT	O	V_{DFCTL}	Defect comparator output pin. (DC voltage : connected to a 10 k-ohm load)
22	MIRR	O	V_{MIRL}	Mirror comparator output pin. (DC voltage : connected to a 10 k-ohm load)
23	CP	I	–1.3	Mirror hold capacitor output pin. Mirror comparator non-inverted input.
24	CB	I	0	Defect bottom hold capacitor connect pin.
25	DGND	–	–2.5	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply. Connected to GND (V_{EE}) when using a single-voltage power supply.
26	ASY	I	–	Auto asymmetry control input pin.
27	EFM	O	V_{EFMH}	EFM comparator output pin. (DC voltage : connected to a 10 k-ohm load)
28	FOL	O	V_{FOKL}	FOK comparator output pin. (DC voltage : connected to a 10 k-ohm load)
29	LD ON	I	–2.5 (D_{GND})	LD ON/OFF select pin. (DC voltage : when LD ON)
30	V_{CC}	–	2.5	Positive power supply.

* APC : Automatic Power Control

CIRCUIT DESCRIPTION

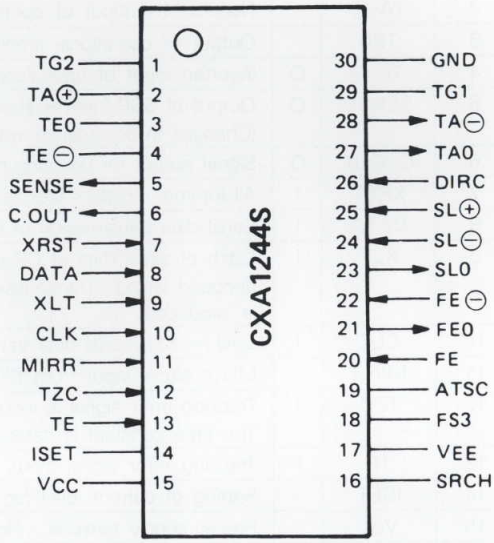
5. Servo Signal Processor : CXA1244S (IC5)

CXA1244S is a bipolar IC developed for servo of compact disc (CD) players, and it provides the following functions.

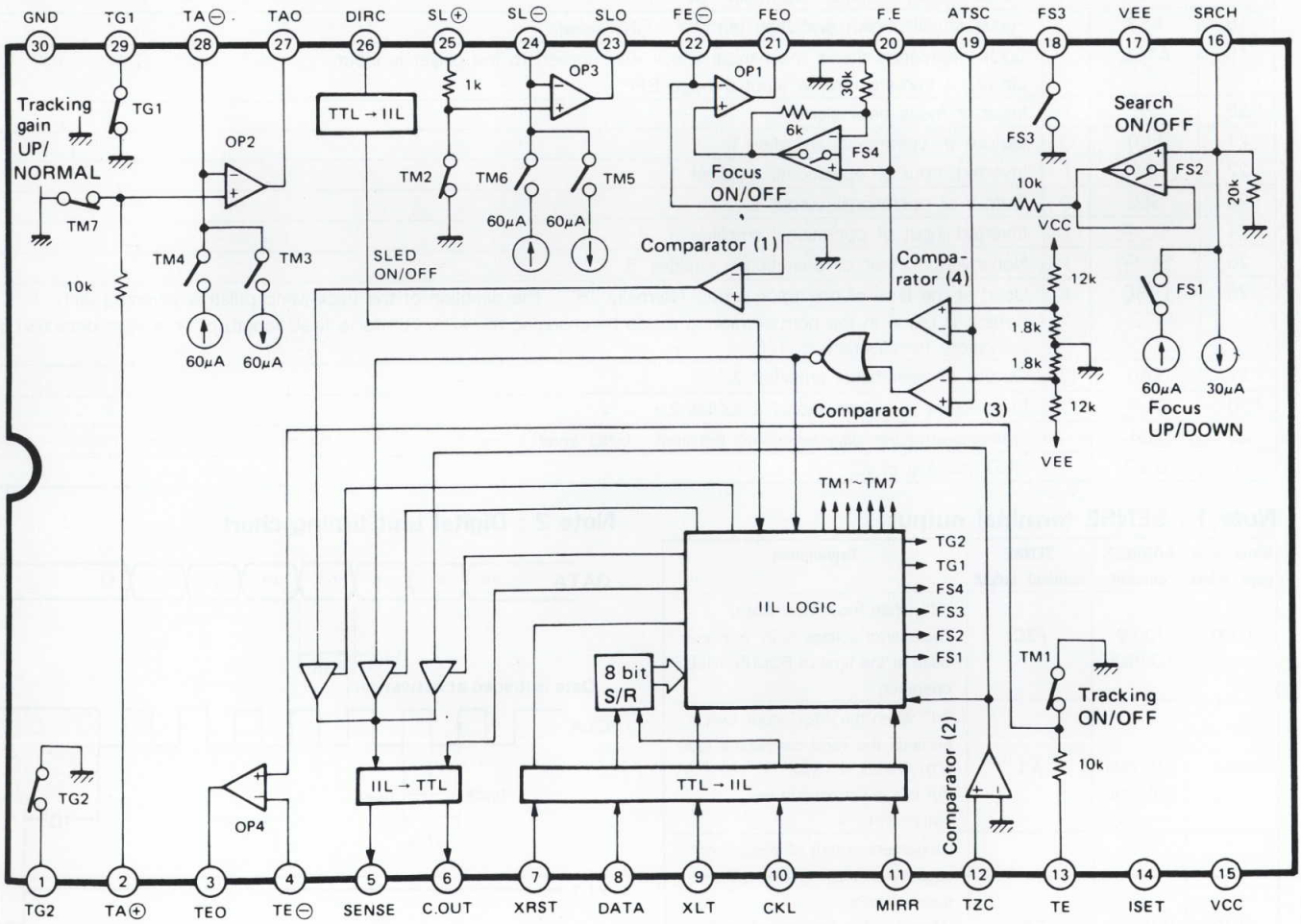
- Focus control (search ON/OFF, gain control)
- Tracking control (servo ON/OFF, single track jump, multiple track jump, gain control, phase compensation control, brake circuit)
- Sled control (servo ON/OFF, fast forward, fast reverse)

Servo function of each of focus, tracking and sled as well as random access operation are realized through control by microcomputer. Furthermore, the serial data bus can be shared with CX23035.

5-1. Terminal connection diagram



5-2. Block diagram



CIRCUIT DESCRIPTION

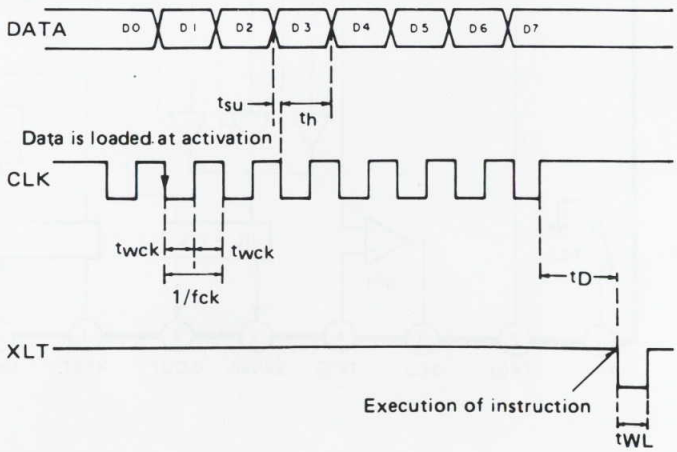
5-3. Terminal functions

Pin No.	Pin name	I/O	Function
1	TG2		Trackingamplifier gain switching terminal. GND level.
2	TA ⊕		Non-inverted input of operational amplifier 2.
3	TE0		Output of operational amplifier 4.
4	TE ⊖	O	Inverted input of operational amplifier 4.
5	SENSE	O	Output of SSP internal status that corresponds to ADDRESS of CPU → SSP. (Changes in accordance with ADDRESS content of internal serial register.) See Note 1.
6	C. OUT	O	Signal output for counting number of tracks at the time of high speed access.
7	XRST	I	All internal registers are cleated when CPU → SSP "L". Connected with CPU RESET. See Note 2.
8	DATA	I	Serial data transmission of CPU → SSP. Input is made from LSB, D0 ~ D7.
9	XLT	I	Latch of serial data of CPU → SSP. (The contents of internal serial register are transmitted to each address decoded latch.) Transmission at "L". Change to "H" occurs immediately after execution because no edge trigger is produced.
10	CLK	I	CPU → SSP serial data transmission block. Data is read at falling. "H" level before and after transmission.
11	MIRR	I	Mirror signal input from RF amplifier.
12	TZC	I	Tracking error signal is input with C couple. The time constant is determined by one single track jump, but it is usually around 2kHz.
13	TE	I	Tracking error signal input.
14	ISET		Setting of current level for determining focus search voltage, tracking jump voltage and thread feed voltage.
15	Vcc		Power supply terminal. Normally –5V.
16	SRCH		The condenser for determining the time constant of charge/discharge waveform for focus search is connected.
17	VEE		Power supply terminal. Normally –5V.
18	FS3		Focus amplifier gain switching terminal. GND level.
19	ATSC		Such information that a mechanical shock was applied to the player is input. Simply, a tracking error is input through BPF.
20	FE	I	Input of focus error signal.
21	FE0	O	Output of operational amplifier 1.
22	FE ⊖	I	Inverted input of operational amplifier 1.
23	SL0	O	Output of operational output 3.
24	SL ⊖	I	Inverted input of operational amplifier 3.
25	SL ⊕	I	Non-inverted input of operational amplifier 3.
26	DIRC	I	Used at the time of one track jump. Normally "H". The direction of the track jump pulse is reversed with "L". Setting is made in the normal tracking mode by changing to "H". "L" for a fixed length of time with detection of activation, deactivation of TZC.
27	TA0	O	Output of operational amplifier 2.
28	TA ⊖	O	Inverted input of operational amplifier 2.
29	TG1		Tracking amplifier gain switching terminal. GND level.
30	GND		GND terminal of IC.

Note 1 : SENSE terminal output

Serial data upper 4 bits	ADDRESS content	SENSE terminal output	Explanation
0000	FOCUS CONTROL	FZC	"H" when focus zero cross, Focus error voltage is 0V or higher. Used at the time of FOCUS PULL operation.
0001	TRACKING CONTROL	AS	"H" when the ATSC input level exceeds the wind comparator level (VTH = ±Vcc x 13%). But this is not used in this equipment.
0010	TRACKING MODE	TZC	Judgement output of positive or negative of tracking zero cross, tracking error. When used at the time of single track jump, DIRC is reduced to "L" on detection of TZC ↑, in FWD JUMP or on detection of TZC ↓ in REV JUMP.

Note 2 : Digital unit timing chart



CIRCUIT DESCRIPTION

6. Digital Signal Processor : CXD1167Q (IC10)

General

The CXD1167Q is a digital signal processing LSI for Compact Disc player, and has the following functions.

- Bit clock reproduction by an EFM-PLL circuit
- EFM data demodulation
- Frame sync signal detection, protection and insertion
- Powerful error detection and correction
- Interpolation with an average value, or by holding the previous value
- Demodulation of a sub code signal, error detection of a sub code Q
- Spindle motor CLV servo
- 8-bit tracking counter
- CPU interface with a serial bus
- Sub code Q register
- Digital filter
- Digital audio interface output

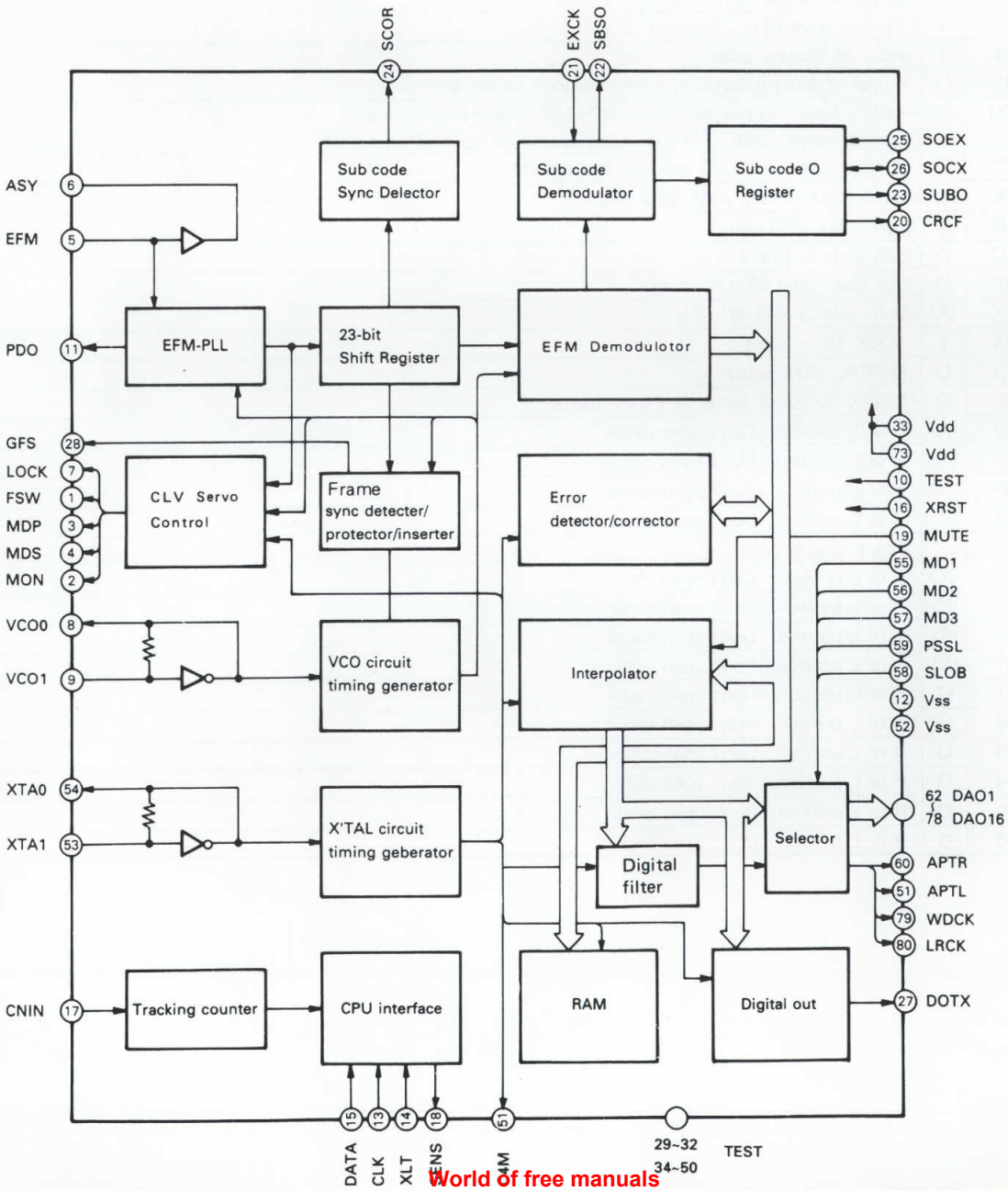
Features

- All digital signals used in playback can be processed using only a single chip.
- An aperture-correction digital filter is built-in.

Structure

CMOS IC

6-1. Block diagram



CIRCUIT DESCRIPTION

6-2. Terminal functions

Pin No.	Pin name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level to EFM signal.
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high. When it is "L" for eight times, in arrow, outputs "L".
8	VCOO	O	VCO output. f = 8.6436MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V).
11	PDO	O	Phase comparison output of EFM signal and VCO/2.
12	Vss	–	GND (0V).
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	I	Input of tracking pulse.
18	SENS	O	output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case when ATTM of internal register A is "L". Normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of cub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code serial output.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync S0 + S1 output.
25	SQCK	I/O	Sub code Q read-off clock.
26	SQEX	I	SQCK select input.
27	DOTX	O	DIGITAL OUT output.
28	GFS	O	Display output of frame sync lock status.
29	DB08	I/O	H or L position. Don't open circuit.
30	DB07	I/O	H or L position. Don't open circuit.
31	DB06	I/O	H or L position. Don't open circuit.
32	DB05	I/O	H or L position. Don't open circuit.
33	VDD	–	Power supply (+5V).
34	DB04	I/O	H or L position. Don't open circuit.
35	DB03	I/O	H or L position. Don't open circuit.
36	DB02	I/O	H or L position. Don't open circuit.
37	DB01	I/O	H or L position. Don't open circuit.
38	RA01	O	H or L position. Don't open circuit.
39	RA02	O	H or L position. Don't open circuit.
40	RA03	O	H or L position. Don't open circuit.
41	RA04	O	H or L position. Don't open circuit.
42	RA05	O	H or L position. Don't open circuit.
43	RA06	O	H or L position. Don't open circuit.

CIRCUIT DESCRIPTION

Pin No.	Pin name	I/O	Function
44	RA07	O	H or L position. Don't open circuit.
45	RA08	O	H or L position. Don't open circuit.
46	RA09	O	H or L position. Don't open circuit.
47	RA10	O	H or L position. Don't open circuit.
48	RA11	O	H or L position. Don't open circuit.
49	RAWE	O	H or L position. Don't open circuit.
50	RACS	O	H or L position. Don't open circuit.
51	C4M	O	Crystal dividing output. f = 4.2336MHz
52	Vss	–	GND (0V).
53	XTAI	I	Crystal oscillator input. f = 8.4672MHz or 16.9344MHz depending on the mode selected.
54	XTAO	O	Crystal oscillator output. f = 8.4672MHz or 16.9344MHz depending on the mode selected.
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select input. Serial output when "L", parallel output when "H".
60	APTR	O	Aperture compensation control output. "H" when R-ch
61	APTL	O	Aperture compensation control output. "H" when L-ch
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL = "H", C1F1 output when PSSL = "L".
63	DA02	O	DA02 output when PSSL = "H", C1F2 output when PSSL = "L".
64	DA03	O	DA03 output when PSSL = "H", C2F1 output when PSSL = "L".
65	DA04	O	DA04 output when PSSL = "H", C2F2 output when PSSL = "L".
66	DA05	O	DA05 output when PSSL = "H", C2FL output when PSSL = "L".
67	DA06	O	DA06 output when PSSL = "H", C2PO output when PSSL = "L".
68	DA07	O	DA07 output when PSSL = "H", RFCK output when PSSL = "L".
69	DA08	O	DA08 output when PSSL = "H", WFCK output when PSSL = "L".
70	DA09	O	DA09 output when PSSL = "H", $\overline{\text{PLCK}}$ output when PSSL = "L".
71	DA10	O	DA10 output when PSSL = "H", UGFS output when PSSL = "L".
72	DA11	O	DA11 output when PSSL = "H", GTOP output when PSSL = "L".
73	VDD	–	Power supply (+5V).
74	DA12	O	DA12 output when PSSL = "H", RAOV output when PSSL = "L".
75	DA13	O	DA13 output when PSSL = "H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL = "H", $\overline{\text{C210}}$ output when PSSL = "L".
77	DA15	O	DA15 output when PSSL = "H", C210 output when PSSL = "L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL = "H", DATA output when PSSL = "L".
79	WDCK	O	Strobe signal output. 176.4kHz when DF is ON, 88.2kHz with CXD1167Q or when DF is OFF.
80	LRCK	O	Strobe signal output. 88.2kHz when DF is ON, 44.1kHz with CXD1167Q or when DF is OFF.

Notes :

C1F1 : Error correction status monitor output for C1 decode.

C1F2 : Error correction status monitor output for C1 decode.

C2F1 : Error correction status monitor output for C2 decode.

C2F2 : Error correction status monitor output for C2 decode.

C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.

C2PO : C2 pointer signal. Synchronized to the audio data output.

RFCK : Read frame clock output. 7.35MHz when locked to the crystal line.

WFCK : Write frame clock output. 7.35MHz when locked to the crystal line.

$\overline{\text{PLCK}}$: VCO/2 output. f = 4.3218MHz when locked to the EFM signal.

UGFS : Non-protected frame sync pattern output.

GTOP : Frame sync protect status display output.

RAOV : ±4 frame jitter absorption RAM overflow and underflow display output.

C4LR : Strobe signal. 352.8kHz when DF is ON, 176.4kHz with CXD1167Q or DF is OFF.

$\overline{\text{C210}}$: C210 invert output.

C210 : Bit clock output. 4.2336MHz when DF is ON, 2.1168MHz with CXD1167Q or when DF is OFF.

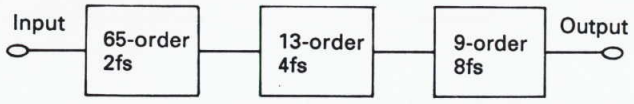
DATA : Audio signal serial data output.

CIRCUIT DESCRIPTION

7. Digital Filter : PD0060 (IC12)

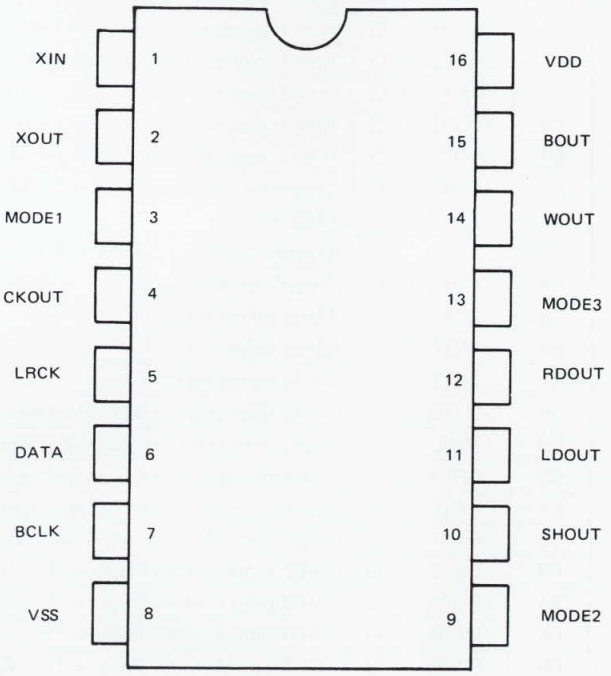
7-1. Functions and features

· Composition of filters



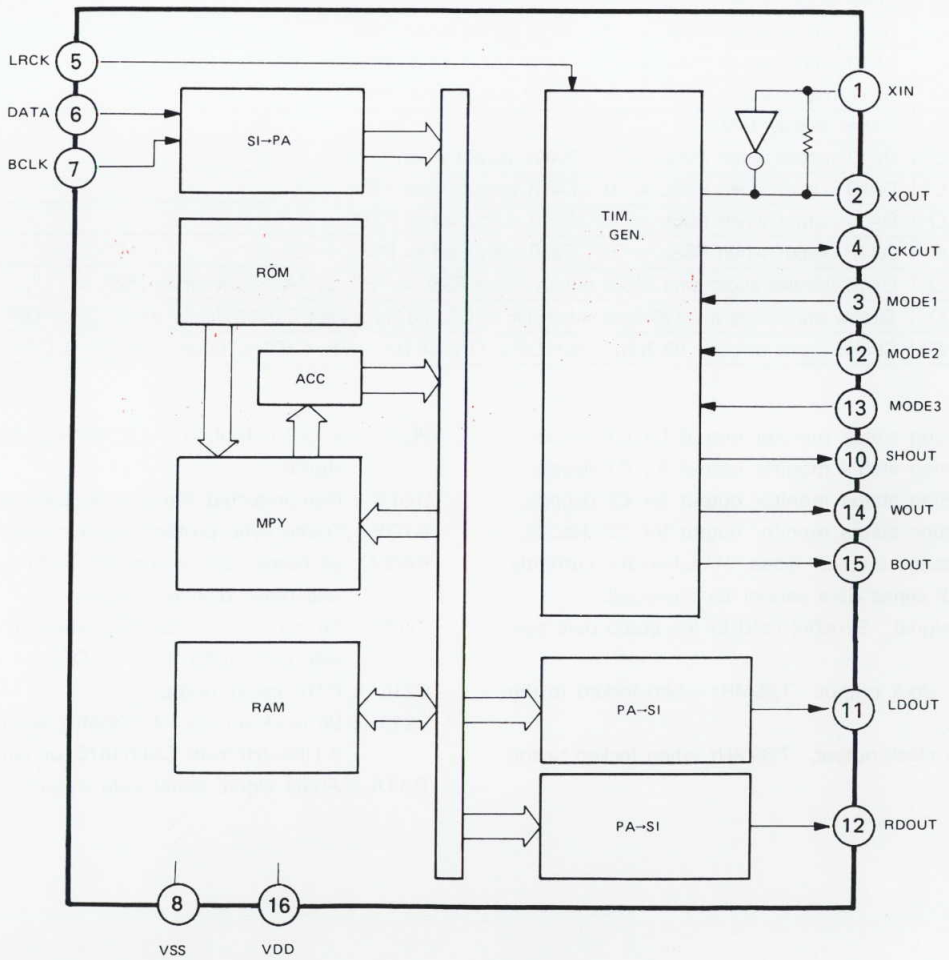
· Input data
  Two's complement, MSB first
· Output data
  Two's complement, MSB first
· TTL compatible
· Jitter free
· 1st noise shaping

7-2. Terminal connection diagram



TOP VIEW

7-3. Block diagram



CIRCUIT DESCRIPTION

7-4. Terminal function

Pin No.	Symbol	Name	I/O	Function
1	XIN	XIN	I	Crystal oscillator circuit input or external input.
2	XOUT	XOUT	O	Crystal oscillator circuit output.
3	MODE1	MODE1	I	Master clock (XIN) and CKOUT select. *1
4	CKOUT	CLOCK OUT	O	External clock output. *1
5	LRCK	LR CLOCK	I	LR clock input.
6	DATA	DATA	I	Serial data input (Two's complement, MSB first).
7	BCLK	BIT CLOCK	I	Bit clock input for input data.
8	Vss	–	–	Grounding terminal.
9	MODE2	MODE2	I	"H" : 18-bit data output. "L" : 16-bit data output. *2
10	SHOUT	SHOUT	O	Sample holding pulse output.
11	LDOUT	Lch DATA OUT	O	Lch data output (Two's complement, MSB first).
12	RDOUT	Rch DATA OUT	O	Rch data output (Two's complement, MSB first).
13	MODE3	MODE3	I	"H" : 16 or 18-bit data output. "L" : 20-bit data output. *2
14	WOUT	WORD CK OUT	O	Word clock output.
15	BOUT	BIT CK OUT	O	Bit clock output for LDOUT and RDOUT.
16	VDD	–	–	+5V power terminal.

*1 : Master clock (Frequency of crystal oscillator or that of external input) can be selected from the following by using terminal MODE1. Recognition of CKOUT (384fs/192fs, 392fs/196fs) is automatically.

MODE1	Master clock (XIN)	CKOUT
H	384fs/392fs	384fs/392fs
L	192fs/196fs	192fs/196fs

*2 : Data output selected by terminals MODE2 and MODE3

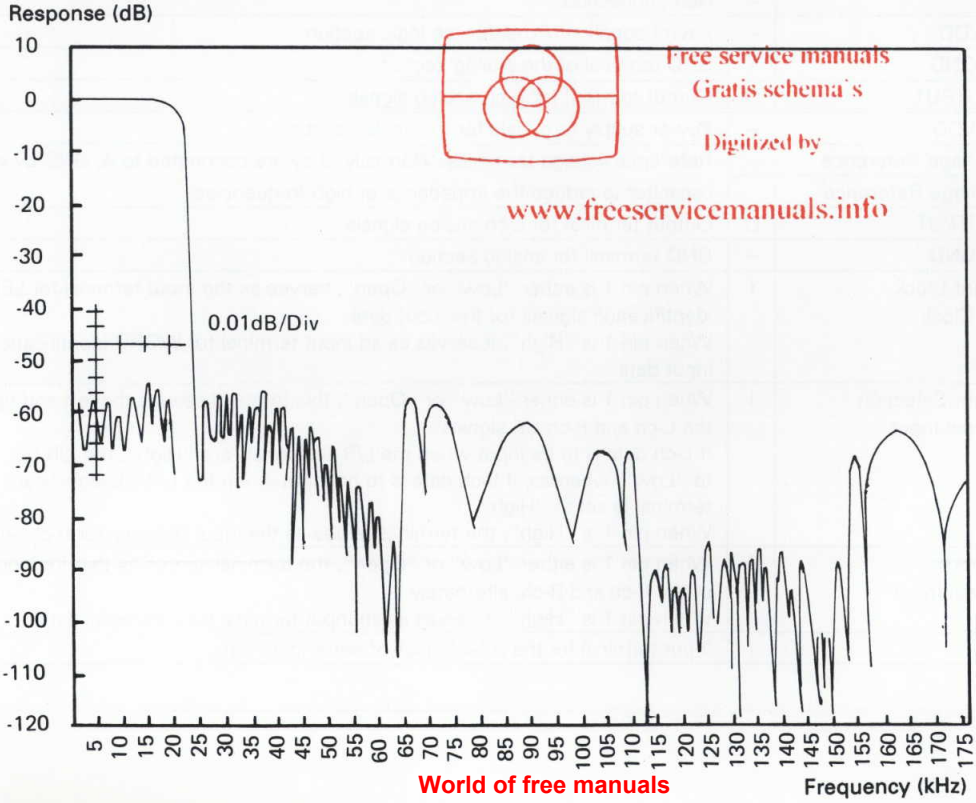
MODE3	MODE2	Data output
H	H	18-bit
H	L	16-bit
L		20-bit

7-5. Filter characteristics

- **Over sampling filter**
  (Frequency = 0 ~ 176.4kHz, fs = 44.1kHz)

Characteristics item	Performance
Pass band	0 ~ 20kHz
Attenuation band	24.1kHz or more
Ripple	Within –0.046 ± 0.023dB
Attenuation characteristics	53dBm or more

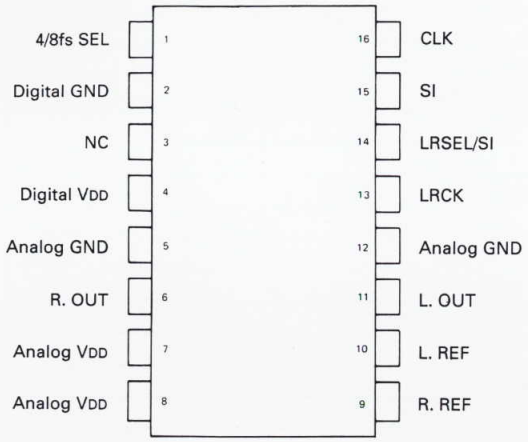
- **Sampling frequency (fs = 44.1kHz)**



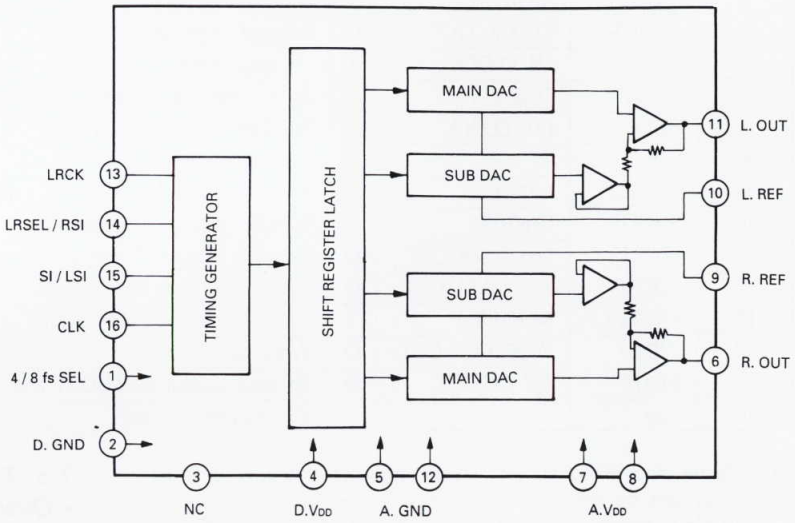
CIRCUIT DESCRIPTION

8. D/A Converter : μPD6376CX (IC14)

8-1. Terminal connection diagram



8-2. Block diagram



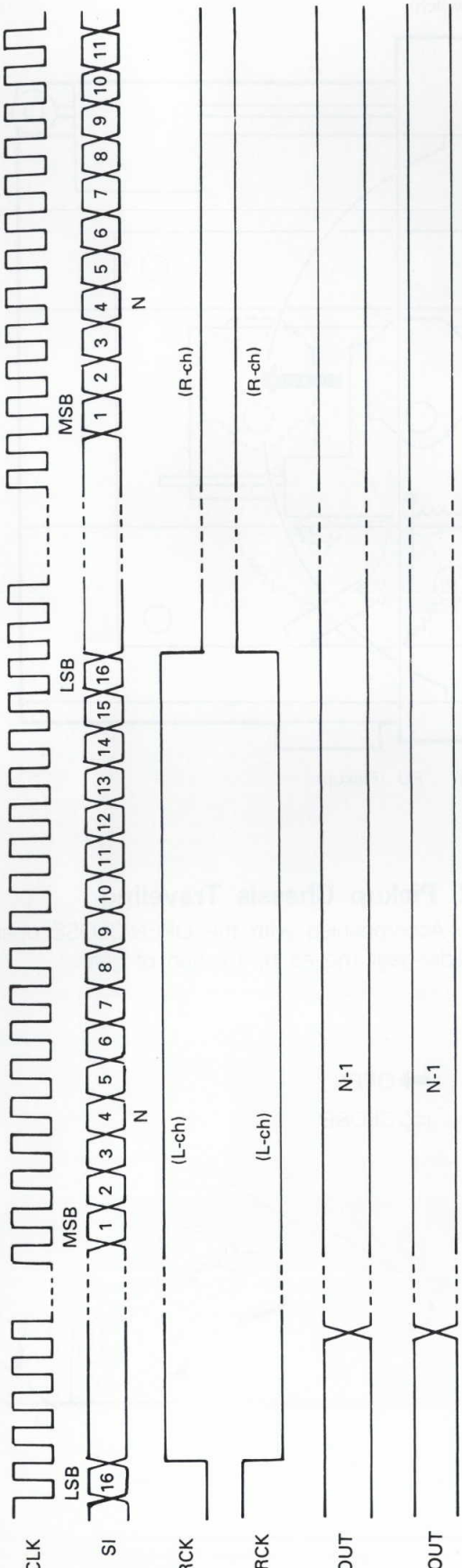
8-3. Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	4/8fs SEL	I	When this terminal is set to "Low" or "Open", time-sharing input of the L-ch and R-ch data will take place from pin 15. When set to "High", the L-ch data will be input from pin 15, while the R-ch data will be input from pin 14. (Pull-down is provided inside the IC by means of a 100kΩ resistor.)
2	Digital GND	–	GND terminal of the logic section.
3	NC	–	Non connection.
4	Digital VDD	–	Power supply terminal for the logic section.
5	Analog GND	–	GND terminal of the analog section.
6	R-ch OUTPUT	O	Output terminal for R-ch analog signals.
7, 8	Analog VDD	–	Power supply terminals for the analog section.
9	R-ch Voltage Reference	–	Reference voltage terminals. Normally, they are connected to A. GND by way of a capacitor to reduce the impedance at high frequencies.
10	L-ch Voltage Reference		
11	L-ch OUTPUT	O	Output terminal for L-ch analog signals.
12	Analog GND	–	GND terminal for analog section.
13	Left/Right Clock WORD Clock	I	When pin 1 is either "Low" or "Open", serves as the input terminal for LEFT/RIGHT identification signals for the input data. When pin 1 is "High", it serves as an input terminal for WORD identification signals for the input data.
14	Left/Right Selection R-ch Serial Input	I	When pin 1 is either "Low" or "Open", this terminal selects the left and right polarities for the L-ch and R-ch CK signals. If L-ch data is to be input when the L/R CK signals are "High", the L/R SEL terminal is set to "Low", whereas, if L-ch data is to be input when the L/R CK signals are "Low", the terminal is set to "High". When pin 1 is "High", the terminal serves as the input terminal for R-ch serial data.
15	Serial Input L-ch Serial Input	I	When pin 1 is either "Low" or "Open", the terminal serves as that for inputting serial data of the L-ch and R-ch, alternately. When pin 1 is "High", it serves as an input terminal for L-ch serial data.
16	CLOCK	I	Input terminal for the READ clock of serial input data.

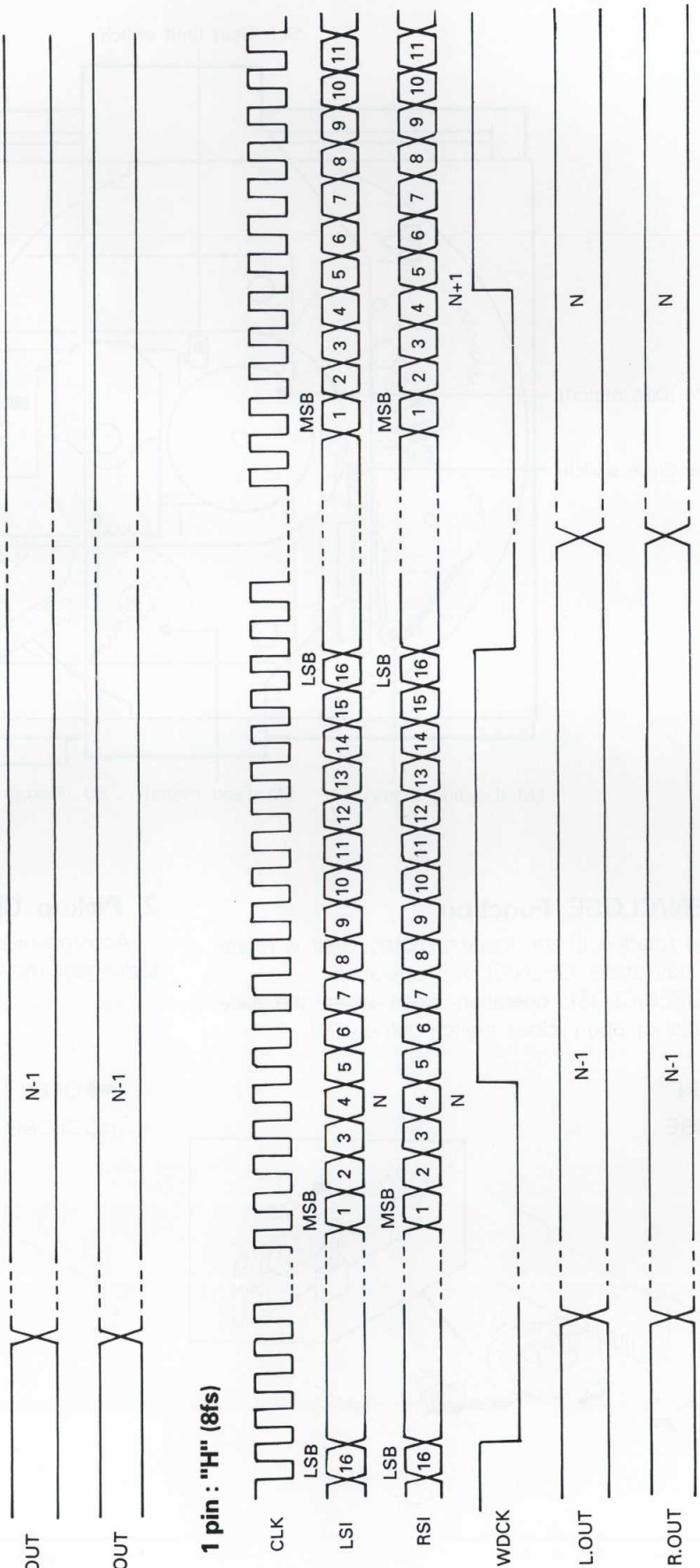
CIRCUIT DESCRIPTION

8-4. Timing chart

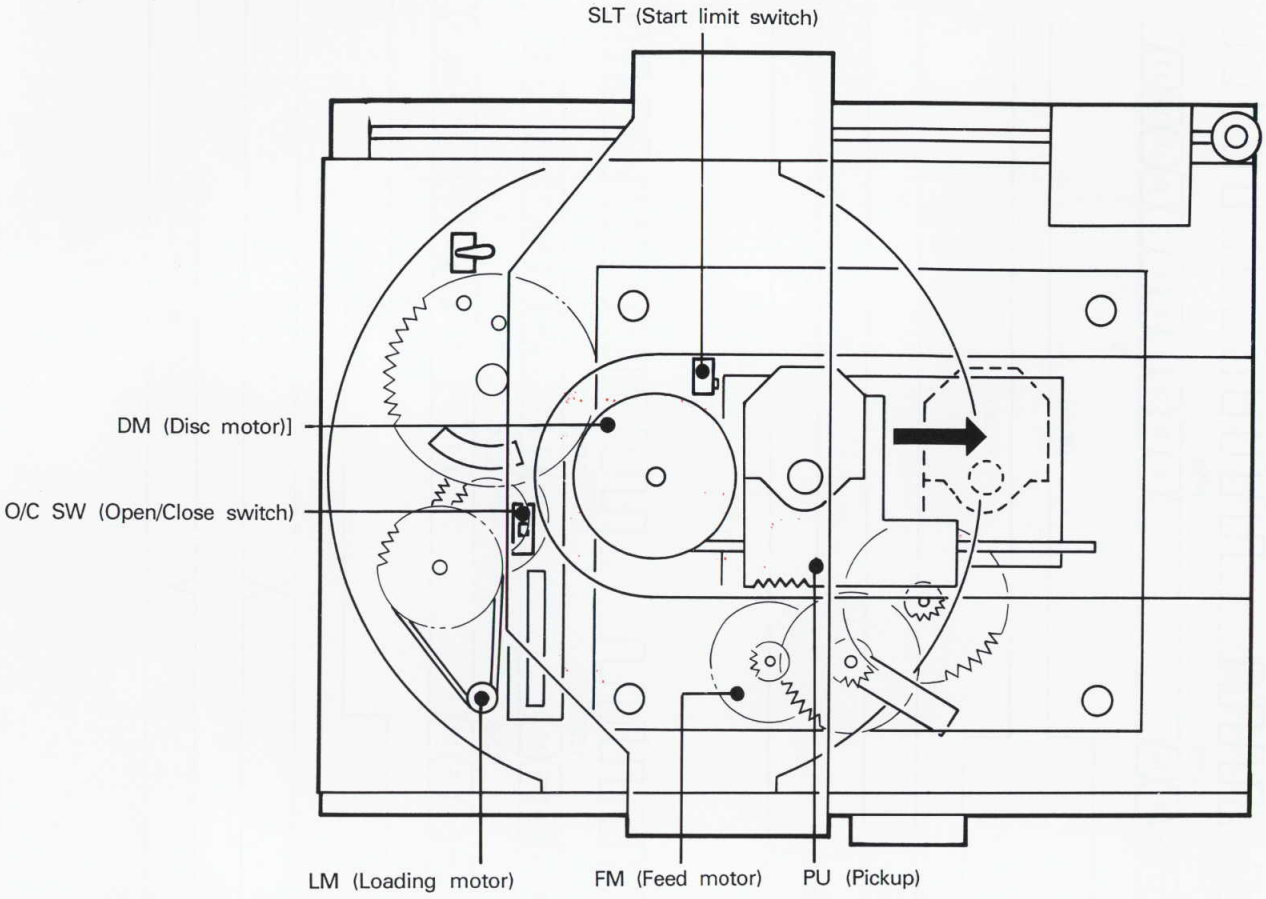
• 1 pin : "L" or open (4fs)



• 1 pin : "H" (8fs)



MECHANISM OPERATION DESCRIPTION

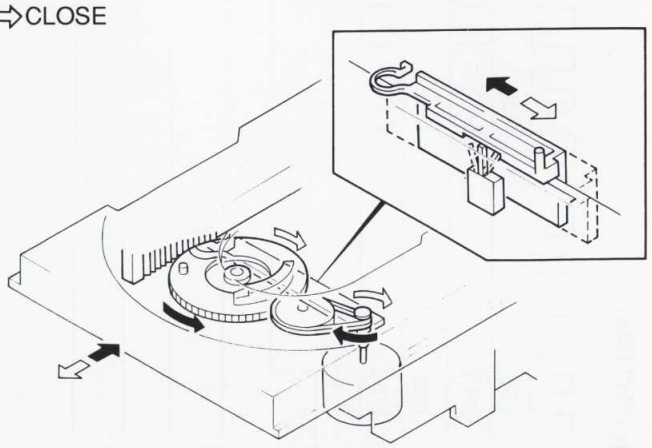


1. OPEN/CLOSE Function

By the rotation of the loading motor, Gear is rotate and the tray starts OPEN/CLOSE operation.

The OPEN/CLOSE operation stops when the slide gear travels or open /close switch comes ON.

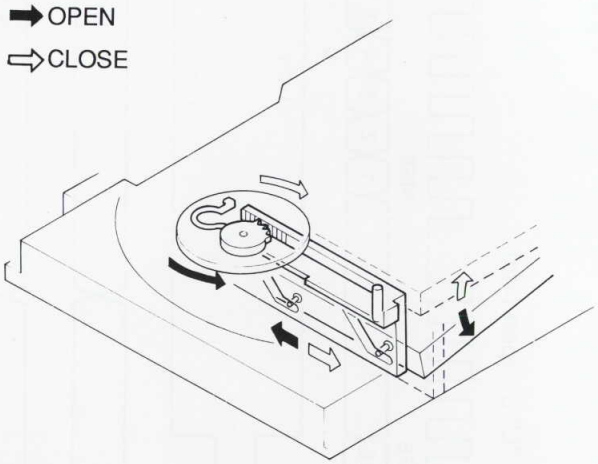
➡OPEN
⇨CLOSE



2. Pickup Chassis Traveling

Accompanied with the OPEN/CLOSE operation, the slider-gear moves by rotation of gear.

➡OPEN
⇨CLOSE



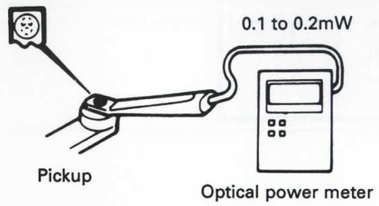
DP-711

ADJUSTMENT

No.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG.
1	LASER POWER	–	Apply the sensor section of the optical power meter on the pickup lens.	Short-circuit pins TEST and turn the power on to enter the test mode. Press the MANUAL S. (▶▶) to move the pickup outwards. Press the RANDOM keyto check that the LD emits light. Then, confirm that the display is "03".	–	On the power from 0.1 to 0.2mW, when the diffraction grating is correctly a ligned with the RF level of 1.5Vp-p or more and the TE (servo open) level of 1.5Vp-p or more, the pickup is acceptable.	(a)
2	VCO	–	Connect a frequency counter to PLCK (TP6).	Press the STOP key. and confirm that the display is "01".	L2	4.275MHz ± 5kHz	(b)
3	TRACKING ERROR BALANCE	Test disc Type 4	Connect an oscilloscope as follows. CH1: RF (CN6-1) CH2: TE (CN6-6)	Press the OPEN/CLOSE key to open the tray. Reset to TEST mode. Then, press the RANDOM key. Confirm that the display is "03".	TE BALANCE VR1	Symmetry between upper and lower patterns, or DC=0±0.05V	(c)
4	FOCUS ERROR BALANCE	Test disc Type 4	Connect an oscilloscope as follows. CH1: RF (CN6-1) CH2: TE (CN6-6)	Press the PLAY key. Confirm that the display is "05".	FE BALANCE VR2	Optimum eyepattern	(d)
5	FOCUS GAIN	Test disc Type 4 Apply signal of 800Hz, 0.1Vrms to CN6 pin 2 and 3.	Connect a LPF to CN6 pin 2-3, to which connect an oscilloscope or two AC voltmeters.	Press the PLAY key. Confirm that the display is "05".	FOCUS GAIN VR3	0.1Vrms	(e)
6	TRACKING GAIN	Test disc Type 4 Apply signal of 1.0kHz, 0.1Vrms to CN6 pin 5 and 6.	Connect a LPF to CN6 pin 5-6, to which connect an oscilloscope or two AC voltmeters. or two AC voltmeters.	Press the PLAY key. Confirm that the display is "05".	TRACKING GAIN VR4	0.1Vrms	(e)

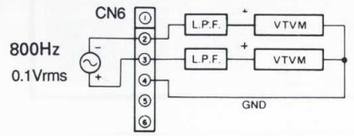
(NOTE) Type 4 disc : SONY YEDS-18 TEST DISC or equivalent.
LPF: around 47kohms+390pF or so.
Adjustment procedures are in TEST MODE.

(a) Laser Power

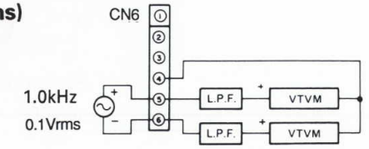


(e) Focus Gain and Tracking Gain

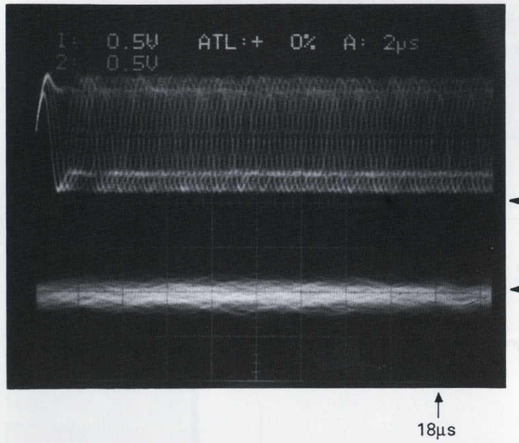
Focus gain : 0dB (0.1Vrms)



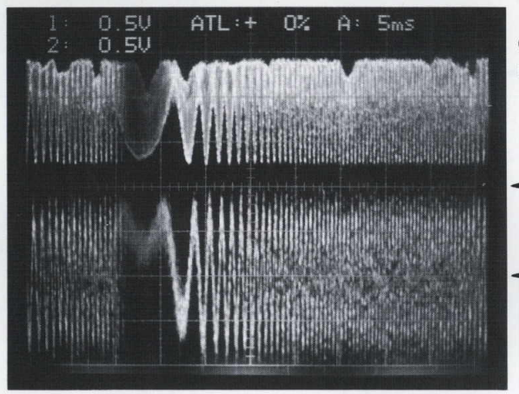
Tracking gain : 0dB (0.1Vrms)



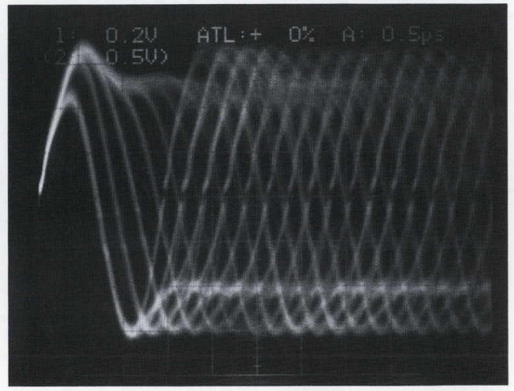
ADJUSTMENT



- RF signal and E.Spot signal in test mode (PLAY).
- If the diffraction grating has been adjusted properly, the influence of triggering is observed on the E.Spot waveform of approx. 18µs after RF signal, in the form of a projection.

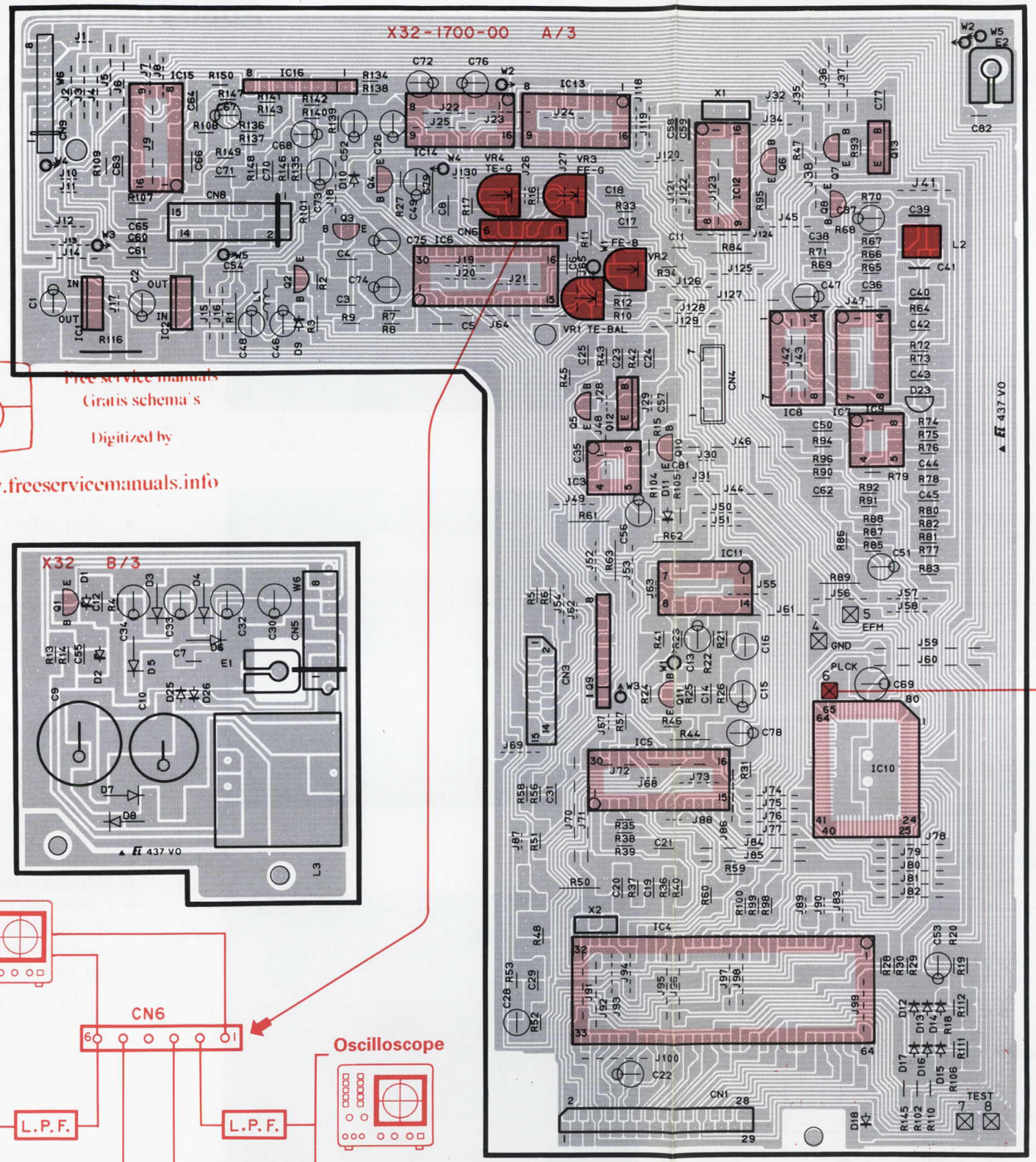


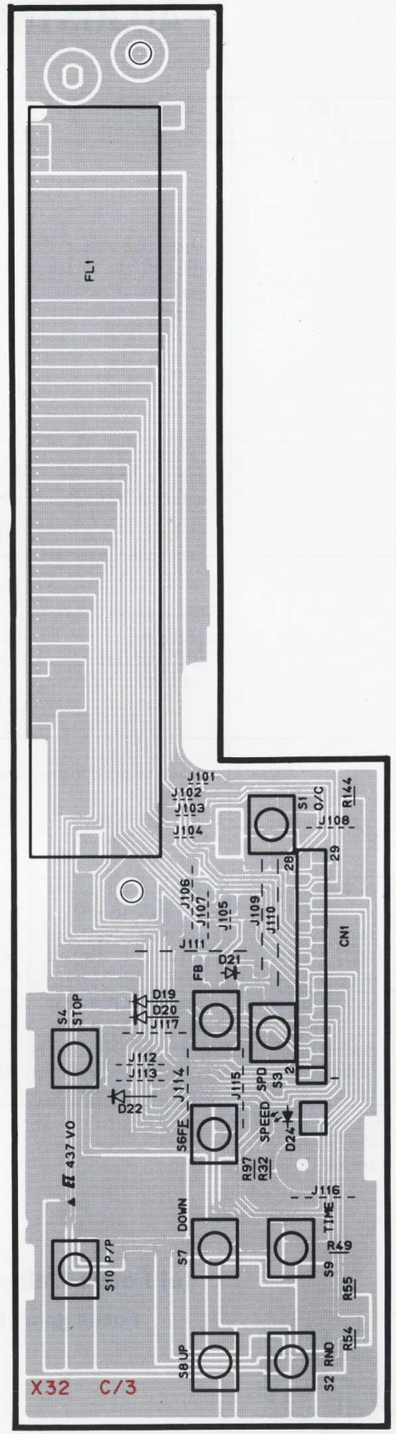
- RF signal and T.Error signal; in test mode (Focusing ON). (Disc type 4)
- Adjust T.Error so that the waveform is symmetrical above and below 0V. (VR1)



- RF signal in test mode (PLAY).
- Perform the tangential and focusing offset adjustments so that each of the center cross points are focused into one point on the display. The crossing points above and below the center shall also be displayed clearly.

PC BOARD (COMPONENT SIDE VIEW)





Oscilloscope

(c) Tracking error balance
: Symmetry between upper and lower patterns, or DC = 0 ± 0.05V

(d) Focus error balance
: Optimum eyepattern

CN6

Oscilloscope

L.P.F.

L.P.F.

AC voltmeter

(e) Tracking gain : 0.1Vrms

Oscilloscope

L.P.F.

L.P.F.

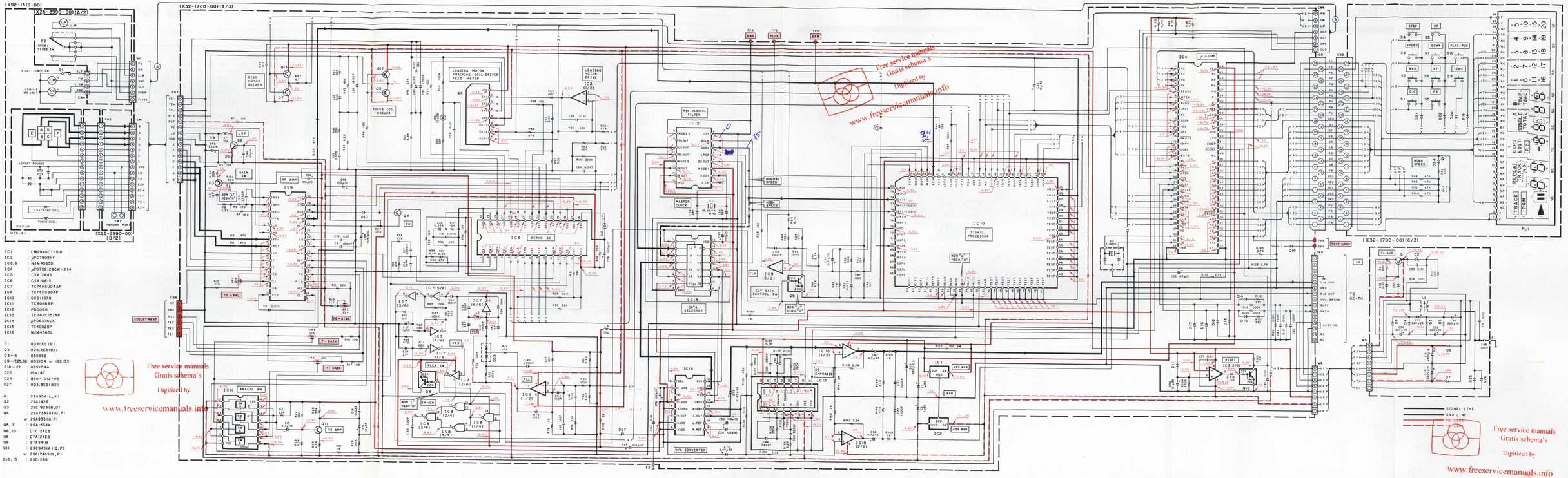
AC voltmeter

(e) Focus gain : 0.1Vrms

Frequency counter

(b) VCO : 4.275MHz ± 5kHz

Refer to the schematic diagram for the values of resistors and capacitors.



IC1 : LM2940CT-5.0
IC2 : μPC7905HF
IC3,9 : NJM4565D
IC4 : μPD75212ACW-214
IC5 : CXA1244S
IC6 : CXA1081S
IC7 : TC74HCU04AP
IC8 : TC74HC00AP
IC10 : CXD1167Q
IC11 : TC4066BP
IC12 : PD0060
IC13 : TC74HC157AP
IC14 : μPD6376CX
IC15 : TC4052BP
IC16 : NJM4565L

D1 : RD3OES(B)
D2 : RD6.2ES(B2)
D3~8 : S5566B
D9~12,26 : HSS104 or 1SS133
D18~22 : HSS104A
D23 : 1SV147
D24 : B30-1012-05
D27 : RD3.3ES(B2)

Q1 : 2SA954(L,K)
Q2 : 2SA1426
Q3 : 2SC1923(R,O)
Q4 : 2SA733(A1Q,P) or 2SA933(Q,R)
Q5,7 : 2SA1534A
Q6,10 : DTC124ES
Q8 : DTA124ES
Q9 : STA341M
Q11 : 2SC945(A1Q,P) or 2SC1740S(Q,R)
Q12,13 : 2SD1266

2SA1534A
2SA733(A)
2SA954
2SC1923
2SC945(A)

DTC124ES

2SD1266

2SA1426

DTA124ES
2SA933S
2SC1740S

TC4066BP
TC74HCU04SAP
TC74HC00AP

TC4052BP
TC74HC157AP
μPD6376CX

NJM4565D

STA341M

LM2940CT-5.0

CXA1081S
CXA1244S

CXD1167Q

μPD75212ACW-214

μPC7905HF

CAUTION : For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments and units.

Y22-2190-11

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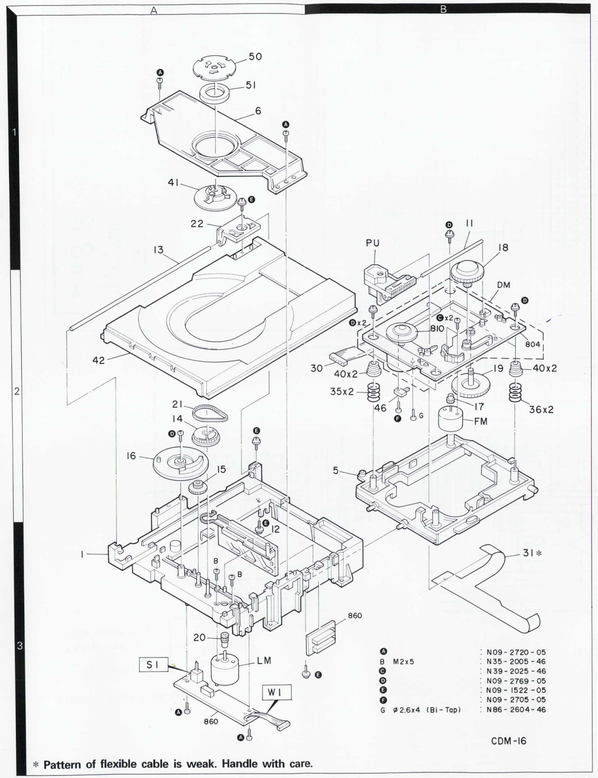
KENWOOD

EXPLODED VIEW (MECHANISM)



B	M2x5	: N09-2720-05
C		: N35-2005-46
D		: N39-2025-46
E		: N09-2769-05
F		: N09-1522-05
G		: N09-2705-05
G	ø2.6x4 (Bi-Tap)	: N86-2604-46

* Pattern of flexible cable is weak. Handle with care.

Parts with the exploded numbers larger than 700 are not supplied.

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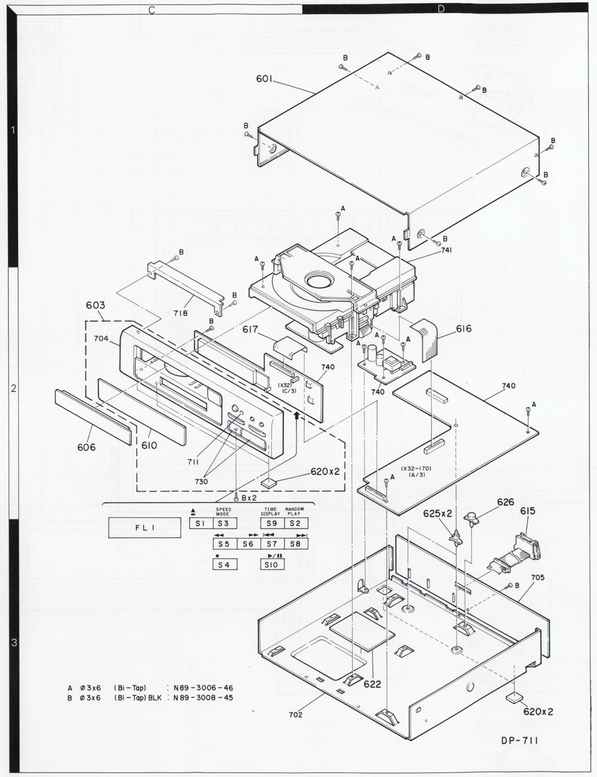
EXPLODED VIEW (UNIT)



Parts with the exploded numbers larger than 700 are not supplied.

DP-711

PARTS LIST

※ New Parts
Parts without **Parts No.** are not supplied.
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Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名/規格	Destination 仕向	Remarks 備考
			DP-711			
601	1C	*	A01-1865-01	METALLIC CABINET		
603	2C	*	A20-6053-12	PANEL ASSY		
606	2C	*	A29-0169-03	PANEL (TRAY)		
610	2C	*	B10-1091-04	FRONT GLASS		
-			B46-0092-03	WARRANTY CARD	K	
-			B46-0094-03	WARRANTY CARD	Y	
-			B46-0095-03	WARRANTY CARD	Y	
-			B46-0096-13	WARRANTY CARD	X	
-			B46-0121-03	WARRANTY CARD	P	
-			B46-0122-13	WARRANTY CARD	E	
-			B46-0143-13	WARRANTY CARD	T	
615	2D	*	E30-2625-05	CORD WITH CONNECTOR		
616	2D		E31-4799-05	WIRING HARNESS		
617	2C		E31-4941-05	WIRING HARNESS		
620	2D,3D	*	G11-2017-04	CUSHION		
-		*	H01-8842-04	ITEM CARTON CASE		
-		*	H10-5019-04	POLYSTYRENE FOAMED FIXTURE		
-		*	H10-5020-04	POLYSTYRENE FOAMED FIXTURE		
-		*	H20-0566-04	PROTECTION COVER	M	
-		*	H21-0277-04	PROTECTION SHEET		
-			H25-0232-04	PROTECTION BAG (235X350X0.03)	KPYXTE	
-			H25-0400-04	PROTECTION BAG	KPYXTE	
625	2D		J19-0586-05	UNIT HOLDER		
626	2D	*	J19-3322-05	UNIT HOLDER		
A			N89-3008-45	BINDING HEAD TAPTITE SCREW		
B			N89-3006-46	BINDING HEAD TAPTITE SCREW		
			MECHANISM UNIT (X25-3990-00)			
CN1 ,2			E10-1507-05	FLAT CABLE CONNECTOR		
S1		*	S33-2062-05	LEVER SWITCH		
			CONTROL UNIT (X32-1700-00)			
D24			B30-1012-05	LED(SLP-981C-50)		
C1 ,2			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C3			CC45FSL1H220J	CERAMIC 22PF J		
C4			CC45FSL1H060D	CERAMIC 6.0PF D		
C5			CF92FV1H472J	MF 4700PF J		
C6			CF92FV1H333J	MF 0.033UF J		
C7			CF92FV1H103J	MF 0.010UF J		
C8			CF92FV1H102J	MF 1000PF J		
C9			CE04KW1C682M	ELECTRO 6800UF 16WV		
C10			CE04KW1C222M	ELECTRO 2200UF 16WV		
C11 ,12			CF92FV1H103J	MF 0.010UF J		
C13			CE04KW1V100M	ELECTRO 10UF 35WV		
C14			CF92FV1H223J	MF 0.022UF J		
C15			CE04KW1V100M	ELECTRO 10UF 35WV		
C16			C90-1333-05	NP-ELEC 22UF 10WV		
C17			CF92FV1H104J	MF 0.10UF J		
C18			CC45FSL1H181J	CERAMIC 180PF J		
C19			CF92FV1H563J	MF 0.056UF J		

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C20			CF92FV1H183J	MF 0.018UF J		
C21			CF92FV1H104J	MF 0.10UF J		
C22			CE04KW1V100M	ELECTRO 10UF 35WV		
C23			CF92FV1H124J	MF 0.12UF J		
C24			CF92FV1H132J	MF 1300PF J		
C25			CF92FV1H753J	MF 0.075UF J		
C26			CE04KW1A101M	ELECTRO 100UF 10WV		
C28			C90-1332-05	NP-ELEC 10UF 25WV		
C29			CF92FV1H103J	MF 0.010UF J		
C30			CE04KW1C221M	ELECTRO 220UF 16WV		
C31			CF92FV1H103J	MF 0.010UF J		
C32 -34			CE04KW1E221M	ELECTRO 220UF 25WV		
C35			CF92FV1H103J	MF 0.010UF J		
C36			CF92FV1H102J	MF 1000PF J		
C37			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C38			CC45FSL1H270J	CERAMIC 27PF J		
C39			CC45FSU1H221J	CERAMIC 220PF J		
C40			CC45FUJ1H330J	CERAMIC 33PF J		
C41			CC45FUJ1H050C	CERAMIC 5.0PF C		
C42 ,43			CF92FV1H222J	MF 2200PF J		
C44			CF92FV1H124J	MF 0.12UF J		
C45			CC45FSL1H101J	CERAMIC 100PF J		
C46 ,47			CE04KW1A101M	ELECTRO 100UF 10WV		
C48			CE04KW1C330M	ELECTRO 33UF 16WV		
C49			CE04KW1HR47M	ELECTRO 0.47UF 50WV		
C50			CF92FV1H222J	MF 2200PF J		
C51			CE04KW1HR47M	ELECTRO 0.47UF 50WV		
C52 ,53			CE04KW1A101M	ELECTRO 100UF 10WV		
C54			CF92FV1H473J	MF 0.047UF J		
C55			CF92FV1H103J	MF 0.010UF J		
C56			CE04KW1V100M	ELECTRO 10UF 35WV		
C57			CF92FV1H103J	MF 0.010UF J		
C58			CC45FCH1H390J	CERAMIC 39PF J		
C59			CC45FCH1H390J	CERAMIC 39PF J		
C60			CK45FB1H102K	CERAMIC		
C61			CC45FSL1H221J	CERAMIC 220PF J		
C62			CF92FV1H333J	MF 0.033UF J		
C63 ,64			CF92FV1H332J	MF 3300PF J		
C65 ,66			CF92FV1H682J	MF 6800PF J		
C67 ,68			CE04KW1E4R7M	ELECTRO 4.7UF 25WV		
C69			CE04KW0J331M	ELECTRO 330UF 6.3WV		
C70 ,71			CF92FV1H102J	MF 1000PF J		
C72 ,73			CE04KW1E4R7M	ELECTRO 4.7UF 25WV		
C74 -76			CE04KW1A101M	ELECTRO 100UF 10WV		
C77			CF92FV1H104J	MF 0.10UF J		
C78			CE04KW1A101M	ELECTRO 100UF 10WV		
C79			C91-0769-05	CERAMIC 0.01UF K		
C81			CK45FF1H103Z	CERAMIC 0.010UF Z		
C82			CK45FF1H103Z	CERAMIC 0.010UF Z		
CN1			E10-2903-05	FLAT CABLE CONNECTOR		
CN2			E10-2904-05	FLAT CABLE CONNECTOR		
CN3			E10-1507-05	FLAT CABLE CONNECTOR		
L1			L40-1001-17	SMALL FIXED INDUCTOR(10UH,K)		
L2			L32-0355-05	OSCILATING COIL		

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L3			L19-0067-05	TRANSFORMER FOR CONVERTER		
X1			L77-1164-05	CRYSTAL RESONATOR		
X2			L78-0218-05	RESONATOR		
R116			RS14KB3D101J	FL-PROOF RS 100 J 2W		
VR1 ,2			R12-3128-05	TRIMMING POT.(22K)		
VR3 ,4			R12-3126-05	TRIMMING POT.(10K)		
S1 -10			S40-1064-05	PUSH SWITCH		
D1			HZS30N(B)	ZENER DIODE		
D1			RD30ES(B)	ZENER DIODE		
D2			HZS6.2N(B2)	ZENER DIODE		
D2			RD6.2ES(B2)	ZENER DIODE		
D3 -8			S5566B	DIODE		
D9 -17			HSS104	DIODE		
D9 -17			1SS133	DIODE		
D18 -22			HSS104A	DIODE		
D18 -22			1SS131	DIODE		
D23			1SV147	VARISTOR		
D25 ,26			HSS104	DIODE		
D25 ,26			1SS133	DIODE		
FL1		*	FIP9KM5	FLUORESCENT INDICATOR TUBE		
IC1			LM2940CT-5.0	IC(LOW VOLTAGE REGULATOR)		
IC2			UPC7905HF	IC(VOLTAGE REGULATOR/ -5V)		
IC3			NJM4565D	IC(OP AMP X2)		
IC4		*	UPD75212ACW-214	IC(MICROPROCESSOR)		
IC5			CXA1244S	IC(SERVO SIGNAL PROCESSOR)		
IC6			CXA1081S	IC(RF AMP)		
IC7			TC74HCU04AP	IC(CMOS INVERTER)		
IC8			TC74HC00AP	IC(QUAD 2-INPUT NAND GATE)		
IC9			NJM4565D	IC(OP AMP X2)		
IC10			CXD1167Q	IC(DIGITAL SIGNAL PROCESSOR)		
IC11			TC4066BP	IC(ANALOG/ DIGITAL SW)		
IC12		*	PD0060	IC		
IC13			TC74HC157AP	IC(QUAD 2-CHANNEL MULTIPLEXER)		
IC14		*	UPD6376CX	IC(D/A CONVETER)		
IC15			TC4052BP	IC(4CH MPX/DE-MPX)		
IC16			NJM4565L	IC		
Q1			2SA954(L,K)	TRANSISTOR		
Q2			2SA1426	TRANSISTOR		
Q3			DTC124ES	DIGITAL TRANSISTOR		
Q4			2SA733(A)(Q,P)	TRANSISTOR		
Q4			2SA933S(Q,R)	TRANSISTOR		
Q5			2SA1534A	TRANSISTOR		
Q6			DTC124ES	DIGITAL TRANSISTOR		
Q7			2SA1534A	TRANSISTOR		
Q8			DTA124ES	DIGITAL TRANSISTOR		
Q9			STA341M	TRANSISTOR		
Q10			DTC124ES	DIGITAL TRANSISTOR		
Q11			2SC1740S(Q,R)	TRANSISTOR		
Q11			2SC945(A)(Q,P)	TRANSISTOR		
Q12 ,13			2SD1266	TRANSISTOR		
MECHANISM (X92-1510-00)						
1	3A	*	A10-2713-01	CHASSIS		
5	2B	*	A11-0682-08	SUB CHASSIS		

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6	1A	*	A11-0683-03	SUB CHASSIS		
11	1B		D10-2325-04	ROD		
12	3A	*	D10-2433-03	SLIDER		
13	1A	*	D10-2434-04	ROD		
14	2A	*	D13-0876-04	GEAR		
15	2A	*	D13-0877-04	GEAR		
16	2A	*	D13-0878-03	GEAR		
17	2B	*	D13-0879-08	GEAR		
18	1B	*	D13-0880-08	GEAR		
19	2B	*	D13-0881-08	GEAR		
20	3A	*	D15-0309-04	PULLEY ASSY		
21	2A	*	D16-0301-05	BELT		
22	1A	*	D23-0265-03	RETAINER		
30	2B	*	E31-7592-08	WIRING HARNESS		
31	3B	*	E31-7595-05	FLAT CABLE		
35	2B	*	G01-2474-08	COMPRESSION SPRING		
36	2B	*	G01-2475-08	COMPRESSION SPRING		
40	2B	*	J02-1057-05	INSULATOR		
41	1A	*	J11-0164-03	CLAMPER		
42	2A	*	J99-0083-01	TRAY		
A		*	N09-2720-05	TAPTITE SCREW (2.6X8)		
B			N35-2005-46	BINDING HEAD MACHINE SCREW		
C			N39-2025-46	PAN HEAD MACHINE SCREW		
D		*	N09-2769-05	MACHINE SCREW		
E			N09-1522-05	SET SCREW (3X8)		
F			N09-2705-05	MACHINE SCREW		
G		*	N86-2604-46	BINDING HEAD TAPTITE SCREW		
46	2B		S33-1022-05	LEVER SWITCH		
50	1A	*	T50-1054-04	YOKE		
51	1A	*	T99-0503-05	MAGNET		
DM	2B	*	A11-0678-15	DISC MOTOR ASSY		
FM	2B	*	T42-0566-05	FEED MOTOR		
LM	3A	*	T42-0567-05	LOADING MOTOR		
PU	1B	*	T25-0009-05	OPTICAL PICKUP HEAD		

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SPECIFICATIONS

Format

Type	Compact disc player
Read system	Non-contact optical pickup
Rotational speed	About 200 to 500 rpm

Audio

Frequency response	20Hz ~ 20kHz +1dB, –2.0dB
Signal-to-noise ratio	More than 90dB
Wow flutter	Below measurable limit

General

Dimensions	270 W x 70 H x 250 D (mm)
Weight	2.0kg

Note : KENWOOD follows a policy of continuous advancements in development. For this reason specifications may be changed without notice.

Note :
Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the U.S.A. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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