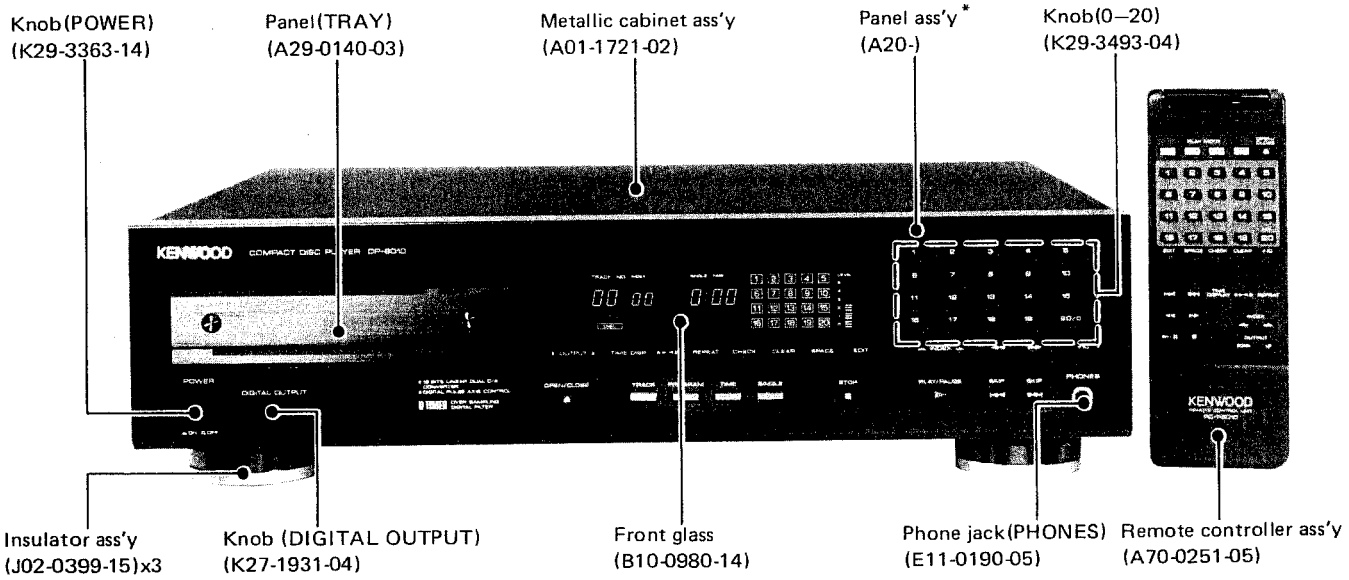
COMPACT DISC PLAYER

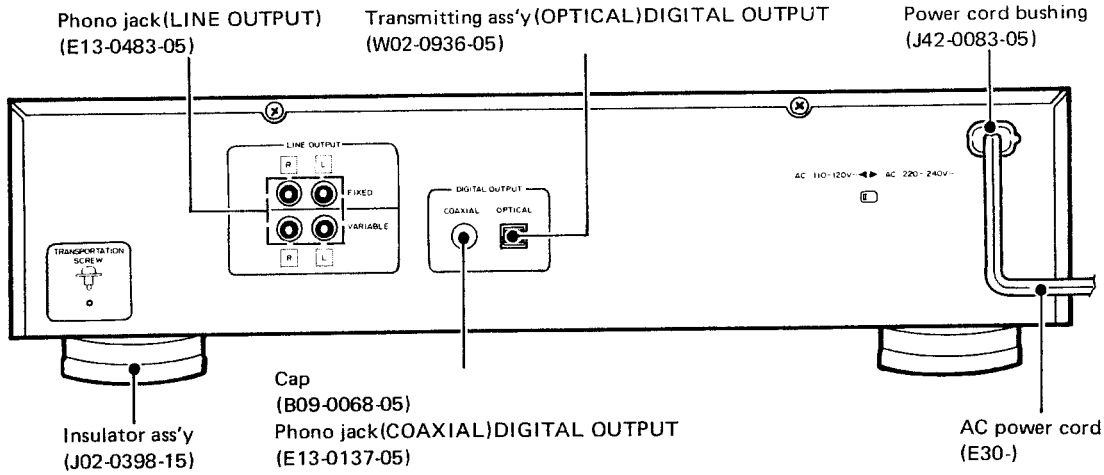
DP-8010

SERVICE MANUAL

KENWOOD

B51-3679-00(O)2503





In complicance with Federal Regulations, following are reproductions of labels on, or inside the product relating to laser product safety.

KENWOOD-Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040. 10, Chapter 1, Subchapter J.

DANGER : Laser radiation when open and interlock defeated. AVOID DIRECT EXPOSURE TO BEAM.

* Refer to parts list on page 77.

DP-8010

CONTENTS/BEFORE OPERATION

Contents

Before Operation

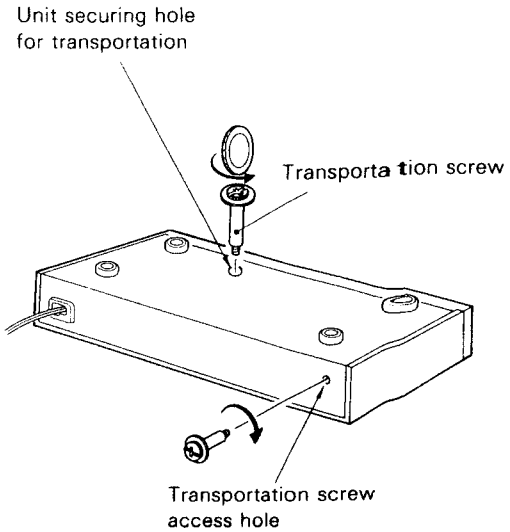
- **Transportation screw**

Before operation, remove the red-headed screw attached to the bottom of the unit used during transportation from the factory. Remove the screw using a coin or screwdriver, etc.

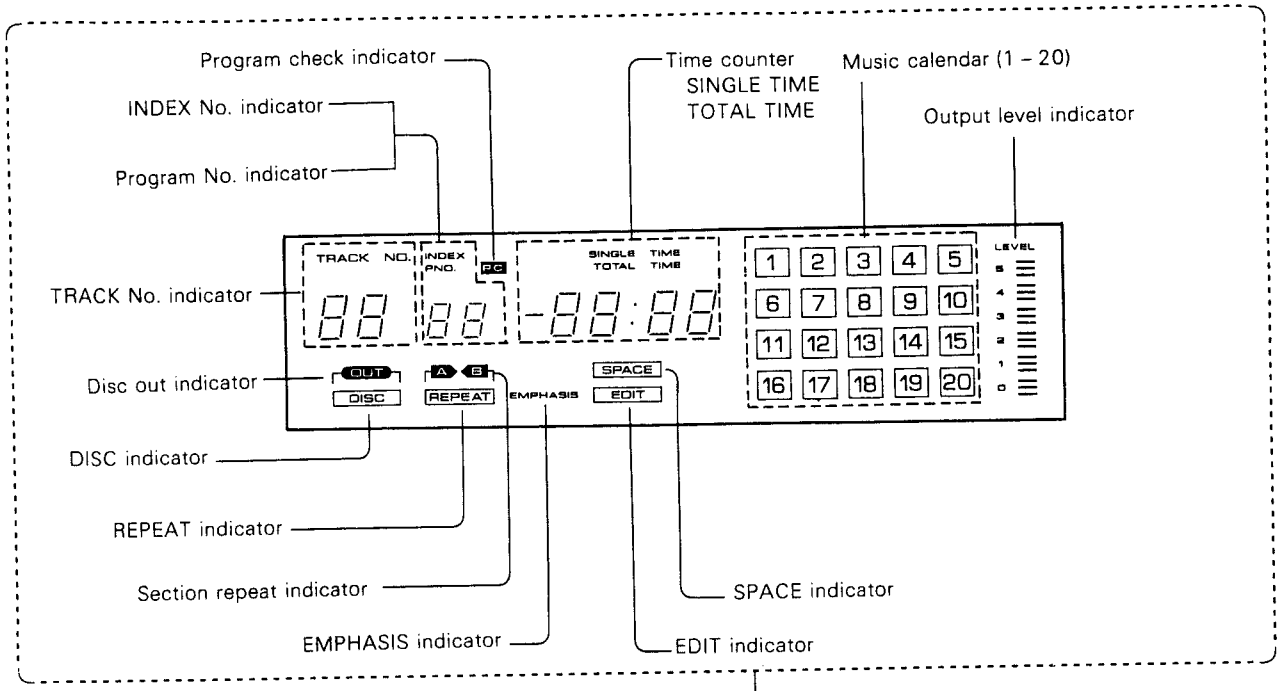
- After removing, retain the screw together with the Warranty card and other documents.
- When the unit is to be transported again, be sure to replace the screw to its original position.

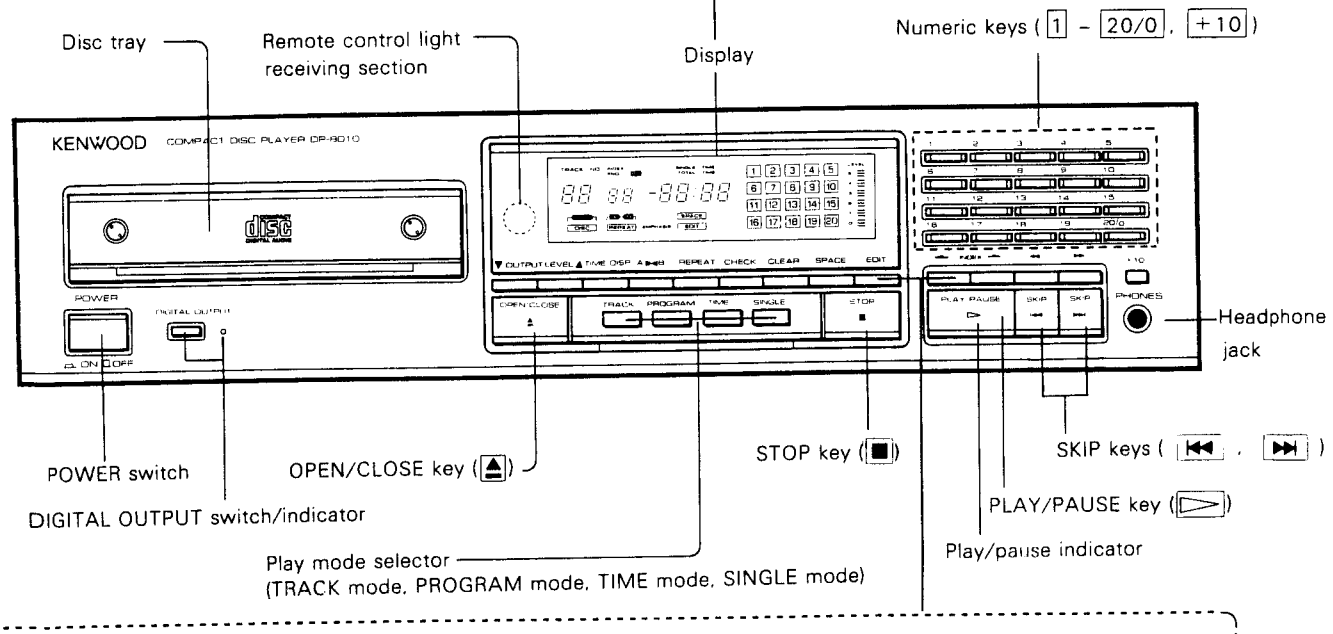
1. Turn ON the power switch when no disc is loaded.
2. Wait a few seconds until the disc OUT indicator comes "ON". Then turn "OFF" the power.

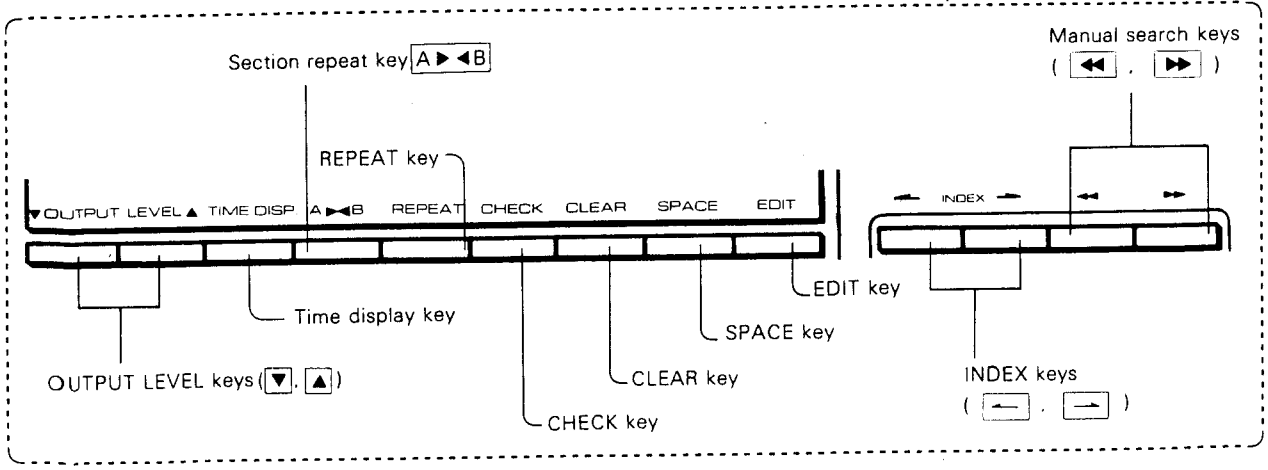
3. Firmly tighten the transportation screw.



CONTROLS AND INDICATORS



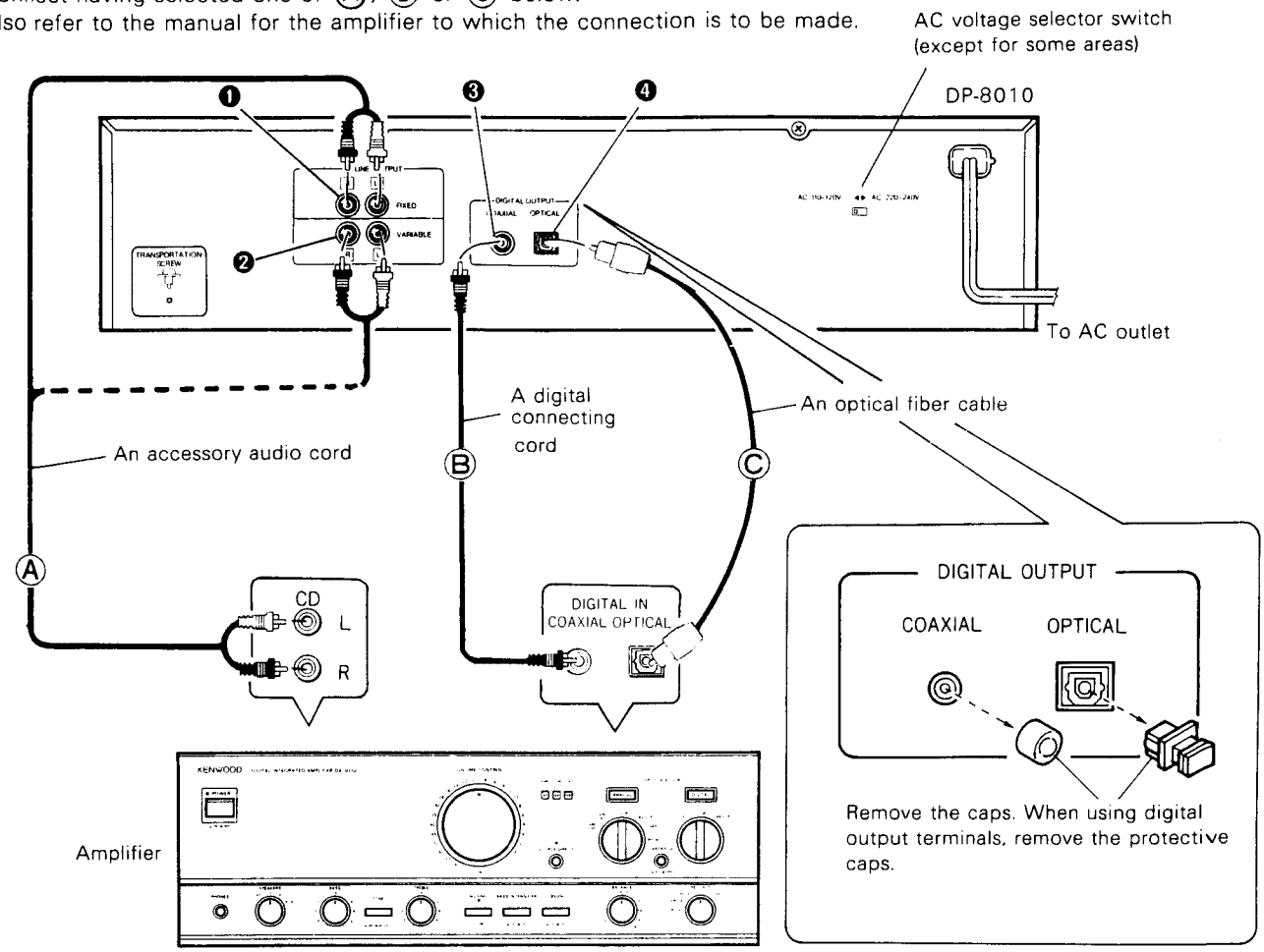




DP-8010

SYSTEM CONNECTIONS

Do not put the plug into the socket until the connecting is completed.
Connect having selected one of Ⓐ, Ⓑ or Ⓒ below.
Also refer to the manual for the amplifier to which the connection is to be made.



■ Conventional amplifier connection (Ⓐ)

Connect output terminal (LINE OUTPUT) ❶ or ❷ to the CD input terminal of the amplifier with the accessory audio cord supplied.

■ Connection to an amplifier equipped with digital input (Ⓑ or Ⓒ)

Connect COAXIAL input terminal of the amplifier to the DIGITAL OUTPUT COAXIAL ❸ with a digital cord, or connect OPTICAL input terminal of the amplifier to the DIGITAL OUTPUT OPTICAL ❹ with an optical fiber cable.

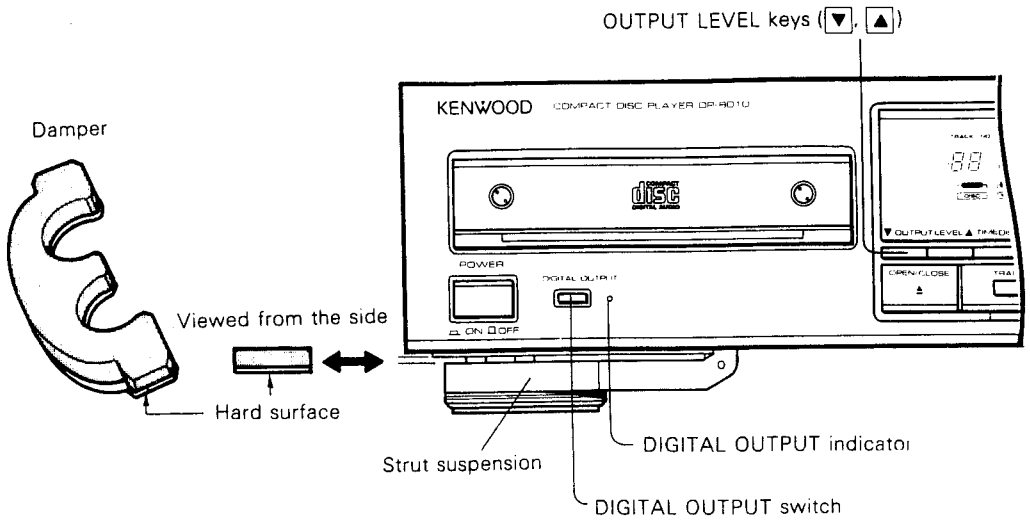
❶ Fixed output (FIXED):
Output voltage is fixed to 2 Vrms. Use these stereo output jacks for connection to a typical amplifier or receiver.

❷ Variable output (VARIABLE)
The output level of the head phones and the VARIABLE output level can be changed simultaneously by means of the OUTPUT LEVEL keys on the front (▼, ▲) or remote control. The output levels are indicated on the display. Use this when you want to match the output levels with other equipment.

❸ DIGITAL OUTPUT COAXIAL
This terminal is for outputting the audio signals in the original digital code. Do not connect it to anything other than the digital input terminal of the amplifier because this could risk damaging the amplifier and speaker.

❹ DIGITAL OUTPUT OPTICAL
This terminal is for converting and outputting the audio signals from digital to optical.
Connect it to the digital amplifier attached to the optical input terminal.

SYSTEM CONNECTIONS



Strut suspension adjustment

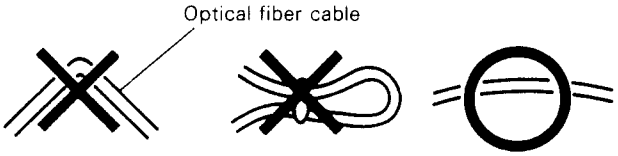
Dampers are provided on the 4 legs of this unit for the strut suspension (see figure above). The suspension can be adjusted by attachment or removal of these dampers. Use them if you feel they are required for sound quality.
Turn the unit over when attaching or removing the dampers. We recommend that you do not place other components on top of this unit as it will impair the suspension effect.

DIGITAL OUTPUT switch

- When using the DIGITAL OUTPUT terminal on the rear side, press the switch shown in the above diagram to get the indicator to illuminate.
- When using the LINE OUTPUT terminal, set the DIGITAL OUTPUT switch to OFF (turn off the indicator).

■ Connecting optical fiber cable

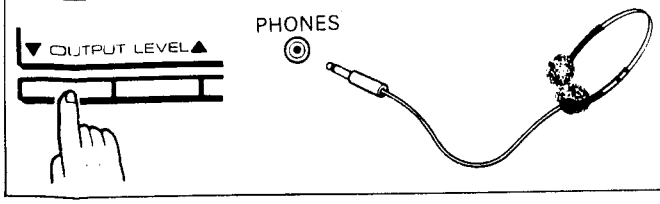
1. **When connecting the optical cable, insert it straight until you hear it click into place.**
2. **Never bend or tie the optical fiber cable.**



3. **Not all optical cables available on the market can be used. If you cannot connect up, consult the store where you bought it from or your nearest sales outlet.**

■ Connecting power cord

It is useful to connect the power cord for this unit to the linking power socket (SWITCHED) of an amplifier. (Except for some areas)



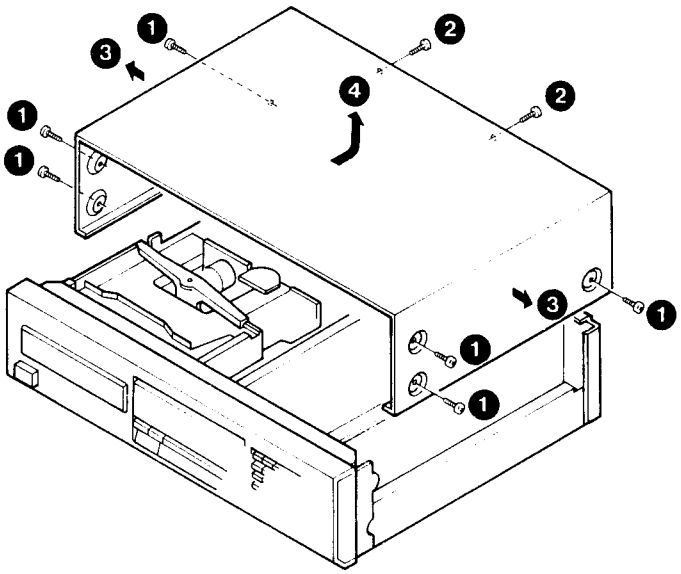
Using stereo headphones

Plug the stereo headphone into the PHONES terminal and adjust with the OUTPUT LEVEL keys ▼ ▲ to get the desired volume.

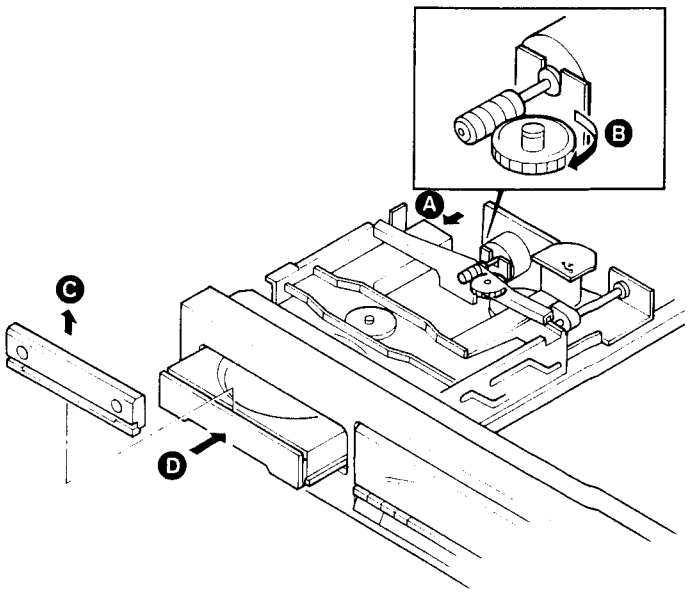
DISASSEMBLY FOR REPAIR

1. Removing the mechanism

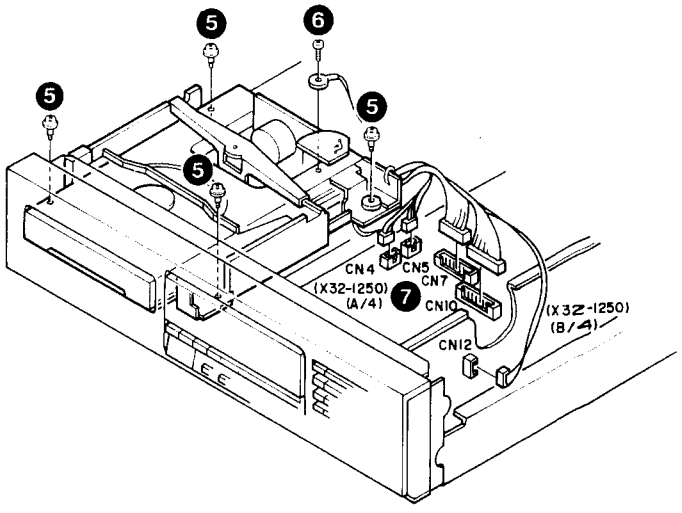
1. Remove the six screws (❶) at the both sides of the case and the two screws (❷) at the rear, and take out the case in the direction of arrow (❹) while holding slightly open the both deep sides of the case in the directions of arrows (❸).



2. When the gear which is moved through the worm from the clamp DC motor (M1) is slowly rotated in the direction of arrow (Ⓑ), the clamp mechanism rises. Next, push the left rear portion of the tray in the direction (arrow (Ⓐ)) of the front panel, and the tray will come out forwards.
   Unless the tray comes out forwards even by pushing, it can be assumed that the clamp mechanism is not undone sufficiently. Therefore, rotate the said gear once again in the direction of arrow (Ⓑ) as shown on the right.
3. Detach the panel by slowly pushing it up in the direction of arrow (Ⓒ) from below.
   Then, push back the tray slowly to its original position in the direction of arrow (Ⓓ).



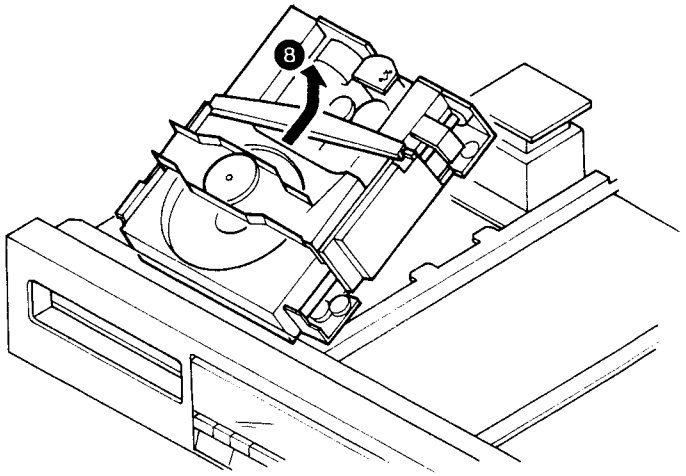
4. Remove the four screws (❺) fixing the mechanism and remove the one GND screw (❻).
5. Disconnect the five connectors running out of the mechanism (❼).
   On PC board X32-1250 (A/4) :
   CN4 (GRN) — 4P
   CN5 (WHT) — 4P
   CN7 — 11P
   CN10 — 9P
   On PC board X32-1250 (B/4) :
   CN12 — 2P



DISASSEMBLY FOR REPAIR

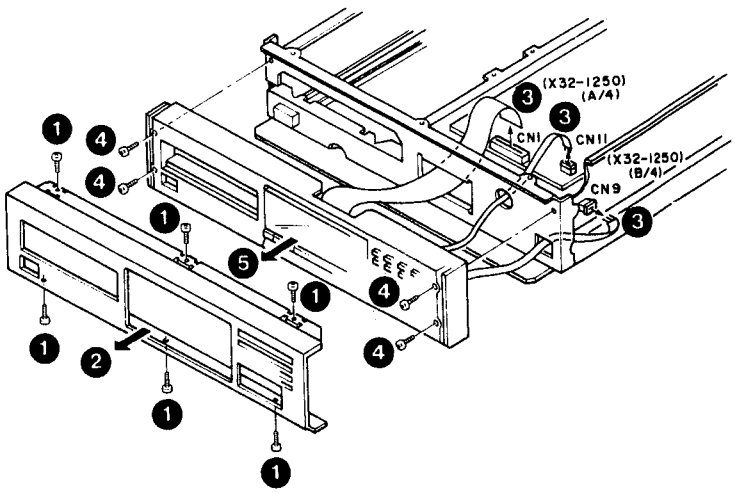
When each connector has been disconnected, hold the clamp bracket with both hands and draw it up slowly in the direction of arrow (❽).

Note: The pickup, unfixed, can move forwards and backwards.
Accordingly, be careful not to hit the objective lens, etc. by fingers. In addition, draw adequate attention not to hit the slanted line portion of the tray surface against the chassis, as this cause damage to the tray surface.



2. Removing the front panel

1. Remove total six screws (❶), three on the upper portion of the front panel and three on the lower portion, then take out the front panel in the direction of arrow (❷).
2. Disconnect the parallel cable running from the display board to a connector (CN1) on the main board, and the cables running to CN11 and CN9 on X32-1250 (B/4) (❸).
3. Remove the four screws (❹) at the both sides of the sub panel and draw out the front panel towards you in the direction of arrow (❺).

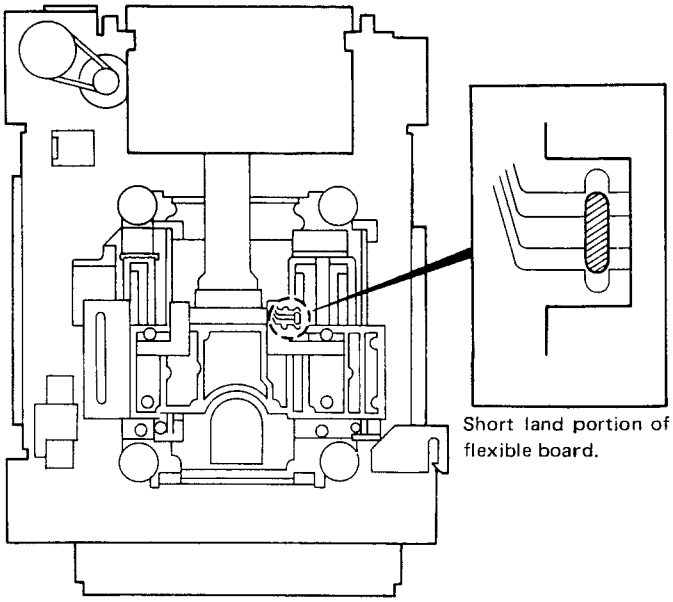


DISASSEMBLY FOR REPAIR

3. Replacement procedure of laser pickup

1. When checking or removing the laser pickup, first make a solder bridge on the short land provided to the side of the laser pickup.
   In addition, as to the new pickup, its flexible board is longer one step, and a solder bridge is made on an additional short land.

Note: When replacing the pickup, after its installation is completed, cut short the flexible board for use.



Short land portion of flexible board.

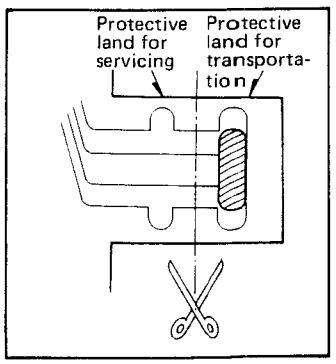
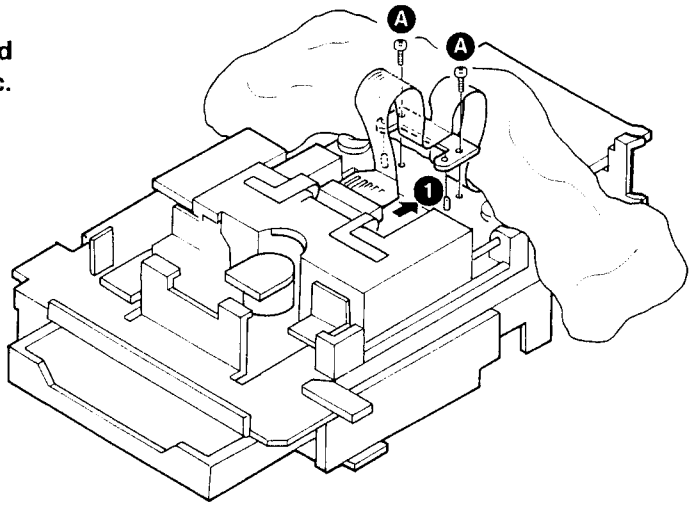


Diagram of flexible board as a service parts

* Following the installation of the new pickup, cut the board along the broken line for use.

2. Draw out the connection flexible board of the laser pickup in the direction of arrow (❶).

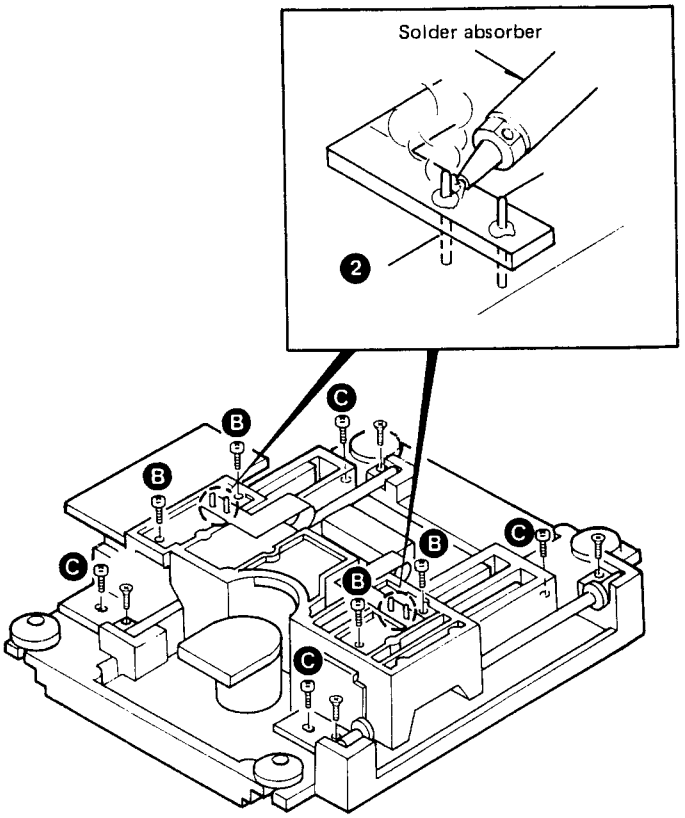
Note: In the replacement work, cover the PC board with a cloth, etc. to protect your fingers, etc. from the soldering face of the RF unit.



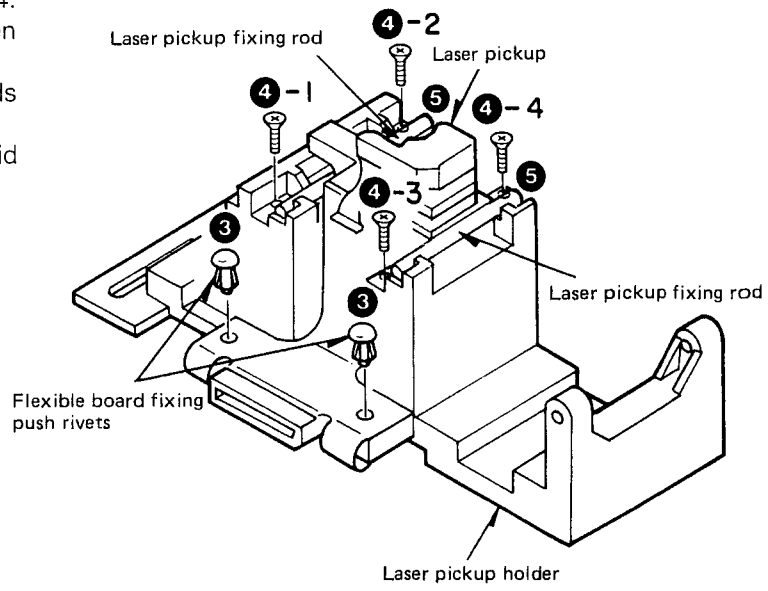
DISASSEMBLY FOR REPAIR

3. Subsequently, unsolder the flexible board and the yoke ass'y. As shown on the right, unsolder between the yoke ass'y pins and the flexible board thoroughly by a solder absorber (❷).

Note: When the reinforcement plate of the flexible board is slowly lifted up, the yoke ass'y pins should not be lifted up together.



4. Remove the two push rivets (❸) fixing the flexible board of the pickup from the upper side of the mechanism.
5. Remove the four flat head screws ((❹)-1 to (❹)-4. fixing the laser pickup itself in numerical order, then pull up the laser pickup slowly.
6. Subsequently, draw out the laser pickup fixing rods (❺) slowly, then install the new pickup.
   Reversely to the removal at step 5., tighten the said screws (❹)-4 to (❹)-1 to secure the rods.

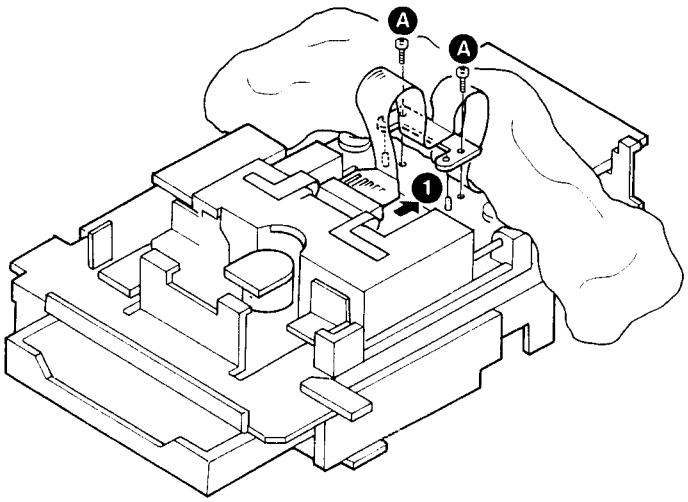


DISASSEMBLY FOR REPAIR

4. Replacement procedure of yoke ass'y

1. In the sequence exposed in "3. Replacement procedure of laser pickup", disconnect the flexible cord (❶).
2. As shown on the right, remove the two screws (Ⓐ) of the acryl plate fixing the flexible cord.

Note: In this case, be sure to make a solder bridge to prevent the static breakdown.



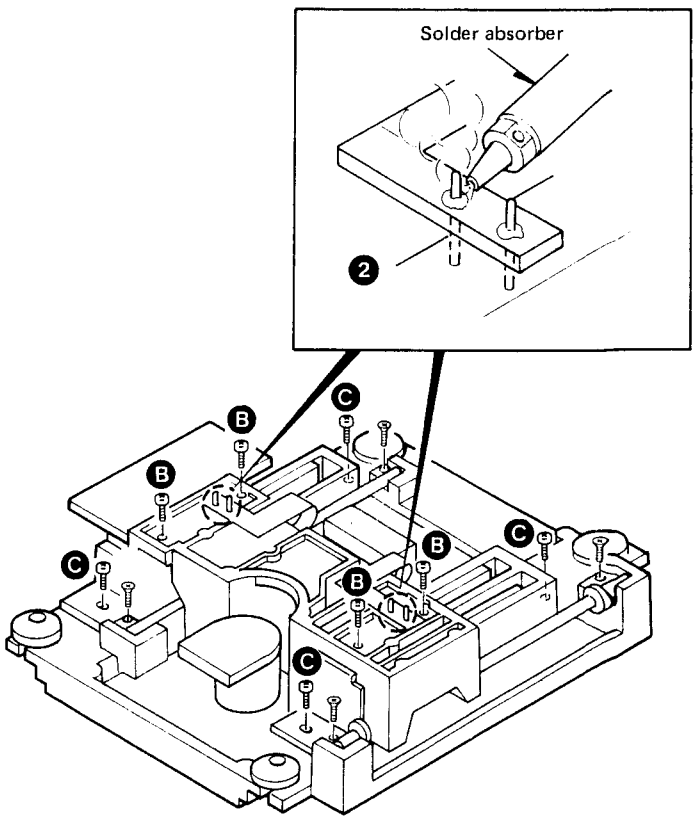
3. Unsolder thoroughly at four points the left and right yoke assi'es of the flexible board supplied as an accessory to the laser pickup by a solder absorber (❷).

Note: If any pin of yoke ass'y is heated for an extended period of time or is subject to the application of an excessive force, it may be broken or come off.

4. Remove the four screws (Ⓑ) fixing the laser pickup holder and yoke assi'es.
5. Remove the four screws (Ⓒ) at the sensor section yoke ass'y and drive section yoke ass'y.

Note: In each yoke ass'y, a coil magnet is incorporated. If disassembled, a load can be applied in the sliding action or unwanted matter (screw, lead cutting dusts, etc.) can adhere to the magnet.

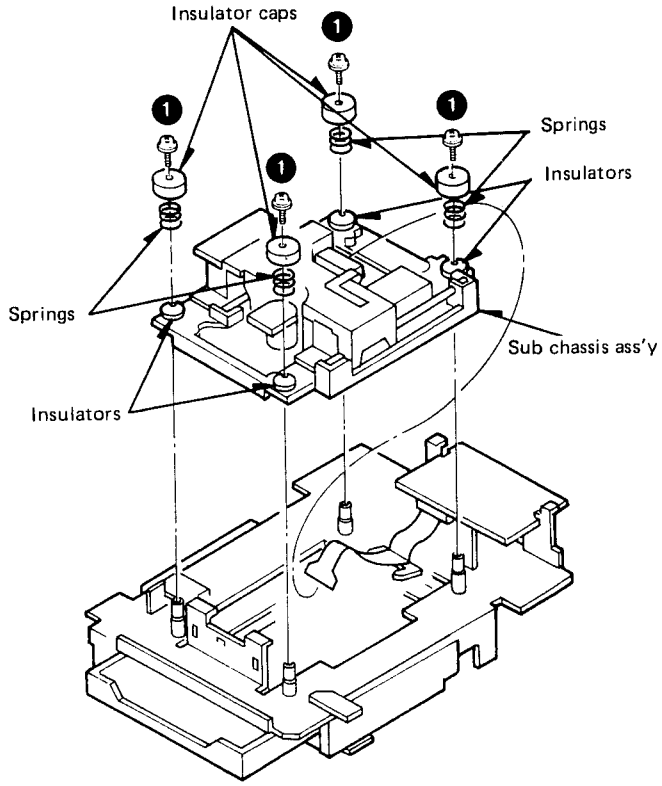
Moreover, after completion of repair, also check whether or not unwanted matters such as screw, lead cutting dusts, etc. adhere to the magnet.



DISASSEMBLY FOR REPAIR

5. Removing the sub chassis and the insulators

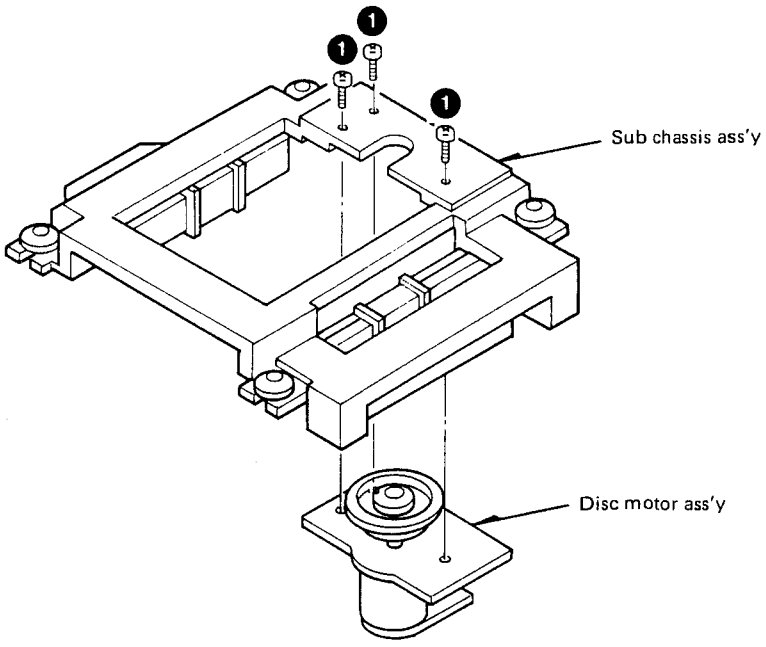
1. As shown on the right, remove the four tapping screws (❶), and the laser pickup section will be detached together with the sub chassis ass'y to which it is installed.



6. Replacing the disc motor

1. Remove the three screws (❶) fixing the sub chassis ass'y, then replace the disc motor ass'y.

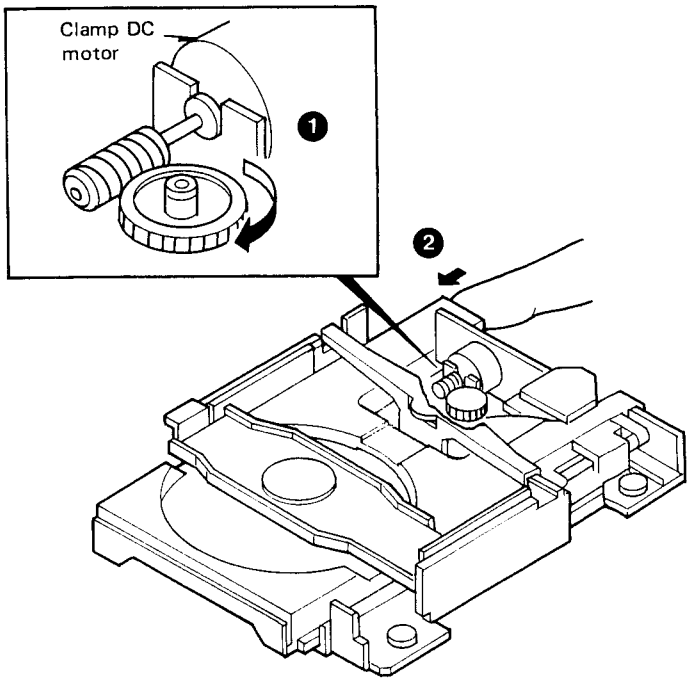
Note: When installing the new disc motor, be sure to positively mount it in alignment with the two grooved portions of the sub chassis ass'y.



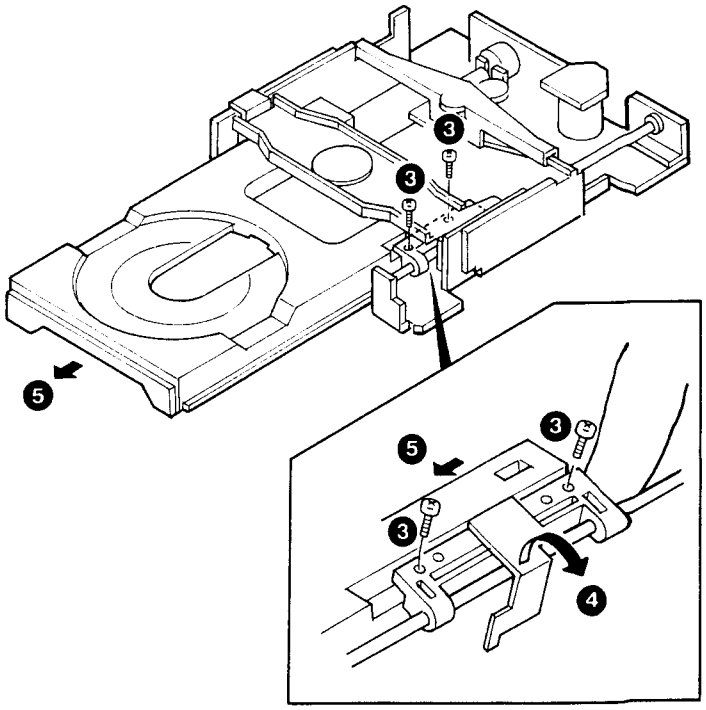
DISASSEMBLY FOR REPAIR

7. Removal and replacement procedure of tray ass'y

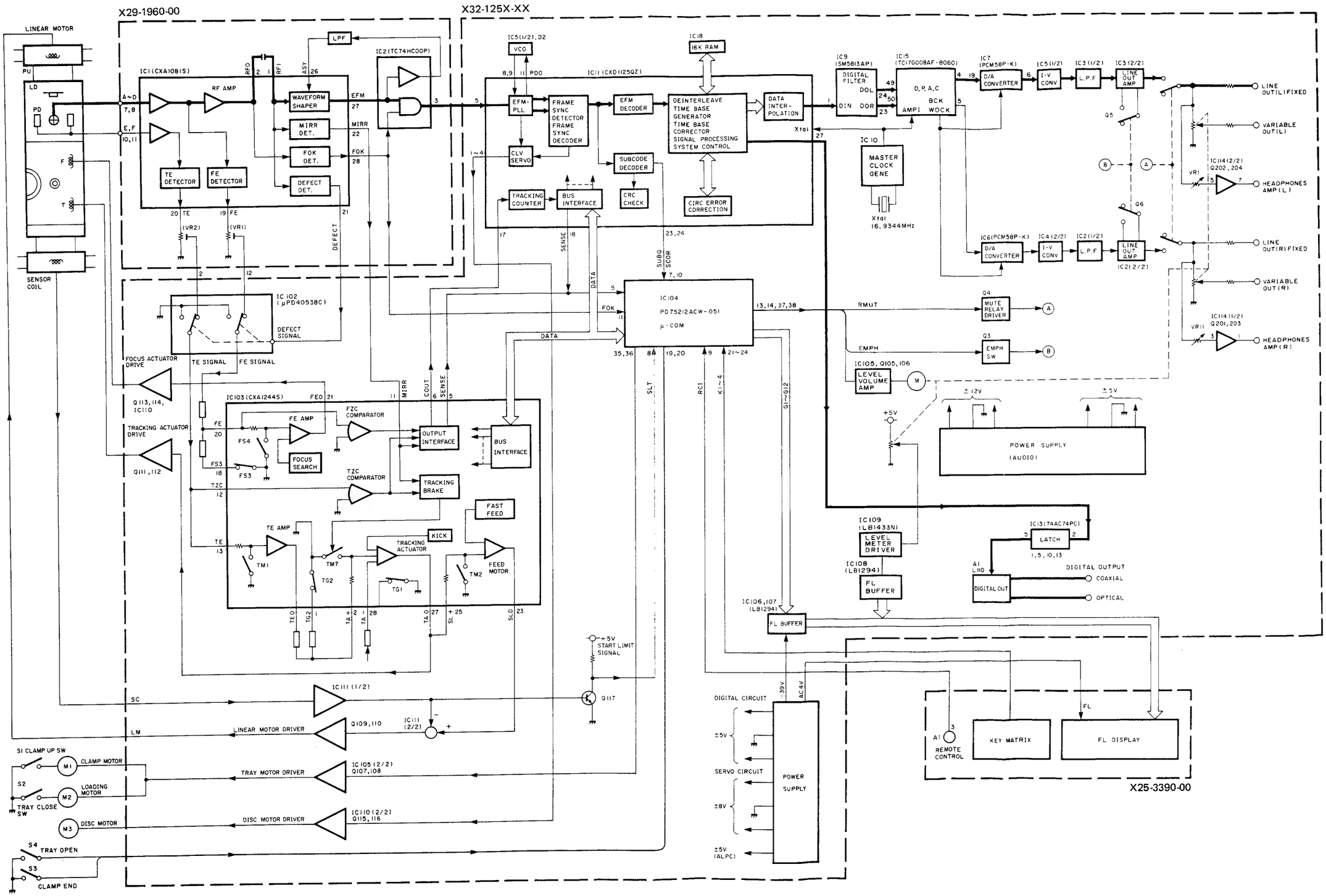
1. When drawing out the tray from the clamped state, rotate the gear slowly by finger in the direction of arrow (❶) as shown on the right, and the tray will be released from the clamped state so that the tray can be opened.
2. Push the tray in the direction of arrow (❷) from its rear and draw it out towards you.



3. Remove the two screws (❸) of the sliding section fixing the tray.
4. Put down the holder in the direction of arrow (❹) and pull the tray in the direction of arrow (❺), and the tray will be detached.



BLOCK DIAGRAM



CIRCUIT DESCRIPTION

1. Description of components

1–1. OPERATION UNIT (X25-3390-00)

Ref. No.	Part No.	Use/Function	Operation/Condition/Compatibility
IC1	TD62003AP	Transistor array	Drives each mode lamp/LED.
IC2	TC74HC174F	D flip-flop	Controls each mode lamp/LED.
A1	W02-0973-05	Remote control light receiver	Converts the infrared remote control signal into a logic signal.

1–2. CONTROL CIRCUIT UNIT (X29-1960-00)

Ref. No.	Part No.	Use/Function	Operation/Condition/Compatibility
IC1	CXA1081S	RF amplifier	Generation of focus error signal, generation of tracking error signal, generation of RF signal and its phase correction, and auto asymmetry correction.
IC2	TC74HC00P	NAND gate	EFMT signal waveform detection.
Q1	2SC945(A)(Q,P) 2SC1740S(Q,R)	Bias switch	Focus error amplifier bias select switch.
Q2	2SA1426	LD switch	LD power switch, which is controlled by pin 5 (LD) of IC1.

1–3. CD PLAYER UNIT (X32-125X-XX) 0-11 : K,P,X,T,E 0-21 : M

Ref. No.	Part No.	Use/Function	Operation/Condition/Compatibility
IC1	M5218P NJM4560D	Operation amplifier	Error amplifier of ±12V regulated power supply.
IC2	NJM5532D-D	Operation amplifier	(1/2) : Rch output amplifier, (2/2) : Rch low pass buffer.
IC3	NJM5532D-D	Operation amplifier	(1/2) : Lch low pass buffer, (2/2) : Lch output amplifier.
IC4	NJM5532D-D	Operation amplifier	(1/2) : Error amplifier of ±5V regulated power supply (for DAC). (2/2) : I-V converter (Rch).
IC5	NJM5532D-D	Operation amplifier	(1/2) : I-V converter (Lch). (2/2) : Error amplifier of ±5V regulated power supply (for DAC).
IC6	PCM58P	D/A converter	Rch : 18-bit serial input D/A converter, which converts the digital form of serial data into an analog form.
IC7	PCM58P	D/A converter	Lch : 18-bit serial input D/A converter, which converts the digital form of serial data into an analog form.
IC8	M5218P NJM4560D	Operation amplifier	(1/2) : Error amplifier of +5V regulated power supply (for IC9, IC10 and IC15). (2/2) : Error amplifier of –5V regulated power supply (for IC14(1/2) VCO).
IC9	SM5813AP	Digital filter	8x over-sampling digital filter.
IC10	TC74HCU04P	Clock oscillator	Master clock oscillation (16.9344MHz).
IC11	CXD1125Q CXD1125QZ	Digital signal processing LSI	EFM data demodulation/correction/interpolation, PLL CLV servo, and digital out.
IC12	CXK5816SP-12L	S-RAM	Signal processing 16K static RAM.
IC13	74AC74PC	Digital out switch	Digital out ON/OFF selection, and digital out data DPAC.
IC14	M5218P NJM4560D	Operation amplifier	(1/2) : PLL compensation circuit (LPF + amplifier). (2/2) : CLV compensation circuit (LPF + level shifter).
IC15	TC17G008AF-8060	DPAC	For details, refer to page 44.
IC16	M5F78M05L	3-terminal regulator	+5V regulation (for IC11, IC14 (1/2) and IC12).
IC101	NJM4558D	Operation amplifier	Error amplifier of ±5V regulated power supply.
IC102	µPD4053BC	Analog switch	This receives the flaw detection signal (pin 21 (DEFECT) of IC1 (CXA1081S)). With a flaw, it turns OFF the focus servo and tracking servo to hold the signal prior to the flaw detection. (Pins 10/11 (A/B) : "L" normally, "H" with flaw).
IC103	CXA1244S	Servo IC	Generation of various pulse signals for each of focus, tracking and sled servo controls.
IC104	µPD75212ACW-051	Microprocessor	Display, each key input process and servo IC control.
IC105	NJM4558D	Operation amplifier	(1/2) : For variable level VR drive. (2/2) : For tray motor drive.
IC106~108	LB1294	FL driver	FL tube drive.
IC109	LB1433N	Linear scale level meter IC	Variable VR position display output.

DP-8010

CIRCUIT DESCRIPTION

Ref. No.	Part No.	Use/Function	Operation/Condition/Compatibility
IC110	NJM4558D	Operation amplifier	(1/2) : For focus actuator drive. (2/2) : For disc motor drive.
IC111	NJM4558D	Operation amplifier	(1/2) : Velocity sensor coil signal amplification. (2/2) : For linear motor drive.
IC112	M51951ASL	Reset IC	Generation of reset signal at power ON/OFF.
IC113	LA6500	Operation amplifier	Extension of dynamic range to drive the drive coil of linear motor.
IC114	µPC4570C-A	Operation amplifier	(1/2) : Rch headphone amplifier. (2/2) : Lch headphone amplifier.
Q1,2	2SD1266	Ripple filter	±12V power supply.
Q3	DTC124EN	Digital switch	De-emphasis control switch.
Q4	2SC945(A)(Q,P) 2SC1740S(Q,R)	Driver	Output muting relay drive.
Q5,6	2SC2878(B)	Switch	De-emphasis switch.
Q7,8	2SC3940A	Ripple filter	For ±5V DA converter regulated power supply.
Q9	2SC3940A	Ripple filter	Ripple filter for ±5V regulated power supply.
Q10	2SA1534A	Ripple filter	Ripple filter for –5V regulated power supply.
Q101	2SA1534A	Ripple filter	Ripple filter for +5V power supply.
Q102	2SC3940A	Ripple filter	Ripple filter for –5V power supply.
Q103	2SC3940A	Ripple filter	Ripple filter for +8V power supply (for lamps/LEDs).
Q104	2SA1534A	Ripple filter	Ripple filter for –30V power supply (for FL reference voltage).
Q105	2SA1534A	Driver	Variable VR motor drive.
Q106	2SC3940A	Driver	Variable VR motor drive.
Q107	2SA1534A	Driver	Tray motor drive.
Q108	2SC3940A	Driver	Tray motor drive.
Q109	2SA1534A	Driver	Linear motor drive.
Q110	2SC3940A	Driver	Linear motor drive.
Q111	2SA1534A	Driver	Tracking actuator drive.
Q112	2SC3940A	Driver	Tracking actuator drive.
Q113	2SA1534A	Driver	Focus actuator drive.
Q114	2SC3940A	Driver	Focus actuator drive.
Q115	2SA1534A	Driver	Disc motor drive.
Q116	2SC3940A	Driver	Disc motor drive.
Q117	2SC945(A)(Q,P) 2SC1740S(Q,R)	Switch	Pickup start limit position detection by linear motor speed signal.
Q201,202	2SC3940A	Driver	Headphone amplifier drive.
Q203,204	2SA1534A	Driver	Headphone amplifier drive.

CIRCUIT DESCRIPTION

2. CD player unit (X32-1250-XX)

• Pickup carry circuit by linear motor

The speed sensor generates a voltage proportional to the moving speed of the pickup mount. More, since this voltage is yet low in level, it is amplified at IC111(1/2).

Therefore, the voltage at point Ⓐ becomes the signal standing for the moving speed of the pickup mount. This speed signal is inverted and amplified, and further the drive coil is driven so that the pickup amount is servo-controlled in respect to the moving speed.

The power OP amplifier of IC113 (LA6500) is used to extend the dynamic range of driving the drive coil of the linear motor. The voltage at point Ⓑ serves as the moving speed reference of the pickup amount. In addition, the pickup amount moves at a speed proportional to the voltage at point Ⓑ.

Example: When the voltage at point Ⓑ is 0V, the pickup mount does not move, whereas when it is positive, the pickup mount moves inwards at a speed proportional to that voltage.

The voltage at point Ⓑ is the same as the voltage driving the pickup carry motor in a conventional mechanism and can be represented to a servo block diagram as shown in Figure 2-1, which manifests a direct feedback system.

Thus, if value |A> is sufficiently large, Ⓐ = Ⓑ.

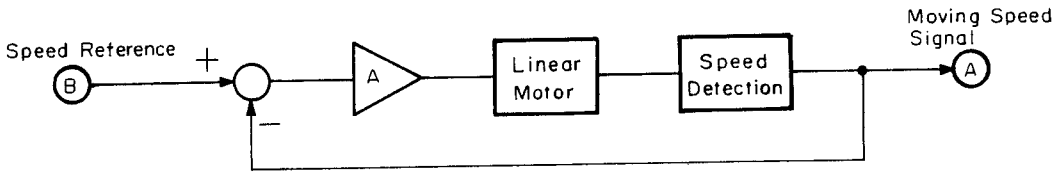


Fig. 2–1

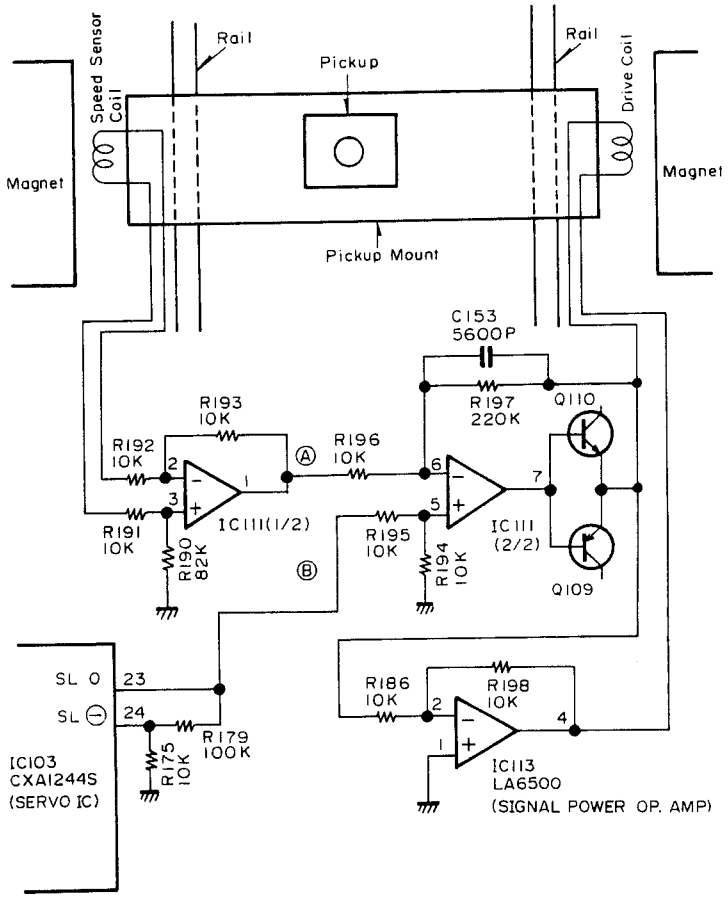


Fig. 2–2 Pickup carry circuit by linear motor

CIRCUIT DESCRIPTION

• D.P.A.C (Digital Pulse Axis Control) circuit

Two different distortions are attendant on the conversion of the digital signal into an analog signal. One is a distortion on the level axis (voltage axis), which is determined mainly by the resolution of the D/A converter, and in case of using a ladder resistor type, by its error.

The other is a distortion on the time axis, which is not so prevailing as to appear on the distortion meter but has great influence on the sound quality. It is the D.P.A.C that is to operate as a circuit to improve this point.

Figure 2-3 shows the error (distortion) on the voltage axis of the D/A converter output for the original sound, and Figure 2-4 shows the error (distortion) on the time axis of the D/A converter output for the original sound.

As seen from this, even with a variation in time axis, there appears a regenerated waveform different from the original sound.

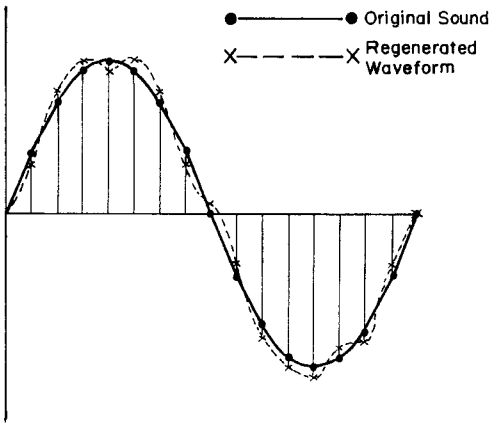


Fig. 2–3 Error (distortion) on voltage axis

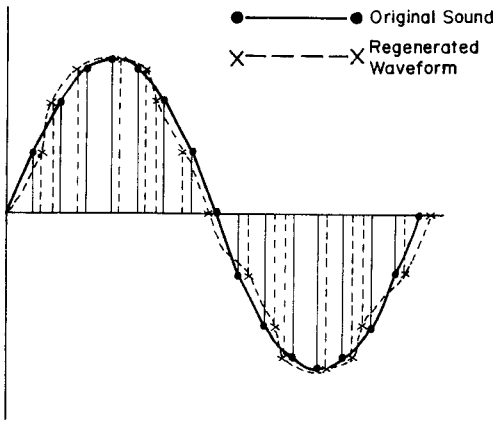


Fig. 2–4 Error (distortion) on time axis

Next, let us deal with the theory of the D.P.A.C operation by a basic D.P.A.C circuit of this time.

Also when the latch signal Ⓐ from the digital filter is disturbed, an accurate latch signal like Ⓒ can be obtained at the rise of the master clock pulse Ⓑ. By virtue of this latch signal, a proper voltage signal is output from the D/A converter.

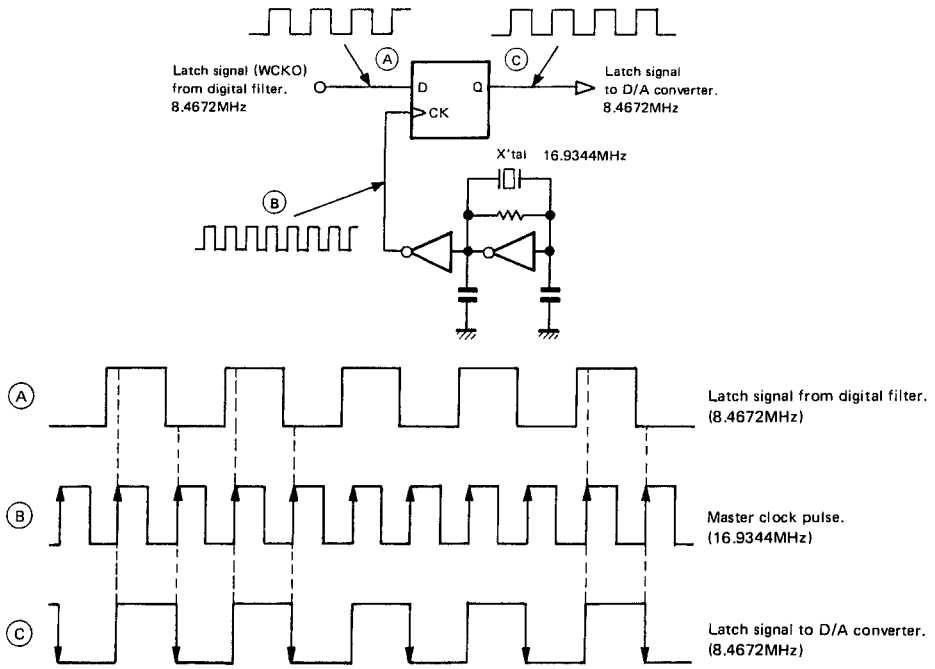


Fig. 2–5 D.P.A.C basic circuit

CIRCUIT DESCRIPTION

Let us show the signal timing in a practical circuit.

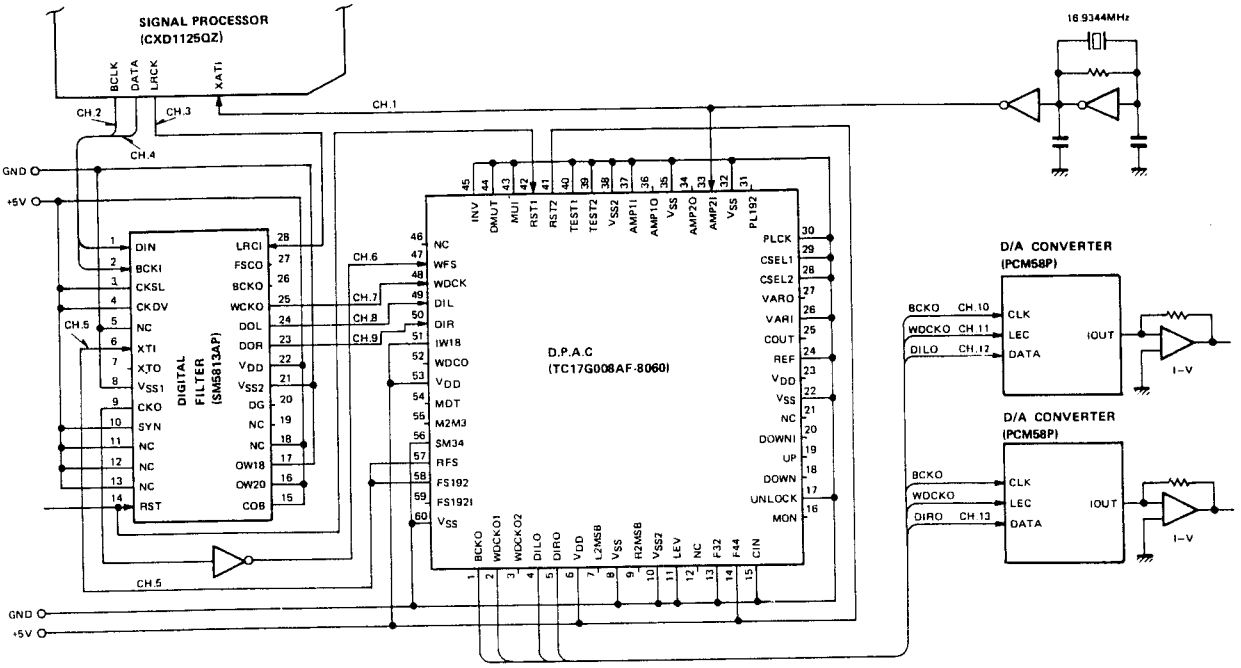


Fig. 2–6

Signal : 1kHz, 0dB (at play)

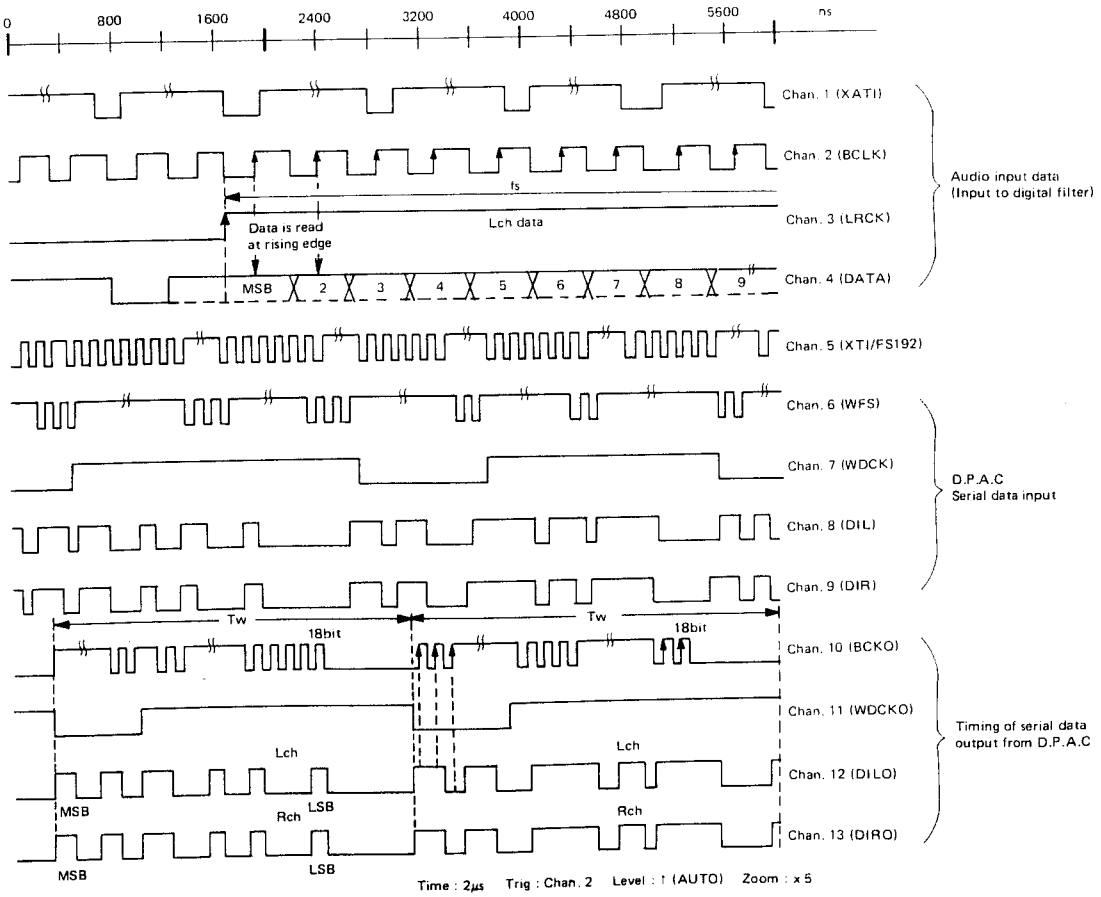
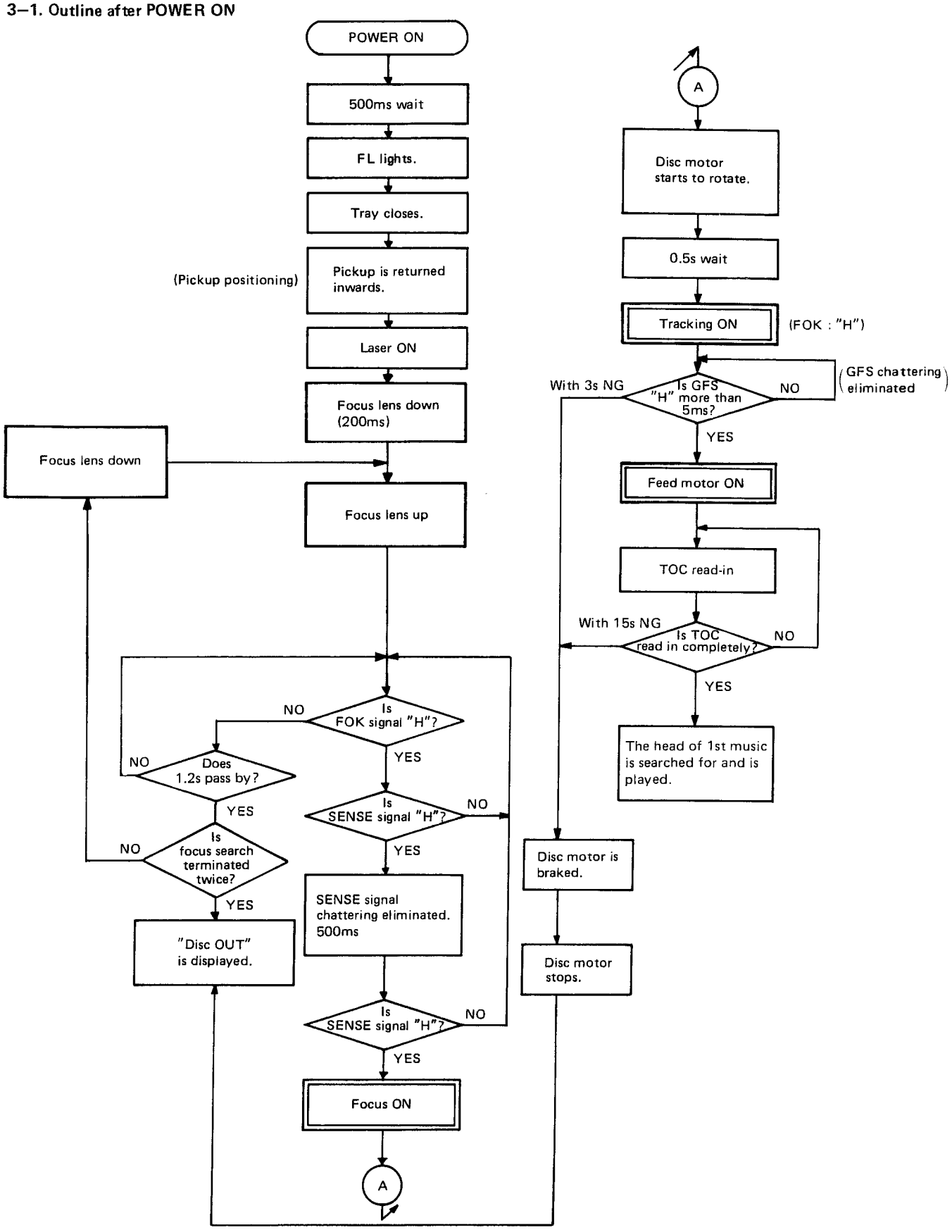


Fig. 2–7 D.P.A.C timing chart

CIRCUIT DESCRIPTION

3. Set Mode Flowchart

3–1. Outline after POWER ON

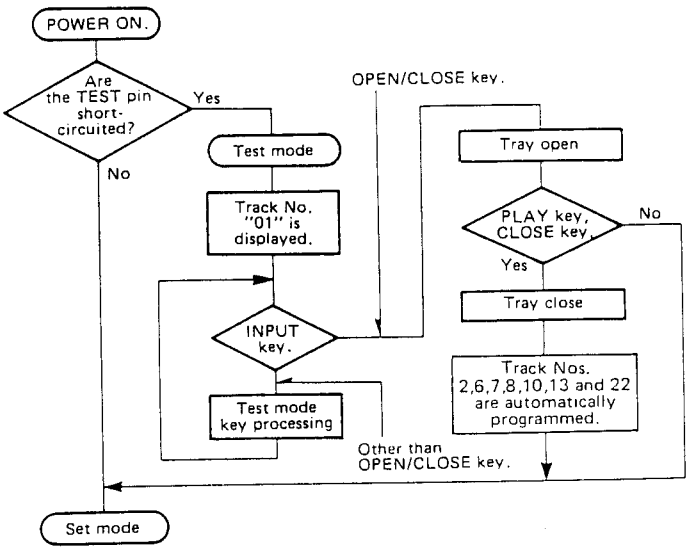


CIRCUIT DESCRIPTION

4. Test mode

With the DP-8010, the microprocessor can be set to test mode by short-circuiting pin 4 and pin 5 of the CD PLAYER UNIT (X32-1250).

Note : "Set mode" shows the normal status.



4-1. Key and functions valid in test mode

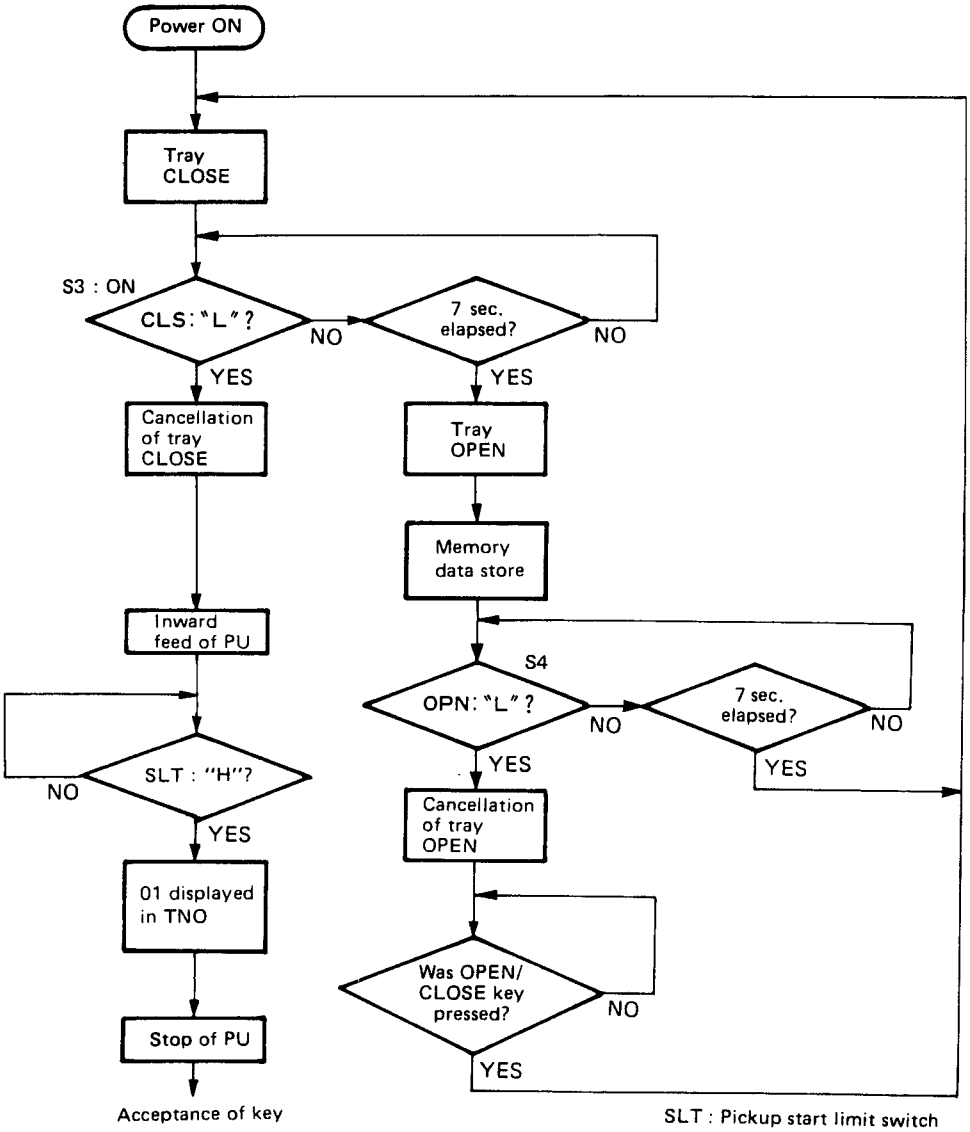
No.	Input key	Function	Track No. display
1	PLAY/PAUSE	(1) Focusing servo ..... ON (2) Tracking servo ..... ON (3) Feed servo ..... ON When the key is pressed in the STOP mode, the servoes are switched ON automatically in the order from (1) to (3).	TRACK NO. 05 ↓ Display for a few seconds after completion of (1), (2) and (3). ↓ Disc Track No. is displayed.
2	CHECK	(1) Focusing servo ..... ON (2) Tracking servo ..... OFF (3) Feed servo ..... OFF	TRACK NO. 03
3	CLEAR	(1) Focusing servo ..... ON (2) Tracking servo ..... ON (3) Feed servo ..... OFF	TRACK NO. 04
4	STOP	(1) Focusing servo ..... OFF (2) Tracking servo ..... OFF (3) Feed servo ..... OFF	TRACK NO. 01
5	REPEAT	(1) Tray ..... Opened (2) Laser ..... ON The REPEAT function is canceled when the tray is closed by pressing the tray. The Track No. display 01	TRACK NO. 02
6	▶▶	In the STOP mode, moves the pickup slightly toward the outer position of disc. When feed servo is ON, sets the track gain to "H".	
7	◀◀	In the STOP mode, moves the pickup slightly toward the inner position of disc. When feed servo is ON, sets the track gain to "L".	
8	Numeric key (0 ~ 9)	Jumps tracks as shown below.	
9	OPEN/CLOSE or +10	When the tray is opened and the closed again in test mode, Track Nos 2, 6, 7, 8, 10, 13 and 22 are automatically programmed. Opening the tray again will cause the unit to enter set mode.	
10	SKIP ▶▶|	Turns all FL display lamps ON.	
11	SKIP |◀◀	Turns all FL display lamps OFF. (except Track No. and levels)	

Key	1	2	3	4	5
Number of tracks	1	4	16	32	1000
Direction	Outer				
Key	6	7	8	9	0
Number of tracks	1	4	16	32	1000
Direction	Inner				

CIRCUIT DESCRIPTION

4–2. Flow chart of test mode

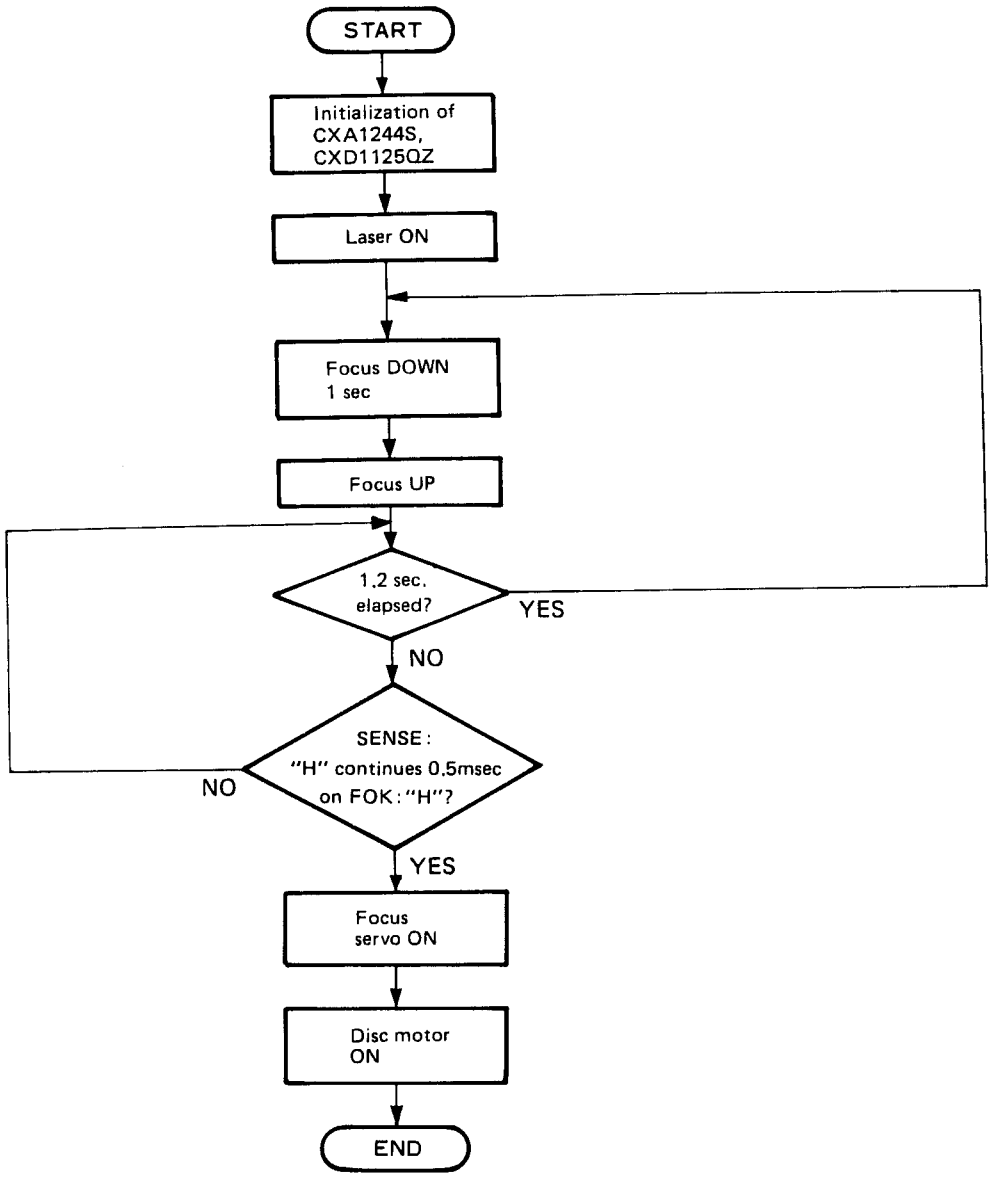
- **Flow chart from tray OPEN status after power ON**



SLT : Pickup start limit switch
CLS : Tray close detect switch
OPEN : Tray open detect switch

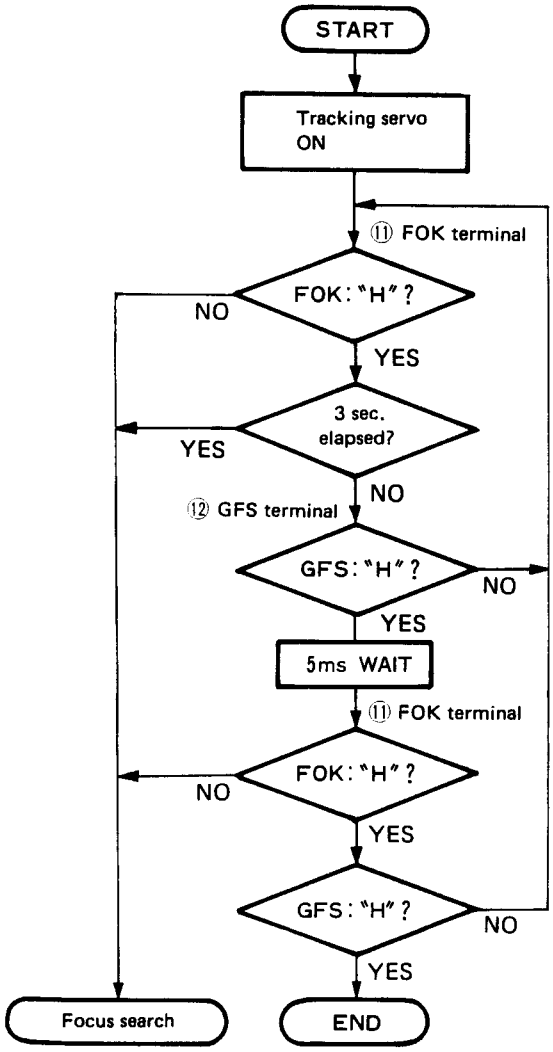
CIRCUIT DESCRIPTION

- Focus search & focus servo ON

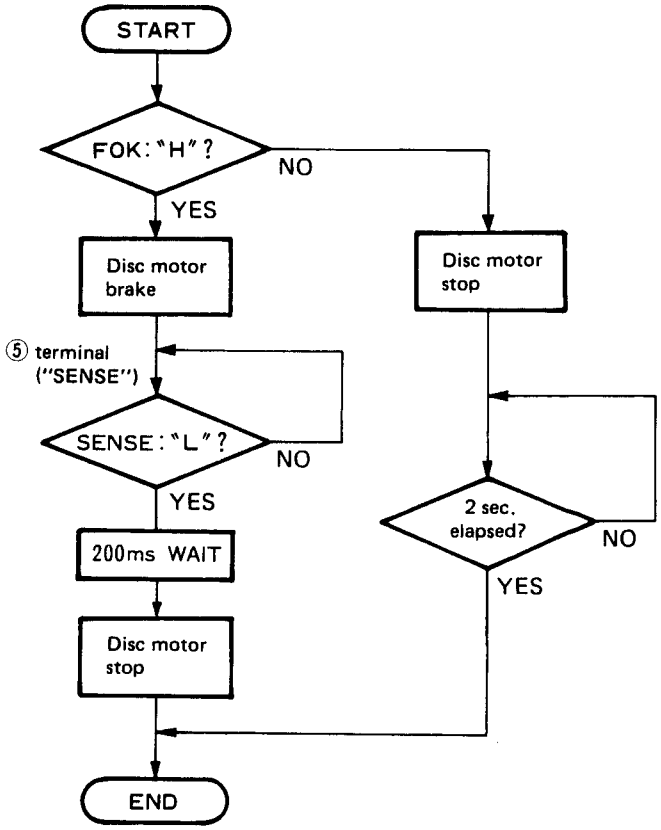


CIRCUIT DESCRIPTION

- Tracking servo ON

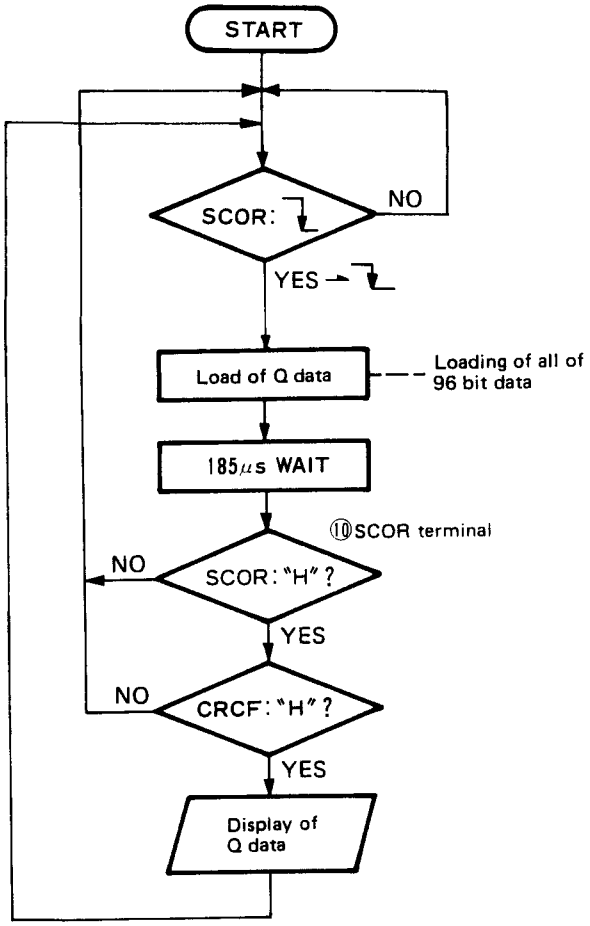


- Disc motor STOP

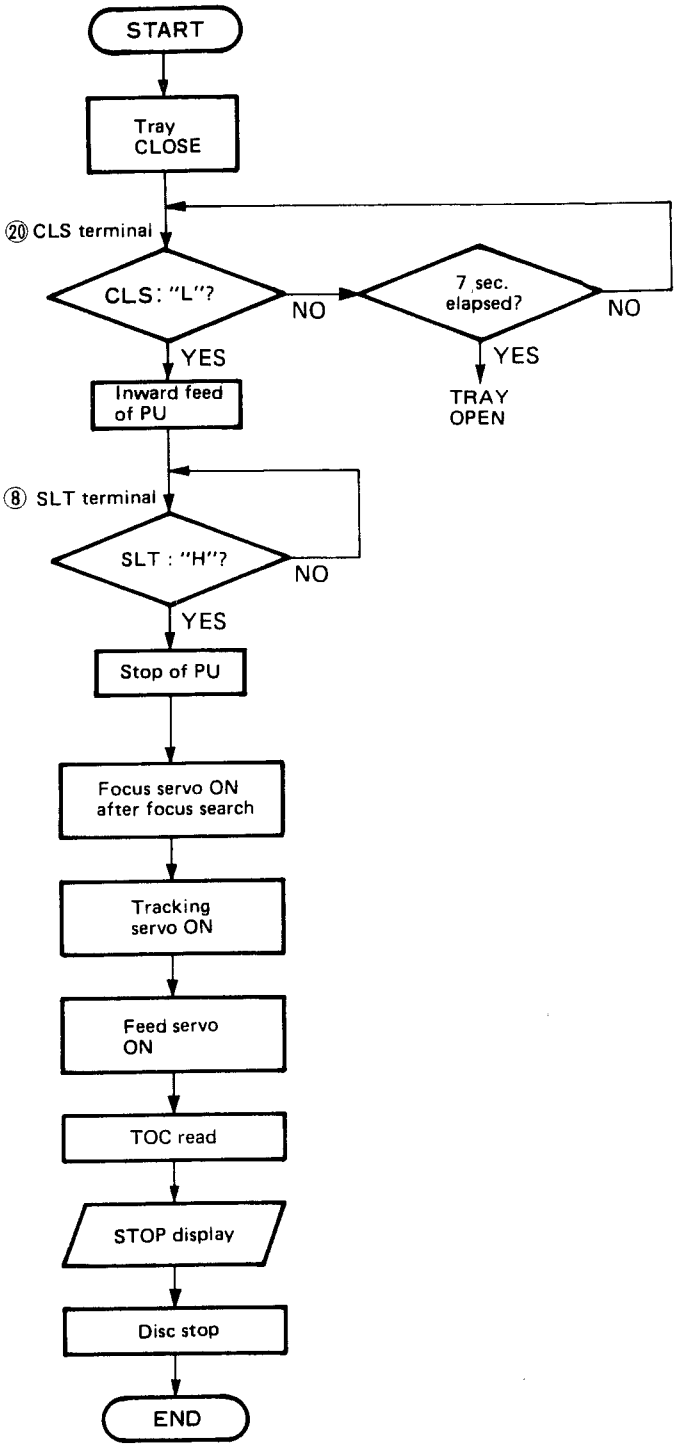


CIRCUIT DESCRIPTION

- From loading of Q data to display



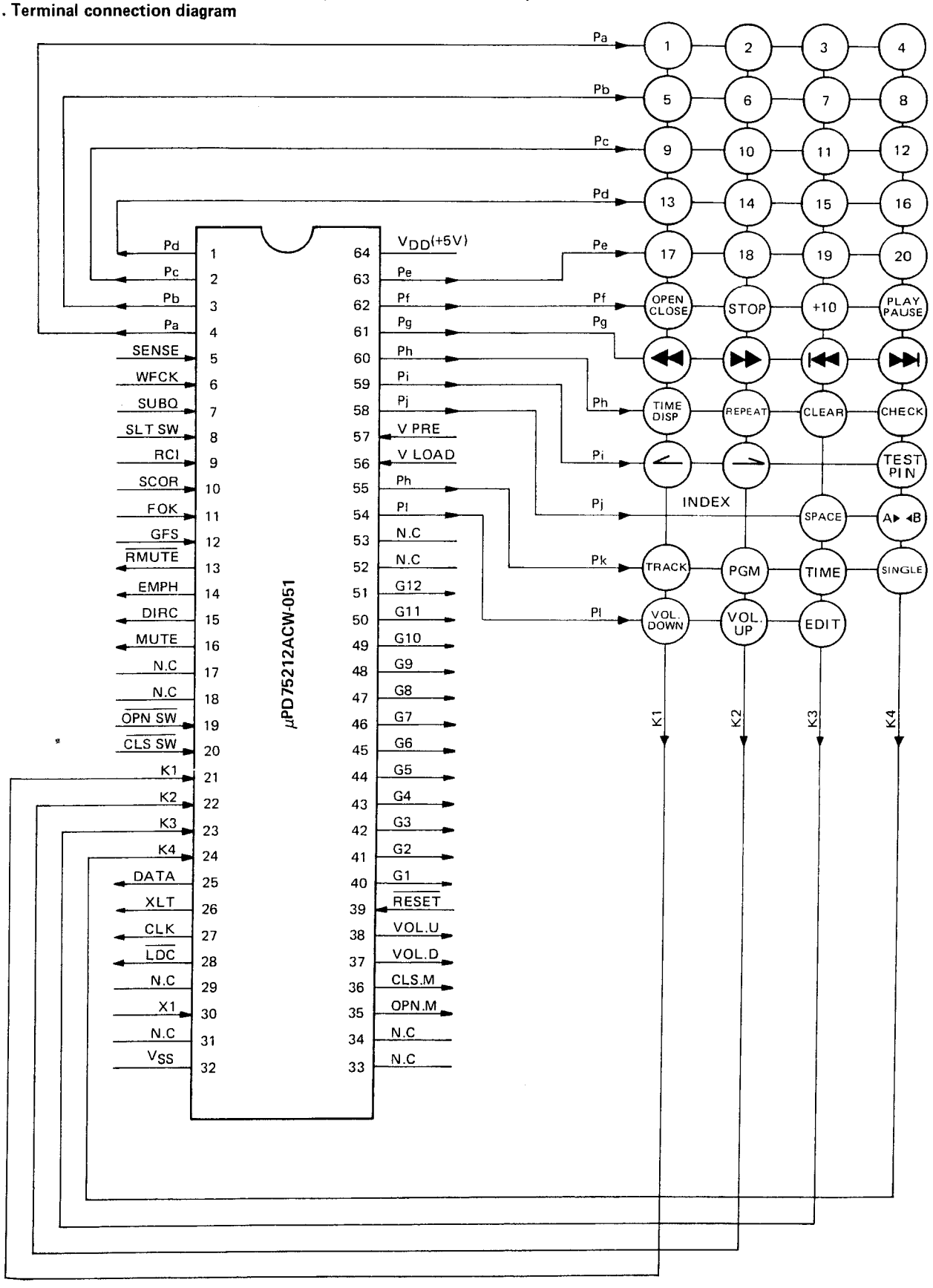
- In a usual case, since the tray was pushed when the tray is OPEN until STOP display is made.



CIRCUIT DESCRIPTION

5. Microprocessor μPD75212ACW-051(X32-1250-11 : IC104)
(X32-1250-21 : IC104)

5–1. Terminal connection diagram



CIRCUIT DESCRIPTION

5–2. Explanation of terminals

Pin No.	Pin Name	I/O	Function
1~4	Pd~Pa	O	FL segment control pins (also for key scan signal).
5	SENSE	I	Signal processing, pin to detect the SENSE signal from servo IC.
6	WFCK	I	Q data read-out clock pulse input pin.
7	SUBQ	I	Q data input pin.
8	SLTSW	I	Sled limit switch (Innermost : "L").
9	RCI	I	Remote control input pin.
10	SCOR	I	Sub-code frame sync detection signal input pin (input from CXD1125QZ).
11	FOK	I	RF amplifier FOK signal input pin (At focus OK : "H").
12	GFS	I	Frame sync signal input pin (In frame sync : "H").
13	$\overline{\text{RMUTE}}$	O	Analog mute control pin (Active "L").
14	EMPH	O	De-emphasis control pin (Active "H").
15	DIRC	O	Servo IC DIRC pin (output to CXA1244S).
16	MUTG	O	Signal processing IC mute pin (Active "H").
17,18	–	–	Unused.
19	$\overline{\text{OPNSW}}$	I	Tray open switch (When open : "L").
20	$\overline{\text{CLSSW}}$	I	Tray close switch (When close : "L").
21~24	K1~K4	I	Key matrix key return input pins.
25	DATA	O	Signal processing, servo IC control output pin (Control data signal).
26	XLT	O	Signal processing, servo IC control output pin (Control data latch signal).
27	CLK	O	Signal processing, servo IC control output pin (Control data transmission clock signal).
28	$\overline{\text{LDC}}$	O	Laser ON/OFF signal output pin (Active "L").
29	–	–	Unused.
30	X1	I	System clock pulse input pin.
31	–	–	Unused.
32	VSS	–	GND.
33,34	–	–	Unused.
35	OPN.M	O	Tray open/close motor drive signal output pins. Normally ..... OPN.M : "L", CLS.M : "L" When open ..... OPN.M : "H", CLS.M : "L" When close ..... OPN.M : "L", CLS.M : "H"
36	CLS.M	O	
37	VOL.D	O	Motor volume level down output pin.
38	VOL.U	O	Motor volume level up output pin.
39	$\overline{\text{RESET}}$	I	Reset input pin (Active "L").
40~51	G1~G12	O	FL digit control pins.
52,53	–	–	Unused.
54,55	Pl,Pk	O	FL segment control pins (also for key scan signal).
56	VLOAD	I	FL driver negative power supply (–30V).
57	VREF	I	FL pre-driver negative power supply (–5V).
58~63	Pj~Pe	O	FL segment control pins (also for key scan signal).
64	VDD	–	Power supply (+5V).

CIRCUIT DESCRIPTION

6. RF AMP CXA1081S(X29-1960-00 : IC1)

General

The CXA1081S is an IC developed for use in Compact Disc players. It incorporates a 3-spot optical pickup RF output amplifier, a focusing error amplifier, a tracking error amplifier, and other signal processing circuitry, such as focus OK, mirror, defect, and EFM comparator circuits, as well as a laser diode APC (Automatic Power Control) circuit.

Features

- Operates on a signal +5 V power supply, as well as on a ±5 V dual-voltage power supply.
- Low power consumption (100 mW with ±5 V, 50 mW with +5 V).
- An APC circuit which accepts either a P-sub or N-sub laser diode.
- A minimum of external parts required.
- A disc defect detector circuit for improved playability

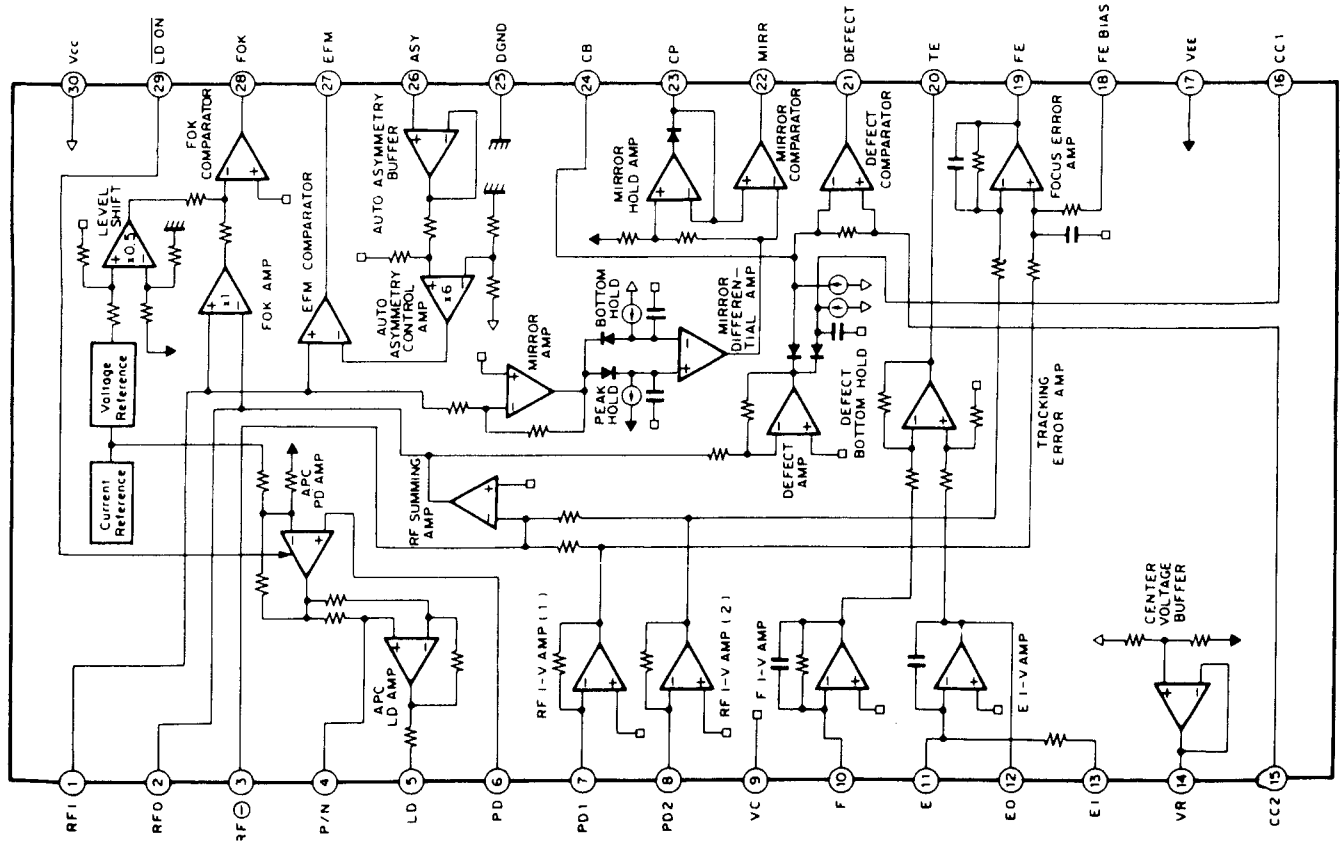
Structure

Bipolar silicon monolithic IC

Functions

- RF amplifier
- Focus OK detector circuit
- Mirror detector circuit
- Tracking error amplifier
- Defect detector circuit
- APC circuit
- EFM comparator
- Auto asymmetry control amplifier

6—1. Block diagram



CIRCUIT DESCRIPTION

6—2. Explanation of terminals (V_{CC}=2.5V, V_{EE}=D_{GND}=–2.5V, VC=GND)

Terminal No.	Terminal name	I/O	DC voltage (V)	Function
1	RFI	I	0	Input pin for the C-coupled signal output from the RF summing amplifier
2	RFO	O	V_{RFO}	RF summing amplifier output pin. Used as the check point for the eye pattern
3	RF⊖	I	0	RF summing amplifier feedback input pin.
4	P/N	I	0 (VC)	P-sub/N-sub select pin for the LD (Laser Diode) (DC voltage: in N-sub mode)
5	LD	O	–1.8	*APC LD amplifier output pin. (DC voltage: PD open in N-sub mode)
6	PD	I	0	*APC LD amplifier input pin. (DC voltage: open)
7	PD1	I	0	RF I-V amplifier (1) inverted input pin. Current input by connecting to the photodiode A + C terminal
8	PD2	I	0	RF I-V amplifier (2) inverted input pin Current input by connecting to the photodiode B + D terminal
9	VC	—	0	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply Connected to VR (pin 14) when using a single-voltage power supply
10	F	I	0	F I-V amplifier inverted input pin Current input by connecting to the photodiode F terminal
11	E	I	0	E I-V amplifier inverted input pin Current input by connecting to the photodiode E terminal
12	EO	O	0	E I-V amplifier output pin
13	EI	I	0	E I-V amplifier feedback input pin. For E I-V amplifier gain adjustment
14	VR	O	V_{CVO}	DC voltage output pin of (V_{CC} + V_{EE})/2.
15	CC2	I	1.0	Input pin for the C-coupled signal output from the defect bottom hold
16	CC1	O	1.2	Defect bottom hold output pin
17	V_{EE}	—	–2.5	Connected to the negative power supply when using a positive (+)/negative (–) dual-voltage power supply. Connected to GND when using a single-voltage power supply
18	FE BIAS	I	0	Bias pin on the focus error amplifier non-inverted side For CMR adjustment of the focus error amplifier
19	FE	O	V_{FEO}	Focus error amplifier output pin.
20	TE	O	V_{TEO}	Tracking error amplifier output pin.
21	DEFECT	O	V_{DFCTL}	Defect comparator output pin (DC voltage: connected to a 10 k-ohm load)
22	MIRR	O	V_{MIRL}	Mirror comparator output pin (DC voltage: connected to a 10 k-ohm load)
23	CP	I	–1.3	Mirror hold capacitor output pin. Mirror comparator non-inverted input.
24	CB	I	0	Defect bottom hold capacitor connect pin
25	DGND	—	–2.5	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply Connected to GND (V_{EE}) when using a single-voltage power supply.
26	ASY	I	—	Auto asymmetry control input pin.
27	EFM	O	V_{EFMH}	EFM comparator output pin. (DC voltage: connected to a 10 k-ohm load)
28	FOK	O	V_{FOKL}	FOK comparator output pin. (DC voltage: connected to a 10 k-ohm load)
29	LD ON	I	–2.5 (DGND)	LD ON/OFF select pin. (DC voltage: when LD ON)
30	V_{CC}	—	2.5	Positive power supply.

*APC: Automatic Power Control

CIRCUIT DESCRIPTION

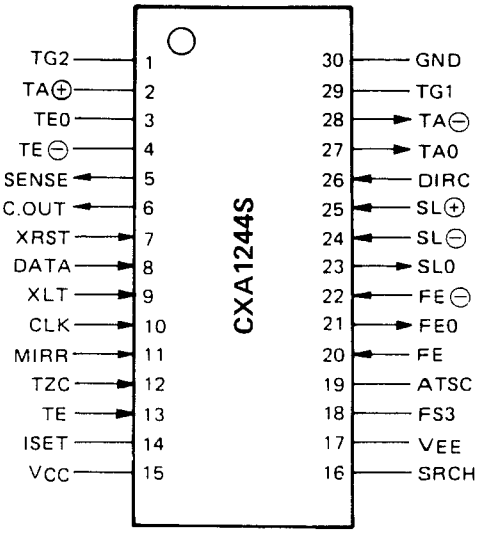
7. Servo control CXA1244S(X32-1250-11 : IC103) (X32-1250-21 : IC103)

CXA1244S is a bipolar IC developed for servo of compact disc (CD) players, and it provides the following functions.

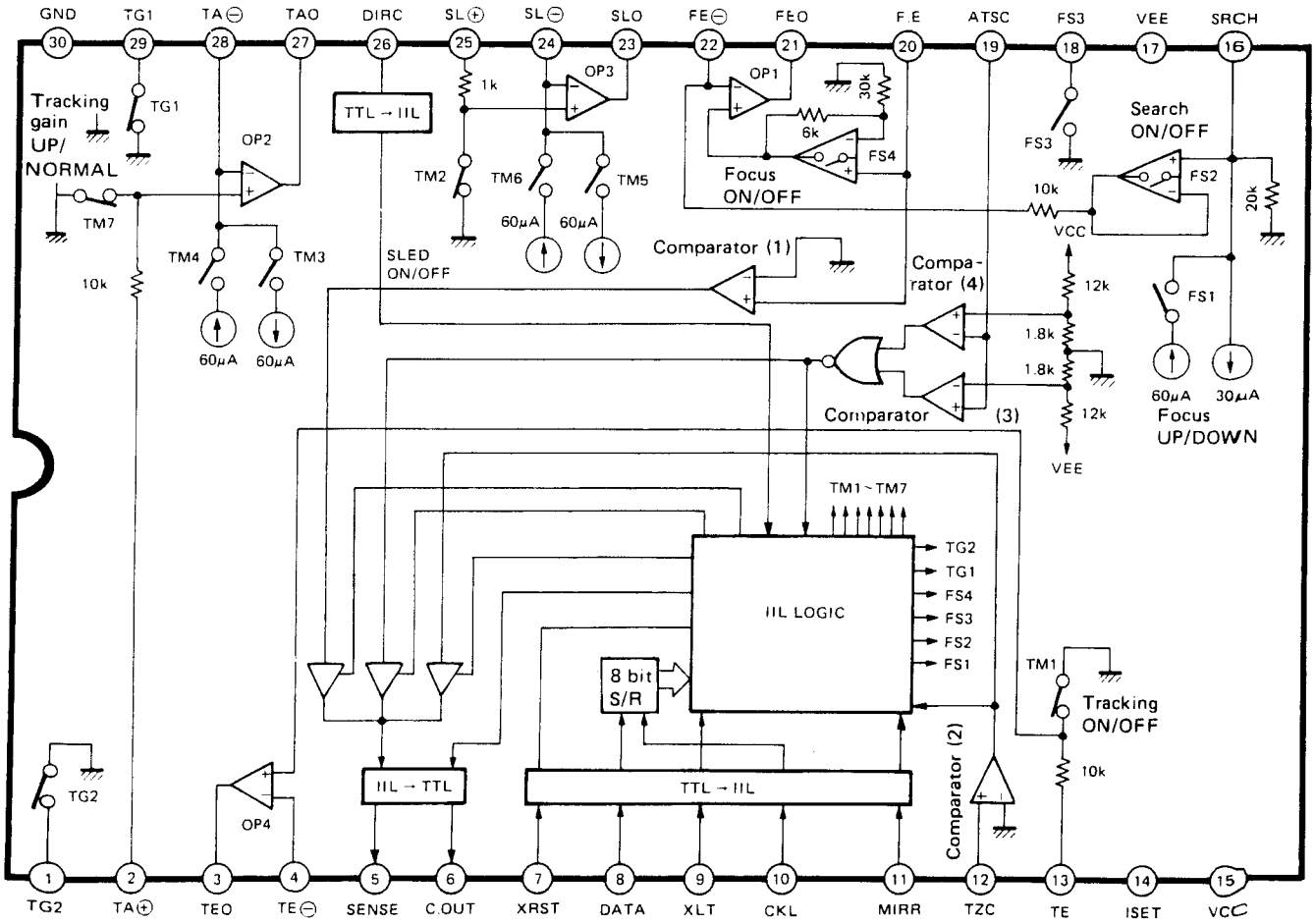
- ○Focus control (search ON/OFF, gain control)
- ○Tracking control (servo ON/OFF, single track jump, multiple track jump, gain control, phase compensation control, brake circuit)
- ○ Sled control (servo ON/OFF, fast forward, fast reverse)

Servo function of each of focus, tracking and sled as well as random access operation are realized through control by microcomputer. Furthermore, the serial data bus can be shared with CXD1125Q.

7–1. Terminal connection diagram



7–2. Block diagram



CIRCUIT DESCRIPTION

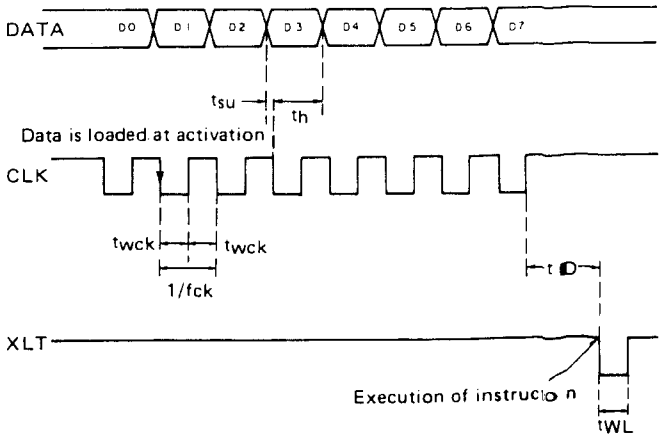
7—3. Explanation of terminals

Terminal No.	Terminal name	I/O	Functions
1	TG2		Tracking amplifier gain switching terminal. GND level.
2	TA ⊕		Non-inverted input of operational amplifier 2.
3	TE0		Output of operational amplifier 4.
4	TE ⊖	O	Inverted input of operational amplifier 4.
5	SENSE	O	Output of SSP internal status that corresponds to ADDRESS of CPU → SSP. (Changes in accordance with ADDRESS content of internal serial register.) See Note 1.
6	C. OUT	O	Signal output for counting number of tracks at the time of high speed access.
7	XRST	I	All internal registers are cleared when CPU → SSP "L". Connected with CPU RESET. See Note 2.
8	DATA	I	Serial data transmission of CPU → SSP. Input is made from LSB. D0~D7.
9	XLT	I	Latch of serial data of CPU → SSP. (The contents of internal serial register are transmitted to each address decoded latch.) Transmission at "L". Change to "H" occurs immediately after execution because no edge trigger is produced.
10	CLK	I	CPU → SSP serial data transmission clock. Data is read at falling. "H" level before and after transmission.
11	MIRR	I	Mirror signal input from RF amplifier.
12	TZC	I	Tracking error signal is input with C couple. The time constant is determined by one single track jump, but it is usually around 2kHz.
13	TE	I	Tracking error signal input.
14	ISET		Setting of current level for determining focus search voltage, tracking jump voltage and sled feed voltage.
15	Vcc		Power supply terminal. Normally −5V.
16	SRCH		The capacitor for determining the time constant of charge/discharge waveform for focus search is connected.
17	VEE		Power supply terminal. Normally −5V.
18	FS3		Focus amplifier gain switching terminal. GND level.
19	ATSC		Such information that a mechanical shock was applied to the player is input. Simply, a trakcing error is input through B.P.F.
20	FE	I	Input of focus error signal.
21	FE0	O	Output of operational amplifier 1.
22	FE ⊖	I	Inverted input of operational amplifier 1.
23	SL0	O	Output of operational output 3.
24	SL ⊖	I	Inverted input of operational amplifier 3.
25	SL ⊕	I	Non-inverted input of operational amplifier 3.
26	DIRC	I	Used at the time of one track jump. Normally "H". The direction of the track jump pulse is reversed with "L". Setting is made in the normal tracking mode by changing to "H" "L" for a fixed length of time with detection of activation, deactivation of TZC.
27	TA0	O	Output of operational amplifier 2.
28	TA ⊖	O	Inverted input of operational amplifier 2.
29	TG1		Tracking amplifier gain switching terminal. GND level.
30	GND		GND terminal of IC.

Note 1 : SENSE terminal output

Serial data upper 4 bits	ADDRESS content	SENSE terminal output	Explanation
0 0 0 0	FOCUS CONTROL	FZC	"H" when focus zero cross. Focus error voltage is 0V or higher. Used at the time of FOCUS PULL operation
0 0 0 1	TRACKING CONTROL	AS	"H" when the ATSC input level exceeds the wind comparator level (VTH = ±Vcc x 13%) But this is not used in this equipment.
0 0 1 0	TRACKING MODE	TZC	Judgement output of positive or negative of tracking zero cross, tracking error. When used at the time of single track jump, DIRC is reduced to "L" on detection of TZC ↑ in FWD JUMP or on detection of TZC ↓ in REV JUMP

Note 2 : Digital unit timing chart



CIRCUIT DESCRIPTION

7–4. System control

COMMAND	ADDRESS				DATA				SENSE
	D7	D6	D5	D4	D3	D2	D1	D0	
FOCUS CONTROL	0	0	0	0	FS4 FOCUS ON	FS3 GAIN DOWN	FS2 SEARCH ON	FS1 SEARCH UP	FZC
TRACKING CONTROL	0	0	0	1	ANTI SHOCK	BREAK ON	TG2 GAIN	TG1* SET	AS
TRACKING MODE	0	0	1	0	TRACKING* MODE		SLED* MODE		TZC

GAIN SET* TG1, TG2 may be set independently.
In the case of ANTI SHOCK = 1 (00011XXX), both TG1, TG2 are inverted when ANTI SCHOCK = "H".

SLED MODE*

	D1	D0
OFF	0	0
SERVO ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

TRACKING MODE*

	D3	D2
OFF	0	0
SERVO ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

CIRCUIT DESCRIPTION

8. Signal processor CXD1125QZ(X32-1250-11 : IC11) (X32-1250-21 : IC11)

General

The CXD1125QZ is a digital signal processing LSI for a Compact Disc player, and has the following functions.

1. Bit clock reproduction by an EFM-PLL circuit
2. EFM data demodulation
3. Frame sync signal detection, protection and insertion
4. Powerful error detection and correction
5. Interpolation with an average value, or by holding the previous value
6. Demodulation of a sub code signal, error detection of a sub code Q
7. Spindle motor CLV servo
8. 8-bit tracking counter
9. CPU interface with a serial bus
10. Sub code Q register
11. Digital filter
12. Digital audio interface output

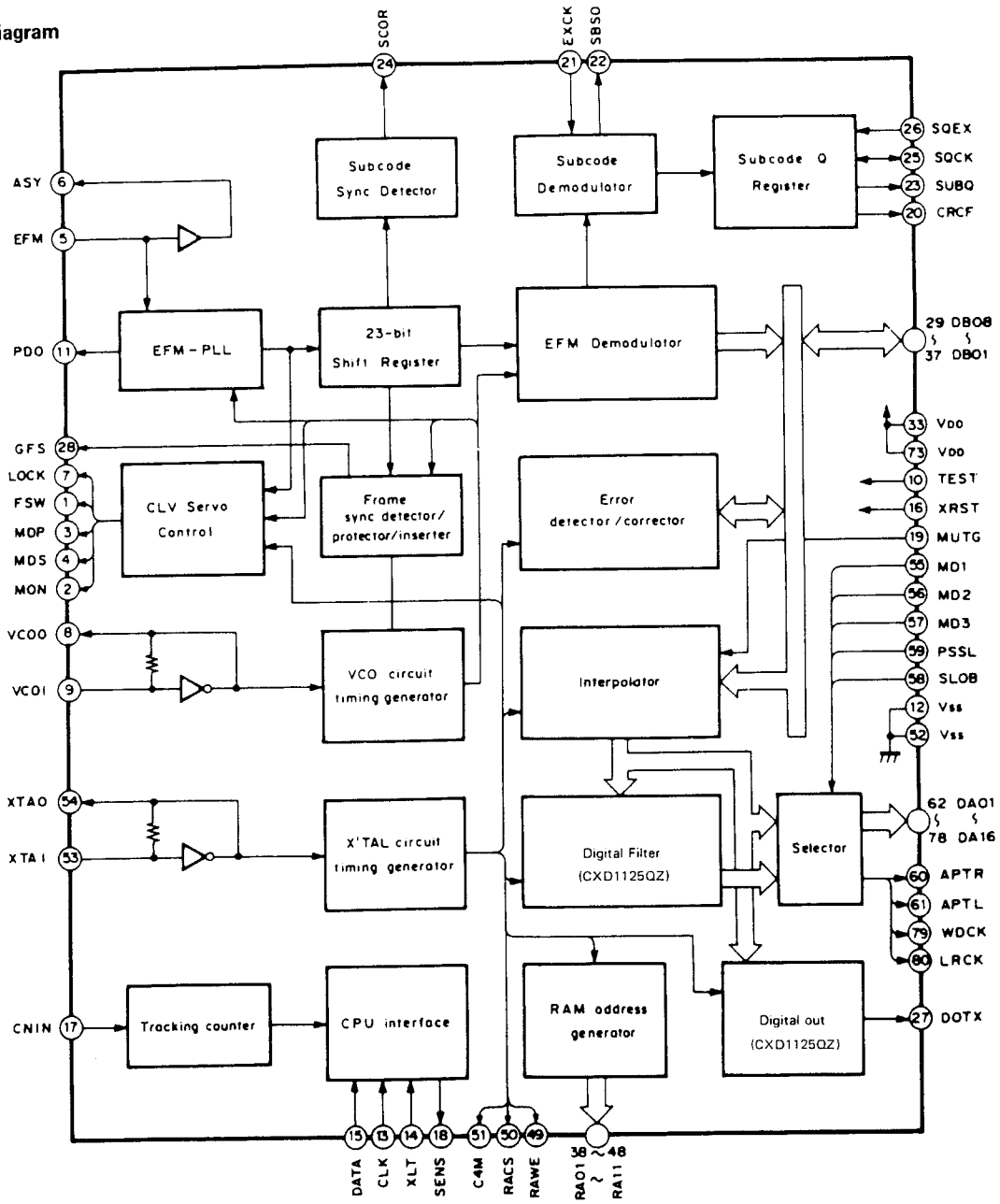
Features

- All digital signals used in playback can be processed using only a single chip.
- An aperture-correction digital filter is built in.

Structure

CMOS IC

8–1. Block diagram



CIRCUIT DESCRIPTION

8–2. Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode
5	EFM	I	EFM signal input from RF amplifier
6	ASY	O	Output for controlling the slice level of EFM signal
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high When it is "L" for eight times, in arrow, outputs "L"
8	VCOO	O	VCO output. f = 8 6436 MHz when locked to EFM signal
9	VCOI	I	VCO input
10	TEST	I	(0 V)
11	PDO	O	Phase comparison output of EFM signal and VCO/2
12	V_{SS}	—	GND (0 V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L"
17	CNIN	I	Input of tracking pulse.
18	SENS	O	Output of internal status in correspondence to the address
19	MUTG	I	Muting input. In the case when ATTM of internal register A is "L" Normal status when MUTG is "L" or soundless state when it is "H"
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code serial output
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync S0 + S1 output.
25	SQCK	I/O	Sub code Q read-off clock
26	SQEX	I	SQCK select input.
27	DOTX	O	DIGITAL OUT output. (Outputs the $\overline{\text{WFCK}}$ signal when CXD1130Q or D0 is off)
28	GFS	O	Display output of frame sync lock status.
29	DB08	I/O	Data pin of external RAM. DATA8 (MSB)
30	DB07	I/O	Data pin of external RAM. DATA7
31	DB06	I/O	Data pin of external RAM. DATA6
32	DB05	I/O	Data pin of external RAM. DATA5
33	V_{DD}	—	Power supply (+5 V)
34	DB04	I/O	Data pin of external RAM. DATA4
35	DB03	I/O	Data pin of external RAM. DATA3
36	DB02	I/O	Data pin of external RAM. DATA2
37	DB01	I/O	Data pin of external RAM. DATA1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM. (Active at "L").
50	RACS	O	Chip select signal output to external RAM. (Active at "L").
51	C4M	O	Crystal dividing output. f = 4.2336 MHz.
52	Vss	—	GND (0 V).
53	XTAI	I	Crystal oscillator input. f = 8.4672 MHz or 16.9344 MHz depending on the mode selected.
54	XTAO	O	Crystal oscillator output. f = 8.4672 MHz or 16.9344 MHz depending on the mode selected.
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select input. Serial output when "L", parallel output when "H"
60	APTR	O	Aperture compensation control output. "H" when R-ch.
61	APTL	O	Aperture compensation control output. "H" when L-ch.
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL = "H", C1F1 output when PSSL = "L".
63	DA02	O	DA02 output when PSSL = "H", C1F2 output when PSSL = "L"
64	DA03	O	DA03 output when PSSL = "H", C2F1 output when PSSL = "L".
65	DA04	O	DA04 output when PSSL = "H", C2F2 output when PSSL = "L".
66	DA05	O	DA05 output when PSSL = "H", C2FL output when PSSL = "L".
67	DA06	O	DA06 output when PSSL = "H", C2PO output when PSSL = "L".
68	DA07	O	DA07 output when PSSL = "H", RFCK output when PSSL = "L"
69	DA08	O	DA08 output when PSSL = "H", WFCK output when PSSL = "L".
70	DA09	O	DA09 output when PSSL = "H", $\overline{\text{PLCK}}$ output when PSSL = "L".
71	DA10	O	DA10 output when PSSL = "H", UGFS output when PSSL = "L".
72	DA11	O	DA11 output when PSSL = "H", GTOP output when PSSL = "L".
73	VDD	—	Power supply (+5 V).
74	DA12	O	DA12 output when PSSL = "H", RAOV output when PSSL = "L".
75	DA13	O	DA13 output when PSSL = "H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL = "H", $\overline{\text{C21O}}$ output when PSSL = "L".
77	DA15	O	DA15 output when PSSL = "H", C21O output when PSSL = "L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL = "H", DATA output when PSSL = "L".
79	WDCK	O	Strobe signal output. 176.4 kHz when DF is ON, 88.2 kHz with CXD1125Q or when DF is OFF.
80	LRCK	O	Strobe signal output. 88.2 kHz when DF is ON, 44.1 kHz with CXD1125Q or when DF is OFF

Notes:

C1F1 :
C1F2 :] Error correction status monitor output for C1 decode.

C2F1 :
C2F2 :] Error correction status monitor output for C2 decode.

C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.

C2PO : C2 pointer signal. Synchronized to the audio data output.

RFCK : Read frame clock output. 7.35 MHz when locked to the crystal line.

WFCK : Write frame clock output. 7.35 MHz when locked to the crystal line.

$\overline{\text{PLCK}}$: VCO/2 output. f = 4.3218 MHz when locked to the EFM signal.

UGFS : Non-protected frame sync pattern output.

GTOP : Frame sync protect status display output.

RAOV : ±4 frame jitter absorption RAM overflow and underflow display output.

C4LR : Strobe signal. 352.8 kHz when DF is ON, 176.4 kHz with CXD1125Q or when DF is OFF.

$\overline{\text{C21O}}$: C21O invert output.

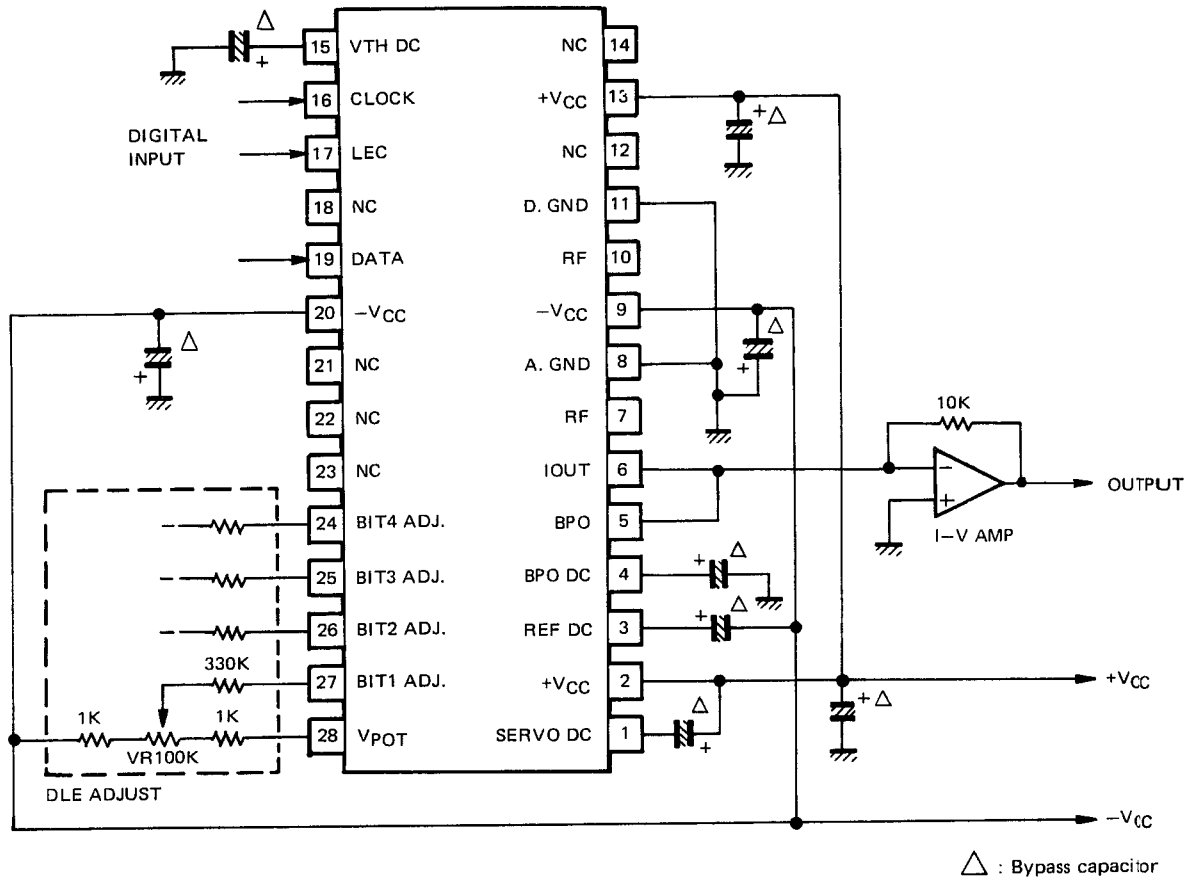
C21O : Bit clock output. 4.2336 MHz when DF is ON, 2.1168 MHz with CXD1125Q or when DF is OFF.

DATA : Audio signal serial data output.

CIRCUIT DESCRIPTION

9. 18-bit serial input D/A converter PCM58P(X32-1250-11 : IC6, IC7)
(X32-1250-21 : IC6, IC7)

9–1. Terminal connection diagram

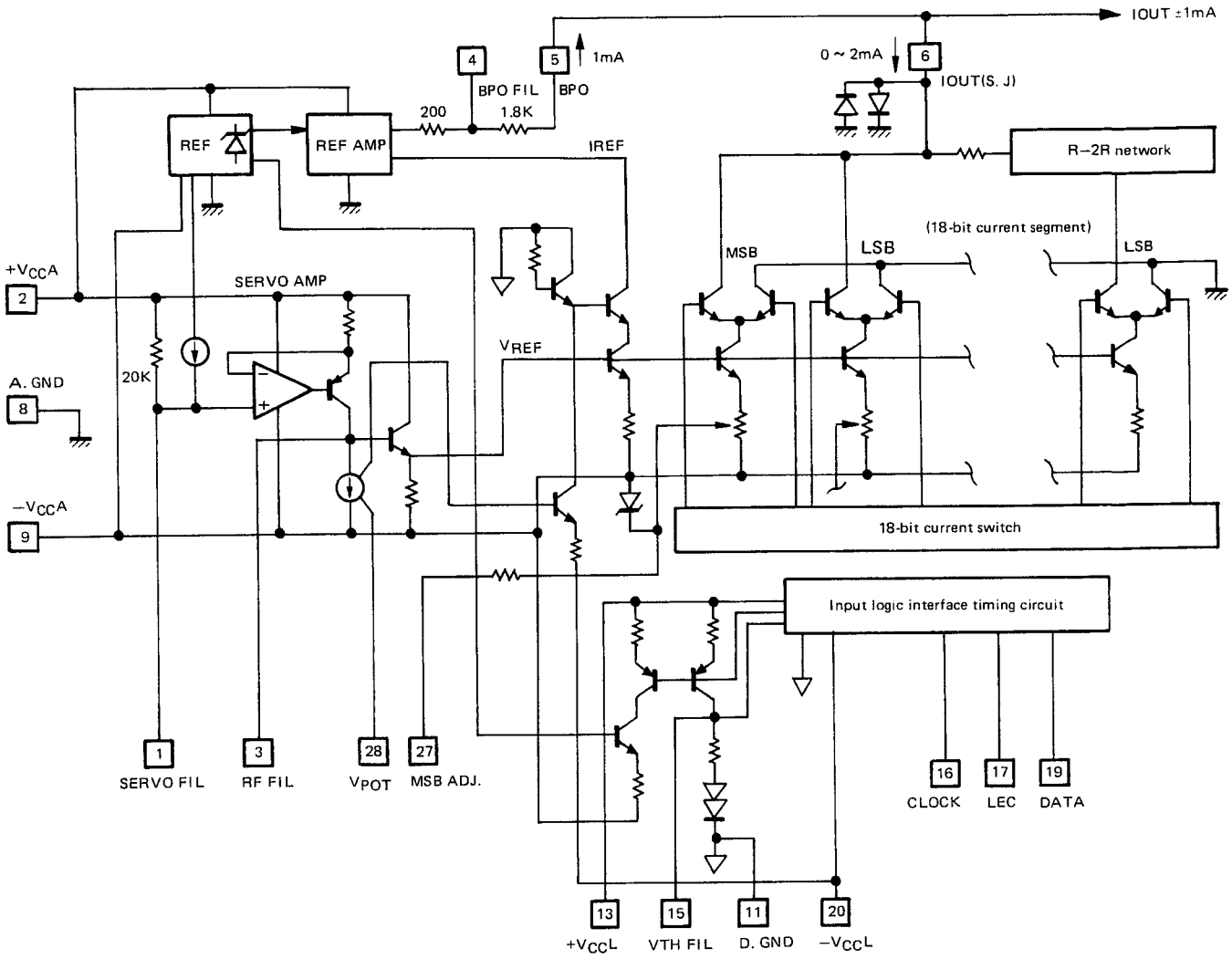


9–2. Terminal connections

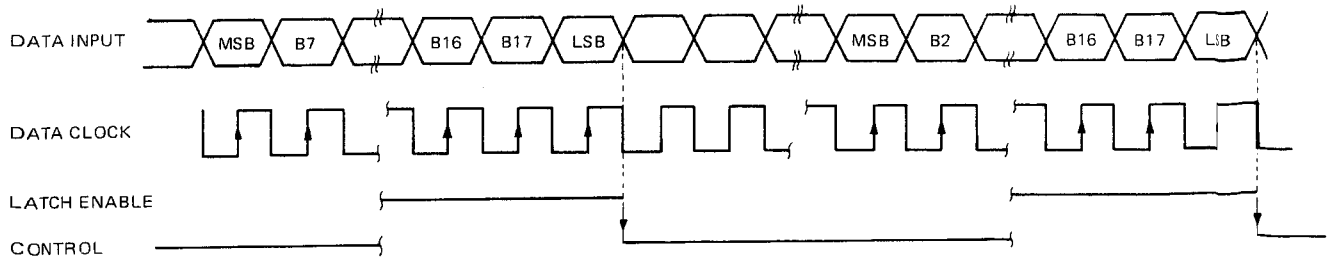
Pin No.	Pin Name	Pin No.	Pin Name
1	Servo filter	15	VTH filter
2	+Vcc	16	Clock pulse input
3	Reference filter	17	LEC input
4	BPO filter	18	NC
5	Bipolar offset	19	Data input
6	Current output	20	-Vcc
7	RF	21	NC
8	Analog COM	22	NC
9	-Vcc	23	NC
10	RF	24	BIT4 ADJ
11	Digital COM	25	BIT3 ADJ
12	NC	26	BIT2 ADJ
13	+Vcc	27	BIT1 ADJ
14	NC	28	VPOT

CIRCUIT DESCRIPTION

9–3. Block diagram



9–4. Timing chart



- The data format is of 2's complement, right-justified or continuous data of MSB first.
- Data is taken in to the shift register at the rise of the data clock pulse.

CIRCUIT DESCRIPTION

10. 8x over-sampling digital filter SM5813AP(X32-1250-11 : IC9) (X32-1250-21 : IC9)

10-1. Function

- 2-channel processing
- 8x over-sampling (interpolation) filter (hereinafter referred to as 8fs for short)
- Serial input data
  2's complement, MSB first
  16-bit
- Serial output data
  MSB first
  2's complement/COB selectable
  Selectable between 16-, 18- and 20-bit
- Jitter-free
  Prevents any faulty operation due to the jitter of the input clock signal, thus eliminating the jitter transmission over to the output.
- System clock pulse
  Selectable from 192fs, 256fs, 384fs and 512fs
- Crystal oscillation circuit incorporated
- I/O TTL compatible
- 5 V single power supply
- 28-pin plastic DIP

10-2. Filter configuration

- Interpolation filter
  Linear phase FIR filter 3-stage configuration
  First stage (fs — 2fs), 153rd
  Second stage (2fs — 4fs), 29th
  Third stage (4fs — 8fs), 17th
- 22-bit filter coefficient, 20x22 bit parallel multiplier/25-bit accumulator high-accuracy operation
- Overflow limiter incorporated

10-3. Applications

- CD playback
- DAT playback
- PCM playback

10-4. Filter characteristics

Characteristic item	Performance
Pass band	0 ~ 0.4535fs
Reject band	0.5465fs ~ 7.4535fs
Pass band ripple	Within ±0.00005dB
Reject band attenuation	More than 110dB
Group delay time	Fixed

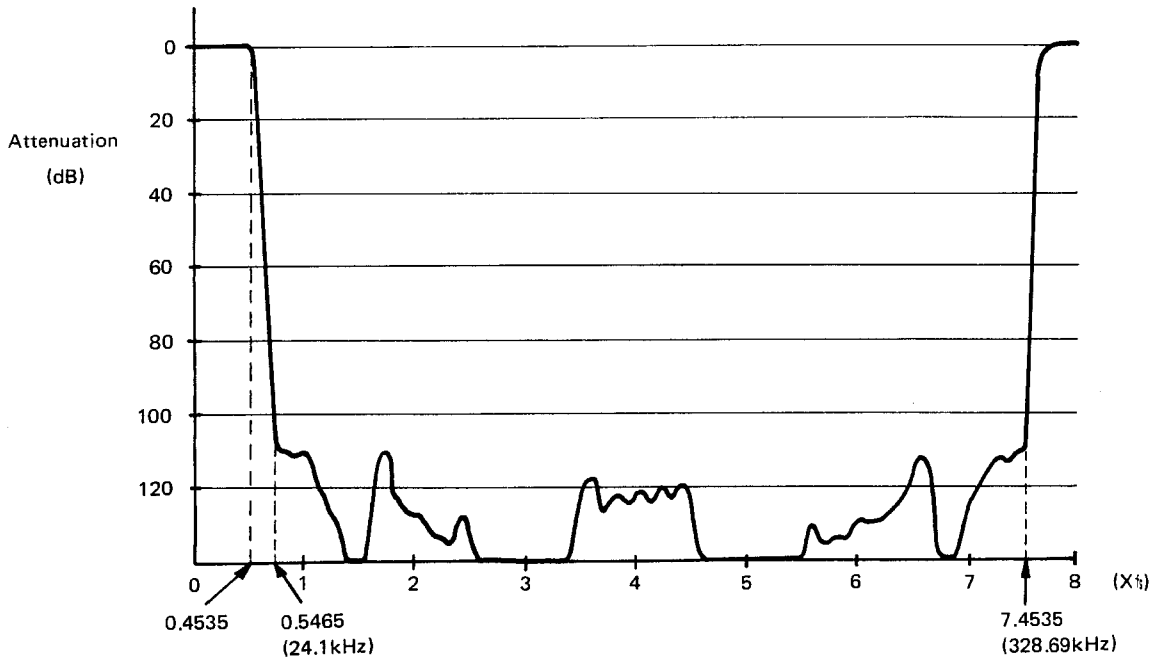
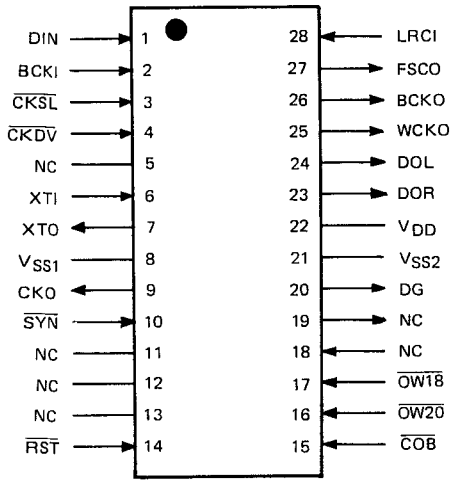


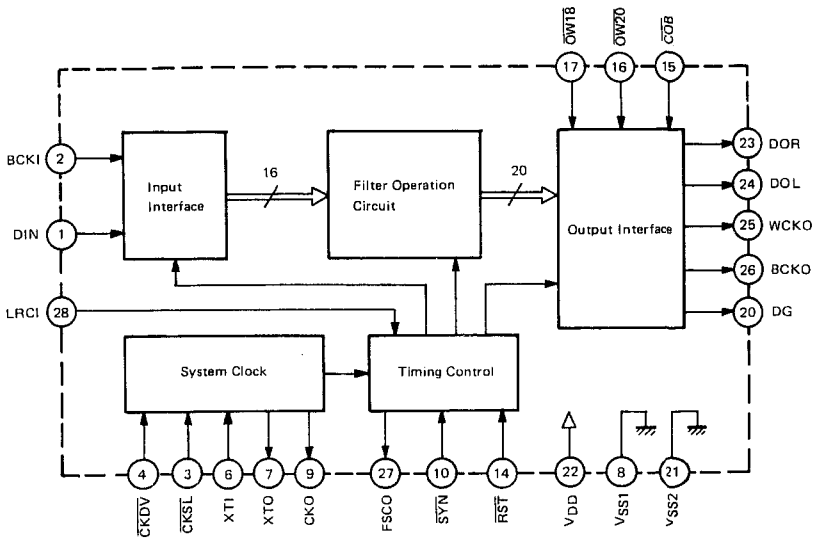
Fig. 10—1 Frequency response

CIRCUIT DESCRIPTION

10–5 Terminal connection diagram



10–6 Block diagram



10–7. Explanation of terminals

"fs" occurring in the description means the sampling frequency of the input data.

Pin No.	Pin Name	I/O	Function
1	DIN	I	Input data.
2	BCKI	I	Input data beat clock pulse.
3,4	CKSL, CKDV	I	XTI pin input frequency selection. (For details, refer to the description of XTI pin.)
5	NC	–	Unused.
6	XTI	I	Oscillator section input pin. 192 fs : CKSL = "H", CKDV = "H" 256 fs : CKSL = "H", CKDV = "L" 384 fs : CKSL = "L", CKDV = "H" 512 fs : CKSL = "L", CKDV = "L"
7	XTO	O	Oscillator section output pin.
8	VSS1	–	GND1.
9	CKO	O	Oscillator section output clock pulse. (Frequency is the same as in XTI pin.)
10	SYN	I	Jitter-free mode/compulsory sync mode selection. ("H : Jitter-free mode, "L" : Compulsory sync mode)
11~13	NC	–	Unused.
14	RST	I	System reset. ("H" : normal operation, "L" : system reset)
15	COB	I	2's complement/COB selection. ("H" : 2's complement, "L" : COB)
16,17	OW20, OW18	I	Number-of-output-bits selection. No. of output bits: 16 — OW18: H, OW20: H; 18 — OW18: L, OW20: H; 20 — OW18: H, OW20: L
18,19	NC	–	Unused.
20	DG	O	Deglitch control clock pulse.
21	VSS2	–	GND2.
22	VDD	–	Power supply (+5V).
23	DOR	O	Rch 8x over-sampling output data.
24	DOL	O	Lch 8x over-sampling output data.
25	WCKO	O	Output data word clock pulse.
26	BCKO	O	Output data bit clock pulse.
27	FSCO	O	fs-period internal operation timing clock pulse.
28	LRCI	I	Input data sampling rate (fs) clock pulse. ("H" : Lch, "L" : Rch)

CIRCUIT DESCRIPTION

10-8. Function

• 8x over-sampling (interpolation) filter function

This function works to output the over-sampling data of sampling rate 8fs. In this case, sampling noises between 0.5465fs (24.1kHz) and 7.4535fs (328.69kHz) are removed.

The interpolation operation block configuration of this LSI is of a cascade connection of three 2x interpolation filters (FIR).

• System clock (XTI, XTO, CKO, $\overline{CKSL}$, $\overline{CKDV}$)

The system clock pulse can be selected from 192fs, 256fs, 384fs and 512fs. More, operation is feasible even by an external clock (input to pin XTI) or a crystal oscillator (inserted between pins XTI and XTO). In this unit, a clock pulse of 8.4672 MHz is input to pin XTI.

From pin CKO, the system clock pulse is output. (See Figure 10-3.)

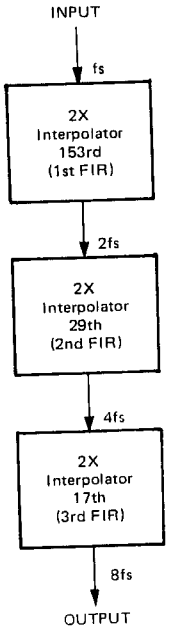


Fig. 10–2 Configuration of basic operation section

$\overline{CKDV}$		H		L	
$\overline{CKSL}$		H	L	H	L
XTI input clock frequency (Fxi)	Fxi = 1/tXI	192fs	256fs	384fs	512fs
Clock pulse input method		External clock (input to pin XTI) or internal clock (a crystal oscillator inserted between pin XTI and XTO).			
Internal system clock pulse period	Tsys	tXI		2*tXI	

tXI stands for the XTI input clock pulse period.

Table 10–1 System clock frequency selection and internal system clock

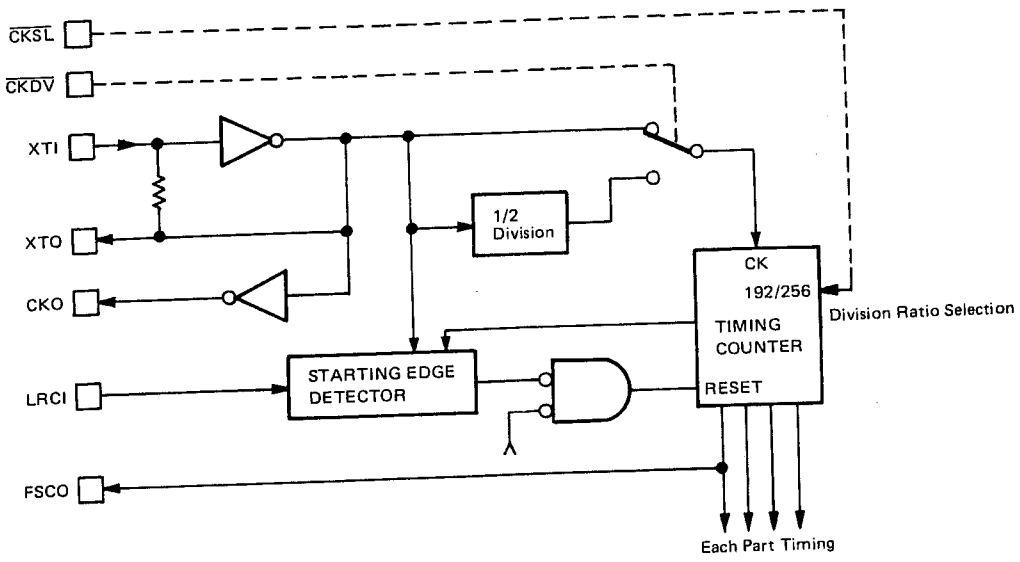


Fig. 10–3 Clock generation circuit

CIRCUIT DESCRIPTION

• Auto data input (DIN, BCKI, LRCI)

The input data is handled as being of 2's complement, MSB first. Each bit of the serial data input to pin DIN is read in to register SIPO (serial/parallel conversion register) a the leading edge of bit clock pulse BCKI, in which it is in turn converted into a parallel data. The output of SIPO is transferred to each of the Lch and Rch input registers at the trailing/leading edge of clock pulse LRCI.

In addition, the operation section and the output section are independent in signal timing from the input section and are therefore unsusceptible to the jitter of the input section. (Jitter-free mote: For details, refer to the description occurring later.)

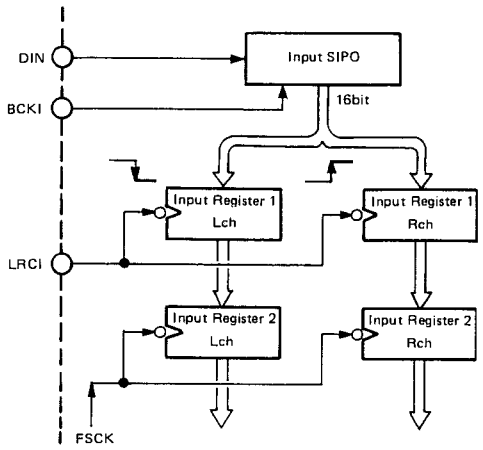
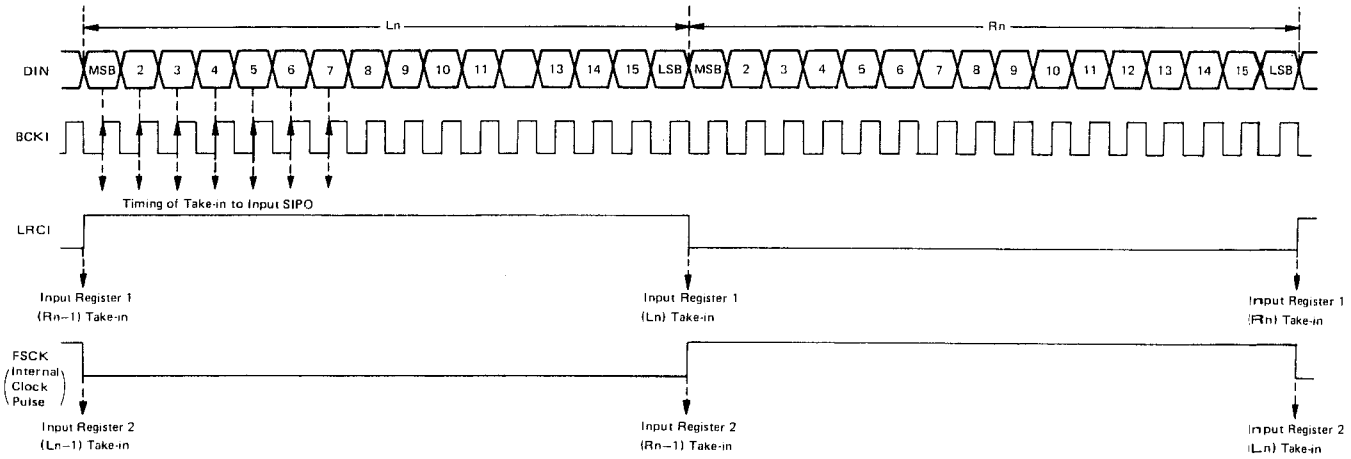


Fig. 10–4 Configuration of audio data input section



16bits right before LRCI edge is taken in as data.

Fig. 10–5 Audio data input timing example

• Selection between jitter-free mode and compulsory sync mode ($\overline{SYN}$, FSCO)

The signal timing (internal timing) applied to internal operation or output, that is produced from the system clock pulse (input to pin XTI), is independent from that of the data input section (BCKI, LRCI).

For this internal timing, the method of countering the jitter of clock pulse input LRCI is available in two types, "jitter-free mode" and "compulsory sync mode". Selection between these both is feasible by setting $\overline{SYN}$.

1) Jitter-free mode ($\overline{SYN}$="H")

As long as the phase difference between clock pulse LRCI and the internal timing is within +3/8 to –3/8 of the input sampling period (1/fs), the internal timing is not adjusted. Accordingly, even with a jitter component in clock pulse LRCI, the internal timing is not affected so that it is free from faulty operation or jitter transmission to output.

When the phase difference is without the above range, the internal timing is put in phase synchronously with the start side of clock pulse LRCI. More, this treatment is also performed when the reset input is given.

2) Compulsory sync mode ($\overline{SYN}$="L")

When this mode is engaged, the internal timing is always reset at a pulse edge of the start side of input LRCI. In this case, when a pulse period shorter than the specified system clock pulse period exists due to the jitter of input LRCI, a faulty operation may result.

Conversely, when a pulse period longer exists, the operation is properly made but no equal output timing is obtained.

3) Clock pulse FSCO (output)

This is a clock pulse with a period of fs obtained from the dividing process of clock pulse XTI.

CIRCUIT DESCRIPTION

• Data and DAC control signal output (DOL, DOR, BCKO, WCKO, DG, $\overline{COB}$, $\overline{OW18}$,$\overline{OW20}$)

1) Output data format

1) MSB first
2) 2's complement/COB (Complemented Offset Binary) selection ($\overline{COB}$)
   2's complement format ($\overline{COB}$="H")
   COB format ($\overline{COB}$="L")

2) Output data number-of-bits selection ($\overline{OW18}$, $\overline{OW20}$)

As to the number of bits for the output data, any of 16, 18 and 20-bit can be selected.
16-bit output ($\overline{OW18}$="H", $\overline{OW20}$="H")
18-bit output ($\overline{OW18}$="L", $\overline{OW20}$="H")
20-bit output ($\overline{OW18}$="H", $\overline{OW20}$="L")
However, this unit is set at the 18-bit output mode.

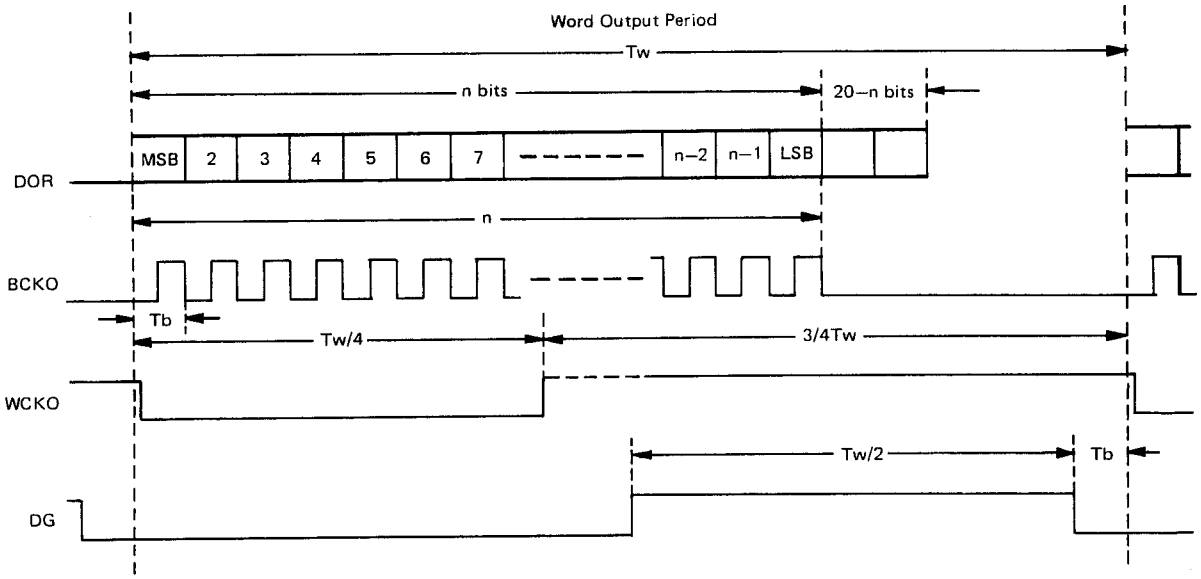
3) Output timing

The output timing of the audio output section is determined according to each internal system clock pulse frequency.

Item	Symbol in diagram	$\overline{CKSL}$	
		H	L
Internal system clock pulse frequency		192fs	256fs
Bit clock pulse period	Tb	Tsys	Tsys
Data word length	Tw	24*Tsys	32*Tsys

Tsys : internal clock pulse period (Refer to Table 10-1.)
Tb, Tw : serial output timing (Refer to Figure 10-6.)

Table 10–2 Output timing



Note : n means the number of output wordbits.

Fig. 10–6 Output timing

• System reset ($\overline{RST}$)

When the reset input is made in the jitter-free mode, the internal operation timing is reset in synchronization with the leading edge of input LRCI. Making use of this, the output timing in the jitter-free mode can be aligned with input LRCI.

In the compulsory sync mode, no system reset is needed. Even in the jitter-free mode, the output timing does not need to be aligned with input LRCI and no system reset is necessary.

For system reset at power ON, externally connect a capacity of around 100pF to pin $\overline{RST}$. (Figure 10-7)

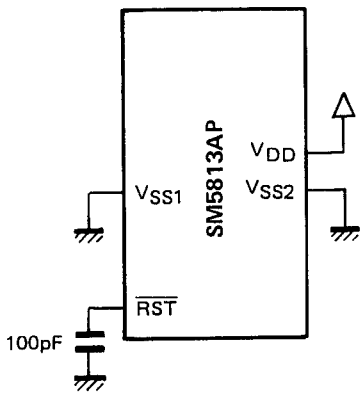
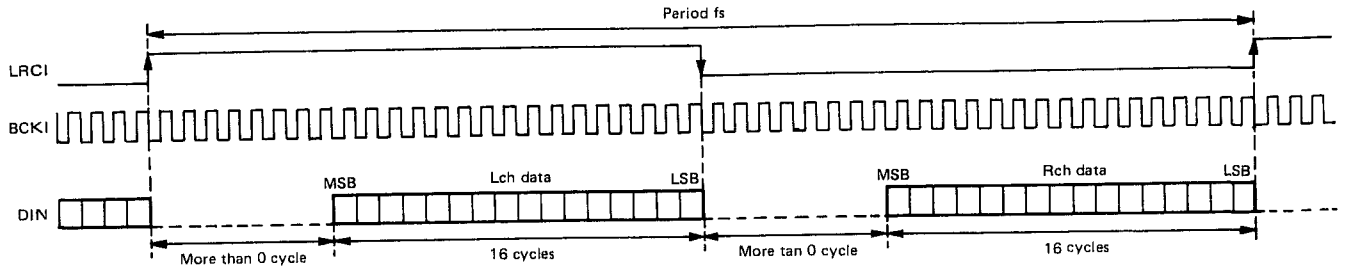


Fig. 10–7 Circuit example of system reset at power ON

CIRCUIT DESCRIPTION

10—9. Timing chart

- Serial input timing (DIN, BCKI, LRCI)



Note : BCKI should have 18 cycles or more for one word.

Fig. 10—8 Serial input timing

- Serial output timing (DOL, DOR, BCKO, WCKO, DG)

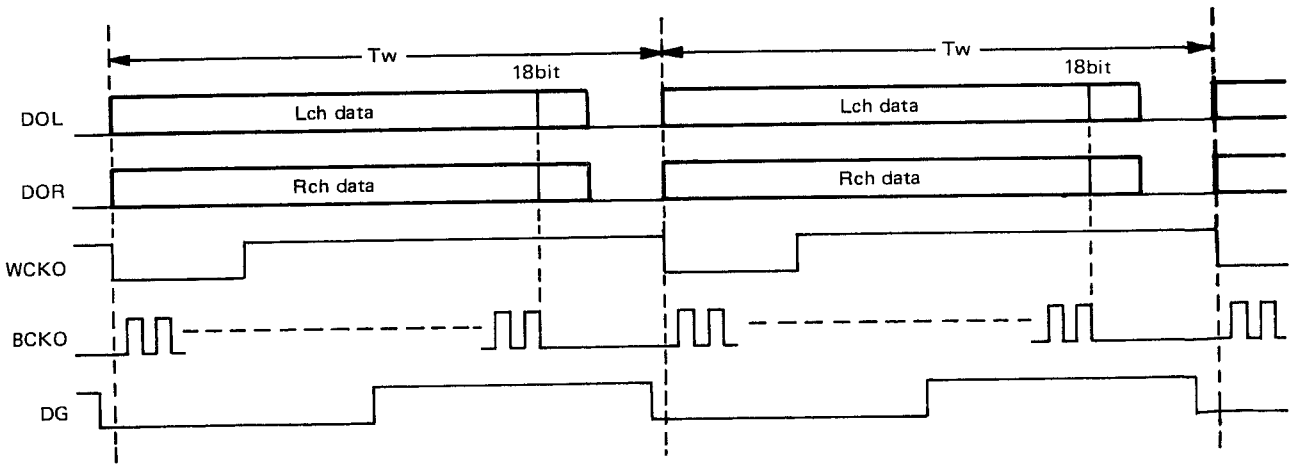
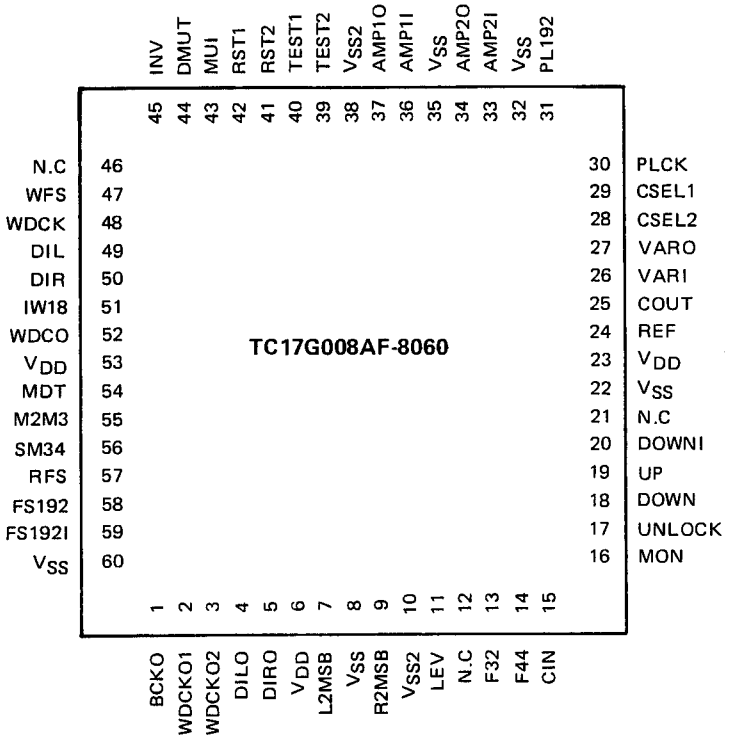


Fig. 10—9 Serial output timing

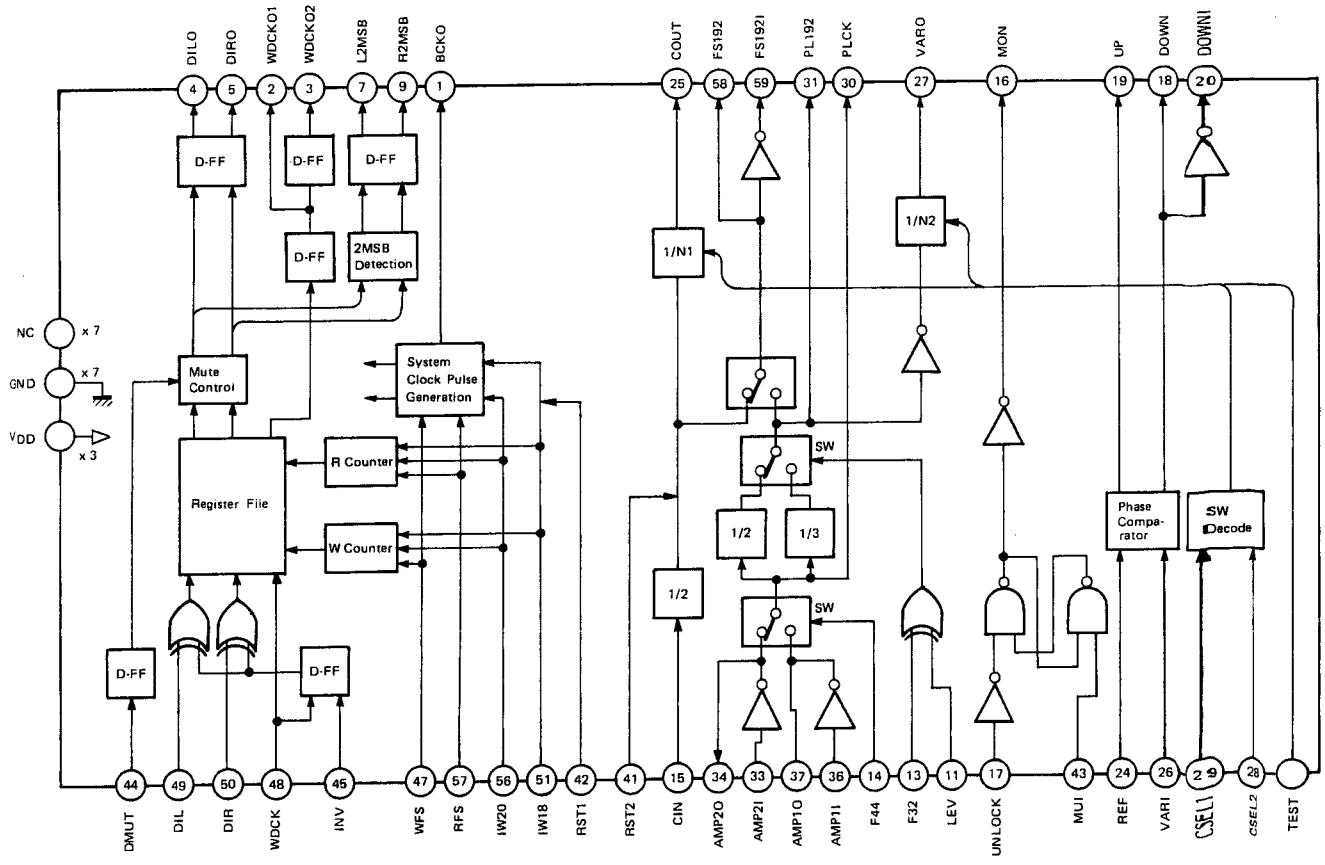
CIRCUIT DESCRIPTION

11. D. P. A. C IC TC17G008AF-8060(X32-1250-11 : IC15)
(X32-1250-21 : IC15)

11–1. Terminal connection diagram



11–2. Block diagram



CIRCUIT DESCRIPTION

11–3. Explanation of terminals

Pin No.	Pin Name	I/O	Function
1	BCKO	O	Bit clock pulse
2	WDCKO1	O	Output word clock pulse. Synchronous with the rise of data.
3	WDCKO2	O	Output word clock pulse. Delayed half clock pulse width from the rise of data.
4	DILO	O	Lch output data.
5	DIRO	O	Rch output data.
6	V_{DD}	I	Power supply (+5V).
7	L2MSB	O	Lch 2MSB level output.
8	V_{SS}	–	GND.
9	R2MSB	O	Rch 2MSB level output.
10	V_{SS2}	–	GND.
11	LEV	I	VCXO clock pulse division selection.
12	NC	–	Unused.
13	F32	I	FS32 flag.
14	F44	I	FS44 flag.
15	CIN	I	384FS clock pulse.
16	MON	O	Monitoring to see which of unlock and lock modes is engaged.
17	UNLOCK	I	
18	DOWN	O	Phase comparator down output.
19	UP	O	Phase comparator up output.
20	DOWNI	O	Inversion output of DOWN.
21	NC	–	Unused.
22	V_{SS}	–	GND.
23	V_{DD}	I	Power supply (+5V).
24	REF	I	Phase comparator R input.
25	COUT	O	Clock pulse obtained from 1/N1 division of 384FS clock pulse.
26	VARI	I	Phase comparator V input.
27	VARO	O	Clock pulse obtained from 1/N2 division of VCXO.
28	CSEL2	I	Division setting.
29	CSEL1	I	
30	PLCK	O	Check to see whether VCXO is 18MHz or 16MHz.
31	PL192	O	FS192 monitor.
32	V_{SS}	–	GND.
33	AMP2I	I	VCO (16MHz) clock pulse amplifier.
34	AMP2O	O	VCO (16MHz) clock pulse amplifier.
35	V_{SS}	–	GND.
36	AMP1I	I	VCO (18MHz) clock pulse amplifier.
37	AMP1O	O	VCO (18MHz) clock pulse amplifier.
38	V_{SS2}	–	GND.
39	TEST2	I	Test pin, fixed to 0V.
40	TEST1	I	Test pin, fixed to 0V.
41	RST2	I	PLL system reset input pin (Reset at "L").
42	RST1	I	TBC system reset input pin (Reset at "L").

CSEL1	CSEL2	N1	N2	Application
0	0	1	1	–
1	0	8	96	BS
0	1	192	192	AMP
1	1	256	256	AMP

CIRCUIT DESCRIPTION

Pin No.	Pin Name	I/O	Function
43	MUI	I	PLL system mute input pin.
44	DMUT	I	TBC system mute input pin (Mute at "H").
45	INV	I	Input data inversion (both Lch and Rch) (Inversion at "H").
46	NC	–	Unused.
47	WFS	I	Write clock pulse synchronous with input data.
48	WDCK	I	Input word clock pulse.
49	DIL	I	Lch input data.
50	DIR	I	Rch input data.
51	IW18	I	Data bit length selection (16-bit/18-bit = "L"/"H").
52	WDCO	O	Digital filter MEN signal.
53	V_{DD}	I	Power supply (+5V).
54	MDT	O	Digital filter MDT signal.
55	M2M3	O	Digital filter A1/A2 input signal.
56	SM34	I	Digital filter selection.
57	RFS	I	Read clock pulse synchronous with output data.
58	FS192	O	FS192 clock pulse.
59	FS192I	O	FS192 clock pulse inversion.
60	V_{SS}	–	GND.

CIRCUIT DESCRIPTION

11-4. Functions

• TBC function

The write data clock pulse (WFS) and the read data clock pulse (RFS) are independent in operation from each other. Thus, the jitter margin ranges ±1 clock pulse widths.

For 2MSB detection, the level (2's complement) of the 2MLSB detection value at playback is output for both Lch and Rch.

Figure 11-1 shows the I/O waveforms in use of each digital filter.

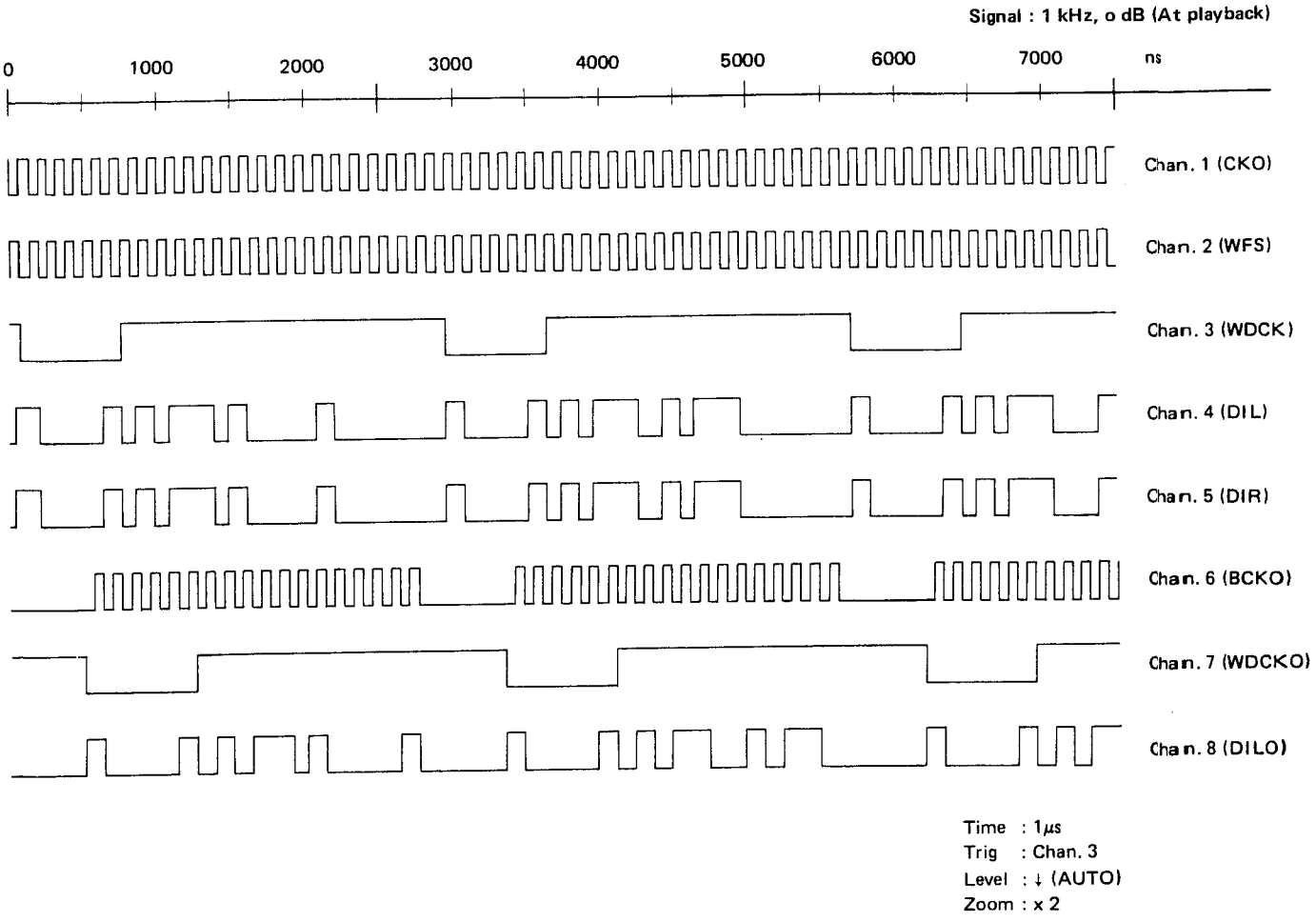


Fig. 11–1 D.P.A.C timing chart

• PLL function

Since the phase comparator is of a well-known system, its description is not made here.

For the counter setting of the divider, the type of the input clock pulse, LPF and VCXO circuit configuration, etc., refer to "11-2 Block diagram" and "11-3 Pin functions".

• Digital filter mode setting

Only two modes are available, 16-bit and 18-bit modes. This unit is set at the 18-bit mode.

The mode change is performed at the time of muting. The status right before the cancel of muting is held.

DP-8010

MECHANISM OPERATION DESCRIPTION

Figure 1 illustrates the positional relationship of the mechanism in the STOP mode. The position of each switch with the tray closed is as follows:

S1	Clamp UP switch	OFF
S2	Tray CLOSE switch	ON
S3	Clamp END switch	ON
S4	Tray OPEN switch	OFF

Note: The figure in ( ) following a parts name occurring in the drawing below is the same as in the exploded view of the service manual.

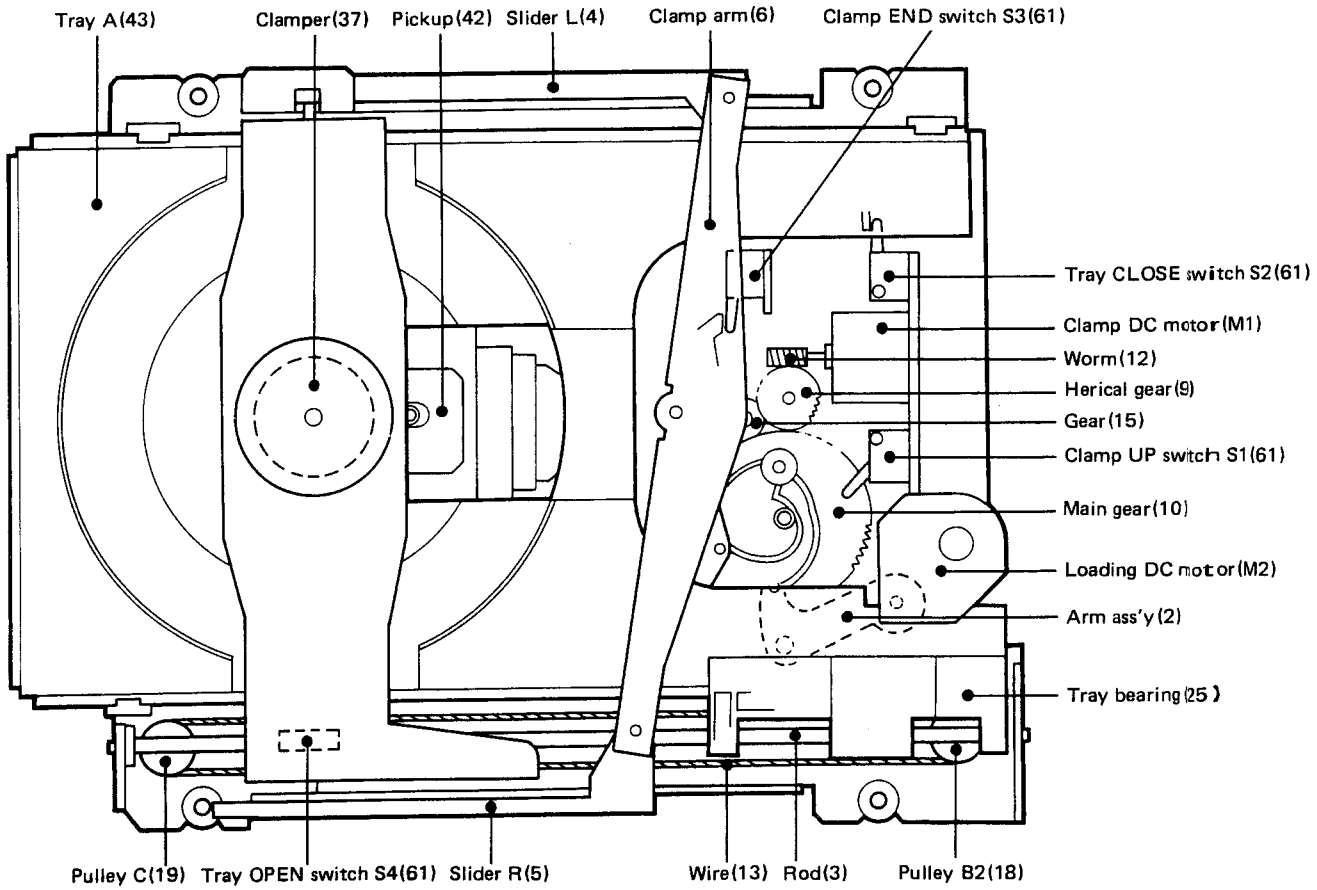


Fig. 1 Tray CLOSE status (as viewed perspectively from above)

MECHANISM OPERATION DESCRIPTION

1. Tray OPEN operation

When the OPEN/CLOSE key is pressed, an "H" signal is output from the pin 33 of the microprocessor. This signal is then amplified by IC105 (2/2), Q107 and Q108 and input to the mechanism.

At first, the clamp DC motor (M1) thus rotates in the direction of arrow (❶). Further, the main gear rotates in the direction of arrow (❷) by an intermediate gear (Figure 2).

A groove as shown in Figures 3 and 4 exists in the lower side of the main gear. The arm ass'y moves along this groove to control the tray OPEN/CLOSE operation (Figure 3).

Figure 4 shows the position of the main gear with the tray opened.

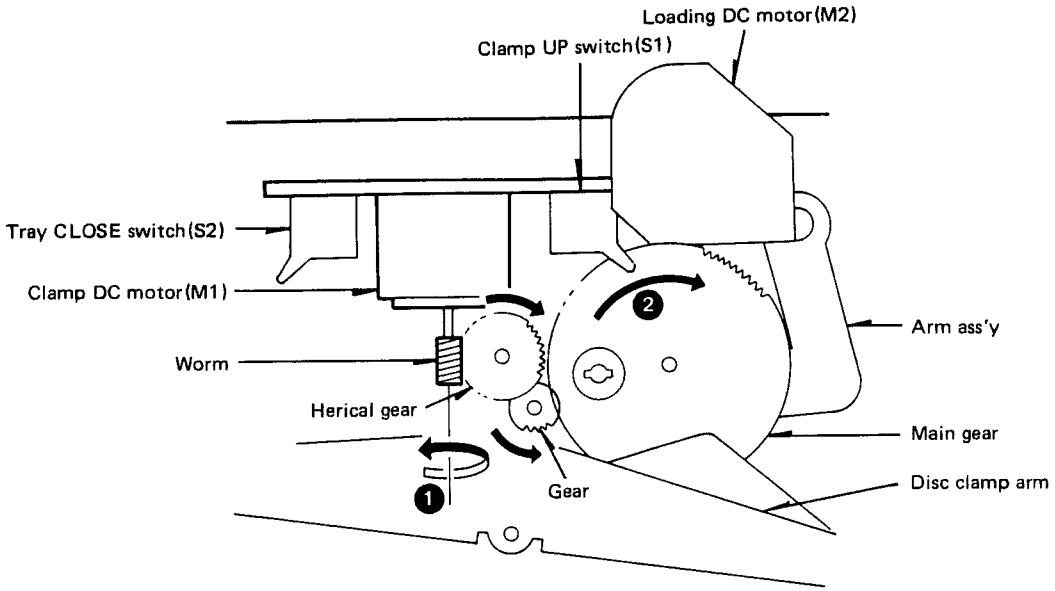


Fig. 2 Tray OPEN operation (1)

Due to the rotation in the direction of the arrow, the position of the arm ass'y moves in the direction of the broken line and comes to the location as shown in Fig.4. (At CLOSE, it moves in the reverse direction.)

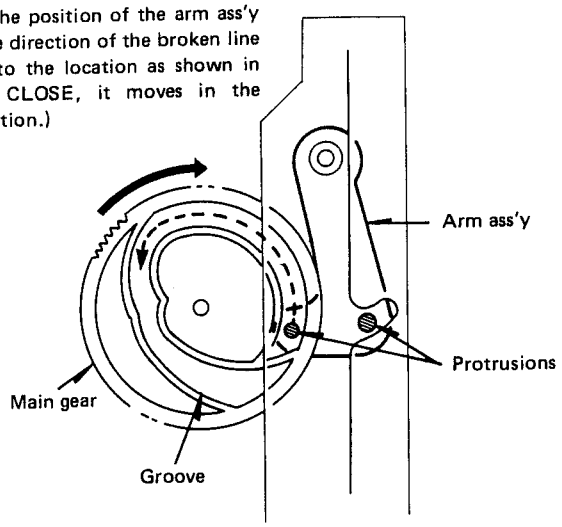


Fig. 3 Positional relationship between arm ass'y and main gear with tray closed (as viewed perspectively from above the main gear)

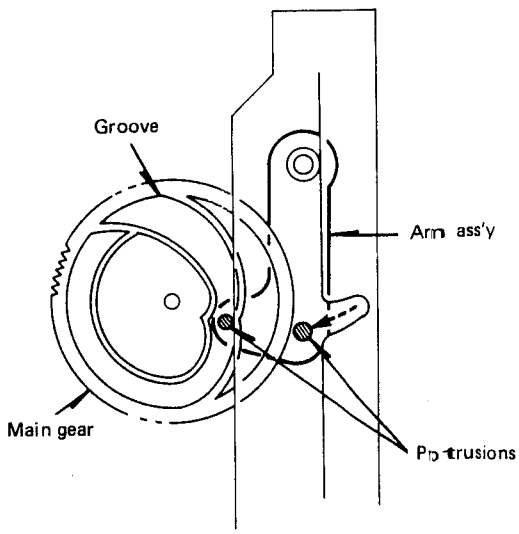


Fig. 4 Rear of main gear when tray opens

MECHANISM OPERATION DESCRIPTION

A similar groove is given in the upper side of the main gear. Along this groove, control is made over the clamp switch and the clamp mechanism. From the positional status with the tray closed as shown in Figure 3, when the clamp DC motor (M1) rotates in the direction of an arrow as indicated before, the protrusion placed at the lower side of the disc clamp arm is led in the direction of arrow (❸) along the groove of the main gear. Thereby, the disc clamp arm is rotated in the direction of arrow (❹) (Figure 5).

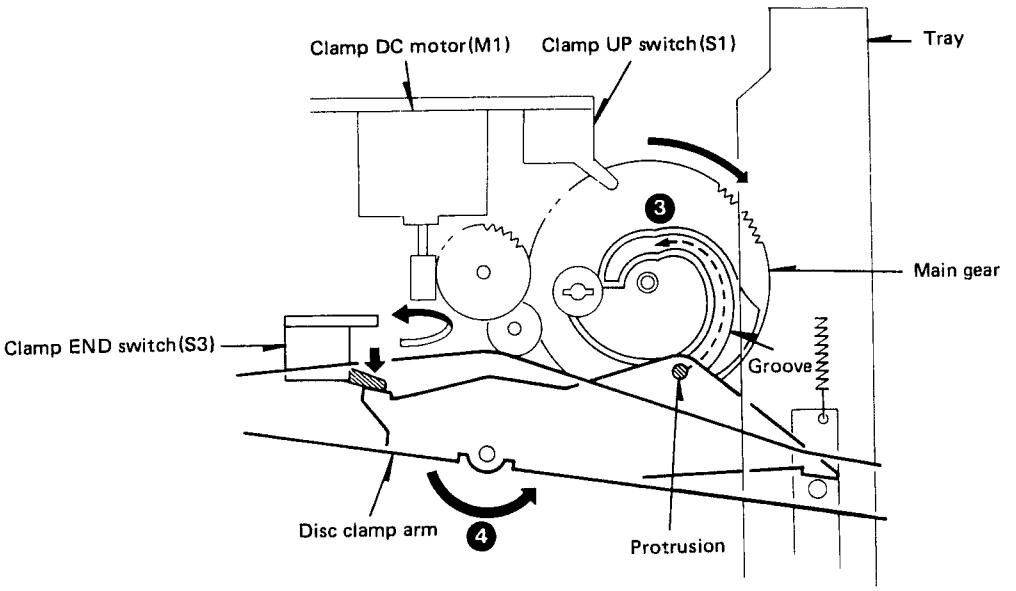


Fig. 5 Tray OPEN operation (2)

In addition, the top ends of the disc clamp arm are moved in the direction of arrows (❺) in response to the slider mechanism in order to raise and lower the disc clamper (Figure 6).

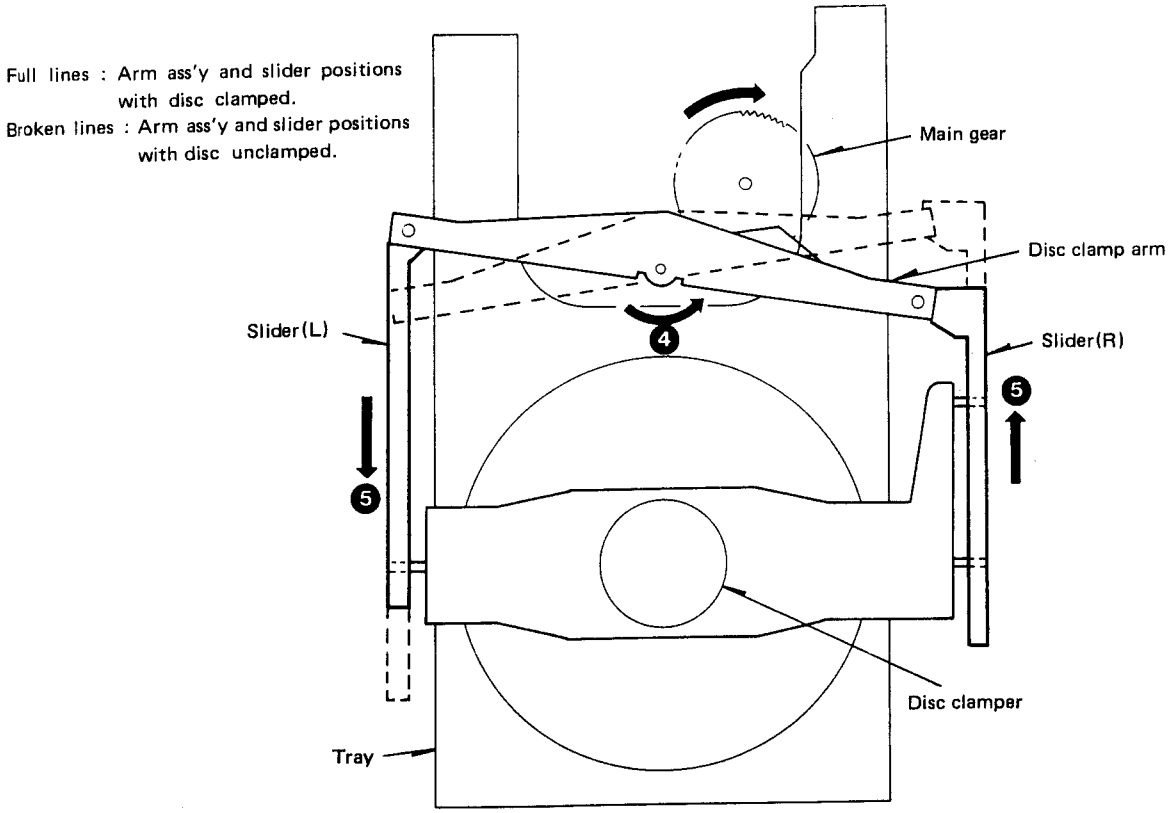


Fig. 6 Tray clamper UP/DOWN operation (1)

MECHANISM OPERATION DESCRIPTION

At this time, the tray is raised and lowered by the bent portion at the right lower side of the disc clamp arm. Figures 8 and 9 are the illustration on the process that the disc clamp arm moves in the direction of arrow (❹), the protrusion of the tray is released backwards by a spring and the tray rises entirely.

The left and right sliders are provided with slits as shown Figure 7, along which the left and right pins attached to the disc clamp arm slide up to unclamp. At this time, the disc clamp arm with the disc clamper fully raised is positioned with its left side down as opposed to the previous clamp position. (Figures 6, 7 and 8)

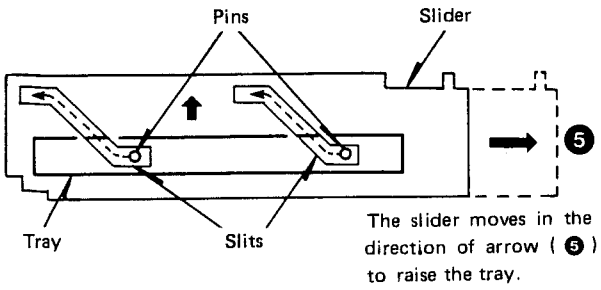
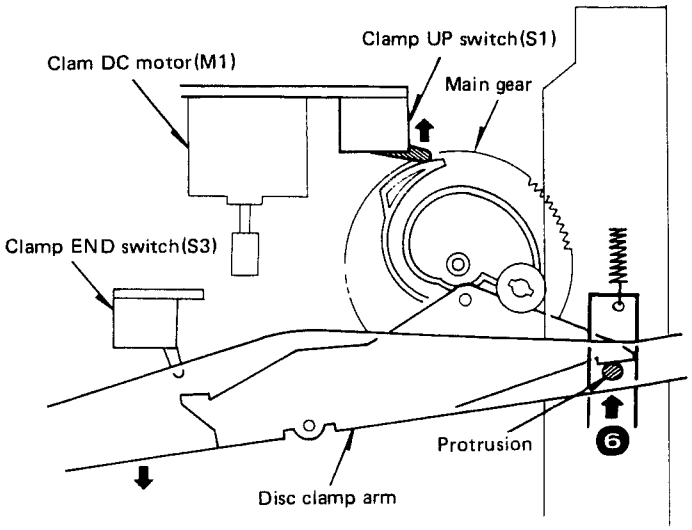


Fig. 7 Tray clamp UP/DOWN operation (2) (Side slider section)



Normally, when the disc is clamped, the spring is expanded. Thus, it moves in the direction of arrow (❻) with the arm movement.

Fig. 8 Clamp UP switch (S1) ON and unclamping

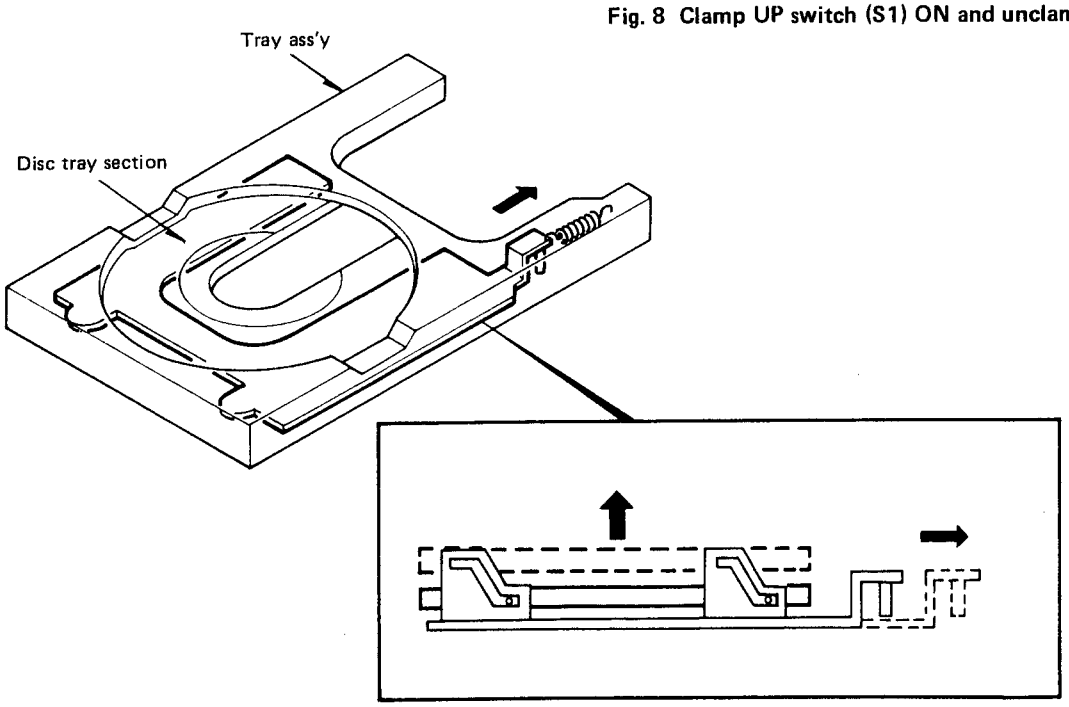


Fig. 9 Disc tray section UP/DOWN operation

MECHANISM OPERATION DESCRIPTION

Subsequently, S1 (clamper UP switch) turns ON by the groove at the upper side of the main gear, and the loading DC motor (M2) rotates in the direction of arrow (❼) to pull the wire via the belt (Figure 10).

As shown in Figure 11, a foot is given under the tray bearing by which the tray is installed to the rod. This foot works to turn ON/OFF S4 (tray OPEN switch). The loading DC motor (M2) rotates until S4 is turned ON by this foot to open the tray.

Note: The tray CLOSE operation is reverse to the tray OPEN operation in respect to the operational sequence. Therefore, the description of the tray CLOSE operation is here omitted.

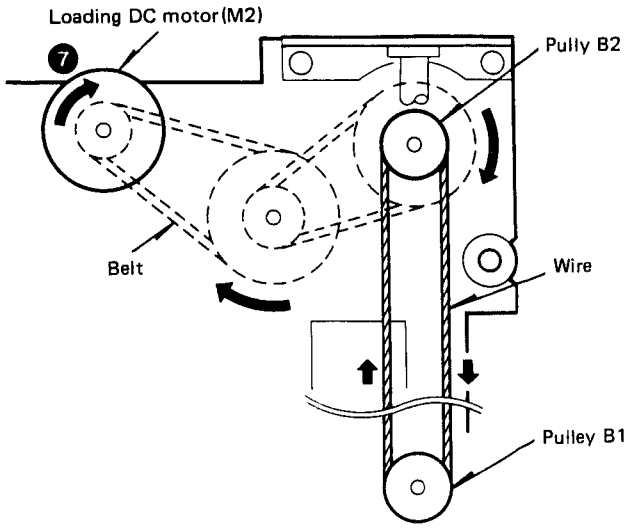


Fig. 10 Tray OPEN operation (3)

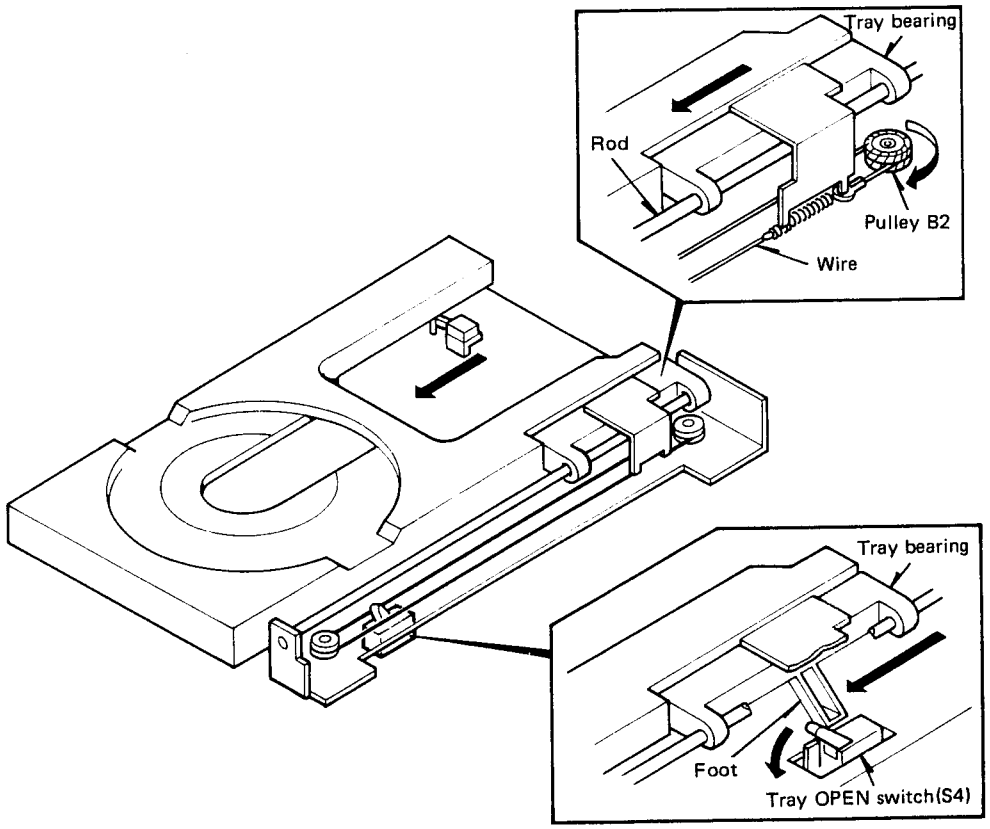


Fig. 11 Tray OPEN operation (4)

ADJUSTMENT

No.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG
1	LASER POWER	-	Apply the sensor section of the optical power meter on the pickup lens.	Short-circuit pins TEST and turn power on to enter the Test mode. Press the REPEAT key, the tray opens and the LD emits light.	-	When the power is from 0.35mW, RF level is 1.0Vp p or more, TE (servo open) is 2.0Vp p or more and the diffraction grating is aligned correctly, the pickup is acceptable.	(a)
2	VCO	-	Connect a frequency counter between CN8 pin 1(PLCK) and GND. (X32-1250)	Turn off the power once, and turn on the power again. Stop mode	L4 (X32-1250)	4.30MHz	(b)
3	DIFFRACTION GRATING	Test disc Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1960 CN2 pin 4) CH2: TE (X32-1250 pin 1)	Short pins TEST to enter the test mode. Press the CHECK key to confirm that the display is " 03 ".	-	Check that the diffraction grating is aligned correctly.(The diffraction grating cannot be adjusted.)	(c)
4	TRACKING ERROR BALANCE	Test disc Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1960 CN2 pin 4) CH2: TE (X32-1250 pin 1)	Short pins TEST to enter the test mode. Press the CHECK key to confirm that the display is " 03 ".	TE.BALANCE VR1 (X29-1960)	Symmetry between upper and lower patterns, or DC-0±0.05V	(d)
5	FOCUS ERROR BALANCE	Test disc Type 4	Connect an oscilloscope as follows. CH1: RF (X29-1960 CN2 pin 4) CH2: FE (X32-1250 pin 3)	Press the PLAY key, and confirm that the display is " 05 ".	FE BALANCE VR2 (X29-1960)	Optimum eye pattern	(e)
6	FOCUS GAIN	Test disc Type 4 Apply signal of 1.4kHz, 0.5Vrms to CN6 pin 2. (X32-1250)	Use a servo jig, or connect an oscilloscope or AC voltmeter to pin 1 of CN6 via a 47kΩ, 470 pF LPF. (X32-1250)	Turn off the power once, and turn on the power again. Press the PLAY key.	FOCUS GAIN VR3 (X29-1960)	50mVrms	(f)
7	TRACKING GAIN	Test disc Type 4 Apply signal of 1.4kHz, 0.5Vrms to CN6 pin 4. (X32-1250)	Use a servo jig, or connect an oscilloscope or AC voltmeter to pin 5 of CN6 via a 47kΩ, 470 pF LPF. (X32-1250)	PLAY	TRACKING GAIN VR4 (X29-1960)	50mVrms	(f)
8	DAC DISTORTION (MSB)	Test disc Type 4	Connect a distortion meter to the output terminal(FIXED).	Play the 1kHz, -20dB signal in track No.15.	VR1: L VR2: R (X32-1250)	Minimum distortion	(g)
9	DAC DISTORTION (2SB)	Test disc Type 4	Connect a distortion meter to the output terminal(FIXED).	Play the 100Hz, 0dB signal in track No.4.	VR3: L VR4: R (X32-1250)	Minimum distortion	(g)

(Note) Type 4 disc: SONY YEDS-18 Test Disc or equivalent.

REGLAGE

N°	ITEM	REGLAGE D'ENTREE	REGLAGE DE SORTIE	REGLAGE DE LA LECTURE	POINT D'ALIGNEMENT	ALIGNEMENT POUR	FIG
1	PUISSANCE LASER	–	Appliquer la section détecteur du compteur de puissance optique sur la lentille du capteur.	Court-circuiter les broches TEST et mettre sous tension pour passer dans le mode d'essai. Appuyer sur la touche REPEAT, le plateau s'ouvre et le LD émet de la lumière.	–	Quand l'alimentation est de 0,35mW, le niveau RF de 1,0Vc-c ou plus, TE (asservissement ouvert) de 2,0Vc-c ou plus et le réseau de diffraction aligné correctement, le capteur est acceptable.	(a)
2	VCO	–	Raccoder un compteur de fréquence entre CN8 broche 1 (PLCK)et GND. (X32-1250)	Couper l'alimentation, puis la refournir. Mode d'arrêt	L4 (X32-1250)	4,30MHz	(b)
3	RESEAU DE DIFFRACTION	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1960 CN2 broche 4) CH2: TE (X32-1250 broche 1)	Court-circuiter les broches TEST pour entrer en mode de test. Presser la touche CHECK pour vérifier que l'affichage est " 03 ".	–	Vérifier que le réseau de diffraction est correctement aligné. (Le réseau de diffraction ne peut pas être ajusté.)	(c)
4	BALANCE D'ERREUR D'ALIGNEMENT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1960 CN2 broche 4) CH2: TE (X32-1250 broche 1)	Court-circuiter les broches TEST pour entrer en mode de test. Presser la touche CHECK pour vérifier que l'affichage est " 03 ".	TE BALANCE VR1 (X29-1960)	Symétrie entre les formes supérieure et inférieure ou DC=0±0,05V	(d)
5	BALANCE D'ERREUR DE MISE AU POINT	Disque test Type 4	Raccorder un oscilloscope comme suit. CH1: RF (X29-1960 CN2 broche 4) CH2: FE (X32-1250 broche 3)	Presser la touche PLAY et s'assurer que l'affichage est " 05 ".	FE BALANCE VR2 (X29-1960)	Forme optimum	(e)
6	GAIN DE MISE AU POINT	Disque test Type 4 Appliquer un signal de 1,4kHz, 0,5Vrms à CN6 broche 2. (X32-1250)	Utiliser un gabarit d'asservisement ou raccorder un oscilloscope ou un voltmètre CC à la broche 1 de CN6 via un FPB de 47kΩ, 470pF.(X32-1250)	Couper l'alimentation puis la refournir. Presser la touche PLAY.	GAIN DE MISE AU POINT VR3 (X29-1960)	50mVrms	(f)
7	GAIN D'ALIGNEMENT	Disque test Type 4 Appliquer un signal de 1,4kHz, 0,5Vrms à CN6 broche 4. (X32-1250)	Utiliser un gabarit d'asservisement ou raccorder un oscilloscope ou un voltmètre CC à la broche 5 de CN6 via un FPB de 47kΩ, 470pF.(X32-1250)	PLAY	GAIN D'ALIGNEMENT VR4 (X29-1960)	50mVrms	(f)
8	DISTORSION DAC (MSB)	Disque test Type 4	Raccorder un compteur de distorsion sur la borne de sortie(FIXED).	Lire le signal 1kHz,-20dB dans la piste N°15.	VR1:G VR2:D (X32-1250)	Distorsion minimum	(g)
9	DISTORSION DAC (2SB)	Disque test Type 4	Raccorder un compteur de distorsion sur la borne de sortie(FIXED).	Lire le signal 100Hz, 0dB dans la piste N° 4.	VR3:G VR4:D (X32-1250)	Distorsion minimum	(g)

(Remarque)Disque de type 4:Disque test SONY YEDS-18 ou équivalent.

ABGLEICH

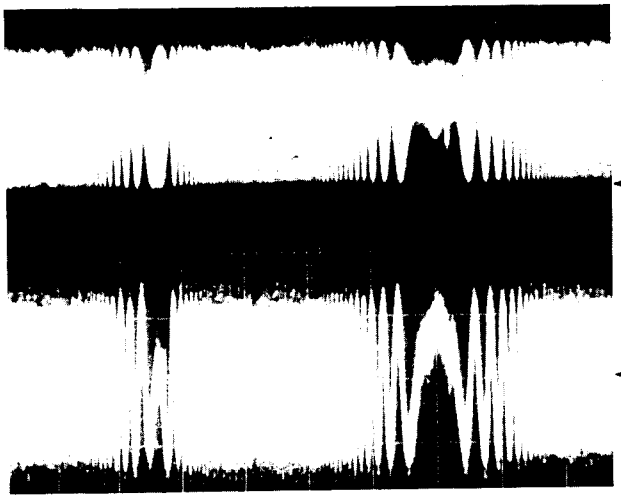
NR.	GEGENSTAND	EINGANGS-EINSTELLUN	AUSGANGS-EINSTELLUNGE	SPIELER-EINSTELLUNG	ABGLEICH-PUNKT	ABGLEICHUNG	ABB.
1	LASERLEISTUNG	–	Das Sensorteil des optischen Leistungmeters auf die Aufnehmerlinse ansetzen.	Die Stifte TEST kurzschließen und die Spannungsversorgung einschalten, um den Test-Modus zu aktivieren. Die Taste REPEAT drücken, dann öffnet sich der Träger, und die LD gibt Licht aus.	–	Wenn bei einer Spannung von 0,35mW der RF Pegel 1,0Vs-s oder mehr, TE (Servo Offen) 2,0Vs-s beträgt und das Beugungsgitter richtig ausgerichtet ist, ist der Abtaster in Ordnung.	(a)
2	VCO	–	Einen Frequenzzähler zwischen CN8 Stift 1 (PLCK) und GND anschließen. (X32-1250)	Die Spannungsversorgung einmal ausschalten und dann wieder einschalten. Stop-Betriebsart	L4 (X32-1250)	4,30MHz	(b)
3	OPTISCHES GITTER	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF (X29-1960 CN2 Stift 4) Kanal 2: TE (X32-1250 Stift 1)	Die Stifte TEST kurzschleißen, um den Testmodus zu aktivieren. Die CHECK-Taste drücken, um sicherzustellen, daß " 03 " angezeigt wird.	–	Prüfen, ob das Beugungsgitter richtig ausgerichtet ist.(Das Beugungsgitter kann nicht eingestellt werden.)	(c)
4	SPURHALTEFEHLER-AUSGLEICH	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF (X29-1960 CN2 Stift 4) Kanal 2: TE (X32-1250 Stift 1)	Die Stifte TEST kurzschleißen, um den Testmodus zu aktivieren. Die CHECK-Taste drücken, um sicherzustellen, daß " 03 " angezeigt wird.	TE BALANCE VR1 (X29-1960)	Symmetrie zwischen oberen und unteren Mustern oder Gleichstrom DC=0±0,05V	(d)
5	FOKUS-FEHLERAUSGLEICH	Testdisc Typ 4	Ein Oszilloskop wie folgt anschließen: Kanal 1: RF (X29-1960 CN2 Stift 4) Kanal 2: FE (X32-1250 Stift 3)	Die PLAY-Taste drücken und prüfen, daß " 05 " auf dem Display angezeigt wird.	FOKUS FEHLERAUSGLEICH VR2 (X29-1960)	Optimales Augenmuster	(e)
6	FOKUSVERSTÄRKUNG	Testdisc Typ 4 Ein Signal von 1,4kHz, 0,5Vrms an CN6 Stift 2 anlegen. (X32-1250)	Eine Servo-Lehre verwenden oder ein Oszilloskop oder einen Wechselstrom-Voltmeter an Stift 1 von CN6 über ein 47kΩ, 470pF Tiefpaßfilter anschließen. (X32-1250)	Die Spannungsversorgung einmal ausschalten und dann wieder einschalten. Die PLAY-Taste drücken.	FOKUSVERSTÄRKUNG VR3 (X29-1960)	50mVrms	(f)
7	SPURHALTE-VERSTÄRKUNG	Testdisc Typ 4 Ein Signal von 1,4kHz, 0,5Vrms an CN6 Stift 4 anlegen. (X32-1250)	Eine Servo-Lehre verwenden oder ein Oszilloskop oder einen Wechselstrom-Voltmeter an Stift 5 von CN6 über ein 47kΩ, 470pF Tiefpaßfilter anschließen. (X32-1250)	PLAY	SPURHALTE-VERSTÄRKUNG VR4	50mVrms	(f)
8	DAC-VERZERRUNG (MSB)	Testdisc Typ 4	Einen Verzerrungsmesser an die Ausgangsklemme(FIXED) anschließen.	Das 1kHz, -20dB Signal in Titel Nr.15 wiedergeben.	VR1: L VR2: R (X32-1250)	Minimale Verzerr ung	(g)
9	DAC-VERZERRUNG (2SB)	Testdisc Typ 4	Einen Verzerrungsmesser an die Ausgangsklemme(FIXED) anschließen.	Das 100Hz, 0dB Signal in Titel Nr.4 wiedergeben.	VR3: L VR4: R (X32-1250)	Minimale Verzerr ung	(g)

(Hinweis) Typ 4 Disc: SONY YEDS-18 Testdisc oder Äquivalent.

DP-8010

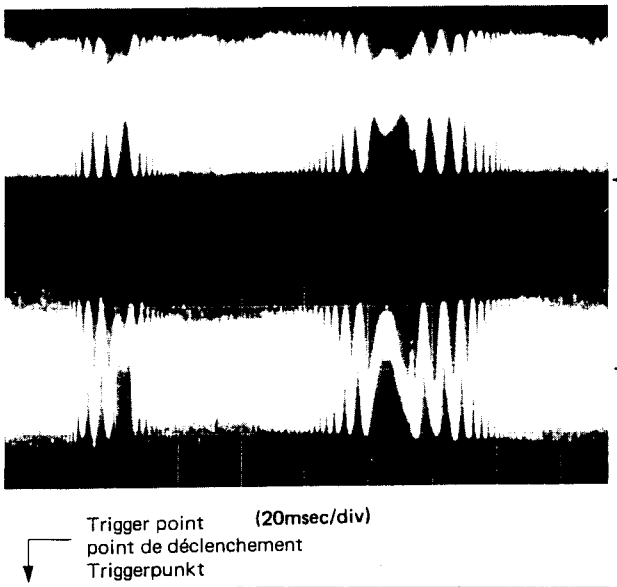
ADJUSTMENT/REGLAGE/ABGLEICH

DIFFRACTION GRID ADJUSTMENT/REGLAGE DU RESEAU DE DIFFRACTION/BEUGUNGSGITTER-EINSTELLUNG



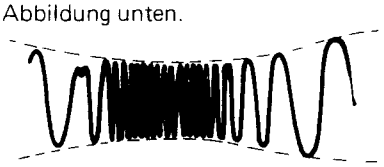
(Photo. 1)
(Photo. 1)
(Foto. 1)

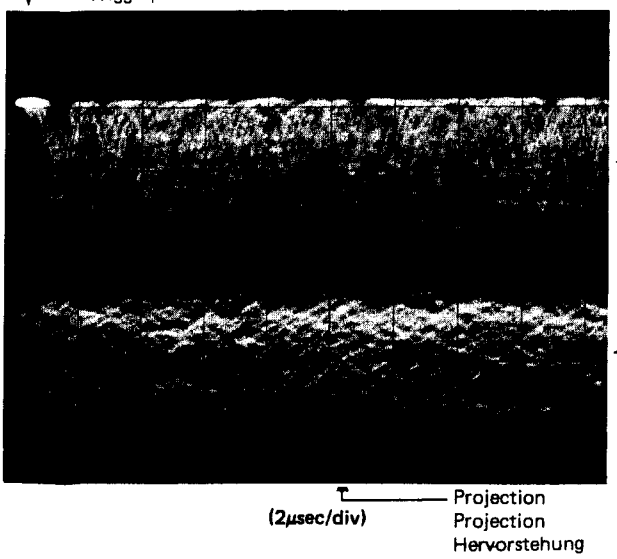
- RF signal and T.Error signal after diffraction grating adjustment.
- Signal RF et signal T.Error après ajustement de réseau de diffraction.
- RF-Signal und T.Error-Signal nach Diffraktions-gitter-Einstellung.



(Photo. 2)
(Photo. 2)
(Foto. 2)

- RF signal and T.Error signal when there is small diffraction grating position error.
- The T.Error signal level is small, and the envelope is as shown in the diagram below.
- Signal RF et signal T.Error quand il y a une petite erreur de position du réseau de diffraction.
- Le niveau de signal T.Error est petit et l'enveloppe est telle qu'indiquée dans le diagramme ci-dessous.
- RF-Signal und T.Error-Signal bei kleinem Diffraktions-gitter-Positionierungsfehler.
- Der T.Error-Signalpegel ist klein, und die Hüll-kurve ist wie in der Abbildung unten.

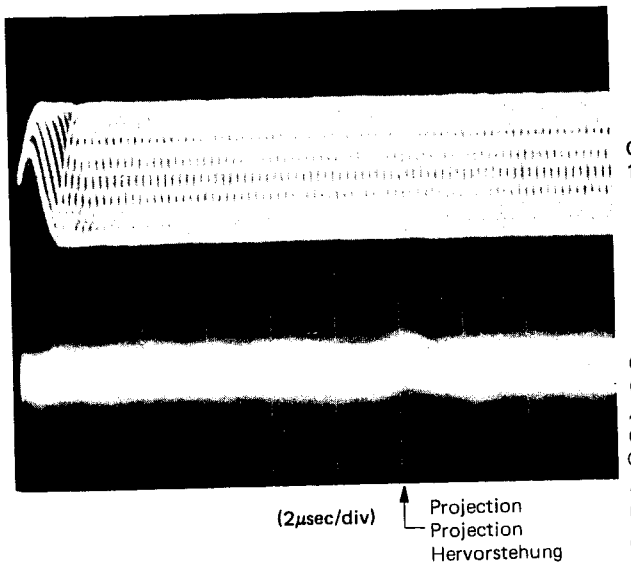




(Photo. 3)
(Photo. 3)
(Foto. 3)

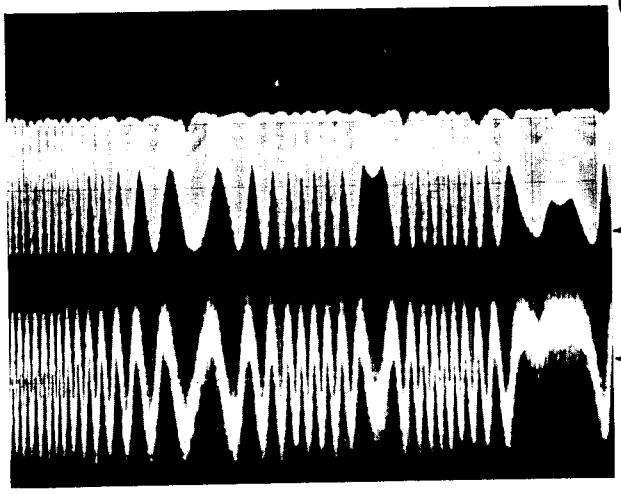
- RF signal and T.Error signal in test mode (with focusing ON).
- When the sub-beam traces the same bit series as the main beam during diffraction grating adjustment, bringing the RF trigger point to the position shown in the Photo causes a "projection" to be observies in the T.Error waveform.
- Le signal RF et le signal T.Error en mode de test (avec la mise au point sur ON).
- Quand un faisceau auxiliaire tracela même série de bits que le faisceau principal pendant l'ajustement de réseau de diffraction, l'apport du point de déclenchement RF à la position indiquée dans la photo provoque une "projection" qui s'observe dans la forme d'onde d' T.Error.
- RF-Signal und T.Error-Signal im Testmodus (bei eingeschalteter Fokussierung).
- Wenn der Nebenstrahl die gleiche Bitreihe wie der Hauptstrahl während der Diffraktionsgitter-Einstellung verfolgt und den RF-Triggerpunkt auf die im Foto gezeigte Position bringt, wird eine "Hervorstehung" verursacht, die in der T.Error-Wellenform beobachtet werden kann.

ADJUSTMENT/REGLAGE/ABGLEICH



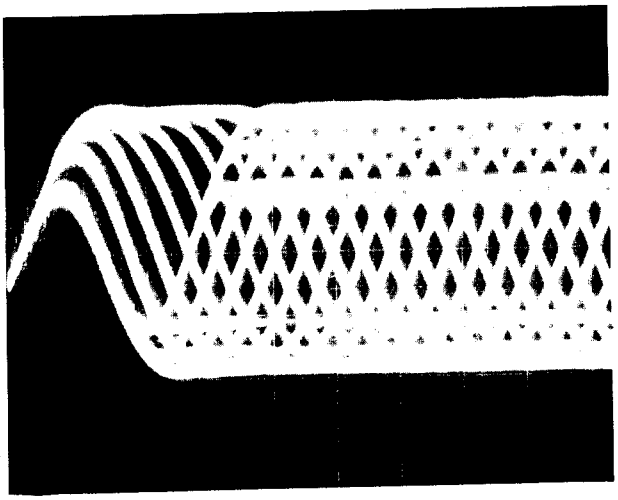
(Photo. 4)
(Photo. 4)
(Foto. 4)

- RF signal and E.Spot signal in test mode (PLAY).
- If the diffraction grating has been adjusted properly, the influence of triggering is observed on the E.Spot waveform of approx. 12μs after RF signal, in the form of a projection.
- Signal RF et signal E.Spot en mode de test (PLAY).
- Si le réseau de diffraction a été ajusté correctement, l'influence du déclenchement s'observe sur la forme d'onde E.Spot d'environ 12μs après le signal RF, sous la forme d'une projection.
- RF-Signal und E.Spot-Signal im Testmodus (PLAY).
- Wenn das Diffraktionsgitter richtig eingestellt wurde, wird der Einfluß des Triggers in der E.Spot-Wellenform etwa 12μs nach dem RF-Signal in der Form einer Hervorstehung beobachtet.



(Photo. 5)
(Photo. 5)
(Foto. 5)

- RF signal and T.Error signal; in test mode (Focusing ON). (Disc type 4)
- Adjust T.Error so that the waveform is symmetrical above and below 0V. (VR1 of X29-1960)
- Signal RF et signal T.Error; en mode test (mise au point ON). (Disque de type 4)
- Ajuster T.Error pour que la forme d'onde soit symétrique en-dessus et au-dessous de 0V. (VR1 de X29-1960)
- RF-Signal und T.Error-Signal; im Testmodus (Fokussierung eingeschaltet). (Disc-Typ 4)
- T.Error so einstellen, daß die Wellenform über und unter 0V symmetrisch ist. (VR1 von X29-1960)



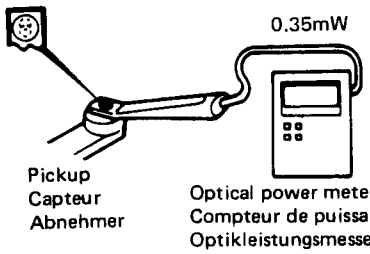
(Photo. 6)
(Photo. 6)
(Foto. 6)

- RF signal in test mode (PLAY).
- Perform the tangential and focusing offset adjustments so that each of the center cross points are focused into one point on the display. The crossing points above and below the center shall also be displayed clearly.
- Signal RF en mode de test (PLAY).
- Effectuer les ajustements d'offset tangentiel et de mise au point pour que chacun des points de croisement central soit mis au point sur un point de l'affichage. Les points de croisement au-dessus et en-dessous du centre doivent aussi être affichés clairement.
- RF-Signal im Testmodus (PLAY).
- Die Tangential- und Fokusversatz-Einstellungen so durchführen, daß jeder der mittleren Kreuzungspunkte in einem Punkt auf dem Display fokussiert wird. Auch die Kreuzungspunkte über und unter der Mitte müssen klar angezeigt werden.

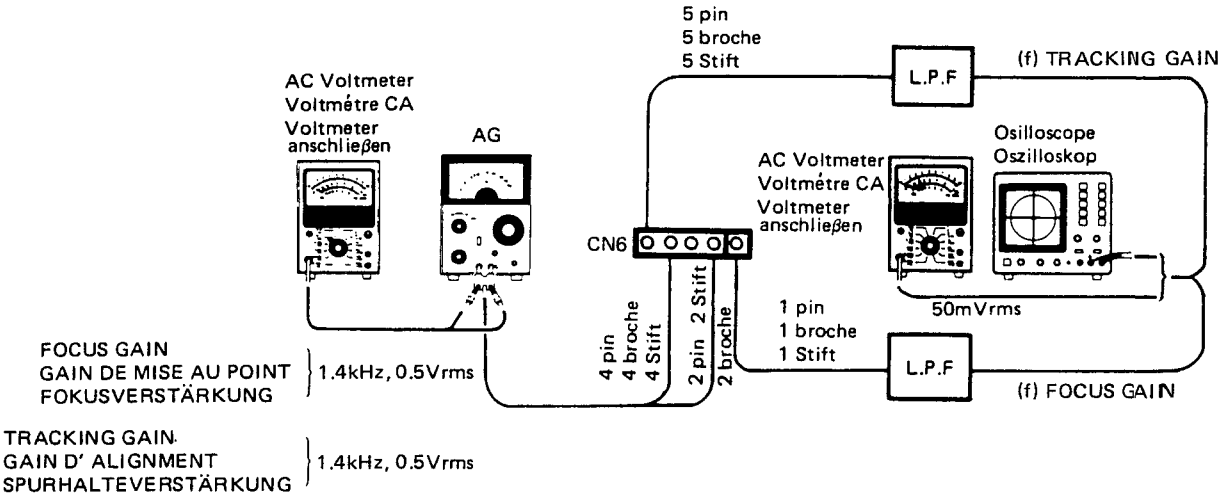
DP-8010

ADJUSTMENT/REGLAGE/ABGLEICH

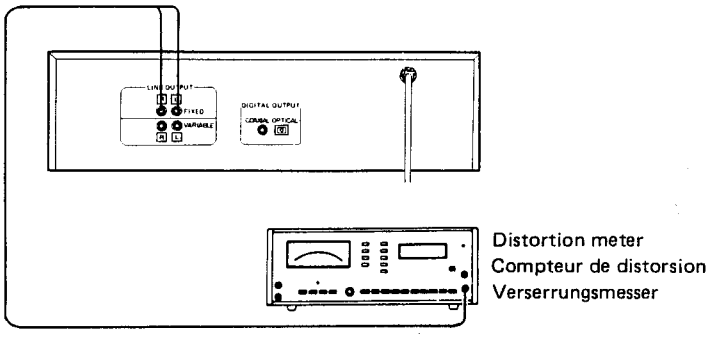
(a) Laser Power



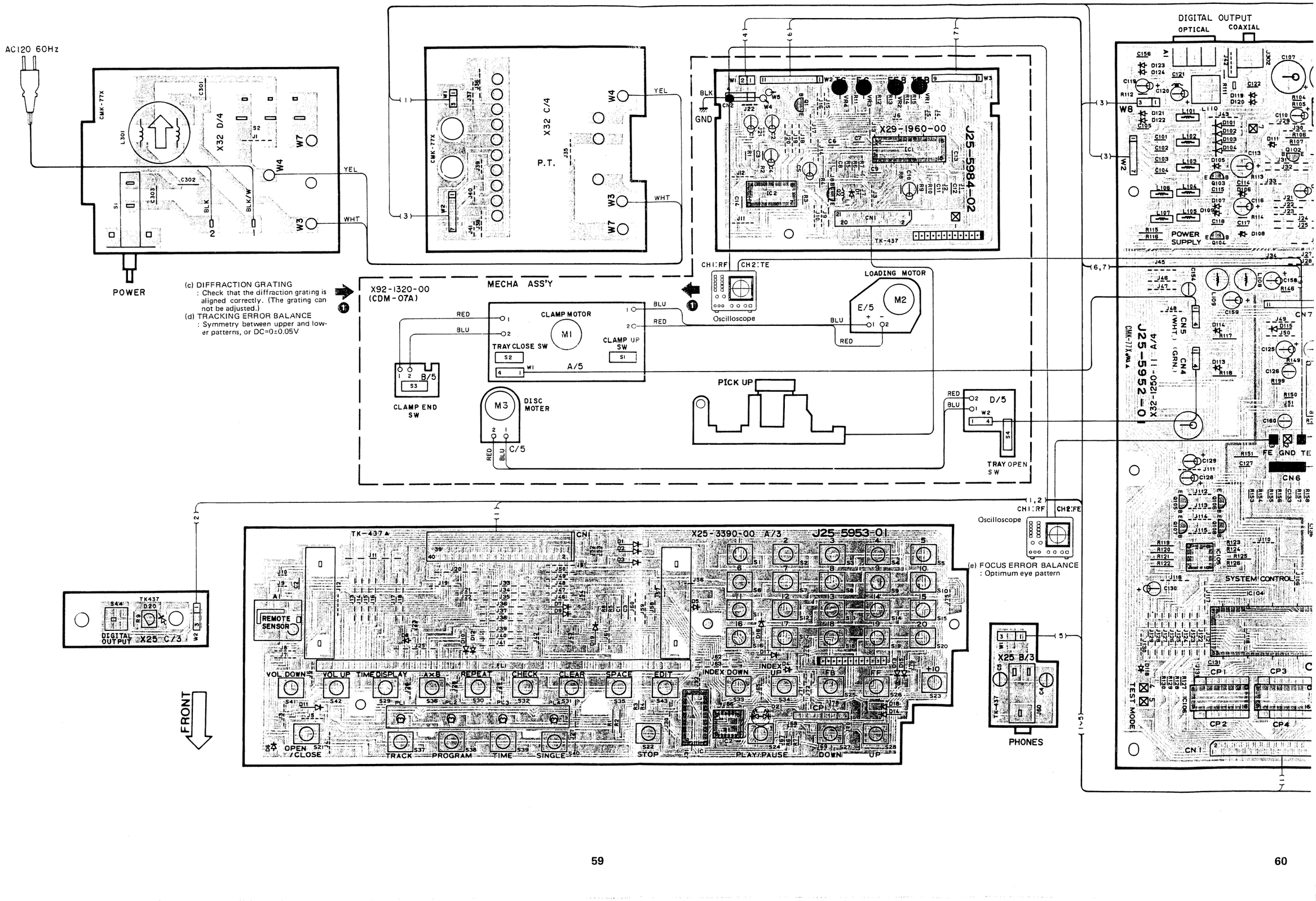
(f) Focus Gain and Tracking Gain

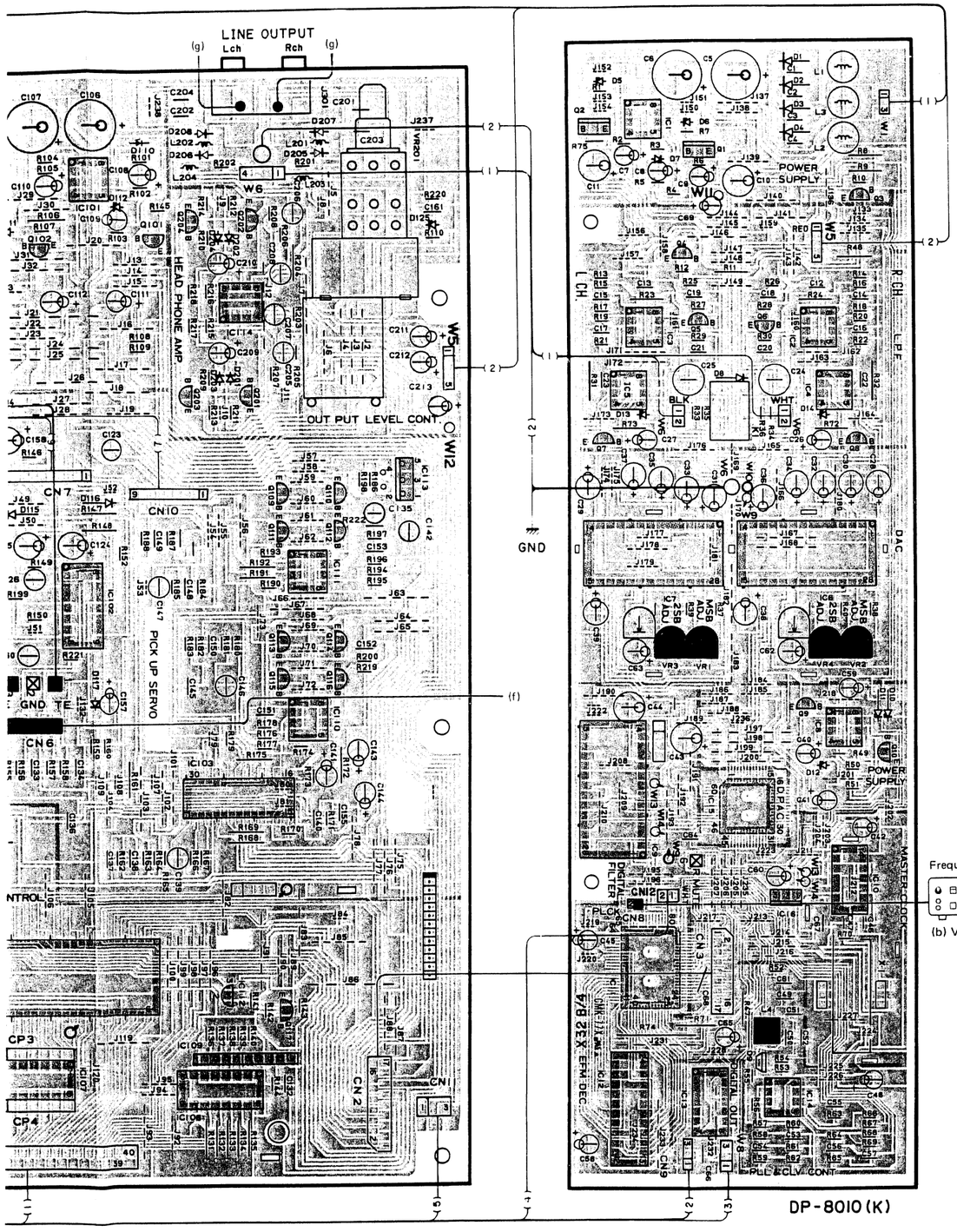


(g) DAC Distortion



PC BOARD (COMPONENT SIDE VIEW)





Refer to the schematic diagram for the values of resistors and capacitors.

(X32-1250-XX)

IC1

1	-3.3V
2,3	0V
4	-16.7V
5,6	5.5V
7	0.9V
8	15.8V

IC2,3

1~3	0V
4	-11.8V
5~7	0V
8	11.6V

IC4

1	5.7V
2	5.1V
3	5.0V
4	-11.8V
5~7	0V
8	11.6V

IC5

1~3	0V
4	-11.8V
5	5.0V
6	5.1V
7	5.7V
8	11.6V

IC6

1	0.7V
2	5.1V
3	-6.1V
4	3.1V
6,8	0V
9	-11.3V
11	0V
13	5.1V
15	3.4V
16	1.9V
17	3.6V
19	0V
20	-11.8V
26	-10.9V
27	-10.8V
28	-10.2V

IC7

1	0.7V
2	5.1V
3	-6.1V
4	3.1V
6,8	0V
9	-11.8V
11	0V
13	5.1V
15	3.4V
16	1.9V
17	3.8V
19	0V(2.0V)
20	-11.8V
26,27	-10.9V
28	-10.2V

IC8

1	5.7V
2,3	5.0V
4	-11.7V
5,6	0V
7	-5.6V
8	11.6V

IC9

1	0V
2	2.4V
3,4	5.1V
6	2.3V
8	0V
9	2.3V
10	0V
14	5.0V
15,16	0V
17	5.1V
21	0V
22	5.1V
23,24	0V
25	3.8V
28	2.5V

IC10

1	2.3V
2	2.9V
3	2.7V
4,5	2.9V
6	2.8V
7	0V
8	2.7V
9	2.5V
14	5.1V

IC11

1~4	0V
5	0V(4.2V)
6	0V(4.5V)
7	0V
8,9	2.4V
10	0V
11	2.5V
12	0V
13~16	5.1V
17	0V(4.5V)
18,19	5.1V(0V)
20~24	0V
25	2.5V
26	0V
27	2.5V
28	0V
29~31	0.6V
32	2.8V
33	5.0V
34,35	2.8V
36	2.2V
37	4.5V
38~45	2.5V
46~49	4.4V
50,51	2.3V
52	0V
53	2.9V
54	2.1V
55,56	0V
57	5.0V
58,59	0V
70	2.4V
73	5.0V
76	2.5V
78	0V(2.4V)
80	2.5V

IC12

1~8	2.5V
9,10	2.8V
11	0.6V
12	0V
13,14	0.6V
15	2.8V
16	2.2V
17	4.3V
18	2.3V
19	2.5V
20	2.3V
21	4.4V
22,23	2.5V
24	5.0V

IC13

9	2.5V
10	0V
11	2.7V
12	2.5V
13	0V(5.0V)

IC14

1	0V
2,3	2.5V
4	-5.1V
5~7	0V
8	5.0V

IC15

1	1.9V
2	3.8V
4,5	0V(2.0V)
6	5.1V
8,10	0V
11,13	0V
14	5.1V
15,17	0V
22	0V
23	5.1V
24,26	0V
28~30	0V
32	0V
33	2.9V
35	0V
37~40	0V
41,42	5.1V
43~45	0V
47	2.9V
48	3.8V
49,50	0V
51,53	5.1V
56	0V
57,58	2.3V
60	0V

IC16

1	15.9V
2	0V
3	5.0V

IC101

1	-4.0V
2,3	0V
4	-9.0V
5,6	4.7V
7	3.8V
8	8.9V

IC102

1~4	0V
5	-4.6V
6	0V
7	-5.1V
8	0V
9	4.7V
10~15	0V
16	5.1V

IC103

1~4	0V
5	5.1V
6	0V
7	5.1V
8~13	0V
14	-4.3V
15	5.1V
16	0V
17	-5.1V
18	4.7V
19	0V
20	0.2V
21~25	0V
26	5.1V
27	-0.6V
28~30	0V

IC104

1	-6.7V
2	-4.4V
3,4	-4.3V
5	5.1V
6	2.5V
7	0V
8,9	5.1V
10~14	0V
15,16	5.1V
19	5.1V
20	0.6V
21~24	0V
25~28	5.1V
30	2.4V
32	0V
35~38	0V
39	5.0V
40~51	0.3V
54	-20.6V
55	-15.8V
56	-28.0V
57	-5.1V
58	-18.4V
59	-9.0V
60,61	-27.7V
62,63	-11.3V
64	5.1V

IC105

1	0.5V
2,3	0V
4	-9.0V
5,6	0V
7	0.5V
8	8.9V

IC106,107

1~6	0.3V
7	0V
8	5.1V
9	-28.1V
11~16	-25.7V

IC108

1	0V
2~4	3.9V
5,6	0.2V
7	0V
8	5.1V
9	-28.1V
11,12	-27.7V
13~15	3.8V

IC109

1,2	0.2V
3,4	3.9V
5	0V
6	3.9V
7	0.9V
8	0V
9	5.1V

IC110

1	-1.0V
2,3	0V
4	-9.0V
5,6	0V
7	-0.6V
8	8.9V

IC111

1~3	0V
4	-9.0V
5,6	0V
7	-0.7V
8	8.9V

IC112

1	5.1V
2	0V
3	5.1V

IC113

1,2	0V
3	-9.0V
4	0V
5	8.9V

IC114

1	-0.4V
2,3	0V
4	-11.3V
5,6	0V
7	0.4V
8	11.6V

	B	C	E
Q1	12.1V	11.6V	15.9V
Q2	-16.7V	-16.1V	-11.8V
Q3	-11.8V	-11.8V	6.8V
Q4	-11.8V	-11.8V	0V
Q5,6	0.7V	0V	0V
Q7~9	5.7V	5.1V	11.6V
Q10	-5.6V	-11.7V	-5.1V
Q101	8.8V	8.9V	5.1V
Q102	-8.3V	-9.0V	-5.1V
Q103	8.1V	7.5V	12.6V
Q104	-28.7V	-28.1V	-38.9V
Q105,107	0.5V	0V	-9.0V
Q106,108	0.5V	0V	8.9V
Q109	-0.7V	0V	-9.0V
Q110	-0.7V	0V	8.9V
Q111	-0.6V	0V	-9.0V
Q112	-0.6V	0V	8.9V
Q113	-1.0V	-0.3V	-9.0V
Q114	-1.0V	-0.3V	8.9V
Q115	-0.6V	0V	-9.0V
Q116	-0.6V	0V	8.9V
Q117	-	-	5.1V

(X29-1960-00)

IC1

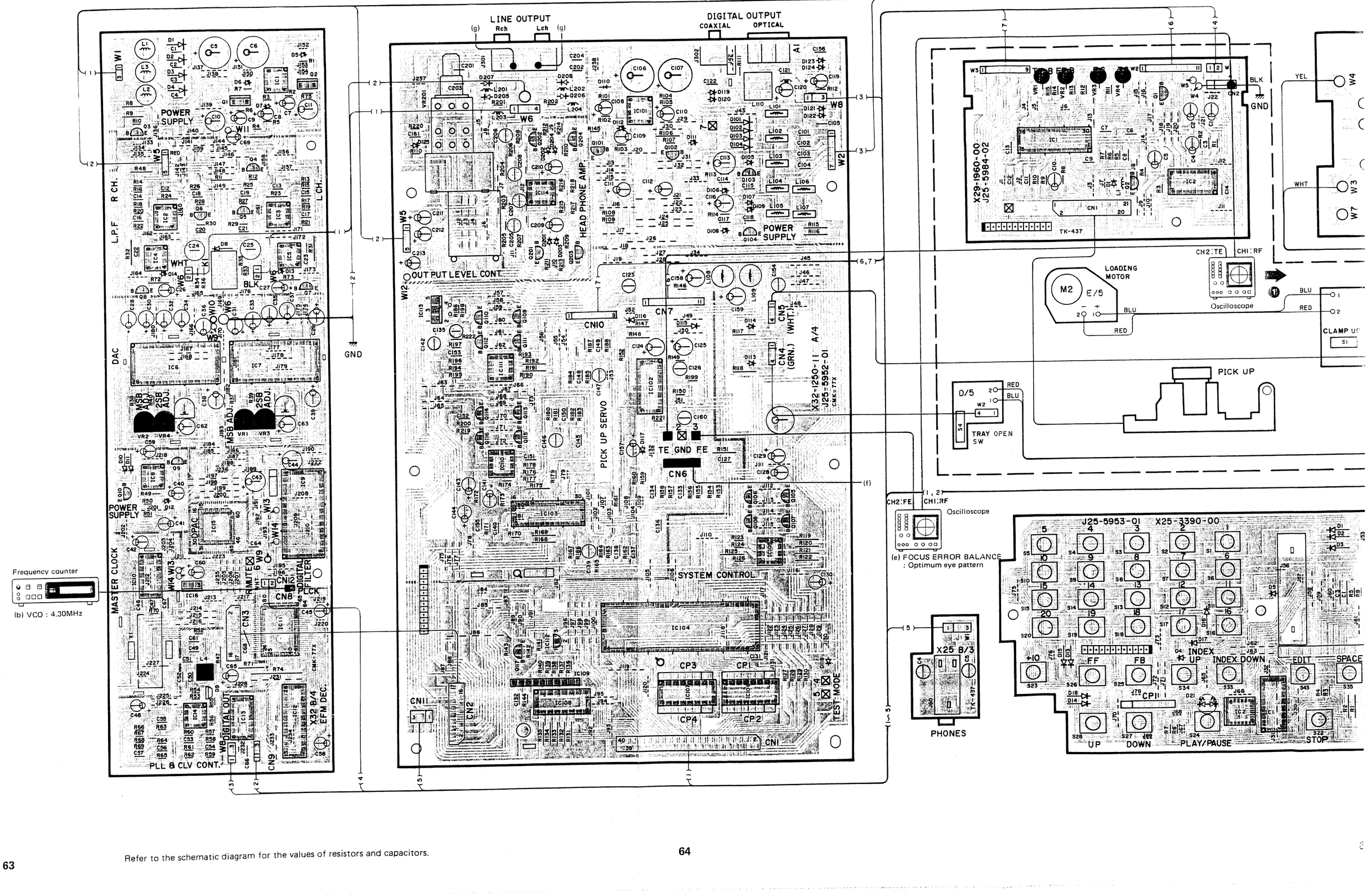
1~3	0V
5	4.7V(0V)
6	-5.1V
7~14	0V
15	-11V
16	1.3V
17	-5.1V
18~20	0V
21	-5.1V
22	0V
23	-3.7V
24~26	0V
27	4.3V
28	0V
29,30	5.1V

IC2

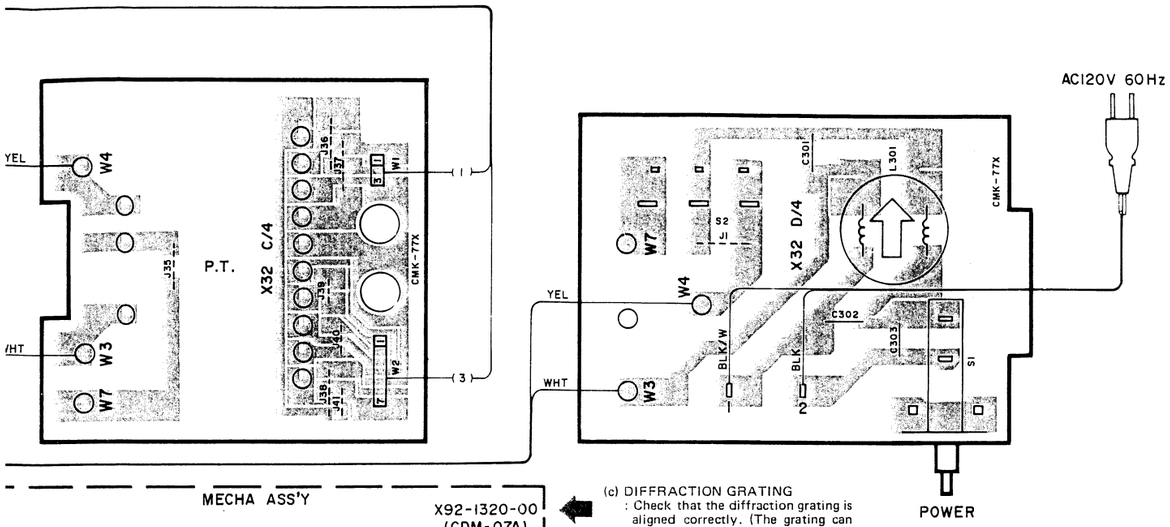
9	4.3V
10	0V
14	5.1V

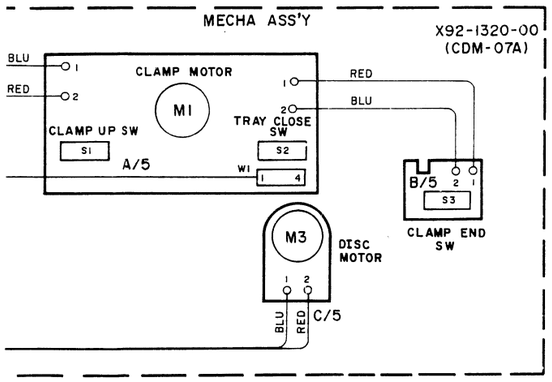
	B	E	C
Q1	0.6V	0V	0V
Q2	4.7V (0V)	5.1V	0V (5.1V)

PC BOARD (FOIL SIDE VIEW)



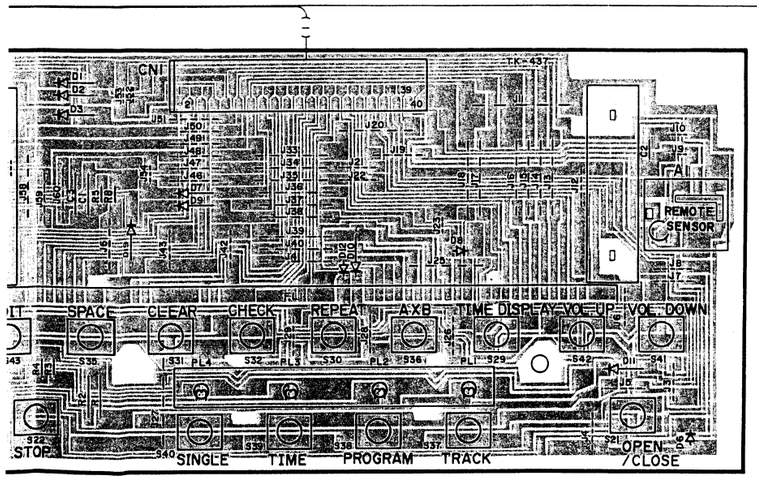
Refer to the schematic diagram for the values of resistors and capacitors.

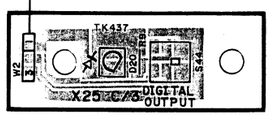




(c) DIFFRACTION GRATING
: Check that the diffraction grating is aligned correctly. (The grating can not be adjusted.)

❶ (d) TRACKING ERROR BALANCE
: Symmetry between upper and lower patterns, or DC=0±0.05V





FRONT

DP-8010(K)

(X32-125X-XX)

IC1

1	-3.3V
2,3	0V
4	-16.7V
5,6	5.5V
7	0.9V
8	15.8V

IC2,3

1~3	0V
4	-11.8V
5~7	0V
8	11.6V

IC4

1	5.7V
2	5.1V
3	5.0V
4	-11.8V
5~7	0V
8	11.6V

IC5

1~3	0V
4	-11.8V
5	5.0V
6	5.1V
7	5.7V
8	11.6V

IC6

1	0.7V
2	5.1V
3	-6.1V
4	3.1V
6,8	0V
9	-11.8V
11	0V
13	5.1V
15	3.4V
16	1.9V
17	3.6V
19	0V
20	-11.8V
26	-10.9V
27	-10.8V
28	-10.2V

IC7

1	0.7V
2	5.1V
3	-6.1V
4	3.1V
6,8	0V
9	-11.8V
11	0V
13	5.1V
15	3.4V
16	1.9V
17	3.8V
19	0V(2.0V)
20	-11.8V
26,27	-10.9V
28	-10.2V

IC8

1	5.7V
2,3	5.0V
4	-11.7V
5,6	0V
7	-5.6V
8	11.6V

IC9

1	0V
2	2.4V
3,4	5.1V
6	2.3V
8	0V
9	2.3V
10	0V
14	5.0V
15,16	0V
17	5.1V
21	0V
22	5.1V
23,24	0V
25	3.8V
28	2.5V

IC10

1	2.3V
2	2.9V
3	2.7V
4,5	2.9V
6	2.8V
7	0V
8	2.7V
9	2.5V
14	5.1V

IC11

1~4	0V
5	0V(4.2V)
6	0V(4.5V)
7	0V
8,9	2.4V
10	0V
11	2.5V
12	0V
13~16	5.1V
17	0V(4.5V)
18,19	5.1V(0V)
20~24	0V
25	2.5V
26	0V
27	2.5V
28	0V
29~31	0.6V
32	2.8V
33	5.0V
34,35	2.8V
36	2.2V
37	4.5V
38~45	2.5V
46~49	4.4V
50,51	2.3V
52	0V
53	2.9V
54	2.1V
55,56	0V
57	5.0V
58,59	0V
70	2.4V
73	5.0V
76	2.5V
78	0V(2.4V)
80	2.5V

IC12

1~8	2.5V
9,10	2.3V
11	0.6V
12	0V
13,14	0.6V
15	2.8V
16	2.2V
17	4.3V
18	2.3V
19	2.5V
20	2.3V
21	4.4V
22,23	2.5V
24	5.0V

IC13

9	2.5V
10	0V
11	2.7V
12	2.5V
13	0V(5.0V)

IC14

1	0V
2,3	2.5V
4	-5.1V
5~7	0V
8	5.0V

IC15

1	1.9V
2	3.8V
4,5	0V(2.0V)
6	5.1V
8,10	0V
11,13	0V
14	5.1V
15,17	0V
22	0V
23	5.1V
24,26	0V
28~30	0V
32	0V
33	2.9V
35	0V
37~40	0V
41,42	5.1V
43~45	0V
47	2.9V
48	3.8V
49,50	0V
51,53	5.1V
56	0V
57,58	2.3V
60	0V

IC16

1	15.9V
2	0V
3	5.0V

IC101

1	-4.0V
2,3	0V
4	-9.0V
5,6	4.7V
7	3.8V
8	8.9V

IC102

1~4	0V
5	-4.6V
6	0V
7	-5.1V
8	0V
9	4.7V
10~15	0V
16	5.1V

IC103

1~4	0V
5	5.1V
6	0V
7	5.1V
8~13	0V
14	-4.3V
15	5.1V
16	0V
17	-5.1V
18	4.7V
19	0V
20	0.2V
21~25	0V
26	5.1V
27	-0.6V
28~30	0V

IC104

1	-6.7V
2	-4.4V
3,4	-4.3V
5	5.1V
6	2.5V
7	0V
8,9	5.1V
10~14	0V
15,16	5.1V
19	5.1V
20	0.6V
21~24	0V
25~28	5.1V
30	2.4V
32	0V
35~38	0V
39	5.0V
40~51	0.3V
54	-20.6V
55	-15.8V
56	-28.0V
57	-5.1V
58	-18.4V
59	-9.0V
60,61	-27.7V
62,63	-11.3V
64	5.1V

IC105

1	0.5V
2,3	0V
4	-9.0V
5,6	0V
7	0.5V
8	8.9V

IC106,107

1~6	0.3V
7	0V
8	5.1V
9	-28.1V
11~16	-25.7V

IC108

1	0V
2~4	3.9V
5,6	0.2V
7	0V
8	5.1V
9	-28.1V
11,12	-27.7V
13~15	3.8V

IC109

1,2	0.2V
3,4	3.9V
5	0V
6	3.9V
7	0.9V
8	0V
9	5.1V

IC110

1	-1.0V
2,3	0V
4	-9.0V
5,6	0V
7	-0.6V
8	8.9V

IC111

1~3	0V
4	-9.0V
5,6	0V
7	-0.7V
8	8.9V

IC112

1	5.1V
2	0V
3	5.1V

IC113

1,2	0V
3	-9.0V
4	0V
5	8.9V

IC114

1	-0.4V
2,3	0V
4	-11.3V
5,6	0V
7	0.4V
8	11.6V

	B	C	E
Q1	12.1V	11.6V	15.9V
Q2	-16.7V	-16.1V	-11.8V
Q3	-11.8V	-11.8V	6.8V
Q4	-11.8V	-11.8V	0V
Q5,6	0.7V	0V	0V
Q7~9	5.7V	5.1V	11.6V
Q10	-5.6V	-11.7V	-5.1V
Q101	8.8V	8.9V	5.1V
Q102	-8.3V	-9.0V	-5.1V
Q103	8.1V	7.5V	12.6V
Q104	-28.7V	-28.1V	-38.9V
Q105,107	0.5V	0V	-9.0V
Q106,108	0.5V	0V	8.9V
Q109	-0.7V	0V	-9.0V
Q110	-0.7V	0V	8.9V
Q111	-0.6V	0V	-9.0V
Q112	-0.6V	0V	8.9V
Q113	-1.0V	-0.3V	-9.0V
Q114	-1.0V	-0.3V	8.9V
Q115	-0.6V	0V	-9.0V
Q116	-0.6V	0V	8.9V
Q117	-	-	5.1V

(X29-1960-00)

IC1

1~3	0V
5	4.7V(0V)
6	-5.1V
7~14	0V
15	-11V
16	1.3V
17	-5.1V
18~20	0V
21	-5.1V
22	0V
23	-3.7V
24~26	0V
27	4.3V
28	0V
29,30	5.1V

IC2

9	4.3V
10	0V
14	5.1V

	B	E	C
Q1	0.6V	0V	0V
Q2	4.7V (0V)	5.1V	0V (5.1V)

(X29-1960-00)
IC1 : CXA1081S
IC2 : TC74HC00P

Q1 : 2SC945(A)(Q,P)
or 2SC1740S(Q,R)
Q2 : 2SA1426

D1 : HSS104 or ISS133

D1 ~ 3 : S5566B

MECHA. ASS'Y (X92-1320-00) (CDM-07) ( ) : AT PLAY

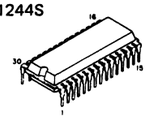
(X32-1250-00)

IC101, 105, 110, 111	: NJM4558D
IC102	: μPD4053BC
IC103	: CXA1244S
IC104	: μPD75212ACW-051
IC106 ~ 108	: LB1294
IC109	: LB1433N
IC112	: M51951ASL
IC113	: LA6500
IC114	: μPC4570C-A

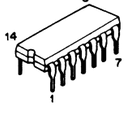
Q101, 104, 105, 107, 109, 111, 113, 115, 203, 204	: 2SA1534A
Q102, 103, 106, 108, 110, 112, 114, 116, 201, 202	: 2SC3940A
Q117	: 2SC945(A)(Q,P) or 2SC1740S(Q,R)

D101 ~ 104	: S5566B
D105, 113 ~ 117, 119 ~ 124, 201 ~ 208	: ISS133 or HSS104
D106, 109	: RD8.2ES(B) or HZS8.2N(B)
D107, 118	: ISS131 or HSS104A
D108	: RD30ES(B) or HZS30N(B)
D110 ~ 112	: RD4.7ES(B) or HZS4.7N(B)
D125	: RD3.9ES(B) or HZS3.9N(B)

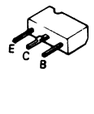
CXA1081S
CXA1244S



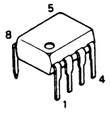
TC74HC00P



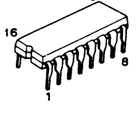
2SA1426



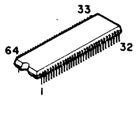
NJM4558D



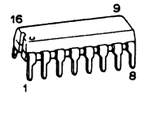
TD62003AP
μPD4053BC



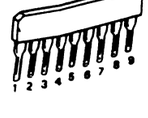
μPD75212ACW-051



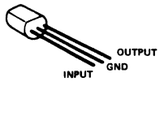
LB1294



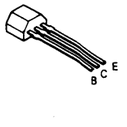
LB1433N

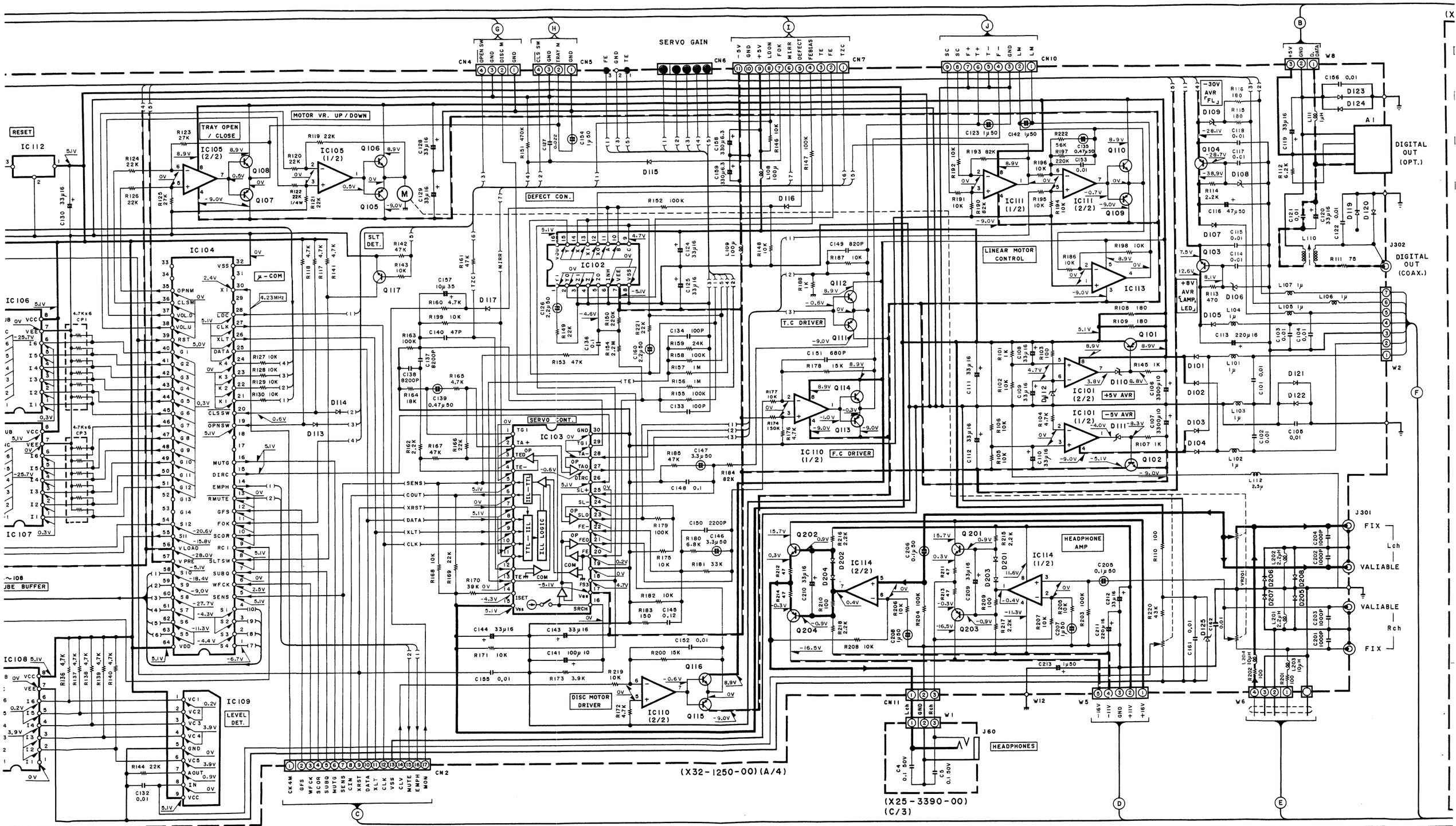


M51951ASL

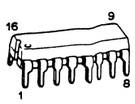


2SC1740S

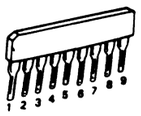




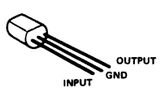
LB1294



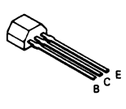
LB1433N



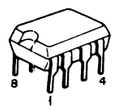
M51951ASL



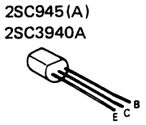
2SC1740S



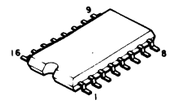
μPC4570C-A



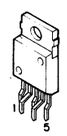
2SA1534A
2SC945(A)
2SC3940A



TC74HC174F

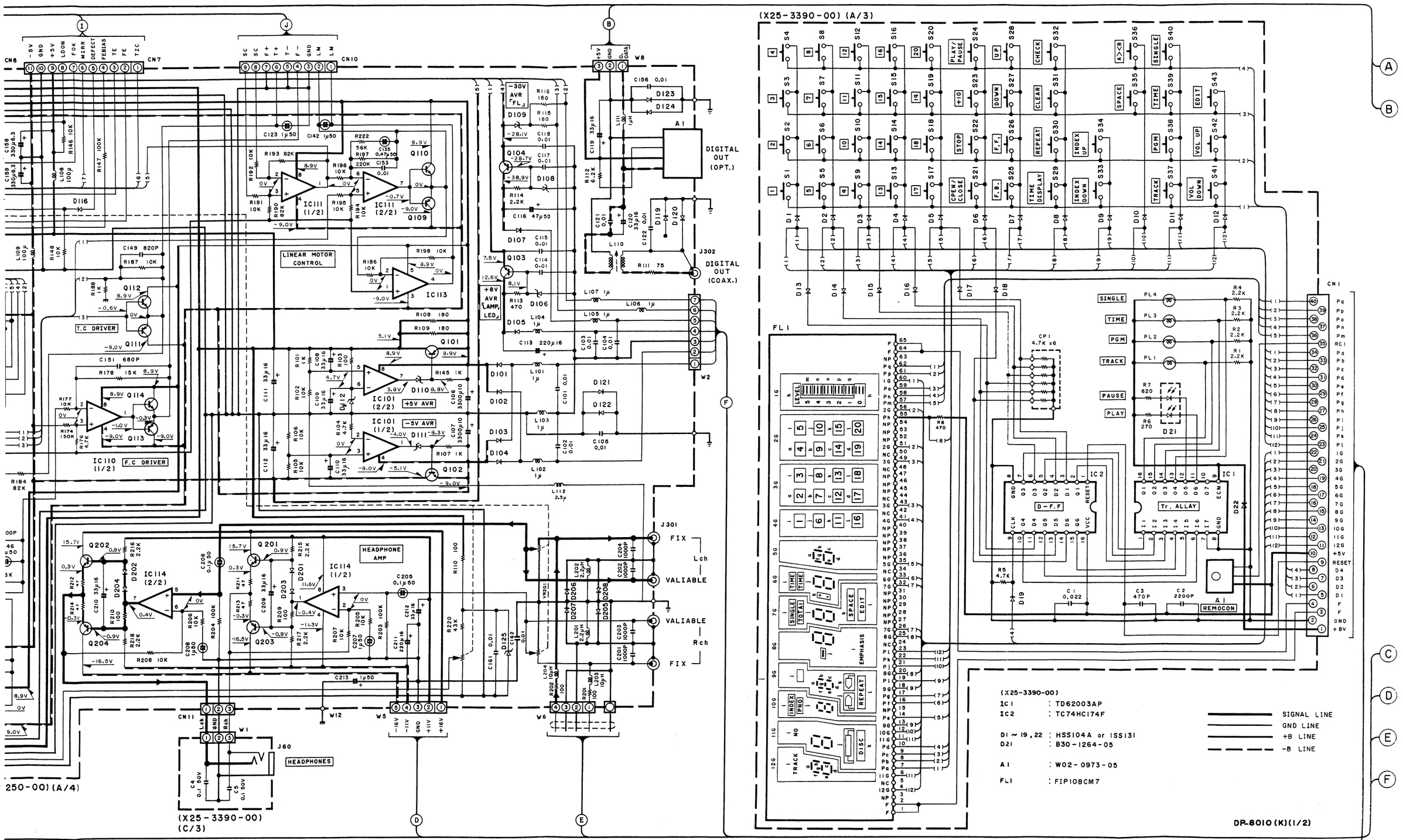


LA6500

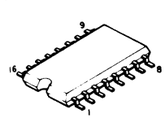


CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

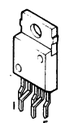
- DC voltages are as m voltmeter. Values ma between individual ins
- Les tensions c.c. doiv mètre à haute impéda légèrement du fait appareils et aux ins



TC74HC174F



LA6500

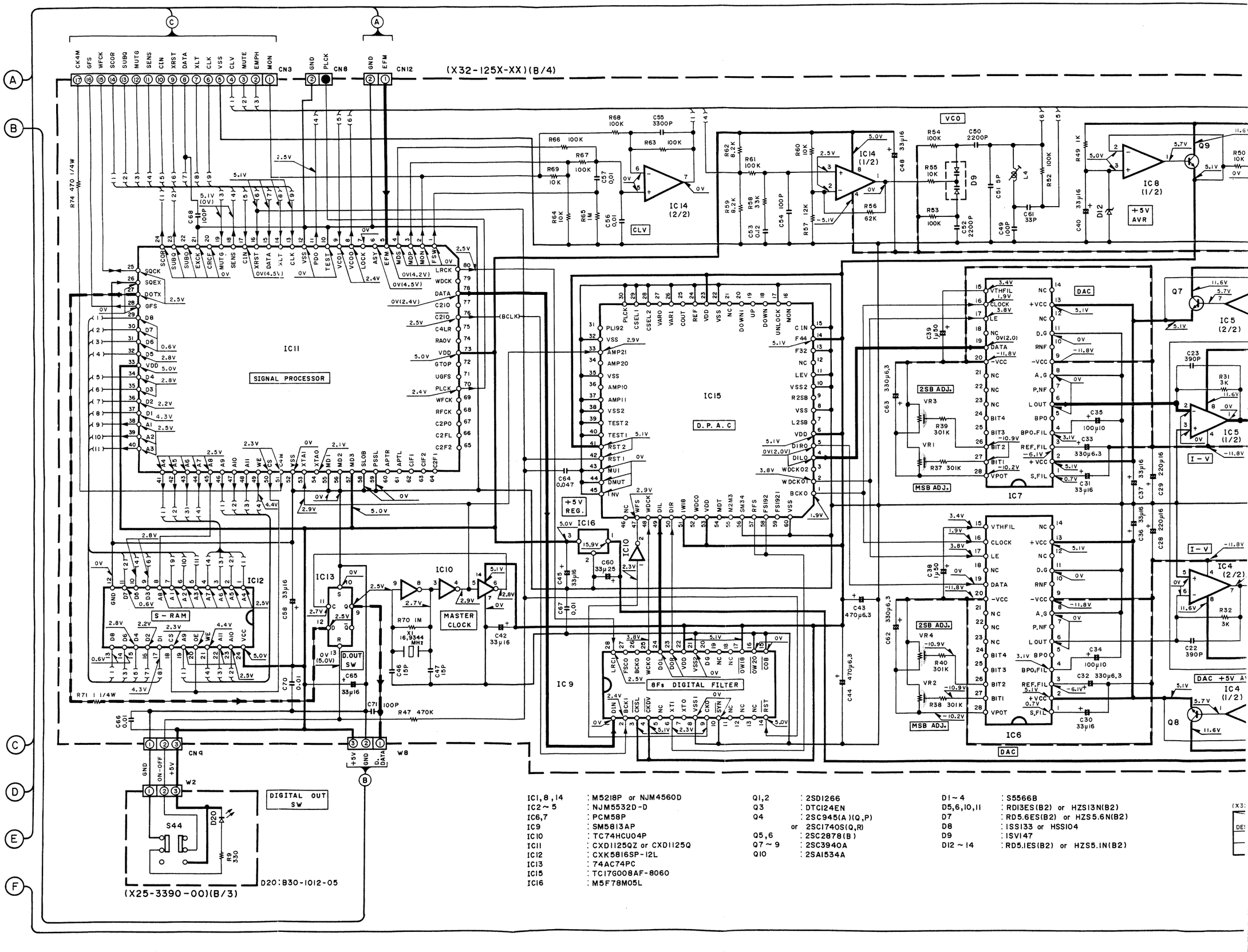


CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

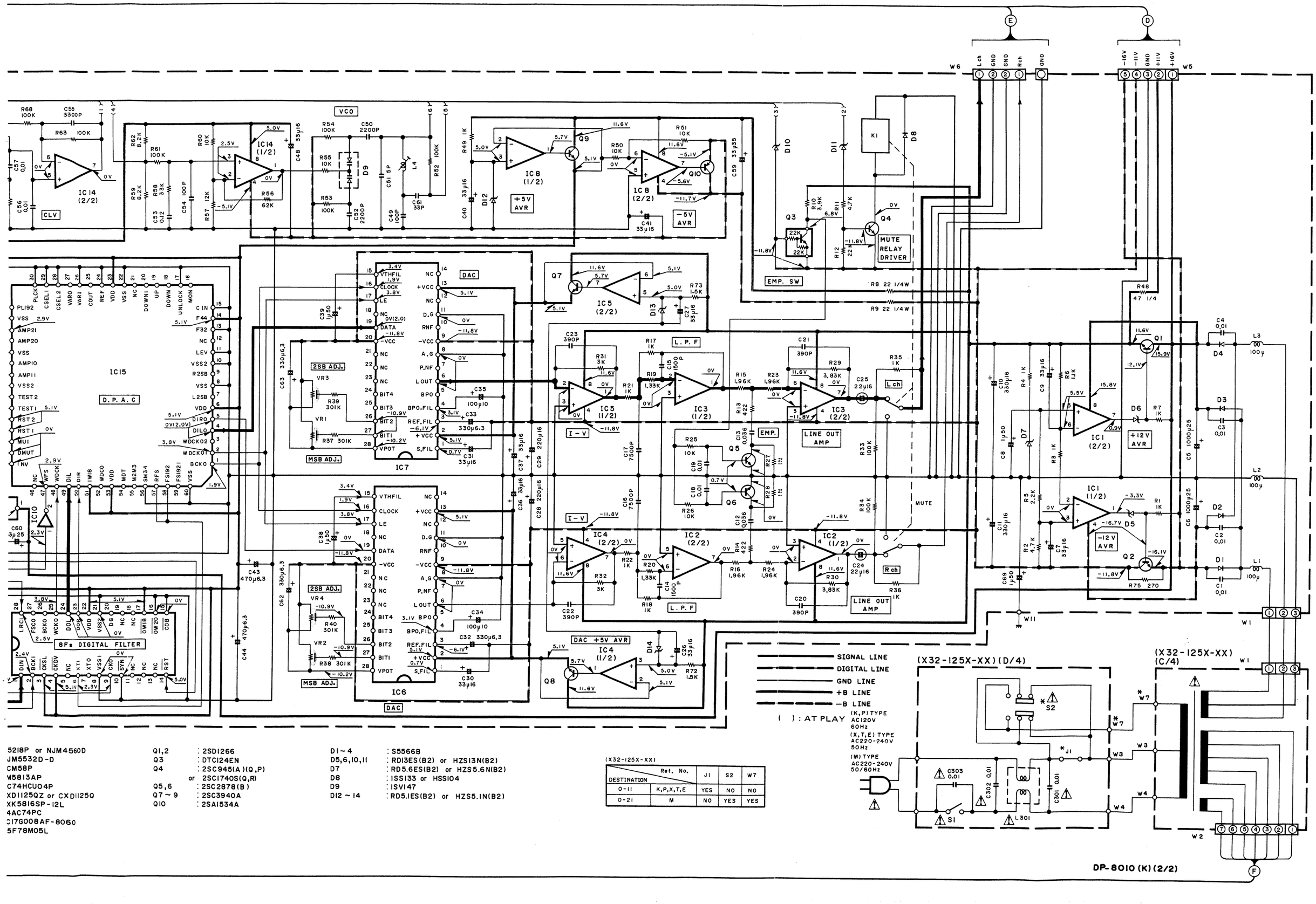
- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
- Les tensions c.c. doivent être measurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.
- Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Voltmeter gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen instrumenten oder Geräten u.U. geringfügig.

Y22-1560-11

DP-8010
KENWOOD



IC1,8,14	: M5218P or NJM4560D	Q1,2	: 2SD1266	D1~4	: S5566B
IC2~5	: NJM5532D-D	Q3	: DTC124EN	D5,6,10,11	: RD13ES(B2) or HZS13N(B2)
IC6,7	: PCM58P	Q4	: 2SC945(A)(Q,P)	D7	: RD5.6ES(B2) or HZS5.6N(B2)
IC9	: SM5813AP		or 2SC1740S(Q,R)	D8	: ISS133 or HSS104
IC10	: TC74HCU04P	Q5,6	: 2SC2878(B)	D9	: ISV147
IC11	: CXD1125QZ or CXD1125Q	Q7~9	: 2SC3940A	D12~14	: RD5.1ES(B2) or HZS5.1N(B2)
IC12	: CXK5816SP-12L	Q10	: 2SA1534A		
IC13	: 74AC74PC				
IC15	: TC17G008AF-8060				
IC16	: M5F78M05L				



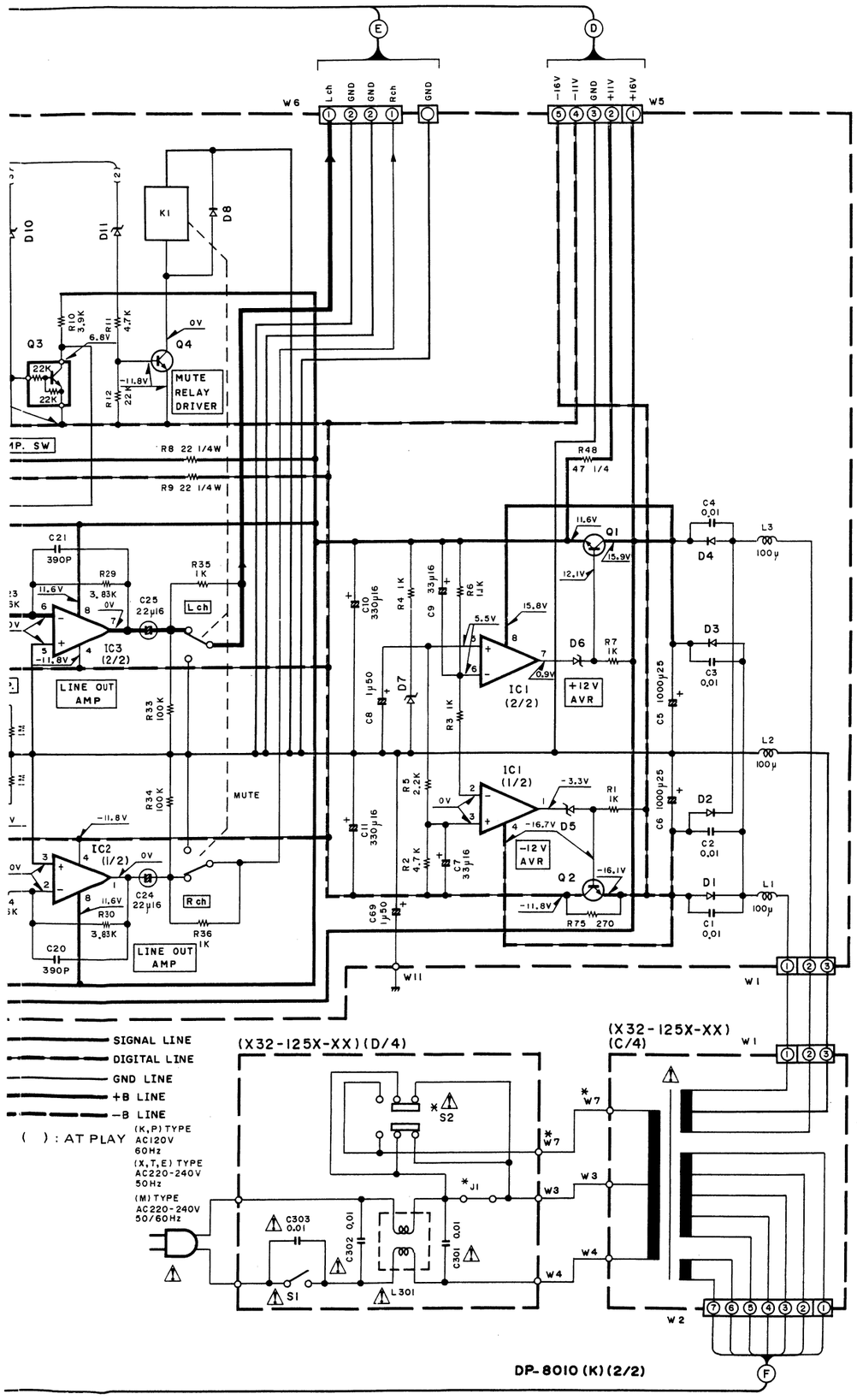
5218P or NJM4560D	Q1,2	: 2SD1266
JM5532D-D	Q3	: DTC124EN
CM58P	Q4	: 2SC945(A)(Q,P)
M5813AP		or 2SC1740S(Q,R)
C74HCU04P	Q5,6	: 2SC2878(B)
XD1125QZ or CXD1125Q	Q7 ~ 9	: 2SC3940A
XK5816SP-12L	Q10	: 2SA1534A
4AC74PC		
CI7G008AF-8060		
5F78M05L		

D1 ~ 4	: S5566B
D5,6,10,11	: RD13ES(B2) or HZS13N(B2)
D7	: RD5.6ES(B2) or HZS5.6N(B2)
D8	: 1SS133 or HSS104
D9	: 1SV147
D12 ~ 14	: RD5.1ES(B2) or HZS5.1N(B2)

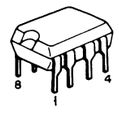
(X32-125X-XX)

DESTINATION \ Ref. No.	K,P,X,T,E	J1	S2	W7
0-11		YES	NO	NO
0-21	M	NO	YES	YES

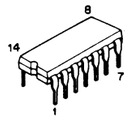
DP-8010(K)(2/2)



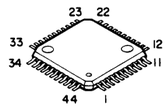
M5218P



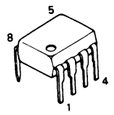
TC74HCU04P



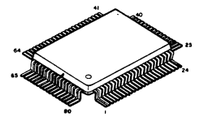
TC17G008AF-8060



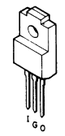
NJM4560D
NJM5532D-D



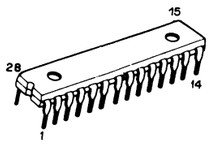
CXD1125QZ



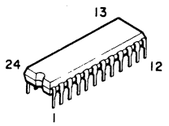
M5F78M05L



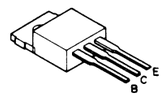
PCM58P



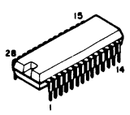
CXK5816SP-12L



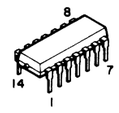
2SD1266



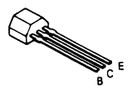
SM5813AP



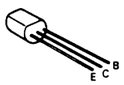
74AC74PC



2SC1740S



DTC124EN
2SA1534A
2SC945(A)
2SC2878
2SC3940A



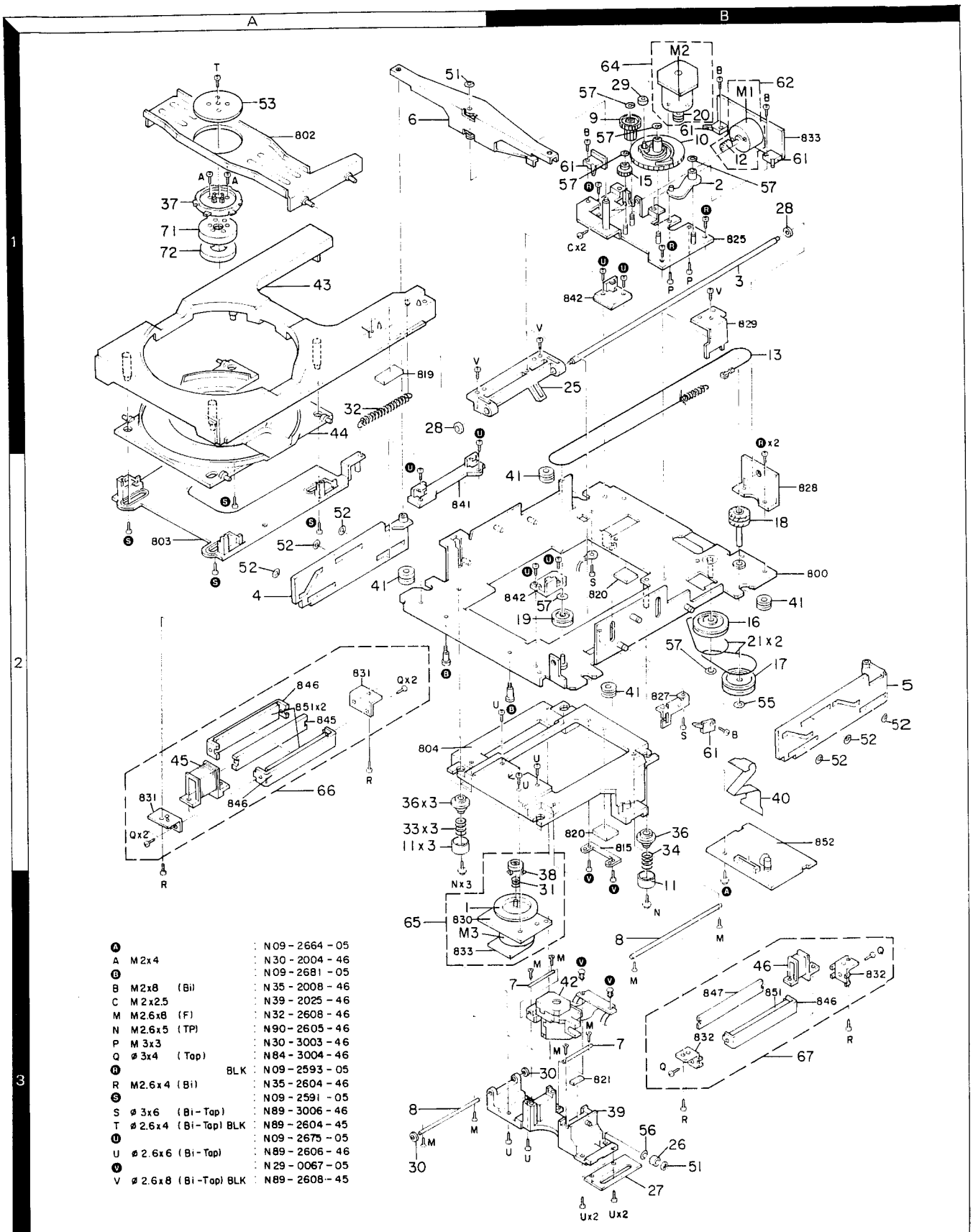
CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
- Les tensions c.c. doivent être measurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.
- Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Voltmeter gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen instrumenten oder Geräten u.U. geringfügig.

Y22-1560-11

DP-8010
KENWOOD

EXPLODED VIEW (MECHANISM)

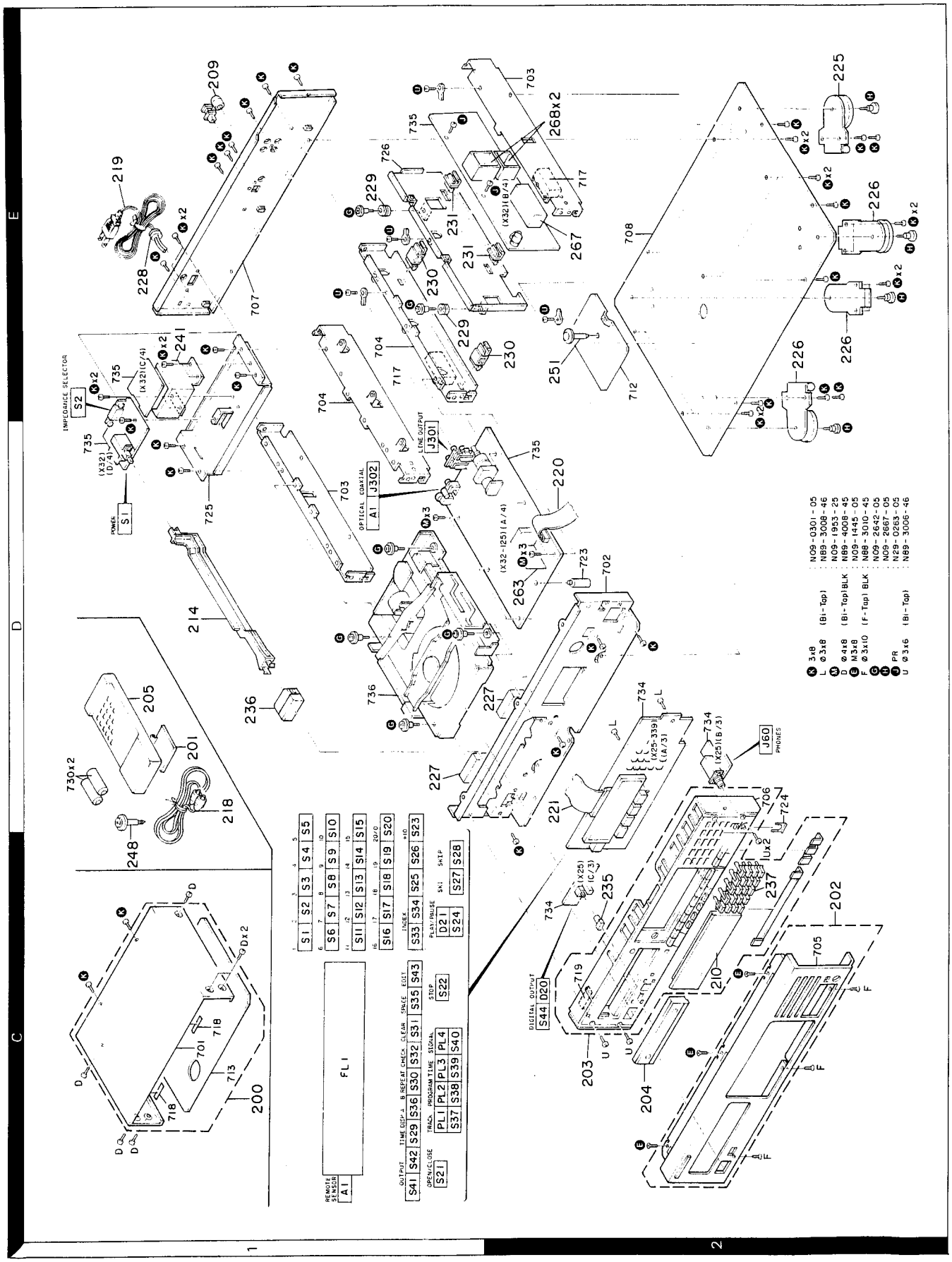


A			N09-2664-05
A	M2x4		N30-2004-46
B			N09-2681-05
B	M2x8	(Bi)	N35-2008-46
C	M2x2.5		N39-2025-46
M	M2.6x8	(F)	N32-2608-46
N	M2.6x5	(TP)	N90-2605-46
P	M3x3		N30-3003-46
Q	ø3x4	(Tap)	N84-3004-46
R		BLK	N09-2593-05
R	M2.6x4	(Bi)	N35-2604-46
S			N09-2591-05
S	ø3x6	(Bi-Tap)	N89-3006-46
T	ø2.6x4	(Bi-Tap) BLK	N89-2604-45
U			N09-2675-05
U	ø2.6x6	(Bi-Tap)	N89-2606-46
V			N29-0067-05
V	ø2.6x8	(Bi-Tap) BLK	N89-2608-45

Parts with the exploded numbers larger than 700 are not supplied.

DP-8010

EXPLODED VIEW (UNIT)



Parts with the exploded numbers larger than 700 are not supplied.

PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
			DP-8010			
200	1C	*	A01-1721-02	METALLIC CABINET ASSY		
201	1D	*	A09-0078-08	BATTERY COVER(REMOTE CONTROL)		
202	2C	*	A20-5657-02	PANEL ASSY	KPMX	
202	2C	*	A20-5730-02	PANEL ASSY	TE	
203	2C	*	A22-1042-12	SUB PANEL ASSY		
204	2C	*	A29-0140-03	PANEL (TRAY)		
205	1D	*	A70-0251-05	REMOTE CONTROLLER ASSY		
209	1E		B09-0068-05	CAP		
210	2C	*	B10-0980-14	FRONT GLASS		
-			B46-0092-03	WARRANTY CARD	KP	
-			B46-0096-13	WARRANTY CARD	X	
-			B46-0122-13	WARRANTY CARD	E	
-			B46-0143-03	WARRANTY CARD	T	
-		*	B50-9339-00	INSTRUCTION MANUAL		
-		*	B50-9340-00	INSTRUCTION MANUAL	PME	
-		*	B50-9341-00	INSTRUCTION MANUAL	M	
-		*	B50-9342-00	INSTRUCTION MANUAL	E	
-			B58-0400-04	CAUTION CARD		
-		*	B58-0895-04	CAUTION CARD		
214	1D	*	D21-1504-03	EXTENSION SHAFT		
218	1D		E30-0505-05	AUDIO CORD		
⚠ 219	1E		E30-0459-05	AC POWER CORD	E	
⚠ 219	1E		E30-0780-05	AC POWER CORD	KP	
⚠ 219	1E		E30-0812-05	AC POWER CORD	M	
⚠ 219	1E		E30-1341-05	AC POWER CORD	X	
⚠ 219	1E		E30-1416-05	AC POWER CORD	T	
220	2D	*	E31-4819-05	WIRING HARNESS		
221	2D	*	E31-4820-05	WIRING HARNESS (FLAT CABLE)		
-		*	H01-8389-04	ITEM CARTON CASE		
-		*	H10-3755-02	POLYSTYRENE FOAMED FIXTURE (L)		
-		*	H10-3756-02	POLYSTYRENE FOAMED FIXTURE (R)		
-			H20-0553-04	PROTECTION COVER	M	
-			H25-0232-04	PROTECTION BAG (235X350X0.03)		
-			H25-0319-04	PROTECTION BAG	KPXTE	
225	2E	*	J02-0398-15	INSULATOR ASSY		
226	2E	*	J02-0399-15	INSULATOR ASSY		
227	1D,2D		J11-0106-05	CLAMPER		
⚠ 228	1E		J42-0083-05	POWER CORD BUSHING		
229	1E		J42-0142-04	BUSHING		
230	1E,2E		J50-0132-05	HINGE		
231	1E	*	J50-0134-05	HINGE		
-			J61-0307-05	WIRE BAND		
235	2C		K27-1931-04	KNOB (BUTTON)(DIGITAL OUTPUT)		
236	1D		K29-3363-14	KNOB (POWER)		
237	2C		K29-3493-04	KNOB (0-20)		
⚠ 241	1E	*	L01-5601-05	POWER TRANSFORMER	KP	
⚠ 241	1E	*	L01-5602-05	POWER TRANSFORMER	XTE	
⚠ 241	1E	*	L01-5604-05	POWER TRANSFORMER	M	
248	1C	*	N09-2648-05	STEPPED SCREW		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE : AAFES(Europe) X: Australia

⚠ indicates safety critical components.

DP-8010

PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile onne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
251	2E	*	N29-0264-05	CANOE CLIP		
E	2C		N09-1445-05	SET SCREW (M3X8 FLAT)		
G	1D,1E	*	N09-2642-05	STEPPED SCREW(MECHA,HARDWERE)		
H	2D,2E	*	N09-2667-15	STEPPED SCREW(FOOT)		
J	1E,2E	*	N29-0263-05	PUSH RIVET (PR)		
K	1E,2E		N09-0301-05	TAPTITE SCREW(3X8,+BIND)		
M	1D,2D		N09-1953-25	MACHINE SCREW		
OPERATION UNIT (X25-3390-00)						
D20	2C		B30-1012-05	LED(SLP-981C-50,OUTPUT)		
D21		*	B30-1264-05	LED		
PL1 -4			B30-1207-05	LAMP		
C1			C91-0085-05	CERAMIC 0.022UF N		
C2			CK45FB1H222K	CERAMIC 2200PF K		
C3			C91-0753-05	CHIP C 470PF K		
C4 ,5			C90-1455-05	NP-ELEC 0.1UF 50WV		
CN1		*	E10-4002-05	FLAT CABLE CONNECTOR		
J60	2D	*	E11-0190-05	PHONE JACK (PHONES)		
CP1			R90-0227-05	MULTI-COMP 4.7KX6 J 1/6W		
S1 -43			S40-1064-05	PUSH SWITCH		
S44	2C		S40-2323-05	PUSH SWITCH (DIGITAL)		
D1 -19			HSS104A	DIODE		
D1 -19			1SS131	DIODE		
D22			HSS104A	DIODE		
D22			1SS131	DIODE		
FL1	1C	*	FIP10BCM7	FLUORESCENT INDICATOR TUBE		
IC1			TD62003AP	IC(DARLINGTON DRIVER)		
IC2			TC74HC174F	IC(D-FLIP FLOP)		
A1	1C	*	W02-0973-05	ELECTRIC CIRCUIT MODULE		
CONTROL CIRCUIT UNIT (X29-1960-00)						
C1 ,2			CE04KW1C330M	ELECTRO 33UF 16WV		
C3			CK45FF1H103Z	CERAMIC 0.010UF Z		
C4			CE04KW1H0R1M	ELECTRO 0.1UF 50WV		
C5			CE04KW1A101M	ELECTRO 100UF 10WV		
C6			CF92FV1H103J	MF 0.010UF J		
C7			CF92FV1H333J	MF 0.033UF J		
C8			CC45FSL1H180J	CERAMIC 18PF J		
C9			CF92FV1H472J	MF 4700PF J		
C10			CE04KW1C330M	ELECTRO 33UF 16WV		
C11 ,12			CC45FSL1H150J	CERAMIC 15PF J		
C13			CF92FV1H333J	MF 0.033UF J		
C14			CK45FF1H473Z	CERAMIC 0.047UF Z		
CN1			E10-2103-05	FLAT CABLE CONNECTOR		
-			J61-0019-05	WIRE BAND		
L1			L40-1001-17	SMALL FIXED INDUCTOR(10UH,K)		
VR1			R12-3128-05	TRIMMING POT. (TE BAL)		
VR2 -4			R12-3126-05	TRIMMING POT. (FE BAL,F/T GAIN)		
D1			HSS104	DIODE		
D1			1SS133	DIODE		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

* New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
IC1			CXA1081S	IC(RF AMP)		
IC2			TC74HC00P	IC(QUAD 2-INPUT NAND GATE)		
Q1			2SC1740S(Q,R)	TRANSISTOR		
Q1			2SC945(A)(Q,P)	TRANSISTOR		
Q2			2SA1426	TRANSISTOR		
CD PLAYER UNIT (X32-125X-XX) 0-11 : K,P,X,T,E, 0-21 : M						
C1 -4			CK45FF1H103Z	CERAMIC 0.010UF Z		
C5 ,6			CE04KW1E102M	ELECTRO 1000UF 25WV		
C7			CE04KW1C330M	ELECTRO 33UF 16WV		
C8			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C9			CE04KW1C330M	ELECTRO 33UF 16WV		
C10			CE04KW1C331M	ELECTRO 330UF 16WV		
C11			CE04KW1C331M	ELECTRO 330UF 16WV		
C12 ,13			CF92FV1H363J	MF 0.036UF J		
C14 ,15			CF92FV1H152J	MF 1500PF J		
C16 ,17			CF92FV1H752J	MF 7500PF J		
C18 ,19			CF92FV1H103J	MF 0.010UF J		
C20 -23		*	CF92FV1H391K	MF 390PF K		
C24 ,25			C90-1748-05	ALMINIUM ELECTROLYTIC C.		
C26 ,27			CE04KW1C330M	ELECTRO 33UF 16WV		
C28			CE04KW1C221M	ELECTRO 220UF 16WV		
C29			CE04KW1C221M	ELECTRO 220UF 16WV		
C30 ,31			CE04KW1C330M	ELECTRO 33UF 16WV		
C32 ,33			CE04KW0J331M	ELECTRO 330UF 6.3WV		
C34 ,35			CE04KW1A101M	ELECTRO 100UF 10WV		
C36 ,37			CE04KW1C330M	ELECTRO 33UF 16WV		
C38 ,39			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C40 -42			CE04KW1C330M	ELECTRO 33UF 16WV		
C43 ,44			CE04KW0J471M	ELECTRO 470UF 6.3WV		
C45			CE04KW1C330M	ELECTRO 33UF 16WV		
C46 ,47			C91-0980-05	CERAMIC 15PF G		
C48			CE04KW1C330M	ELECTRO 33UF 16WV		
C49		*	CC45FUJ1H101J	CERAMIC 100PF J		
C50			CK45FB1H222K	CERAMIC 2200PF K		
C51			CC45FUJ1H050C	CERAMIC 5.0PF C		
C52			CK45FB1H222K	CERAMIC 2200PF K		
C53			CF92FV1H124J	MF 0.12UF J		
C54			CC45FSL1H101J	CERAMIC 100PF J		
C55			CK45FB1H332K	CERAMIC 3300PF K		
C56 ,57			CK45FF1H103Z	CERAMIC 0.010UF Z		
C58			CE04KW1C330M	ELECTRO 33UF 16WV		
C59			CE04KW1V330M	ELECTRO 33UF 35WV		
C60			CE04KW1E330M	ELECTRO 33UF 25WV		
C61			CC45FUJ1H330J	CERAMIC 33PF J		
C62 ,63			CE04KW0J331M	ELECTRO 330UF 6.3WV		
C64			CK45FF1H473Z	CERAMIC 0.047UF Z		
C65			CE04KW1C330M	ELECTRO 33UF 16WV		
C66 ,67			CK45FF1H103Z	CERAMIC 0.010UF Z		
C68			C91-0745-05	CERAMIC 100PF K		
C69			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C70			CK45FF1H103Z	CERAMIC 0.010UF Z		
C71			CC45FSL1H101J	CERAMIC 100PF J		
C101-105			CK45FF1H103Z	CERAMIC 0.010UF Z		
C106,107		*	CE04KW1A332M	ELECTRO 3300UF 10WV		
C108-112			CE04KW1C330M	ELECTRO 33UF 16WV		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE : AAFES(Europe) X: Australia

⚠ indicates safety critical components.

DP-8010

PARTS LIST

＊ New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

	Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
	C113			CE04KW1C221M	ELECTRO 220UF 16WV		
	C114,115			CK45FF1H103Z	CERAMIC 0.010UF Z		
	C116			CE04KW1H470M	ELECTRO 47UF 50WV		
	C117,118			CK45FF1H103Z	CERAMIC 0.010UF Z		
	C119,120			CE04KW1C330M	ELECTRO 33UF 16WV		
	C121,122			CK45FF1H103Z	CERAMIC 0.010UF Z		
	C123			C90-1349-05	NP-ELEC 1UF 50WV		
	C124,125			CE04KW1C330M	ELECTRO 33UF 16WV		
	C126			C90-1350-05	NP-ELEC 2.2UF 50WV		
	C127			CF92FV1H223J	MF 0.022UF J		
	C128-130			CE04KW1C330M	ELECTRO 33UF 16WV		
	C131,132			CK45FF1H103Z	CERAMIC 0.010UF Z		
	C133,134			CC45FSL1H101J	CERAMIC 100PF J		
	C135			C90-1331-05	NP-ELEC 0.47UF 50WV		
	C136			CF92FV1H104J	MF 0.10UF J		
	C137,138			CF92FV1H822J	MF 8200PF J		
	C139			C90-1331-05	NP-ELEC 0.47UF 50WV		
	C140			CC45FSL1H470J	CERAMIC 47PF J		
	C141			CE04KW1A101M	ELECTRO 100UF 10WV		
	C142			C90-1349-05	NP-ELEC 1UF 50WV		
	C143,144			CE04KW1C330M	ELECTRO 33UF 16WV		
	C145			CF92FV1H124J	MF 0.12UF J		
	C146,147			C90-1351-05	NP-ELEC 3.3UF 50WV		
	C148			CF92FV1H104J	MF 0.10UF J		
	C149			CK45FB1H821K	CERAMIC 820PF K		
	C150			CK45FB1H222K	CERAMIC 2200PF K		
	C151			CK45FB1H681K	CERAMIC 680PF K		
	C152			CK45FF1H103Z	CERAMIC 0.010UF Z		
	C153			CF92FV1H103J	MF 0.010UF J		
	C154			C90-1349-05	NP-ELEC 1UF 50WV		
	C155,156			CK45FF1H103Z	CERAMIC 0.010UF Z		
	C157			CE04KW1V100M	ELECTRO 10UF 35WV		
	C158,159			CE04KW0J331M	ELECTRO 330UF 6.3WV		
	C160			C90-1350-05	NP-ELEC 2.2UF 50WV		
	C161,162			CK45FF1H103Z	CERAMIC 0.010UF Z		
	C201-204			CF92FV1H102J	MF 1000PF J		
	C205,206			C90-1455-05	NP-ELEC 0.1UF 50WV		
	C207,208			C90-1349-05	NP-ELEC 1UF 50WV		
	C209,210			CE04KW1C330M	ELECTRO 33UF 16WV		
	C211			CE04KW1C221M	ELECTRO 220UF 16WV		
	C212			CE04KW1C330M	ELECTRO 33UF 16WV		
	C213			CE04KW1H010M	ELECTRO 1.0UF 50WV		
⚠	C301-303			C91-0647-05	CERAMIC 0.01UF P		
	CN1		＊	E10-4001-05	FLAT CABLE CONNECTOR		
	CN2 ,3			E10-1705-05	FLAT CABLE CONNECTOR		
	J301	1D		E13-0483-05	PHONO JACK (LINE OUT)		
	J302	1D	＊	E13-0137-05	PHONO JACK (COAXIAL)		
⚠				F29-0072-05	INSULATING COVER	KPXTE	
	263	2D	＊	F10-0695-04	SHIELDING PLATE		
	267	2E	＊	F11-0420-04	SHIELDING CASE		
	268	2E	＊	F11-0421-04	SHIELDING CASE		
	L1 -3			L33-0328-05	CHOKE COIL		
	L4			L32-0328-15	OSCILATING COIL(VCO)		
	L101-107		＊	L33-0358-05	CHOKE COIL		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

* New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Telle ohne Parts No. werden nicht gellefert.

	Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
	L108,109			L33-0328-05	CHOKE COIL		
	L110			L39-0152-05	MATCHING COIL		
	L111		*	L40-1091-17	SMALL FIXED INDUCTOR		
	L112			L39-0187-05	PHASE-COMPENSATION COIL	KPXTE	
	L201,202		*	L40-2291-17	SMALL FIXED INDUCTOR		
	L203,204			L40-1001-17	SMALL FIXED INDUCTOR(10UH,K)		
⚠	L301			L79-0733-05	LINE FILTER		
	X1		*	L77-1159-05	CRYSTAL RESONATOR		
	CP1			R90-0227-05	MULTI-COMP 4.7KX6 J 1/6W		
	CP2			R90-0426-05	MULTI-COMP 100KX6 J 1/6W		
	CP3			R90-0227-05	MULTI-COMP 4.7KX6 J 1/6W		
	CP4			R90-0426-05	MULTI-COMP 100KX6 J 1/6W		
	R8 ,9			RD14GB2E220J	FL-PROOF RD 22 J 1/4W		
	R13 ,14		*	RN14BK2C4220F	RN 422.0 F 1/6W		
	R15 ,16			RN14BK2C1961F	RN 1.96K F 1/6W		
	R17 ,18			RN14BK2C1001F	RN 1.00K F 1/6W		
	R19 ,20		*	RN14BK2C1331F	RN 1.33K F 1/6W		
	R21 ,22			RN14BK2C1001F	RN 1.00K F 1/6W		
	R23 ,24			RN14BK2C1961F	RN 1.96K F 1/6W		
	R29 ,30			RN14BK2C3831F	RN 3.83K F 1/6W		
	R31 ,32		*	R92-0393-05	RD 3.3K J 1/2W		
	R33 ,34			RN14BK2C1003F	RN 100K F 1/6W		
	R35 ,36			RN14BK2C1001F	RN 1.00K F 1/6W		
	R37 -40		*	RN14BK2C3013F	RN 301K F 1/6W		
	R48			RD14GB2E470J	FL-PROOF RD 47 J 1/4W		
	R70			RN14BK2C1004F	RN 1.00M F 1/6W		
	R201,202			RN14BK2C1000F	RN 100.0 F 1/6W		
	VR1 -4			R12-5058-05	TRIMMING POT.(DAC DISTORTION)		
	VR201			R29-1001-05	POTENTIOMETER		
	K1			S51-2074-05	MAGNETIC RELAY		
⚠	S1	1D		S40-1103-05	PUSH SWITCH (POWER TYPE)		
⚠	S2	1E		S31-2131-05	SLIDE SWITCH (POWER TYPE)	M	
	D1 -4			S5566B	DIODE		
	D5 ,6			HZS13N(B2)	ZENER DIODE		
	D5 ,6			RD13ES(B2)	ZENER DIODE		
	D7			HZS5.6N(B2)	ZENER DIODE		
	D7			RD5.6ES(B2)	ZENER DIODE		
	D8			HSS104	DIODE		
	D8			1SS133	DIODE		
	D9			1SV147	VARISTOR		
	D10 ,11			HZS13N(B2)	ZENER DIODE		
	D10 ,11			RD13ES(B2)	ZENER DIODE		
	D12 -14			HZS5.1N(B2)	ZENER DIODE		
	D12 -14			RD5.1ES(B2)	ZENER DIODE		
	D101-104			S5566B	DIODE		
	D105			HSS104	DIODE		
	D105			1SS133	DIODE		
	D106			HZS8.2N(B)	ZENER DIODE		
	D106			RD8.2ES(B)	ZENER DIODE		
	D107			HSS104A	DIODE		
	D107			1SS131	DIODE		
	D108			HZS30N(B)	ZENER DIODE		
	D108			RD30ES(B)	ZENER DIODE		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

DP-8010

PARTS LIST

* New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
D109			HZS8.2N(B)	ZENER DIODE		
D109			RD8.2ES(B)	ZENER DIODE		
D110-112			HZS4.7N(B)	ZENER DIODE		
D110-112			RD4.7ES(B)	ZENER DIODE		
D113-117			HSS104	DIODE		
D113-117			1SS133	DIODE		
D118			HSS104A	DIODE		
D118			1SS131	DIODE		
D119-124			HSS104	DIODE		
D119-124			1SS133	DIODE		
D125			HZS3.9N(B)	ZENER DIODE		
D125			RD3.9ES(B)	ZENER DIODE		
D201-208			HSS104	DIODE		
D201-208			1SS133	DIODE		
IC1			M5218P	IC(OP AMP X2)		
IC1			NJM4560D	IC(OP AMP X2)		
IC2 -5			NJM5532D-D	IC(OP AMP X2)		
IC6 ,7		*	PCM58P	IC(DA CONVERTER)		
IC8			M5218P	IC(OP AMP X2)		
IC8			NJM4560D	IC(OP AMP X2)		
IC9		*	SM5813AP	IC(8FS DIGITAL FILTER)		
IC10			TC74HCU04P	IC(HEX INVERTER)		
IC11			CXD1125Q	IC(DIGITAL SIGNAL PROCESSOR)		
IC11			CXD1125QZ	IC(DIGITAL SIGNAL PROCESSOR)		
IC12			CXK5816SP-12L	IC(2KX8 RAM)		
IC13		*	74AC74PC	IC(D-FLIP FLOP)		
IC14			M5218P	IC(OP AMP X2)		
IC14			NJM4560D	IC(OP AMP X2)		
IC15			TC17G008AF-8060	IC(DPAC)		
IC16			M5F78M05L	IC(VOLTAGE REGULATOR/ +5V)		
IC101			NJM4558D	IC(OP AMP X2)		
IC102			UPD4053BC	IC(3-INPUT 2CH MPX/DE-MPX)		
IC103			CXA1244S	IC(SERVO SIGNAL PROCESSOR)		
IC104		*	UPD75212ACW-051	IC(MICROPROCESSOR)		
IC105			NJM4558D	IC(OP AMP X2)		
IC106-108			LB1294	IC(6CH DARLINGTON DRIVER)		
IC109			LB1433N	IC(LEVEL METER DRIVER)		
IC110,111			NJM4558D	IC(OP AMP X2)		
IC112			M51951ASL	IC(SYSTEM RESET)		
IC113			LA6500	IC(OP AMP)		
IC114			UPC4570C-A	IC(OP AMP X2)		
Q1 ,2			2SD1266	TRANSISTOR		
Q3			DTC124EN	DIGITAL TRANSISTOR		
Q4			2SC1740S(Q,R)	TRANSISTOR		
Q4			2SC945(A)(Q,P)	TRANSISTOR		
Q5 ,6			2SC2878(B)	TRANSISTOR		
Q7 -9			2SC3940A	TRANSISTOR		
Q10			2SA1534A	TRANSISTOR		
Q101			2SA1534A	TRANSISTOR		
Q102,103			2SC3940A	TRANSISTOR		
Q104,105			2SA1534A	TRANSISTOR		
Q106			2SC3940A	TRANSISTOR		
Q107			2SA1534A	TRANSISTOR		
Q108			2SC3940A	TRANSISTOR		
Q109			2SA1534A	TRANSISTOR		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

PARTS LIST

* New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Telle ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
Q110			2SC3940A	TRANSISTOR		
Q111			2SA1534A	TRANSISTOR		
Q112			2SC3940A	TRANSISTOR		
Q113			2SA1534A	TRANSISTOR		
Q114			2SC3940A	TRANSISTOR		
Q115			2SA1534A	TRANSISTOR		
Q116			2SC3940A	TRANSISTOR		
Q117			2SC1740S(Q,R)	TRANSISTOR		
Q117			2SC945(A)(Q,P)	TRANSISTOR		
Q201,202			2SC3940A	TRANSISTOR		
Q203,204			2SA1534A	TRANSISTOR		
A1	1D		W02-0936-05	TRANSMITTING ASSY (OPTICAL)		
MECHANISM ASS'Y (X92-1320-00)						
11	2A,3B	*	B09-0088-04	CAP		
C1			CK45FF1H103Z	CERAMIC 0.010UF Z		
C2			C91-0769-05	CERAMIC 0.01UF M		
C3			CK45FF1H103Z	CERAMIC 0.010UF Z		
1	3A	*	D02-0085-04	TURNTABLE PLATTER		
2	1B	*	D10-2231-04	ARM ASSY		
3	1B	*	D10-2233-04	ROD		
4	2A	*	D10-2234-03	SLIDER (L,CLAMP)		
5	2B	*	D10-2235-03	SLIDER (R,CLAMP)		
6	1A	*	D10-2237-03	ARM (CLAMP)		
7	3B	*	D10-2238-04	ROD		
8	3A,3B	*	D10-2270-04	ROD		
9	1B	*	D13-0725-04	GEAR (HELICAL)		
10	1B	*	D13-0726-03	GEAR (MAIN)		
12	1B	*	D13-0743-04	WORM		
13	1B	*	D19-0253-14	WIRE (WITH SPRING)		
15	1B	*	D13-0744-04	GEAR		
16	2B	*	D15-0285-04	PULLEY (A)		
17	2B	*	D15-0286-04	PULLEY (B1)		
18	2B	*	D15-0287-04	PULLEY (B2)		
19	2B	*	D15-0288-04	PULLEY (C)		
20	1B	*	D15-0289-04	MOTOR PULLEY (T42-0498-04ASSY)		
21	2B	*	D16-0192-04	BELT		
25	1B	*	D23-0237-04	RETAINER		
26	3B	*	D23-0238-05	RETAINER		
27	3B	*	D32-0177-04	STOPPER		
28	1A,1B	*	G11-1302-04	CUSHION (ROD)		
29	1B	*	G11-1321-14	CUSHION		
30	3A,3B	*	G11-1322-14	CUSHION		
31	3B		G01-2105-04	COMPRESSION SPRING		
32	1A	*	G01-2281-04	EXTENSION SPRING		
33	2A	*	G01-2282-04	COMPRESSION SPRING(A)		
34	2B	*	G01-2283-04	COMPRESSION SPRING(B,BLACK)		
36	2A,2B		J02-0192-05	INSULATOR		
37	1A	*	J11-0137-03	CLAMPER		
38	3B		J19-2874-04	HOLDER (TURNTABLE)		
39	3B	*	J19-3058-05	HOLDER		
40	2B	*	J25-6074-05	PRINTED WIRING BOARD ASSY		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE : AAFES(Europe) X: Australia

⚠ indicates safety critical component

DP-8010

PARTS LIST

* New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
41	2A,2B	*	J42-0165-04	BUSHING		
42	3B	*	J91-0377-05	PICKUP		
43	1A	*	J99-0056-01	TRAY (A)		
44	1A	*	J99-0058-02	TRAY (B)		
-			J61-0019-05	WIRE BAND (D40-0866-02ASSY)		
45	2A	*	L90-0015-08	COIL		
46	3B		L90-0016-08	COIL		
51	1A,3B		N19-0891-04	FLAT WASHER		
52	2A,2B	*	N19-0921-04	FLAT WASHER		
53	1A		N19-0945-04	FLAT WASHER		
55	2B	*	N19-1212-04	FLAT WASHER		
56	3B		N19-0143-04	FLAT WASHER		
57	1B,2B	*	N19-1211-04	FLAT WASHER		
A	3B	*	N09-2664-05	STEPPED SCREW		
B	2A,2B	*	N09-2681-05	STEPPED SCREW		
R	1B,2B	*	N09-2593-05	TAPTITE SCREW		
S	2A	*	N09-2591-05	TAPTITE SCREW		
U	1B,2B	*	N09-2675-05	TAPTITE SCREW		
V	3B		N29-0067-05	PUSH RIVET (3.5X4.5)		
R1			RS14KB3A470J	FL-PROOF RS 47 J 1W		
61	1B,2B		S33-1017-05	LEVER SWITCH		
62	1B	*	T42-0485-04	MOTOR ASSY (CLAMP)		
64	1B	*	T42-0498-04	MOTOR ASSY (LOADING)		
65	3A	*	T42-0499-14	MOTOR ASSY (DISC)		
66	2A	*	T50-1037-15	YOKE ASSY		
67	3B	*	T50-1038-15	YOKE ASSY		
71	1A	*	T50-1041-04	YOKE		
72	1A		T99-0222-05	MAGNET		
M1	1B		T42-0439-05	DC MOTOR (CLAMP MOTOR)		
M2	1B		T42-0486-05	DC MOTOR (LOADING MOTOR)		
M3	3A		T42-0496-05	DC MOTOR (DISC MOTOR)		
D1 -D3			S5566B	DIODE		

E: Scandinavia & Europe K: USA P: Canada
U: PX(Far East, Hawaii) T: England M: Other Areas
UE: AAFES(Europe) X: Australia

⚠ indicates safety critical components.

DP-8010

SPECIFICATIONS

[Format]

Type: ..... Compact disc player
Read system: ..... Non-contact optical pickup
Rotational speed: ..... About 200 to 500 rpm

[Audio]

Frequency responce: ..... 4 Hz ~ 20 kHz
Signal-to-noise ratio: ..... more than 112 dB
Total harmonic distortion: ..... 0.0015% at 1 kHz
Channel separation: ..... more than 110 dB at 1 kHz
Wow flutter: ..... Below measurable limit
Output
LINE (FIXED): ..... 2.0 V
(VARIABLE): ..... 0 ~ 2.0 V
Digital (COAXIAL): ..... 0.5 V p-p, 75 ohms
(OPTICAL): ..... – 15 dBm ~ – 21 dBm
Headphone jack: ..... 60 mW (8 ohms)

[General]

Power consumption: ..... 25 W
Maximum dimensions: ..... W: 440 mm (17-5/16")
H: 121 mm (4-3/4")
D: 361 mm (14-3/16")
Weight: ..... 9.6 kg (21.2 lb)

[Wireless remote control unit]

Model: RC-P8010
Type: ..... Infrared pulse
Power supply: ..... DC 3 V (two R6/AA batteries)
Maximum dimensions: ..... W: 64 mm (2-1/2")
H: 18 mm (11/16")
D: 176 mm (6-15/16")
Weight: ..... 121 g (with batteries) (0.27 lb)

Note:
KENWOOD follows a policy of continuous development. For this reason specifications may be changed without notice.

Note :
Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the U.S.A. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

KENWOOD CORPORATION
Shionogi Shibuya Building, 17-5, 2-chome Shibuya, Shibuya-ku, Tokyo 150, Japan

KENWOOD U.S.A. CORPORATION
2201 East Dominguez Street, Long Beach, CA 90810 :
550 Clark Drive, Mount Olive, NJ 07828, U.S.A.

KENWOOD ELECTRONICS CANADA INC.
P.O. Box 1075 959 Gana Court, Mississauga, Ontario, Canada L4T 4C2

KENWOOD ELECTRONICS BENELUX N.V.
Mechelsesteenweg 418 B-1930 Zaventem, Belgium

KENWOOD ELECTRONICS DEUTSCHLAND GMBH
Rembrucker-Str. 15, 6056 Heusenstamm, West Germany

TRIO-KENWOOD FRANCE S.A.
Hi-Fi・VIDEO・CAR Hi-Fi
13, Boulevard Ney, 75018 Paris, France

TRIO-KENWOOD U.K. LTD.
17 Bristol Road, The Metropolitan Centre, Greenford, Middx. UB6 8UP England

KENWOOD ELECTRONICS AUSTRALIA PTY. LTD.
4E Woodcock Place, Lane Cove, N.S.W. 2066, Australia

KENWOOD & LEE ELECTRONICS, LTD.
Wang Kee Building, 4th Floor, 34-37, Connaught Road, Central, Hong Kong