DP-969

SPECIFICATIONS

Audio

Frequency response	4 Hz ~ 20 kHz
Signal -to-Noise ratio	more than 95 dB
Dynamic range	more than 93 dB
Total harmonic distortion	0.0035 % or less (1 kHz, THD)
Channel separation	more than 90 dB
Wow & flutter	Below measurable limit (±0.001 %, W PEAK)
Line output level	2.0 V

Format

Type	Compact disc player
Read system	Non-contact optical pick-up system
Laser pick-up	GaAlAs, λ = 780 nm, 3-beam type
Spindle speed	About 200 rpm — 500 rpm
Error correction	Cross Interleave Read Solomon Code
Number of channels	2 channels

General

Power consumptions	16 W
Dimentions	W: 340 mm (13-3/8″) H: 84 mm (3-5/16″) D: 349 mm (13-3/4″)
Weight (Net)	4.0 kg (8.8 lb)

Remote control unit

Model	RC-P969
System	Infrared beam pulse
Power requirements	DC 3 V: R6 (AA) x 2
Dimentions	H: 157 mm (6-3/16″) W: 68 mm (2-11/16″) D: 18 mm (11/16″)
Weight	115 g (0.253 lb) (With batteries)

Note:
We follow a policy of advancements in development. For this reason specifications may be changed without notice.

Note :
Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the Europe (E) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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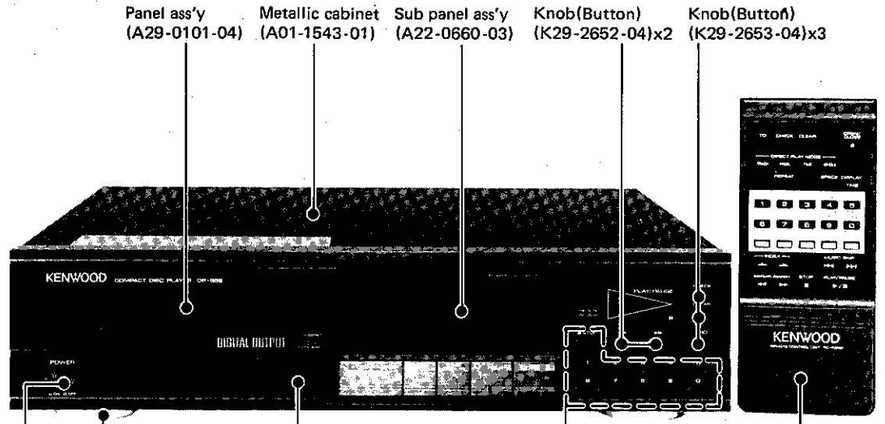
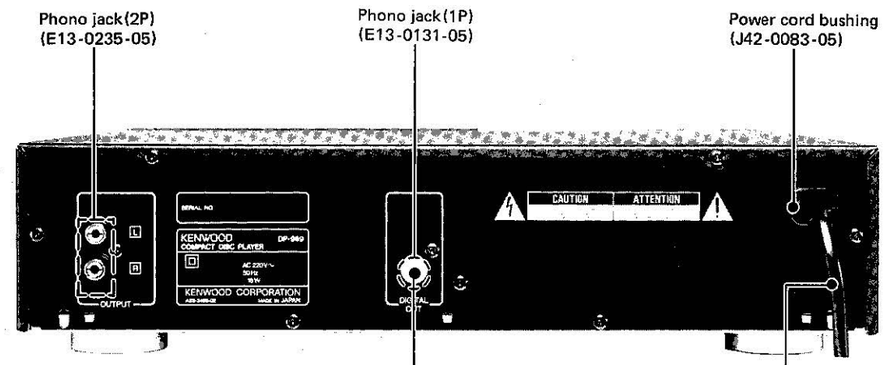
COMPACT DISC PLAYER

DP-969

SERVICE MANUAL

KENWOOD





In complicance with Federal Regulations, following are reproductions of labels on, or inside the product relating to laser product safety.

KENWOOD-Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040. 10, Chapter 1, Subchapter J.

DANGER : Laser radiation when open and interlock defeated.
AVOID DIRECT EXPOSURE TO BEAM.

*** Refer to parts list on page 73.**

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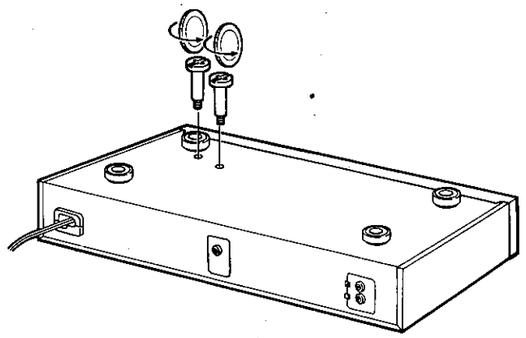
CAUTION/DISASSEMBLY FOR REPAIR

CAUTION

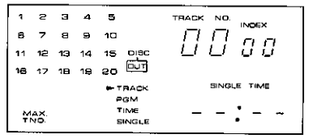
TRANSPORTATION SCREW

Before operation, remove the two red screws attached to the bottom of the unit used during transport from the factory. Remove both screws using a coin, etc. and, after removing, retain them together with the Warranty card and other documents. When the unit is to be transported again, be sure replace the two screws to their original position.



ATTACHING THE TRANSPORTATION SCREWS

1. Turn the power ON without loading disc.
2. Turn OFF the power after the display shows the following indication.

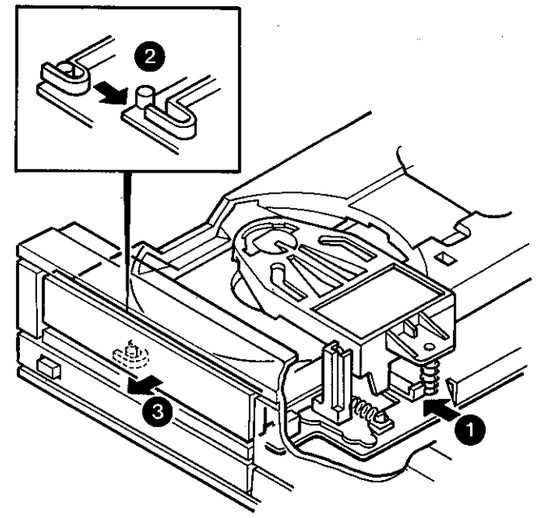


3. Install the transportation screws.

DISASSEMBLY FOR REPAIR

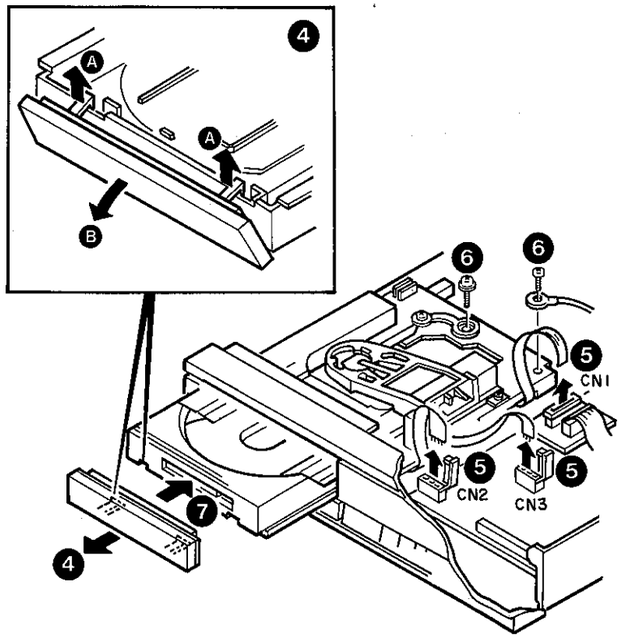
DISASSEMBLING THE MECHANISM

1. Push the projection of the slider ass'y under the disc clamper as arrow ❶.
2. The roller of the slider ass'y is dislocated at the stopper position (❷).
3. Lightly draw the tray out as arrowed with your hand (❸).



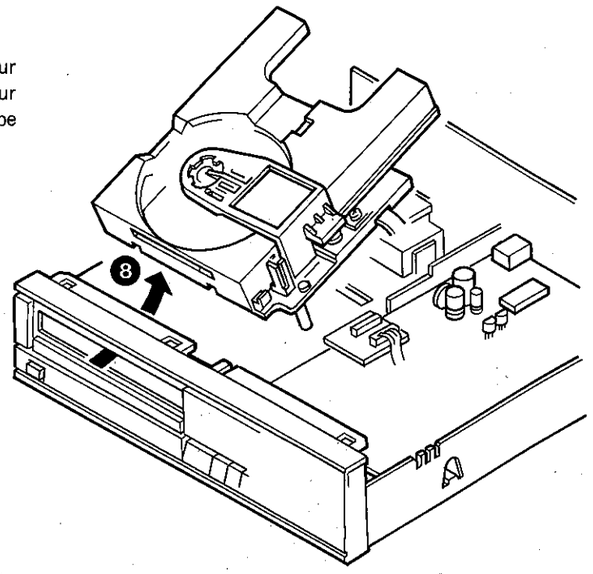
DISASSEMBLY FOR REPAIR

4. Lightly pull up the two tray panel hooks as arrowed Ⓐ to dislocate them and then slowly remove the tray as arrowed Ⓑ (❹).
5. Disconnect the three flat cables from the mechanism ❺, remove the mechanism and ground line terminal set screws ❻.
6. Push the tray in as arrowed again ❼.



7. Slowly raise the mechanism as arrowed ❽ and then pull it out.

Note : This mechanism is floated from the chassis with four rubber bushes. When replacing the mechanism, the four outsert legs on the bottom side of the mechanism must be firmly inserted into the rubber bush holes.

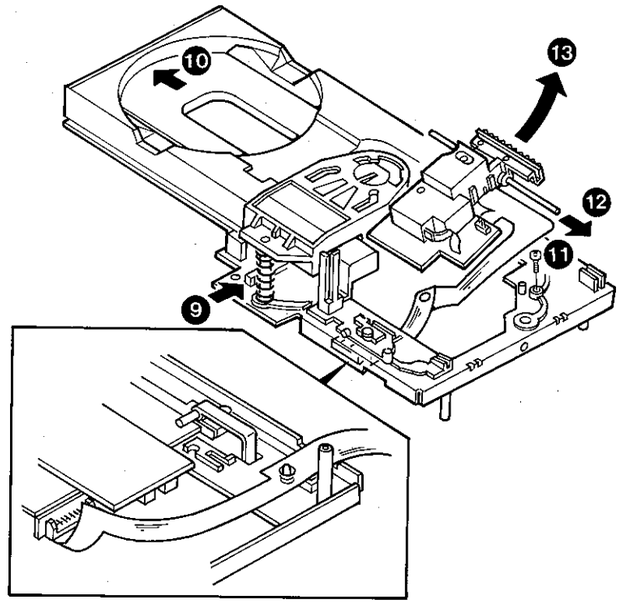


DISASSEMBLY FOR REPAIR

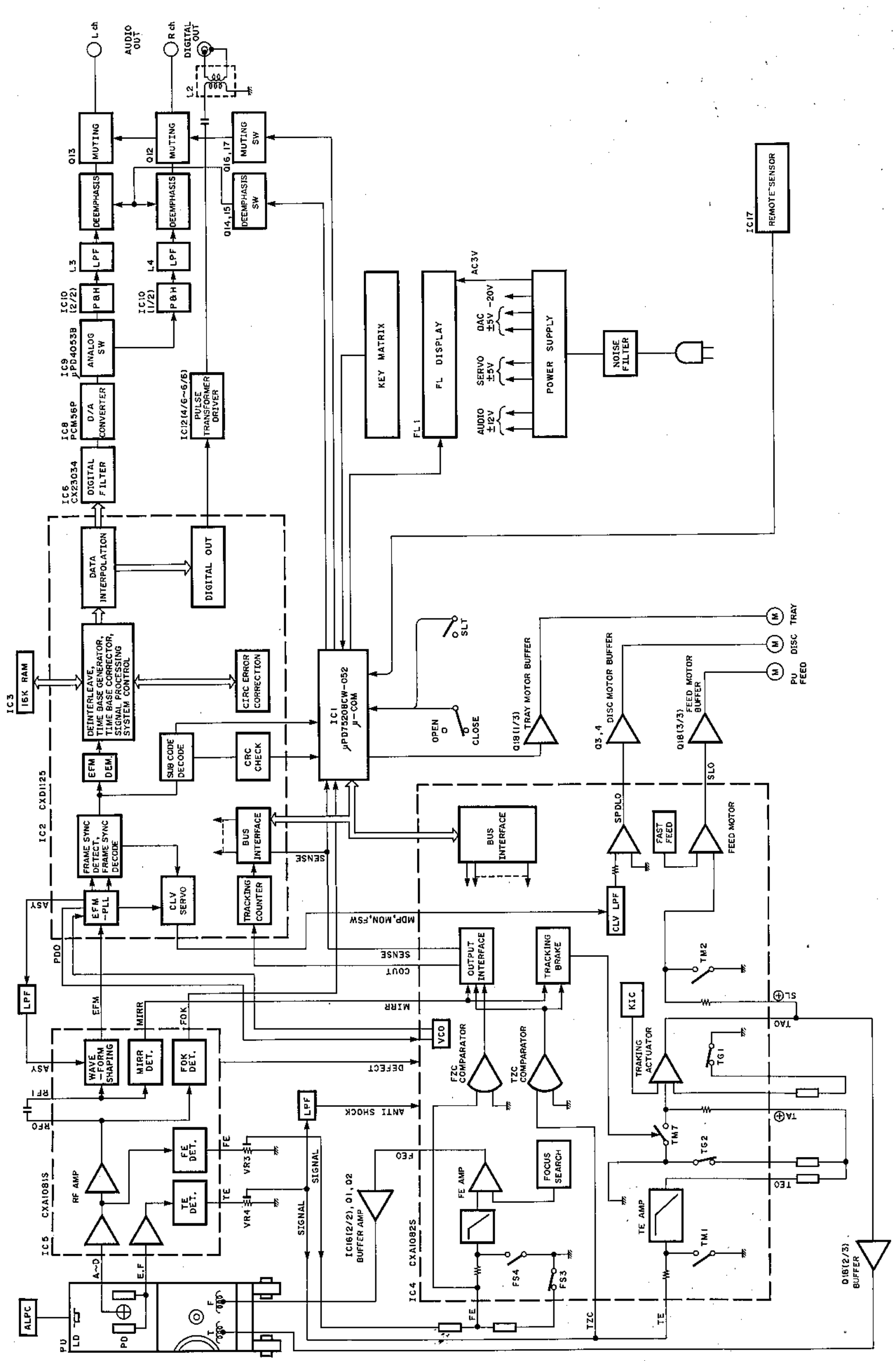
REMOVING THE PICKUP

1. Push in the projection of the slider ass'y located at the bottom of the disc clamper as arrowed ❾ here again.
2. While holding the projection pushed in, slowly pull the tray out as arrowed ❿.
3. Remove the laser pickup rail set screw ⓫.
4. Move the rail as arrowed ⓬ and then slowly pull the laser pickup out as arrowed ⓭.

Note : Be careful not to forcibly stretch the flexible PCB from the pickup which is also fixed to the mechanism chassis. When replacing the pickup, do not fail to firmly fix the flexible PCB to the clamping hook on the bottom side of the mechanism.



BLOCK DIAGRAM



CIRCUIT DESCRIPTION

Description of components

1–1. ELECTRIC UNIT (X25-2932-71)

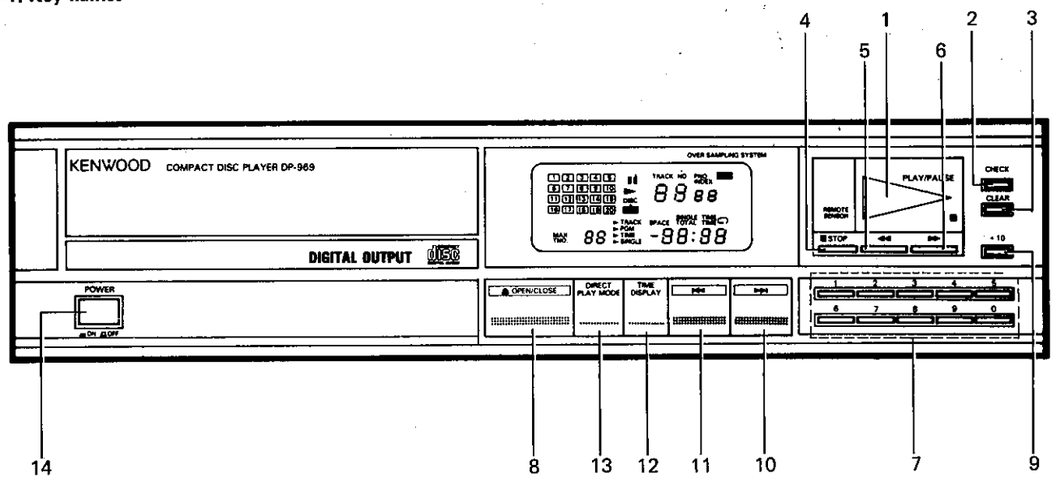
Component	Use/Function	Operation/Condition/Compatibility
IC1	Main microprocessor	Controls display and system operation.
IC2	Signal processing IC	See the description of each component for details.
IC3	Memory S-RAM	Error correction, de-interleave, jitter absoption.
IC4	Servo signal processor	Generates "search" pulses for addressing the focus servo, tracking servo, or drive motor servo. (See the description of CXA1082S for details.)
IC5	RF amplifier	Generates a focus error signal, a tracking error signal, and a RF signal. This also provides a phase and an automatic symmetry correction capabilities. (See the description of CXA1081S for details.)
IC6	Digital filter	A 96th degree digital filter which doubles the sampling frequency of 44.1kHz to 88.2kHz and sends out produced data.
IC7	Quad 2-input NAND gate	Provides buffers of DATA, BCK and LRCK of CX23034 and digital out of IC2 (CXD1125).
IC8	D/A converter	Digital to Analog convertion IC.
IC9	Analog switch	Used as the switch for the sample holding circuit.
IC10	Operation amplifier	Sample holding amplifier.
IC11	Quad 2-input NAND gate	Generates "sample" pulses for holding of L-R CH.
IC12	Hex-inverter	Pulse transformer driver for digital out. Used as the filter for MUTE and EMPH. of DIN connector output.
IC13	Operation amplifier	±5V regulator for digital line.
IC14	Operation amplifier	±5V regulator for analog line (DAC).
IC15	Operation amplifier	±12V regulator for analog line.
IC16	Operation amplifier	(1/2) : Tray driver circuit, (2/2) : Focus actuator driver.
IC17	Remocon sensor	
Q1,Q2	Current buffer	Current buffer for focus actuator driver circuit.
Q3,Q4	Current amplifier	Current buffer for disc motor driver circuit.
Q5	FL driver	Generates –30V with D13 for driving FL display.
Q6	–5V for digital line	Provides ±5V for digital line using IC13.
Q7	+5V for digital line	Using ±5V of analog line reference voltage.
Q8	–5V for digital line	Provides ±5V for analog line using IC14.
Q9	+5V for digital line	Determines reference voltage of zener diode D50.
Q10	–12V for analog line	Provides ±12V for analog line using IC15.
Q11	+12V for analog line	Determines reference voltage of zener diode D38.
Q12,Q13	Muting switch	Provides muting circuit for audio output.
Q14,Q15	De-emphasis switch	Provides interface circuit for between muting, de-emphasis circuit and
Q16,Q17	Muting ON-OFF switch	signal from microprocessor.
Q18	Current buffer	(1/3) : Current buffer for tray motor drive circuit. (2/3) : Current buffer for tracking actuator drive circuit. (3/3) : Current buffer for feed motor drive circuit.

Table 1–1

CIRCUIT DESCRIPTION

2. Key namas and displays

2–1. Key names



1 : PLAY/PAUSE key
2 : CHECK key
3 : CLEAR key
4 : STOP key
5 : Manual search key (FF key : ▶▶)
6 : Manual search key (FB key : ◀◀)
7 : Numeric keys (0 to 9)
8 : OPEN/CLOSE key
9 : Numeric key (+10 key)
10 : Music skip key (UP key : ▶▶|)
11 : Music skip key (DOWN key : |◀◀)
12 : TIME DISPLAY key
13 : DIRECT PLAY MODE key
14 : POWER switch key

Fig. 2–1 Front panel

2–2. Display panel

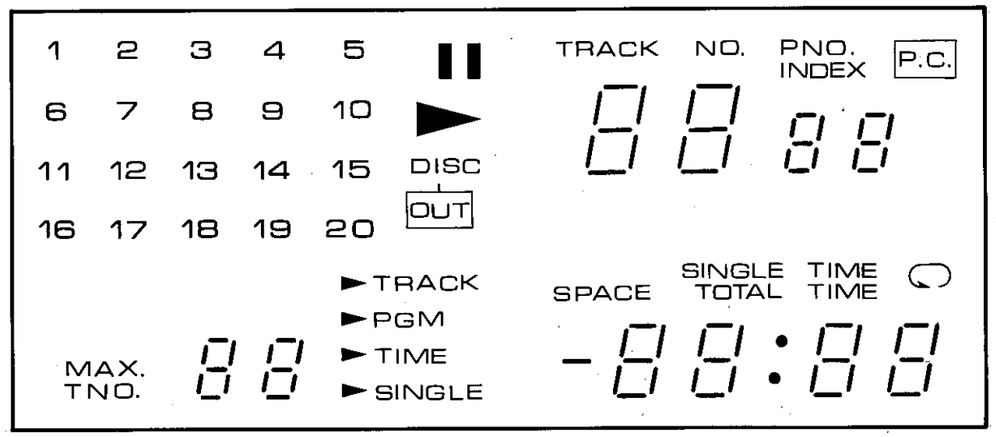


Fig. 2–2 Display panel

DP-969

CIRCUIT DESCRIPTION

2–3. Display Description

No.	Display	Function
1	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	Music calendar (Displays TRACK NO.)
2	① ▮▮ ② ▶ DISC ③ ④ OUT	① . . . . . Indecates PAUSE mode. ② . . . . . Indecates PLAY mode. Blinks only when the tracks are programmed in STOP mode. ③ . . . . . Lights up when the disc tray is closed. ④ . . . . . Lights up when the disc tray is closed and there is no disc placed.
3	TRACK NO. 88	Displays the TRACK NO. of the track being played, or the designed TRACK NO. during programming or when recalling a program for a check, etc.
4	①--PNO. ②--INDEX P.C. ③ 88 ④	Normal play mode . . . . . ② lights up and ④ displays the INDEX NO. Program mode . . . . . ① lights up and ④ displays the Program No. When checking a program . . . . . ① and ③ light up and ④ displays the Program No.
5	MAX. TNO. 88	Displays the maximum TRACK NO. after the TOC is read.
6	▶TRACK ▶PGM ▶TIME ▶SINGLE	Indicates the four types of direct play mode. The "▶ " (arrow) indicator, located to the left of the designed mode lights up.
7	① ④ ② SINGLE TOTAL TIME TIME ③ –88:88	When ① lights, ④ displays the relative remaining time of the TRACK NO. being played. When ② lights, ④ displays the absolute remaining time of the current position on the disc. (from the beginning of the disc.) When ① and ③ light, ④ displays the relative remaining time fo the TRACK NO. being played. When ② and ③ light, ④ displays the absolute remaining time on the disc. (from the current position to the end of the disc.)
8	↻	Lights up when repeat plays is designated. (Repeat indicator)
9	SPACE	Lights up when the gap between tracks is set to 4 seconds.

Table 2–1

CIRCUIT DESCRIPTION

3. Microprocessor μPD75208CW-052 (X25-2932-71 : IC1)

3–1. Terminal connection diagram

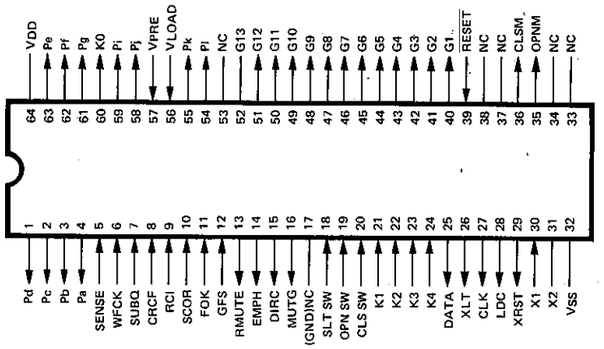


Fig. 3–1

3–2. Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1~4	Pd~Pa	O	FL tube segment display outputs.
5	SENSE	I	SENSE signal input (from CXD1125Q, CXA1082S).
6	WFCK	I	Q data readout clock input (from CXD1125Q).
7	SUBQ	I	Q data input (from CXD1125Q).
8	CRCF	I	Q data CRC OK ("H") input (from CXD1125Q).
9	RCI	I	Remote control signal input.
10	SCOR	I	Q data sync signal input (from CXD1125Q).
11	FOK	I	Focus OK ("H") input (from CXA1081S).
12	GFS	I	EMF sync OK ("H") input (from CXD1125Q).
13	RMUTE	O	Relay muting ON/OFF ("L"/"H") signal output.
14	EMPH	O	Emphasis ON/OFF ("L"/"H") signal output.
15	DIRC	O	DIRC signal output (to CXA1081S).
16	MUTG	O	MUTG signal output for muting ON/OFF ("H"/"L") (from CXD1125Q).
18	SLT SW	I	Start limit SW signal input (SW ON : "L").
19	OPN SW	I	Tray open SW signal input (SW ON : "L").
20	CLS SW	I	Tray close SW signal input (SW ON : "L").
21~24	K1~K4	I	Main unit key inputs.
25	DATA	O	Control data signal output (to CXD1125Q, CXA1082S).
26	XLT	O	Control data latch signal output (to CXD1125Q, CXA1082S).
27	CLK	O	Control data clock signal output (to CXD1125Q, CXA1082S).
28	LDC	O	Laser ON/OFF ("H"/"L") signal output.
29	XRTS	O	Control reset signal output (to CXD1125Q, CXD1082S).
30	X1	I	Clock oscillation X'tal connection terminals. (Oscillation frequency = 4.194MHz).
31	X2	O	
32	Vss	–	GND.
35	OPNM	O	Tray open/close signal output. Normally OPNM : "L" and CLSM : "L".
36	CLSM	O	For opening, OPNM : "H" and CLSM : "L". For closing, OPNM : "L" and CLSM : "H".
39	$\overline{\text{RESET}}$	I	Reset signal input.
40~52	G1~G13	O	FL tube digit display output.
54	Pl	O	FL tube segment display output.
55	Pk	O	
56	VLOAD	I	GND.
57	VPRE	I	GND.
58	Pj	O	FL tube segment display output.
59	Pi	O	
60	KO	O	Key sense output signal.
61~63	Pg~Pe	O	FL tube segment display output.
64	VDD	–	+5V.

Table 3–1

CIRCUIT DESCRIPTION

3–3. Test mode

If the TEST pins are short-circuited when the power is turned ON, the microprocessor enters test mode. With the microprocessor set to test mode, each operation can be easily checked after making a repaire or adjustment.

With the DP-969, the microprocessor can be set to test mode by short-circuiting pin 8 and pin 9 of the ELECTRIC UNIT (X25-2932-71).

Note : "Set mode" shows the normal status.

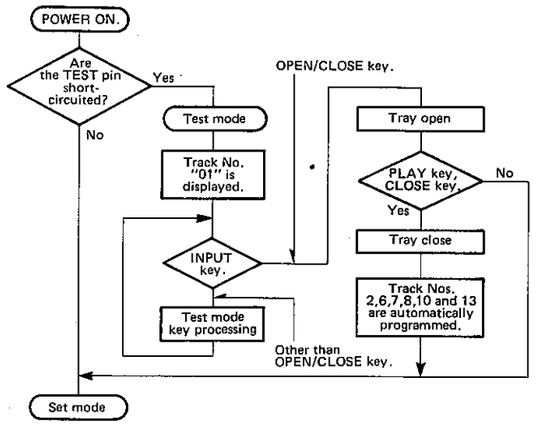


Fig. 3–2

• Effective keys in the Test mode and their functions

No.	Input key	Function	Track No. display
1	PLAY	(1) Focus servo . . . . . ON. (2) Tracking servo . . . . . ON. (3) Feed servo . . . . . ON. When the key is pressed in the Stop mode, the servoes are switched ON automatically in the order from (1) to (3).	TRACK NO. 01 → Displayed for a few seconds after (1) to (3). → Disc's Track No. is displayed.
2	CHECK	(1) Focus servo . . . . . ON. (2) Tracking servo . . . . . OFF. (3) Feed servo . . . . . OFF.	TRACK NO. 03
3	CLEAR	(1) Focus servo . . . . . ON. (2) Tracking servo . . . . . ON. (3) Feed servo . . . . . OFF.	TRACK NO. 04
4	STOP	(1) Focus servo . . . . . OFF. (2) Tracking servo . . . . . OFF. (3) Feed servo . . . . . OFF.	TRACK NO. 01
5	FF (▶▶)	In Stop mode : Moves the PU slightly to the outer tracks. With feed servo ON : Switches the tracking gain to "H".	
6	FR (◀◀)	In Stop mode : Moves the PU slightly to the inner tracks. With feed servo ON : Switches the tracking gain to "L".	
7	Numeric (digit) keys (0~9)	Jumps the number of tracks as follows: Key: 1 / Number of tracks: 1 / Direction: Outward Key: 2 / Number of tracks: 4 / Direction: Outward Key: 3 / Number of tracks: 16 / Direction: Outward Key: 4 / Number of tracks: 32 / Direction: Outward Key: 5 / Number of tracks: 1000 / Direction: Outward Key: 6 / Number of tracks: 1 / Direction: Inward Key: 7 / Number of tracks: 4 / Direction: Inward Key: 8 / Number of tracks: 16 / Direction: Inward Key: 9 / Number of tracks: 32 / Direction: Inward Key: 0 / Number of tracks: 1000 / Direction: Inward	
8	OPEN/CLOSE	When the tray is opened and the closed again in test mode, TRACK NOs. 2, 6, 7, 8, 10 and 13 are automatically programmed. Opening the tray again will cause the unit to enter set mode.	

Table 3–2

CIRCUIT DESCRIPTION

3–4. Flow chart of test mode

- **Flow chart from tray OPEN status after power ON**

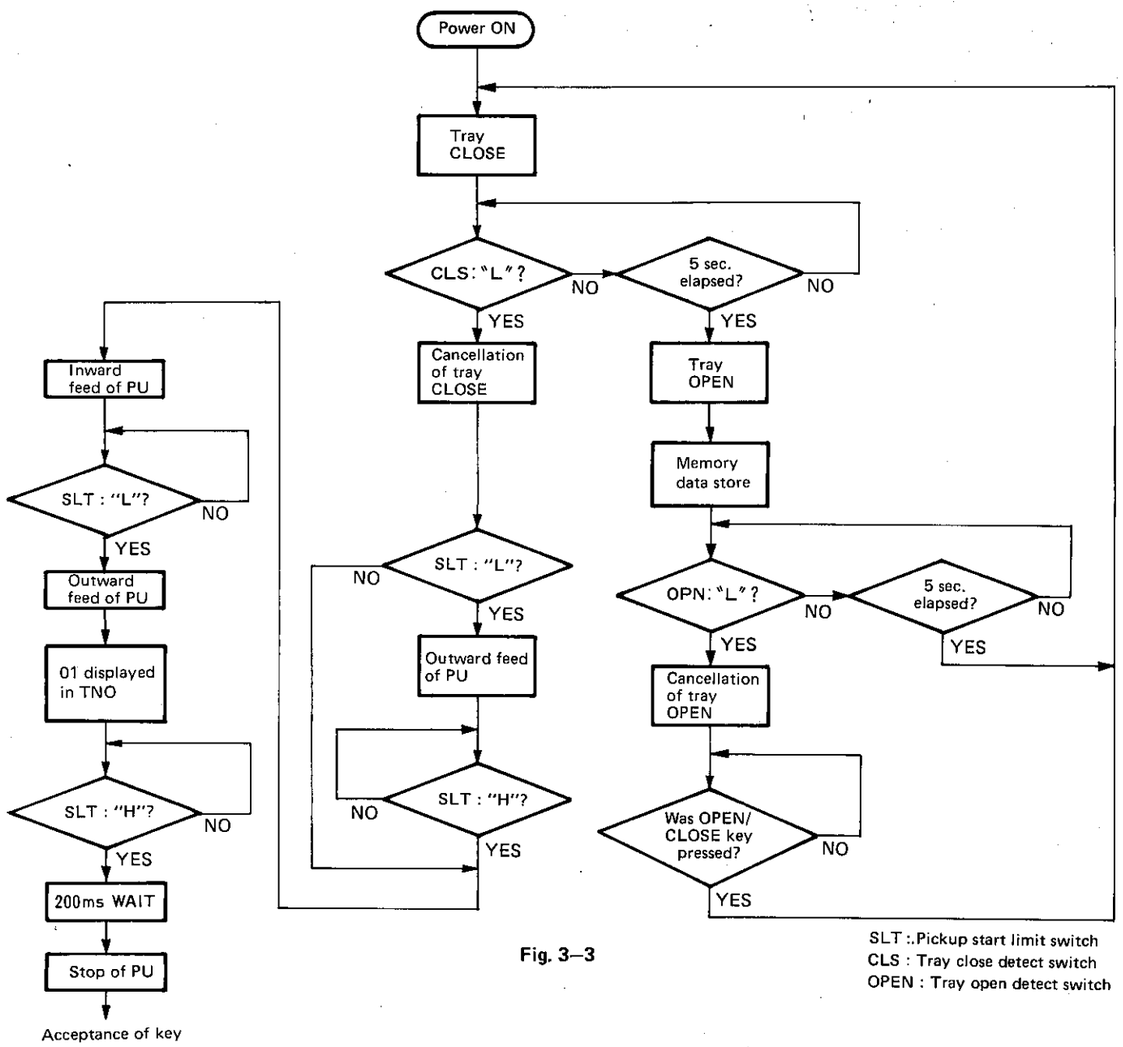


Fig. 3–3

SLT :.Pickup start limit switch
CLS : Tray close detect switch
OPEN : Tray open detect switch

CIRCUIT DESCRIPTION

- **Focus search & focus servo ON**

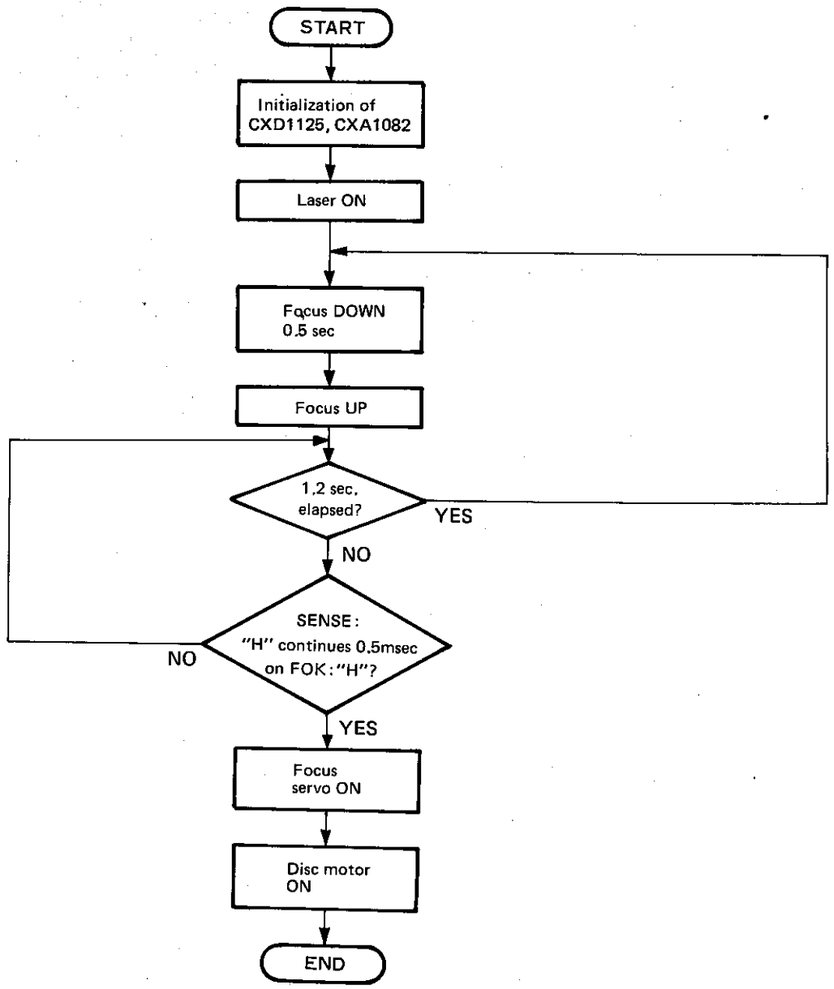


Fig. 3–4

CIRCUIT DESCRIPTION

- **Tracking servo ON**

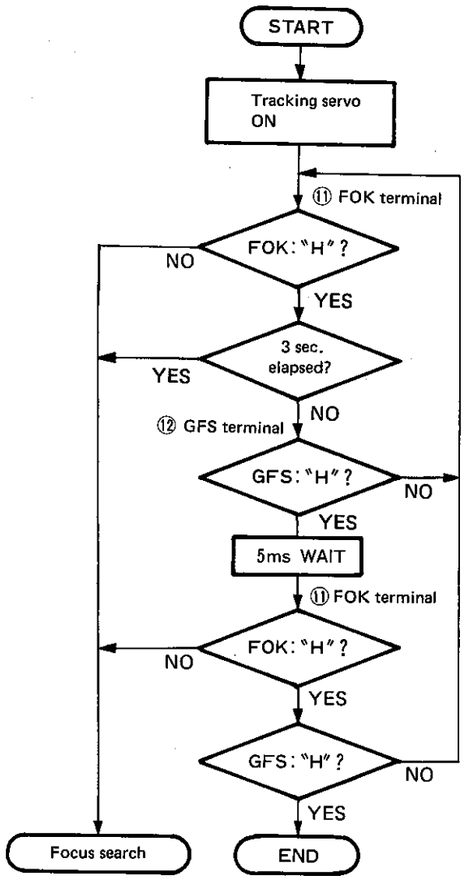


Fig. 3–5

- **Disc motor stop**

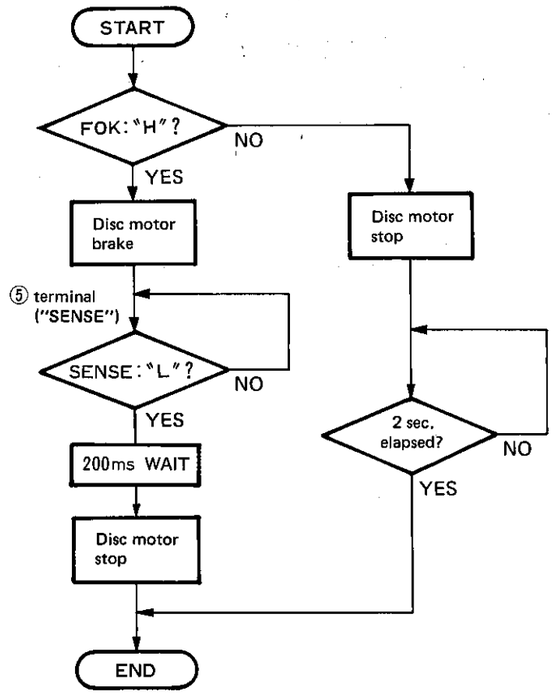


Fig. 3–6

DP-969

CIRCUIT DESCRIPTION

- **From loading of Q data to display**

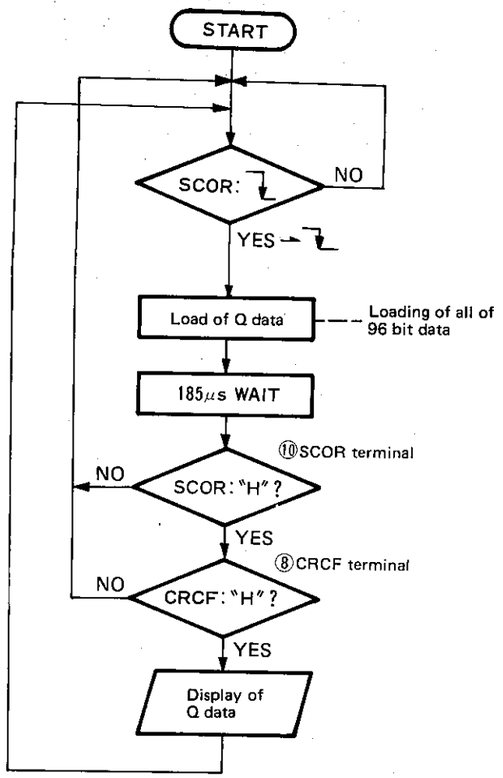


Fig. 3–7

- **Flow chart from the time the tray opens until the STOP indicator lights, after pressing the tray.**

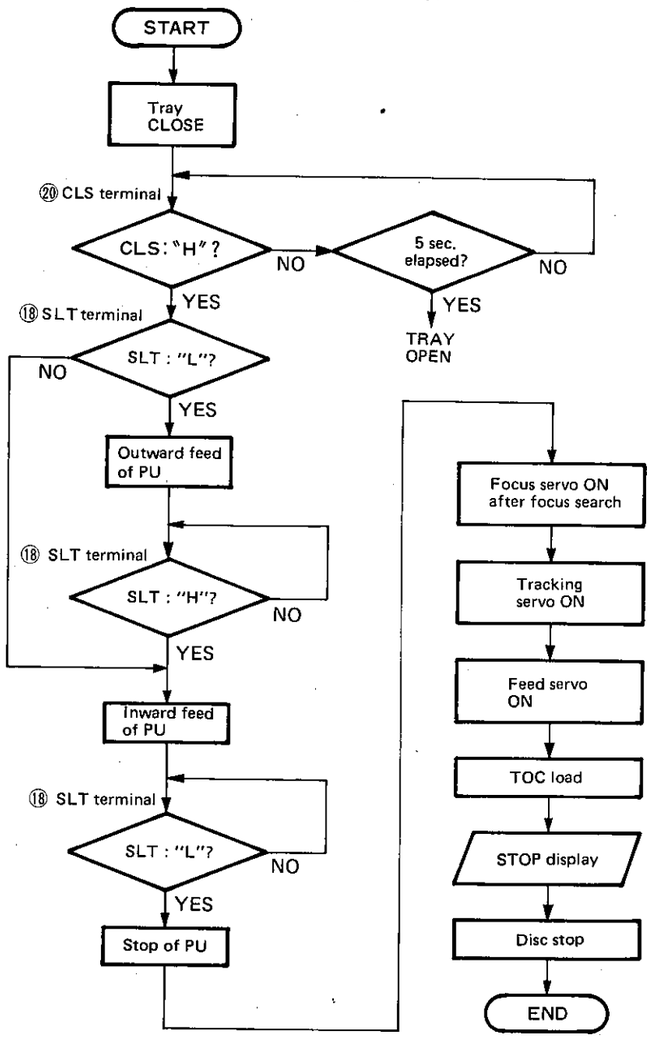


Fig. 3–8

CIRCUIT DESCRIPTION

4. RF amplifier CXA1081S (X25-2932-71 : IC5)

The CXA1081S supplies the following functions as required for controlling the RF amp in the compact disc player.

- RF amp
- Focusing error amp
- Tracking error amp
- APC circuit
- Auto asymmetry control amp
- Focus OK detection circuit
- Mirror detection circuit
- Defect detection circuit
- EFM comparator

4–1. Block diagram

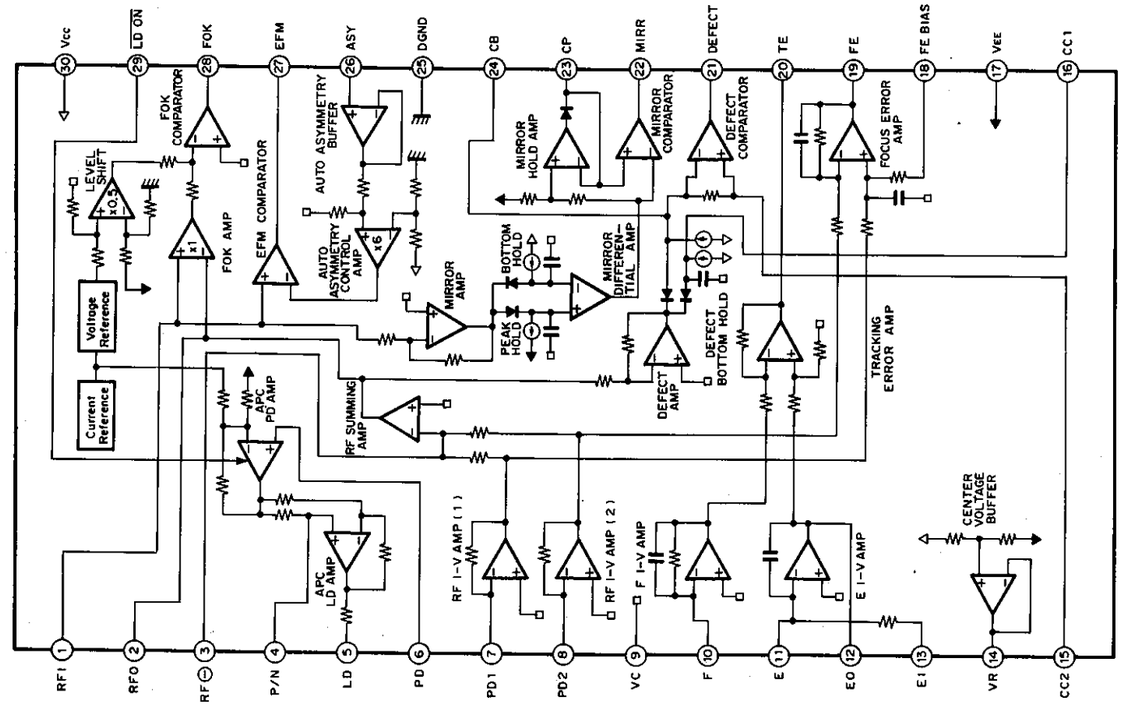


Fig. 4–1

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CIRCUIT DESCRIPTION

4–2. Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	RFI	I	Input pin of the C-coupled signal output from the RF summing amp.
2	RFO	O	Check point of eye pattern for the RF summing amp output pin.
3	RF ⊖	I	RF summing amp feedback input pin.
4	P/N	I	P-sub/L-sub select pin of LD. (DC voltage: in N-sub mode)
5	LD	O	APC LD amp output pin. (DC voltage: PD open in N-sub mode)
6	PD	I	APC PD amp input pin. (DC voltage: open)
7	PD1	I	RF I–V amp (1) invert input pin. Current input by connecting to PIN diode A + C.
8	PD2	I	RF I–V amp (2) invert input pin. Current input by connecting to PIN diode B + D.
9	VC	–	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply. Connected to VR (pin 14) when using a single-voltage power supply.
10	F	I	F I–V amp invert input pin. Current input by connecting to PIN diode F.
11	E	I	E I–V amp invert input pin. Current input by connecting to PIN diode E.
12	EO	O	E I–V amp output pin.
13	EI	I	E I–V amp feedback input pin. For E I–V amp gain adjustment.
14	VR	O	DC voltage output pin of (Vcc + V_{EE})/2.
15	CC2	I	Input pin of the C-coupled signal output from the defect bottom hold.
16	CC1	O	Defect bottom hold output pin.
17	VEE	–	Connected to the negative power supply when using a positive (+)/negative (–) dual-voltage power supply. Connected to GND when using a single-voltage power supply.
18	FE BIAS	I	Bias pin at the focus error amp non-invert side. For CMR adjustment of the focus error amp.
19	FE	O	Focus error amp output pin.
20	TE	O	Tracking error amp output pin.
21	DEFECT	O	Defect comparator output pin. (DC voltage: connected to a 10kΩ load).
22	MIRR	O	Mirror comparator output pin. (DC voltage: connected to a 10kΩ load).
23	CP	I	Mirror hold capacitor output pin. Mirror comparator non-invert input.
24	CB	I	Defect bottom hold capacitor connect pin.
25	DGND	–	Connected to GND when using a positive (+)/negative (–) dual-voltage power supply. Connected to GND (V_{EE}) when using a single-voltage power supply.
26	ASY	I	Auto asymmetry control input pin.
27	EFM	O	EFM comparator output pin. (DC voltage: connected to a 10kΩ load).
28	$\overline{FOK}$	O	FOK comparator output pin. (DC voltage: connected to a 10kΩ load).
29	$\overline{LD\ ON}$	I	LD ON/OFF select pin. (DC voltage: when LD ON).
30	Vcc	–	Positive power supply.

Table 4–1

CIRCUIT DESCRIPTION

4–3. Explanation of function

- **RF amp**

The photodiode current input to the input pins (PD1, PD2) is converted to a voltage by an equivalent resistance of 58kΩ in RF I–V amp (1) and (2) respectively. The voltage which is converted from the current of the photodiode (A + B + C + D) is added in the RF summing amp and is output from the RFO pin. The eye pattern can be checked at this pin.

The low frequency component of the RFO output voltage, V_{RFO} is represented by the following equation:

$$V_{RFO} = 2.2 \times (V_A + V_B)$$
$$= 127.6k\,\Omega \times (i_{PD1} + i_{PD2})$$

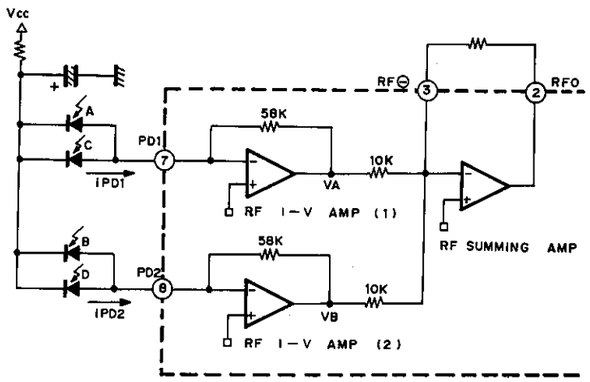

Fig. 4–2 RF I–V amplifier

- **Focus error amp**

The difference between the RF I–V amp (1) output (VA) and the RF I–V amp (2) output (VB) is calculated, and the current of the photodiode (A + C – B – D) is converted to a voltage and output.

The FE output voltage (low frequency) is represented by the following equation:

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (i_{PD2} - i_{PD1}) \times 315.4k\,\Omega$$

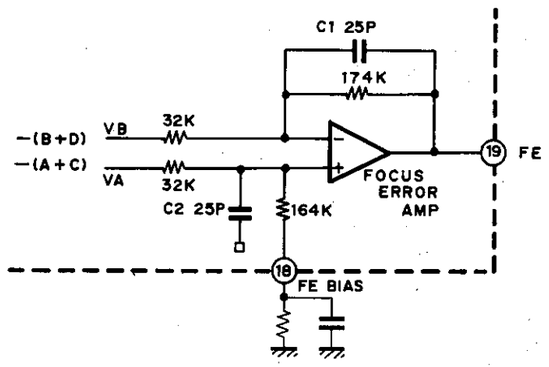

Fig. 4–3

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CIRCUIT DESCRIPTION

- **Tracking error amp**

The current from the side spot photodiodes is input to pins E and F and is converted to a voltage by the E I–V amp and F I–V amp respectively. That is:

$$V_F = iF \times 403k\,\Omega$$
$$V_E = iE \times 260k\,\Omega \times R_A/(R_B + 22k) + (R_A + 260k)$$

The difference between the E I–V amp and the F I–V amp is calculated by the tracking error amp, and the photodiode (E–F) current is converted to a voltage and output.

$$V_{TE} = (V_E - V_F) \times 3.2$$
$$= (iE - iF) \times 1290k\,\Omega$$

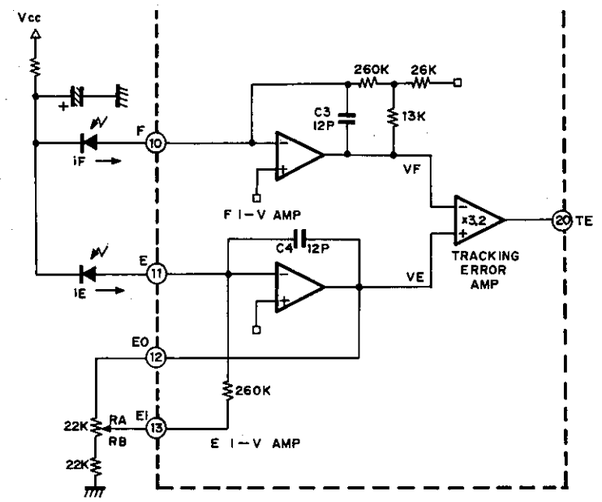

Fig. 4–4

- **Focus OK circuit**

The focus OK circuit creates a timing window, turning the focusing servo ON with the focus search status.

While the RF signal is present at pin 2, its HPF output is present at pin 1. At the same time, the LPF output (opposite phase) of the focus OK amp is obtained.

The focus OK output is inverted when $V_{RFI} - V_{RFO} \fallingdotseq -0.37V$.

C34 is used to determine the time constants of the EFM comparator, the HPF in the mirror circuit, and the LPF in the focus OK amp. Normally, C34 = 0.01μF is selected, with fc = 1kHz. This will prevent degradation of the block error rate due to an RF envelope lack caused by cracks, etc. on the disc.

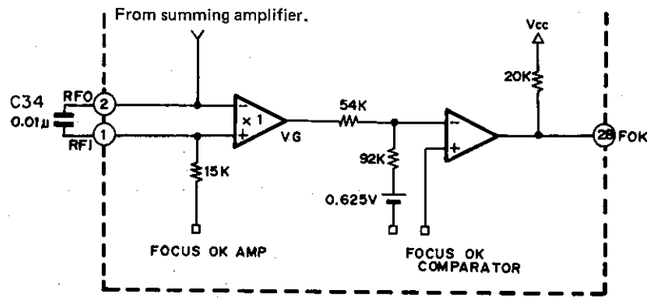

Fig. 4–5

CIRCUIT DESCRIPTION

- **Mirror circuit**

In the mirror circuit, after the RFI signal is amplified, both peak and bottom holds are held by a time constant which can follow a traverse of 30kHz, while only the bottom hold is held by a time constant which can follow a cyclic period envelope variation respectively.

These peak/bottom hold signals, H and I are differentially amplified to obtain the DC-reproduced envelope signal J.

This signal is compared with signal K, that the 2/3 level of the peak value is peak held by a large time constant so that the mirror output is obtained. That is, the mirror output goes "L" on the disc tracks and goes "H" between tracks (mirror section). In addition, the output goes "H" when a defect is detected. The time constant of the mirror hold should be quite larger when compared with the traverse signal.

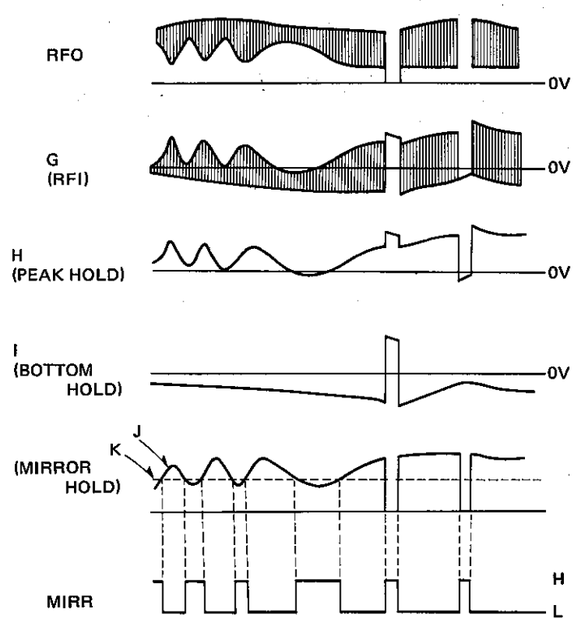

Fig. 4–6

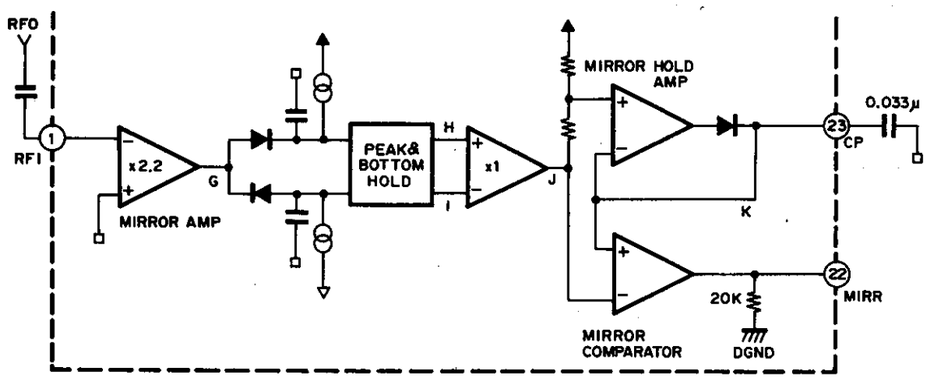

Fig. 4–7

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CIRCUIT DESCRIPTION

- **EFM comparator**

The EFM comparator converts the RF signal into a binary coded signal. Since asymmetry caused by dispersion when manufacturing the discs cannot be reduced by AC coupling only, the reference voltage of the EFM comparator is controlled using the characteristics that the present probability of a 1 or 0 is 50% each for the binary coded EFM signal.

The EFM comparator is designed as a current switching type, and the "H" and "L" levels are not equal to the power voltages. Therefore, feedback is required via a CMOS buffer.

R51, R50, C30 and C31 constitute a LPF to obtain the DC component of (Vcc + DGND)/2 (V). If the cut-off frequency (fc) is set to more than 500Hz, leakage of the EFM low frequency signals will be greatly increased and will result in a degradation of the block error rate.

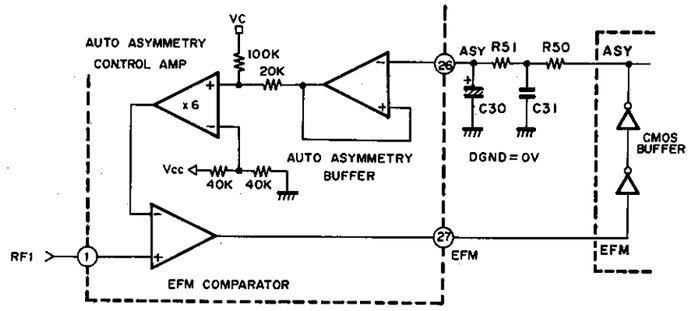

Fig. 4–8

- **Defect circuit**

After inverting the RFI signal, the defect circuit bottom holds with the two long/short time constants. The bottom hold with a shorter time constant responds to a mirror defect of more than 0.1msec on the disc, and the bottom hold with a longer time constant holds the mirror level obtained immediately before the defective section. These signals are C-coupled, then differentiated with level shifting. The signals are compared with each other to generates the mirror defect detecting signals.

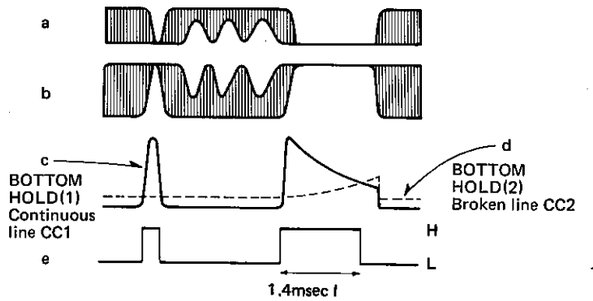

Fig 4–9

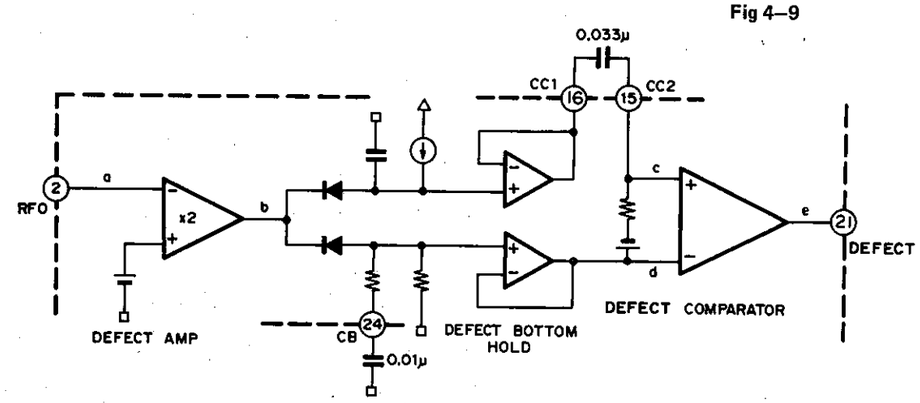

Fig. 4–10

CIRCUIT DESCRIPTION

5. Servo signal processor CXA1082S (X25-2932-71 : IC4)

CXA1082S is the servo signal processor for the compact disc players, and has the following functions:

- Focusing servo control
- Tracking servo control
- Thread servo control
- Spindle servo
  Low Pass Filter, drive amp
- EFM clock generating PLL
  Loop filter: 8.64MHz VCO
- Auto sequencer, incorporating a ROM

5–1. Terminal connection diagram

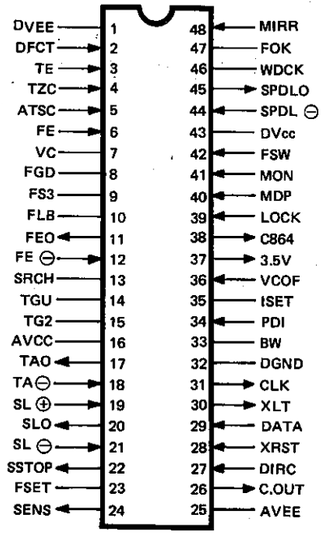

Fig. 5–1

5–2. Block diagram

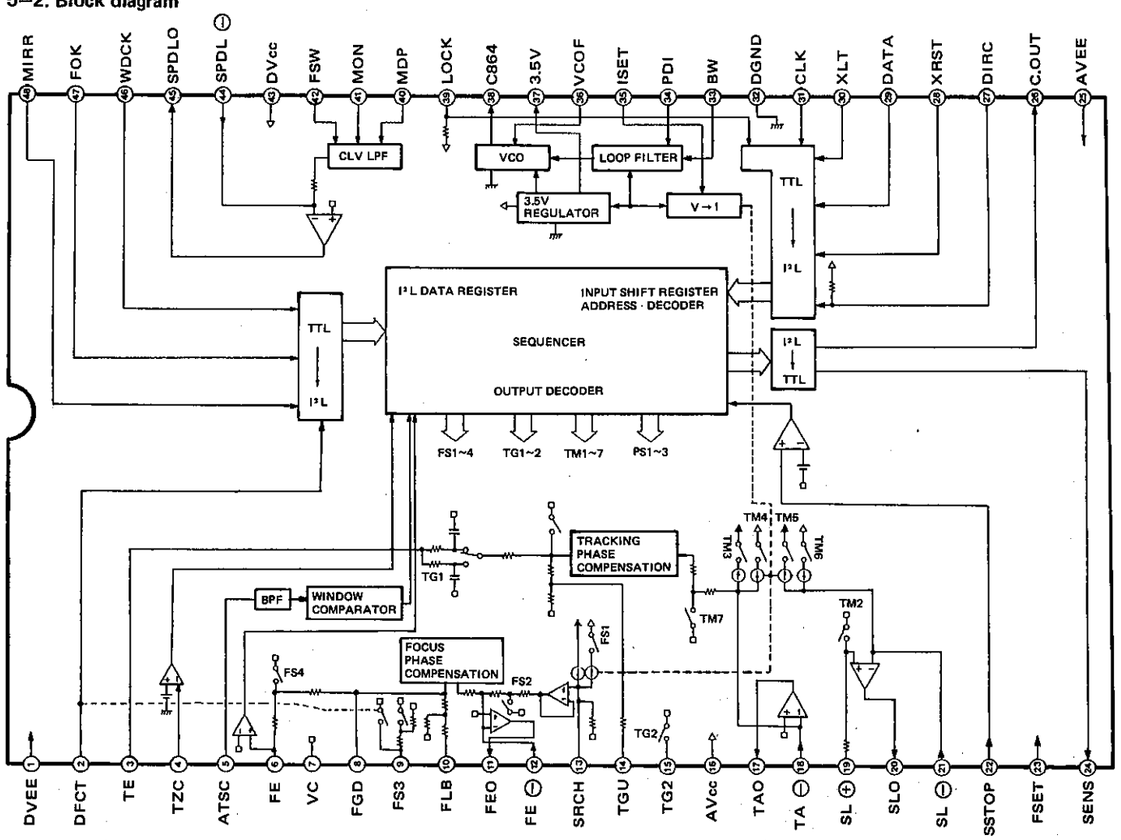

Fig. 5–2

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CIRCUIT DESCRIPTION

5–3. Explanation of terminal

Terminal No.	Terminal name	I/O	Function
1	DVEE	–	Digital line power supply pin.
2	DFCT	I	Input pin for an interface with a microprocessor, etc.
3	TE	I	Tracking error signal input pin.
4	TZC	I	Tracking zero-cross comparator input pin.
5	ATSC	I	Window comparator input pin for ATSC detection.
6	FE	I	Focus error signal input pin.
7	VC	–	Analog line power supply pin.
8	FGD		When lowering the high frequency gain of the focus servo, insert a capacitor between this pin and pin 9 (FS3).
9	FS3		High frequency gain of the focus servo is selected by switching FS3 ON/OFF.
10	FLB		Time constant external connect pin for boosting the focus servo low frequencies.
11	FEO	O	Power transistor drive op amp output pin.
12	FE ⊖	I	Focus amp invert input pin.
13	SRCH		Time constant external connect pin for creating the focus search waveform.
14	TCU		Time constant external connect pin for selecting the tracking high frequency gain.
15	TG2		Time constant external connect pin for selecting the tracking high frequency gain.
16	AVcc	–	Analog line power supply pin.
17	TAO	O	Power transistor drive op amp output pin.
18	TA ⊖	I	Tracking amp non-invert input pin.
19	SL ⊕	I	Thread amp non-invert input pin.
20	SLO	O	Power transistor drive op amp output pin.
21	SL ⊖	I	Thread amp invert input pin.
22	SSTOP	I	Limit switch ON/OFF detection signal input pin for detecting innermost edge of the disc.
23	FSET	I	Setting pin for the focus tracking phase peak value compensation, and f_0 of the CLV LPF.
24	SENS	O	Input for an interface with a microprocessor.
25	AVEE	–	Analog line power supply pin.
26	C.OUT	O	Output pin for an interface with a microprocessor.
27	DIRCT	I	Input pin for an interface with a microprocessor.
28	XRST	I	Input pin for an interface with a microprocessor.
29	DATA	I	Input pin for an interface with a microprocessor.
30	XLT	I	Input pin for an interface with a microprocessor.
31	CLK	I	Input pin for an interface with a microprocessor.
32	DGND	–	Digital line GND pin.
33	BW	I	Loop filter time constant external connect pin.
34	PDI	I	Input pin for the phase comparator output PD0 of the CXD1125Q.
35	ISET	I	Follows the current which determines the level of the focus search, track jump and thread kick.
36	VCOF	I	The resistance between this pin and pin 37 (3.5V) is almost proportional to the self-advancing frequency of the VCO.
37	3.5V	O	3.5V stabilizing power supply output pin.
38	C864	O	8.64MHz VCP output pin.
39	LOCK	I	Input pin for an interface with a microprocessor.
40	MDP	I	CXD1125Q MDP pin connect pin.
41	MON	I	CXD1125Q MON pin connect pin.
42	FSW	I	LPF time constant external connect pin for the CLV servo error signal.
43	DVcc	–	Digital line power supply pin.
44	SPDL ⊖	I	Spindle drive amp invert input pin.
45	SPDLO	O	Power transistor drive op amp output pin.
46	WDCK	I	Input pin for an interface with a microprocessor.
47	FOK	I	Input pin for an interface with a microprocessor.
48	MIRR	I	Input pin for an interface with a microprocessor.

Table 5–1

CIRCUIT DESCRIPTION

6. Digital signal processing LSI CXD1125Q (X25-2932-71 : IC2)

The CXD1125Q is the digital signal processing LSI for the compact disc player, and has the following functions. All the digital signals for reproduction can be processed internally with this one-chip design.

- Bit clock reproduction by an EFM-PLL circuit.
- EFM data demodulation.
- Frame sync signal detection, protection and insertion.
- Powerful error detection and correction.
- Interpolation with average value or by holding the previous value.
- Demodulaiton of sub code signal or error detection of sub code Q.
- Spindle motor CLV servo.
- 8-bit tracking counter.
- CPU interface with a serial bus.
- Sub code Q register.
- D/A interface output.

6–1. Block diagram

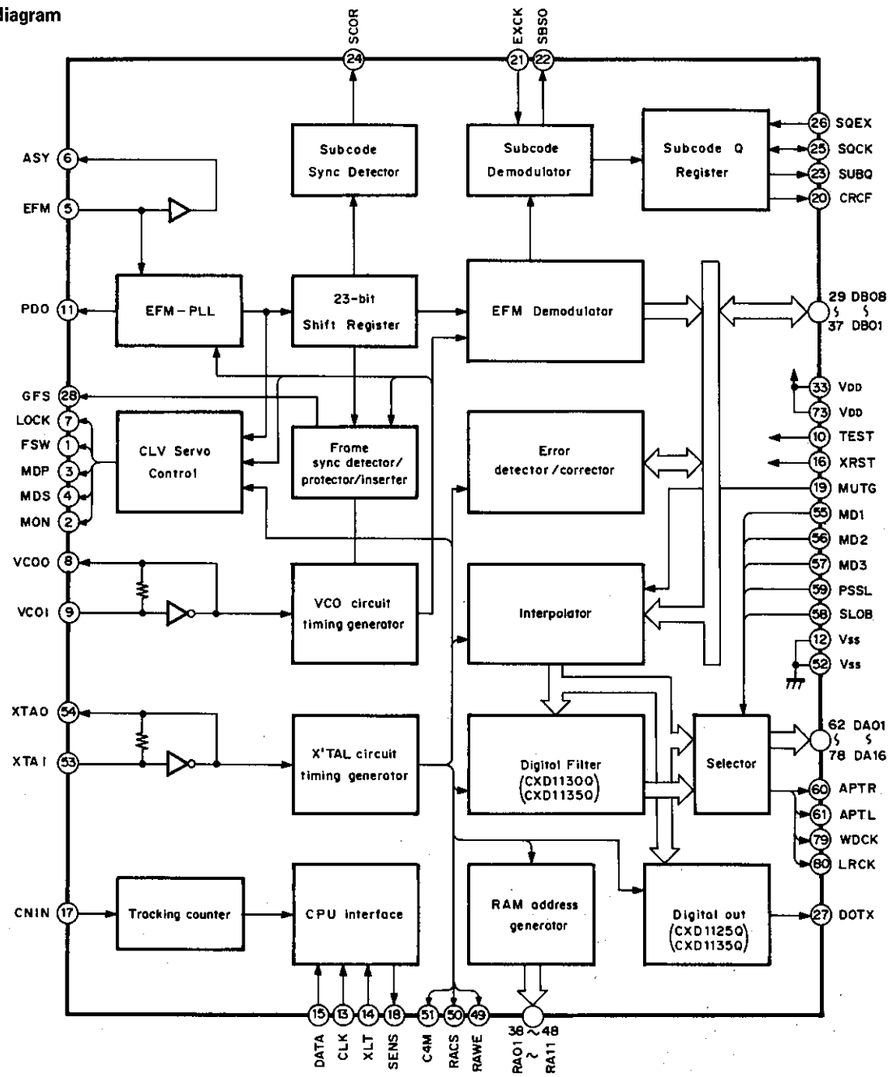


Fig. 6–1

DP-969

CIRCUIT DESCRIPTION

6–2. Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high. When it is "L" for eight times, in arow, outputs "L".
8	VCOO	O	VCO output. f = 8.6436MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V)
11	PDO	O	Phase comparison output of EFM signal and VCO/2.
12	Vss	–	GND (0V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	I	Input of tracking pulse.
18	SENSE	O	Output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case where ATTM of internal register A is "L". normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code Q read-off clock.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync SO + S1 output.
25	WFCK	O	Write Frame Clock output. f = 7.35kHz when the frame sync is locked.
28	CFS	O	Output of display of lock status of frame sync.
29	DB08	I/O	Data terminal of external RAM. DATA 8 (MSB)
30	DB07	I/O	Data terminal of external RAM. DATA 7
31	DB06	I/O	Data terminal of external RAM. DATA 6
32	DB05	I/O	Data terminal of external RAM. DATA 5
33	VDD	—	Power supply (+ 5V)
34	DB04	I/O	Data terminal of external RAM. DATA 4
35	DB03	I/O	Data terminal of external RAM. DATA 3
36	DB02	I/O	Data terminal of external RAM. DATA 2
37	DB01	I/O	Data terminal of external RAM. DATA 1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM. (active at "L").
50	RACS	O	Chip select signal output to external RAM. (active at "L").

Table 6–1

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
51	C4M	O	Crystal dividing output. f = 4.2336MHz.
52	Vss	–	GND (0V).
53	XTAI	I	Crystal oscillator input. f = 8.4672MHz or 16.9344MHz depending on the mode selected.
54	XTAO	O	Crystal oscillator output. f = 8.4672MHz or 16.9344MHz depending on the mode selected.
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select output. Serial output when "L", parallel output when "H".
60	APTR	O	Aperture compensation control output. "H" when R-ch.
61	APTL	O	Aperture compensation control output. "H" when L-ch.
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL = "H", C1F1 output when PSSL = "L".
63	DA02	O	DA02 output when PSSL = "H", C1F2 output when PSSL = "L".
64	DA03	O	DA03 output when PSSL = "H", C2F1 output when PSSL = "L".
65	DA04	O	DA04 output when PSSL = "H", C2F2 output when PSSL = "L".
66	DA05	O	DA05 output when PSSL = "H", C2FL output when PSSL = "L".
67	DA06	O	DA06 output when PSSL = "H", C2PO output when PSSL = "L".
68	DA07	O	DA07 output when PSSL = "H", RFCK output when PSSL = "L".
69	DA08	O	DA08 output when PSSL = "H", WFCK output when PSSL = "L".
70	DA09	O	DA09 output when PSSL = "H", $\overline{\text{PLCK}}$ output when PSSL = "L".
71	DA10	O	DA10 output when PSSL = "H", UGFS output when PSSL = "L".
72	DA11	O	DA11 output when PSSL = "H", GTOP output when PSSL = "L".
73	VDD	–	Power supply (+ 5V).
74	DA12	O	DA12 output when PSSL = "H", RAOV output when PSSL = "L".
75	DA13	O	DA13 output when PSSL = "H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL = "H", $\overline{\text{C21O}}$ output when PSSL = "L".
77	DA15	O	DA15 output when PSSL = "H", C21O output when PSSL = "L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL = "H", DATA output when PSSL = "L".
79	WDCK	O	Strobe signal output. 88.2kHz.
80	LRCK	O	Strobe signal output. 44.1kHz.

Notes:

C1F1 :
C1F2 : } Error correction status monitor output for C1 decode.

C2F1 :
C2F2 : } Error correction status monitor output for C2 decode.

C2PO : C2 pointer signal.

C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.

RFCK : Read frame clock output. 7.35MHz when locked to the crystal line.

WFCK : Write frame clock output. 7.35MHz when locked to the crystal line.

$\overline{\text{PLCK}}$: VCO/2 output. f = 4.3218MHz when locked to the EFM signal.

UGFS : Non-protected frame sync pattern output.

GTOP : Frame sync protect status display output.

RAOV : ±4 frame jitter absorption RAM overflow and underflow display output.

C4LR : Strobe signal. 176.4kHz.

$\overline{\text{C21O}}$: C21O invert output.

C21O : Bit clock output. 2.1168MHz.

DATA : Audio signal serial data output.

Table 6–1

CIRCUIT DESCRIPTION

6–3. Explanation of functions

- **CPU interface**

1) Data input

Each register may be set by input of 4 bit address, and 4 bit data from LSB in the timing that is shown in Fig. 6–2 to three terminals, XLT, CLK and DATA. The address and data of each terminal are as shown in Table 6–2, and their functions are as follows. The contents of each register become entirely 0 when XRST = "L".

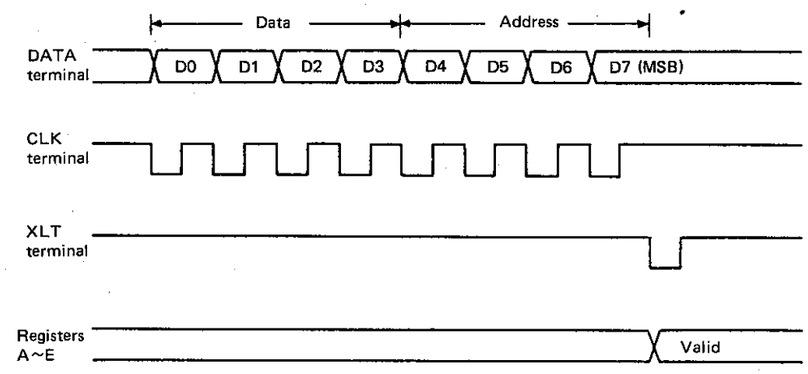


Fig. 6–2 Timing chart for data input

2) Registers

○ Register 9 – New function control

Controls the new functions added to the CX23035.

D3 : ZCMT Switches the zero cross mute function ON/OFF. Details are described in **"Interpolation and Mute, Attenuate"**.

D2 : HZPD One of the defect countermeasures. Switches ON/OFF the function which makes the PD0 pin a high impedance (Z) for a maximum of 0.55ms from the rising edge of GFS. Details are described in **"Countermeasures to defects"**.

D1 : NCLV Switches between the old CLV-P servo and the new CLV-P servo by comparison with newly added base counter. Details are described in **"CLV servo control"**.

D0 : CRCQ Switches ON/OFF the function which outputs the CRCF data to the SUBQ pin from the rising edge of SCOR to the trailing edge of SQCK. Details are described in **"5) Subcode output"**.

○ Register A – Sync. protection, attenuator control

D3 : GSEM
D2 : GSEL
D1 : WSEL } Provided for switching frame synk. protection characteristics in correspondence to the time of playback and time of access. Details will be described in the paragraph of **"EFM demodulation"**.

D0 : ATTM Used for attenuating audio signals by 12dB, and the details will be described in the paragraph of **"D/A interface"**.

○ Registers B and C – Counter set, more significant 4 bits (register C) and less significant 4 bits (register B)

these registers are used for setting the tracking count value. the data of registers B and C are preset in the counter through the 4 bit buffer register assigned by address. Accordingly, when data of either register B or C is input, the contents of both registers are preset in the counter simultaneously as 8 bit data (either buffer register is of "OLD" data.)

D3 : DIV The dividing ratio of RFCK and WFCK in CLV-P mode is fixed, and the phase is compared with RFCK/4 or WFCK/4 respectively, regardless of the status of D3, then output from the MDP pin.

○ Register D-CLV control

D3 : DIV Used for setting the frequency dividing ratio of RFCK, WFCK in the CLV-P mode. When D3 = 0,, phase comparison of RFCK/4 and WFCK/4 is made, and when D3 = 1, phase comparison of RFCK/8 and WFCK/8 is made, and output is made out of MDP terminal in each case.

D2 : T_B Used for determining the period of bottom hold in the CLV-S and CLV-H modes.
Bottom hold is made in the period of RFCK /32 when D2 = 0 or in the period of RFCK/16 when D2 = 1.

D1 : Tp Used for setting the period of peak hold in the CLV-S mode. Peak hold is made in the period of RFCK/4 when D1 = 0 or in the period of RFCK/2 when D1 = 1.

D0 : GAIN Used for setting the gain of MDP terminal output in the CLV-S and CLV-H modes. It is –12dB (time of 3/4 out of the period of RFCK/2 is of high impedance) when D0 = 0 or is 0dB when D0 = 1.

CIRCUIT DESCRIPTION

○ Register E-CLV mode
It is as shown in Table 6–2.
The details of each mode will be described in the paragraph of CLV servo control.

Register name	Command	Address D7~D4	Data D3	D2	D1	D0	SENSE terminal
9*1	New function control	1001	ZCMT	HZPD	NCLV	CRCQ	Z
A*2	Sync protection, attenuator control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Less significant 4 bits	1011	Tc3	Tc2	Tc1	Tc0	$\overline{\text{COMPLETE}}$
C	Counter set, More significant 4 bits	1100	Tc7	Tc6	Tc5	Tc4	$\overline{\text{COUNT}}$
D*3	CLV control	1101	DIV	TB	TP	GAIN	Z
E*4	CLV mode	1110		CLV mode			$\overline{\text{Pw} \geqq 64}$

*1 **Register 9**

		Dn = 0	Dn = 1
ZCMT	D3	Zero-cross MUTE off	Zero-cross MUTE on
HZPD	D2	PDC pin is always active	PDC pin is "Z" at the trailing edge of GFS
NCLV	D1	CLV-P servo for the frame sync signal	CLV-P servo for the base counter
CRCQ	D0	CRCF is not superimposed on SUBQ	SUBQ = CRCF at the raising edge of SCOR

*2 **Register A**

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTG terminal	dB
0	0	0
0	1	$-\infty$
1	0	−12
1	1	−12

*3 **Register D**

DIV	D3	0	RFCK/4 & WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8 & WFCK/8	
TB	D2	0	RFCK/32	Bottom hold period in CLV-S, CLV-H mode
		1	RFCK/16	
TP	D1	0	RFCK/4	Peak hold frequency in CLV-S mode
		1	RFCK/2	
GAIN	D0	0	−12dB	Gain at MDP terminal in CLV-S, CLV-H mode
		1	0dB	

*4 **Register E**

Mode	D3~D0	MDP terminal	MDS terminal	FSW terminal	MON terminal
STOP	0000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	CLV-P	Z	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Z : High impedance

Table 6–2 List of registers

CIRCUIT DESCRIPTION

3) Trakcing counter

This counter is provided for facilitating track jump. Load the number of tracks to be jumped in register B and C. Count of CNIN pulses is started at raising edge of XLT after it was loaded in either register B or C.

When n (n = 256 is meant when register B = register C = 0) is loaded in registers and the address is set at "B", a signal ($\overline{\text{COMPLETE}}$) that is of HIGH level up to "n" pulses and is of LOW level after "n" pulses is output of SENSE terminal. When the address is set at "C", signal ($\overline{\text{COUNT}}$) of CNIN/2n (Hz) is output.

The tracking counter timing chart is shown in Fig. 6–3.

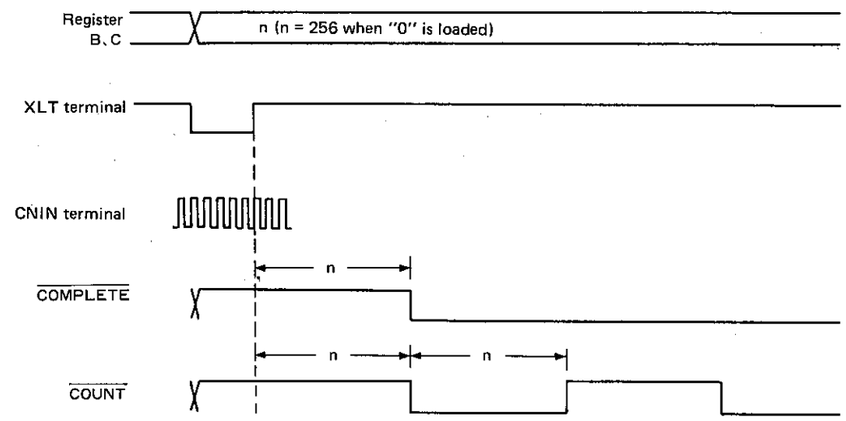


Fig. 6–3 Tracking counter timing chart

4) SENSE

The following signals are output from SENSE terminal depending on the address of D7~D4.

1. $\overline{\text{COMPLETE}}$: Address is "B"; Shown in Fig. 6–3.
2. $\overline{\text{COUNT}}$: Address is "C"; Shown in Fig. 6–3.
3. $\overline{\text{PW} \geqq 64}$: Address is "E"; this signal is of LOW level when the pulse width after bottom hold is over 63, and is of HIGH level otherwise. It is used for detection of a drop in the speed of the spindle motor after braking and so on.

Note : Address setting is determined only by the data that corresponds to D4~D7 which can be input from DATA terminal shown in Fig. 6–2.

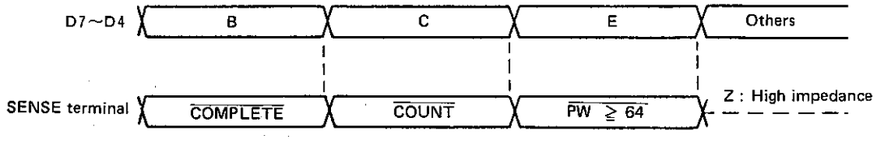


Fig. 6–4 Timing chart of SENSE terminal

CIRCUIT DESCRIPTION

5) Sub code output

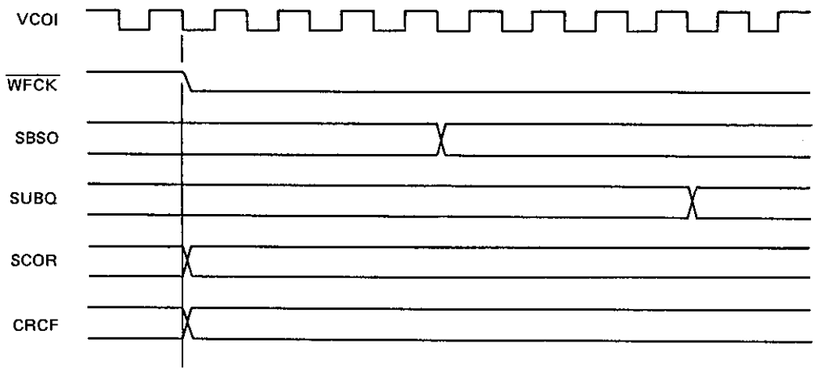
Sub codes P~W loaded in the 8 bit shift register are output out of SBSO terminal in accordance with the clock input through EXCK terminal. when SCOR terminal is "H", S0 · S1 signal is output.

Sub code Q is as follows, depending on the SQEX pin status.

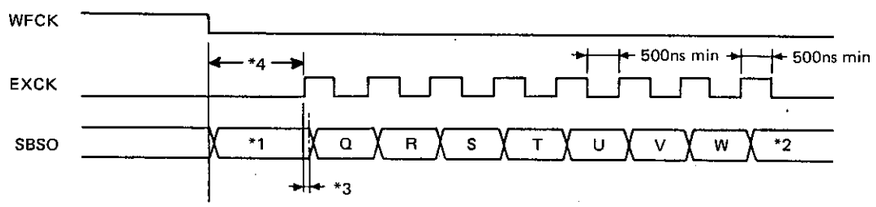
(i) When the SQEX pin is "L", sub code Q is output from the SUBQ pin in synchronism with the WFCK signal in the same way as for the CX23035. The $\overline{\text{WFCK}}$ is also output from the SQCK pin.

(ii) When the SQEX pin is "H", sub code Q is output from the SUBQ pin in synchronism with the external clock (as from the microprocessor). Two 80-bit shift registers, for reading and writing, are incorporated, and while the microprocessor reads, the new sub code Q is written to another register. The microprocessor is interrupted from the outside at the rising edge of the SCOR pin, and after checking the CRCF flag (output to the CRCF pin, or the SUBQ pin when the CRCQ flag is "1"), the CRCF is checked. If CRCF = "H", a shift lock is output and the new sub code Q is read. After the LSB side is replaced with the MSB side by a unit of 4 bits, the data is stored in register. As the microprocessor serially inputs from the LSB first, replacing the 4 bits of data is unnecessary.

(a) Timing of SBSO, SUBQ, SCOR, CRCF



(b) Timing of SBSO, EXCK



*1 : Sub code P is output when SCOR is 0.
S0 · S1 is output when SCOR is 1.
*2 : SBSO is 0 when 8 or more pulses are input to EXCK.
*3 : 4T ~ 6T if the period of VCO is expressed as T.
*4 : Make EXCK low for 10μs from the rising edge of WFCK.
One time period of T = 8.6436MHz.

Fig. 6–5 (1) Timing chart of sub code outputs

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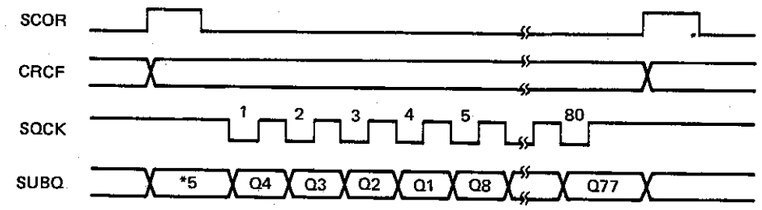
CIRCUIT DESCRIPTION

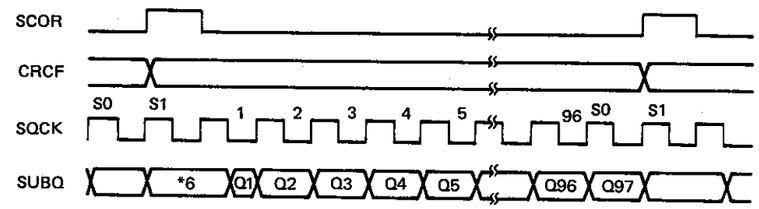
(c) Timing of SCOR, CRCF, SQCK, SUBQ

SQEX= "H" level



*5 : CRCF when CRCQ flag is "1", undefined when "0".

SQEX= "L" level



*6 : CRCF when CRCQ flag is "1", Q98,Q1 when "0".

Fig. 6–5 (2) Timing chart of sub code outputs

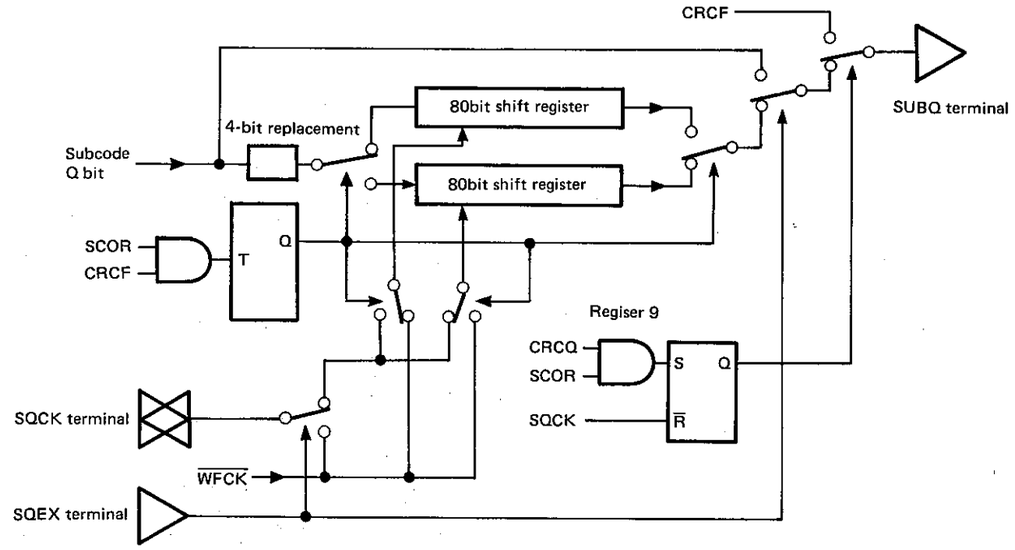


Fig. 6–6

CIRCUIT DESCRIPTION

- **EFM demodulation**

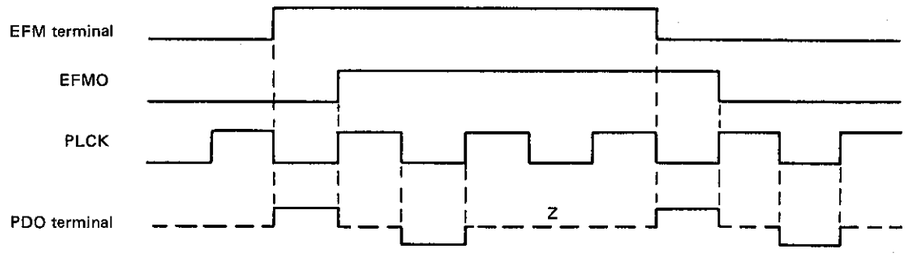
1) Playback of bit clock by EFM-PLL circuit

The EFM signal read out of the optical block contains a clock component of 2.16MHz. Therefore, it is possible to take out a bit clock (PLCK) of 4.32MHz synchronized with this clock by the EFM-PLL circuit.

At each edge of EFM signal, phase comparison is made with PLCK, which is 1/2 of VCO, is made and output is made by TRI STATE out of PDO terminal. The mean value of PDO terminal is about 1/2 VDD if synchronized, but the mean value drops when VCO becomes higher. On the other hand, the mean value increases when VCO becomes less.

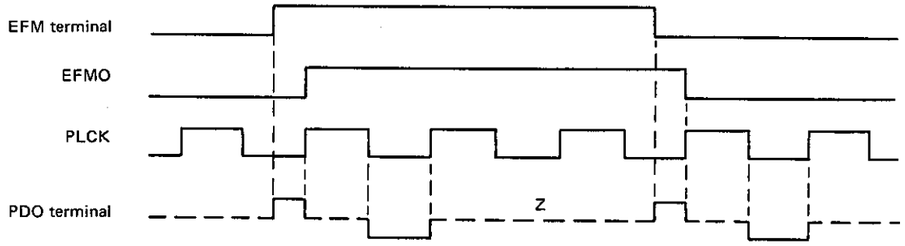
The timing charts of EFM terminal, EFMO, PLCK and PDO are shown in Fig. 6–7.

(a) When EFM signal and VCO are synchronized



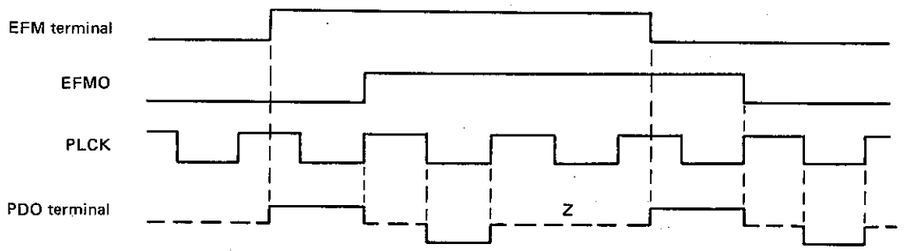
Z : High impedance

(b) When VCO is higher than EFM signal



Z : High impedance

(c) When VCO is less than EFM signal



Z : High impedance

Fig. 6–7 Timing charts of EFM-PLL circuit

CIRCUIT DESCRIPTION

2) Detection, protection and interpolation of frame synchronizing signals

There are cases during recording where the same pattern is detected in the data due to the influence of drop-out and jitter, even if a pattern that is same as the synchronizing signal will not appear.

On the other hand, there also are cases where original frame synchronizing signal is not detected. Therefore, protection and interpolation are required besides detection.

The edge portion only of EFM signal (EFMO) latched with PLCK is converted to "1" and the rest to "0", and then input is to a 23 bit shift register and a frame synchronizing signal is detected.

In order to protect a frame synchronizing signal, a window is provided and the same patterns outside of this window are removed. This width can be selected with WSEL. If no frame synchronizing signal is located in this window, interpolation is made with a signal produced by 588-mal counter (4.3218MHz/588 = 7.35kHz)

A 4 bit counter for counting the number of these frames to be interpolated is provided, and when its count reaches the level selected with GSEL, GSEM, the window is ignored and the 4 bit counter is reset with the next frame synchronizing signal. the GTOP terminal is of "H" while this operation is performed. Further, GFS terminal is of "H" when the frame synchronizing signal generated by the 588-mal counter for making interpolation is synchronized with the frame synchronizing signal from the disc.

The frame synchronizing signal before passage through the window or the wondow is output out of UGFS (DA05 terminal at the time when PSSL = L.)

WSEL	Window width
0	±3 clock
1	±7 clock

GSEM	GSEL	Number of frames to be interpolated	UGFS (PSSL = "L")
0	0	2 frames	Window
0	1	4 frames	Window
1	0	8 frames	Frame synchronizing signal before passage through window.
1	1	13 frames	Window

The timing for write request signal (WREQ), Write Frame Clock (WFCK), etc. is generated based on the protected and interpolated frame synchronizing signal.

3) EFM demodulation

14 bit data is taken out of the 23 bit shift register and is demodulated to 8 bit data through 14 → 8 conversion circuit composed of array logics. Then a write request (WREQ) signal is output to the RAM interface block, and the data is then output to the data bus (DB08~DB01) terminals) of the RAM in accordance with the OENB signal transmitted from said block.

- **Sub code demodulation**

1) Sub code demodulation

synchronizing signals S0, S1 of 14 bit sub codes are detected out of the 23 bit shift register, and sampling is made in the timing that is synchronized with WFCK.

After delay of S0 by one frame, S0 + S1 is output out of SCOR terminal and S0 · S1 is output out of SBSO terminal (only when SCOR = H.)

Data (P~W) of sub codes only is input to the register in the timing synchronized with WFCK after EFM demodulation; and sub code Q is output out of SUBQ terminal, and at the same time, it is loaded in the 8 bit shift register and is output out of SBSO terminal in correspondence to a clock from EXCK terminal.

The detials of this timing will be shown in the paragraph of CPU interface.

2) Sub code Q error detection

The CRC sub code result is output from the CRCF pin in synchronism with the SCOR pin. It goes "L" when an error is detected. At the same time as the CRCQ flag is "1", the CRCF flag is output from the SUBQ pin during the time from the rising edge of the SCOR pin to the trailing edge of the SUBQ pin. This timing is detialed in **"CPU interface"**.

CIRCUIT DESCRIPTION

- **RAM interface (generation of external RAM address)**

1) Request from EFM demodulation block (Write RAM request)

When one symbol of demodulation is complete in the EFM demodulation block, the EFM demodulation block requests to write data to the external RAM to the RAM interface block. This request is WREQ signal. This block gives priority orders to requests from other blocks and processes these requests.

When EFM write request is received, an address is generated to the RAM and Write Enable state is produced. Furthermore, a data output instruction is issued against the EFM demodulation block. This instruction is OENB signal.

Clocks of PLL system are used for EFM block and for requests (WREQ) from EFM block, but clocks of X'Tal system are used for processing thereafter.

2) Request from D/A converter output circuit (Read to D/A request)

This is a de-interleaved data request issued out of the timing generator in this block. This request is of the highest priority among all requests, and addresses of three types are generated against this request.

This request is generated once every 24 periods based on the period of system clock C212 (8.4672MHz/4). The data output out of the RAM is C2 pointer first, less significant 8 bits out of 16 bits and finally more significant 8 bits.

3) Request from error correction block (C1/C2 correction, pointer R/W)

The error correction block requests the data located on the system (C1/C2) to be corrected. Furthermore, there is a request to rewrite incorrect data to correct data. In addition, there is a request for pointer R/W which indicates reliability of data.

These requests are made by the 8 bit data directed to the RAM interface block from the error correction block. The requests from the error correction unit are of the lowest priority among requests of three types. After acceptance of a request, data from RAM is directed to the 3rd clock of C212.

The data of acceptance of a request is output to the error correction block as a PREN signal. This block generates the address of the requested data, and controls R/W of the RAM at the same time.

4) Address generation

The data after EFM demodulation is data subjected to interleave processing. This interleave processing is subjected to data lag by the unit of a frame. Data of 108 frames are required for de-interleave. In other words, for obtaining one frame of audio data played in a certain length of time, data of 108 frames after EFM demodulation are required. Further, the system data of C1/C2 is of the system in the process of application of interleave, and therefore, is included in 108 frames.

Data in practice are generated continuously. That is, de-interleave should be updated by the unit of a frame. Therefore, Read/Write base counters are required. This base counter performs counting by the unit of a frame.

The writer base counter is used only at the time of EFM data writer. The address directed to the external RAM is determined by the relative lag value to EFM demodulation data and their number of frames.

5) Priority of address generation request

The system control block determines priority of address generation requests made to the RAM interface block.

The priority order is as follows beginning with higher priority.

1. Read to D/A request
2. Write to RAM request
3. C1/C2 request

The number of times of requests is as follows.

1. Requests of 12 times in the frame section
   The number of times of address generation to it is 36 times.
2. Requests of 32 times in the frame section
   The number of times of address generation to it is 32 times.
3. Maximum number of times of request (C1 Double error correction, C2 pointer copy)
   Read R/W 64 times, Pointe R/W 65 times in one frame section
   The number of times of address generation to it is 129 times.

288 C212 (clocks) are included in a frame, and the number of times of operation of the RAM in it is 197 times at maximum. In the system control block, against request 1, the timing of its occurrence is reserved in advance. Requests 2, 3 are not accepted in this timing. When requests 2, 3 are generated simultaneously, priority is given to request 2, and if a requestis generated during execution of either request, priority is given to the job in execution.

CIRCUIT DESCRIPTION

6) Jitter margin

The EFM demodulation data is synchronized with data's playback system (PLL) as described earlier. Accordingly, it includes disturbance (wow, flutter, etc.) of disc rotation servo, etc. It is loaded to the external RAM. As the data taken out of the RAM is synmchronized with the clock of X'Tal system, this RAM is subjected to time axis correction.

However, the limit of time axis correction is determined by the capacity of the RAM. In this system, other data is destroyed when read/write frames are spaced apart by ±5 frames. In such a status how the playback sound is cannot be guaranteed. The base counter monitor is provided in order to avoid it.

In other words, when the difference between read base counter and write base counter exceeds ±4 frames, the write base counter is set in the value of the read base counter. As a result, there is no case where data without error correction is output to the D/A.

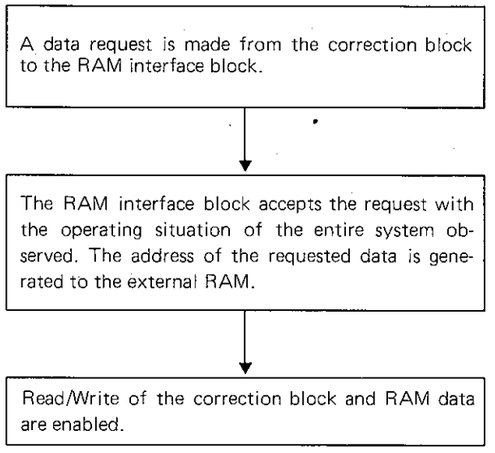
The RAOV signal is of "H" for one frame (WFCK) section when the difference between base counters exceeded ±4 frames.

- **Error correction**

1) The error correction block makes correction up to double errors with each of C1 correction and C2 correction.
2) This system adopts a unique pointer erasure method in order to minimize erroneous correction. Accordingly, the external 16k RAM stores these pointer data in addition to audio data.
3) The pointer generated in C1 correction is called C1 pointer and the pointer generated in C2 correction is called C2 pointer.
4) When the data of C1 system is judged as reliable, a C1 pointer is set in this system.
5) During C2 correction, whether correction is to be made or not to be made and whether the data is reliable or unreliable are judged from the error location, locations and number of C1 pointers obtained through computation. A C2 pointer is set against an unreliable word (16 bits).
6) The word in which a C2 pointer was set is subjected to previous value hold or mean value interpolation when it is output out of this LSI.
7) Terminal C2FL becomes "H" when one or more C1 pointers are set in the data included in the C2 system at the time of C2 correction. C2FL is reset to "L" when a period of minimum 472ns after deactivation of terminal RFCK. C2FL is the AND of C2F1 and C2F2.

Note : 472ns : One period of 2.1168MHz

8) The flow of data with the external RAM is as follows.



9) When PSSL is set at "L", a signal that is capable of monitoring error correction is output. C1F1, C1F2, C2F2 output to DA01~DA04 are these monitor signals. This signal is reset to "L" when a period of minimum 472 ns has elapsed since deactivation of RFCK.

The levels and meanings of these signals at the time of deactivaiton of RFCK are as follows.

C1F1	C1F2	C1 correction status
0	0	No Error
1	0	Single error correction
0	1	Double error correction
1	1	Irretrievable error

C2F1	C2F2	C2FL	C2 correction status
0	0	0	No Error
1	0	0	Single error correction
0	1	0	Double error correction
1	1	1	Irretrievable error

CIRCUIT DESCRIPTION

- **CLV servo control**

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP terminal for controlling synchronization of velocity and phase, MDS terminal for controlling synchronization of velocity, FSW terminal for making selection of filter constant and MON terminal for controlling motor ON/OFF.

1) STOP : Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = "L", MDS = "Z"

2) KICK : Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = "H", MDS = "Z", FSW = "L".

3) BRAKE: Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = "L", MDS = "Z", MON = "H".

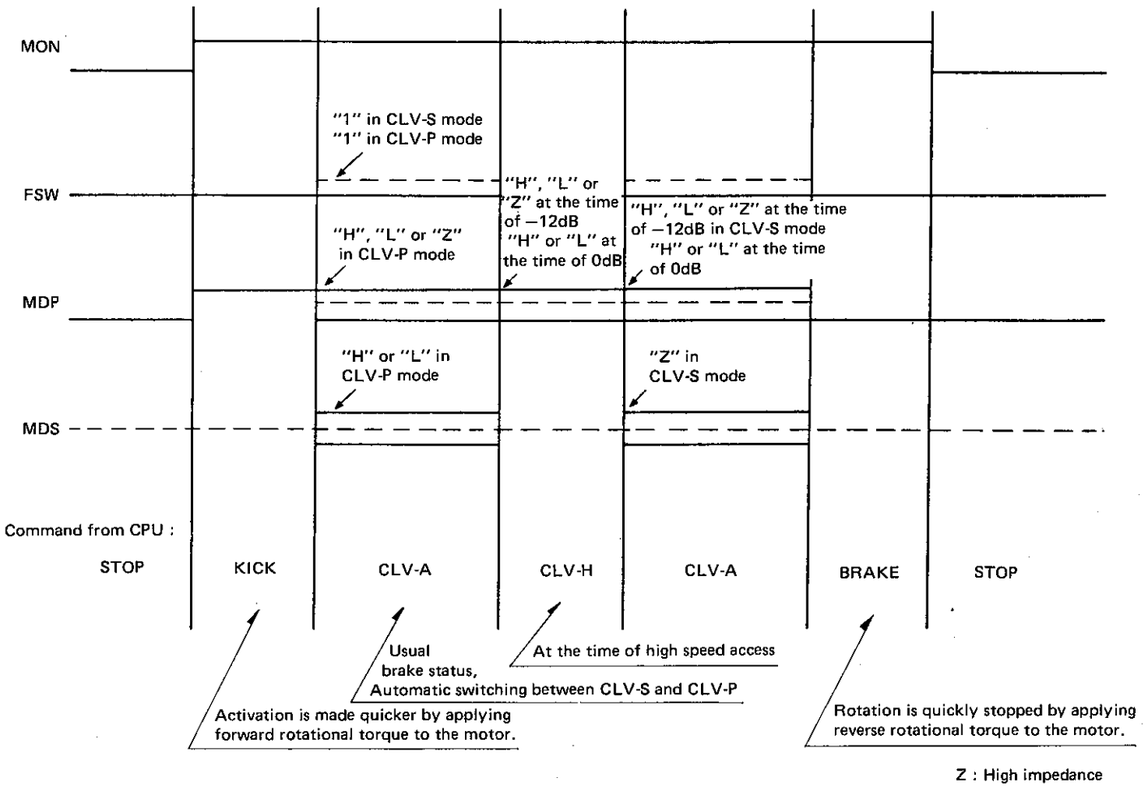


Fig. 6–8 Typical control of spindle motor

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CIRCUIT DESCRIPTION

4) CLV-S : Register E = 1100'B
Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason. When the period of VCO's oscillation frequency 8.6436MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practive, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulses are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal. "L" is produced out of MDS terminal while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more.
Either 0dB or 12dB can be selected as its gain.
MDS = "Z", FSW = "L", MON = "H".

5) CLV-P: Register E = 1111'B
PLL servo mode.
When the NCLV of register 9 is "0", the phase of the WFCK/4 signal and the phase of the RFCK/4 signal are compared and output to the MDP pin. When NCLV = "1", 1/4 of the base counter frame frequencies at the Write side and the Read side are phase-compared and output to the MDP pin. It goes "H" when WFCK is slow, "L" when it is fast, and is "Z" when synchronized. If the 8.4672/2MHz period is T, and the time when WFCK is "H" is tHW, then the MDS pin outputs a signal which goes "H" during the time from the trailing edge of WFCK to the time represented by (tHW−279T) X 32, and then goes "L" until the next trailing edge of WFCK.
MDS $\leqq$ "H" when tHW = 279T,
MDS = "L" when tHW $\geqq$ 279T.
The MDS pin varies between 32T and 544T, in 32T steps, when 280T $\leqq$ tHW $\leqq$ 296T. For example, when synchronized (rotating at the standard speed), that is when tHW = 288T, a 7.35kHz signal, with a duty cycle of 50% is output.
FSW = "Z", MON = "H".

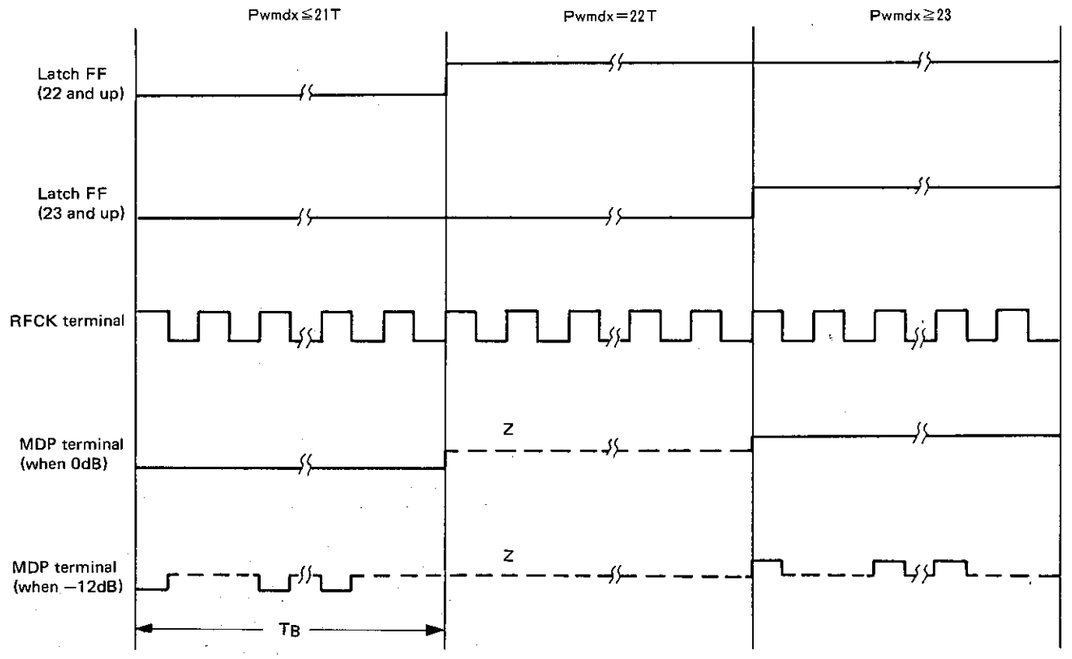


Fig. 6–9 Timing chart in CLV-S, CLV-H mode (1)

CIRCUIT DESCRIPTION

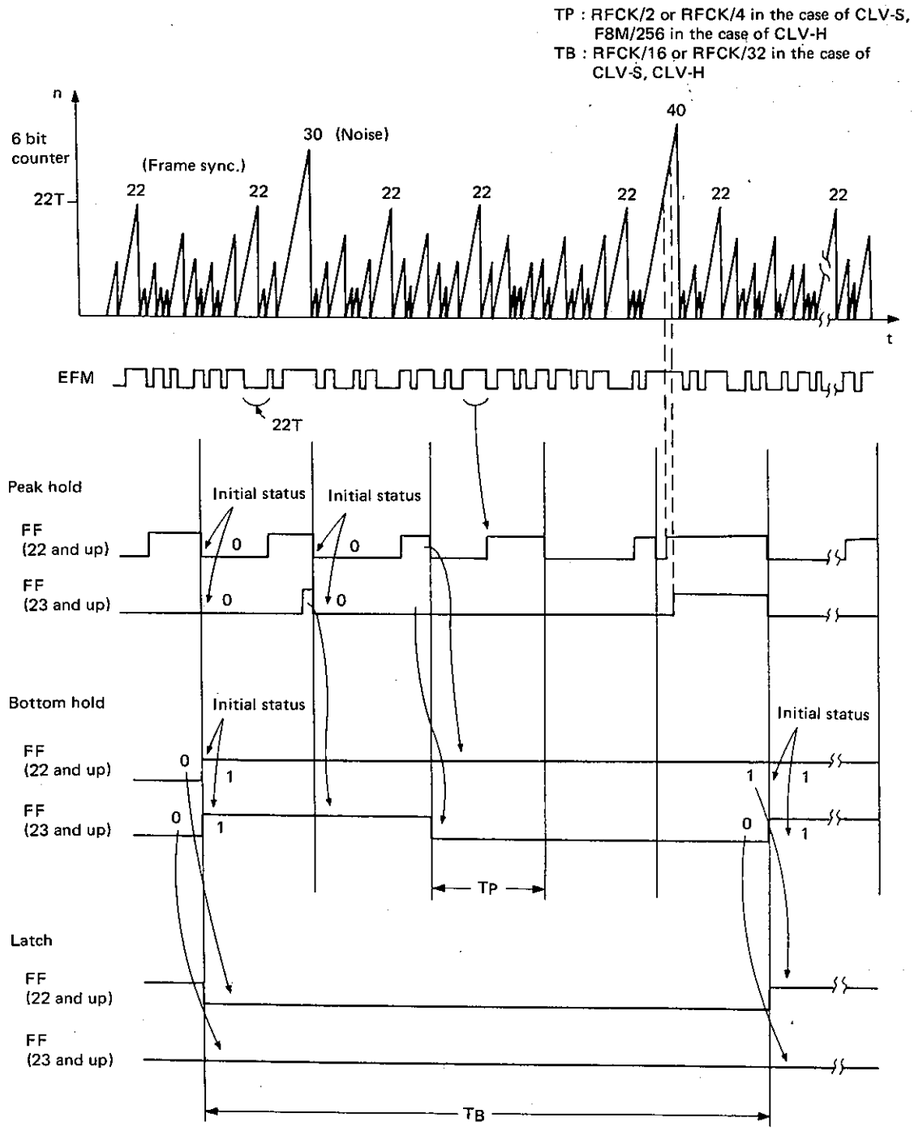


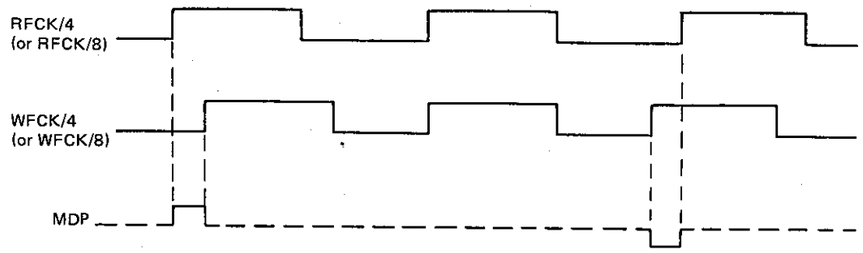
Fig. 6—10 Timing chart in CLV-S, CLV-H mode (2)

CIRCUIT DESCRIPTION

6) CLV-P : Register E = 1111'B
PLL servo mode.
Phase comparison of signals WFCK/4 and RFCK/4 or WFCK/8 and RFCK/8 is made, and output is made out of MDP terminal. "H" when WFCK has delayed, "L" when WFCK is fast, and "Z" when synchronized. When the period of 8.4672/2MHz is expressed at T and the length of time when WFCK is "H" is expressed at tHW, such a signal that is of "H" during (tHW—279T)

x 32 with 7.35kHz as a period and that is "L" during the remaining time is produced out of MDS terminal. MDS = "L" when tHW ≦ 279T. MDS = "H" when tHW ≦ 297T. When 280T ≦ tHW ≦ 296T, the MDS terminal changes in 32T steps from 32T to 544T. When synchronized, for instance, that is, when tHW = 288T, a signal of 7.35kHz of DUTY 50% is produced. FSW = "Z", MON = "H".

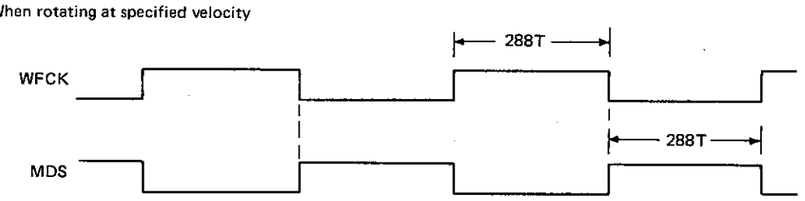
MDP terminal



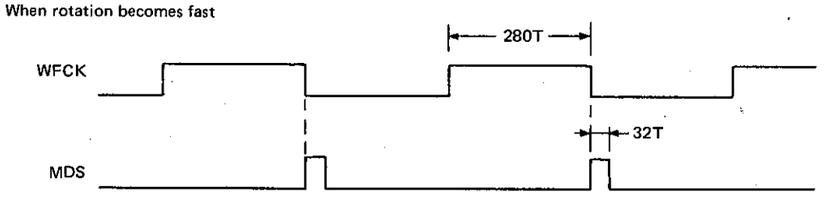
Z : High impedance

MDS terminal (The Period of 4.2336MHz is expressed as "T".)

(1) When rotating at specified velocity



(2) When rotation becomes fast



(3) When rotation becomes slow

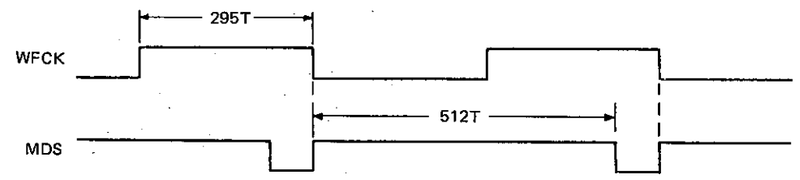


Fig. 6—11 Timing chart in CLV-P mode

CIRCUIT DESCRIPTION

7) CLV-A: Register E = 0110'B
The mode used for normal play status.
The GFS signal ("H" when locked, "L" when unlocked), after frame sync detection, protection and insertion block, is sampled at WFCK/16, and functions in CLV-P mode when the signal is "H". When the "L" signal continues for 8 times, the mode is automatically changed to CLV-S mode. When in the CLV-S mode, setting of the peak hold period, and setting of the period and gain of the bottom hold of the CLV-S and CLV-H are performed in register D, and the selection of each mode is perfomred in register E. The description of these registers are detialed in **"CPU interface"**.
Note: When PSSL = "L", DA07 pin outputs WFCK/4 or WFCK/8 as FCKV, and DA08 outputs EFCK/4 or EFCK/8 as FCKX.

8) CLV-A' : Register E = 0101'B
New auto servo mode added to the CX23035. The difference between CLV-A. and CLV-A is in the rough servo system. With the old rough servo system, the EFM pattern is measured by a crystal and the servo is applied so that the width of the sync pattern is a fixed value, and the rotation speed of the spindle motor is roughly fixed. In this case, if the value is out of the VCO capture range, the VCO never locks with the EFM. With the new rough servo system, a VCO is used for measurement instead of a crystal. If the VCO center is shifted from true center the VCO tends to lock, since the rotation of the spindle motor varies in the same direction.
The new rough servo functions only in CLV-A' mode. The rough servo in CLV-A mode and CLV-S mode is the old rough servo.

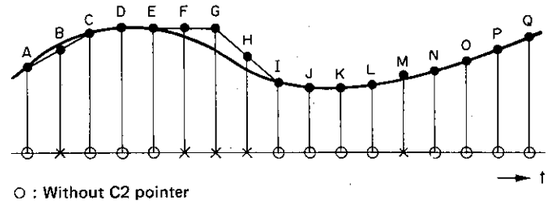
CIRCUIT DESCRIPTION

• Interpolation and D/A converter interface

1) Interpolation circuit block

3 byte data can be obtained with a Read to D/A request. They are C2 pointer, less significant 8 bits and more significant 8 bits. The total 16 bits constitute the data generated per sampling (2's complement.)

The C2 pointer expresses the reliability of this 16 bit data. Therefore, data with C2 pointer is subject to interpolation in this block.



O : Without C2 pointer
X : With C2 pointer

Fig. 6–12

Mean value interpolation

$$B=\frac{1}{2}(A+C)$$

$$H=\frac{1}{2}(E+I)$$: When pointers are continuous

$$M=\frac{1}{2}(L+N)$$

Previous value hold

$$F=G=E$$

16 bit data is alternately output to L-ch and R-ch, R-ch data is output in the section in which LRCK is "L" and L-ch data is output in the section in which LRCK is "H". C2PO signal outputs C2 pointer to the 16 bit data directed to DA01–DA16 (PSSL = H), DA16 (PSSL = L). In other words, it means that the 16 bit data that is output when C2PO is "H" is interpolated data.

2) Explanation of muting and attenuator

In the muting block it is possible to mute (– ∞ dB) or attenuate (–12dB) the audio signal in accordance with the MUTG terminal and ATTM signal of the CPU interface block.

ATTM	MUTG	Attenuation value	Remarks
0	0	0dB	
1	0	–12dB	
0	1	– ∞ dB	See Note
1	1	–12dB	See Note

NOTE : When the MUTG is set to "H" level with the NCLV flag set to "0", the read base counter value is continuously loaded into the write base counter as well as the muting.
Except at CLV-A, CLV-P, CLV-S, or CLV-A' with the NCLV flag set to "1", the base counter is loaded.

CIRCUIT DESCRIPTION

- **Mode setting**

The various kinds of mode can be set by combining the following pins. (Refer to the table below.)

MD1 pin : Mainly for selection of the oscillator clock at the XTAI or XTAO pin.

MD2 pin : Mainly for selection of the digital out function.

MD3 pin : Mainly for selection of the digital filter function.

PSSL pin : Mainly for selection between serial and parallel output.

SLOB pin : Selection between offset binary and 2's complement.

Input terminal					Function						Compatible IC	
MD1	MD2	MD3	PSSL	SLOB	8M/16M	DO OFF/ON	DF OFF/ON	P/S	OB/2's	CD ROM/AUDIO (Note)	CXD1125	CXD1130
L	L	L	L	L	16M	DO ON	DF ON	Seri	2's	AUDIO		
L	L	L	H	H	↓	↓	↓	Para	OB	↓		
L	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	
L	H	L	L	L	↓	DO OFF	DF ON	↓	↓	↓		○
L	H	L	H	H	↓	↓	↓	Para	OB	↓		○
L	H	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
L	H	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	L	L	L	L	8M	↓	DF ON	Seri	2's	↓		○
H	L	L	H	H	↓	↓	↓	Para	OB	↓		○
H	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
H	L	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	H	H	L	L	16M	DO ON	↓	Seri	2's	CD ROM	○	
H	H	H	H	L	8M	DO OFF	↓	↓	↓	↓	○	○

(Note)

- 8M/16M : Selection of clock, XTAL or XTAO. 8.4672MHz/16.9344MHz
- DO OFF/ON : Digital out OFF/ON
- DF OFF/ON : Digital filter OFF/ON
- P/S : Parallel output/serial output
- OB/2's : Offset binary/2's complement
- CD ROM/AUDIO : Compatible to CD ROM/Compatible to audio

1) Selection of clock

The oscillator clock for XTAI and XTAO is available at 16.9344MHz and 8.4672MHz. However, when digital out is used, the clock must be set to 16.9344MHz.

2) Selection of digital out (Refer to "D/A interface")

When digital out is set to ON, a signal conforming to the D/A interface format is output from the DOTX pin. When it is set to OFF, the DCTX pin outputs the WFCK signal. In the DP-969, this function is fixed to ON.

3) Selection of digital filter

When the digital filter function is set to ON, the DAC interface signal are all set to double speed.

4) Selection of parallel output/serial output

When the parallel output is selected, DA01 to DA16 pins output the 16-bit parallel data. When the serial output is selected, DA01 to DA16 pin output the following signals respectively.

DA01 → C1F1 : } Error correction status monitor
DA02 → C1F2 : } output at C1 decode.
DA03 → C2F1 : } Error correction status monitor
DA04 → C2F2 : } output at C2 decode.
DA05 → C2FL : Correction status output, C2FL = C2F1·C2F2.

DA06 → C2PO : C2 pointer signal.
DA07 → RFCK : Read frame clock signal, 7.35kHz when locked to the crystal line.
DA08 → WFCK : Write frame clock signal, 7.35kHz when locked.
DA09 → $\overline{\text{PLCK}}$: 1/2 of the divided signal from the VCO pin, 4.3218MHz when locked.
DA10 → UGFS : Non-protect frame sync signal.
DA11 → GTOP : Frame sync protect status display signal.
DA12 → RAOV : Jitter margin over or underflow display signal.
DA13 → C4LR : 4 times the LRCK signal.
DA14 → $\overline{\text{C21O}}$: Bit clock (invert signal of C21O).
DA15 → C21O : Internal system clock (4.2336MHz when DF is ON, 2.1168MHz when CXD1125Q or DF is OFF).
DA16 → DATA : Serial data output (MSB or LSB first output).

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CIRCUIT DESCRIPTION

5) Selection of OFFSET BINARY/2'S COMPLEMENT

When the SLOB pin is "H", an offset binary signal is output, and when it is "L", a 2's complement signal is output.

6) Selection of CD ROM/AUDIO compatibility

When MD1 = MD2 = MD3 = "H", the player is compatible with a CD ROM and outputs the C2 pointer for each byte. At the same time, the average value interpolation and the previous value holding operations are not performed. For example, when there is an error in the upper 8 bits of the 16 bits, only the C2 pointer corresponding to the upper 8 bits goes "H", and the lower 8 bits are processed as the correct data.

- **D/A Interface**

The player incorporates a D/A interface output (digital output) and the digital signal is output from the DOTX pin. The digital signal is output after passing through interpolation, mute and attenuator circuits. The 4 control bits (ID0, ID1, COPY, EMPHASIS) in the C-bit channel status perform a CRC check and are revised only when it's OK.

- **Countermeasures to defect**

To counter a defect, the PDC pin is set to "Hi-Z" during the time until GFS goes "H" again after inverting from "H" to "L" or after approx. 0.55ms has elapsed. However, this operation is performed only when the HZPD flag of register 9 is "1". When HZPD = "0", it will never be set to "Hi-Z".

The signal switching between the rough servo in the CLV-A or CLV-A' mode and the PLL servo is output from the LOCK pin. After the GFS signal is sampled at WFCK/16, and when the signal is "1", the LOCK pin goes "H", when a "0" is present 8 times in a row, the LOCK pin goes "L".

This operation is similar to that for the FSW pin. However, while the FSW outputs a fixed signal when not in CLV-A' mode, the LOCK pin always output the above signal.

- **Timing chart**

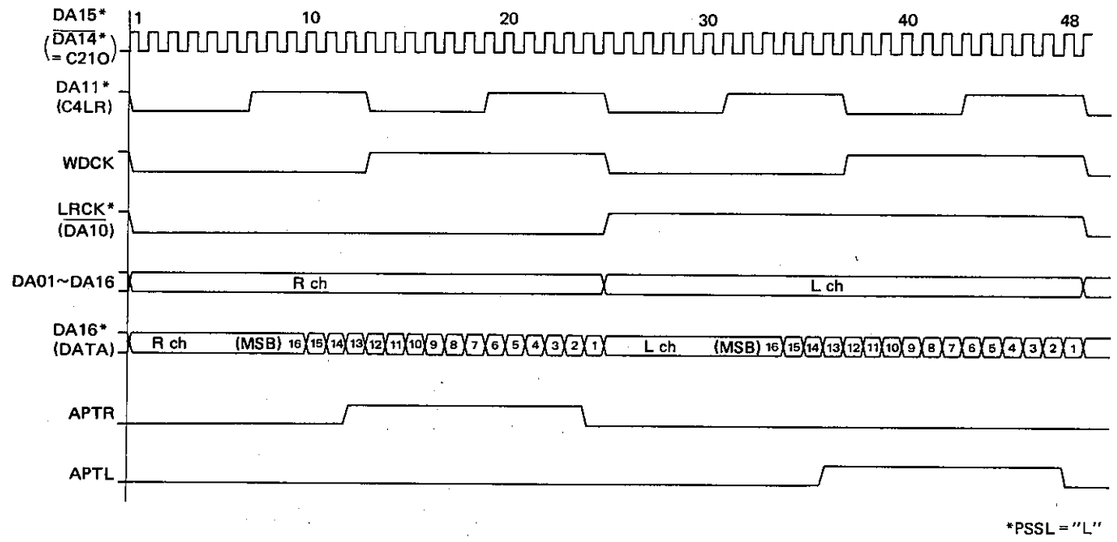
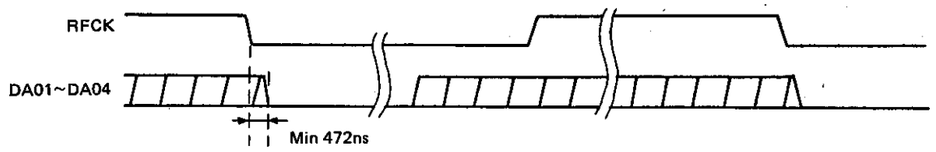
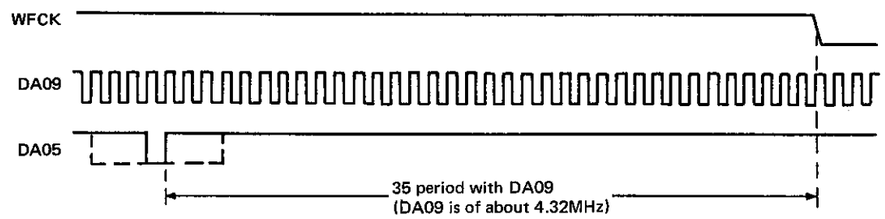


Fig. 6–13 Timing chart of audio output

CIRCUIT DESCRIPTION



* DA01~DA04 (C1F1, C1F2, C2F1, C2F2) are cleared when a period of minimum 472 ns has elapsed since RFCK was deactivated.
* ANDing signal of C2F1 and C2F2 is output out of C2FL termnal.



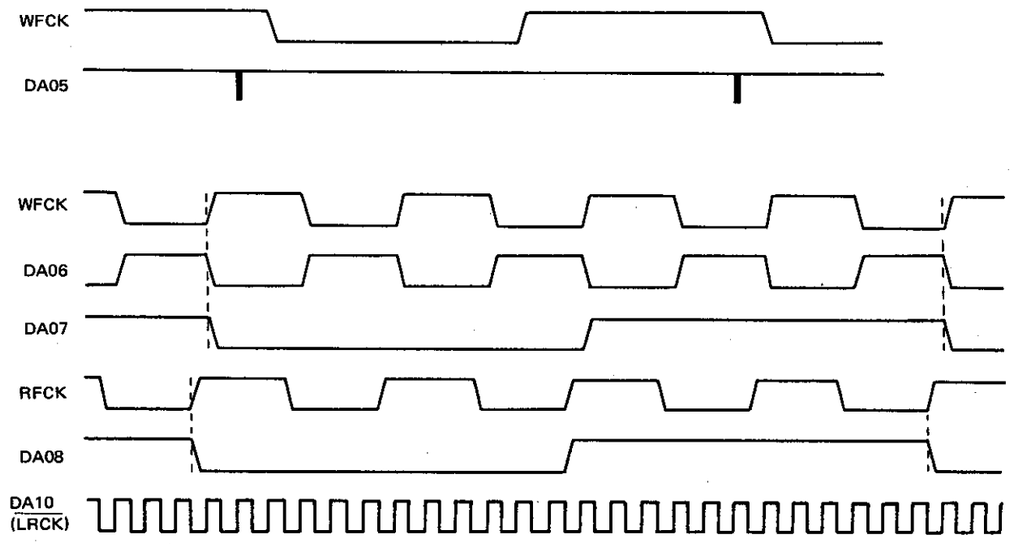


Fig. 6–14 Timing chart of DA01~DA16 output when PSSL = "L"

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CIRCUIT DESCRIPTION

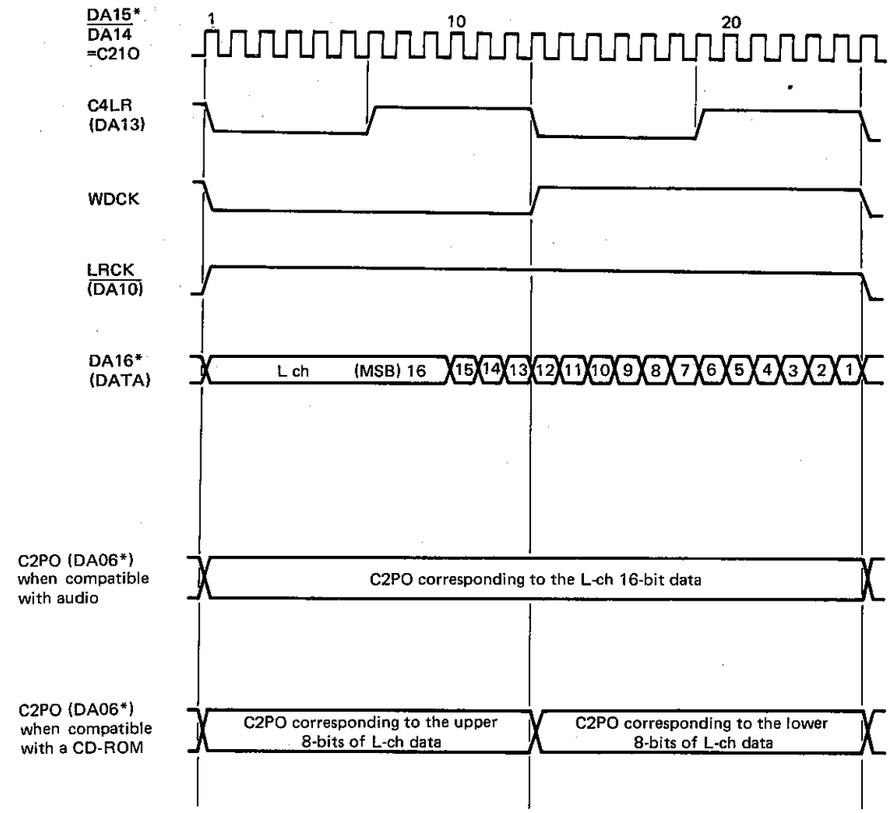

Fig. 6–15 Timing chart of C2PO output (when PSSL = "L")

* RAOV becomes "H" for one frame (synchronized with WFCK) when a jitter that exceeds ±4 frames is generated between RFCK and WFCK.

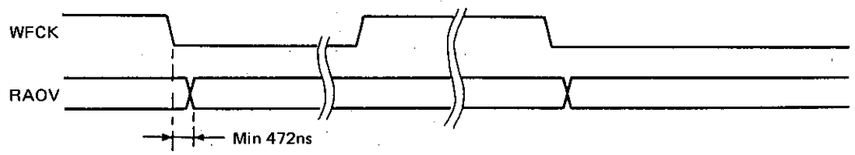

Fig. 6–16 Timing chart of RAOV output

MECHANISM OPERATION DESCRIPTION

Mechanism operation description

Fig. 1 shows the mechanism positioning in the STOP mode. The OPEN/CLOSE operation when loading the disc is described below.

Note :

In the operation description, the black and white arrows shows the following code :

Black arrow : Shows the opening direction of the tray (Tray OPEN).

White arrow : Shows the closing direction of the tray (Tray CLOSE).

Also in the operation description and illustrations, numbers in brackets ( ) followed by the part name show the identifying numbers of the disassembly diagram in the Service Manual.

1. OPEN/CLOSE operation

The center of the OPEN/CLOSE lug detection leaf switch installed on the PC board (J25-4904-02(A/3)) on the rear of the mechanism is pressed to the right by lower side of the tip of the black switch arm (6) installed on the slider ass'y (11) when the tray is closed, and the information is transferred to the microprocessor. This status is called the tray CLOSE operation. The operation from this status to the condition when the tray is completely opened by pressing the OPEN/CLOSE key is described.

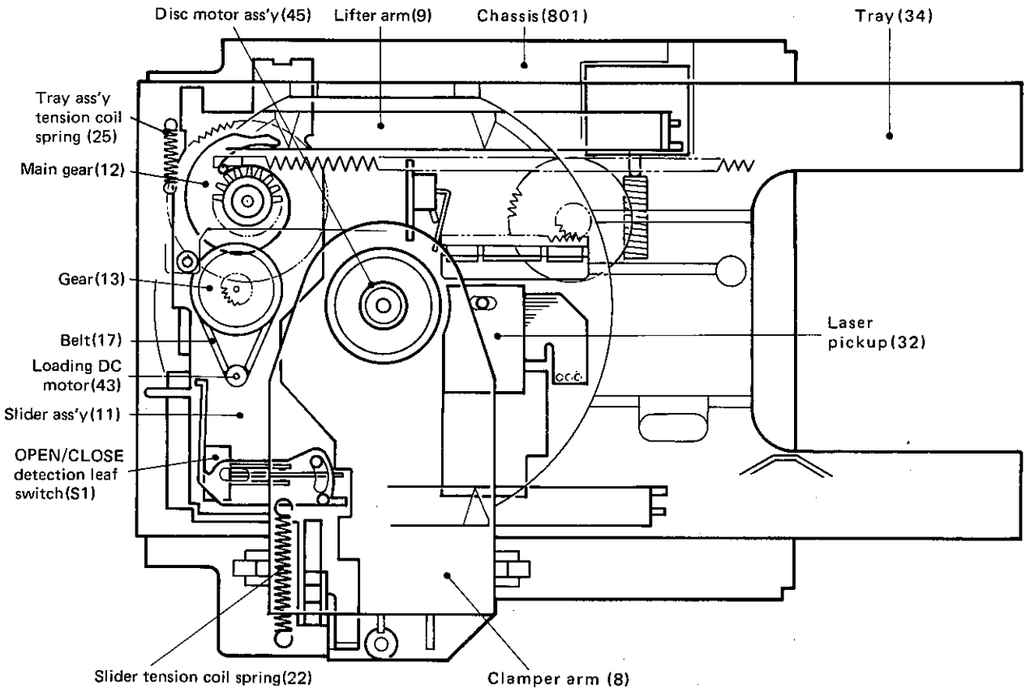

Fig. 1 Tray closed status

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MECHANISM OPERATION DESCRIPTION

As shown in Fig. 2, loading DC motor (43) rotates in the direction of the black arrow ❶ and transfers the rotation of the black arrow ❷ to the gear (13) via the belt (17), and also rotates the main gear (12) in the direction of the black arrow ❸ with the lower gear section of the gear (13). The main gear (12) contains the cam on its upper surface. Along with the surface of the cam, protrusion A located in the lower side of the slider ass'y (11) is shifted and the slider ass'y (11) begins to move in the direction of the black arrow ❹ .

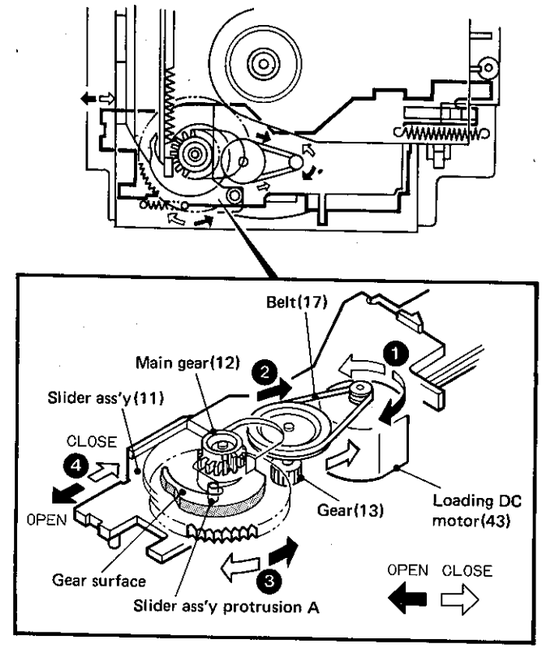

Fig. 2 Loading motor rotation transmission

Fig. 3 shows the movement of protrusion A of the slider ass'y(11) in the direction of the black arrow ❹ until the tray is completely opened.

The slider ass'y(11) releases the OPEN/CLOSE detection leaf switch(S1) from the CLOSE condition and pulls the foot section of the clamper arm(8) in the direction of the black arrow ❹ by the groove section of the slider ass'y(11). By this, the clamper arm(8) is lifted in the direction of the black arrow ❻ with a support as a center to the disc release condition from the disc clamping condition.

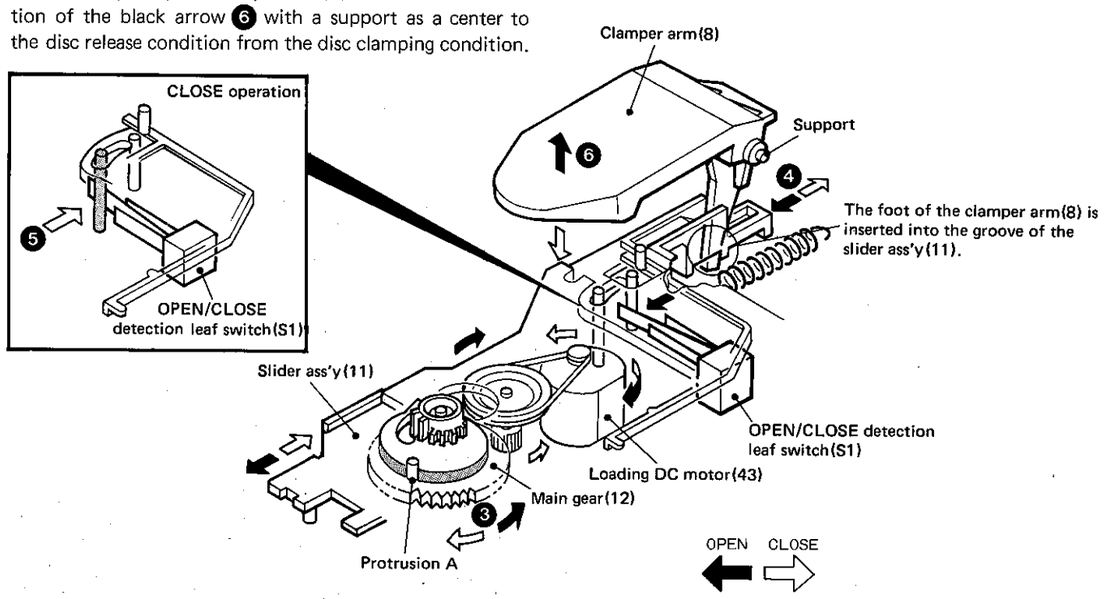

Fig. 3 Clamper arm operation

MECHANISM OPERATION DESCRIPTION

Fig. 4 shows the condition when the tray is completely opened. The tray is "sloped" as shown in the figure. When the tray moves in the direction of the black arrow ❺ OPEN direction, the white protrusion climbs the "slope" to short the OPEN/CLOSE detection leaf switch(S1) in the reverse direction of the STOP condition, then informs the microprocessor that the OPEN operation has completed and to stop the rotation of the loading DC motor(43).

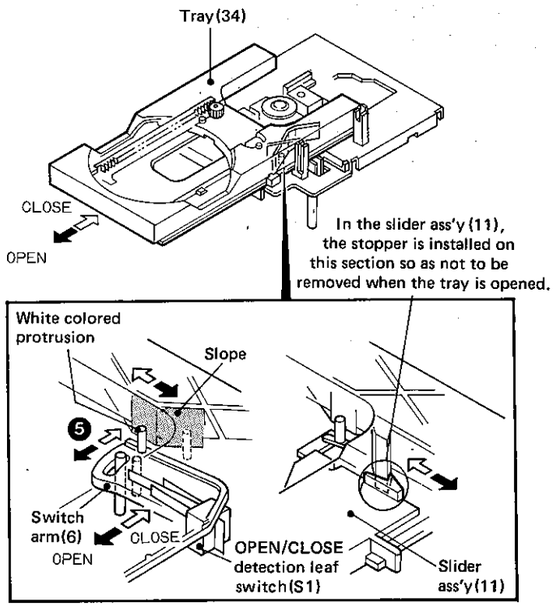

Fig. 4 Each limit switch when opening/closing the tray

Fig. 5 shows the OPEN operation until the disc is lifted from the turntable and placed on the disc tray so that the disc is removed from the player. These operations are performed almost at the same time as the up operations of the clamper arm(8) when the tray is opened as described in Fig. 2 to 4 above.

The tray(34) incorporates the lifter arm(9) which is required to support the disc when the tray is opened/closed and the lifter slider(10) which drives the lifter.

When the tray is opened, the slider ass'y(11) is shifted in the direction of the black arrow ❹. In the slider ass'y, lug a is installed to slide the lifter slider horizontally (toward the left and right). And the lifter slider(10) is always pulled in the direction of the black arrow ❼ by the tray ass'y tension coil spring(25).

For this, when the slider ass'y(11) is moved to the OPEN direction (in the direction of the black arrow ❹), the lifter slider(10) is also shifted to the left by the lug a. The lifter slider(10) has grooves on its left and right ends to lift the lifter arm up/down.

In the OPEN operation, when the lifter slider(10) is moved in the direction of the black arrow ❼, protrusion B of the lifter arm(9) is slide in the groove using the support as a center, and the lifter arm is lifted in the direction of the black arrow ❽.

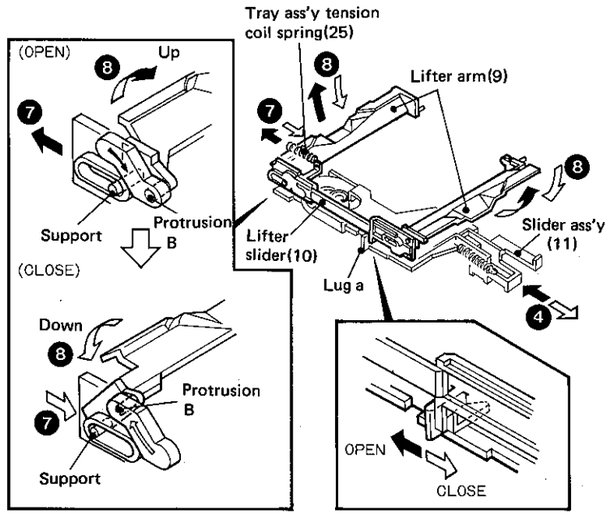

Fig. 5 Lifter arm up/down operation

MECHANISM OPERATION DESCRIPTION

Fig. 6 shows the operation of the main gear(12) which actually performs the OPEN/CLOSE operation of the tray described above.

In the upper surface of the main gear(12), there's a gear to open or close the tray. Among the gear teeth, only two teeth are longer than the other, for triggering the OPEN operation.

First these longer teeth trigger the OPEN operation, then the whole gear engages the gear rack of the surface of the tray to initiate the OPEN operation.

At this time, protrusion A installed on the lower side of the slider ass'y(11) is located at the position where the main gear(12) is rotated approx. 360 degree from the STOP position. At this position, when the triggering gear and the gear rack of the tray are engaged to initiate the OPEN operation, protrusion A will drop to the STOP position again from the convex of the main gear(12) cam surface. To prevent this, the white colored roller installed on the slider ass'y(11) releases protrusion A from the cam surface of the main gear(12), so as not to contact with the cam surface while the main gear(12) is engaged with the gear rack on the back of the tray in OPEN/CLOSE operation.

Since this roller is always pulled in the right direction (viewd from the front) by the slider tension coil spring(22) and the arm pressure coil spring(24), it slides while pressing the guide surface on the back of the tray in the right direction in the tray OPEN/CLOSE operation.

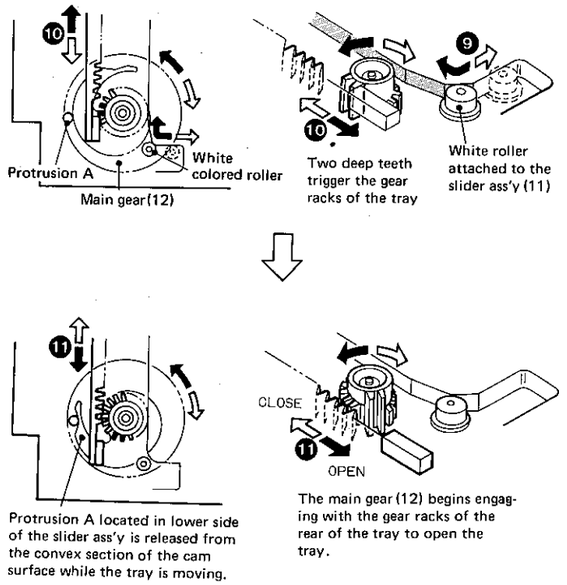

Fig. 6 Gear (12) operations

2. Disassembling procedure of mechanism section

2–1. Removing the clamper arm

1) While lightly pressing the clamper arm from the top ❶, remove the fixing lugs on both sides in the direction of arrows ❷ and ❸.
2) Remove the clamper arm in the direction of arrow ❹.

Note : Be sure to remove the fixing lugs on both sides of the clamper arm while pressing the clamper arm in the direction of arrow ❶. Since the lugs are solid, if forcibly performed, they might be broken.

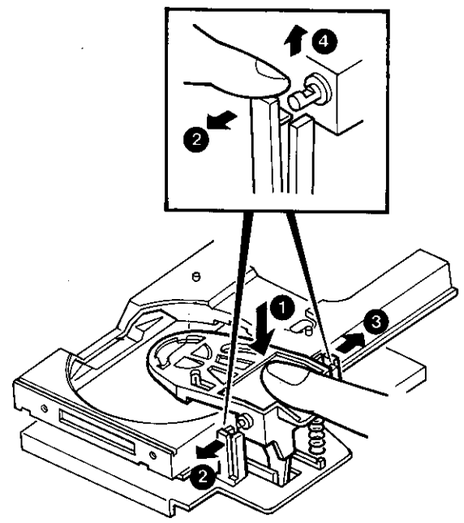

Fig. 1 Removing the clamper arm

MECHANISM OPERATION DESCRIPTION

2–2. Attaching the clamper arm

1) Insert the foot section of the clamper arm into the groove of the slider ass'y (❺).
2) At this time confrim that portrusion A of the clamper arm is inserted into the center of the arm pressure coil spring.
3) Put the support of the clamper arm to the lug section of the outsert of the mechanism by pressing from the top (❻).

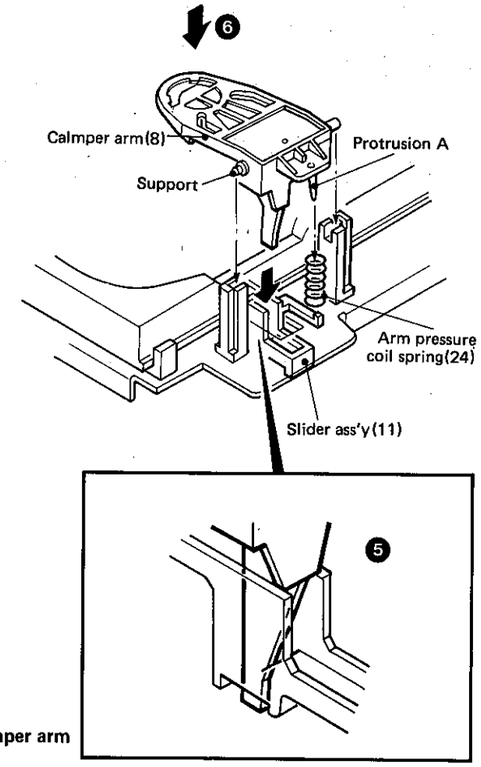

Fig. 2 Attaching the clamper arm

2–3. Removing the tray

1) While pressing the hook section of the slider ass'y in the direction of arrow ❼ , pull out the tray in the direction of arrow ❽ to remove it (❾).

Note : Be sure not to release your finger when pressing the hook. If the hook is released, the stopper on the upper surface of the slider ass'y will come in contact with the stopper of the tray and the tray will not be removed.

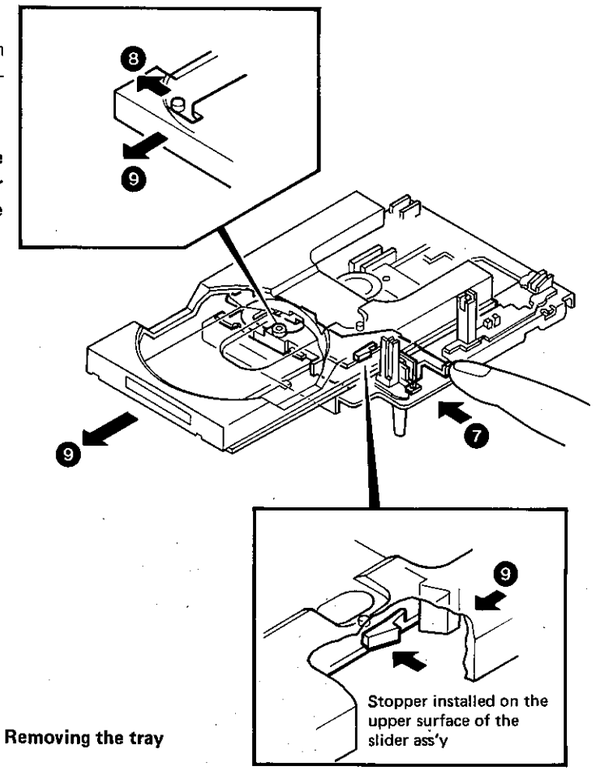

Fig. 3 Removing the tray

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MECHANISM OPERATION DESCRIPTION

2–4. Attaching the tray

1) Attach the collars firmly on both sides of the tray to the four section supporting and guiding the tray as shown in the Fig. 4.
   First attach the front two section then attach the rear two sections as shown in ❿.

Note : The gear offset of the mechanism after removing/ attaching the tray will be reset automatically by performing the OPEN/CLOSE operation

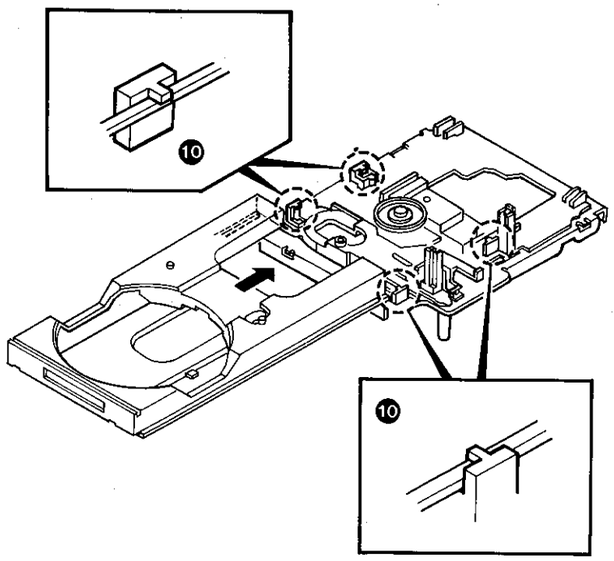


Fig. 4 Attaching the tray

2–5. Removing the slider ass'y

1) Removing the slider tension coil spring attached to the slider ass'y (⓫).
2) Slide the slider ass'y in the direction of arrow ⓬ until it reaches the position where it can be removed from the outsert section supporting the slider ass'y.
3) Remove the slider ass'y by pulling out right above in the direction of arrow ⓭ .

Note : If the slider ass'y is removed askew, the OPEN/ CLOSE detection leaf switch on the back of the tray might be bent down.

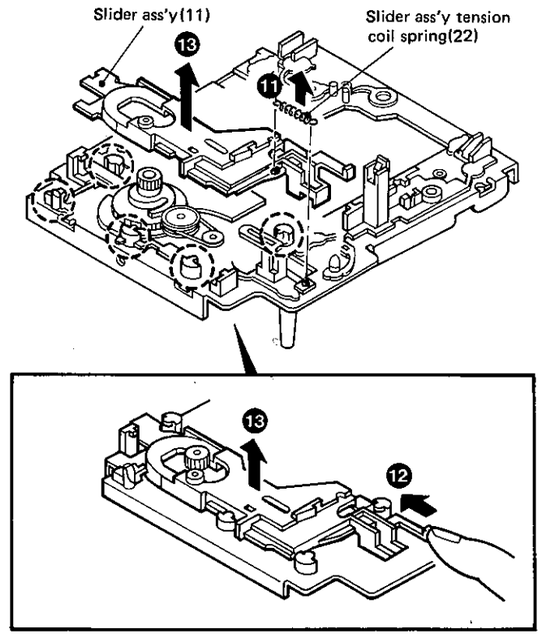


Fig. 5 Removing the slider ass'y

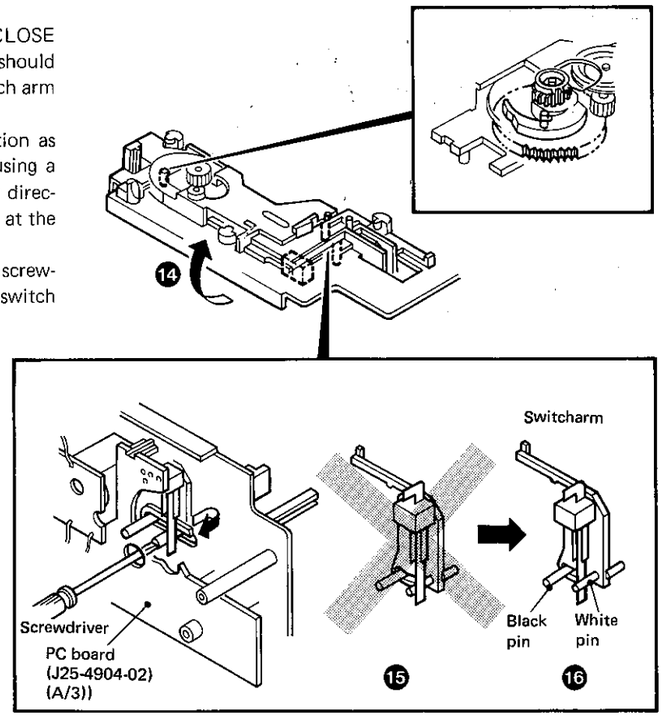
MECHANISM OPERATION DESCRIPTION

2–6. Attaching the slider ass'y

The long metal piece at the center of the OPEN/CLOSE detection leaf switch on the rear of the mechanism should be set between the white and black pins of the switch arm installed on the rear of the slider ass'y.

If it is inserted simply, it will be set the position as shown in ⑮. At this time, correct the position using a screwdriver by lifting the slider ass'y slightly in the direction ⑭ so that the white pin of the switch arm is set at the position as shown in ⑯.

A round hole is on the PC board for inserting the screwdriver. This is used for correcting/checking the switch position when working.



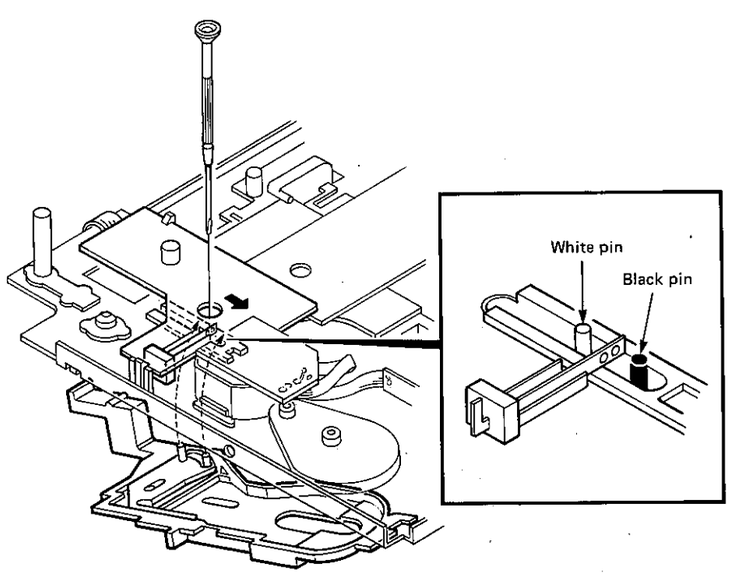


Fig. 6 Attaching the slider ass'y

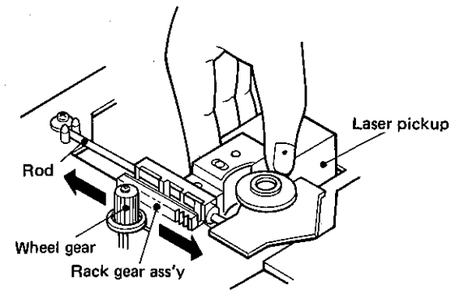
MECHANISM OPERATION DESCRIPTION

2–7. When moving the pickup forcibly

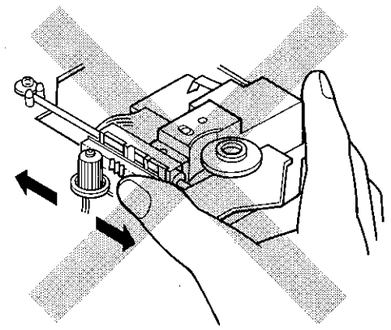
Do not move the rack gear ass'y by hand as shown in Fig. (B). The clearance between the wheel gear and the rack gear ass'y might be changed if bent.

When moving the pickup on repair, hold the main body of the pickup with the section as close to the rod as possible, then move it forcibly. (Fig. A).

Note : Do not move the pickup forcibly unless required.



(A)



(B)

Fig. 7 Pickup gear movement

ADJUSTMENT

No.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG
1	LASER POWER	–	Apply the senser section of the optical power meter onto the pickup lens.	Short-circuit pins 8 and 9 and turn power on to enter the Test mode. Press the +10 key, the tray opens and the LD emits light.	VR1 ALPC circuit VR installed on the pickup (X29-1760-00)	0.1mW	(a)
2	LASER PICKUP OPERATING CURRENT (Only when the pickup seems defective.)	–	Remove pin 1 of CN1 and connect the DC ammeter. (X29-1760-00)	Short-circuit pins 8 and 9 and turn power on to enter the Test mode. Press the +10 key, the tray opens and the LD emits light.	–	+5.5mA current value labeld on the laser pickup. If current is 40mA or more over the above value, it's defective.	(b)
3	FOCUS ERROR BALANCE	Test disc	Connect an oscilloscope to TP(RF). (X25-2932-71)	PLAY	FE BALANCE VR3 (X25-2932-71)	Optimum eye pattern	(c)
4	TANGENTIAL	Test disc	Connect an oscilloscope to TP(RF). (X25-2932-71)	PLAY	Screw on right side of mechanism (Fig.A)	Optimum eye pattern	(c)
5	DIFFRACTION GRATING (1)	Test disc	Connect an oscilloscope to TP(RE). (X25-2932-71)	Turn power on while short-circuiting pins 8 and 9 to put the microcomputer to the test mode. Press the PLAY key to search the Track No.1 for 1 to 2 minutes. Then press the CHECK key to set the tracking servo to OFF.	Adjusting hole in the lower side of the laser pickup (Fig.B)	Maximum amplitude (See Photos 1 and 2.)	(d)
6	DIFFRACTION GRATING (2) " Polarity check "	Test disc	Connect an oscilloscope to TP(RF). (X25-2932-71)	With the microcomputer in the test mode, press the CLEAR key to set the tracking servo to ON. (Feed servo is set to OFF.)	Adjusting hole in the lower side of the laser pickup (Fig.B)	Confirm that the eye pattern is presented correctly.	(c)
7	DIFFRACTION GRATING (3) " Check that the sub-beams are spotted on the same track "	Test disc	Trigger at TP(RF) and connect an oscilloscope to TP(SUB). (X25-2932-71)	PLAY	Adjusting hole in the lower side of the laser pickup (Fig.B)	Check that they are as Photo 3. *Photo 4 shows the defective example.	(e)
8	TRACKING ERROR BALANCE	Test disc	Connect an oscilloscope to TP(TE) or DC voltmeter. (X25-2932-71)	In the test mode, press the CHECK key to set the tracking servo to OFF.	TE.BALANCE VR2 (X25-2932-71)	Symmetry between upper and lower patterns, or DC=0 ±0.05V	(d)

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ADJUSTMENT

No.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG
9	FOCUS GAIN	Test disc: Apply 1kHz, 0.5Vrms to CN7 pin 2 of X25-2932-71	Connect LPF with 47kΩ, 470pF to CN7 pin 1 of X25-2932-71, and connect an oscilloscope or AC voltmeter.	PLAY	FOCUS GAIN VR4 (X25-2932-71)	50mVrms *It is 1/10 of input voltage (When the oscilloscope is used, check the 1kHz signal component only.)	(f)
10	TRACKING GAIN	Test disc: Apply 1kHz, 0.5Vrms to CN7 pin 4 of X25-2932-71	Connect LPF with 47kΩ, 470pF to pin 5 of X25-2932-71, and connect an oscilloscope or AC voltmeter.	PLAY	TRACKING GAIN VR5 (X25-2932-71)	50mVrms *It is 1/10 of input voltage (When the oscilloscope is used, check the 1kHz signal component only.)	(f)
11	PLL		Connect a frequency counter to TP(PLCK). (X25-2932-71)	STOP Short-circuit the PLCK and F.TEST terminals.	F.ADJ. VR1 (X25-2932-71)	FREQUENCY ADJ. 4.4MHz±0.15MHz.	(g)

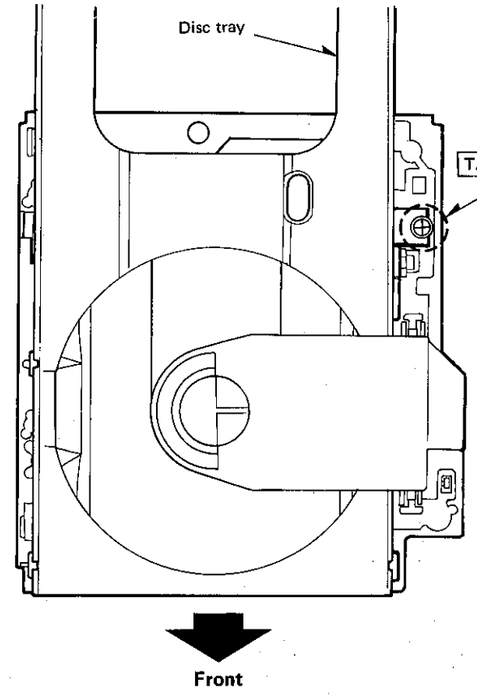

Fig. A : Mechanism ass'y (Top view)

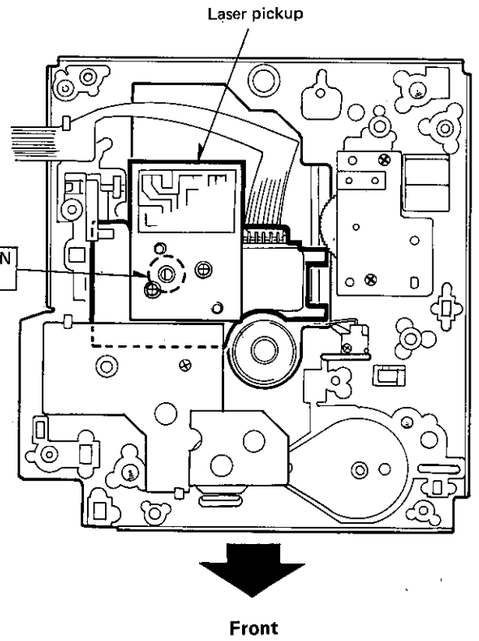

Fig. B : Mechanism ass'y (Bottom view)

REGLAGE

N°	ITEM	REGLAGE D'ENTREE	REGLAGE DE SORTIE	REGLAGE DE LA LECTURE	POINT D'ALIGNEMENT	ALIGNEMENT POUR	FIG
1	PUISSANCE LASER	–	Appliquer la section détecteur du compteur de puissance optique sur la lentille du capteur.	Court-circuiter les broches 8 et 9 et mettre sous tension pour passer dans le mode d'essai. Appuyer sur la touche +10, le plateau s'ouvre et le LD émet de la lumière.	VR1 VR de circuit ALPC installé sur le capteur (X29-1760-00)	0.1mW	(a)
2	Courant de fonctionnement du capteur laser (Uniquement quand le capteur semble défectif.)	–	Retirer la broche 1 de CN1 et reccorder l'ampèremèter CC. (X29-1760-00)	Court-circuiter les broches 8 et 9 et mettre sous tension pour passer dans le mode d'essai. Appuyer sur la touche +10, le plateau s'ouvre et le LD émet de la lumière.	–	+5,5mA de valeur de courant indiquée sur le capteur laser. Si le courant est de 40mA ou bien supérieur à la valeur ci-dessus, il est défectif.	(b)
3	BALANCE D'ERREUR DE MISE AU POINT	Disque test	Raccorder un oscillcscope à TP(RF). (X25-2932-71)	PLAY	FE BALANCE VR3 (X25-2932-71)	Forme optimum	(c)
4	TANGENTIEL	Disque test	Raccorder un oscillcscope à TP(RF). (X25-2932-71)	PLAY	Vis sur le côté droite du mécanisme (Fig.A)	Forme optimum	(c)
5	RESEAU DE DIFFRACTION (1)	Disque test	Raccorder un oscilloscope à TP(TE). (X25-2932-71)	Fournir l'alimentation tout en court-circuitant les broches 8 et 9 pour mettre le micro-ordinateur en mode de test. Presser la touche PLAY pour rechercher la piste n° 1 pendant 1 à 2 minutes. Presser ensuite la touche CHECK pour régler l'asservissement d'alignement sur OFF.	Trou d'ajustement dans le côté inférieur du capteur laser (Fig.B)	Amplitude maximum (voir le photos 1 et 2.)	(d)
6	RESEAU DE DIFFRACTION (2) " Vérification de polarité "	Disque test	Raccorder un oscillcscope à TP(RF). (X25-2932-71)	Le micro ordinateur en mode de test, presser la touche CLEAR pour régler l'asservissement d'alignement sur ON. (L'asservissement d'alimentation est réglé sur OFF.)	Trou d'ajustement dans le côté inférieur du capteur laser (Fig.B)	S'assurer que la forme se présente correctement.	(c)
7	RESEAU DE DIFFRACTION (3) " Vérieur que les faisceaux auxiliaires se rassemblent sur la même Piste "	Disque test	Déclencher à TP(RF) et raccorder un oscilloscope à TP(SUB). (X25-2932-71)	PLAY	Trou d'ajustement dans le côté inférieur du capteur laser (Fig.B)	Vérieur qu'ils sont comme dans la photo 3. *La photo 4 montre un exemple défectif.	(e)

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REGLAGE

N°	ITEM	REGLAGE D'ENTREE	REGLAGE DE SORTIE	REGLAGE DE LA LECTURE	POINT D'ALIGNEMENT	ALIGNEMENT POUR	FIG
8	BALANCE D'ERREUR D'ALIGNEMENT	Disque test	Raccorder un oscilloscope à TP(TE) ou un voltmètre CC. (X25-2932-71)	En mode de test, persser la touche CHECK pour régler l'asservissement d'alignement sur OFF.	TE BALANCE VR2 (X25-2930-00)	Symétrie entre les formes supérieure et inférieure ou • DC=0 ±0,05V	(d)
9	GAIN DE MISE AU POINT	Disque test: Appliquer un signal 1kHz, 0,5Vrms à la troche 2 de CN7 sur la plaquette X25-2932-71.	Raccorder LPF avec 47 kohmes, 470pF sur la broche 1 CN7 de X25-2932-71 et y raccorder un oscilloscope ou un voltmètre CA.	PLAY	GAIN DE MISE AU POINT VR4 (X25-2932-71)	50mVrms *1/10 d'entrée (quand l'oscilloscope est utilisé, vérifier uniquement le composant 1kHz.)	(f)
10	GAIN D'ALIGNEMENT	Disque test: Appliquer un signal 1kHz, 0,5Vrms à la troche 4 de CN7 sur la plaquette X25-2932-71.	Raccorder LPF avec 47 kohmes, 470pF sur la broche 5 de X25-2932-71 et y raccorder un oscilloscope ou un voltmètre CA.	PLAY	GAIN D'ALIGNEMENT VR5 (X25-2932-71)	50mVrms *1/10 d'entrée (quand l'oscilloscope est utilisé, vérifier uniquement le composant 1kHz.)	(f)
11	PLL		Raccorder un ompteur de fréquence à TP(PLCK). (X25-2932-71)	ARRET Court-circuiter les bornes PLCK et F.TEST.	ADJ.FREQUENCE VR1 (X25-2932-71)	ADJ. FREQUENCE 4,4MHz ±0,15MHz.	(g)

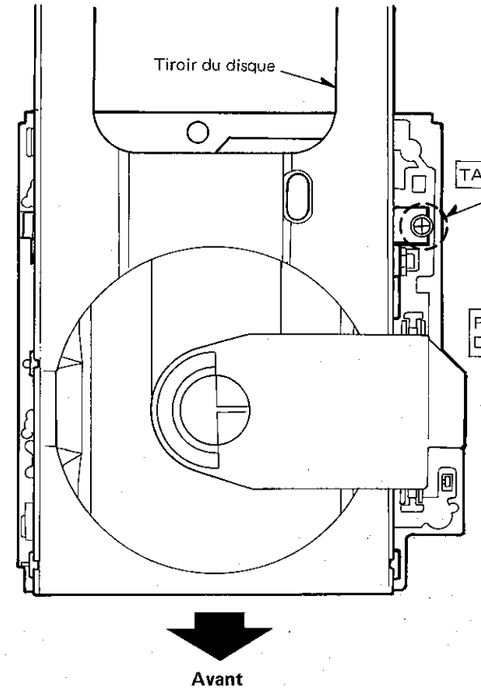

Fig. A : Ensemble du méchanisme (vue du dessus)

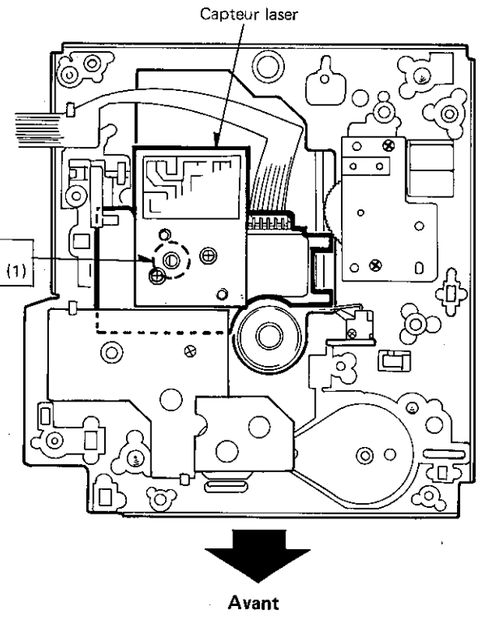

Fig. B : Ensemble du méchanisme (vue du dessous)

ABGLEICH

NR.	GEGENSTAND	EINGANGS-EINSTELLUN	AUSGANGS-EINSTELLUNGE	SPIELER-EINSTELLUNG	ABGLEICH-PUNKT	ABGLEICHUNG	ABB.
1	LASERLEISTUNG	–	Das Sensorteil des optischen Leistungmeters auf die Aufnehmerlinse ansetzen.	Die Stifte 8 und 9 kurzschließen und die Spannungsver-. sorgung einschalten, um den Test-Modus zu aktivieren. Die Taste +10 drücken, dann öffnet sich der Träger, und die LD gibt Licht aus.	VR1 Regelwiderstand des ALPC-Schaltkreises am Tonabnehmer (X29-1760-00)	0,1 mW	(a)
2	BETRIEBSSTROM DES LASERTONABNEHMERS (Nur wenn der Tonabnehmer defekt zu sein scheint)	–	Stift 1 von CN1 entfernen und das Gleichstrom Ampermeter anschließen. (X29-1760-00)	Die Stifte 8 und 9 kurzschließen und die Spannungsversorgung einschalten, um den Test-Modus zu aktivieren. Die Taste +10 drücken, dann öffnet sich der Träger, und die LD gibt Licht sus.	–	Stromwert + 5,5mA auf dem Lasertonabnehmer markiert. Wenn der Strom 40mA oder mehr über dem obigen Wert liegt, ist er defekt.	(b)
3	FOKUS-FEHLERAUSGLEICH	Testdisc	Ein oszilloskop an TP(RF) anschließen. (X25-2932-71)	PLAY	FOKUS-FEHLERAUSGLEICH VR3 (X25-2932-71)	Optimales Augenmuster	(c)
4	TANGENTIAL	Testdisc	Ein oszilloskop an TP(RE) anschließen.	PLAY	Schraube an der rechten Seite des Mechanismus (Abb.A)	Optimales Augenmuster	(c)
5	OPTISCHES GITTER (1)	Testdisc	Ein oszilloskop an TP(TE) anschließen. (X25-2932-71)	Die Spannungsversorgung einschalten, während die Stifte 8 und 9 kurzgeschlossen werden, um den Mikrocomputer in die Test-Betriebsart zu versetzen. Die PLAY-Taste für 1 bis 2 Minuten drücken, um den Titel Nr. 1 zu suchen. Dann die CHECK-Taste drücken, um den Spurhalte-Servo auf Off zu stellen.	Einstellöffnung unten am Laser-Tonabnehmer (Abb.B)	Maximal-Amplitude (Siehe Photo 1 und 2.)	(d)
6	OPTISCHES GITTER (2) " Überprüfung der Polarit t "	Testdisc	Ein Oszilloskop an TP(RF) anschließen. (X25-2932-71)	Die CLEAR-Taste drücken, um den Spurhalteservo auf ON einzustellen, während sich der Mikrocomputer in Testbetriebsart befindet. (Der Vorschubservo steht auf OFF.)	Einstellungsöffnung an der Unterseite des Laser-tonabnehmers (Abb.B)	Überprüfen, daß das Augenmuster richtig ausgegeben wird.	(c)
7	OPTISCHES GITTER (3) " Überprüfen, daß die Nebenstraflen auf der selben Spur erscheinen. "	Testdisc	TP(RF) auslösen und ein Oszilloskop an TP(SUB) anschließen. (X25-2932-71)	PLAY	Einstellungsöffnung an der Unterseite des Laser-tonabnehmers (Abb.B)	Überprüfen, daß sie Photo 3 entsprechen. *Photo 4 zeigt das Beispiel eines defekten Tonabnehmers.	(e)

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ABGLEICH

NR.	GEGENSTAND	EINGANGS-EINSTELLUNG	AUSGANGS-EINSTELLUNG	SPIELER-EINSTELLUNG	ABGLEICH-PUNKT	ABGLEICHUNG	ABB.
8	SPURHALTEFEHLER-AUSGLEICH	Testdisc	Ein Oszilloskop oder ein Gleighstrom-Voltmeter an TP(TE) anschließen. (X25-2932-71)	In der Testbetriebsart die CHECK-Taste drücken, um den Spurhalteservo auf OFF zu stellen.	TE BALANCE VR2 (X25-2932-71)	Symmetrie zwischen oberen und unteren Mustern oder Gleichstrom DC=0 ±0,05V	(d)
9	FOKUSVERSTÄRKUNG	Testdisc: Ein 1kHz, 0,5Vrms Signal an Stift 2 von CN7 an Platine X25-2932-71 anlegen.	LPF mit 47kohm, 470pF an Stift 1 von CN7 an X25-2932-71 und ein Oszilloskop oder Wechselstrom-Voltmeter anschließen.	PLAY	FOKUSVERSTÄRKUNG VR4 (X25-2932-71)	50mVrms *Das ist 1/10 der Eingangs spannung (Bei Verwendung eine Oszilloskop nur die 1kHz Komponente überprüfen.)	(f)
10	SPURHALTE-VERSTÄREKUNG	Testdisc: Ein 1kHz, 0,5Vrms Signal an Stift 4 von CN7 an platine X25-2932-71 anlegen.	LPF mit 47kohm, 470pF an Stift 5 von an X25-2932-71 und ein Oszilloskop oder Wechselstrom-Voltmeter anschließen.	PLAY	SPURHALTE-VERSTÄREKUNG VR5 (X25-2932-71)	50mVrms *Das ist 1/10 der Eingangs spannung (Bei Verwendung eine Oszilloskop nur die 1kHz Komponente überprüfen.)	(f)
11	PLL		Einen Frequenzz hler an TP(PLCK) anschließen. (X25-2932-71)	HALT Die Anschlüsse PLCK und F.TEST kurzschließen.	F.ADJ. VR1 (X25-2932-71)	Frequenz ADJ. 4,4MHz ±0,15MHz	(g)

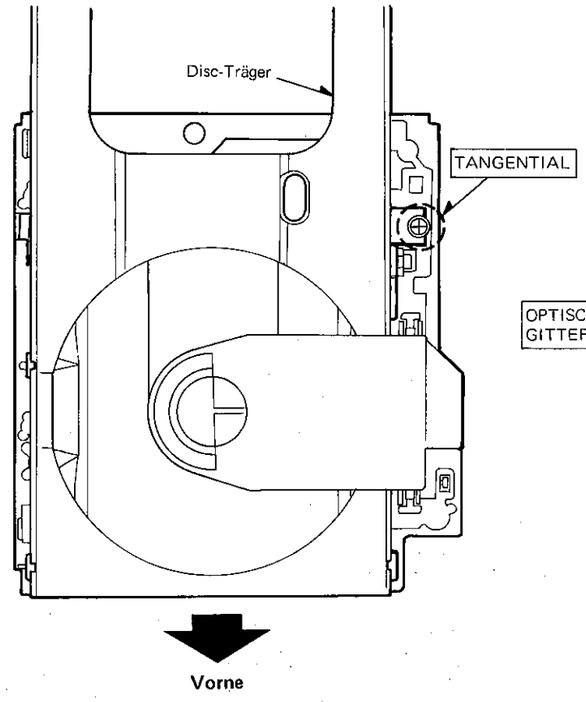


Abb. A : Mechanismus-Baugruppe (Draufsicht)

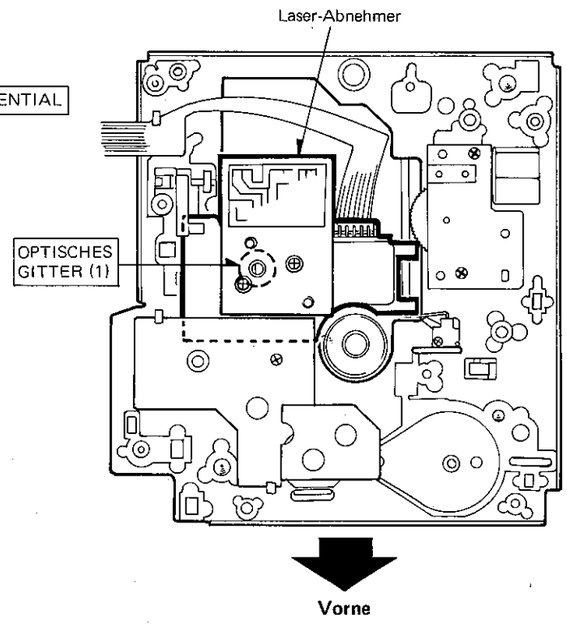


Abb. B : Mechanismus-Baugruppe (Unteransicht)

ABGLEICH

NR.	GEGENSTAND	EINGANGS-EINSTELLUNG	AUSGANGS-EINSTELLUNG	SPIELER-EINSTELLUNG	ABGLEICH-PUNKT	ABGLEICHUNG	ABB.
8	SPURHALTEFEHLER-AUSGLEICH	Testdisc	Ein Oszilloskop oder ein Gleighstrom-Voltmeter an TP(TE) anschließen. (X25-2932-71)	In der Testbetriebsart die CHECK-Taste drücken, um den Spurhalteservo auf OFF zu stellen.	TE BALANCE VR2 (X25-2932-71)	Symmetrie zwischen oberen und unteren Mustern oder Gleichstrom DC=0 ±0,05V	(d)
9	FOKUSVERSTÄRKUNG	Testdisc: Ein 1kHz, 0,5Vrms Signal an Stift 2 von CN7 an Platine X25-2932-71 anlegen.	LPF mit 47kohm, 470pF an Stift 1 von CN7 an X25-2932-71 und ein Oszilloskop oder Wechselstrom-Voltmeter anschließen.	PLAY	FOKUSVERSTÄRKUNG VR4 (X25-2932-71)	50mVrms *Das ist 1/10 der Eingangs spannung (Bei Verwendung eine Oszilloskop nur die 1kHz Komponente überprüfen.)	(f)
10	SPURHALTE-VERSTÄREKUNG	Testdisc: Ein 1kHz, 0,5Vrms Signal an Stift 4 von CN7 an platine X25-2932-71 anlegen.	LPF mit 47kohm, 470pF an Stift 5 von an X25-2932-71 und ein Oszilloskop oder Wechselstrom-Voltmeter anschließen.	PLAY	SPURHALTE-VERSTÄREKUNG VR5 (X25-2932-71)	50mVrms *Das ist 1/10 der Eingangs spannung (Bei Verwendung eine Oszilloskop nur die 1kHz Komponente überprüfen.)	(f)
11	PLL		Einen Frequenzz hler an TP(PLCK) anschließen. (X25-2932-71)	HALT Die Anschlüsse PLCK und F.TEST kurzschließen.	F.ADJ. VR1 (X25-2932-71)	Frequenz ADJ. 4,4MHz ±0,15MHz	(g)

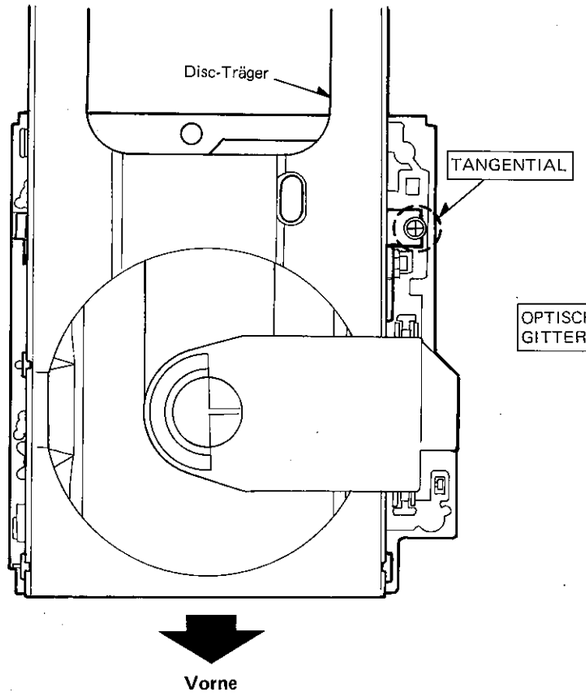


Abb. A : Mechanismus-Baugruppe (Draufsicht)

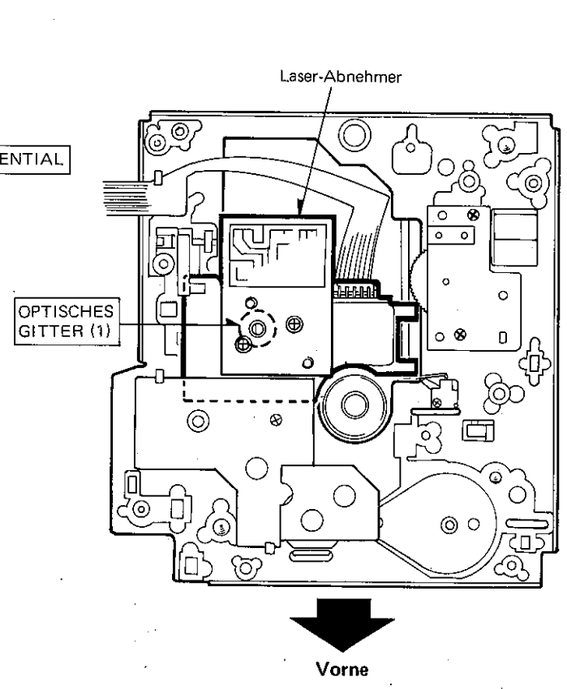
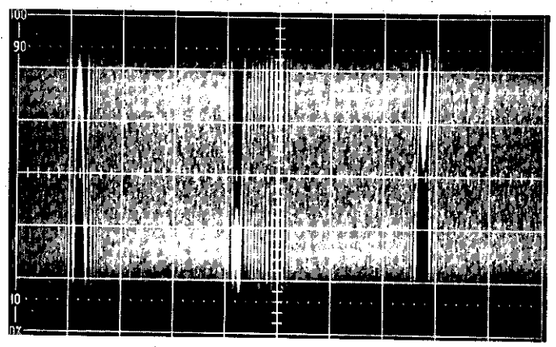


Abb. B : Mechanismus-Baugruppe (Unteransicht)

ADJUSTMENT/REGLAGE/ABGLEICH

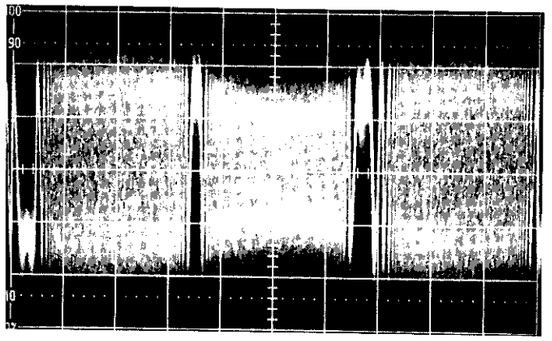
DIFFRACTION GRID ADJUSTMENT/REGLAGE DU RESEAU DE DIFFRACTION/BEUGUNGSGITTER-EINSTELLUNG



Correctly adjusted waveform
Forme d'onde correctement réglée
Richtig eingestellte Wellenform

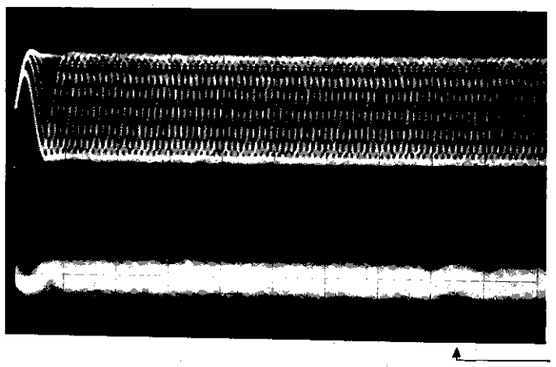
Photo 1
Photo 1
Foto 1

Tracking error waveform
Upper : 0.5V/div.
Lower : 20ms/div.
Forme d'onde d'erreur d'alignement
Supérieure : 0.5V/div.
Inférieure : 20ms/div.
Spurhaltefehler-Wellenform
Oben : 0.5V/Teilung
Unten : 20ms/Teilung



Incorrect (shifted) waveforms
Forme d'onde incorrecte (dérivée)
Falsche (verschobene) Wellenform

Photo 2
Photo 2
Foto 2

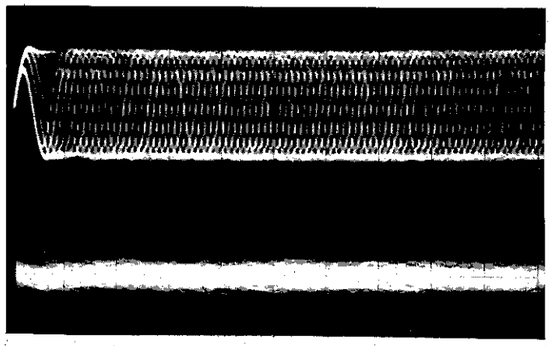


Correctly adjusted waveform
Forme d'onde correctement réglée
Richtig eingestellte Wellenform

Photo 3
Photo 3
Foto 3

Upper : RF signal 1V/div.
Lower : Sub spot beam signal 0.1V/div. 0.5μs/div.
Supérieure : signal HF 1V/div.
Inférieure : signal de rayon spot auxiliaire 0.1V/div., 0.5μs/div.
Oben : HF-Signal 1V/Teilung
Unten : Nebenpunktstrahl-Signal 0,1V/Teilungs, 0,5μs/Teilung

17~18μs later
17~18μs us plus tard
17~18μs später



Waveform when the sub beam is shifted to the adjacent track.
Forme d'onde quand le rayon auxiliaire est décalé sur la piste adjacente.
Wellenform, wenn der Nebenstrahl zur benachbarten Spur verschoben ist.

Photo 4
Photo 4
Foto 4

DP-969 DP-969

VOLTAGE CHECK TABLE

X25-2932-71

	B	C	E
Q1	0.8V	8.9V	0V
Q2	0.8V	8.2V	0V
Q3	–0.5V	8.2V	0V
Q4	–0.5V	–8.9V	0V
Q5	–29.9V	–41.3V	–29.3V
Q6	–5.8V	–8.9V	–5.1V
Q7	–5.7V	8.2V	5.1V
Q8	–5.7V	–16.2V	–5.1V
Q9	5.7V	15.7V	5.1V
Q10	–16.2V	–12.8V	–12.2V
Q11	–12.9V	15.7V	12.2V
Q14	2.4V	3.0V	3.1V
Q15	–12.1	11.5V	–12.2V
Q16	0V	12.1V	0V
Q17	–12.2V	44V	–12.2V

Q8

1	8.2V	5	–8.9V
2	0.5V	6	0V
3	–0.6V	7	0V
4	0.5V	8	0V

IC1

1	(–16.3V)	33	2.3V
2	(0.3V)	34	2.4V
3	(–2.0V)	35	0V
4	(–11.5V)	36	0V
5	0V (5.1V)	37	5.0V (0V)
6	(2.5V)	38	5.1V
7	1.3V (4.2V)	39	4.6V
8	5.1V (0V)	40	(–26.6V)
9	5.1V	41	(–26.6V)
10	0V	42	(–26.6V)
11	4.3V (0V)	43	(–26.6V)
12	5.1V (0V)	44	(–26.6V)
13	5.0V (0V)	45	(–26.6V)
14	0V (5.1V)	46	(–26.6V)
15	5.1V	47	(–26.6V)
16	0V (5.1V)	48	(–26.6V)
17	0.6V	49	(–26.6V)
18	5.1V (0.6V)	50	(–26.6V)
19	5.1V	51	(–26.6V)
20	0.6V	52	(–26.6V)
21	0V	53	(–28.9V)
22	0V	54	(–21.3V)
23	0V	55	(–21.2V)
24	0V	56	(–29.3V)
25	5.1V	57	(–5.1V)
26	5.1V	58	(–19.0V)
27	5.1V	59	(–14.1V)
28	5.0V (0V)	60	(–28.6V)
29	5.1V	61	(–26.1V)
30	2.3V	62	(–11.5V)
31	2.6V	63	(–11.5V)
32	0V	64	5.1V

IC2

1	0V	41	2.5V
2	5.1V (0V)	42	2.5V
3	2.4V (0V)	43	2.5V
4	2.8V (0V)	44	2.5V
5	2.4V	45	2.5V
6	2.5V	46	2.5V
7	5.1V (0V)	47	2.5V
8	2.5V	48	2.5V
9	2.5V	49	4.4V
10	0V	50	2.2V
11	1.8V (2.8V)	51	2.2V
12	0V	52	0V
13	5.1V	53	2.5V
14	5.1V	54	2.5V
15	5.1V	55	0V
16	4.6V	56	0V
17	0.1V	57	5.1V
18	0.1V (5.1V)	58	0V
19	0V (5.1V)	59	0V
20	5.1V (0V)	60	1.2V
21	0.4V	61	1.2V
22	0V (3.9V)	62	0V (3.7V)
23	1.3V (4.1V)	63	0V (3.7V)
24	0V	64	0V (1.9V)
25	2.5V (0V)	65	0V (1.9V)
26	0V	66	0V (1.9V)
27	2.5V	67	0V (5.1V)
28	5.1V (0V)	68	2.5V
29	1.8V (2.1V)	69	2.5V
30	1.8V (1.6V)	70	2.3V
31	1.8V (2.1V)	71	5.1V
32	1.8V (1.6V)	72	0V (5.1V)
33	5.1V	73	5.1V
34	1.8V (1.7V)	74	0V (5.1V)
35	1.8V (3.8V)	75	2.5V
36	1.8V (2.5V)	76	2.4V
37	1.8V (2.5V)	77	2.4V
38	2.5V	78	2.5V (0V)
39	2.5V	79	2.5V
40	2.5V	80	2.5V

IC3

1	2.5V	13	1.7V
2	2.5V	14	1.6V
3	2.5V	15	2.1V
4	2.5V	16	2.2V
5	2.5V	17	2.1V
6	2.5V	18	2.2V
7	2.5V	19	–
8	2.5V	20	2.2V
9	2.5V	21	4.4V
10	3.8V	22	2.5V
11	1.6V	23	2.5V
12	0V	24	5.1V

IC4

1	–5.1V	25	–5.1V
2	–4.2V	26	0V
3	0V	27	5.1V
4	0V	28	4.6V
5	0V	29	5.1V
6	0V	30	5.1V
7	0V	31	5.1V
8	0V	32	0V
9	0V	33	2.8V
10	0V	34	2.8V
11	0V	35	2.2V
12	0V	36	2.3V
13	0V	37	2.5V
14	0V	38	2.5V
15	0V	39	5.1V (0V)
16	5.1V	40	2.4V (0V)
17	–0.6V	41	5.1V (0V)
18	0V	42	2.5V (0V)
19	0V	43	5.1V
20	0.5V	44	0V
21	0V	45	0.8V (–0.5V)
22	0V	46	0.5V
23	–4.1V	47	0V
24	0.1V (5.1V)	48	0V

IC5

1	0V	16	–5.1V
2	1.4V (0V)	17	–5.1V
3	0V	18	0V
4	4.7V	19	0V
5	4.6V	20	0V
6	0V	21	–4.2V
7	0V	22	0V
8	0V	23	–2.2V (–3.6V)
9	0V	24	–1.7V (0V)
10	0V	25	0V
11	0V	26	2.5V
12	–1.1V (0V)	27	2.4V
13	–0.7V	28	4.7V (0V)
14	0V	29	5V
15	–2.6V (1.0V)	30	5.1V

IC6

1	2.0V	13	1.2V
2	2.5V	14	2.5V
3	0V	15	1.4V (0V)
4	2.1V	16	1.5V (0V)
5	2.5V	17	1.6V (0V)
6	2.5V	18	1.8V (0V)
7	2.5V (0V)	19	1.8V (0V)
8	2.4V	20	2.3V
9	0V	21	2.5V
10	0V	22	2.5V
11	1.2V	23	2.5V
12	0V	24	5.7V

IC7

1	1.8V (0V)	8	2.5V
2	5.1V	9	2.3V
3	3.2V (5.1V)	10	5.1V
4	5.1V	11	2.5V
5	2.5V	12	4.6V
6	2.5V	13	2.5V
7	0V	14	5.1V

IC8

1	–5.1V	9	0V
2	0V	10	0V
3	5.1V	11	0V
4	0V	12	0V
5	2.3V	13	0V
6	2.5V	14	–2.6V
7	1.8V (0V)	15	2.3V
8	5.1V	16	5.1V

IC9

1	0V	9	0V
2	0V	10	4.4V
3	0V	11	4.4V
4	0V	12	0V
5	0V	13	0V
6	0V	14	0V
7	–5.1V	15	0V
8	0V	16	5.1V

IC10

1	0V	5	0V
2	0V	6	0V
3	0V	7	0V
4	–12.2V	8	12.2V

IC11

1	2.5V	8	4.4V
2	1.2V	9	1.2V
3	4.4V	10	2.5V
4	0V	11	2.5V
5	0V	12	2.5V
6	–	13	2.5V
7	0V	14	5.1V

IC12

1	0V	8	2.5V
2	5.1V	9	2.5V
3	5.1V	10	2.5V
4	0V	11	2.5V
5	5.1V	12	2.5V
6	0V	13	2.5V
7	0V	14	5.1V

IC13

1	–5.8V	5	0V
2	–5.1V	6	0V
3	–5.1V	7	5.7V
4	–12.2V	8	12.2V

IC14

1	–5.7V	5	5.1V
2	0V	6	5.1V
3	0V	7	5.7V
4	–12.2V	8	12.2V

IC15

1	–5.8V	5	0V
2	–5.1V	6	0V
3	–5.1V	7	5.7V
4	–12.2V	8	12.2V

IC16

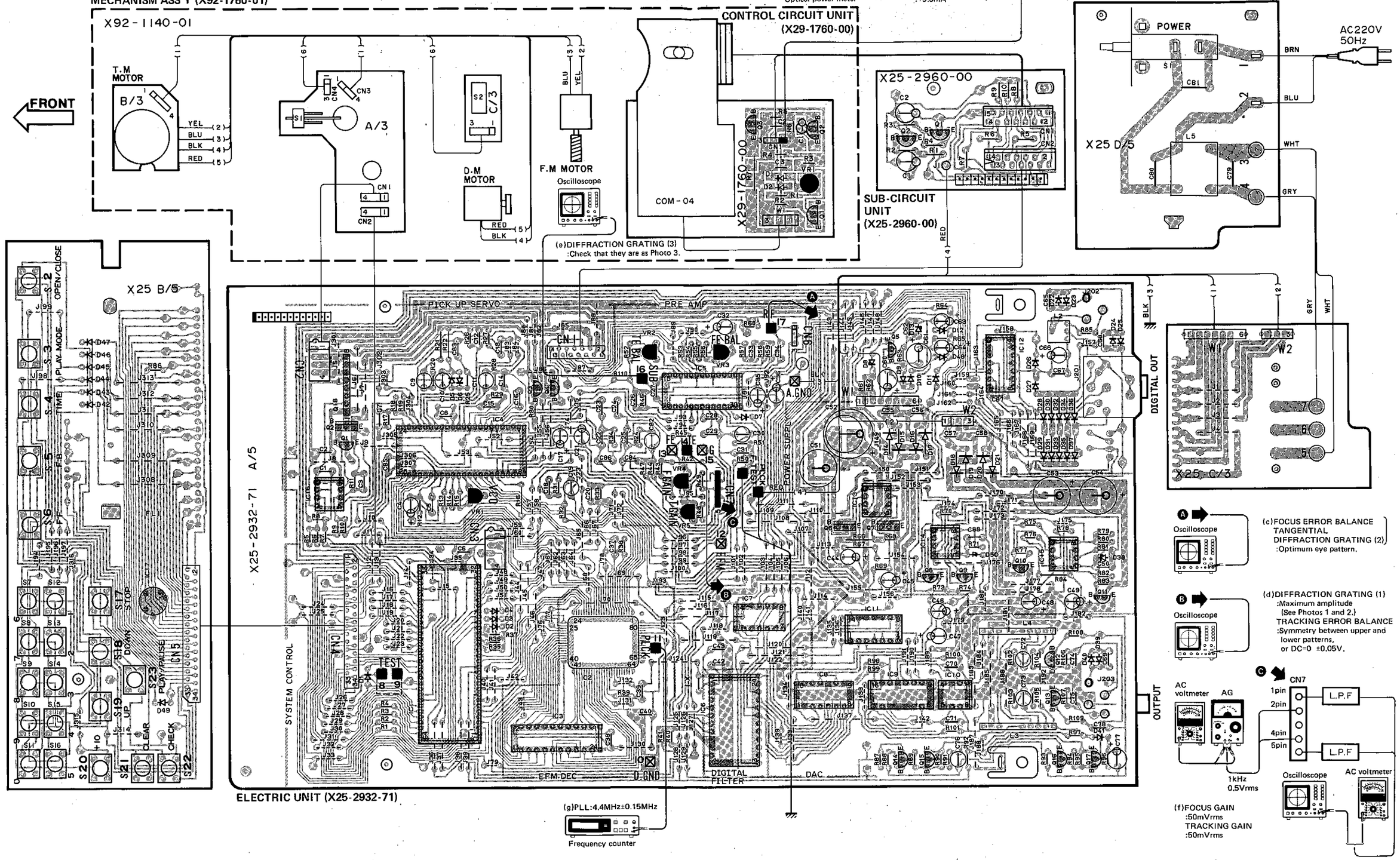
1	0.5V	5	0V
2	0V	6	0V
3	0V	7	0.8V
4	–8.9V	8	8.2V

X25-2960-00

	B	C	E
Q1	4.3V (5.0V)	5.0V (–4.7V)	5.1V
Q2	0V (5.0V)	0.6V (0V)	0V

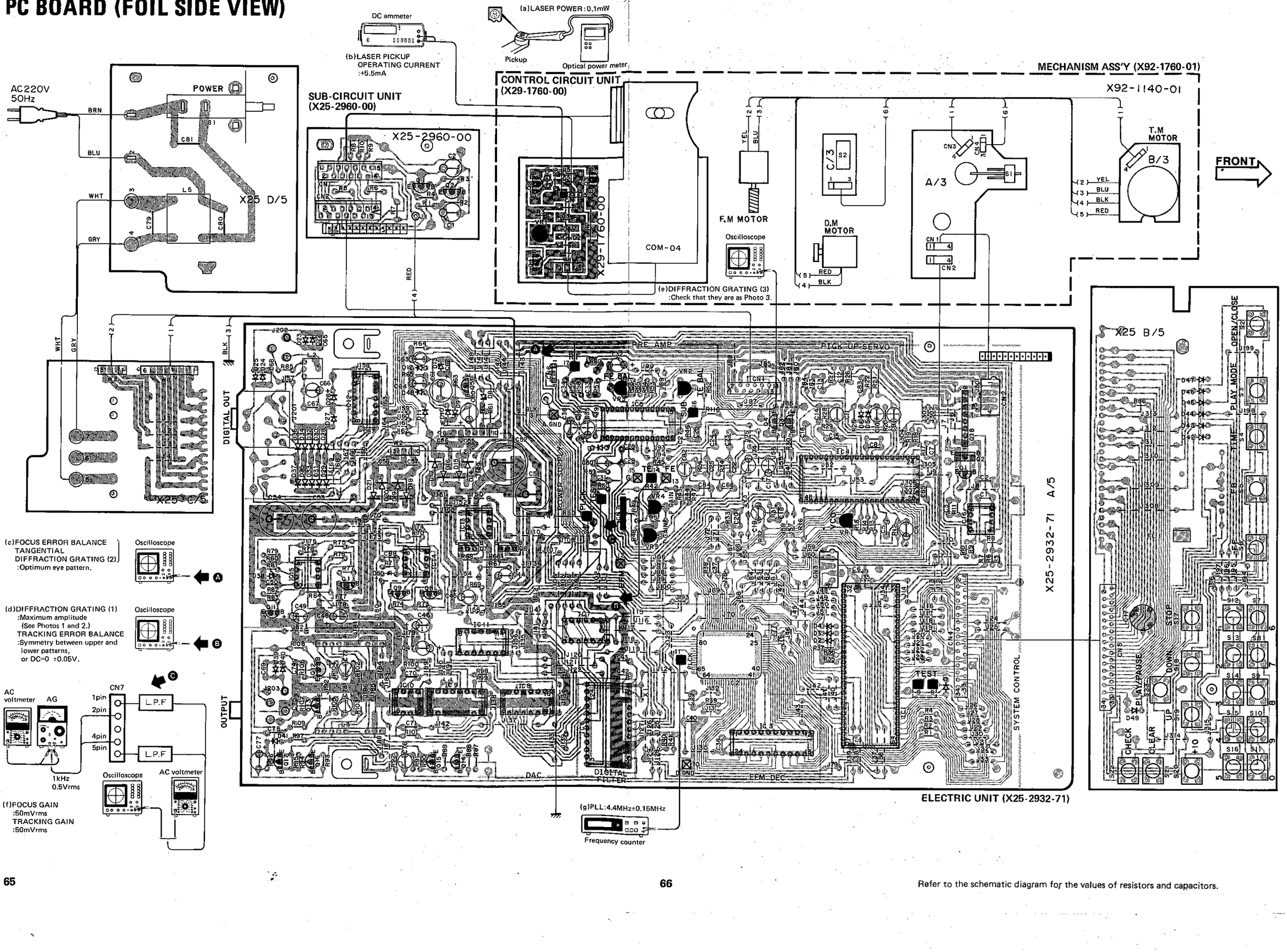
- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.
- Les tensions c.c. doivent être measurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.
- Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen. Voltmeter gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen instrumenten oder Geräten u.U. geringfügig.

PC BOARD (COMPONENT SIDE VIEW)



Refer to the schematic diagram for the values of resistors and capacitors.

PC BOARD (FOIL SIDE VIEW)



ELECTRIC UNIT (X25-2932-71)

Refer to the schematic diagram for the values of resistors and capacitors.

MECHA. ASSY CDM-04B(X92-1140-01)

(X92-1140-01)(A/3)

(X92-1140-01)(B/4)

(X92-1140-01)(C/3)

(X25-2960-00)

(X25-2960-00)
Q1 : 2SA1286
Q2 : 2SC945(A)(Q,P)

(X25-2932-71)(A/5)

(X29-1760-00)

(X29-1760-00)
Q1 : 2SC945(A)(G,R)
Q2,3 : 2SC3666

D1 : 1SS176 or 1SS133
D2 : RD3.0ES(B)

(X25-2932-71)

IC1	: μPD75208CW-052
IC2	: CXD1125Q
IC3	: TMM2115BP-15, LC3516AS-15 or LC3517AS-15
IC4	: CXA1082S
IC5	: CXA1081S
IC6	: CX23034
IC7, 11	: TC74HC00P
IC8	: PCM56P
IC9	: μPD4053BC or BU4053B
IC10	: μPC4072C or NJM072BD
IC12	: TC74HCU04P
IC13~16	: NJM4558
IC17	: BX-1408
Q1,5,8,10	: 2SA1534A
Q2,7	: 2SD1266
Q3	: 2SD882
Q4	: 2SB772
Q6	: 2SB941
Q9,11	: 2SC3940A
Q12,13	: 2SC2878
Q14,16	: 2SA733(A)(Q,P) or 2SA999(E,F)
Q15,17	: 2SC945(A)(Q,P) or 2SC2320(E,F)
Q18	: STA341M
D1, 42~47, 49	: 1SS131 or 1SS178
D2~7, 9~12, 22, 23, 26, 27, 39, 40, 41, 48	: 1SS133 or 1SS176
D8, 38	: HZS5.6N(B2) or RD5.6ES(B2)
D13	: HZS30N(B) or RD30ES(B)
D14~21	: DSM1A1
D50	: HZS5.1N(B2) or RD5.1ES(B2)

2SA1286 2SC2320
2SA1534A 2SC2878
2SA733 2SC3940A
2SA999 2SC945

2SB772
2SD882

2SD1266

2SC3666

2SB941

NJM072BD
NJM4558D

PCM56P

BU4053B
μPD4053BC

CX23034

μPC4072C

SAT341M

CXD1125Q

CXA1081S

J K L M N O P Q R S T

(X25-2932-71)(B/5)

CN2 CN3 CN4 TEST

TRACKING COIL DRIVER

FEED MOTOR DRIVER

TRAY MOTOR DRIVER

SERVO CONTROL

IC 4

VCO

± 5V DIGITAL AVR

± 5V DAC AVR

± 12V ANALOG AVR

IC 1 μ-COM

D/A CONVERTER

ANALOG SW

IC 9

OP AMP

EMPHASIS SW

MUTE SW

MUTE CONTROL

PULSE TRANS DRIVER

INVERTER

FL-1

IC17 REMOCON IC

CN5

S11 S12 S13 S14 S15 S16 S7 S8 S9 S10 S20 S2 S17 S5 S6 S18 S19 S4 S21 S22 S23 S3

D47 D46 D43 D42 D45 D44

0 1 2 3 4 5 6 7 8 9 +10 DP/CL STOP FB FF DOWN UP TIME CLEAR CHECK PLAY/PAUSE P-MODE

(X25-2932-71)(C/5) (X25-2932-71)(D/5)

W1 W2 AC 3.9V AC 19V AC 7.6V AC 15V

S1 AC220Hz 50Hz

(E,T)TYPE

J203 R ch L ch

J202 DIGITAL OUT

XD1125Q

CXA1081S

CXA1082S

μPD75208CW-052

TC74HCU04P
TC74HC00P

Signal line
Recording signal line
Ground line
+B line
−B line

DP-969(K)

* Some logic circuit of IC7 and IC12 are not used.

- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

DP-969

KENWOOD

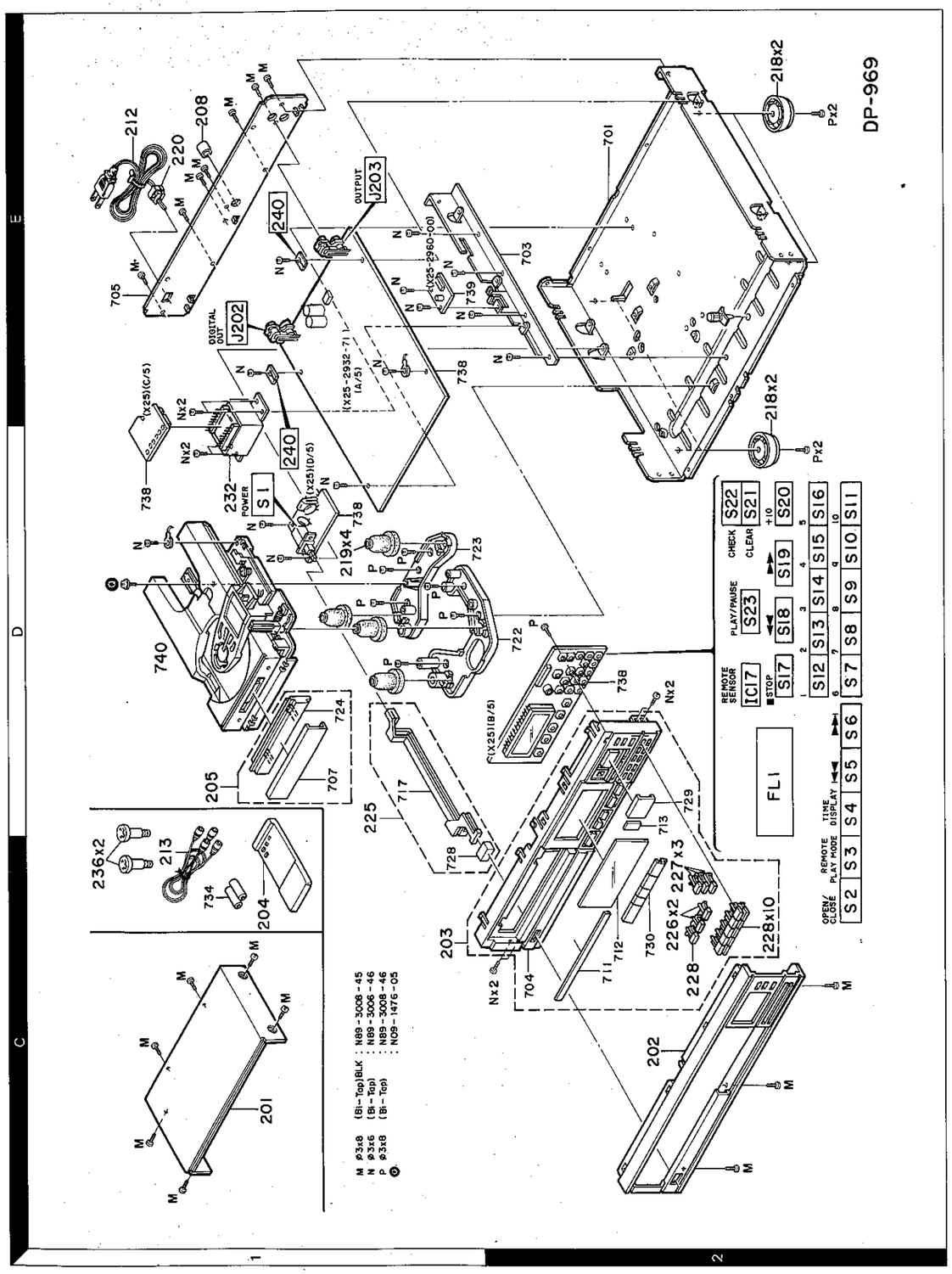
EXPLODED VIEW (MECHANISM)

A	ø3x8	(TP)	: N09-1522-05
B	ø2.6x22		: N86-2622-46
C	M2x10	(Bi)	: N35-2010-46
D	M2.6x5	(TP)	: N90-2605-46
E	ø2.6x10	(Bi)	: N86-2610-46
F	M2x2.5		: N39-2025-46
G	M3x14	(TP)	: N90-3014-46
L	M2.6x10		: N86-2610-46

: These portions should be coated with grease.

Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)



Parts with the exploded numbers larger than 700 are not supplied.

PARTS LIST

* New Parts
Parts without Parts No. are not supplied.
Les articles non mentionnes dans le Parts No. ne sont pas fournis.
Teile ohne Parts No. werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
			DP-969			
201	1C	*	A01-1543-01	METALLIC CABINET		
202	2C	*	A20-5185-02	PANEL		
203	1C	*	A22-0660-03	SUB PANEL ASSY		
204	1C	*	A70-0168-05	REMOTE CONTROLLER ASSY		
205	1D	*	A29-0101-04	PANEL ASSY (TRAY)		
208	1E	*	B09-0068-05	CAP		
-			B46-0122-13	WARRANTY CARD	E	
-			B46-0143-03	WARRANTY CARD	T	
-		*	B50-6796-00	INSTRUCTION MANUAL(ENGLISH)		
-		*	B50-6797-00	INSTRUCTION MANUAL(FRENCH)	E	
-		*	B50-6800-00	INSTRUCTION MANUAL(G,D,I)	E	
-			B58-0400-04	CAUTION CARD		
⚠ 212	1E		E30-0459-05	AC POWER CORD	E	
⚠ 212	1E		E30-1416-05	AC POWER CORD	T	
213	1C		E30-0505-05	AUDIO CORD		
-		*	H01-7553-04	ITEM CARTON CASE		
-			H10-1788-04	POLYSTYRENE FOAMED FIXTURE		
-		*	H10-3429-02	POLYSTYRENE FOAMED FIXTURE		
-		*	H10-3430-02	POLYSTYRENE FOAMED FIXTURE		
-			H25-0223-04	PROTECTION BAG (750X350X0.03)		
-			H25-0232-04	PROTECTION BAG (235X350X0.03)		
218	2E		J02-0186-05	FOOT		
219	1D		J02-0191-05	INSULATOR		
⚠ 220	1E		J42-0083-05	POWER CORD BUSHING		
225	2D		K29-2553-03	KNOB ASSY (POWER)		
226	2C	*	K29-2652-04	KNOB (BUTTON) FF,REW		
227	2C		K29-2653-04	KNOB (BUTTON) CHECK,CLEAR,+10		
228	2C	*	K29-2654-04	KNOB (BUTTON) STOP,1-0		
⚠ 232	1D	*	L01-7882-05	POWER TRANSFORMER		
236	1C		N09-1759-05	MACHINE SCREW		
Q	1D		N09-1476-05	MACHINE SCREW (Ø3X16)		
			ELECTRIC UNIT (X25-2932-71)			
C1			CK45FB1H102K	CERAMIC 1000PF K		
C2			CK45FF1H103Z	CERAMIC 0.010UF Z		
C3			CK45FB1H102K	CERAMIC 1000PF K		
C4			CE04KW1C330M	ELECTRO 33UF 16WV		
C5			CF92FV1H104J	MF 0.10UF J		
C6			C91-0700-05	CERAMIC 0.1UF J		
C7			CF92FV1H103J	MF 0.010UF J		
C8			CF92FV1H104J	MF 0.10UF J		
C9			C90-1333-05	NP-ELEC 22UF 10WV		
C10			C90-1350-05	NP-ELEC 2.2UF 50WV		
C11			C90-1333-05	NP-ELEC 22UF 10WV		
C12			CC45FSL1H101J	CERAMIC 100PF J		
C13			CF92FV1H333J	MF 0.033UF J		
C14			CF92FV1H104J	MF 0.10UF J		
C15			CC45FSL1H271J	CERAMIC 270PF J		
C16			CF92FV1H104J	MF 0.10UF J		
C17			CE04KW1C330M	ELECTRO 33UF 16WV		
C18			CF92FV1H333J	MF 0.033UF J		

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C19			C90-1331-05	NP-ELEC 0.47UF 50WV		
C20			CK45FF1H473Z	CERAMIC 0.047UF Z		
C21			CE04KW1C330M	ELECTRO 33UF 16WV		
C22			CK45FB1H332K	CERAMIC 3300PF K		
C23 ,24			CF92FV1H473J	MF 0.047UF J		
C25			CC45FSL1H470J	CERAMIC 47PF J		
C26			CK45FF1H103Z	CERAMIC 0.010UF Z		
C27 ,28			CF92FV1H333J	MF 0.033UF J		
C29			CF92FV1H103J	MF 0.010UF J		
C30			C90-1331-05	NP-ELEC 0.47UF 50WV		
C31			CK45FF1H103Z	CERAMIC 0.010UF Z		
C32			CE04KW1C330M	ELECTRO 33UF 16WV		
C33			CC45FSL1H150J	CERAMIC 15PF J		
C34			CK45FF1H103Z	CERAMIC 0.010UF Z		
C35 ,36			CE04KW1C330M	ELECTRO 33UF 16WV		
C37			CK45FB1H102K	CERAMIC 1000PF K		
C38			CK45FF1H103Z	CERAMIC 0.010UF Z		
C39			CK45FB1H102K	CERAMIC 1000PF K		
C40			C91-0700-05	CERAMIC 0.1UF J		
C42 ,43			CC45FSL1H100D	CERAMIC 10PF D		
C44 ,45		*	C90-1505-05	ELECTRO 1000UF 6.3WV		
C46 -49			CE04KW1C330M	ELECTRO 33UF 16WV		
C50			CK45FF1H103Z	CERAMIC 0.010UF Z		
C51 ,52			CE04KW1C222M	ELECTRO 2200UF 16WV		
C53 ,54			CE04KW1E102M	ELECTRO 1000UF 25WV		
C55 -58			CK45FF1H103Z	CERAMIC 0.010UF Z		
C60			CE04KW1E101M	ELECTRO 100UF 25WV		
C61			CE04KW1H101M	ELECTRO 100UF 50WV		
C62			CK45FF1H103Z	CERAMIC 0.010UF Z		
C63			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C64			CE04KW1V4R7M	ELECTRO 4.7UF 35WV		
C65			CK45FF1H103Z	CERAMIC 0.010UF Z		
C66			CE04KW1V100M	ELECTRO 10UF 35WV		
C67			CK45FF1H103Z	CERAMIC 0.010UF Z		
C69			CK45FF1H103Z	CERAMIC 0.010UF Z		
C70 ,71			C91-0090-05	POLYSTY 150PF J		
C72 ,73			C90-1332-05	NP-ELEC 10UF 16WV		
C74 ,75			CC45FSL1H101J	CERAMIC 100PF J		
C76			C90-1332-05	NP-ELEC 10UF 16WV		
C77			CE04KW1C101M	ELECTRO 100UF 16WV		
C78			CK45FF1H103Z	CERAMIC 0.010UF Z		
⚠ C79 -81			C91-0647-05	CERAMIC 0.01UF P		
C82			C90-1456-05	NP-ELEC 0.22UF 50WV		
C83			CF92FV1H473J	MF 0.047UF J		
C84			CC45FSL1H151J	CERAMIC 150PF J		
C85			CK45FF1H103Z	CERAMIC 0.010UF Z		
C86			CK45FB1H152K	CERAMIC 1500PF K		
C87 -89			CK45FF1H103Z	CERAMIC 0.010UF Z		
C90			CK45FF1H473Z	CERAMIC 0.047UF Z		
C91 ,92			C91-0725-05	CERAMIC 15PF J		
240	1D		E23-0149-05	TERMINAL		
CN1		*	E10-1409-05	FLAT CABLE CONNECTOR		
CN4 ,5		*	E10-3401-05	FLAT CABLE CONNECTOR		
J202	1E	*	E13-0131-05	PHONO JACK(1P)DIGITAL OUT		
J203	1E		E13-0235-05	PHONO JACK(2P) OUTPUT		

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	L2		*	L39-0147-05	MATCHING COIL		
	L3 ,4		*	L79-0738-05	ACTIVE FILTER		
⚠	L5			L79-0723-05	LINE FILTER		
	X1			L77-1114-05	CRYSTAL RESONATOR		
	VR1			R12-1067-05	TRIMMING POT.(2.2K)VCO		
	VR2			R12-3097-05	TRIMMING POT.(22K) TE BAL		
	VR3			R12-5046-05	TRIMMING POT.(100K)FE BAL		
	VR4 ,5			R12-3096-05	TRIMMING POT.(10K) F/T GAIN		
⚠	S1	1D		S40-1103-05	PUSH SWITCH (POWER TYPE)		
	S2 -23	2C,2D		S40-1064-05	PUSH SWITCH		
	D1			1SS131	DIODE		
	D1			1SS178	DIODE		
	D2 -7			1SS133	DIODE		
	D2 -7			1SS176	DIODE		
⚠	D8			HZS5.6N(B2)	ZENER DIODE		
⚠	D8			RD5.6ES(B2)	ZENER DIODE		
⚠	D9 -12			1SS133	DIODE		
⚠	D9 -12			1SS176	DIODE		
	D13		*	HZS30N(B)	ZENER DIODE		
	D13		*	RD30ES(B)	ZENER DIODE		
⚠	D14 -21			DSM1A1	DIODE		
	D22 ,23			1SS133	DIODE		
	D22 ,23			1SS176	DIODE		
	D26 ,27			1SS133	DIODE		
	D26 ,27			1SS176	DIODE		
	D38			HZS5.6N(B2)	ZENER DIODE		
	D38			RD5.6ES(B2)	ZENER DIODE		
	D39 -41			1SS133	DIODE		
	D39 -41			1SS176	DIODE		
	D42 -47			1SS131	DIODE		
	D42 -47			1SS178	DIODE		
⚠	D48			1SS133	DIODE		
⚠	D48			1SS176	DIODE		
	D49			1SS131	DIODE		
	D49			1SS178	DIODE		
	D50		*	HZS5.1N(B2)	ZENER DIODE		
	D50			RD5.1ES(B2)	ZENER DIODE		
	D51			1SS133	DIODE		
	D51			1SS176	DIODE		
	FL1	2D	*	FIP12DM6	FLUORESCENT INDICATOR TUBE		
	IC1		*	UPD75208CW-052	IC(MICROPROCESSOR)		
	IC2		*	CXD1125Q	IC(DIGITAL SIGNAL PROCESSOR)		
	IC3		*	LC3516AS-15	IC(2KX8 RAM)		
	IC3		*	LC3517AS-15	IC(2KX8 RAM)		
	IC3			TMM2115BP-15	IC(2KX8 RAM)		
	IC4		*	CXA1082S	IC(SERVO SIGNAL PROCESSOR)		
	IC5		*	CXA1081S	IC(RF AMP)		
	IC6			CX23034	IC(CD DIGITAL FILTER)		
	IC7			TC74HC00P	IC(QUAD 2-INPUT NAND GATE)		
	IC8			PCM56P	IC(DA CONVERTER)		
	IC9			BU4053B	IC(3-INPUT 2CH MPX/DE-MPX)		
	IC9			UPD4053BC	IC(3-INPUT 2CH MPX/DE-MPX)		
	IC10		*	NJM072BD	IC(FET OP AMP X2)		
	IC10		*	UPC4072C	IC(OP AMP X2)		

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IC11			TC74HC00P	IC(QUAD 2-INPUT NAND GATE)		
IC12			TC74HCU04P	IC(HEX INVERTER)		
IC13-16			NJM4558D	IC(OP AMP X2)		
IC17	2D	*	BX-1408	IC(REMOTE SENSOR)		
Q1			2SA1534A	TRANSISTOR		
Q2			2SD1266	TRANSISTOR		
Q3			2SD882	TRANSISTOR		
Q4			2SB772	TRANSISTOR		
Q5			2SA1534A	TRANSISTOR		
Q6			2SB941	TRANSISTOR		
Q7			2SD1266	TRANSISTOR		
Q8			2SA1534A	TRANSISTOR		
Q9			2SC3940A	TRANSISTOR		
Q10			2SA1534A	TRANSISTOR		
Q11			2SC3940A	TRANSISTOR		
Q12 ,13			2SC2878	TRANSISTOR		
Q14			2SA733(A)(Q,P)	TRANSISTOR		
Q14			2SA999(E,F)	TRANSISTOR		
Q15			2SC2320(E,F)	TRANSISTOR		
Q15			2SC945(A)(Q,P)	TRANSISTOR		
Q16			2SA733(A)(Q,P)	TRANSISTOR		
Q16			2SA999(E,F)	TRANSISTOR		
Q17			2SC2320(E,F)	TRANSISTOR		
Q17			2SC945(A)(Q,P)	TRANSISTOR		
Q18			STA341M	TRANSISTOR		
SUB-CIRCUIT UNIT (X25-2960-00)						
C1			CE04KW1H010M	ELECTRO 1.0UF 50WV		
C2			CE04KW1C330M	ELECTRO 33UF 16WV		
CN2			E10-1409-05	FLAT CABLE CONNECTOR		
Q1			2SA1286	TRANSISTOR		
Q2			2SC945(A)(Q,P)	TRANSISTOR		
MECHANISM ASS'Y (X92-1140-01)						
C1 -3			C91-0769-05	CERAMIC 0.01UF M		
5	2B		D10-1270-14	ROD		
6	1B	*	D10-1738-04	ARM (SWITCH)		
7	2B	*	D10-1740-03	ARM (TANGENTIAL)		
8	1B		D10-1741-13	ARM (CALMPER)		
9	1A	*	D10-1742-02	ARM (LIFTER)		
10	2A	*	D10-1743-03	SLIDER (LIFTER)		
11	1A	*	D10-1782-14	SLIDER ASSY		
12	2A	*	D13-0359-13	GEAR (MAIN)		
13	2B	*	D13-0360-04	GEAR		
14	1B	*	D13-0361-05	GEAR ASSY (RACK)		
16	3B		D13-0363-08	GEAR (WHEEL)		
17	2A	*	D16-0140-14	BELT		
18	3B	*	D40-0375-05	DRIVE MECHANISM ASSY		
22	1B	*	G01-1890-04	EXTENSION SPRING (SLIDER)		
23	2B	*	G01-1891-04	COMPRESSION SPRING(ARM)		
24	1B	*	G01-1892-14	COMPRESSION SPRING(ARM)		
25	1A	*	G01-1893-04	EXTENSION SPRING (TRAY ASSY)		
30	1B		J11-0086-04	CLAMPER (DISK)		
31	2B	*	J25-4905-22	PRINTED WIRING BOARD(PU)		

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32	2B	*	J91-0280-15	PICKUP		
34	1A	*	J99-0035-01	TRAY		
35	2B	*	J21-3941-14	MOUNTING HARDWARE ASSY(TRAY)		
38	3B		N19-0366-04	FLAT WASHER (GEAR)		
39	2A,2B	*	N19-1043-05	FLAT WASHER		
A	1B		N09-1522-05	SET SCREW (3X8)ROD		
S1	3B	*	S46-1087-05	LEAF SWITCH (OPN/CLS)		
S2	3A		S33-1019-05	LEVER SWITCH (SLT)		
43	3A	*	T42-0097-05	DC MOTOR (ROADING)		
44	3A		T42-0099-05	DC MOTOR		
45	2A	*	T42-0100-04	MOTOR ASSY (DISK)		
CONTROL CIRCUIT UNIT (X29-1760-00)						
C1			CE04JW0J100M	ELECTRO 10UF 6.3WV		
C2 ,3			C91-0769-05	CERAMIC 0.01UF M		
R7			RS14DB3A120J	FL-PROOF RS 12 J 1W		
VR1		*	R12-3118-05	TRIMMING POT.(10K)LDP ADJ		
D1			1SS133	DIODE		
D1			1SS176	DIODE		
D2		*	RD3.0ES(B)	ZENER DIODE		
Q1 ,2			2SC945(A)(Q,P)	TRANSISTOR		
Q3			2SC3666	TRANSISTOR		

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SPECIFICATIONS

Audio

Frequency response ..... 4 Hz ~ 20 kHz
Signal-to-Noise ratio ..... more than 95 dB
Dynamic range ..... more than 93 dB
Total harmonic distortion .... 0.0035 % or less (1 kHz, THD)
Channel separation ..... more than 90 dB
Wow & flutter ..... Below measurable limit (±0.001 %, W PEAK)
Line output level ..... 2.0 V

Format

Type ..... Compact disc player
Read system ..... Non-contact optical pick-up system
Laser pick-up ..... GaAlAs, λ = 780 nm, 3-beam type
Spindle speed ..... About 200 rpm — 500 rpm
Error correction ..... Cross Interleave Read Solomon Code
Number of channels ..... 2 channels

General

Power consumptions ..... 16 W
Dimentions ..... W: 340 mm (13-3/8″)
H: 84 mm (3-5/16″)
D: 349 mm (13-3/4″)
Weight (Net) ..... 4.0 kg (8.8 lb)

Remote control unit

Model RC-P969
System ..... Infrared beam pulse
Power requirements ..... DC 3 V: R6 (AA) × 2
Dimentions ..... H: 157 mm (6-3/16″)
W: 68 mm (2-11/16″)
D: 18 mm (11/16″)
Weight ..... 115 g (0.253 lb) (With batteries)

Note:
We follow a policy of advancements in development. For this reason specifications may be changed without notice.

Note :
Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the Europe (E) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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