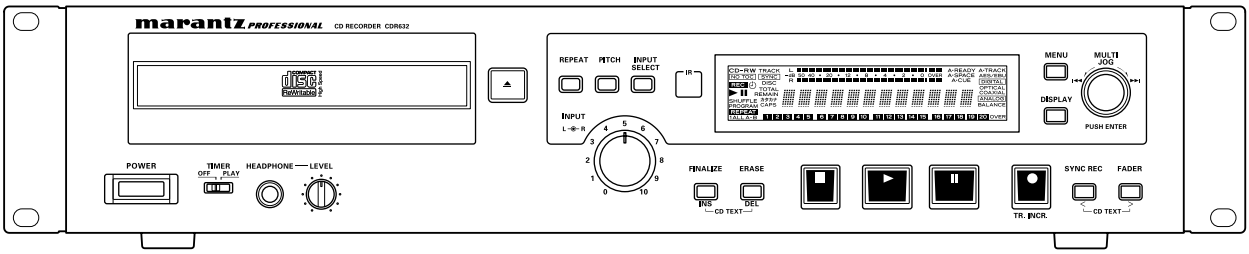
Service Manual

CDR632 /N1B/U1B

CD Recorder

CDR632



COMPACT disc ReWritable High Speed

TABLE OF CONTENTS

Please use this service manual with referring to the user guide (D.F.U.) without fail.
修理の際は、必ず取扱説明書を準備し操作方法を確認の上作業を行ってください。

marantz PROFESSIONAL

CDR632

Part no. 90M42AZ855010
First Issue 2006.01
ecm

SHOCK, FIRE HAZARD SERVICE TEST :

CAUTION : After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins (with unit NOT connected to AC mains and its Power switch ON), and the face or Front Panel of product and controls and chassis bottom.

Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before it is return to the user/customer.

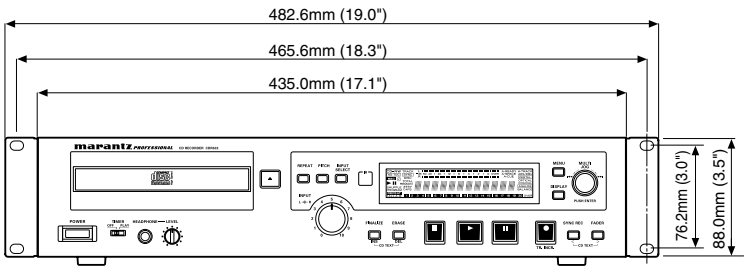
Ref. UL Standard No. 60065.

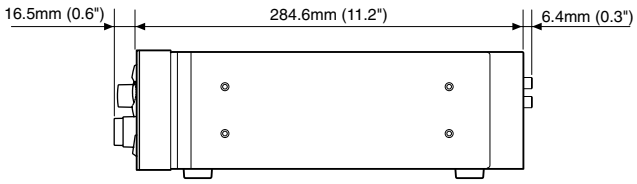
In case of difficulties, do not hesitate to contact the Technical Department at above mentioned address.

1. TECHNICAL SPECIFICATIONS

Recordable discs	CD-R, CD-R-DA, CD-RW, CD-RW-DA (High Speed CD-RW is supported)	
Quantization bit depth	16-bit linear	
Sampling frequency	44.1 kHz	
Frequency response	20Hz–20KHz	
	±0.8 dB (playback)	
	±1.0 dB (recording)	
S/N	95 dB or better (playback)	
	90 dB or better (recording)	
Dynamic range	95 dB or better (playback)	
	90 dB or better (recording)	
Distortion	0.006% or less (playback)	
	0.008% or less (recording)	
Channel separation	90 dB or better (playback: 1 kHz)	
	80 dB or better (recording: 1 kHz)	
Wow and flutter	below measurable limits (less than 0.001%)	
Analog inputs	unbalanced input	RCA jack
	Nominal input level	–10 dBV (at full scale: –16 dB)
	Minimum input level	–19 dBV or higher (minimum input level that can be adjusted to nominal level (Full Scale –16 dB))
	Input impedance	22 kΩ ±10% (unbalanced)
Analog outputs	unbalanced output	RCA jack
	Nominal output level	–10 dBV ±2 dB (at full scale: –16 dB)
	Maximum output level	+6 dBV ±2 dB
	Output impedance	600Ω ±10% (unbalanced)
Phones output	stereo phone jack (1/4")	
	20 mW or greater	
	32Ω load	
Digital output	COAXIAL	RCA jack (IEC-60958 Type II)
	OPTICAL	TOSLINK (IEC-60958 Type II)
Power supply /U1B	120 VAC/60Hz	
/N1B	230 VAC/50Hz	
Current consumption		
/U1B 18 W		
/N1B 20W		
Dimensions	Width 482.6 mm (19.0")	
	Height 98.0 mm (3.9")	
	Depth 307.5 mm (12.1")	
Weight	4.9 kg (10.8 lbs)	

Dimensions



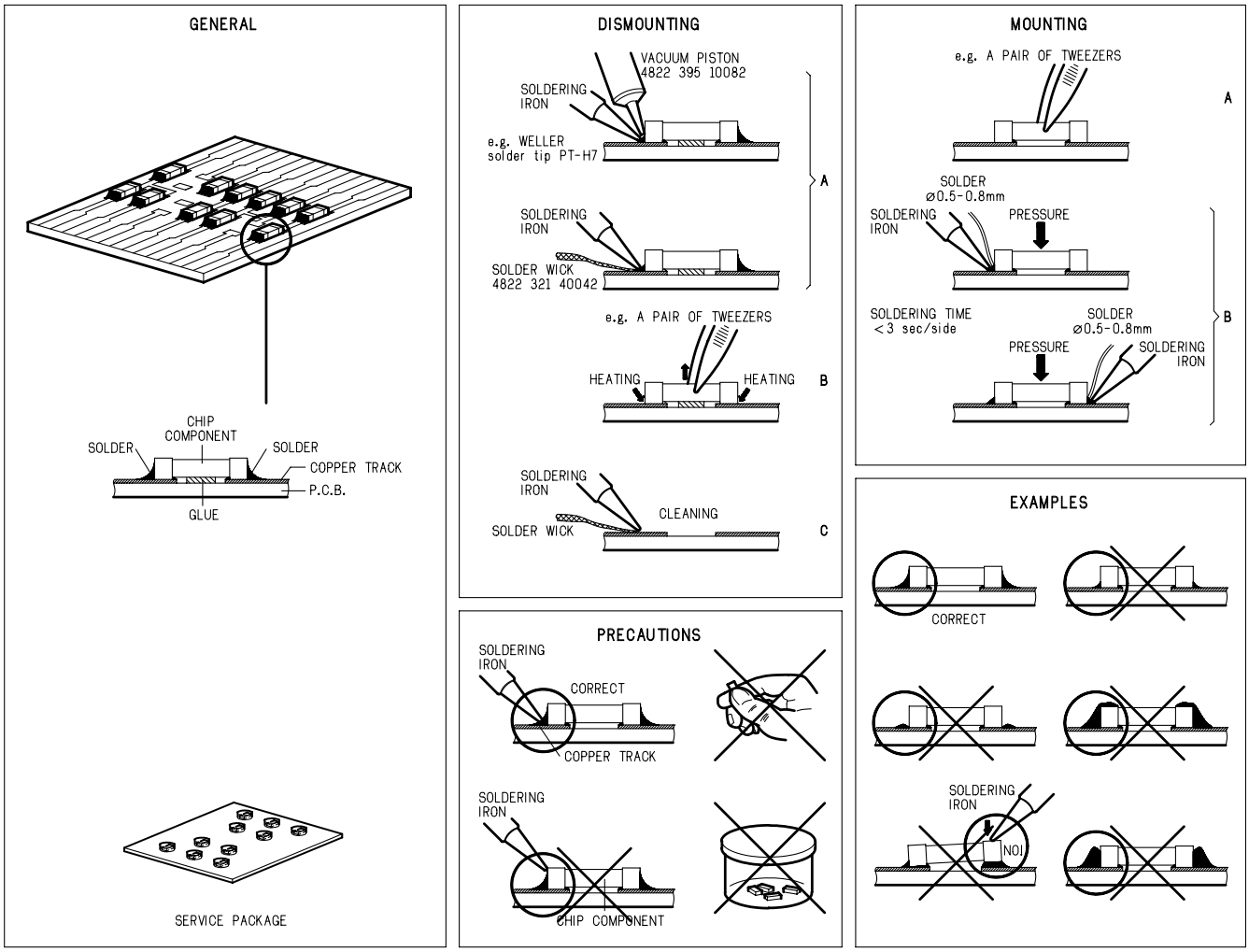


2. INTRODUCTION ABOUT DISCS

About discs

CD-R	
CD-RW	

3. SERVICE HINTS AND TOOLS



SERVICE TOOLS

Audio signals disc	4822 397 30184
Disc without errors (SBC444)+	
Disc with DO errors, black spots and fingerprints (SBC444A)	4822 397 30245
Disc (65 min 1kHz) without no pause	4822 397 30155
Max. diameter disc (58.0 mm)	4822 397 60141
Torx screwdrivers	
Set (straight)	4822 395 50145
Set (square)	4822 395 50132
13th order filter	4822 395 30204

4. WARNING AND LASER SAFETY INSTRUCTIONS

(GB) WARNING

All ICs and many other semi-conductors are susceptible to electrostatic discharges (ESD).
Careless handling during repair can reduce life drastically.
When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance.
Keep components and tools also at this potential.

ESD

(NL) WAARSCHUWING

Alle IC's en vele andere halfgeleiders zijn gevoelig voor elektrostatische ontladingen (ESD).
Onzorgvuldig behandelen tijdens reparatie kan de levensduur drastisch doen verminderen.
Zorg ervoor dat u tijdens reparatie via een polsband met weerstand verbonden bent met hetzelfde potentiaal als de massa van het apparaat.
Houd componenten en hulpmiddelen ook op ditzelfde potentiaal.

(F) ATTENTION

Tous les IC et beaucoup d'autres semi-conducteurs sont sensibles aux décharges statiques (ESD).
Leur longévité pourrait être considérablement écourtée par le fait qu'aucune précaution n'est prise a leur manipulation.
Lors de réparations, s'assurer de bien être relié au même potentiel que la masse de l'appareil et enfiler le bracelet serti d'une résistance de sécurité.
Veiller a ce que les composants ainsi que les outils que l'on utilise soient également a ce potentiel.

(D) WARNUNG

Alle IC und viele andere Halbleiter sind empfindlich gegen elektrostatische Entladungen (ESD).
Unsorgfältige Behandlung bei der Reparatur kann die Lebensdauer drastisch vermindern.
Sorgen sie dafür, das Sie im Reparaturfall über ein Pulsarmband mit Widerstand mit dem Massepotential des Gerätes verbunden sind.
Halten Sie Bauteile und Hilfsmittel ebenfalls auf diesem Potential.

(I) AVVERTIMENTO

Tutti IC e parecchi semi-conduttori sono sensibili alle scariche statiche (ESD).
La loro longevita potrebbe essere fortemente ridatta in caso di non osservazione della piu grande cauzione alla loro manipolazione.
Durante le riparazioni occorre quindi essere collegato allo stesso potenziale che quello della massa dell'apparecchio tramite un braccialetto a resistenza.
Assicurarsi che i componenti e anche gli utensili con quali si lavora siano anche a questo potenziale.

(GB)

Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.

(NL)

Veiligheidsbepalingen vereisen, dat het apparaat in zijn oorspronkelijke toestand wordt terug gebracht en dat onderdelen, identiek aan de gespecifieerde worden toegepast.

(D)

Bei jeder Reparatur sind die geltenden Sicherheitsvorschriften zu beachten.
Der Originalzustand des Gerats darf nicht verandert werden.
Fur Reparaturen sind Original-Ersatzteile zu verwenden.

(I)

Le norme di sicurezza esigono che l'apparecchio venga rimesso nelle condizioni originali e che siano utilizzati pezzi di ricambiago idetici a quelli specificati.

(F)

Les normes de sécurité exigent que l'appareil soit remis a l'état d'origine et que soient utilisées les pièces de rechange identiques à celles spécifiées.

"Pour votre sécurité, ces documents doivent être utilisés par des spécialistes agrées, seuls habilités à réparer votre appareil en panne."

LASER SAFETY

This unit employs a laser. Only a qualified service person should remove the cover or attempt to service this device, due to possible eye injury.

USE OF CONTROLS OR ADJUSTMENTS OR PERFORMANCE OF PROCEDURE OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.

AVOID DIRECT EXPOSURE TO BEAM

WARNING

The use of optical instruments with this product will increase eye hazard.
Repair handling should take place as much as possible with a disc loaded inside the player

WARNING LOCATION: INSIDE ON LASER COVERSHIELD

CAUTION VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGÅ UDSÆTTELSE FOR STRÅLING
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL Å PNES UNNGÅ EKSPONERING FOR STRÅLEN
VARNING SYNLIG OCH OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD BETRAKTA EJ STRÅLEN
VARO! AVATT AESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTTÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN
VORSICHT SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETSEN
DANGER VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM
ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

5. Test Mode

5.1 How to Enter the Test Mode

While Pressing the **PLAY**, **PAUSE** and **FADER** buttons, turn on the power switch.
The device becomes the test mode.

5.2 Test Mode Menu

In the test mode, turn the **MULT JOG** dial to select the individual test mode.
To determine the selection, push the **MULTI JOG** dial.
The types of the individual test mode are as follows.

- DISPLAY CHK
- KEY CHECK
- ENCODER CHK
- TIMER SW CHK
- KEYBOARD CHK
- RS-232C CHK
- EEP CHECK
- VERSION CHK

By pushing the **STOP** button in the individual test mode, the mode goes back to the test mode.
To exit the test mode, turn off the power switch.

5.3 Description of Individual Test Mode

● [DISPLAY CHK]
Every time when the **DISPLAY** button is pressed, all of GRID, character portions and LED are displayed on the screen of this device.
To exit the test mode, press the **STOP** button.

- The display lights out.
- GRID1 lights up. (e.g., INPUT, Auto xxx)
- GRID2 lights up. (e.g., the level meter)
- GRID15 lights up. (e.g., the PLAY, PAUSE and REC marks)
- GRID16 lights up. (calendar)
- The character lights up. (vertical stripes)
- The character lights up. (horizontal stripes)
- The character lights up. (checker flag)
- All the characters light up.
- Push the DISPLAY button again to exit this mode.

● [KEY CHECK]
On the screen, display one after the other the individual key to be pushed.
Complete checking all the keys in order to complete the key check.
Otherwise, the test mode cannot be exited.

5. テストモード

5.1 テストモードの入り方

本機の **PLAY** ボタンと **PAUSE** ボタンと **FADER** ボタンを同時に押した状態で、電源スイッチを ON にします。
テストモード状態になります。

5.2 テストモードメニュー

テストモード状態で、**MULTI JOG** ダイヤルを回してテストモードを選択します。
決定するには、**MULTI JOG** ダイヤルを押します。
テストモードの種類は以下の通りです。

- DISPLAY CHK
- KEY CHECK
- ENCODER CHK
- TIMER SW CHK
- KEYBOARD CHK
- RS-232C CHK
- EEP CHECK
- VERSION CHK

各テストモードに入った状態で **STOP** ボタンを押すと、テストモード状態に戻ります。
テストモードを終了するには、電源スイッチを OFF にします。

5.3 各テストモードの説明

●「DISPLAY CHK」
DISPLAY ボタンを押す度に、本機ディスプレイに GRID、キャラクター部、LED を全て表示します。
STOP ボタンを押すことで、このテストモードを終了します。

- ディスプレイ消灯。
- GRID1 点灯。（INPUT、Auto xxx 等）
- GRID2 点灯。（レベルメーター）
- GRIG15 点灯。（PLAY、PAUSE、REC マーク等）
- GRID16 点灯。（カレンダー）
- キャラクター点灯。（縦縞）
- キャラクター点灯。（横縞）
- キャラクター点灯。（チェッカーフラッグ）
- キャラクター全点灯。
- 再度、DISPLAY ボタンで終了します。

●「KEY CHECK」
ディスプレイにてプッシュするべきキーを表示していきます。
このモードは、最後までキーチェックをしてください。
キーチェックが完了しないと、テストモードは終了しません。

● [ENCODER CHK]
Display the encoder to be operated and its operation method on the screen.
Check it in the following order.
[Turn the encoder left, equivalent to the click of 3 times]
[Turn the encoder right, equivalent to the click of 3 times]
[Push the encoder.]

●[TIMER SW CHK]
In this mode, the present position of the timer switch will be displayed.
If the position is in the ON side, [TIMER SW ON] is displayed, and in the OFF side, [TIMER SW OFF] is displayed.
Confirm the display for the both positions.

●[KEYBOARD CHK]
As with KEY CHECK, push the individual key according to the display on the screen.
Contrary to KEY CHECK, not all the keys are needed to be checked to complete the test.

●[RS-232C CHK] (No need for the test on CDR632.)

●[EEP CHECK]
[DEFAULT]
Initial setting of EEP ROM. For plant shipment.
[DEF PARA]
Initial setting of EEP ROM, but the elapsed time of playback and recording time is not initialized.
[CLR TIME]
Initialize only the elapsed time of playback and recording time. Used when the CD drive is replaced during maintenance service.

●[VERSION CHK]
Turning the **MULTI JOG** dial leads to the following displays.
[SYS Ver xx.xx]
[KEY Ver xx.xx]
[DRV Ver xxxx]
[BUILD xxxxx]
[PTIME= xxxxh]
[RTIME=xxxxh]

●「ENCODER CHK」
ディスプレイにて、操作するべきエンコーダーと方法を表示します。
「エンコーダーの左回し、クリック３回分」
「エンコーダーの右回し、クリック３回分」
「エンコーダーのプッシュ」
の順番にチェックします。

●「TIMER SW CHK」
このテストモードに入ると、現在のタイマースイッチの位置を表示します。
ON 側にある場合は「TIMER SW ON」、OFF 側にある場合は「TIMER SW OFF」と表示します。
両方表示されることを確認してください。

●「KEYBOARD CHK」
「KEY CHECK」と同様にディスプレイに表示しているキーを実際に押します。
「KEY CHECK」のテストモードとは異なり、すべてのキーをチェックする必要はありません。

●「R S-232C CHK」（CDR632 ではテストの必要はありません。）

●「EEP CHECK」
「DEFAULT」
EEP ROM の初期化設定。工場出荷用です。
「DEF PARA」
EEP ROM の初期化設定。ただし、再生時間、記録時間の積算時間は初期化しません。
「CLR TIME」
CD の再生・記録積算時間だけの初期化。サービスにて CD ドライブを交換したときに使用します。

●「VERSION CHK」
MULTI JOG ダイヤルを回すことで、下記のように表示されます。
「SYS Ver xx.xx」
「KEY Ver xx.xx」
「DRV Ver xxxx」
「BUILD xxxxx」
「PTIME= xxxxh」
「RTIME=xxxxh」

6. UPDATE MODE

CDR632 has the system firmware and the CD-DRIVE firmware. Each firmware can be updated. They cannot be updated together by single operation. Update them individually.

6.1 How to Enter the Update Mode

While pressing the **STOP**, **RECORD** and **SYNC REC** buttons, turn on the power switch.

6.2 Update Mode Menu

In the update mode, turn the **MULT JOG** dial to select individual update mode.
To determine the selection, push the **MULT JOG** button.
The types of the update mode are as follows.

- SYSTEM UP
- DRIVE UP

6.3 Description of Individual Update Mode

●[SYSTEM UP]

Update the version of FALSH ROM.
Save the file to be update in a disc (CD-R) with the volume label [UPDATE] and the file name [FLASH MOT].
*(The file name can be [CDR632_xxxx.MOT], where xxxx is recommended to be numerals.)
Push the **ENTER** button, while [Sys Update?] is displayed.
The tray opens automatically ([Disc Set] is displayed).
Put the prepared disc on the tray and push the **OPEN/CLOSE** button to close the tray.
[File Check] is displayed and the system starts checking the loaded disc.
When the file is recognized as the updating file, “xx.xx → yy.yy” is displayed, where “xx.xx” indicates the current version number, and “yy.yy” does the version number of the updating file.
Press the **ENTER** button to start the update.
During the update, the sector numbers of FLASH ROM are displayed.
Upon completion of the update, “Complete” is displayed and the tray is opened.
Take the disc out. Turn off and back on the power to restart the unit.

6. アップデートモード

CDR632 にはシステムファームウェアと CD - DRIVE ファームウェアがあります。それぞれアップデートすることができます。2 つのファームウェアを同時に 1 回でバージョンアップすることはできません。個別にアップデートしてください。

6.1 アップデートモードの入り方

本機の **STOP** ボタンと **RECORD** ボタンと **SYNC REC** ボタンを同時に押した状態で、電源スイッチを ON にします。

6.2 アップデートモードメニュー

アップデートモード状態で、**MULTI JOG** ダイヤルを回してアップデートモードを選択します。
決定するには、**MULTI JOG** ダイヤルを押します。アップデートモードの種類は以下の通りです。

- SYSTEM UP
- DRIVE UP

6.3 各アップデートモードの説明

●「SYSTEM UP」

FLASH ROM のアップデートを実行します。
アップデート元のファイルはボリュームラベル「UPDATE」、ファイル名「FLASH.MOT」にして、ディスク（CD-R）に記録しておきます。
*（ファイル名は「CDR632_xxxx.MOT」でもかまいません。xxxx 部は数字を推奨。）
「Sys Update?」と表示されている状態で、**ENTER** ボタンを押します。
トレイが自動的にオープンするので（表示は「Disc Set」）準備したディスクをトレイに乗せ、**OPEN/CLOSE** ボタンでトレイを閉めます。
「File Check」が表示され、挿入したディスクのチェックが開始されます。
アップデートファイルであることを認識すると「xx.xx → yy.yy」（xx.xx は現在のバージョン、yy.yy はアップデートファイルのバージョンを示す）と表示しますので、**ENTER** ボタンを押してアップデートを実行します。
実行中は FLASH ROM の書き込みセクタナンバーを表示します。
アップデートが完了すると、「Complete」が表示となり、トレイがオープンするのでディスクを取り出します。
バージョンアップ後は電源を入れ直して再起動してください。

● [DRIVE UP]

Update the version of DRIVE.

Save the file to be update in a disc (CD-R) with the volume label [UPDATE] and the file name [W58xxxx.ABF].

*(The file name can be [T58xxxx.ABF].)

Push the **ENTER** button, while [Drv Update?] is displayed.

The tray opens automatically ([Disc Set] is displayed).

Put the prepared disc on the tray and push the **OPEN/CLOSE** button to close the tray.

[File Check] is displayed and the system starts checking the loaded disc.

When the file is recognized as the updating file, “x.xx → y.yy” is displayed, where “x.xx” indicates the current version number, and “y.yy” does the version number of the updating file.

Press the **ENTER** button to start the update.

During the update, the display [Drive Update] blinks.

Upon completion of the update, “Complete” is displayed and the tray is opened.

Take the disc out. Turn off and back on the power to restart the unit.

＊ **NOTE:**

Do not write the updating files from the System Firmware and CD-DRIVE Firmware into the same disc.

● 「DRIVE UP」

DRIVE のアップデートを実行します。

アップデート元のファイルはボリュームラベル「UPDATE」、ファイル名「W58xxxx.ABF」にして、ディスク（CD-R）に記録しておきます。

*（ファイル名は「T58xxxx.ABF」でもかまいません。）

「Drv Update?」と表示されている状態で、**ENTER** ボタンを押します。

トレイが自動的にオープンするので（表示は「Disc Set」）準備したディスクをトレイに乗せ、**OPEN/CLOSE** ボタンでトレイを閉めます。

「File Check」が表示され、挿入したディスクのチェックが開始されます。

アップデートファイルであることを認識すると「x.xx → y.yy」（x.xx は現在のバージョン、y.yy はアップデートファイルのバージョンを示す）と表示しますので、**ENTER** ボタンを押してアップデートを実行します。

実行中は「Drive Update」が点滅表示されます。

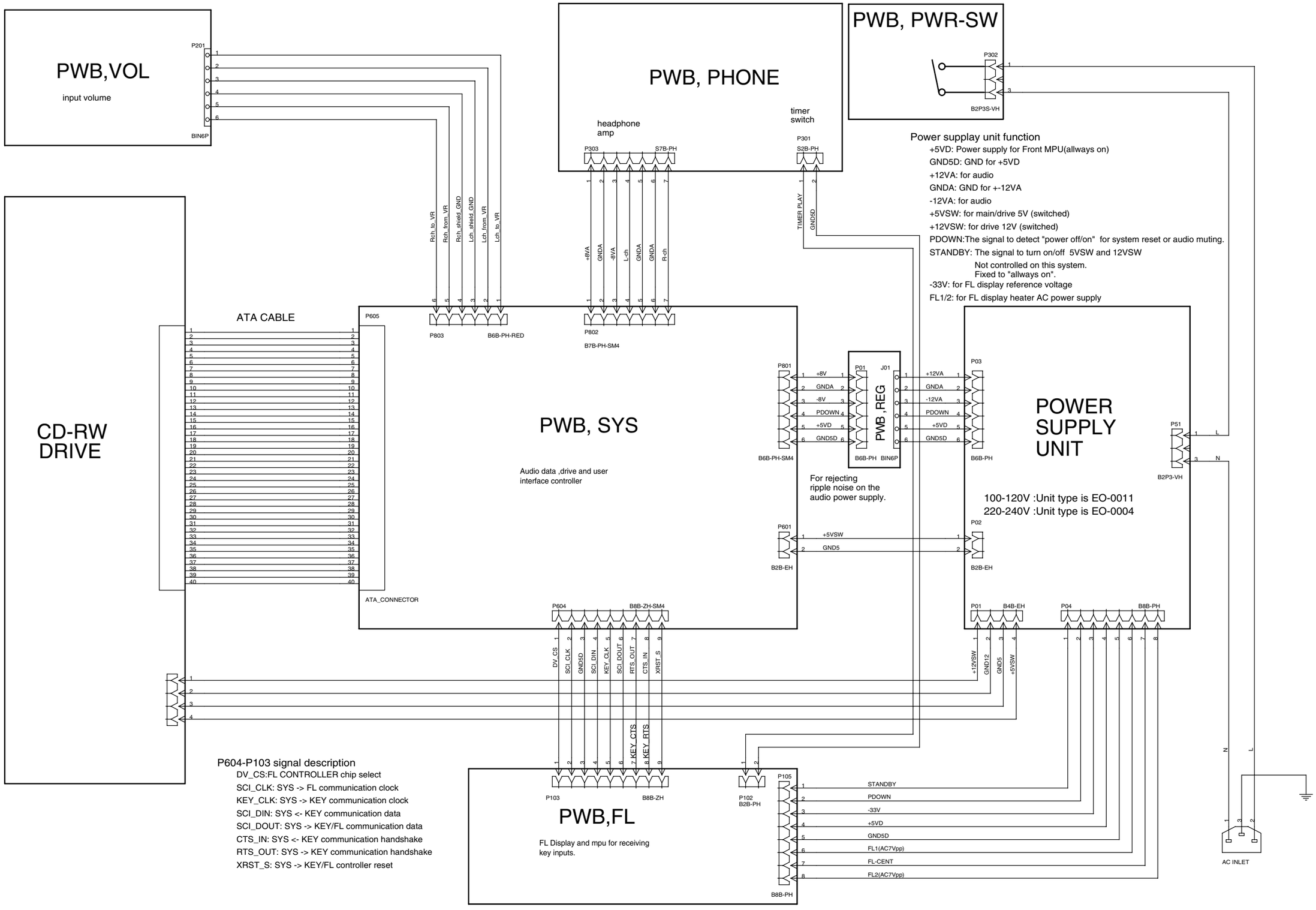
アップデートが完了すると、「Complete」が表示となり、トレイがオープンするのでディスクを取り出します。

バージョンアップ後は電源を入れ直して再起動してください。

＊ **NOTE:**

システムファームウェアのバージョンアップファイルと CD-DRIVE ファームウェアのバージョンアップファイルを同じディスクに書き込んではいけません。

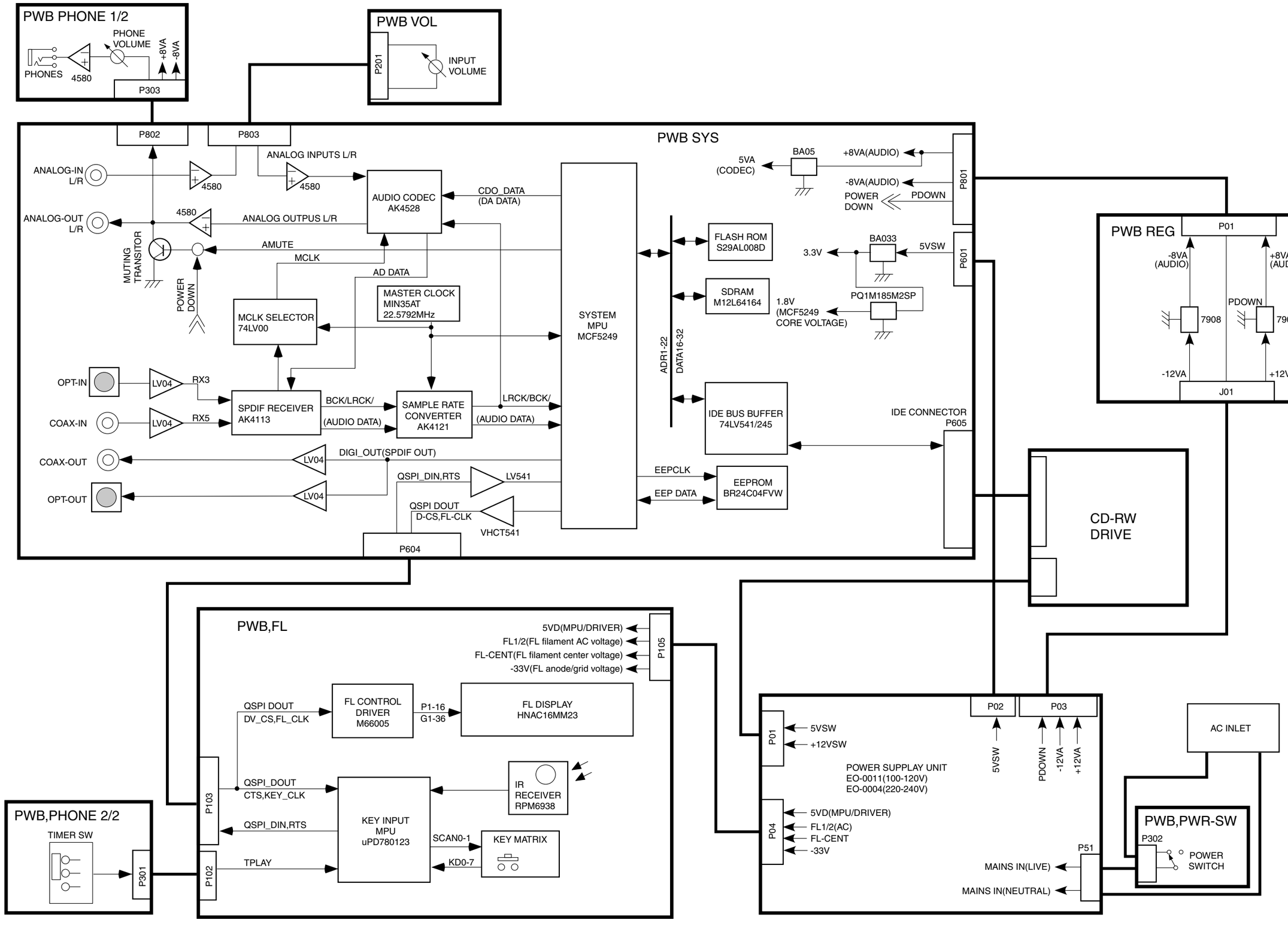
7. Wiring Diagram



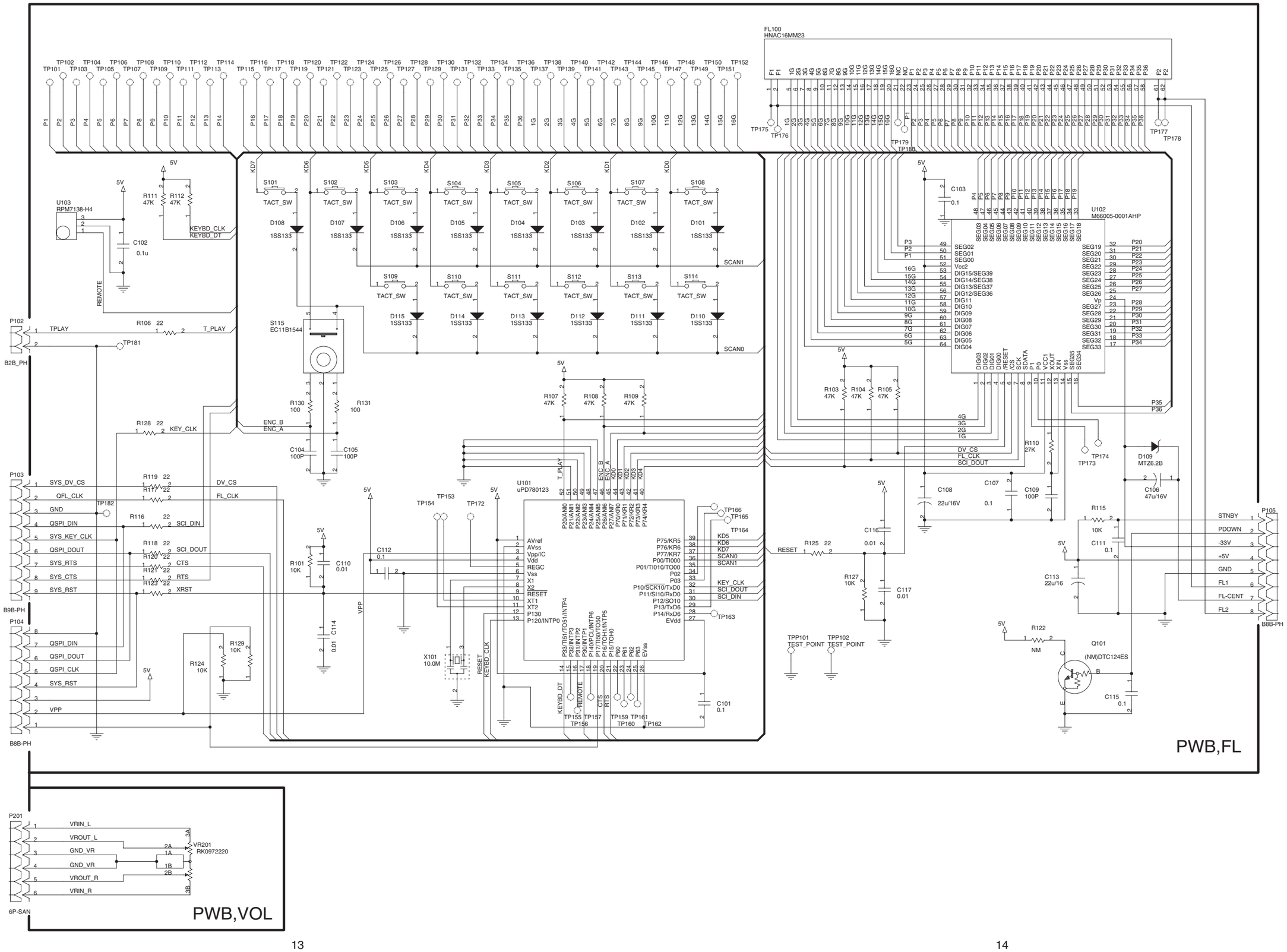
P604-P103 signal description

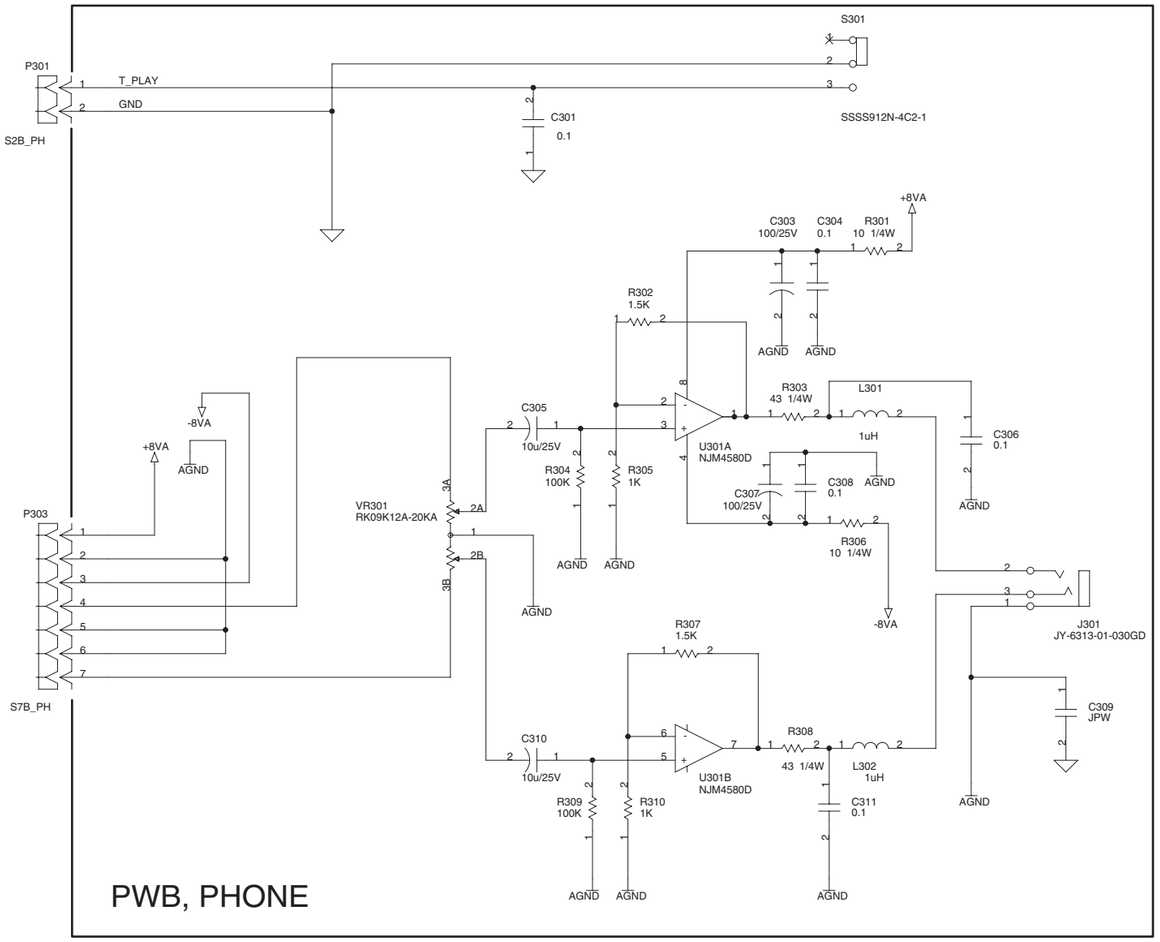
- DV_CS:FL CONTROLLER chip select
- SCI_CLK: SYS -> FL communication clock
- KEY_CLK: SYS -> KEY communication clock
- SCI_DIN: SYS <- KEY communication data
- SCI_DOUT: SYS -> KEY/FL communication data
- CTS_IN: SYS <- KEY communication handshake
- RTS_OUT: SYS -> KEY communication handshake
- XRST_S: SYS -> KEY/FL controller reset

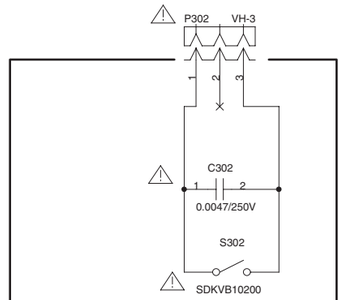
8. Block Diagram

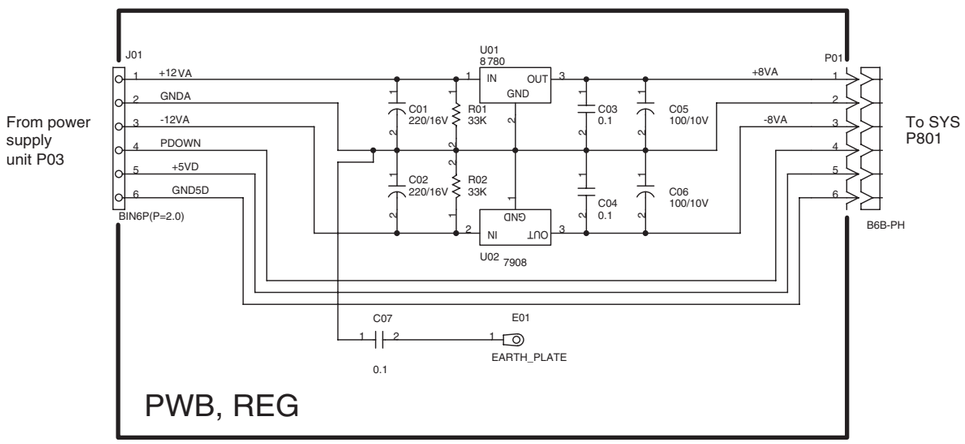


9. SCHEMATIC DIAGRAM




P301
T_PLAY
GND
S2B_PH
S301
SSSS912N-4C2-1
C301
0.1
+8VA
C303
100/25V
C304
0.1
R301
10 1/4W
R302
1.5K
AGND
R303
43 1/4W
L301
1uH
C305
10u/25V
U301A
NJM4580D
C306
0.1
-8VA
+8VA
AGND
R304
100K
R305
1K
C307
100/25V
C308
0.1
VR301
RK09K12A-20KA
3A
2A
2B
3B
R306
10 1/4W
P303
S7B_PH
J301
JY-6313-01-030GD
R307
1.5K
C309
JPW
C310
10u/25V
R308
43 1/4W
L302
1uH
U301B
NJM4580D
R309
100K
R310
1K
C311
0.1
PWB, PHONE


P302
VH-3
C302
0.0047/250V
S302
SDKVB10200
PWB, PWR-SW


From power supply unit P03
J01
+12VA
GNDA
-12VA
PDOWN
+5VD
GND5D
BIN6P(P=2.0)
U01
8780
IN
OUT
GND
C01
220/16V
R01
33K
C02
220/16V
R02
33K
C03
0.1
C04
0.1
C05
100/10V
C06
100/10V
+8VA
-8VA
P01
To SYS P801
B6B-PH
U02
7908
C07
0.1
E01
EARTH_PLATE
PWB, REG

PWB, SYS(1/3)
E902460-00B

P803 PH-6-RED — TO INPUT VOL UME PWB

INPUT LCH (L) — 3CB — R831 33K — C832 10/16V — U804A NJM4580V — C834 10/16V — R833 100 — TP830 TP831 TP832 TP833 TP834 TP835

INPUT RCH (R) — J801B RJ-1073-09-0320 A — 2BB — R931 33K — C932 10/16V — U804B NJM4580V — C934 10/16V — R933 100

G — 1AB

C833 33p — R832 47K — C830 10/16V — C831 10/16V — C933 33p — R932 47K

C843 0.001 — R845 68K — R846 220K — C943 0.001 — R945 68K — R946 220K

+8VA — -8VA

U805B NJM4580V — R836 1K — C836 33p — R834 47K — R835 2.2K — C835 10/16V

U805A NJM4580V — C837 10/16V — C838 10/16V — R837 10K F — R838 10K F — C839 10/16V — C840 10/16V — R839 330 F — R840 330 F

U905B NJM4580V — C935 10/16V — C936 33p — R936 1K — R934 47K — R935 2.2K

U905A NJM4580V — C937 10/16V — C938 10/16V — R937 10K F — R938 10K F — R940 330 F — R939 330 F — C940 10/16V — C939 10/16V

AUDIO_GND

+5VA — D830 1SS355 — D832 1SS355 — D831 1SS355 — D833 1SS355 — C841 0.001 — D931 1SS355 — D933 1SS355 — D930 1SS355 — D932 1SS355

R841 100K F — R842 100K F — R843 9.1K — R941 100K F — R942 100K F — C842 47/6.3V — R844 10K — AUDIO_GND

+8VA — TP807 TP808 TP809 TP820 TP821 — P802 B7B-PH-SM4 — To H/P

-8VA — R847 10K — R947 10K — AUDIO_GND

R863 0 — AUDIO_GND

+8VA — N.M.(RB161L-40) D853 — TP850 — +5VA — TP851

U801 BA05FP — IN NC GND OUT — R801 0 — C801 47/6.3V — C803 0.1 — C802 0.1 — AUDIO_GND

W902 SHORT_PAD — CODEC_GND

C807 0.1 — C806 10/16V — CODEC_GND

U802 AK4528 — VCOM AOUTR+ AINR+ AOUTR- AINL+ AOUTL+ AINL- AOUTL- VREF DGND AGND VD VA VT P/S DEM1 MCLK DEM0 LRCK PDN BICK DFS SDTO CSN SDTI CCLK CDTI

C804 10/16V — C805 0.1 — CODEC_GND — C811 (NM)10p

C810 0.1 — C809 0.1 — C808 10/16V — D3.3V — R803 47K — R804 100 — from mpu s ection GND — DIGITAL_GND

+5VA — R802 4.7 — D3.3V — R805 47K

R806 47K — R807 47K — R808 47K — R809 47K — DIGITAL_GND

MCLK — LRCK — BICK — DIF SECTION

DIF SECTION — AD_DATA — CDO_DATA

MPU SECTION — CODEC_DOUT — CODEC_CS — CODEC_CLK — CODEC_RST — DEMO1 — AMUTE — emphasis

R821 5.1K F — C812 10/16V — C822 470p — C823 10/16V — R820 4.7K F — R824 180 F — C821 0.033 — R822 4.7K F — R825 180 F — R823 5.1K F — C820 470p — C813 10/16V — U803A NJM4580V — R923 5.1K F — C819 0.033 — R922 4.7K F — R925 180 F — U803B NJM4580V — R920 4.7K F — R924 180 F — C818 0.033 — C922 470p — C923 10/16V — R921 5.1K F

R826 1K — R827 1K — Q820 2SC4213 — R828 4.7K — C824 0.1 — R829 100 — R830 100K — C825 0.001 — 3CA — L — OUTPUT Lch — 1AA — G — AUDIO_GND — C924 0.1 — Q920 2SC4213 — R928 4.7K — R927 1K — R926 1K — R929 100 — R930 100K — C925 0.001 — 2BA — R — OUTPUT Rch — J801A RJ-1073-09-032 0A

FRONT IF SECTION — ALL_RST — R862 0 — R861 22K — R860 3.3K — +8VA — C850 100/16V — C852 0.1 — C851 100/16V — C853 0.1 — W901 SHORT_PAD — AUDIO_GND — -8VA — R858 NM — +5VD — C854 (NM)100/16V — W903 SHORT_PAD — W904 OPEN_PAD — DIGITAL_GND — from mpu section GND

P801 — 1 +8VA — 2 GNDA — 3 -8VA — 4 PDOWN — 5 +5VD — 6 GND5D — TP801 TP802 TP803 TP804 TP805 TP806 — B6B-PH-SM4 — From power supply unit

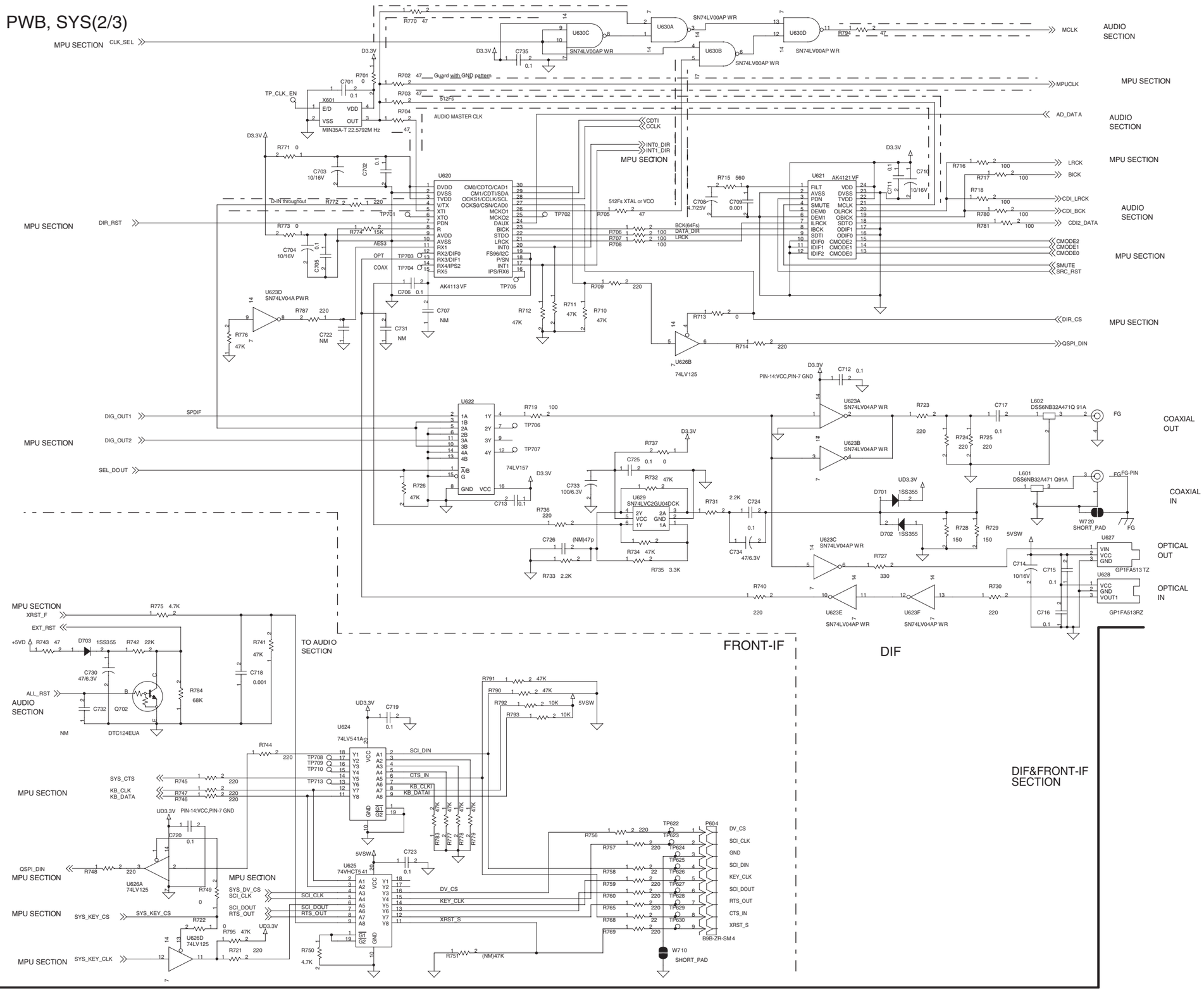
5VSW — C855 0.1 — U850 VDD VOUT ER SUB GND — BD46285G — R850 100 — C856 10/16V — D850 1SS355 — R856 2.2K — TP_MUTE — C857 (NM)0.01 — C858 0.01

+5VD — R851 47 — D851 1SS355 — +5VA — R852 NM — D852 (NM)1SS355 — C859 100/6.3V — R853 1.2K — from mp u sectio n GND

Q852 DTA124E UA — Q853 DTC124EUA — R854 NM — Q850 DTC124EUA — Q851 DTC124EUA — AUDIO_GND — R857 1K — R855 47K — C860 0.47/50V — R859 NM — -8VA

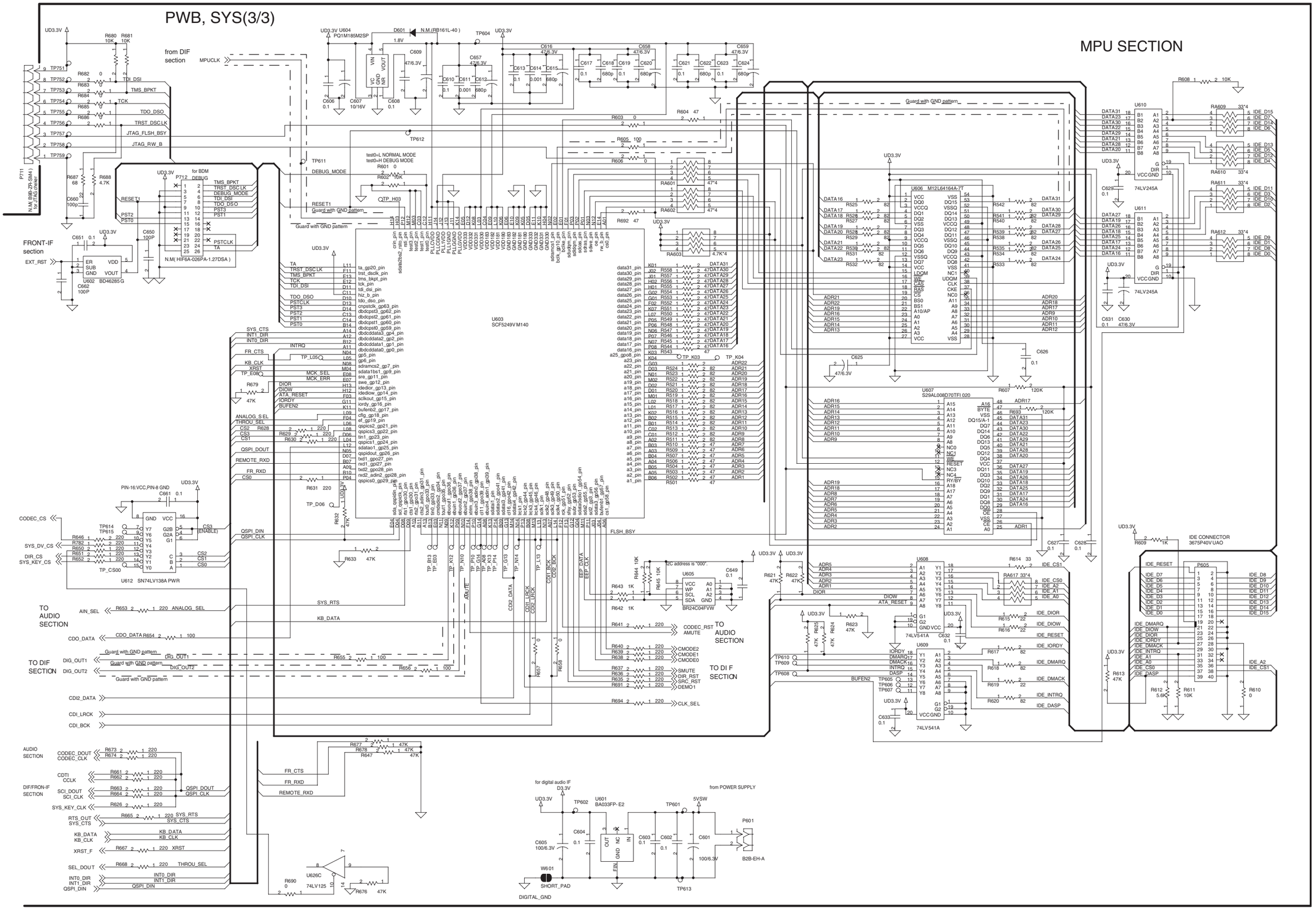
AUDIO SECTION

PWB, SYS(2/3)

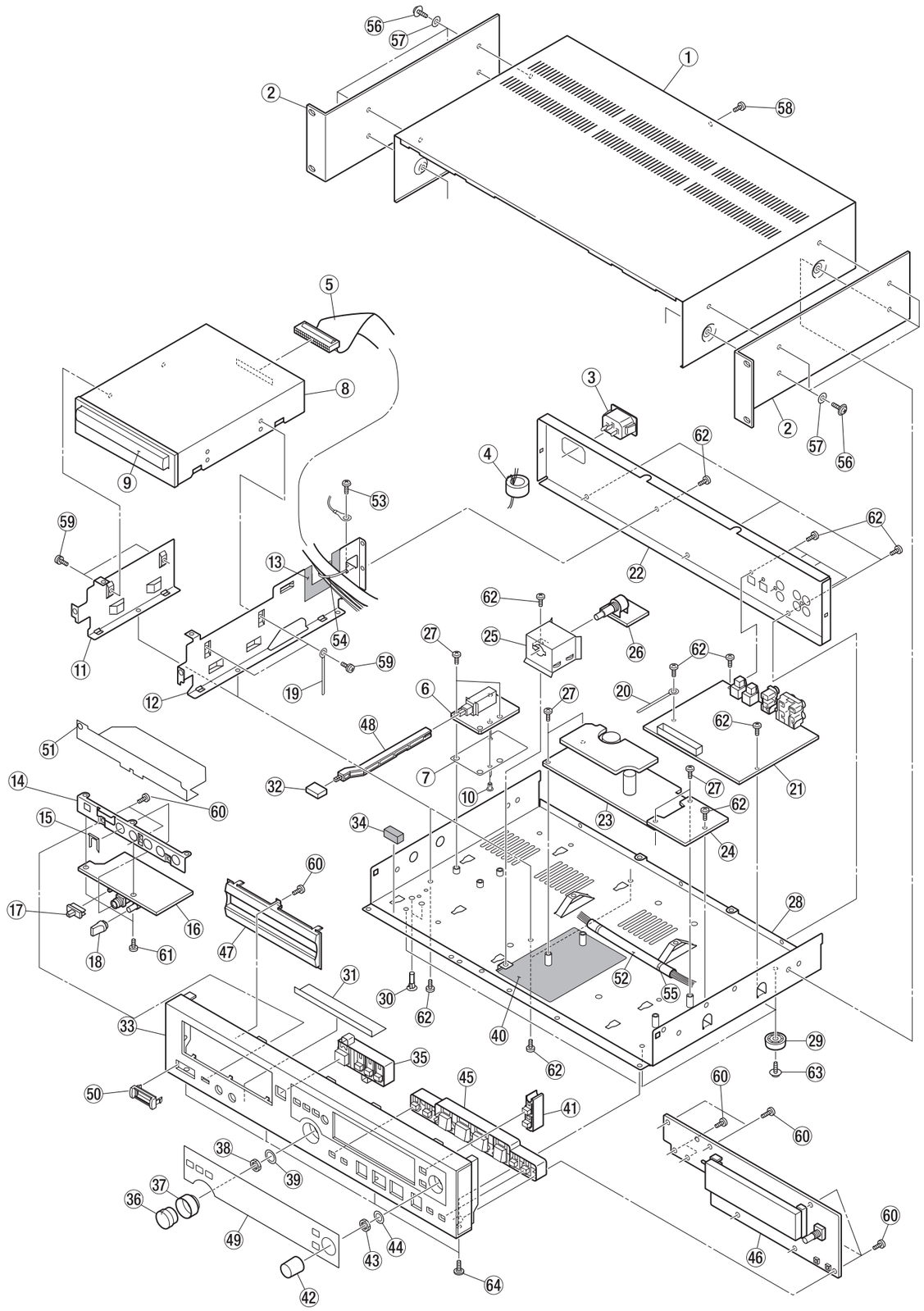

MPU SECTION
CLK_SEL
D3.3V
R770 47
U630A
U630B
U630C
U630D
SN74LV00AP WR
C735 0.1
MCLK
AUDIO SECTION
R794 47
R701 0
R702 47 Guard with GND pattern
R703 47
R704 47
512Fs
TP_CLK_EN
X601
E/D
VDD
VSS
OUT
MIN35A-T 22.5792M Hz
AUDIO MASTER CLK
MPUCLK
MPU SECTION
AD_DATA
C701 0.1
C702 0.1
C703 10/16V
R771 0
U620
CDTI
CCLK
INT0_DIR
INT1_DIR
DIR_RST
D-IN throughout
R772 220
TP701
TP702
512Fs XTAL or VCO
R705 47
C704 10/16V
C705 0.1
R773 0
R774 15K
AES3
OPT
COAX
TP703
TP704
TP705
AK4113VF
C706 0.1
C707 NM
C731 NM
C722 NM
R776 47K
U623D SN74LV04A PWR
R787 220
R712 47K
R711 47K
R710 47K
R709 220
R706 100
R707 100
R708 100
BCK(64Fs)
DATA_DIR
LRCK
U621 AK4121VF
R715 560
C708 4.7/25V
C709 0.001
C710 10/16V
C711 0.1
R716 100
R717 100
R718 100
R780 100
R781 100
LRCK
BICK
CDI_LRCK
CDI_BCK
CDI2_DATA
CMODE2
CMODE1
CMODE0
SMUTE
SRC_RST
R713 0
R714 220
U626B 74LV125
DIR_CS
QSPI_DIN
PIN-14:VCC,PIN-7 GND
C712 0.1
U623A SN74LV04AP WR
U623B SN74LV04AP WR
R723 220
R724 220
R725 220
C717 0.1
L602 DSS6NB32A471Q 91A
FG
COAXIAL OUT
DIG_OUT1
SPDIF
DIG_OUT2
SEL_DOUT
U622
74LV157
R719 100
TP706
TP707
R726 47K
C713 0.1
C733 100/6.3V
C725 0.1
R737 0
R732 47K
U629 SN74LVC2GU04DCK
R731 2.2K
C724 0.1
C734 47/6.3V
R736 220
C726 (NM)47p
R733 2.2K
R734 47K
R735 3.3K
L601 DSS6NB32A471 Q91A
FG-PIN
W720 SHORT_PAD
COAXIAL IN
D701 1SS355
D702 1SS355
R728 150
R729 150
5VSW
U623C SN74LV04AP WR
R727 330
U627 GP1FA513TZ
C714 10/16V
C715 0.1
U628 GP1FA513RZ
C716 0.1
OPTICAL OUT
OPTICAL IN
R740 220
U623E SN74LV04AP WR
U623F SN74LV04AP WR
R730 220
DIF
MPU SECTION
XRST_F
EXT_RST
+5VD
R743 47
D703 1SS355
R742 22K
R741 47K
C718 0.001
ALL_RST
AUDIO SECTION
C730 47/6.3V
C732 NM
Q702 DTC124EUA
R784 68K
TO AUDIO SECTION
FRONT-IF
R775 4.7K
R791 47K
R790 47K
R792 10K
R793 10K
5VSW
UD3.3V
C719 0.1
U624 74LV541A
R744 220
SCI_DIN
CTS_IN
KB_CLKI
KB_DATAI
SYS_CTS
KB_CLK
KB_DATA
R745 220
R747 220
R746 220
TP708
TP709
TP710
TP713
R763 47K
R777 47K
R778 47K
R779 47K
C720 0.1
U626A 74LV125
R748 220
R749 0
QSPI_DIN
U625 74VHCT541
C723 0.1
SYS_DV_CS
SCI_CLK
SCI_DOUT
RTS_OUT
SYS_KEY_CS
SYS_KEY_CLK
R722 0
R795 47K
U626D 74LV125
R721 220
R750 4.7K
R751 (NM)47K
DV_CS
KEY_CLK
XRST_S
R756 220
R757 220
R758 22
R759 220
R760 220
R765 220
R768 220
R769 220
TP622
TP623
TP624
TP625
TP626
TP627
TP628
TP629
TP630
P604
B9B-ZR-SM4
W710 SHORT_PAD
DV_CS
SCI_CLK
GND
SCI_DIN
KEY_CLK
SCI_DOUT
RTS_OUT
CTS_IN
XRST_S
DIF&FRONT-IF SECTION

PWB, SYS(3/3)

MPU SECTION



10. EXPLODED VIEW AND PARTS LIST

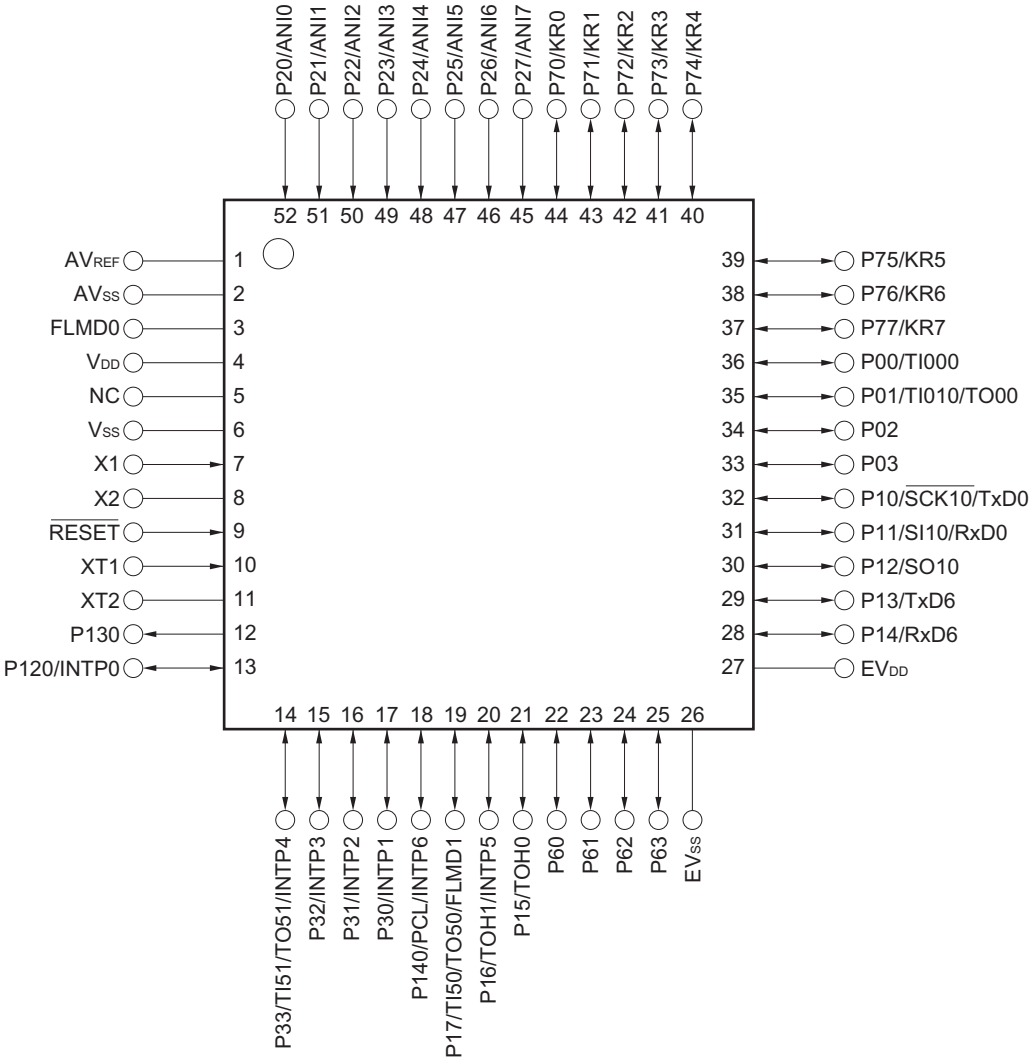


POS. NO.	VERS. COLOR	PART NO. (FOR EUR)	PART NO. (MZ)	PART NAME	DESCRIPTION	
⚠ 3		90M-YT004790R	90M-YT004790R	TERMINAL	MAINS INLET,3 POLE M1816	5332030400
6,16		90M-ZZ003340R	90M-ZZ003340R	PWB ASSY	GATHER PCBA,PHN-PW 632	E95256000A
8		90M42AZ304010	90M42AZ304010	MECHANISM	MECH LOADER AND MECH TRAVERSE CD-W58DB-T05	1L77156T05
9		90M42AZ063010	90M42AZ063010	ESCUTCHEON	PANEL,TRAY 632 G	M02038110B
15		nsp	nsp	BRACKET	MOUNT PLATE JACK G	3E011630
17		90M42AZ154020	90M42AZ154020	KNOB	KNOB,SLIDE(B) MD-5B G	3M0057400A
18		90M42AZ154010	90M42AZ154010	KNOB	KNOB,PHONE VOLUME AD500 G	3M0024800A
21		90M-ZZ003320R	90M-ZZ003320R	PWB ASSY	PCB ASSY,SYS CDR632	E95246010A
22	/N1B	nsp	nsp	PANEL	REAR PANEL,EUR-Y 632 G	M02237401A
22	/U1B	nsp	nsp	PANEL	REAR PANEL,UL 632 G	M02237400A
23-2	/N1B	90M-ZZ003360R	90M-ZZ003360R	PWB ASSY	SW RGLTD PS,EO-0004 EUR	E00646800B
23-1	/U1B	nsp	90M-ZZ003370R	PWB ASSY	SW RGLTD PS,EO-0011 UL	E00989200B
24		90M-ZZ003350R	90M-ZZ003350R	PWB ASSY	GATHER PCBA,REG CDR632	E95259700A
26,46		90M-ZZ003330R	90M-ZZ003330R	PWB ASSY	GATHER PCBA,FRONT CDR632	E95255900A
29		90M42AZ057010	90M42AZ057010	LEG	FOOT,21MM G	3M001950
32		90M42AZ270040	90M42AZ270040	BUTTON	BUTTON,POWER FLAT 632 G	M01891201A
33		90M42AZ248010	90M42AZ248010	PANEL	FRONT PANEL,(V0) 632 G	M02237300C
35		90M42AZ270020	90M42AZ270020	BUTTON	BUTTON,OPCLS 632 G	M02237800B
36		90M42AZ154040	90M42AZ154040	KNOB	KNOB,REC(R) 632 G	M02238100B
37		90M42AZ154030	90M42AZ154030	KNOB	KNOB,REC(L) 632 G	M02238000B
41		90M42AZ270010	90M42AZ270010	BUTTON	BUTTON,MENU 632 G	M02237700A
42		90M42AZ154050	90M42AZ154050	KNOB	KNOB,D17 632 G	M01335501A
45		90M42AZ270030	90M42AZ270030	BUTTON	BUTTON,OPE 632 G	M02237900B
47		90M42AZ063020	90M42AZ063020	ESCUTCHEON	ESCUTCHEON,FRONT 632 G	M02237500B
48		90M42AZ121010	90M42AZ121010	LINK	LINK,PWRSW CD1U G	M02138000B
49		90M42AZ158010	90M42AZ158010	WINDOW	WINDOW,FL 632 G	M02237600A
50		90M42AZ063030	90M42AZ063030	ESCUTCHEON	ESCUTCHEON,PWR FLAT 632 G	M01890701A
⚠ F1		90M-FS001340R	90M-FS001340R	FUSE	FUSE T2A L 250V SLOW BLOW	V0014130
J620		90M-YT004810R	90M-YT004810R	TERMINAL	JACK,RJ-1060A-31-0341A G	3E017600
J801		90M-YT004800R	90M-YT004800R	TERMINAL	JACK,RJ-1073B-09-0320A G	3E010590
U627		90M-YJ002990R	90M-YJ002990R	OPT CONN.	IC,GP1FA513TZOF G	3S035390G
U628		90M-YJ003000R	90M-YJ003000R	OPT CONN.	IC,GP1FA513RZOF G	3S035750G
PACKING						
		90M42AZ851010	90M42AZ851010	USER GUIDE	USER GUIDE,MULT1 632 G	D00884100A
		90M-ZK000570R	90M-ZK000570R	UNIT KIT	REMOTE CONTROLLER RC632 G	E01105400A
⚠	/N1B	90M-ZC000520R	90M-ZC000520R	MAINS CORD	MAINS CORD,EUR-G	3E014160
⚠	/U1B	nsp	90M-ZC000510R	MAINS CORD	MAINS CORD,UL-G	3E014150
NOT STANDARD SPARE PART						
		nsp	90M42AZ801010	PACKING CASE	PACKING CASE,INNER 632 G	M02238200A
		nsp	90M42AZ809010	CUSHION	CUSHION (L) RW800 G	3M0095600C
		nsp	90M42AZ809020	CUSHION	CUSHION (R) RW800 G	3M0095700B
		nsp	90M42AZ809030	CUSHION	CUSHION ADD RW800 G	3M0101400A
	/N1B	nsp	90M42AZ805020	MASS CARTON	CARTON BOX,OUTER T/C 632	M02238320A
	/U1B	nsp	90M42AZ805010	MASS CARTON	CARTON BOX,OUTER 632 G	M02238300A
1		nsp	90M42AZ257010	LID	TOP COVER RW800B G	3M0058120C
2		nsp	90M42AZ253010	HANDLE	RACK MOUNT ANGLE 632 G	3M0073230A

NOTE : "nsp" PART IS LISTED FOR REFERENCE ONLY, MARANTZ WILL NOT SUPPLY THESE PARTS.

11. MICROPROCESSOR AND IC DATA

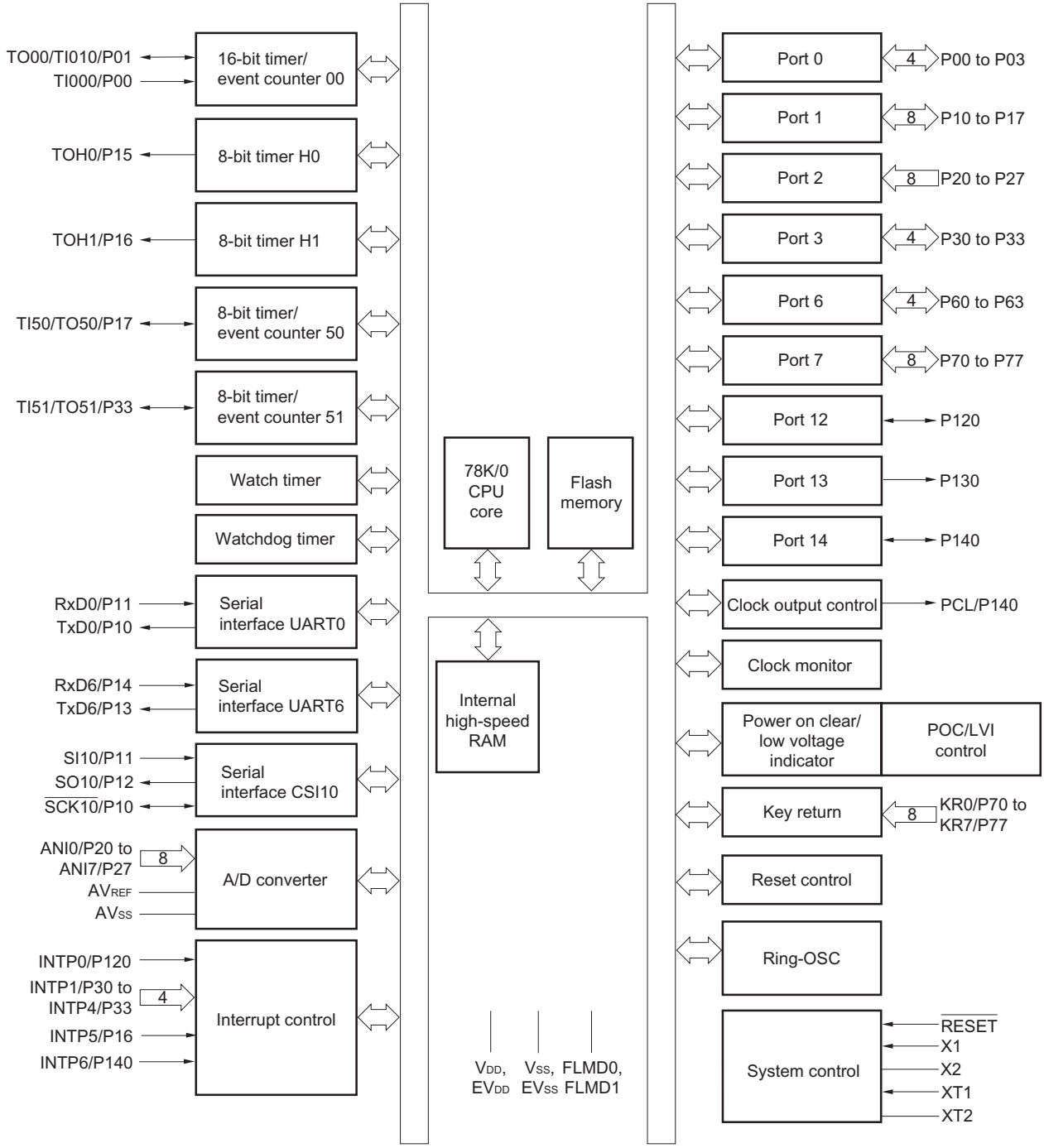
U101 : µPD78F0123H



Pin Identification

ANI0 to ANI7:	Analog input	P130:	Port 13
AVREF:	Analog reference voltage	P140:	Port 14
AVSS:	Analog ground	PCL:	Programmable clock output
EVDD:	Power supply for port	RESET:	Reset
EVSS:	Ground for port	RxD0, RxD6:	Receive data
FLMD0, FLMD1:	Flash programming mode	SCK10:	Serial clock input/output
INTP0 to INTP6:	External interrupt input	SI10:	Serial data input
KR0 to KR7:	Key return	SO10:	Serial data output
NC:	Non-connection	TI000, TI010,TI50, TI51:	Timer input
P00 to P03:	Port 0	TO00, TO50, TO51,	
P10 to P17:	Port 1	TOH0, TOH1:	Timer output
P20 to P27:	Port 2	TxD0, TxD6:	Transmit data
P30 to P33:	Port 3	VDD:	Power supply
P60 to P63:	Port 6	VSS:	Ground
P70 to P77:	Port 7	X1, X2:	Crystal oscillator (high-speed system clock)
P120:	Port 12	XT1, XT2:	Crystal oscillator (subsystem clock)

U101 : µPD78F0123H



U101 : µPD78F0123H

(1) Port pins

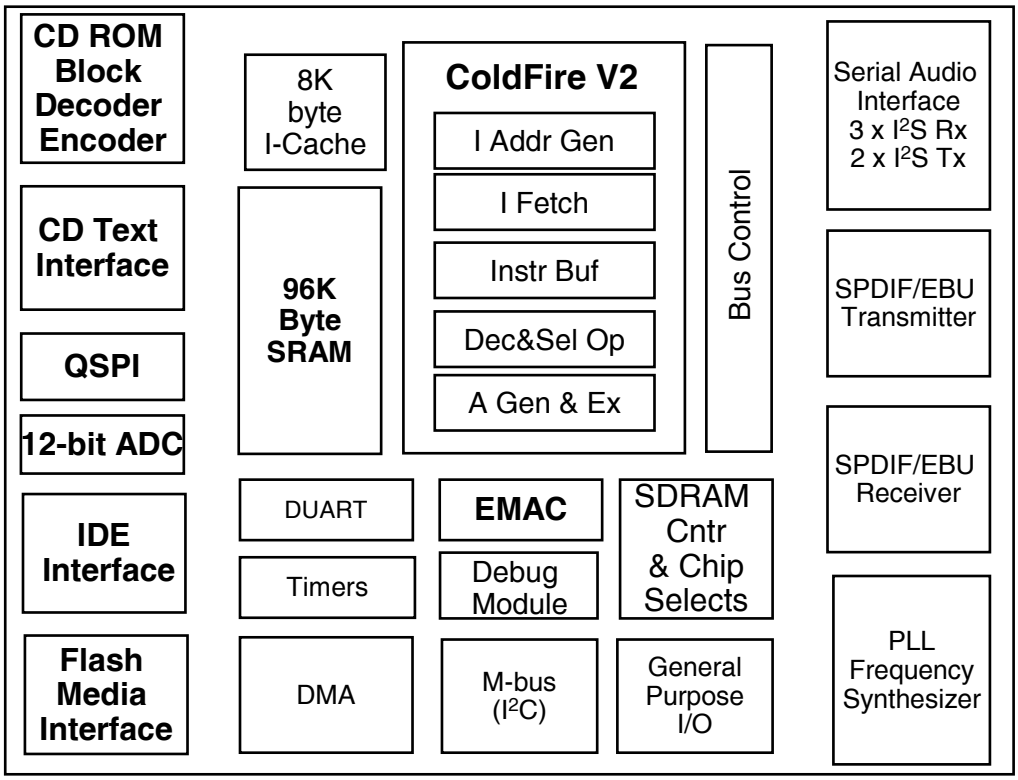
Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	TI000
P01				TI010/TO00
P02				–
P03				–
P10	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	$\overline{\text{SCK10}}$/TxD0
P11				SI10/RxD0
P12				SO10
P13				TxD6
P14				RxD6
P15				TOH0
P16				TOH1/INTP5
P17				TI50/TO50/FLMD1
P20 to P27	Input	Port 2. 8-bit input-only port.	Input	ANI0 to ANI7
P30 to P32	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	INTP1 to INTP3
P33				INTP4/TI51/TO51
P60 to P63	I/O	Port 6. 4-bit I/O port (N-ch open drain). Input/output can be specified in 1-bit units.	Input	–
P70 to P77	I/O	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	KR0 to KR7
P120	I/O	Port 12. 1-bit I/O port. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	INTP0
P130	Output	Port 13. 1-bit output-only port.	Output	–
P140	I/O	Port 14. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	PCL/INTP6

U101 : µPD78F0123H

(2) Non-port pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P120
INTP1 to INTP3				P30 to P32
INTP4				P33/TI51/TO51
INTP5				P16/TOH1
INTP6				P140/PCL
SI10	Input	Serial data input to serial interface	Input	P11/RxD0
SO10	Output	Serial data output from serial interface	Input	P12
$\overline{SCK10}$	I/O	Clock input/output for serial interface	Input	P10/TxD0
RxD0	Input	Serial data input to asynchronous serial interface	Input	P11/SI10
RxD6				P14
TxD0	Output	Serial data output from asynchronous serial interface	Input	P10/$\overline{SCK10}$
TxD6				P13
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00	Input	P00
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P01/TO00
TO00	Output	16-bit timer/event counter 00 output	Input	P01/TI010
TI50	Input	External count clock input to 8-bit timer/event counter 50	Input	P17/TO50/FLMD1
TI51		External count clock input to 8-bit timer/event counter 51		P33/TO51/INTP4
TO50	Output	8-bit timer/event counter 50 output	Input	P17/TI50/FLMD1
TO51		8-bit timer/event counter 51 output		P33/TI51/INTP4
TOH0		8-bit timer H0 output		P15
TOH1		8-bit timer H1 output		P16/INTP5
PCL	Output	Clock output (for trimming of high-speed system clock, subsystem clock)	Input	P140/INTP6
ANI0 to ANI7	Input	A/D converter analog input	Input	P20 to P27
AV_{REF}	Input	A/D converter reference voltage input and positive power supply for port 2	–	–
AV_{SS}	–	A/D converter ground potential. Make the same potential as EV_{SS} or V_{SS}.	–	–
KR0 to KR7	Input	Key interrupt input	Input	P70 to P77
$\overline{RESET}$	Input	System reset input	–	–
X1	Input	Connecting resonator for high-speed system clock	–	–
X2	–		–	–
XT1	Input	Connecting resonator for subsystem clock	–	–
XT2	–		–	–
V_{DD}	–	Positive power supply (except for ports)	–	–
EV_{DD}	–	Positive power supply for ports	–	–
V_{SS}	–	Ground potential (except for ports)	–	–
EV_{SS}	–	Ground potential for ports	–	–
FLMD0	–	Flash memory programming mode setting.	–	–
FLMD1			Input	P17/TI50/TO50
NC	–	Not internally connected. Leave open.	–	–

U603 : SCF5249



144 QFP Pin Number	Name	Type	Description
01	SCL/QSPI_CLK	I/O	IIC clock/QSPI clock pin function select is PLLCR(11)
02	CS0	O	static chip select 0
03	A21	O	SDRAM address / static adr
04	A11	O	SDRAM address / static adr
05	A10	O	SDRAM address / static adr
06	A9	O	SDRAM address / static adr
07	A18	O	SDRAM address / static adr
08	A17	O	SDRAM address / static adr
09	BCLK/GPIO10	I/O	sdram clock output

U603 : SCF5249

144 QFP Pin Number	Name	Type	Description
10	SCLK_OUT/GPIO15	I/O	MemoryStick/SD
11	BCLKE	O	sdram clock enable output
12	SDA/QSPI_DIN	I/O	IIC data/QSPI data in function select is PLLCR(11)
13	DATA24	I/O	data
14	A22	O	SDRAM address / static adr
15	SDUDQM	O	SDRAM UDQM
16	EF/GPIO19	I/O	error flag input
17	DATA25	I/O	data
18	DATA26	I/O	data
19	DATA27	I/O	data
20	PAD-GND		PAD-GND
21	DATA28	I/O	data
22	DATA29	I/O	data
23	SDATA3/GPIO56	I/O	SD interface data line
24	DATA30	I/O	data
25	BUFENB1/GPIO57	I/O	external buffer 1 enable
26	DATA31	I/O	data
27	CORE-VDD		CORE-VDD
28	A13	O	SDRAM address / static adr
29	CORE-GND		CORE-GND
30	A23	O	SDRAM address / static adr
31	A14	O	SDRAM address / static adr
32	A15	O	SDRAM address / static adr
33	A16	O	SDRAM address / static adr
34	PAD-VDD		PAD-VDD
35	A19	O	SDRAM address / static adr

U603 : SCF5249

144 QFP Pin Number	Name	Type	Description
36	A20	O	SDRAM address / static adr
37	TEST2	I	test
38	SDRAM-CS1	O	SDRAM chip select out 1
39	SDATA1_BS1/GPIO9	I/O	Memory Stick / SD
40	SDRAS	O	SDRAM RAS
41	SDCAS	O	SDRAM CAS
42	SDWE	O	SDRAM write enable
43	SDLDQM	O	SDRAM LDQM
44	GPIO5	I/O	GPIO5
45	QSPI_CS0/GPIO29	I/O	QSPI chip select 0
46	QSPI_DOUT/GPIO26	I/O	QSPI data out
47	GPIO6	I/O	GPIO6
48	DATA21	I/O	data
49	DATA19	I/O	data
50	QSPI_CS2/GPIO21	I/O	QSPI chip select 2
51	DATA20	I/O	data
52	DATA22	I/O	data
53	DATA18	I/O	data
54	DATA23	I/O	data
55	DATA17	I/O	data
56	PADD-VDD		PAD-VDD
57	DATA16	I/O	data
58	CFLG/GPIO18	I/O	CFLG input
59	EBUOUT1/GPO36	O	audio interfaces EBU out 1
60	CORE-GND		CORE-GND
61	EBUIN3/ADIN0/GPI38	I	audio interfaces EBU in 3 / AD convertor input0

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144 QFP Pin Number	Name	Type	Description
62	EBUIN2/GPI37	I	audio interfaces EBU in 2
63	CORE-VDD		CORE-VDD
64	SCL2/GPIO3	I/O	IIS2 clock line
65	RSTI	I	Reset
66	TOUT1/ADOUT/GPO35	O	timer output 1 / AD output
67	LRCK2/GPIO44	O	audio interfaces EBU out 1
68	OE	O	Output Enable
69	SDA2/GPIO55	I/O	IIS2 data
70	SDATAO2/GPO41	O	audio interfaces serial data output 2
71	SCLK2/GPIO48	I/O	audio interfaces serial clock 2
72	PAD-GND		PAD-GND
73	TEST3	I	test
74	SDATAO1/GPIO25	I/O	audio interfaces serial data output 1
75	LRCK1	I/O	audio interfaces word clock 1
76	LRCK4/GPIO46	I/O	audio interfaces word clock 4
77	SDATAI4/GPI42	I	audio interfaces serial data in 4
78	SCLK1	I/O	audio interfaces serial clock 1
79	SCLK4/GPIO50	I/O	audio interfaces serial clock 4
80	TA/GPIO20	I/O	Transfer acknowledge
81	SDATAI1	I	audio interfaces serial data in 1
82	EBUIN1/GPI36	I	audio interfaces EBU in 1
83	PLLGRDVDD		PLLGRDVDD
84	PLLGRDGND		PLLGRDGND
85	PLLPADGND		PLLPADGND
86	PLLPADVDD		PLLPADVDD
87	PLLCOREGND		PLLCOREGND
88	PLLCOREVDD		PLLCOREVDD

U603 : SCF5249

144 QFP Pin Number	Name	Type	Description
89	IDE-DIOW/GPIO14	I/O	ide diow
90	CRIN	I	crystal
91	IDE-DIOR/GPIO13	I/O	ide dior
92	IDE-IORDY/GPIO16	I/O	ide iordy
93	MCLK1/GPO39	O	Audio master clock output 1
94	MCLK2/GPO42	O	Audio master clock output 2
95	XTRIM/GPO38	O	audio interfaces X-tal trim
96	TRST/DSCLK	I	Debug / interrupt monitor output 2
97	CORE-VDD		CORE-VDD
98	RW_B	O	Bus write enable
99	TMS/BKPT	I	JTAG/debug
100	CORE-GND		CORE-GND
101	TCK	I	JTAG
102	PAD-GND		PAD-GND
103	PST3/GPIO62	I/O	debug
104	CNPSTCLK/GPO63	O	debug
105	PST1/GPIO60	I/O	debug
106	PAD-VDD		PAD-VDD
107	PST2/GPIO61	I/O	debug
108	PST0/GPIO59	I/O	debug
109	TDI/DSI	I	jtag/debug
110	TEST0	I	test
111	TIN0/GPI33	I	timer input 0
112	HI-Z	I	jtag
113	DDATA3/GPIO4	I/O	debug
114	TOUT0/GPO33	O	timer output 0
115	DDATA1/GPIO1	I/O	debug

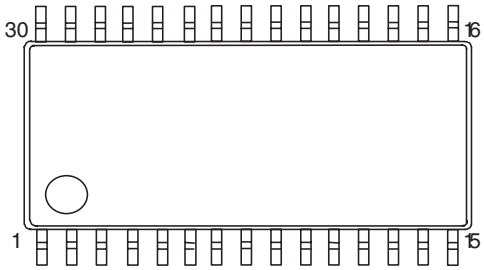
U603 : SCF5249

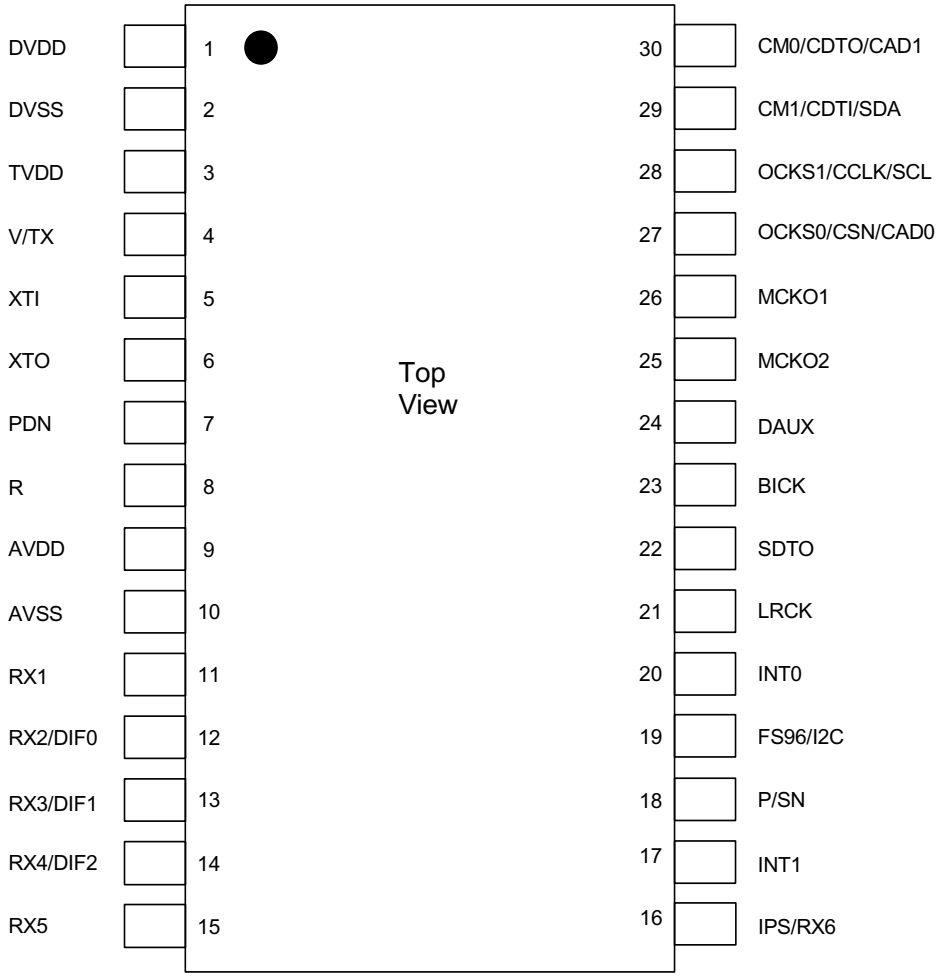
144 QFP Pin Number	Name	Type	Description
116	DDATA2/GPIO2	I/O	debug
117	CTS2_B/ADIN3/GPI31	I	second UART clear / AD input 3
118	DDATA0/GPIO0	I/O	debug
119	RXD2/GPI28/ADIN2	I	second UART receive data input / AD input 2
120	TDSO	O	JTAG/debug
121	RTS2_B/GPO31	O	second UART request to send
122	SDATAI3/GPI41	I	audio interfaces serial data input 3
123	CTS1_B/GPI30	I	first UART clear to send
124	TXD2/GPO28	O	second UART transmit data output
125	RTS1_B/GPO30	O	first UART request to send
126	EBUIN4/ADIN1/GPI39	I	audio interfaces EBU input 4 / AD input 1
127	TXD1/GPO27	O	first UART transmit data output
128	128 RXD1/GPI27	I	first UART receive data input
129	CS1/GPIO58	I/O	chip select 1
130	CORE-GND		CORE-GND
131	A1	O	SDRAM address / static adr
132	TIN1/GPIO23	I/O	Timer input 1
133	A2	O	address
134	A3	O	address
135	PAD-GND		PAD-GND
136	A4	O	address
137	A6	O	address
138	A5	O	address
139	A8	O	address
140	A7	O	address

U603 : SCF5249

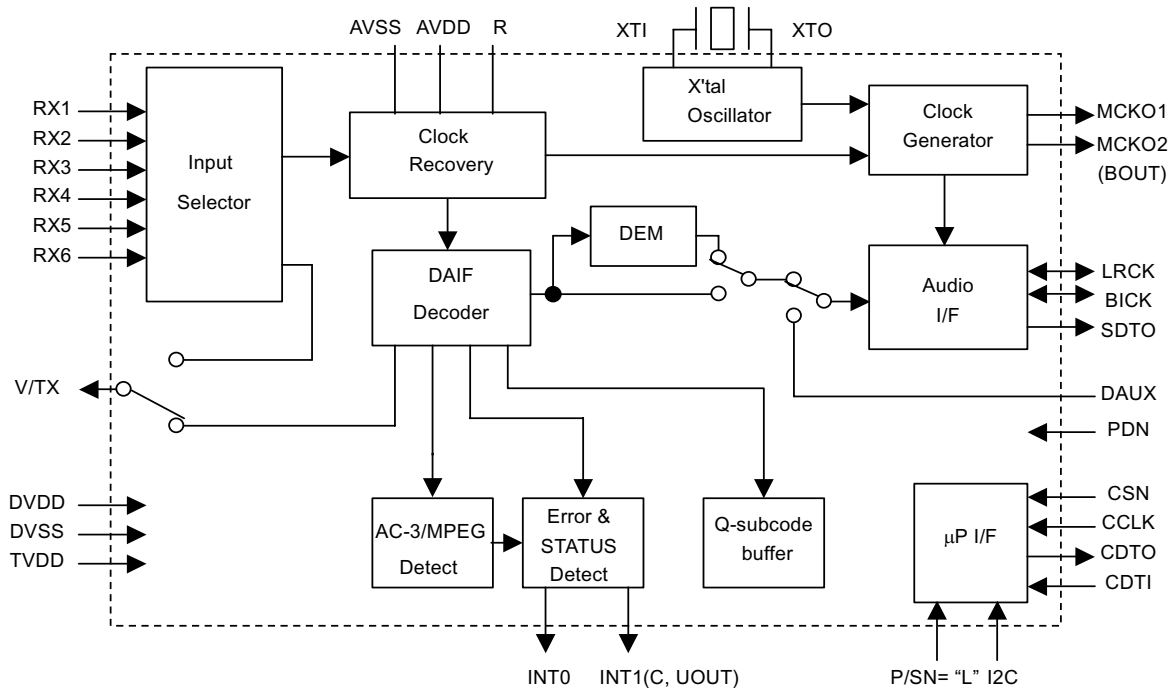
144 QFP Pin Number	Name	Type	Description
141	CORE-VDD		CORE-VDD
142	A12	O	address
143	TEST1	I	test
144	PAD-VDD		PAD-VDD

U620 : AK4113


30
16
1
15


DVDD 1
DVSS 2
TVDD 3
V/TX 4
XTI 5
XTO 6
PDN 7
R 8
AVDD 9
AVSS 10
RX1 11
RX2/DIF0 12
RX3/DIF1 13
RX4/DIF2 14
RX5 15
30 CM0/CDTO/CAD1
29 CM1/CDTI/SDA
28 OCKS1/CCLK/SCL
27 OCKS0/CSN/CAD0
26 MCKO1
25 MCKO2
24 DAUX
23 BICK
22 SDTO
21 LRCK
20 INT0
19 FS96/I2C
18 P/SN
17 INT1
16 IPS/RX6
Top
View

U620 : AK4113


AVSS
AVDD
R
XTI
XTO
X'tal
Oscillator
Clock
Generator
MCKO1
MCKO2
(BOUT)
RX1
RX2
RX3
RX4
RX5
RX6
Input
Selector
Clock
Recovery
DEM
DAIF
Decoder
Audio
I/F
LRCK
BICK
SDTO
V/TX
DAUX
PDN
DVDD
DVSS
TVDD
AC-3/MPEG
Detect
Error &
STATUS
Detect
Q-subcode
buffer
µP I/F
CSN
CCLK
CDTO
CDTI
INT0
INT1(C, UOUT)
P/SN= “L” I2C

U620 : AK4113

No.	Pin Name	I/O	Function
1	DVDD	-	Digital Power Supply Pin, 3.3V
2	DVSS	-	Digital Ground Pin
3	TVDD	-	Input Buffer Power Supply Pin, 3.3V or 5V
4	V	O	Validity Flag Output Pin in Parallel control mode
	TX	O	Transmit channel (Through data) Output Pin in serial control mode
5	XTI	I	X'tal Input Pin
6	XTO	O	X'tal Output Pin
7	PDN	I	Power-Down Mode Pin When "L", the AK4113 is powered-down and reset.
8	R	-	External Resistor Pin This pin must be connected to AVSS via 15kΩ ±5% resistor.
9	AVDD	-	Analog Power Supply Pin
10	AVSS	-	Analog Ground Pin
11	RX1	I	Receiver Channel #1 Pin (Internal Biased Pin)
12	DIF0	I	Audio Data Interface Format #0 Pin in parallel control mode
	RX2	I	Receiver Channel #2 Pin in serial control mode (Internal Biased Pin)
13	DIF1	I	Audio Data Interface Format #1 Pin in parallel control mode
	RX3	I	Receiver Channel #3 Pin in serial control mode (Internal Biased Pin)
14	DIF2	I	Audio Data Interface Format #2 Pin in parallel control mode
	RX4	I	Receiver Channel #4 Pin in serial control mode (Internal Biased Pin)
15	RX5	I	Receiver Channel #5 Pin (Internal Biased Pin)
16	IPS	I	Input Channel Select Pin in parallel control mode
	RX6	I	Receiver Channel #6 Pin (Internal Biased Pin)
17	INT1	O	Interrupt #1 Pin (when BCU bit = "0")
			U-bit Output Pin (when BCU bit = "1", UCE bit = "0")
			C-bit Output Pin (when BCU bit = "1", UCE bit = "1")
18	P/SN	I	Parallel/Serial Select Pin "L": Serial control mode, "H": Parallel control mode
19	FS96	O	96kHz Sampling Detect Pin in parallel control mode This function is enabled when the input frequency of XTI is 24.576MHz. "L": fs=54kHz or less, "H": fs=64kHz or more
	I2C	I	I^2C Select Pin in Serial control mode. "L": 4-wire Serial, "H": I^2C
20	INT0	O	Interrupt #0 Pin
21	LRCK	I/O	Output Channel Clock Pin
22	SDTO	O	Audio Serial Data Output Pin
23	BICK	I/O	Audio Serial Data Clock Pin
24	DAUX	I	Auxiliary Audio Data Input Pin
25	MCKO2	O	Master Clock #2 Output Pin (when BCU bit = "0")
			Block Start Signal Output Pin (when BCU bit = "1")
26	MCKO1	O	Master Clock #1 Output Pin
27	OCKS0	I	Output Clock Select #0 Pin in parallel control mode
	CSN	I	Chip Select Pin in serial control mode, I2C pin = "L"
	CAD0	I	Chip Address #0 Pin in serial control mode, I2C pin = "H"

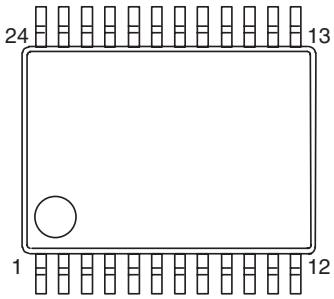
Note 1. Do not allow digital input pins expect internal biased pins (RX1-6 pins) to float.

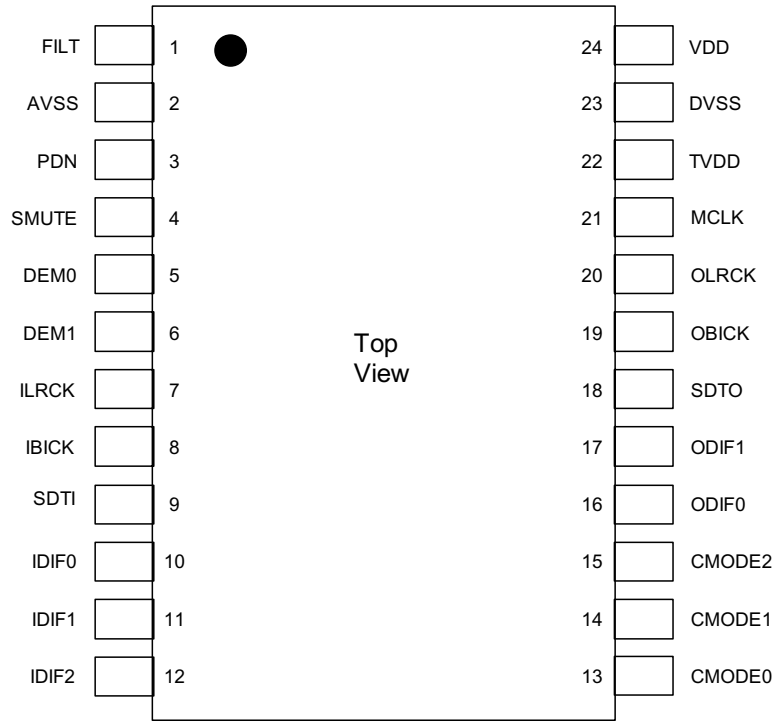
U620 : AK4113

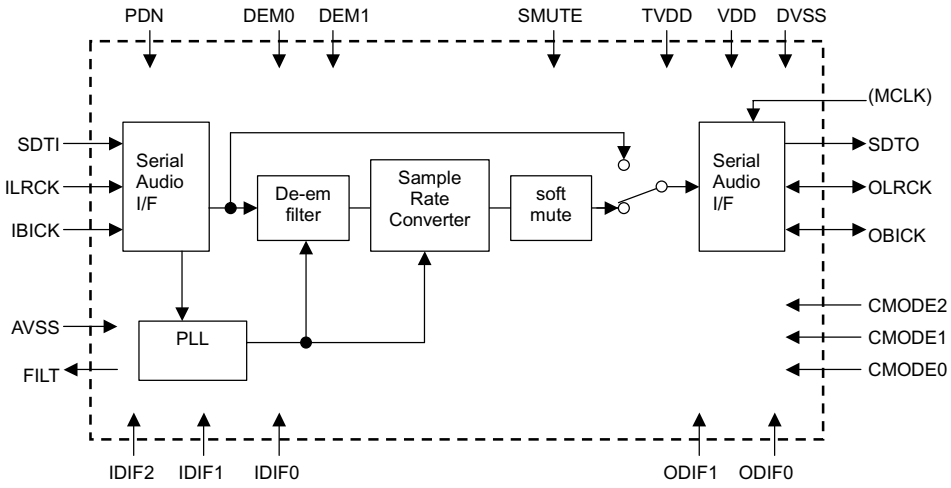
No.	Pin Name	I/O	Function
28	OCKS1	I	Output Clock Select #1 Pin in parallel control mode
	CCLK	I	Control Data Clock Pin in serial control mode, I2C pin = “L”
	SCL	I	Control Data Clock Pin in serial control mode, I2C pin = “H”
29	CM1	I	Master Clock Operation Mode #1 Pin in parallel control mode
	CDTI	I	Control Data Input Pin in serial control mode, I2C pin = “L”
	SDA	I/O	Control Data Pin in serial control mode, I2C pin = “H”
30	CM0	I	Master Clock Operation Mode #0 Pin in parallel control mode
	CDTO	O	Control Data Output Pin in serial control mode
	CAD1	I	Chip Address #1 Pin in serial control mode, I2C pin = “H”

Note 1. Do not allow digital input pins expect internal biased pins (RX1-6 pins) to float.

U621 : AK4121


24
13
1
12

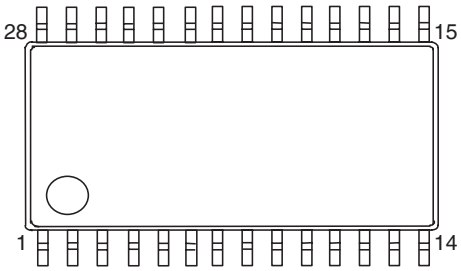

FILT 1
AVSS 2
PDN 3
SMUTE 4
DEM0 5
DEM1 6
ILRCK 7
IBICK 8
SDTI 9
IDIF0 10
IDIF1 11
IDIF2 12
24 VDD
23 DVSS
22 TVDD
21 MCLK
20 OLRCK
19 OBICK
18 SDTO
17 ODIF1
16 ODIF0
15 CMODE2
14 CMODE1
13 CMODE0
Top
View

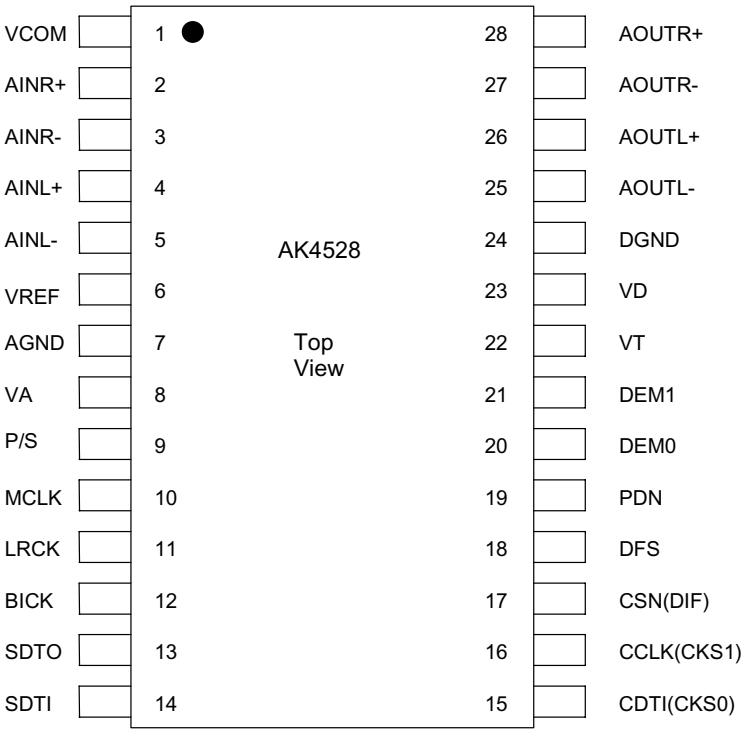

PDN
DEM0
DEM1
SMUTE
TVDD
VDD
DVSS
(MCLK)
SDTI
ILRCK
IBICK
Serial
Audio
I/F
De-em
filter
Sample
Rate
Converter
soft
mute
Serial
Audio
I/F
SDTO
OLRCK
OBICK
AVSS
FILT
PLL
CMODE2
CMODE1
CMODE0
IDIF2
IDIF1
IDIF0
ODIF1
ODIF0

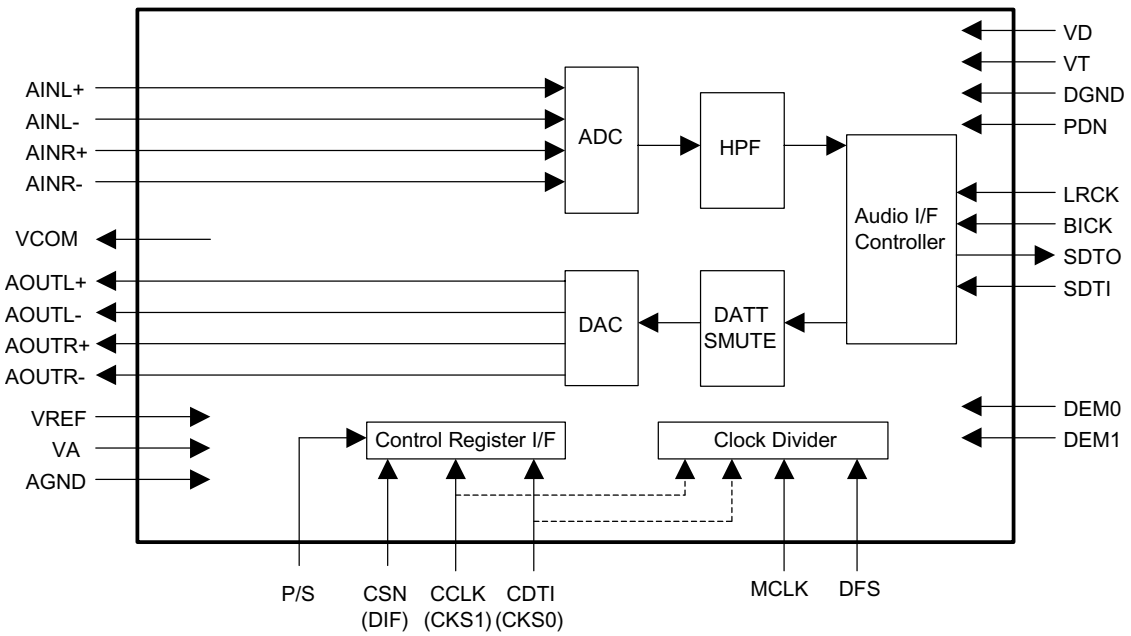
U621 : AK4121

No.	Pin Name	I/O	Function
1	FILT	O	Loop-Filter Pin for PLL
2	AVSS	I	Analog Ground Pin
3	PDN	I	Power-Down pin When “L”, the AK4121 is powered-down and reset.
4	SMUTE	I	Soft Mute Pin
5	DEM0	I	De-emphasis Filter Control Pin #0
6	DEM1	I	De-emphasis Filter Control Pin #1
7	ILRCK	I	L/R Clock Pin for Input
8	IBICK	I	Audio Serial Data Clock Pin for Input
9	SDTI	I	Audio Serial Data Input Pin
10	IDIF0	I	Input Data Format pin #0
11	IDIF1	I	Input Data Format pin #1
12	IDIF2	I	Input Data Format pin #2
13	CMODE0	I	Clock Mode Select Pin #0
14	CMODE1	I	Clock Mode Select Pin #1
15	CMODE2	I	Clock Mode Select Pin #2
16	ODIF0	I	Output Data Format pin #0
17	ODIF1	I	Output Data Format pin #1
18	SDTO	O	Audio Serial Data Output Pin
19	OBICK	I/O	Audio Serial Data Clock Pin for Output
20	OLRCK	I/O	L/R Clock Pin for Output
21	MCLK	I	Master Clock Pin for Output
22	TVDD	I	Input Buffer Power Supply Pin, 3.3V or 5V
23	DVSS	I	Digital Ground Pin
24	VDD	I	Power Supply Pin, 3.3V

U802 : AK4528


28
15
1
14


VCOM 1
AINR+ 2
AINR- 3
AINL+ 4
AINL- 5
VREF 6
AGND 7
VA 8
P/S 9
MCLK 10
LRCK 11
BICK 12
SDTO 13
SDTI 14
28 AOUTR+
27 AOUTR-
26 AOUTL+
25 AOUTL-
24 DGND
23 VD
22 VT
21 DEM1
20 DEM0
19 PDN
18 DFS
17 CSN(DIF)
16 CCLK(CKS1)
15 CDTI(CKS0)
AK4528
Top
View


AINL+
AINL-
AINR+
AINR-
VCOM
AOUTL+
AOUTL-
AOUTR+
AOUTR-
VREF
VA
AGND
ADC
HPF
DAC
DATT
SMUTE
Audio I/F
Controller
Control Register I/F
Clock Divider
VD
VT
DGND
PDN
LRCK
BICK
SDTO
SDTI
DEM0
DEM1
P/S
CSN
(DIF)
CCLK
(CKS1)
CDTI
(CKS0)
MCLK
DFS

U802 : AK4528

No.	Pin Name	I/O	Function
1	VCOM	O	Common Voltage Output Pin, VA/2 Bias voltage of ADC inputs and DAC outputs.
2	AINR+	I	Rch Positive Input Pin
3	AINR−	I	Rch Negative Input Pin
4	AINL+	I	Lch Positive Input Pin
5	AINL−	I	Lch Negative Input Pin
6	VREF	I	Voltage Reference Input Pin, VA Used as a voltage reference by ADC & DAC. VREF is connected externally to filtered VA.
7	AGND	-	Analog Ground Pin
8	VA	-	Analog Power Supply Pin, 4.75 ~ 5.25V
9	P/S	I	Parallel/Serial Mode Select Pin "L": Serial Mode, "H": Parallel Mode
10	MCLK	I	Master Clock Input Pin
11	LRCK	I	Input/Output Channel Clock Pin
12	BICK	I	Audio Serial Data Clock Pin
13	SDTO	O	Audio Serial Data Output Pin
14	SDTI	I	Audio Serial Data Input Pin
15	CDTI	I	Control Data Input Pin in Serial Mode
	CKS0	I	Master Clock Select Pin
16	CCLK	I	Control Data Clock Pin in Serial Mode
	CKS1	I	Master Clock Select Pin
17	CSN	I	Chip Select Pin in Serial Mode
	DIF	I	Digital Audio Interface Select Pin "L": 24bit MSB justified, "H": I^2S compatible
18	DFS	I	Double Speed Sampling Mode Pin
19	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initialize the control register.
20	DEM0	I	De-emphasis Control Pin
21	DEM1	I	De-emphasis Control Pin
22	VT	-	Output Buffer Power Supply Pin, 2.7 ~ 5.25V
23	VD	-	Digital Power Supply Pin, 4.75 ~ 5.25V
24	DGND	-	Digital Ground Pin
25	AOUTL−	O	Lch Negative Analog Output Pin
26	AOUTL+	O	Lch Positive Analog Output Pin
27	AOUTR−	O	Rch Negative Analog Output Pin
28	AOUTR+	O	Rch Positive Analog Output Pin

Note: All input pins should not be left floating.