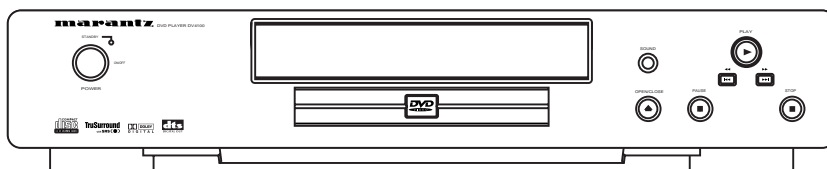


# Service Manual

DV4100/A1B, /N1B, /S1G, /U1B

DVD Player



## TABLE OF CONTENTS

1. TECHNICAL SPECIFICATION .....	1
2. CONNECTION FACILITIES .....	3
3. INFORMATIONS .....	4
4. SERVICING HINT .....	5
5. WARNING AND LASER SAFETY INSTRUCTIONS .....	6
6. SERVICE HINTS .....	8
7. BLOCK DIAGRAM .....	9
8. WIRING DIAGRAM .....	13
9. DISMANTLING INSTRUCTIONS .....	15
10. EXPLODED VIEW AND PARTS LIST .....	17
11. SCHEMATIC DIAGRAM AND PARTS LOCATION .....	21
12. TROUBLESHOOTING .....	47
13. DIAGNOSTIC SOFTWARE : SCRIPT INTERFACES .....	53
14. INTERACTIVE TESTS .....	55
15. TEST INSTRUCTIONS DISPLAY BOARD .....	62
16. CURRENT MODE POWER SUPPLY 20PS203 .....	64
17. CIRCUIT DESCRIPTIONS AND ABBREVIATIONS .....	68
18. ELECTRICAL PARTS LIST .....	70

Please use this service manual with referring to the user guide (D.F.U) without fail.

# marantz®

## DV4100

## MARANTZ DESIGN AND SERVICE

Using superior design and selected high grade components, **MARANTZ** company has created the ultimate in stereo sound. Only original **MARANTZ** parts can insure that your **MARANTZ** product will continue to perform to the specifications for which it is famous.

Parts for your **MARANTZ** equipment are generally available to our National Marantz Subsidiary or Agent.

### ORDERING PARTS :

Parts can be ordered either by mail or by Fax.. In both cases, the correct part number has to be specified.

The following information must be supplied to eliminate delays in processing your order :

1. Complete address
2. Complete part numbers and quantities required
3. Description of parts
4. Model number for which part is required
5. Way of shipment
6. Signature : any order form or Fax. must be signed, otherwise such part order will be considered as null and void.

#### USA

**MARANTZ AMERICA, INC.**  
440 MEDINAH ROAD  
ROSELLE, ILLINOIS 60172  
USA  
PHONE : 630 - 307 - 3100  
FAX : 630 - 307 - 2687

#### EUROPE / TRADING

**MARANTZ EUROPE B.V.**  
P.O.BOX 80002, BUILDING SFF2  
5600 JB EINDHOVEN  
THE NETHERLANDS  
PHONE : +31 - 40 - 2732241  
FAX : +31 - 40 - 2735578

#### BRAZIL

**PHILIPS DA AMAZONIA IND. ELET. ITDA**  
CENTRO DE INFORMACOES AO  
CEP 04698-970  
SAO PAULO, SP, BRAZIL  
PHONE : 0800 - 123123(Discagem Direta Gratuita)  
FAX : +55 11 534. 8988

#### PROFESSIONAL AMERICAS

**SUPERSCOPE TECHNOLOGIES, INC.**  
MARANTZ PROFESSIONAL PRODUCTS  
2640 WHITE OAK CIRCLE, SUITE A  
AURORA, ILLINOIS 60504 USA  
PHONE : 630 - 820 - 4800  
FAX : 630 - 820 - 8103

#### PROFESSIONAL AUSTRALIA

**TECHNICAL AUDIO GROUP PTY, LTD**  
558 DARLING STREET,  
BALMAIN, NSW 2041,  
AUSTRALIA  
PHONE : 61 - 2 - 9810 - 5300  
FAX : 61 - 2 - 9810 - 5355

#### CANADA

**LENBROOK INDUSTRIES LIMITED**  
633 GRANITE COURT,  
PICKERING, ONTARIO L1W 3K1  
CANADA  
PHONE : 905 - 831 - 6333  
FAX : 905 - 831 - 6936

#### AUSTRALIA

**QualiFi Pty Ltd,**  
24 LIONEL ROAD,  
MT. WAVERLEY VIC 3149  
AUSTRALIA  
PHONE : +61 - (0)3 - 9543 - 1522  
FAX : +61 - (0)3 - 9543 - 3677

#### THAILAND

**MRZ STANDARD CO.,LTD**  
746 - 754 MAHACHAI ROAD.,  
WANGBURAPAPIROM, PHRANAKORN,  
BANGKOK, 10200 THAILAND  
PHONE : +66 - 2 - 222 9181  
FAX : +66 - 2 - 224 6795

#### SINGAPORE

**WO KEE HONG DISTRIBUTION PTE LTD**  
130 JOO SENG ROAD  
#03-02 OLIVINE BUILDING  
SINGAPORE 368357  
PHONE : +65 858 5535 / +65 381 8621  
FAX : +65 858 6078

#### NEW ZEALAND

**WILDASH AUDIO SYSTEMS NZ**  
14 MALVERN ROAD MT ALBERT  
AUCKLAND NEW ZEALAND  
PHONE : +64 - 9 - 8451958  
FAX : +64 - 9 - 8463554

#### TAIWAN

**PAI- YUING CO., LTD.**  
6 TH FL NO, 148 SUNG KIANG ROAD,  
TAIPEI, 10429, TAIWAN R.O.C.  
PHONE : +886 - 2 - 25221304  
FAX : +886 - 2 - 25630415

#### MALAYSIA

**WO KEE HONG ELECTRONICS SDN. BHD.**  
SUITE 8.1, LEVEL 8, MENARA GENESIS,  
NO. 33, JALAN SULTAN ISMAIL,  
50250 KUALA LUMPUR, MALAYSIA  
PHONE : +60 3 - 2457677  
FAX : +60 3 - 2458180

#### JAPAN *Technical*

**MARANTZ JAPAN, INC.**  
35- 1, 7- CHOME, SAGAMIONO  
SAGAMIHARA - SHI, KANAGAWA  
JAPAN 228-8505  
PHONE : +81 42 748 1013  
FAX : +81 42 741 9190

#### 日本マランツ株式会社

本社 〒228-8505  
神奈川県相模原市相模大野7-35-1  
営業本部 〒150-0022  
東京都渋谷区恵比寿南1-11-9

#### KOREA

**MK ENTERPRISES LTD.**  
ROOM 604/605, ELECTRO-OFFICETEL, 16-58,  
3GA, HANGANG-RO, YONGSAN-KU, SEOUL  
KOREA  
PHONE : +822 - 3232 - 155  
FAX : +822 - 3232 - 154

### SHOCK, FIRE HAZARD SERVICE TEST :

**CAUTION :** After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins ( with unit NOT connected to AC mains and its Power switch ON ), and the face or Front Panel of product and controls and chassis bottom.

Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before it is return to the user/customer.

Ref. UL Standard No. 1492.

In case of difficulties, do not hesitate to contact the Technical Department at above mentioned address.

# 1. TECHNICAL SPECIFICATIONS (N1B)

## PLAYBACK SYSTEM

DVD-Video  
Video CD  
CD (CD-R and CD-RW)

## OPTICAL READOUT SYSTEM

Lasertype	Semiconductor AlGaAs	
Numerical Aperture	0.60 (DVD) 0.45 (VCD/CD)	
Wavelength	650 nm (DVD) 780 nm (VCD/CD)	

## DVD DISC FORMAT

Medium	Optical Disc	
Diameter	12cm (8cm)	
Playing time (12cm)	One layer	2.15 h*
	Dual layer	4 h*
	Two side	4.30 h*
	Single layer	
	Two side	8 h*
	Dual layer	

## TV STANDARD

	<b>EUROPE</b>	<b>USA</b>
	(PAL/50Hz)	(NTSC/60Hz)
Number of lines	625	525
Playback	Multistandard	(PAL/NTSC)

## VIDEO FORMAT

DA Converter	10 bits
Signal handling	Components
Digital Compression	MPEG2 for DVD, MPEG1 for VCD

## DVD

Horiz. Resolutio	720 pixels**	720 pixels**
Vertical Resolution	576 lines	480 lines

## VCD

Horiz. Resolution	352 pixels	352 pixels
Vertical Resolution	288 lines	240 lines

## VIDEO PERFORMANCE

Video output	1 Vpp into 75 ohm
S-Video output	Y: 1 Vpp into 75 ohm C: 0.3 Vpp into 75 ohm
RGB output	1 Vpp into 75 ohm
Black Level Shift	On/Off
Video Shift	Left/Right

## AUDIO FORMAT

Digital	MPEG	Compressed Digital
	DTS/AC-3 PCM	
	16, 20, 24 bits fs, 44.1, 48, 96 kHz	

Analog Sound Stereo  
Dolby Pro Logic downmix from AC-3 multi-channel sound  
3D Sound for virtual 5.1 channel sound on 2 speakers

## AUDIO PERFORMANCE

DA Converter	24 bits	
DVD	fs 96 kHz	4 Hz - 22kHz
	fs 48 kHz	4 Hz - 22 kHz
Video CD	fs 48 kHz	4 Hz - 22 kHz
CD	fs 44.1 kHz	4 Hz - 20 kHz
Signal-Noise (1kHz)		95 dB
Dynamic Range (1kHz)		90 dB
Crosstalk (1kHz)		110 dB
Distortion and Noise (1kHz)		85 dB

## CONNECTIONS

SCART	Euroconnector 2x
S-Video Output	Mini DIN, 4 pins
Video Output	Cinch (yellow)
Audio L+R output	Cinch (white/red)
Digital Output	1 coaxial, 1 optical
	IEC958 for CDDA / LPCM
	IEC1937 for MPEG1/2, AC-3 and DTS

## CABINET

Dimensions(w x h x d)	440 x 92 x 305 mm
Weight	Approx. 3.8 Kg

## PACKAGE CONTENTS

DVD-Video Player  
Remote Control & Batteries  
AC Power cable  
User Manual  
SCART cable (Euroconnector)  
Audio/Video cable

## GENERAL FUNCTIONALITY

Stop / Play / Pause  
Fast Forward / Backward  
Time search  
Step Forward / Backward  
Slow  
Title / Chapter / Track Select  
Skip Next / Skip Previous  
Repeat (Chapter / Title / All) or (Track / All)  
A-B Repeat  
Shuffle  
Enhanced ease of use graphical interface  
Perfect Still with digital multi-tap filter  
Zoom (x1.33, x2, x4) with picture enhancement  
3D Sound  
Virtual jog shuttle  
Audio and video bit rate indicator *(only available in certain countries)*

## DVD FUNCTIONALITY

Multi-angle Selection  
Audio Selection (1 out of max. 8 languages)  
Subtitles Selection (1 out of max. 32 languages)  
Aspect Ratio conversion (16:9, 4:3 Letterbox, 4:3 Pan Scan)  
Parental Control and Disk Lock  
Disc Menu support (Title Menu and Root Menu)  
Resume (5 discs) after stop / standby  
Screen Saver (Dim 75% after 15 min.)  
Programming Titles/chapters with Favorite Selection

## VIDEO CD FUNCTIONALITY

Playback Control for VCD 2.0 discs  
Parental Control and Disc lock  
Resume (5 discs) after stop / standby  
Screen Saver (Dim 75% after 15 min.)  
Programming Tracks with Favorite Selection

## AUDIO CD FUNCTIONALITY

Time Display (Total / Track)  
Full audio functionality with remote control  
Programming with Favorite Track Selection

\* typical playing time for movie with 2 spoken languages and 3 subtitle languages.

\*\* equivalent to 500 lines on your TV

Specifications subject to change without prior notice

## (/A1B, /S1G, /U1B)

### PLAYBACK SYSTEM

DVD-Video  
Video CD  
CD (CD-R and CD-RW)

### OPTICAL READOUT SYSTEM

Lasertype	Semiconductor AlGaAs
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Wavelength	650 nm (DVD) 780 nm (VCD/CD)

### DVD DISC FORMAT

Medium	Optical Disc
Diameter	12cm (8cm)
Playing time (12cm)	One layer 2.15 h <sup>*</sup> Dual layer 4 h <sup>*</sup> Two side 4.30 h <sup>*</sup> Single layer Two side 8 h <sup>*</sup> Dual layer

### TV STANDARD

	EUROPE	USA
	(PAL/50Hz)	(NTSC/60Hz)
Number of lines	625	525
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### VIDEO PERFORMANCE

Video output	1 Vpp into 75 ohm
S-Video output	Y: 1 Vpp into 75 ohm C: 0.3 Vpp into 75 ohm
Y	1 Vpp into 75 ohm
CR	0.7 Vpp into 75 ohm
Cb	0.7 Vpp into 75 ohm
Black Level Shift	On/Off
Video Shift	Left/Right

### AUDIO FORMAT

Digital	MPEG	Compressed
	DTS/AC-3	
	PCM	16, 20, 24 bits fs, 48, 96 kHz

Analog Sound Stereo

Dolby Pro Logic downmix from AC-3 multi-channel sound  
3D Sound for virtual 5.1 channel sound on 2 speakers

### AUDIO PERFORMANCE

DA Converter	24 bits
DVD	fs 96 kHz 4 Hz - 44 kHz fs 48 kHz 4 Hz - 22 kHz
Video CD	fs 48 kHz 4 Hz - 22 kHz
CD	fs 44.1 kHz 4 Hz - 20 kHz
Signal-Noise (1kHz)	95 dB
Dynamic Range (1kHz)	90 dB
Crosstalk (1kHz)	110 dB
Distortion and Noise (1kHz)	85 dB

### CONNECTIONS

S-Video Output	Mini DIN, 4 pins
Component Video	Y Cinch (green) U (CR) Cinch (blue) V (Cb) Cinch (red) Cinch (yellow) 2x Cinch (white/red) 2x
Video Output	1 coaxial, 1 optical
Audio L+R output	IEC958 for CDDA / LPCM
Digital Output	IEC1937 for MPEG1/2, AC-3 and DTS

### CABINET

Dimensions (w x h x d)	440 x 92 x 305mm
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User Manual  
Audio/Video cord

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Time search  
Step Forward / Backward  
Title / Chapter / Track Select  
Skip Next / Skip Previous  
Repeat (Chapter / Title / All) or (Track / All)  
A-B Repeat  
Shuffle  
Enhanced ease of use graphical interface  
Perfect Still with digital multi-tap filter  
Zoom (x1.33 x2. x4) with picture enhancement  
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Full audio functionality with remote control  
Programming with Favorite Track Selection

\* typical playing time for movie with 2 spoken languages and 3 subtitle languages.  
\*\* equivalent to 500 lines on your TV

*Specifications subject to change without prior notice*

## 2. CONNECTION FACILITIES

### SCART (/N1B versions only)

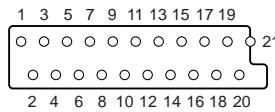
Full according PQR3 IMS

Connector implementation according EN50049-1; color = black; dual SCART

Fully according to prEN1057-2-1

Signal switching is P50 controlled; supported features of mode 3 see survey of applicable standards.

#### 2-1 Video performance (/N1B only)



##### 2-1-1 SCART II (connected to TV)

Pin signals:

1	Output	Audio R	1.8V RMS
2	Input	Audio R	
3	Output	Audio L	1.8V RMS
4		Audio GND	
5		Blue/Chroma GND	
6	Input	Audio L	
7	Bi-dir	Blue out/Chroma in	0.7pp +/-0.1V into 75 Ohm (*)
8	Output	Function switch	<2V = TV >4.5V / <7V = asp. ratio 16:9 DVD >9.5V / <12V = asp. ratio 4:3 DVD
9		Green GND	
10		Bi-dir P50 control	
11	Output	Green	0.7Vpp +/-0.1V into 75 Ohm (*)
12		not connected	
13		Red/Chroma GND	
14		fast switch GND	
15	Output	Red out/Chroma out	0.7Vpp +/-0.1V into 75 Ohm (*) +/-3dB 0.3Vpp in case of Chroma
16	Output	fast switch RGB /CVBS or Y	>1V / <3V into 75 Ohm = RGB 0.4V into 75 Ohm = CVBS
17		Y/CVBS GND	
18		fast switching GND	
19	Output	CVBS/Y/RGB sync	1Vpp +/-0.1V into 75 Ohm (*)
20	Input	CVBS/Y	
21		Shield	

##### SCART I (connected to AUX)

Pin signals:

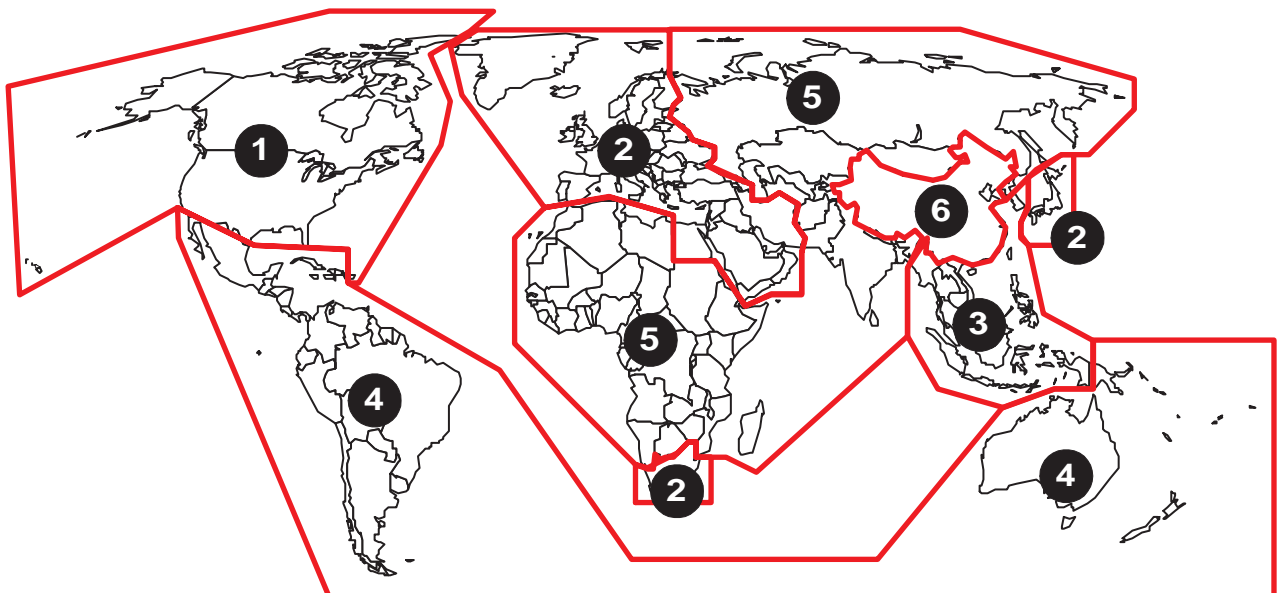
1	Output	Audio R	1.8V RMS
2	Input	Audio R	
3	Output	Audio L	1.8V RMS
4		Audio GND	
5		Blue/Chroma GND	
6	Input	Audio L	
7	Bi-dir	Blue in/Chroma out	+/-3dB 0.3Vpp Chroma
8	Input	Function switch	
9		Green GND	
10	Bi-dir	P50 control	
11	Input	Green	
12		not connected	
13		Red/Chroma GND	
14		fast switch GND	
15	Input	Red in/Chroma in	
16	Input	fast switch RGB/CVBS or Y	
17		CVBS GND	
18		fast switching GND	
19			
20	Input	CVBS/Y	
21		Shield	

(\*) for 100% white

#### What are "regional codes"?

Motion picture studios want to control the home release of movies in different countries because theater releases aren't simultaneous (a movie may come out on DVD in the US when it's just hitting screens in Europe). Therefore they have required that the DVD standard include codes which can be used to lock out the playback of certain discs in certain geographical regions. Players sold in each region will have that region's code built into the player. The player will refuse to play these "region coded" discs which are not allowed in the region. However, regional codes are entirely optional. Discs without codes will play on any player in any country. Some studios have already announced that only their new releases will have regional codes. There are six regions:

1. United States and Canada
2. Europe and Japan
3. Far East (except Japan & China)
4. South America and Oceania
5. Africa and the Middle East
6. China (except Hong Kong)



Map of DVD Regions





### 3. INFORMATIONS

#### REGION CODE

VERSION	REGION CODE	COUNTRY
/N1B	2	EUROPE
/S1G	3	ASIAN PACIFIC
/U1B	1	USA/CANADA
/A1B	4	AUSTRALIA

#### THE DISCS THAT THE DV4100 CAN HANDLE

The following discs can be played back with a DV4100.

disc	mark	playback capability	size	side
DVD		Audio/Video	12 cm 8 cm	single/double
CD		Audio	12 cm 8 cm	single
VCD	 	Audio/Video	12 cm 8 cm	single

**Note:** The regional code of the discs must meet to the regional code of the DV4100.

#### DVD INFORMATION

Below is a glossary of the new terms related to DVD.

##### Title:

A disc may have more than one story/movie on it, so each story/movie is called a "title".

For example, if there are 2 movies on the disc, they are separated into Title 1 and Title 2.

##### Chapter:

A title may also be separated into chapters.

For example, a movie (title) may be separated into 3 scenes (chapters).

Title 1			Title 2		
Chapter 1	Chapter 2	Chapter 3	Chapter 1	Chapter 2	Chapter 3

##### Subtitles:

DVDs are recorded with up to 32 different subtitle languages. If a disc has more than one subtitle language, you can select the subtitle language that you want to read.

##### Soundtrack language:

DVDs are recorded with up to 8 different soundtrack languages. If a disc has more than one language, you can select the soundtrack language that you want to listen to.

##### Multi-angles:

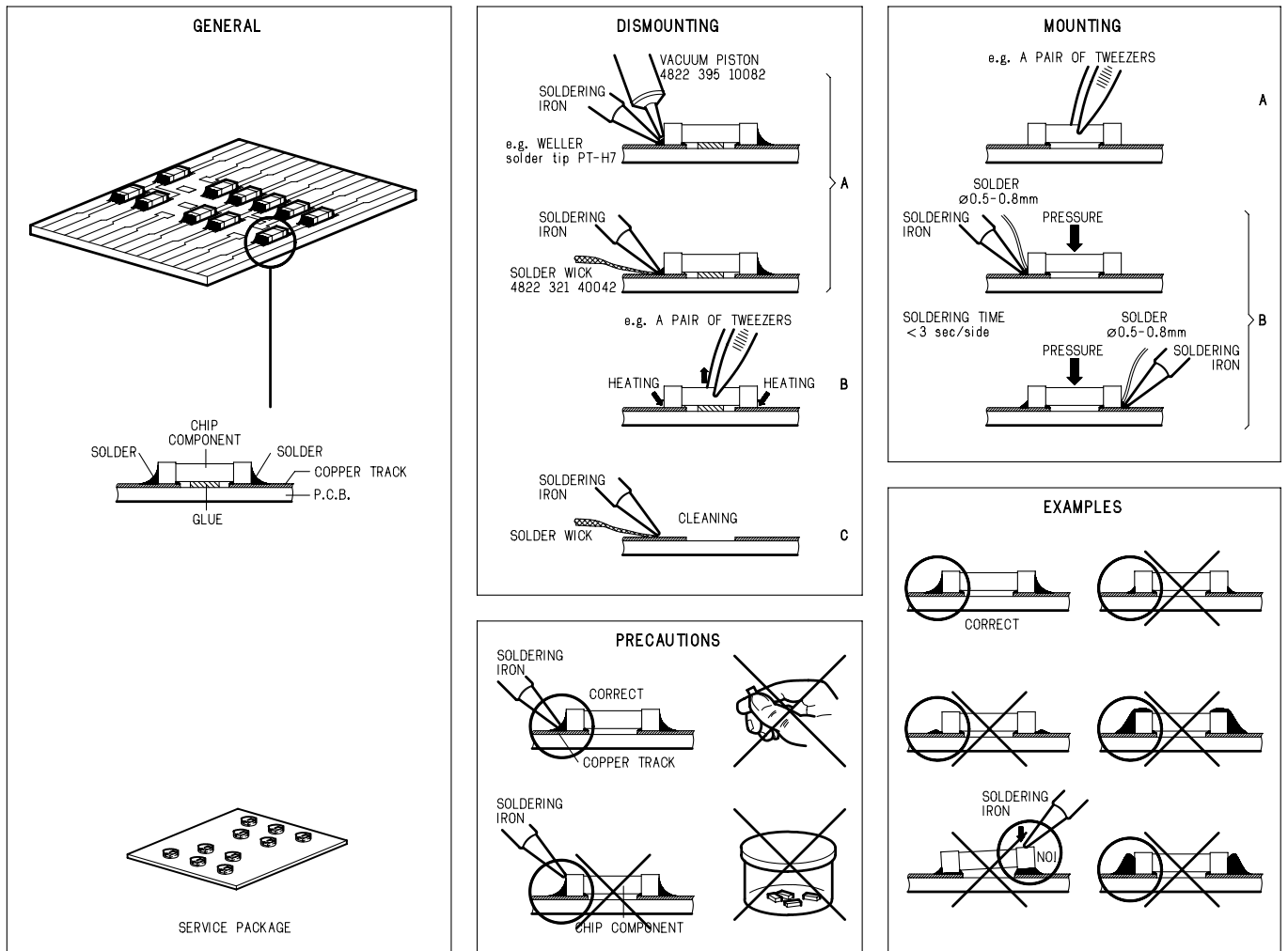
On some DVDs, scenes have been filmed from different angles (up to a maximum of 9). On these discs, you can select the angle that you want to watch. Please refer to the DVD's manual to see which scenes have multi-angles.



\* It is important to note that CD-R, CD-RW discs must be FINALIZED before they can be played on this player. The disc types which run on the player feature one or more of these logos on the disc packaging.

## 4. SERVICING HINT

### SERVICE HINTS



### SERVICE TOOLS

Audio signals disc	4822 397 30184
Disc without errors (SBC444)+	
Disc with DO errors, black spots and fingerprints (SBC444A)	4822 397 30245
Disc (65 min 1kHz) without no pause	4822 397 30155
Max. diameter disc (58.0 mm)	4822 397 60141
Torx screwdrivers	
Set (straight)	4822 395 50145
Set (square)	4822 395 50132
13th order filter	4822 395 30204
DVD test disc	4822 397 10131
TEST software for PC : ComPair V1. 2	4822 727 21634
ComPair V1. 3	4822 727 21637
Connection Cable	3122 785 90017

## 5. WARNING AND LASER SAFETY INSTRUCTIONS

### **GB** WARNING

All ICs and many other semi-conductors are susceptible to electrostatic discharges (ESD). Careless handling during repair can reduce life drastically.

When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance.

Keep components and tools also at this potential.

ESD



### **NL** WAARSCHUWING

Alle IC's en vele andere halfgeleiders zijn gevoelig voor elektrostatische ontladingen (ESD).

Onzorgvuldig behandelen tijdens reparatie kan de levensduur drastisch doen verminderen.

Zorg ervoor dat u tijdens reparatie via een polsband met weerstand verbonden bent met hetzelfde potentiaal als de massa van het apparaat.

Houd componenten en hulpmiddelen ook op ditzelfde potentiaal.

### **F** ATTENTION

Tous les IC et beaucoup d'autres semi-conducteurs sont sensibles aux décharges statiques (ESD).

Leur longévité pourrait être considérablement écourtée par le fait qu'aucune précaution n'est prise à leur manipulation.

Lors de réparations, s'assurer de bien être relié au même potentiel que la masse de l'appareil et enfilez le bracelet serti d'une résistance de sécurité.

Veiller à ce que les composants ainsi que les outils que l'on utilise soient également à ce potentiel.

### **D** WARNUNG

Alle IC und viele andere Halbleiter sind empfindlich gegen elektrostatische Entladungen (ESD).

Unvorsichtige Behandlung bei der Reparatur kann die Lebensdauer drastisch vermindern. Sorgen sie dafür, das Sie im Reparaturfall über ein Pulsarmband mit Widerstand mit dem Massepotential des Gerätes verbunden sind.

Halten Sie Bauteile und Hilfsmittel ebenfalls auf diesem Potential.

### **I** AVVERTIMENTO

Tutti IC e parecchi semi-conduttori sono sensibili alle scariche statiche (ESD).

La loro longevità potrebbe essere fortemente ridotta in caso di non osservazione della più grande cauzione alla loro manipolazione.

Durante le riparazioni occorre quindi essere collegato allo stesso potenziale che quello della massa dell'apparecchio tramite un braccialetto a resistenza.

Assicurarsi che i componenti e anche gli utensili con quali si lavora siano anche a questo potenziale.

### **GB**

Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.

### **NL**

Veiligheidsbepalingen vereisen, dat het apparaat in zijn oorspronkelijke toestand wordt terug gebracht en dat onderdelen, identiek aan de gespecificeerde worden toegepast.

### **D**

Bei jeder Reparatur sind die geltenden Sicherheitsvorschriften zu beachten. Der Originalzustand des Gerats darf nicht verändert werden. Für Reparaturen sind Original-Ersatzteile zu verwenden.

### **I**

Le norme di sicurezza esigono che l'apparecchio venga rimesso nelle condizioni originali e che siano utilizzati pezzi di ricambio identici a quelli specificati.

### **F**

Les normes de sécurité exigent que l'appareil soit remis à l'état d'origine et que soient utilisées les pièces de rechange identiques à celles spécifiées.



## SHOCK, FIRE HAZARD SERVICE TEST:

**CAUTION:** After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins (with unit NOT connected to AC mains and its Power switch ON), and the face or Front Panel of product and controls and chassis bottom,

Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before return to user/customer.

Ref.UL Standard NO.1492.

## NOTE ON SAFETY:

Symbol  : Fire or electrical shock hazard. Only original parts should be used to replace any part with symbol  Any other component substitution (other than original type), may increase risk of fire or electrical shock hazard.



## LASER SAFETY

This unit employs a laser. Only a qualified service person should remove the cover or attempt to service this device, due to possible eye injury.

### LASER DEVICE UNIT

Type:	SemiconductorlaserGaAlAs
Wave length:	650 nm (DVD) 780 nm (VCD/CD)
Output Power:	7 mW (DVD) 10 mW (VCD/CD)
Beam divergence:	60 degree



**USE OF CONTROLS OR ADJUSTMENTS OR PERFORMANCE OF PROCEDURE OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.**

### AVOID DIRECT EXPOSURE TO BEAM

### WARNING

The use of optical instruments with this product will increase eye hazard.  
Repair handling should take place as much as possible with a disc loaded inside the player

### WARNING LOCATION: INSIDE ON LASER COVERSIELD

**CAUTION** VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM  
**ADVARSEL** SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGÅ UDSÆTTELSE FOR STRÅLING  
**ADVARSEL** SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL ÅPNES UNNGÅ EKSPONERING FOR STRÅLEN  
**VARNING** SYNLIG OCH OSYNLIG LASERSTRÅLNING NÅR DENNA DEL ÄR ÖPPNAD BETRAKTA EJ STRÅLEN  
**VARO!** AVATT AESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTT ÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN  
**VORSICHT** SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETZEN  
**DANGER** VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM  
**ATTENTION** RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

## Warning for powersupply on position 1005

**The primary side of the powersupply including the heatsink carries live mains voltage when the player is connected to the mains even when the player is swiched off !**

This primary area is not shielded so it is possible to touch copper tracks and/or components when servicing the player. Service personel have to take precautions to prevent touching this area or components in this area .

The primary side of the powersupply has been indicated with a lightning stroke and a stripe-marked printed on the printed wiring board

### Note:

**The screws on the basic Engine (position 218 in on the exploded view drawing) may never be touched removed or re-adjusted.**

**Handle the Basic engine with care when the unit has to be exchanged!**

**The mechanism of the basic engine is very sensative for dropping or shocks**

## 6. SERVICE HINTS

### 6.1 DVD-Module 218

The DVD mechanism has to be exchanged completely in case of failure. A new or repaired mechanism can be ordered with codenumber 9305 023 61001.

Return the defective unit complete assembled in original package to Philips Consumer Service in Eindhoven.

The monoboard has to be repaired on component level.

### 6.3 Power Supply options

3122 427 21750		3122 427 21370		3122 427 21760	
110V USA		220V Europe China		Multi voltage A/P	
2261	CAP 330pF	2121	ELCO 100uF 385V	2261	CAP 330pF
2121	ELCO 150uF 250V			2121	ELCO 150uF 400V
3133	Resistor 10M				

### 6.4 Compair

For assistance with the repair process of the monoboard an electronic Fault finding guidance has been developed , this program is called COMPAIR.

This COMPAIR program is available on CDROM.

The Version of the CDROM for repair of the monoboard is V1.3 and can be ordered with codenumber : 4822 727 21637.

This is an update CDROM , so when the COMPAIR CDROM is used for the first time , one has to install the COMPAIR ENGINE CDROM V1.2 first.

The V1.2 CDROM can be ordered with codenumber 4822 727 634 and has to be registered after installation , the procedure for registration is explained in the help file of the program and in the booklet from the CDROM.

The cable to connect the monoboard with a PC can be ordered with codenumber 3122 785 90017.

All the hardware and software requirements of the systems necessary for working with COMPAIR is described on the CDROM.

### 6.5 Monoboard repair

For repair of the monoboard the service manual 3122 785 10045 must be used.

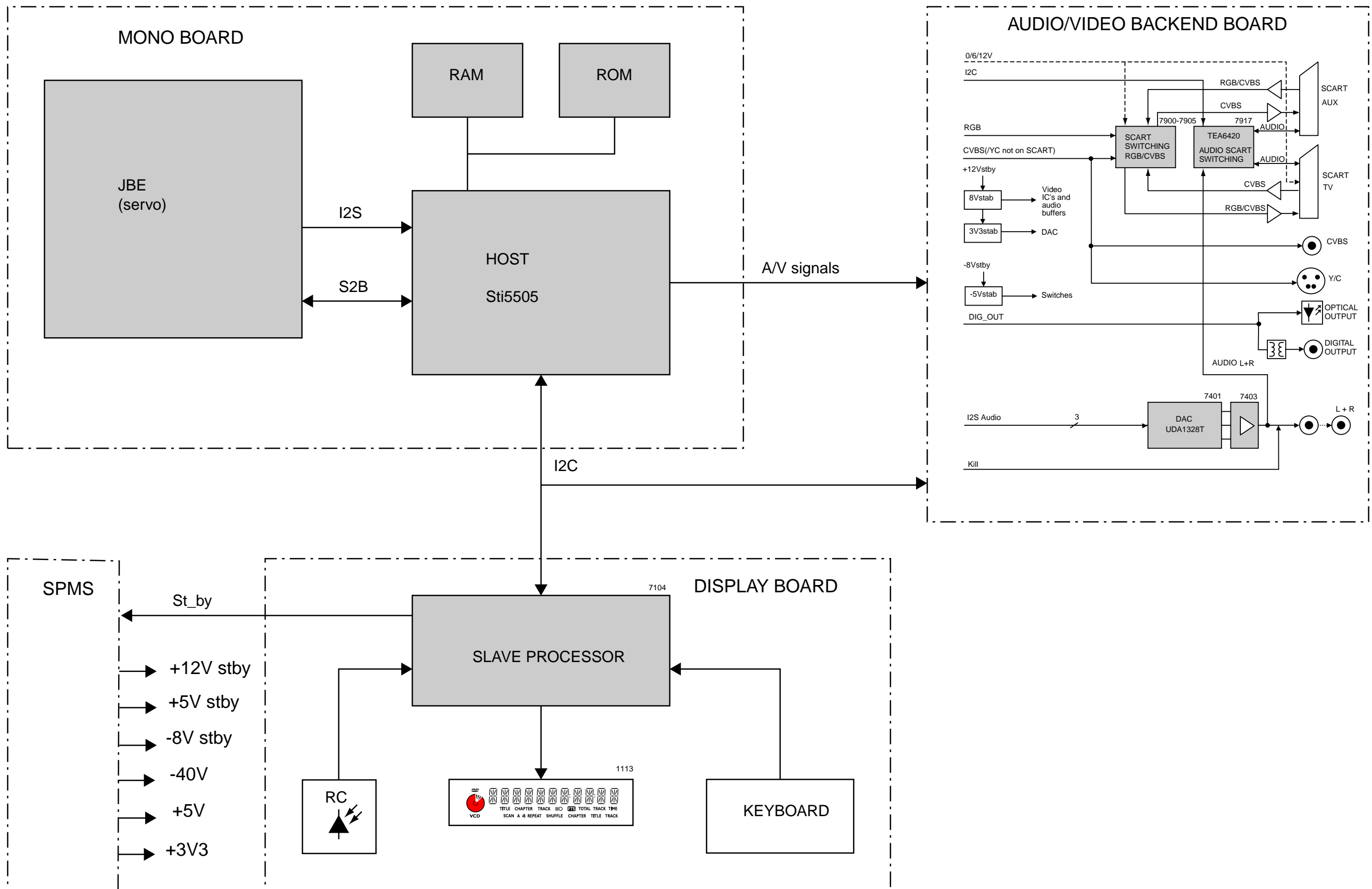
### 6.2 Diagnostic software

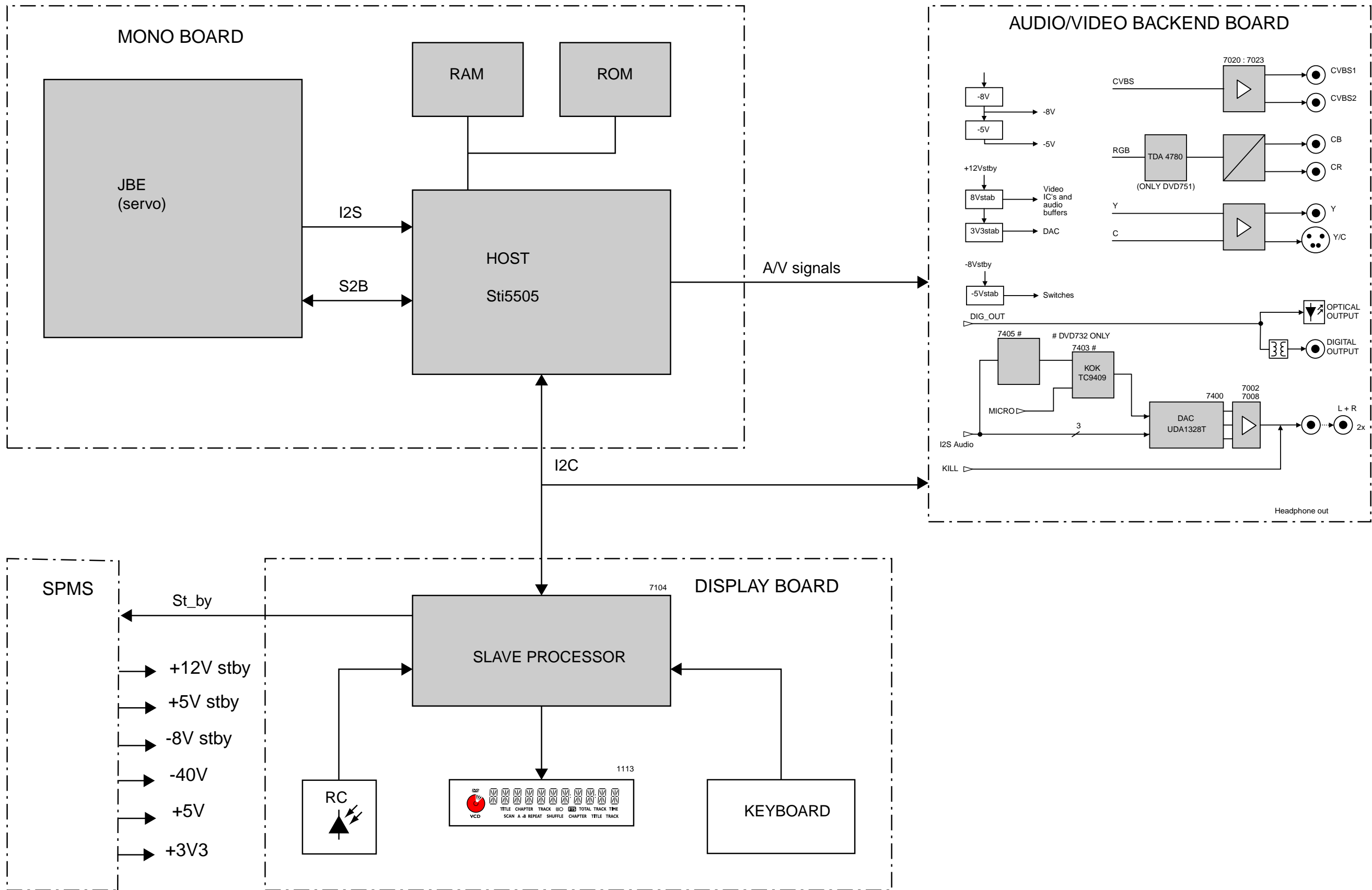
In chapter "Diagnostic software" some tests are referring to the SCART functionality.

These tests are for sets with RGB-output.

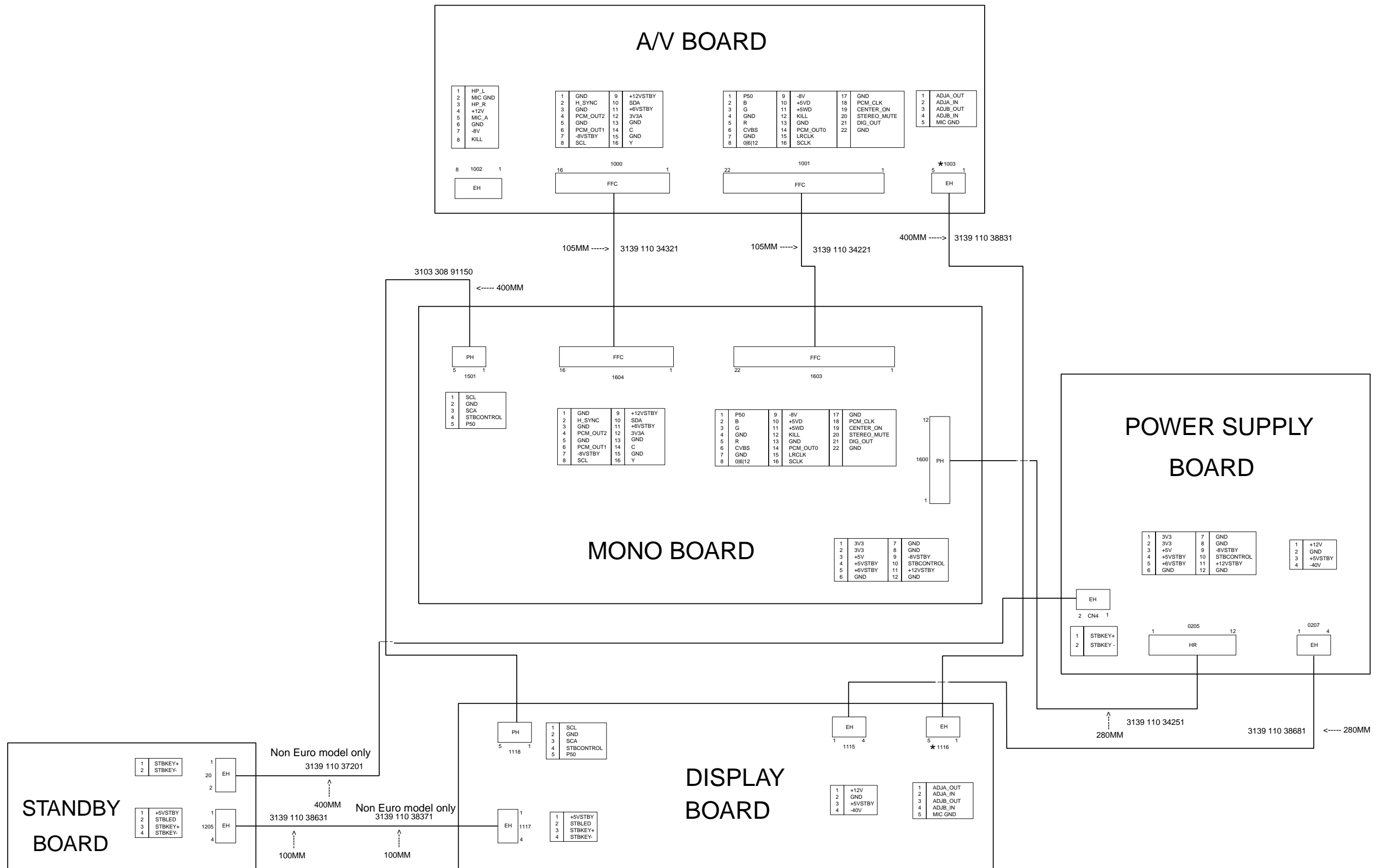
For sets without RGB-output no SCART connector is mounted. In these sets the SCART tests will automatically be skipped

7. BLOCK DIAGRAM (/N1B)

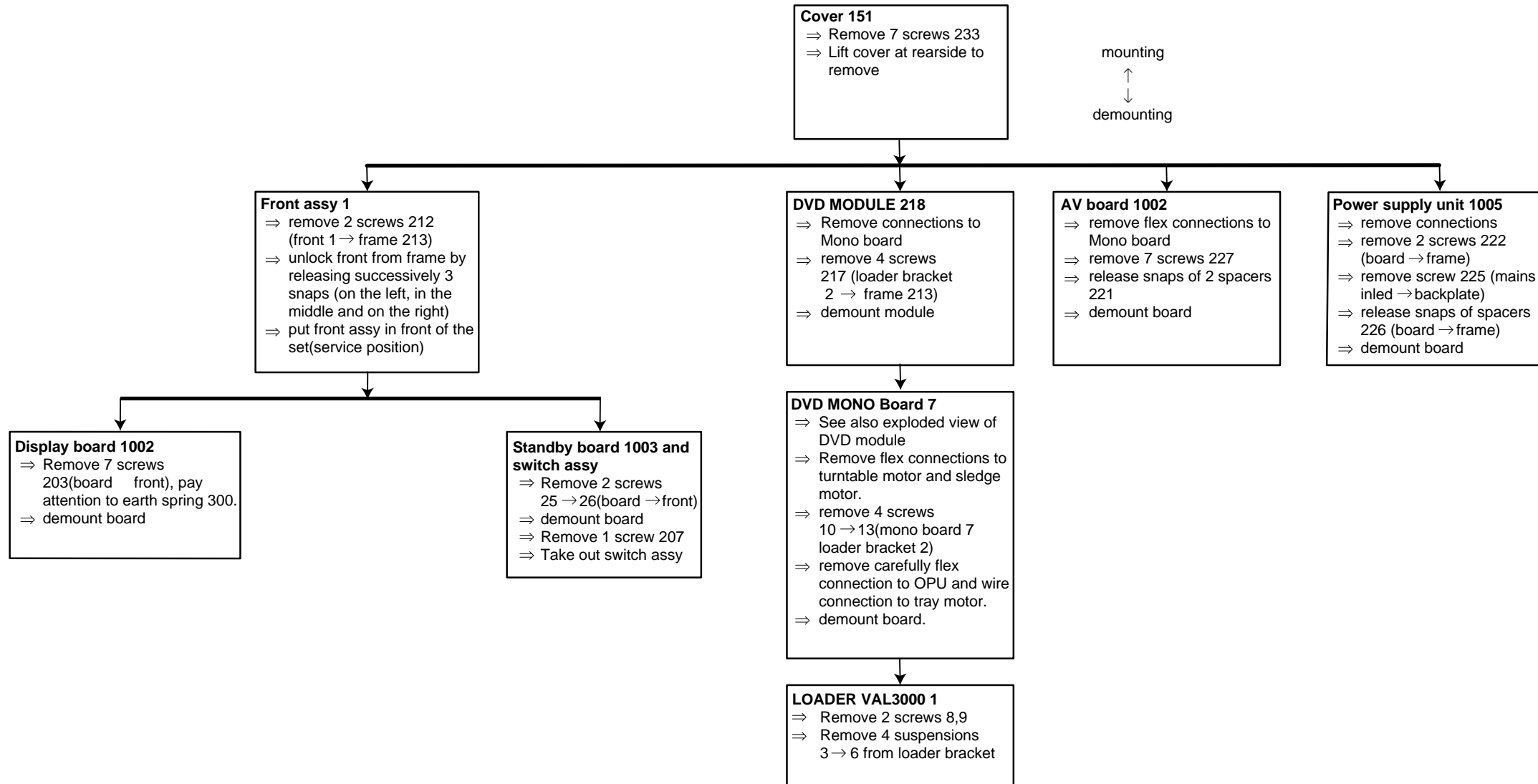




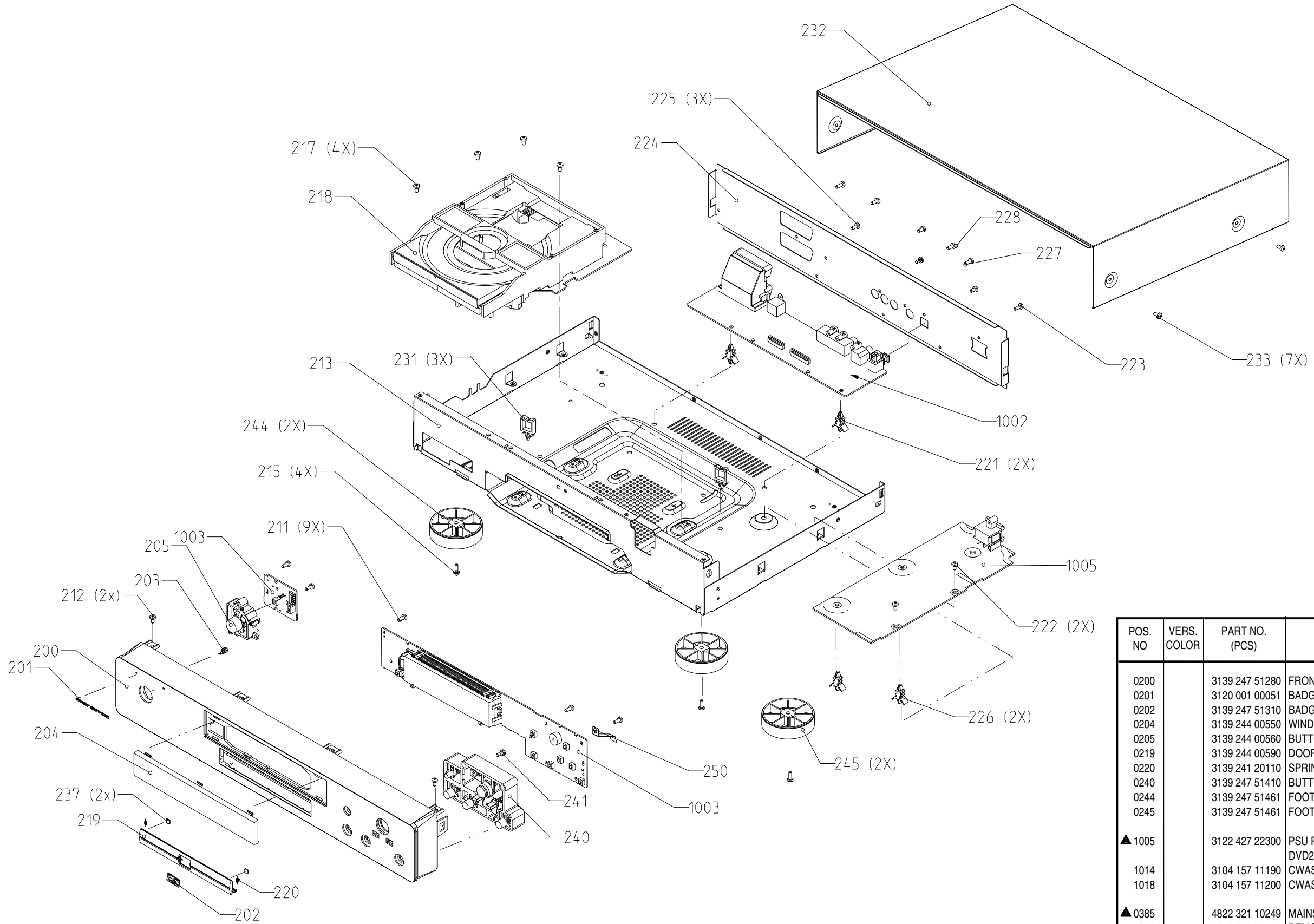
# 8. WIRING DIAGRAM



## 9. DISMANTLING INSTRUCTIONS

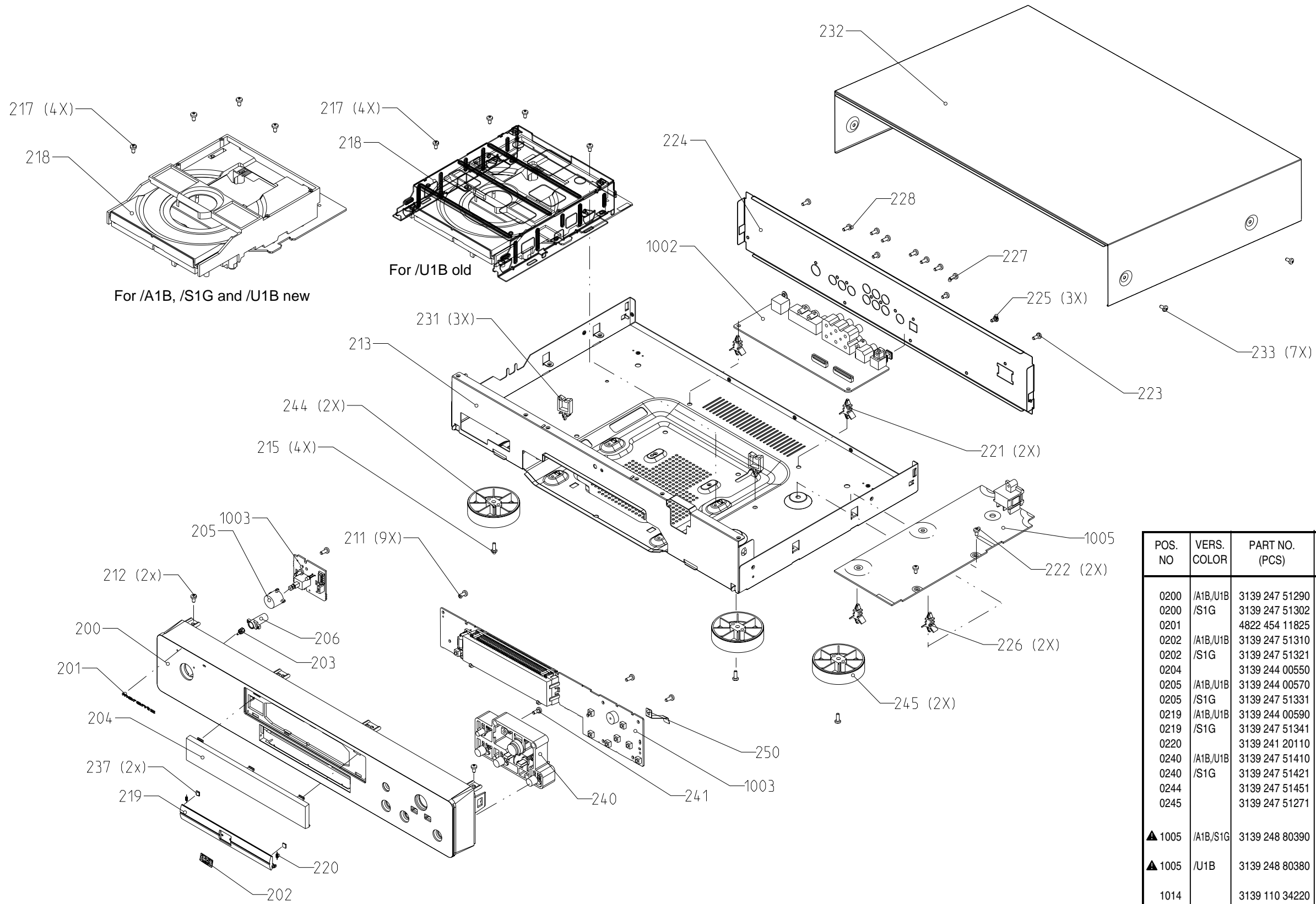


10. EXPLODED VIEW AND PARTS LIST (/N1B)



POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJ)
0200		3139 247 51280	FRONT PANEL (BLACK)	QT24751280
0201		3120 001 00051	BADGE MARANTZ	QZ00100051
0202		3139 247 51310	BADGE DVD	QT24751310
0204		3139 244 00550	WINDOW	QT24400550
0205		3139 244 00560	BUTTON STANDBY	QT24400560
0219		3139 244 00590	DOOR	QT24400590
0220		3139 241 20110	SPRING DOOR	QT24120110
0240		3139 247 51410	BUTTON CONTROL	QT24751410
0244		3139 247 51461	FOOT	QT24751461
0245		3139 247 51461	FOOT	QT24751461
▲ 1005		3122 427 22300	PSU PCB ASSY DVD2B+ 20PS223	
1014		3104 157 11190	CWAS FLEX DVD 22 130 32S	QW15711190
1018		3104 157 11200	CWAS FLEX DVD 16 130 32S	QW15711200
▲ 0385		4822 321 10249	MAINS CORD	QP32110249
0384		3139 228 85500	REMOTE CONTROL	QT22885500
0387		3139 246 10340	USER GUIDE (/N1B)	QT24610340

(/A1B, /S1G, /U1B)

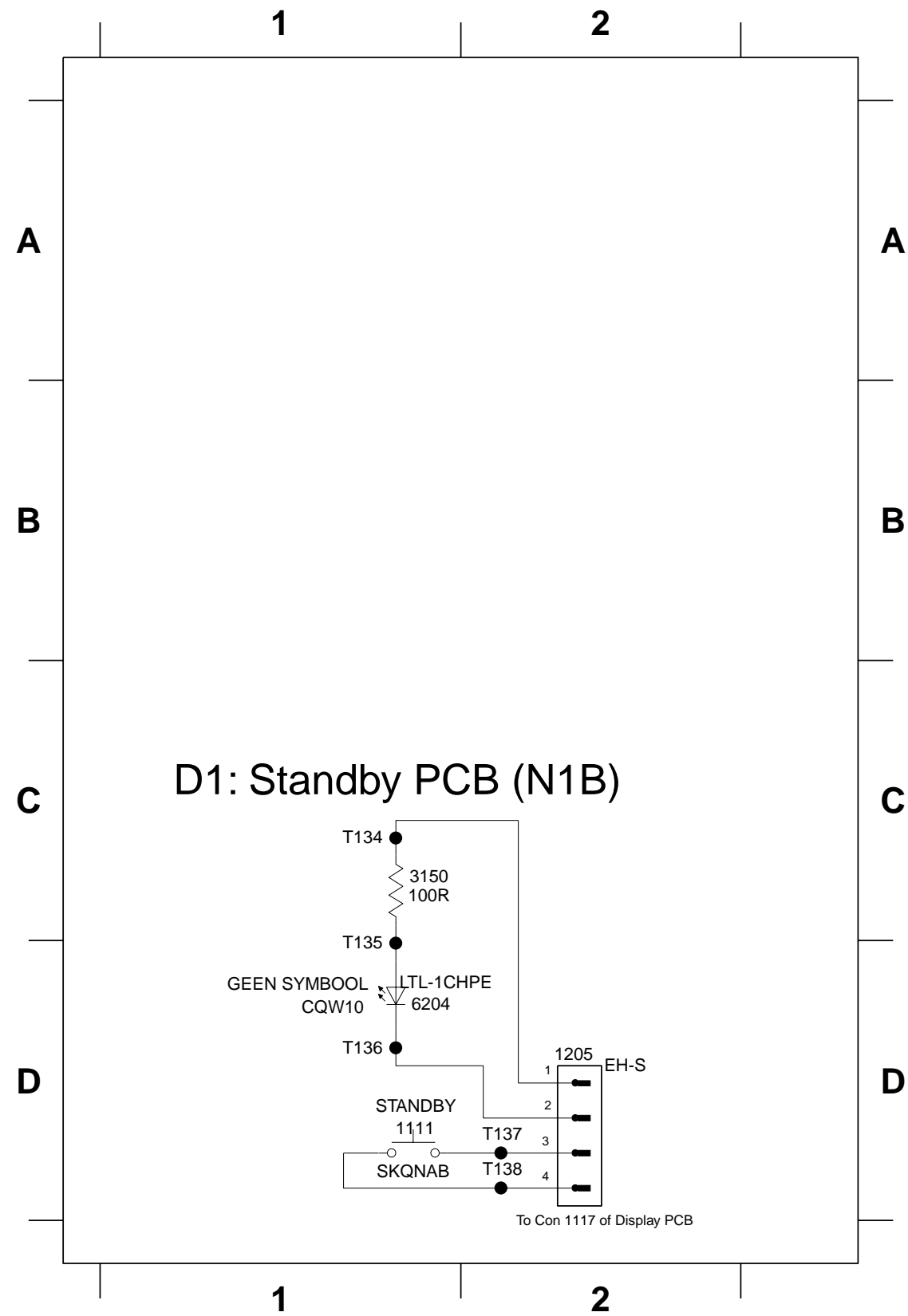


POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
0200	/A1B,/U1B	3139 247 51290	FRONT PANEL (BLACK)	QT24751290
0200	/S1G	3139 247 51302	FRONT PANEL (GOLD)	QT24751302
0201		4822 454 11825	BADGE MARANTZ	QP45411825
0202	/A1B,/U1B	3139 247 51310	BADGE DVD (BLACK)	QT24751310
0202	/S1G	3139 247 51321	BADGE DVD (GOLD)	QT24751321
0204		3139 244 00550	WINDOW	QT24400550
0205	/A1B,/U1B	3139 244 00570	BUTTON POWER (BLACK)	QT24400570
0205	/S1G	3139 247 51331	BUTTON POWER (GOLD)	QT24751331
0219	/A1B,/U1B	3139 244 00590	DOOR (BLACK)	QT24400590
0219	/S1G	3139 247 51341	DOOR (GOLD)	QT24751341
0220		3139 241 20110	SPRING DOOR	QT24120110
0240	/A1B,/U1B	3139 247 51410	BUTTON CONTROL (BLACK)	QT24751410
0240	/S1G	3139 247 51421	BUTTON CONTROL (GOLD)	QT24751421
0244		3139 247 51451	FOOT	QT24751451
0245		3139 247 51271	FOOT	QT24751271
▲ 1005	/A1B,/S1G	3139 248 80390	PSU PCB ASSY DVD2000 (OVS)	QT24880390
▲ 1005	/U1B	3139 248 80380	PSU PCB ASSY DVD2000 (USS)	QT24880380
1014		3139 110 34220	FFC FOIL 22P/105/22P BD B	QT11034220
1018		3139 110 34230	FFC FOIL 16P/105/16P BD B	QT11034230
0384		3139 228 85500	REMOTE CONTROL	QT22885500
▲ 0385	/A1B	3139 118 73040	MAINS CORD (/A1B)	QT11873040
▲ 0385	/S1G	4822 321 10249	MAINS CORD (/S1G)	QP32110249
▲ 0385	/U1B	4822 321 11466	MAINS CORD (/U1B)	QP32111466
0387	/U1B	3139 246 10350	USER GUIDE (/U1B)	QT24610350
0387	/A1B,/U1B	3139 246 10521	USER GUIDE (/A1B,/S1G)	QT24610521

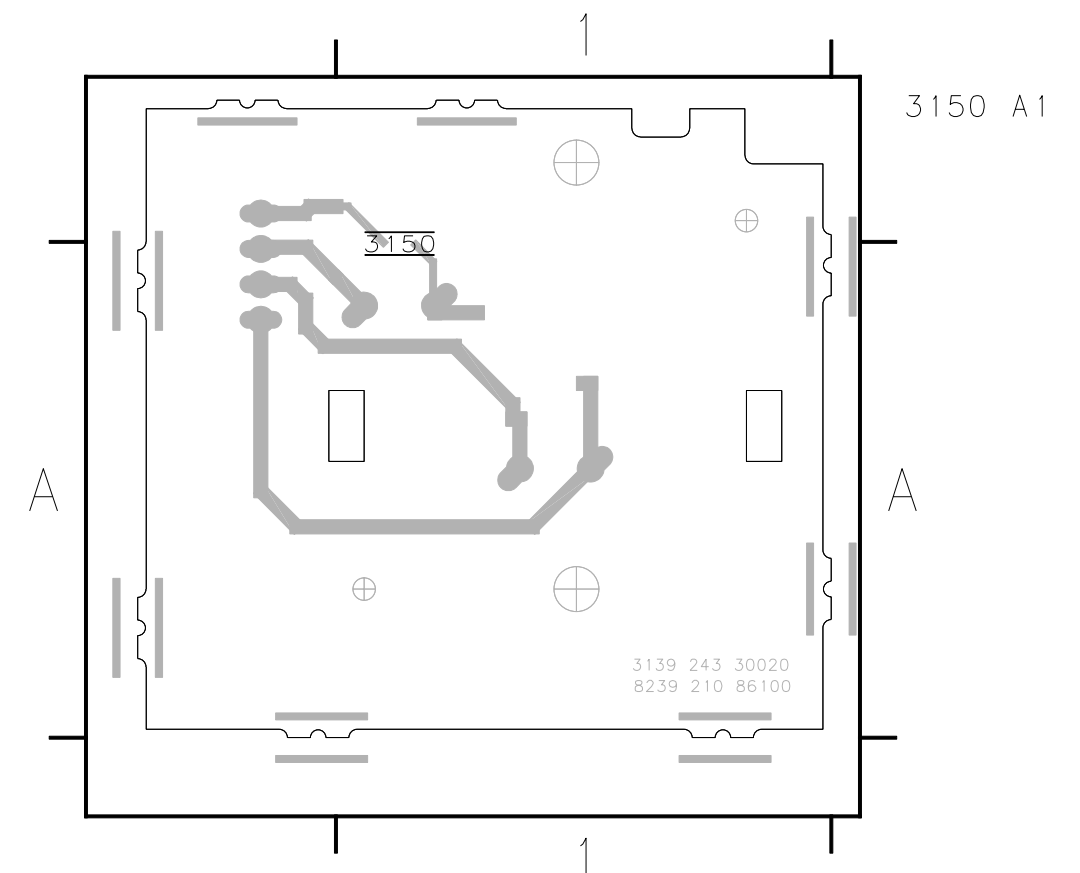
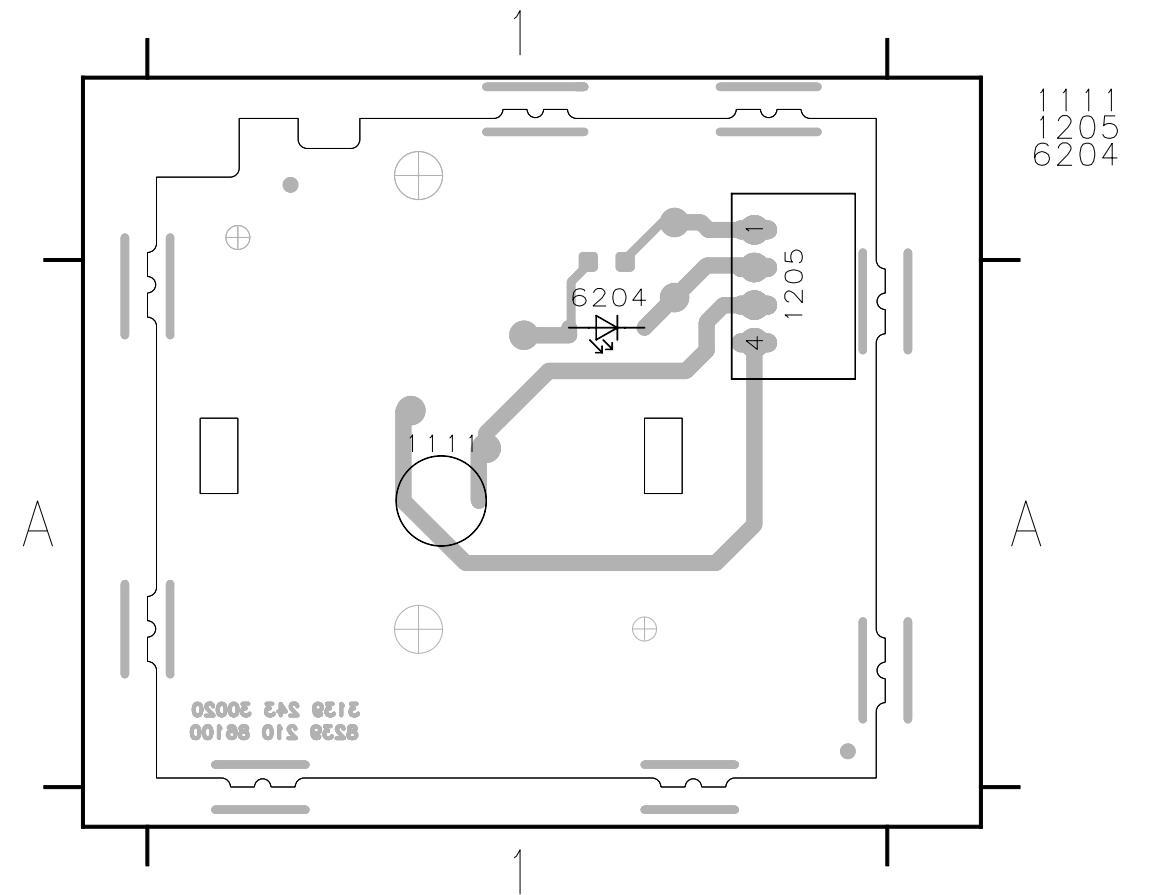


## 12. SCHEMATIC DIAGRAM AND PARTS LOCATION

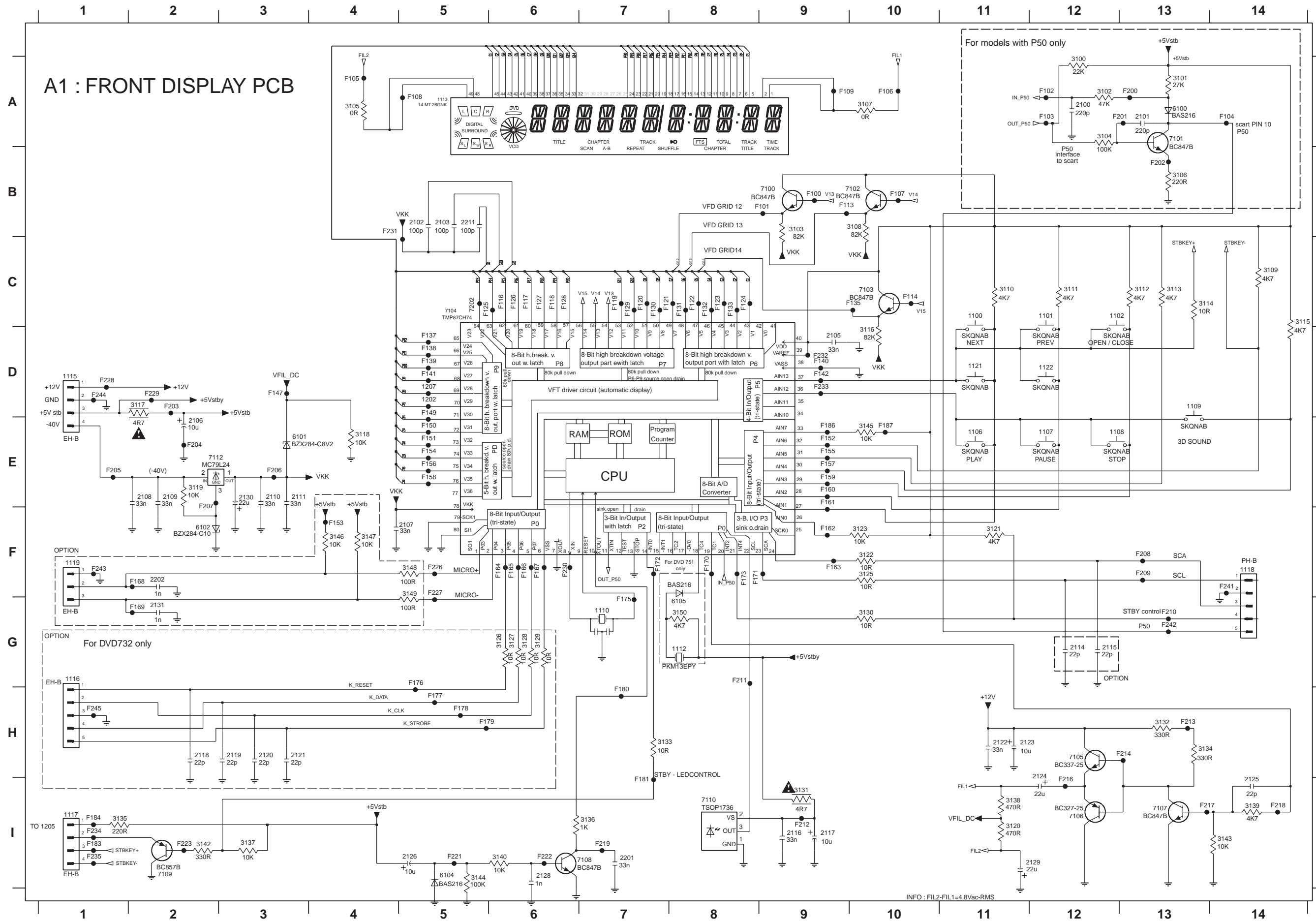
Volume / Standby PWB



- 1111 D1
- 1205 D2
- 3150 C1
- 6204 D1
- T134 C1
- T135 D1
- T136 D1
- T137 D2
- T138 D2

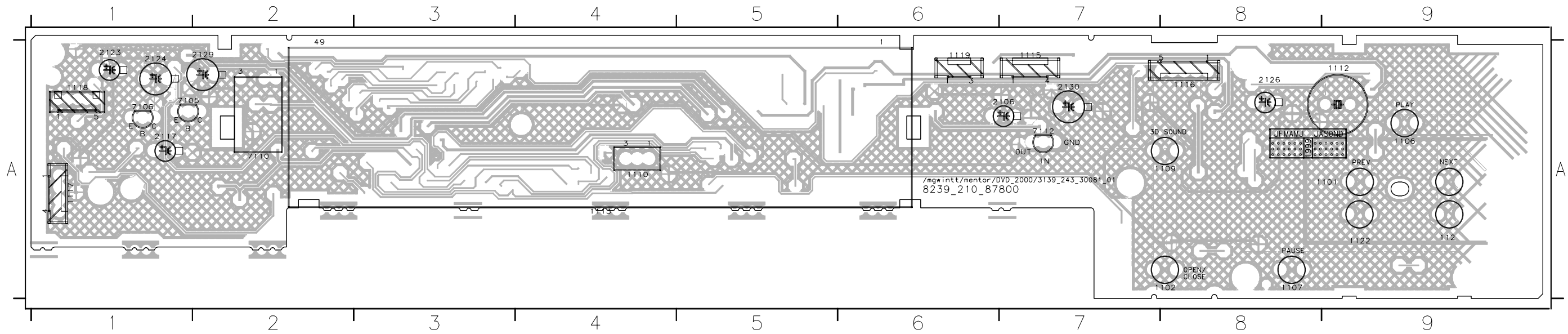


Display

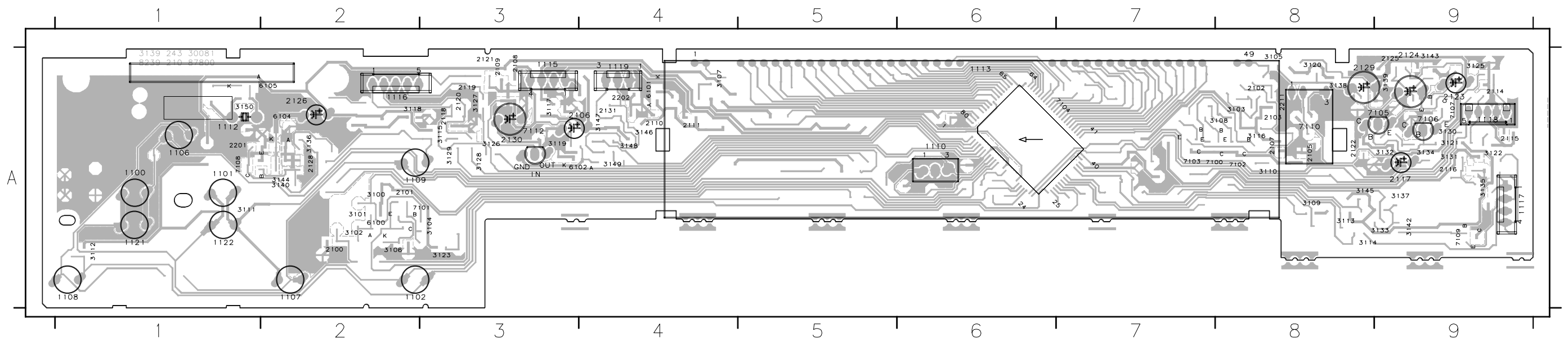


# Display PWB

1100 A9101 A9102 A8106 A9107 A8108 A9109 A8110 A4112 A9113 A4115 A7116 A8117 A1118 A1119 A6121 A9122 A9106 A7117 A2123 A2124 A2126 A8129 A2130 A7105 A7106 A7110 A7112 A7

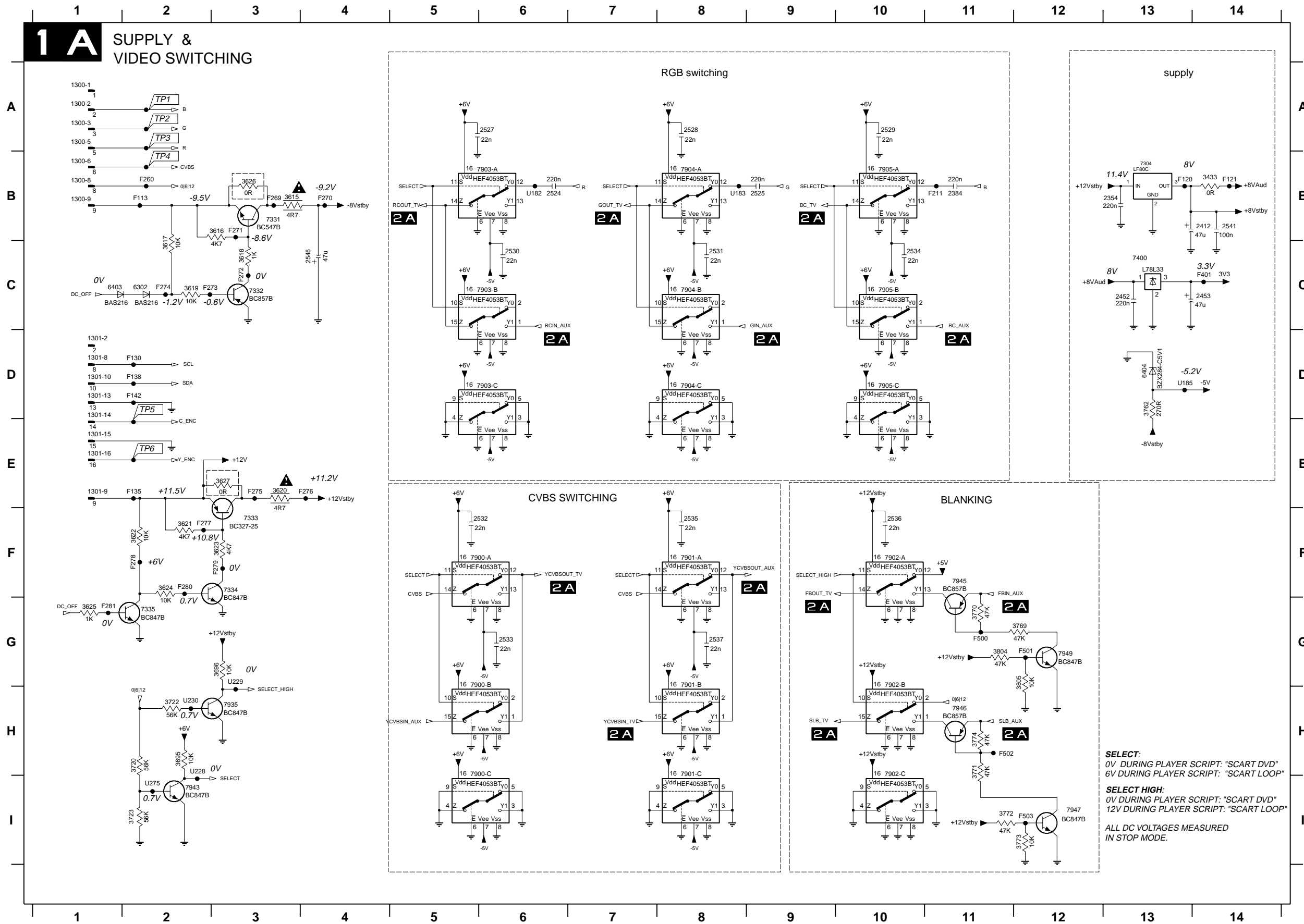


2100 A2103 A8108 A7111 A4116 A9120 A7125 A9201 A3100 A2103 A8106 A2109 A8112 A3115 A8118 A2121 A9125 A9128 A8131 A9134 A9137 A9140 A2144 A2147 A8150 A6102 A7100 A7103 A7108 A1  
 2101 A2105 A8108 A7114 A9118 A9121 A8128 A2202 A43101 A2104 A8108 A8107 A2110 A8110 A8113 A3116 A8119 A8120 A8122 A9126 A8129 A8130 A9133 A9135 A9138 A9141 A9145 A8148 A6100 A6104 A7101 A7104 A9109 A9  
 2102 A9107 A8110 A7115 A9119 A9122 A8131 A4221 A8102 A2105 A8108 A8111 A7114 A8117 A8120 A8123 A9127 A8130 A9133 A9135 A9138 A9143 A9146 A2149 A6101 A6105 A7102 A7107 A9

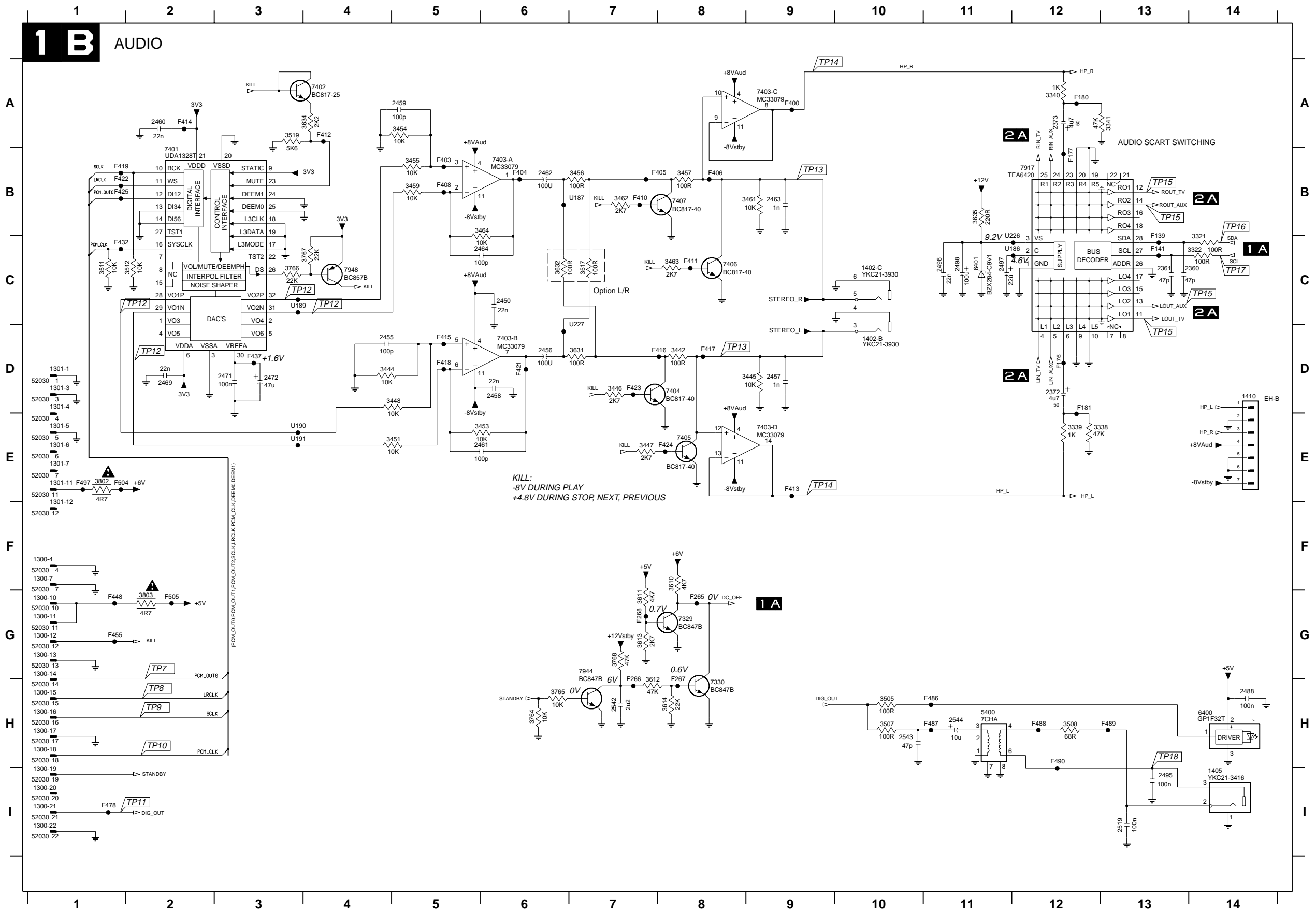


Supply and video switching (/N1B)

**1 A** SUPPLY & VIDEO SWITCHING

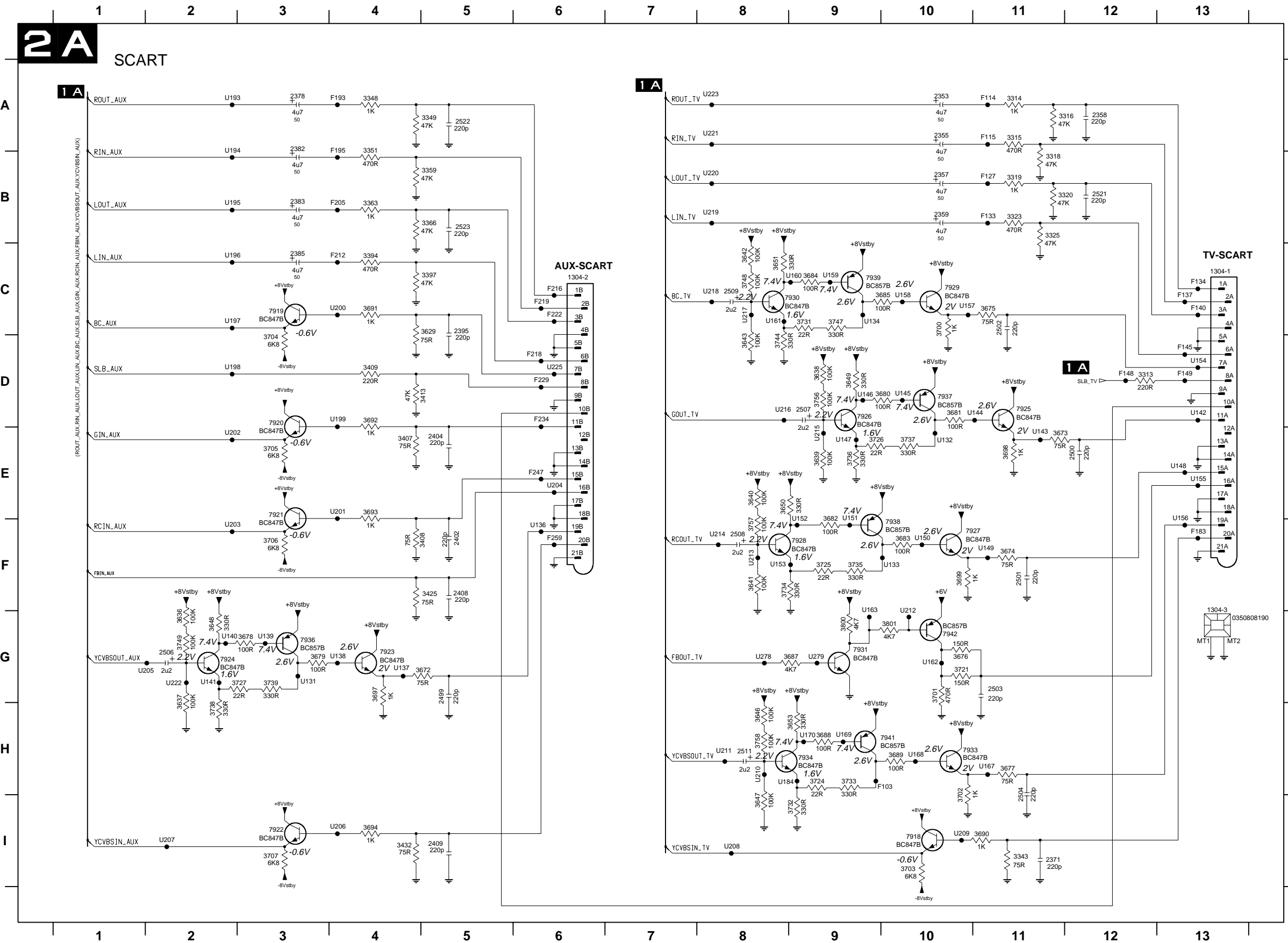


Audio A/V MUX (N1B)



- 1300-10 G1
- 1300-11 G1
- 1300-12 G1
- 1300-13 G1
- 1300-14 G1
- 1300-15 H1
- 1300-16 H1
- 1300-17 H1
- 1300-18 H1
- 1300-19 H1
- 1300-20 I1
- 1300-21 I1
- 1300-22 I1
- 1300-4 F1
- 1300-5 F1
- 1300-6 F1
- 1300-7 F1
- 1300-8 D1
- 1300-9 D1
- 1300-10 D1
- 1300-11 D1
- 1300-12 D1
- 1300-13 D1
- 1300-14 D1
- 1300-15 D1
- 1300-16 D1
- 1300-17 D1
- 1300-18 D1
- 1300-19 D1
- 1300-20 D1
- 1300-21 D1
- 1300-22 D1
- 1300-4 B1
- 1300-5 B1
- 1300-6 B1
- 1300-7 B1
- 1300-8 B1
- 1300-9 B1
- 1300-10 B1
- 1300-11 B1
- 1300-12 B1
- 1300-13 B1
- 1300-14 B1
- 1300-15 B1
- 1300-16 B1
- 1300-17 B1
- 1300-18 B1
- 1300-19 B1
- 1300-20 B1
- 1300-21 B1
- 1300-22 B1
- 1300-4 A1
- 1300-5 A1
- 1300-6 A1
- 1300-7 A1
- 1300-8 A1
- 1300-9 A1
- 1300-10 A1
- 1300-11 A1
- 1300-12 A1
- 1300-13 A1
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- 1300-16 A1
- 1300-17 A1
- 1300-18 A1
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- 1300-5 C1
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- 1300-8 C1
- 1300-9 C1
- 1300-10 C1
- 1300-11 C1
- 1300-12 C1
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- 1300-15 C1
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- 1300-22 E1
- 1300-4 G1
- 1300-5 G1
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- 1300-7 G1
- 1300-8 G1
- 1300-9 G1
- 1300-10 G1
- 1300-11 G1
- 1300-12 G1
- 1300-13 G1
- 1300-14 G1
- 1300-15 G1
- 1300-16 G1
- 1300-17 G1
- 1300-18 G1
- 1300-19 G1
- 1300-20 G1
- 1300-21 G1
- 1300-22 G1
- 1300-4 H1
- 1300-5 H1
- 1300-6 H1
- 1300-7 H1
- 1300-8 H1
- 1300-9 H1
- 1300-10 H1
- 1300-11 H1
- 1300-12 H1
- 1300-13 H1
- 1300-14 H1
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- 1300-16 H1
- 1300-17 H1
- 1300-18 H1
- 1300-19 H1
- 1300-20 H1
- 1300-21 H1
- 1300-22 H1
- 1300-4 I1
- 1300-5 I1
- 1300-6 I1
- 1300-7 I1
- 1300-8 I1
- 1300-9 I1
- 1300-10 I1
- 1300-11 I1
- 1300-12 I1
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- 1300-14 I1
- 1300-15 I1
- 1300-16 I1
- 1300-17 I1
- 1300-18 I1
- 1300-19 I1
- 1300-20 I1
- 1300-21 I1
- 1300-22 I1
- 7944 G7
- 7948 C4
- F139 C13
- F141 C13
- F176 D12
- F177 B12
- F180 A12
- F181 D12
- F265 G8
- F266 H7
- F268 G7
- F400 A9
- F403 B5
- F404 B6
- F405 B8
- F406 B8
- F408 B5
- F410 B7
- F411 C8
- F412 A4
- F413 E9
- F414 A2
- F415 D5
- F416 D8
- F417 D8
- F418 D5
- F421 D6
- F422 B1
- F423 D7
- F424 E8
- F425 B1
- F432 C1
- F437 D3
- F448 G1
- F455 G1
- F478 I1
- F486 H11
- F487 H11
- F488 H12
- F489 H13
- F490 H12
- F497 E1
- F504 E1
- F505 G2
- U186 C12
- U187 B7
- U188 C3
- U189 C3
- U190 E3
- U191 E3
- U226 C12
- U227 D7

Scart panel (N1B)

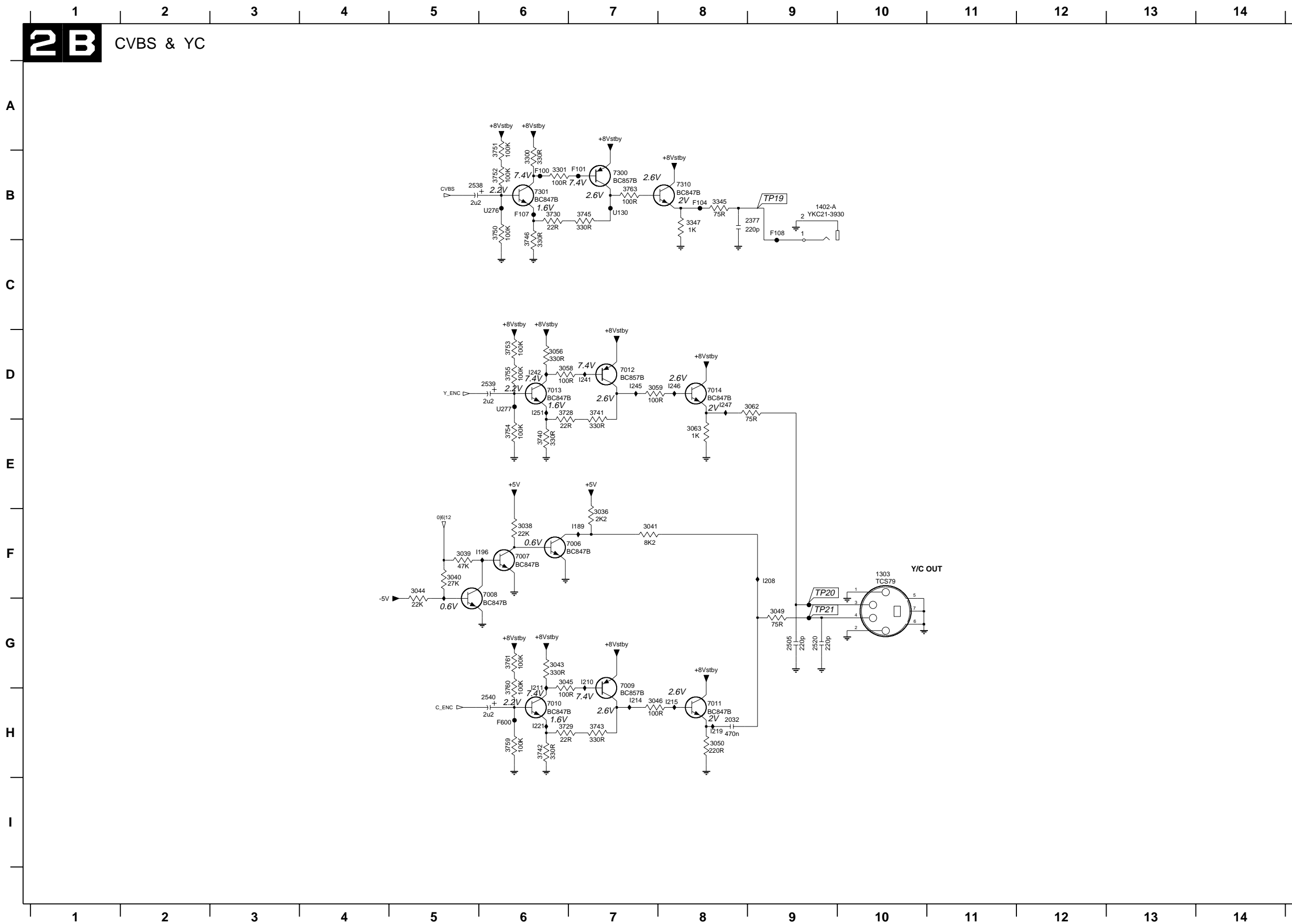


- 1304-1 C13
- 1304-2 C6
- 1304-3 G13
- 2353 A10
- 2355 A10
- 2357 B10
- 2358 A12
- 2359 B10
- 2371 H11
- 2378 A3
- 2382 A3
- 2383 B3
- 2385 C3
- 2395 C5
- 2402 F5
- 2404 E5
- 2408 F5
- 2409 I5
- 2499 G5
- 2500 E12
- 2501 F11
- 2502 C11
- 2503 G11
- 2504 H11
- 2506 G2
- 2507 D9
- 2508 F8
- 2509 C8
- 2511 H8
- 2521 B12
- 2522 A5
- 2523 B5
- 3113 D12
- 3114 A11
- 3115 A11
- 3116 A12
- 3118 B11
- 3119 B11
- 3120 B12
- 3123 B11
- 3125 B11
- 3143 I11
- 3148 A4
- 3149 A5
- 3151 B4
- 3159 B5
- 3163 B4
- 3165 B4
- 3167 C4
- 3168 C4
- 3169 C4
- 3170 H9
- 3171 H9
- 3172 H9
- 3173 H9
- 3174 H9
- 3175 F9
- 3176 E9
- 3177 G3
- 3178 C9
- 3179 C9
- 3180 G9
- 3181 G10
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- 3460 H10
- 3461 H10
- 3462 H10
- 3463 H10
- 3464 H10
- 3465 H10
- 3466 H10
- 3467 H10
- 3468 H10
- 3469 H10
- 3470 H10
- 3471 H10
- 3472 H10
- 3473 H10
- 3474 H10
- 3475 H10
- 3476 H10
- 3477 H10
- 3478 H10
- 3479 H10
- 3480 H10
- 3481 H10
- 3482 H10
- 3483 H10
- 3484 H10
- 3485 H10
- 3486 H10
- 3487 H10
- 3488 H10
- 3489 H10
- 3490 H10
- 3491 H10
- 3492 H10
- 3493 H10
- 3494 H10
- 3495 H10
- 3496 H10
- 3497 H10
- 3498 H10
- 3499 H10
- 3500 H10

CVBS / YC panel (N1B)

**2B**

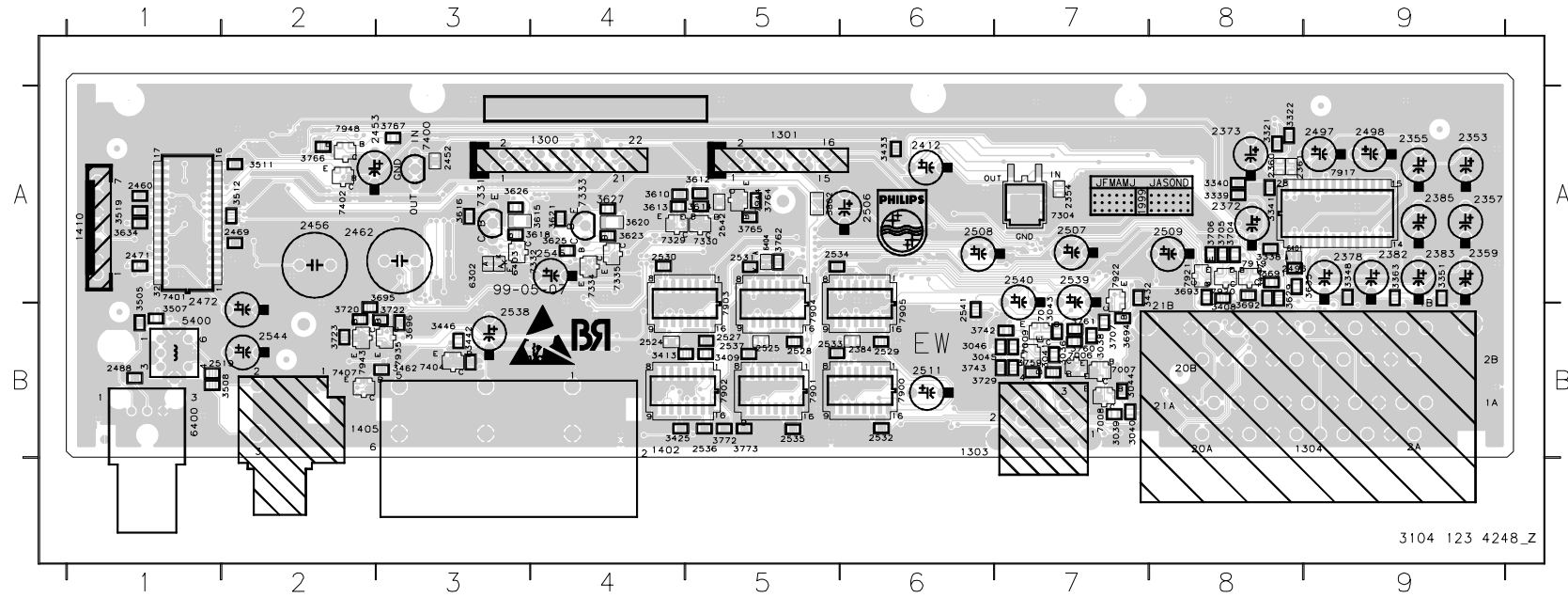
CVBS & YC



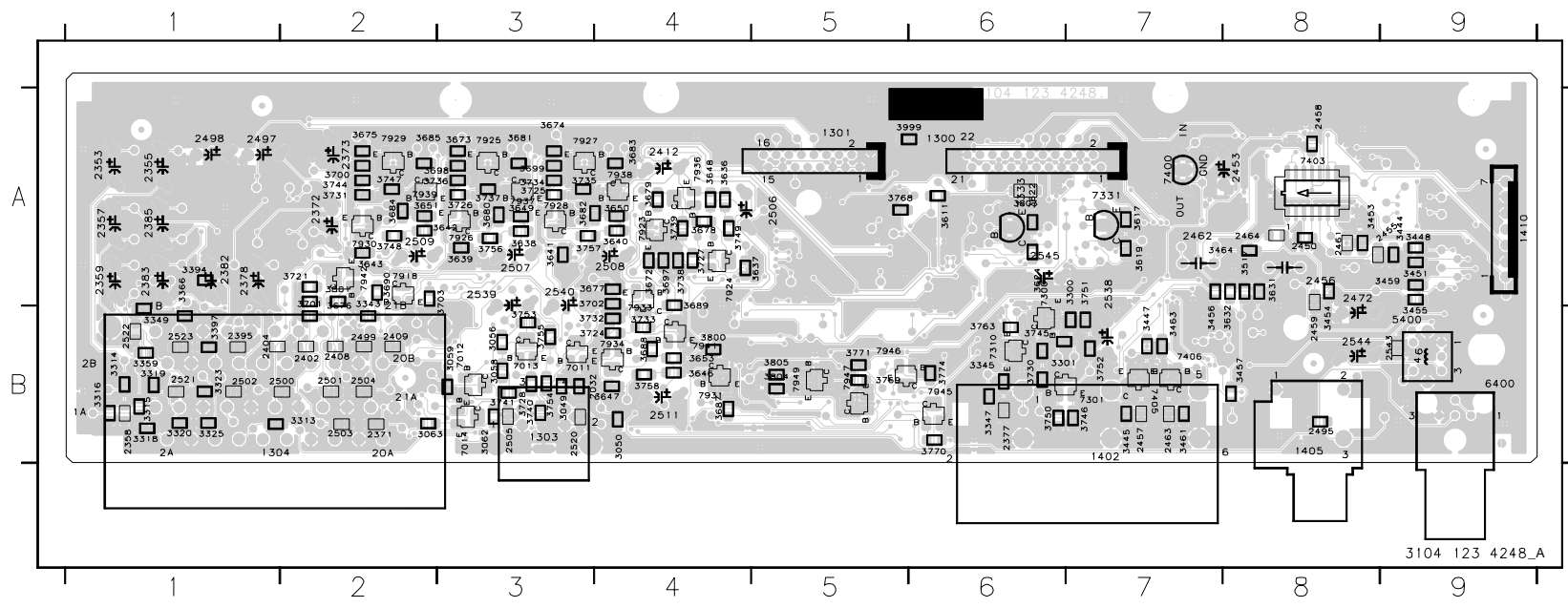
- 1303 F10
- 1402-A B9
- 2032 H8
- 2377 B9
- 2505 G9
- 2520 G9
- 2538 B5
- 2539 D6
- 2540 H6
- 3036 F7
- 3038 F6
- 3039 F5
- 3040 F5
- 3041 F7
- 3043 G6
- 3044 F5
- 3045 G6
- 3046 H7
- 3049 G9
- 3050 H8
- 3056 D6
- 3058 D6
- 3059 D7
- 3062 D9
- 3063 E8
- 3300 B6
- 3301 B6
- 3345 B8
- 3347 B8
- 3729 H6
- 3730 B6
- 3740 E6
- 3741 D7
- 3742 H6
- 3743 H7
- 3745 B7
- 3746 B6
- 3750 B6
- 3751 A6
- 3752 B6
- 3753 D6
- 3754 E6
- 3755 D6
- 3759 H6
- 3760 G6
- 3761 G6
- 3763 B7
- 3899 I1
- 7006 F6
- 7007 F6
- 7008 F6
- 7009 G7
- 7010 H6
- 7011 H8
- 7012 D7
- 7013 D6
- 7014 D8
- 7300 B7
- 7301 B6
- 7310 B8
- F100 B6
- F101 B7
- F104 B8
- F107 B6
- F108 B9
- F600 H6
- I189 F7
- I191 F6
- I196 F6
- I200 G5
- I208 F9
- I210 G7
- I211 G6
- I214 H7
- I215 H8
- I219 H8
- I221 H6
- I241 D7
- I242 D6
- I245 D7
- I246 D8
- I247 D8
- I251 D6
- U130 B7
- U192 G9
- U224 G9
- U276 B6
- U277 D6

**A/V Mux panel (N1B)**

1300 A4	2357 A9	2385 A9	2498 B1	2524 B4	2535 B5	3036 B7	3322 A8	3409 B5	3508 B1	3618 A3	3691 A8	3720 B2	3764 A5	6401 A8	7330 A5	7407 B2	7921 A8
1301 A5	2359 A9	2412 A6	2496 A8	2525 B5	2536 B5	3038 B7	3338 A8	3413 B5	3511 A2	3620 A4	3692 A8	3722 B3	3765 A5	6403 A3	7331 A3	7900 B6	7922 A7
1303 B7	2360 A8	2452 A3	2497 A9	2527 B5	2537 B5	3039 B7	3339 A8	3425 B4	3512 A2	3621 A4	3693 A8	3723 B2	3766 A2	6404 A5	7332 A3	7901 B5	7935 B3
1304 B9	2361 A8	2453 A2	2498 A9	2528 B5	2538 B3	3040 B7	3340 A8	3432 A7	3519 A1	3623 A4	3694 B7	3729 B7	3767 A3	7006 B7	7333 A4	7902 B4	7943 B2
1402 B3	2372 A8	2456 A2	2506 A6	2529 B6	2539 A7	3041 B7	3341 A8	3433 A6	3610 A4	3625 A4	3695 B2	3742 B7	3772 B5	7007 B7	7334 A4	7903 B4	7944 A5
1405 B2	2373 A8	2460 A1	2507 A7	2530 A4	2540 A7	3043 B7	3348 A9	3442 B3	3612 A5	3626 A3	3696 B3	3743 B7	3773 B5	7008 B7	7335 A4	7904 B5	7948 A2
1410 A1	2378 A9	2462 A3	2508 A6	2531 A5	2541 B6	3044 B7	3351 A9	3446 B3	3613 A4	3627 A4	3704 A8	3759 B7	3802 A5	7009 B7	7400 A3	7905 B6	
2353 A9	2382 A9	2469 A2	2509 A8	2532 B6	2542 A5	3045 B7	3363 A9	3462 B3	3614 A5	3629 A8	3705 A8	3760 B7	3805 A5	7010 B7	7401 A1	7917 A9	
2354 A7	2383 A9	2471 A1	2511 B6	2533 B5	2544 B2	3046 B7	3407 A8	3505 B1	3615 A3	3634 A1	3706 A8	3761 B7	6302 A3	7304 A7	7402 A2	7919 A8	
2355 A9	2384 B6	2472 B2	2519 B1	2534 A5	2545 A4	3321 A8	3408 A8	3507 B1	3616 A3	3635 A8	3707 B7	3762 A5	6400 B1	7329 A4	7404 B3	7920 A8	

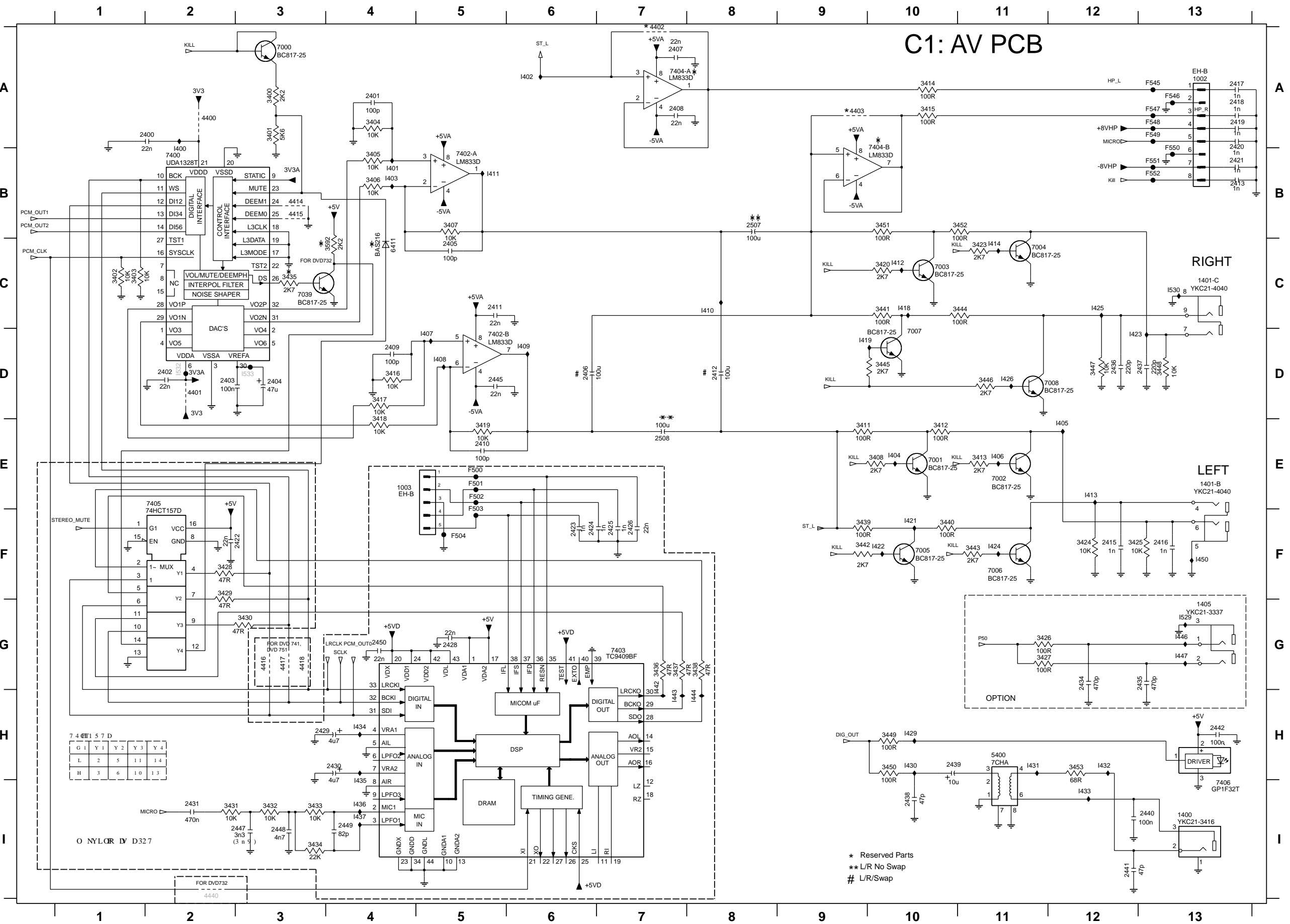


2032 B3	2504 B2	3323 B1	3464 A8	3653 B4	3701 B2	3746 B7	3805 B5	7934 B4
2358 B1	2505 B3	3325 B1	3517 A8	3672 A4	3702 A4	3747 A2	3999 A6	7936 A4
2371 B2	2520 B3	3343 B2	3611 A6	3673 A3	3703 A2	3748 A2	7011 B5	7937 A3
2377 B6	2521 B1	3345 B6	3617 A7	3674 A3	3721 A2	3749 A4	7012 B3	7938 A4
2395 B1	2522 B1	3347 B6	3619 A7	3675 A2	3724 B4	3750 B6	7013 B3	7939 A2
2402 B2	2523 B1	3349 B1	3622 A6	3676 A2	3725 A3	3751 B7	7014 B3	7941 B4
2404 B1	2543 B9	3359 B1	3624 A6	3677 A4	3726 A3	3752 B7	7300 B6	7942 A2
2408 B2	3049 B3	3366 B1	3631 A8	3678 A4	3727 A4	3753 B3	7301 B6	7945 B6
2409 B2	3050 B4	3394 A1	3632 A8	3679 A4	3728 B3	3754 B3	7310 B6	7946 B5
2450 A8	3056 B3	3397 B1	3636 A4	3680 A3	3730 B6	3755 B3	7403 A8	7947 B5
2459 A8	3058 B3	3444 A9	3637 A4	3681 A3	3731 A2	3756 A3	7405 B7	7949 B5
2457 B7	3059 B3	3445 B7	3638 A3	3682 A4	3732 B2	3757 A3	7406 B7	
2458 A8	3062 B3	3447 B7	3639 A3	3683 A4	3733 B4	3758 B4	7918 A2	
2459 A8	3063 B2	3448 A9	3640 A4	3684 A2	3734 A3	3763 B6	7923 A4	
2461 A8	3300 B7	3451 A9	3641 A3	3685 A2	3735 A3	3768 A5	7924 A4	
2463 B7	3301 B6	3453 A8	3642 A2	3687 B4	3736 A3	3769 B5	7925 A3	
2464 A8	3313 B1	3454 A8	3643 A2	3688 B4	3737 A3	3770 B6	7926 A3	
2495 B8	3314 B1	3455 A9	3646 B4	3689 A4	3738 A4	3771 B5	7927 A3	
2499 B2	3315 B1	3456 A7	3647 B4	3690 A2	3739 A4	3774 B6	7928 A3	
2500 B2	3316 B1	3457 B8	3648 A4	3697 A4	3740 B3	3800 B4	7929 A2	
2501 B2	3318 B1	3459 A9	3649 A3	3698 A3	3741 B3	3801 A2	7930 A5	
2502 B1	3319 B1	3461 B7	3650 A4	3699 A3	3744 A2	3803 A6	7931 B4	
2503 B2	3320 B1	3463 B7	3651 A2	3700 A2	3745 B6	3804 B5	7933 A4	

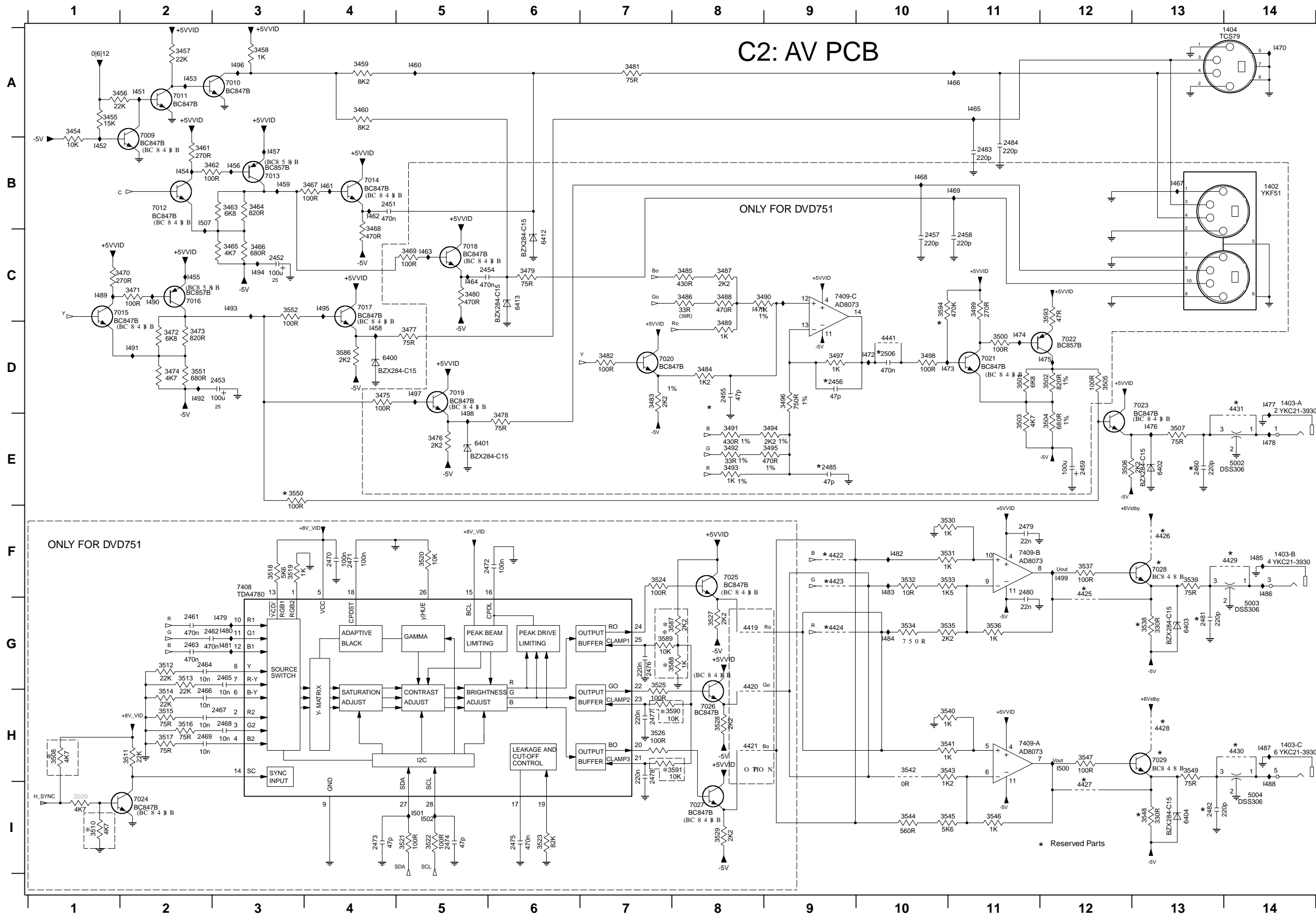




A/V board (A1B, /S1G, /U1B)



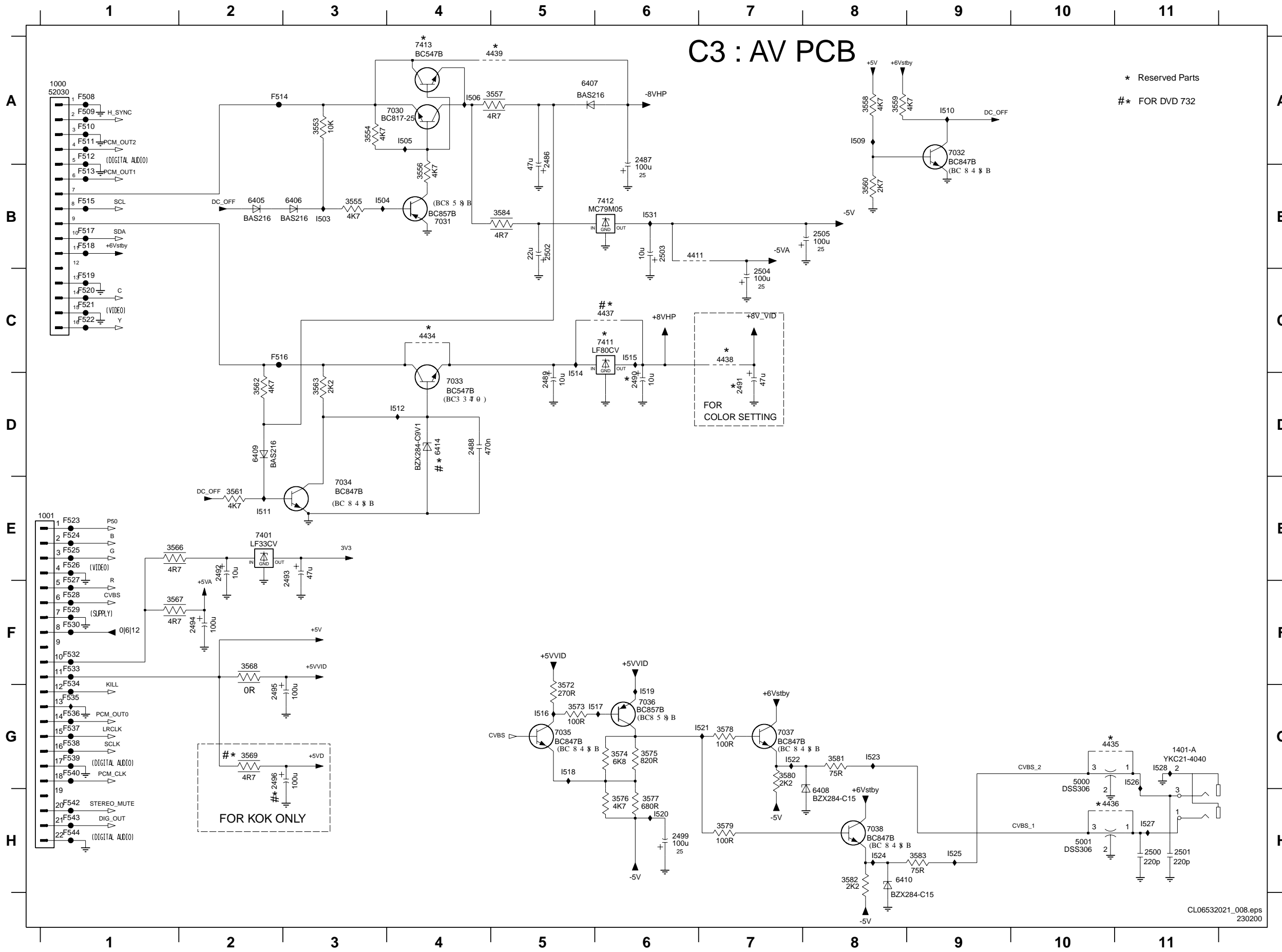
A/V board (A1B, /S1G, /U1B)



1402 B14	3526 H7	I481 G3
1403-A D14	3527 G8	I482 F10
1403-B F14	3528 H8	I483 F10
1403-C H14	3529 I8	I484 G10
1404 A14	3530 F10	I485 F14
2451 B4	3531 F10	I486 F14
2452 C3	3532 F10	I487 H14
2453 D3	3533 F10	I488 H14
2454 C5	3534 G10	I489 C1
2455 D8	3535 G10	I490 C2
2456 D9	3536 G11	I491 D2
2457 C10	3537 F12	I492 D2
2458 C11	3538 G13	I493 C3
2459 E12	3539 F13	I494 C3
2460 E13	3540 H10	I495 C4
2461 G2	3541 H10	I496 A3
2462 G2	3542 H10	I497 D5
2463 G2	3543 H10	I498 E5
2464 G2	3544 I10	I499 F12
2465 G3	3545 I10	I500 H12
2466 H2	3546 I11	I501 I5
2467 H3	3547 H12	I502 I5
2468 H3	3548 I13	I507 B2
2469 H2	3549 H13	4441 D10
2470 F4	3550 E3	
2471 F4	3551 D2	
2472 F6	3552 C3	
2473 H4	3556 D4	
2474 I5	3587 G8	
2475 I6	3588 G8	
2476 G7	3589 G7	
2477 H7	3590 H8	
2478 H7	3591 H8	
2479 F11	3593 C12	
2480 F11	3594 C10	
2481 G13	4420 G8	
2482 I13	4421 H8	
2483 B11	4422 B11	
2484 B11	4423 F9	
2485 E9	4424 G9	
2506 D10	4425 F12	
3454 A1	4426 F13	
3455 A1	4427 I12	
3456 A1	4428 H13	
3457 A2	4429 F14	
3458 A3	4430 H14	
3459 A4	4431 D14	
3460 A4	5002 E14	
3461 B2	5003 G14	
3462 B2	5004 I14	
3463 B3	5005 I14	
3464 B3	6400 D4	
3465 C3	6401 E5	
3466 C3	6402 E13	
3467 B4	6403 G13	
3468 C4	6404 I13	
3469 C5	6412 C6	
3470 C2	6413 C6	
3471 C2	7009 E2	
3472 D2	7010 F3	
3473 D2	7011 A2	
3474 D2	7012 B2	
3475 D4	7013 B3	
3476 E5	7014 B4	
3477 D5	7015 C1	
3478 E6	7016 C2	
3479 C6	7017 C4	
3480 C5	7018 C5	
3481 A7	7019 D5	
3482 D7	7020 D7	
3483 D7	7021 D11	
3484 D8	7022 D12	
3485 C8	7023 D13	
3486 C8	7024 I2	
3487 C8	7025 F8	
3488 C8	7026 H8	
3489 D8	7027 I8	
3490 C8	7028 F13	
3491 E8	7029 H13	
3492 E8	7408 F3	
3493 E8	7409-A H11	
3494 E9	7409-B F11	
3495 E9	7409-C C9	
3496 D9	I451 A2	
3497 D9	I452 B1	
3498 D10	I453 A2	
3499 C11	I454 B2	
3500 D11	I455 C2	
3501 D11	I456 B3	
3502 D12	I457 B3	
3503 E11	I458 D4	
3504 E12	I459 B3	
3505 D12	I460 A5	
3506 E12	I461 B4	
3507 E13	I462 B4	
3508 H1	I463 C5	
3509 I1	I464 C5	
3510 I1	I465 A11	
3511 H2	I466 A11	
3512 G2	I467 B13	
3513 G2	I468 B10	
3514 H2	I469 B11	
3515 H2	I470 A14	
3516 H2	I471 C8	
3517 H2	I472 D10	
3518 F3	I473 D10	
3519 F3	I474 D11	
3520 F5	I475 D12	
3521 I5	I476 E13	
3522 I5	I477 D14	
3523 I6	I478 E14	
3524 F7	I479 G3	
3525 G7	I480 G3	

A/V board (A1B, /S1G, /U1B)

C3 : AV PCB

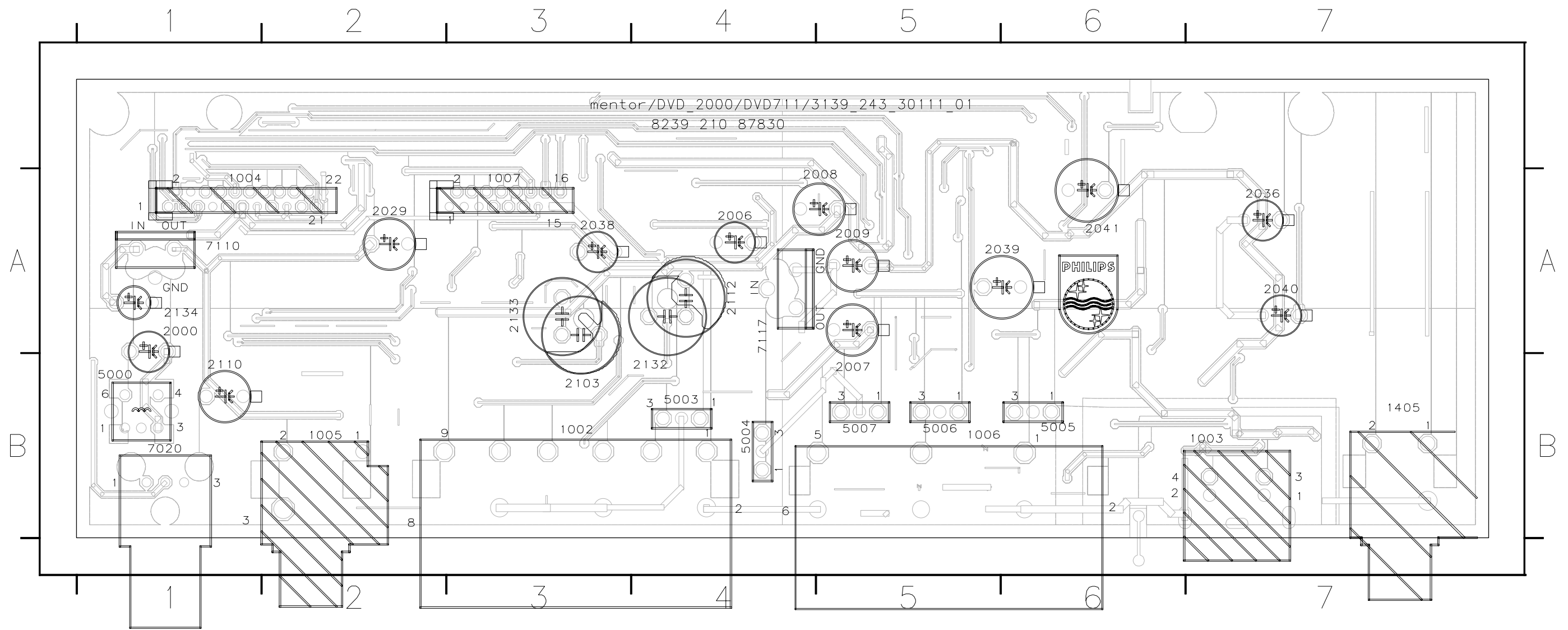


\* Reserved Parts  
\*\* FOR DVD 732

1000 A1	F534 G1
1001 E1	F535 G1
1401-A G11	F536 G1
2486 A5	F537 G1
2487 A6	F538 G1
2488 D4	F539 G1
2489 D5	F540 G1
2490 D6	F542 H1
2491 D7	F543 H1
2492 E2	F544 H1
2493 E3	I503 B3
2494 F2	I504 B3
2495 G2	I505 A4
2496 G2	I506 A4
2499 H6	I509 A8
2500 H11	I510 A9
2501 H11	I511 E2
2502 B5	I512 D4
2503 B6	I514 D5
2504 C7	I515 C6
2505 B8	I516 G5
3553 A3	I517 G6
3554 A3	I518 G5
3555 B3	I519 G6
3556 B4	I520 H6
3557 A5	I521 G7
3558 A8	I522 G7
3559 A8	I523 G8
3560 B8	I524 H8
3561 E2	I525 H9
3562 D2	I526 G11
3563 D3	I527 H11
3566 E1	I528 G11
3567 F1	I531 B6
3568 F2	
3569 G2	
3572 G5	
3573 G5	
3574 G6	
3575 G6	
3576 H6	
3577 H6	
3578 G7	
3579 H7	
3580 G7	
3581 G8	
3582 H8	
3583 H9	
3584 B5	
4411 B6	
4434 C4	
4435 G10	
4436 H10	
4437 C6	
4438 C7	
4439 A5	
5000 G10	
5001 H10	
6405 B2	
6406 B3	
6407 A5	
6408 H8	
6409 D2	
6410 H8	
6414 D4	
7030 A4	
7031 B4	
7032 A9	
7033 D4	
7034 E3	
7035 G5	
7036 G6	
7037 G7	
7038 H8	
7401 E2	
7411 C6	
7412 B6	
7413 A4	
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F511 A1	
F512 A1	
F513 B1	
F514 A2	
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F516 C1	
F517 B1	
F518 B1	
F519 C1	
F520 C1	
F521 C1	
F522 C1	
F523 E1	
F524 E1	
F525 E1	
F526 E1	
F527 F1	
F528 F1	
F529 F1	
F530 F1	
F531 F1	
F532 F1	
F533 F1	

**AV Pwb (A1B, /S1G, /U1B)**

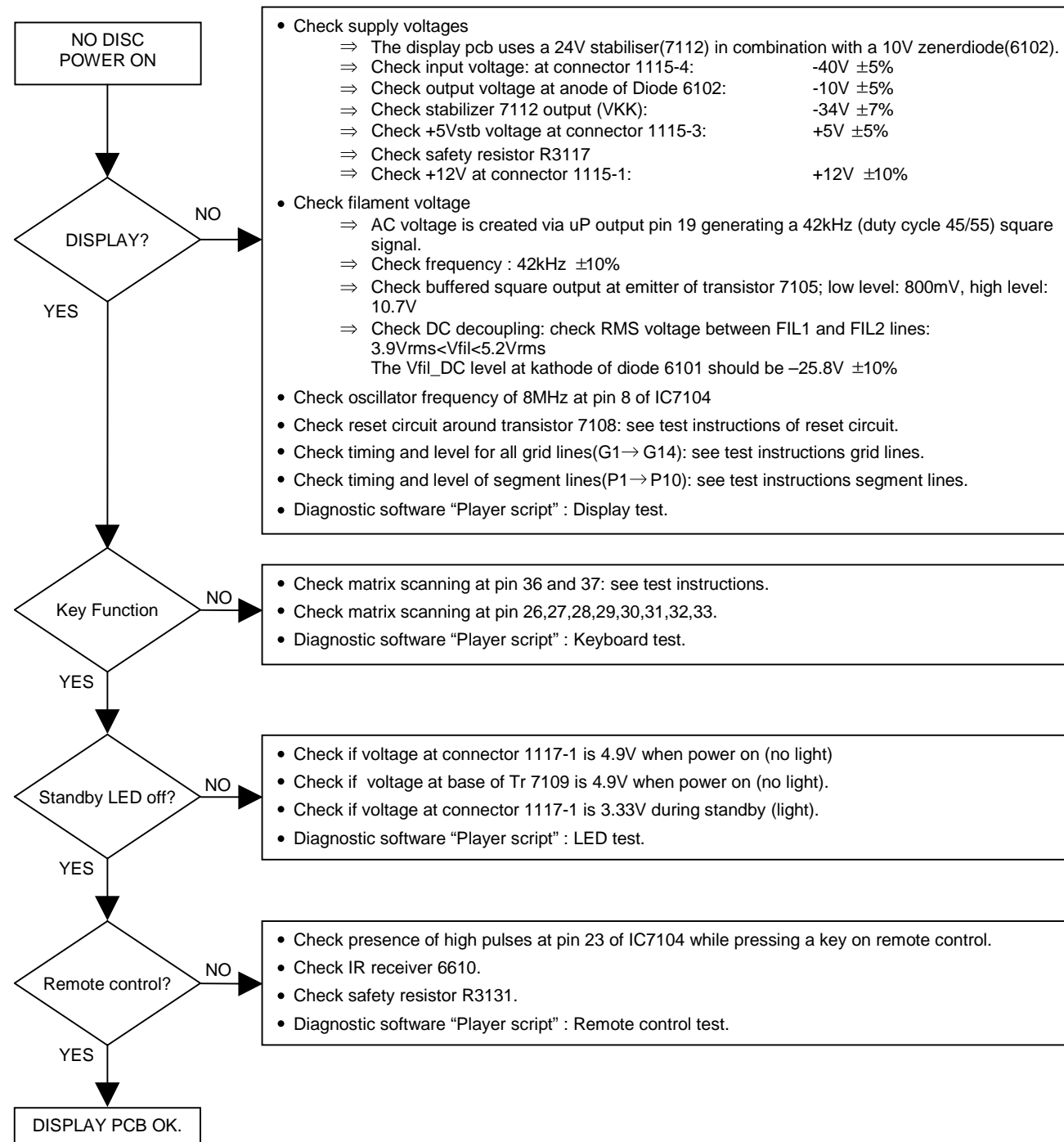
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1003	B7	1006	B5	2000	A1	2008	A5	2036	A7	2040	A7	2110	B1	2133	A3	5003	B4	5006	B5	7110	A1
1004	A1	1007	A3	2006	A4	2009	A5	2038	A3	2041	A6	2112	A4	2134	A1	5004	B4	5007	B5	7117	A4





## 12. TROUBLESHOOTING

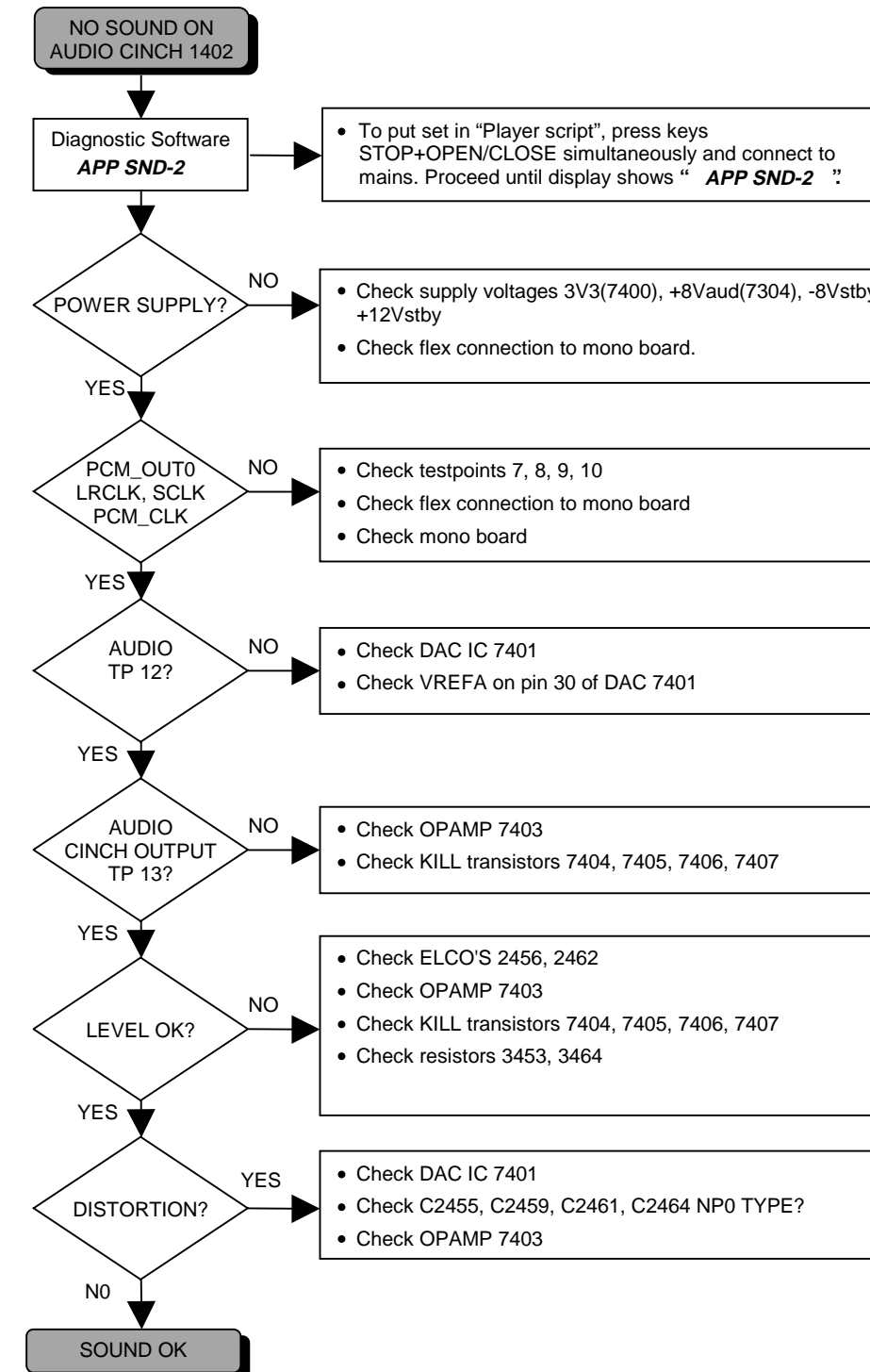
### TROUBLESHOOTING DISPLAY BOARD

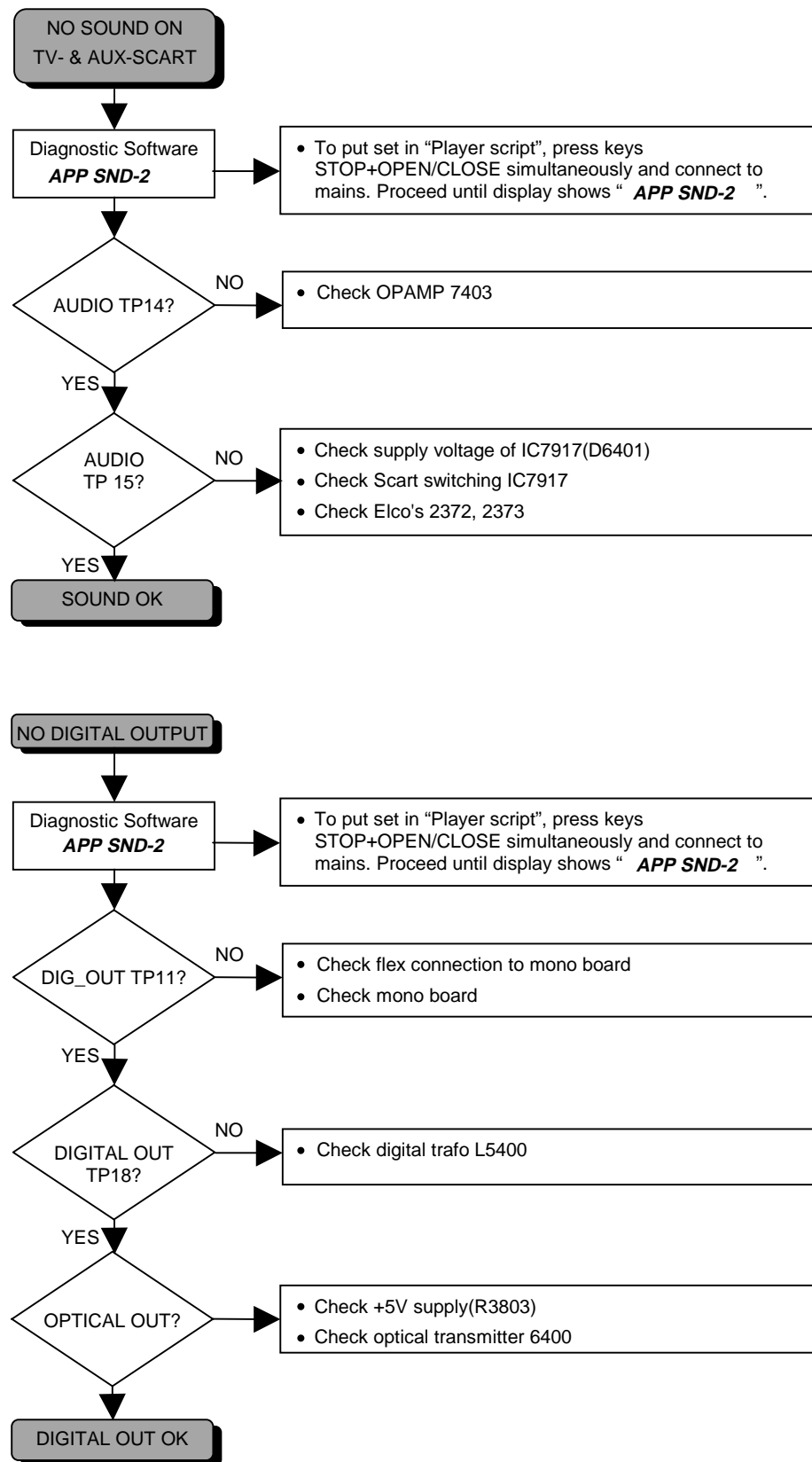


### TROUBLESHOOTING A/V BOARD

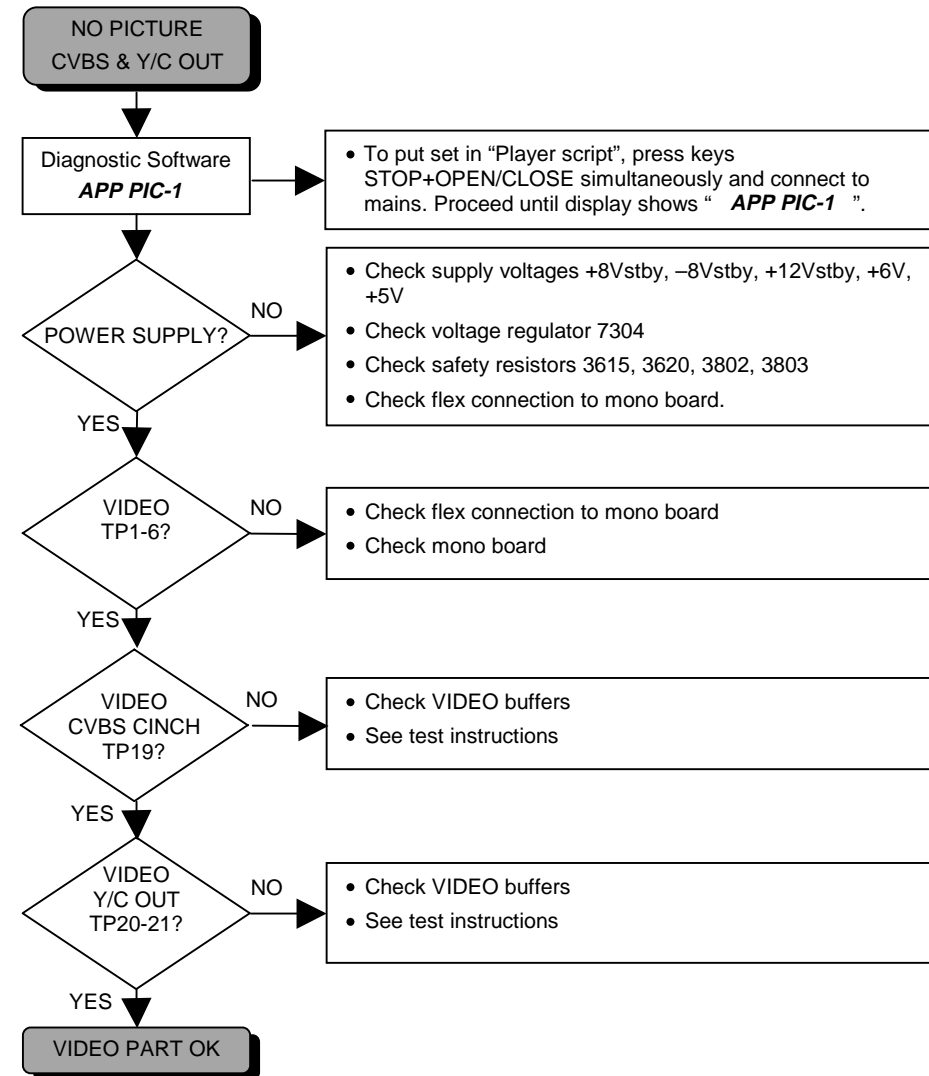
Testing of A/V board can be done using diagnostic software "Player script". Mono board is used to generate a sinus with the soundtest SND-2 or a VIDEO signal with the picture test PIC-1. See description in chapter "Diagnostic Software : Script Interfaces"

#### AUDIO PART





**VIDEO PART**



NO PICTURE SCART  
SCART SWITCHING

Diagnostic Software  
**SCART DVD**

- To put set in "Player script", press keys STOP+OPEN/CLOSE simultaneously and connect to mains. Proceed until display shows "**SCART DVD**".

PICTURE TV?

- NO
- Check "0/6/12" on connector 1300-8 = +10V
  - Check flex connection to mono board
  - Check "SELECT" = 0V, "SELECT HIGH" = 0V
  - Check transistors 7935, 7943
  - Check switches 7900-7905
  - Check "SLB\_TV: 9V, "FBOUT\_TV: 5V
  - Check video buffers, see test instructions.

YES

Diagnostic Software  
**SCART LOOP**

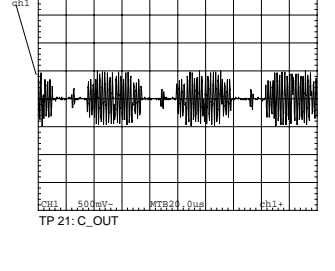
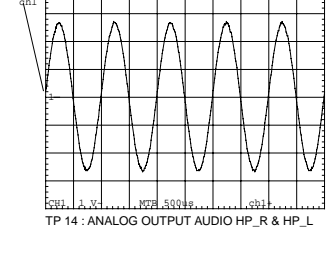
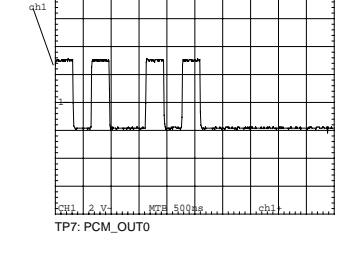
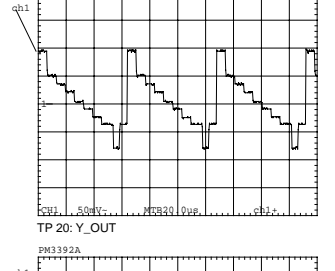
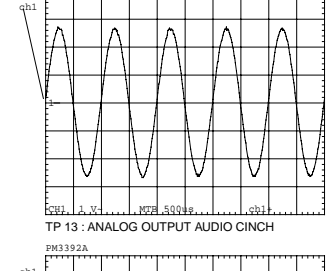
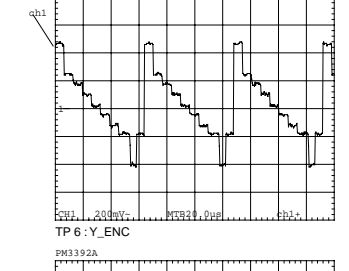
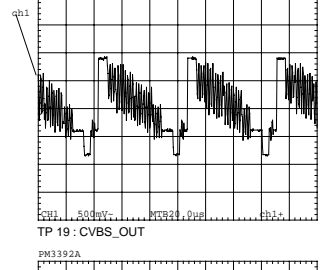
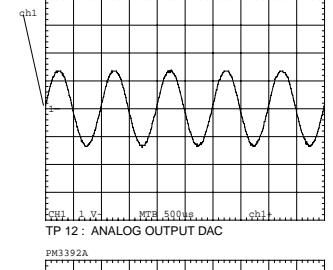
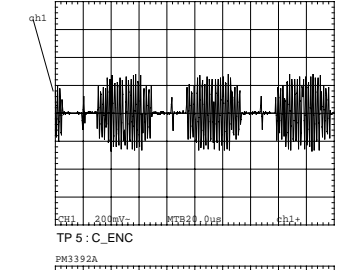
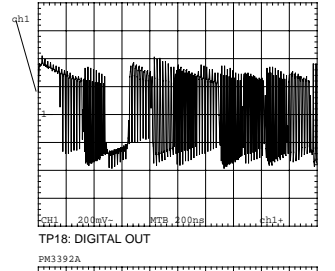
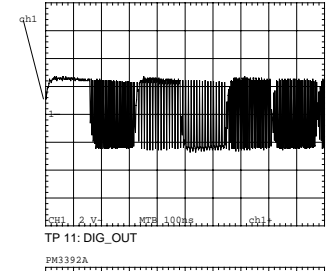
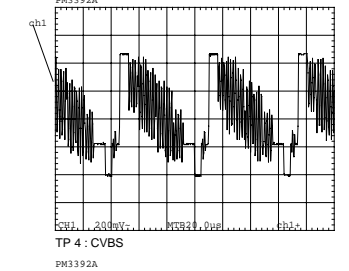
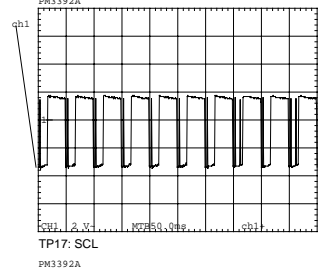
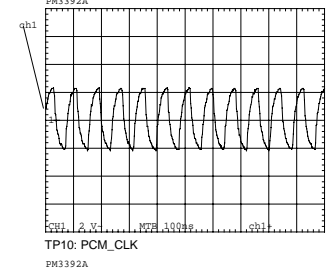
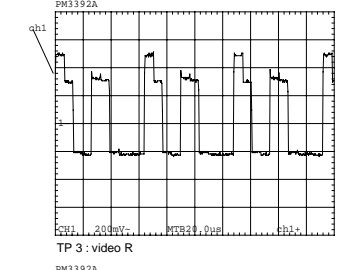
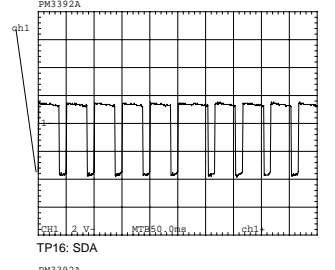
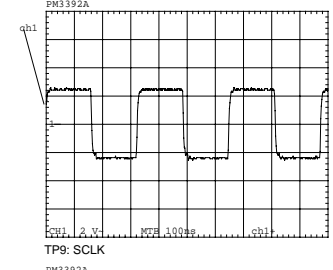
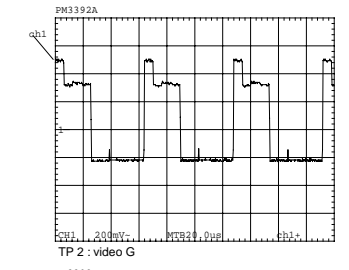
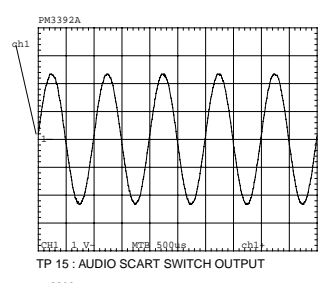
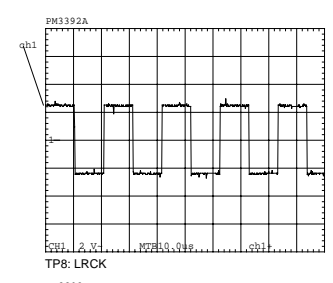
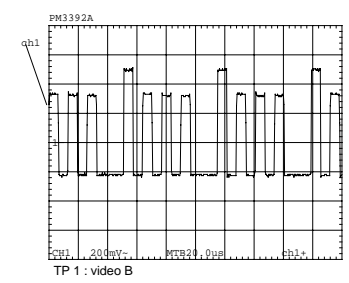
- press NEXT. Display shows: "**SCART LOOP** Pressing PREVIOUS will return to "**SCART DVD**".

PICTURE AUX/VCR IN ON TV?

- NO
- Check "0/6/12" on connector 1300-8 = 0V
  - Check flex connection to mono board
  - Check "SELECT" = 6V, "SELECT HIGH" = 12V
  - Check transistors 7935, 7943
  - Check switches 7900-7905
  - Check "SLB\_TV = 0V, "FBOUT\_TV = 0V.
  - Check video buffers, see test instructions.

YES

SCART SWITCHING  
OK





### 13. DIAGNOSTIC SOFTWARE : SCRIPT INTERFACES

#### 13.1 DEALER SCRIPT

##### 13.1.1 Purpose of Dealer Script

The dealer script can give a diagnosis on a standalone DVD player; no other equipment is needed to perform a number of hardware tests to check if the DVD player is faulty. The diagnosis is simply a "error" or "pass" message; no indication is given of faulty hardware modules. Only tests within the scope of the diagnostic software will be executed hence only faults within this scope can be detected.

##### 13.1.2 Contents of Dealer Script

The dealer script executes all diagnostic nuclei that do not need any user interaction and are meaningful on a standalone DVD player.

The nuclei called in the dealer script are the following (the number after each nucleus name corresponds with the number being on the local display when the nucleus is executed during the dealer script):

Nucleus	Description
VideoColSetupComm	Checks the I2C interface with the RGB video processor on the Audio/Video board (only for DVD players with RGB video processor).
VideoScartSwComm	Checks the I2C interface with the scart switch on the Audio/Video board
PapChksFl	Calculate and verify checksum of FLASH memory.
PapDramWrR	Pattern test of all locations in the DRAM(s).
PapI2cDisp	Checks the I2C interface with the slave processor on the display PCB.
PapS2bEcho	Checks the I2C interface to the basic engine.
PapI2cNvram	Checks the I2C interface with the NVRAM.
PapNvramWrR	Pattern test of all locations in the NVRAM
CompSdramWrR	Pattern test of all locations in the SDRAM(s).

Figure 13-1

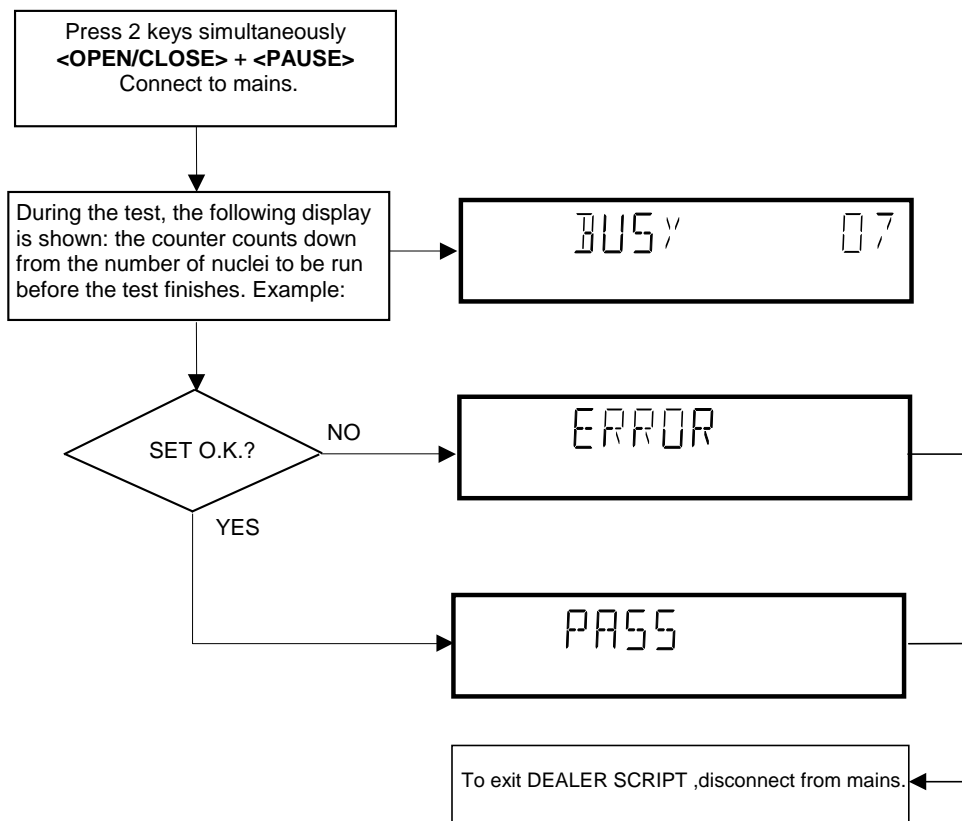


Figure 13-2

## 13.2 PLAYER SCRIPT

### 13.2.1 Purpose of Player Script

The Player script will give the opportunity to perform a test that will determine which of the DVD player's modules are faulty, to read the error log and error bits and to perform an endurance loop test. To successfully perform the tests, the DVD player must be connected to a tv set to check the output of a number of nuclei. For DVDv2b a multi-channel amplifier, a set of 6 boxes and an external video source are necessary to test. To be able to check results of certain nuclei, the player script expects some interaction of the user (i.e. to approve a test picture or a test sound). Some nuclei (e.g. nuclei that test functionality of the Basic Engine module) require that the DVD player itself is opened, to enable the user to observe moving parts and approve their movement visually. Only tests within the scope of the diagnostic software will be executed hence only faults within this scope can be detected.

### 13.2.2 Contents of Player Script

The player script contains all nuclei that are useful on a DVD player that is connected to a tv-set and help to determine which module of the DVD player is faulty, as well as to read out the contents of the error logs.

### 13.2.3 Structure of Player Script

The player script consists of a set of nuclei testing the three hardware modules in the DVD player: the Display PWB, the Digital PWB and the Basic Engine.

Nuclei run by the player test need some user interaction; in the next paragraph this interaction is described. The player test is done in two phases:

1. Interactive tests: this part of the player test depends strongly on user interaction and input to determine nucleus results and to progress through the full test. Reading the error log and error bits information can be useful to determine any errors that occurred recently during normal operation of the DVD player.
2. The loop test will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely.

### 13.2.4 Survey

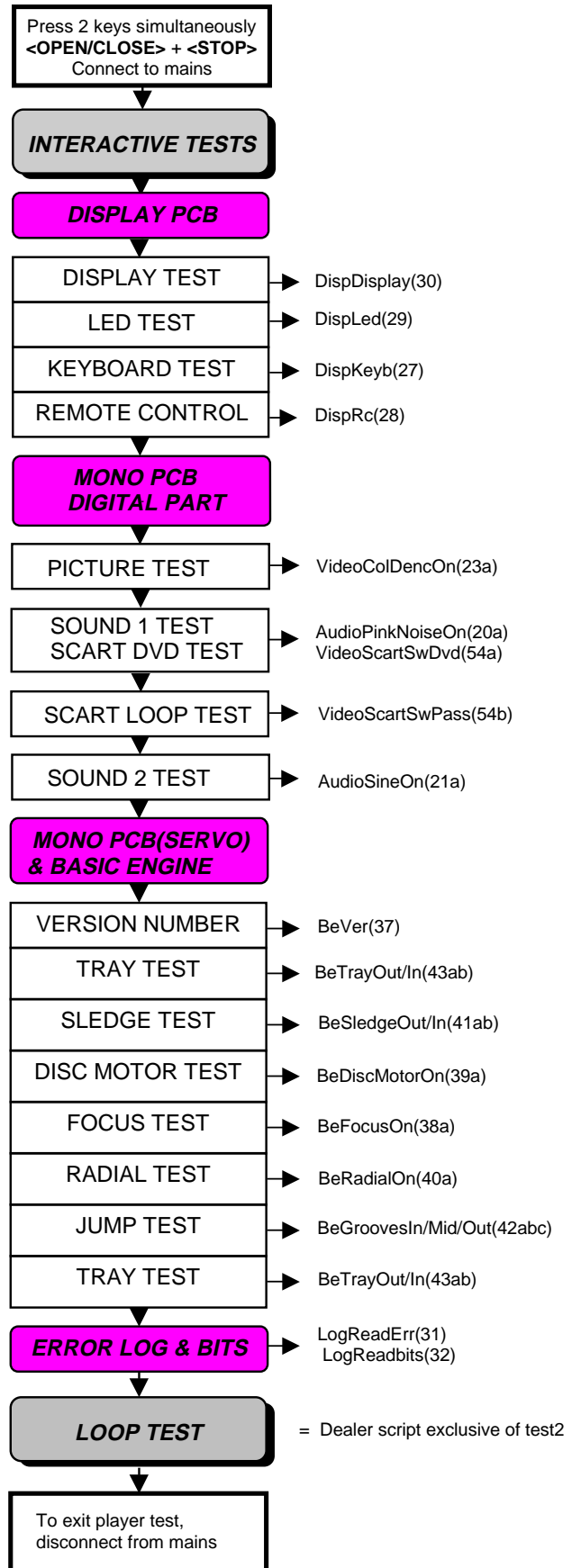


Figure 13-3

## 14. INTERACTIVE TESTS

### 14.1 DISPLAY PCB

#### 14.1.1 DISPLAY TEST

The display test is performed by nucleus DispDisplay. By putting a series of test patterns on the local display, the local display is tested. To step through all different patterns, the user must either press PLAY (pattern is ok) or PAUSE (pattern was incorrect) to proceed to the next pattern. The display of patterns is continued in a cyclic manner until the user presses NEXT. If the user presses NEXT before all display patterns are tested, the DispDisplay nucleus will return TRUE (display test successful).

#### 14.1.2 LED TEST

The LED(s) on the DVD player is (are) tested by nucleus DispLed. The user must check if the LED(s) is (are) lighted; if it is, press PLAY, if it is not, press PAUSE. By pressing NEXT the script will proceed to the next test. If the user presses NEXT before PLAY or PAUSE, the DispLed nucleus will return TRUE (LED test successful).

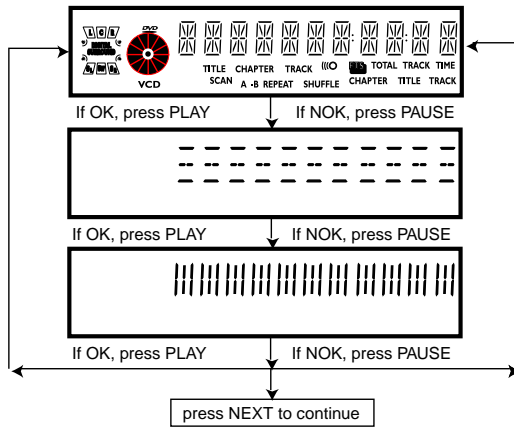


Figure 14-1

#### 14.1.3 KEYBOARD TEST

The keyboard of the DVD player is tested by nucleus DispKeyb. The user is expected to press all keys on the local keyboard once. The code of the key pressed is shown on the local display (1 hexadecimal digit) immediately followed by a (hexadecimal) number indicating how many times that key has been pressed. Example of the local display during this test:

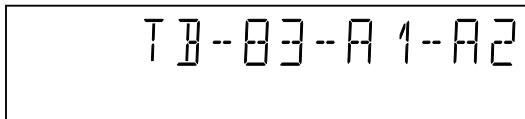


Figure 14-2

The key-codes displayed on the local display will scroll from right to left when the display gets full, the text "tb-" will remain on display.

key id.	key
0	PLAY
1	NEXT
2	PREVIOUS
3	PAUSE
4	STOP
5	OPEN / CLOSE
6	SOUND

Figure14-3

If any keys are detected more than once (due to hardware error), the key-code is displayed twice (or more), with the second digit increased by 1.

If the user does not press all keys minimally once (in any order), the DispKeys nucleus will return FALSE and cause an error in the overall result of the player script.

The user can leave the keyboard test by pressing the NEXT key on the local display of the DVD player for at least one full second.

The result of the keyboard test is shown on local display as follows:

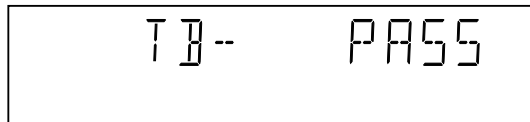


Figure 14-4

Or

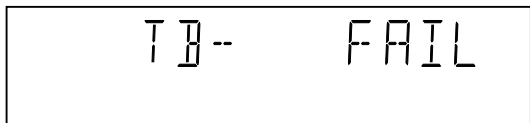


Figure 14-5

Pressing NEXT on the local keyboard again will proceed to the next text.

#### 14.1.4 REMOTE CONTROL TEST

The remote control of the DVD player is tested by nucleus DispRc. The user must press any key on the remote control just once. The codes of the key pressed will be shown on the local display in hexadecimal format. Example:

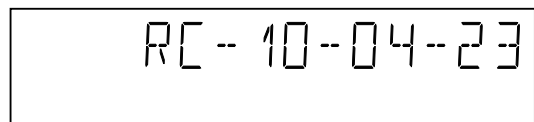


Figure 14-6

In this example 23 is the hexadecimal code of the pressed RC key. The user can leave the remote-control test by pressing NEXT on the local keyboard of the DVD player. The remote control test is successful if a code was received before the user pressed the NEXT key; pressing the NEXT key before pressing a key on the remote control gives an error in the remote control test (note that the remote control test will also fail if a key on the remote control was pressed but no code was received). The remote control test does not check upon the contents of the received code, that is it will not be checked if the received code matches the key pressed. If desired, the user can manually check this code by using a code-table for the remote control key-codes.

RC Key id	Hexadecimal code
STANDBY	C
STOP	31
PLAY	2C
PAUSE	30
NEXT	20
PREVIOUS	21
CURSOR UP	58
CURSOR DOWN	59
CURSOR LEFT	5A
CURSOR RIGHT	5B
OK	5C
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
ANGLE	85
AUDIO	4E
SUBTITLES	4B
ROOT MENU	54
OSD ON/OFF	F
RETURN	83
SHUFFLE	1C
REPEAT	1D
A/B REPEAT	3D

Figure 14-7

After pressing NEXT, the result of the remote control test is displayed on the local display of the DVD player as follows:

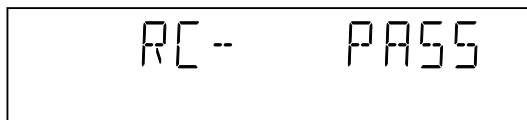


Figure 14-8

Or

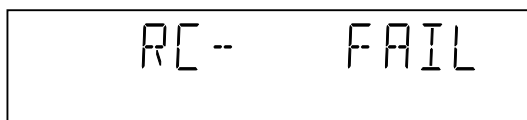


Figure 14-9

Pressing NEXT on the local keyboard again will proceed to the next test.

## 14.2 MONO PCB DIGITAL PART

### 14.2.1 PICTURE TEST

The picture test is performed by putting a predefined picture (colour bar) on the display (nucleus VideoColDencOn) and asking the user for confirmation. The display will show the following message:

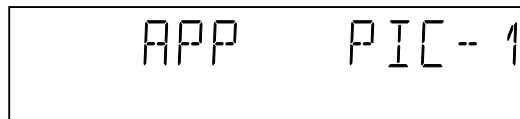


Figure 14-10

By pressing PLAY the user confirms the test, pressing PAUSE will indicate the picture was invisible or incorrect. Pressing NEXT will proceed to the next test

### 14.2.2 SOUND 1 & SCART DVD TEST

The first soundtest is performed by starting a pink noise sound that needs confirmation from the user (nucleus AudioPinkNoiseOn); the display will show the following message very shortly:

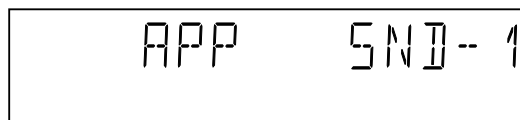


Figure 14-11

This sound will only be audible from version cut3.1 of Sti5505(item7503 on mono board) onwards. After starting up sound 1, SCART loop-trough will be simultaneously active during this test. SCART loop-trough will be measured with the aid of an external video source. When entering the SCART loop-trough, the local display indicates:



Figure 14-12

On the TV screen a colour bar (generated by nucleus VideoColDencOn) is visual and the internally generated pinknoise is audible. By pressing PLAY the user confirms the test, pressing PAUSE will indicate the sound was inaudible or incorrect. Pressing NEXT will proceed to the next test; if the user presses NEXT without pressing PLAY or PAUSE first, the result of this test will be TRUE (sound ok). By pressing the NEXT button there will be switched over to the external source, this must become now visible on the TV screen (using the SCART). The local display indicates:



Figure 14-13

The internally generated colour bar is still available on the CVBS and Y/C outputs. And the pinknoise-signal is still available on the cinch audio outputs. By pressing the PREV button, the internal generated colour bar becomes visual again. The test can be left by pressing the NEXT key for more than one second.

#### 14.2.3 SOUND 2 TEST

The second soundtest is performed by producing a sine sound (nucleus AudioSineOn). The signal can be stopped by pressing the STOP-key. The display will show the following message:

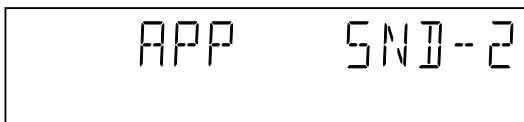


Figure 14-14

By pressing PLAY the user confirms the test, pressing PAUSE will indicate that something went wrong. Pressing NEXT will proceed to the next; if the user presses NEXT without pressing PLAY or PAUSE first, the result of this test will be TRUE (sound ok).

### 14.3 BASIC ENGINE

#### 14.3.1 VERSION NUMBER

In the basic engine tests, the version number of the Basic Engine will be shown first, as the following example:

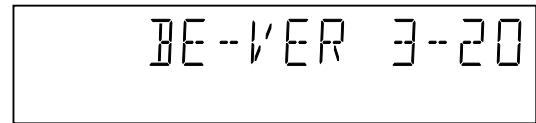


Figure 14-15

By pressing the NEXT key, the Basic Engine tests are started.

#### 14.3.2 TRAY TEST

First, the tray is tested. The purpose of this test is also to give the user the opportunity to put a disc in the tray of the DVD player. Some tests on the Basic Engine require that a disc (e.g. DVD MPTD test disc) is present in the player. At the end of the Basic Engine tests this tray test will be repeated solely to enable the user to remove the disc in the tray. The local display will look as follows:

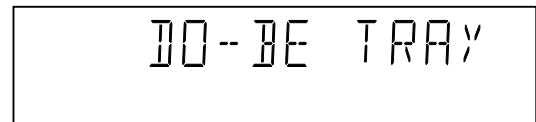


Figure 14-16

By pressing PLAY or PAUSE the user can toggle the position of the tray. Note that this test will not contribute to the test result of the Basic Engine. Pressing NEXT will proceed to the next test, after the tray has been closed (by the software) if it was open.

#### 14.3.3 SLEDGE TEST(visual test)

The second Basic Engine test tests the sledge; the user can move the sledge as many times as desired by using PLAY (nucleus BeSledgeOut) and PAUSE (nucleus BeSledgeIn). Pressing NEXT on the local keyboard proceeds to the next test. Note that this test will not contribute to the test result of the Basic Engine. The local display will look as follows during the sledge test:

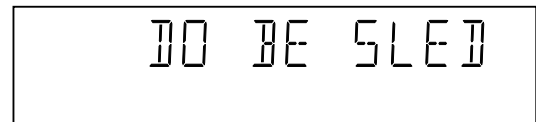
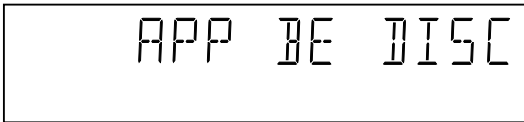


Figure 14-17

#### 14.3.4 DISC MOTOR TEST(visual test)

The third Basic Engine test tests the disc motor (nucleus BeDiscMotorOn); the local display looks as follows:

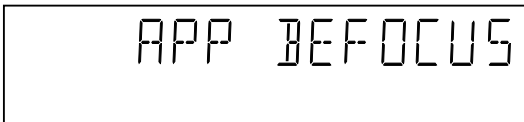


**Figure 14-18**

By pressing PLAY the user confirms that the disc motor is running; pressing PAUSE indicates the disc motor does not work. Pressing NEXT proceeds to the next test, after a reset of the disc motor (nucleus BeDiscMotorOff). If the user presses NEXT before pressing PLAY or PAUSE, the result of this test will be TRUE (disc motor is running).

#### 14.3.5 FOCUS TEST(visual test)

The fourth Basic Engine test tests the focussing; first focussing is turned on by calling nucleus BeFocusOn. The display will look as follows:

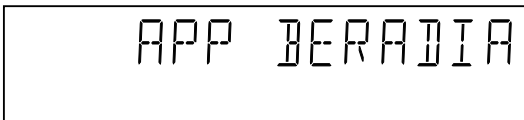


**Figure 14-19**

By pressing PLAY the user confirms that the focussing was successful; pressing PAUSE indicates a focussing failure. Pressing NEXT proceeds to the next test after a reset of the focussing (nucleus BeFocusOff); if NEXT is pressed before PLAY or PAUSE, the result of this test will be TRUE (focus successful).

#### 14.3.6 RADIAL TEST(visual & listening test)

The fifth Basic Engine test tests the radial functionality (nucleus BeRadialOn); the local display looks as follows:

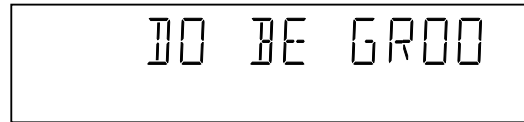


**Figure 14-20**

By pressing PLAY the user confirms that the radial function worked; pressing PAUSE indicates the function does not work. Pressing NEXT proceeds to the next test, after a reset of the radial (nucleus BeRadialOff). If the user presses NEXT before pressing PLAY or PAUSE, the result of this test will be TRUE (radial successful).

#### 14.3.7 JUMP TEST(listening test)

The sixth and last Basic Engine test tests the jumping by calling nuclei BeGroovesIn, BeGroovesMid and BeGroovesOut. During this test, the local display looks as follows:

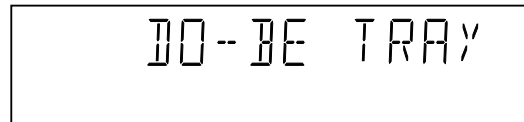


**Figure 14-21**

The user can switch between the three different types of groove settings by pressing PLAY (forward to next nucleus in the list In-Mid-Out) or PAUSE (backward in the list In-Mid-Out). This is done in a cyclic manner; note that this test will not contribute to the test result of the Basic Engine. Pressing NEXT proceeds to the next test, after the disc motor has been shut off with a call to nucleus BeDiscMotorOff.

#### 14.3.8 TRAY TEST

As a last action for the Basic Engine tests, the tray test is repeated. The local display will look as follows:



**Figure 14-22**

This test is meant to give the user the opportunity to remove the disc in the tray. The tray position can be toggled using the PLAY and PAUSE key. The tray will be closed (by the software, if it is open) before proceeding to the next test when the user presses the NEXT key.

### 14.3.9 ERROR LOG

Reading the error log and error bits information can be useful to determine any errors that occurred recently during normal operation of the DVD player. Reading the error log is done by nucleus LogReadErr. The display during the errorlog readout looks as follows :

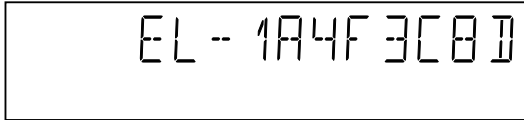


Figure 14-23

By pressing PLAY or PAUSE the user can move forward or backward (respectively) through the logged error codes. The highlighted number indicates which errorcode is currently on display (in the example above, errorcode number 4 is displayed). If "0000" is displayed at all positions, the error log is empty. Display of the logged errors is done in a cyclic manner. The errorcode with the lowest highlighted number is the most

recent. By pressing NEXT on the local keyboard, the user can proceed to the next test.

### 14.3.10 ERROR BITS

Reading the error bits is done by nucleus LogReadBits. The display during the errorbits readout looks as follows:



Figure 14-24

Only the set errorbits will be shown by their (decimal) number. Refer to the appropriate documentation for the explanation of each bit number. If the display only shows "EB-0", no error bits were set. By pressing NEXT the user can continue to the next test.

See table below:

Error log / bits table	Read ERROR LOG in player script	Read ERROR BITS in player script
Basic engine errors	Value:	Value:
Command to the Basic Engine not allowed in this state or unknown command	150101	8
Parameter(s) from the command to the Basic Engine is not valid	150102	7
Sledge could not be moved to the inner home position	150103	6
Focus failure	150104	5
Turntable motor speed could not be reached within timeout	150105	4
Radial servo could not get on track on the disc	150106	3
PLL could not lock in the accessing or tracking state	150107	2
Subcode or sector information could not be read	150108	1
requested subcode could not be found	150109	16
Tray could not be closed or opened completely	15010A	15
TOC could not be read within timeout	15010B	14
The requested seek on the disc could not be executed	15010C	13
A requested lead-in is not on the disc	15010D	12
A non existing burst cutting area is requested	15010E	11
S2b communication error	1501F0	10
S2b communication error	1501F1	9
S2b communication error	1501F3	24
S2b communication error	1501F4	23
S2b communication error	1501F5	22
Digital PWB errors		
Communication error with the Sti 5505	90000	32
Communication error with the Sti 5505	90001	31
Disply processor errors		
Communication error with the display processor	190000	40

## 14.4 LOOP TEST

At the start of the loop test, the display will show the result of the interactive player test:

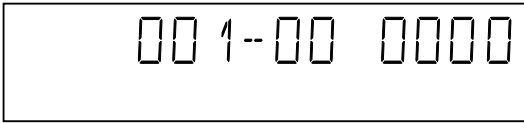


Figure 14-25

The left side of the display contains a 3-digit code, which can have a value between 000 and 111. These values are to be interpreted as follows:

Displayed Value	Indication for each module		
	Basic Engine	Mono PCB	Display PCB
000	ok	ok	ok
001	ok	ok	faulty
010	ok	faulty	ok
011	ok	faulty	faulty
100	faulty	ok	ok
101	faulty	ok	faulty
110	faulty	faulty	ok
111	faulty	faulty	faulty

Figure 14-26

The loop test will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely. The display of the DVD player will display not only the three digits indicating correct/faulty modules and the last found error code (as mentioned, faults are detected as far as they can be within the scope of the diagnostic software), but also a loop counter indicating how many times the loop has been gone through. Example:

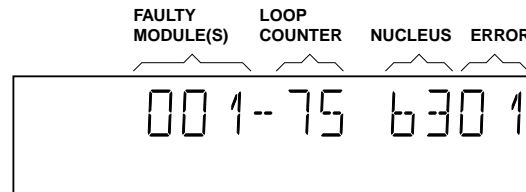


Figure 14-27

The number after the hyphen indicates the number of times the loop test has been performed; the 4 digits at the right side of the display show the last error that was found when running the loop test: the leftmost two digits of this code indicate which nucleus resulted in a fault; the rightmost two digits refer to the faultcode within that nucleus. For further explanation of this error code, see list of error codes below.

### ERROR CODES LOOP TEST

ERROR CODE	NUCLEUS NUMBER	ERROR DESCRIPTION
<b>0601</b>	6	Calculated checksum of FLASH is not correct
<b>0901</b>	9	The DVD DRAM is faulty
<b>1104</b>	11	I2C bus busy before start
<b>1102</b>		NVRAM access time-out
<b>1103</b>		No NVRAM Acknowledge
<b>1104</b>		NVRAM reply time-out
<b>1201</b>	12	I2C bus busy
<b>1202</b>		I2C bus not working
<b>1203</b>		Slave controller not responding
<b>1204</b>		Slave response is not correct
<b>1301</b>	13	Parity error from basic engine to serial
<b>1302</b>		Parity error from serial to basic engine
<b>1303</b>		No communication between serial and basic engine
<b>1304</b>		Communication time-out error
<b>1601</b>	16	The SDRAM is faulty

Figure 14-28



## 14.5 Servicing DVD module and MONO board

For /U1B with old DVD module "VAE3000". (Production WEEK36 or earlier)

The DVD module(Basic Engine and the mono board) has to be exchanged completely in case of failure. A new module for DV4100 can be ordered with codenumber 3104 129 51980.

For other DV4100

Please refer the DVD Module ADS-1 Service Manual (3122 785 10840) attached with this Service Manual.

For servicing DVD Module ADS-1, the service application software "ComPair" is necessary.

### 14.5.1 Reprogramming of new mono boards.

#### Caution

**This information is confidential and may not be distributed. Only a qualified service person should reprogram the mono board.**

After replacement of the mono board, all the customer settings and also the region code will be lost. Reprogramming of the mono board will put the player back in the state in which it has left the factory, i.e. with the default settings and the allowed region code.

Reprogramming is limited to 25 times

When the counter reaches 25, reprogramming is not possible anymore

Reprogramming will be done by way of the remote control.

Put the player in stop mode, no disc loaded.

Press the following keys on the remote control:

<PLAY> followed by numerical keys <2> <7> <4>

The display shows: "-----"

Press now successively the following keys :

for DV4100/A1B : <0><1><5> <0><0><0><0><0><0><0><0><0><0> PAL / NTSC

for DV4100/N1B : <0><1><2> <0><0><0><0><0><0><0><0><0><0> PAL / NTSC

for DV4100/S1G : <0><1><3> <0><0><0><0><0><0><0><0><0><0> PAL / NTSC

for DV4100/U1B : <0><1><0> <0><0><0><0><0><0><0><0><0><0> PAL / NTSC

Press <PLAY> again.

The TV screen will become BLUE during a short time to confirm that the mono board has been reprogrammed, then the set goes to standby mode.

Figure 14-29

### 14.5.2 Reset of Virgin Mode

After the player has been powered up for test by the dealer, it would have gone through the Virgin Mode. It is possible to reset the settings made during that mode before the delivery of player to the customer. This can be done as shown in the following diagram:

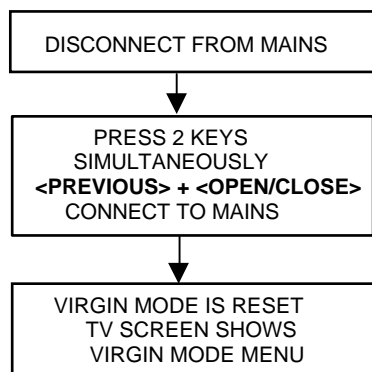


Figure 14-30

### TRADE MODE

**When the player is in Trade Mode, the player cannot be controlled by means of the front key buttons, but only by means of the remote control.**

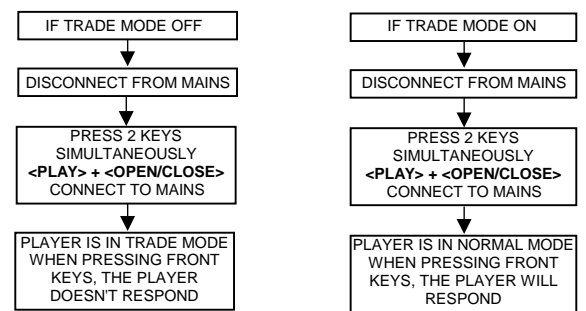


Figure 14-31

# 15. TEST INSTRUCTIONS DISPLAY BOARD

## 15.1 Display board

### 15.1.1 Introduction

These test instructions are written for all versions of the display PCB 3104 123 42230.

The contents of the PCB can be split up into next blocks:

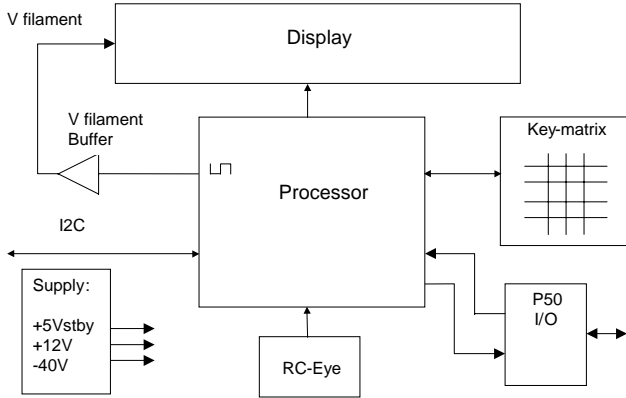


Figure 15-1

### 15.1.2 Functionality description:

The essential component of the display PCB is the  $\mu P$  (slave). This slave works on an 8MHz resonator and has a reset circuit that is triggered by the +5Vstby. After the reset pulse, the standby control line will release the reset of the host  $\mu P$ . This host  $\mu P$  will then initialise the slave. In addition, when going to stand-by, the slave will put the host  $\mu P$  in reset. When the slave receives the right IR or key code to leave the standby mode, the reset of the host  $\mu P$  will be released.

Other slave functions are:

- Square signal generator to generate the filament voltage, which is required for an AC FTD.
- Generates the grid and segment scanning for the FTD.
- Generates a scanning grid for the keys (separated from display scanning).
- Has inputs for RC (RC5 and RC6) and P50 (P50 controller is built in).

### 15.1.3 General

- Oscilloscope measurements have been carried out using a Philips PM3392A.
- Impedance of measuring-equipment should be  $> 1M\Omega$ .
- To do correct measurements we recommend to use supply 3122 427 21370, which is used in all "second generation B" DVD-players. Make sure that the main 3.3V has a 0.7A load.

### 15.1.4 Reset

Check next reset timing with an oscilloscope at pin 10 of the microprocessor.

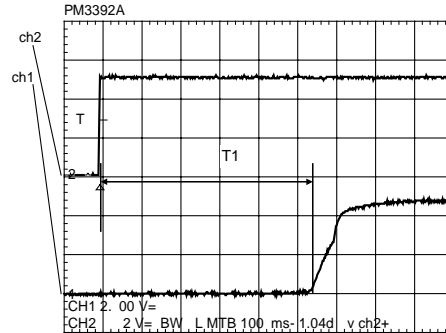


Figure 15-2

Timing:  $400\text{msec} < T1 > 700\text{msec}$ .  
 CH1: +5Vstby voltage at power on.  
 CH2: Voltage at pin 10.

### 15.1.5 Display steernign

Check next timing and level for all grid-lines (G1 r G14).

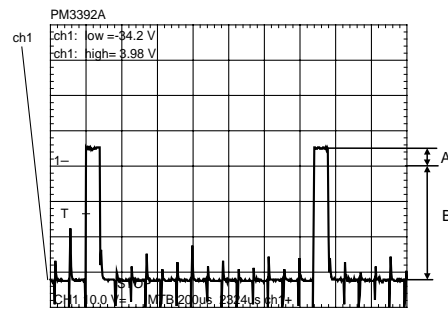


Figure 15-3

1. Check level A: +4V5 +/-10% for grid lines 1 => 11
2. Check level A: +4V0 +/-10% for grid lines 12 => 14
3. Check level B: -33V +/-10%
4. Check timing and levels of segment-lines P1 => P10:

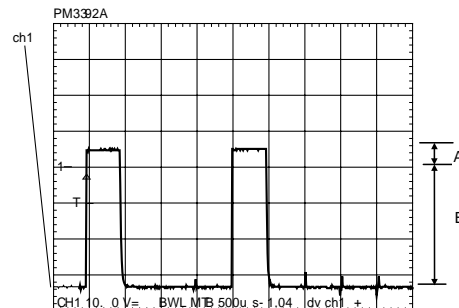


Figure 15-4

Level A: +4V5 +/-10%

Level B: -33V +/-10%

The data on these segment lines depend on the characters that are displayed.

The characters can be set by sending I2C commands to the display.

See the Slave URS how to send a display command.

### 15.1.6 Key-matrix

Connect an extra 10k pull-up to pin 36 and 37 of the P and check next matrix scanning at these pins.

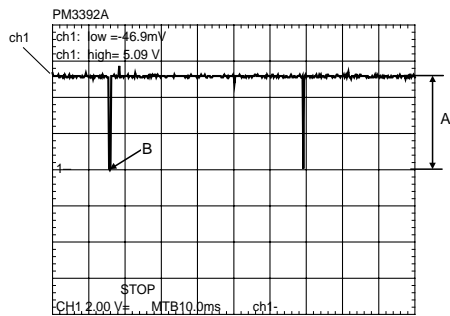


Figure 15-5

Level A: 5.0V +/-7%

Level B: 0V +/-200mV

Check matrix scanning from pin 26 until 33 of the  $\mu$ P. The results should be the same as the diagram above.

### 15.1.7 I.R. receiver

Check at pin 23 of the  $\mu$ P if this line switches from low (< 0.3V) to high (> 4.5V), while pressing a key on a Philips RC5 or RC6 remote control.

### 15.1.8 P50 interface

P50 is a bi-directional serial interface, which is used for communication between video equipment. For European sets, this communication goes via pin 10 of the scart-bus. In other regions, it can be a cinch bus at the back of the set.

1. Keep the P in reset by short-circuiting emitter and collector of transistor 7108, via resistor 3100 and 3104 transistor 7101 is switched on.
2. Check the voltage at the P50 output connector 1118-5: < 200mV.

When the reset is released the P output-pin becomes low and transistor 7101 is switched off.

1. Check the voltage at the P50 output connector 1118-5: 4V9 +/-5%.
2. Check also the  $\mu$ P P50 input ( $\mu$ P pin 20): 5V +/-5%.
3. Connect the P50 line (connector 1118-5) to ground.
4. Check again the  $\mu$ P P50 input ( $\mu$ P pin 20): <0V3.

## 16. CURRENT MODE POWER SUPPLY 20PS203

### 16.1 Blockdiagram

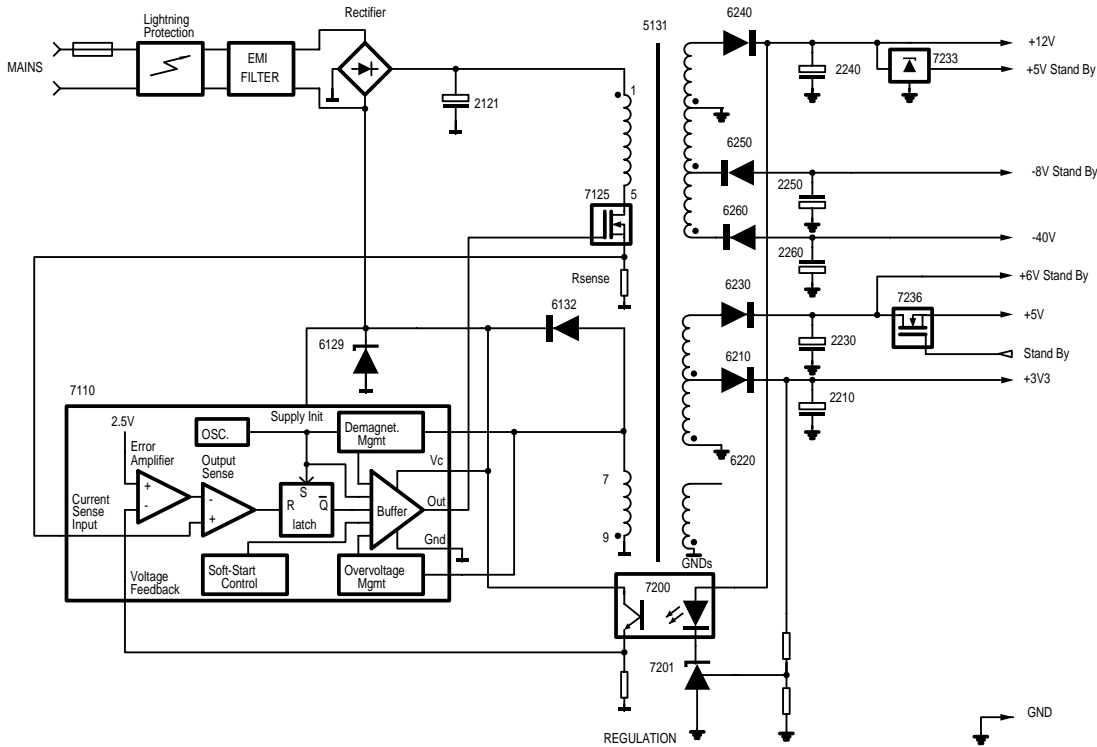


Figure 16-1

#### 16.1.1 Function description of the current mode power supply

MOSFET 7125 is used as a power switch controlled by the controller IC 7110. When the switch is closed, energy is transferred from the mains into the transformer. This energy is then supplied to the load when the switch is opened. By control of the switched-on time, the energy transferred in each cycle is regulated so that the output voltages are independent of load or input voltage variations. The controlling device MC44603P is an integrated pulse width modulator. A clock signal initiates power pulses at a fixed frequency. The termination of each output pulse occurs when an analogue of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls the peak inductor current on cycle-by-cycle basis.

#### 16.2 General description of MC44603

The MC44603 is an enhanced high performance controller that is specifically designed for Off-line and dc-to dc converter applications. This device has the unique ability of automatically changing operating modes if the converter output is overloaded., unloaded, or shorted. The MC44603 has several distinguishing features when compared to conventional SMPS controllers. These features consist of a foldback facility for overload protection, a standby mode when the converter output is slightly loaded, a demagnetisation detection for reduced switching stresses on transistor and diodes, and a high current totem pole output ideally suited for driving a power MOSFET. It

can also be used for driving a bipolar transistor in low power converters. It is optimised to operate in discontinuous mode but can also operate in continuous mode. Its advanced design allows use in current mode or voltage mode control applications.

#### 16.3 Pin connections

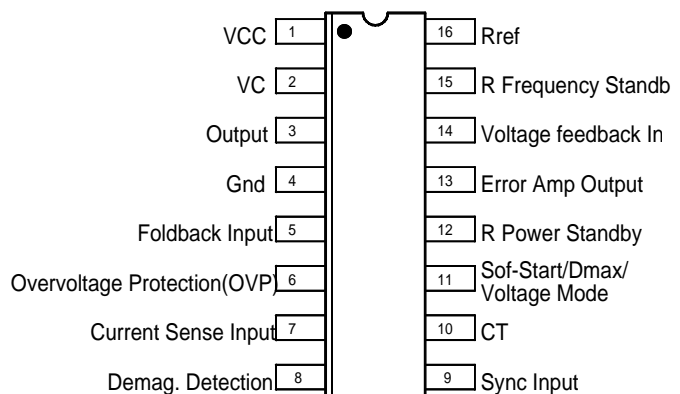


Figure 16-2

## 16.4 Blockdiagram of MC44603

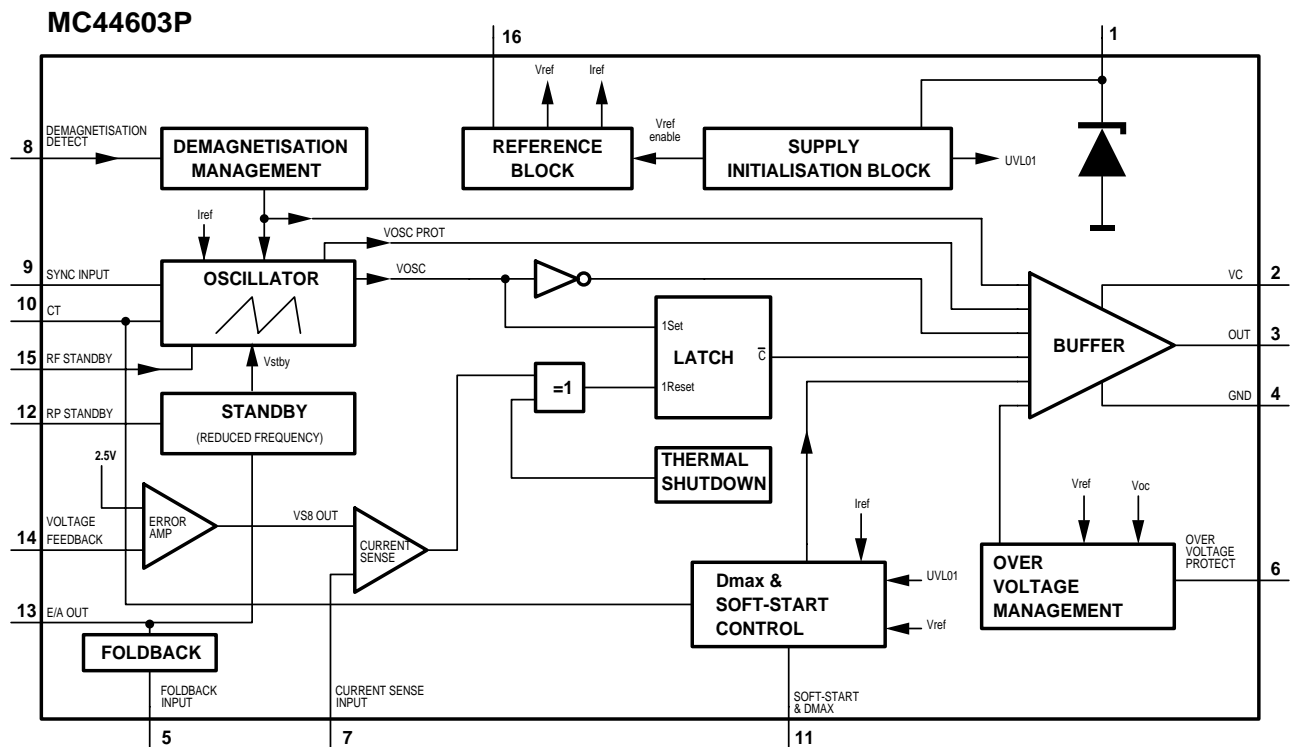


Figure 16-3

## 16.5 Pin function description

### Pin function description

Pin	Name	Description
1	VCC	This pin is the positive supply of the IC. The operating voltage range after start-up is 9.0 to 14.5 V.
2	VC	The output high state (VOH) is set by the voltage applied to this pin.
3	Output	Peak currents up to 750 mA can be sourced or sunk, suitable for driving either MOSFET or Bipolar transistors.
4	Gnd	The groundpin is a single return, typically connected back to the power source.
5	Foldback Input	The foldback function provides overload protection.
6	Overvoltage Protection	When the overvoltage protection pin receives a voltage greater than 2.5V, the device is disabled and requires a complete restart sequence.
7	Current Sense Input	A voltage proportional to the current flowing into the power switch is connected to this input.
8	Demagnetisation Detection	A voltage delivered by an auxiliary transformer winding provides to the demagnetisation pin an indication of the magnetisation state of the flyback transformer. A zero voltage detection corresponds to complete core saturation.
9	Synchronisation Input	The synchronisation input pin can be activated with either a negative pulse going from a level between 0.7V and 3.7V to Gnd or a positive pulse going from a level between 0.7V and 3.7V up to a level higher than 3.7V. The oscillator runs free when Pin 9 is connected to Gnd.
10	C <sub>T</sub>	The normal mode oscillator frequency is programmed by the capacitor C <sub>T</sub> choice together with the R <sub>ref</sub> resistance value. C <sub>T</sub> , connected between Pin 10 and Gnd, generates the oscillator sawtooth.
11	Soft-Start/Dmax/Voltage-Mode	A capacitor, resistor or a voltage source connected to this pin limits the switching duty-cycle. This pin can be used as a voltage mode control input. By connecting Pin 11 to Ground, the MC44603 can be shut down.
12	RP Standby	A voltage level applied to the RP Standby pin determines the output power level at which the oscillator will turn into the reduced frequency mode of operation(i.e. standby mode). An internal hysteresis comparator allows to return in the normal mode at a higher output power level.
13	E/A Out	The error amplifier output is made available for loop compensation.
14	Voltage Feedback	This is the inverting input of the Error Amplifier. It can be connected to the switching power supply output through an optical (or other) feedback loop.
15	RF Standby	The reduced frequency or standby frequency programming is made by the RF Standby resistance choice.
16	R <sub>ref</sub>	R <sub>ref</sub> sets the internal reference current. The internal reference current ranges from 100µA to 500µA. This requires that $5.0k\Omega \leq R_{ref} \leq 25k\Omega$ .

Figure 16-4

## 16.6 Operating description

The input voltage  $V_{cc}$  (pin 1) is monitored by a comparator with hysteresis, enabling the circuit at 14.5V and disabling the circuit below 7.5V. The error amplifier compares a voltage  $V_{fb}$  (pin 14) related to the output voltage of the power supply, with an internal 2.5V reference. The current sense comparator compares the output of the error amplifier with the switch current  $I_{sense}$  (pin 7) of the power supply. The output of the current sense comparator resets a latch, which is set every cycle by the oscillator. The output stage is a totem pole, capable of driving a MOSFET directly.

### 16.6.1 Start-up sequence

#### *t1: Charging the capacitor at $V_{cc}$*

C2129 will be charged via R3123 and R3134, C2133 and C2111 via R3129. The output is switched off during  $t1$ .

#### *t2: Charging of output capacitors*

When the input voltage of the IC exceeds 14.5V, the circuit is enabled and starts to produce output pulses. The current consumption of the circuit increases to about 17mA, depending on the external loads of the IC. At first, the capacitor at the  $V_{cc}$  pin will discharge because the primary auxiliary voltage, coming from winding 7-9 is below the  $V_{cc}$  voltage. At some moment during  $t2$ , the primary auxiliary voltage reaches the same level as  $V_{cc}$ . The  $V_{cc}$  voltage is now determined by this primary auxiliary voltage.

#### *t3: regulation*

The output voltage of the power supply is in regulation

#### *t4: overload*

When the output is shorted, the supply voltage of the circuit will decrease and after some time drop below the lower threshold voltage. At that moment, the output will be disabled and the process of charging the  $V_{cc}$  capacitor starts again. If the output is still shorted at the next  $t2$  phase, the complete start-and stop sequence will repeat. The power supply comes in a hiccup mode

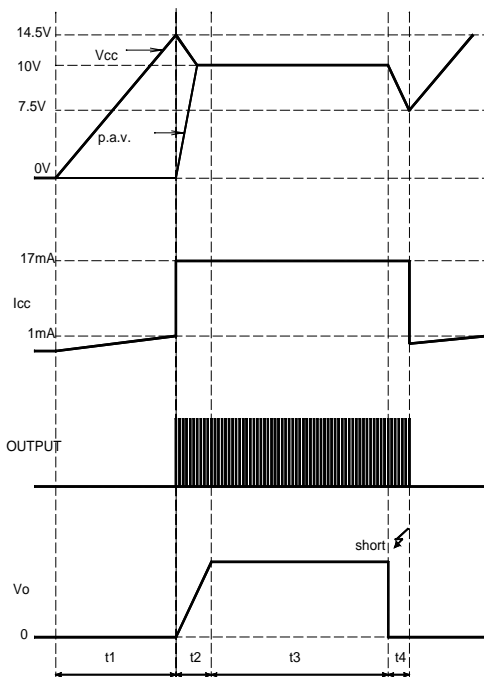


Figure 16-5 Start-up sequence

## 16.7 Regulation

Figure 16-6 shows the most relevant signals during the regulation phase of the power supply.

The oscillator voltage ramps up and down between  $V1$  and  $V2$ . The voltage at the current sense terminal is compared every cycle with the output of the error amplifier  $V_{comp}$ . The output is switched off when the current sense level exceeds the level at the output of the error amplifier.

1. TimeON phase : A drain current will flow from the positive supply at pin 1 of the transformer through the transformer's primary winding, the MOSFET and  $R_{sense}$  to ground. As the positive voltage at pin 1 of the transformer is constant, the current will increase linearly and create a ramp dependent on the mains voltage and the inductance of the primary winding. A certain amount of energy is stored in the transformer in the form of a magnetic field. The polarity of the voltages at the secondary windings is such that the diodes are non-conducting.
2. TimeDIODE phase : When the MOSFET is switched off, energy is no longer supplied to the transformer. The inductance of the transformer now tries to maintain the current which has been flowing through it at a constant level. The polarity of the voltage from the transformer therefore becomes reversed. This results in a current flow through the transformer's secondary winding via the diodes, electrolytic capacitors and the load. This current is also ramp shaped but decreasing.
3. TimeDEAD phase : when the stored energy has been supplied to the load, the current in the secondary windings stops flowing. At this point the drain voltage of the MOSFET will drop to the voltage of C2121 with a ringing caused by the Drain-Source capacitance with the primary inductance.

The oscillator will start a next cyclus which consists of the described three phases. The time of the different phases depends on the mains voltage and the load. TimeDEAD is maximum at an input of 400VDC and minimum load, it will be zero at an input of 100VDC and overload.

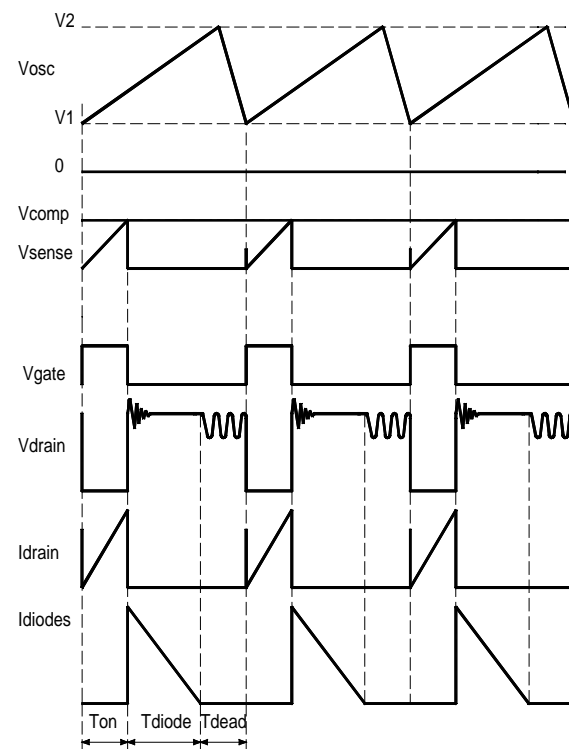
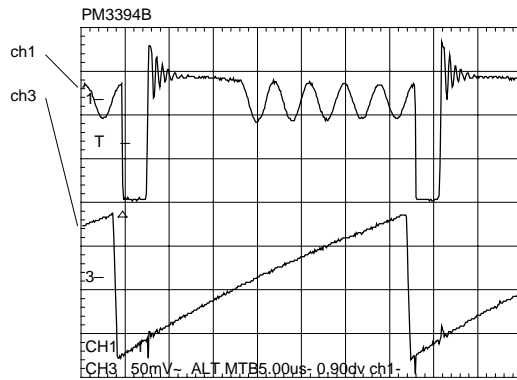


Figure 16-6 Regulation

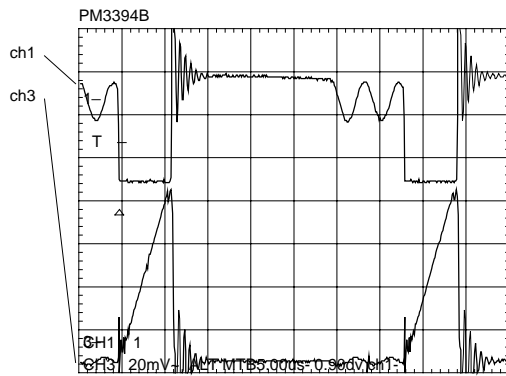
## 16.8 Oscillograms



ch1 : Drain voltage  
ch2 : Drain current  
ch3 : Gate voltage



ch1 : Drain voltage  
ch2 : Oscillator voltage



ch1 : Drain voltage  
ch3 : Sense voltage

Figure 16-7

## 17. CIRCUIT DESCRIPTIONS AND ABBREVIATIONS

### 17.1 Input circuit

The input circuit consists of a lightning protection circuit and an EMI filter.

The lightning protection comprises R3120, gasarrestor 1125 and R3124. The EMI filter is formed by C2120, L5120, C2125 and C2126. It prevents inflow of noises into the mains.

### 17.2 Primary rectifier/smoothing circuit

The AC input is rectified by rectifier bridge 6120 and smoothed into C2121. The voltage over C2121 is approximately 300V. It can vary from 100V to 390V.

### 17.3 Start circuit and Vcc supply

This circuit is formed by R3123, R3134, C2129, D6129, R3129, R3111, C2133 and C2111.

When the power plug is connected to the mains voltage, the stabilised voltage over D6129(24V) will charge C2133 via R3129. When the voltage reaches 14.5V across C2111, the control circuit of IC7110 is turned on and the regulation starts. During regulation, Vcc of IC7110 will be supplied by the rectified voltage from winding 7-9 via R3135, D6132 and C2133.

### 17.4 Control circuit

The control circuit exists of IC7110, C2102, 2104, 2107, 2109, 2110, R3102, 3103, 3104, 3107, 3108, 3109 and 3110. The frequency of the oscillator is defined by C2102 and R3110.

Power switch circuit

This circuit comprises MOSFET 7125, Rsense 3126, 3127 and 3128, R3125, C2127, L5125, R3112 and R3113. R3125 is a pull-down resistor to remove static charges from the gate of the MOSFET.

### 17.5 Regulation circuit

The regulation circuit comprises opto-coupler 7200 which isolates the error signal from the control IC on the primary side and a reference component 7201. The TL431(7201) can be represented by two components:

- a very stable and accurate reference diode
- a high gain amplifier

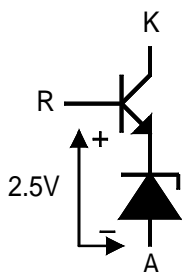


Figure 17-1

TL431 will conduct from cathode to anode when the reference is higher than the internal reference voltage of about 2.5V. If the reference voltage is lower, the cathode current is almost zero.

The cathode current flows through the LED of the opto-coupler. The collector current of the opto-coupler flows through R3106, producing an error voltage, connected to voltage feedback pin 14 of IC7110.

### 17.6 Demagnetisation

The auxiliary winding (7-9) voltage is used to detect magnetic saturation of the transformer core and connected via R3101 to pin 8 of IC7110. During the demagnetisation phase, the output will be disabled.

### 17.7 Overvoltage protection circuit

This circuit consist of D6114, C2114, R3115 and R3116.

When the regulation circuit is interrupted due to an error in the control loop, the regulated output voltage will increase (overvoltage). This overvoltage is sensed on the primary winding 7-9.

When an overvoltage longer than 2.0 (s is detected, the output is disabled until VCC is removed and then re-applied. The power supply will come in a hiccup mode as long as the error in the control loop is present.

### 17.8 Secondary rectifier/smoothing circuit

There are 5 rectifier/smoothing circuits on the secondary side. Each voltage depends on the number of windings of the transformer.

The +5Vstby power supply is derived from the +12Vstby by voltage regulator 7233, C2233 and L5233.

The -5V voltage is regulated by voltage regulator 7259 and will be switched off via D6256, T7256 and T7255 during standby (control signal STAND BY is high). When jumper 4250 is mounted instead of this circuit, a supply voltage -8Vstby will be present at pin 9 of connector 0205. -5V is used in DVD730 MK II, DVD 930 MK II and DVD710. -8Vstby is used in DVD750 and DVD950.

The +5V power supply is derived from +6Vstby by the loader-up circuit formed by MOSFET 7236, reference component 7237, R3236, R3237 and C2239. This voltage will be switched off during STAND BY via T7235.

The 3V3 power supply is regulated by the control loop (7201, 7200, 7110) of the switched mode PSU.



## 17.9 List of abbreviations

B	Buffered Video input Blue from DVD monoboard
BC_AUX	Blue or Chroma input from AUX-scart
BC_TV	Blue or Chroma output to TV-scart
C_ENC	Buffered Chroma input from DVD monoboard
CVBS	Buffered Composite video input from DVD monoboard
DC_OFF	Control signal to switch off -8Vstby and +12Vstby during standby
DIG_OUT	Digital out
FBIN_AUX	Fast blanking input from AUX-scart
FBOUT_TV	Fast blanking output to TV-scart
G	Buffered Video input Green from DVD monoboard
GIN_AUX	Video input Green from AUX-scart
GOUT_TV	Video output Green to TV-scart
HP_L	Audio output left to headphone and audio scart switch TEA6420
HP_R	Audio output right to headphone and audio scart switch TEA6420
KILL	Kill control signal for audio outputs and for soft mute of DAC
LIN_AUX	Audio input left from AUX-scart
LIN_TV	Audio input left from TV-scart
LOUT_AUX	Audio output left to AUX-scart
LOUT_TV	Audio output left to TV-scart
LRCLK	Left/Right clock
PCM_CLK	Audio system clock for DAC
PCM_OUT0	Audio serial output data
R	Buffered Video input Red from DVD monoboard
RCIN_TV	Red or Chroma input from TV-scart
RCOUT_TV	Red or Chroma output to TV-scart
RIN_AUX	Audio input right from AUX-scart
RIN_TV	Audio input right from TV-scart
ROUT_AUX	Audio output right to AUX-scart
ROUT_TV	Audio output right to TV-scart
SCL	I2C bus clock
SCLK	Audio serial bit clock
SDA	I2C bus data
SELECT	Control signal for video scart switches; high = TV ,low = AUX
SELECT_HIGH	Control signal for switching fast blanking and slow blanking signals; high = TV ,low = AUX
SLB_AUX	Slow blanking control signal from AUX-scart
SLB_TV	Slow blanking control signal to TV-scart
STANDBY	Control signal from ST15505 used to swith off -8Vstby and +12Vstby during standby.
STEREO_L	Audio cinch output left
STEREO_R	Audio cinch output right
Y_ENC	Buffered Luma input from DVD monoboard
YCVBSIN_AUX	Luma or CVBS input from AUX-scart
YCVBSIN_TV	Luma or CVBS input from TV-scart
YCVBSOUT_AUX	Luma or CVBS output to AUX-scart
YCVBSOUT_TV	Luma or CVBS output to TV-scart
0/6/12	Scart switch control signal A/V board. 0V : loop through (AUX to TV), 6V : play 16:9 format, 12V : play 4:3 format

## 18. ELECTRICAL PARTS LIST

### ASSIGNMENT OF COMMON PARTS CODES.

#### RESISTORS

R\*\*\* : 1) GD05 x x x 140, Carbon film fixed resistor, ±5% 1/4W  
 R\*\*\* : 2) GD05 x x x 160, Carbon film fixed resistor, ±5% 1/6W  
 ① Resistance value

Examples

① Resistance value

0.1Ω ..... 001    10Ω ..... 100    1kΩ ..... 102    100kΩ ..... 104  
 0.5Ω ..... 005    18Ω ..... 180    2.7kΩ ..... 272    680kΩ ..... 684  
 1Ω ..... 010    100Ω ..... 101    10kΩ ..... 103    1MΩ ..... 105  
 6.8Ω ..... 068    390Ω ..... 391    22kΩ ..... 223    4.7MΩ ..... 475

**Note** : Please distinguish 1/4W from 1/6W by the shape of parts used actually.

#### CAPACITORS

C\*\*\* : CERAMIC CAP.

3) DD1 x x x x 370, Ceramic capacitor  
 Disc type  
 Temp. coeff. P350~N1000, 50V  
 ③ Capacity value  
 ② Tolerance

Examples

② Tolerance (Capacity deviation)

±0.25 pF ..... 0  
 ±0.5 pF ..... 1  
 ±5 % ..... 5

Tolerance of COMMON PARTS handled here are as follows :

0.5 pF - 5 pF ..... ± 0.25 pF  
 6 pF - 10 pF ..... ± 0.5 pF  
 12 pF - 560 pF ... ± 5 %

③ Capacity value

0.5 pF .... 005    3 pF .... 030    100 pF ..... 101  
 1 pF .... 010    10 pF ..... 100    220 pF ..... 221  
 1.5 pF .... 015    47 pF ..... 470    560 pF ..... 561

C\*\*\* : CERAMIC CAP.

4) DK16 x x x 300, High dielectric constant ceramic capacitor  
 Disc type  
 Temp. chara. 2B4, 50V  
 ④ Capacity value

Examples

④ Capacity value

100 pF ..... 101    1000 pF .... 102    10000 pF .... 103  
 470 pF ..... 471    2200 pF .... 222

C\*\*\* : 5) ELECTROLY CAP. (  ), 6) FILM CAP (  )

5) EA x x x x x 10, Electrolytic capacitor  
 One-way lead type, Tolerance ±20%  
 ⑥ Working voltage  
 ⑤ Capacity value

Examples

⑤ Capacity value

0.1 μF .... 104    4.7 μF .... 475    100 μF ..... 107  
 0.33 μF .... 334    10 μF .... 106    330 μF ..... 337  
 1 μF .... 105    22 μF .... 226    1100 μF ..... 118  
 2200 μF .... 228

⑥ Working voltage

6.3 V ..... 006    25 V ..... 025  
 10 V ..... 010    35 V ..... 035  
 16 V ..... 016    50 V ..... 050

6) DF15 x x x 350 → Plastic film capacitor  
 DF15 x x x 310 → One-way type, Mylar ±5% 50V  
 DF16 x x x 310 → Plastic film capacitor  
 One-way type, Mylar ±10% 50V  
 ⑦ Capacity value

Examples

⑦ Capacity value

0.001 μF (1000 pF) ..... 102    0.1 μF ..... 104  
 0.0018 μF ..... 182    0.56 μF ..... 564  
 0.01 μF ..... 103    1 μF ..... 105  
 0.015 μF ..... 153

**NOTE** 1) The above CODES(R\*\*\*, R\*\*\*, C\*\*\*, C\*\*\* and C\*\*\*) are omitted on the schematic diagram in some case.  
 2) On the occasion, be confirmed the common parts on the parts list.  
 3) Refer to "Common Parts List" for the other common parts(R105, DD4, DK4).

### NOTE ON SAFETY FOR FUSIBLE RESISTOR :

The suppliers and their type numbers of fusible resistors are as follows ;

1. KOA Corporation

Part No.(MJI)	Type No.(KOA)	Description
NH05 x x x 140	RF25S x x x x Ω	J ±5% (1/4W)
NH05 x x x 120	RF50S x x x x Ω	J ±5% (1/2W)
NH85 x x x 110	RF73B2A x x x x Ω	J ±5% (1/10W)
NH95 x x x 140	RF73B2E x x x x Ω	J ±5% (1/4W)

\* Resistance value    Resistance value(0.1Ω - 10k Ω)

2. Matsushita Electronic Components Co., Ltd

Part No.(MJI)	Type No.(MEC)	Description
NF05 x x x 140	ERD-2FCJ x x x	(±5% 1/4W)
RF05 x x x 140		
NF02 x x x 140	ERD-2FCG x x x	(±2% 1/4W)
RF02 x x x 140		

\* Resistance value

Examples



\* Resistance value

0.1Ω ..... 001    10Ω ..... 100    1kΩ ..... 102    100kΩ ..... 104  
 0.5Ω ..... 005    18Ω ..... 180    2.7kΩ ..... 272    680kΩ ..... 684  
 1Ω ..... 010    100Ω ..... 101    10kΩ ..... 103    1MΩ ..... 105  
 6.8Ω ..... 068    390Ω ..... 391    22kΩ ..... 223    4.7MΩ ..... 475


### ABBREVIATION AND MARKS

ANT. : ANTENNA	BATT. : BATTERY
CAP. : CAPACITOR	CER. : CERAMIC
CONN. : CONNECTING	DIG. : DIGITAL
HP : HEADPHONE	MIC. : MICROPHONE
μ-PRO : MICROPROCESSOR	REC. : RECORDING
RES. : RESISTOR	SPK : SPEAKER
SW : SWITCH	TRANSF. : TRANSFORMER
TRIM. : TRIMMING	TRS. : TRANSISTOR
VAR. : VARIABLE	X' TAL : CRYSTAL

### NOTE ON SAFETY:

Symbol  Fire or electrical shock hazard. Only original parts should be used to replaced any part marked with symbol  Any other component substitution ( other than original type), may increase risk of fire or electrical shock hazard.

### 安全上の注意 :

 がついている部品は、安全上重要な部品です。必ず指定されている部品番号の部品を使用して下さい。



POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)	POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
3103		4822 117 10833	10k 1% 0.1W	QP11710833				<b>AV CIRCUIT BOARD (N1B)</b>	
3105		4822 117 10833	10k 1% 0.1W	QP11710833				<b>CAPACITORS</b>	
3106		4822 117 10833	10k 1% 0.1W	QP11710833				CER. 470NF +80 -20% 16V	
3107		4822 051 20101	100R00 5% 0.1W	QP05120101				ELECT 4.7µF 20% 100V	
3108		4822 117 11152	4R7 5%	QP11711152				2354 4822 126 14076 CER. 220N 25V	
3109		4822 117 11152	4R7 5%	QP11711152				2355 4822 124 40769 ELECT 4.7µF 20% 100V	
3110		4822 117 10833	10k 1% 0.1W	QP11710833				2357 4822 124 40769 ELECT 4.7µF 20% 100V	
3112		4822 117 12955	2K7 1% 0.1W	QP11712955				2358 4822 122 33575 CER. 220pF 5% 63V	
3113		4822 117 12955	2K7 1% 0.1W	QP11712955				2359 4822 124 40769 ELECT 4.7µF 20% 100V	
3114		4822 117 10833	10k 1% 0.1W	QP11710833				2360 4822 126 13692 CER. 47pF 1% 63V	
{								2361 4822 126 13692 CER. 47pF 1% 63V	
3117		4822 051 20101	100R00 5% 0.1W	QP05120101				2371 4822 122 33575 CER. 220pF 5% 63V	
3118								2372 4822 124 40769 ELECT 4.7µF 20% 100V	
3119								2373 4822 124 40769 ELECT 4.7µF 20% 100V	
3120								2377 4822 122 33575 CER. 220pF 5% 63V	
3121		4822 117 10833	10k 1% 0.1W	QP11710833				2378 4822 124 40769 ELECT 4.7µF 20% 100V	
3122		4822 117 12955	2K7 1% 0.1W	QP11712955				2382 4822 124 40769 ELECT 4.7µF 20% 100V	
3123		4822 117 12955	2K7 1% 0.1W	QP11712955				2383 4822 124 40769 ELECT 4.7µF 20% 100V	
3124		4822 117 10833	10k 1% 0.1W	QP11710833				2385 4822 124 40769 ELECT 4.7µF 20% 100V	
3126		4822 051 20101	100R00 5% 0.1W	QP05120101				2395 4822 122 33575 CER. 220pF 5% 63V	
3127		4822 117 10833	10k 1% 0.1W	QP11710833				2402 4822 122 33575 CER. 220pF 5% 63V	
3129		4822 117 12955	2K7 1% 0.1W	QP11712955				2404 4822 122 33575 CER. 220pF 5% 63V	
3130		4822 051 20101	100R00 5% 0.1W	QP05120101				2408 4822 122 33575 CER. 220pF 5% 63V	
3131		4822 117 10833	10k 1% 0.1W	QP11710833				2409 4822 122 33575 CER. 220pF 5% 63V	
3132		4822 117 12955	2K7 1% 0.1W	QP11712955				2412 4822 124 40433 ELECT 47µF 20% 25V	
3135		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487				2450 5322 122 32654 CER. 22N 63V	
3136		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487					
3137		4822 117 12635	10R 1% 0.125W	QP11712635					
3138		4822 117 11139	1k5 1% 0.1W	QP11711139					
3139		4822 117 11931	750R 1% 0.1W	QP11711931					
3140		2120 108 92619	SM ERJ6EN 2K2PM1						
3141		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487					
3142		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487					
3143		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487					
3144		4822 117 11953	560R 1% 0.1W	QP11711953					
3145		2120 108 92625	SM ERJ6EN 5K6PM1						
3147		2120 108 92616	SM ERJ6EN 1k2 PM1						
3148		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487					
3150		4822 117 11927	75R 1% 0.1W	QP11711927					
3153		4822 051 20101	100R00 5% 0.1W	QP05120101					
3154		4822 117 11927	75R 1% 0.1W	QP11711927					
3157		4822 117 11927	75R 1% 0.1W	QP11711927					
3158		4822 117 11449	2K2 5% 0.1W	QP11711449					
3159		4822 051 20101	100R00 5% 0.1W	QP05120101					
3160		4822 117 10833	10k 1% 0.1W	QP11710833					
<b>MISCELLANEOUS</b>									
1002		2422 026 05047	CONNECTOR CINC H 6P F RDWHYE B	QU02605047	{	4822 122 33575	CER. 220pF 5% 63V	QP12233575	
1003		4822 267 10994	CONNECTOR 4P MDIN	QP26710994	2505				
1004		2422 025 16526	CONNECTOR 22P F 1.00 FFC 0.3 R	QU02516526	2506 {	4822 124 40763	ELECT 2.2µF 100V	QP12440763	
1005		4822 267 31729	CONNECTOR	QP26731729	2509	4822 124 40763	ELECT 2.2µF 100V	QP12440763	
1006		2422 026 05049	CON BM CINC H 3P F	QU02605049	2511				
1007		2422 025 16525	CONNECTOR 16P F 1.00 FFC 0.3 R	QU02516525	2520 {	4822 122 33575	CER. 220pF 5% 63V	QP12233575	
5000		4822 157 70601	COIL 100UH (920927085A)	QP15770601	2523	5322 122 32654	CER. 22N 63V	QQ12232654	
5003		4822 242 10756	FILTER L/C DSS306-92Y5S221M100	QP24210756	{				
{					2537	4822 124 40763	ELECT 2.2µF 100V	QP12440763	
5007					2538	4822 124 40763	ELECT 2.2µF 100V	QP12440763	
7020					2540	4822 124 40763	ELECT 2.2µF 100V	QP12440763	
					2541	4822 126 14585	CER. 100NF 10% 50V	QP12614585	
					2542	4822 126 14491	CER. 2.2µF 10V	QP12614491	
		2543	4822 126 13692	CER. 47pF 1% 63V	QP12613692				
		2544	4822 124 40248	ELECT 10µF 20% 63V	QP12440248				
		2545	4822 124 40433	ELECT 47µF 20% 25V	QP12440433				



POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)	POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
3622		4822 117 10833	10k 1% 0.1W	QP11710833	3999		4822 117 12842		QP11712842
3623		4822 051 20472	4K70 5% 0.1W	QP05120472					
3624		4822 117 10833	10k 1% 0.1W	QP11710833					
3625		4822 051 10102	1K00 2% 0.25W	QP05110102	1300		4822 265 11154	<b>MISCELLANEOUS</b> CONNECTOR	QP26511154
3629		4822 117 11927	75R 1% 0.1W	QP11711927				52030-2210 (22P)	
3632		4822 051 20101	100R00 5% 0.1W	QP05120101	1301		4822 265 11103	CONNECTOR	QP26511103
3634		4822 117 11449	2K2 5% 0.1W	QP11711449				52030-1610 (16P)	
3635		4822 117 11503	220R 1% 0.1W	QP11711503	1303		4822 267 10994	CONNECTOR 4P MDIN	QP26710994
3636					1304		2422 033 00334	CON BM EURO H 42P F	QU03300334
3643		4822 117 10837	100k 1% 0.1W	QP11710837				BK GRND-L	
3646		4822 117 10837	100k 1% 0.1W	QP11710837	1402		4822 265 11566	CONNECTOR 3P YKC21-3930	QP26511566
3647		4822 117 10837	100k 1% 0.1W	QP11710837	1405		4822 267 31729	CONNECTOR	QP26731729
3648					1410		4822 265 41392	CONNECTOR B7B-EH-A	QP26541392
3651		4822 117 13577	330R 1% 1.25W	QP11713577	5400		4822 157 70601	COIL 100µH (920927085A)	QP15770601
3653		4822 117 13577	330R 1% 1.25W	QP11713577	6400		4822 130 10845	CONNECTOR GP1F32T	QP13010845
3672								<b>FRONT CIRCUIT BOARD</b>	
3675		4822 117 11927	75R 1% 0.1W	QP11711927				<b>CAPACITORS</b>	
3676		4822 117 10353	150R 1% 0.1W	QP11710353	2100	/N1B	4822 122 33575	CER. 220pF 5% 63V	QP12233575
3677		4822 117 11927	75R 1% 0.1W	QP11711927	2101	/N1B	4822 122 33575	CER. 220pF 5% 63V	QP12233575
3678					2102		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
3685		4822 051 20101	100R00 5% 0.1W	QP05120101	2103		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
3687		4822 051 20472	4K70 5% 0.1W	QP05120472	2105		4822 126 12105	CER. 33NF 50V	QP12612105
3688		4822 051 20101	100R00 5% 0.1W	QP05120101	2106		4822 124 40248	ELECT 10µF 20% 63V	QP12440248
3689		4822 051 20101	100R00 5% 0.1W	QP05120101	2107				
3690							4822 126 12105	CER. 33NF 50V	QP12612105
3694		4822 051 10102	1K00 2% 0.25W	QP05110102	2111				
3695		4822 117 10833	10k 1% 0.1W	QP11710833	2114		5322 122 32658	CER. 22pF 5% 50V	QQ12232658
3696		4822 117 10833	10k 1% 0.1W	QP11710833	2115		5322 122 32658	CER. 22pF 5% 50V	QQ12232658
3697					2116		4822 126 12105	CER. 33NF 50V	QP12612105
3700		4822 051 10102	1K00 2% 0.25W	QP05110102	2117		4822 124 40248	ELECT 10µF 20% 63V	QP12440248
3701		4822 051 20471	470R00 5% 0.1W	QP05120471	2122		4822 126 12105	CER. 33NF 50V	QP12612105
3702		4822 051 10102	1K00 2% 0.25W	QP05110102	2123		4822 124 11947	ELECT 10µF 20% 16V	QP12411947
3703					2124		3198 028 42290	ELECT 22µF 35V	
3707		4822 117 11148	56K 1% 0.1W	QP11711148	2125		5322 122 32658	CER. 22pF 5% 50V	QQ12232658
3720		4822 117 11148	56K 1% 0.1W	QP11711148	2126		4822 124 40248	ELECT 10µF 20% 63V	QP12440248
3721		4822 117 10353	150R 1% 0.1W	QP11710353	2128		5322 122 31647	CER. 1NF 10% 63V	QQ12231647
3722		4822 117 11148	56K 1% 0.1W	QP11711148	2129		3198 028 42290	ELECT 22µF 35V	
3723		4822 117 11148	56K 1% 0.1W	QP11711148	2130		3198 028 42290	ELECT 22µF 35V	
3724					2201		4822 126 12105	CER. 33NF 50V	QP12612105
3731		4822 051 20229	22R00 5% 0.1W	QP05120229	2211		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
3732								<b>DIODES</b>	
3747		4822 117 13577	330R 1% 1.25W	QP11713577	6100	/N1B	4822 130 83757	DIODE BAS216	QP13083757
3748					6101		4822 130 11666	DIODE BZX284-C8V2	QP13011666
3761		4822 117 10837	100k 1% 0.1W	QP11710837	6102		4822 130 10794	DIODE BZX284-C10	QP13010794
3762		4822 117 11504	270R 1% 0.1W	QP11711504	6104		4822 130 83757	DIODE BAS216	QP13083757
3763		4822 051 20101	100R00 5% 0.1W	QP05120101	6200		4822 130 82978	LED LTL-16KPE-P	QP13082978
3764		4822 117 10833	10k 1% 0.1W	QP11710833				<b>SEMICONDUCTORS</b>	
3765		4822 117 10833	10k 1% 0.1W	QP11710833	7104	/N1B	3104 123 94532	IC DIG TMP87CH74F-1E29-V2.	QW12394532
3768					7104	/A1B, /S1G,U1B	3104 123 94761	18-DVDSLAVE IC DIG ROM TMP87CH74	QW12394761
3772		4822 117 10834	47k 1% 0.1W	QP11710834	7112		4822 209 31257	IC ANA MC79L24ACP	QP20931257
3773		4822 117 10833	10k 1% 0.1W	QP11710833	7100		5322 130 60159	TRS. BC846B	QQ13060159
3774		4822 117 10834	47k 1% 0.1W	QP11710834	7101	/N1B	5322 130 60159	TRS. BC846B	QQ13060159
3800		4822 051 20472	4K70 5% 0.1W	QP05120472	7102		5322 130 60159	TRS. BC846B	QQ13060159
3801		4822 051 20472	4K70 5% 0.1W	QP05120472	7103		5322 130 60159	TRS. BC846B	QQ13060159
!3802		4822 117 11152	4R7 5%	QP11711152	7105		4822 130 40855	TRS. BC337	QP13040855
!3803		4822 117 11152	4R7 5%	QP11711152	7106		4822 130 40854	TRS. BC327	QP13040854
3804		4822 117 10834	47k 1% 0.1W	QP11710834	7107		5322 130 60159	TRS. BC846B	QQ13060159
3805		4822 117 10833	10k 1% 0.1W	QP11710833	7108		5322 130 60159	TRS. BC846B	QQ13060159
					7109		4822 130 60373	TRS. BC856B	QP13060373
					7110		4822 212 30842	REMOTE RECEIVER TSOP1736SB1	QP21230842

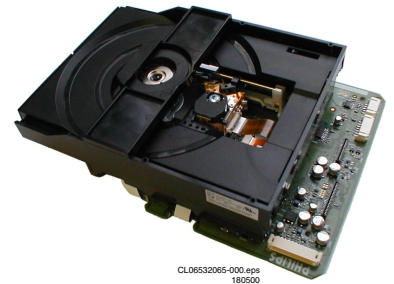
POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)	POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
<b>RESISTORS</b>									
3100	/N1B	4822 051 20223	22K00 5% 0.1W	QP05120223					
3101	/N1B	4822 051 20273	27K00 5% 0.1W	QP05120273					
3102	/N1B	4822 117 10834	47k 1% 0.1W	QP11710834					
3103		4822 117 11149	82k 1% 0.1W	QP11711149					
3104	/N1B	4822 117 10837	100k 1% 0.1W	QP11710837					
3106	/N1B	4822 117 11503	220R 1% 0.1W	QP11711503					
3108		4822 117 11149	82k 1% 0.1W	QP11711149					
3109									
3113		4822 051 20472	4K70 5% 0.1W	QP05120472					
3114		4822 051 20109	10R00 5% 0.1W	QP05120109					
3115		4822 051 20472	4K70 5% 0.1W	QP05120472					
3116		4822 117 11149	82k 1% 0.1W	QP11711149					
3117		4822 117 11152	4R7 5%	QP11711152					
3118		4822 117 10833	10k 1% 0.1W	QP11710833					
3119		4822 117 10833	10k 1% 0.1W	QP11710833					
3120		4822 051 20471	470R00 5% 0.1W	QP05120471					
3121		4822 051 20472	4K70 5% 0.1W	QP05120472					
3122		4822 051 20109	10R00 5% 0.1W	QP05120109					
3123		4822 117 10833	10k 1% 0.1W	QP11710833					
3125		4822 051 20109	10R00 5% 0.1W	QP05120109					
3130		4822 051 20109	10R00 5% 0.1W	QP05120109					
3131		4822 117 11152	4R7 5%	QP11711152					
3132		4822 117 13577	330R 1% 1.25W	QP11713577					
3133		4822 051 20109	10R00 5% 0.1W	QP05120109					
3134		4822 117 13577	330R 1% 1.25W	QP11713577					
3135		4822 117 11503	220R 1% 0.1W	QP11711503					
3136		4822 051 10102	1K00 2% 0.25W	QP05110102					
3137		4822 117 10833	10k 1% 0.1W	QP11710833					
3138		4822 051 20471	470R00 5% 0.1W	QP05120471					
3139		4822 051 20472	4K70 5% 0.1W	QP05120472					
3140		4822 117 10833	10k 1% 0.1W	QP11710833					
3142		4822 117 13577	330R 1% 1.25W	QP11713577					
3143		4822 117 10833	10k 1% 0.1W	QP11710833					
3144		4822 117 10837	100k 1% 0.1W	QP11710837					
3145		4822 117 10833	10k 1% 0.1W	QP11710833					
3151		4822 051 20101	100R00 5% 0.1W	QP05120101					
<b>MISCELLANEOUS</b>									
0002		3139 244 00440	FTD HOLDER DVD711	QT24400440					
0020	/A1B, /S1G,U1B	2422 025 04849	CONNECTOR,BMT 2P	QU02504849					
1100		4822 276 13775	SWITCH PUSH BUTTON	QP27613775					
1101		4822 276 13775	SWITCH PUSH BUTTON	QP27613775					
1102		4822 276 13775	SWITCH PUSH BUTTON	QP27613775					
1106									
1109		4822 276 13775	SWITCH PUSH BUTTON	QP27613775					
1110		2422 540 98423	RES CER 8MHZ CSTS*MG03	QU54098423					
1111	/N1B	4822 276 13775	SWITCH PUSH BUTTON	QP27613775					
1113		2722 171 07172	VIDEO DECODER UNIT 14-MT-27GNK						
1115		4822 267 10565	CONNECTOR PRINTED CIRCUIT 4P	QP26710565					
1117	/N1B	4822 267 10565	CONNECTOR PRINTED CIRCUIT 4P	QP26710565					
1117	/A1B, /S1G,U1B	2412 020 00724	CONNECTOR 2P						
1118		4822 267 10637	CONNECTOR 5P	QP26710637					
1205	/N1B	4822 267 10567	CONNECTOR 4P	QP26710567					
1205	/A1B, /S1G,U1B	2422 025 12488	CONNECTOR 2P	QU02512488					

**– CAUTION –**

**For repairing the DVD Module ADS-1,  
the service application software "ComPair"  
is needed. The application CD-ROM  
"ComPair" is available via MARANTZ  
organization or PCS. <Refer the page 5>  
A "service Bulletin" will publish the latest  
"ComPair" information.**



Service  
Service  
**Service**



# Service Manual



**Contents**

	<b>Page</b>		
1	Technical specifications		2
2	Warnings and remarks		4
3	Directions for use (not available)		6
4	Mechanical instructions		7
5	Test instructions		9
	Diagnostic software description		17
6	Block diagram Servo part		29
	Block diagram Digital part		30
7	<i>Electrical diagrams &amp; pwb's</i>		<i>Diagr. PWB</i>
	Servo DALAS	(Diagram 1)	31 37-42
	Servo MACE	(Diagram 2)	32 37-42
	Decoder	(Diagram 3)	33 37-42
	Memory	(Diagram 4)	34 37-42
	ST1 5505	(Diagram 5)	35 37-42
	Service interface and back-end	(Diagram 6)	36 37-42
	Testpoint overview		43 37-42
8	Alignments (not available)		45
9	IC Descriptions		45
10	Sparepart list		85

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# 1. Technical Specifications

## 1.1 Connections

### 1.1.1 Connector 1600: Supply input connector.

1. +3V3stby
2. +3V3stby
3. +5V
4. +5Vstby
5. Vreserved
6. GND
7. GND
8. GND
9. -8Vstby
10. Standby control line
11. +12Vstby
12. GND

### 1.1.2 Connector 1603: A/V 1 connector.

1. P50
2. Blue Video
3. Green Video
4. GND
5. Red Video
6. CVBS
7. GND
8. Slow blanking scart
9. -8Vstby
10. +5V
11. +5V
12. Audio mute
13. GND
14. I2S data0 out
15. I2S wordselect
16. I2S bitclock
17. GND
18. I2S systemclock
19. Center\_on
20. Kar\_bypass
21. Kar\_bypass
22. GND

### 1.1.3 Connector 1604: A/V 2 connector.

1. GND
2. Hor. sync.
3. GND
4. I2S data 2 out
5. GND
6. I2S data 1 out
7. -8Vstby
8. I2C clock
9. +12Vstby
10. I2C data
11. Vreserved
12. +3V3
13. GND
14. C video
15. GND
16. Y video

### 1.1.4 Connector 1501: I2C interface connector.

1. I2C clock
2. GND
3. I2C data
4. Standby control line

5. P50

### 1.1.5 Connector 1602: Service connector.

1. TXD
2. Service activation
3. RXD
4. Reserved for RTS
5. 5: GND
6. Reserved for CTS
7. +5V

## 1.2 Signal specifications

This the specification of all signals as described under "Connections"

H = +5V ±0.5V

h = 3V3 ±0.3V

L = 0V ±0.5V

I = 0V ±0.3V

Stby

: If the set supports a "standby" function, all supply voltages marked with "stby" have to stay on during standby.

Standby control line

: HStandby mode  
: LOn mode.

P50

: Connection between front and A/V board, and can be used as P50 signal line. The signal is not connected to the module electronics.

Slow blanking scart

: This signal switches between  
: 0V (220Ω output impedance)  
: 12Vstby/2 (455Ω output impedance)  
: 12vstby (690Ω output impedance)

Audio mute

: Can be used for audio mute transistors during stop or power on/off.  
: Mute on : +5Vstby  
: Mute off: -8Vstby via a 10kΩ resistor.

I2S data0 out

: I2S front data output.  
: Level h/l

I2S wordselect / I2S bitclock

: I2S timing signals  
: Level h/l

I2S systemclock

: 256xFS audio systemclock.  
: Level H/L

Kar\_bypass

: Bypasses the karaoke chip on the A/V board.  
: Bypass activeH  
: Bypass offL

Center\_on

: Switches the center audio to the scart output.  
: Center to scarth

SPDIF out

: L/R to scartl  
: Digital audio output  
: Level H/L

Hor. Sync	: Video Horizontal synchronisation
I2S data1 out	: I2S surround data output.
I2S data2 out	: I2S center/sub data output.
I2C clock / I2C data	: I2C databus
TXD / RXD / RTS / CTS	: Service UART to be connected direct to PC serial input.
Service activation	: Signal openNormal module start-up
Vreserved	: Reserved in case the A/V board requires an extra supply voltage.

**1.3.4 Video.**

**Standards**

**Outputs**

**Specification.**

determined by the external DAC circuit.

- : The video output standard will follow the source material.
- : The OSD standard is switchable between PAL or NTSC.
- : The module has 6 analog outputs (3 formats): Y/C CVBS RGB.
- : The output is fully according PQR3 IMS except
- : Output load > 1kΩ to GND / Cap. load < 47pF.
- : Level 0.5Vpp with 100% white
- : DC-level Sync bottom = -0.65V ± 10%
- : Some specification points are significantly better than PQR3
- : SNR on all video outputs is better than 60dB.
- : Video bandwidth > 5MHz (±3dB)

**1.3 Performance:**

**1.3.1 Digital output**

CDDA/LPCM	: according IEC958
MPEG1 is converted to LPCM	:
MPEG2, AC3 audio.	: according IEC1937
DTS.	: according IEC61937 amendment 1.
	: Digital output level is 0V / 5V with GND as reference. To meet the standards a decouple circuit is necessary.

**1.3.2 I2S output**

Accuracy	: Up to 24bit.
Sample rate	: 44.1kHz / 48kHz.
Standard	: Philips I2S output
Number of I2S outputs	: 3 (6 channel: Front / Surround / Center-Bass)
Deemphasis	: Already processed in module.
Audio source streams	: CDDA / MPEG1 / LPCM / MPEG2 / AC3
Audio trick modes	: No DTS decoding.
	: Dolby Pro Logic (multichannel downmix on front output)
	: 3D sound.

**1.3.3 Analog output**

The module has no analog audio output.	: The analog audio specification will be
--	--

## 2. Warnings and Laser safety instructions

### GB WARNING

All ICs and many other semi-conductors are susceptible to electrostatic discharges (ESD). Careless handling during repair can reduce life drastically.

When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance.

Keep components and tools also at this potential.

ESD



### NL WAARSCHUWING

Alle IC's en vele andere halfgeleiders zijn gevoelig voor elektrostatische ontladingen (ESD).

Onzorgvuldig behandelen tijdens reparatie kan de levensduur drastisch doen verminderen.

Zorg ervoor dat u tijdens reparatie via een polsband met weerstand verbonden bent met hetzelfde potentiaal als de massa van het apparaat.

Houd componenten en hulpmiddelen ook op ditzelfde potentiaal.

### F ATTENTION

Tous les IC et beaucoup d'autres semi-conducteurs sont sensibles aux décharges statiques (ESD).

Leur longévité pourrait être considérablement écourtée par le fait qu'aucune précaution n'est prise à leur manipulation.

Lors de réparations, s'assurer de bien être relié au même potentiel que la masse de l'appareil et enfiler le bracelet serti d'une résistance de sécurité.

Veiller à ce que les composants ainsi que les outils que l'on utilise soient également à ce potentiel.

### D WARNUNG

Alle IC und viele andere Halbleiter sind empfindlich gegen elektrostatische Entladungen (ESD).

Unvorsichtige Behandlung bei der Reparatur kann die Lebensdauer drastisch vermindern.

Sorgen sie dafür, das Sie im Reparaturfall über ein Pulsarmband mit Widerstand mit dem Massepotential des Gerätes verbunden sind.

Halten Sie Bauteile und Hilfsmittel ebenfalls auf diesem Potential.

### I AVVERTIMENTO

Tutti IC e parecchi semi-conduttori sono sensibili alle scariche statiche (ESD).

La loro longevita potrebbe essere fortemente ridatta in caso di non osservazione della piu grande cauzione alla loro manipolazione.

Durante le riparazioni occorre quindi essere collegato allo stesso potenziale che quello della massa dell'apparecchio tramite un braccialetto a resistenza.

Assicurarsi che i componenti e anche gli utensili con quali si lavora siano anche a questo potenziale.

### GB

Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.

### NL

Veiligheidsbepalingen vereisen, dat het apparaat in zijn oorspronkelijke toestand wordt terug gebracht en dat onderdelen, identiek aan de gespecificeerde worden toegepast.

### D

Bei jeder Reparatur sind die geltenden Sicherheitsvorschriften zu beachten. Der Originalzustand des Gerats darf nicht verändert werden. Für Reparaturen sind Original-Ersatzteile zu verwenden.

### I

Le norme di sicurezza esigono che l'apparecchio venga rimesso nelle condizioni originali e che siano utilizzati pezzi di ricambio idetici a quelli specificati.

### F

Les normes de sécurité exigent que l'appareil soit remis à l'état d'origine et que soient utilisées les pièces de rechange identiques à celles spécifiées.

### SHOCK, FIRE HAZARD SERVICE TEST:

**CAUTION:** After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins (with unit NOT connected to AC mains and its Power switch ON), and the face or Front Panel of product and controls and chassis bottom,

Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before return to user/customer.

Ref.UL Standard NO.1492.

### NOTE ON SAFETY:

Symbol : Fire or electrical shock hazard. Only original parts should be used to replace any part with symbol Any other component substitution (other than original type), may increase risk or fire or electrical shock hazard.

## LASER SAFETY

This unit employs a laser. Only a qualified service person should remove the cover or attempt to service this device, due to possible eye injury.

### LASER DEVICE UNIT

Type:	SemiconductorlaserGaAIAs
Wave length:	650 nm (DVD) 780 nm (VCD/CD)
Output Power:	7 mW (DVD) 10 mW (VCD/CD)
Beam divergence:	60 degree



**USE OF CONTROLS OR ADJUSTMENTS OR PERFORMANCE OF PROCEDURE OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.**

### AVOID DIRECT EXPOSURE TO BEAM

### WARNING

The use of optical instruments with this product will increase eye hazard.  
Repair handling should take place as much as possible with a disc loaded inside the player

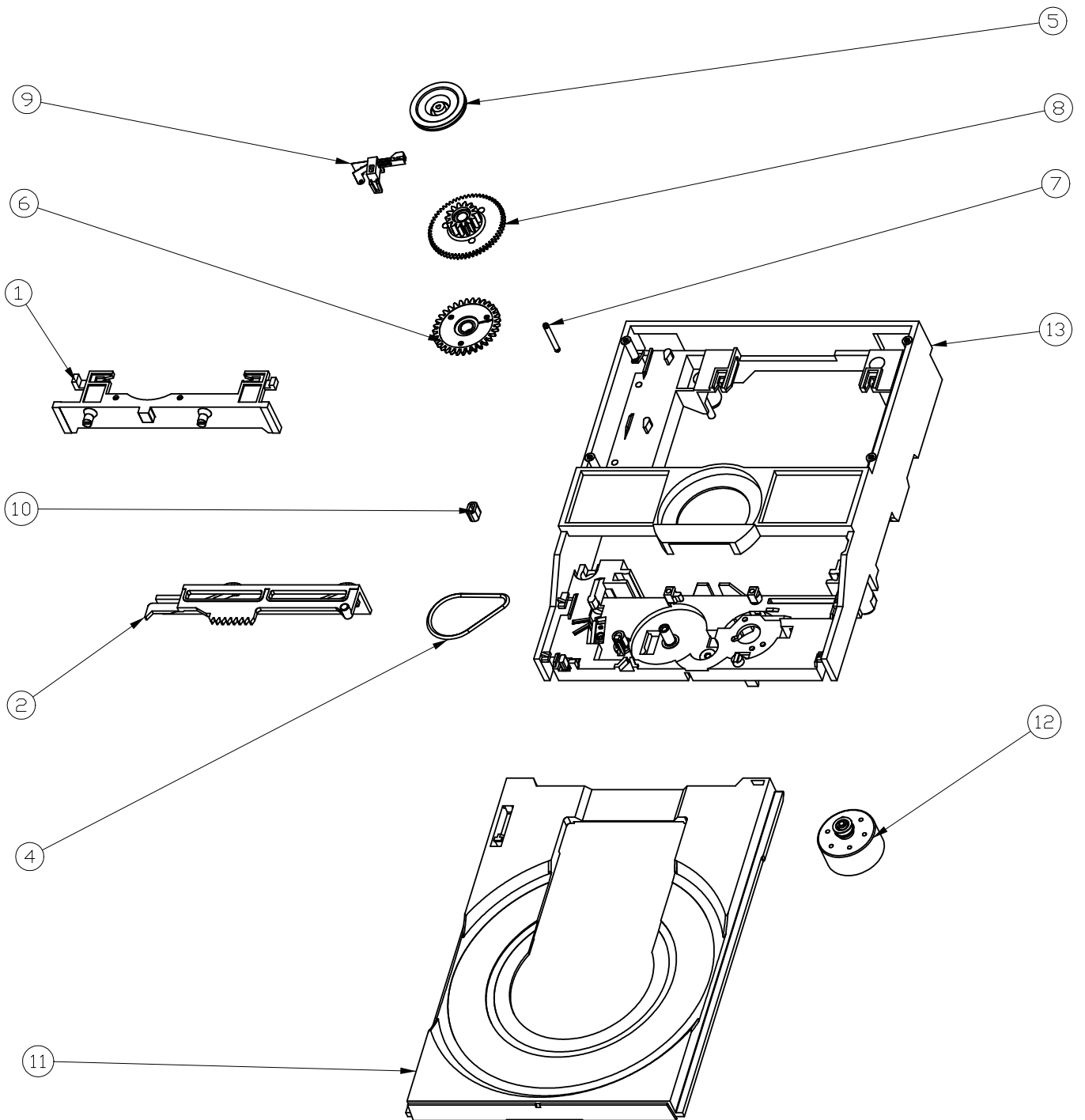
### WARNING LOCATION: INSIDE ON LASER COVERSIELD

CAUTION VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM  
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGÅ UDSÆTTELSE FOR STRÅLING  
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL ÅPNES UNNGÅ EKSPONERING FOR STRÅLEN  
VARNING SYNLIG OCH OSYNLIG LASERSTRÅLNING NÅR DENNA DEL ÅR ÖPPNAD BETRAKTA EJ STRÅLEN  
VARO! AVATT AESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTTÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN  
VORSICHT SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETZEN  
DANGER VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM  
ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

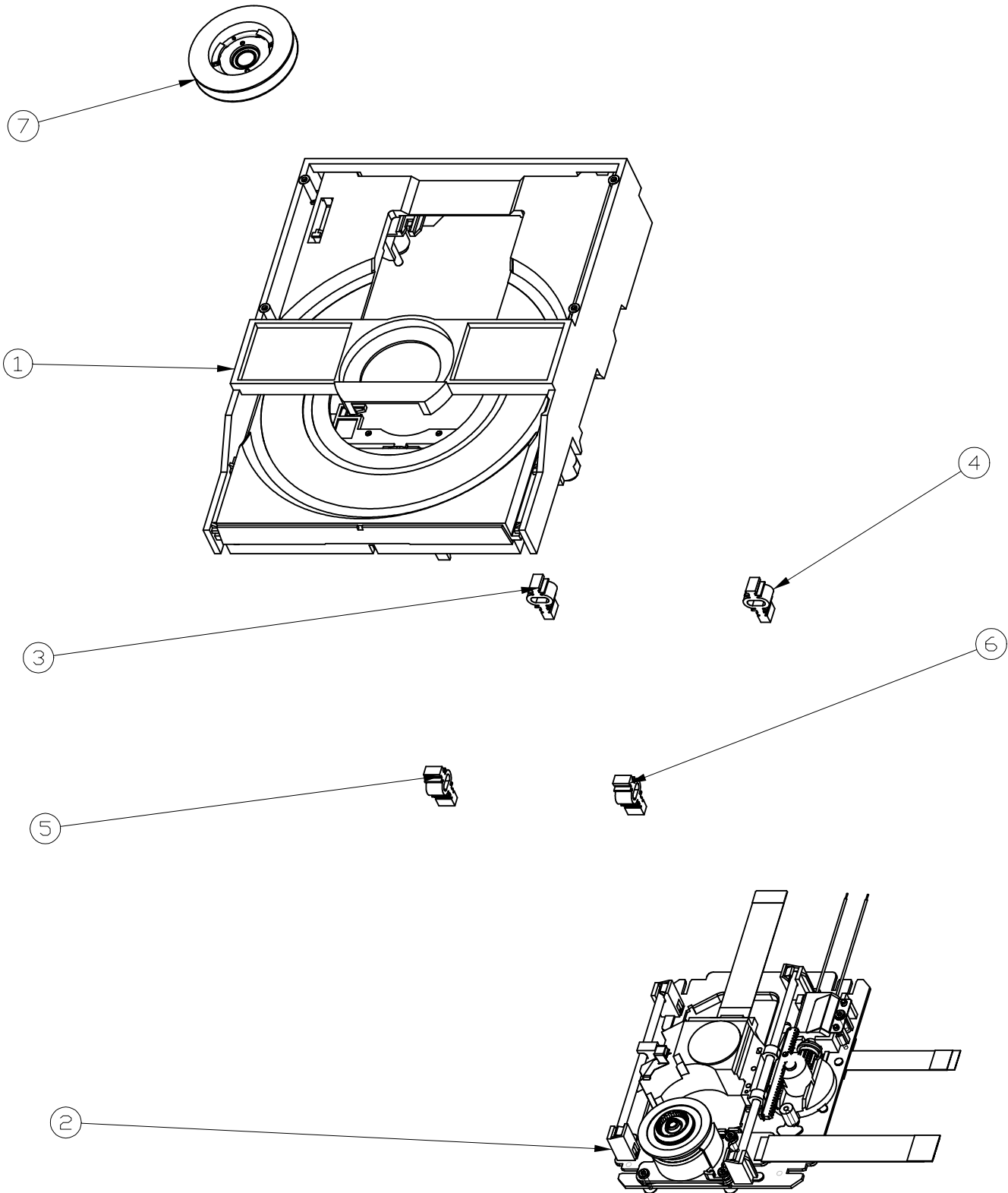
### 3. Directions for use

There is no DFU available

# 4. Mechanical instructions



- |    |                |                 |
|----|----------------|-----------------|
| 4  | 4822 358 10266 | BELT            |
| 9  | 3139 198 80010 | SWITCH          |
| 10 | 4822 532 13097 | TULE            |
| 11 | 3139194 00270  | TRAY            |
| 12 | 3139 197 50060 | TRAY MOTOR ASSY |



	9305 023 61101	VAL6011/01 LOADER COMPLETE
1	3139 197 60090	GENEVA LP LOADER ASSY
2	9305 022 60101	VAM6001/01
3+4	3139 194 00710	SUSPENSION (YELLOW)
5+6	3139 194 00620	SUSPENSION (BLUE)
7	3139 197 60060	CLAMPER ASSY



# 5. Test instructions mono board DVD-ASD1

## 5.1 General

- Impedance of measuring-equipment should be > 1MΩ.
- Most tests have to be done by software commands. Together with the software command you will find a Ref.# nbr. This is the number of the diagnostic nucleus used for this test. More detailed information can be find in the chapter "Diagnostic Nuclei".
- Levels: Most measurements are digital measurements. The high and low levels in this document got to have next specification:
  - low                   : < 0.3V
  - high                 : > 3.0V
  - LOW                 : < 0.4V
  - HIGH                : > 4.5V
- All voltages marked with "stby" have to stay on during standby.

## 5.2 General start-up measurements

### 5.2.1 Supply check:

Pin nbr.	Supply
1600-1	3V3
1600-2	3V3
1600-3	+5V0V during STAND BY
1600-4	+5Vstby
1600-5	+6V
1600-6	0V
1600-7	0V
1600-8	0V
1600-9	-8V
1600-10	0V5V during STAND BY
1600-11	+12Vstby
	0V

Check the supply currents to be sure there are no large failures on the board. Before measuring the currents, make sure that no A/V board, display board or Mercury 1 loader is connected to the mono board and that the PC interface cable is connected to the board.

Also check if the servo part gets its power.

Testpoint F608: +3V3 ±5%

Testpoint F101: +9V ±5%

The supply currents can be measured using a Tektronix AM503B current probe.

Supply	power consumption	
3V3	400mA ±10%	
5V	370mA ±10%	
5Vstby	< 5mA	
-8V	55mA ±10%	fluctuation: ±20mA
12Vstby	30mA ±20%	fluctuation: ±150mA

### 5.2.2 Reset check:

The reset circuit is triggered by the stand-by line. First make sure that the STB\_CONT line is HIGH by connecting 5V to testpoint F505. Then switch STB\_CONT over to LOW and check next timing at the STI5505 reset input (testpoint F503):

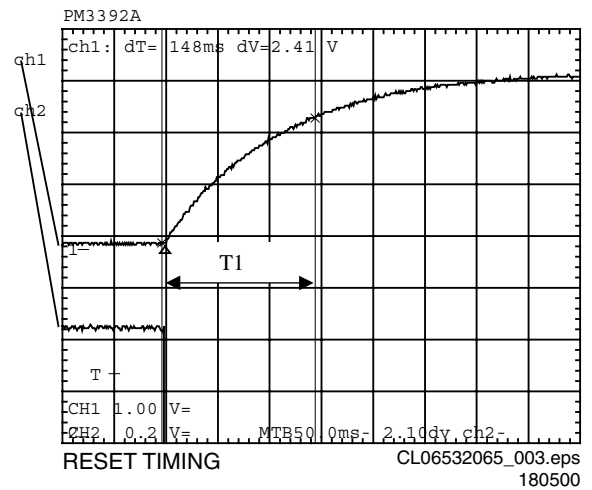


Figure 5-1

T 1 = 150msec ±25% (From 0V to 3V3 -3db)

If the reset input doesn't go high then check the circuit around transistor 7501.

### 5.2.3 Clock check

To check the correct functioning of the STI5505, we first have to check the presence of all clocks.

All clocks to be measured with 0.02% tolerance.

Clock-name	Testpoint	Frequency
27M_CLK	F051	27MHz
PCM_CLK	F566	11.2896MHz

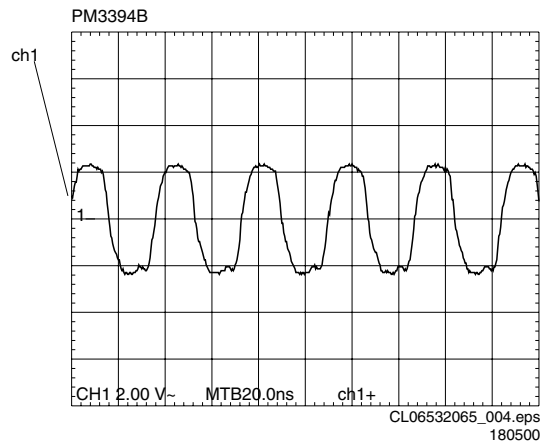


Figure 5-2

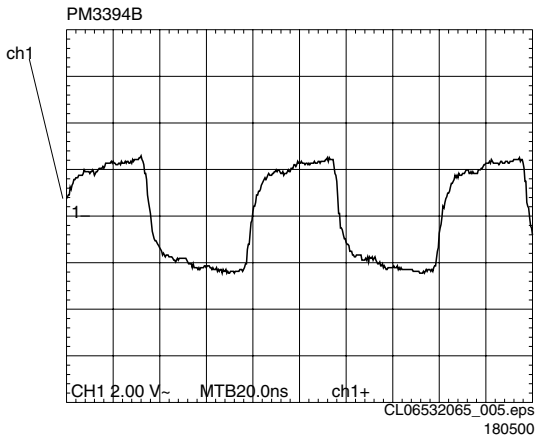


Figure 5-3

**5.3 μP environment:**

**5.3.1 General:**

All the tests are carried out by software tests. To start the software tests, connect a PC to the serial bus of the STI5505. Use connector 1602 for this connection:

Connector pin	Signal
1602-1	TXD (STI5505 out)
1602-2	Service-mode select
1602-3	RXD (STI5505 in)
1602-4	RTS (STI5505 out)
1602-5	GND
1602-6	CTS (STI5505 in)
1602-7	+5V

Now start the terminal program. Make sure that the service-pin of the μP is pulled low

(pin 1602-2) and then reset the μP (make the STB\_CONT line low). The terminal program of your PC should now display: "DVD2 Diagnostic software version ...". This message already means that the μP is running. The first 5 commands from the diagnostic software will be carried out automatically during diagnostic start-up. The other commands can be carried out by selecting the "command input". Just type the reference nbr. to do the test.

To be sure that the μP is able to run the diagnostic software, serial port will be checked during start-up.

Ref. #	Reference Name	Remark
(1)	BasicSpAcc	Serial port Access test/initialisation
(2)	BasicDramWrR	DRAM Write Read

**5.3.2 Memory check:**

The μP has a data bus that is connected to a DRAM (not present!!) and a Flash.

The μP has also an internal link to the MPEG SDRAM interface.

Next databus checks will be done at start-up to check this databus and SDRAM bus.

Ref. #	Command Name	Remark
(2b)	BasicInterconSDRAM	Data and address bus Interconnection
(2c)	BasicInterconFlash	Data and address bus Interconnection

There are 2 memory checks left that can be done by hand command

Ref. #	Command Name	Remark
6	PapChksFl	Checksum FLASH
16	CompSdramWrR	SDRAM Write Read

**5.4 General I/O port & peripherals check**

**5.4.1 I2C bus / EEprom check**

To access the EEprom, the I2C bus is used. So by writing and reading to the EEprom the chip and the bus is checked. With next commands a certain byte is written to the EEprom. The original information will always be written back into the EEprom.

Ref. #	Command Name	Remark
11	PapI2cNvram	I2C NVRAM access

The complete Eeprom can also be checked on failures by writing to all addresses and reading back. This test takes a long time (110 sec).

Ref. #	Command Name	Remark
15	PapNvramWrR	NVRAM Write Read

**5.4.2 Audio clock switch check**

For a DVD disc the audio clock has to be switched from 44.1KHz sampling to 48KHz sampling.

To do so IO-port 1 / 4 has to be switched. Send next commands and check the audio-clock

Ref. #	Remark	Testpoint	Frequency
7a	(Clock A_CLK in 44.1kHz mode)	F566	11.2896MHz ± 0.02%
7b	(Clock A_CLK in 48kHz mode)	F566	12.288MHz ± 0.02%

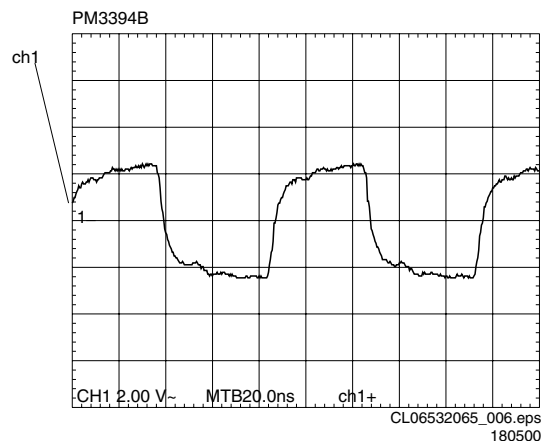
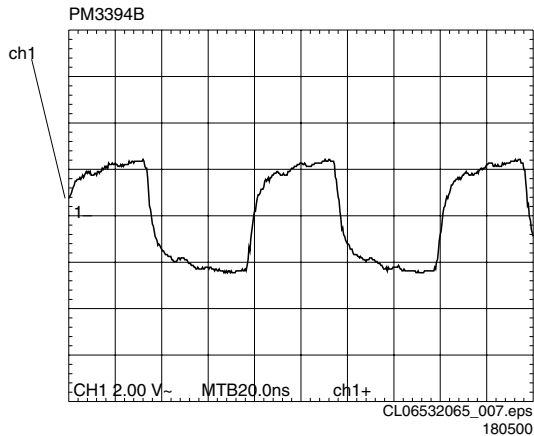


Figure 5-4

**5.4.5 Audio I2S check**

To check the audio output, connect a audio DAC to the I2S output (DVD950 A/V board) and start-up the audio test. Look at the audio outputs from the A/V board for both sine and pink noise.



**Figure 5-5**

**5.4.3 Audio deemphasis check**

The STI5505 output pins PIO 4-0 and PIO 4-1 were used to switch deemphasis on a previous type of DAC. This function is not used anymore, because deemphasis is done internally in STI5505, but the name still remains. The lines are now used for a series of functions such as centre\_on\_stereo or karaoke\_bypass. The PIO 4-0 has got a pull-up to +5V and the PIO 4-1 has not. To check these pins these commands can be used.

Ref. #	Command Name	Remark	Testpoint	Value
18e	AudioDeemp0TristateOn	PIO 4-0 Tristate On	-----	
56a	AudioDeemp0On	PIO 4-0 On	F630	HIGH
56b	AudioDeemp0Off	PIO 4-0 Off	F630	low
18f	AudioDeemp0TristateOff	PIO 4-0 Tristate Off	-----	
56c	AudioDeemp1On	PIO 4-1 On	F633	high
56d	AudioDeemp1Off	PIO 4-1 Off	F633	low

**5.4.4 Audio mute check**

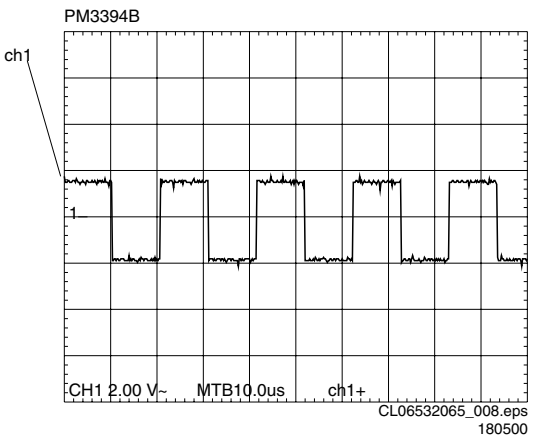
Switch on the Mute circuit by sending next command:

Ref. #	Command Name	Remark
19a	AudioMuteOn	AudioMuteOn

Check the Mute output again at testpoint F625: 4.7V ±10%  
Switch off the Mute circuit by sending next command

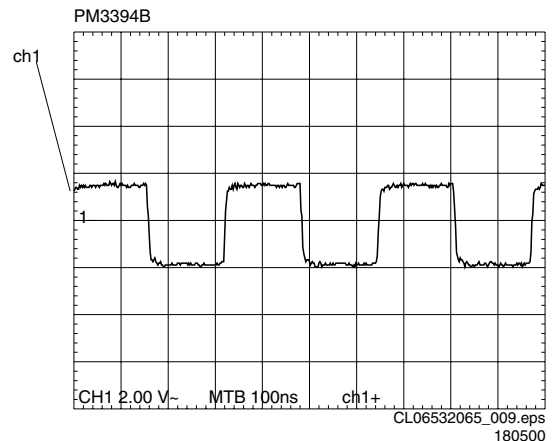
Ref. #	Command Name	Remark
19a	AudioMuteOff	AudioMuteOff

Check the Mute output at testpoint F625: -8V ±10%



**Figure 5-6**

SCLK at testpoint F637



**Figure 5-7**

PCM\_OUT0 at testpoint F638  
PCM\_OUT1 at testpoint F659  
PCM\_OUT2 at testpoint F658

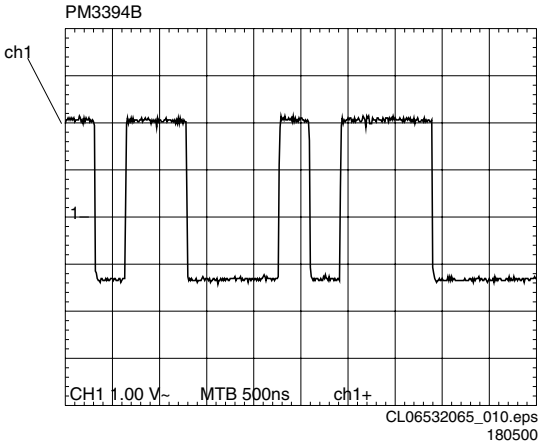


Figure 5-8

PCM\_CLK at testpoint F640

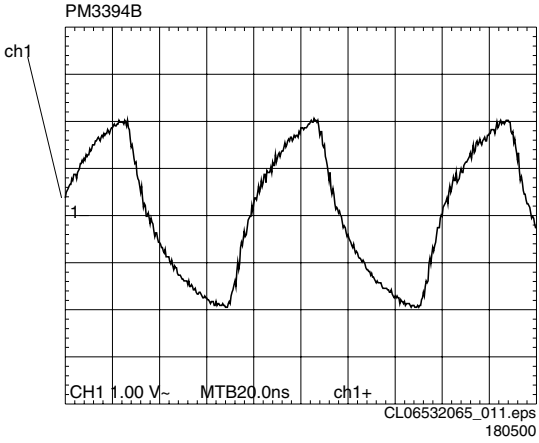


Figure 5-9

SPDIF at testpoint F644

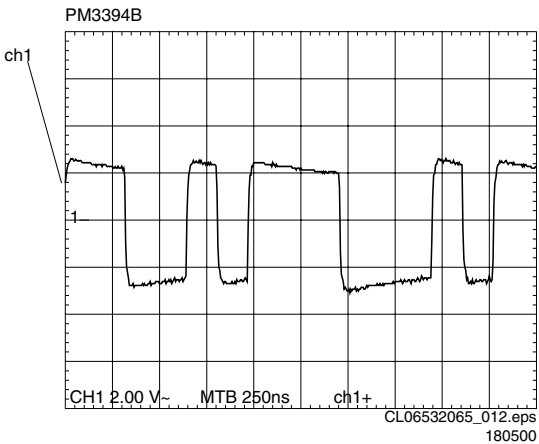


Figure 5-10

To switch the audio signal off, press the STOP button on the front.  
Without A/V board all levels should be switching between low and high except:

- PCM\_OUT1 and PCM\_OUT2 only between low and high for pink noise. For sine, this is low.
- PCM\_CLK and SPDIF switches between LOW and HIGH

Alternatively, there is a check that can be done without A/V board.

First, let the decoder generate pink noise on the audio outputs.

Ref. #	Command Name	Remark
20a	AudioPinkNoiseOn	Audio Pinknoise On

Measure then these signals on level and frequency.

Signal	Level between	Frequency
LRCLK	low/high	48kHz ± 0.02%
SCLK	low/high	3.072MHz ± 0.02%
PCM_CLK	LOW/HIGH	12.288 MHz ± 0.02%
PCM_OUT0, 1, 2	low/high	N/A
SPDIF	LOW/HIGH	N/A

Put the pink noise off:

Ref. #	Command Name	Remark
20b	AudioPinkNoiseOff	Audio Pinknoise Off

## 5.5 VIDEO

### 5.5.1 Video output check

Check DC output-level at all video-outputs at conn 1603-2,3,5,6 and conn 1604-16: -0.65V ± 10%

Generate a color-bar via next software commands:

Ref. #	Command Name	Remark
23a	VideoColDencOn	Colourbar DENC On
23b	VideoColDencOff	Colourbar DENC Off

Check video output at the next testpoints:

F646: R\_VID

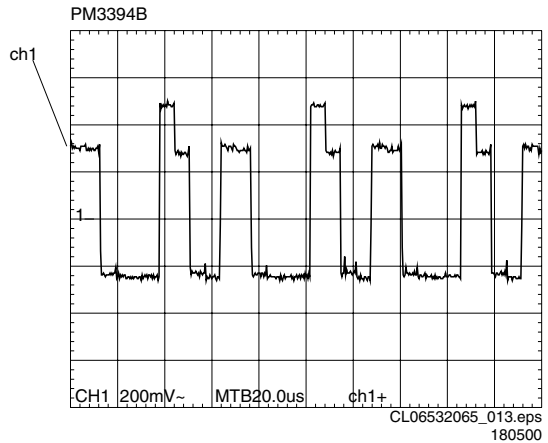


Figure 5-11

F649: G\_VID

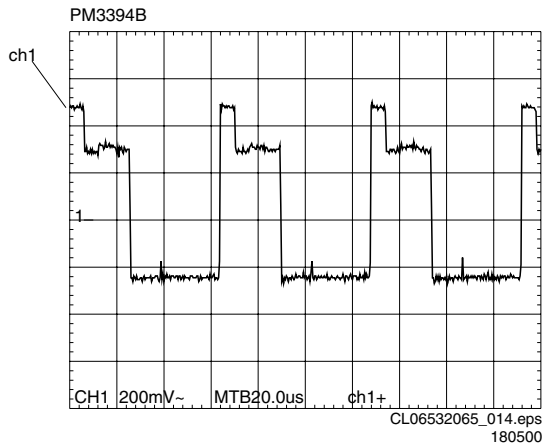


Figure 5-12

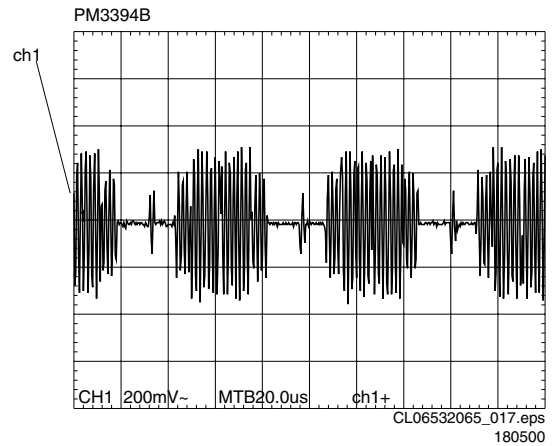


Figure 5-15

F653: B\_VID

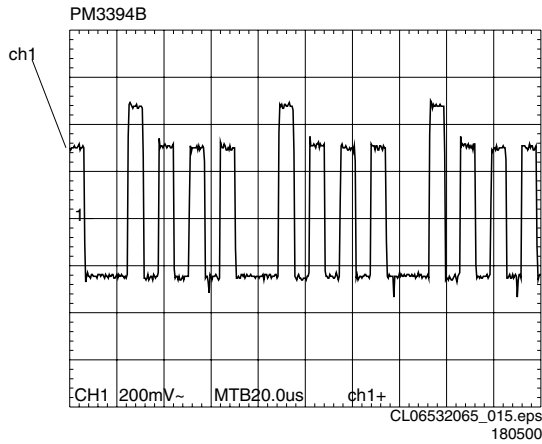


Figure 5-13

F666: Y\_VID

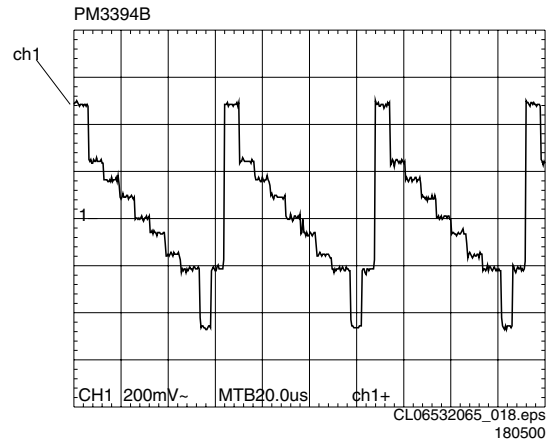


Figure 5-16

F657: CVBS

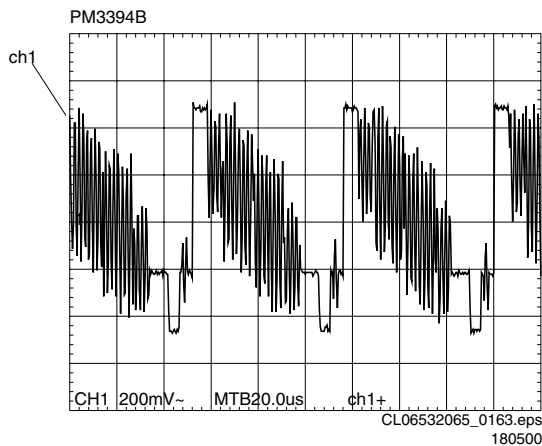


Figure 5-14

F665: C\_VID

### 5.5.2 Scart-switching voltage

An additional part of the video-path is the scart-switching voltage.

This voltage can be 0V, 6V, 12V.

Check at testpoint F620 the output-voltage while using next commands:

Ref. #	Command Name	Remark
25a	VideoScartLo	Sends out 0V ± 0.5V
25b	VideoScartMi	Sends out 6V ± 10%
25c	VideoScartHi	Sends out 12V ± 10%

### 5.5.3 Video Hsync check.

To measure the correctness of this output, F656 should be checked.

Ref. #	Command Name	Remark	Value
23a	VideoColDencOn	Colourbar	DENC on 15.625 kHz ± 0.02% Vpeak-peak > 3V
23b	VideoColDencOff	Colourbar	DENC off No measurements needed

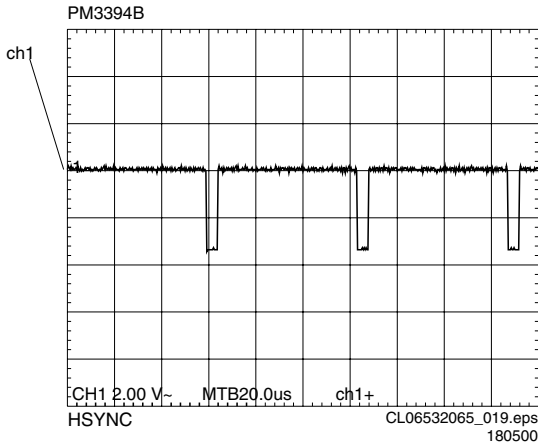


Figure 5-17

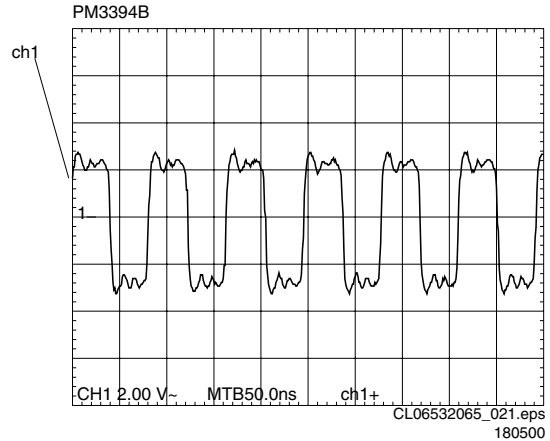


Figure 5-19

5.6 Servo

5.6.1 General start-up measurements:

Reset the Basic Engine part

Ref. #	Command Name	Remark
44	BeReset	Basic Engin

Check Vref

Name	Testpoint	Value
Vref	F188	2.5V+/-0.3

Check I2S interface

Name	Testpoint	Value
B_BCLK	F347	6.0MHz +/-0.1

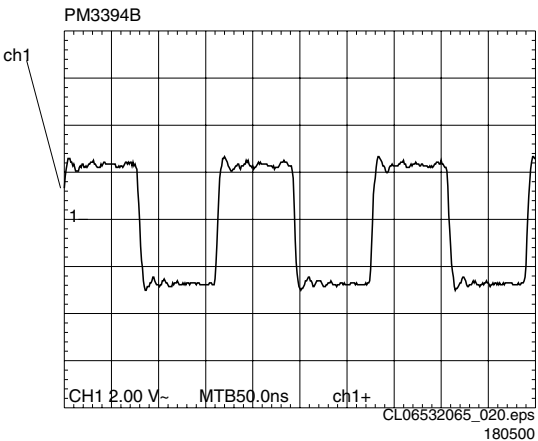


Figure 5-18

CL1F33712.0MHz +/-0.2

- B\_WCLKF343HIGH
- StopclkF338HIGH
- B\_SyncF344HIGH
- B\_V4F348HIGH

5.6.2 Spindle Motor:

Before switching on the discmotor, check the following testpoints:

Name	Testpoint	Value
Stby	F357	high
Stby-out	F355	LOW
Moto1	F361	3V±0.3

Switch the Discmotor on/off with next commands:

Ref. #	Command Name	Remark
39a	BeDiscmotorOn	Discmotor on
39b	BeDiscmotorOff	Discmotor off

Check the following signals when discmotor has been switched on::

Name	Pin nr.	Frequency
Stby	F357	low
Stby-out	F355	HIGH
Moto1	F361	3V±0.5V
A3	F350	see oscillogram
A2	F352	see oscillogram
A1	F353	see oscillogram

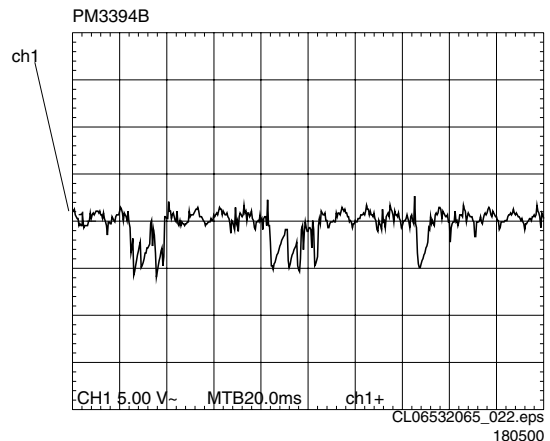


Figure 5-20

- T1 F280 see oscillogram
- T2 F368 see oscillogram
- T3 F371 see oscillogram

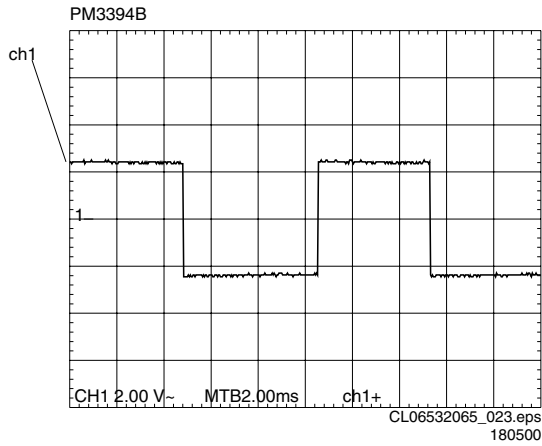


Figure 5-21

- VH F365 3V±0.5V
- H1+ F354 see oscillogram
- H1- F359 see oscillogram
- H2+ F364 see oscillogram
- H2- F366 see oscillogram
- H3+ F367 see oscillogram
- H3- F370 see oscillogram

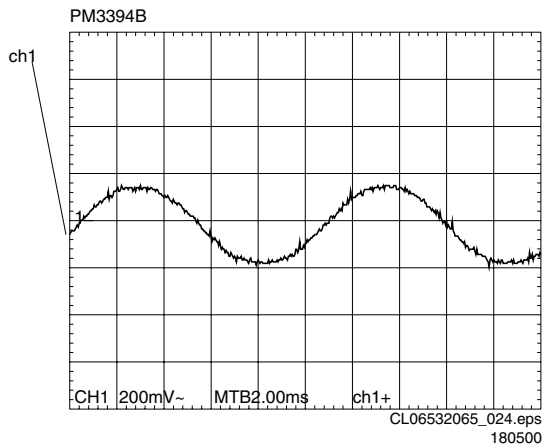


Figure 5-22

Switch the discmotor off.

5.6.3 Radial

Switch the radial control on/off with the following commands:

Ref. #	Command Name	Remark
40a	BeRadialOn	Radial control on
40b	BeRadialOff	Radial control off

Check the following signals:

Name	Testpoint	Value
Rad -	F128	4.3V±0.5V
Rad +	F121	4.3V±0.5V

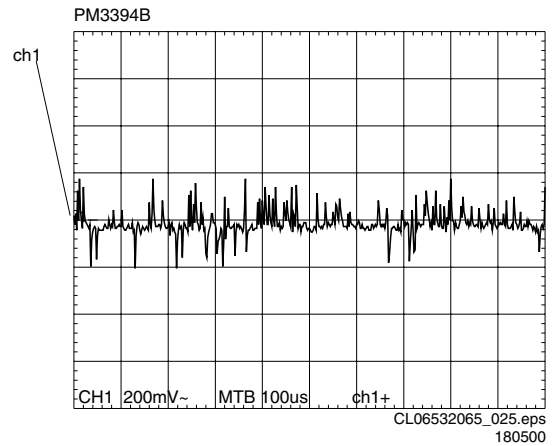


Figure 5-23

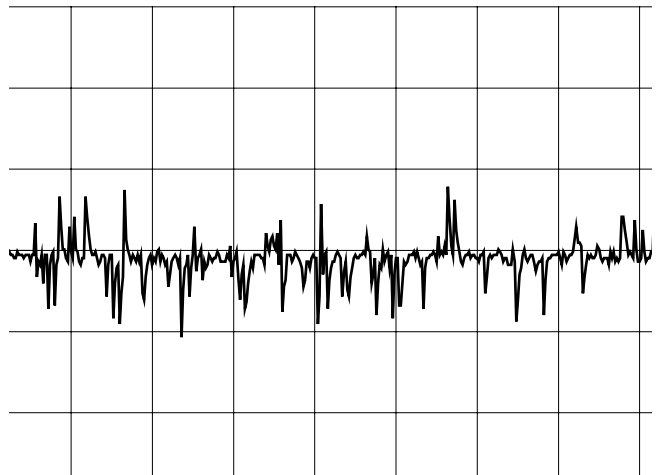


Figure 5-24

Check for pulse density signal RA at testpoint F227

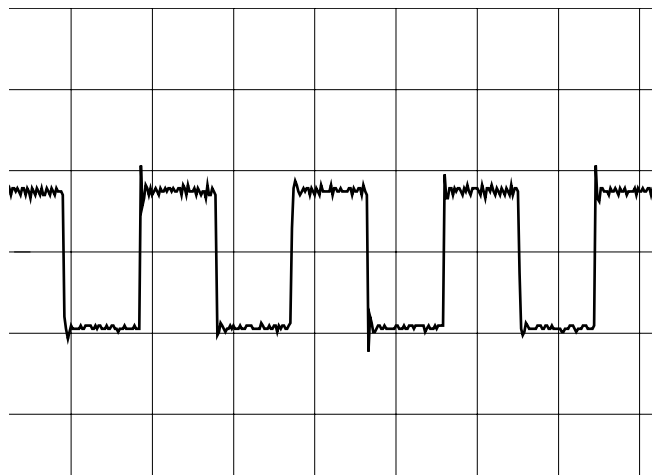


Figure 5-25

Check if laser is switched on (visual check of laserlight).  
Switch the radial control off.

5.6.4 Sledge

Use the following commands to move the sledge:

Ref. #	Command Name	Remark
41a	BeSledgeIn	Sledge inwards
41b	BeSledgeOut	Sledge outwards

Check pulse density signal SL at testpoint F221

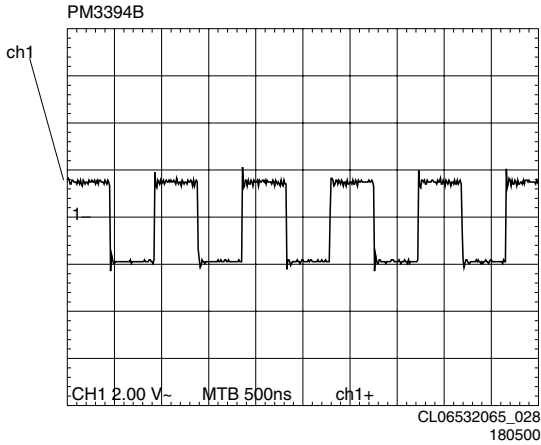


Figure 5-26

Name Testpoint Value

SI - F012 4.5V±0.5V

SI + F011 4.5V±0.5V

Measure peak to peak signal on SL- and SL+ while moving sledge outwards.

Name Testpoint Value

SI - F012 10Vptp +/-0.5

SI + F011 10Vptp +/-0.5

Measure input sledge control (sledge in home position)

Name Testpoint Value

Sinph F182 2.2V±0.5V

Cosph F192 2.2V±0.5V

5.6.5 Tray:

To open and close the tray use the following commands:

Ref. #	Command Name	Remark
43a	BeTrayIn	Tray in
43b	BeTrayOut	Tray out

Measure the driver outputs of the BA5938FM for the tray closed.

Name Testpoint Value

Vo2 - F116 4.3V±2.0V

Vo2 + F111 4.3V±2.0V

Measure again the driver outputs while the tray is opening.

Name Testpoint Value

Vo2 - F116 2.0V±1.0V

Vo2 + F111 6.0V±1.0V

5.6.6 Focus

To switch the Focus motor on/off, use the following commands:

Ref. #	Command Name	Remark
38a	BeFocusOn	Focus on
38b	BefocusOff	Focus off

Measure the driver outputs of the BA5938FM for the Focus off.

Name Testpoint Value

foc - F124 4.3V±0.5V

foc + F127 4.3V±0.5V

Switch the focus on

Measure again the driver outputs

Name Testpoint Value

Foc - (sawtooth) F124 1V±0.2V

Foc + (sawtooth) F127 1V±0.2V

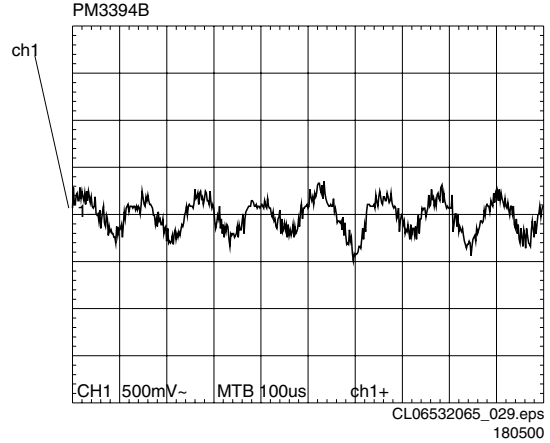


Figure 5-27

Check for pulse density signal FO at testpoint F234

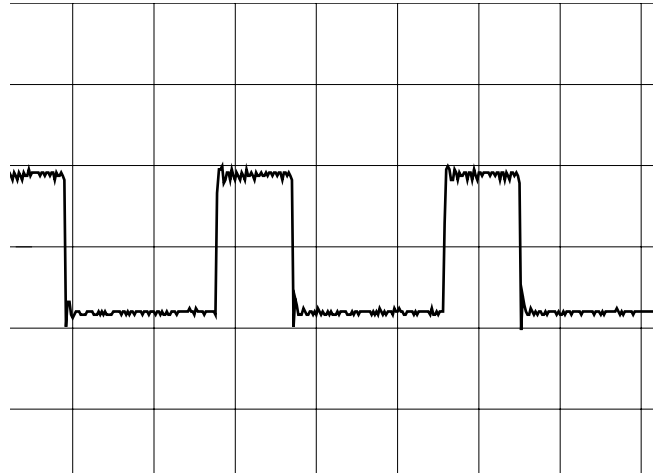


Figure 5-28

Check for laserlight.

Switch the focus off

5.6.7 Hf path

Play DVD test disc.

Measure outputs of diodes A, B, C, D, E, F.

Name Testpoint Value

A F140 2.6V±0.2V

B F141 2.6V±0.2V

C F143 2.6V±0.2V

D F144 2.6V±0.2V

E F147 2.6V±0.2V

F F148 2.6V±0.2V

At outputs of diodes A, B, C, D the following oscillogram can be measured:



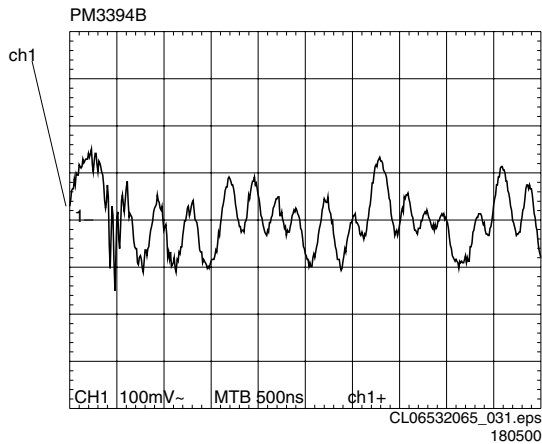


Figure 5-29 cl06532065-031

Measure DVDALAS outputs

Name	Testpoint	Value
RFO DC	F146	2.5V ±0.2V
O1	F156	25mV±10mV
O2	F159	25mV±10mV
O3	F169	25mV±10mV
O4	F166	25mV±10mV
S1	F174	25mV±10mV
S2	F175	25mV±10mV

At output RFO, the following oscillogram can be measured:

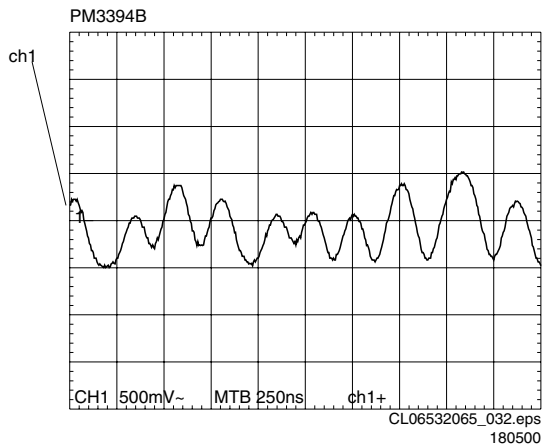


Figure 5-30

## 5.7 Diagnostic software description

### Introduction

#### 5.7.1 Introduction

**Purpose**

This document describes all interfaces from the outside world to the diagnostic software, what is needed to use these interfaces and how to access them. Changes for DVDv2b are marked.

**Scope**

This document has been realised within the framework of the product development of the second generation DVD video player. This player forms the basis for future DVD developments as described in the DVDv2 Overall Project Management Plan.

#### 5.7.2 Definitions and abbreviations

**Definitions**

Control PC	Automatic test equipment, part of the production control system in the factory, to control the execution of Diagnostic Nuclei in the DVD player.
Diagnostic Nucleus	Part of the Diagnostic Software. Each nucleus contains an atomic and software independent diagnostic test, testing a functional part of the DVD player hardware on component level.
Script	Part of the Diagnostic Software. Each script contains a sequence of Diagnostic Nuclei to be executed.
Service PC	PC used by a service- or repair-person to communicate with the Diagnostic Software in the DVD player.

**Abbreviations**

FDS	Full Diagnostic Software
-----	--------------------------

## 5.8 Overview of Interfaces

The table below shows an overview of the user interfaces of the Diagnostic Software. The table is based on logical interface, interfaces as seen from user perspective. A logical interface can use one or more physical interface components. The DVD has only a single RS232 port, implying that all interfaces using this port are mutually exclusive.

Logical Interface	Description	Physical interface components
Menu Interface	Menu-driven activation of individual nuclei, used for Level 2/ Second Line diagnostic mode. Users are service or repair people	Service PC running a terminal emulation program, connected to the RS232 port of the DVD player Test pin
Command Line Interface	Used during Level 1 diagnostic mode. Used to send commands from the Control PC into the DVD hardware.	Control PC, running a control program (e.g. Asterix), connected to RS232 port of the DVD player Test pin
Script Interface	Used to execute Player Test Script (including reading the error log) and Dealer Test Script.	Local keyboard Local display
S2B interface	Used for S2B communication with the Basic Engine	Service PC, running a S2B monitor program, connected to the RS232 port of DVD player Test pin
Download Interface	Used to download diagnostic software into the DVD player	Service PC running a terminal emulation program, connected to the RS232 port of the DVD player Test pin

In the next chapters the logical user interfaces are described in more detail including the exact use of the physical interface components.

## 5.9 Description Of Interfaces

### 5.9.1 Menu Interface

The menu interface is part of the Level 2 / Second Line diagnostic mode. Via the menu interface it is possible to control the execution of the Diagnostic Nuclei.

#### Set-up physical interface components

Hardware required:

- Service PC
- one free COM port on the Service PC
- special cable to connect DVD player to Service PC

The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM port must be connected via a special cable to the RS232 port of the DVD player. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

### 5.9.2 Code nr. PC interface cable: 3122 785 90017

#### Activation

Switch the player on and the following text will appear on the screen of the terminal (program):

```
DVDv2 Diagnostic Software version 1.0

SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK

(M)enu, (C)ommand (S)2B-interface or (D)ownload? [M]:@M <-
<main menu>
Select>

CL06532065-033.eps
180500
```

The first line indicates that the Diagnostic software has been activated and contains the version number of the diagnostic; this is also an indication that the first basic nucleus (nucleus number 1) has been executed successfully. The next three lines are the successful result of the subsequent basic tests (nuclei 2, 3, 4 and initialisation of Karaoke chip respectively). If not all these messages appear on the terminal screen, then the related nucleus found an error. The last line is the prompt asking to choose for an interface form. If a choice for Menu Interface has been made, the main menu will appear. For the layout of the menus, see page 25.

To switch between interfaces, the DVD player needs to be switched off and on again.

Note1 : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.

Note2 : The Dram tests are no longer executed because the player has no DRAM .

Note3 : When the stack is located in the internal memory, the test with the SRAM doesn't work and will be left out.

Note4 : The karaoke initialisation will also take place if there is no karaoke-chip in the player.

#### Usage

A selection can be given by the user by typing the number of the menu-item chosen at the prompt. Each entry must be terminated with a . Invalid selections will cause an error message by the Menu Handler. Example:

```
Select > 60
0001 Invalid menu selection ER @
Press RETURN to continue...@

CL96532111_021.eps
071099
```

Result and output of an activated (and terminated) nucleus will be sent back to the service terminal. Example:

```
Select > 16
1601 Data line X is not connected to the SDRAM ER @
Press RETURN to continue...@

CL96532111_022.eps
071099
```

After the user presses a key, the current menu is rebuilt on screen.

Pressing < return > at the prompt without any further input at the terminal will always rebuild the main menu.

#### Termination

The menu interface is terminated by switching off the DVD player.

### 5.9.3 Command Line Interface

The command line interface is part of level 1 diagnostic mode. Via a command line interface the execution of Diagnostic Nuclei can be controlled.

#### Set-up physical interface components

Hardware required:

- Control PC
  - one free COM port on the Control PC
  - special cable to connect DVD player to the Control PC
- The control PC must use the following port settings for the used COM port: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The control PC is connected with a special cable to the RS232 port of the DVD player. Via the same connection the test pin will be connected to ground.

#### Activation

After power on the next text will sent to the control PC

```
DVDv2 Diagnostic Software version 1.0
SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK

(M)enu, (C)ommand (S)2B-interface or (D)ownload? [M]:@ C <-
DD>                                     CL06532065_034.eps
                                         180500
```

The first line indicates that the Diagnostic software has been activated and contains the version number; this is also an indication that the first basic nucleus (nucleus number 1) has been executed successfully. The next three lines are the successful result of two subsequent basic tests (nuclei 2, 3, 4 and karaoke initialisation respectively). If not all these messages appear on the terminal screen, then the related nucleus found an error. The fifth line lets the user choose between the two possible interface forms. The last line is the prompt ("DD>"). The diagnostic software is now ready to receive commands.

Note1 : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.

Note2 : When it is a player without DRAM, the DRAM tests are left out.

#### Usage

The commands that can be given are the names or the numbers of the nuclei. A command must be terminated with a < return > character from the control PC. When typing commands, the backspace key can be used to make corrections.

In case of typing errors in the command, an error message is returned. Example:

```
DD >CompSdarmWrR
0001 Unknown command ER @
DD>                                     CL96532111_024.eps
                                         071099
```

If the command (the nucleus name or number) is recognised, the nucleus is executed. Result and output of an activated (and terminated) nucleus will be sent back to the control PC according to the standard layout as defined in Appendix C.

Example in case the command is correct:

```
DD >CompSdarmWrR
1600 OK @
DD>                                     CL96532111_025.eps
                                         071099
```

Example in case the result is an error:

```
DD >CompSdarmWrR
1601 Address line X not connected to the SDRAM @
DD>                                     CL96532111_026.eps
                                         071099
```

#### Termination

The command line interface is terminated by switching off the DVD player.

### 5.9.4 S2B Interface (not for service)

#### Set-up physical interface components

Hardware needed:

- Control PC
- one free COM port on the Control PC
- special cable to connect DVD player to Control PC
- S2B monitor tool running on the Control PC

#### Activation

To start the S2B interface, connect the RS232 cable to the Control PC in the correct manner. Then start the PC, start the monitor tool and start the DVD player; turn off the monitor tool, turn on S2B monitor tool. The S2B monitor tool now takes all communication.

The S2B interface is activated by sending the bit pattern 110x xxxx with the first character to the DVD player, when the user is asked to choose an interface type. The command handler will then activate the S2B pass-through nucleus. The character sent will be passed to this nucleus without loss.

Note: The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.

#### Termination

To terminate S2B pass-through mode, switch off the DVD player.

### 5.10 Script Interfaces

This interface is used during execution of the Player Script and the Dealer Script to display output and error messages. The local display will be used to display the output and the error messages.

#### 5.10.1 Dealer Script

#### Set-up physical interface components

Hardware required:

- DVD player
- The DVD player is tested stand-alone: no other equipment than the DVD player is needed.

#### Activation

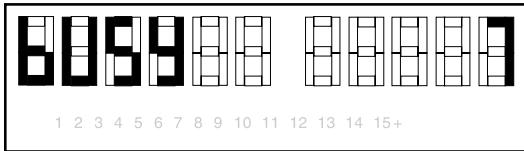
The dealer script is activated by pressing OPEN/CLOSE and PAUSE on the local keyboard of the DVD player simultaneously during power-on.

Note : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.

### Usage

The test requires no user interaction. A number of nuclei will be run before a message is returned indicating if there is a failure in the DVD player.

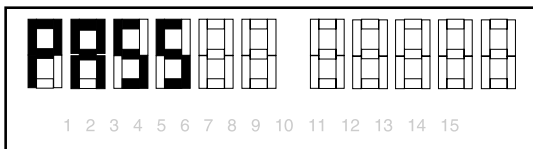
During the execution of a script, a progress indicator is displayed on the local display of the DVD player.



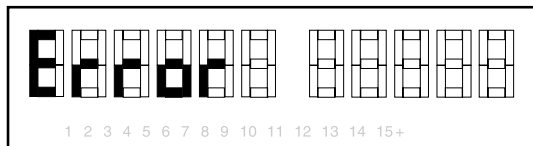
CL96532111\_017.eps  
071099

The counter at the right side of the display counts down from the number of nuclei to be run to zero. At zero all nuclei from the script have been run and the result (PASS/Error) is displayed on the local display of the DVD player.

When the dealer script has been completed, the results are displayed in the following manner:



CL96532111\_018.eps  
071099



CL96532111\_019.eps  
071099

### Termination

To turn off the dealer test, the DVD player must be powered down.

## 5.10.2 Player Script

### Set-up physical interface components

Hardware needed:

- DVD player
- television set, connected to the DVD player
- 6 audio speakers
- an external video source

### Activation

To activate the player script, press OPEN, CLOSE and STOP keys on the local keyboard of the DVD player simultaneously during power-on.

### Usage

The player test requires human interaction to decide whether nuclei give correct output, e.g. the user needs to confirm the results of the display test. This needs to be given through the

local keyboard on the DVD player. Which keys can be used for this purpose is described with each test.

Module test (with user interaction)

During the first phase of the dealer test, the three main modules (Digital PWB, Display PWB and Basic Engine) are tested; some interaction from the user is required.

#### 1. Testing the Display PWB

This involves testing the local display and keyboard, but also testing the remote control and the leds.

#### The Display Test

During the display test, different patterns will be shown on the local display of the DVD player. The user needs to step through these patterns using the PLAY key on the local keyboard. If any of the displayed patterns is incorrect, the display test has failed, and also the player test has failed.

The test patterns on display will be repeated in a loop (stepped through using PLAY) until the user presses NEXT on the local keyboard to proceed to the next test.

#### The LED Test

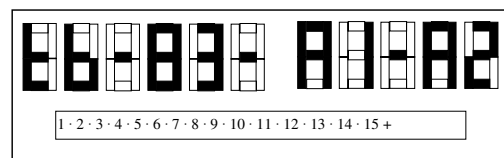
Next is the LED test; the LEDs on the DVD player are lit.

Pressing PLAY will indicate that all LEDs are operational. To indicate that a LED did not light up, the user must press the PAUSE key. Pressing PLAY or PAUSE will proceed the user into the next test.

#### The Keyboard Test

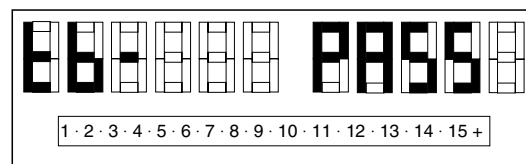
During the keyboard test, the user needs to press all the keys on the local keyboard one by one. On the local display each key is represented by its scancode (a hexadecimal 2-digit code identifying the key to the DVD player).

Pressing a key will show its representing code on the local display of the DVD player: the first hexadecimal digit identifies the key pressed, the second indicates how many times this particular key was detected. In case the key is pressed more than once, the scancode is displayed as many times, with the second digit of its code increased each time. The display of scancodes scrolls from right to left, with the most recent scancode at the right. The following example gives a possible layout of the local display during the display/remote control test:



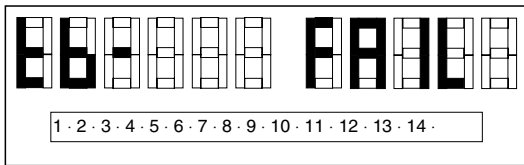
CL 96532097\_004.eps  
130999

To terminate the keyboard test, press the NEXT key on the local keyboard of the DVD player and keep it pressed for 1 (one) full second. The keyboard test will terminate with a message on the local display. In case the keyboard test was successful, the message is:



CL 96532097\_007.eps  
130999

In case the keyboard test was not successful, the message will be:

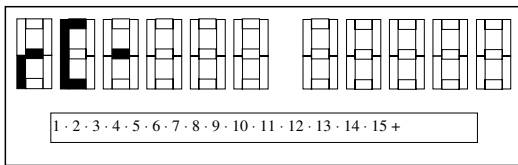


CL 96532097\_008.eps  
130999

If the "tbFAIL"-message is displayed, the player test has failed. This is the end of the player test: turn off the DVD player, or press NEXT on the local keyboard of the DVD player to proceed to the next test.

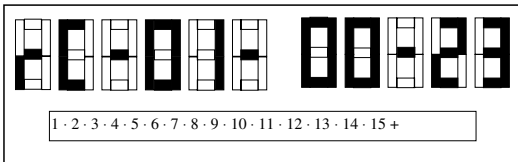
*The remote control test*

For the remote control test, the user must press a key (any key) on the DVD's remote control. The display at the start of the test looks as follows:



CL 96532111\_032.eps  
071099

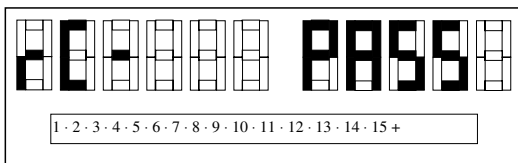
When a remote control code has been received, its scancode is displayed as follows:



CL 96532097\_009.eps  
130999

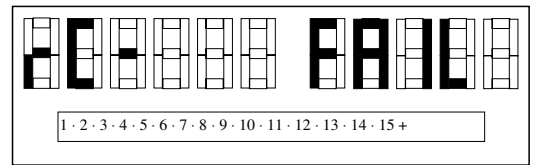
The NEXT key can be pressed to exit this test. However, if the user requires to test all keys on the remote control, (s)he can continue to press keys and these will all be displayed on the local display. With a code-table at hand this test can be used to test the full functionality of the DVD's remote control.

When the user has pressed NEXT on the local keyboard (NOT on the remote control!), the result of the remote control test is shown on the local display as follows:



CL 96532097\_011.eps  
130999

in case of succes;



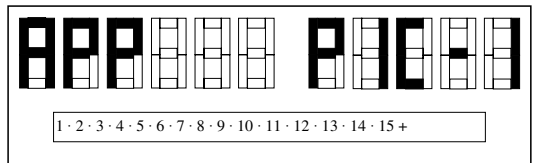
CL 96532097\_012.eps  
130999

if the test fails.

Pressing NEXT on the local keyboard again will proceed to the next test.

2. Testing the Monoboard

The picture tests involve putting a predefined picture on the connected television set, and asking the user for confirmation. When the picture has been put on screen, the local display asks for confirmation by the user as follows:

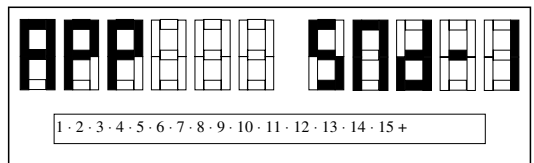


CL 96532097\_013.eps  
130999

If the user presses PLAY, he confirms the test; pressing PAUSE will indicate a fault in the test. At this time, the player test had failed and the DVD player can be switched off, or the user can proceed to the next test by pressing NEXT on the local keyboard of the DVD player.

Pressing the NEXT key on the local keyboard will start the next picture test (Colour set-up functional test).

When the picture tests are finished, the sound tests are run. A predefined sound will be generated, and again the user is asked to confirm this. The local display looks as follows:



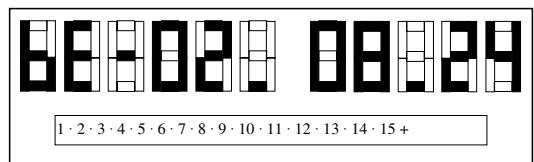
CL 96532097\_014.eps  
130999

Pressing PLAY confirms the test, PAUSE indicates test failure. If the test is faulty, the player test failed and the DVD player can be shut off. Subsequent sound tests will be numbered in ascending order.

Pressing NEXT on the local keyboard of the DVD player will take the user into the next test.

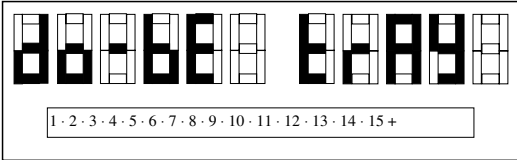
3. Testing the Basic Engine

Most tests on the basic engine require user interaction. When the basic engine tests are started, the version of the basic engine which is present in the DVD player is shown on the local display, as follows:



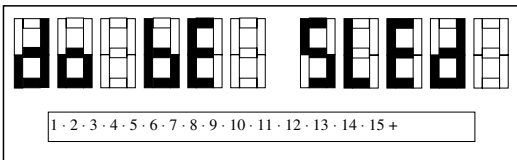
CL 96532097\_015.eps  
130999

The version number is displayed in decimal representation (the underscore replacing the dot). When the user presses NEXT on the local keyboard, the tests on the basic engine are started. First, the tray operation is tested. The user can move the tray in and out by pressing the PLAY or PAUSE key on the local keyboard (both keys have essentially the same function). The results need to be checked visually by the user, the software cannot detect any faults. The local display looks as follows:



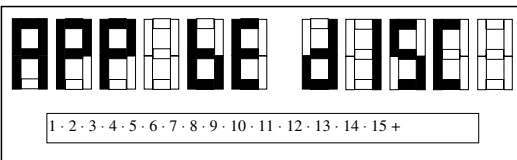
CL 96532097\_016.eps  
130999

To indicate this is a test of which the result is to be checked by the user, the first word on the local display is "do". Except for testing the tray, this test is also meant to give the user the opportunity to put a disc into the DVD player for subsequent basic engine tests. Some of the following tests need a disc in the DVD player to operate properly. Always put a disc into the DVD player during this test! At the end of the basic engine tests there is opportunity to remove it (before the looptests start). Pressing the NEXT key on the local keyboard proceeds to the next test. Second test is the sledge test; the user is asked to move the sledge by using the keys PLAY and PAUSE on the local keyboard (both keys have essentially the same function). This test needs to be checked visually by the user; the software cannot detect any faults. The local display during this test looks as follows:



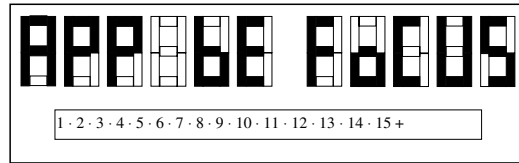
CL96532097\_017.eps  
130999

After pressing NEXT on the local keyboard the discmotor is tested; the local display looks as follows:



CL 96532097\_018.eps  
130999

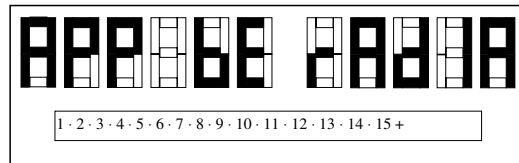
The user is required to listen if the disc motor is running; this must be confirmed by pressing PLAY on the local keyboard. The PAUSE key is used to indicate the discmotor does not run. Pressing NEXT on the local keyboard starts the focus test. The local display looks as follows during this test:



CL 96532097\_019.eps  
130999

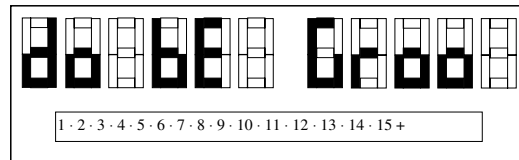
By pressing PLAY the user confirms successful focussing by the basic engine; pressing PAUSE indicates a fault in the focus function.

Pressing NEXT on the local keyboard starts the radial function; the local display looks as follows:



CL 96532097\_020.eps  
130999

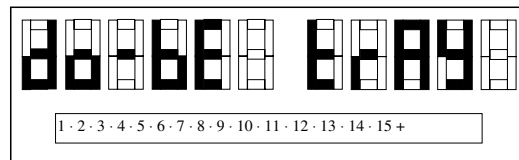
Again, PLAY confirms the result, PAUSE indicates an error. After pressing NEXT on the local keyboard, the grooves/jump test is started. As this is also a test that cannot be checked by the software, the user needs to perform a visual test. The local display looks as follows:



CL 96532097\_021.eps  
130999

By pressing PLAY the next grooves/jump position is taken; pressing PAUSE will go to the previous grooves/jump position. Switching through the different positions is done in a cyclic manner.

Press the NEXT key on the local keyboard to proceed to the last basic engine test: again, the tray is tested. This has been done at the beginning of the basic engine test already, the repeat is only meant to enable the user to remove the disc in the tray before proceeding. The local display will look as follows:



CL 96532097\_016.eps  
130999

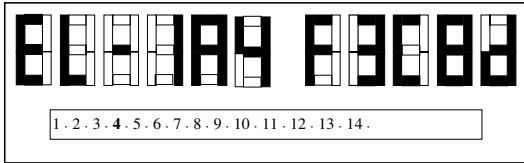
Press PLAY or PAUSE to operate the tray; remove the disc in the tray.

The tray will be closed automatically (if needed) before proceeding to the next tests (by pressing NEXT on the local keyboard).

Read Error Log

The contents of the error log will be displayed on the local display, as follows :

Note: This is an example only; no actual errorcode is intended



CL 96532097\_022.eps  
130999

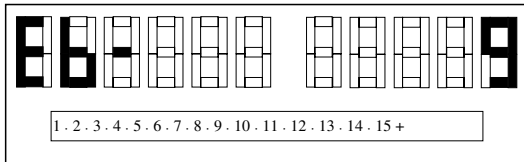
The first two characters on the local display ("EL") indicate that the read-out mode of the error log is activated. After the hyphen 8 hexadecimal digits (one faultcode) are displayed. Below the row of 7-segment displays the highlighted number indicates the number of the faultcode being displayed. (Not for DVDv2B) The highest number indicates the oldest faultcode.

If, in the future, more than 15 faultcodes need to be displayed, the "+" character can be used to indicate the display of a faultcode in the range 16 - 30.

To step through the different fault codes, the PLAY (next) and PAUSE (previous) key on the local keyboard can be used. The display of faultcodes is cyclic. If the error log does not contain any fault codes, all displayed error codes will be "000 00000". To switch off the display of the error log, the NEXT key must be pressed on the local keyboard.

**Read Error Bits**

The error bits are used to indicate that an error occurred once or more times; if that is the case the bit representing the error is set. To read out this field of error bits, the local display is used. Only the numbers of the errors where the bit is set will be displayed on the local display. The layout of the local display is (globally) as follows2:



CL 96532097\_023.eps  
130999

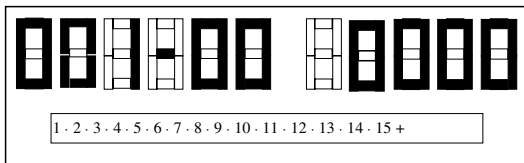
The number of the set bits is displayed in a cyclic manner. Scrolling through the set error bits can be done with the PLAY key for 'next' and PAUSE key for 'previous'. Pressing the PLAY key at the last bit number will display the first bit number again, pressing the PAUSE button at the first bit number will display the last bit number in the list. The representation of bit numbers is decimal.

If no error bits are set, the number on the right side of the display will be "00"

**Module Looptest**

The module looptest is an infinite loop in which a number of nuclei are executed over and over again. The nuclei run are the same as in the dealer test; user interaction is not required.

During this looptest, the display looks as follows3:



CL 96532097\_025.eps  
130999

The leftmost three digits indicate which of the DVD player's modules is faulty; the explanation is in the following table:

Displayed Value	Indication for each module		
	Loader	Mono-board	Display PCB
000	ok	ok	ok
001	ok	ok	faulty
010	ok	faulty	ok
011	ok	faulty	faulty
100	faulty	ok	ok
101	faulty	ok	faulty
110	faulty	faulty	ok
111	faulty	faulty	faulty

CL 06532065\_052.eps  
230500

After the hyphen the (decimal) number indicates the number of times the looptest was performed.

The right side of the display shows an error code DNER (in decimal representation), which is built from a nucleus number (DN) and an error number (ER). This code indicates the last nucleus that returned an error code. For explanation of this DNER code, see document [SDD\_DN].

Pressing NEXT on the local keyboard of the DVD player will exit this loop and show the end result of the player test. End result of the player test is equal to the last display shown above: it shows which module is faulty and which nucleus caused the last error, as well as how many loops were performed.

**Termination**

To terminate the player test, switch off the DVD player.

**5.11 Download Interfaces (not for service)**

The download interface enables the user to download another version of diagnostic software into the RAM of the DVD player. The downloaded software will overrule the software which is placed in the DVD player's ROM; running the original diagnostic software is disabled until the DVD player is switched off and on again.

For download of diagnostic software, the RS232 port may be used.

**5.11.1 Set-up physical interface components**

Hardware required:

- Service PC
- one free COM port on the Service PC
- special cable to connect DVD player to Service PC

The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm in Windows95) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control.

The free COM port must be connected via a special cable to the RS232 port of the DVD player. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

**5.11.2 Activation**

Switch the DVD player on and the following text will appear on the screen of the terminal (emulation program):

```
DVDv2 Diagnostic Software version 1.0
SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK

(M)enu, (C)ommand (S)2B-interface or (D)ownload? [M]:@ D <-
DVD diagnostic software awaiting download...@
CL06532065_035.eps
180500
```

The DVD player is now in a wait-mode, awaiting the download of a file in Motorola S3-format.

Enter the download command (which will be an "upload" from the terminal!) at the terminal:

```
upload <file>
CL96532111_028.eps
071099
```

Progress seen by the diagnostic software is indicated by displaying the character "\*" on screen repeatedly; if the download software encounters an error, the end of the downloaded file will be awaited and instead of the "\*" character, the "+" character will be used to indicate (erroneous) progress.

When download is finished, the following message will come from the DVD player:

```
Download succesful
Press return to start downloaded program...
CL96532111_029.eps
071099
```

When the user then presses a key, the DVD player will report

```
DVD Diagnostic Software version X.X
CL96532111_030.eps
071099
```

and start to run the downloaded software.

Note1 : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.

Note2 : For players without DRAM, the DRAM-tests will be scipped.

### 5.11.3 Usage

The usage of the downloaded software depends on the contents of that software and cannot be described here.

### 5.11.4 Termination (not for service)

To exit the download-interface and remove the downloaded software from the DVD player, switch off the DVD player.

#### External Scripts

A script is a sequence of nucleus calls. Internal scripts (e.g. scripts built into the diagnostic software itself) are in the form of a C-language module. However it cannot be expected from a customer to write C-modules in order to create new scripts.

The scripts that can be made externally are therefor in one of the following two forms:

1. A Procomm or Telex script Procomm or Telex can be used to write diagnostic scripts. The script language of both communication packages contains possibilities for construction of loops and branches in the scripts. Commands then going over the line will be exactly the same as described in the chapter "Command Interface". The diagnostic software (the engine) will receive normal RS232 commands and processes these as defined, sending results of these nuclei back over the RS232 line. In the Terminal the Procomm or Telex script determines which command sequence is followed
2. An Asterix-script Asterix-scripts are C-programs in which commands are sent to the diagnostic software (the engine). The construction of branches and loops is again located in the remote machine, i.e. the Asterix machine. Commands going over the line will be exactly the same as described in the chapter "Command Interface". The diagnostic software (the engine) will receive normal RS232 commands and processes these as defined, sending results of the called nuclei back over the RS232 line. In the Asterix PC the C-program determines which command sequence is followed.

#### Layout of menus and submenus for the Service Terminal

NOTE: a symbol "-->" in the next menu layouts indicates that that specific menu choice will invoke the display of a submenu. This symbol will also be used in the implementation of the menus (i.e. the "-->" will also appear in the user interface).

#### Main Menu

##### MAIN MENU

1. Audio -->
2. Basic Engine -->
3. Display PWB -->
4. Processor & Peripherals -->
5. Karaoke -->
6. Log -->
7. Miscellaneous -->
8. Video -->

#### First Level Submenus

##### AUDIO MENU

1. Deemphasis -->
2. Mute -->
3. PinkNoise -->
4. SineWave -->

##### BASIC ENGINE MENU

1. Disc Motor -->
2. Focus -->
3. Grooves -->
4. Radial -->
5. Reset [44]
6. Sledge -->
7. Tray -->
8. Version [37]

##### DISPLAY PWB MENU

1. Display [30]
2. Keyboard [27]
3. LEDs [29]
4. Remote control [28]
5. Version [28]

##### LOG MENU

1. Read last errors [31]
2. Read error bits [32]



3. Reset [33]

#### PROCESSOR AND PERIPHERALS MENU

1. Clock -->
2. DRAM Write/Read [9]
3. Flash -->
4. I2C -->
5. S2B -->
6. SDRAM Write/Read [16]

#### MISCELLANEOUS MENU

1. NVRam Utils -->
2. PalNtsc Line --> (Not for DVDv2B)
3. 2B Utils -->
4. Statistics Info -->
5. Read Application Version [46]

#### VIDEO MENU

1. Colourbar -->
2. Scart -->

#### KARAOKE MENU

1. Karaoke Mode Off [48a]
2. Karaoke Mode On [48b]
3. KaraokeMicInput [49]
4. KaraokeKey On [50a]
5. KaraokeKey Off [50b]
6. Karaoke Echo On [51a]
7. Karaoke Echo Off [51b]

#### Second level submenus

##### DEEMPHASIS MENU

1. Deemphasis 0 On [18a]
2. Deemphasis 0 Off [18b]
3. Deemphasis 1 On [18c]
4. Deemphasis 1 Off [18d]

##### for DVDv2B:

1. Deemphasis On [18a]
2. Deemphasis Off [18b]
3. Deemp 0 Tristate On [18e]
4. Deemp 0 Tristate Off [18f]
5. Deemp 1 Tristate On [18g]
6. Deemp 1 Tristate Off [18h]

##### MUTE MENU

1. Mute On [19a]
2. Mute Off [19b]

##### PINKNOISE MENU

1. Pinknoise On [20a]
2. Pinknoise Off [20b]

##### SINEWAVE MENU

1. Audio Sine On [21a]
2. Audio Burst On [21b]

##### DISC MOTOR MENU

1. Disc Motor On [39a]
2. Disc Motor Off [39b]

##### FOCUS MENU

1. Focus On [38a]
2. Focus Off [38b]

##### GROOVES MENU

1. Jump Grooves to Inside [42a]
2. Jump Grooves to Middle [42b]
3. Jump Grooves to Outside [42c]

##### RADIAL MENU

1. Radial Control On [40a]
2. Radial Control Off [40b]

##### SLEDGE MENU

1. Sledge Inwards [41a]
2. Sledge Outwards [41b]

##### TRAY MENU

1. Open Tray [43b]
2. Close Tray [43a]

##### LASER MENU

1. Laser Cd On[58a]
2. Laser Cd Off[58b]
3. Laser DVD On[58c]
4. Laser DVD Off[58d]

##### UCLOCK MENU

1.  $\mu$ Clock A\_CLK in CDDA Mode [7a]
2.  $\mu$ Clock A\_CLK in DVD Mode [7b]

##### FLASH MENU

1. Checksum FLASH [6]
2. Flash write access [10]

##### I2C MENU

1. I2C NVRAM Access [11]
2. I2C Display PWB [12]

##### S2B MENU

1. S2B Echo [13]
2. S2B Pass-through [14]

##### NVRAM MENU

1. NVRAM Config [34]
2. NVRAM reset [35]
3. NVRAM Mod [36]
4. NVRAM write/read [15]

##### PAL/NTSC MENU (Not for DVDv2B)

1. PalNtscHi [45a]
2. PalNtscLo [45b]

##### 2B UTILS MENU

1. I2C Scart Check [54]
2. Scart to DVD [55a]
3. Scart Pass through [55b]
4. VideoColSetupI2C [52]
5. VideoColSetupHi [53a]
6. VideoColSetupLo [53b]

##### VIDEO COLOURBAR MENU

1. Colourbar DENC On [23a]
2. Colourbar DENC Off [23b]

##### SCART MENU

1. Scart Low [25a]
2. Scart Medium [25b]
3. Scart High [25c]

##### STATISTICS INFO MENU

1. Total Nr of Times Tray Open [47a]
2. Toat Time Power On [47b]
3. Total Play-time CDDA & VCD [47c]
4. Total Play-time DVD [47d]

**Screen layout with menus**

When menus are used, no specific screen layout can be given: menu information will not be in a special format, except for the layout as mentioned in the previous paragraphs.

A typical menu session can look as follows:

```
-----< top of screen >-----
DVDv2 Diagnostic Software version 1.0
SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK
(M)enu, (C)ommand, (S)2B-interface or (D)ownload? [M]:@
M <--
```

**MAIN MENU**

```
1. Audio -->
2. Basic Engine -->
3. Display PWB -->
4. Processor & Peripherals -->
5. Karaoke -->
6. Log -->
7. Miscellaneous -->
8. Video -->
Select> 4 <--
```

**PROCESSOR AND PERIPHERALS MENU**

```
1. Clock -->
2. DRAM Write/Read [9]
3. Flash -->
4. I2C -->
5. S2B -->
6. SDRAM Write/Read [16]
Select> 6 <--
```

```
-----< bottom of screen >-----
Depending on the height of the screen, the text will start
scrolling off the top of the screen.
```

**Layout of Results diagnostic nuclei on control/service PC**

Results returned from a Diagnostic Nucleus to the control/ service PC will have a maximum length of 300 characters and are terminated by a CR character (included in the string length) The result has the following layout

```
< number >< string > [OK | ER] @< CR >
```

The use of the "@" enables the Asterix system on the Control PC to parse the output string of each nucleus into a database. < number > is a 4-digit decimal number padded with leading zeros if its value is less than 4 digits. The first two digits identify the generating nucleus (or group of nuclei), the latter two digits indicate the error number.

< string > is a text string containing information about the result of the Diagnostic Nucleus.

< number > and < string > are defined in [SDD\_DN] in the output sections of each Nucleus.

Examples:

```
1. 0001 Unknown command ER @
2. 3100 OK @
3. 0901 Data line X is not connected to the DRAM ER @
```

CL96532111\_031.eps  
071099

**5.12 Diagnostic Nuclei**

Each nucleus contains an atomic and independent diagnostic test, testing a functional part of the DVD player hardware on component level. Each Nucleus returns a result message to its caller. Some tests (e.g. generating a colour bar) can only return an "OK" result. Internal communication will be done via a uniform interface between the diagnostic Engine, Scripts and the Diagnostic Nuclei.

The diagnostic Engine can only operate if a certain (minimal) set of hardware is functioning properly. To test this set of hardware, a set of basic diagnostic nuclei is embedded in the DVD player. Each basic diagnostic nucleus will only test that part of the hardware which is required for execution of the diagnostic Engine, e.g. a RAM test will only test that part of RAM that is used by the diagnostic engine. After the Diagnostic Engine is operational it is possible to do a full RAM diagnostic. All basic diagnostic nuclei start with prefix 'Basic'.

In the overview each Diagnostic Nucleus consists of a reference number, a reference name and remarks. Reference number and name are coupled and one of them is enough for unique identification. The reference number can be used to find the description of the Diagnostic Nucleus in paragraph Error! Reference source not found..# where # is the reference number.

**5.12.1 Basic Diagnostic Nuclei**

Ref.	Reference Name	Remark
1	BasicSpAcc	Serial port Access test/initialisation
2a	BasicInterconDram	Data and address bus Interconnection (only for DVDv2A)
2b	BasicInterconSdram	Data and address bus interconnection
3	BasicDramWrR	DRAM Write Read (only for DVDv2A)
4	BasicSdramWrR	SDRAM Write Read
5	BasicSramWrR	SRAM Write Read

**5.12.2 Processor and Peripherals**

Ref.	Reference Name	Remark
6	PapChksFl	Checksum FLASH
7a	PapUclAcIkCdda	uClock A_CLK in CD-DA mode
7b	PapUclAcIkDvd	uClock A_CLK in DVD mode
9	PapDramWrR	DRAM Write Read (only for DVDv2A)
10	PapFlashWrAcc	FLASH Write Access
11	PapI2cNvram	I2C NVRAM access
12	PapI2cDisp	I2C Display PWB
13	PapS2bEcho	S2B Echo
14	PapS2bPass	S2B Pass-through
15	PapNvramWrR	NVRAM Write Read

**5.12.3 Components**

Ref. #	Reference Name	Remark
16	CompSdramWrR	SDRAM Write Read

**5.12.4 Audio**

Ref.	Reference Name	Remark
17	AudioSig	Audio Signature (Optional)
18a	AudioDeemp0On	Audio De-emphasis 0 On
	AudioDeempOn (DVD2B)	Audio De-emphasis On (DVDv2B)
18b	AudioDeemp0Off	Audio De-emphasis 0 Off
	AudioDeempOff (DVD2B)	Audio De-emphasis Off (DVDv2B)
18c	AudioDeemp1On	Audio De-emphasis 1 On (Not for DVDv2B)
18d	AudioDeemp1Off	Audio De-emphasis 1 Off (Not for DVDv2B)
18e	AudioDeemp0TristateOn	Audio De-emphasis 0 in tristate/bidirectional mode (DVDv2B)
18f	AudioDeemp0TristateOff	Audio De-emphasis 0 back in output mode (Off) (DVDv2B)
18g	AudioDeemp1TristateOn	Audio De-emphasis 1 in tristate/bidirectional mode (DVDv2B)
18h	AudioDeemp1TristateOff	Audio De-emphasis 1 back in output mode (Off) (DVDv2B)
19a	AudioMuteOn	Audio Mute On
19b	AudioMuteOff	Audio Mute Off
20a	AudioPinkNoiseOn	Audio Pinknoise On
20b	AudioPinkNoiseOff	Audio Pinknoise Off
21a	AudioSineOn	Audio Sine signal On/Off
21b	AudioSineBurst	Audio Sine signal Burst
56a	AudioDeemp0On	PIO-pins as used in 2A for Deemphasis
56b	AudioDeemp0Off	PIO-pins as used in 2A for Deemphasis
56c	AudioDeemp1On	PIO-pins as used in 2A for Deemphasis
56d	AudioDeemp1Off	PIO-pins as used in 2A for Deemphasis

**5.12.5 Video**

Ref.	Reference Name	Remark
23a	VideoColDencOn	Colourbar DENC On
23b	VideoColDencOff	Colourbar DENC Off
25a	VideoScartLo	Scart Low
25b	VideoScartMi	Scart Medium
25c	VideoScartHi	Scart High
52	VideoColSetupCom	Colour Setup Communication
53a	VideoColSetupHi	Colour Setup High
53b	VideoColSetupLo	Colour Setup Low
54	VideoScartSwComm	Scart Switch communication
55a	VideoScartSwDvd	Scart Switch Dvd
55b	VideoScartSwPass	Scart Switch Pass-through

Ref.	Reference Name	Remark
57a	VideoScartPinLo	PIO-pins as used in 2A for Scart-switching
57b	VideoScartPinMi	PIO-pins as used in 2A for Scart-switching
57c	VideoScartPinHi	PIO-pins as used in 2A for Scart-switching

#### 5.12.6 DisplayPWB (slave processor)

Ref.	Reference Name	Remark
26	DispVer	Version number
27	DispKeyb	Keyboard
28	DispRc	Remote Control
29	DispLed	LEDs
30	DispDisplay	Display

#### 5.12.7 Log (error logging in NVRAM)

Ref.	Reference Name	Remark
31	LogReadErr	Read last Errors
32	LogReadBits	Read errors Bits
33	LogReset	Reset

#### 5.12.8 Miscellaneous

Ref.	Reference Name	Remark
34	MiscReadConfig	Read Configuration area from NVRAM
35	MiscNvramReset	NVRAM Reset
36	MiscNvramMod	Modify NVRAM contents
45a	MiscPalNtscHi	Check if PAL/NTSC line is high (Not for DVDv2B)
45b	MiscPalNtscLo	Check if PAL/NTSC line is low (Not for DVDv2B)
46	MiscAppVer	Read version of application software
47a	MiscTrayOpenNr	Read the number of times the tray opened
47b	MiscPowerOnTime	Read the total time the player's power has been on
47c	MiscPlayTimeCddaVcd	Read the Playtime of CDDA and VCD discs
47d	MiscPlayTimeDvd	Read the Playtime of DVD discs

#### 5.12.9 Basic Engine

Ref.	Reference Name	Remark
37	BeVer	Version number
38a	BeFocusOn	Focus On
38b	BeFocusOff	Focus Off
39a	BeDiscmotorOn	Discmotor On
39b	BeDiscmotorOff	Discmotor Off

Ref.	Reference Name	Remark
40a	BeRadialOn	Radial control On
40b	BeRadialOff	Radial control Off
41a	BeSledgeIn	Sledge Inwards
41b	BeSledgeOut	Sledge Outwards
42a	BeGroovesIn	jump Grooves to Inside
42b	BeGroovesMid	jump Grooves to Middle
42c	BeGroovesOut	jump Grooves to Outside
43a	BeTrayIn	Tray In
43b	BeTrayOut	Tray Out
44	BeReset	Reset Basic Engine
58a	LaserCdOn	CD Laser on
58b	LaserCdOff	CD Laser off
58c	LaserDvdOn	DVD Laser on
58d	LaserDvdOff	DVD Laser off

#### 5.12.10 Karaoke

Ref.	Reference Name	Remark
48a	KaraokeModeOff	Switch Karaoke mode off
48b	KaraokeModeOn	Switch Karaoke mode on
49	KaraokeMicInput	Check path from the microphone input to audio output
50a	KaraokeKeyOn	Set Karaoke Key to the maximum level (1200 cent)
50b	KaraokeKeyOff	Set Karaoke Key to flat octave (0 cent)
51a	KaraokeEchoOn	Set Echo Control function on
51b	KaraokeEchoOff	Set Echo Control function off

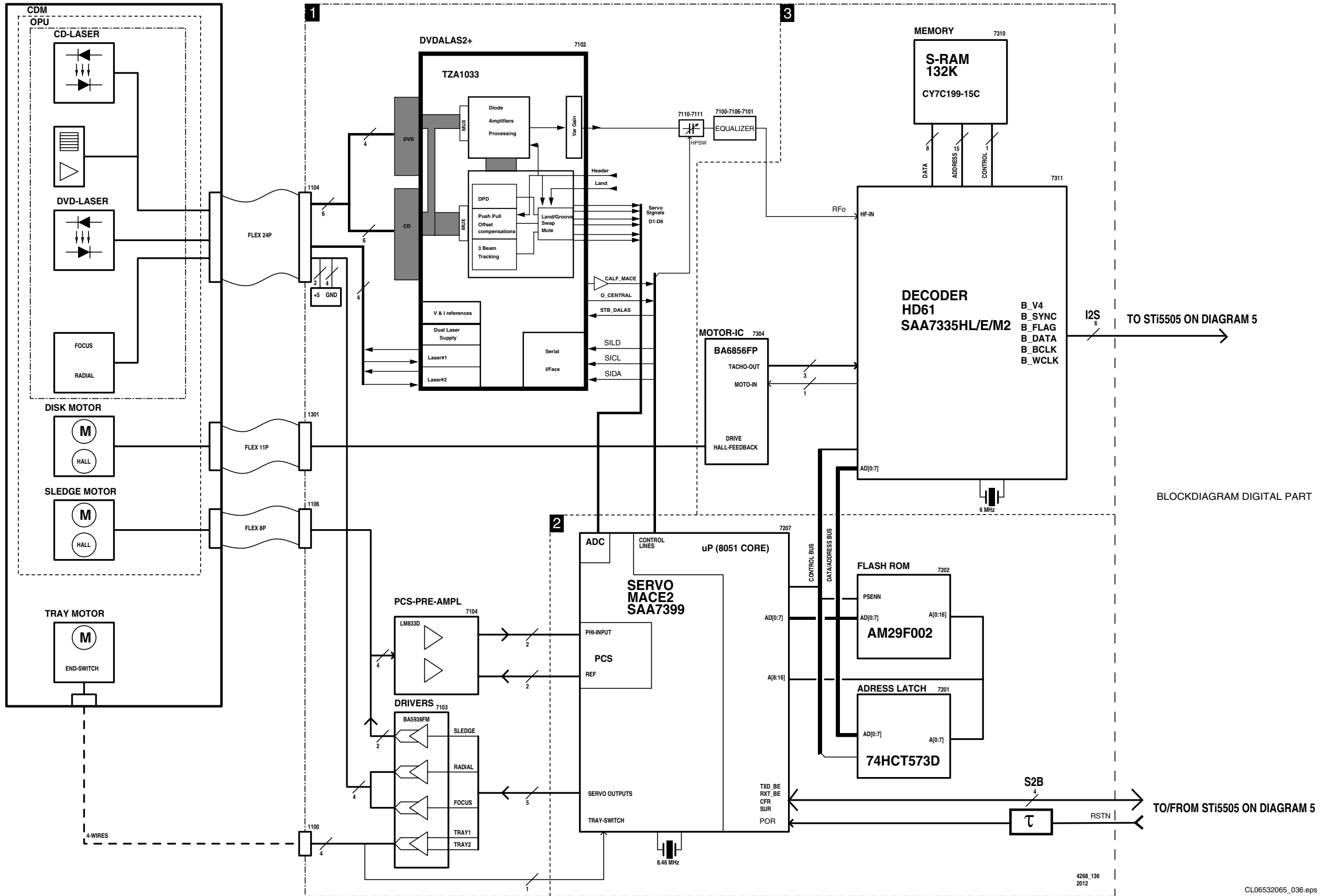
Note: A new Compar version for repair of the MONO boards will be developed.

# 6. Block diagrams

## Servo

### LOADER

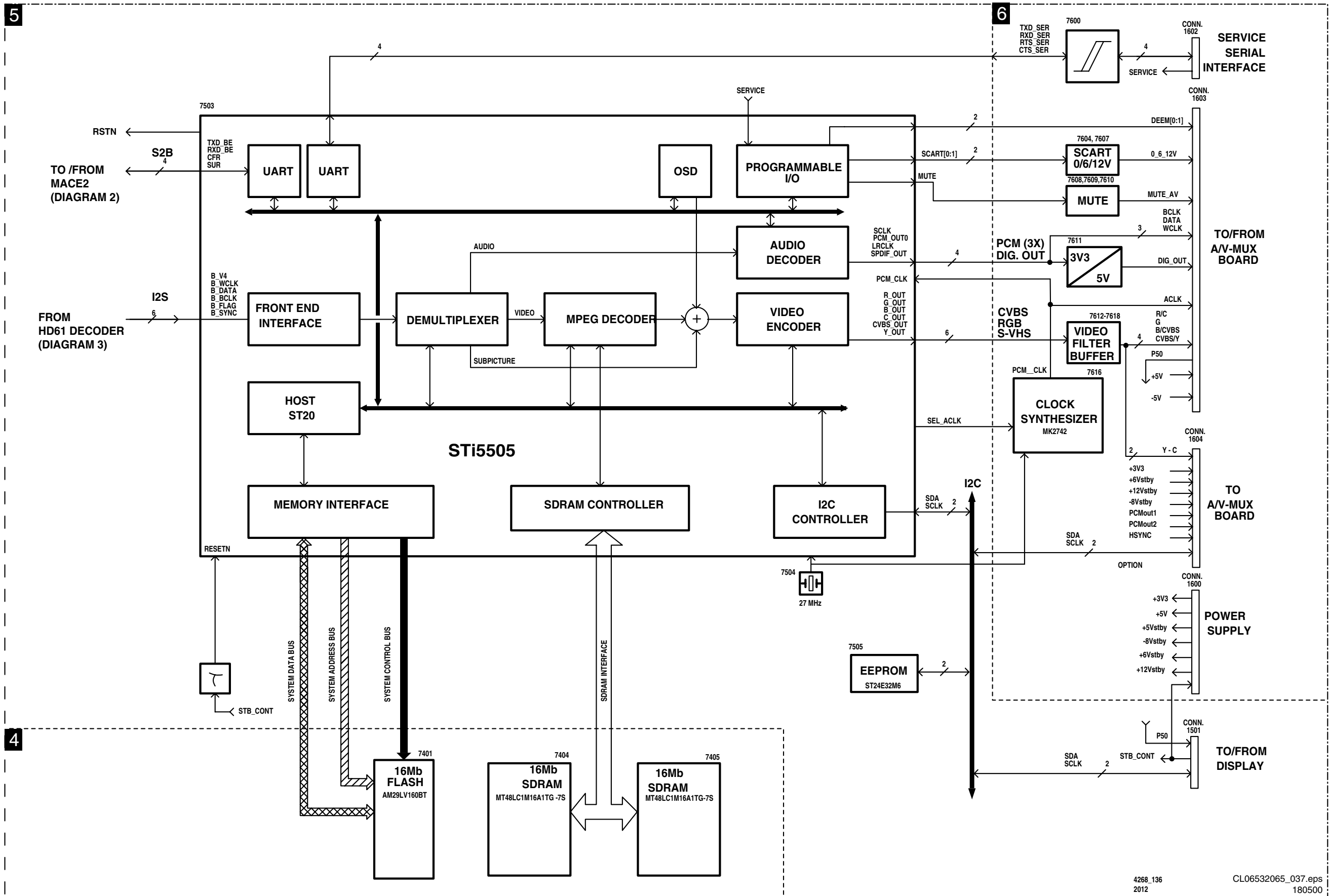
### ASD1 BOARD SERVO PART



4268\_136  
2012

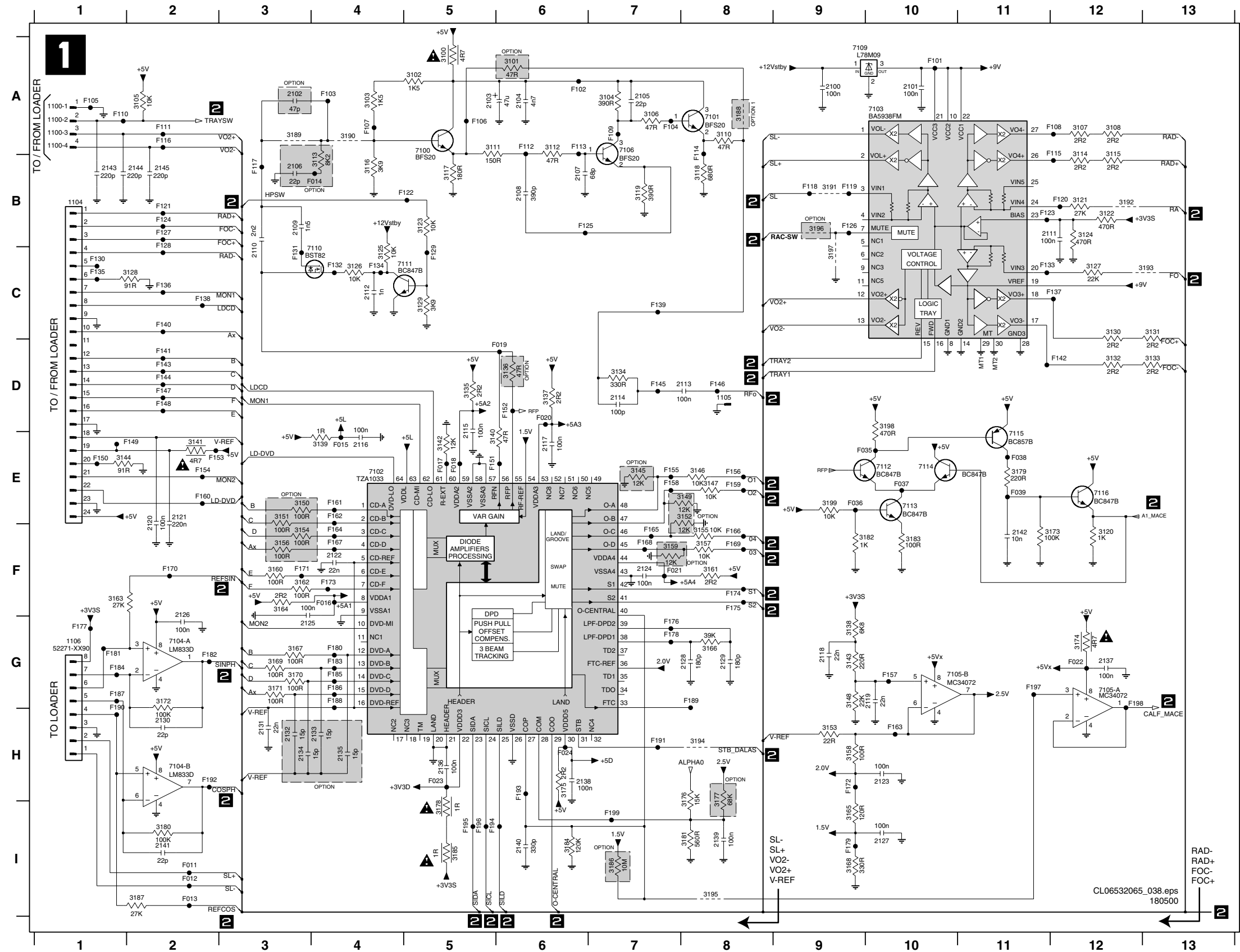
Didital

ASD1 BOARD DIGITAL PART



# 7. Electrical diagrams and PWB's

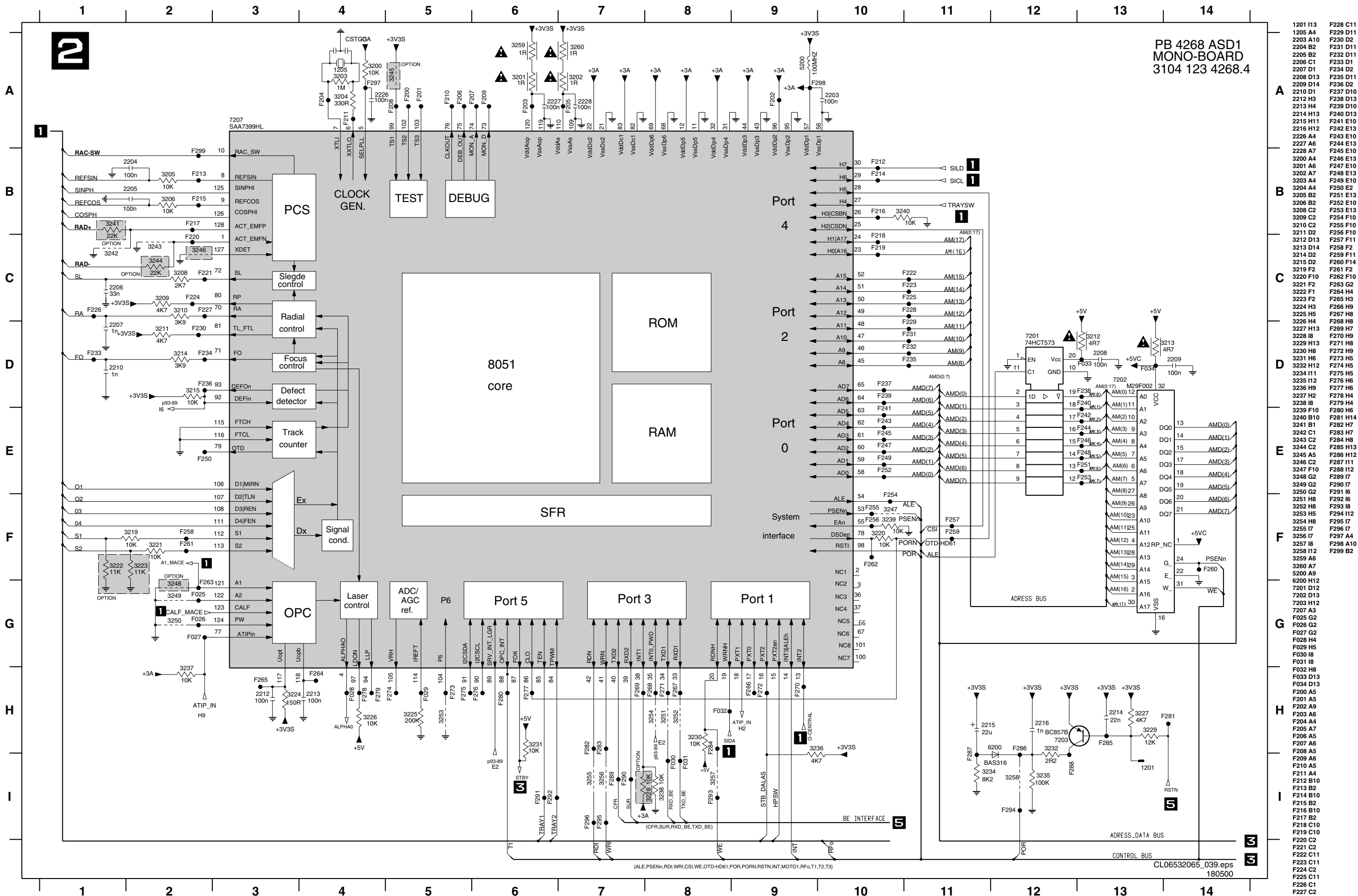
## SERVO DALAS



1100-1 A1	3165 I9	F147 D2
1100-2 A1	3165 G8	F148 D2
1100-3 A1	3167 G3	F149 E2
1100-4 A1	3168 I9	F150 E1
1104 B1	3169 G3	F151 E5
1105 D8	3170 G3	F152 D6
1106 G1	3171 G3	F153 E2
2100 A9	3172 G2	F154 E2
2101 A10	3173 F12	F155 E7
2102 A3	3174 G12	F156 E8
2103 A5	3175 H6	F157 G10
2104 A6	3176 H8	F158 E7
2105 A7	3177 H8	F159 E8
2106 B3	3178 I5	F160 E2
2107 B6	3179 E11	F161 E4
2108 B6	3180 I2	F162 E4
2109 B3	3181 I8	F163 H10
2110 B3	3182 F10	F164 F4
2111 B11	3183 F10	F165 F7
2112 C4	3184 I6	F166 F8
2113 D8	3185 I5	F167 F4
2114 D7	3186 I7	F168 F7
2115 D5	3187 I2	F169 F8
2116 E4	3188 A8	F170 F2
2117 E6	3189 A3	F171 F3
2118 G9	3190 A4	F172 H9
2119 G10	3191 B9	F173 F4
2120 E2	3192 B12	F174 F8
2121 E2	3193 C13	F175 F7
2122 F4	3194 H8	F176 G7
2123 H10	3195 I8	F177 G1
2124 F7	3196 B9	F178 G7
2125 G3	3197 C9	F179 I9
2126 G2	3198 D10	F180 G4
2127 I10	3199 E9	F181 G1
2128 G8	7100 A5	F182 G2
2129 G8	7101 A8	F183 G4
2130 H2	7102 E4	F184 G1
2131 H3	7103 A10	F185 G4
2132 H3	7104-A G2	F186 G4
2133 H4	7104-B H2	F187 G1
2134 H3	7105-A G12	F188 G4
2135 H4	7105-B G10	F189 G8
2136 H5	7106 A7	F190 H1
2137 G12	7109 A9	F191 H7
2138 H6	7110 C4	F192 H2
2139 I8	7111 C5	F193 H6
2140 I6	7112 E10	F194 I5
2141 I2	7113 E10	F195 I5
2142 F11	7114 E10	F196 I5
2143 B1	7115 D11	F197 G11
2144 B2	7116 E12	F198 G12
2145 B2	F011 I2	F199 I7
3100 A5	F012 I2	
3101 A6	F013 I2	
3102 A5	F014 B4	
3103 A4	F015 E4	
3104 A7	F016 F4	
3105 A2	F017 E5	
3106 A7	F018 E5	
3107 A12	F019 D5	
3108 A12	F020 D6	
3110 A8	F021 F7	
3111 A5	F022 G12	
3112 A6	F023 H5	
3113 B4	F024 H6	
3114 B12	F025 E9	
3115 B12	F026 E9	
3116 B4	F027 E10	
3117 B5	F028 E11	
3118 B8	F029 E11	
3119 B7	F030 A10	
3120 F12	F031 A5	
3121 B12	F032 A4	
3122 B12	F033 A7	
3123 B5	F034 A1	
3124 B12	F035 A5	
3125 C4	F036 A4	
3126 C4	F037 A12	
3127 C12	F038 A7	
3128 C2	F039 A1	
3129 C5	F040 A1	
3130 C12	F041 A6	
3131 C13	F042 A6	
3132 D12	F043 A8	
3133 D13	F044 B12	
3134 D7	F045 A2	
3135 D5	F046 B3	
3136 D6	F047 B9	
3137 D6	F048 B9	
3138 G9	F049 B12	
3139 E4	F050 B2	
3140 E5	F051 B5	
3141 E2	F052 B11	
3142 E5	F053 B2	
3143 G9	F054 B6	
3144 E1	F055 B9	
3145 E7	F056 B2	
3146 E8	F057 B2	
3147 E8	F058 C5	
3148 G9	F059 C1	
3149 E9	F060 C1	
3150 E3	F061 C4	
3151 E3	F062 C11	
3152 E8	F063 C4	
3153 H9	F064 C1	
3154 F3	F065 C1	
3155 F3	F066 F8	
3156 F3	F067 C2	
3157 F8	F068 C7	
3158 H9	F069 C2	
3159 F7	F070 D2	
3160 F3	F071 D2	
3161 F8	F072 D2	
3162 F3	F073 D2	
3163 F1	F074 D7	
3164 F3	F075 D8	

PB 4268 ASD1  
 MONO-BOARD  
 3104 123 4268.4

SERVO MACE



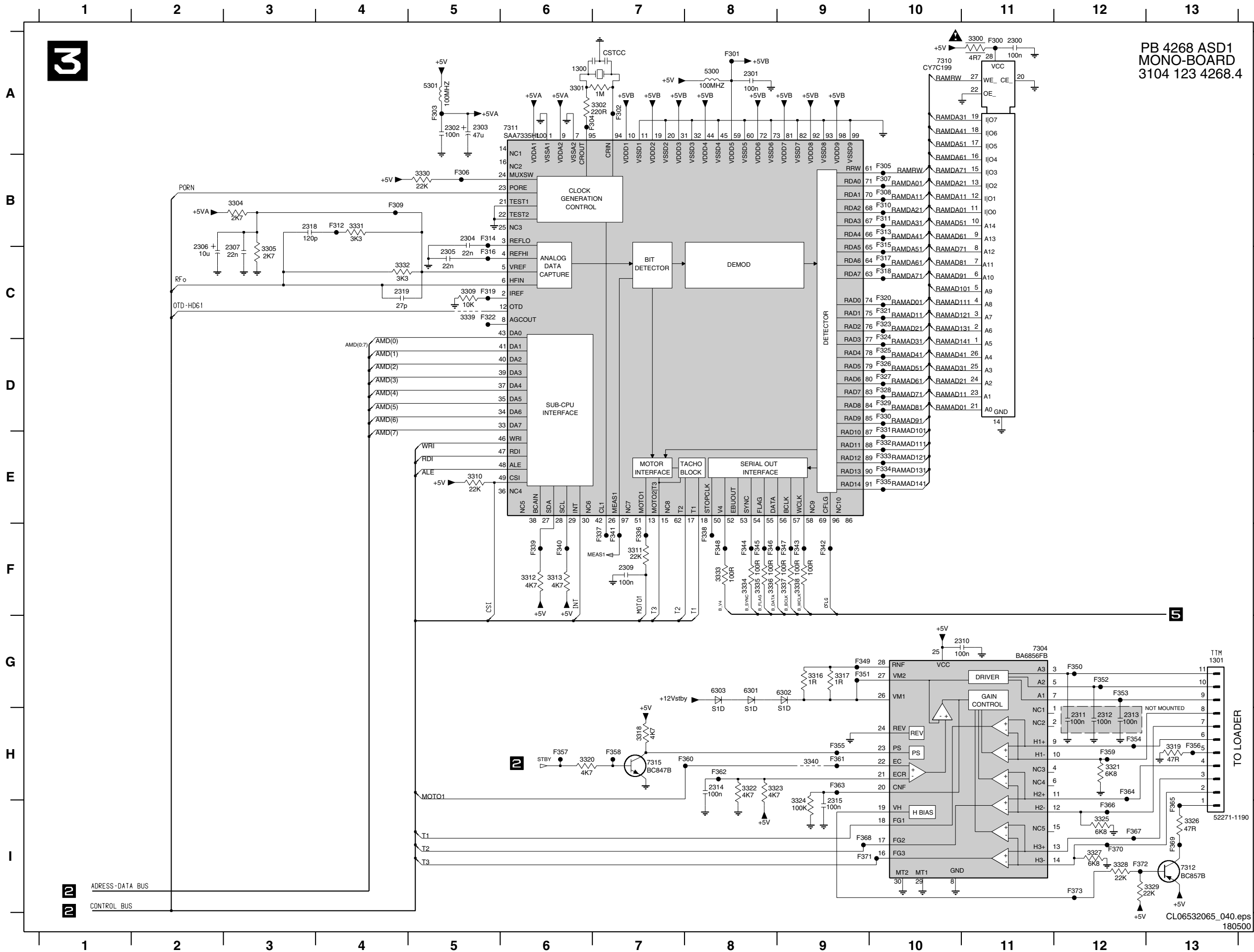
PB 4268 ASD1  
MONO-BOARD  
3104 123 4268.4

- 1201 I13
- 1205 A4
- 1206 A10
- 1206 B2
- 1206 B2
- 1206 C1
- 1207 D1
- 1208 D13
- 1209 D14
- 1210 D1
- 1212 H3
- 1213 H4
- 1214 H13
- 1215 H11
- 1216 H12
- 1226 A4
- 1227 A6
- 1228 A7
- 1200 A4
- 1201 A6
- 1202 A7
- 1203 A4
- 1204 A4
- 1205 B2
- 1206 B2
- 1208 C2
- 1209 C2
- 1210 C2
- 1211 D2
- 1212 D13
- 1213 D14
- 1214 D2
- 1215 D2
- 1219 F2
- 1220 F10
- 1221 F2
- 1222 F1
- 1223 F2
- 1224 H3
- 1225 H5
- 1226 H4
- 1227 H13
- 1228 H8
- 1229 H13
- 1230 H8
- 1231 H6
- 1232 H12
- 1234 I11
- 1235 I12
- 1236 H9
- 1237 H2
- 1238 I8
- 1239 F10
- 1240 B10
- 1241 B1
- 1242 C1
- 1243 C2
- 1244 C2
- 1245 A5
- 1246 C2
- 1247 F10
- 1248 G2
- 1249 G2
- 1250 G2
- 1251 H8
- 1252 H8
- 1253 H5
- 1254 H8
- 1255 I7
- 1256 I7
- 1257 I8
- 1258 I12
- 1259 A6
- 1260 A7
- 1260 A9
- 1260 H12
- 1261 D12
- 1262 D13
- 1263 H12
- 1267 A3
- 1268 G2
- 1269 I7
- 1270 G2
- 1272 H4
- 1273 H5
- 1274 H5
- 1275 H5
- 1276 H6
- 1277 H6
- 1278 H4
- 1279 H4
- 1280 H6
- 1281 H14
- 1282 H7
- 1284 H8
- 1285 H13
- 1286 H12
- 1287 I11
- 1288 I12
- 1289 I7
- 1290 I7
- 1291 I6
- 1292 I6
- 1293 I8
- 1294 I12
- 1295 I7
- 1296 I7
- 1297 A4
- 1298 A10
- 1299 B2
- F228 C11
- F229 D11
- F230 D2
- F231 D11
- F232 D11
- F233 D1
- F234 D2
- F235 D11
- F236 D2
- F237 D10
- F238 D13
- F239 D10
- F240 D13
- F241 E10
- F242 E13
- F243 E10
- F244 E13
- F245 E10
- F246 E13
- F247 E10
- F248 E13
- F249 E10
- F250 E2
- F251 E13
- F252 E10
- F253 E13
- F254 F10
- F255 F10
- F256 F10
- F257 F11
- F258 F2
- F259 F11
- F260 F14
- F261 F2
- F262 F10
- F263 G2
- F264 H4
- F265 H3
- F266 H9
- F267 H8
- F268 H8
- F269 H7
- F270 H9
- F271 H8
- F272 H9
- F273 H5
- F274 H5
- F275 H5
- F276 H6
- F277 H6
- F278 H4
- F279 H4
- F280 H6
- F281 H14
- F282 H7
- F284 H8
- F285 H13
- F286 H12
- F287 I11
- F288 I12
- F289 I7
- F290 I7
- F291 I6
- F292 I6
- F293 I8
- F294 I12
- F295 I7
- F296 I7
- F297 A4
- F298 A10
- F299 B2

(ALE,PSEN,RD,WR,CS,WE,OTD-HD61,POR,PORN,RSTN,INT,MOT01,RF0,T1,T2,T3)



Decoder



PB 4268 ASD1  
MONO-BOARD  
3104 123 4268.4

- 1300 A6 F353 G12
- 1301 G13 F354 H12
- 2300 A11 F355 H9
- 2301 A8 F356 H13
- 2302 A5 F357 H6
- 2303 A5 F358 H7
- 2304 B5 F359 H12
- 2305 C5 F360 H8
- 2306 C2 F361 H9
- 2307 C3 F362 H8
- 2309 F7 F363 H9
- 2310 G11 F364 H12
- 2311 H12 F365 H13
- 2312 H12 F366 H12
- 2313 H12 F367 H12
- 2314 H8 F368 I9
- 2315 I9 F369 H13
- 2318 B3 F370 H12
- 2319 C4 F371 I9
- 3300 A11 F372 H12
- 3301 A6 F373 I12
- 3302 A7
- 3303 B3
- 3305 C3
- 3309 C5
- 3310 E5
- 3311 F7
- 3312 F6
- 3313 F6
- 3316 G9
- 3317 G9
- 3318 H7
- 3319 H13
- 3320 H6
- 3321 H12
- 3322 H8
- 3323 H8
- 3324 I9
- 3325 I12
- 3326 I13
- 3327 I12
- 3328 I12
- 3329 I13
- 3330 B5
- 3331 B4
- 3332 C4
- 3333 F8
- 3334 F8
- 3335 F8
- 3336 F8
- 3337 F9
- 3338 F9
- 3339 C5
- 3340 H9
- 5300 A8
- 5301 A5
- 6301 G8
- 6302 G9
- 6303 G8
- 7300 G11
- 7310 A10
- 7311 A6
- 7312 I13
- 7315 H7
- F300 A11
- F301 A8
- F302 A7
- F303 A5
- F304 A6
- F305 B10
- F306 B5
- F307 B10
- F308 B10
- F309 B4
- F310 B10
- F311 B10
- F312 B4
- F313 B10
- F314 B5
- F315 C10
- F316 C5
- F317 C10
- F318 C10
- F319 C5
- F320 C10
- F321 C10
- F322 C5
- F323 C10
- F324 D10
- F325 D10
- F326 D10
- F327 D10
- F328 D10
- F329 D10
- F330 D10
- F331 E10
- F332 E10
- F333 E10
- F334 E10
- F335 E10
- F336 F7
- F337 F7
- F338 F8
- F339 F6
- F340 F6
- F341 F7
- F342 F9
- F343 F9
- F344 F8
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- F348 F8
- F349 G9
- F350 G12
- F351 G9
- F352 G12

TO LOADER

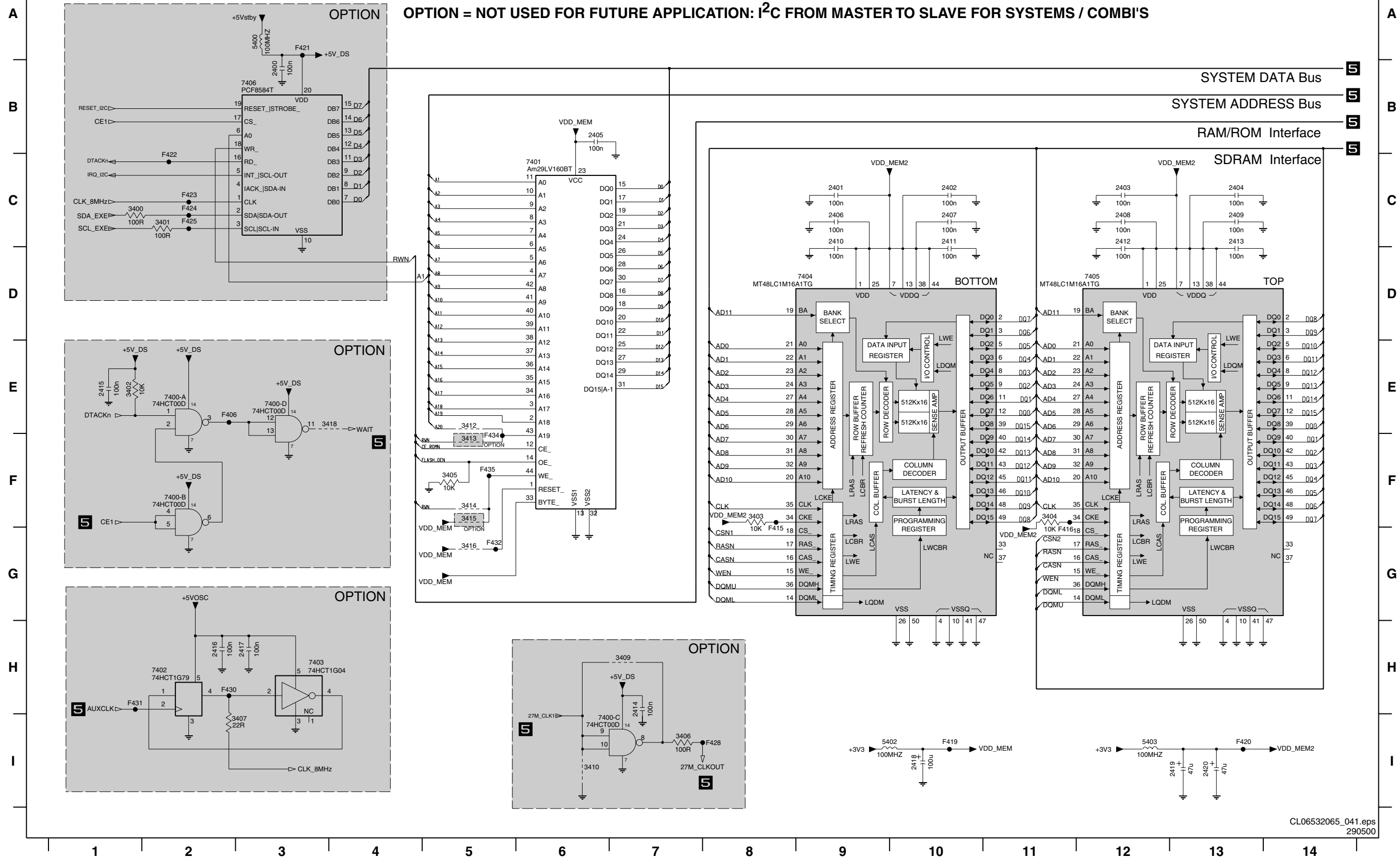
Memory

4

MEMORY PART

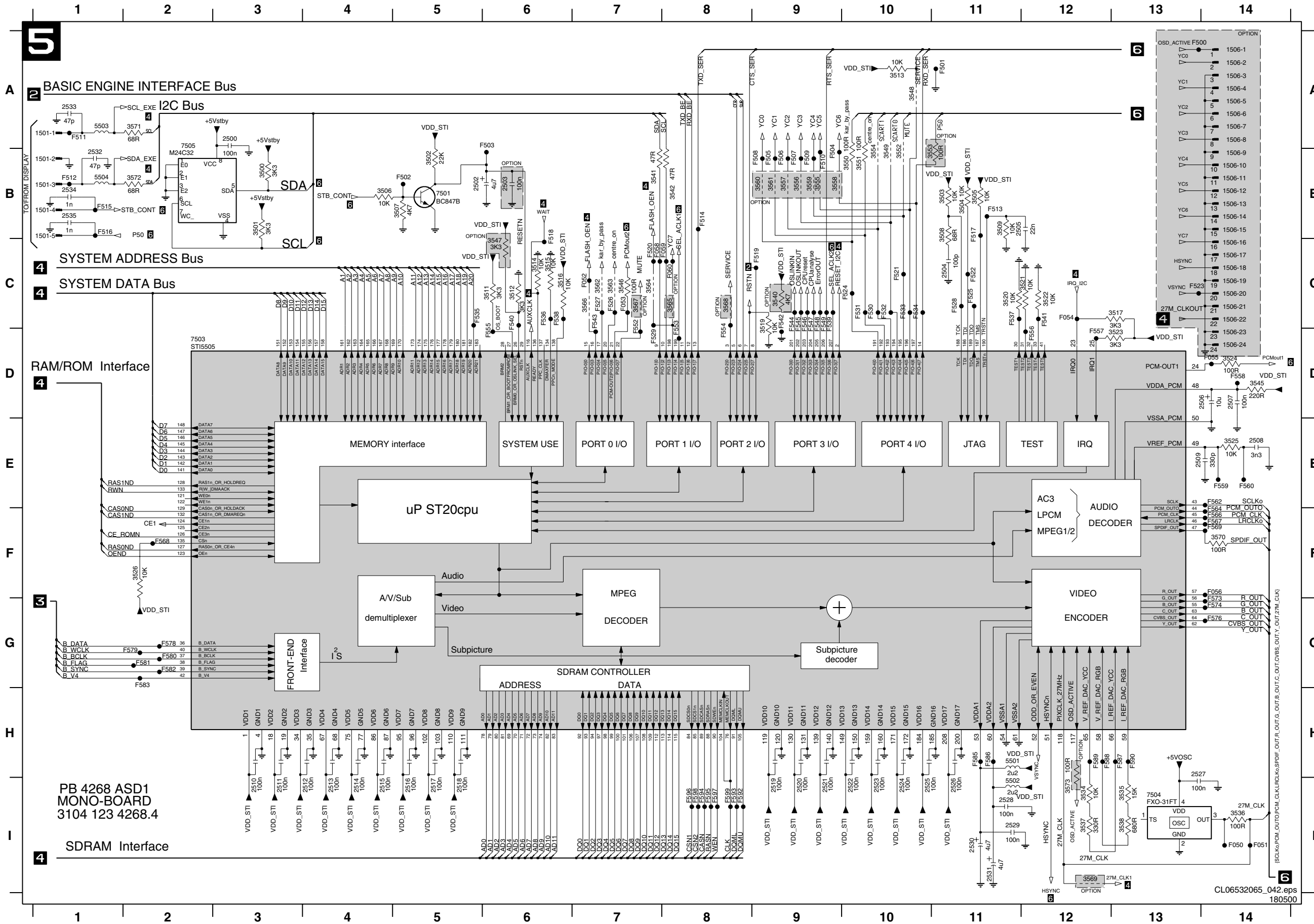
PB 4268 ASD1  
MONO-BOARD  
3104 123 4268.4

OPTION = NOT USED FOR FUTURE APPLICATION: I<sup>2</sup>C FROM MASTER TO SLAVE FOR SYSTEMS / COMBI'S



- 2400 B3
- 2401 C9
- 2402 C10
- 2403 C12
- 2404 C13
- 2405 B6
- 2406 C9
- 2407 C10
- 2408 C12
- 2409 C13
- 2410 C9
- 2411 C10
- 2412 C12
- 2413 C13
- 2414 H7
- 2415 E1
- 2416 H2
- 2417 H3
- 2418 I10
- 2419 I13
- 2420 I13
- 3400 C1
- 3401 C2
- 3402 E1
- 3403 F8
- 3404 F11
- 3405 F5
- 3406 I7
- 3407 I3
- 3408 H7
- 3409 H7
- 3410 I6
- 3412 E5
- 3413 F5
- 3414 F5
- 3415 F5
- 3416 G5
- 3418 E4
- 5400 A3
- 5402 I9
- 5403 I12
- 7400-A E2
- 7400-B F2
- 7400-C I6
- 7400-D E3
- 7401 C6
- 7402 H2
- 7403 H3
- 7404 D9
- 7405 D12
- 7406 B3
- F402 E2
- F415 G8
- F416 G11
- F419 I10
- F420 I13
- F421 A3
- F422 C2
- F423 C2
- F424 C2
- F425 C2
- F428 I8
- F430 H2
- F431 H1
- F432 G5
- F434 F5
- F435 F5

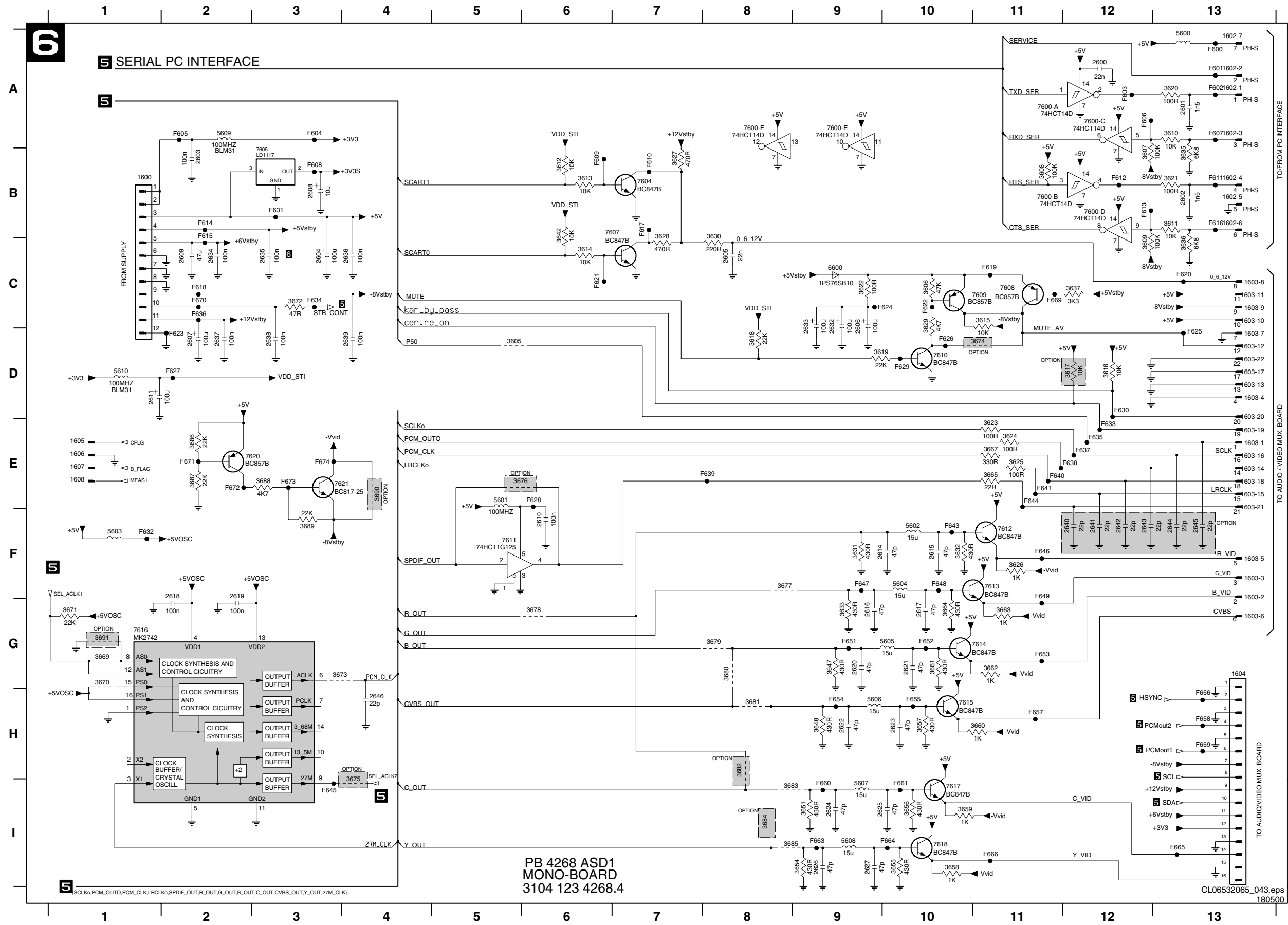
STI 5505



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1501-5 B1	3569 I12
1506-1 A14	3570 F14
1506-10 B14	3571 A2
1506-11 B14	3572 B2
1506-12 B14	3573 I12
1506-13 B14	5501 H11
1506-14 B14	5502 H11
1506-15 B14	5503 A1
1506-16 C14	5504 B1
1506-17 C14	7501 B5
1506-18 C14	7503 D2
1506-19 C14	7504 I13
1506-2 A14	7505 A2
1506-20 C14	F500 A14
1506-21 C14	F501 H14
1506-22 C14	F502 C7
1506-23 D14	F503 C7
1506-24 D14	F504 C12
1506-3 A14	F505 D14
1506-4 A14	F506 F14
1506-5 A14	F507 C8
1506-6 A14	F508 C8
1506-7 A14	F509 A13
1506-8 A14	F510 B9
1506-9 B14	F511 A1
2500 A3	F512 B1
2502 B5	F513 B11
2502 B6	F514 B8
2503 C11	F515 B1
2505 B11	F516 B1
2506 D14	F517 B11
2507 D14	F518 B6
2508 E14	F519 C9
2509 E13	F520 C7
2510 A3	F521 C10
2511 I3	F522 C11
2512 A4	F523 C13
2513 I4	F524 C10
2514 I4	F525 C11
2515 A4	F526 C7
2516 I5	F527 C7
2517 I5	F528 C11
2518 I5	F529 D7
2519 I9	F530 C10
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2522 I10	F533 C10
2523 I10	F534 C10
2524 I10	F535 C5
2525 I10	F536 C6
2526 I11	F537 C11
2527 H13	F538 C6
2528 H11	F539 C6
2529 H11	F540 C6
2530 H11	F541 C12
2531 H11	F542 C9
2532 B1	F543 C7
2533 A1	F544 C9
2534 B1	F545 C9
2535 B1	F546 C9
3500 B3	F547 C8
3501 B3	F548 C9
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3503 B11	F550 C7
3504 B11	F551 C7
3505 B11	F552 C7
3506 B4	F553 C8
3507 B5	F554 D8
3508 B11	F555 D6
3509 B11	F556 D12
3510 C9	F557 D12
3520 C11	F558 D14
3521 C12	F559 E14
3522 C12	F560 E14
3523 D13	F561 E14
3524 D14	F562 E14
3525 E14	F563 F14
3526 F2	F564 F14
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3535 I13	F566 F2
3536 I14	F567 F14
3537 I12	F568 F14
3538 I13	F569 G14
3540 C9	F570 G14
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3542 B8	F572 G2
3543 D14	F573 G2
3544 C7	F574 G14
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3549 B10	F577 G2
3550 B10	F578 G2
3551 B10	F579 G2
3552 B10	F580 G2
3553 B11	F581 G2
3554 B10	F582 G2
3555 B9	F583 G2
3556 B9	F584 H11
3557 B9	F585 H11
3558 B9	F586 H11
3559 B9	F587 H13
3560 B9	F588 H12
3561 B9	F589 H12
3562 C7	F590 H13
3563 C7	F591 I8
3564 C7	F592 I8
	F593 I8
	F594 I8
	F595 I8
	F596 I8
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	F598 I8
	F599 I8

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MONO-BOARD  
3104 123 4268.4

Service interface and Back-end



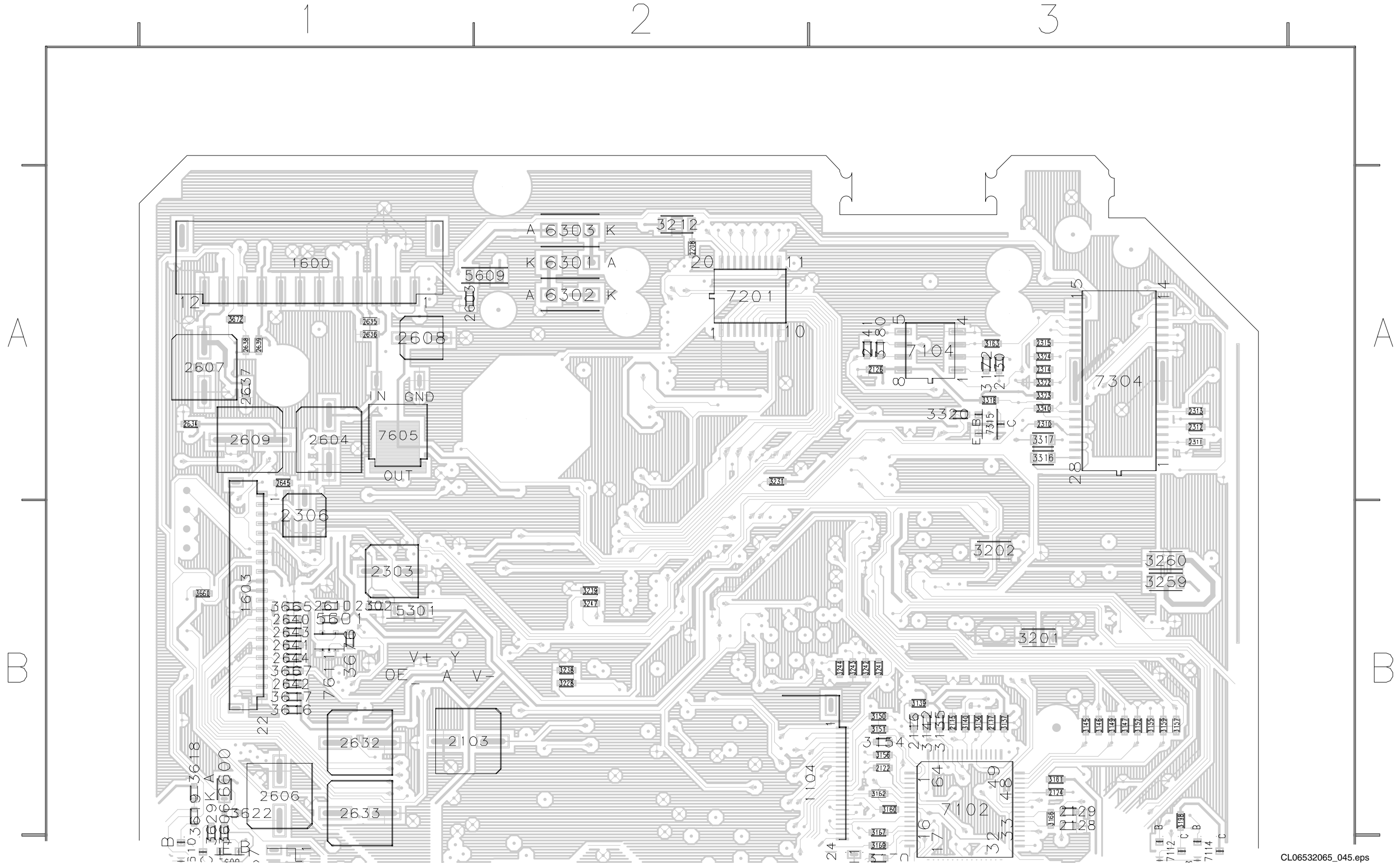
PB 4268 ASD1  
MONO-BOARD  
3104 123 4268.4

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1602-3 A13	3661 G10	F655 H10
1602-4 B13	3662 G11	F656 H13
1602-5 B13	3663 G11	F657 H11
1602-6 B13	3664 G10	F658 H13
1602-7 A13	3665 E11	F659 H13
1603-1 E13	3667 E11	F660 I9
1603-10 C13	3669 G1	F661 I10
1603-11 C13	3670 G1	F663 I9
1603-12 D13	3671 G1	F664 H10
1603-13 D13	3672 C3	F665 H13
1603-14 E13	3673 G3	F666 H11
1603-15 E13	3674 D11	F669 C11
1603-16 E13	3675 I4	F670 C2
1603-17 D13	3676 E5	F671 E2
1603-18 E13	3677 F8	F672 E2
1603-19 E13	3678 G6	F673 E3
1603-2 G13	3679 G8	F674 E3
1603-20 F13	3680 H8	
1603-21 F13	3681 H8	
1603-22 D13	3682 H8	
1603-3 F13	3683 I8	
1603-4 D13	3684 I8	
1603-5 F13	3685 I8	
1603-6 G13	3686 E2	
1603-7 D13	3687 E2	
1603-8 C13	3688 E3	
1603-9 C13	3689 F3	
1604 G13	3690 E4	
1605 E1	3691 G1	
1606 E1	5600 A13	
1607 E1	5601 E5	
1608 E1	5602 F10	
2600 A12	5603 F10	
-80V1 A13	5604 F10	
5605 B13	5605 G10	
2603 B2	5606 H9	
2604 C3	5607 I9	
2605 C8	5608 I9	
2606 C9	5609 A2	
2607 D2	5610 D1	
2608 B3	6000 C9	
2609 C2	7600-A A11	
1610 F6	7600-B B11	
2611 D1	7600-C A12	
2614 F9	7600-D B12	
2615 F10	7600-E A9	
2616 G9	7600-F A8	
2617 G10	7604 B7	
2618 F2	7605 B3	
2619 F2	7607 B6	
2620 G9	7608 C11	
2621 G10	7609 C10	
2622 H9	7610 D10	
2623 H10	7611 F5	
2624 I9	7612 F11	
2625 I9	7613 F11	
2626 I9	7614 G10	
2627 I9	7615 H10	
2632 C9	7616 G1	
2633 C9	7617 H10	
2634 C10	7618 I10	
2635 C3	7620 E2	
2636 C4	7621 E3	
2637 D2	F600 A13	
2638 D3	F601 A13	
2639 D4	F602 A13	
2640 F12	F603 A12	
2641 F12	F604 A3	
2642 F12	F605 A2	
2643 F12	F606 A12	
2644 F13	F607 A13	
2645 F13	F608 B3	
2646 H4	F609 B6	
3605 D5	F610 B7	
3606 C10	F611 B13	
3607 B12	F612 B12	
3608 B11	F613 B12	
3609 C12	F614 B2	
3610 A13	F615 B2	
3611 B13	F616 B13	
3612 B6	F617 B7	
3613 B6	F618 C2	
3614 C6	F619 C11	
3615 C11	F620 C13	
3616 D12	F621 C6	
3617 D12	F622 C10	
3618 D8	F623 D2	
3619 D9	F624 C10	
3620 A13	F625 D13	
3621 B13	F626 D10	
3622 C9	F627 D2	
3623 E11	F628 E6	
3624 E11	F629 D10	
3625 E11	F630 D12	
3626 F11	F631 B3	
3627 B7	F632 F1	
3628 C7	F633 E2	
3629 C10	F634 C3	
3630 C8	F635 E12	
3631 F9	F636 C2	
3632 F10	F637 E12	
3633 G9	F638 E12	
3635 B13	F639 E8	
3636 C13	F640 E11	
3637 C12	F641 E11	
3642 B6	F643 F10	
3647 G9	F644 E11	
3648 H9	F645 I3	
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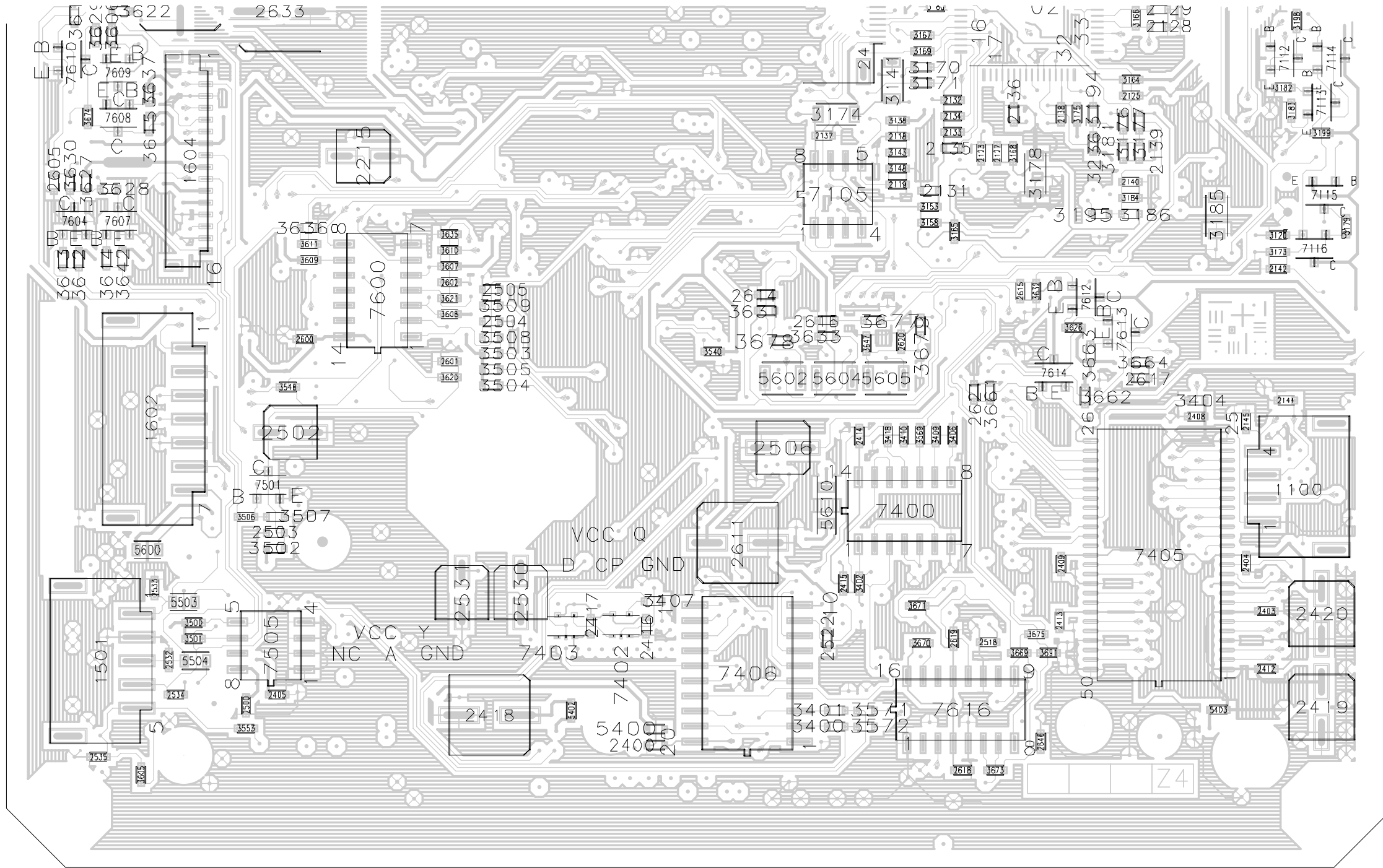
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180500



Detailed Top view 1



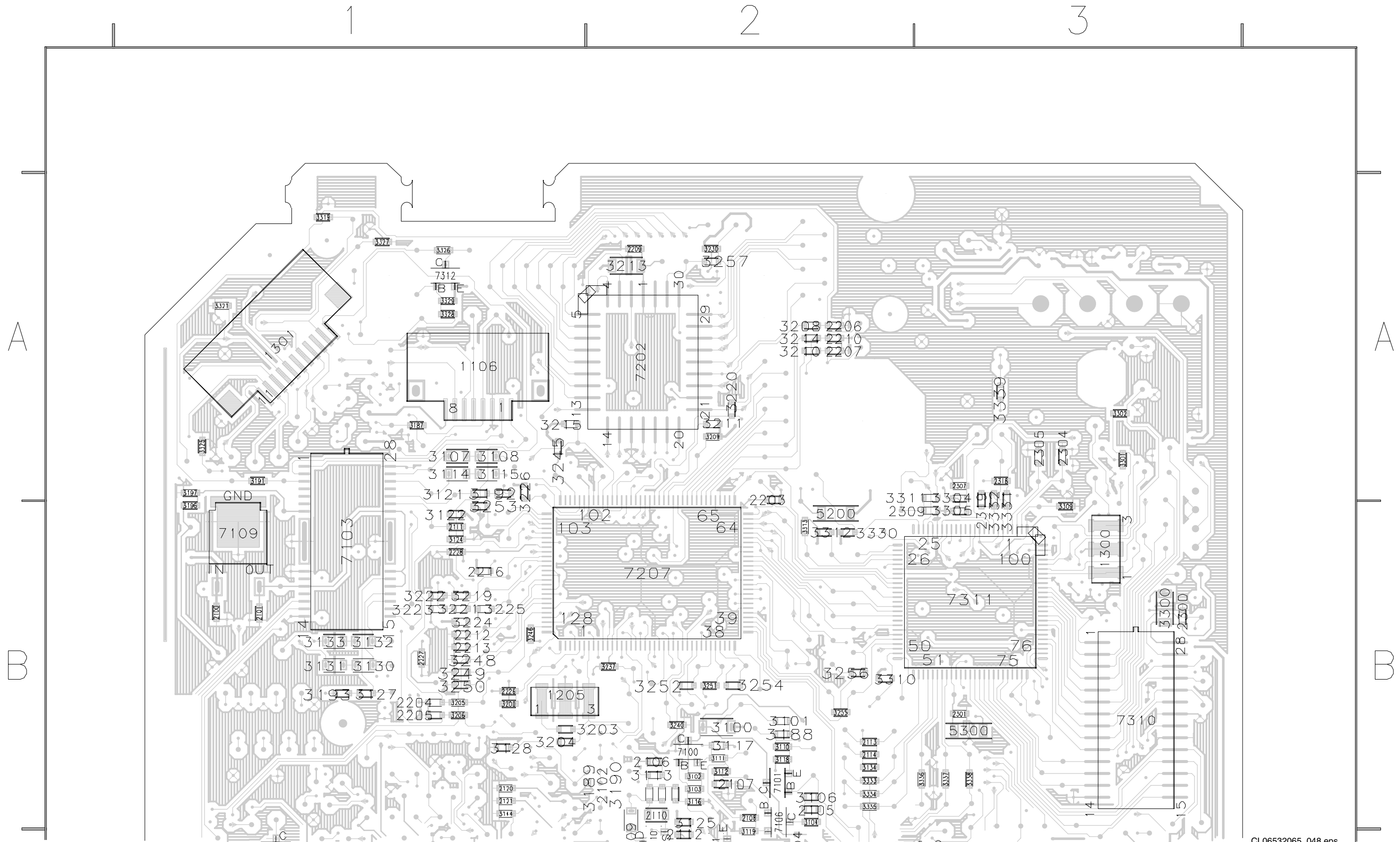
Detailed Top view 2



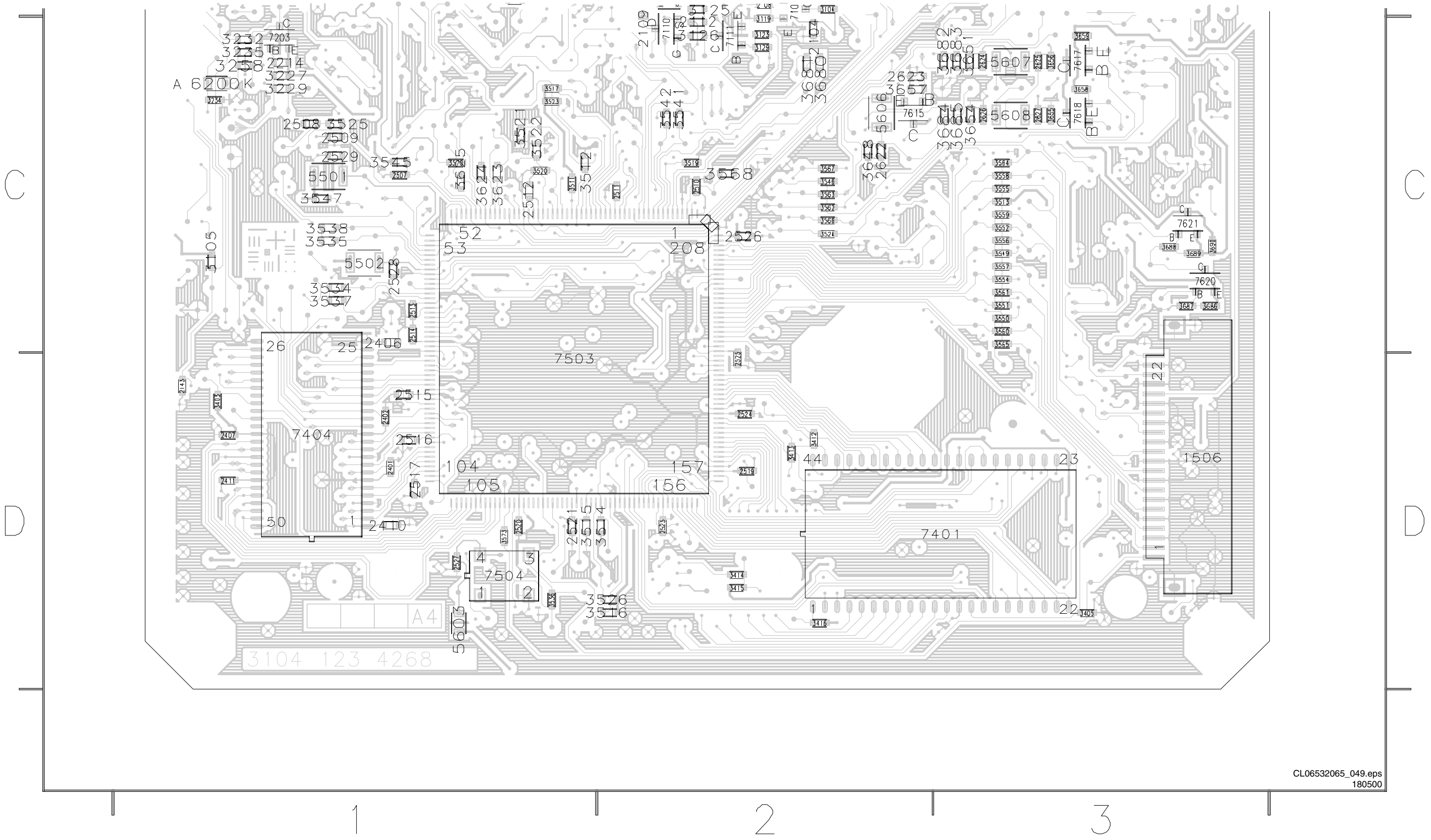




Detailed Bottom view 1



Detailed Bottom view 2







## 8. Alignments

No alignments available

## 9. IC Descriptions.

### 9.1 SAA7399 (MACE2) General.

Mace2 is a name used for the successor of the ACE1 IC. The term MACE (mini-ACE) is used because MACE2 does not have a decoder on board. Application area's: Mainly CD-R(W) and prototyping of DVD(-ROM) or high speed CD-ROM.

Functions implemented on-board of MACE2:

A further improved digital servo module. Derived from the ACE1 servo module, but with improvements (make the input switchable between diode signal and error signal processing, improved brake).

The 80C51 micro-controller with external ROM.

The OPC. Optimum Power calibration, used for CDR.

The PCS. Position Control Sledge. A way to speed up sledge movement using hall sensors.

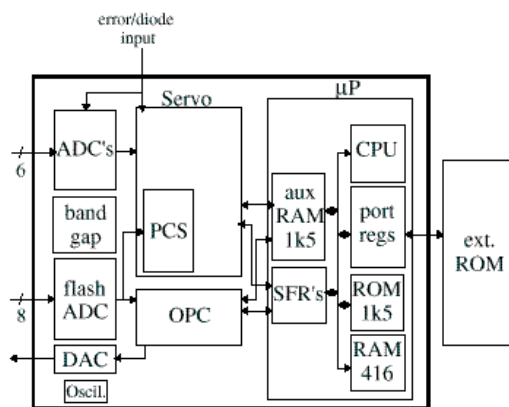


Figure 9-1 Overall block diagram MACE2.

### 9.2 Features

- Focus and Radial servo loop.
- Built-in access procedure.
- Selectable servo error or servo diode inputs.
- Focus noise performance equivalent to DSICS
- Automatic closed loop gain control available for focus and radial loops
- High speed track crossing velocity measurement > 350 kHz.
- Fast Radial Brake circuitry.
- Sledge motor servo loop, with pulsed sledge support and PCS
- Incorporated micro-controller equivalent to 80C51 --> 66MHz.
- Programmable wait state controller.
- Two embedded RAM's of 416 bytes and 1.5 kB res.
- Optimum Power Calibration Hardware support up to write at N=8.
- Debug facilities.
- Memory mapped interface to sub-modules.
- Programmable clock multiplier.
- 8 Multipurpose I/O lines.
- 5 external interrupt lines.
- External Flash ROM support.

- Sledge stepper motor support.

### 9.3 The Digital Servo block.

In a CD system, there are some 12 control loops active. About six of them are needed to adjust the servo error signals, that is once per disc rotation offsets, signal amplitudes and loop gains (AGC's) are adjusted to enlarge system robustness and to avoid expensive potentiometer adjustments in production. The other six loops determine the laser spot position on the disc in the radial, axial (focus) and tangential directions. The servo in MACE2 takes care of these controls.

The servo inside Mace2 also has to take care that the spot accesses a required position as fast as possible. This access system consists of two parts, namely the actuator and the sled, which are within a certain range, mechanically and electrically independent. So during an access the servo has to control as well the actuator as the sled.

### 9.4 Functional description servo

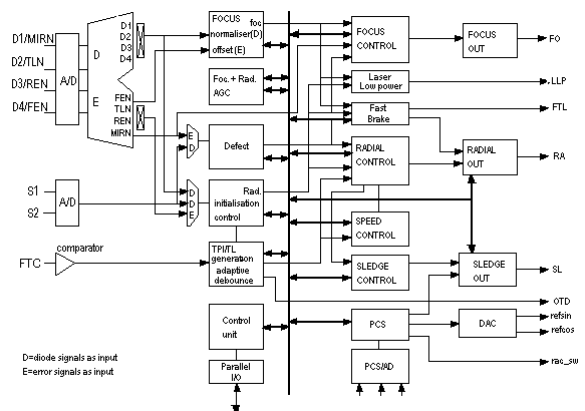


Figure 9-2 Mace2 servo block diagram.

The following functions can be distinguished:

- A to D conversion: a direct AD-conversion of the diode/error currents.
- Pulse density D to A conversion: Noise shaper output stages.
- Control unit: Provides mainly the communication and on/off functions.
- Focus normaliser: A partial division of focus and sum signal. Special saturating provisions are included when dividing through very small numbers.
- Initialisation control: Includes the radial normaliser, automatic radial offset compensation and level initialisation for the Track Position Indicator (TPI) for both diode and error input signals.
- TPI/TL generation and adaptive debounce: Generates Track loss (TL) which is protected against disc defects. The TL is made out of the unprotected TPI signal. The debouncer (with improved debounce times) minimises the disturbing effect of HF on the TL and Rp crossovers for the track count circuitry.

- Defect detector: Holds the focus and/or radial control signal on disc dropouts.
- Speed control: Used during access. With radial actuator feed forward.
- Focus control: PID controller with wide range adjustable characteristics.
- Radial control: PID controller with wide range adjustable characteristics.
- Sledge control: PID controller with wide range adjustable characteristics and a pulsed sledge controller.
- Laser Low Power: Switches the laser from write back to read power whenever the device tends to go off-track.

## 9.5 Input circuits servo

Five out of six of the MACE2 servo inputs can be switched between diode current inputs (for audio and data application) and error signal inputs (for recordable applications).

The analogue signals from the diode pre processor are converted into a digital representation using A/D converters.

## 9.6 Focus control.

### 9.6.1 Focus start-up.

To bring the actuator in focus position a triangular shaped voltage is applied to the actuator to perform a search movement. When the lens moves from or to the disc, CA (central aperture) is monitored to reach a certain programmable absolute level. When this value is CA level is reached, the FOK signal becomes true and FEn is passed to the FEn level detector.

At the moment this FEn level is reached the wait for the focus mode is entered and the focus control loop is enabled to detect a sign inversion in the FEn signal.

When this zero crossing in this FEn signal is detected, the loop is closed to function as PID controlled loop and is switched to the PID mode.

During focus start-up a dither signal is added to the output signal of the integrator. It prevents the actuator from hitting its natural resonance. With this technique quantisation, effects are compensated for during start-up.

### 9.6.2 Focus Position Control loop.

The focus control loop contains a digital PID controller that has 5 parameters available to the user. These coefficients influence the integrating, proportional and differential action of this PID and a digital low pass filter following the PID. The fifth coefficient influences the loop gain.

### 9.6.3 Dropout detection.

This detector can be influenced by one parameter. The FOK signal will become false and the integrator of the PID will hold if the CA signal drops below this programmable absolute CA level. When the FOK signal becomes false, it is assumed as caused by a black dot in the first place.

### 9.6.4 Focus Loss detection and Fast restart.

Whenever FOK is false longer than about 2 ms, it is assumed that the focus point is lost. A fast restart procedure is initiated which is capable of restarting the focus loop within 200 to 300 ms depending on the uP-programmed coefficients.

### 9.6.5 Focus Automatic Gain Control loop.

The loop gain of the focus control loop can be corrected automatically to eliminate tolerances in the focus loop. This gain control injects a signal into the loop that is used to

correct the loop gain. Since this decreases the optimal performance, the gain control should only be activated shortly (for instance when starting a new disc).

## 9.7 Radial control.

The MACE2 digital controller includes the following radial servo functions:

### 9.7.1 Level initialisation:

During start-up an automatic adjustment procedure is activated to set the values of the radial error gain, offset and satellite sum/MIRN signal gain for TPI level generation. The initialisation procedure runs in a radial open loop situation and is < 200 ms. This start-up time period may coincide with the last part of the turntable motor start-up time period.

### 9.7.2 Automatic gain adjustment:

Because of this initialisation the amplitude of the RE signal is adjusted within  $\pm 10\%$  around the nominal RE amplitude. Offset adjustment: The additional offset in RE due to the limited accuracy of the start-up procedure is less than  $\pm 50\text{nm}$ .

### 9.7.3 TPI level generation:

The accuracy of the initialisation procedure is such that the duty cycle range of TPI becomes  $0.4 < \text{duty cycle} < 0.6$ .

#### **Sledge home:**

Sledge moves to reference position at the inner side of the disc with user defined voltage.

#### **Tracking control:**

The actuator is controlled using a PID loop filter with user defined coefficients.

#### **Access:**

In Mace2 there are two fundamentally different ways to perform an access:

#### *Using the PCS*

A more detailed description of this access method is given in another section.

#### *Using the servo controlled access:*

The way it was done in the predecessors of Mace2. This access procedure is divided into 3 different modes, depending on the requested jump size:

access type    size    access speed

Actuator jump    decreasing velocity

Sledge jump    maximum power to sledge 1

Controlled sl. jump    controlled brake power

The access procedure makes use of a track counting mechanism, a velocity signal based upon the number of tracks passed within a fixed time interval, a velocity setpoint calculated from the number of tracks to go and a user programmable parameter indicating the maximum sledge performance.

If the number of tracks to jump is too large, then the Sledge jump mode is activated, else the actuator jump is performed. The requested jump size together with the required sledge braking distance at maximum access speed defines the value of the maximum numbers of tracks.

During the actuator jump mode, velocity control with a PI controller is used for the actuator. The sledge is then continuously controlled using the filtered value of the integrator contents of the actuator. All filter parameters (for actuator and sledge) are user programmable.

In the sledge jump mode maximum power (user programmable) is applied to the sledge in the correct direction, while the actuator becomes idle.

#### **Radial Automatic Gain Control loop:**

The loop gain of the radial control loop can be corrected automatically to eliminate tolerances in the radial loop. This gain control injects a signal into the loop which is used to correct the loop gain. Since this decreases the optimal performance the gain control should only be activated shortly (for instance when starting a new disc). This gain control differs from the earlier mentioned level initialisation. This level initialisation should be done first. The level initialisation without the gain control reduces tolerances from the front-end only.

### 9.8 The radial PID.

Since we are dealing with a big variety of applications and drives, the servo controllers in MACE2 should be adjustable within a large frequency range.

In order to read out the track properly - a track consists of sequential ordered data pit's which hold audio, video or ROM data - the focus and radial position controls must follow the moving track within some tenths of a micrometer, despite of disc imperfections and external disturbances.

For instance, a rotating disc causes, due to track eccentricity, track unroundness, or disc skew, track movements up to some millimetres. The control loop reduces this to about one tenth of a micrometer.

### 9.9 Initialisation control.

Due to optical, electrical and mechanical tolerances in CD players, properties of the servo signals such as offset and gain can vary. In general, without proper signal processing, a simple PID controller function cannot cope with this relatively large offset and gain spreads. Therefore, gain and offset adjustments during manufacture or active control, to compensate for these signal imperfections, become inevitable.

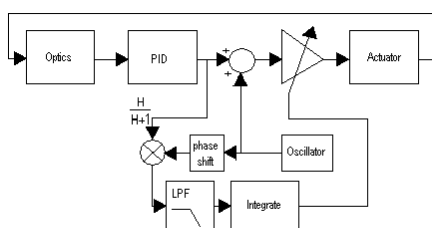
Adjustment procedures in the factory are expensive. So, automatic adjustment procedures have been implemented in order to avoid most of the potentiometer adjustments. In the MACE2 servo automatic adjustments are applied to the radial error signal only.

### 9.10 The AGC.

The Automatic Gain Control is used in the MACE2 digital servo to adjust the radial and focus bandwidths to a nominal value. Injecting a signal in the loop and measuring the phase of its resulting signal (wobble method) does this.

Principle of the Automatic Gain Control.

The principle of the Automatic Gain Control (AGC) circuit, as used in MACE2, is drawn in the next figure.



**Figure 9-3 Principle of the automatic gain control.**

A sine wave signal with a certain frequency is injected in the control loop at the summation point. The resulting signal is

measured before the injection point. The injected signal is shaped by  $H/1+H$ . This measured signal is multiplied by a phase shifted version of the injected signal. The result of the multiplication is low pass filtered and integrated. (The integrator is started at the nominal gain of the control loop). The result of the integration is fed to the adjustable loop gain. This principle, synchronous detection, is also known as 'wobble method'.

### 9.11 The Fast brake.

The fast brake is an aid to speed up radial capture after a high-speed jump. It is a separate radial control with a much higher bandwidth. The radial control output can be switched between fast brake mode and original radial control mode. The fast brake helps the radial actuator at the end of a jump to "stick" to the right track. In fast brake mode, the actuator starts to follow the track movements. It's a bit like jumping on a moving train. If you run as fast as the train, you can just step in. After a radial open loop jump the tracks are moving (as a result of eccentricity) at a very high speed underneath the radial actuator. This speed is too high for a normal radial control loop to do radial capture. When the radial control is switched over to fast brake mode for a short term, this moving of the tracks underneath the actuator becomes much slower, (because the actuator follows the track movement), so when you switch back to original radial control, it's much easier to do radial capture.

### 9.12 The Defect Detector.

Because of the possible earlier mentioned defects (fingerprints, etc) a defect detection circuit is incorporated into the MACE2 servo. If a defect is detected, the radial and focus error signals may be zeroed, resulting in better playability.

#### 9.12.1 Operation:

The defect detector prevents the light spot from going out of focus and going off track due to disc dropout excitations. The defect detector can be switched on and off under software control and can be applied to the focus control only, or both to the focus and radial control.

Whenever this circuit detects a defect, it will hold all radial and focus controls.

The hold signal is generated whenever the reflected light intensity drops rapidly ( $< 1.5$  ms) down to roughly 75% of the actual intensity level. In that case the output of the comparator becomes active and controls the focus and radial signal switch.

This circuit improves the playability of the application (black dot performance, etc) and is programmable to optimise it for specific disc defects. The actions of this circuit can be monitored on the DEFO pin (active high).

An external defect detection circuit can be added by removing the connection between DEFO and DEF1 (normal operation) and inserting the external circuitry.

These signals are afflicted with some uncertainties caused by:

- Disc defects like scratches and fingerprints
- The HF information on the disc, which is considered as noise by the detector signals.

### 9.13 Laser Drive On.

The LDON pin is used to switch the laser drive off and on. It is an open drain output. In case the laser is on, the output has a high impedance. The pin will be automatically driven if the focus control loop is switched on.

### 9.14 Laser Low Power (LLP).

The LLP output can be used by write-able systems to switch the laser back to read power when the light spot goes off-track while writing discs. To prevent that the neighbour tracks are damaged when the spot goes off-track the laser has to be switched very fast to the safe read power. The laser is not switched off (like LDON does), so the system can carry on reading.

The tracking (radial) and focus error signals are used to disable the laser write power. This is done through the LLPn, active low Laser Low Power, signal. Note that LLPn is a servo output, which is inverted before it is output via the LLP pin, so the LLP pin is active high.

So, if any of the following conditions is true, the laser write power is disabled by the MACE2 servo.

- Off Track, more than a quarter off a track away from the correct one
- ORD, radial error signal too large. Larger than the given setpoint, which should be chosen at a critical write failure level. An adjustable band pass filter first processes the radial error signal.
- OFD, focus error signal too large. Larger than the given setpoint, which should also be chosen with care. An adjustable band pass filter also first processes the focus error signal. All settings of the focus and radial part are independent.
- OTR, prot stat flag which becomes active if ORD becomes active during an actual laser write ( LWR) action. This flag is reset only by a status read ( RSTAT) command. So until then LLPN stays active.
- OFO, prot stat flag that becomes active if OFD becomes active during an actual laser write action. Same idea as OTR.

This error detection circuit can be switched off (apart from the Off Track detection) by raising the setpoint levels to its maximum value.

### 9.15 The OPC.

The OPC block in Mace2 is used for the following functions:

- During write actions, it stores Pw samples, which can be evaluated by the microprocessor.
- During OPC read actions, it stores A1, A2 and CALF samples, which are used for calculating the asymmetry and the modulation index.
- The OPC block is used for EFM detection.
- During reading of a disc, it stores A1 and CALF samples, which can be monitored.

Although the OPC block is used for multiple functions, it got its name from the OPC procedure, which is its main task.

The OPC (Optimum Power Calibration) procedure is used in CD-R/CD-RW/DVD-RAM applications. It is used to "calibrate" the laser write power in writable systems. It reads in 3 analogue signals from an analogue pre-processor like AEGER-2 (A1, A2, and CALF) and the actual write power (Pw) from the laser controller and feeds an analogue output signal Alpha0 back to AEGER-2. A1, A2 and CALF represent the max, min and average value of the EFM signal respectively. Alpha0 controls the laser write power. All analogue signals are converted to an 8 bit digital signal. Conversion frequency at 16.9MHz base clock is 88kHz (each channel).

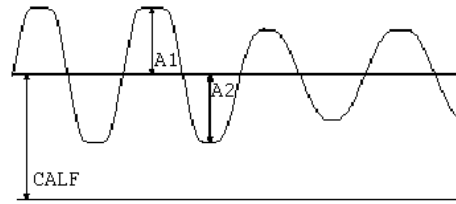


Figure 9-4 Definition of the A1, A2 and CALF signals.

### 9.16 Definition of terms.

The asymmetry ( and modulation index m of the EFM signal are calculated from the analogue inputs:

$$\beta = \frac{A1 - A2}{A1 + A2}$$

$$m = \frac{A1 + A2}{A1 + CALF}$$

### 9.17 Rough description of the OPC procedure

Basically the OPC procedure tries to find out the optimum laser power to be used on a specific disc. The OPC procedure uses about 15 ATIP frames. These frames are located in the "PCA" area. This is a special part of the disc used only for power calibration. The drive first checks whether there are 15 frames "empty" in the PCA. Next the OPC is performed in these 15 frames.

The OPC operation consists of two stages: A "write" and a "read" stage. First 15 ATIP frames are written (during which the OPC block stores Pw samples), and then the same 15 ATIP frames are read back again, (during which the OPC block stores A1, A2 and CALF samples). During the write stage, random EFM is written in a test area located on the inner side of the disc. During this recording the write power is increased stepwise from a low to a high power level.

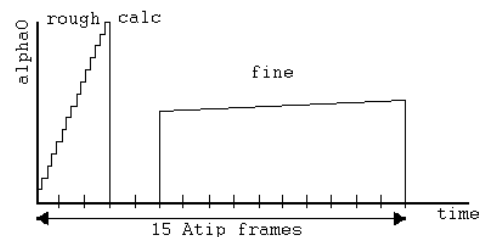


Figure 9-5 Figure 5: OPC write profile.

First during 3 ATIP frames the power is increased in rather big steps (rough OPC). During this action Pw samples are stored into memory. During the rough OPC, the OPC makes 7 steps per ATIP frame. This gives 21 samples into the OPC memory. From these samples, the microprocessor can calculate what's roughly the best alpha0 setting for this typical disc.

After 2 frames of calculations, another 10 ATIP frames are written using smaller steps (fine OPC) around the alpha0 setting, which gave the best result during the rough OPC. The second stage of the OPC procedure is the "read" phase



in which the pattern recorded in the previous stage is read back.

During this read phase the OPC block stores A1, A2 and CALF samples from exact the same location where during the OPC write phase the Pw samples where stored. The samples for A1, A2, CALF and Pw are listed side by side into memory. After the read back phase the processor calculates at which setting of alpha0 the least jitter is encountered. This setting will be used to write the disc with.

### 9.18 The OPC top level.

The OPC block as a whole has 5 possible modes:

- Recording mode: This can be either OPC writing (writing EFM test patterns to disc and Alpha0 stepping) or standard write mode (i.e. alpha0 is constant).
- OPC reading: Reading back OPC test patterns from disc.
- Normal read mode: detects the presence of EFM.
- DVD read mode: used for DVD-RAM experiments.
- EFMD only mode: no data being written to the AUX RAM, but the EFM detector and the PW monitor still running. Contents of the QUX RAM remain unchanged.

All actions in the OPC hardware are synchronised to the ATIP frame sync, which can be either generated internally or received from the encoder/decoder during writing. The microprocessor writes data asynchronously to the OPC hardware. The OPC block synchronises this data to the sync either internally generated, or obtained from CDR-60.

### 9.19 The Analogue to Digital converter.

The analogue to digital converter of the OPC is shared with the ADC required by the PCS.

### 9.20 The digital input filters.

The combined ADC for the OPC and the PCS delivers a multiplexed stream of 8 bit words. A sequential low-pass filter filters this multiplexed stream. The 4 analogue multiplexed input signals from the OPC (A1, A2, CALF and Pw) are filtered by 4 identical LPF's. (One for each channel). This filters can be adapted to various speeds by changing the subsampling factor (i.e. the sample rate of the filter), the cut off frequency scales with the sample frequency. The sample frequency of the filter is equivalent to the OPC timebase frequency, which is the output of the pre-scaler.

### 9.21 OPC demux.

The OPC demux block demultiplexes the stream supplied by the LPF. This same block also changes the format of the digital data from signed (representation inside the filter) to unsigned (representation in the rest of the OPC). The demultiplexing process introduces one baseclock delay.

### 9.22 The sequencer.

The OPC sequencer controls the timing of all the hardware actions in the OPC hardware. It generates the OPC timebase and locks it to the ATIP pulse. A programmable pre-scaler generates the OPC timebase.

Dividing the ADC sample clock by 8 derives the input clock of this pre-scaler. (= Identical to the sample rate per channel). The pre-scaler can divide this clock by a number in the range from 1-16. The division factor can be programmed via the OPC ctrl register. The OPC timebase is locked to the selected ATIP source, which can be either an external ATIP sync or an internally generated sync. (Programmable). The OPC timebase clock supplies the sample frequency for

the input LPF's, the OPC pre-processor and the EFM detector.

The sequencer controls the timing of all the hardware actions in the OPC hardware. The sequencer is started either by an external ATIP sync or an internally generated sync (programmable).

All data acquisition and alpha0 settings change synchronised to this sync signal (rising edge of the ATIP sync). An exception on this is the switching of the ATIP input itself, which is immediately changed whenever the bit in the OPC ctrl register is changed. When this was latched on the ATIP source itself, it would create a deadlock when there was no ATIPin from CDR-60.

### 9.23 The Pw monitor

The Pw monitor is used during the "OPC write" and normal write mode. The comparator compares the incoming Pw with two programmable thresholds PW MAX and PW MIN. Both these thresholds can be programmed via the OPC PW register, which contains 4 bits for each threshold. Internally both 4-bit thresholds PW MAX and PW MIN are extended to 8 bit values. The compare function performs an unsigned compare.

The first threshold is used to detect fingerprints. The second is used to check the correct operation of the laser driver.

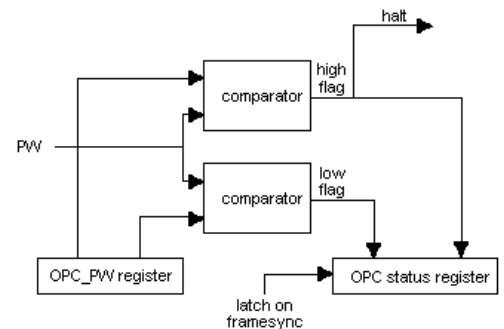


Figure 9-6 OPC PW monitor.

## DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply

**TZA1033**

### FEATURES

- Operates with DVD-ROM, DVD-RAM, DVD+RW, DVD-RW, CD-ROM and CD-RW media
- Operates up to 64x CD-ROM and 8x DVD-ROM
- Support for Dual Light pen DVD systems (DVD/CDRW)
- DVD-RAM (C) playback capability
- DVD-RAM Land-Groove servo polarity switching
- 3 different tracking servo strategies:  
Conventional 3 beam tracking for CD  
Differential Phase Detection (DPD) for DVD-ROM (including option to emulate traditional drop out detection; drop out concealment)  
Advanced Push Pull with dynamic offset compensation for DVD-RAM (recorded and unrecorded areas)
- Radial error signal for fast track counting (FTC)
- 2 different strategies to read header data:  
- Full bandwidth Push Pull signal  
- Left and Right side signal
- Universal photo diode IC interface using internal conversion resistors and offset cancelation
- Flexible adaption to different light pen configurations
- Input buffer amplifiers with low-pass filtering
- RF data amplifier with wide (programmable) bandwidth equivalent to 64xCD / 8x DVD when using equaliser function
- Built-in equalisers cover CAV inner-outer disc range at highest speed.
- Programmable RF gain for DVD-ROM / DVD-RAM / CD-RW / CDRom applications (approx 50dB range)
- Balanced RF-Data signal transfer (single ended still supported)
- Fully automatic laser control including stabilization and an ON/OFF switch, plus a separate supply pin for power efficiency
- Automatic monitor diode polarity selection.
- 3 and 5 V compatible digital interface
- Enhanced signal conditioning in DPD circuit for optimal tracking performance under noisy conditions.

### GENERAL DESCRIPTION

The DVDALAS2 is an analogue preprocessor and laser supply circuit for DVD / CD read only players. The device contains data amplifiers, several options for radial tracking and focus control. The preamplifier forms a versatile, programmable interface between dual, voltage output CD/DVD mechanisms to Philips' digital signal processor family for CD and DVD (Gecko, HDR65, Iguano, etc..)

The device contains several options for radial tracking:  
Conventional 3 beam tracking for CD;  
Differential Phase Detector (DPD) for DVD;  
Push Pull for DVD-RAM with flexible L/R weighting to compensate dynamic offsets e.g. beamlanding offset.  
A radial error signal is generated to allow fast track count (FTC) during track jumps.

The dynamic range of this preamp/processor combination can be optimized for the LF servo and RF data paths. The gain in both channels can be programmed separately. This will guarantee an optimal playability for all kind of discs.

Several functions are included to allow playback of DVD-RAM(C) discs:

- The header information can be read via the data output path (RF)
- DC offset compensation techniques provide a fast settling after disc errors.
- Radial servo Polarity switch for land/groove
- two settings for focus offset correction for land and groove

The device can accommodate astigmatic, single focault and double focault detectors and can be used with P-type lasers with N- or P-sub monitor diodes. After an initial adjustment, the circuit will maintain control over the laser diode current. With an on-chip reference voltage generator, a constant and stabilized output power is ensured independent of ageing. A separate power supply connection allows the internal power dissipation to be reduced by connecting a low voltage supply.

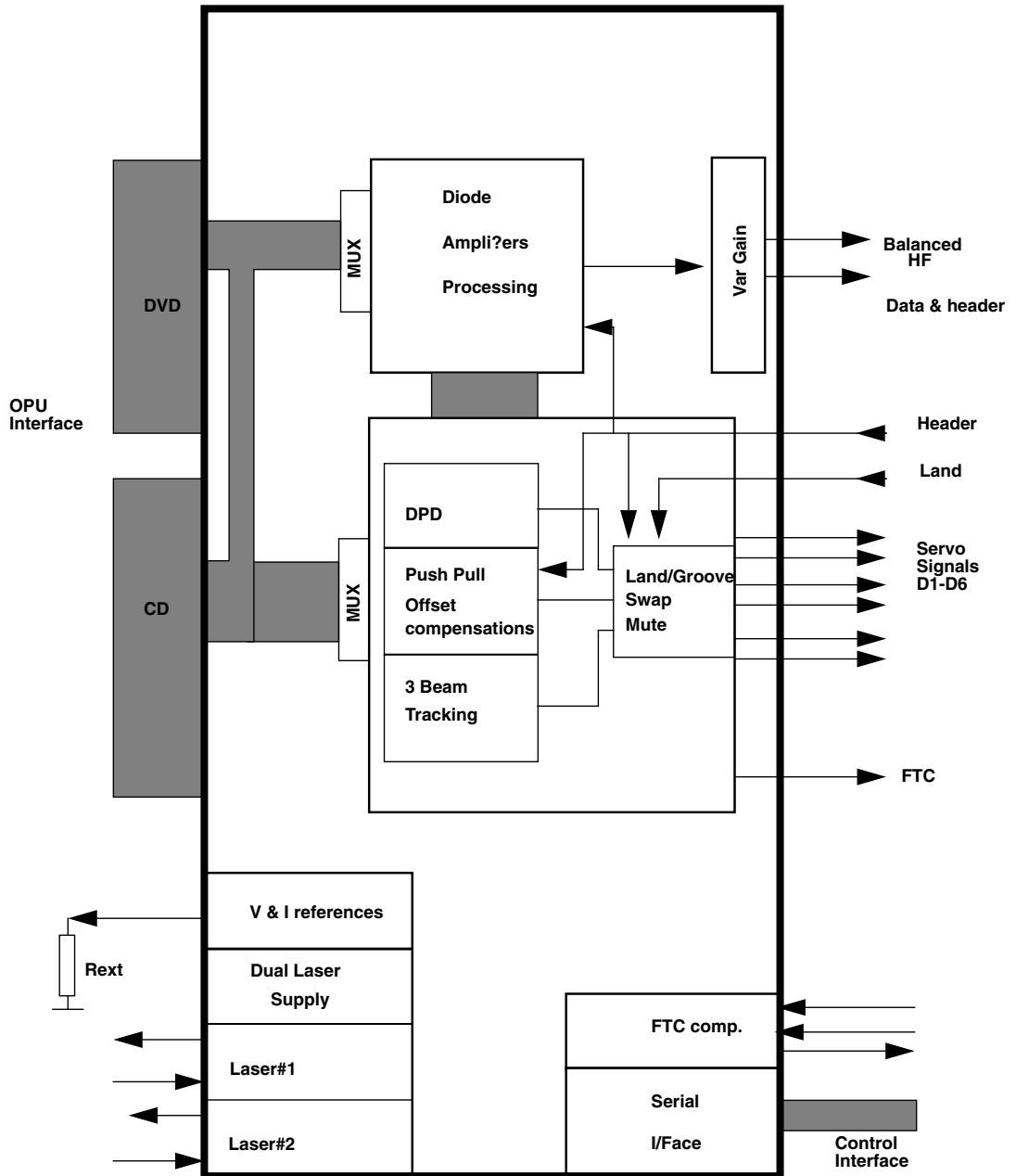
### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA1023	LQFP64	Plastic low profile QFP64; body 10 x 10 x 1.4 mm	SOT314-2

DVDALAS2plus Advanced Analogue DVD  
Signal Processor and Laser Supply

TZA1033

DEVICE BLOCK DIAGRAM



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**DVDALAS2plus Advanced Analogue DVD  
Signal Processor and Laser Supply**


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TZA1033

**PINNING**

<b>Name</b>	<b>Pin</b>	<b>Description</b>
CD-A	1	CD pick up input A
CD-B	2	CD pick up input B
CD-C	3	CD pick up input C
CD-D	4	CD pick up input D
CD-REF	5	CD pick up reference voltage
CD-E	6	CD pick up input E
CD-F	7	CD pick up input F
DVD-A	12	DVD pick up input A
DVD-B	13	DVD pick up input B
DVD-C	14	DVD pick up input C
DVD-D	15	DVD pick up input D
DVD-ref	16	DVD pick up reference voltage
O-A	48	Servo current output for Focus-A
O-B	47	Servo current output for Focus-B
O-C	46	Servo current output for Focus-C
O-D	45	Servo current output for Focus-D
O-central	40	Testpin for offset cancelation
TD2	37	Internally connected
FTC-ref	36	Servo output voltage reference input
S1	42	Servo current output for radial tracking
S2	41	Servo current output for radial tracking
TD1	35	Internally connected
FTC	33	Fast track count voltage output
RFP	55	pos. RF output signal
RFN	56	neg. RF output signal
RF-REF	54	DC Reference signal input RF
LPF-DPD1	38	DPD Low pass bandwidth capacitor, channel pos
LPF-DPD2	39	DPD Low passbandwidth capacitor, channel neg
Land	20	Land/groove toggle input
HEADER	21	Header detector window input
CD-MI	62	CD laser monitor input
DVD-MI	10	DVD laser monitor input
CD-LO	61	CD laser output
DVD-LO	64	DVD laser output
COP	27	Positive inputFTC comparator
COM	28	Inverting inputFTC comparator
COO	29	FTC comparator output

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**DVDALAS2plus Advanced Analogue DVD  
Signal Processor and Laser Supply**

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TZA1033

<b>Name</b>	<b>Pin</b>	<b>Description</b>
SIDA	23	Serial host interface data input
SICL	24	Serial host interface clock input
SILD	25	Serial host interface load
VDDA1	8	Analog Supply voltage 1 (RF input)
VDDA2	59	Analog Supply voltage 2 (RF internal)
VDDA3	53	Analog Supply voltage 3 (RF output stage)
VDDA4	44	Analog Supply voltage 4 (Servo)
VDDD5	30	Digital Supply voltage (5V dig core)
VDDD3	22	Digital Supply voltage (3V I/O pads and FTC comp.)
VDDL	63	Supply voltage for laser
VSSA1	9	Analog Ground 1
VSSA2	58	Analog Ground 2
VSSA3	57	Analog Ground 3
VSSA4	43	Analog Ground 4
VSSD	26	Digital ground
Rext	60	Reference current input (Connect 12k1 to VSSA4)
STB	31	Standby input
TM	19	Testmode input
TDO	34	test data out

DVDALAS2plus Advanced Analogue DVD  
Signal Processor and Laser Supply

TZA1033

PINNING

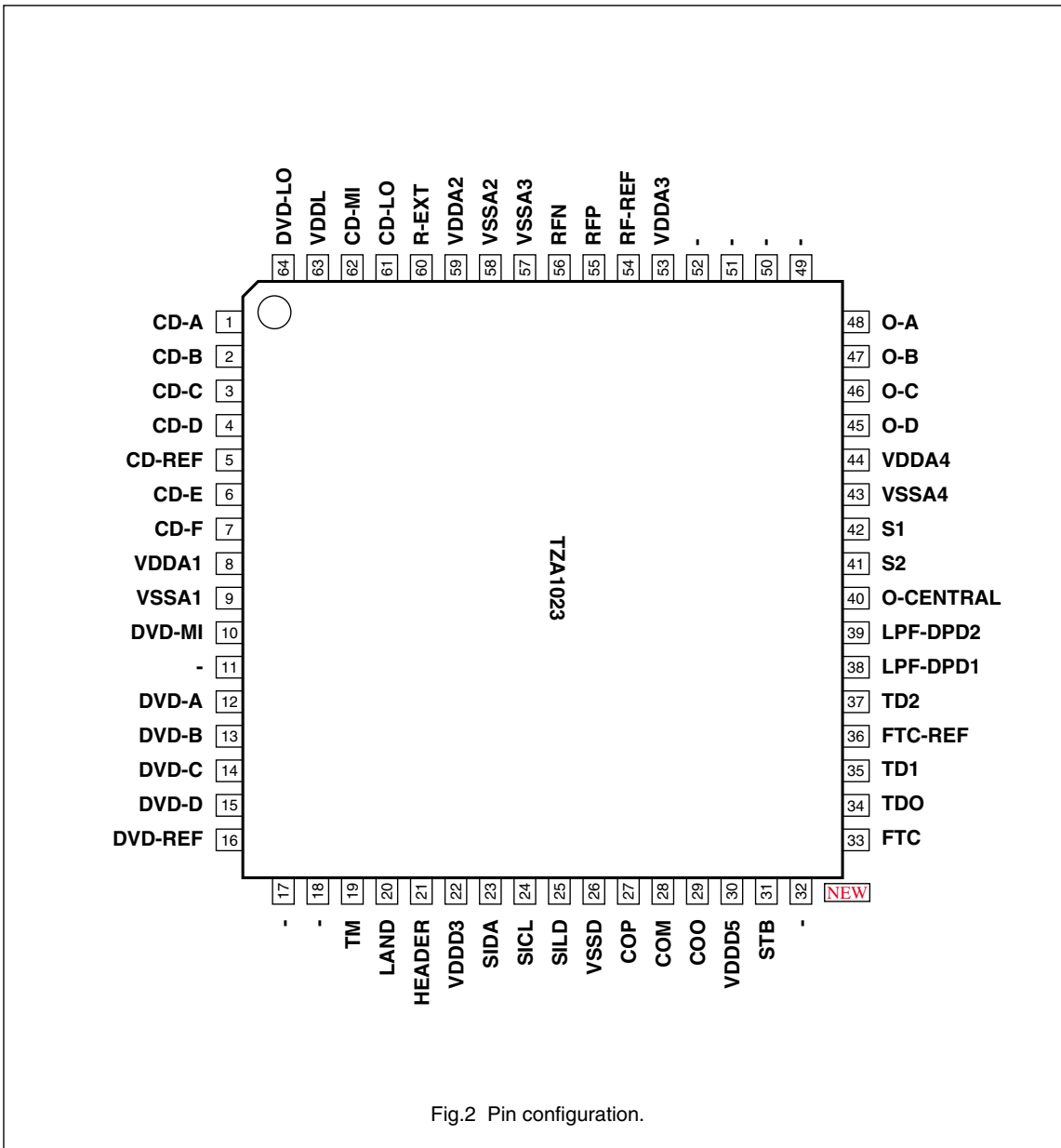


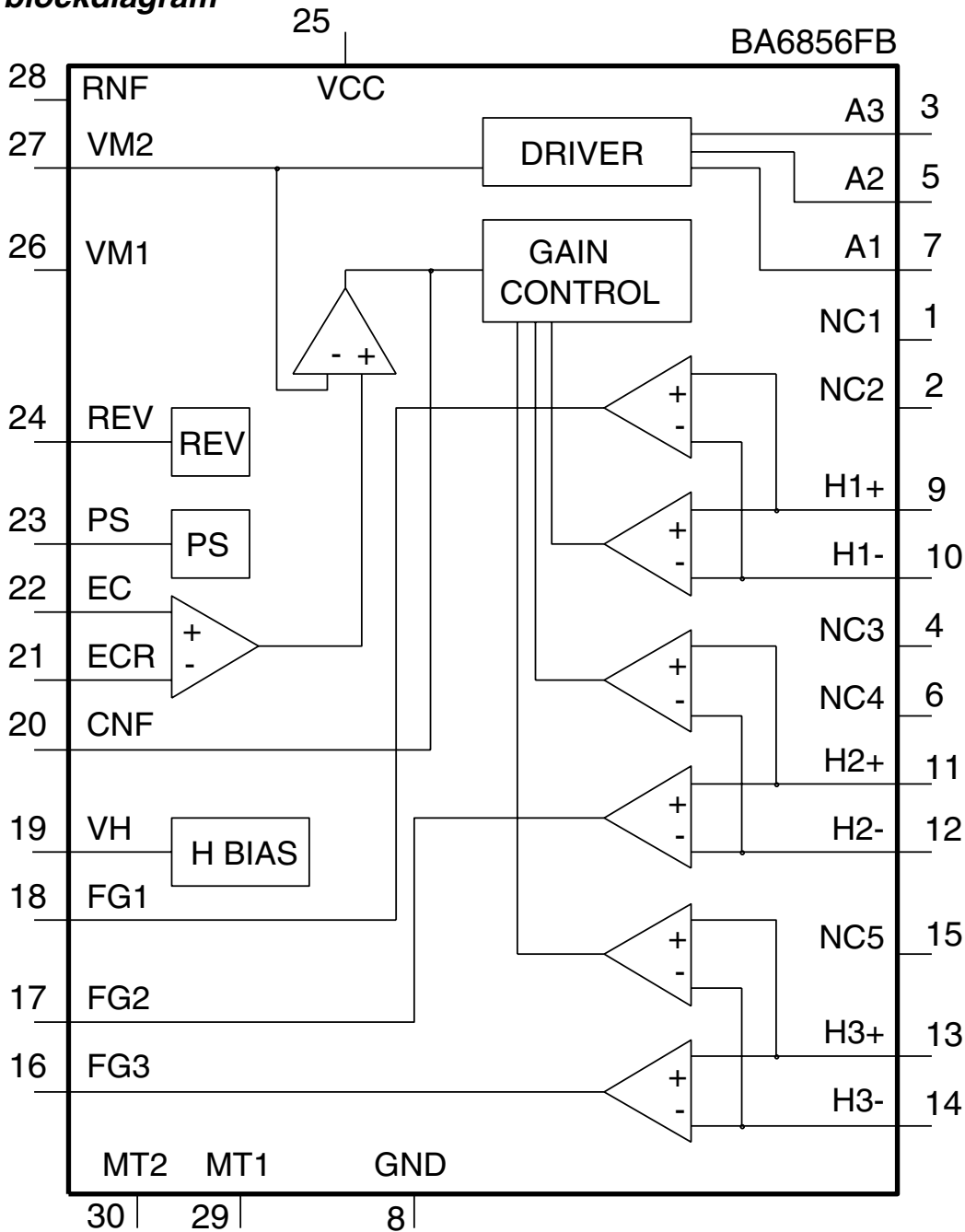
Fig.2 Pin configuration.

## BA6856FP: 3 PHASE MOTOR DRIVER FOR DVD PLAYERS

### Features

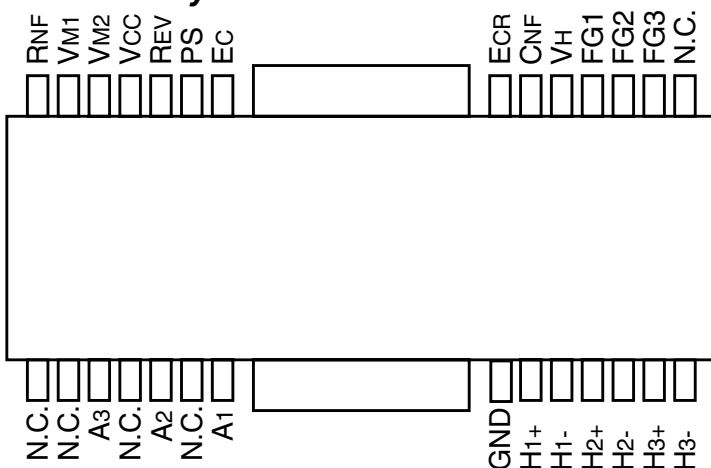
- 1/3-phase, full-wave pseudo linear driving system
- built-in power save
- built-in thermal shut down circuit
- built-in current limit circuit
- built in Hall bias circuit
- built in FG-output (3-phase parallel output)
- with switching function of regular/ reverse rotations

### blockdiagram



**pin description**

PIN No	PIN NAME	DESCRIPTION
1	N.C.	Not connected
2	N.C.	Not connected
3	A <sub>3</sub>	Output 3 for motor
4	N.C.	Not connected
5	A <sub>2</sub>	Output 2 for motor
6	N.C.	Not connected
7	A <sub>1</sub>	Output 1 for motor
8	GND	Ground
9	H <sub>1</sub> <sup>+</sup>	Hall input Amp1. positive input
10	H <sub>1</sub> <sup>-</sup>	Hall input Amp1. negative input
11	H <sub>2</sub> <sup>+</sup>	Hall input Amp2. positive input
12	H <sub>2</sub> <sup>-</sup>	Hall input Amp2. negative input
13	H <sub>3</sub> <sup>+</sup>	Hall input Amp3. positive input
14	H <sub>3</sub> <sup>-</sup>	Hall input Amp3. negative input
15	N.C.	Not connected
16	FG3	FG3 signal output terminal
17	FG2	FG2 signal output terminal
18	FG1	FG1 signal output terminal
19	V <sub>H</sub>	Hall Bias
20	C <sub>NE</sub>	Capacitor connection pin for phase compensation
21	E <sub>CR</sub>	Torque control standard voltage input terminal
22	E <sub>C</sub>	Torque control voltage input terminal
23	PS	POWER SAVE switch
24	R <sub>EV</sub>	Reverse terminal
25	V <sub>CC</sub>	Power supply for sinal division
26	V <sub>M2</sub>	Power supply 2 for driver
27	V <sub>M1</sub>	Power supply 2 for driver
28	R <sub>NE</sub>	Power supply for driver division
FIN	FIN	GND

**Terminal lay-out**



## DSP for CD and DVD-ROM systems

## SAA7335

### FEATURES

- Compatibility with CD-I, CD-ROM, MPEG-video DVD-ROM and DVD-video applications
- Designed for very high playback speeds
- Typical CD-ROM operation up to  $n = 12$ , DVD-ROM to  $n = 1.9$ , maximum rates (tbf)
- Matched filtering, quad-pass error correction (C1-C2-C1-C2), overspeed audio playback function included (up to 3 kbytes buffer)
- Lock-to-disc playback, Constant Angular Velocity (CAV), pseudo-Constant Linear Velocity (CLV) and CLV motor control loops
- Interface to 32 kbytes SRAM for DVD error correction and de-interleave
- Sub-code/ header processing for DVD and CD formats
- Programmable HF equalizer
- In DVD mode it is still compatible with Philips block decoders
- Sub-CPU interface can be parallel or fast I<sup>2</sup>C-bus
- On-chip clock multiplier.



In DVD modes double-pass C1-C2 error correction is used which is capable of correcting up to 5 C1 frame errors and 16 C2 frame errors.

The SAA7335 contains all the functions required to decode an EFM or EFM+ HF signal directly from the laser pre-amplifier, including analog front-end, PLL data recovery, demodulation and error correction. The spindle motor interface provides both motor control signals from the demodulator and, in addition, contains a tachometer loop that accepts tachometer pulses from the motor unit.

The SAA7335 has two independent microcontroller interfaces. The first is a serial I<sup>2</sup>C-bus and the second is a standard 8-bit multiplexed parallel interface. Both of these interfaces provide access to a total of  $32 \times 8$ -bit registers for control and status.

This data sheet contains an descriptive overview of the device together with electrical and timing characteristics. For a detailed description of the device refer to the user guide "SAU/UM96018".

Supply of this CD/DVD IC does not convey an implied license under any patent right to use this IC in any CD or DVD application.

### GENERAL DESCRIPTION

This device is a high-end combined Compact Disc (CD) and Digital Versatile Disc (DVD) compatible decoding device. The device operates with an external 32 kbytes S-RAM memory for de-interleaving operations. The device provides quad-pass error correction for CD-ROM applications (C1-C2-C1-C2) and operates in lock-to-disk, CAV, pseudo CLV and CLV modes.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DDD</sub>	digital supply voltage	4.5	5.0	5.5	V
I <sub>DDD</sub>	digital supply current	–	70	300	mA
V <sub>DDA</sub>	analog supply voltage	4.5	5.0	5.5	V
I <sub>DDA</sub>	analog supply current	–	70	300	mA
f <sub>xtal</sub>	crystal input frequency	4	25	tbf	MHz
T <sub>amb</sub>	operating ambient temperature	–20	–	+70	°C
T <sub>stg</sub>	storage temperature	–55	–	+125	°C

DSP for CD and DVD-ROM systems

SAA7335

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7335GP	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

**BLOCK DIAGRAM**

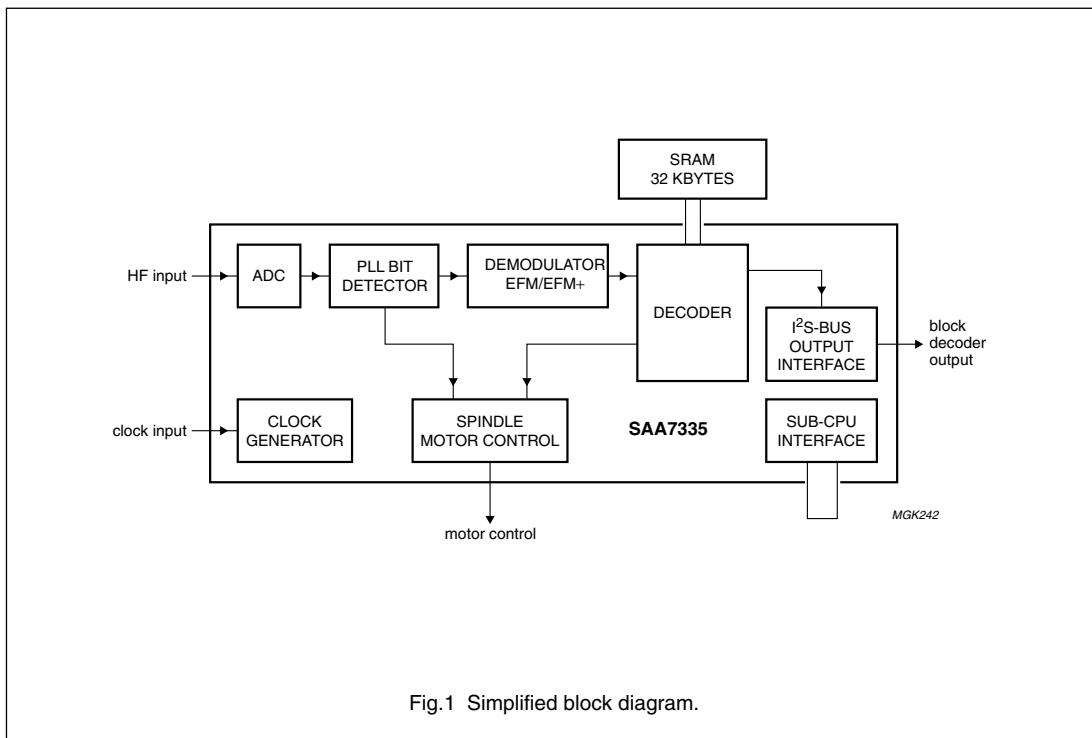


Fig.1 Simplified block diagram.

## DSP for CD and DVD-ROM systems

SAA7335

## PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
V <sub>SSA1</sub>	1	supply	analog ground 1
I <sub>ref</sub>	2	I	analog current reference input for ADC
REFLo	3	I	analog low reference input for ADC
REFHi	4	I	analog high reference input for ADC
VREF	5	I	analog negative input
HFIN	6	I	analog positive input
V <sub>SSA2</sub>	7	supply	analog ground 2
AGCOUT	8	O	analog test pin output
V <sub>DDA2</sub>	9	supply	analog supply voltage 2
V <sub>DDD1</sub>	10	supply	digital supply voltage 1
V <sub>SSD1</sub>	11	supply	digital ground 1
OTD	12	I	off track detect input
MOTO1	13	O	3-state motor control output
n.c.	14	–	not connected, reserved
MOTO2/T3	15	I/O	motor control output/tachometer 3 input
n.c.	16	–	not connected, reserved
T1	17	I	tachometer 1 input
T2	18	I	tachometer 2 input
V <sub>DDD2</sub>	19	supply	digital supply voltage 2
V <sub>SSD2</sub>	20	supply	digital ground 2
TEST1	21	I	test input 1
TEST2	22	I	test input 2
POR	23	I	power-on reset input
MUXSWICH	24	I	use clock multiplier input
n.c.	25	–	not connected, reserved
CL1	26	O	divided clock output
BCAIN	27	I	BCA input
SDA	28	I/O	sub-CPU I <sup>2</sup> C-bus serial data input/output
SCL	29	I	sub-CPU I <sup>2</sup> C-bus serial clock input
INT	30	O	sub-CPU interrupt output (open-drain)
V <sub>DDD3</sub>	31	supply	digital supply voltage 3
V <sub>SSD3</sub>	32	supply	digital ground 3
da7	33	I/O	sub-CPU data bus bit 7 input/output (parallel)
da6	34	I/O	sub-CPU data bus bit 6 input/output (parallel)
da5	35	I/O	sub-CPU data bus bit 5 input/output (parallel)
n.c.	36	–	not connected, reserved
da4	37	I/O	sub-CPU data bus bit 4 input/output (parallel)
n.c.	38	–	not connected, reserved
da3	39	I/O	sub-CPU data bus bit 3 input/output (parallel)
da2	40	I/O	sub-CPU data bus bit 2 input/output (parallel)

## DSP for CD and DVD-ROM systems

SAA7335

SYMBOL	PIN	TYPE	DESCRIPTION
da1	41	I/O	sub-CPU data bus bit 1 input/output (parallel)
n.c.	42	–	not connected, reserved
da0	43	I/O	sub-CPU data bus bit 0 input/output (parallel)
V <sub>DD4</sub>	44	supply	digital supply voltage 4
V <sub>SS4</sub>	45	supply	digital ground 4
$\overline{\text{WRi}}$	46	I	sub-CPU write enable input (active LOW)
$\overline{\text{RDi}}$	47	I	sub-CPU read enable input (active LOW)
ALE	48	I	sub-CPU address latch enable input
CSi	49	I	sub-CPU chip select input (active HIGH)
STOPCLOCK	50	O	stop clock output
n.c.	51	–	not connected, reserved
V4	52	O	serial subcode output (for CD)
EBUOUT	53	O	digital audio output
SYNC	54	O	I <sup>2</sup> S-bus sector sync output
FLAG	55	O	I <sup>2</sup> S-bus correction flag output
DATA	56	O	I <sup>2</sup> S-bus serial data output
BCLK	57	I/O	I <sup>2</sup> S-bus bit serial clock input/output
WCLK	58	I/O	I <sup>2</sup> S-bus word clock input/output
V <sub>DD5</sub>	59	supply	digital supply voltage 5
V <sub>SS5</sub>	60	supply	digital ground 5
RAMRW	61	O	RAM read/write control output
n.c.	62	–	not connected, reserved
RAMDA7	63	I/O	RAM data bus bit 7 input/output
RAMDA6	64	I/O	RAM data bus bit 6 input/output
RAMDA5	65	I/O	RAM data bus bit 5 input/output
RAMDA4	66	I/O	RAM data bus bit 4 input/output
RAMDA3	67	I/O	RAM data bus bit 3 input/output
RAMDA2	68	I/O	RAM data bus bit 2 input/output
n.c.	69	–	not connected, reserved
RAMDA1	70	I/O	RAM data bus bit 1 input/output
RAMDA0	71	I/O	RAM data bus bit 0 input/output
V <sub>DD6</sub>	72	supply	digital supply voltage 6
V <sub>SS6</sub>	73	supply	digital ground 6
RAMAD0	74	O	RAM address bit 0 output
RAMAD1	75	O	RAM address bit 1 output
RAMAD2	76	O	RAM address bit 2 output
RAMAD3	77	O	RAM address bit 3 output
RAMAD4	78	O	RAM address bit 4 output
RAMAD5	79	O	RAM address bit 5 output
RAMAD6	80	O	RAM address bit 6 output
V <sub>DD7</sub>	81	supply	digital supply voltage 7

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 DSP for CD and DVD-ROM systems

SAA7335

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SYMBOL	PIN	TYPE	DESCRIPTION
V <sub>SSD7</sub>	82	supply	digital ground 7
RAMAD7	83	O	RAM address bit 7 output
RAMAD8	84	O	RAM address bit 8 output
RAMAD9	85	O	RAM address bit 9 output
n.c.	86	–	not connected, reserved
RAMAD10	87	O	RAM address bit 10 output
RAMAD11	88	O	RAM address bit 11 output
RAMAD12	89	O	RAM address bit 12 output
RAMAD13	90	O	RAM address bit 13 output
RAMAD14	91	O	RAM address bit 14 output
V <sub>DDD8</sub>	92	supply	digital supply voltage 8
V <sub>SSD8</sub>	93	supply	digital ground 8
CRIN	94	I	analog crystal input
CROUT	95	O	analog crystal output
CFLG	96	O	correction statistics output
MEAS1	97	O	front-end telemetry output
V <sub>DDD9</sub>	98	supply	digital supply voltage 9
V <sub>SSD9</sub>	99	supply	digital ground 9
V <sub>DDA1</sub>	100	supply	analog supply voltage 1

DSP for CD and DVD-ROM systems

SAA7335

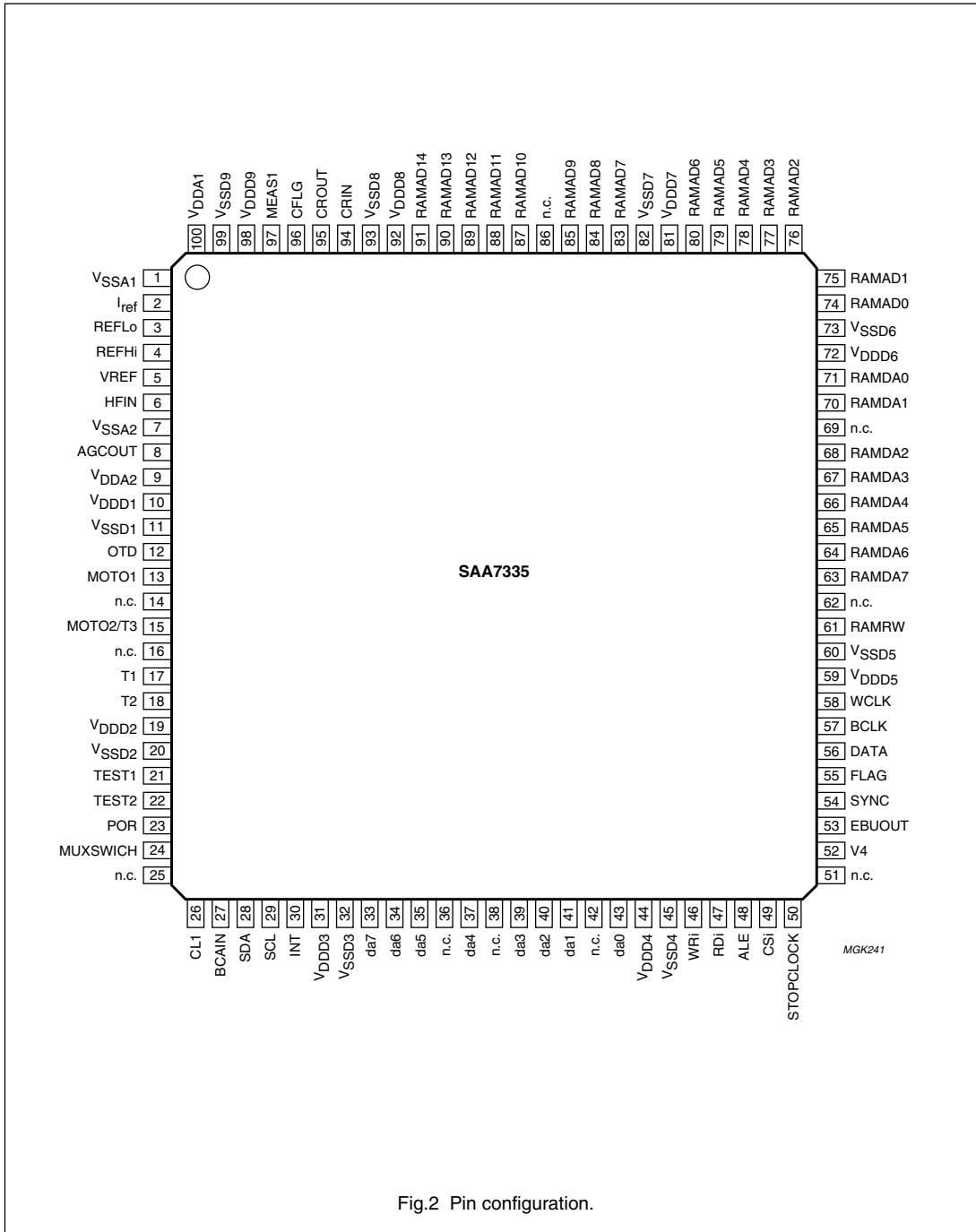


Fig.2 Pin configuration.

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 DSP for CD and DVD-ROM systems
 

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SAA7335

**FUNCTIONAL DESCRIPTION****Analog front-end**

This block converts the HF input to the digital domain using an 8-bit ADC preceded by an AGC circuit to obtain the optimum performance from the convertor. This block is clocked by ADCCLK which is set by the external crystal frequency plus a flexible clock multiplier and divider block.

**PLL and bit detector**

This subsystem recovers the data from the channel stream. The block corrects asymmetry, performs noise filtering and equalisation and finally recovers the bit clock and data from the channel using a digital PLL.

The equalizer and the data slicer are programmable.

**Digital logic**

All the digital system logic is clocked from the master ADC clock (ADCCLK) described above.

**Advanced bit detector**

The advanced bit detector offers improved data recovery for multi-layer discs and contains two extra detection circuits to increase the margins in the bit recovery block:

1. Adaptive slicer: adds a second stage slicer with higher bandwidth
2. Run length 2 push-back: all T2 run lengths are pushed back to T3, thereby automatically determining the erroneous edge and shifting the transitions on that edge.

**Demodulator****FRAME SYNC PROTECTION CD MODE**

This circuit detects the frame synchronization signals. Two synchronization counters are used in the SAA7335:

1. The coincidence counter: this is used to detect the coincidence of successive syncs. It generates a sync coincidence signal if 2 syncs are  $588 \pm 1$  EFM clocks apart.
2. The main counter: this is used to partition the EFM signal into 17-bit words. This counter is reset when:
  - a) A sync coincidence is generated
  - b) A sync is found within  $\pm 6$  EFM clocks of its expected position.

The sync coincidence signal is also used to generate the lock signal which will go active HIGH when 1 sync coincidence is found. It will reset to LOW when, during 61 consecutive frames, no sync coincidence is found.

**FRAME SYNC PROTECTION DVD MODE**

This circuit detects the frame synchronization signals. Two synchronization counters are used in the SAA7335:

1. The coincidence counter: this is used to detect the coincidence of successive syncs. It generates a sync coincidence signal if 2 syncs are  $1488 \pm 3$  EFM+ clocks apart.
2. The main counter: this is used to partition the EFM+ signal into 16-bit words. This counter is reset when:
  - a) A sync coincidence is generated
  - b) A sync is found within  $\pm 10$  EFM+ clocks of its expected position.

The sync coincidence signal is also used to generate the lock signal which will go active HIGH when 1 sync coincidence is found. It will reset to LOW when, during 61 consecutive frames, no sync coincidence is found.

**EFM/EFM+ demodulation**

The 14-bit EFM (16-bit EFM+) data and subcode words are decoded into 8-bit symbols.

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 DSP for CD and DVD-ROM systems
 

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SAA7335

**Microcontroller interface**

The SAA7335 has two microcontroller interfaces, one serial I<sup>2</sup>C-bus and one parallel (8051 microcontroller compatible).

The two communication modes may be operated at the same time, the modes are described below:

1. Parallel mode: protocol compatible with 8052 multiplexed bus:
  - a) da0 to da7 = address/data bus
  - b) ALE = Address Latch Enable, latches the address information on the bus
  - c)  $\overline{WRi}$  = active LOW write signal for write to SAA7335
  - d)  $\overline{RDi}$  = active LOW read signal for read from SAA7335
  - e) CSi = active HIGH Chip Select signal (this signal gates the  $\overline{RDi}$  and  $\overline{WRi}$  signals).
2. I<sup>2</sup>C-bus mode: I<sup>2</sup>C-bus protocol where SAA7335 behaves as slave device where:
  - a) SDA = I<sup>2</sup>C-bus data
  - b) SCL = I<sup>2</sup>C-bus clock
  - c) I<sup>2</sup>C-bus slave address (write mode) = 3EH
  - d) I<sup>2</sup>C-bus slave address (read mode) = 3FH
  - e) Maximum data transfer rate = 400 kbits/s.

**MICROCONTROLLER INTERFACE (I<sup>2</sup>C-BUS MODE)**

Bytes are transferred over the interface in single bytes of which there are two types; write data commands and read data commands.

The sequence for a write data command (1 data byte) is as follows:

- Send START condition
- Send address 3EH (write)
- Write command address byte
- Write data byte
- Send STOP condition.

The sequence for a read data command (that reads 1 data byte) is as follows:

- Send START condition
- Send address 3EH (write)
- Write status address byte
- Send STOP condition
- Send START condition
- Send address 3FH (read)
- Read data byte
- Send STOP condition.

**READING AND WRITING DATA TO THE SAA7335**

The SAA7335 has 32 × 8-bit configuration and status registers as shown in Table 1. Not all locations are currently defined and some remain reserved for future upgrades. These can be written to or read from via the microcontroller interface using either the serial or parallel control bus.



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# Am29LV160BT/Am29LV160BB

## 16 Megabit (2 M x 8-Bit/1 M x 16-Bit) CMOS 3.0 Volt-only Sector Erase Flash Memory

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### DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
    - Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
    - Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
  - **Manufactured on 0.35  $\mu\text{m}$  process technology**
  - **Supports Common Flash Memory Interface (CFI)**
  - **High performance**
    - Full voltage range: access times as fast as 90 ns
    - Regulated voltage range: access times as fast as 80 ns
  - **Ultra low power consumption (typical values at 5 MHz)**
    - 200 nA Automatic Sleep mode current
    - 200 nA standby mode current
    - 10 mA read current
    - 20 mA program/erase current
  - **Flexible sector architecture**
    - One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and thirty-one 64 Kbyte sectors (byte mode)
    - One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
    - Supports full chip erase
    - Sector Protection features:
      - A hardware method of locking a sector to prevent any program or erase operations within that sector
      - Sectors can be locked in-system or via programming equipment
      - Temporary Sector Unprotect feature allows code changes in previously locked sectors
  - **Top or bottom boot block configurations available**
  - **Embedded Algorithms**
    - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
    - Embedded Program algorithm automatically writes and verifies data at specified addresses
  - **Minimum 100,000 write cycle guarantee per sector**
  - **Package option**
    - 48-ball FBGA
    - 48-ball  $\mu\text{BGA}$
    - 48-pin TSOP
    - 44-pin SO
  - **Compatibility with JEDEC standards**
    - Pinout and software compatible with single-power supply Flash
    - Superior inadvertent write protection
  - **Data# Polling and toggle bits**
    - Provides a software method of detecting program or erase operation completion
  - **Ready/Busy# pin (RY/BY#)**
    - Provides a hardware method of detecting program or erase cycle completion (not available on 44-pin SO)
  - **Erase Suspend/Erase Resume**
    - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
  - **Hardware reset pin (RESET#)**
    - Hardware method to reset the device to reading array data
-

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## GENERAL DESCRIPTION

The Am29LV160B is a 16 Mbit, 3.0 Volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words. The device is offered in 48-ball FBGA, 48-ball  $\mu$ BGA, 44-pin SO, and 48-pin TSOP packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed in-system with the standard system 3.0 volt  $V_{CC}$  supply. A 12.0 V  $V_{PP}$  or 5.0  $V_{CC}$  are not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 80, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The Am29LV160B is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically pre-programs the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

**Hardware data protection** measures include a low  $V_{CC}$  detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

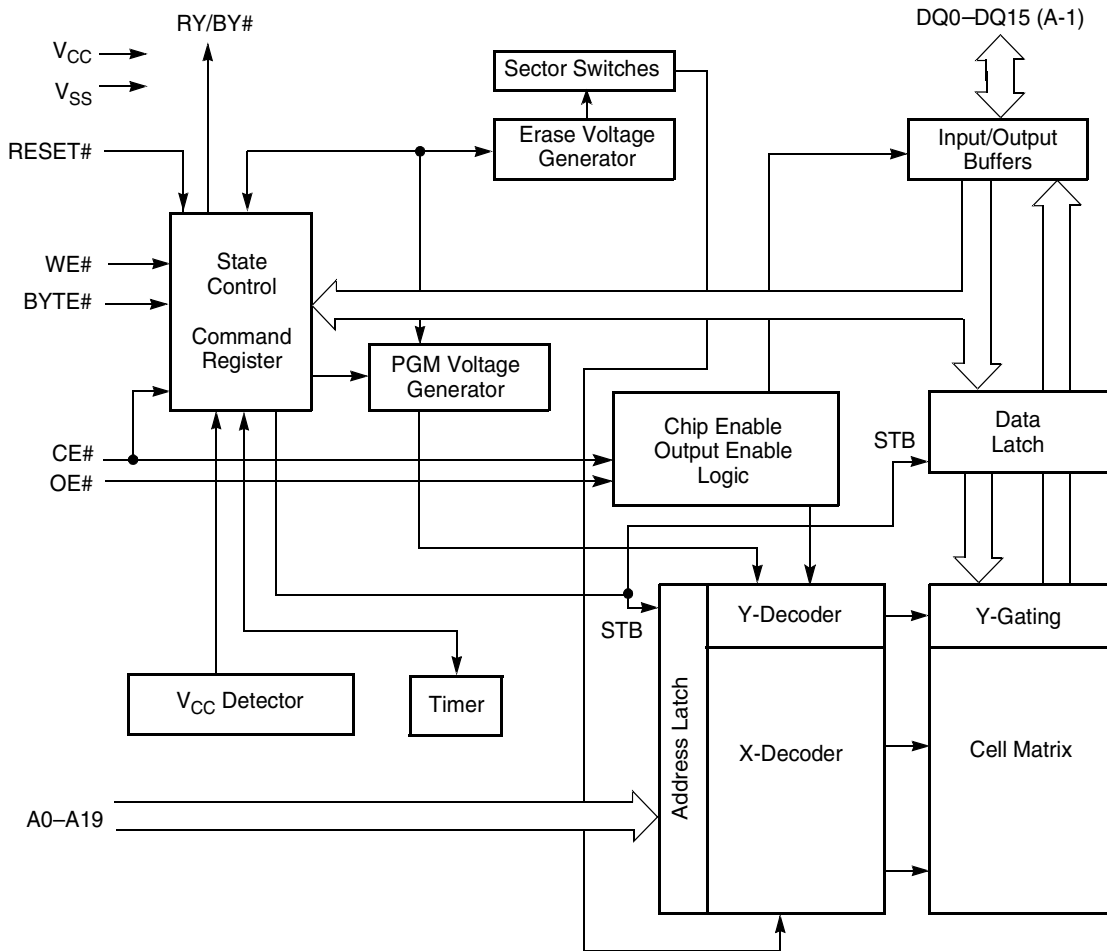
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**PRODUCT SELECTOR GUIDE**

Family Part Number	Am29LV160B		
Ordering Part Number: $V_{CC} = 3.0-3.6\text{ V}$	80R		
$V_{CC} = 2.7-3.6\text{ V}$		90	120
Max access time, ns ( $t_{ACC}$ )	80	90	120
Max CE# access time, ns ( $t_{CE}$ )	80	90	120
Max OE# access time, ns ( $t_{OE}$ )	30	35	50

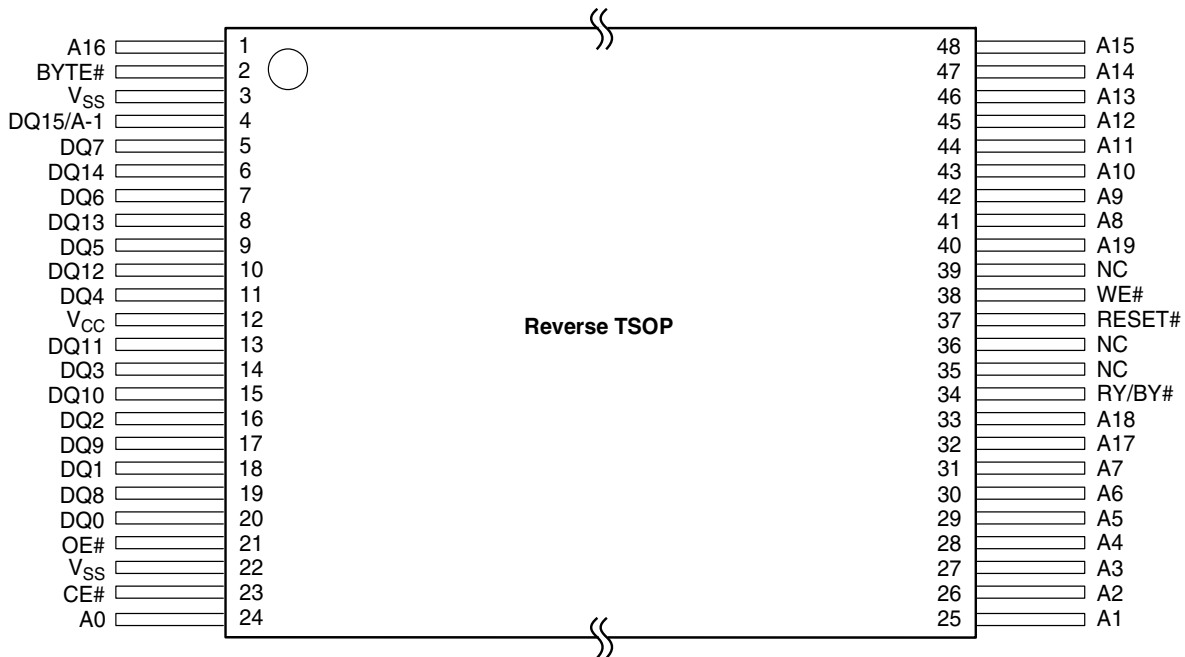
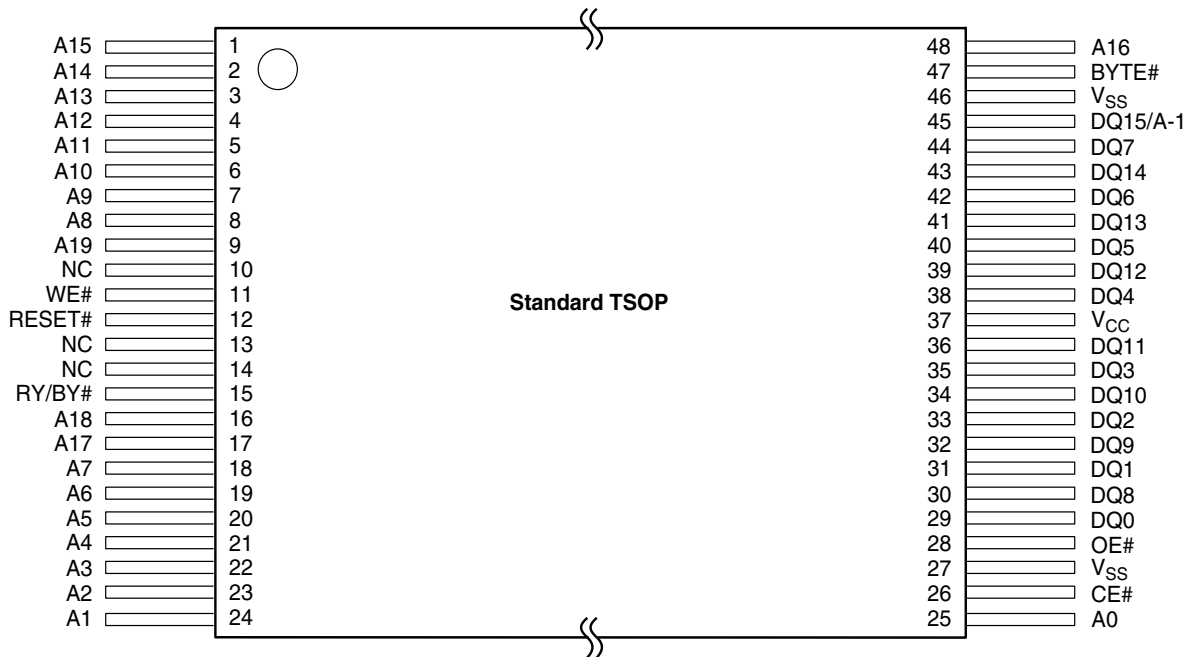
*Note: See "AC Characteristics" for full specifications.*

**BLOCK DIAGRAM**



21358C-1

**CONNECTION DIAGRAMS**



# SYNCHRONOUS DRAM

MT48LC1M16A1 S - 512K x 16 x 2 banks

## FEATURES

- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge  
1 Meg x 16 - 512K x 16 x 2 banks architecture with 11 row, 8 column addresses per bank
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge Mode, includes CONCURRENT AUTO PRECHARGE
- Self Refresh and Adaptable Auto Refresh Modes
  - 32ms, 2,048-cycle refresh or
  - 64ms, 2,048-cycle refresh or
  - 64ms, 4,096-cycle refresh
- LVTTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- Supports CAS latency of 1, 2 and 3

## OPTIONS

- Configuration  
1 Meg x 16 (512K x 16 x 2 banks)
- Plastic Package - OCPL\*  
50-pin TSOP (400 mil)
- Timing (Cycle Time)
  - 6ns (166 MHz)
  - 7ns (143 MHz)
  - 8ns (125 MHz)
- Refresh  
2K or 4K with Self Refresh Mode at 64ms
- Part Number Example: MT48LC1M16A1TG-7S

## MARKING

1M16A1

TG

-6  
-7  
-8A

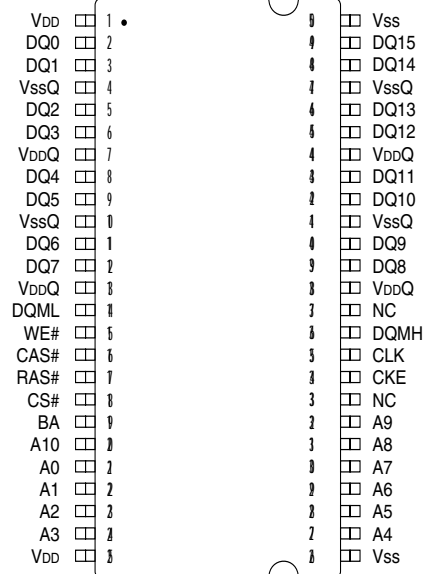
S

## KEY TIMING PARAMETERS

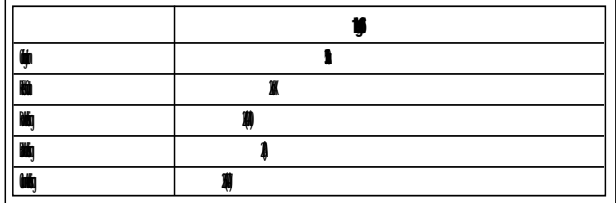
CL	f <sub>max</sub>	t <sub>RC</sub>	t <sub>RD</sub>	t <sub>WR</sub>
-6	166 MHz	5.5ns	2ns	1ns
-7	143 MHz	5.5ns	2ns	1ns
-8A	125 MHz	6ns	2ns	1ns

\*Off-center parting line  
\*\*CL = CAS (READ) latency

## PIN ASSIGNMENT (Top View) 50-Pin TSOP



Note: The # symbol indicates signal is active LOW.



## 16Mb (x16) SDRAM PART NUMBER

MT48LC1M16A1TG S	1 Meg x 16
------------------	------------

## GENERAL DESCRIPTION

The 16Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 16,777,216 bits. It is internally configured as a dual 512K x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 16-bit banks is organized as 2,048 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed

**16Mb: x16  
SDRAM****GENERAL DESCRIPTION (continued)**

sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 1 Meg x 16 SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the  $2n$  rule of prefetch architectures,

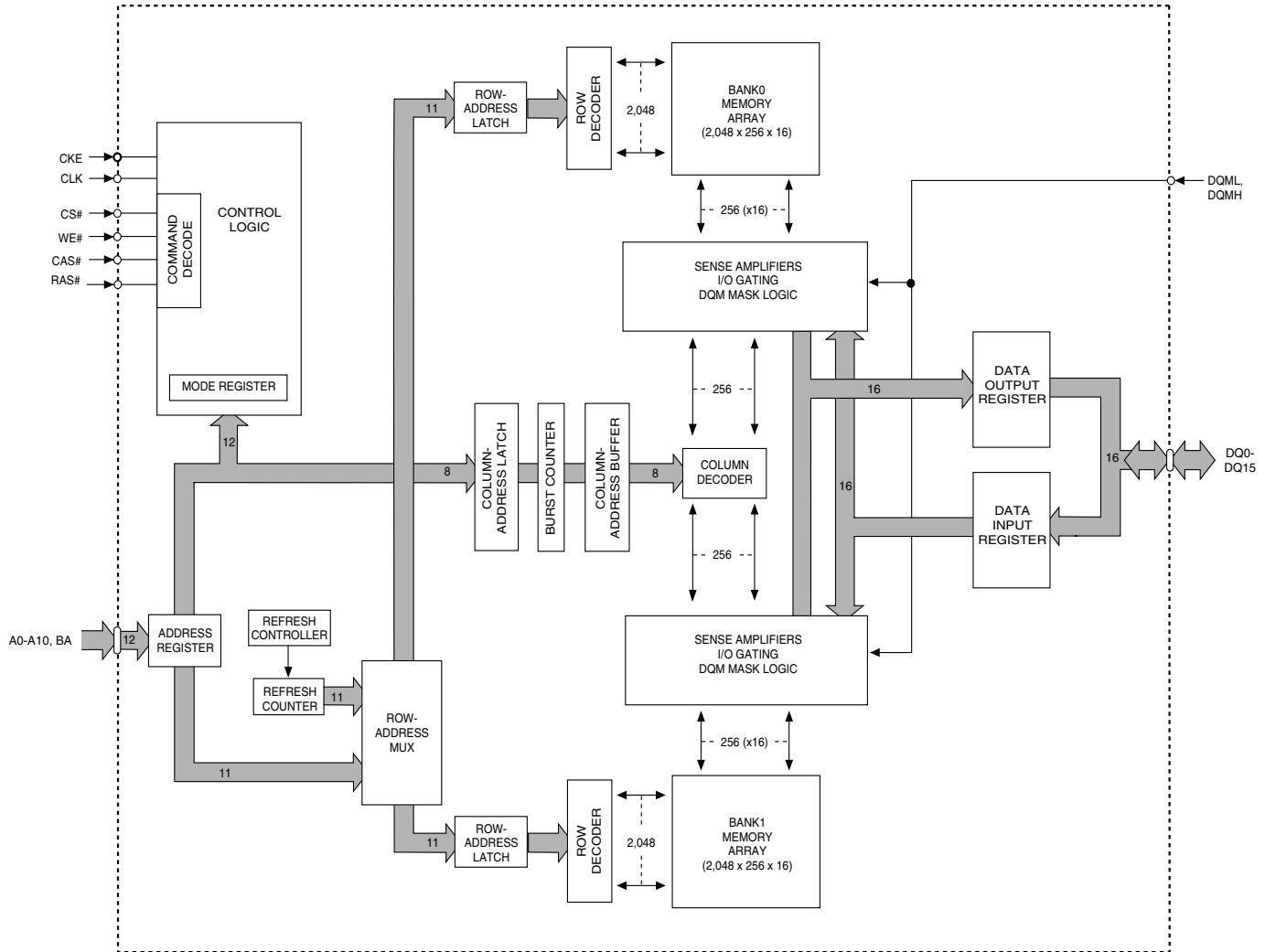
but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 1 Meg x 16 SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

**16Mb: x16  
SDRAM**

**FUNCTIONAL BLOCK DIAGRAM  
1 Meg x 16 SDRAM**



**16Mb: x16  
SDRAM**

## PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
35	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
34	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), ACTIVE POWER-DOWN (row ACTIVE in either bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
18	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
15, 16, 17	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
14, 36	DQML, DQMH	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQML corresponds to DQ0-DQ7; DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
19	BA	Input	Bank Address Inputs: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the twelfth bit of the Mode Register.
21-24, 27-32, 20	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7, with A10 defining AUTO PRECHARGE) to select one location out of the 512K available in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	DQ0-DQ15	Input/Output	Data I/Os: Data bus.
33, 37	NC	–	No Connect: These pins should be left unconnected.
7, 13, 38, 44	V <sub>DDQ</sub>	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
4, 10, 41, 47	V <sub>SSQ</sub>	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 25	V <sub>DD</sub>	Supply	Power Supply: +3.3V ±0.3V.
26, 50	V <sub>SS</sub>	Supply	Ground.



## STi5505 (Rev. Ax)

### DVD BACKEND DECODER WITH INTEGRATED HOST PROCESSOR

PRODUCT PREVIEW

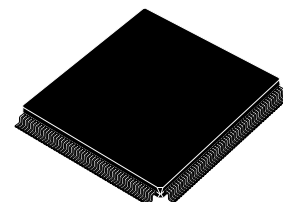
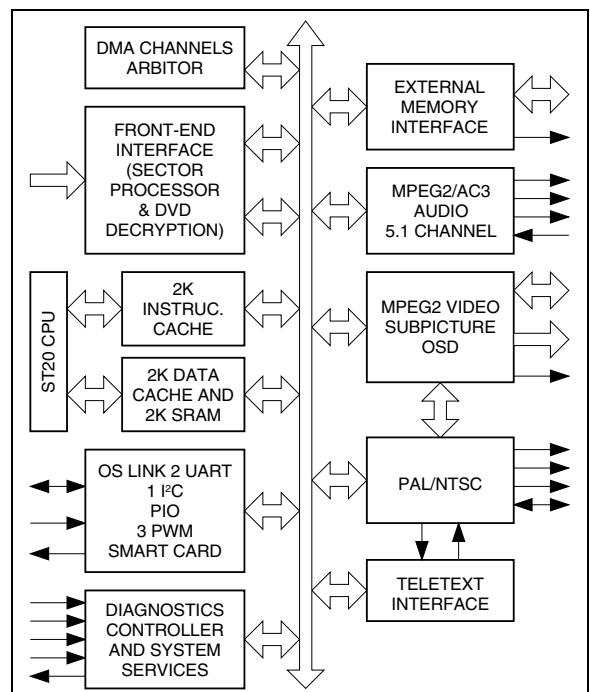
- INTEGRATED 32-BIT RISC HOST CPU
  - 2KBYTES INSTRUCTION CACHE, 2KBYTES DATA CACHE/SRAM
  - 50K DHRYSTONES/SEC (2.1) - 50MHz
- VIDEO DECODER
  - FULLY SUPPORTS MPEG-2 MP@ML
  - MEMORY REDUCTION - PAL IN 12MBITS
- SUBPICTURE DECODER
- HIGH PERFORMANCE ON-SCREEN DISPLAY
- AUDIO DECODER
  - 5.1 CHANNEL DOLBY AC-3® / MULTI CHANNEL MPEG-2 DECODING
  - DOWNMIX TO STEREO OR TO DOLBY PRO-LOGIC COMPATIBLE OUTPUTS FOR MPEG-2 AND AC-3
  - IEC6958 - IEC61937 COMPATIBLE OUTPUT
  - LPCM (DVD) MODE SUPPORTED
  - 6 CHANNELS OUTPUT
- PAL/NTSC ENCODER
  - MACROVISION™ 7.01/6.1 COMPATIBLE
  - TELETEXT, AND CLOSED CAPTION
- HIGH PERFORMANCE SDRAM INTERFACE
- PROGRAMMABLE MEMORY INTERFACE FOR DRAM, ROM, PERIPHERALS ETC.
- FRONT-END CHANNEL IC INTERFACE
  - DVD, VCD AND CD-DA COMPATIBLE
  - DSS - DVB BISTREAMS
  - SERIAL AND PARALLEL INTERFACES
  - HARDWARE SECTOR FILTERING
  - INTEGRATED CSS DECRYPTION AND TRACK BUFFER
- INTEGRATED PERIPHERALS
  - 2 UARTS, 1 I<sup>2</sup>C CONTROLLER, 3 PWM OUTPUTS, 3 TIMERS, 3 CAPTURE TIMERS, SMART CARD
  - 34 BITS OF PROGRAMMABLE I/O
  - OS LINK
- PROFESSIONAL TOOLSET SUPPORT
  - ANSI C COMPILER AND LIBRARIES
  - OPERATING SYSTEMS SUPPORT
  - ADVANCED DEBUGGING TOOLS
- 208 PIN PQFP PACKAGE

#### DESCRIPTION

The STi5505 provides a very highly integrated back-end solution for DVD and combo DVD-DVB (Set Top Box) applications. The STi5505 incorporates a host CPU which handles both general application (DVD navigation, CD-DA, VCD, DVB) and drivers of the different embedded peripherals (audio/video, subpicture decoders, OSD, PAL/NTSC encoder...).

The STi5505 offers one of the best cost-effective (memory savings, internal peripherals availability) solution to DVD-DVB applications with rapid time to market (Reference design, DVD-DVB Software Toolkit).

Figure 1 : General Block Diagram



PQFP208 (Plastic Quad Flat Pack)  
ORDER CODE : STi5505ACV

## I - GENERAL DESCRIPTION

The performance offered by the ST20 CPU and its associated hardware (decoders, encoder, peripherals...) allows an integrated and unified DVD or DVD-DVB software solution.

All the following operations are performed inside the STi5505 :

- application management (DVD Navigation, VCD, CD-DA, DVB-Program Guide ...),
- device data retrieval drivers (demultiplex, stream buffer management ...),
- device presentation drivers (video decoder, sub-picture decoder, on-screen display, audio decoder, PAL/NTSC encoder ...),
- embedded peripherals drivers (UART, I<sup>2</sup>C, Programmable I/O, Smart Card ...).

### I.1 - ST20 32-bit CPU

The ST20 micro-core family has been developed by SGS-THOMSON Microelectronics to provide the tools and building blocks to enable the development of highly integrated application-specific 32-bits device at the lowest cost and fastest time to market.

The STi5505 integrates a ST20 C2 core with the following characteristics :

- 50K Dhrystones/s at 50MHz,
  - 8/16 bits instructions (32 most common instructions in 8 bits),
  - instruction cache 2Kbytes - write back replacement policy,
  - internal SRAM 2Kbytes to ensure fast access to critical code, data, interrupt handler ...
  - data cache 2 Kbytes - write back replacement policy,
- The STi5505's ST20 is provided with advanced debugging tools :

- on-chip real-time emulation,
- debugging with minimal impact on software and performance,
- non intrusive attachment to the host via JTAG (IEEE1149.1),
- no intrusion into the performance of the CPU core,
- no intrusion into user code space by a debug kernel,
- only 40bytes used for breakpoint handler.

### I.2 - Video Decoder

The video decoder implemented in the STi5505 uses a patented memory reduction/bandwidth reduction scheme to offer the user the best band-

width/memory size compromise.

The algorithm is lossless and uses "on-the-fly" decoding to reduce the memory requirements to two frame buffers in memory reduction mode.

In this mode, PAL decoding is contained in 12Mbits. When used in bandwidth reduction mode, the memory usage is the normal three buffers but the bandwidth required by the decoder is significantly reduced compared to a classical implementation.

In summary, the features of the decoder are :

- MPEG-2 Main Profile/Main Level (MP@ML) support,
- MPEG-2 program streams, Packet Elementary streams and MPEG-1 system streams support,
- memory reduction architecture allowing sharing of single 16 Mbits SDRAM between MPEG decoding, micro and transport functions - memory expandable to 32 Mbits of SDRAM,
- letter box (16:9) filter,
- pan-scan, horizontal and vertical image resizing,
- automatic error concealment.

### I.3 - Subpicture Decoder

The STi5505 has a hardware DVD compliant subpicture decoder. Subpicture units are copied by DMA into subpicture bit buffer.

The subpicture decoder can decode complete subpicture units without any interaction from the ST20.

The main subpicture decoder features are :

- up to 720x480 or 720x576 subpicture area,
- internal LUTs for Sub Picture, Highlight and PCI (4 bits color and contrast outputs),
- internal color LUT (4 bits from SP, HL, PCI to 24 Y,Cr,Cb bits) for SP color inputs to MPEG, OSD, SP mixer.

### I.4 - Audio Decoder

The audio decoder cell is a fully compatible Dolby AC-3™ / MPEG-1/MPEG-2 decoder capable of decoding both 5.1 and 2 channel streams compatible with the DVD standard.

Downmix from 5.1 channels is supported for both Dolby and MPEG-2 streams. The output can be sent directly to external DACs or formatted for transmission in accordance with the IE6958 standard.

The decoder can also handle linear PCM in accordance with the DVD standard. An integrated downsampler is provided for conversion from 96 kHz to 48kHz.

## STi5505 (Rev. Ax)

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### I - GENERAL DESCRIPTION (continued)

The main features of the decoder core are :

- Decodes 5.1 Dolby AC-3 Digital surround,
- Output to 6 channels. Downmix modes : 1, 2, 3 or 4 channels for MPEG and AC-3 streams,
- Karaoke mode for DVD. MPEG-2 capable, AC-3 capable,
- MPEG-1, 2-channel audio decoder layers 1 and 2,
- MPEG-2, 6-channel audio decoder layer 2,
- PCM : transparent. downsampling 96 to 48 kHz,
- Accepts MPEG-2 PES stream format for : MPEG-2, MPEG-1, Dolby AC-3 and Linear PCM,
- IEC6958 Output Interface,
- CD-DA PCM format (subcode output in IEC6958 user data),
- Downmix for Dolby Pro Logic compatible outputs for AC-3 and MPEG-2 (Pro Logic encoder),
- Pro Logic decoder,
- PLL for Internal 44.1 and 48kHz PCM clock generation,
- On chip pink noise generator.

#### I.5 - High Performance On-Screen Display

The graphics performance of the STi5505 supports the new requirements for intelligent program guides and interactive applications.

The display interface supports up to 256 colors for each OSD region and a transparency feature allows mixing of video with the OSD. Fast access graphics and many other additional features are available and are supported by a graphics library.

Very high system performance is obtained by closely coupling the ST20 RISC processor and cache with the MPEG audio/video core and display memory.

Low latency RISC access and DMA engines allow rapid construction of bit maps.

#### I.6 - PAL/NTSC Encoder

The STi5505 integrates a PAL/NTSC encoder. It converts the digital MPEG/Sub Picture/OSD stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. Six analog output pins are available on which it is possible to output CVBS, S-VHS (Y/C) and RGB formats.

The encoder handles interlaced and non-interlaced mode.

It can perform Closed Captions, CGMS or Teletext encoding and allows Macrovision 7.01/6.1 copy protection.

The encoder supports both master and slave modes for synchronization.

#### I.7 - Memory Interfaces

The STi5505 has been designed to minimize system costs by enabling various memory savings. Two kinds of memory interfaces are used on the STi5505 : a programmable External Memory Interface (EMI) and a high performance SDRAM interface.

The External Memory Interface supports several address ranges (memory banks). In each bank, a set of signals are entirely programmable and can be used to map 8/16 bits peripherals such as Front End channel ICs in DVD applications.

The EMI contains a zero glue logic DRAM and a low-cost EPROM interface.

This interface can be programmed to interface very easily peripherals.

The SDRAM memory interface supports gluelessly 125 MHz SDRAMs providing the adequate bandwidths to achieve MPEG decoding and display, OSD drawing and display, and general system use.

Memory savings can be realized on ROM requirements too : the ST20 VL-RISC micro-core has the highest code density of any 32 bit CPU, leading to the lowest cost program ROM.

#### I.8 - Front-End Interface

The STi5505 's front end interface accepts :

- DVD, VCD and CD-DA sectors,
- DVB-DSS transport stream.

In DVD mode, DVD, VCD and CD-DA information can be input into STi5505 through a serial interface or a generic parallel interface.

In serial mode, data are captured and filtered from I2S and V4 interfaces by an internal sector processor. V4 interface is used to capture VCD and CD-DA subcode information. In parallel mode, sector processor is bypassed.

**I - GENERAL DESCRIPTION** (continued)

The main features of the DVD interface are :

- DVD, VCD and CD-DA compatible,
- hardware sector filtering,
- subcode error correction for CD-DA,
- integrated CSS decryption,
- integrated track buffer support,
- DMA engine to ST20 memory.

In DVB-DSS mode, DVB-DSS transport stream is input through a serial interface. The STi5505 extracts and descrambles Packet Elementary Streams belonging to one user selected program to be decoded and presented.

The main features of the DVB-DSS interface are :

- descrambling (transport packet and packet elementary streams in DVB mode, transport packet in DSS mode ; up to 32 streams descrambling),
- PID and section filtering,
- clock recovery,
- DMA engine.

In DVB-DSS mode, a high speed digital interface

allows to transfer packets between the Set Top Box and external units, either for recording or playback purposes. This interface provides also full support for an external IEEE1394 connection.

**I.9 - Integrated Peripherals**

Several peripherals generally used in DVD players or DVD-DVB combos have been integrated into the STi5505.

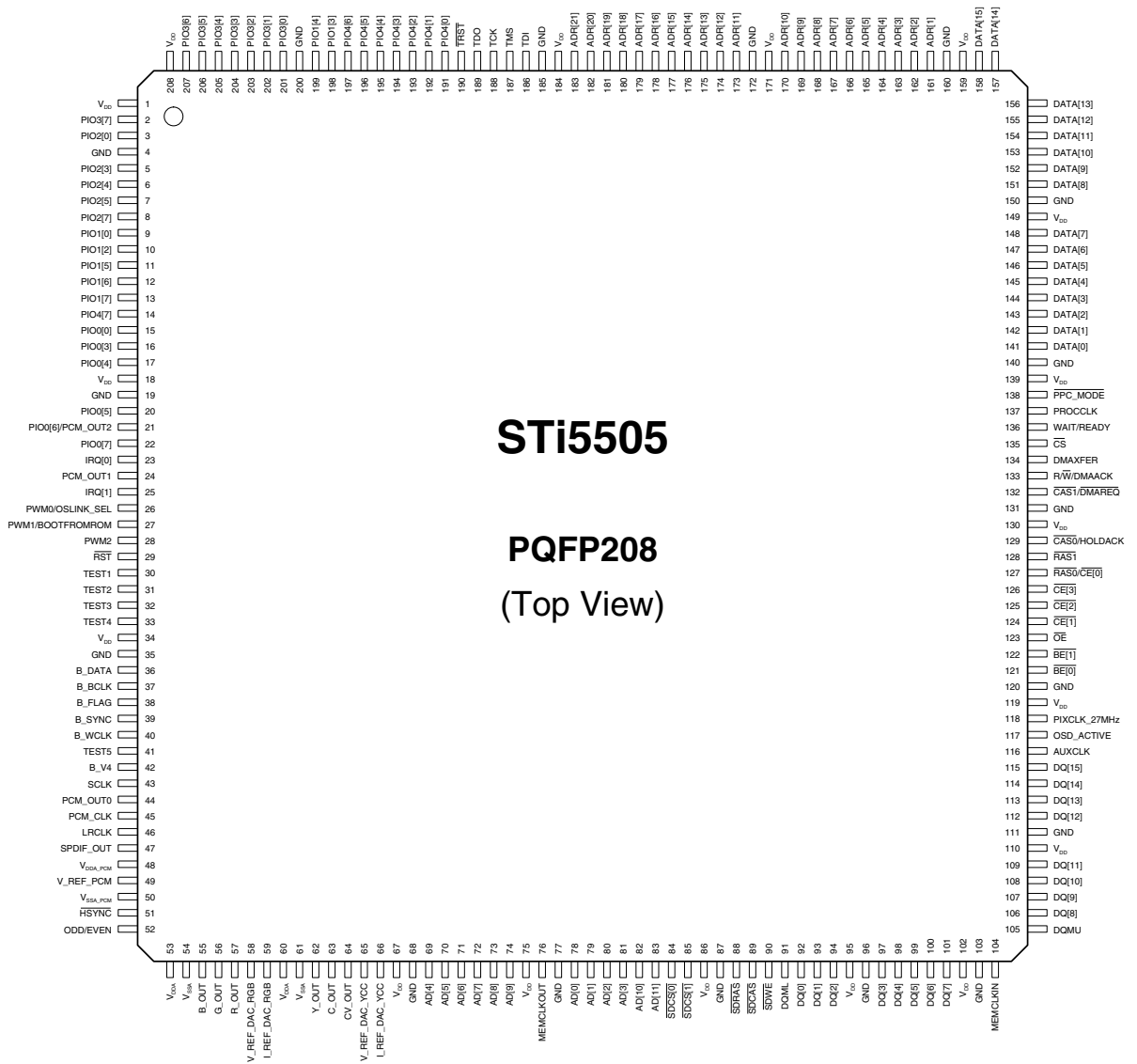
They are :

- two UARTs to interface remote control receivers, DVD front end, modem ...,
  - one I<sup>2</sup>C controller to interface serial memories, remote control receivers, microcontrollers...,
  - 2 SmartCard interfaces (ISO7816-3) for DVB-DSS conditionnal access, pay per view ...,
  - PWM/timer module for control of system clock,
  - 34 programmable I/O pins,
  - OS Link interface,
  - JTAG with boundary scan for debug.
-

STi5505 (Rev. Ax)

II - PIN DESCRIPTION

II.1 - Pin Connections



## II - PIN DESCRIPTION (continued)

## II.2 - Pin List

Pin	Name	Type	Function
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## SUPPLIES

1, 18, 34, 67, 75, 86, 95, 102, 110, 119, 130, 139, 149, 159, 171, 184, 208	V <sub>DD</sub>		Power Supply
4, 19, 35, 68, 77, 87, 96, 103, 111, 120, 131, 140, 150, 160, 172, 185, 200	GND		Ground
53, 60	V <sub>DDA</sub>		Analog Power Supply for DENC D/A Converters
54, 61	V <sub>SSA</sub>		Analog Ground for DENC D/A Converters
48	V <sub>DDA_PCM</sub>		Analog Power Supply for PLL PCM
49	V <sub>REF_PCM</sub>		Analog Reference for PLL PCM
50	V <sub>SSA_PCM</sub>		Analog Ground for PLL PCM

## FRONT-END INTERFACE

36	B_DATA	I	I <sup>2</sup> S Data (DVD) or PARA_DATA[2] (DVD//) or Link Data (DVB/DSS)
40	B_WCLK	I/O	I <sup>2</sup> S Word Clock or PARA_DATA[6] (DVD//) or NRSS_CLK (DVB/DSS)
37	B_BCLK	I	I <sup>2</sup> S Bit Clock (DVD) or PARA_DATA[3] (DVD//) or Link Bit Clock (DVB/DSS)
38	B_FLAG	I	Error Flag (DVD) or PARA_DATA [4] (DVD//) or Link Sync (DVB/DSS)
39	B_SYNC	I	Sector / Abs Time Sync (DVD) or PARA_DATA[5] (DVD//) or Link Not Valid (DVB/DSS)
42	B_V4	I	Versatile Input Pin (Subcode Input) or PARA_DATA[7] (DVD//) or NRSS_IN (DVB/DSS)

## VIDEO OUTPUT INTERFACE

57	R_OUT	O	Red Output
56	G_OUT	O	Green Output
55	B_OUT	O	Blue Output
63	C_OUT	O	Chroma Output
64	CV_OUT	O	Composite Video Output
62	Y_OUT	O	Luma Output
59	I_REF_DAC_RGB	I	DAC Current Reference
66	I_REF_DAC_YCC	I	DAC Current Reference
58	V_REF_DAC_RGB	I	DAC Voltage Reference
65	V_REF_DAC_YCC	I	DAC Voltage Reference
117	OSD_ACTIVE	I/O	OSD Active
118	PIXCLK_27MHz	I	System Clock Input
51	HSYNC	I/O	Horizontal Sync
52	ODD/EVEN	I/O	Vertical Sync

## AC-3/MPEG1-2 AUDIO OUTPUT INTERFACE

43	SCLK	O	Serial Bit Clock
44	PCM_OUT0	O	Audio Serial Output Data 0
24	PCM_OUT1	O	Audio Serial Output Data 1
21	PCM_OUT2	O	Audio Serial Output Data 2
45	PCM_CLK	I/O	PCM Clock In or Out
46	LRCLK	O	Left/Right Clock
47	SPDIF_OUT	O	SPDIF Output

**STi5505 (Rev. Ax)****II - PIN DESCRIPTION** (continued)**II.2 - Pin List** (continued)

Pin	Name	Type	Function
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## EXTERNAL INTERRUPTS

23, 25	IRQ[0:1]	I	External Interrupts
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## PROGRAMMABLE I/O AND ALTERNATE FUNCTION (see Device Configuration Chapter)

15	PIO0 [0]	I/O	General Purpose I/O or PARA_SYNC (DVD//Front End) or Sc1Data (Smart Card 1 Data I/O)
16	PIO0 [3]	I/O	General Purpose I/O or PARA_REQ (DVD//Front End) or Sc1Clk (Smart Card 1 Clock)
17	PIO0 [4]	I/O	General Purpose I/O or PARA_STR (DVD//Front End) or Sc1RST (Smart Card 1 Reset)
20	PIO0 [5]	I/O	General Purpose I/O or PARA_DATA[0] (DVD//Front End) or Sc1Cmd V <sub>CC</sub> (Smart Card 1 Voltage Enable)
21	PIO0 [6]	I/O	General Purpose IO or Sc1DataDir (Smart Card 1 Dir)
22	PIO0 [7]	I/O	General Purpose I/O or PARA_DATA[1] (DVD//Front End) or Sc1Detect(Smart Card 1 Detect)
9	PIO1 [0]	I/O	General Purpose I/O or I <sup>2</sup> C Data
10	PIO1 [2]	I/O	General Purpose I/O or I <sup>2</sup> C Clock
198, 199	PIO1 [3:4]	I/O	General Purpose IO
11	PIO1 [5]	I/O	General Purpose IO or ASC1 TXD
12	PIO1 [6]	I/O	General Purpose IO or ASC1 RXD
13	PIO1 [7]	I/O	General Purpose IO or ASC3 TXD
3	PIO2 [0]	I/O	General Purpose I/O or Sc0Data (Smart Card 0 Data I/O)
5	PIO2 [3]	I/O	General Purpose I/O or Sc0Clk (Smart Card 0 Clock)
6	PIO2 [4]	I/O	General Purpose I/O or Sc0RST (Smart Card 0 Reset)
7	PIO2 [5]	I/O	General Purpose I/O or Sc0CmdV <sub>CC</sub> (Smart Card 0 Voltage Enable)
8	PIO2 [7]	I/O	General Purpose I/O or Sc0Detect (Smart Card 0 Detect)
201	PIO3 [0]	I/O	General Purpose IO or OSLink In
202	PIO3 [1]	I/O	General Purpose IO or OSLink Out
203	PIO3 [2]	I/O	General Purpose IO or CPUReset
204	PIO3 [3]	I/O	General Purpose IO or CPU Analyse
205	PIO3 [4]	I/O	General Purpose IO or ErrorOut
206, 207, 2	PIO3 [5:7]	I/O	General Purpose IO
191-197	PIO4 [0:6]	I/O	General Purpose IO
14	PIO4 [7]	I/O	General Purpose IO or ASC3 RXD

## JTAG INTERFACE

188	TCK	I	Test Clock
186	TDI	I	Test Data Input
189	TDO	O	Test Data Input
187	TMS	I	Test Mode Select
190	TRST	I	Test Reset

## SYSTEM USE

28	PWM2	O	PWM2 Output
27	PWM1/BOOTFROMROM	O/I	PWM1 Output or Configuration Oslink Pins
26	PWM0/OSLINK_SEL	O/I	PWM0 Output or Boot from ROM during Reset
29	RST	I	Reset
116	AUXCLK	O	Auxiliary Clock for Any Purpose

## II - PIN DESCRIPTION (continued)

## II.2 - Pin List (continued)

Pin	Name	Type	Function
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## SDRAM INTERFACE

78-81, 69, 70-74, 82, 83	AD[0:11]	O	SDRAM Address Bus
92-94, 97-101, 106-109, 112-115	DQ[0:15]	I/O	SDRAM Data (Lower Byte)
84, 85	$\overline{\text{SDCS}}[0:1]$	O	SDRAM Chip Selects
89	$\overline{\text{SDCAS}}$	O	SDRAM CAS
88	$\overline{\text{SDRAS}}$	O	SDRAM RAS
90	$\overline{\text{SDWE}}$	O	SDRAM Write Enable
104	MEMCLKIN	I	SDRAM Memory Clock Input
76	MEMCLKOUT	O	SDRAM Memory Clock Output
91	DQML	O	DQ Mask Enable (Lower)
105	DQMU	O	DQ Mask Enable (Upper)

## EXTERNAL MEMORY INTERFACE

161-170, 173-183	ADR[1:21]	I/O	External Memory Address Bus
141-148, 151-158	DATA[0:15]	I/O	External Memory Data Bus
128	$\overline{\text{RAS1}}/\text{HOLDREQ}$	O	DRAM RAS or reserved
136	$\overline{\text{WAIT}}/\text{READY}$	I/O	External Wait States or Reserved
133	$\overline{\text{R}}/\overline{\text{W}}/\text{DMAACK}$	I/O	DRAM R/W Strobe or Reserved
121, 122	$\overline{\text{BE}}[0:1]$	O	Byte enable
129	$\overline{\text{CAS0}}/\text{HOLDACK}$	O/I	DRAM CAS or Reserved
132	$\overline{\text{CAS1}}/\text{DMAREQ}$	O	DRAM CAS or Reserved
124-126	$\overline{\text{CE}}[1:3]$	O	Chip Select for Banks 1 - 3
135	$\overline{\text{CS}}$	I	Reserved
137	$\overline{\text{PROCCLK}}$	I/O	ST20 Clock or Reserved
127	$\overline{\text{RAS0}}/\overline{\text{CE0}}$	O	DRAM RAS or Chip Select for Bank 0
134	$\overline{\text{DMA}}/\overline{\text{FER}}$	I	Reserved
138	$\overline{\text{PPC\_MODE}}$	I	Reserved
123	$\overline{\text{OE}}$	I/O	Output Enable or Reserved

## SDAV/P1394 INTERFACE

30	TEST1	I/O	DATA_RX/STROBE_TX (SDAV Mode) or SDAV_CLK (P1394 Mode)
31	TEST2	I/O	STROBE_RX/DATA_TX (SDAV Mode) or DATA_IN/DATA_OUT (P1394 Mode)
32	TEST3	I/O	Direction (SDAV Mode) or DATA_VALID In/Out (P1394 Mode)

## MISCELLANEOUS

41	TEST5	O	NRSS_OUT (DVB/DSS)
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## STi5505 (Rev. Ax)

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### III - FUNCTIONAL DESCRIPTION

#### III.1 - Functional Modules

Figure 1 shows the subsystem modules that make up the STi5505. These modules are outlined below.

##### III.1.1 - CPU

The Central Processing Unit (CPU) on the STi5505 is the ST20-C2 32-bit processor core. It contains instruction processing logic, instruction and data pointers and an operand register. It directly accesses the high speed on-chip SRAM memory, which can store data or programs, and uses the Caches to reduce access time to off chip program and data memory.

The processor can access memory via the general purpose External Memory Interface (EMI) or via the SDRAM EMI which is shared with the MPEG decoder.

##### III.1.2 - Memory Subsystem

The STi5505 on-chip SRAM memory system provides 160 Mbytes/s internal data bandwidth, supporting pipelined 2 cycles internal memory access at 25ns cycle times. The STi5505 memory system consists of 2 Kbytes of SRAM, 2Kbytes of instruction cache, a 2Kbytes data cache that can be programmed to be SRAM, and an external memory interface (EMI).

The STi5505 product has 2 Kbytes of on-chip SRAM. The advantage of this is the ability to store time critical code on chip, for instance interrupt routines, software kernels or device drivers, and even frequently used data without these being flushed from the caches.

The instruction and data caches are direct mapped with a write-back system for the data cache and support burst accesses to the external memories for refill and write-back which are effective for increasing performance with page-mode and SDRAM memories.

The STi5505 EMI controls access to the external memory and peripherals while the SDRAM EMI provides access to the SDRAM buffer for the MPEG decoders, ST20 and DMA peripherals.

The STi5505 EMI can access a 16 Mbytes (or greater if DRAM is used) physical address space in each of the four general purpose memory banks, and provides sustained transfer rates of up to 80 Mbytes/s. Peripherals that support an asynchronous data acknowledge are supported as is an external Power PC which can share the bus with the STi5505 and access the SDRAM buffer through the device.

High memory bandwidths up to 200 Mbytes/s can be supported by the SDRAM EMI.

The STi5505 internal memory interconnect provides buffering and arbitration of memory access requests to sustain very high throughput of memory accesses.

##### III.1.3 - System Services Module

The STi5505 system services module includes :

- Phase locked loop (PLL) - accepts 27MHz input and generates all the internal high frequency clocks needed for the CPU and the OS-Link.
- test access port - JTAG compatible.
- Diagnostics controller accessed via the JTAG port providing :
  - Bootstrapping during development
  - Hardware breakpoint and watchpoint
  - Real time trace
  - External LSA triggering support.

##### III.1.4 - Serial Communications

To facilitate the connection of this system the front end device and other peripherals, two UARTs (ASCs) are included in the device. The UARTs provide an asynchronous serial interface.

The UART can be programmed to support a range of baud rates and data formats, for example, data size, stop bits and parity. Two synchronous serial communications (SSC) interfaces are provided on the device. These can be used for a remote control device for example via an I<sup>2</sup>C or SPI bus.

##### III.1.5 - Interrupt Subsystem

The STi5505 interrupt subsystem supports eight prioritized interrupt levels. Two external interrupt pins are provided. Level assignment logic allows any of the internal or external interrupts to be assigned and, if necessary, share any interrupt level.

##### III.1.6 - Front End Interface & DVD Decryption

The front end interface accepts sectors in the case of DVD, MPEG-1 system stream in the case of VCD and PCM data for CD-DA applications on an I2S interface. In the case of VCD and CD-DA disks the subcode information is input via a simple asynchronous serial interface similar to a UART.

The bitstream and subcode stream then pass through a "sector processor" block which handles sector filtering in the case of DVD and sectorizing using the subcode stream for VCD and CD-DA systems.

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### III - FUNCTIONAL DESCRIPTION (continued)

The block also handles overspeed processing for all systems. The capturing of CD-DA sectors is based on a flywheel timer to improve robustness by concealing errors in the subcode stream. For DVD the data, having had sector headers removed, then passes through a DVD conformant de-encryption stage and is written into any of the system memories using a programmable DMA engine. When a subcode stream is present it is locally buffered, by subcode block and can be read by the CPU for subsequent processing, if required.

#### III.7 - PWM and counter module

This unit includes three separate pulse width modulator (PWM) generators using a shared counter, and three timer compare and capture channels sharing a second counter.

The counters can be clocked from a pre-scaled internal clock or from a pre-scaled external clock via the capture clock input and the event on which the timer value is captured is also programmable.

The PWM counters are 8-bit with 8-bit registers to set the output high time. The capture/compare counter and the compare and capture registers are 32-bit.

#### III.8 - Parallel Programmable IO module

40 bits of parallel I/O are provided. 34 of them are connected to actual PIO pins. Each bit is programmable as an output or an input. The output can be configured as a totem pole or open drain driver. Input compare logic is provided which can generate an interrupt on any change on any input bit.

Many pins of the STi5505 device are multi-function and can either be configured as PIO or connected to an internal peripheral signal.

#### III.9 - MPEG Video decoder

The video decoder is a real-time video compression processor supporting the MPEG-1 and MPEG-2 standards at video rates up to 720 x 480 x 60 Hz and 720 x 576 x 50 Hz. Picture format conversion for display is performed by vertical and horizontal filters. User-defined bitmaps may be superimposed on the display picture through use of the on-screen display function.

#### III.10 - PAL/NTSC encoder

The digital encoder which is integrated in the STi5505 converts a multiplexed 4:2:2 YUV stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. The encoder can also perform closed-caption, CGMS or teletext encoding

and allows Macrovision™ 7.01/6.1 copy protection.

#### III.11 - MPEG-2 Audio / Dolby AC-3 Decoder

The audio decoder is a Dolby AC-3 decoder capable of decoding both 5.1 and 2 channel DVD conformant bitstreams. The decoder also handles MPEG-1 (layers 1 & 2) and MPEG-2 layer 2 (6 channels). Downmix to 2 channels is possible for Dolby and MPEG standards with optional pro-logic encoding.

The decoder directly accepts MPEG-2 PES streams as input. The decoder is capable of supporting IEC6958-IEC61937 formatted outputs for AC-3 and MPEG audio, linear PCM (left & right, 16, 18, 20 & 24 bits), zero output (Mute mode) and PCM audio.

# ST24E32 ST25E32

## 32K SERIAL I<sup>2</sup>C EEPROM with EXTENDED ADDRESSING

NOT FOR NEW DESIGN

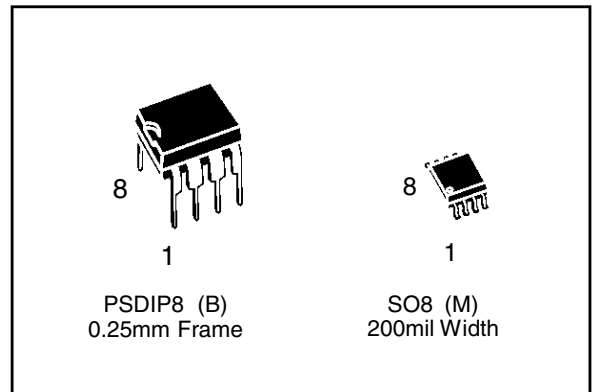
- COMPATIBLE with I<sup>2</sup>C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 1 MILLION ERASE/WRITE CYCLES, OVER the FULL SUPPLY VOLTAGE RANGE
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - ± 4.5V to 5.5V for ST24E32 version
  - ± 2.5V to 5.5V for ST25E32 version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES
- **ST24E32 and ST25E32 are replaced by the M24C32**

### DESCRIPTION

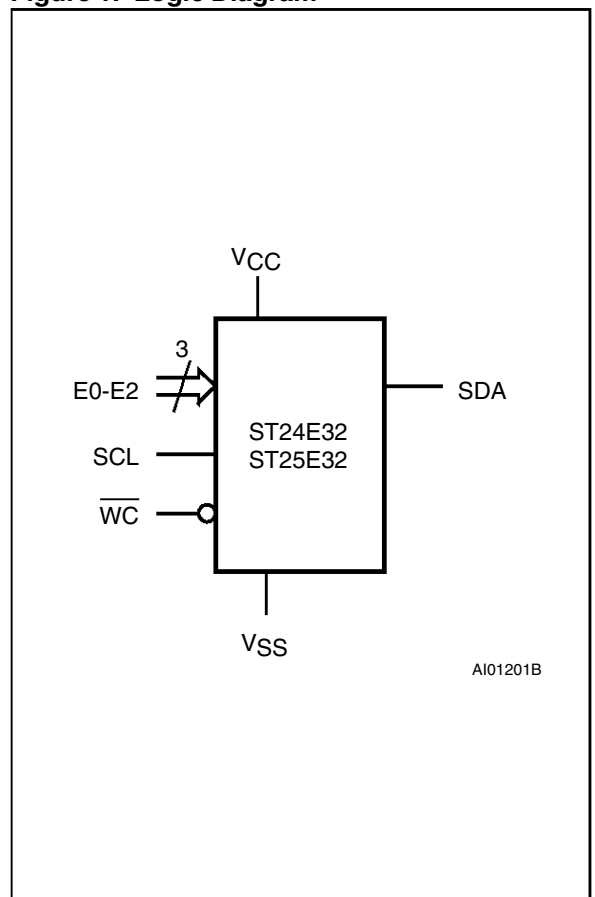
The ST24/25E32 are 32K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 512 x 8 bits. The ST25E32 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

**Table 1. Signal Names**

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{\text{WC}}$	Write Control
V <sub>cc</sub>	Supply Voltage
V <sub>ss</sub>	Ground



**Figure 1. Logic Diagram**



## ST24E32, ST25E32

Figure 2A. DIP Pin Connections

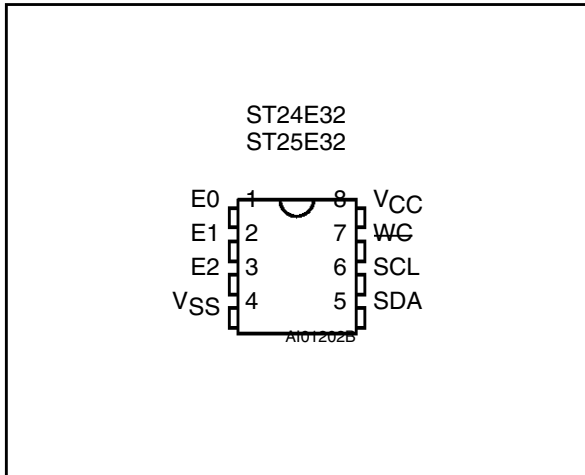


Figure 2B. SO Pin Connections

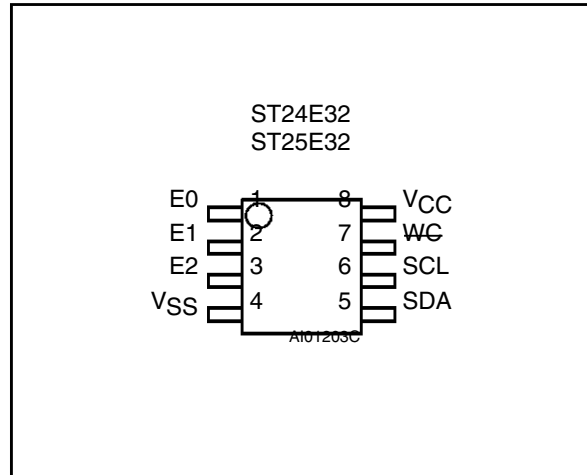


Table 2. Absolute Maximum Ratings <sup>(1)</sup>

Symbol	Parameter	Value	Unit	
T <sub>A</sub>	Ambient Operating Temperature	±40 to 125	°C	
T <sub>STG</sub>	Storage Temperature	±65 to 150	°C	
T <sub>LEAD</sub>	Lead Temperature, Soldering	40 sec 10 sec	215 260	°C
V <sub>IO</sub>	Input or Output Voltages	±0.6 to 6.5	V	
V <sub>CC</sub>	Supply Voltage	±0.3 to 6.5	V	
V <sub>ESD</sub>	Electrostatic Discharge Voltage (Human Body model) <sup>(2)</sup>	4000	V	
	Electrostatic Discharge Voltage (Machine model) <sup>(3)</sup>	500	V	

**Notes:** 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. 100pF through 1500Ω; MIL-STD-883C, 3015.7

3. 200pF through 0Ω; EIAJ IC-121 (condition C)

### DESCRIPTION (cont'd)

Each memory is compatible with the I<sup>2</sup>C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E32 carry a built-in 4 bit, unique device identification code (1010) corresponding to the I<sup>2</sup>C bus definition. The ST24/25E32 behave as

slave devices in the I<sup>2</sup>C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit.





6302	9322 128 69685	S1D
6303	9322 128 69685	S1D
6600	4822 130 11528	1PS76SB10



7100	5322 130 42718	BFS20
7101	5322 130 42718	BFS20
7102	9352 637 37518	
7103	4822 209 17229	BA5938FM
7104	4822 209 30095	LM833D
7105	4822 209 32073	MC34072D
7106	5322 130 42718	BFS20
7109	4822 209 15083	AN78M09
7110	5322 130 60803	BST72A
7111	5322 130 60159	BC846B
7112	5322 130 60159	BC846B
7113	5322 130 60159	BC846B
7114	5322 130 60159	BC846B
7115	4822 130 60373	BC856B
7116	5322 130 60159	BC846B
7201	9351 869 80118	
7202	3104 123 95660	
7203	4822 130 60373	BC856B
7207	9352 636 60557	SAA7399HL/M2A
7304	4822 209 16877	BA6856FP
7310	4822 209 15899	CY7C199-15C
7311	9352 622 13557	SAA7335HL
7312	4822 130 60373	BC856B
7315	5322 130 60159	BC846B
7401	9322 132 01668	AM29LV160B
7404	9322 144 59668	IC SM MT48LC1M16A1TG- 7S (MRN)R
7405	9322 144 59668	IC SM MT48LC1M16A1TG- 7S (MRN)R
7501	5322 130 60159	BC846B
7503	9322 151 16671	IC SM STI5505AVC (ST00) Y
7504	4822 242 10838	27MHZ 120P FX0-31FT
7505	8204 056 05580	IC SM M24C32- WMN6TNKSA
7600	5322 209 71568	PC74HCT14T
7604	5322 130 60159	BC846B
7605	4822 209 17398	LD1117DT33
7607	5322 130 60159	BC846B
7608	4822 130 60373	BC856B
7609	4822 130 60373	BC856B
7610	5322 130 60159	BC846B
7611	9352 456 80115	
7612	5322 130 60159	BC846B
7613	5322 130 60159	BC846B
7614	5322 130 60159	BC846B
7615	5322 130 60159	BC846B
7616	4822 209 16062	MK2742-03S
7617	5322 130 60159	BC846B
7618	5322 130 60159	BC846B
7620	4822 130 60373	BC856B
7621	4822 130 42804	BC817-25

<b>marantz®</b> <b>SERVICE BULLETIN</b>		Date: 16-Mar.-2004	Model: DV4100
		Page: 1 / 1	REF.NBR: MZ04-027
Circulation:		Application:	
x for information customer complaint in case of service mandatory .....		See Below	
		Subject: The improvement of Playability. (A fault phenomenon is nothing).	
		Int.ref:	

**[PHENOMENON]**

A fault phenomenon is nothing.

**[SOLUTION]**

Update the firmware to **Ver 7.27**.

**[NECESSARY PART]**

Update of the firmware disc **\*DV4100CD2**

**[REMARKS]**

The production of DV4100 has been finished.