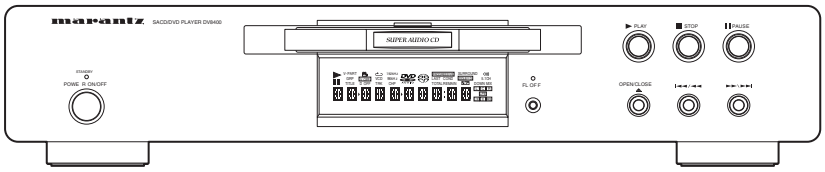
Service Manual

DV8400 /F1N/N1G/S1G /N1S/A1B/F1B/N1B/U1B

Super Audio CD / DVD Player



REMARK:
This service manual shows only the differences between the model DV8300 and the model DV8400.
This unit is a modified version adding DVI-D output, RS-232C control terminal to the DV8300 and making changes that come with the added functions.
All other information is described in the service manual of the model DV8300 (Code number 02AK855010).
For the dispatch of the after-sales service parts, refer to those service manuals with the first priority. Therefore, please use this document with referring to the model DV8300 service manual without fail.

TABLE OF CONTENTS

Please use this service manual with referring to the user guide (D.F.U.) without fail.
修理の際は、必ず取扱説明書を準備し操作方法を確認の上作業を行ってください。

marantz®

DV8400

11AK855010 MIT
First Issue 2003.03

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Using superior design and selected high grade components, **MARANTZ** company has created the ultimate in stereo sound. Only original **MARANTZ** parts can insure that your **MARANTZ** product will continue to perform to the specifications for which it is famous.

Parts for your **MARANTZ** equipment are generally available to our National Marantz Subsidiary or Agent.

ORDERING PARTS :

Parts can be ordered either by mail or by Fax.. In both cases, the correct part number has to be specified.

The following information must be supplied to eliminate delays in processing your order :

1. Complete address
2. Complete part numbers and quantities required
3. Description of parts
4. Model number for which part is required
5. Way of shipment
6. Signature : any order form or Fax. must be signed, otherwise such part order will be considered as null and void.

USA

MARANTZ AMERICA, INC
1100 MAPLEWOOD DRIVE
ITASCA, IL. 60143
USA
PHONE : 630 - 741 - 0300
FAX : 630 - 741 - 0301

EUROPE / TRADING

MARANTZ EUROPE B.V.
P. O. BOX 8744, BUILDING SILVERPOINT
BEEMDSTRAAT 11, 5653 MA EINDHOVEN
THE NETHERLANDS
PHONE : +31 - 40 - 2507844
FAX : +31 - 40 - 2507860

CANADA

LENBROOK INDUSTRIES LIMITED
633 GRANITE COURT,
PICKERING, ONTARIO L1W 3K1
CANADA
PHONE : 905 - 831 - 6333
FAX : 905 - 831 - 6936

PROFESSIONAL **AMERICAS**

SUPERSCOPE TECHNOLOGIES, INC.
MARANTZ PROFESSIONAL PRODUCTS
2640 WHITE OAK CIRCLE, SUITE A
AURORA, ILLINOIS 60504 USA
PHONE : 630 - 820 - 4800
FAX : 630 - 820 - 8103

PROFESSIONAL **AUSTRALIA**

TECHNICAL AUDIO GROUP PTY, LTD
43-53 Bridge Rd.,
STANMORE NSW 2048
AUSTRALIA
PHONE : +61 - (0)2 - 9519 - 0900
FAX : +61 - (0)2 - 9519 - 0600

PROFESSIONAL **HONG KONG**

Jolly ProAudio Broadcast Engineering Ltd.
UNIT 2, 10F, WAH HUNG CENTRE,
41 HUNG TO ROAD, KWUN TONG, KLN.,
HONG KONG
PHONE : 852 - 21913660
FAX : 852 - 21913990

AUSTRALIA

QualiFi Pty Ltd,
24 LIONEL ROAD,
MT. WAVERLEY VIC 3149
AUSTRALIA
PHONE : +61 - (0)3 - 9543 - 1522
FAX : +61 - (0)3 - 9543 - 3677

THAILAND

MRZ STANDARD CO., LTD
746 - 754 MAHACHAI ROAD.,
WANGBURAPAPIROM, PHRANAKORN,
BANGKOK, 10200 THAILAND
PHONE : +66 - 2 - 222 9181
FAX : +66 - 2 - 224 6795

SINGAPORE

WO KEE HONG DISTRIBUTION PTE LTD
130 JOO SENG ROAD
#03-02 OLIVINE BUILDING
SINGAPORE 368357
PHONE : +65 6858 5535 / +65 6381 8621
FAX : +65 6858 6078

NEW ZEALAND

WILDASH AUDIO SYSTEMS NZ
14 MALVERN ROAD MT ALBERT
AUCKLAND NEW ZEALAND
PHONE : +64 - 9 - 8451958
FAX : +64 - 9 - 8463554

TAIWAN

PAI- YUING CO., LTD.
6 TH FL NO, 148 SUNG KIANG ROAD,
TAIPEI, 10429, TAIWAN R.O.C.
PHONE : +886 - 2 - 25221304
FAX : +886 - 2 - 25630415

MALAYSIA

WO KEE HONG ELECTRONICS SDN. BHD.
2ND FLOOR BANGUNAN INFINITE CENTRE
LOT 1, JALAN 13/6, 46200 PETALING JAYA
SELANGOR DARUL EHSAN, MALAYSIA
PHONE : +60 - 3 - 7954 8088
FAX : +60 - 3 - 7954 7088

JAPAN *Technical*

MARANTZ JAPAN, INC.
35- 1, 7- CHOME, SAGAMIONO
SAGAMIHARA - SHI, KANAGAWA
JAPAN 228-8505
PHONE : +81 42 748 1013
FAX : +81 42 741 9190

日本マランツ株式会社

本　社　〒228-8505
神奈川県相模原市相模大野7-35-1

KOREA

MK ENTERPRISES LTD.
ROOM 604/605, ELECTRO-OFFICETEL, 16-58,
3GA, HANGANG-RO, YONGSAN-KU, SEOUL
KOREA
PHONE : +822 - 3232 - 155
FAX : +822 - 3232 - 154

SHOCK, FIRE HAZARD SERVICE TEST :

CAUTION : After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins (with unit NOT connected to AC mains and its Power switch ON), and the face or Front Panel of product and controls and chassis bottom.

Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before it is return to the user/customer.

Ref. UL Standard No. 1492.

In case of difficulties, do not hesitate to contact the Technical Department at above mentioned address.

1. TECHNICAL SPECIFICATIONS

General

System..... DVD-Video, DVD-Audio, DVD-R/RW, Video-CD, SACD, CD and MP3 files

Power requirements

- A Version ..... AC 240 V, 50 Hz
- C Version ..... AC 220 V, 60 Hz
- F Version..... AC 100 V, 50 / 60 Hz
- K Version ..... AC 220 V, 50 Hz
- L Version..... AC 110 V, 60 Hz
- N Version ..... AC 230 V, 50 Hz
- S Version ..... AC 230 V, 50 / 60 Hz
- U Version ..... AC 120 V, 60 Hz

Power consumption

- F Version..... 18 W
- Other Version..... 19 W

Weight ..... 6.5 kg (13 lb 44 oz)

Dimensions.....440 (W) x 311 (D) x 89 (H) mm (17 5/16 (W) x 12 1/4 (D) x 3 1/2 (H) in.) (Not including protruding cables, etc.)

Operating temperature .....+5 °C to +35 °C (+41 °F to +96 °F)

Operating humidity .....5% to 85% (no condensation)

S-Video output

Y (luminance) - Output level ..... 1 Vp-p (75 Ω)

C (color) - Output level : NTSC..... 286 mVp-p (75 Ω)

: PAL ..... 300 mVp-p (75 Ω)

Jacks .....S-VIDEO jack

Video output (2 individual outputs)

Output level..... 1 Vp-p (75 Ω)

Jacks ..... RCA jack

Component video output (Y, C_B/P_B, C_R/P_B)

Output level..... Y : 1.0 Vp-p (75 Ω)

C_B/P_B, C_R/P_B : 0.7 Vp-p (75 Ω)

Jacks ..... RCA jack

R / G / B output

Output level.....R / G / B : 0.7 Vp-p (75 Ω)

Jacks (N Version)..... 21 pin SCART connector

D1/D2 video output (except for N, U Version)

Output level..... Y : 1.0 Vp-p (75 Ω)

C_B/P_B, C_R/P_B : 0.7 Vp-p (75 Ω)

Jacks ..... D terminal

DVI-D output

Jacks .....DVI-D 24 pin

The interface is based on TMDS(Transition Minimized Differential Signaling) tecnologe.

Audio output (2 individual outputs)

Output level

During audio output ..... 200 mVrms (1 kHz, –20 dB)

Number of channels 2

Jacks ..... RCA jack

Audio output (multi-channel / L, R, C, SW, LS, RS)

Output level

During audio output ..... 200 mVrms (1 kHz, –20 dB)

Number of channels 6

Jacks ..... RCA jack

Digital audio characteristics

Frequency response.....4 Hz to 44 kHz (DVD fs: 96 kHz) 4 Hz to 88 kHz (DVD-Audio fs: 192 kHz)

S/N ratio..... more than 125 dB

Dynamic range ..... more than 110 dB

Total harmonic distortion .....0.00095 %

Wow and flutter..... Limit of measurement(0.001% W. PEAK) or lower

Digital output

Optical digital output..... Optical digital jack

Coaxial digital output ..... RCA jack

Accessories

Audio/Video cord 1

System Control cord.....1

Power Cord.....1

Remote control unit 1

AA (R6P) dry cell batteries.....2

Operating Instructions 1

Notification

Concerning HDCP compatible DVI-D output

This product is equipped with an HDCP compatible DVI-D output terminal, but its output format is not formally authorized at this time for copyright protection reasons.

Therefore, when it is shipped, this output is not possible. When the format has been formally authorized, an upgrade will provide compatibility necessary to perform this output.

お知らせ

HDCP 対応 DVI-D 出力について

本製品には HDCP 対応 DVI-D 出力端子を備えておりますが、この出力フォーマットは著作権保護の立場から現時点に於いては正式に許可されていません。

従いまして出荷時点では出力できない状態になっています。正式に許可され次第、アップグレードにて出力できるように対応する予定です。

3. INFORMATIONS

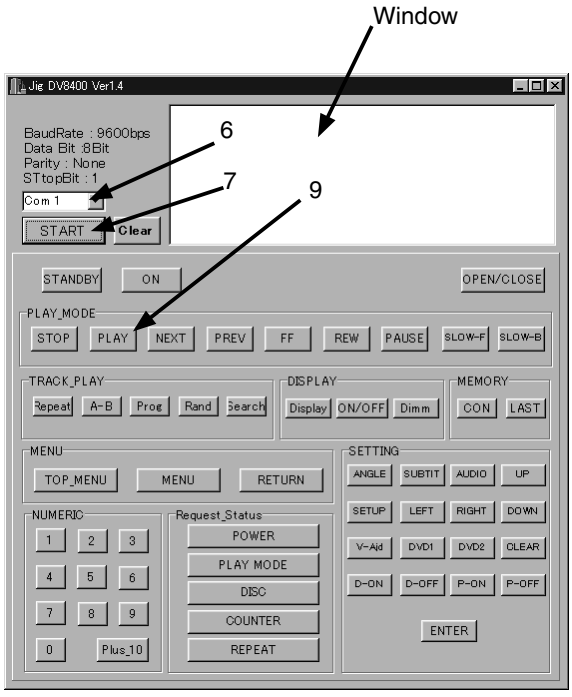
HOW TO CONFIRM THE RS-232C CONTROL FUNCTION

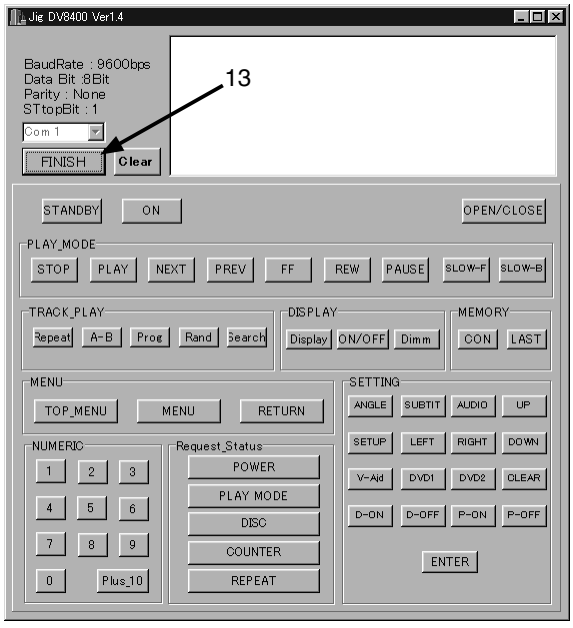
Necessary Equipment

- Windows PC
- RS-232C straight cable female-female
- Function check software (*DV8400RSR)

Operation procedure

1. Connect the RS-232C cable to the RS-232C connector on the rear panel of DV8400.
2. Turn on power of DV8400 and insert a CD disc.
3. Copy "232C_CONTROL" folder in (*DV8400RSR) to the PC.
4. Open the (*DV8400RSR) folder just copied to the PC.
5. Double click "Jig_DV8400_14.exe" to launch this communication software.
6. Select the COM port. (Ex. **Com1**)
7. Click "**START**".
8. Set the RS-232C CONTROL SW on the rear panel of DV8400 to RS-232C.
9. Click "**PLAY**" on the communication software in the PC.
10. If DV8400 turns into PLAY mode and time counter is indicated in window, this function check is OK.
11. Press STOP button.
12. Set the RS-232C CONTROL SW on the rear panel of DV8400 to RC-5/6.
13. Click "**FINISH**" on the communication software.
14. This function check is completed.





DVI

DVI is an abbreviation of Digital Visual Interface.
It is a digital display interface standard decided by DDWG (Digital Display Working Group). This standard is to transmit video signal in digital.

HDCP

HDCP is an abbreviation of High-bandwidth Digital Content Protection.
This is a video signal encoding process system for DVI. The purpose of HDCP is to protect video contents from illegal copies. A display with HDCP adopted DVI input is needed to receive the encoded signal.

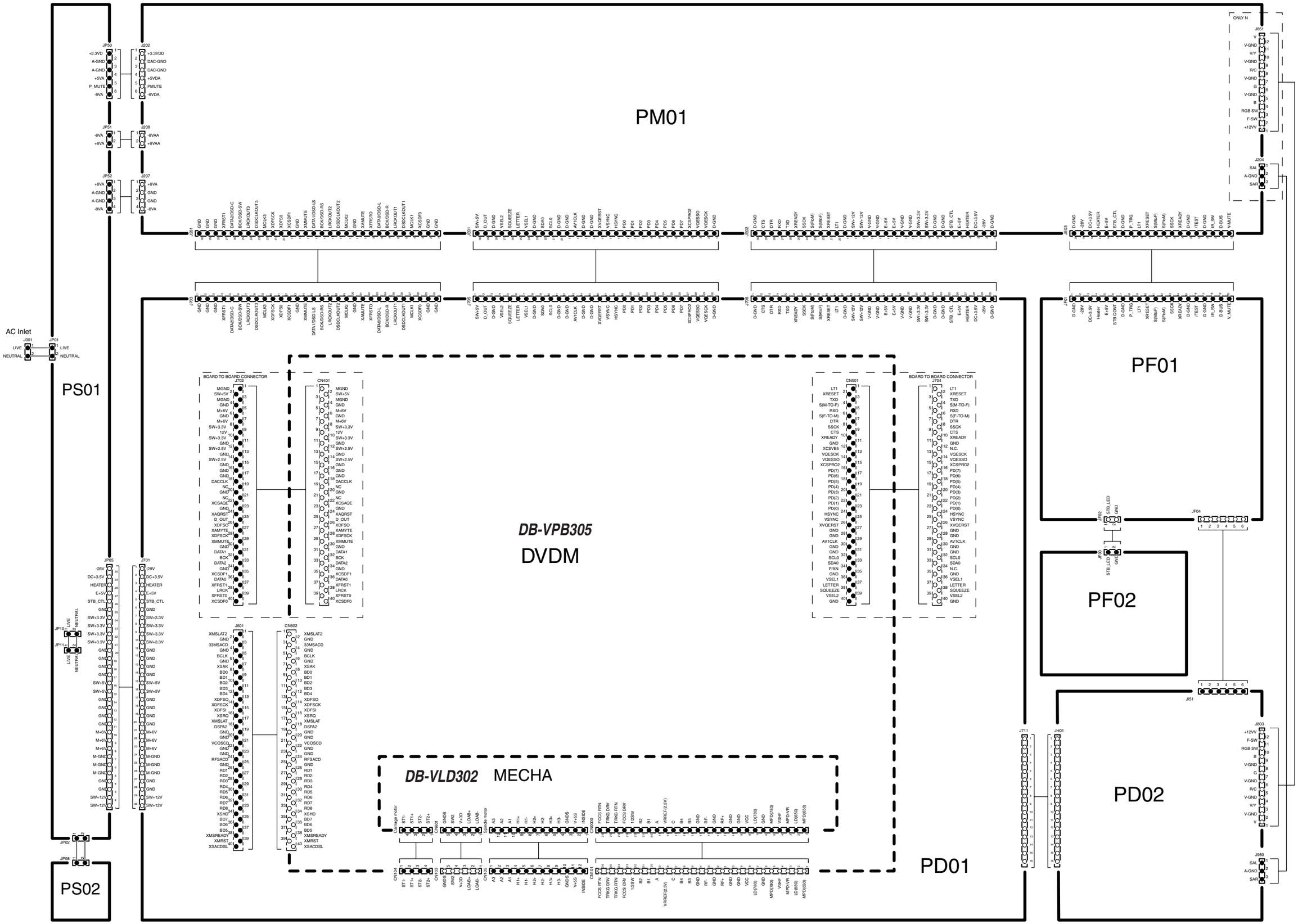
DVI

Digital Visual Interface の略です。
DDWG(Digital Display Working Group) が策定したデジタルディスプレイインターフェース規格です。ビデオ信号をデジタルで伝送することが出来ます。

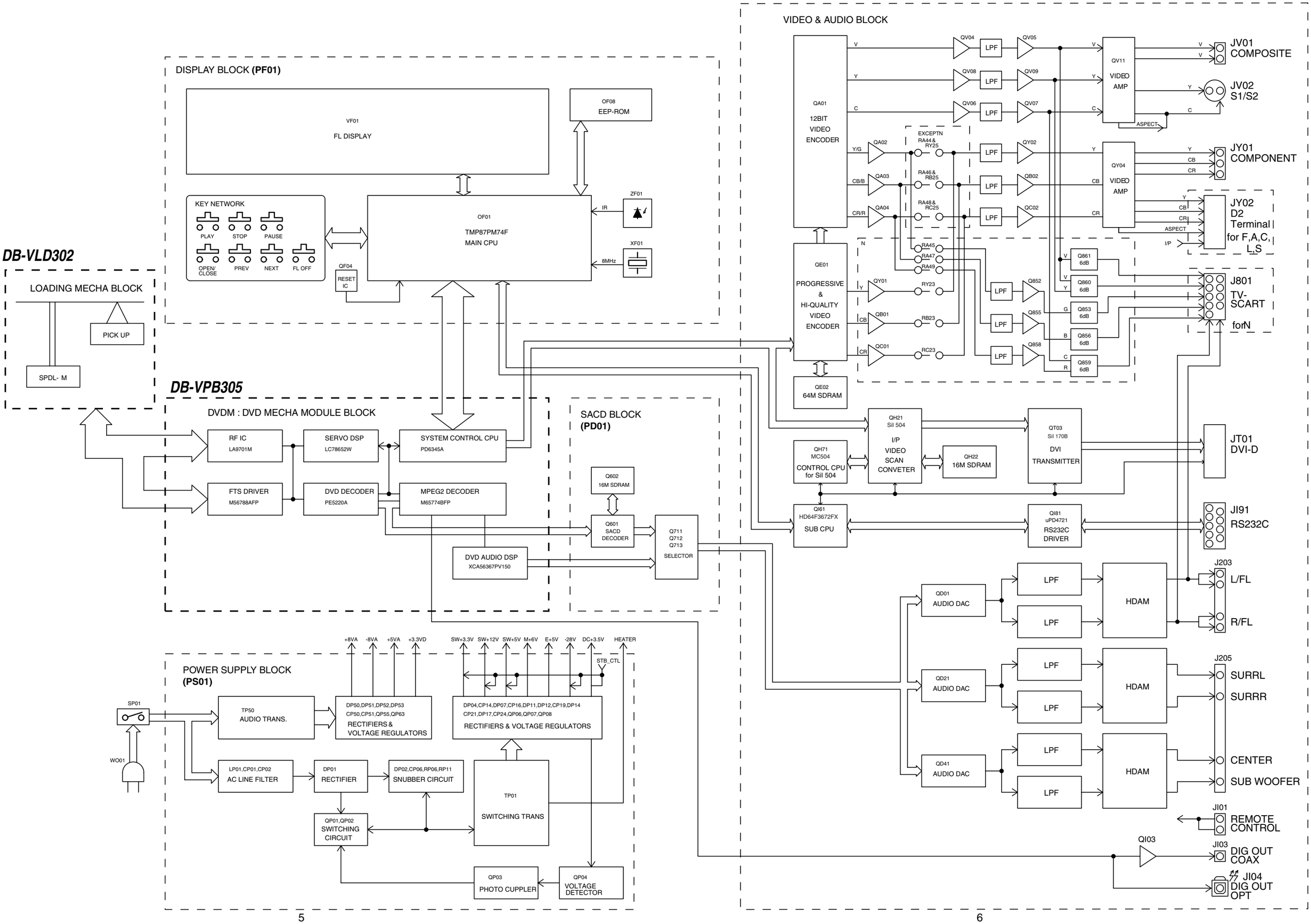
HDCP

High-bandwidth Digital Content Protection の略です。
DVI 用の映像向け暗号化処理方式です。映像コンテンツの違法コピーに対する保護を目的としており、暗号化された信号を受信するには、HDCP 対応の DVI 入力付ディスプレイが必要になります。

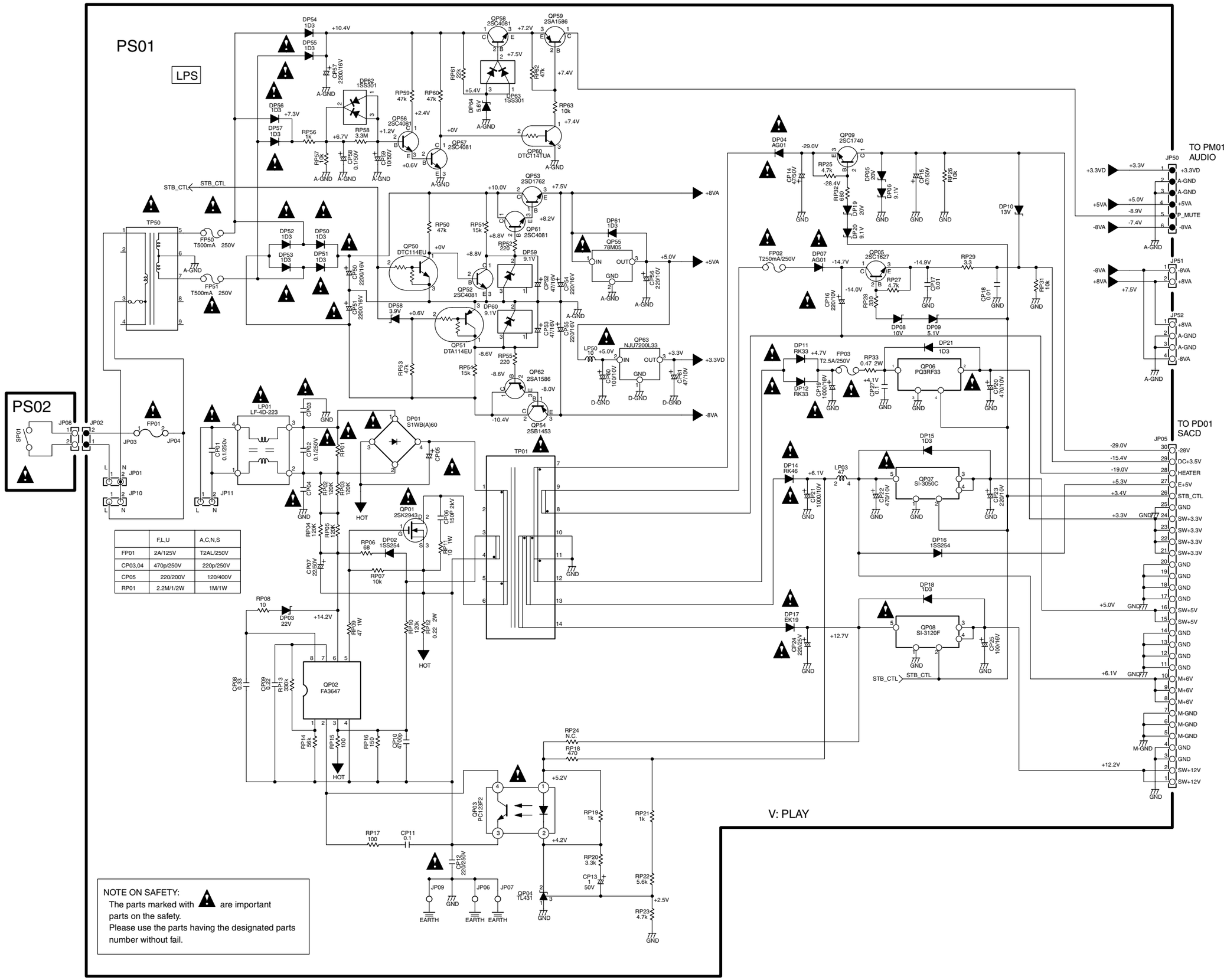
8. WIRING DIAGRAM



9. BLOCK DIAGRAM



10. SCHEMATIC DIAGRAM



	F,L,U	A,C,N,S
FP01	2A/125V	T2AL/250V
CP03,04	470p/250V	220p/250V
CP05	220/200V	120/400V
RP01	2.2M/1/2W	1M/1W

PD01-1/2

Q602
HY57V161610DTC-8

Q601
CXD2753R

Q603
TS7SH08FU

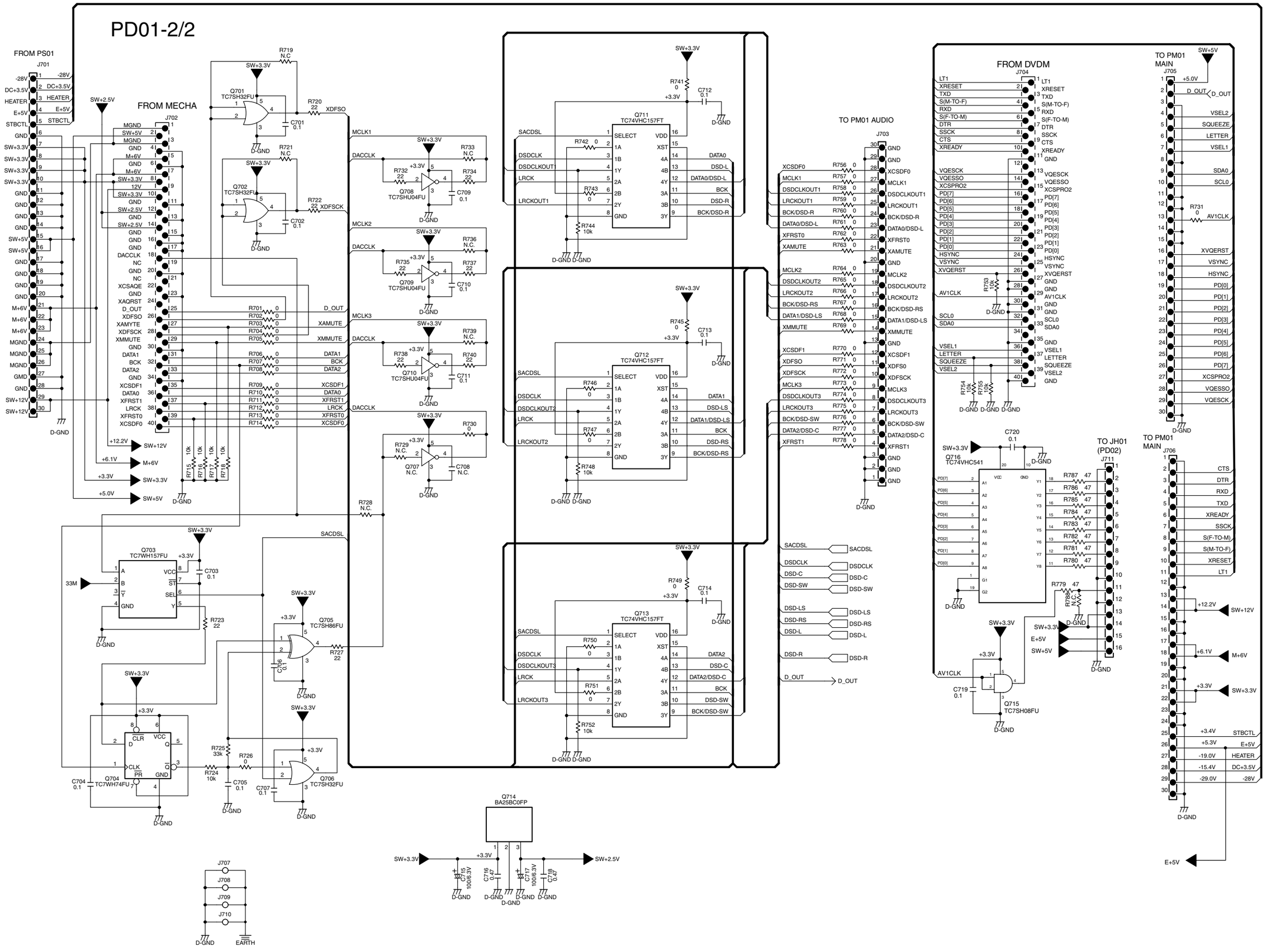
Q604
TC74VHC74FT

Q606
BA25BC0FP

FROM
DVDM

J601

PD01-2/2


FROM PS01
J701
-28V
DC+3.5V
HEATER
E+5V
STBCTL
GND
SW+3.3V
SW+2.5V
SW+5V
M+6V
MGND
GMD
SW+12V
D-GND
FROM MECHA
J702
MGND
M+6V
12V
XCSAQE
XAQRST
D_OUT
XDFSO
XAMUTE
XDFSCK
XMMUTE
DATA1
BCK
DATA2
XCSDF1
DATA0
XFRST1
LRCK
XFRST0
XCSDF0
+12.2V
+6.1V
+3.3V
+5.0V
R715 10k
R716 10k
R717 10k
R718 10k
R719 N.C
Q701 TC7SH32FU
R720 22
XDFSO
C701 0.1
R721 N.C
Q702 TC7SH32FU
R722 22
XDFSCK
C702 0.1
R701 0
R702 0
R703 0
R704 0
R705 0
R706 0
R707 0
R708 0
R709 0
R710 0
R711 0
R712 0
R713 0
R714 0
R728 N.C.
MCLK1
DACCLK
Q708 TC7SHU04FU
R732 22
R733 N.C
R734 22
C709 0.1
MCLK2
Q709 TC7SHU04FU
R735 22
R736 N.C.
R737 22
C710 0.1
MCLK3
Q710 TC7SHU04FU
R738 22
R739 N.C.
R740 22
C711 0.1
Q707 N.C.
R729 N.C.
R730 0
C708 N.C.
SACDSL
Q703 TC7WH157FU
33M
R723 22
C703 0.1
Q705 TC7SH86FU
R727 22
C706 0.1
Q704 TC7WH74FU
C704 0.1
R724 10k
R725 33k
R726 0
C705 0.1
Q706 TC7SH32FU
C707 0.1
J707
J708
J709
J710
EARTH
Q711 TC74VHC157FT
R741 0
C712 0.1
R742 0
R743 0
R744 10k
DSDCLK
DSDCLKOUT1
LRCKOUT1
DATA0
DSD-L
DATA0/DSD-L
BCK
DSD-R
BCK/DSD-R
Q712 TC74VHC157FT
R745 0
C713 0.1
R746 0
R747 0
R748 10k
DSDCLKOUT2
LRCKOUT2
DATA1
DSD-LS
DATA1/DSD-LS
DSD-RS
BCK/DSD-RS
Q713 TC74VHC157FT
R749 0
C714 0.1
R750 0
R751 0
R752 10k
LRCKOUT3
DATA2
DSD-C
DATA2/DSD-C
DSD-SW
BCK/DSD-SW
Q714 BA25BC0FP
C715 100/6.3V
C716 0.47
C717 100/6.3V
C718 0.47
TO PM01 AUDIO
J703
XCSDF0
MCLK1
DSDCLKOUT1
LRCKOUT1
BCK/DSD-R
DATA0/DSD-L
XFRST0
XAMUTE
MCLK2
DSDCLKOUT2
LRCKOUT2
BCK/DSD-RS
DATA1/DSD-LS
XMMUTE
XCSDF1
XDFSO
XDFSCK
MCLK3
DSDCLKOUT3
LRCKOUT3
BCK/DSD-SW
DATA2/DSD-C
XFRST1
R756 0
R757 0
R758 0
R759 0
R760 0
R761 0
R762 0
R763 0
R764 0
R765 0
R766 0
R767 0
R768 0
R769 0
R770 0
R771 0
R772 0
R773 0
R774 0
R775 0
R776 0
R777 0
R778 0
SACDSL
DSDCLK
DSD-C
DSD-SW
DSD-LS
DSD-RS
DSD-L
DSD-R
D_OUT
FROM DVDM
J704
LT1
XRESET
TXD
S(M-TO-F)
RXD
S(F-TO-M)
DTR
SSCK
CTS
XREADY
VQESCK
VQESSO
XCSPRO2
PD[7]
PD[6]
PD[5]
PD[4]
PD[3]
PD[2]
PD[1]
PD[0]
HSYNC
VSYNC
XVQERST
AV1CLK
SCL0
SDA0
VSEL1
LETTER
SQUEEZE
VSEL2
R753 10k
R754 10k
R755 10k
C720 0.1
Q716 TC74VHC541
C719 0.1
Q715 TC7SH08FU
R779 47
R780 47
R781 47
R782 47
R783 47
R784 47
R785 47
R786 47
R787 47
R788 N.C
TO JH01 (PD02)
J711
TO PM01 MAIN
J705
+5.0V
D_OUT
VSEL2
SQUEEZE
LETTER
VSEL1
SDA0
SCL0
R731 0
AV1CLK
XVQERST
VSYNC
HSYNC
PD[0]
PD[1]
PD[2]
PD[3]
PD[4]
PD[5]
PD[6]
PD[7]
XCSPRO2
VQESSO
VQESCK
TO PM01 MAIN
J706
CTS
DTR
RXD
TXD
XREADY
SSCK
S(F-TO-M)
S(M-TO-F)
XRESET
LT1
+12.2V
+6.1V
+3.3V
+3.4V
+5.3V
-19.0V
-15.4V
-29.0V
STBCTL
E+5V
HEATER
DC+3.5V
-28V
D-GND
EARTH

PM01-1/5

FROM PD01

FROM PS01

XFRST0
DATA0/DSD-L
BCK/DSD-R
XFRST1
DATA2/DSD-C
BCK/DSD-SW
LRCKOUT3
DSDCLKOUT3
MCLK3
XDFSCK
XDFSO
XCSDF0
XMMUTE
DATA1/DSD-LS
BCK/DSD-RS
LRCKOUT2
DSDCLKOUT2
MCLK2
XAMUTE
XFRST1
DATA1/DSD-LS
BCK/DSD-RS
LRCKOUT2
MCLK2
DSDCLKOUT2
XDFSCK
XDFSO
XCSDF1

PMUTE
MUTE+12V
SW+12V

L
R
FL
FR
SL
SR
C
SW

N only

PM01-2/5

FROM PD01

JE01

SW+5V
D_OUT
D-GND
VSEL2
SQUEEZE
LETTER
VSEL1
D-GND
SDA0
SCL0
D-GND
D-GND
AV1CLK
D-GND
D-GND
XVQERST
VSYNC
HSYNC
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
XCSPRO2
VQESSO
VQESCK
D-GND

RE01 0 D_OUT
CE01 N.C.
RE02 0 VSEL2
RE03 0 SQUEEZE
RE04 0 LETTER
RE05 0 VSEL1
RE06 0 SDA0
RE07 0 SCL0
RE08 0 AV1CLK
RE84 0 CKE
RE09 0 XVQERST
RE10 0 VSYNC
RE11 0 HSYNC
RE12 22 PD0
RE13 22 PD1
RE14 22 PD2
RE15 22 PD3
RE16 22 PD4
RE17 22 PD5
RE19 22 PD6
RE20 22 PD7
RE21 0 XCSPRO2
RE22 0 VQESSO
VQESCK

+5.0V → SW+5V

FROM PD01

JE02

D-GND
CTS
DTR
RXD
TXD
XREADY
SSCK
S(FtoM)
S(MtoF)
XRESET
LT1
D-GND
SW+12V
SW+12V
V-GND
V-GND
E+6V
E+6V
V-GND
V-GND
SW+3.3V
SW+3.3V
D-GND
D-GND
STB_CTL
E+5V
HEATER
DC+3.5V
-28V
D-GND

RE23 0 CTS
RE24 0 DTR
RE25 0 RXD
RE26 0 TXD
XREADY
SSCK
S(FtoM)
S(MtoF)
XRESET
LT1
+12.2V → SW+12V
V-GND
+6.1V → E+6V
V-GND
+3.3V → +3VD
STB_CTL
E+5V
HEATER
DC+3.5V
-28V

FROM PD01

JE03

D-GND
-28V
DC+3.5V
HEATER
E+5V
STB_CTL
D-GND
P_TRG
LT1
XRESET
S(MtoF)
S(FtoM)
SSCK
XREADY
D-GND
/TEST
D-GND
IR_SW
D-BUS
V-MUTE

-29.0V -28V
-15.4V DC+3.5V
-19.0V HEATER
+5.3V E+5V
+3.4V STB_CTL
P_TRG

RE36 N.C.
RE27 0 IR_SW
RE28 0 D-BUS
RE29 0 V-MUTE

QE01
PM0033A

XVQERST
VQESSO
XCSPRO2
PC3 PC4 PC5 PC6 PC7 PC8 PC9
PB6 PB7 PB8 PB9
PB0 PB1 PB2 PB3 PB4 PB5
PC0 PC1 PC2

CE34 N.C.
CE36 0.01
RE76 75
RE74 0
CE35 0.1
RE75 22k
RE73 0
RE72 N.C.
RE70 0
RE71 0
RE66 0
RE65 0
RE64 0
RE63 0
RE62 0
RE61 0
RE60 0
RE58 0
RE57 0
CE23 0.1
CE32 0.1
CE31 0.1
CE30 0.1
CE27 100/10v
CE28 100/10v
CE29 0.1
RE55 BLM11B601S
+2.5VD
+2.5V
D-GND

CE02 0.1
CE37 0.1
CE03 0.1
CE04 0.1
CE05 0.1
CE06 0.1
CE07 0.1
CE08 0.1
CE09 0.1
CE10 0.1
CE12 0.1
CE13 0.1
CE14 100/10v
CE15 0.1

RE30 0
RE31 0
RE32 0
RE33 0
RE34 0
RE35 0RX4
RE38 0
RE39 0RX4
RE43 0
RE44 0
AV1CLK
PR2CLK
PPD0 PPD1 PPD2 PPD3 PPD4 PPD5 PPD6 PPD7
HSYNC
VSYNC

VDD3 CLKI PLL_TEST PLL_EN VDD2 CLKO PD0 PD1 PD2 PD3 PD4 GND VDD3 PD5 PD6 PD7 PD8 PD9 GND GND VDD3 NHS NVS PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 MA4 MA3 MA5 MA2 GND VDD3
VDD2 MA6 MA1 MA7 MA0 MA8 MA10 VDD3 MA9 MA11 GND RAS MCLK CAS WE VDD3 MD8 MD7 MD9 PDOEN GND MD6 MD10 MD5 VDD3 MD11 MD4 MD12 MD3 MD13 GND VDD3 MD2 MD14 MD1 MD15 MD0 VDD2
VDD3 SPR7 SPR6 GND SPR5 SPR4 SPR3 SPR2 VDD3 SPR1 SPR0 TEST4 TEST3 TEST2 TEST1 TEST0 CLMP GND GND GND GND AGND VG AVDD2 VREF AVDD2 DAO_Cr AGND DAO_Cb AVDD2 DAO_Y AGND GND MD19 MD18 MD17 MD16 GND VDD3

RE54 0 SPR4
CE24 0.1
CE26 0.1
CE25 0.1
CE22 NC
CE56 100/10V
CE23 0.1
CE21 0.1
RE52 330
RE51 8.2k
CE20 0.1
CE18 0.1
CE19 0.1
RE49 N:2.2k Except N:1.2k
CE17 0.1
RG23 100 MD19
RG22 100 MD18
RG21 100 MD17
RG20 100 MD16
CE16 0.1
RE46 BLM11B601S +3.3V
LE01 10
RE53 0
+2.5V

QE02
K4S643232E-TC60

RE78 10RX4
RE79 10RX4
RE80 10RX4
RE81 10k
RE48 NC
CKE
CE44 0.1
CE43 0.1
CE42 0.1
CE41 0.1
CE40 0.1
CE58 100/10v
RE47 +3.3V
CE59 0.1
CE45 0.1
CE46 0.1
CE47 0.1
CE48 0.1
CE49 0.1
CE50 0.1
CE51 0.1
+3VD

VDD DQ23 VDDQ DQ22 DQ21 VSSQ DQ20 DQ19 VDDQ DQ18 DQ17 VSSQ DQ16 NC VDD DQM2 A2 A1 A0 A10/AP BS1 BS0 /CS /RAS /CAS /WE DMI VDD NC DQ7 VSSQ DQ6 DQ5 VDDQ DQ4 DQ3 VSSQ DQ2 DQ1 VDDQ DQ0 VDD
VSS DQ24 VSSQ DQ25 DQ26 VDDQ DQ27 DQ28 VSSQ DQ29 DQ30 VDDQ DQ31 NC VSS DQM3 A3 A4 A5 A6 A7 A8 A9 CKE CLK NC VREF DQM1 VSS NC DQ8 VDDQ DQ9 DQ10 VSSQ DQ11 DQ12 VDDQ DQ13 DQ14 VSSQ DQ15 VSS

QE03
BA25BC0FP

+3VD
+3.3V
+2.5V
+2.5VD
CE52 100/10v
CE53 0.1
CE54 100/10v
CE55 0.1

QE04
DTC114EUA

QE05
DTC114EUA

+5VV
RE82 10K
RE83 10K
P/XI
Prog: +3.2V
Int: +0V
Prog: +5.0V
Int: +0V
SPR4

QA01
ADV7300

+3VD
+2.5VD
+2.5V
RA01 BLM11B601S
RA02 N.C.
RA03 BLM11B601S
CA01 100/10v
CA02 0.1
CA03 0.1
CA04 0.1
CA05 0.1
CA06 0.1
CA07 N.C.
CA08 N.C.
CA09 N.C.
CA10 100p
CA11 820p
CA12 390p
CA13 N.C.
CA14 0.1
CA15 0.1
CA16 0.1
CA17 0.1
CA19 N.C.
CA21 0.1
CA22 0.1
CA23 0.1
CA26 470/16V
CA27 N.C.
RA04 0
RA05 0
RA06 0
RA07 0
RA08 2.2k
RA09 2.2k
RA10 10k
RA11 10k
RA12 0
RA13 100
RA14 680
RA15 1.5k
RA16 47
RA23 6.8k
RA24 N.C.
RA25 6.8k
RA26 1.5k
RA28 0
RA29 10k
RA30 10k
RA31 10k
LA01 10
JE04
JE05
JE06
JE07
EARTH

PC0 PC1 PC2 PC3 PC4 PC5 PC6 PC7 PC8 PC9 PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7 PB8 PB9 PR2CLK
PPD7 PPD6 PPD5 PPD4 PPD3 PPD2 PPD1 PPD0 HSYNC VSYNC XS_HSYNC XS_VSYNC XS_BLANK
XSPII2C ALSB_SO SDA_CLKSP SCLK_SI XP_HSYNC XP_VSYNC P_BLANK RTC_SCR_TR CLKIN_A
SDAO SCLO XVQERST

AD_V AD_Y AD_C AD_Y/G AD_Cb/B AD_Cr/R

***

	RA44	RA45	RA46	RA47	RA48	RA49
EXCEPT N	0	NC	0	NC	0	NC
N	NC	0	NC	0	NC	0

+5VV
+5.0V
+0.9V
+1.0V
+0.3V
QA02 2SA1586
QA03 2SA1586
QA04 2SA1586
RA34 100
RA38 100
RA42 100
RA30 680
RA36 680
RA40 680
RA33 560
RA37 560
RA41 560
CA24 0.1
CA25 0.1
CA28 100/10v
RA35 1.8k
RA39 1.8k
RA43 1.8k
RA44 RA45 RA46 RA47 RA48 RA49 0
AD_Y2 AD_G AD_Cb AD_B AD_Cr AD_R
AD_Y/G AD_Cb/B AD_Cr/R
V-GND
V-GNDD

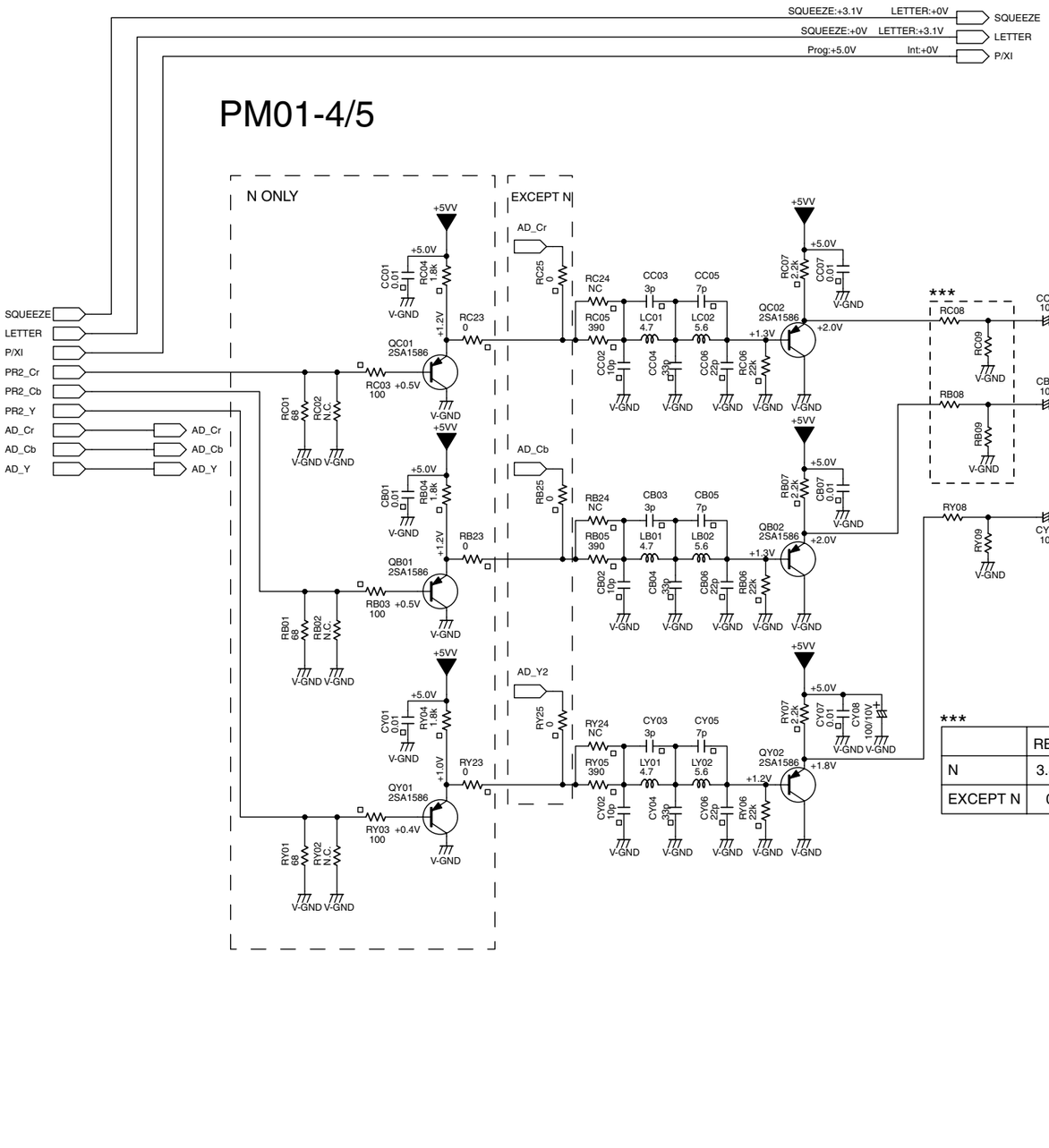
PR2_Cr PR2_Cb PR2_Y

PM01-3/5

***	RV05	RV06	RV12	RV13	RV19	RV20	RV28	RV29
N ONLY	680	560	680	560	680	560	NC	0
EXCEPT N	470	470	470	470	470	470	0	NC

N only

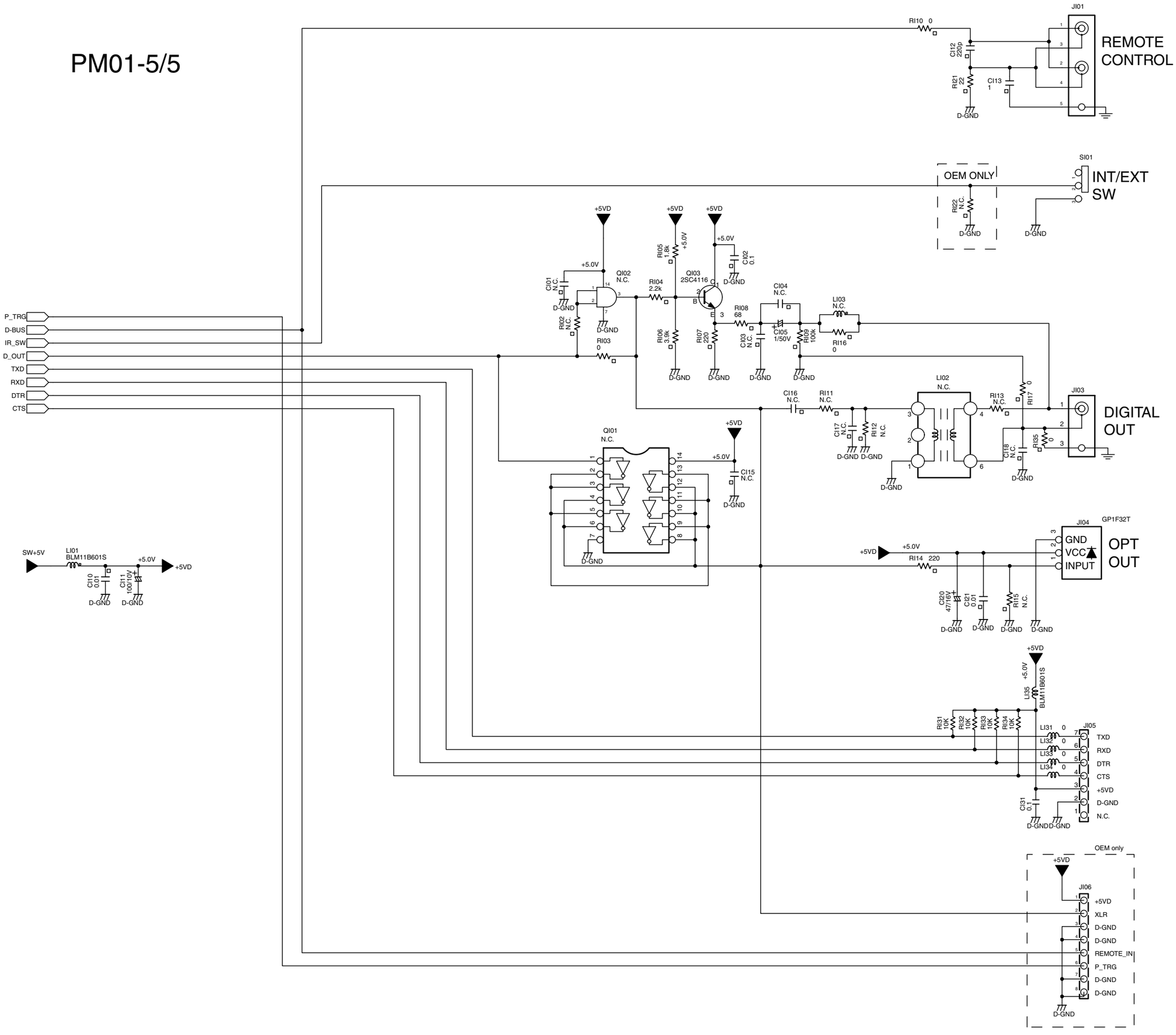
PM01-4/5



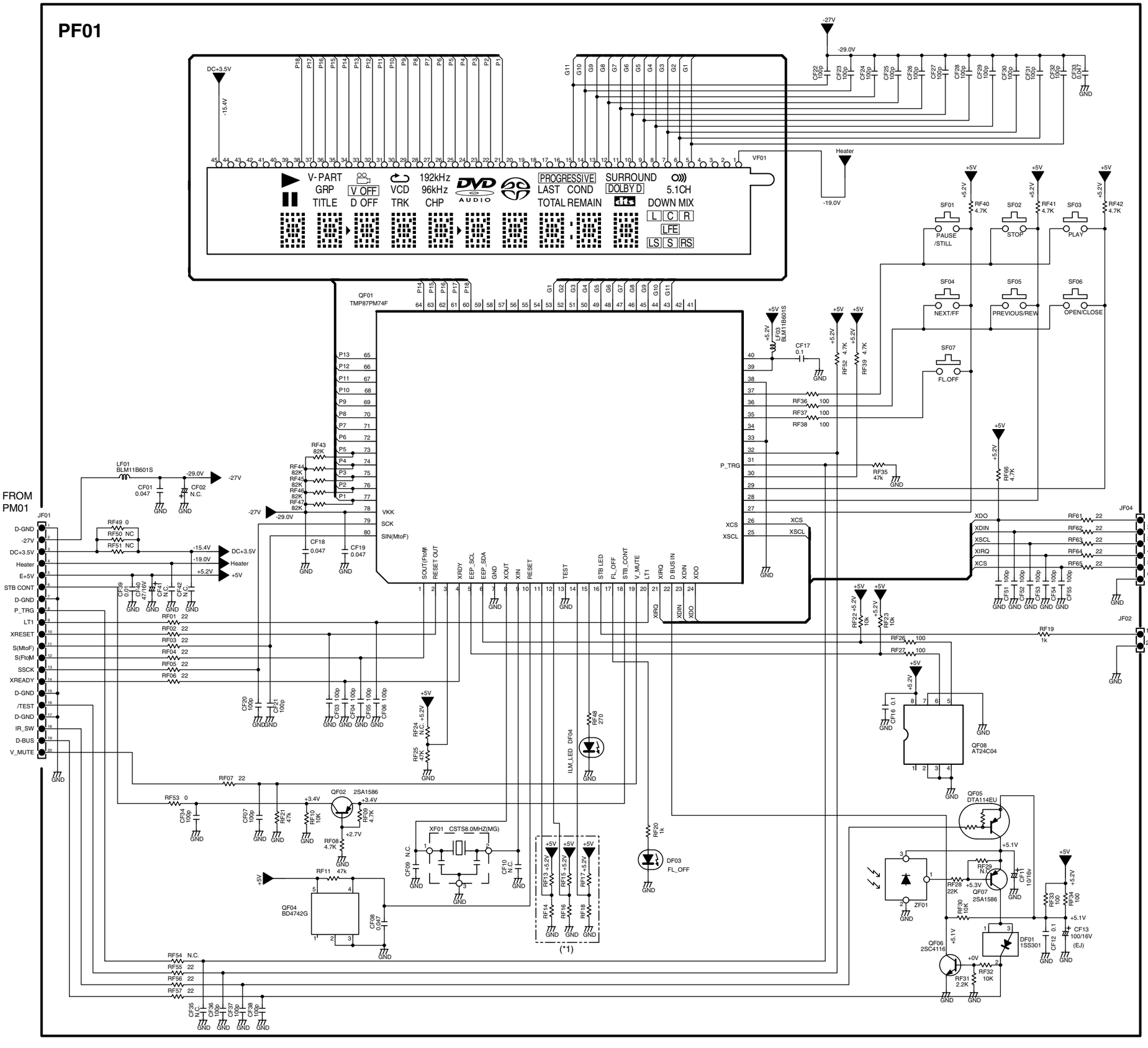
***

	RB08	RB09	RC08	RC09
N	3.3k	5.6k	3.3k	5.6k
EXCEPT N	0	N.C.	0	N.C.

PM01-5/5


P_TRG
D-BUS
IR_SW
D_OUT
TXD
RXD
DTR
CTS
SW+5V
LI01 BLM11B601S
CI10 0.01
CI11 100/10V
+5.0V
+5VD
D-GND
RI10 0
CI12 220p
RI21 22
CI13 1
JI01
REMOTE CONTROL
OEM ONLY
RI22 N.C.
SI01
INT/EXT SW
QI01 N.C.
QI02 N.C.
QI03 2SC4116
RI02 N.C.
RI03 0
RI04 2.2k
RI05 1.8k
RI06 3.9k
RI07 220
RI08 68
RI09 10K
RI16 0
CI01 N.C.
CI02 0.1
CI03 N.C.
CI04 N.C.
CI05 1/50V
LI03 N.C.
CI15 N.C.
CI16 N.C.
RI11 N.C.
RI12 N.C.
CI17 N.C.
LI02 N.C.
RI13 N.C.
RI17 0
RI35 0
CI18 N.C.
JI03
DIGITAL OUT
JI04
GP1F32T
GND
VCC
INPUT
OPT OUT
RI14 220
CI20 47/16V
CI21 0.01
RI15 N.C.
LI35 BLM11B601S
RI31 10K
RI32 10K
RI33 10K
RI34 10K
LI31 0
LI32 0
LI33 0
LI34 0
CI31 0.1
JI05
TXD
RXD
DTR
CTS
+5VD
D-GND
N.C.
OEM only
JI06
XLR
REMOTE_IN
P_TRG

PF01



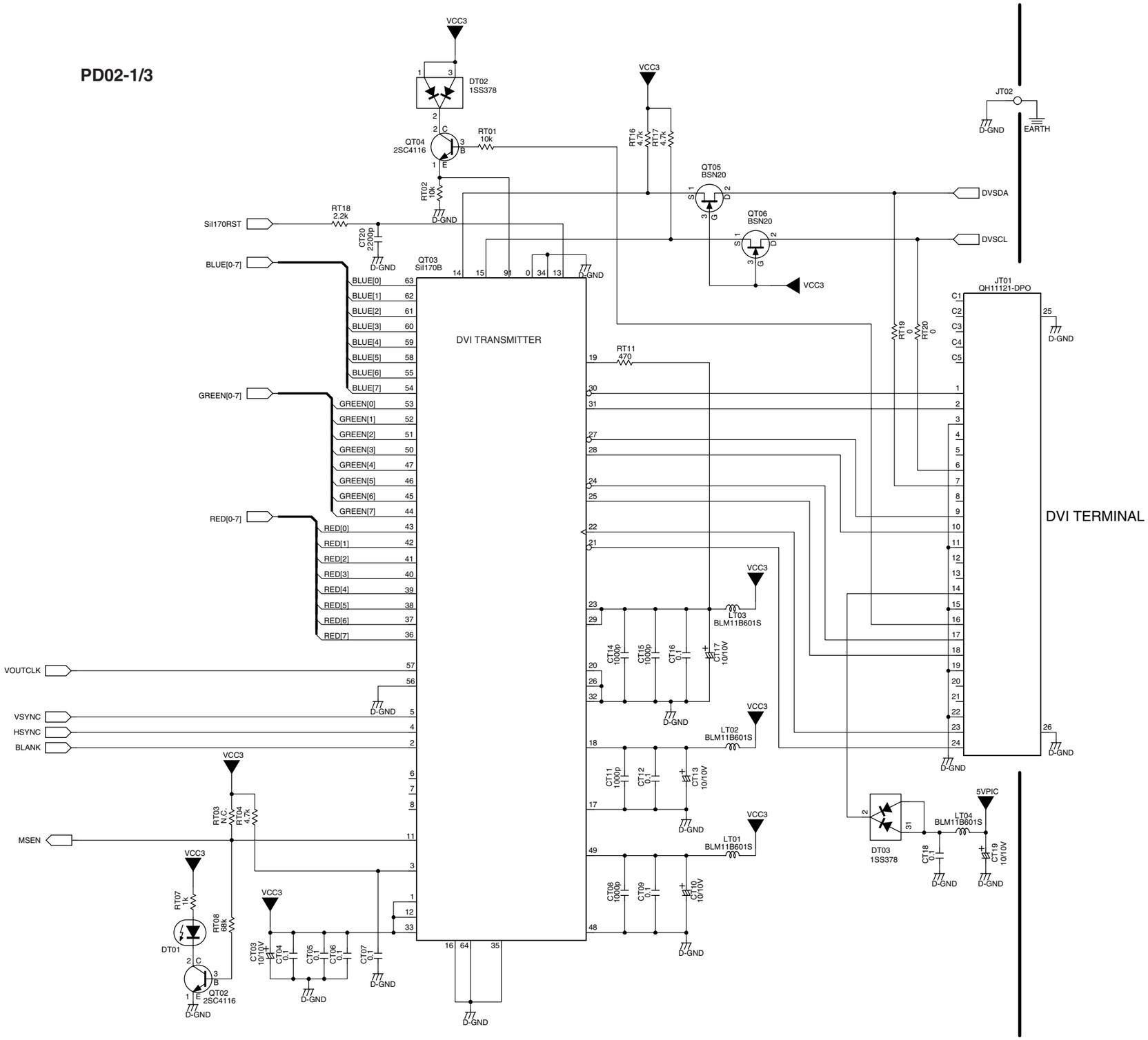
(*1)
QF01 Pin No.11,12,14 SETTING

Region	Distination	Pin No. / MS1	11	12	14
2	JAPAN	0	L	L	L
1	USA	1	H	L	L
4	AUS	2	L	H	L
3	ASIA	2	H	H	L
2	EURO	4	L	L	H
5	--	4	H	L	H
6	CHINA	2	H	H	H

-AREA INDICATION-

F:Japan
K:China
N:Europe
S:S'Pore
U:USA and Canada

PD02-1/3


DVI TRANSMITTER
DVI TERMINAL
QT03 Sil170B
JT01 QH11121-DPO
JT02
DT02 1SS378
DT03 1SS378
DT01
QT04 2SC4116
QT02 2SC4116
QT05 BSN20
QT06 BSN20
LT01 BLM11B601S
LT02 BLM11B601S
LT03 BLM11B601S
LT04 BLM11B601S
RT01 10k
RT02 10k
RT03 N.C.
RT04 4.7K
RT07 1k
RT08 68k
RT11 470
RT16 4.7k
RT17 4.7K
RT18 2.2k
RT19 0
RT20 0
CT20 2200p
CT03 10/10V
CT04 0.1
CT05 0.1
CT06 0.1
CT07 0.1
CT08 1000p
CT09 0.1
CT10 10/10V
CT11 1000p
CT12 0.1
CT13 10/10V
CT14 1000p
CT15 1000p
CT16 0.1
CT17 10/10V
CT18 0.1
CT19 10/10V
VCC3
5VPIC
D-GND
EARTH
Sil170RST
BLUE[0-7]
GREEN[0-7]
RED[0-7]
VOUTCLK
VSYNC
HSYNC
BLANK
MSEN
DVSDA
DVSCL

PD02-2/3

TO J711
(PD01)

QH21
Sil504

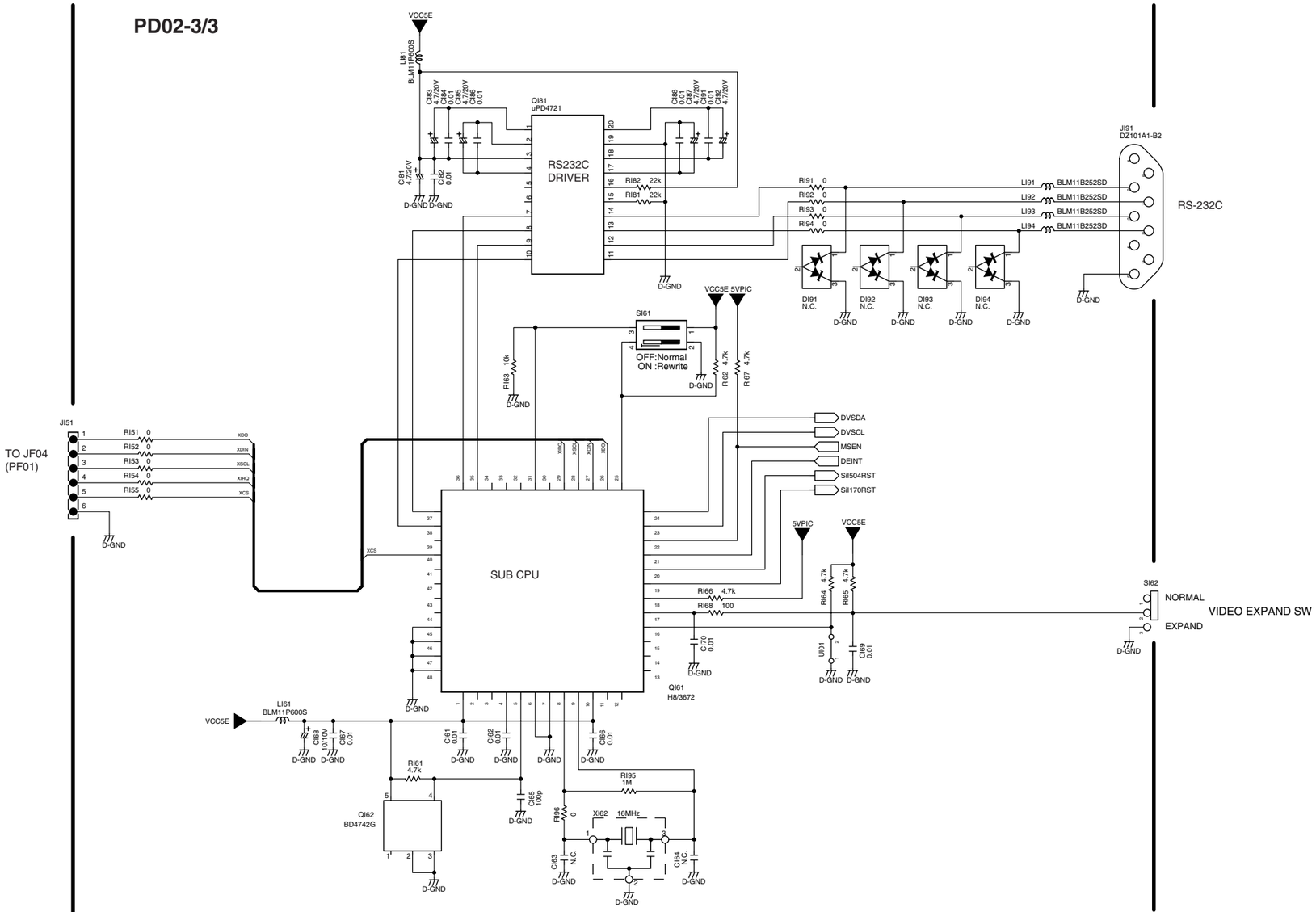
I/P VIDEO SCAN CONVETER

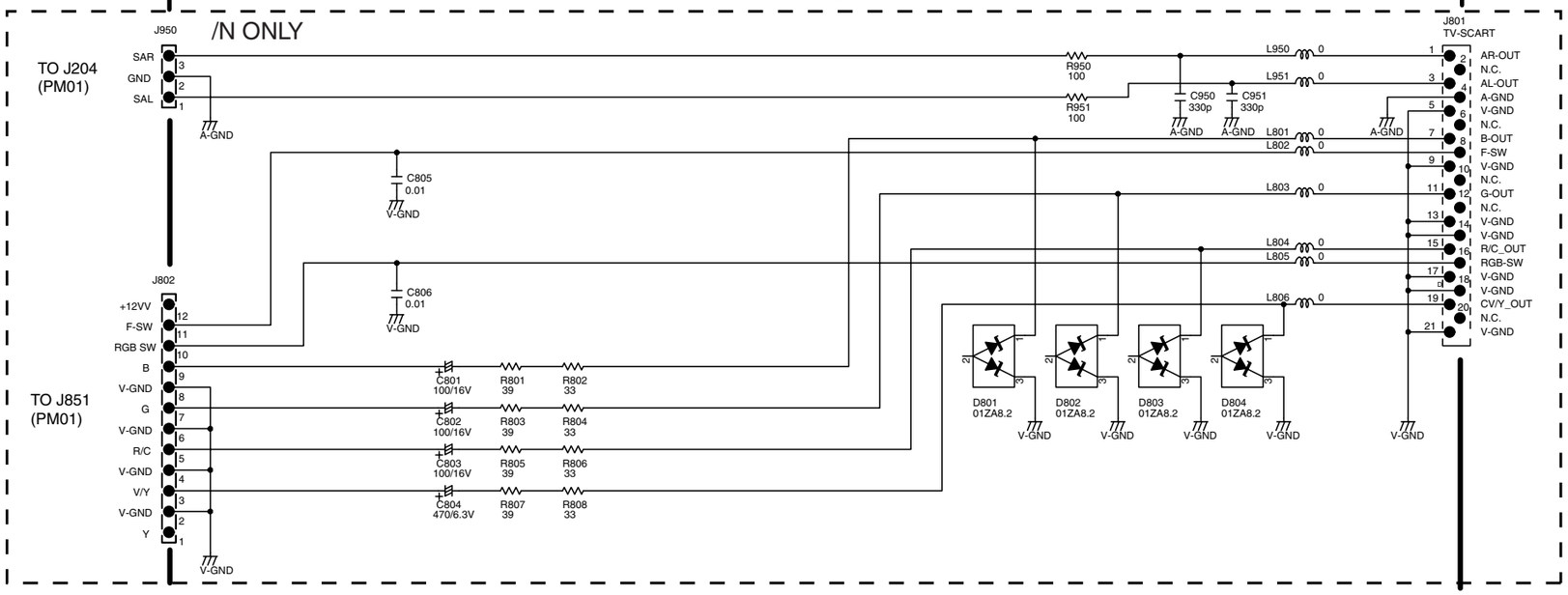
QH2
K4S643232E-TC60

QH71
PIC16C63A

QH1
BA18BC0FP

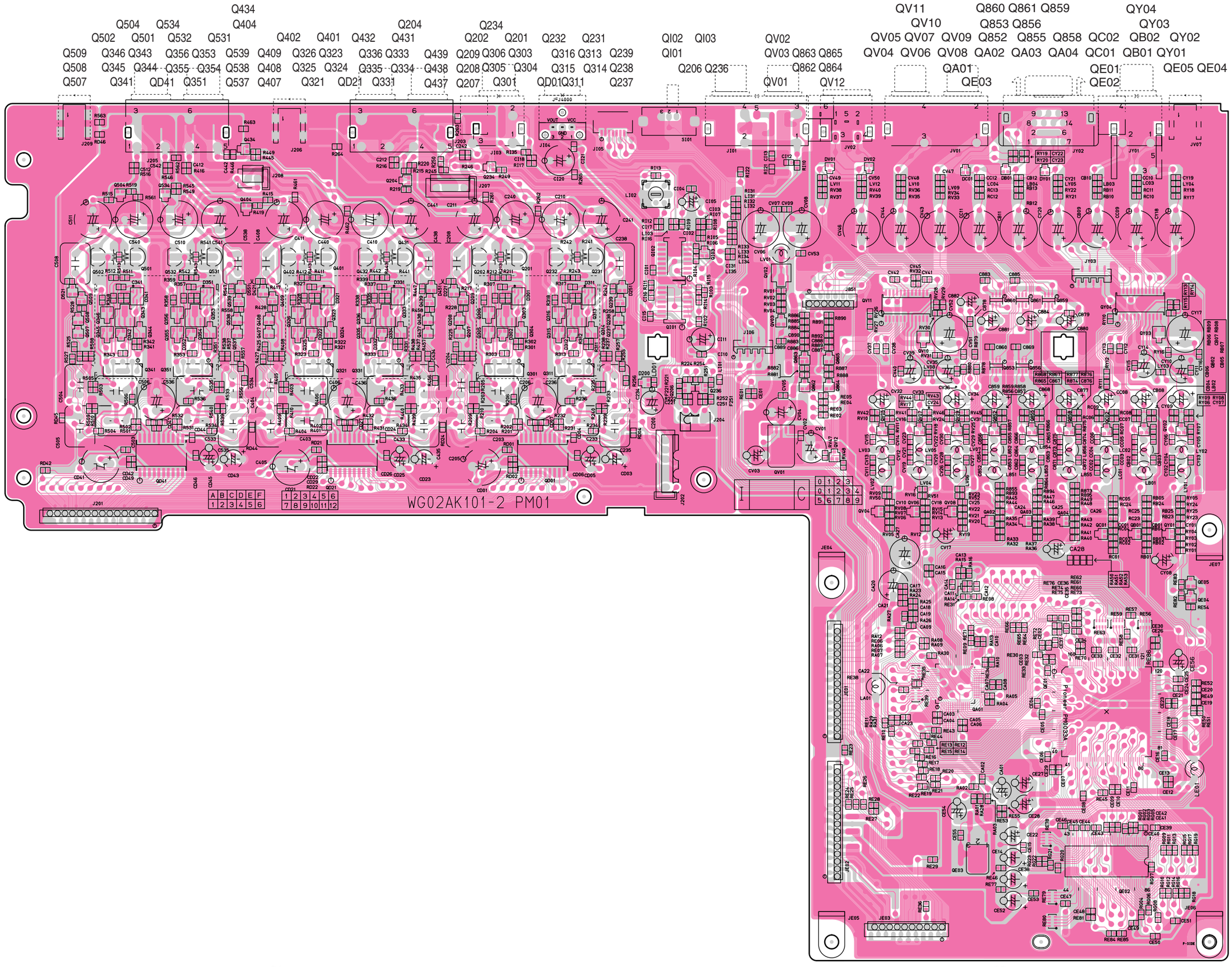
PD02-3/3


VCC5E
LB1 BLM11P600S
QI81 uPD4721
RS232C DRIVER
CI81 4.7/20V
CI82 0.01
CI83 4.7/20V
CI84 0.01
CI85 0.01
CI86 4.7/20V
CI87 0.01
CI88 0.01
CI89 4.7/20V
CI90 0.01
CI91 0.01
CI92 4.7/20V
RI81 22k
RI82 22k
D-GND
RI91 0
RI92 0
RI93 0
RI94 0
LI91 BLM11B252SD
LI92 BLM11B252SD
LI93 BLM11B252SD
LI94 BLM11B252SD
JI91 DZ101A1-B2
RS-232C
DI91 N.C.
DI92 N.C.
DI93 N.C.
DI94 N.C.
5VPIC
SI61
OFF:Normal
ON :Rewrite
RI63 10k
RI62 4.7k
RI67 4.7k
JI51
TO JF04 (PF01)
RI51 0
RI52 0
RI53 0
RI54 0
RI55 0
XDO
XDIN
XSCL
XIRQ
XCS
SUB CPU
DVSDA
DVSCL
MSEN
DEINT
SII504RST
SII170RST
RI66 4.7k
RI68 100
RI64 4.7k
RI65 4.7k
CI70 0.01
CI69 0.01
LI01
SI62
NORMAL
EXPAND
VIDEO EXPAND SW
QI61 H8/3672
LI61 BLM11P600S
CI68 100/6.3V
CI67 0.01
CI61 0.01
CI62 0.01
CI66 0.01
RI61 4.7k
CI65 100p
QI62 BD4742G
RI95 1M
RI96 0
XI62 16MHz
CI63 N.C.
CI64 N.C.

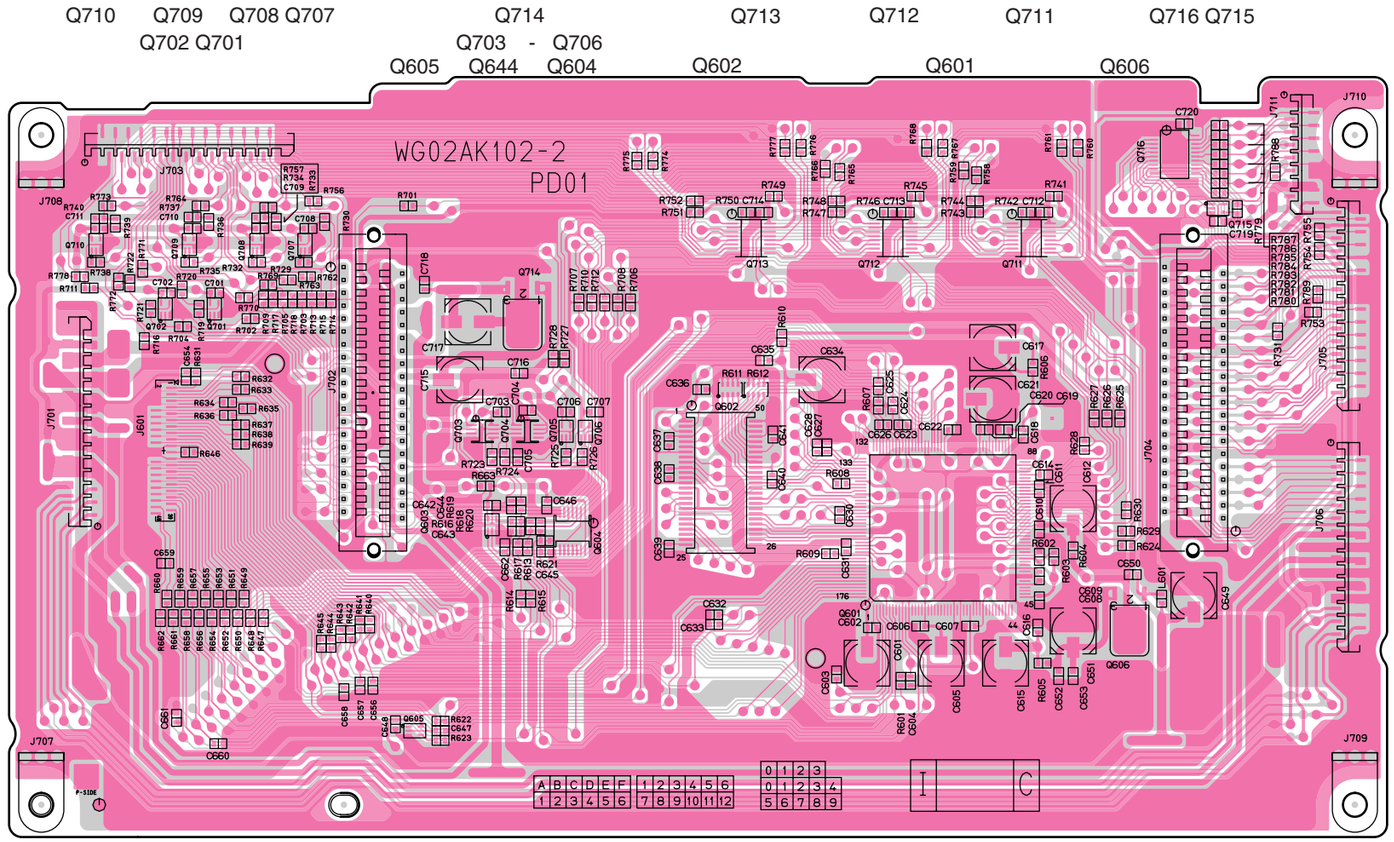

/N ONLY
TO J204 (PM01)
J950
SAR
GND
SAL
A-GND
R950 100
R951 100
C950 330p
C951 330p
L950 0
L951 0
L801 0
L802 0
L803 0
L804 0
L805 0
L806 0
J801 TV-SCART
AR-OUT
N.C.
AL-OUT
A-GND
V-GND
N.C.
B-OUT
F-SW
V-GND
N.C.
G-OUT
N.C.
V-GND
V-GND
R/C_OUT
RGB-SW
V-GND
V-GND
CV/Y_OUT
N.C.
V-GND
C805 0.01
C806 0.01
V-GND
J802
TO J851 (PM01)
+12VV
F-SW
RGB SW
B
V-GND
G
V-GND
R/C
V-GND
V/Y
V-GND
Y
C801 100/16V
C802 100/16V
C803 100/16V
C804 470/6.3V
R801 39
R802 33
R803 39
R804 33
R805 39
R806 33
R807 39
R808 33
D801 01ZA8.2
D802 01ZA8.2
D803 01ZA8.2
D804 01ZA8.2

11. PARTS LOCATION

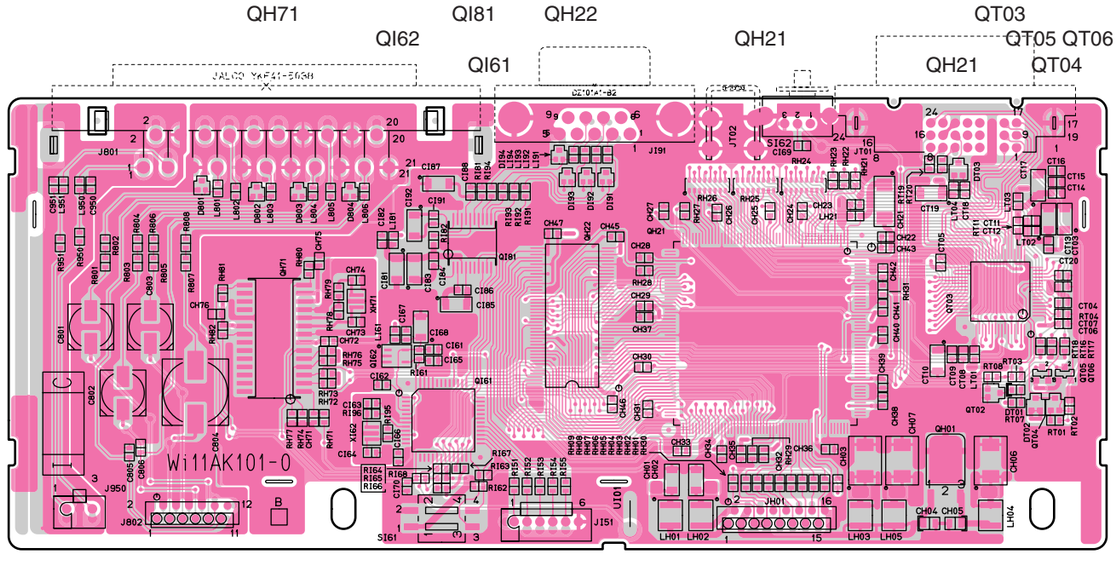
PM01



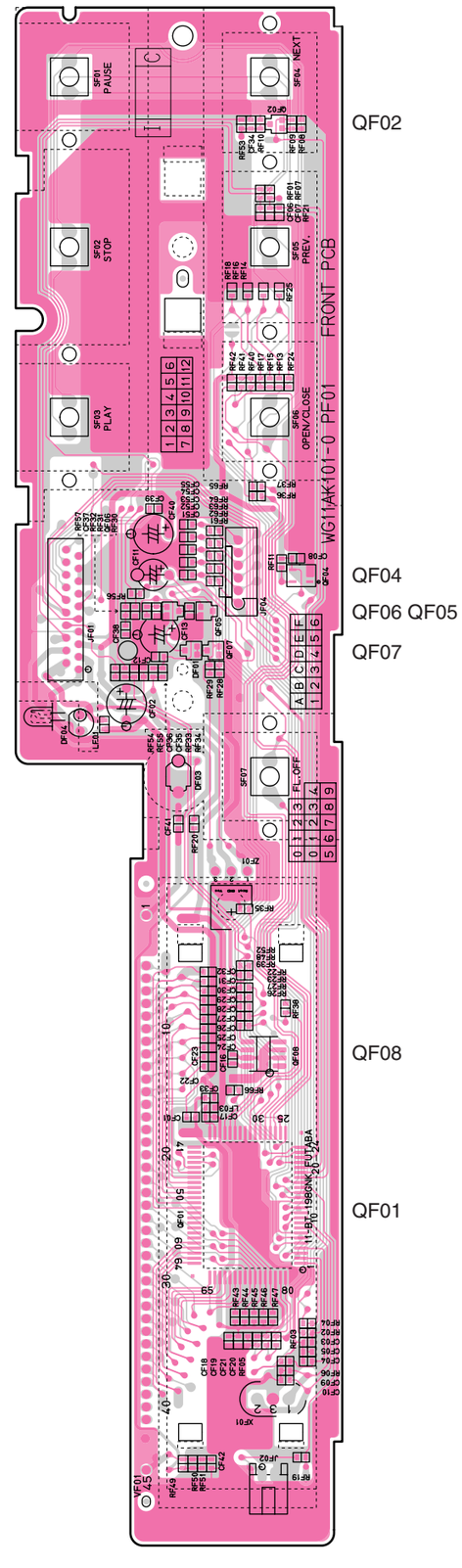
PD01



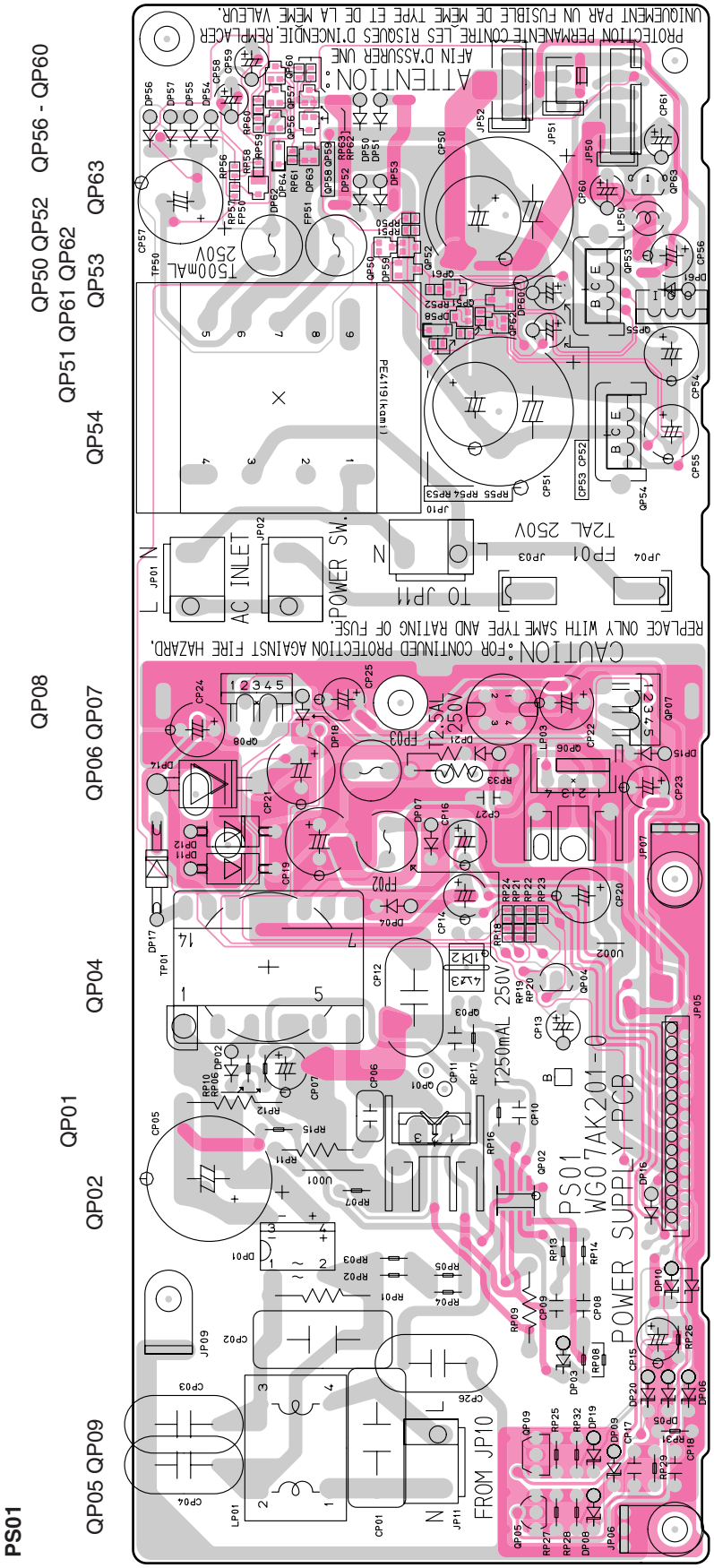
PD02



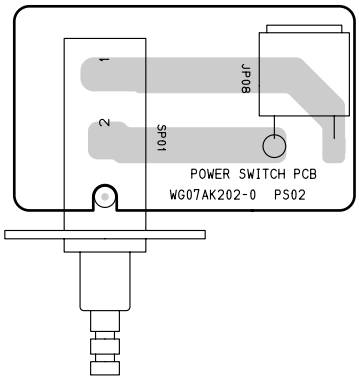
PF01



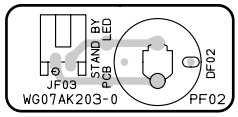
PS01



PS02



PF02



12 MICROPROCESSOR AND IC DATA

QF01:TMP87PM74F

Pin	PORT	Signal name	I/O	Contents of control	
1	P02/SO1	SOUT (F to M)	O	Serial bus data output for DV747	
2	P03	RESET_OUT	O	For the DV747 RESET terminal control	RESET: L
3	P04				
4	P05	XRDY	O	Serial data communication request signal for DV747	High: request /Low: no
5	P06	SCL	O	I2C clock (EEPROM control)	AT24C04
6	P07	SDA	I/O	I2C data (EEPROM control)	AT24C04
7	VSS			GND	
8	XOUT			8MHz X'TAL	
9	XIN			8MHz X'TAL	
10	RESET	RESET	I	Reset signal for the microprocessor	
11	P22	MODEL1	I	Set up of version	
12	P2	MODEL2	I	Set up of version	
13	TEST			GND	
14	P20	MODEL3	I	Set up of version	
15	P10	ILM_LED	O	ILM LED for FL	Light burned: H
16	P11	STB_LED	O	It is light at the STANDBY	Light burned: H
17	P12	FL_OFF_LED	O	Lighting (FL Lights-out)	Light burned: H
18	P13	STB_CONT	O	Power supply control for DV747	Stand-by time: LOW
19	P14	V_MUTE	O	Mute control for Video	At the time of Mute: L
20	P15	LT1	I	Serial bus data Ready/Busy input for DVD747	High:Ready/Low:Busy
21	P16	XIRQ	I	Serial bus data receiving control for Sub microprocessor	
22	P17/TC3	IR	I	IR sensor input	
23	P	DIN	I	Serial bus data output for Sub maicroprocessor	
24	P31	DO	O	Serial bus data input for Sub microprocessor	
25	P32	SCK	I	Serial bus clock input for Sub microprocessor	
26	P40	XCS	O	Serial bus data transmitting control for Sub microprocessor	
27	P41	KEY_IN_0	I	Key matrix input (Tactile switch)	
28	P42	KEY_IN_1	I	Key matrix input (Tactile switch)	
29	P43	KEY_IN_2	I	Key matrix input (Tactile switch)	
30	P44	KEY_IN_3	I	Key matrix input (Tactile switch) spare	
31	P45				
32	P46				
33	P47			GND	
34	P50	KEY_OUT_0	O	Tactile switch spare	
35	P51	KEY_OUT_1	O	Tactile switch	
36	P52	KEY_OUT_2	O	Tactile switch	
37	P53	KEY_OUT_3	O	Tactile switch	
38	VASS	GND		GND for A/D	
39	VAREF	+5V	O	A reference voltage for A/D	
40	VDD	+5V		Power supply	
41	P60	N.C.			
42	P6	N.C.			
43	P62	G11	O	FL indication	
44	P63	G10	O	FL indication	
45	P64	G9	O	FL indication	
46	P65	G8	O	FL indication	
47	P66	G7	O	FL indication	
48	P67	G6	O	FL indication	
49	P70	G5	O	FL indication	
50	P71	G4	O	FL indication	
51	P72	G3	O	FL indication	
52	P73	G2	O	FL indication	
53	P74	G1	O	FL indication	
54	P75	N.C.			
55	P76	N.C.			
56	P77	N.C.			
57	P80	N.C.			
58	P81	N.C.			
59	P82	N.C.			
60	P83	P18	O	FL indication	

Pin	PORT	Signal name	I/O	Contents of control	
61	P84	P17	O	FL indication	
62	P85	P16	O	FL indication	
63	P86	P15	O	FL indication	
64	P87	P14	O	FL indication	
65	P90	P13	O	FL indication	
66	P91	P12	O	FL indication	
67	P92	P11	O	FL indication	
68	P93	P10	O	FL indication	
69	P94	P9	O	FL indication	
70	P95	P8	O	FL indication	
71	P96	P7	O	FL indication	
72	P97	P6	O	FL indication	
73	PD00	P5	O	FL indication	
74	PD01	P4	O	FL indication	
75	PD02	P3	O	FL indication	
76	PD03	P2	O	FL indication	
77	PD04	P1	O	FL indication	
78	VKK	-27V		Power supply for the FL drive	
79	P00/ SCK1	SCK	O	Serial bus clock output for DV747	
80	P01/SI1	SIN (M to F)	I	Serial bus data input for DV747	

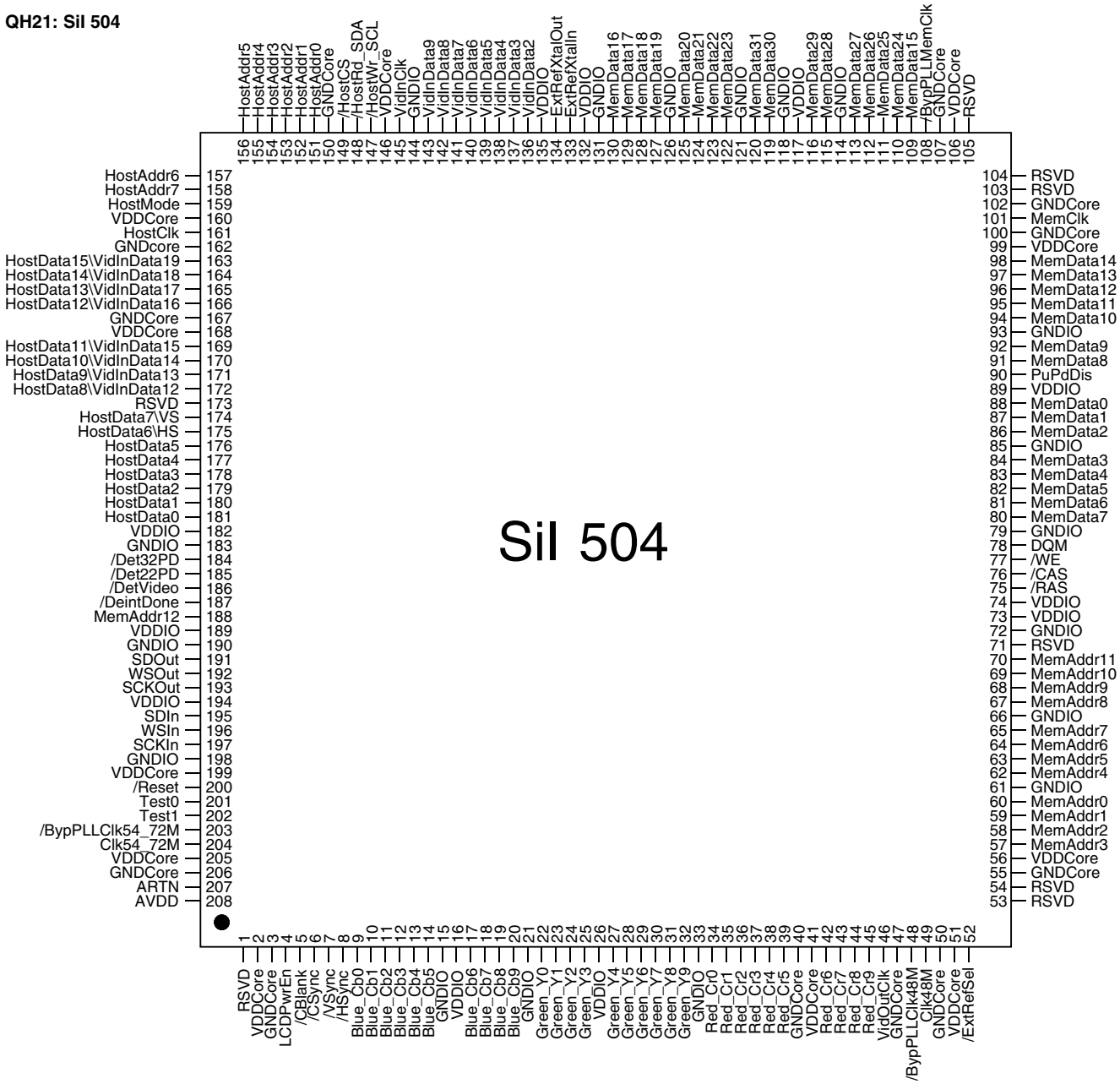
QI61:HD64F3672FX

No	Name	Port	I/O	Function
1	+5V	Avcc	-	
2	NC	NC	-	
3	NC	NC	-	
4		Vcl	-	
5	RESET	$\overline{RES}$	-	RESET
6	GND	TEST	-	
7	GND	Vss	-	
8	X2	OSC2	-	
9	X1	OSC1	-	
10	+5V	Vcc	-	
11		P50/$\overline{WKP0}$		
12		P51/$\overline{WKP1}$		
13		P52/$\overline{WKP2}$		
14		P53/$\overline{WKP3}$		
15		P54/$\overline{WKP4}$		
16	DVI_SW	P55/$\overline{WKP5}$/$\overline{ADTRG}$	I	Hi: ON, Low: soft control
17	V_EXPAND	P10	I	Hi: OFF, Low: ON
18	P_MONITOR	P11	I	Hi: Power ON, Low: Standby
19	SiI170RST	P12	O	
20	SiI504RST	P56	O	
21	DEINT	P57	I	
22	MSEN	P74/TMRIV	I	
23	DVSCL	P75/TMCIV	O	
24	DVSDA	P76/TMOV	IO	
25	MD	$\overline{NMI}$	I	
26	XDO	P80/FTCI	I	Front Microprocessor
27	XDIN	P81/FTIOA	O	Front Microprocessor
28	XSCL	P82/FTIOA	O	Front Microprocessor
29	XIRQ	P83/FTIOC	O	Front Microprocessor
30		P84/FTIOD		
31	E10T_0	E10T_0	-	For ET10T Emulator
32	E10T_1	E10T_1	-	For ET10T Emulator
33	E10T_2	E10T_2	-	For ET10T Emulator
34		P20/SCK3		
35	RXD	P21/RXD	I	RS-232C
36	TXD	P22/TXD	O	RS-232C
37	RTS	P14/$\overline{IRQ0}$	O	RS-232C
38	CTS	P15	I	RS-232C
39		P16	O	
40	XCS	P17/$\overline{IRQ3}$/TRGV	I	Front Microprocessor
41	NC	NC	-	
42	NC	NC	-	
43	NC	NC	-	
44	NC	NC	-	
45	GND	PB3/AN3	I	
46	GND	PB2/AN2	I	
47	GND	PB1/AN1	I	
48	GND	PB0/AN0	I	

Pin #	PIC Port	Type	Signal Name	Description
1	MCLR-	Input note 1	DVRESET-	Reset signal to both MC504 and SiI504 *(Requires Vih min =0.8$V_{DD,}$ NOT TTL)*
2	RA0	Bidir	DVSDA	Local Serial Port Data
3	RA1	Output	DVSCL	Local Serial Port Clock
4	RA2	Input TTL	SUBT-	Subtitle Detect: low = look for out-of-sequence subtitles, high = no subtitles
5	RA3	Input TTL	FILM-	Film Bias Mode: low = film bias mode, high = normal detection mode. **Do not set low unless this signal can be dynamically controlled.**
6	RA4	Input ST	PFDA-	PFDA Enabled: low = enable software assist, high = disable software-assist
7	RA5	Input TTL	SA	Serial Port Address Bit - tracks SiI504 Serial Address bit 0High selects address 0xEC, low selects address0xE2
8	VSS	Pwr/Gnd	VSS	Ground
9	OSC1	Input note 1	OSC1	Crystal Input 20MHz *(Requires Vih min =0.7$V_{DD,}$ NOT TTL)*
10	OSC2	Output	OSC2	Crystal Output 20MHz
11	RC0	Input ST	GMODE-	Game Mode enable: low = game mode enabled, high = disabled
12	RC1	Input ST	EXTGMD-	Game mode detect: low = external detect (pin 11), high = auto-detect
13	RC2	Input ST	RSVD1	**Always tie this pin High**
14	RC3	Bidir ST	SCL	External Serial Port Clock
15	RC4	Bidir ST	SDA	External Serial Port Data
16	RC5	Input ST	RSVD0	Reserved
17	RC6	Output	RSVD-TX	Reserved serial port transmit
18	RC7	Input ST	RSVD-RX	Reserved serial port receive
19	VSS	Pwr/Gnd	VSS	Ground
20	VDD	Pwr/Gnd	VDD	+5V
21	RB0	Input ST	DEINTDONE-	**Interrupt input pin. Connect to DeIntDone signal from SiI504, an open drain signal. Pull-up to 5V with 4.7K resistor** (*Requires Vih min =0.8$V_{DD,}$ NOT TTL*)
22	RB1	Input TTL	GPIO_0	General Purpose I/O pin 0
23	RB2	Output	PRMODE0	Processing mode encoding 0
24	RB3	Output	PRMODE1	Processing mode encoding 1
25	RB4	Input TTL	SQMODE-	Squeeze Mode: low = squeeze mode, high = normal
26	RB5	Input TTL	YPRPB-	Color Space Select: low = YPrPb, high = RGB
27	RB6	Input TTL	GPIO_1	General Purpose I/O pin 1
28	RB7	Input TTL	WAVE-	Wave (or Anti-burn-in) mode: low = enabled, high = disabled (Only relevant for squeeze mode.)

ST: Schmitt Trigger Input. See Section 4 for more details.
TTL: TTL level input. See Section 4 for more details.
Note 1: MCLR and OSC1 input levels are specified in Section 4.

QH21: Sil 504



Signal Group	Signal Name	Notes	Type	Description
Video Input	VidInData[9:2]	5V	In	Multiplexed Video Input Data (ITU-R BT.656, 8-bit & H/V syncs formats); Y (luma) Video Input Data (16-bit & H/V syncs format).
	VidInData[19:12] (HostData[15:8])	5V/PD	In	Chroma Video Input Data (16-bit & H/V syncs format only). See Host Interface pin list for pin functions when not used for video input.
	VS (HostData[7])	5V/PD	In	Vertical Sync input (8/16-bit & H/V syncs format only). See Host Interface pin list for pin function when not used for video input.
	HS (HostData[6])	5V/PD	In	Horizontal Sync input (8/16-bit & H/V syncs format only). See Host Interface pin list for pin function when not used for video input.
	VidInClk	5V	In	Video Input Clock, 27.0 MHz
Video Output	Red_Cr[9:0]		Out	Red Data (RGB output mode); Cr Data (YCrCb output mode)
	Green_Y[9:0]		Out	Green Data (RGB output mode); Y Data (YCrCb output mode)
	Blue_Cb[9:0]		Out	Blue Data (RGB output mode); Cb Data (YCrCb output mode)
	/HSync		Out	Horizontal Sync
	/VSync		Out	Vertical Sync
	/CSync		Out	Composite Sync
	/CBlank		Out	Composite Blank
	LCDPwrEn		Out	LCD Power Enable
	VidOutClk		Out	Video Output Clock, 36, 27 or 24 MHz
	Clk48M	5V	InOut	48 MHz Clock. Normally, this pin is a no-connect, outputting an internal PLL-generated 48.0 MHz clock and receiving that same clock through its input buffer. To bypass the PLL, set /BypPLLClk48M = 0, and supply a 48.0 MHz clock to the Clk48M pin.

Signal Group	Signal Name	Notes	Type	Description
Memory	/RAS		Out	SDRAM Row Address Strobe.
	/CAS		Out	SDRAM Column Address Strobe.
	/WE		Out	SDRAM Write Enable.
	DQM		Out	SDRAM Data Mask.
	MemData[31:0]	5V	InOut	SDRAM Data.
	MemAddr[12:0]	5V/PU/PD	InOut	SDRAM Address when an output. Configuration at reset when and input. See Memory Subsystem an Hardware Configuration sections of Functional Description for details. (Note: MemAddr12 is an output-only pin, does not have an internal pullup or pulldown, and is not part of the startup configuration.)
	MemClk	5V	InOut	SDRAM Clock. Normally, this pin is an InOut, outputting an internal PLL-generated 66.0 MHz or 72.0 MHz clock to the SDRAM and receiving that same clock through its input buffer. To bypass the PLL, set /BypPLLMemClk = 0, and supply a 66.0 MHz or 72.0 MHz clock to MemClk.
	/BypPLLMemClk	5V/PU	In	Bypass PLL for MemClk. Normally, this pin is a no-connect, and the internal pullup ensures that the PLL is enabled. To bypass the PLL, set /BypPLLMemClk = 0, and suppy a 66.0 MHz or 72.0 MHz clock to the MemClk pin
Host Interface	/HostWr_SCL	5V/H	In	186-Compatible Write when HostMode = 0. Serial Clock when HostMode = 1.
	/HostRd_SDA	5V/H	InOut	186-Compatible Read when HostMode = 0. Serial Data (InOut, open drain output) when HostMode = 1.
	/HostCS	5V/PU	In	186-Compatible Chip Select when HostMode=0. When HostMode=1, must be tied to VDD or pulled up to VDD.
	HostAddr[7:0]	5V/PD	In	186-Compatible Address when HostMode = 0. No connect when HostMode = 1.

QH21: Sil 504

Signal Group	Signal Name	Notes	Type	Description
Video Output (continued)	/BypPLLClk48M	PU	In	Bypass PLL for Clk48M. Normally, this pin is a no-connect, and the internal pullup ensures that the PLL is enabled. To bypass the PLL, set /BypPLLClk48M = 0, and supply a 48.0 MHz clock to the Clk48M pin.
	Clk54_72M	5V	InOut	54 or 72 MHz Clock. Normally, this pin is a no-connect, outputting an internal PLL-generated 54.0 MHz or 72.0 MHz clock and receiving that same clock through its input buffer. To bypass the PLL, set /BypPLLClk54_72M = 0, and supply a 54.0 or 72.0 MHz clock to the Clk54_72M pin. -
	/BypPLLClk54_72M	5V/PU	In	Bypass PLL for Clk54_72M. Normally, this pin is a no-connect, and the internal pullup ensures that the PLL is enabled. To bypass the PLL, set /BypPLLClk54_72M = 0, and supply a 54.0 MHz or 72.0 MHz clock to the Clk54_72M pin.
Audio/Video Synchronization	SDIn	5V/PD	In	Serial Digital Audio Input Data. See Audio/ Video Synchronization section of Functional Description for audio formats supported.
	WSIn	5V/PD	In	Serial Digital Audio Input Word Select. See Audio/Video Synchronization section for audio formats supported.
	SCKIn	5V/PD	In	Serial Digital Audio Input Clock. Frequency range of clock is 1.411 to 6.144 MHz. See Audio/Video Synchronization section for audio formats supported.
	SDOut		Out	Serial Digital Audio Output Data. Audio output follows audio input, with a delay equal to that of the video processing pipeline.
	WSOut		Out	Serial Digital Audio Output Word Select. Audio output follows audio input, with a delay equal to that of the video processing pipeline.
	SCKOut	5V/PD	In	Serial Digital Audio Output Clock. Same frequency as SCKIn. SDOut and WSOut are generated from SCKOut. See Audio/Video Synchronization section for more details on on audio clocking.

Signal Group	Signal Name	Notes	Type	Description
Host Interface (continued)	HostData[15:8] (VidInData[19:2])	5V/PD	InOut	186-Compatible Data when HostMode = 0. Chroma video input data (16-bit & H/V syncs format) when HostMode = 1.
	HostData[7] (VS)	5V/PD	InOut	186-Compatible Data when HostMode = 0. Vertical sync input (8/16-bit & H/V syncs format) when HostMode = 1.
	HostData[6] (HS)	5V/PD	InOut	186-Compatible Data when HostMode = 0. Horizontal sync input (8/16-bit & H/V syncs format) when HostMode = 1.
	HostData[5:0]	5V/PD	InOut	186-Compatible Data when HostMode = 0. No connnect when HostMode = 1.
	HostClk	5V	InOut	186-Compatible Clock (33.33 MHz max) when HostMode = 0. No Connect (27.0 MHz, InOut) when HostMode = 1. Note that when HostMode= 1, the clock output on HostClk is also received and used internally.
	HostMode	5V/PU	In	Serial Host Interface when HostMode = 1 (internal pullup defaults to this mode). 186-compatible host interface when HostMode = 0.
Video Processing Status	/Det32PD		Out	3:2 Pulldown Sequence Detected.
	/Det22PD		Out	2:2 Pulldown Sequence Detected.
	/DetVideo		Out	Interlaced Video Sequence Detected.
	/DeintDone		Out	Deinterlace processing complete for current field period. Opendrain output.
External APLL Reference Clock	/ExtRefSel	5V/PU	In	External APLL Reference Select. Internal pullup defaults pin to a 1, selecting VidInClk as the APLL reference clock. To select ExtRefXtalIn as the APLL reference clock, set /ExtRefSel to a 0.
	ExtRefXtalIn		In	External APLL Reference Crystal/oscillator Input.
	ExtRefXtalOut		Out	External APLL Reference Crystal Output.

Signal Group	Signal Name	Notes	Type	Description
Reset	/Reset	5V/H	In	Hardware Reset.
Test	Test[1:0]	5V/PD	In	Production hardware test support.
	PuPdDis	5V	In	Internal pullup and pulldown disable test function. Connect to ground for normal operation.
Power	AVDD		Pwr	1.8V Analog Power for PLL. (Qty: 1)
	ARTN		Pwr	Analog Return for PLLs. (Qty: 1)
	VDDCore		Pwr	1.8V Core Power. (Qty: 11)
	GNDCore		Pwr	Digital Ground for Core Power. (Qty: 12)
	VDDIO		Pwr	3.3V I/O Power. (Qty: 11)
	GNDIO		Pwr	Digital Ground for I/O Power. (Qty: 18)

Pin Descrtiption Notes:

1) A "/" preceding a signal name indicates that the signal is active low - i.e., that the signal is asserted or active when low. All other signals are active high.

2) Abbreviations in Notes column of pinout table:
- **5V**: 5 volt tolerant input
- **PU**: internal pullup
- **PD**: internal pulldown
- **H**: Hysteresis on input

3) The pins **HostData[15:6]** are used for two distinct functions. When **HostMode** = 0, these pins are 186-compatible data pins. When **HostMode** = 1, they may be either no connects, or are used for the non-656 video input port. This dual functionality is noted in the pin description table with the unused signal function name in parentheses, and in the Pin Number table and Pin Diagram with the dual pin function names separated by a backslash ("\").

4) Pins marked "Reserved" should be left unconnected - i.e., they should not be pulled up, pulled down, grounded, connected to a power supply source, or any other signal.

QI81:µPD4721

Truth Table

Driver

$\overline{STBY}$	D_{IN}	D_{OUT}	Remarks
L		Z	Standby mode (DC/DC converter is stopped)
H	L	H	Space level output
H	H	L	Mark level output

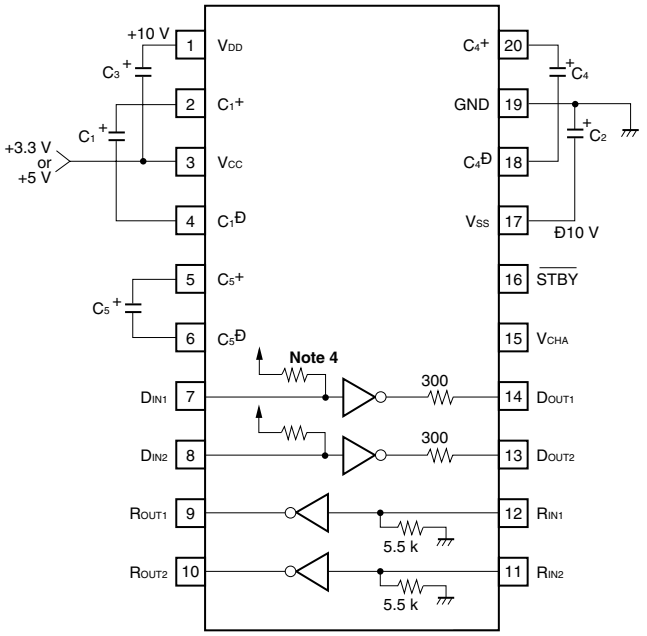
Receiver

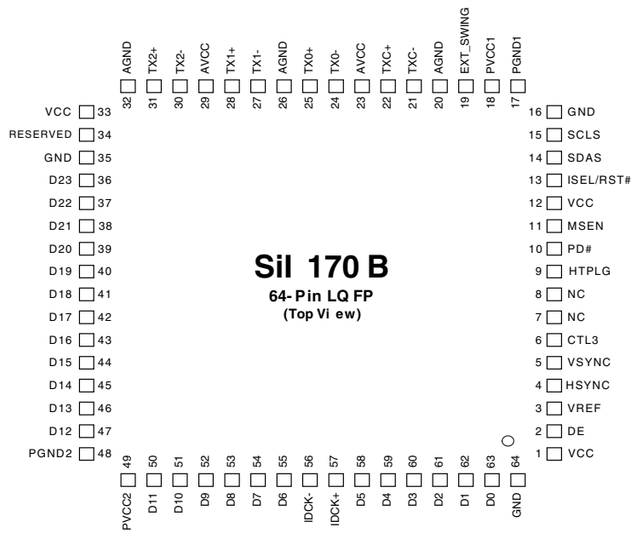
$\overline{STBY}$	R_{IN}	R_{OUT}	Remarks
L		H	Standby mode (DC/DC converter is stopped)
H	L	H	Mark level input
H	H	L	Space level input

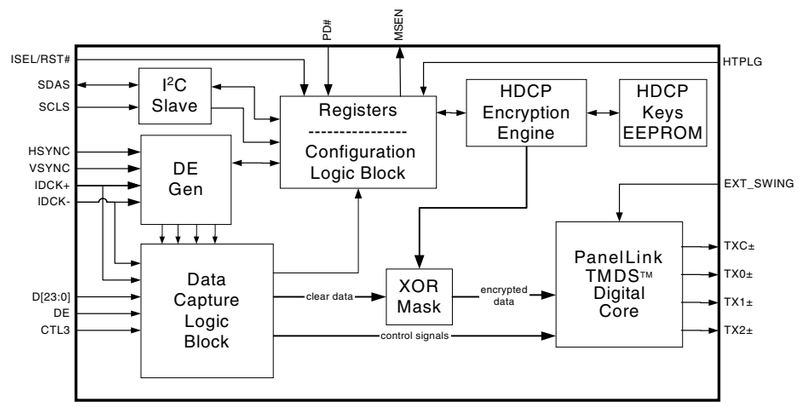
3 V 5 V switching

V_{CHA}	Operating mode
L	5 V mode (double step-up)
H	3 V mode (3 times step-up)

H: high-level, L: low-level, Z: high-impedance, : H or L







Functional Block Diagram

Input Pins

Pin Name	Pin #	Type	Description
D23-D12	See Pin Diagram	In	Upper 12 bits of 24-bit pixel bus. Mode controlled by configuration register bit: When BSEL = HIGH, this bus inputs the top half of the 24-bit pixel bus. When BSEL = LOW, these bits are not used to input pixel data. In this mode, the state of D[23:16] is input to the I²C register CFG. This allows an extra 8-bits of user configuration data to be read by the graphics controller through the I²C interface (see I²C register definition).
D11–D0	See Pin Diagram	In	Bottom half of 24-bit pixel bus / 12-bit pixel bus input. Mode controlled by configuration register bit: When BSEL = HIGH, this bus inputs the bottom half of the 24-bit pixel bus. When BSEL = LOW, this bus inputs ½ a pixel (12-bits) at every latch edge (both falling and/or rising) of the clock.
IDCK+	57	In	Input Data Clock +. This clock is used for all input modes.
IDCK-	56	In	Input Data Clock –. This clock is only used in 12-bit mode when dual edge clocking is turned off (DSEL = LOW). It is used to provide the ODD latching edges for multi-phased clocking. If (BSEL = HIGH) or (DSEL = HIGH) this pin is unused and should be tied to GND.
DE	2	In	Data enable. This signal is high when input pixel data is valid to the transmitter and low otherwise.
HSYNC	4	In	Horizontal Sync input control signal.
VSYNC	5	In	Vertical Sync input control signal.

Input Voltage Reference Pin

Pin Name	Pin #	Type	Description
VREF	3	Analog In	Must be tied to 3.3V.

Power Management Pin

Pin Name	Pin #	Type	Description
PD#	10	In	Power Down (active LOW). A HIGH level (3.3V) indicates normal operation and a LOW level (GND) indicates power down mode. During power down mode, the I²C pins are active, but digital input, output buffers and the PanelLink Digital core are powered down. This pin should be tied LOW to ensure the chip is powered off when RESET is asserted. When PD# is asserted, the differential output pins for TMDS are tri-stated until the PD# register bit is asserted through I²C.

Differential Signal Data Pins

Pin Name	Pin #	Type	Description
TX0+	25	Analog	TMDS Low Voltage Differential Signal output data pairs.
TX0-	24	Analog	These pins are tri-stated when PD# is asserted.
TX1+	28	Analog	
TX1-	27	Analog	
TX2+	31	Analog	
TX2-	30	Analog	
TXC+	22	Analog	TMDS Low Voltage Differential Signal output clock pairs.
TXC-	21	Analog	These pins are tri-stated when PD# is asserted.
EXT_SWING	19	Analog	Voltage Swing Adjust. A resistor should tie this pin to AVCC. This resistor determines the amplitude of the voltage swing. A 510 ohm resistor is recommended for remote display applications. For notebook computers, 680 ohm is recommended.

Configuration/Programming Pins

Pin Name	Pin #	Type	Description
MSEN	11	Out	Monitor Sense. This pin is an open collector output. The output is programmable through the I²C interface (see I²C register definitions). An external 5K pull-up resistor is required on this pin.
RESERVED	34	In	This pin is reserved for Silicon Image use only and should be tied LOW for normal operation.
NC	7,8	NC	These pins are not electrically connected inside the package.

Control Pins

These control pins allow configuration of the transmitter through the slave I²C port, which is required by HDCP.

Pin Name	Pin #	Type	Description
ISEL/RST#	13	In	I²C Interface Select. If HIGH, then the I²C interface is active.
SCLS 1	5	In	DDC I²C Clock. This pin is a slave I²C clock line which interfaces to the DDC bus for communicating with a host side master. HDCP KSV, A_n and R_i values are exchanged over this DDC bus during authentication. The clock may be run up to 400kHz. This pin is not 5V-tolerant; it should be connected through a level shifter to the DDC clock line SCL. This is an open-collector pin.
SDAS 1	4	In/Out	DDC I²C Data. This pin is a slave I²C data line for communicating with a host side master. HDCP KSV, A_n, and R_i values are exchanged over this DDC bus during authentication. Data may be clocked in at up to 400kHz. This pin is not 5V-tolerant; it should be connected through a level shifter to the DDC clock line SDA. This is an open-collector bi-directional pin, and is not made high-impedance when PD#=LOW.
CTL3	6	In	External CTL3. This pin is used to bring in the CTL3 signal for HDCP when the HDCP encryption is performed before the video enters the Sil 170. To enable this input, the CTL3 bit must be programmed in Reg[0x08]. If the CTL3 bit is cleared, then this input pin is ignored and may be left unconnected. This pin is a regular high swing (3.3V) input, containing a weak pull-down resistor so that if left unconnected it will default to LOW.
HTPLG	9	In	Monitor Charge Input. This pin is used to connect to the DVI Hot Plug pin to detect the presence of an attached monitor.

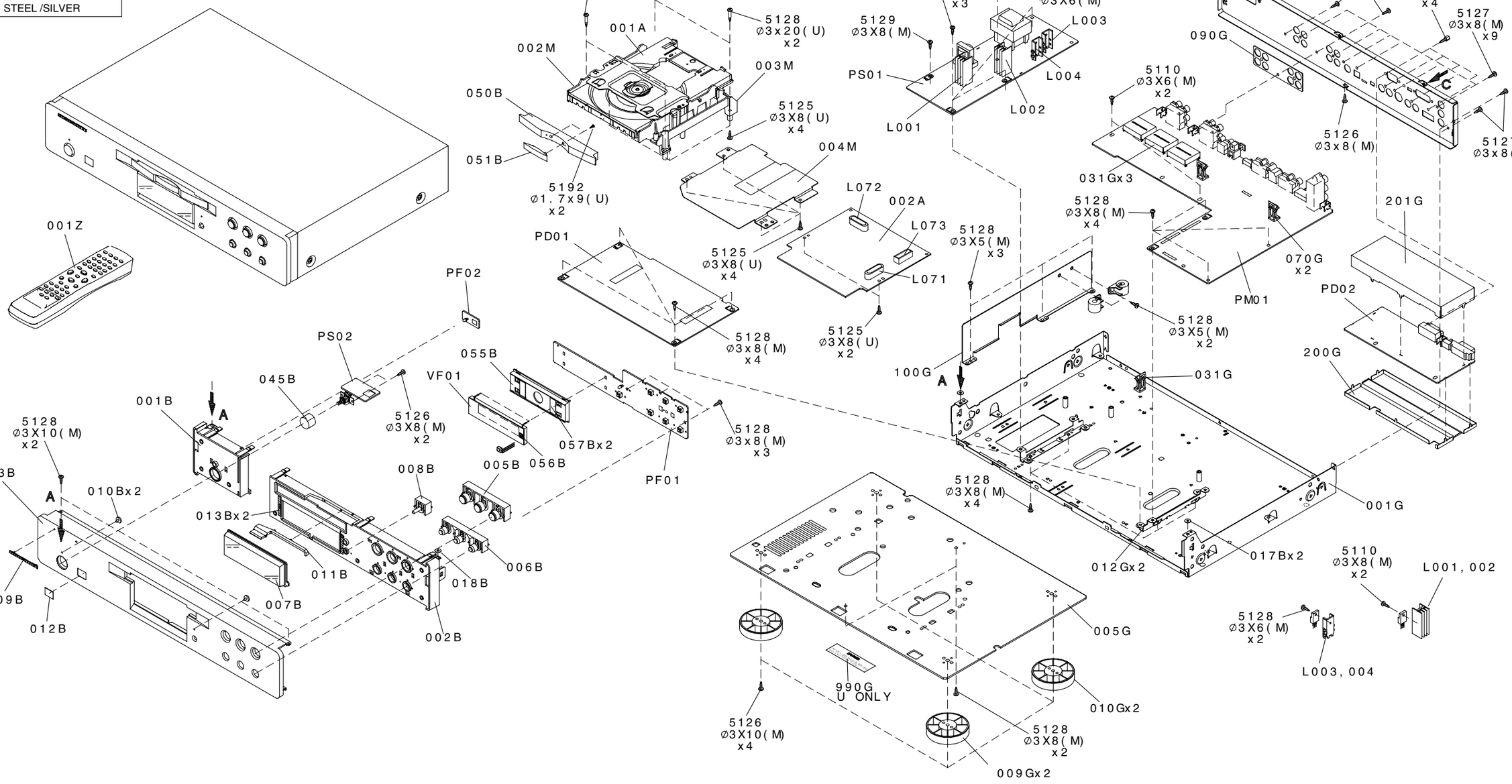
Power and Ground Pins

Pin Name	Pin #	Type	Description
VCC	1,12,33	Power	Digital VCC. Connect to 3.3V supply.
GND	16,35,64	Ground	Digital GND.
AVCC	23,29	Power	Analog VCC. Connect to 3.3V supply.
AGND	20,26,32	Ground	Analog GND.
PVCC1	18	Power	Primary PLL Analog VCC. Connect to regulated 3.3V supply.
PVCC2	49	Power	Filter PLL Analog VCC. Connect to regulated 3.3V supply.
PGND1	17	Ground	PLL Analog GND.
PGND2	48	Ground	PLL Analog GND.

13. EXPLODED VIEW AND PARTS LIST

SYMBOL	STYLE	PARTS NAME
5110		+B. H. M. SCREW
5125		+B. H. TAP TITE SCREW(P TYPE)
5126		+B. H. TAP TITE SCREW W/WASHER
5127		+P. H. TAP TITE SCREW(B TYPE)
5128		+B. H. TAP TITE SCREW(B TYPE)
5129		+B. H. TAP TITE SCREW(W/T. L. WASHER)
5192		+P. H. M. SCREW(MINUTE)
5405		TOOTHED LOCK WASHERS

MARK	MATERIAL/FINISH
(M)	STEEL/COPPER
(U)	STEEL/BLACK
(K)	STEEL/SILVER



POS. NO	VERS. COLOR	PART NO. (FOR EUR)	DESCRIPTION	PART NO. (MJI)
001B	SILVER	02AK105220	FRONT CHASSIS PL(L) SIL	02AK105220
002B	SILVER	02AK105230	FRONT CHASSIS PL(R) SIL	02AK105230
003B	BLACK	02AK248020	FRONT PANEL AL DV8400 BL	02AK248020
003B	GOLD	02AK248120	FRONT PANEL AL DV8400 GL	02AK248120
003B	SILVER	02AK248220	FRONT PANEL AL DV8400 SIL	02AK248220
005B	SILVER	02AK270210	BUTTON FUNCTION SIL	02AK270210
006B	SILVER	02AK270220	BUTTON SUB FUNK SIL	02AK270220
008B	SILVER	02AK270130	BUTTON FL OFF SIL	02AK270130
009B	SILVER	24AW251020	BADGE MARANTZ SILVER	24AW251020
012B	SILVER	02AK251030	BADGE SACD SILVER	02AK251030
045B	SILVER	02AK270240	BUTTON POWER SILVER	02AK270240
050B	SILVER	02AK063210	ESCUTCHEON TRAY FRONT SIL	02AK063210
051B	SILVER	392K063260	ESCUTCHEON SACD SIL	392K063260
009G	SILVER	383K057020	LEG FRONT SIL	383K057020
010G	SILVER	383K057120	LEG REAR SIL	383K057120
L071		FC90400010	FERRITE CORE SSC-40-12 FOR WD04	FC90400010
L072		FC90400010	FERRITE CORE SSC-40-12 FOR WD03	FC90400010
L073		FC90280010	FERRITE CORE HF70SH28X2X10 FOR WD05	FC90280010
WD05		nsp	JUMPER LEAD PD01(J711)-PD02(JH01)	YU16150520
WE01	/N	nsp	JUMPER LEAD PM01(J851)-PD02(J802)	YU12140520
			PACKING	
001T	/A/S	nsp	USER GUIDE DV8400 (A C L S)	11AK851350
001T	/F	nsp	USER GUIDE DV8400 (F)	11AK851110
001T	/N	11AK851310	USER GUIDE DV8400 (N)	11AK851310
001T	/U	nsp	USER GUIDE DV8400 (U)	11AK851250
005T	/N	11AK851320	USER GUIDE DV8400 (N)	11AK851320
			NOT STANDARD SPARE PARTS	
001D	SILVER	nsp	LID TOP COVER SILVER	349K257220
001S		nsp	PACKING CASE DV8400	11AK801010
002S		nsp	CUSHION DV8300	02AK809010

NOTE : "nsp" PART IS LISTED FOR REFERENCE ONLY, MARANTZ WILL NOT SUPPLY THESE PARTS.

POS. NO	VERS. COLOR	PART NO. (FOR EUR)	DESCRIPTION	PART NO. (MJI)
			PD01-Super Audio CD CIRCUIT BOARD	
			PD01-CAPACITORS	
C719		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
C720		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
Q715		HC10440050	IC TC7SH08FU 211931682	HC10440050
			PD01-RESISTORS	
R779 ∫ R787		nsp	CHIP RES. 47Ω ±5% 1/16W	NN05470610
			PD01-SEMICONDUCTOR	
Q716		HC006105K0	IC TC74VHC541FT	HC006105K0
			PD02-DVI CIRCUIT BOARD	
			PD02-CAPACITORS	
C801	/N	EY10700620	TANTL.CHIP 100µF 6.3V	EY10700620
C802	/N	EY10700620	TANTL.CHIP 100µF 6.3V	EY10700620
C803	/N	EY10700620	TANTL.CHIP 100µF 6.3V	EY10700620
C804	/N	EY47701020	TANTL.CHIP 470µF 10V	EY47701020
C805	/N	nsp	CER. CHIP 0.01µF	DK96103300
C806	/N	nsp	CER. CHIP 0.01µF	DK96103300
C950	/N	nsp	CER. CHIP 330pF	DK96331300
C951	/N	nsp	CER. CHIP 330pF	DK96331300
CH01		EY10601070	TANTL.CHIP 10µF 10V	EY10601070
CH02		EY10601070	TANTL.CHIP 10µF 10V	EY10601070
CH03		EY47600630	TANTL.CHIP 47µF 6.3V	EY47600630
CH04		EY10600670	TANTL.CHIP 10µF 6.3V SVSP0J	EY10600670
CH05		EY10600670	TANTL.CHIP 10µF 6.3V SVSP0J	EY10600670
CH06		EY47600630	TANTL.CHIP 47µF 6.3V	EY47600630
CH07		EY47600630	TANTL.CHIP 47µF 6.3V	EY47600630
CH21		EY22600630	TANTL.CHIP 22µF 6.3V	EY22600630
CH22 ∫ CH41		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CH42		nsp	CER. CHIP 2200pF CG 50V	DK96222300
CH43		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CH45		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CH46		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CH47		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CH71		nsp	CER. CHIP 2200pF CG 50V	DK96222300
CH72		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CH75		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CH76		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CI61		nsp	CER. CHIP 0.01µF	DK96103300
CI62		nsp	CER. CHIP 0.01µF	DK96103300
CI65		nsp	CER. CHIP 100pF	DD95101300
CI66		nsp	CER. CHIP 0.01µF	DK96103300
CI67		nsp	CER. CHIP 0.01µF	DK96103300
CI68		EY10601070	TANTL.CHIP 10/10V	EY10601070
CI69		nsp	CER. CHIP 0.01µF ±10% 50V	DK96103300
CI70		nsp	CER. CHIP 0.01µF	DK96103300
CI81		EY47502010	TANTL.CHIP 4.7µF 20V	EY47502010
CI82		nsp	CER. CHIP 0.01µF	DK96103300
CI83		EY47502010	TANTL.CHIP 4.7µF 20V	EY47502010
CI84		nsp	CER. CHIP 0.01µF	DK96103300
CI85		EY47502010	TANTL.CHIP 4.7µF 20V	EY47502010
CI86		nsp	CER. CHIP 0.01µF	DK96103300
CI87		EY47502010	TANTL.CHIP 4.7µF 20V	EY47502010
CI88		nsp	CER. CHIP 0.01µF	DK96103300
CI91		nsp	CER. CHIP 0.01µF	DK96103300
CI92		EY47502010	TANTL.CHIP 4.7µF 20V	EY47502010
CT03		EY10601070	TANTL.CHIP 10µF 10V	EY10601070

POS. NO	VERS. COLOR	PART NO. (FOR EUR)	DESCRIPTION	PART NO. (MJI)
CT04 ∫ CT07		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CT08		nsp	CER. CHIP 1000pF ±10 % B 50V	DK96102300
CT09		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CT10		EY10601070	TANTL.CHIP 10µF 10V	EY10601070
CT11		nsp	CER. CHIP 1000pF ±10 % B 50V	DK96102300
CT12		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CT13		EY10601070	TANTL.CHIP 10µF 10V	EY10601070
CT14		nsp	CER. CHIP 1000pF ±10 % B 50V	DK96102300
CT15		nsp	CER. CHIP 1000pF ±10 % B 50V	DK96102300
CT16		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CT17		EY10601070	TANTL.CHIP 10µF 10V	EY10601070
CT18		nsp	CER. CHIP 0.1µF GRM39F104Z16	DK98104200
CT19		EY10601070	TANTL.CHIP 10µF 10V	EY10601070
CT20		nsp	CER. CHIP 2200pF CG 50V	DK96222300
			PD02-RESISTORS	
R801	/N	nsp	CHIP RES. 39Ω ±5% 1/16W	NN05390610
R802	/N	nsp	CHIP RES. 33Ω ±5% 1/16W	NN05330610
R803	/N	nsp	CHIP RES. 39Ω ±5% 1/16W	NN05390610
R804	/N	nsp	CHIP RES. 33Ω ±5% 1/16W	NN05330610
R805	/N	nsp	CHIP RES. 39Ω ±5% 1/16W	NN05390610
R806	/N	nsp	CHIP RES. 33Ω ±5% 1/16W	NN05330610
R807	/N	nsp	CHIP RES. 39Ω ±5% 1/16W	NN05390610
R808	/N	nsp	CHIP RES. 33Ω ±5% 1/16W	NN05330610
R950	/N	nsp	CHIP RES. 100Ω ±5% 1/16W	NN05101610
R951	/N	nsp	CHIP RES. 100Ω ±5% 1/16W	NN05101610
RH01 ∫ RH09		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
RH21		nsp	CHIP RES. 22Ω ±5% 1/16W	NN05220610
RH22		nsp	CHIP RES. 22Ω ±5% 1/16W	NN05220610
RH23		nsp	CHIP RES. 22Ω ±5% 1/16W	NN05220610
RH24		BW05100010	RES.COMPO. CN1J8TD10J	BW05100010
RH25		BW05100010	RES.COMPO. CN1J8TD10J	BW05100010
RH26		BW05100010	RES.COMPO. CN1J8TD10J	BW05100010
RH27		nsp	CHIP RES. 22Ω ±5% 1/16W	NN05220610
RH28		nsp	CHIP RES. 4.7kΩ ±5% 1/16W	NN05472610
RH29		nsp	CHIP RES. 10kΩ ±5% 1/16W	NN05103610
RH30		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
RH31		nsp	CHIP RES. 100Ω ±5% 1/16W	NN05101610
RH71		nsp	CHIP RES. 100Ω ±5% 1/16W	NN05101610
RH72		nsp	CHIP RES. 2.2kΩ ±5% 1/16W	NN05222610
RH73		nsp	CHIP RES. 2.2kΩ ±5% 1/16W	NN05222610
RH75		nsp	CHIP RES. 10kΩ ±5% 1/16W	NN05103610
RH76		nsp	CHIP RES. 10kΩ ±5% 1/16W	NN05103610
RH77		nsp	CHIP RES. 10kΩ ±5% 1/16W	NN05103610
RH78		nsp	CHIP RES. 1MΩ ±5% 1/16W	NN05105610
RH79		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
RH80		nsp	CHIP RES. 2.2kΩ ±5% 1/16W	NN05222610
RH81		nsp	CHIP RES. 2.2kΩ ±5% 1/16W	NN05222610
RH82		nsp	CHIP RES. 4.7kΩ ±5% 1/16W	NN05472610
RI51		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
RI52		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
RI53		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
RI54		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
RI55		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
RI61		nsp	CHIP RES. 4.7kΩ ±5% 1/16W	NN05472610
RI62		nsp	CHIP RES. 10kΩ ±5% 1/16W	NN05103610
RI63		nsp	CHIP RES. 10kΩ ±5% 1/16W	NN05103610
RI64		nsp	CHIP RES. 4.7kΩ ±5% 1/16W	NN05472610
RI65		nsp	CHIP RES. 4.7kΩ ±5% 1/16W	NN05472610
RI66		nsp	CHIP RES. 4.7kΩ ±5% 1/16W	NN05472610
RI67		nsp	CHIP RES. 4.7kΩ ±5% 1/16W	NN05472610

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POS. NO	VERS. COLOR	PART NO. (FOR EUR)	DESCRIPTION	PART NO. (MJI)
RI68		nsp	CHIP RES. 100Ω ±5% 1/16W	NN05101610
RI81		nsp	CHIP RES. 22kΩ ±5% 1/16W	NN05223610
RI82		nsp	CHIP RES. 22kΩ ±5% 1/16W	NN05223610
RI91				
∫		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
RI94				
RI95		nsp	CHIP RES. 1MΩ ±5% 1/16W	NN05105610
RI96		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
RT01		nsp	CHIP RES. 10kΩ ±5% 1/16W	NN05103610
RT02		nsp	CHIP RES. 10kΩ ±5% 1/16W	NN05103610
RT04		nsp	CHIP RES. 4.7kΩ ±5% 1/16W	NN05472610
RT07		nsp	CHIP RES. 1kΩ ±5% 1/16W	NN05102610
RT08		nsp	CHIP RES. 68kΩ ±5% 1/16W	NN05683610
RT11		nsp	CHIP RES. 470Ω ±5% 1/16W	NN05471610
RT16		nsp	CHIP RES. 4.7kΩ ±5% 1/16W	NN05472610
RT17		nsp	CHIP RES. 4.7kΩ ±5% 1/16W	NN05472610
RT18		nsp	CHIP RES. 2.2kΩ ±5% 1/16W	NN05222610
RT19		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
RT20		nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
			PD02-SEMICONDUCTORS	
D801				
∫	/N	HZ30034050	CHIP DIODE 01ZA8.2	HZ30034050
D804				
DT01		HI10104210	L.E.D. CHIP SML-310MT GREEN	HI10104210
DT02		HZ20039050	CHIP DIODE 1SS378	HZ20039050
DT03		HZ20039050	CHIP DIODE 1SS378	HZ20039050
⚠ QH01		HC98J18210	IC BA18BC0FP-E2 1.8V REG.	HC98J18210
QH21		HC10231990	IC SII504	HC10231990
QH22		HC10001910	IC K4S643232E-TC60	HC10001910
QH71		HS11AKX000	ONE TIME PROM MC504-F2(PIC16C63A-20/SO)	HS11AKX000
QI61		HS11AKH00F	ONE TIME PROM 11AK SUB UCOM VER.1.00	HS11AKH00F
QI62		HC10224210	IC BD4742G	HC10224210
QI81		HC10292060	IC UPD4721	HC10292060
QT02		HX300012A0	CHIP TRS. 2SC4116	HX300012A0
QT03		HC10230990	IC SII170B	HC10230990
QT04		HX300012A0	CHIP TRS. 2SC4116	HX300012A0
QT05		HF70013000	F.E.T. BSN20	HF70013000
QT06		HF70013000	F.E.T. BSN20	HF70013000
			PD02-MISCELLANEOUS	
JI91		YP11000220	PLUG DZ101A1-B2	YP11000220
JT01		YT02240010	TERMINAL QH11121-DPO	YT02240010
JT02		nsp	TERMINAL M1698-A NEJI	YL01010320
L801				
∫	/N	nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
L806				
L950	/N	nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
L951	/N	nsp	CHIP RES. 0Ω ±5% 1/16W	NN05000610
LH01				
∫		LU12222010	CHIP INDUCTANCE	LU12222010
LH05			NL322522-2R2M	
LH21		FN31010060	BLM11P600S	FN31010060
LI61		FN31010060	BLM11P600S	FN31010060
LI81		FN31010060	BLM11P600S	FN31010060
LI91				
LI93		FN31000020	BLM11B252SD	FN31000020
LI94				
LT01				
∫		FC90020110	FERRITE CORE BLM11B601S	FC90020110
LT04				

POS. NO	VERS. COLOR	PART NO. (FOR EUR)	DESCRIPTION	PART NO. (MJI)
SI61		SS02021680	SLIDE SWITCH SSSF021300	SS02021680
SI62		SS01021140	SLIDE SWITCH SSAA110300	SS01021140
XH71		FQ02005070	CERAMIC VIB. CSTCE20M0V53-R0	FQ02005070
XI62		FQ01605110	CERAMIC VIB. CSTCE16M0V51-R0	FQ01605110
			PF01-FRONT CIRCUIT BOARD	
			PF01-CAPACITORS	
CF51				
∫		nsp	CER. CHIP 100pF ±5 % CG 50V	DD95101300
CF55				
QF01		*HS11AKT0R	IC TMP87PM74F ONE TIME PROM BRANK	*HS11AKT0R
QF04		HC10224210	IC BD4742G	HC10224210
			PF01-RESISTORS	
RF61				
∫		nsp	CHIP RES. 22Ω ±5% 1/16W	NN05220610
RF65				
RF66		nsp	CHIP RES. 4.7kΩ ±5% 1/16W	NN05472610
			PM01-AV CIRCUIT BOARD	
			PM01-CAPACITORS	
C859	/N	nsp	ELECT. 10µF M 63V RA-2	OA10606320
C868	/N	nsp	ELECT. 10µF M 63V RA-2	OA10606320
C877	/N	nsp	ELECT. 10µF M 63V RA-2	OA10606320
C880	/N	nsp	ELECT. 10µF M 63V RA-2	OA10606320
C881	/N	nsp	ELECT. 10µF M 63V RA-2	OA10606320
C882	/N	nsp	ELECT. 10µF M 63V RA-2	OA10606320
C884	/N	nsp	ELECT. 10µF M 63V RA-2	OA10606320
CB08		nsp	ELECT. 10µF M 63V RA-2	OA10606320
CB09		nsp	ELECT. 470µF M 10V RA-2	OA47701020
CB11	/A/F/S	nsp	ELECT. 470µF M 10V RA-2	OA47701020
CC08		nsp	ELECT. 10µF M 63V RA-2	OA10606320
CC09		nsp	ELECT. 470µF M 10V RA-2	OA47701020
CC11	/A/F/S	nsp	ELECT. 470µF M 10V RA-2	OA47701020
CD03		nsp	ELECT. 1µF M 100V RA-2	OA10510020
CD05		nsp	ELECT. 1µF M 100V RA-2	OA10510020
CD23		nsp	ELECT. 1µF M 100V RA-2	OA10510020
CD25		nsp	ELECT. 1µF M 100V RA-2	OA10510020
CD43		nsp	ELECT. 1µF M 100V RA-2	OA10510020
CD45		nsp	ELECT. 1µF M 100V RA-2	OA10510020
CI05		nsp	ELECT. 1µF M 100V RA-2	OA10510020
CI20		nsp	ELECT. 47µF M 25V RA-2	OA47602520
CV03		nsp	ELECT. 1µF M 100V RA-2	OA10510020
CV32		nsp	ELECT. 10µF M 63V RA-2	OA10606320
CV34		nsp	ELECT. 10µF M 63V RA-2	OA10606320
CY09		nsp	ELECT. 10µF M 63V RA-2	OA10606320
			PS01-POWER SUPPLY CIRCUIT BOARD	
			PC01-CAPACITORS	
CP13		nsp	ELECT. 1µF M 100V RA-2	OA10510020
CP52		nsp	ELECT. 47µF M 25V RA-2	OA47602520
CP53		nsp	ELECT. 47µF M 25V RA-2	OA47602520
CP54		nsp	ELECT. 220µF M 25V RA-2	OA22702520
CP55		nsp	ELECT. 220µF M 25V RA-2	OA22702520
CP59		nsp	ELECT. 10µF M 63V RA-2	OA10606320
CP61		nsp	ELECT. 47µF M 25V RA-2	OA47602520

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