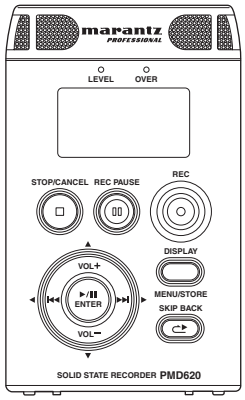
For U.S.A., Canada, Europe, China & Japan model

marantz PROFESSIONAL

SERVICE MANUAL

MODEL PMD620

Handheld Solid State Recorder



Please use this service manual with referring to the user guide (D.F.U.) without fail.
修理の際は、必ず取扱説明書を準備し操作方法を確認の上作業を行ってください。

D&M Holdings Inc.
PROFESSIONAL BUSINESS COMPANY

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Part no. 00M10CS855010
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SECTION **PAGE**

The exchange of the lithium battery(Z701 : CR1220/IFC).

CAUTION

Danger of explosion if battery is incorrectly replaced.
Replace only with the same or equivalent type.

リチウム電池 (Z701 : CR1220/IFC) の交換について

注意

電池を誤って交換すると爆発する危険があります。
同一又は同等の型のものにのみ交換してください。

1. TECHNICAL SPECIFICATIONS

Digital Audio System

System.....Solid State Recorder
Usable media.....SD/SDHC cards
Recording format
  MP3.....MPEG1 LayerⅢ Compression
  WAV .....16/24 bit linear PCM
Recording MP3 bit-rate
  Stereo.....192/128/64 kbps
  Mono .....96/64/32 kbps
Sample rate .....44.1/48 kHz
Number of channels .....2 (Stereo)/1 (Mono)

Audio Performance

Frequency response.....20 Hz - 20 kHz (±1dB)
S/N ratio IEC-A weighted
  MIC.....68 dB
  LINE .....80 dB
Total harmonic distortion at 0 VU
  MIC.....0.06%
  LINE 0.02%
Dynamic range .....81 dB

Inputs

External MIC
  Type .....1/8" stereo jack
  Input sensitivity.....6 mVrms/30 kohms
LINE
  Type .....1/8" stereo jack
  Input sensitivity.....500 mVrms/20 kohms

Outputs

LINE
  Type .....1/8" stereo jack
  Standard level .....1.0 V/10 kohms
Headphone
  Type .....1/8" stereo jack
  Standard level .....16 mW/16 ohms
Speaker
  Standard level .....150 mW/8 ohms

General

Power consumption
  Recording/Playback .....1.5 W (DC)
  Battery life (Alkaline) .....5 hours (Typical)
  Phantom power .....5V, 1mA (Max.)
Environmental conditions
  Operational temperature .....0 - 40°C (32 - 104°F)
  Operational humidity .....25 - 85% (no condensation)
  Storage temperature .....–20 - 60°C (–4 - 140°F)
Dimensions
  Width .....62 mm (2.5")
  Height.....102 mm (4")
  Depth.....25 mm (1")
  Weight (Excl. batteries) .....110g (4 oz)

Included Accessories

Audio cable
USB cable
AC adapter
User guide
CD-ROM (U, N only)
Handy strap
Customer Registration Document (US only)
Tripod/Belt clip adapter
SD card

• Specifications are subject to change without notice.

2. SERVICE MENU

2. SERVICE メニュー

<Service Menu Details>
<サービスメニューの内容>

Display Menu 表示メニュー	Service Details サービス内容
1 OLED Check	Check the display section by lighting all OLED. OLEDの全点灯により、表示部を確認します。
2 LED Check	Check the LED by lighting all LED. LEDの全点灯により、LEDを確認します。
3 Door Sense	Set the door sensor ON/OFF. ドアセンサのON/OFFを設定します。
4 Heat Run	Perform a heat run test by using continuous play. 連続再生によりヒートラン試験を行います。
5 Factory Default	Return to the factory default settings. 工場出荷状態に戻します。

2.1 OLED Check

1) Press the **REC PAUSE** button and **REC LEVEL –** button at the same time, and turn the **POWER slide** switch ON. At this time, the service menu list is displayed in the display section.
2) Press the **VOL +** and **VOL –** buttons to select "OLED Check". At this time, the selected menu item is highlighted.
3) If the ►/**II**/**ENTER** button is pressed, all of the OLED light.
   - If the I◄◄ button is pressed while all OLEDs are lit, the display returns to the service menu list.
   - If the ►/**II**/**ENTER** button is pressed while all OLEDs are lit, the display returns to the service menu list.

2.1 OLEDチェック

1) **REC PAUSE**ボタンと**REC LEVEL –**ボタンを同時に押しながら、**POWER slide**スイッチをOnします。このとき、表示部にサービスメニュー一覧が表示されます。
2) **VOL +**ボタンおよび**VOL –**ボタンを押して、"OLED Check" を選択します。このとき、選択したメニューがハイライト表示されます。
3) ►/**II**/**ENTER**ボタンを押すと、OLEDが全点灯します。
   - OLEDが全点灯中にI◄◄ボタンを押すと、サービスメニュー一覧に戻ります。
   - OLEDが全点灯中に►/**II**/**ENTER**ボタンを押すと、サービスメニュー一覧に戻ります。

2.2 LED Check

1) Press the **REC PAUSE** button and **REC LEVEL –** button at the same time, and turn the **POWER slide** switch ON. At this time, the service menu list is displayed in the display section.
2) Press the **VOL +** and **VOL –** buttons to select "LED Check". At this time, the selected menu item is highlighted.
3) If the ►/II/**ENTER** button is pressed, "∗" is displayed on the back of "LED Check", and all LEDs light (REC, OVER, LEVEL, REMOTE RED, REMOTE GREEN).
   - If the I◄◄ button is pressed while all LEDs are lit, all LEDs go off, and the display returns to the service menu list.
   - If the ►/II/**ENTER** button is pressed while all LEDs are lit, all LEDs go off, the "∗" display switches off, and the display returns to the service menu list.

2.2 LEDチェック

1) **REC PAUSE**ボタンと**REC LEVEL –**ボタンを同時に押しながら、**POWER slide**スイッチをOnします。このとき、表示部にサービスメニュー一覧が表示されます。
2) **VOL +**ボタンおよび**VOL –**ボタンを押して、"LED Check"を選択します。このとき、選択したメニューがハイライト表示されます。
3) ►/II/**ENTER**ボタンを押すと、メニューの"LED Check"の後ろに"∗"が表示され、LEDが全点灯(REC、OVER、LEVEL、REMOTE RED、REMOTE GREEN)します。
   - LEDが全点灯中に I◄◄ボタンを押すと、LEDを全消灯させ、サービスメニュー一覧に戻ります。
   - LEDが全点灯中に ►/II/**ENTER** ボタンを押すと、LEDを全消灯させ、"∗"表示を消灯しサービスメニュー一覧に戻ります。

2.3 Door Sence

1) Press the **REC PAUSE** button and **REC LEVEL –** button at the same time, and turn the **POWER slide** switch ON. At this time, the service menu list is displayed in the display section.
2) Press the **VOL +** and **VOL –** buttons to select "Door Sence". At this time, the selected menu item is highlighted.
3) If the ►/II/**ENTER** button is pressed, the PMD620 sensor is set to OFF.
   - At this time, "Executing…" is displayed in the display section.
   - If the settings are completed, "Completed" is displayed in the display section for 1 second, the display returns to the service menu and "Door Sense OFF" is displayed.

   If the ►/II/**ENTER** button is pressed while "Door Sense OFF" is displayed, the PMD620 sensor is set to ON.

2.3 ドアセンサの設定

1) **REC PAUSE**ボタンと**REC LEVEL –**ボタンを同時に押しながら、**POWER slide**スイッチをOnします。このとき、表示部にサービスメニュー一覧が表示されます。
2) **VOL +**ボタンおよび**VOL –**ボタンを押して、"Door Sense ON"を選択します。このとき、選択したメニューがハイライト表示されます。
3) ►/II/**ENTER**ボタンを押すと、PMD620をセンサOFF状態に設定します。
   - このとき、表示部に"Executing..."が表示されます。
   - 設定が完了すると、表示部に"Completed"が1秒間表示され、サービスメニューに戻り"Door Sense OFF"が表示されます。

   "Door Sense OFF"表示しているときに►/II/**ENTER**ボタンを押すと、PMD620をセンサON状態に設定します。

2.4 Heat Run

1) Press the **REC PAUSE** button and **REC LEVEL –** button at the same time, and turn the **POWER slide** switch ON. At this time, the service menu list is displayed in the display section.
2) Press the **VOL +** and **VOL –** buttons to select “Heat Run”. At this time, the selected menu item is highlighted.
3) If the ►/II/**ENTER** button is pressed, continuous play starts.
   - During continuous play, all switches other than the **POWER slide** switch are inactive.
   - During playback, if playback continues to the final file, all files are repeated and playback continues from the first file.
   - If an error occurs during continuous playback, the display remains in the error display status.

2.4 ヒートラン実行

1) **REC PAUSE**ボタンと**REC LEVEL –**ボタンを同時に押しながら、**POWER slide**スイッチをOnします。このとき、表示部にサービスメニュー一覧が表示されます。
2) **VOL +**ボタンおよび**VOL –**ボタンを押して、“Heat Run” を選択します。このとき、選択したメニューがハイライト表示されます。
3) ►/II/**ENTER**ボタンを押すと、連続再生が始まります。
   - 連続再生中は、**POWER slide**スイッチ以外は無効です。
   - 連続再生では、最後のファイルまで再生が実行すると、最初のファイルへ戻りオールリピートします。
   - 連続再生中にエラーが発生したときは、エラー表示状態のままになります。

2.5 Factory Default

1) Press the **REC PAUSE** button and **REC LEVEL –** button at the same time, and turn the **POWER slide** switch ON. At this time, the service menu list is displayed in the display section.
2) Press the **VOL +** and **VOL –** buttons to select “Factory Default?”. At this time, the selected menu item is highlighted.
3) If the ►/II/**ENTER** button is pressed “Default?” is displayed in the display section.
4) While “Default?” is being displayed, press the I◄◄ button and select “YES”.
5) If the ►/II/**ENTER** button is pressed “Executing…” flashes in the display section.
   - When the settings have returned to the factory default settings, “Completed” is displayed for 1 second, after which the display section returns to the service menu.
   - When the settings have been returned to the factory default settings, the “Date Form” default setting is the setting for the US. This needs to be set correctly for the destination.

   “Date Form”
   US : M/D/Y
   Europe : D/M/Y
6) Turn the **POWER slide** switch OFF.

2.5 工場出荷状態へ戻す

1) **REC PAUSE**ボタンと**REC LEVEL –**ボタンを同時に押しながら、**POWER slide**スイッチをOnします。このとき、表示部にサービスメニュー一覧が表示されます。
2) **VOL +**ボタンおよび**VOL –**ボタンを押して、“Factory Default?” を選択します。このとき、選択したメニューがハイライト表示されます。
3) ►/II/**ENTER**ボタンを押すと、表示部に“Default?”が表示されます。
4) “Default?” が表示中に、I◄◄ ボタンを押して、“YES” を選択します。
5) ►/II/**ENTER**ボタンを押すと、表示部に“Executing...” が点滅表示されます。
   - 工場出荷状態への設定が完了すると、表示部に“Completed”が1秒間表示され、サービスメニューに戻ります。
   - 工場出荷状態へ戻した場合、“Date Form”のデフォルト設定はUS向けの設定となります。出荷先に応じた設定が必要です。

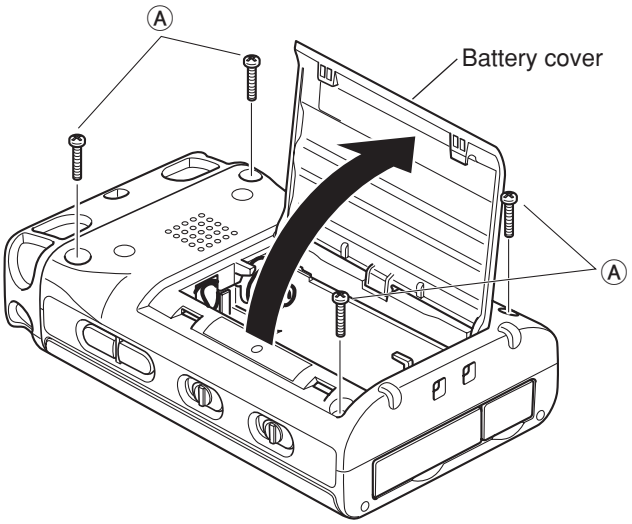
   “Date Form”
   US : M/D/Y
   Europe : D/M/Y
6) **POWER slide**スイッチをOFFします。

3. HOW TO DISASSEMBLE

1) Open the battery cover on the back of the main unit, and remove the 4 "Ⓐ" screws.

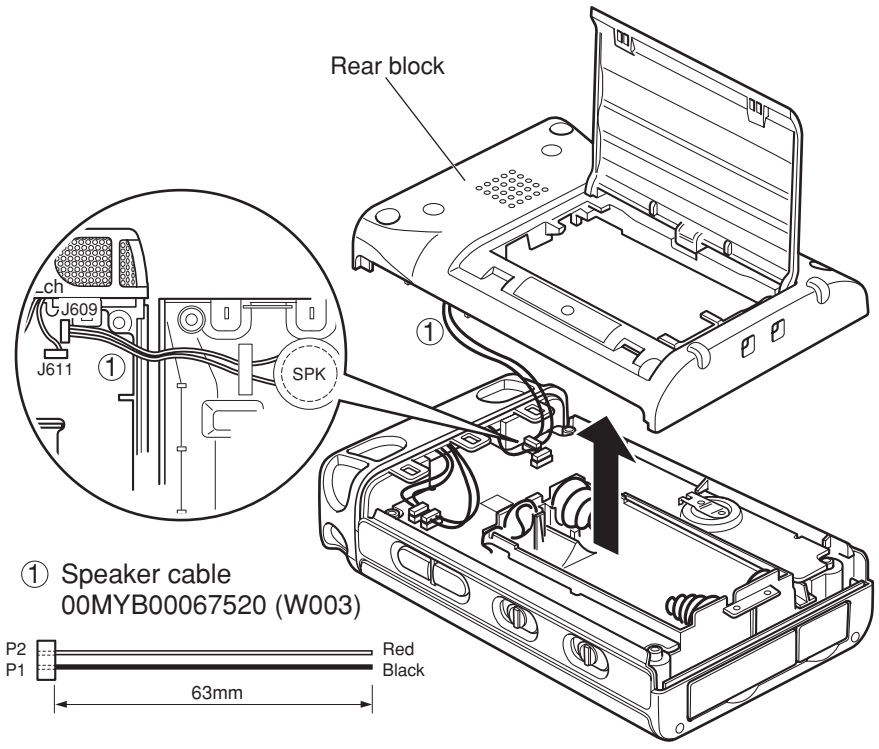
3. 分解方法

1) 本体背面のバッテリーカバーを開き、ネジⒶ 4本を外します。



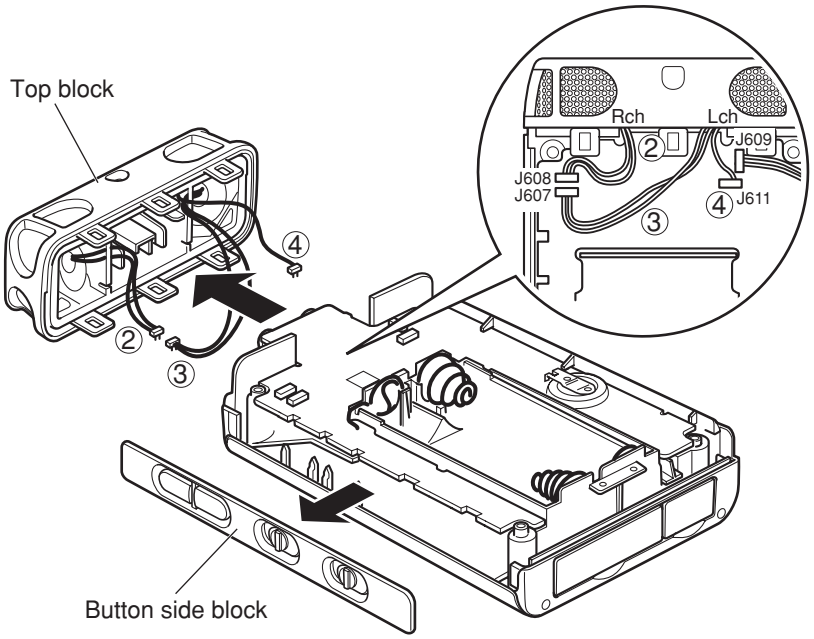
2) Lift the rear block slowly in the direction of the arrows, disconnect the speaker cable ① connector from J609 as shown in the diagram below to remove the rear block.

2) リアブロックをゆっくり矢印の方向へ持ち上げ、下図のようにスピーカケーブル①のコネクタ1ヶ所をJ609から外すと、リアブロックが取り外せます。

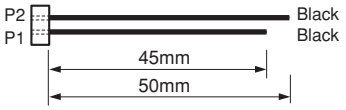


3) As shown in the diagram below, disconnect the Mic Rch cable ② connector from J608, the Mic Lch cable ③ connector from J607, and the Mic shield cable ④ connector from J611, and the top block can now be removed. Also remove the button side block in the direction of the arrow.

3) 下図のようにMic Rchケーブル②のコネクタをJ608から外し、Mic Lch ケーブル③のコネクタをJ607から外し、Mic シールドケーブル④のコネクタをJ611から外すと、トップブロックが取り外せます。またボタンサイドブロックも矢印方向に取り外します。

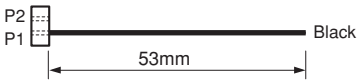


② Mic Rch cable
00MYB00051800 (W002)



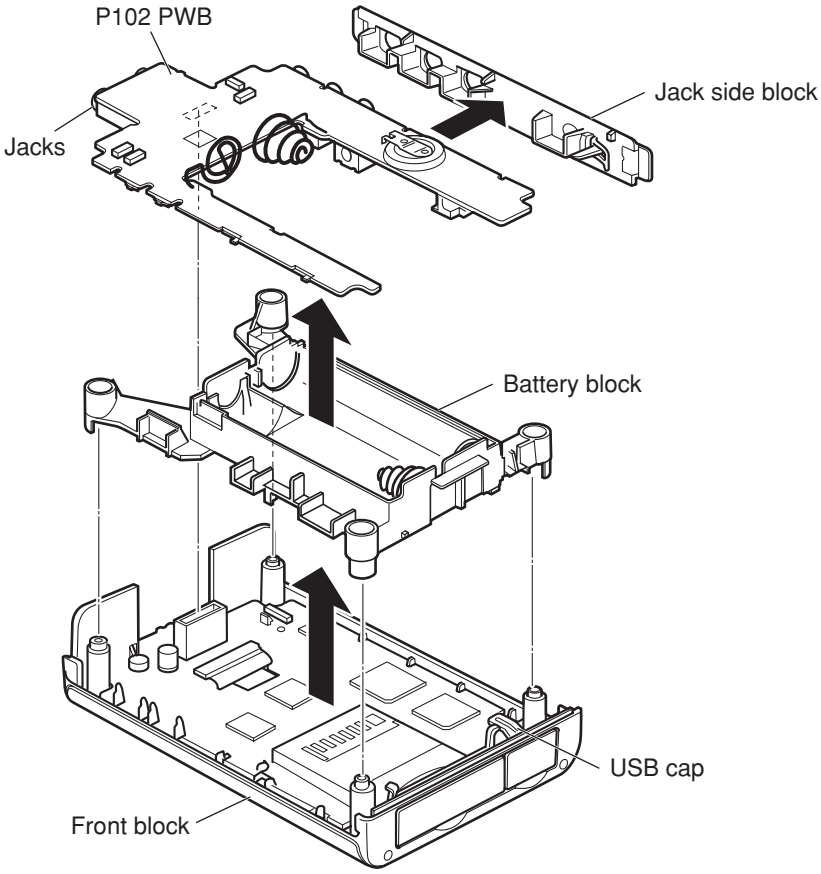
③ Mic Lch cable
00MYB00067540 (W001)

④ Mic shield cable
00MYB00051790 (W004)



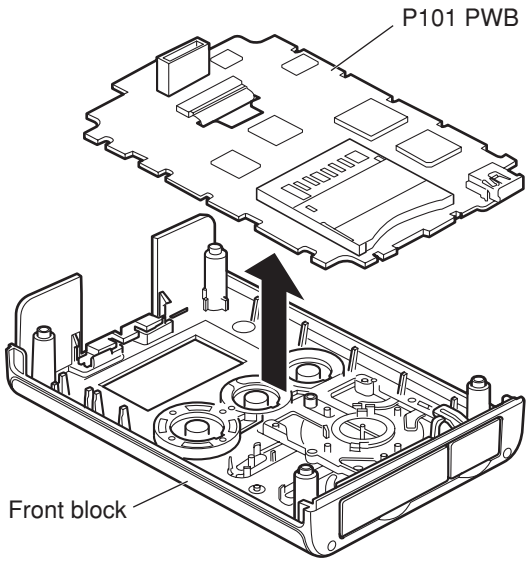
4) Lift the P102 jack section, and remove the P102 board from the battery block in the direction of the arrow. Also, the jack side block can be removed. The battery block is held in place by the foot of the USB cap. Remove the USB cap foot, and remove the battery block from the front block in the direction of the arrow.

4) P102のジャック部分を持ち上げてバッテリブロックからP102基板を矢印方向に取り外します。またジャックサイドブロックも取り外せます。USBキャップの足でバッテリブロックが固定されています。このUSBキャップの足を外して、フロントブロックからバッテリブロックを矢印方向に取り外します。



5) Remove the P101 board from the front block in the direction of the arrow, as shown in the diagram below.

5) 下図のようにフロントブロックからP101基板を矢印方向に取り外します。



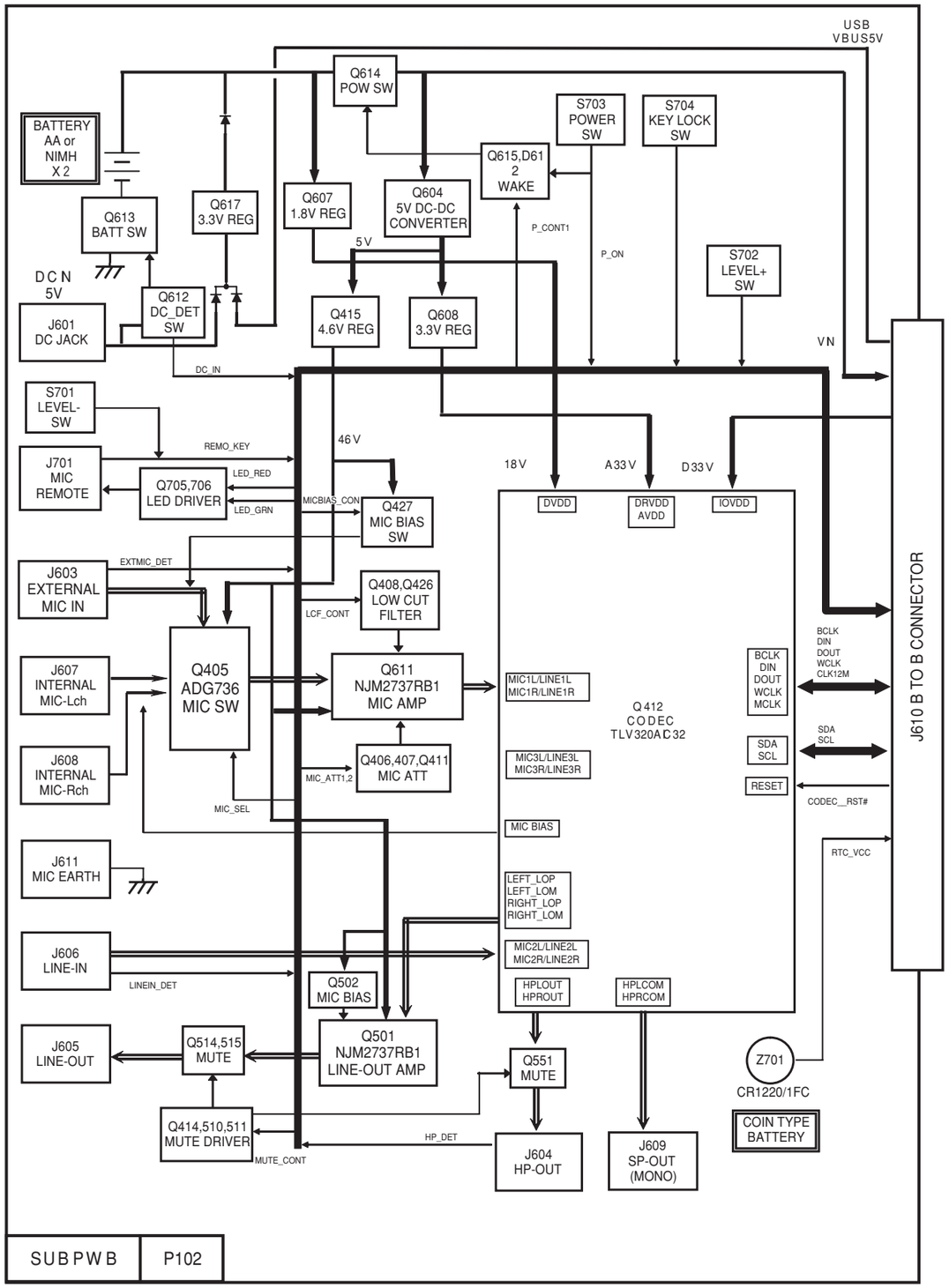
4. Version Update

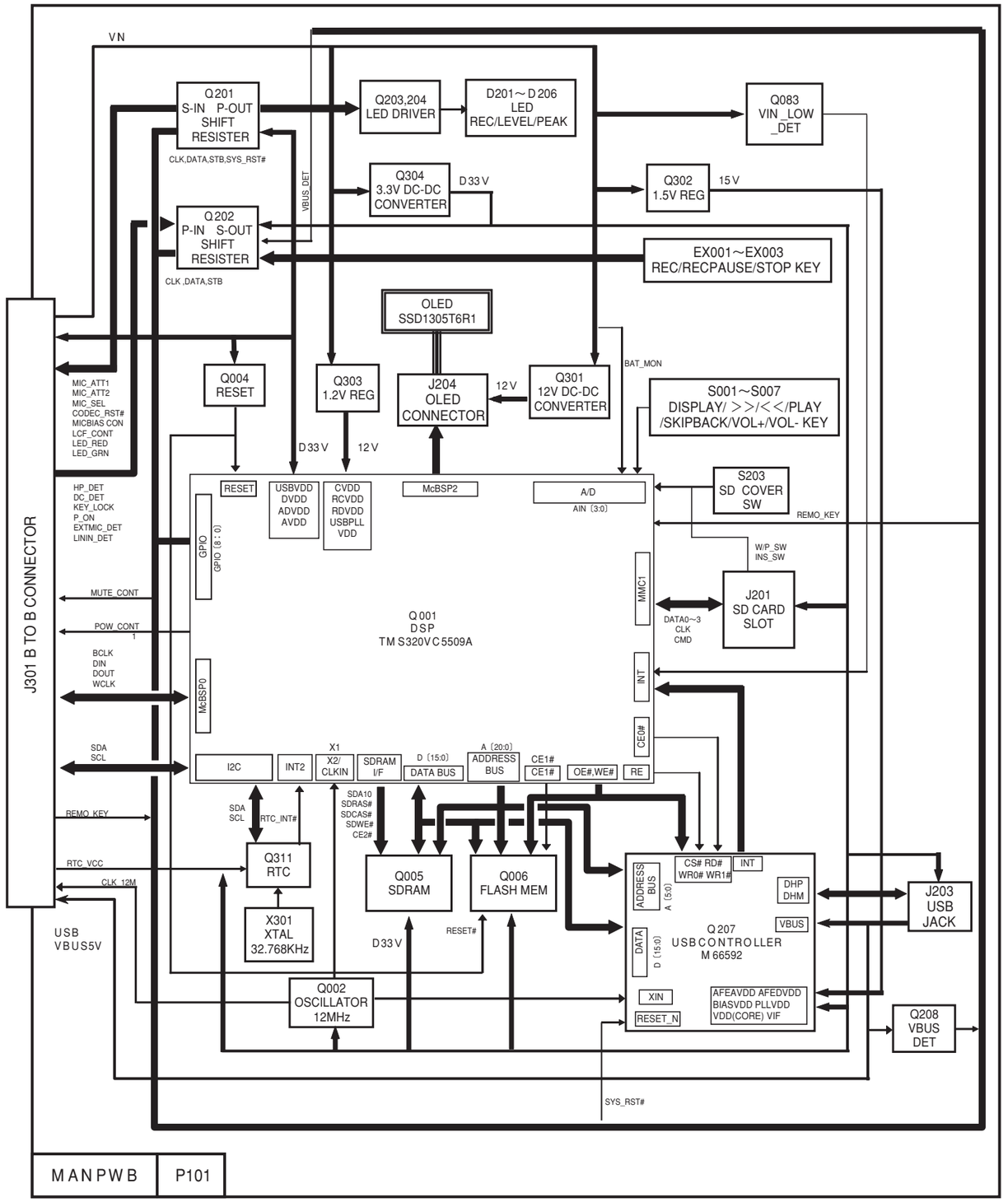
1) Insert the SD card for updating into the loading slot of the main unit.
2) Turn the **POWER slide** switch ON. At this time, “Update A-XXX?” is displayed in the display section.
   If this is not displayed, perform steps 5) ~ 7) and check the version.
3) Press the I◄◄ button, and select “YES”.
4) If the ►/II/**ENTER** button is pressed “Executing…” flashes in the display section, and update begins.
   When update has completed, the system automatically restarts.
5) To check the current main unit version, press the MENU button for 3 seconds. At this time, the menu list is displayed in the display section.
6) Press the **VOL +** and **VOL –** buttons to select “F/W Version”. At this time, the selected menu item is highlighted.
7) If the ►/II/**ENTER** button is pressed, the current version is displayed in the display section.
8) Turn the **POWER slide** switch OFF.

4. SDカードからのバージョンアップ方法

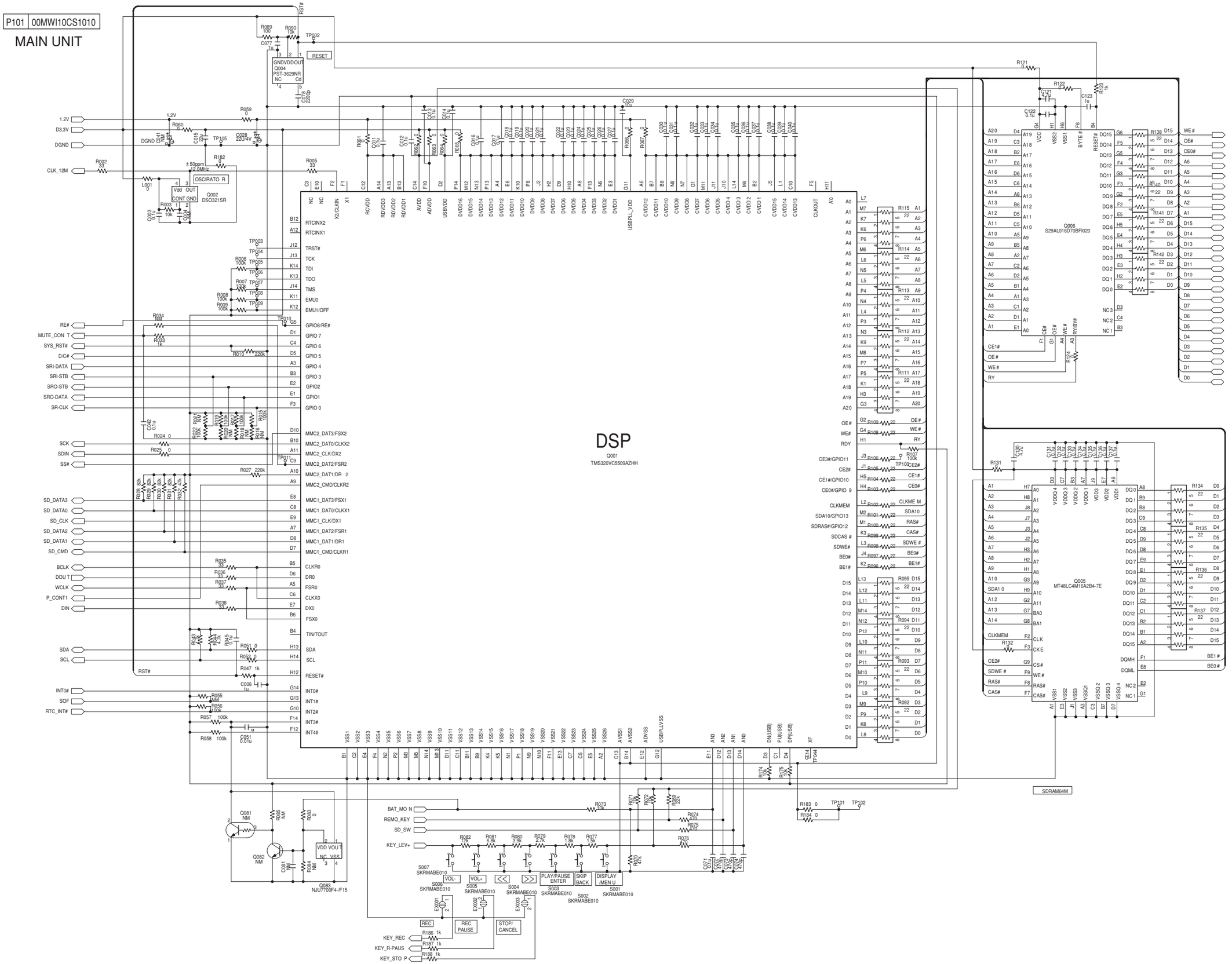
1) アップデート用のSDカードを本体の挿入口に差し込みます。
2) **POWER slide**スイッチをOnします。このとき、表示部に“Up date A-XXX?”が表示されます。
   表示されないときは、手順5)～7)を操作してバージョンを確認してください。
3) I◄◄ ボタンを押して、“YES”を選択します。
4) ►/II/**ENTER**ボタンを押すと、表示部に“Executing...”が点滅表示され、アップデートが始まります。
   アップデートが完了すると、自動的に再起動します。
5) 現在の本体のバージョンを確認するには、MENUボタンを3秒間押します。このとき、表示部にメニュー一覧が表示されます。
6) **VOL +**ボタンおよび**VOL –**ボタンを押して、“F/W Version”を選択します。このとき、選択したメニューがハイライト表示されます。
7) ►/II/**ENTER**ボタンを押すと、表示部に現在のバージョンが表示されます。
8) **POWER slide**スイッチをOFFします。

5. BLOCK DIAGRAM



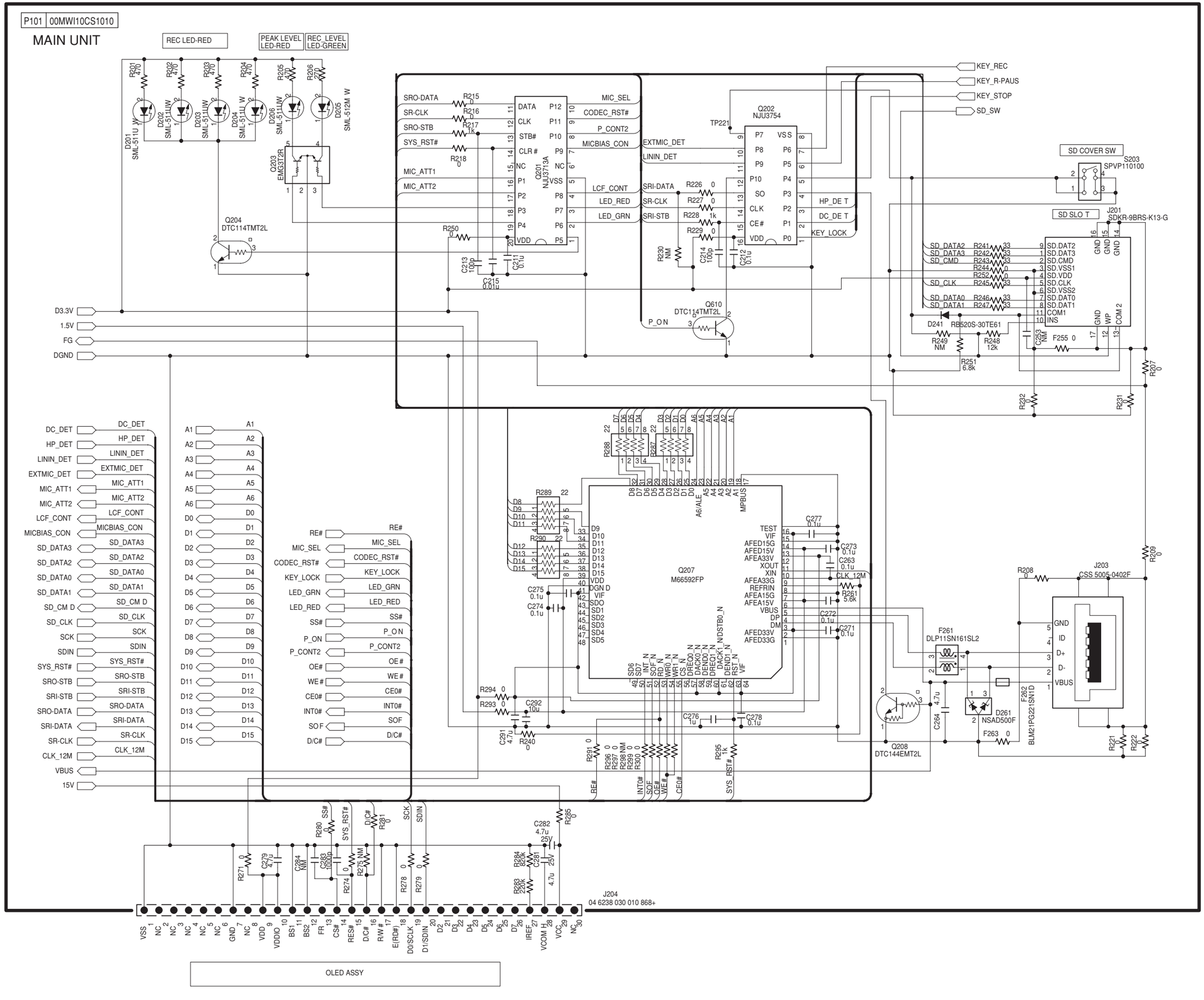


6. SCHEMATIC DIAGRAM



P101 | 00MWI10CS1010

MAIN UNIT



P101 | 00MWI10CS1010

MAIN UNIT

J301
40P9.0JMCS-G-B-TF

LININ_DET
HP_DET
MUTE_CONT
DC_DET
REMO_KEY
P_CONT1
P_CONT2
VBUS
LED_GRN
LED_RED
P_ON
KEY_LEV+
KEY_LOCK
LCF_CONT
MIC_ATT2
MIC_ATT1
MICBIAS_CON
EXTMIC_DET

C305 0.01u

VIN
R301 0
D3.3V
MIC_SEL
TP303
CLK_12M
CODEC_RST#
BCLK
WCLK
DOUT
DIN
SCL
SDA

R342 0
R343 0
FG
R351 0
R352 0
R353 0
DGND
TP304 TP305 TP346
TP301 TP345
L301 10uH
D301 RB551V-30TE-17
TP302 TP341
BAT_MON
R307 0
15V
Q301 LT1615ES5
SW 1 VIN 5
GND 2
FB #SHDN 3 4
R302 100k
C302 10p
C301 10u
R306 1M
C304 0.1u
C303 10u/25V
R304 NM
R305 110K
TP311
TP312 TP342
VIN VOU T
VSS 2
CE 3 NC
Q302 XC6210B152M
R313 0
1.5V
R311 10k
R312 NM
C312 4.7u
C311 1u
D3.3V

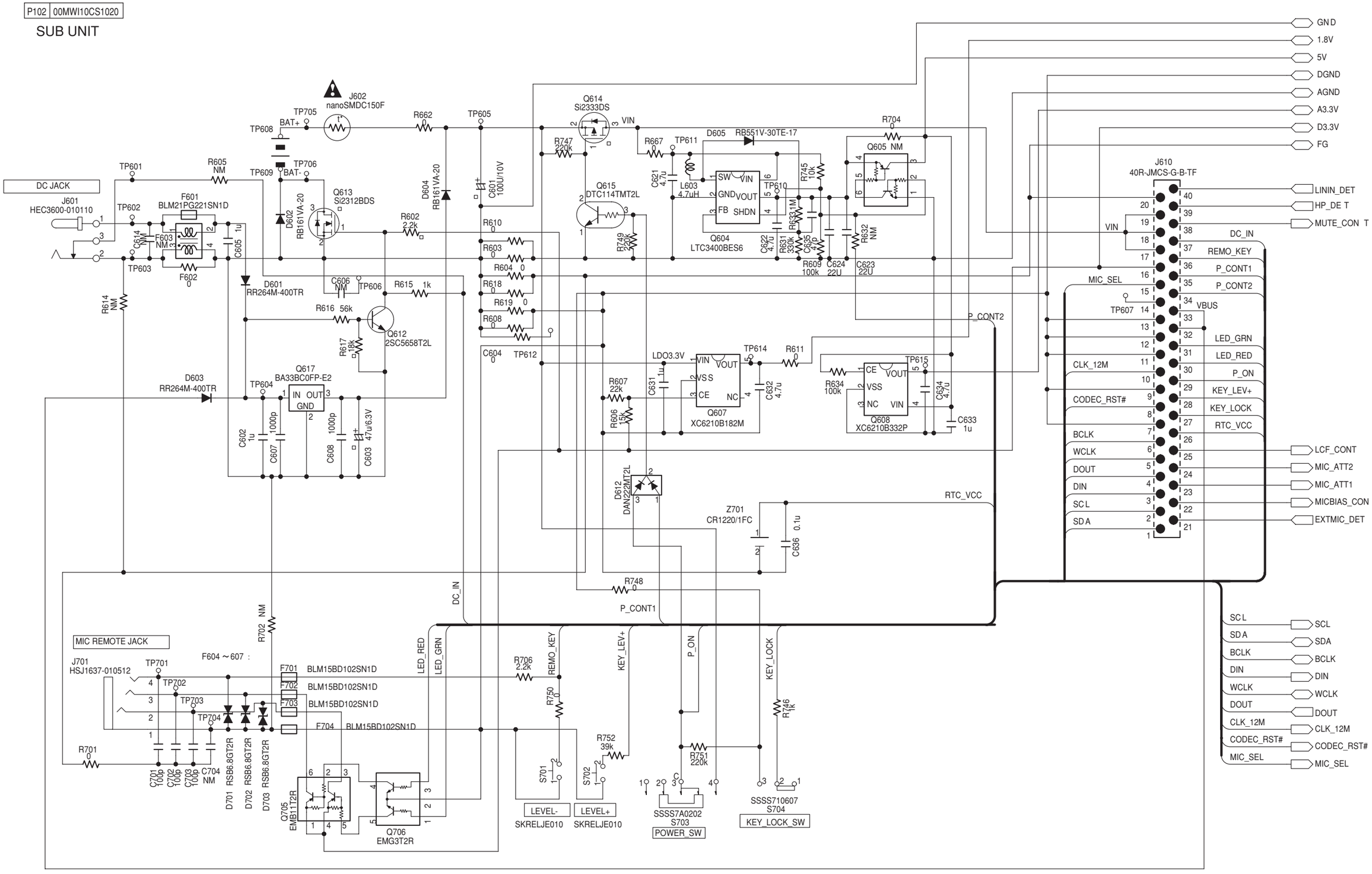
R341 NM
D331 RB551V-30TE-17
L331 4.7uH
C331 4.7u
SW VIN 1 6
GND VOUT 2 5
FB SHDN 3 4
Q304 LTC3400BES6
R331 100k
TP333 TP344
L302 0
R333 560k
R332 NM
C332 4.7u
R334 330k
C313 47p
R321 10k
TP322 TP343
VIN VOUT
VSS 2
CE NC 3
Q303 XC6210B122M
R323 0
1.2V
R322 NM
C321 1u
C322 10u

CODEC_RST#
SDA
SCL
BCLK
WCLK
DIN
DOUT
CLK_12M
RTC_INT#
MIC_SEL

RTC_VCC
R315 10k
R316 1.2k
D311 DAN222MT2L
C317 0.1u
R317 NM
SDA
SCL
RTC_INT#
Q311
S-35390A-I8TG 1
RTC
VDD INT1# XOUTSDA XIN SCL VSS INT2#
8 7 6 5
1 2 3 4
C315 NM
C316 5p
X301
SSP-T6 32.768KHz ±10ppm

P102 | 00MWI10CS1020

SUB UNIT

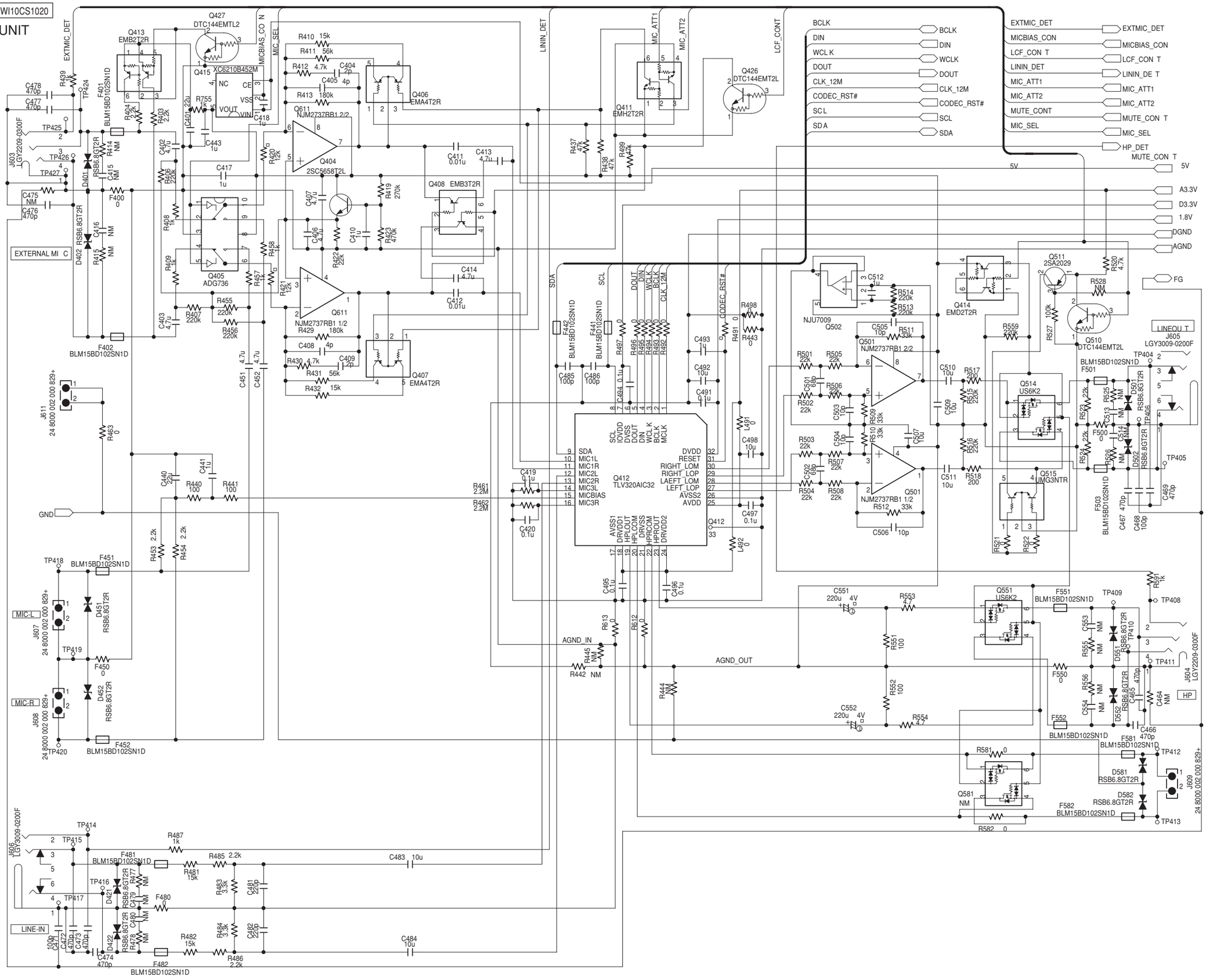


"NOTE ON SAFETY: The parts marked with ⚠ are IMPORTANT PARTS on the safety.

Please use the parts having the designated parts number without fail"

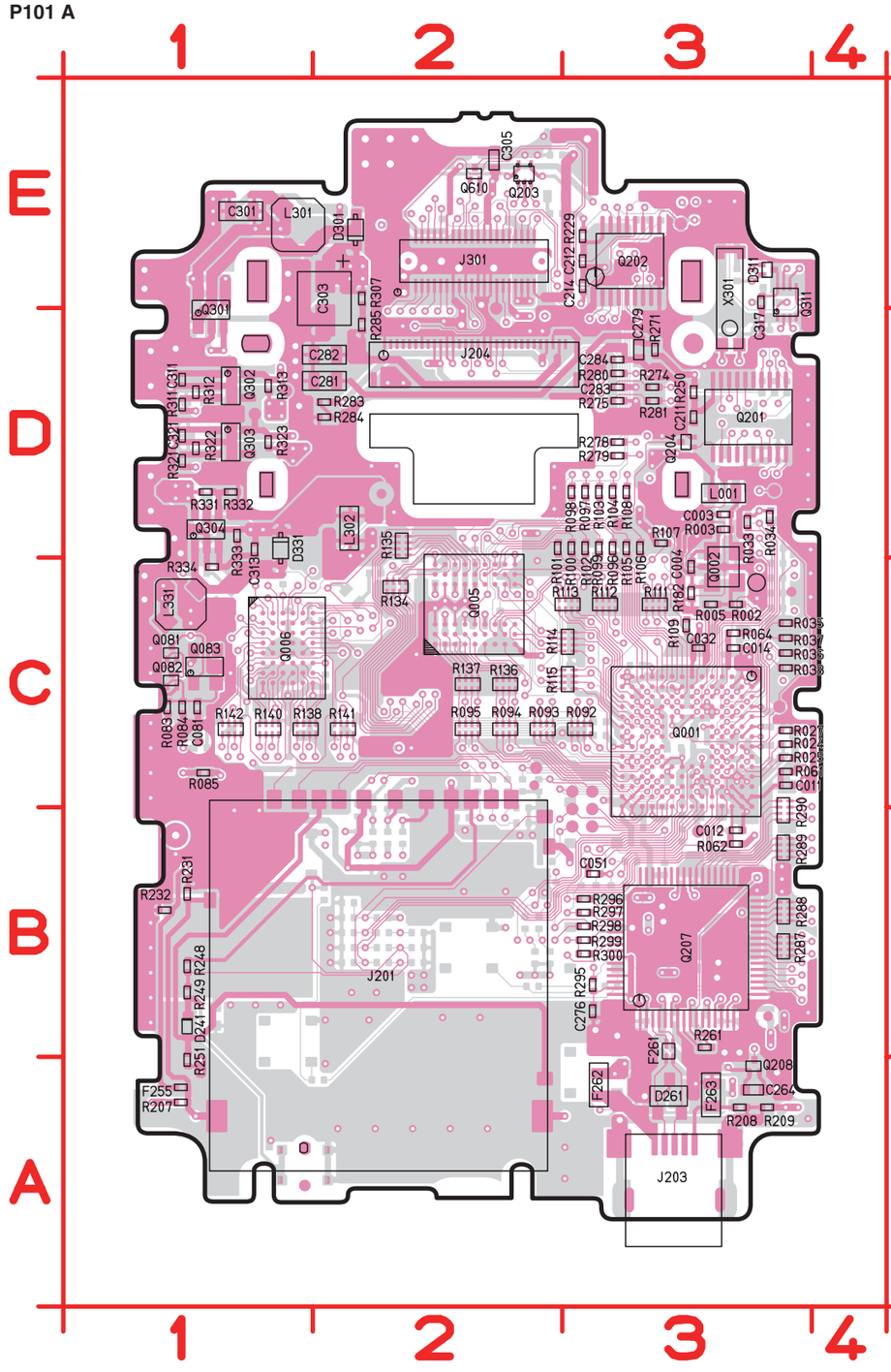
P102 | 00MWI10CS1020

SUB UNIT

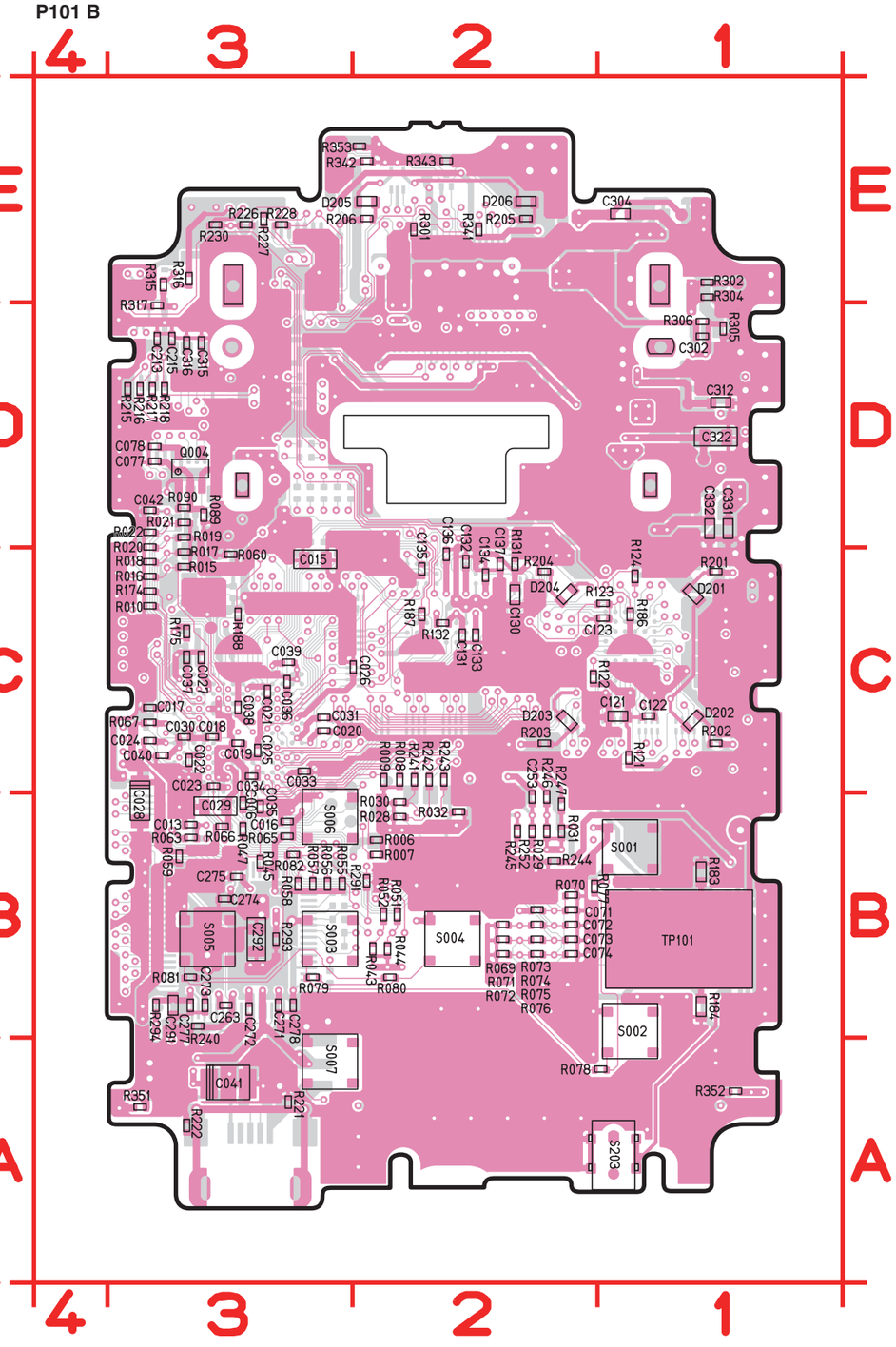


7. PARTS LOCATION

P101 A



P101 B



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C004	A2	R085	A1	C013	A2
C011	A2	R092	A1	C015	A1
C012	A2	R093	A1	C016	A1
C014	A2	R094	A1	C017	A2
C032	A2	R095	A1	C018	A2
C051	A1	R096	A1	C019	A2
C081	A1	R097	A1	C020	A1
C211	B2	R098	A1	C021	A1
C212	B1	R099	A1	C022	A2
C214	B1	R100	A1	C023	A2
C264	A2	R101	A1	C024	A2
C276	A1	R102	A1	C025	A2
C279	B1	R103	A1	C026	A1
C281	B1	R104	A1	C027	A2
C282	B1	R105	A1	C028	A2
C283	B1	R106	A1	C029	A2
C284	B1	R107	A2	C030	A2
C301	B1	R108	A1	C031	A1
C303	B1	R109	A2	C033	A1
C305	C1	R111	A1	C034	A2
C311	B1	R112	A1	C035	A2
C313	A1	R113	A1	C036	A1
C317	B2	R114	A1	C037	A2
C321	B1	R115	A1	C038	A2
D241	B1	R134	A1	C039	A1
D261	B2	R135	A1	C041	A2
D301	B1	R136	A1	C042	A2
D311	B2	R137	A1	C071	A1
D331	A1	R138	A1	C072	A1
F255	A1	R140	A1	C073	A1
F261	A2	R141	A1	C074	A1
F262	A1	R142	A1	C077	A2
F263	A2	R182	A2	C078	A2
J201	A1	R207	B1	C121	A1
J203	A2	R208	B2	C122	A1
J204	B1	R209	B2	C123	A1
J301	B1	R229	B1	C130	A1
L001	A2	R231	A1	C131	A1
L301	B1	R232	A1	C132	A1
L302	A1	R248	A1	C133	A1
L331	A1	R249	A1	C134	A1
Q001	A2	R250	B2	C135	A1
Q002	A2	R251	B1	C136	A1
Q005	A1	R261	A2	C137	A1
Q006	A1	R271	B1	C213	B2
Q081	A1	R274	B1	C215	B2
Q082	A1	R275	B1	C253	A1
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Q201	B2	R279	A1	C271	A1
Q202	B1	R280	B1	C272	A2
Q203	C1	R281	B1	C273	A2
Q204	A2	R283	B1	C274	A2
Q207	A2	R284	B1	C275	A2
Q208	A2	R285	B1	C277	A2
Q301	B1	R287	B2	C278	A1
Q302	B1	R288	A2	C291	B2
Q303	A1	R289	A2	C292	B2
Q304	A1	R290	A2	C302	B1
Q311	B2	R295	A1	C304	B1
Q610	C1	R296	A1	C312	B1
R002	A2	R297	A1	C315	B2
R003	A2	R298	A1	C316	B2
R005	A2	R299	A1	C322	B1
R024	A2	R300	A1	C331	A1
R025	A2	R307	B1	C332	A1
R027	A2	R311	B1	D201	A1
R033	A2	R312	B1	D202	A1
R034	A2	R313	B1	D203	A1
R035	A2	R321	A1	D204	A1
R036	A2	R322	A1	D205	B1
R037	A2	R323	A1	D206	B1
R038	A2	R331	A1	EX00	A1
R061	A2	R332	A1	EX00	A1
R062	A2	R333	A1	EX00	A2
R064	A2	R334	A1	Q004	A2
R083	A1	X301	B2	R006	A1

R043	A1	R241	A1	R315	B2
R044	A1	R242	A1	R316	B2
R045	A2	R243	A1	R317	B2
R047	A2	R244	A1	R341	B1
R051	A1	R245	A1	R342	C1
R052	A1	R246	A1	R343	C1
R063	A1	R247	A1	R351	C2
R065	A1	R252	A1	R352	C1
R066	A2	R291	A1	R353	C1
R067	A2	R293	A1	S001	A1
R069	A2	R294	A2	S002	A1
R070	A1	R301	B1	S003	A1
R071	A1	R302	B1	S004	A1
R072	A1	R304	B1	S005	A2
R073	A1	R305	B1	S006	A1
R074	A1	R306	B1	S007	A1
R075	A1	R315	B2	S203	A1
R076	A1	R316	B2		
R077	A1	R317	B2		
R078	A1	R341	B1		
R079	A1	R342	C1		
R080	A1	R343	C1		
R081	A1	R351	C2		
R082	A1	R352	C1		
R089	A2	R353	C1		
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R121	A1	S002	A1		
R122	A1	S003	A1		
R123	A1	S004	A1		
R124	A1	S005	A2		
R131	A1	S006	A1		
R132	A1	S007	A1		
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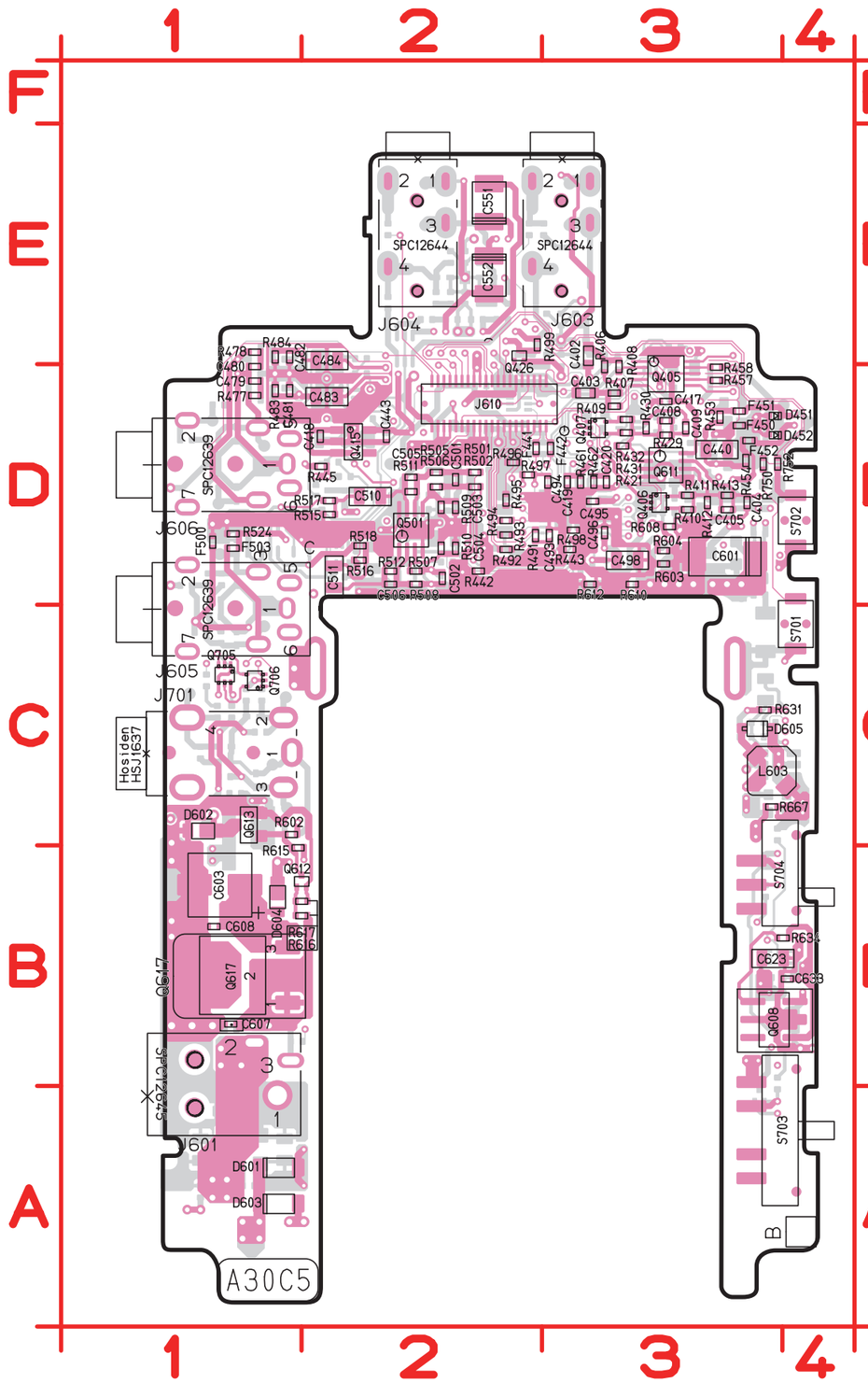
R206	B1				
R215	B2				
R216	B2				
R217	B2				
R218	B2				
R221	B1				
R222	B2				
R226	B2				
R227	B1				
R228	B1				
R230	B2				
R240	A2				

鉛フリー半田
半田付けには、鉛フリー半田 (Sn-Ag-Cu) を使用してください。

Lead-free Solder
When soldering, use the Lead-free Solder (Sn-Ag-Cu).

P102 A



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C607 A1
C608 A1
C623 A2
C633 A2
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D452 B2
D601 B1
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D605 A2
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F442 B1
F450 B2
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F452 B2
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J605 A0
J606 B0
J610 B1
J701 A0
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Q407 B1
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Q426 B1
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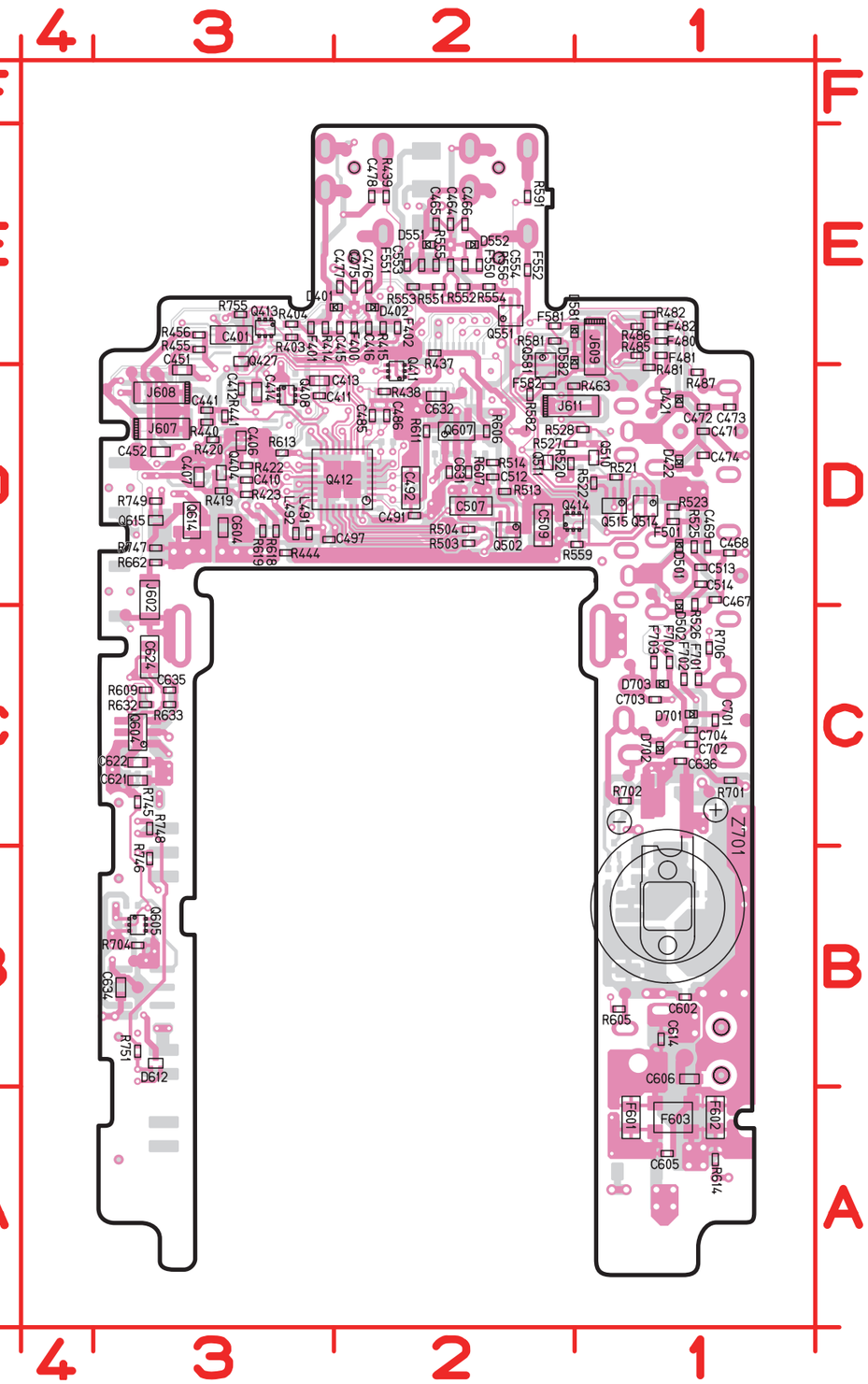
S704 A2

P102 B



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C704 A1
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D422 B1
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D502 A1
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D552 C1
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D582 B1
D612 A2
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D702 A1
D703 A1
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F402 B1
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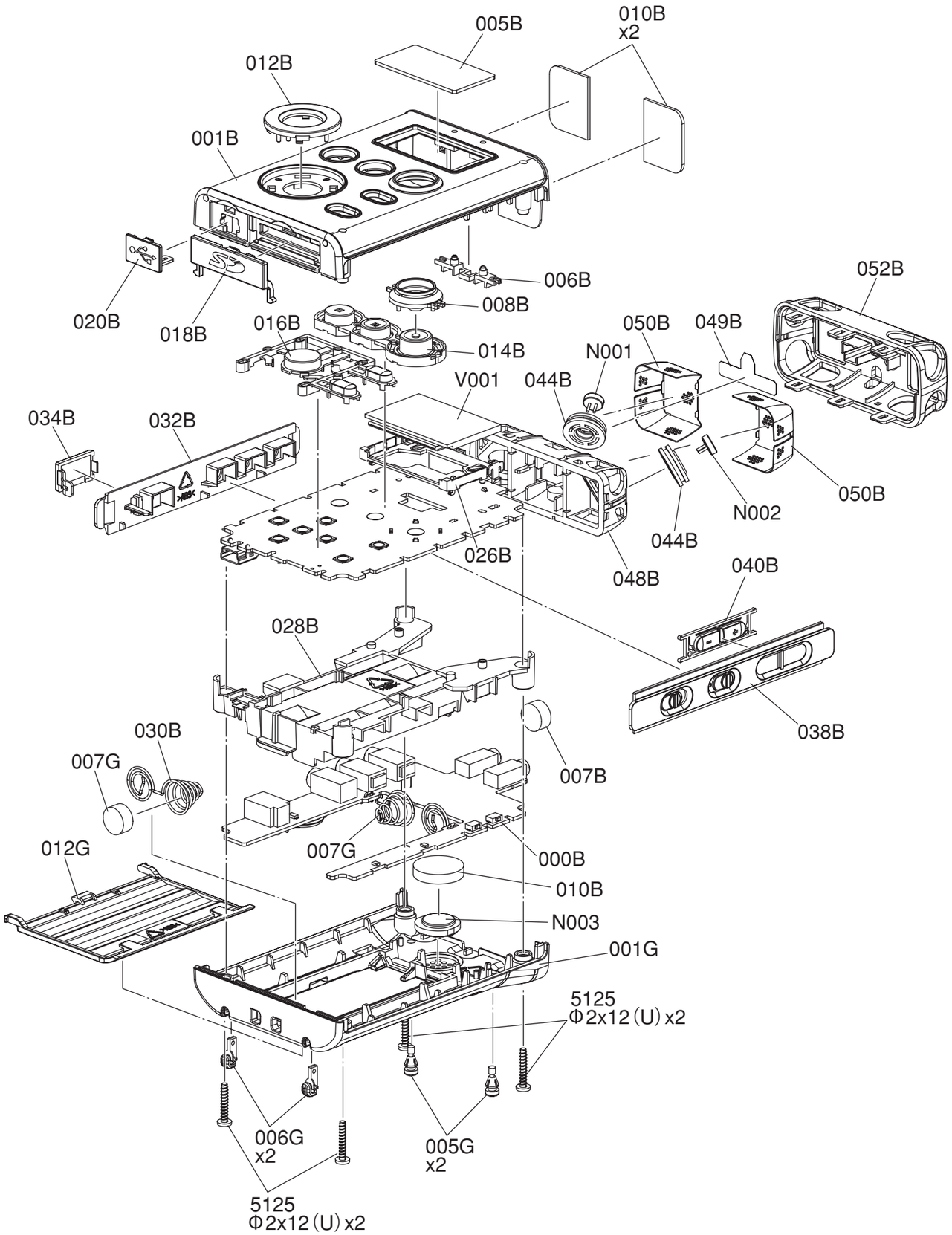
R745 A2
R746 A2
R747 A2
R748 A2
R749 B2
R751 B2
R755 B2
Z701 A1

鉛フリー半田
半田付けには、鉛フリー半田 (Sn-Ag-Cu) を使用してください。

Lead-free Solder
When soldering, use the Lead-free Solder (Sn-Ag-Cu).

8. EXPLODED VIEW AND PARTS LIST

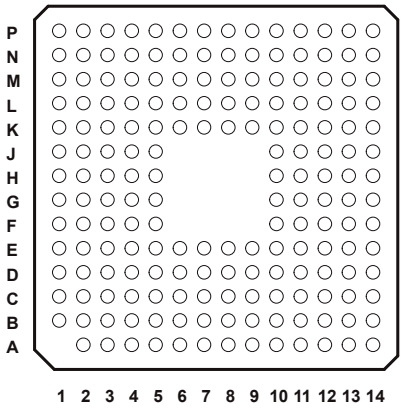


POS. NO.	QTY	PART NO. (FOR EUR)	PART NO. (D&M)	PART NAME	DESCRIPTION
001B	1	00M10CS064510	00M10CS064510	CASE ASSY	TOP CASE ASSY
005B	1	00M10CS158010	00M10CS158010	WINDOW	WINDOW
006B	1	00M10CS355020	00M10CS355020	LENS	LED LENS
008B	1	00M10CS355010	00M10CS355010	LENS	REC LENS
010B	2	00M10CS056010	00M10CS056010	BUFFER	MIC BUFFER
012B	1	00M10CS270010	00M10CS270010	BUTTON	TRACK JUMP BUTTON
014B	1	00M10CS270020	00M10CS270020	BUTTON	REC BUTTON
016B	1	00M10CS270030	00M10CS270030	BUTTON	ENTER BUTTON
018B	1	00M10CS257010	00M10CS257010	LID	SD LID
020B	1	00M10CS257510	00M10CS257510	LID ASSY	USB LID ASSY
026B	1	00M10CS271010	00M10CS271010	HOLDER	OLED HOLDER
028B	1	00M10CS271020	00M10CS271020	HOLDER	BATTERY HOLDER
030B	1	00M10CS123010	00M10CS123010	CONTACTOR	RELAY CONTACTOR
032B	1	00M10CS249020	00M10CS249020	PANEL	L SIDE PANEL
034B	1	00M10CS257500	00M10CS257500	LID ASSY	DC JACK LID ASSY
038B	1	00M10CS249500	00M10CS249500	PANEL ASSY	R SIDE PANEL ASSY
040B	1	00M10CS270040	00M10CS270040	BUTTON	REC LEVEL BUTTON
044B	2	00M10CS271040	00M10CS271040	HOLDER	MIC RUBBER HOLDER
048B	1	00M10CS271030	00M10CS271030	HOLDER	MIC HOLDER
049B	1	00M10CS107010	00M10CS107010	SHEET	MIC EARTH SHEET
050B	2	00M10CS202010	00M10CS202010	NET	MIC NET
052B	1	00M10CS064020	00M10CS064020	CASE	MIC CASE
053B	2	00M10CS107020	00M10CS107020	SHEET	WIRE SHEET
001G	1	00M10CS064530	00M10CS064530	CASE ASSY	BOTTOM CASE ASSY
005G	2	00M10CS057010	00M10CS057010	LEG	RUBBER A LEG
006G	2	00M10CS057020	00M10CS057020	LEG	RUBBER B LEG
007G	2	00M10CS056030	00M10CS056030	BUFFER	CONTACTOR BUFFER
008G	2	00M10CS107020	00M10CS107020	SHEET	WIRE SHEET
010G	1	00M10CS056020	00M10CS056020	BUFFER	SPEAKER BUFFER
012G	1	00M10CS257040	00M10CS257040	LID	BATTERY LID
014G	4	00M51250212U0	00M51250212U0	SCREW	SCREW
015G	1	00M10CS056100	00M10CS056100	BUFFER	BUFFER
016G	1	00M10CS123040	00M10CS123040	GASKET	GASKET CONTACTOR
001T	1	00M10CS851250	00M10CS851250	DFU	DFU FOR (U ,N)
001T	1	00M10CS851350	00M10CS851350	DFU	DFU FOR (K)
002T	1	00M10CS851010	00M10CS851010	DFU	DFU CD-ROM (U ,N)
001Z	1	00MAA90005160	00MAA90005160	AC ADAPTER	AC ADAPTER (5V 1.5A)
⚠ 002Z	1	00MZC01002010	00MZC01002010	MAINS CORD	! MAINS CORD (U)
⚠ 002Z	1	00MZC01003010	00MZC01003010	MAINS CORD	! MAINS CORD (EU)
⚠ 002Z	1	00MZC01008010	00MZC01008010	MAINS CORD	! MAINS CORD (K)
⚠ 003Z	1	00MZC01804110	00MZC01804110	MAINS CORD	! MAINS CORD (UK)
007Z	1	00M10CS156010	00M10CS156010	STRAP	STRAP
010Z	1	00M10CS831010	00M10CS831010	TRIPOD ADAPTER	TRIPOD ADAPTER
⚠ P100			99MZZ10CS1000	MAIN PCB	!MAIN PCB KIT (PMD620)
V001	1	00MHQ49901980	00MHQ49901980	DISPLAY	OLED ASSY (PMD620)
N001	1	00MMS50090110	00MMS50090110	MICROPHONE	MIC KUB4223
N002	1	00MMS50090110	00MMS50090110	MICROPHONE	MIC KUB4223
N003	1	00MQK01302010	00MQK01302010	SPEAKER	SPEAKER 388631
W001	1	00MYB00067540	00MYB00067540	CONNECTIVE CORD	WIRE FOR MIC L
W002	1	00MYB00051800	00MYB00051800	CONNECTIVE CORD	WIRE FOR MIC R
W003	1	00MYB00067520	00MYB00067520	CONNECTIVE CORD	8000-BARA WIRE AWG32 L=6.5
W004	1	00MYB00051790	00MYB00051790	CONNECTIVE CORD	WIRE FOR MIC NET

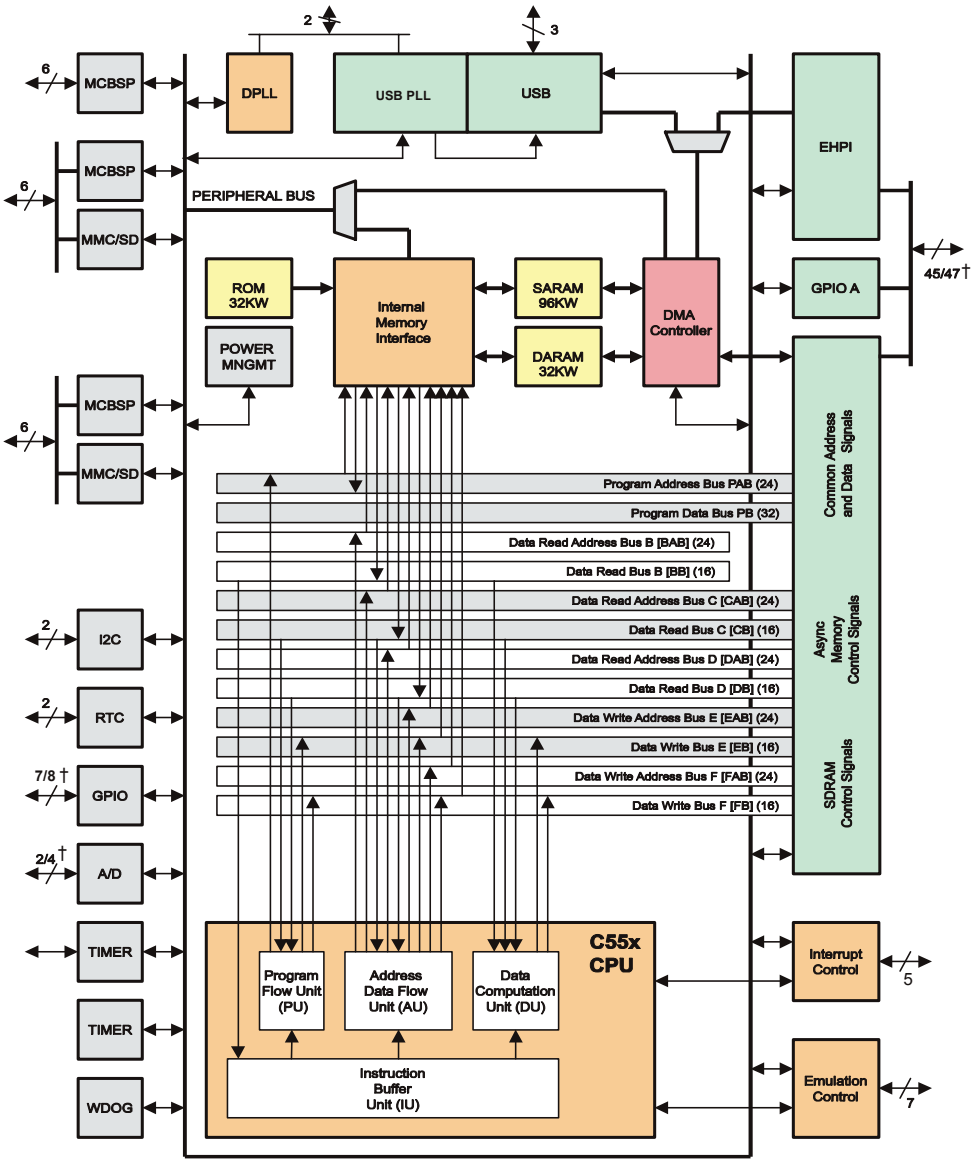
9. IC DATA

Q001 : TMS320VC5509AZHH

179-TERMINAL GHH AND ZHH BALL GRID ARRAY (BOTTOM VIEW)



BLOCK DIAGRAM



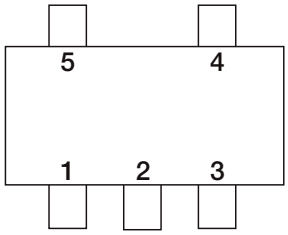
† Number of pins determined by package type.

Q001 : TMS320VC5509AZHH

PIN ASSIGNMENTS FOR THE GHH AND ZHH PACKAGES

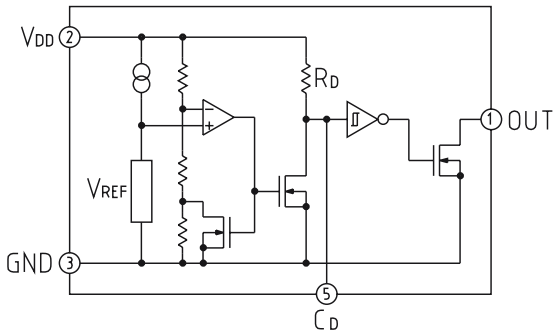
BALL #	SIGNAL NAME	BALL #	SIGNAL NAME	BALL #	SIGNAL NAME	BALL #	SIGNAL NAME
A2	V_{SS}	D5	GPIO5	H2	DV_{DD}	L13	D15
A3	GPIO4	D6	DR0	H3	A19	L14	CV_{DD}
A4	DV_{DD}	D7	S10	H4	C4	M1	C10
A5	FSR0	D8	S11	H5	C5	M2	C13
A6	CV_{DD}	D9	DV_{DD}	H10	DV_{DD}	M3	V_{SS}
A7	S12	D10	S25	H11	A'[0]	M4	CV_{DD}
A8	DV_{DD}	D11	V_{SS}	H12	$\overline{RESET}$	M5	V_{SS}
A9	S20	D12	AIN2	H13	SDA	M6	A5
A10	S21	D13	AIN1	H14	SCL	M7	A1
A11	S23	D14	AIN0	J1	C6	M8	A15
A12	RTCINX1	E1	GPIO1	J2	DV_{DD}	M9	D3
A13	RDV_{DD}	E2	GPIO2	J3	C7	M10	D6
A14	RDV_{DD}	E3	DV_{DD}	J4	C8	M11	CV_{DD}
B1	V_{SS}	E4	V_{SS}	J5	CV_{DD}	M12	DV_{DD}
B2	CV_{DD}	E5	V_{SS}	J10	CV_{DD}	M13	V_{SS}
B3	GPIO3	E6	DV_{DD}	J11	CV_{DD}	M14	D12
B4	TIN/TOUT0	E7	DX0	J12	$\overline{TRST}$	N1	V_{SS}
B5	CLKR0	E8	S15	J13	TCK	N2	V_{SS}
B6	FSX0	E9	S13	J14	TMS	N3	A13
B7	CV_{DD}	E10	NC	K1	A18	N4	A10
B8	CV_{DD}	E11	AIN3	K2	C9	N5	A7
B9	V_{SS}	E12	ADV_{SS}	K3	C11	N6	DV_{DD}
B10	S24	E13	V_{SS}	K4	V_{SS}	N7	CV_{DD}
B11	V_{SS}	E14	XF	K5	V_{SS}	N8	CV_{DD}
B12	RTCINX2	F1	X1	K6	A3	N9	V_{SS}
B13	RDV_{DD}	F2	X2/CLKIN	K7	A2	N10	V_{SS}
B14	AV_{SS}	F3	GPIO0	K8	D1	N11	D8
C1	PU	F4	V_{SS}	K9	A14	N12	D11
C2	V_{SS}	F5	CLKOUT	K10	DV_{DD}	N13	DV_{DD}
C3	NC	F10	ADV_{DD}	K11	EMU0	N14	V_{SS}
C4	GPIO6	F11	V_{SS}	K12	EMU1/$\overline{OFF}$	P1	V_{SS}
C5	V_{SS}	F12	$\overline{INT4}$	K13	TDO	P2	V_{SS}
C6	CLKX0	F13	DV_{DD}	K14	TDI	P3	A12
C7	V_{SS}	F14	$\overline{INT3}$	L1	CV_{DD}	P4	A9
C8	S14	G1	CV_{DD}	L2	C14	P5	A17
C9	S22	G2	C1	L3	C12	P6	A4
C10	CV_{DD}	G3	A20	L4	A11	P7	A16
C11	V_{SS}	G4	C2	L5	A8	P8	DV_{DD}
C12	RCV_{DD}	G5	C0	L6	A6	P9	D2
C13	AV_{SS}	G10	$\overline{INT2}$	L7	A0	P10	D5
C14	AV_{DD}	G11	$USBPLLV_{DD}$	L8	D0	P11	D7
D1	GPIO7	G12	$USBPLLV_{SS}$	L9	D4	P12	D10
D2	$USBV_{DD}$	G13	$\overline{INT1}$	L10	D9	P13	DV_{DD}
D3	DN	G14	$\overline{INT0}$	L11	D13	P14	DV_{DD}
D4	DP	H1	C3	L12	D14		

Q004 : PST3629NR



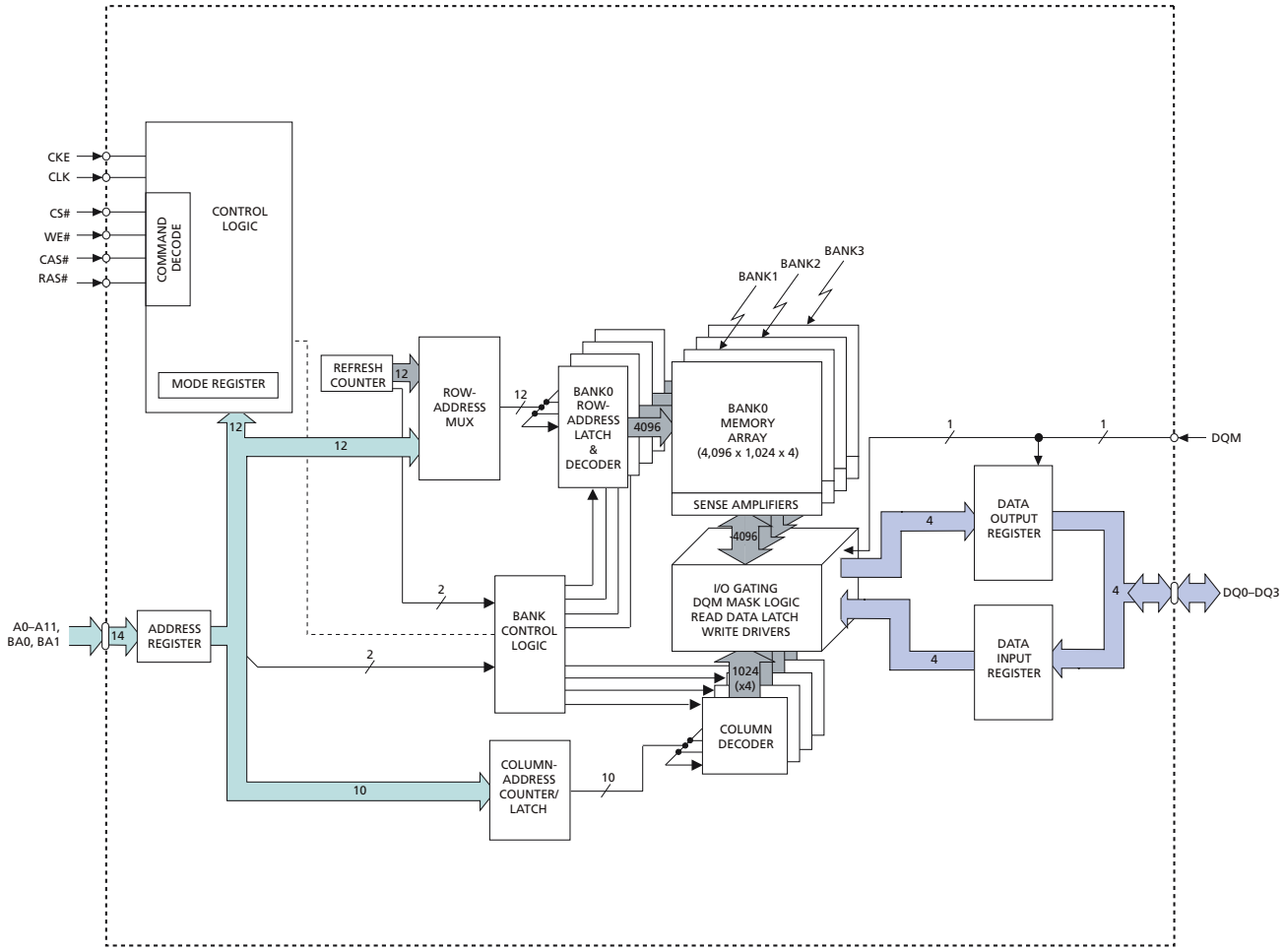
SOT-25A
(TOP VIEW)

1	OUT
2	V_{DD}
3	GND
4	NC
5	Cd



Q005 : MT48LC4M16A2B4-7E

BLOCK DIAGRAM



X16 VFBGA BALL ASSIGNMENT (TOP VIEW, BALL DOWN)

	1	2	3	4	5	6	7	8	9
A	VSS	DQ15	VSSQ				VDDQ	DQ0	VDD
B	DQ14	DQ13	VDDQ				VSSQ	DQ2	DQ1
C	DQ12	DQ11	VSSQ				VDDQ	DQ4	DQ3
D	DQ10	DQ9	VDDQ				VSSQ	DQ6	DQ5
E	DQ8	NC	VSS				VDD	DQML	DQ7
F	DQMH	CLK	CKE				CAS#	RAS#	WE#
G	NC/A12	A11	A9				BA0	BA1	CS#
H	A8	A7	A6				A0	A1	A10
J	VSS	A5	A4				A3	A2	VDD

Notes: The balls at A4, A5, and A6 are absent from the physical package. They are included to illustrate that rows 4, 5, and 6 exist but contain no solder balls.

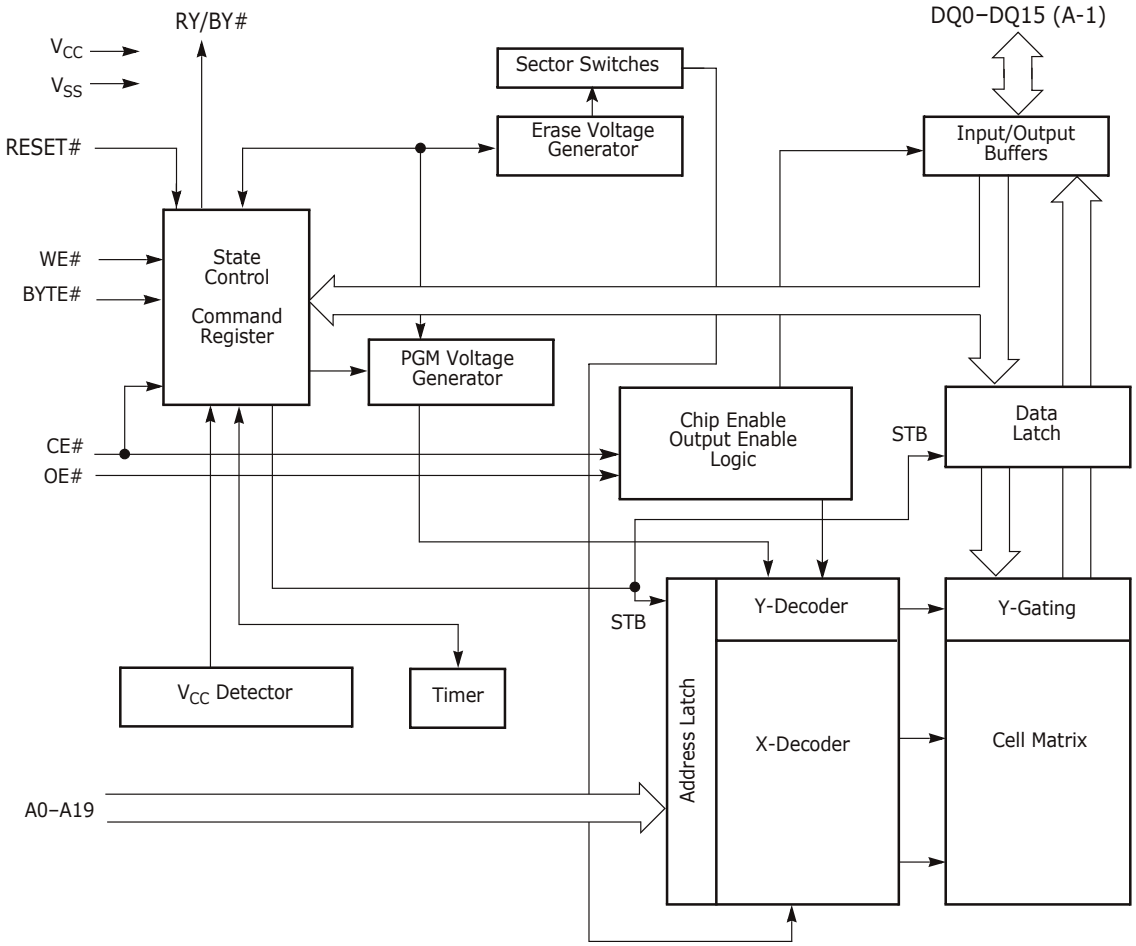
Q005 : MT48LC4M16A2B4-7E

PIN/BALL DESCRIPTIONS

VFBGA Ball Numbers	Symbol	Type	Description
F2	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
F3	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE power-down and SELF REFRESH operation (all banks idle), ACTIVE power-down (row active in any bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
G9	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH, but READ/WRITE bursts already in progress will continue and DQM will retain its DQ mask capability while CS# remains HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
F9, F7, F8	WE#, CAS#, RAS#	Input	Command inputs: WE#, CAS#, and RAS# (along with CS#) define the command being entered.
–	x4, x8: DQM	Input	Input/Output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. On the x4 and x8, DQML (Pin 15) is a NC and DQMH is DQM. On the x16, DQML corresponds to DQ0–DQ7 and DQMH corresponds to DQ8–DQ15. DQML and DQMH are considered same state when referenced as DQM.
E8, F1	x16: DQML, DQMH		
G7, G8	BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2	A0–A11	Input	Address inputs: A0–A11 are sampled during the ACTIVE command (row-address A0–A11) and READ/WRITE command (column-address A0–A9 [x4]; A0–A8 [x8]; A0–A7 [x16]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine if all banks are to be precharged (A10[HIGH]) or bank selected by BA0, BA1 (A1[LOW]). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	DQ0–DQ15	x16: I/O	Data input/output: Data bus for x16 (4, 7, 10, 13, 42, 45, 48, and 51 are NCs for x8; and 2, 4, 7, 8, 10, 13, 42, 45, 47, 48, 51, and 53 are NCs for x4).
–	DQ0–DQ7	x8: I/O	Data input/output: Data bus for x8 (2, 8, 47, 53 are NCs for x4).
–	DQ0–DQ3	x4: I/O	Data input/output: Data bus for x4.
E2	NC	–	No connect: These pins should be left unconnected.
G1	NC	–	Address input (A12) for the 256Mb and 512Mb devices
A7, B3, C7, D3	$V_{DD}Q$	Supply	DQ power: Isolated DQ power on the die for improved noise immunity.
A3, B7, C3, D7	$V_{SS}Q$	Supply	DQ ground: Isolated DQ ground on the die for improved noise immunity.
A9, E7, J9	V_{DD}	Supply	Power supply: +3.3V ±0.3V.
A1, E3, J1	V_{SS}	Supply	Ground.

Q006 : S29AL016D70BFI020

BLOCK DIAGRAM



CONNECTION DIAGRAMS

FBGA
Top View, Balls Facing Down

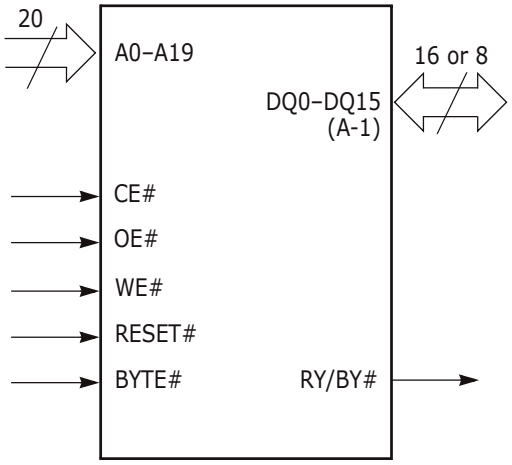
A6	B6	C6	D6	E6	F6	G6	H6
A13	A12	A14	A15	A16	BYTE#	DQ15/A-1	V_{SS}
A5	B5	C5	D5	E5	F5	G5	H5
A9	A8	A10	A11	DQ7	DQ14	DQ13	DQ6
A4	B4	C4	D4	E4	F4	G4	H4
WE#	RESET#	NC	A19	DQ5	DQ12	V_{CC}	DQ4
A3	B3	C3	D3	E3	F3	G3	H3
RY/BY#	NC	A18	NC	DQ2	DQ10	DQ11	DQ3
A2	B2	C2	D2	E2	F2	G2	H2
A7	A17	A6	A5	DQ0	DQ8	DQ9	DQ1
A1	B1	C1	D1	E1	F1	G1	H1
A3	A4	A2	A1	A0	CE#	OE#	V_{SS}

Q006 : S29AL016D70BFI020

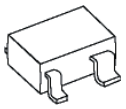
PIN CONFIGURATION

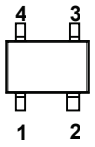
A0–A19	=	20 addresses
DQ0–DQ14	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	=	Selects 8-bit or 16-bit mode
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin
RY/BY#	=	Ready/Busy output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

LOGIC SYMBOL

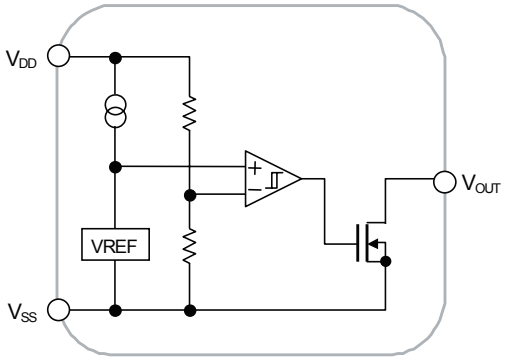


Q083 : NJU7700-F4/F15



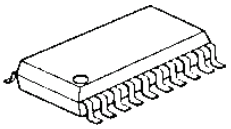


1. V_{OUT}
2. V_{DD}
3. NC
4. V_{SS}

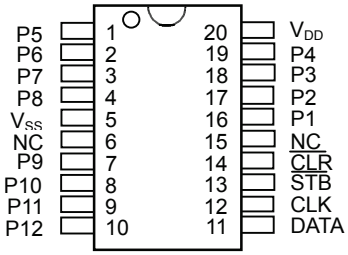


Q201 : NJU3713A

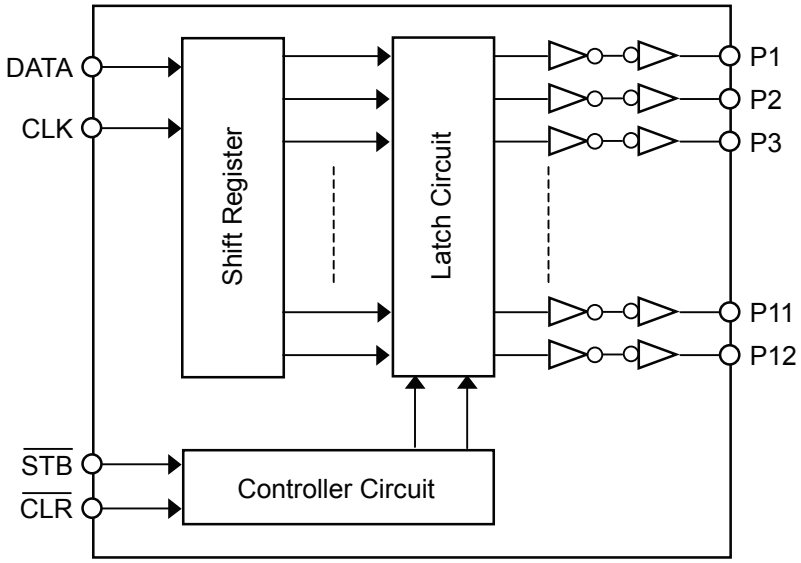
Package Outline
SSOP20



PIN CONFIGURATION



BLOCK DIAGRAM

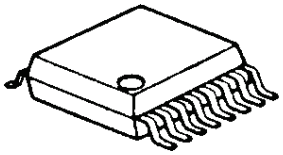


TERMINAL DESCRIPTION

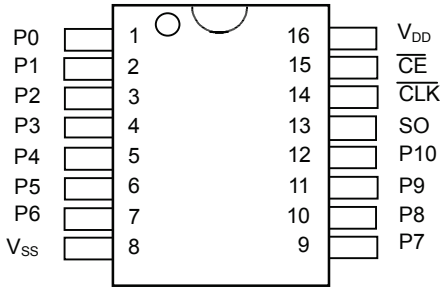
No.	SYMBOL	I/O	FUNCTION
1	P5	O	Parallel Conversion Data Output Terminals
2	P6	O	
3	P7	O	
4	P8	O	
5	V_{SS}	-	GND
6	NC	-	Non Connection
7	P9	O	Parallel Conversion Data Output Terminals
8	P10	O	
9	P11	O	
10	P12	O	
11	DATA	I	Serial Data Input Terminal
12	CLK	I	Clock Signal Input Terminal
13	$\overline{STB}$	I	Strobe Signal Input Terminal
14	$\overline{CLR}$	I	Clear Signal Input Terminal
15	NC	-	Non Connection
16	P1	O	Parallel Conversion Data Output Terminals
17	P2	O	
18	P3	O	
19	P4	O	
20	V_{DD}	-	Power Supply Terminal (2.4 to 5.5V)

Q202 : NJU3754

Package Outline
SSOP16



PIN CONFIGURATION



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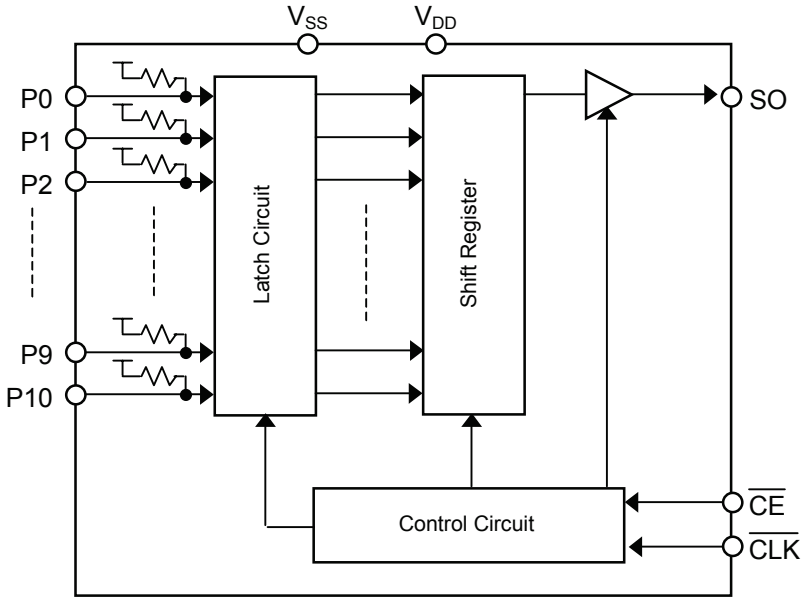
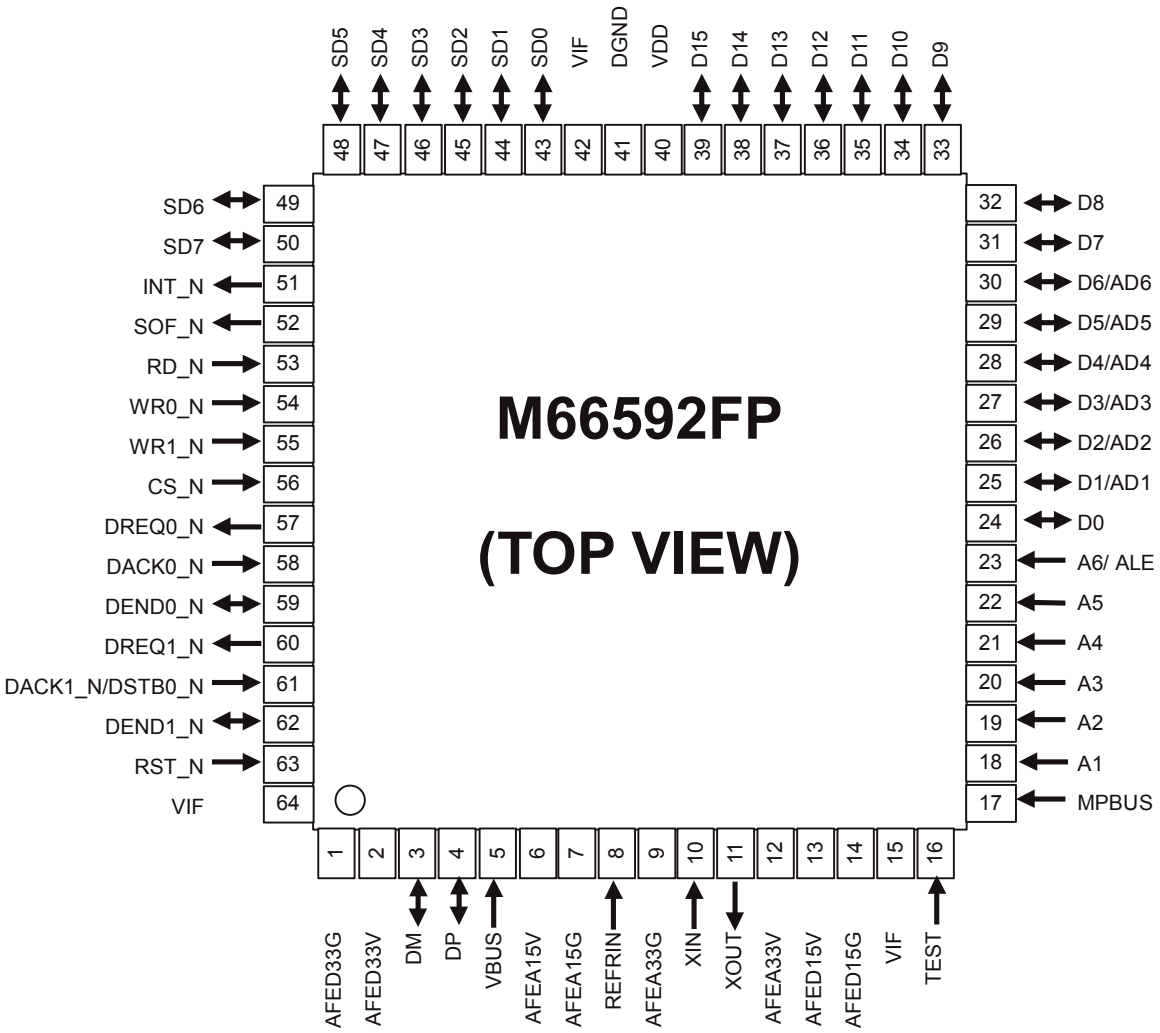


TERMINAL DESCRIPTION

No.	SYMBOL	I/O	FUNCTION
1	P0	I	Parallel Data Input Terminals (with pull-up resistors)
2	P1	I	
3	P2	I	
4	P3	I	
5	P4	I	
6	P5	I	
7	P6	I	
8	V_{SS}	-	Ground
9	P7	I	Parallel Data Input Terminals (with pull-up resistors)
10	P8	I	
11	P9	I	
12	P10	I	
13	SO	O	Serial Data Output Terminal
14	$\overline{CLK}$	I	Serial Clock Input Terminal
15	$\overline{CE}$	I	Chip Enable Input Terminal
16	V_{DD}	-	Power Supply Terminal (2.7 to 5.5V)

Q207 : M66592FP

PIN LAYOUT DIAGRAM



*The "_N" in the signal name indicates that the signal is in the "L" active state.	**Package** **M66592FP : 64pinLQFP (0.5mm pitch)**

Q207 : M66592FP

PIN DESCRIPTIONS

Category	Pin name	Name	I/O	Function	Pin count (Pin nos.)	State of pin *7)		
						RST_N="L"	RST_N goes "H"	PCUT=1
CPU bus interface	D15-0	Data Bus	I/O	This is a 16-bit data bus.	24-39	*4)	*4)	Input (Hi-z)
	AD6-1	Multiplex Address Bus	I/O	When a multiplex bus is specified, this group of pins is used on a time-shared basis for some of the data buses (D6-D1), or for 6 bits of the address bus (A6-A1).				
	A6-1	Address Bus	IN	This is a 6-bit address bus. Because the data bus consists of 16 bits, there is no A0.	18-23	Input *5)	Input *5)	Input (Hi-z) Input
	ALE	Address Latch Enable	IN	When a multiplex bus is specified, the A6 pin is used as the ALE signal.		Input	Input	
	CS_N	Chip Select	IN	Setting this to the "L" level selects this controller.	56	Input *6)	Input *6)	Input
	RD_N	Read Strobe	IN	Setting this to the "L" level reads data from the controller registers.	53	Input	Input	Input
	WR0_N	D7-0 Byte Write Strobe	IN	At the rising edge, D7-D0 are written to the registers of the controller.	54	Input *6)	Input *6)	Input
	WR1_N	D15-8 Byte Write Strobe	IN	At the rising edge, D15-D8 are written to the registers of the controller.	55	Input *6)	Input *6)	Input
	MPBUS*3	Bus Mode Selection	IN	Setting this to the "L" level selects a separate bus. Setting this to the "H" level selects a multiplex bus. This should be fixed at either the "H" or "L" level.	17	Input *3)	Input *3)	Input *3)
Split bus interface	SD7-0	Split Data Bus	I/O	If a split bus is selected, this functions as the data bus for the split bus.	43-50	Input (Hi-z)	Input (Hi-z)	Input (Hi-z)
DMA bus interface	DREQ0_N*1 DREQ1_N*1	DMA Request	OUT	This notifies the system of a D0FIFO port or D1FIFO port DMA transfer request.	57, 60	H	H	H/L *8)
	DACK0_N*1 DACK1_N*1	DMA Acknowledge	IN	Input the DMA Acknowledge signal for the D0FIFO or D1FIFO port.	58, 61	Input	Input	Input
	DSTB0_N*2	Data Strobe 0	IN	This functions as the data strobe signal for the D0FIFO port. Because it is also used for the DMA Acknowledge signal of the D1FIFO port, the DSTB0_N function cannot be used if the DACK1_N function is being used.				
	DEND0_N*1 DEND1_N*1	DMA Transfer End	I/O	<In the FIFO port access writing direction> This receives the Transfer End signal from another peripheral chip or the CPU as an input signal. <In the FIFO port access reading direction> This indicates the transfer end data as an output signal.	59, 62	Input (Hi-z)	Input (Hi-z)	Input (Hi-z)
Interrupt/ SOF output	INT_N	Interrupt	OUT	In the "L" active state, this notifies the system of various types of interrupts relating to USB communication.	51	H	H	H
	SOF_N	SOF pulse output	OUT	When an SOF is detected in the "L" active state, an SOF pulse is output.	52	H	H	H
Clock	XIN	Oscillation input	IN	A crystal oscillator should be connected between XIN and XOUT. When using external clock input, the external clock signal should be connected to XIN, and XOUT should be open.	10			
	XOUT	Oscillation output	OUT		11			

Category	Pin name	Name	I/O	Function	Pin count (Pin nos.)	State of pin *7)		
						RST_N=”L”	RST_N goes “H”	PCUT=1
System control	RST_N	Reset signal	IN	At “L” level, the controller is initialized.	63	Input (L)	Input (H)	Input (H)
	TEST	Test signal	IN	This should be fixed at “L” or open.	16			
USB bus interface	DP	USB D+ data	I/O	This should be connected to the D+ pin of the USB bus.	4	Input (Hi-z)	Input (Hi-z)	Input (Hi-z)
	DM	USB D- data	I/O	This should be connected to the D- pin of the USB bus.	3	Input (Hi-z)	Input (Hi-z)	Input (Hi-z)
VBUS monitor input	VBUS	VBUS input	IN	This should be connected directly to the Vbus of the USB bus. The connected or disconnected state of the Vbus can be detected. If This pin is not connectted with Vbus of a USB bus, connect it with 5V.	5	Input (Hi-z)	Input (Hi-z)	Input (Hi-z)
Reference resistance	REFRIN	Reference input	IN	This should be connected to AFEA33G through a 5.6 kΩ±1% resistance.	8			
Power supply / GND	AFEA33V	Transceiver unit analog power supply	-	This should be connected to 3.3 V.	12			
	AFEA33G	Transceiver unit analog GND	-		9			
	AFED33V	Transceiver unit digital power supply	-	This should be connected to 3.3 V.	2			
	AFED33G	Transceiver unit digital GND	-		1			
	AFEA15V	Transceiver unit analog 1.5 V power supply	-	This should be connected to 1.5 V.	6			
	AFEA15G	Transceiver unit analog GND	-		7			
	AFED15V	Transceiver unit digital 1.5 V power supply	-	This should be connected to 1.5 V.	13			
	AFED15G	Transceiver unit digital GND	-		14			
	VDD	Core power supply	-	This should be connected to 1.5 V.	40			
	VIF	IO power supply	-	This should be connected to 3.3 V or 1.8 V.	15, 42, 64			
	DGND	Digital GND	-		41			

***1)** The “L” active and “H” active states of these pins can be specified using the control program for the user system. ”_N” indicates that the “L” active state is the default state.

***2)** DSTB0_N and DACK1_N are assigned to the same pin, so the functions of one or the other are valid.

***3)** The input level of the MPBUS pin needs to be established just before the end of H/W reset. Also, this should not be switched during operation.

***4)** When CS_N and RD_N are “L”, these pins output “H” or “L”.

***5)** If MPBUS is “H”, these pins can be made to open.

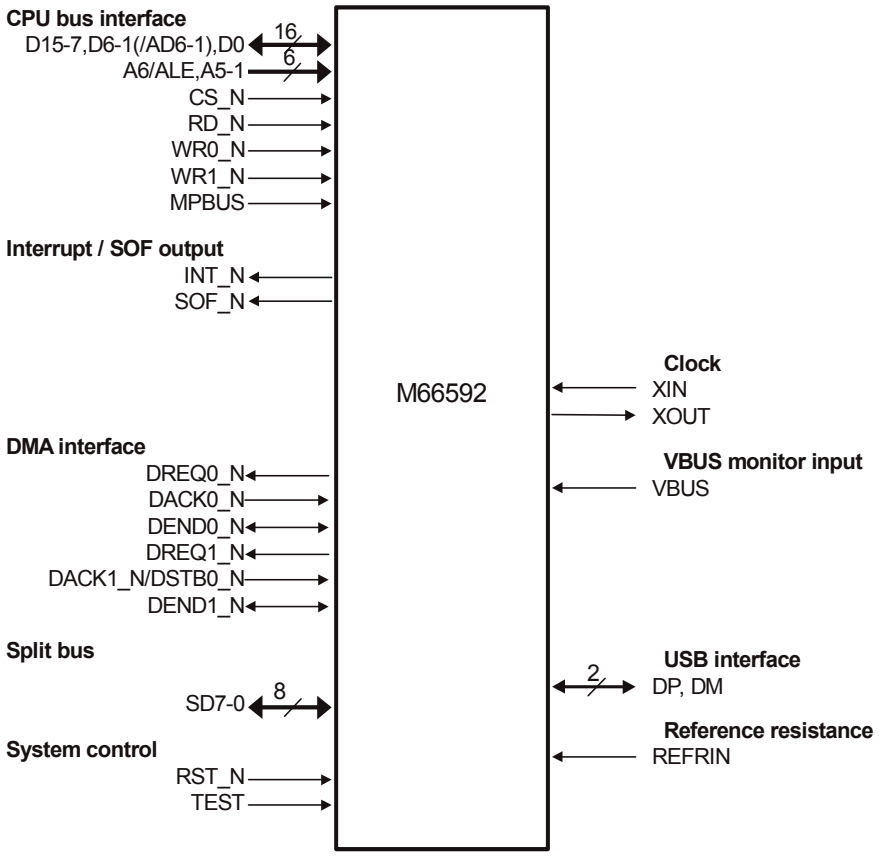
***6)** CS_N, WR0_N, and WR1_N should be kept as (a) or (b) during RST_N=”L” (from RST_N goes "L" to right after RST_N goes "H").
(a) CS_N=”H”
(b) WR0_N=”H” and WR1_N=”H”

***7)** Discription of “State of pin”
(a) Input : Pins are Hi-z state. Please do not make it “open” on a board.
(b) Input(Hi-z) : Pins are Hi-z state. Pins can be “open” on a board.
(c) H, L, H/L : Output states is shown.

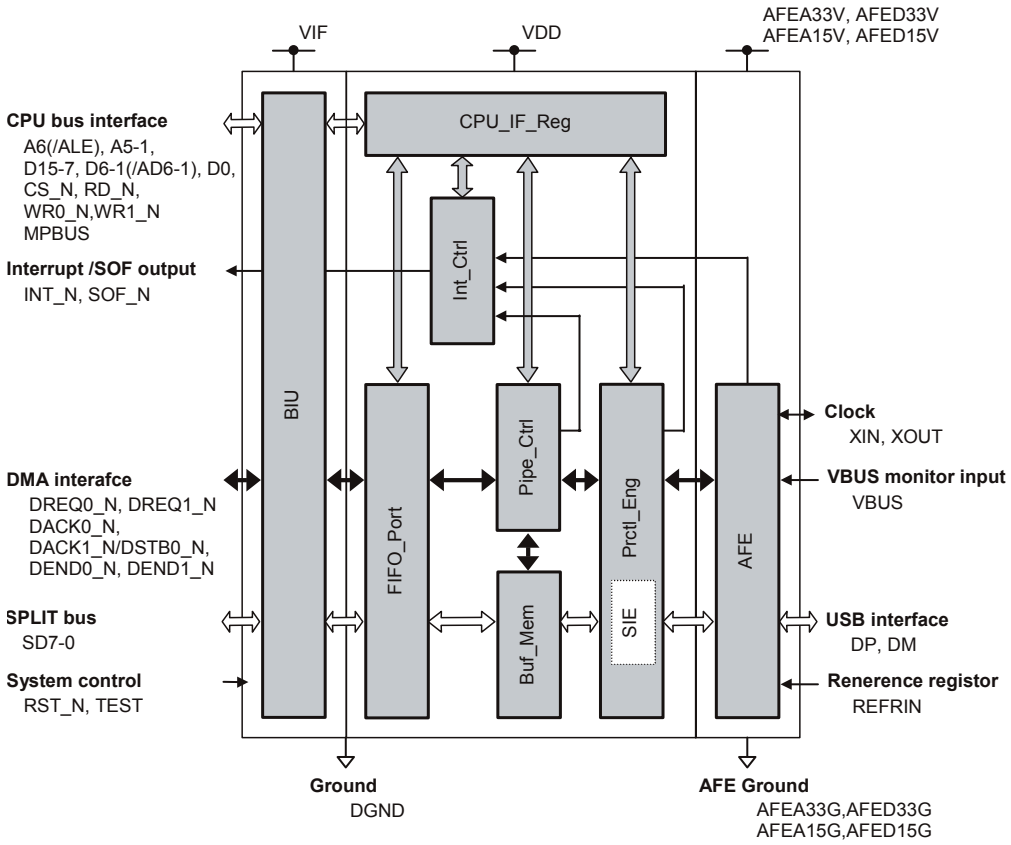
***8)** These pins are in an inactive state.

Q207 : M66592FP

PIN FUNCTION CONFIGURATION DIAGRAM

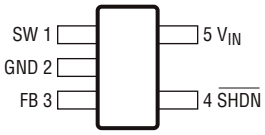


BLOCK DIAGRAM



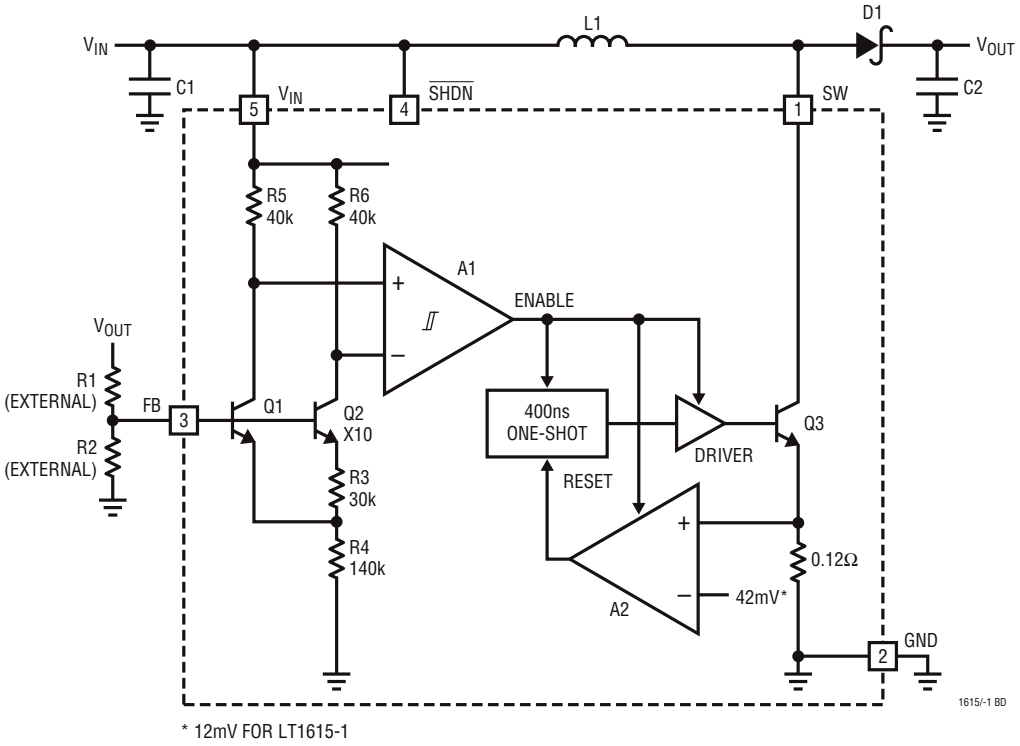
Q301 : LT1615ES5

TOP VIEW



S5 PACKAGE
5-LEAD PLASTIC SOT-23

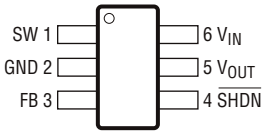
BLOCK DIAGRAM



* 12mV FOR LT1615-1

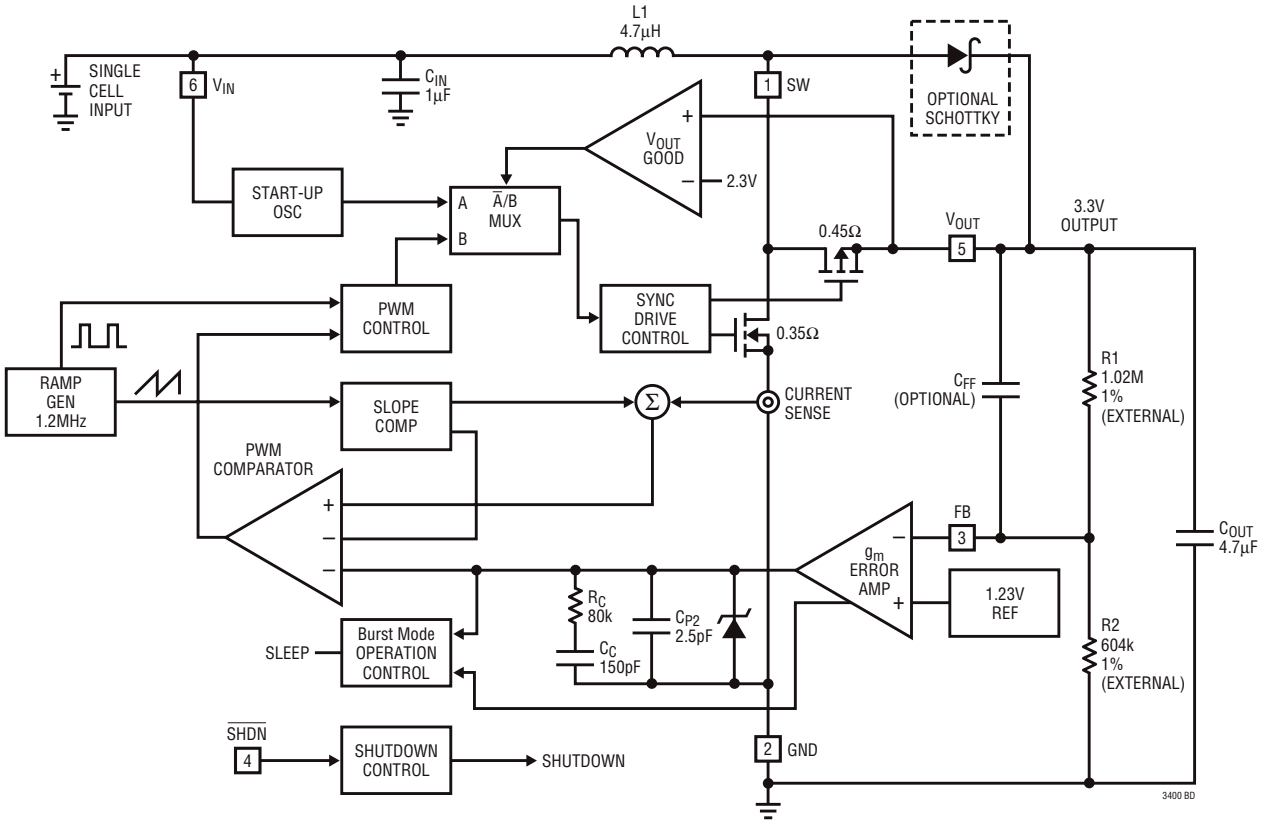
Q304, Q604 : LTC3400BES6

TOP VIEW



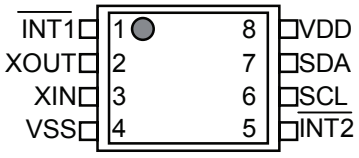
S6 PACKAGE
6-LEAD PLASTIC SOT-23

BLOCK DIAGRAM



Q311 : S-35390A-I8T1G

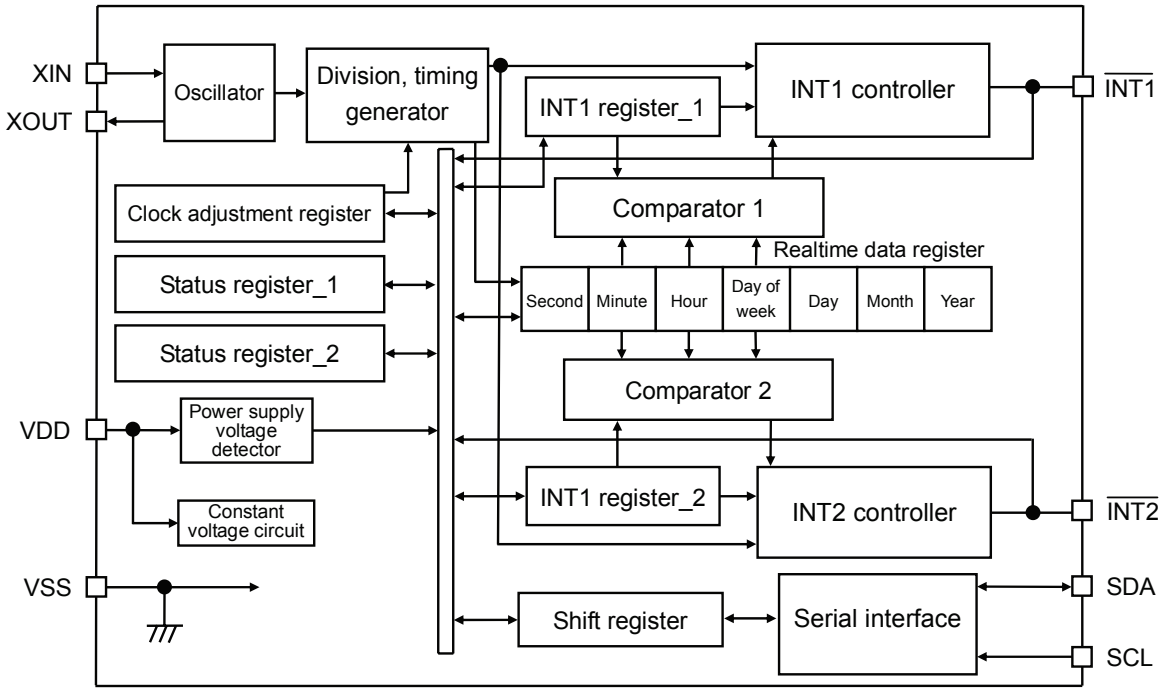
SNT-8A (TOP VIEW)



PIN DESCRIPTION

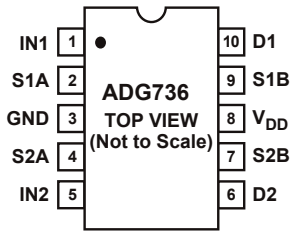
Pin No.	Symbol	Description	Configuration
1	$\overline{INT1}$	Interrupt 1 signal output pin Depending on the mode set by INT1 register_1 and the status register, it outputs low or a clock when the time is reached. It is disabled by rewriting the status register.	Nch open-drain output (no protective diode on the side of VDD)
2	XOUT	Crystal oscillator connect pin (32,768 Hz) (C_d built in, C_g external)	—
3	XIN		
4	VSS	Negative power supply pin (GND)	—
5	$\overline{INT2}$	Interrrupt 2 signal output pin Depending on the mode set by INT1 register_2 and the status register, it outputs low or clock when time is reached. It is disabled by rewriting the status register.	Nch open-drain output (no protective diode on the side of VDD)
6	SCL	Serial clock input pin Since signal processing is done on the SCL signal rising/falling edge, give great care to the rising/falling time and comply strictly with the specifications.	CMOS input (no protective diode on the side of VDD)
7	SDA	Serial data I/O pin Normally, it is pulled up to the V_{DD} voltage by a resistor and connected with another open-drain output or open-collector output device via a wired-OR connection.	Nch open-drain output (no protective diode on the side of VDD) CMOS input
8	VDD	Positive power supply pin	—

BLOCK DIAGRAM



Q405 : ADG736

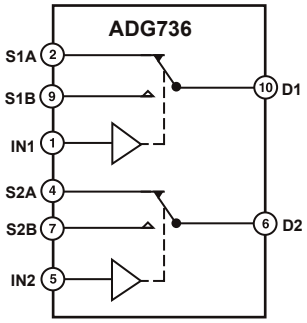
PIN CONFIGURATION
(10-Lead μSOIG)



Truth Table

Logic	Switch A	Switch B
0	OFF	ON
1	ON	OFF

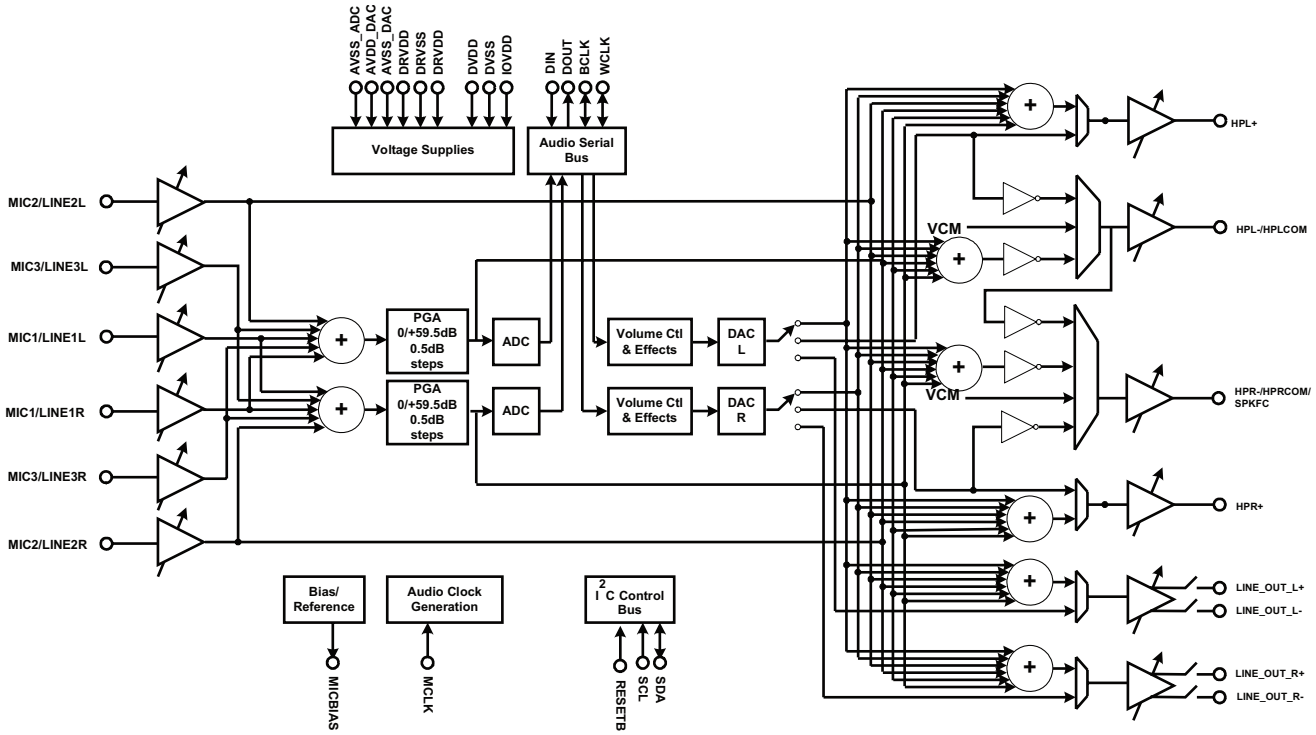
BLOCK DIAGRAM



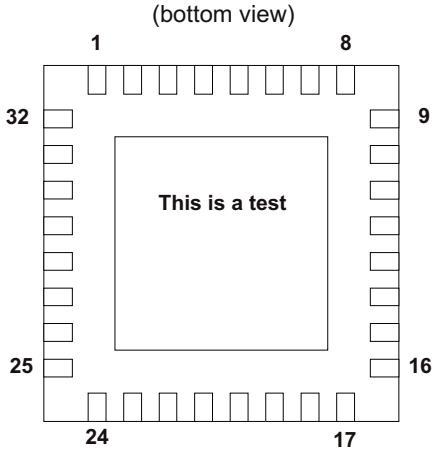
SWITCHES SHOWN FOR A LOGIC "1" INPUT

Q412 : TLV320AIC32

SIMPLIFIED BLOCK DIAGRAM



PIN ASSIGNMENTS

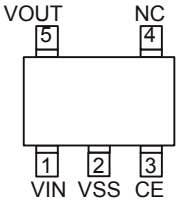


Q412 : TLV320AIC32

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	**QFN NO.**	**I/O**	
MCLK	1	I	Master clock input
BCLK	2	I/O	Audio serial data bus bit clock input/output
WCLK	3	I/O	Audio serial data bus word clock input/output
DIN	4	I	Audio serial data bus data input
DOUT	5	O	Audio serial data bus data output
DVSS	6	I/O	Digital core / I/O Ground Supply, 0 V
IOVDD	7	I/O	Digital I/O voltage supply, 1.1 V – 3.6 V
SCL	8	I/O	I2C serial clock input
SDA	9	I/O	I2C serial data input/output
MIC1L/LINE1L	10	I	Left input 1
MIC1R/LINE1R	11	I	Right input 1
MIC2L/LINE2L	12	I	Left input 2
MIC2R/LINE2R	13	I	Right input 2
MIC3L/LINE3L	14	I	Left input 3
MICBIAS	15	O	Microphone bias voltage output
MIC3R/LINE3R	16	I	Right input 3
AVSS1	17	I	Analog ADC ground supply, 0 V
DRVDD	18	O	Analog ADC and output driver voltage supply, 2.7 V – 3.6 V
HPLOUT	19	O	High power output driver (left +)
HPLCOM	20	O	High power output driver (left - or multi-functional)
DRVSS	21	O	Analog output driver ground supply, 0 V
HPRCOM	22	O	High power output driver (right - or multi-functional)
HPROUT	23	O	High power output driver (right +)
DRVDD	24	O	Analog output driver voltage supply, 2.7 V – 3.6 V
AVDD	25	I	Analog DAC voltage supply, 2.7 V – 3.6 V
AVSS2	26	I	Analog DAC ground supply, 0 V
LEFT_LOP	27	O	Left line output (+)
LEFT_LOM	28	O	Left line output (-)
RIGHT_LOP	29	O	Right lineo output (+)
RIGHT_LOM	30	O	Right line output (-)
$\overline{\text{RESET}}$	31		Reset
DVDD	32	I	Digital core voltage supply, 1.525 V – 1.95 V

Q302 : XC6210B152M, Q303 : XC6210B122M,
Q607 : XC6210B182M, Q415 : XC6210B452M

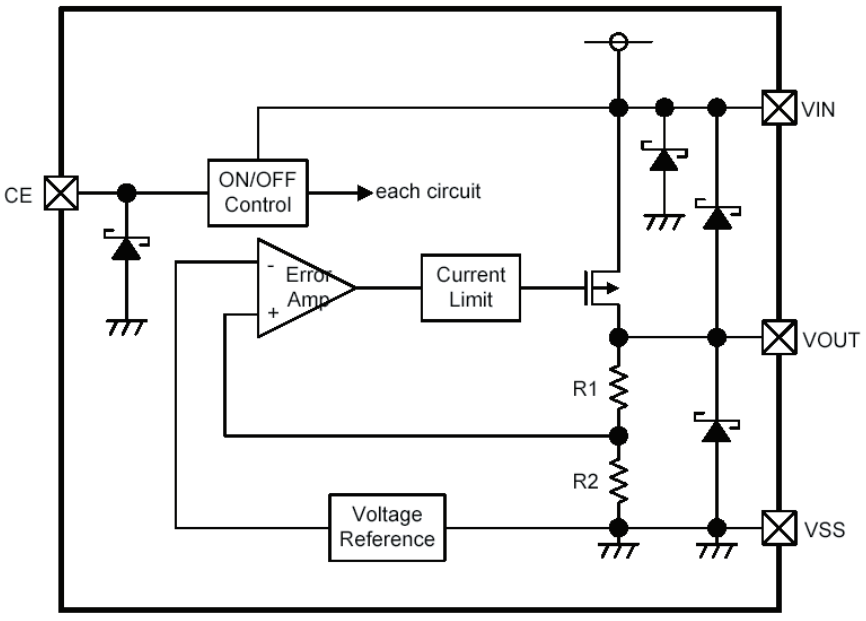


SOT-25
(TOP VIEW)

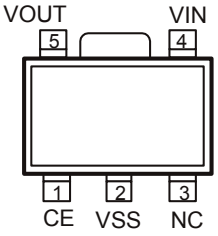
PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTION
SOT-25		
3	CE	ON/OFF Control
1	V_{IN}	Power Input
2	V_{SS}	Ground
5	V_{OUT}	Output
4	NC	No Connection

BLOCK DIAGRAM



Q608 : XC6210B332P

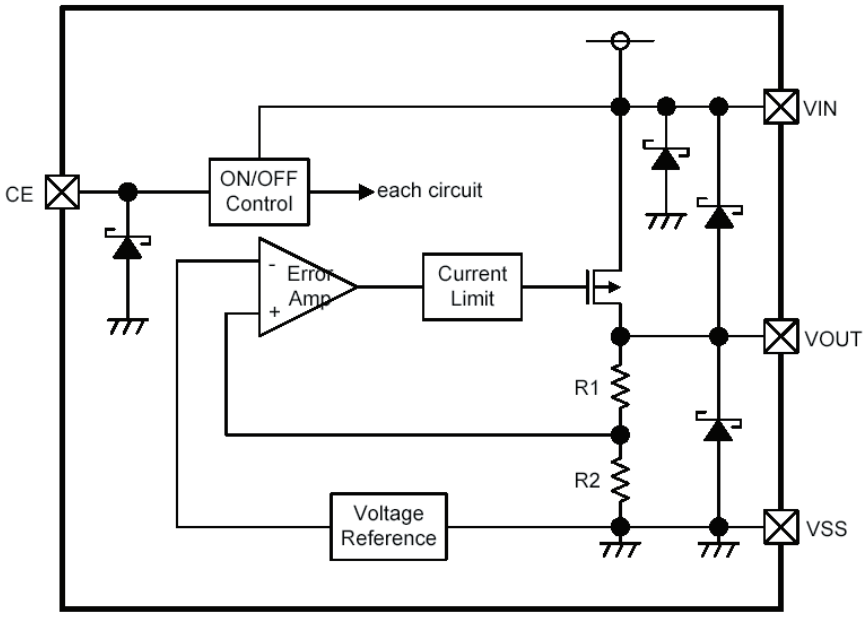


SOT-89-5
(TOP VIEW)

PIN ASSIGNMENT

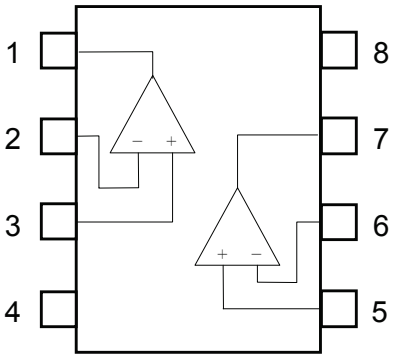
PIN NUMBER SOT-89-5	PIN NAME	FUNCTION
1	CE	ON/OFF Control
4	V_{IN}	Power Input
2	V_{SS}	Ground
5	V_{OUT}	Output
3	NC	No Connection

BLOCK DIAGRAM



Q501, Q611 : NJM2737RB1

PACKAGE OUTLINE



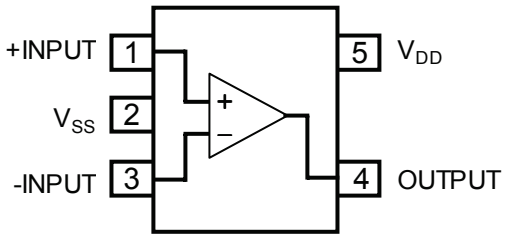
PIN CONFIGURATION

1.OUTPUT1
2.-INPUT1
3.+INPUT1
4.V^-
5.+INPUT2
6.-INPUT2
7.OUTPUT2
8.V^+

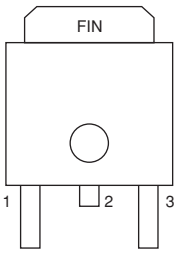
Q502 : NJU7009F3

PACKAGE OUTLINE

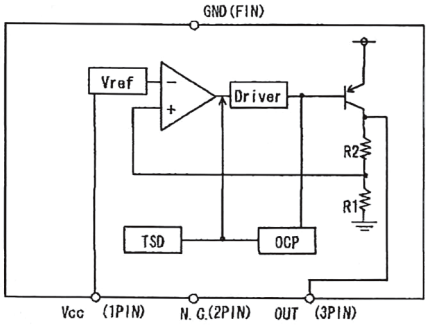
PIN CONFIGURATION



Q617 : BA33BC0FP-E2



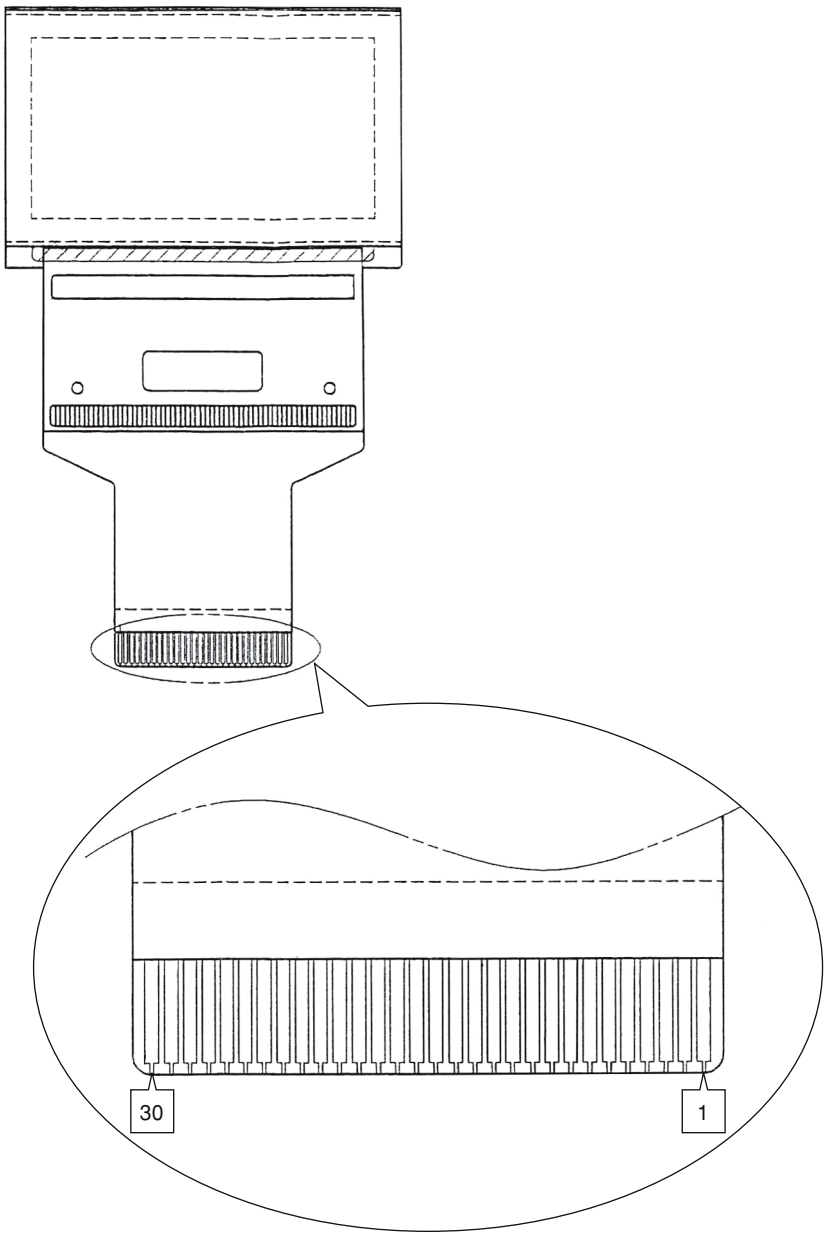
BLOCK DIAGRAM



PIN ASSIGNMENT

PIN NUMBER SOT-25	PIN NAME
1	Vcc
2	N.C.
3	OUT
FIN	GND

V001 : OLED Assy



PIN ASSIGNMENT (CN)

No.	NAME
1	NC
2	VCC
3	VCOMH
4	IREF
5	D7
6	D6
7	D5
8	D4
9	D3
10	D2
11	D1
12	D0
13	E(RD#)
14	R/W#(WR#)
15	D/C#
16	RES#
17	CS#
18	FR
19	BS2
20	BS1
21	VDD 10
22	VDD
23	NC
24	GND
25	NC
26	NC
27	NC
28	NC
29	NC
30	VSS

10. ELECTRICAL PARTS LIST

PARTS INFORMATION

ABBREVIATION AND MARKS			
ANT.	: ANTENNA	BATT.	: BATTERY
CAP.	: CAPACITOR	CER.	: CERAMIC
CONN.	: CONNECTING	DIG.	: DIGITAL
HP	: HEADPHONE	MIC.	: MICROPHONE
μ-PRO	: MICROPROCESSOR	REC.	: RECORDING
RES.	: RESISTOR	SPK	: SPEAKER
SW	: SWITCH	TRANSF.	: TRANSFORMER
TRIM.	: TRIMMING	TRS.	: TRANSISTOR
VAR.	: VARIABLE	X'TAL	: CRYSTAL

NOTE ON SAFETY :

Symbol ⚠ Fire or electrical shock hazard. Only original parts should be used to replaced any part marked with symbol ⚠ . Any other component substitution (other than original type), may increase risk of fire or electrical shock hazard.

安全上の注意：

⚠がついている部品は、安全上重要な部品です。必ず指定されている部品番号の部品を使用して下さい。

NOTE: "nsp" PART IS LISTED FOR REFERENCE ONLY, D&M WILL NOT SUPPLY THESE PARTS.

PWB NAME	POS. NO.	QTY	PART NO. (FOR EUR)	PART NO. (D&M)	PART NAME	DESCRIPTION
					P100 MAIN PWB KIT (00MWI10CS1000)	
					P101 MAIN PWB (00MWI10CS1010)	
P101	J201	1	00MYJ90014790	00MYJ90014790	CONNECTOR	SDKR-9BRS-K13-G
P101	J203	1	00MYJ90014780	00MYJ90014780	CONNECTOR	CSS 5005-0402F
P101	S203	1	00MSP01014720	00MSP01014720	PUSH SWITCH	PUSH SW SPVP110100
					P102 SUB PWB (00MWI10CS1020)	
P102	J601	1	00MYJ04002270	00MYJ04002270	JACK	HEC3600-016110
P102	J603	1	00MYJ01080260	00MYJ01080260	JACK	LGY2209-0300F
P102	J604	1	00MYJ01080260	00MYJ01080260	JACK	LGY2209-0300F
P102	J605	1	00MYJ01080270	00MYJ01080270	JACK	LGY3009-0200F
P102	J606	1	00MYJ01080270	00MYJ01080270	JACK	LGY3009-0200F
P102	J701	1	00MYJ01004520	00MYJ01004520	JACK	HSJ 1637-010512
P102	S701	1	00MSP01014710	00MSP01014710	PUSH SWITCH	SKRELJE010
P102	S702	1	00MSP01014710	00MSP01014710	PUSH SWITCH	SKRELJE010
P102	S703	1	00MSS01030430	00MSS01030430	SLIDE SWITCH	SSSS7A0202
P102	S704	1	00MSS01021150	00MSS01021150	SLIDE SWITCH	SSSS710607
P102	Z701	1	00MZB09050090	00MZB09050090	BATTERY	CR1220/1FC
P102	Z702	1	00M10CS123020	00M10CS123020	CONTACTOR	PLUS CONTACTOR
P102	Z703	1	00M10CS123030	00M10CS123030	CONTACTOR	MINUS CONTACTOR