Service Manual

SR8001 /N1B/N1G/N1S/U1B

AV Surround Receiver

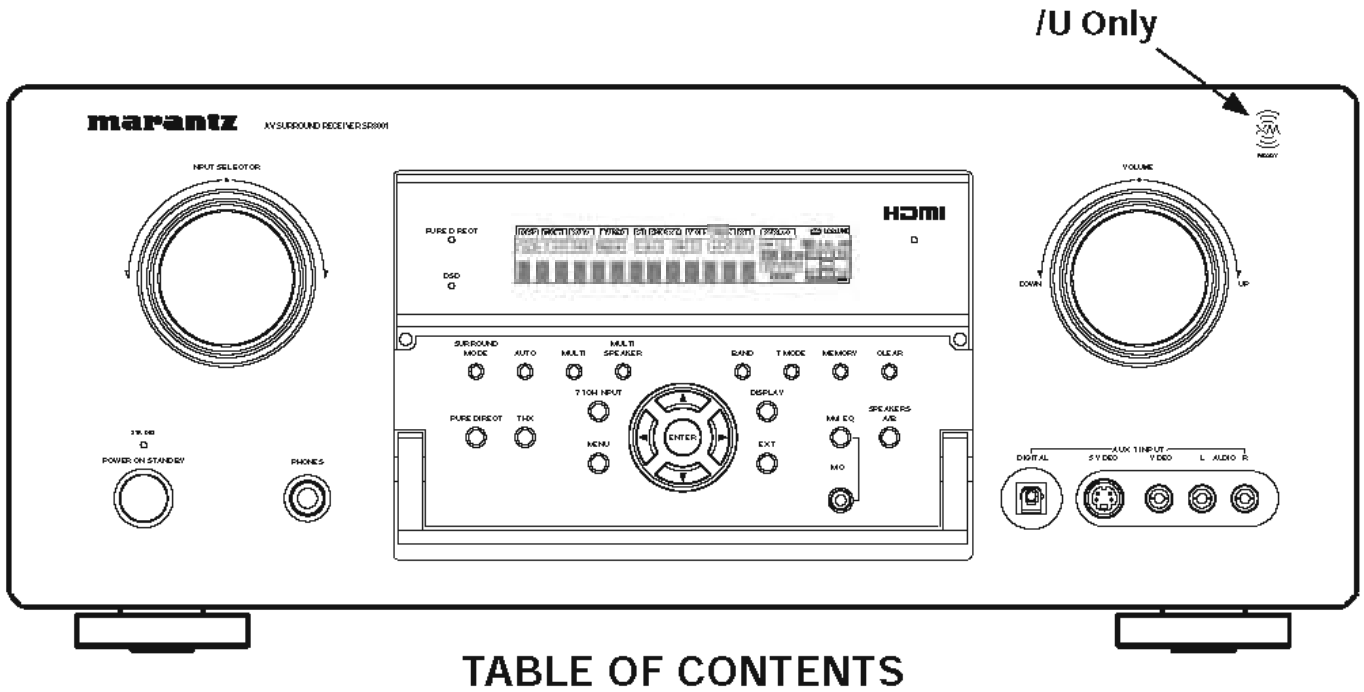


TABLE OF CONTENTS

Please use this service manual with referring to the user guide (D.F.U.) without fail.
修理の際は、必ず取扱説明書を準備し操作方法を確認の上作業を行ってください。

marantz®

SR8001

Part no. 90M06CW855010
First Issue 2006.08
MZ

MARANTZ DESIGN AND SERVICE

Using superior design and selected high grade components, **MARANTZ** company has created the ultimate in stereo sound.
Only original **MARANTZ** parts can insure that your **MARANTZ** product will continue to perform to the specifications for which it is famous.
Parts for your **MARANTZ** equipment are generally available to our National Marantz Subsidiary or Agent.

ORDERING PARTS :

Parts can be ordered either by mail or by Fax.. In both cases, the correct part number has to be specified.
The following information must be supplied to eliminate delays in processing your order :

1. Complete address
2. Complete part numbers and quantities required
3. Description of parts
4. Model number for which part is required
5. Way of shipment
6. Signature : any order form or Fax. must be signed, otherwise such part order will be considered as null and void.

USA

MARANTZ AMERICA, INC
100 CORPORATE DRIVE
MAHWAH, NEW JERSEY 07430
USA

EUROPE / TRADING

MARANTZ EUROPE B.V.
P. O. BOX 8744, BUILDING SILVERPOINT
BEEMDSTRAAT 11, 5653 MA EINDHOVEN
THE NETHERLANDS
PHONE : +31 - 40 - 2507844
FAX : +31 - 40 - 2507860

CANADA

MARANTZ CANADA INC.
5-505 APPLE CREEK BLVD.
MARKHAM, ONTARIO L3R 5B1
CANADA
PHONE : 905 - 415 - 9292
FAX : 905 - 475 - 4159

AUSTRALIA

QualiFi Pty Ltd,
24 LIONEL ROAD,
MT. WAVERLEY VIC 3149
AUSTRALIA
PHONE : +61 - (0)3 - 9543 - 1522
FAX : +61 - (0)3 - 9543 - 3677

THAILAND

MRZ STANDARD CO., LTD
746 - 754 MAHACHAI ROAD.,
WANGBURAPAPIROM, PHRANAKORN,
BANGKOK, 10200 THAILAND
PHONE : +66 - 2 - 222 9181
FAX : +66 - 2 - 224 6795

SINGAPORE

WO KEE HONG DISTRIBUTION PTE LTD
No.1 JALAN KILANG TIMOR
#08-03 PACIFIC TECH CENTRE
SINGAPORE 159303
PHONE : +65 6376 0338
FAX : +65 6376 0166

NEW ZEALAND

WILDASH AUDIO SYSTEMS NZ
14 MALVERN ROAD MT ALBERT
AUCKLAND NEW ZEALAND
PHONE : +64 - 9 - 8451958
FAX : +64 - 9 - 8463554

TAIWAN

PAI- YUING CO., LTD.
6 TH FL NO, 148 SUNG KIANG ROAD,
TAIPEI, 10429, TAIWAN R.O.C.
PHONE : +886 - 2 - 25221304
FAX : +886 - 2 - 25630415

MALAYSIA

WO KEE HONG ELECTRONICS SDN. BHD.
2ND FLOOR BANGUNAN INFINITE CENTRE
LOT 1, JALAN 13/6, 46200 PETALING JAYA
SELANGOR DARUL EHSAN, MALAYSIA
PHONE : +60 - 3 - 7954 8088
FAX : +60 - 3 - 7954 7088

JAPAN

D&M Holdings Inc.
D&M BUILDING, 2-1 NISSHIN-CHO,
KAWASAKI-KU, KAWASAKI-SHI,
KANAGAWA, 210-8569 JAPAN

株式会社 ディーアンドエムホールディングス

本 社 〒210-8569
神奈川県川崎市川崎区日進町2-1 D&Mビル

KOREA

MARANTZ KOREA CO., LTD.
ROOM 604, ELECTRO OFFICE, 16-58,
HANGGANG-RO 3GA, YONGSAN-KU,
SEOUL, 140-013, KOREA
PHONE : +82 - 2 - 323 - 2155
FAX : +82 - 2 - 323 - 2154

CHINA

MARANTZ SHANGHAI TRADING LTD.
ROOM.506 SHANGHAI LIGHT INDUSTRY MANSION
1578 NANJING (WEST) ROAD SHANGHAI
CHINA
TEL : 021 - 6248 - 1064
FAX : 021 - 6248 - 3565

SHOCK, FIRE HAZARD SERVICE TEST :

CAUTION : After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins (with unit NOT connected to AC mains and its Power switch ON), and the face or Front Panel of product and controls and chassis bottom.
Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before it is return to the user/customer.
Ref. UL Standard No. 1492.

In case of difficulties, do not hesitate to contact the Technical Department at above mentioned address.

1. TECHNICAL SPECIFICATIONS

FM TUNER SECTION

Frequency Range ..... 87.5 - 108.0 MHz [/K /N /U]
Usable Sensitivity ..... IHF 1.8 µV/16.4 dBf
Signal to Noise Ratio ..... Mono/Stereo 75/70 dB
Distortion ..... Mono/Stereo 0.2/0.3 %
Stereo Separation ..... 1 kHz 45 dB
Alternate Channel Selectivity ..... ± 300 kHz 60 dB
Image Rejection ..... 98 MHz 70 dB
Tuner Output Level ..... 1 kHz, ± 75 kHz Dev 800 mV

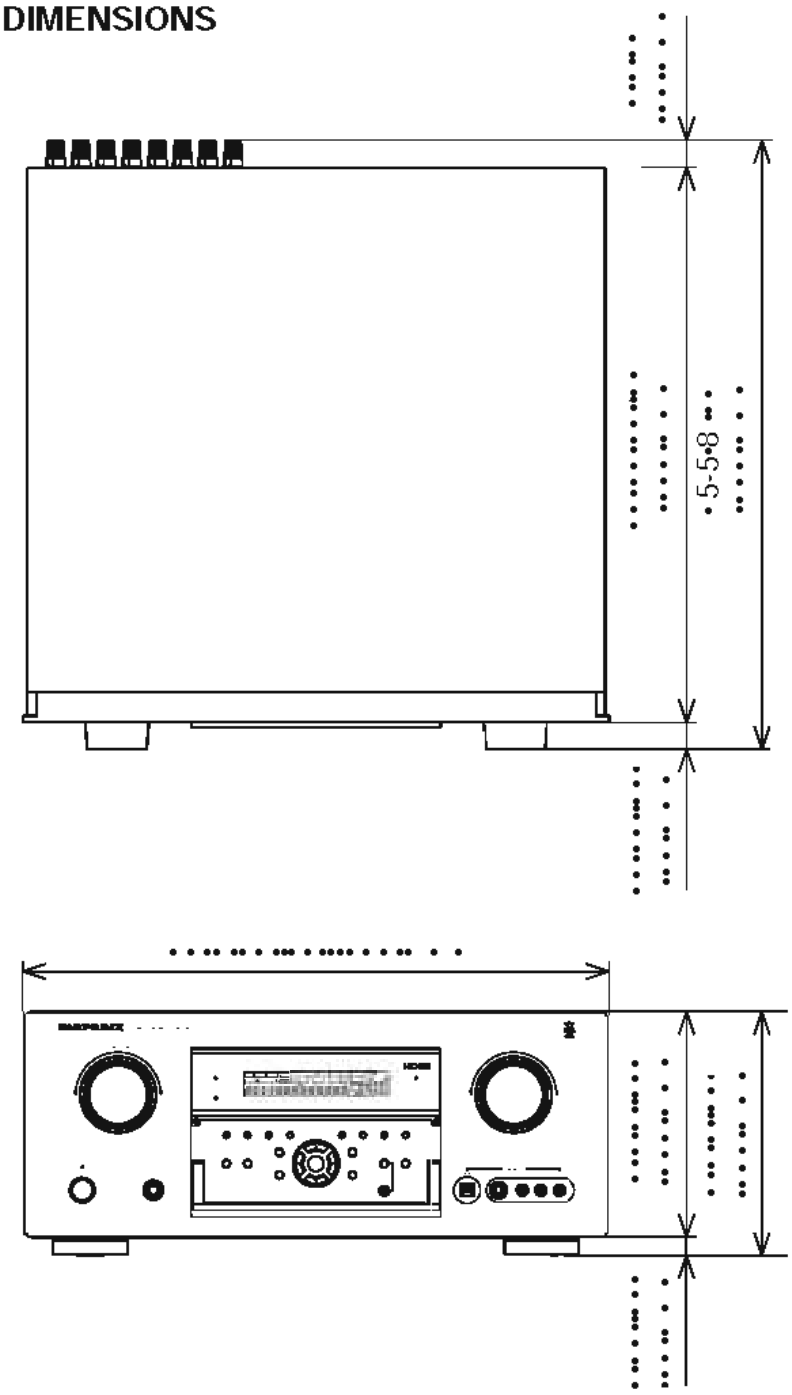
AM TUNER SECTION

Frequency Range ..... 531 - 1602 kHz [/K /N]
..... 520 - 1710 kHz [/U]
Signal to Noise Ratio ..... 50 dB
Usable Sensitivity ..... Loop 400 µV
Distortion ..... 400Hz, 30 % Mod. 0.5 %
Selectivity ..... ± 20 kHz 70 dB

HDMI SECTION

Version ..... 1.2 [INPUT]
..... 1.1 [OUTPUT]

DIMENSIONS



AUDIO SECTION

Power Output (20 Hz - 20 kHz/THD=0.08%)
Front L&R ..... 8 ohms 125 W / Ch
Center ..... 8 ohms 125 W / Ch
Surround L&R ..... 8 ohms 125 W / Ch
Surround Back L&R ..... 8 ohms 125 W / Ch

Front L&R ..... 6 ohms 160 W / Ch
Center ..... 6 ohms 160 W / Ch
Surround L&R ..... 6 ohms 160 W / Ch
Surround Back L&R ..... 6 ohms 160 W / Ch

Input Sensitivity/Impedance ..... 168 mV/ 47 kohms
Signal to Noise Ratio
(Analog Input / Pure Direct) ..... 105 dB
Frequency Response
(Analog Input / Pure Direct) ..... 8 Hz - 100 kHz (± 3 dB)
(Digital Input / 96 kHz PCM) ..... 8 Hz - 45 kHz (± 3 dB)

VIDEO SECTION

Television Format ..... NTSC/PAL
Input Level/Impedance ..... 1 Vp-p/75 ohms
Output Level/Impedance ..... 1 Vp-p/75 ohms
Video Frequency Response ..... 5 Hz to 8 MHz (- 1 dB)
Video Frequency (Component) ..... 5 Hz to 80 MHz (- 1 dB)
S/N ..... 60 dB

GENERAL

Power Requirement ..... AC 220 V 50 Hz [/K]
..... AC 230 V 50/60 Hz [/N]
..... AC 120 V 60 Hz [/U]
Power Consumption ..... 790 W [/N]
..... 6.5 A [/U]

Weight ..... 15.0 kg (33.1 lbs)

ACCESSORIES

Remote Control Unit RC8001SR 1
AAA-size batteries 2
Microphone 1
FM Antenna 1
AM Loop Antenna 1
Front AUX Jack Cover 1
AC cable 1

The relation between the selected surround mode and the input signal

The surround mode is selected with the surround mode buttons on SR7001/SR8001 or the remote control unit. However, the sound you hear is subject to the relationship between the selected surround mode and input signal. That relationship is as follows;

Surround Mode	Input Signal	Decoding	Output Channel					Front information display	
			L/R	C	SL SR	SBL SBR	SubW	Signal format indicators	Channel status
AUTO	Dolby Surr EX	Dolby Digital EX	•	•	•	•	•	DIGITAL EX	L, C, R, SL, SR, S, LFE
	Dolby D (5.1ch)	Dolby Digital 5.1	•	•	•	-	•	DIGITAL	L, C, R, SL, SR, LFE
	Dolby D (2ch)	Dolby Digital 2.0	•	-	-	-	•	DIGITAL	L, R
	Dolby D (2ch Surr)	Pro Logic ••x movie	•	•	•	•	•	DIGITAL SURROUND	L, R, S
	DTS-ES	DTS-ES	•	•	•	•	•	dts, ES	L, C, R, SL, SR, S, LFE
	DTS 96/24	DTS-96/24	•	•	•	-	•	dts 96/24	L, C, R, SL, SR, LFE
	DTS (5.1ch)	DTS 5.1	•	•	•	-	•	dts	L, C, R, SL, SR, LFE
	Multi Ch-PCM	Multi Ch-PCM	•	•	•	-	•	M-PCM	L, C, R, SL, SR, LFE
	Multi Ch-PCM 96kHz	Multi Ch-PCM 96kHz	•	•	•	-	•	M-PCM	L, C, R, SL, SR, LFE
	SA-CD (5.1ch)	Multi Ch-PCM	•	•	•	-	•	SA-CD	L, C, R, SL, SR, LFE
	SA-CD (2ch)	PCM (Stereo)	•	-	-	-	•	SA-CD	L, R
	PCM (Audio)	PCM (Stereo)	•	-	-	-	•	PCM	L, R
	PCM 96kHz	PCM (Stereo 96kHz)	•	-	-	-	•	PCM	L, R
	HDCD	HDCD	•	-	-	-	•	PCM, HDCD	L, R
	Analog	Stereo	•	-	-	-	•	ANALOG	-
	7.1ch input	Multi Ch	•	•	•	•	•	ANALOG	-
SOURCE DIRECT PURE DIRECT	Dolby Surr EX	Dolby Digital EX	•	•	•	•	•	DIGITAL EX	L, C, R, SL, SR, S, LFE
	Dolby D (5.1ch)	Dolby Digital 5.1	•	•	•	-	•	DIGITAL	L, C, R, SL, SR, LFE
	Dolby D (2ch)	Dolby Digital 2.0	•	-	-	-	•	DIGITAL	L, R
	Dolby D (2ch Surr)	Pro Logic ••x movie	•	•	•	•	•	DIGITAL SURROUND	L, R, S
	DTS-ES	DTS-ES	•	•	•	•	•	dts, ES	L, C, R, SL, SR, S, LFE
	DTS 96/24	DTS-96/24	•	•	•	-	•	dts 96/24	L, C, R, SL, SR, LFE
	DTS (5.1ch)	DTS 5.1	•	•	•	-	•	dts	L, C, R, SL, SR, LFE
	Multi Ch-PCM	Multi Ch-PCM	•	•	•	-	•	M-PCM	L, C, R, SL, SR, LFE
	Multi Ch-PCM 96kHz	Multi Ch-PCM 96kHz	•	•	•	-	•	M-PCM	L, C, R, SL, SR, LFE
	SA-CD (5.1ch)	SA-CD (5.1ch)	•	•	•	-	•	SA-CD	L, C, R, SL, SR, LFE
	SA-CD (2ch)	SA-CD (2ch)	•	-	-	-	•	SA-CD	L, R
	PCM (Audio)	PCM (Stereo)	•	-	-	-	-	PCM	L, R
	PCM 96kHz	PCM (Stereo 96kHz)	•	-	-	-	-	PCM	L, R
	HDCD	HDCD	•	-	-	-	-	PCM, HDCD	L, R
	Analog	Stereo	•	-	-	-	-	ANALOG	-
	7.1ch input	Multi Ch	•	•	•	•	•	ANALOG	-
EX/ES	Dolby Surr EX	Dolby Digital EX	•	•	•	•	•	DIGITAL EX	L, C, R, SL, SR, S, LFE
	Dolby D (5.1ch)	Dolby Digital EX	•	•	•	•	•	DIGITAL	L, C, R, SL, SR, LFE
	DTS-ES	DTS-ES	•	•	•	•	•	dts, ES	L, C, R, SL, SR, S, LFE
	DTS (5.1ch)	DTS-ES	•	•	•	•	•	dts	L, C, R, SL, SR, LFE
	Multi-PCM	Multi Ch-PCM + Dolby EX	•	•	•	•	•	M-PCM	L, C, R, SL, SR, LFE
	SA-CD (5.1ch)	Multi Ch-PCM + Dolby EX	•	•	•	•	•	SA-CD	L, C, R, SL, SR, LFE
DOLBY (PL••x movie) (PL••x music) (PL••x game)	Dolby Surr EX	Dolby Digital 5.1	•	•	•	-	•	DIGITAL EX	L, C, R, SL, SR, S, LFE
	Dolby D (5.1ch)	Dolby Digital 5.1	•	•	•	-	•	DIGITAL	L, C, R, SL, SR, LFE
	Dolby D (5.1ch)	Dolby Digital 5.1 + PL••x	•	•	•	•	•	DIGITAL	L, C, R, SL, SR, LFE
	Dolby D (2ch)	Pro Logic ••x	•	•	•	•	•	DIGITAL	L, R
	Dolby D (2ch Surr)	Pro Logic ••x	•	•	•	•	•	DIGITAL SURROUND	L, R, S
	Multi Ch-PCM	Multi Ch-PCM + PL••x	•	•	•	•	•	M-PCM	L, C, R, SL, SR, LFE
	SA-CD (5.1ch)	Multi Ch-PCM + PL••x	•	•	•	•	•	SA-CD	L, C, R, SL, SR, LFE
	SA-CD (2ch)	Pro Logic ••x	•	•	•	•	•	SA-CD	L, R
	PCM (Audio)	Pro Logic ••x	•	•	•	•	•	PCM	L, R
	HDCD	Pro Logic ••x	•	•	•	•	•	PCM, HDCD	L, R
	Analog	Pro Logic ••x	•	•	•	•	•	ANALOG	-
DTS (Neo 6 Cinema) (Neo 6 Music)	DTS-ES	DTS 5.1	•	•	•	-	•	dts, ES	L, C, R, SL, SR, S, LFE
	DTS 96/24	DTS-96/24	•	•	•	-	•	dts 96/24	L, C, R, SL, SR, LFE
	DTS (5.1ch)	DTS 5.1	•	•	•	-	•	dts	L, C, R, SL, SR, LFE
	Dolby D (2ch)	Neo 6	•	•	•	•	•	DIGITAL	L, R
	Dolby D (2ch Surr)	Neo 6	•	•	•	•	•	DIGITAL SURROUND	L, R, S
	SA-CD (2ch)	Neo 6	•	•	•	•	•	SA-CD	L, R
	PCM(Audio)	Neo 6	•	•	•	•	•	PCM	L, R
	HDCD	Neo 6	•	•	•	•	•	PCM, HDCD	L, R
	Analog	Neo 6	•	•	•	•	•	ANALOG	-
CS••Cinema CS••Music CS••Mono	Dolby D (2ch)	CS••	•	•	•	•	•	DIGITAL	L, R
	Dolby D (2ch Surr)	CS••	•	•	•	•	•	DIGITAL SURROUND	L, R, S
	SA-CD (2ch)	CS••	•	•	•	•	•	SA-CD	L, R
	PCM(Audio)	CS••	•	•	•	•	•	PCM	L, R
	HDCD	CS••	•	•	•	•	•	PCM, HDCD	L, R
	Analog	CS••	•	•	•	•	•	ANALOG	-
STEREO	Dolby Surr EX	Stereo	•	-	-	-	•	DIGITAL EX	L, C, R, SL, SR, S, LFE
	Dolby D (5.1ch)	Stereo	•	-	-	-	•	DIGITAL	L, C, R, SL, SR, LFE
	Dolby D (2ch)	Stereo	•	-	-	-	•	DIGITAL	L, R
	Dolby D (2ch Surr)	Stereo	•	-	-	-	•	DIGITAL SURROUND	L, R, S
	DTS-ES	Stereo	•	-	-	-	•	dts, ES	L, C, R, SL, SR, S, LFE
	DTS 96/24	Stereo	•	-	-	-	•	dts 96/24	L, C, R, SL, SR, LFE
	DTS (5.1ch)	Stereo	•	-	-	-	•	dts	L, C, R, SL, SR, LFE
	Multi Ch-PCM	Stereo	•	-	-	-	•	M-PCM	L, C, R, SL, SR, LFE
	Multi Ch-PCM 96kHz	Stereo	•	-	-	-	•	M-PCM	L, C, R, SL, SR, LFE
	SA-CD (5.1ch)	Stereo	•	-	-	-	•	SA-CD	L, C, R, SL, SR, LFE
	SA-CD (2ch)	Stereo	•	-	-	-	•	SA-CD	L, R
	PCM (Audio)	Stereo	•	-	-	-	•	PCM	L, R
	PCM 96kHz	Stereo	•	-	-	-	•	PCM	L, R
	HDCD	Stereo	•	-	-	-	•	PCM, HDCD	L, R
	Analog	Stereo	•	-	-	-	•	ANALOG	-

Surround Mode	Input Signal	Decoding	Output Channel					Front information display	
			L/R	C	SL SR	SBL SBR	SubW	Signal format indicators	Channel status
Dolby Virtual Speaker	Dolby Surr EX	Dolby Virtual Speaker	•	-	-	-	-	DIGITAL EX	L, C, R, SL, SR, S, LFE
	Dolby D (5.1ch)	Dolby Virtual Speaker	•	-	-	-	-	DIGITAL	L, C, R, SL, SR, LFE
	Dolby D (2ch)	Dolby Virtual Speaker	•	-	-	-	-	DIGITAL	L, R
	Dolby D (2ch Surr)	Dolby Virtual Speaker	•	-	-	-	-	DIGITAL SURROUND	L, R, S
	DTS-ES	Dolby Virtual Speaker	•	-	-	-	-	dts, ES	L, C, R, SL, SR, S, LFE
	DTS 96/24	Dolby Virtual Speaker	•	-	-	-	-	dts 96/24	L, C, R, SL, SR, LFE
	DTS (5.1ch)	Dolby Virtual Speaker	•	-	-	-	-	dts	L, C, R, SL, SR, LFE
	Multi Ch-PCM	Dolby Virtual Speaker	•	-	-	-	-	M-PCM	L, C, R, SL, SR, LFE
	SA-CD (5.1ch)	Dolby Virtual Speaker	•	-	-	-	-	SA-CD	L, C, R, SL, SR, LFE
	SA-CD (2ch)	Dolby Virtual Speaker	•	-	-	-	-	SA-CD	L, R
	PCM (Audio)	Dolby Virtual Speaker	•	-	-	-	-	PCM	L, R
	HDCD	Dolby Virtual Speaker	•	-	-	-	-	PCM, HDCD	L, R
	Analog	Dolby Virtual Speaker	•	-	-	-	-	ANALOG	-
Multi Ch Stereo	Dolby Surr EX	Dolby Digital EX	•	•	•	•	•	DIGITAL EX	L, C, R, SL, SR, S, LFE
	Dolby D (5.1ch)	Dolby Digital 5.1	•	•	•	-	•	DIGITAL	L, C, R, SL, SR, LFE
	Dolby D (2ch)	Multi Channel Stereo	•	•	•	•	•	DIGITAL	L, R
	Dolby D (2ch Surr)	Multi Channel Stereo	•	•	•	•	•	DIGITAL SURROUND	L, R, S
	DTS-ES	DTS-ES	•	•	•	•	•	dts, ES	L, C, R, SL, SR, S, LFE
	DTS 96/24	DTS-96/24	•	•	•	-	•	dts 96/24	L, C, R, SL, SR, LFE
	DTS (5.1ch)	DTS 5.1	•	•	•	-	•	dts	L, C, R, SL, SR, LFE
	Multi Ch-PCM	Multi Ch-PCM	•	•	•	-	•	M-PCM	L, C, R, SL, SR, LFE
	Multi Ch-PCM 96kHz	Multi Ch-PCM 96kHz	•	•	•	-	•	M-PCM	L, C, R, SL, SR, LFE
	SA-CD (5.1ch)	Multi Ch-PCM	•	•	•	-	•	SA-CD	L, C, R, SL, SR, LFE
	SA-CD (2ch)	Multi Channel Stereo	•	•	•	•	•	SA-CD	L, R
	PCM (Audio)	Multi Channel Stereo	•	•	•	•	•	PCM	L, R
	HDCD	Multi Channel Stereo	•	•	•	•	•	PCM, HDCD	L, R
	Analog	Multi Channel Stereo	•	•	•	•	•	ANALOG	-
Dolby H.P	Dolby Surr EX	Dolby H.P	•	-	-	-	-	DIGITAL EX	L, C, R, SL, SR, S, LFE
	Dolby D (5.1ch)	Dolby H.P	•	-	-	-	-	DIGITAL	L, C, R, SL, SR, LFE
	Dolby D (2ch)	Dolby H.P	•	-	-	-	-	DIGITAL	L, R
	Dolby D (2ch Surr)	Dolby H.P	•	-	-	-	-	DIGITAL SURROUND	L, R, S
	DTS-ES	Dolby H.P	•	-	-	-	-	dts, ES	L, C, R, SL, SR, S, LFE
	DTS 96/24	Dolby H.P	•	-	-	-	-	dts 96/24	L, C, R, SL, SR, LFE
	DTS (5.1ch)	Dolby H.P	•	-	-	-	-	dts	L, C, R, SL, SR, LFE
	Multi Ch-PCM	Dolby H.P	•	-	-	-	-	M-PCM	L, C, R, SL, SR, LFE
	SA-CD (5.1ch)	Dolby H.P	•	-	-	-	-	SA-CD	L, C, R, SL, SR, LFE
	SA-CD (2ch)	Dolby H.P	•	-	-	-	-	SA-CD	L, R
	PCM (Audio)	Dolby H.P	•	-	-	-	-	PCM	L, R
	HDCD	Dolby H.P	•	-	-	-	-	PCM, HDCD	L, R
	Analog	Dolby H.P	•	-	-	-	-	ANALOG	-
THX (THX Games)	Dolby Surr EX	Dolby Digital + THX Surround EX	•	•	•	•	•	DIGITAL EX	L, C, R, SL, SR, S, LFE
	Dolby D (5.1ch)	Dolby Digital 5.1+ THX 5.1	•	•	•	-	•	DIGITAL	L, C, R, SL, SR, LFE
	Dolby D (2ch)	Pro Logic ••x movie + THX	•	•	•	•	•	DIGITAL	L, R
	Dolby D (2ch Surr)	Pro Logic ••x movie + THX	•	•	•	•	•	DIGITAL SURROUND	L, R, S
	DTS-ES	DTS-ES + THX	•	•	•	•	•	dts, ES	L, C, R, SL, SR, S, LFE
	DTS (5.1ch)	DTS + THX 5.1	•	•	•	-	•	dts	L, C, R, SL, SR, LFE
	Multi Ch-PCM	Multi Ch-PCM + THX5.1	•	•	•	-	•	M-PCM	L, C, R, SL, SR, LFE
	SA-CD (5.1ch)	Multi Ch-PCM + THX5.1	•	•	•	-	•	SA-CD	L, C, R, SL, SR, LFE
	SA-CD (2ch)	Pro Logic ••x movie + THX	•	•	•	•	•	SA-CD	L, R
	PCM (Audio)	Pro Logic ••x movie + THX	•	•	•	•	•	PCM	L, R
	HDCD	Pro Logic ••x movie + THX	•	•	•	•	•	PCM, HDCD	L, R
	Analog	Pro Logic ••x movie + THX	•	•	•	•	•	ANALOG	-
THX Select2 (THX EX) (THX Music) (THX Games)	Dolby Surr EX	Dolby Digital + THX Surround EX	•	•	•	•	•	DIGITAL EX	L, C, R, SL, SR, S, LFE
	Dolby D (5.1ch)	Dolby Digital 5.1+ THX Select2 Cinema	•	•	•	•	•	DIGITAL	L, C, R, SL, SR, LFE
	Dolby D (2ch)	Pro Logic ••x movie + THX	•	•	•	•	•	DIGITAL	L, R
	Dolby D (2ch Surr)	Pro Logic ••x movie + THX	•	•	•	•	•	DIGITAL SURROUND	L, R, S
	DTS-ES	DTS-ES + THX	•	•	•	•	•	dts ES	L, C, R, SL, SR, S, LFE
	DTS (5.1ch)	DTS + THX Select2 Cinema	•	•	•	•	•	dts	L, C, R, SL, SR, LFE
	Multi Ch-PCM	Multi Ch-PCM + THX Select2 Cinema	•	•	•	•	•	M-PCM	L, C, R, SL, SR, LFE
	SA-CD (5.1ch)	Multi Ch-PCM + THX Select2 Cinema	•	•	•	•	•	SA-CD	L, C, R, SL, SR, LFE
	SA-CD (2ch)	Pro Logic ••x movie + THX	•	•	•	•	•	SA-CD	L, R
	PCM (Audio)	Pro Logic ••x movie + THX	•	•	•	•	•	PCM	L, R
	HDCD	Pro Logic ••x movie + THX	•	•	•	•	•	PCM, HDCD	L, R
	Analog	Pro Logic ••x movie + THX	•	•	•	•	•	ANALOG	-

Notes:

3. POWER AMPLIFIER ADJUSTMENT

Idling Current Alignment

1. Each of the measurement points are provided with the two test points. Set a digital Voltage meter to DC voltage input, connect the meter to the test points at both contact points.
2. After the setup above, turn on the main switch.
3. Adjust variable resistors (VR41 - VR71) according to the digital voltmeter readings. The target setting value is the following table for each channel.

Settings: Master Volume — Minimum
Speaker out — No Load
Top lid — OPEN

アイドリング電流調整

1. 電源を ON する前にそれぞれの "+" 端子と "-" 端子間にデジタルボルトメーターを接続します。デジタルボルトメーターを DC 電圧入力にセットします。
2. 上記のセットアップの後に、本機の電源を ON します。
3. デジタルボルトメーターの電圧値を監視しながら可変抵抗器 (VR41 ～ VR71) を調節します。
   各チャンネルの目標値は下記の表を参照下さい。

セッティング : マスター・ボリューム — 最小
スピーカー接続 — 無し
トップカバー — 無し

Channel	Alignment Point	Measurement Point
Front L	VR41	CN41
Center	VR61	CN61
Front R	VR51	CN51
Surround L	VR42	CN42
Surround R	VR52	CN52
Surround Back L	VR62	CN62
Surround Back R	VR71	CN71

Time Table of Idling Current Rise

After Turning ON	Ambient temperature 20 to 30 degrees centigrade
	Measurement Voltage
10 min.	2.4 mV ± 0.3 mV
20 min.	2.4 mV ± 0.3 mV
30 min.	2.4 mV ± 0.3 mV

4. SERVICE MODE

MAIN CPU Version, DSP Version, HDMI CPU Version and Segment Check Mode

1. Connect the mains cord into the unit.
2. Press the **POWER ON/STANDBY** button for turn on the unit.
3. Press the **PURE DIRECT**, **7.1CH INPUT** and **MultEQ** buttons simultaneously more then 3 seconds.
4. The FL display shows "SERVICE MODE" for 2 seconds then shows the model name.

S	E	R	V	I	C	E		M	O	D	E	
			S	R	8	0	0	1				

5. Press the **ENTER** button, the software version of the MAIN CPU (IC17) is displayed in the format below.

V	0	6	0	7	0	7		3	N			

Year, Month, Date, Release No., Destination

6. Press the **ENTER** button again, the serial Number of the unit is displayed.

M	Z		2	9	4	9	6	7	2	9	5	

7. Press the **ENTER** button, the software version of the TI DSP (IC34) is displayed in the format below.

T	I		V	0	3	8	6	0	6	1	2	1

Year, Month, Date, Release No.

8. Press the **ENTER** button, the software version of the HDMI CPU (IC90) is displayed in the format below.

H	D	M	I		V	e	r	.	h	1	8	

9. Press the **ENTER** button again, the left half, right half and center of the label area in the FLD light on and off each other.
10. Press the **ENTER** button again, the segments of the character area in the FLD flick in checker pattern.
11. Press the **ENTER** button again, all the FL segments turns off.
12. Press the **ENTER** button again to quit this mode.

4. SERVICE MODE

MAIN CPU Version, DSP Version, HDMI CPU Version and Segment Check Mode

1. 本機に電源コードを接続します。
2. **POWER ON/STANDBY**ボタンを押し、本機の電源を入れます。
3. **PURE DIRECT**, **7.1CH INPUT**, **MultEQ**の3つのボタンを同時に3秒以上押します。
4. FLに"SERVICE MODE"と2秒表示し、次にモデル名を表示します。

S	E	R	V	I	C	E		M	O	D	E	
			S	R	8	0	0	1				

5. **ENTER**ボタンを押すと、MAINマイコン(IC17)のバージョンが表示されます。

V	0	6	0	7	0	7		3	N			

Year, Month, Date, リリース No., 仕向け

6. 更に**ENTER**ボタンを押すと、シリアルナンバーが表示されます。

M	Z		2	9	4	9	6	7	2	9	5	

7. 更に**ENTER**ボタンを押すと、TI DSP (IC34)のバージョンが表示されます。

T	I		V	0	3	8	6	0	6	1	2	1

Year, Month, Date, リリース No.

8. 更に**ENTER**ボタンを押すと、HDMI CPUのバージョンが表示されます。

H	D	M	I		V	e	r	.	h	1	8	

9. 更に**ENTER**ボタンを押すと、FLのラベル部分の左半分と右半分および中心部が交互に点灯と消灯を繰り返します。
10. 更に**ENTER**ボタンを押すと、FLのキャラクタセグメント部がチェッカーフラグのように点灯と消灯を繰り返します。
11. 更に**ENTER**ボタンを押すと、FLは全消灯します。
12. 更に**ENTER**ボタンを押すと、サービスモードを終了します。

Product Reset

To reset the back up memory of the unit into the default status, follow the procedure below.

Should the operation or display seem to be abnormal, reset the unit with the following procedure.

To turn on the SR7001/SR8001, press and hold the **MULTI** and **SPEAKERS A/B** buttons simultaneously for 3 seconds or more.

Remember that the procedure will reset the settings of the function selector, Surround mode, delay time, TUNER PRESET etc., to their initial settings.

Personal notes:

5. SYSTEM ERROR

1. Trouble in EEP-ROM (DSP PWB / IC15) Interface

- If the communication error that ACK did not return by communication with EEP-ROM (DSP PWB / IC15) occurred 2 seconds and more.

CHECKPOINT

1. Turn the power on. Are the IIC Clock Line (IC17/130pin - IC15 / 6pin) normal?
2. Are the IIC Data Line (IC17/131pin - IC15 / 5pin) normal?
3. Is +3.3V voltage supplied to 8pin of IC15?
4. When no problem to the above 1-3, replace IC15.

2. Trouble in +5V Supply

- If +5V inputted into 68pin of IC17 is troubled and the following the fault of 1 - 4.

CHECKPOINT

1. Turn the power on. Is +5V voltage supplied to CN30/6pin and CN30/7pin of DSP PWB.
2. Is the signal of IC17 H? 29pin (Power Amp Fail)= H. (When 2 second or more "L" state is continuing to 29pin, Abnormalities have occurred in the POWER AMP circuit.)
3. Is the signal of IC17 H? 66pin (Power Line Fail)= H. (When the 2 second and more "L" state is continuing to 66pin, Abnormalities have occurred to +-15V power supply or the power supply for Power Amp.)
4. Is the signal of IC17 H? 77pin (Power Down)= H. (When 2 second and more "L" state is continuing to 77pin, Abnormalities have occurred in IC74 and around IC77 circuit of STANDBY PWB.)

3. Trouble in Protection

- When unusual states, such as overload of Power Amp and DC output, are detected.
  The unusual detection method is the following.
  1. When "L" of 100 msec and more is detected by 29pin (Power Amp Fail) of IC17, the unit will be in standby mode and STANDBY LED will blink.

5. SYSTEM ERROR

1. EEP-ROM (DSP PWB / IC15) Interface異常検出表示

C	H	E	C	K		E	2	P		I	F	

- EEP-ROM (DSP PWB / IC15)との通信でACKが帰ってこない状態（通信エラー）が約２秒以上生じた時に表示されます。

回路上の確認箇所

①. Power ON時にIIC Clock Line (IC17/130pin - IC15 / 6pin)が正常なのを確認する。
②. Power ON時にIIC Data Line (IC17/131pin - IC15 / 5pin)が正常なのを確認する。
③. IC15 / 8pinにVCC (+3.3V)が供給されていることを確認する。
④. 上記の①ー③に不具合が生じていない場合はIC15の不良が考えられます。

2. +5V Supply異常検出表示

C	H	E	C	K		P	O	W	5			

- 電源ON時に68pinに入力される+5Vの検出が出来なかった場合に表示されます。 又、 下記の②～④の不具合発生時にも同様の表示を行います。

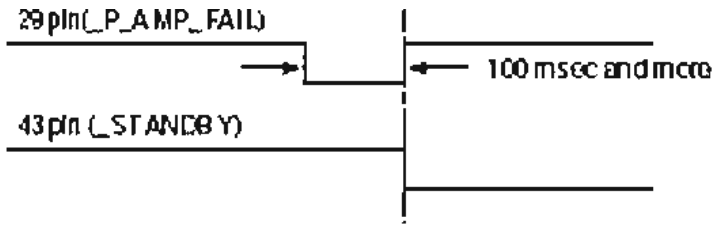
回路上の確認箇所

①. 電源ON時にCN30 (DSP PWB) 6,7pinに+5Vが供給されていることを確認する。
②. 電源ON時にマイコンの29pin (Power Amp Fail) が "H"になっていることを確認する。（29pinが電源ONしてから２秒以上"L"状態が継続している場合はPOWER AMP回路に異常が発生している）
③. 電源ON時にマイコンの66pin(Power Line Fail)が "H"になっていることを確認する。（66pinが電源ONしてから2秒以上"L"状態が継続している場合は+/-15V電源又は、Power Amp用の電源に異常が発生している）
④. 電源ON時にマイコンの77pin (Power Down)が "H"になっていることを確認する。（77pinが電源ONしても"L"状態が継続している場合はSTANDBY PWB上のIC74及び周辺回路に異常が発生している）

3. PROTECTION検出表示

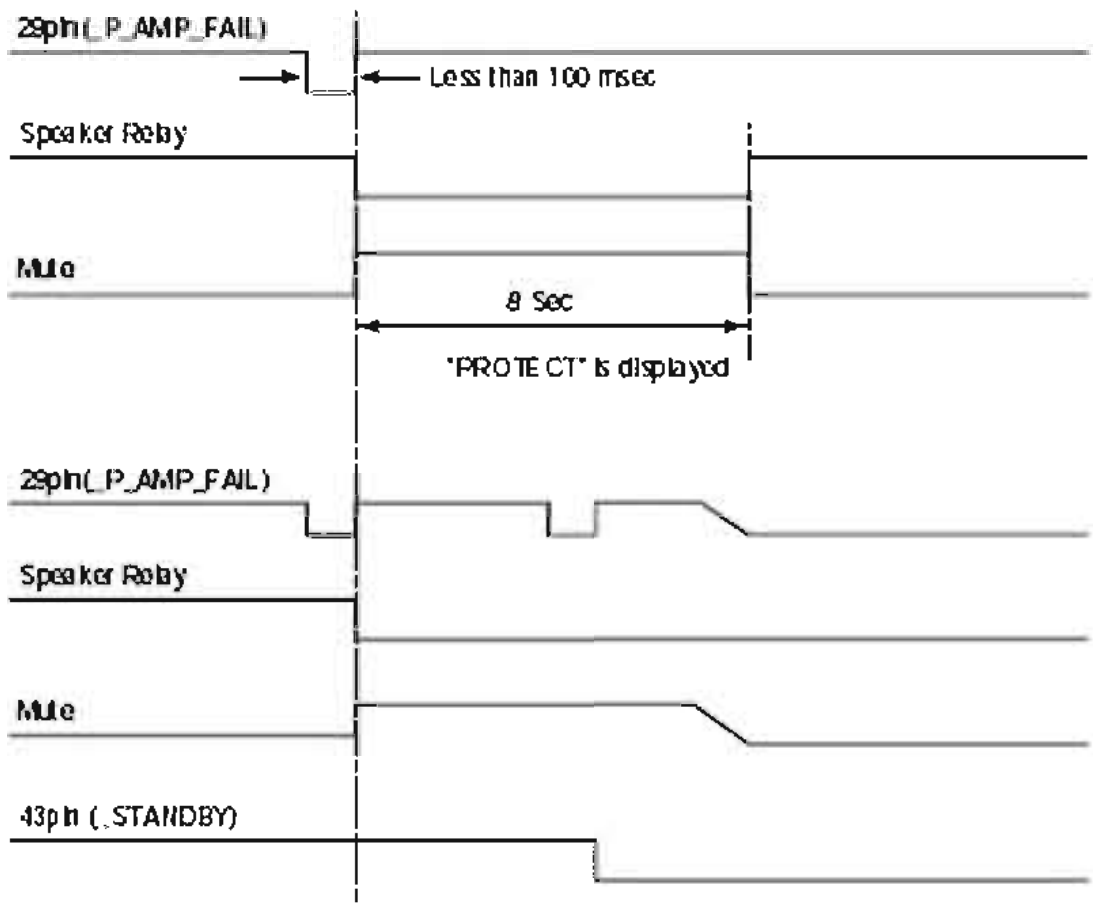
P	R	O	T	E	C	T						

- Power Ampの過負荷、DC出力等の異常状態が検出された際に表示されます。
  また、異常検出は以下の様に行われます。
  ①. マイコンの29pin (Power Amp Fail)に100msec以上の "L"検出がされた場合はSETをSTANDBY状態にしてFront Panel上のSTANDBY LEDを点滅状態にします



2. When "L" of less than 100msec is detected by 29pin (Power Amp Fail) of IC17, Speaker Relay becomes OFF and MUTE becomes ON state, and the state is held for 8 seconds. At this time, "PROTECT" is displayed. When similar abnormal detection was considered to be it for these 8 seconds, the unit will be in standby mode and STANDBY LED will blink. When it was not detected abnormally for 8 seconds, the unit returns to normal use state.

②. マイコンの29pin (Power Amp Fail)に100msec未満の"L"検出がされた場合はSpeaker RelayをOFF, MUTEをON状態にして8秒間その状態を保持する。この間、FL Displayに "PROTECT"の表示を行う。この8秒間に同様の異常検出がされた場合はSETをSTANDBY状態にしてFront Panel上のSTANDBY LEDを点滅状態にします。8秒間、異常検出されなかった時はSETを通常使用状態に戻します。



CHECKPOINT

1. Check AMP PWB.
2. When AMP does not have a problem, it is confirmed whether there is not abnormality by disconnection of pattern of 29pin (Power Amp Fail) and the detect circuit.

回路上の確認箇所

①. Power Ampに不具合が生じている場合は修理を行う。

②. Power Ampに不具合が無い場合は、29pin (Power Amp Fail)のパターンの断線及び検出回路に異常が無いか確認する。

4. **Trouble in Other**

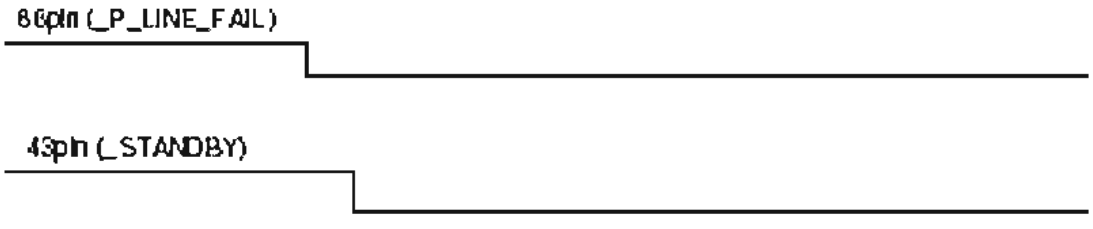
(The contents of detection are not indicated to FL.)

- When the abnormalities of ±15V power supply and the ±power supply for Power Amp are detected, the unit will be in standby mode. The detection is performed by 66pin (P LINE FAIL).

4．その他の異常検出

（FLにCaution表示はしません）

- ±15V電源及び、Power Amp用の±電源の異常を検出した場合、SETをSTANDBYにします。検出は66pin (_P_LINE_FAIL)で行われます。



CHECKPOINT

1. Check Power supply circuit
2. When Power supply circuit does not have a problem, it is confirmed whether there is not abnormality by disconnection of pattern of 66pin (Power Line Fail) and the detect circuit.

回路上の確認箇所

①. 上記の電源回路に不具合が生じている場合は修理を行う。

②. 電源回路に不具合が無い場合は、66pin (Power Line Fail)のパターンの断線及び検出回路に異常が無いか確認する。

6. UPDATE FIRMWARE

[A] SOFTWARE (fdtv306r00.exe) DOWNLOADS AND INSTALLS PROCEDURE

[A-1] DOWNLOADS OF THE SOFTWARE

(Flash Development Toolkit: the rest is FDT)

Download the software for update of the HDMI CPU.

1. Launch the browser.
2. Type the "http://www.renesas.com/" into an address. And click the **Go** or press the **Enter** on keyboard of PC.

NOTE : This site is managed by RENESAS. The following explanation may differ from the actual composition. When different, please proceed along with the site composition of RENESAS.

3. Click the **GLOBAL SITE**.

6. UPDATE FIRMWARE

[A] SOFTWARE (fdtv306r00.exe) DOWNLOADS AND INSTALLS PROCEDURE

[A-1] DOWNLOADS OF THE SOFTWARE

(Flash Development Toolkit: 以下 FDT)

HDMIマイコンの書き込みのためのソフトウェア(FDT)をダウンロードします。

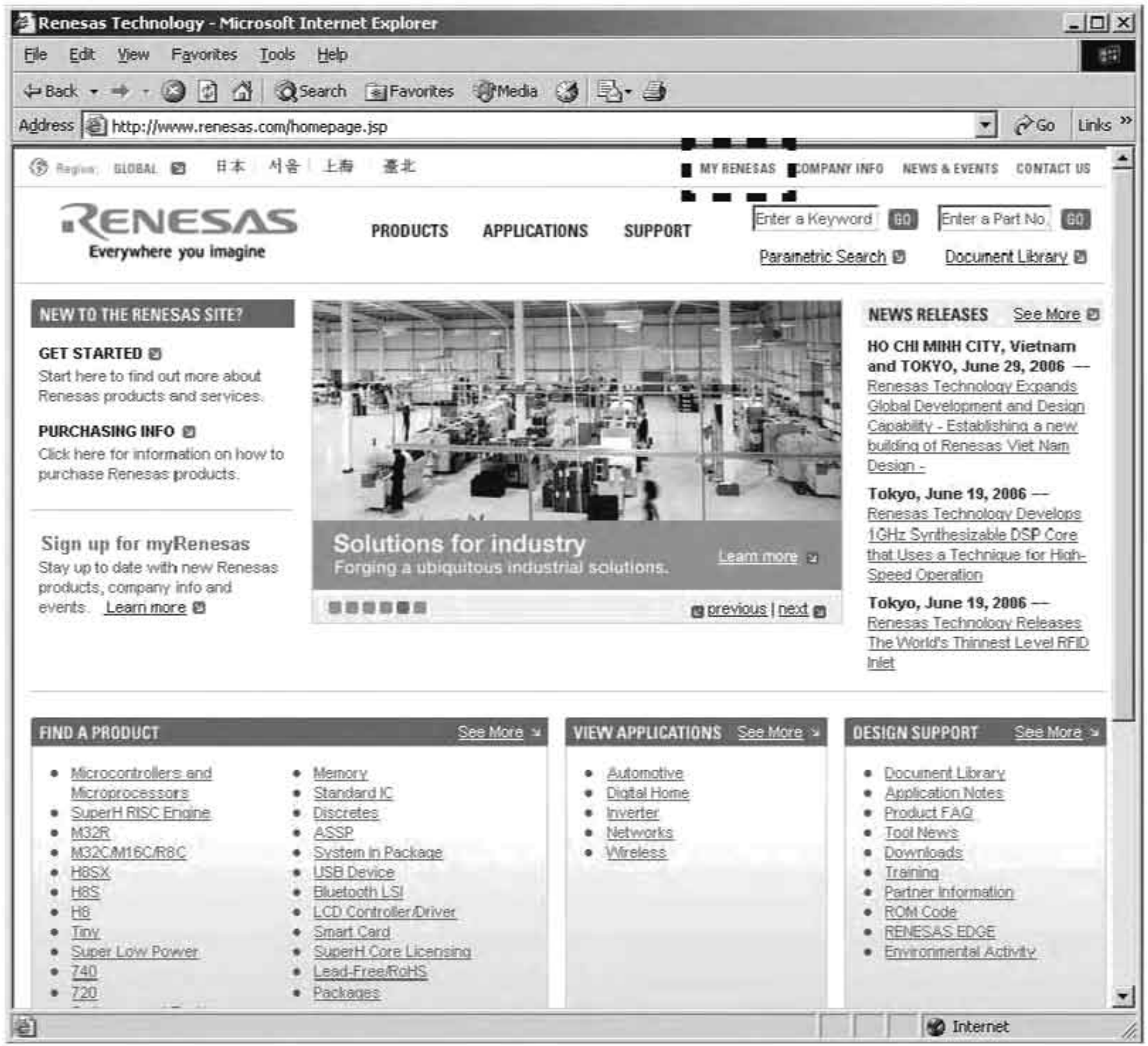
1. ブラウザ(インターネットエクスプローラーなど)を立ち上げます。
2. ブラウザのアドレスに"http://www.renesas.com/"を入力し、移動、またはキーボードの**Enter**を押します。

注意: このサイトはRENESASが管理しているため、以下の説明が実際のサイト構成と異なっている場合があります。その場合は実際のRENESASのサイト構成に沿って進めてください。

3. **GLOBAL SITE**をクリックします。

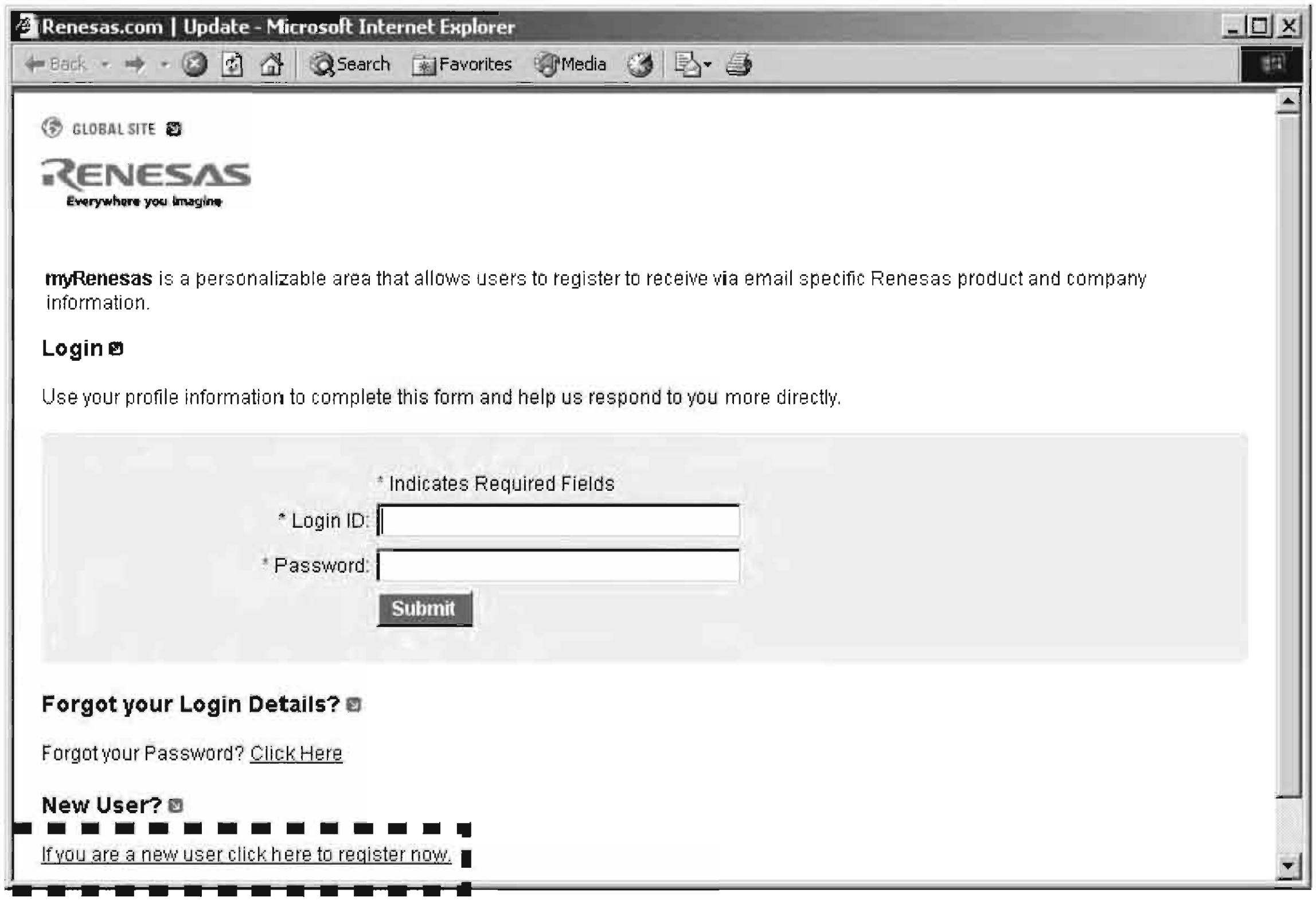
4. A login ID is necessary to download the FDT.
   If you have Login ID, please advance to step 15.
   If you do not have Login ID, Click the **MY RENESAS**.

4. FDTのダウンロードにはLogin IDが必要になります。
   既にLogin IDを持っている方は手順の15へ進んでください。
   Login IDを持っていない方は**MY RENESAS**をクリックします。



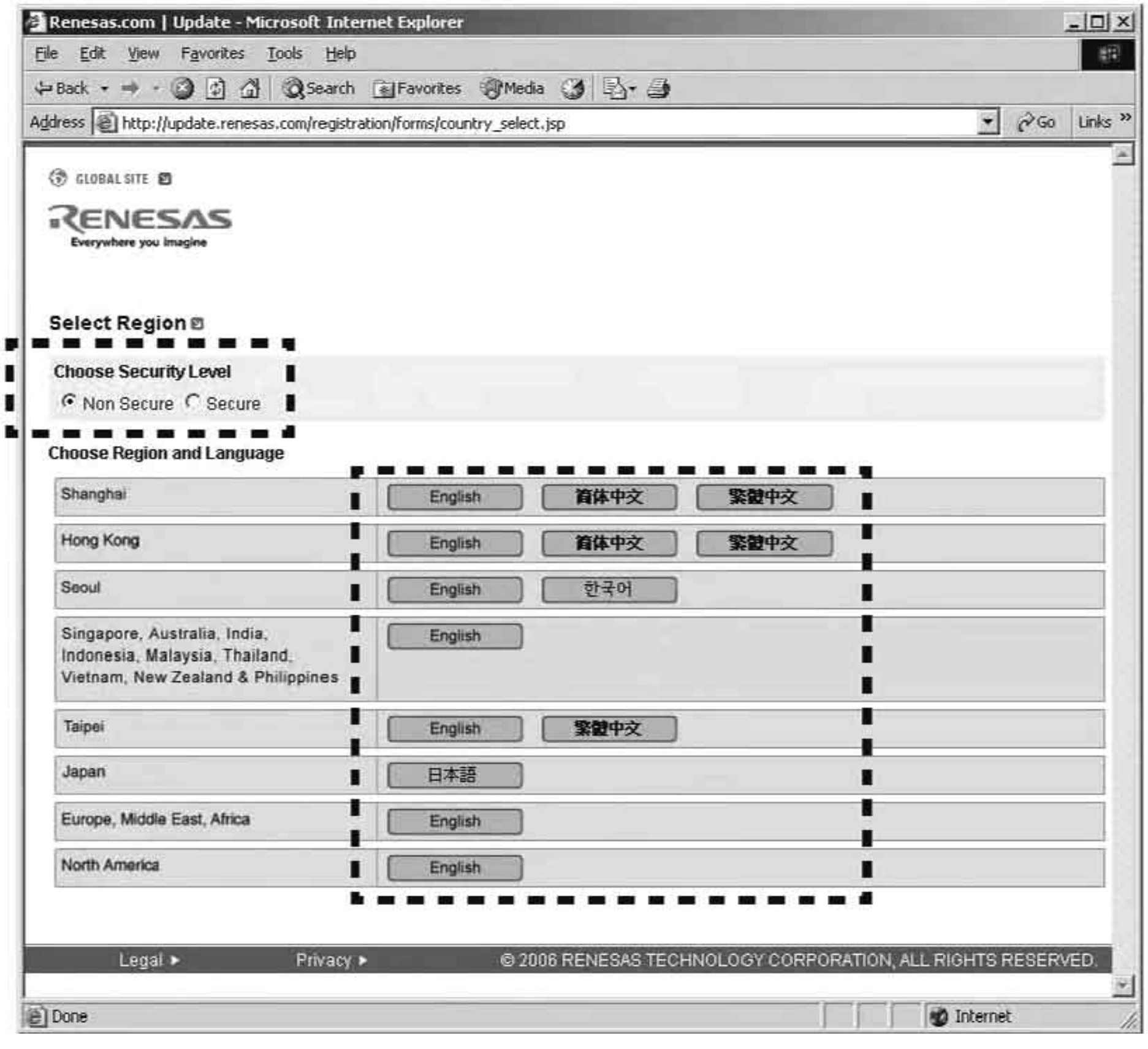
5. Click the If you are a new user click here to register now.

5. If you are a new user click here to register nowをクリックします。



6. Choose **Non Secure** or **Secure** in Security Level at your network environment.
Choose **English** or **another one** in Region and Language.

6. PCのネットワーク環境により**Choose Security Level**から **Non Secure**、または**Secure**を選んでください。
Choose Region and Languageから日本語をクリックします。

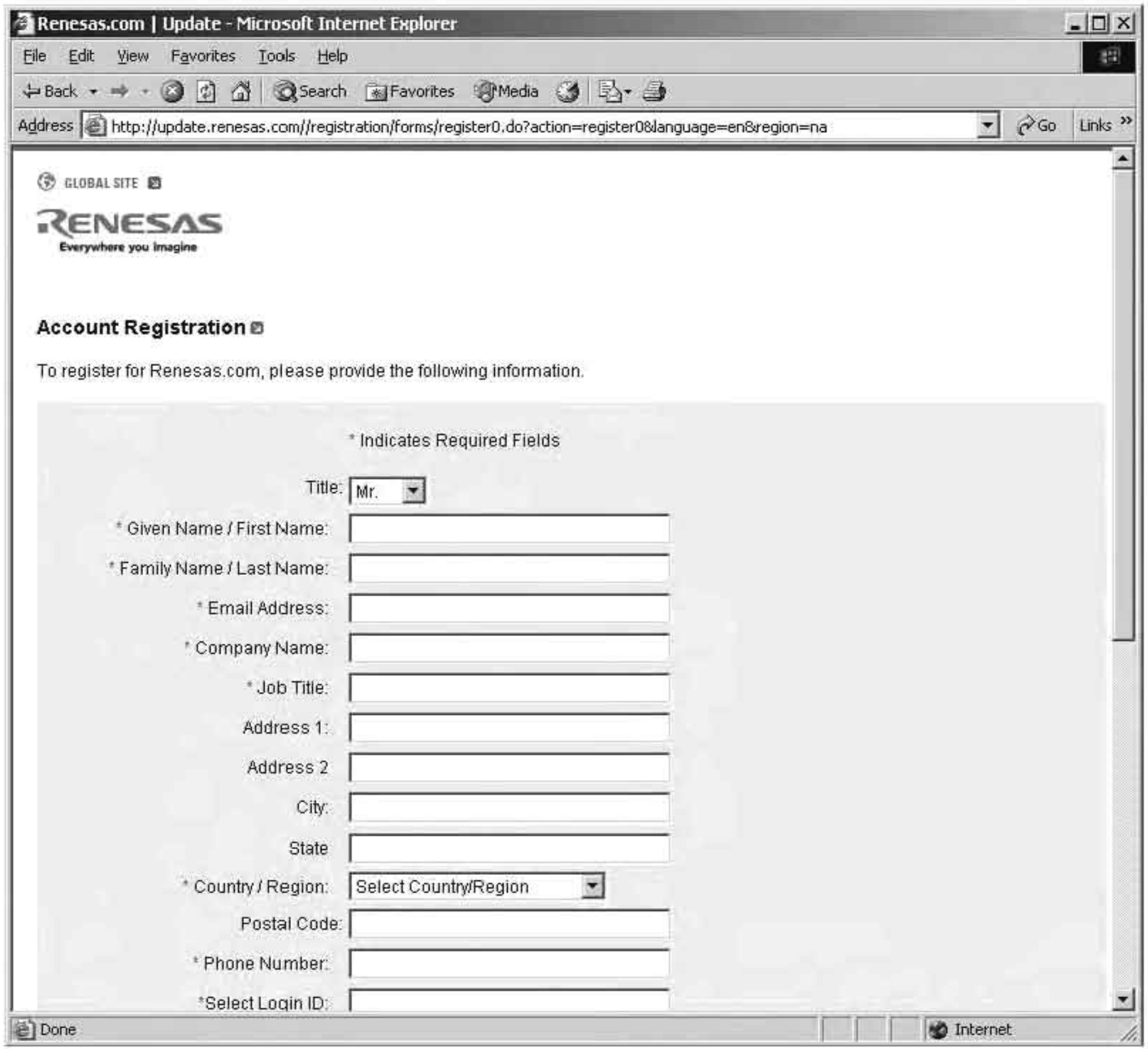


7. Input the each item.

NOTE : The items displayed by a language and region are different.

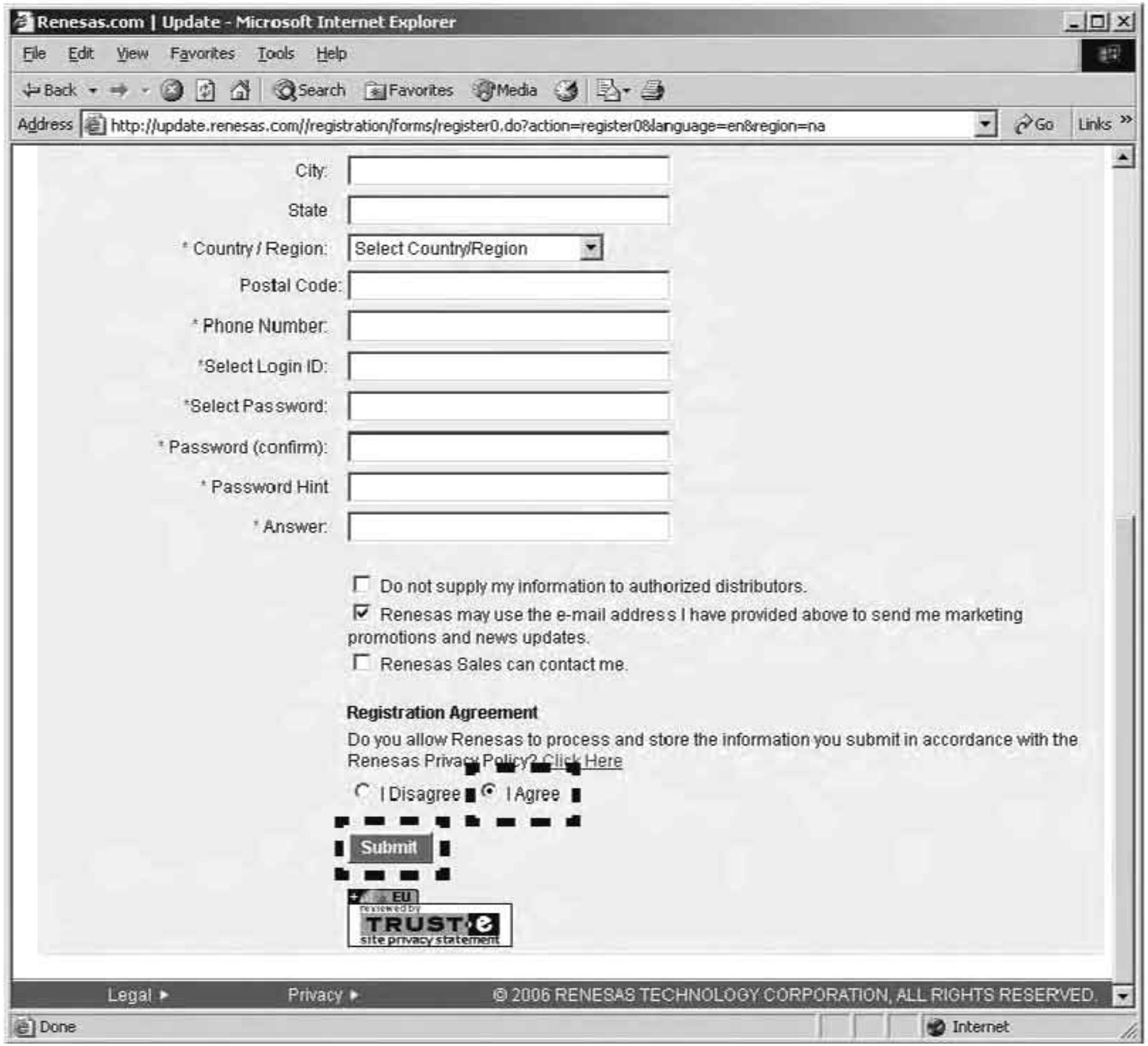
7. 各項目を記入します。

注意: 下記説明は英語ですが、日本語を選んだ場合日本語で表示されます。



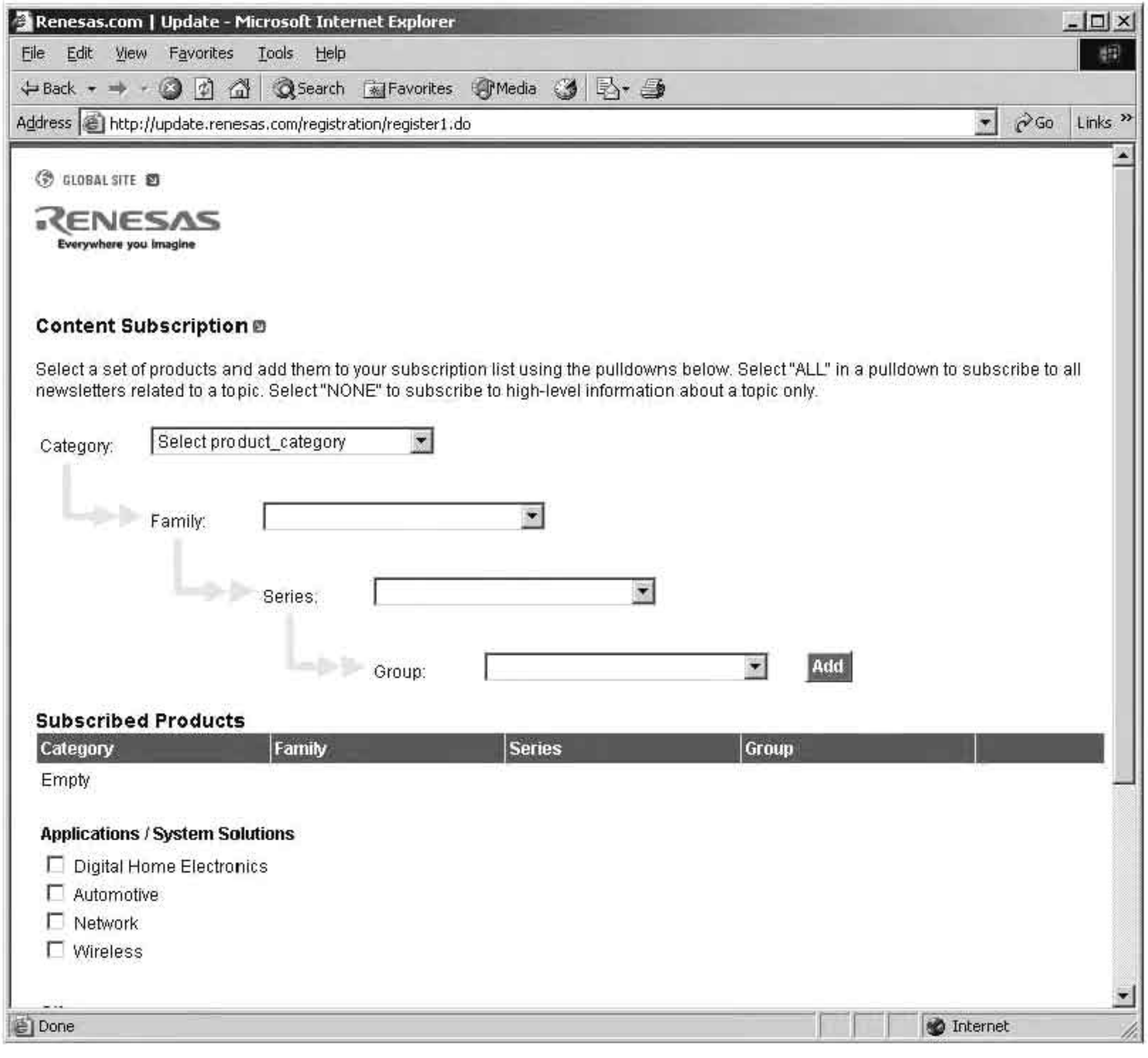
8. If you have inputted the necessary items, check the **I Agree**, and click the **Submit**.

8. 必須項目を入力したならば、同意しますにチェックを入れ、送信をクリックします。



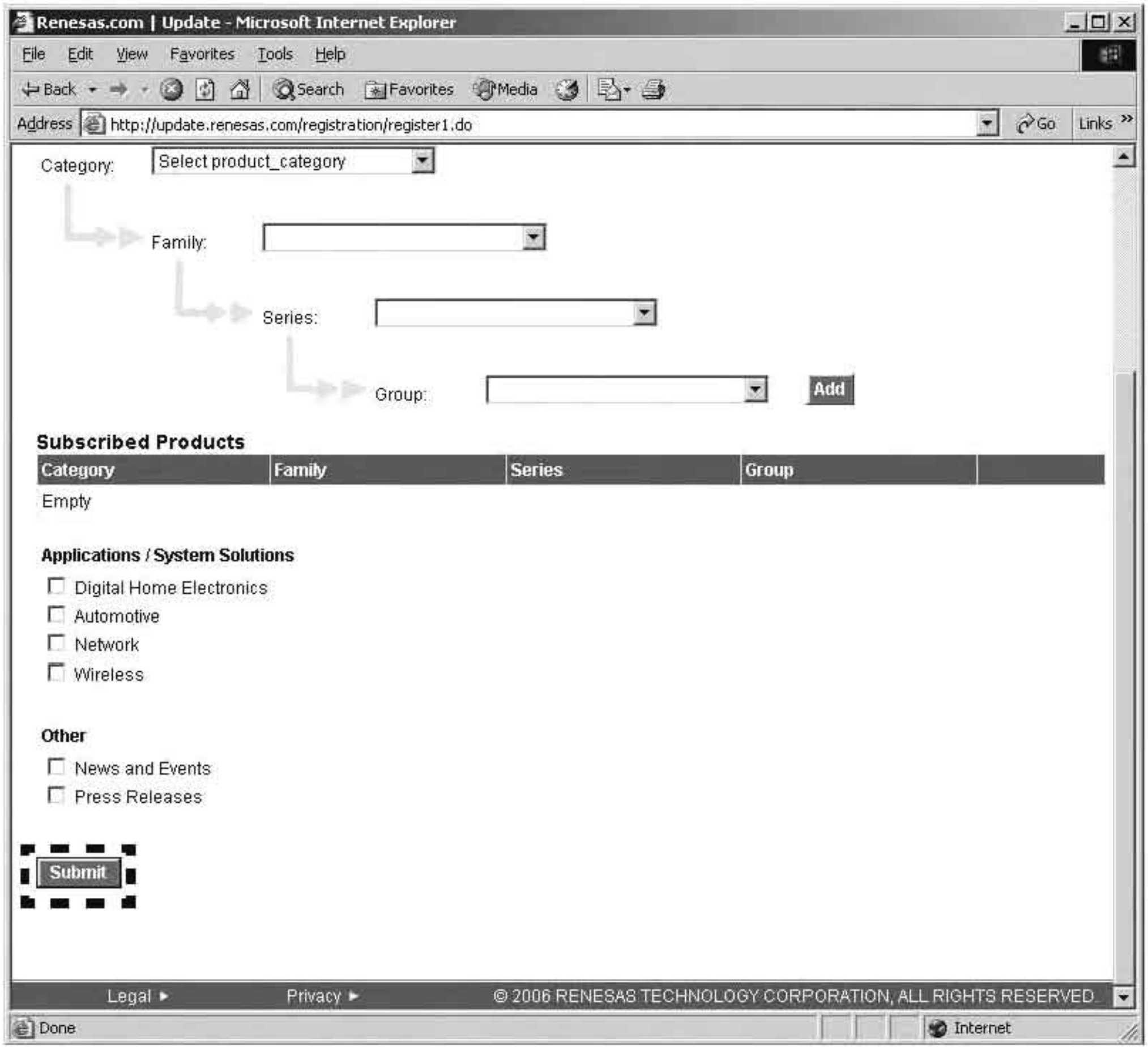
9. The input is needless in this page.
Scroll down the page.

9. このページは入力しなくても結構です。
ページをスクロールダウンします。



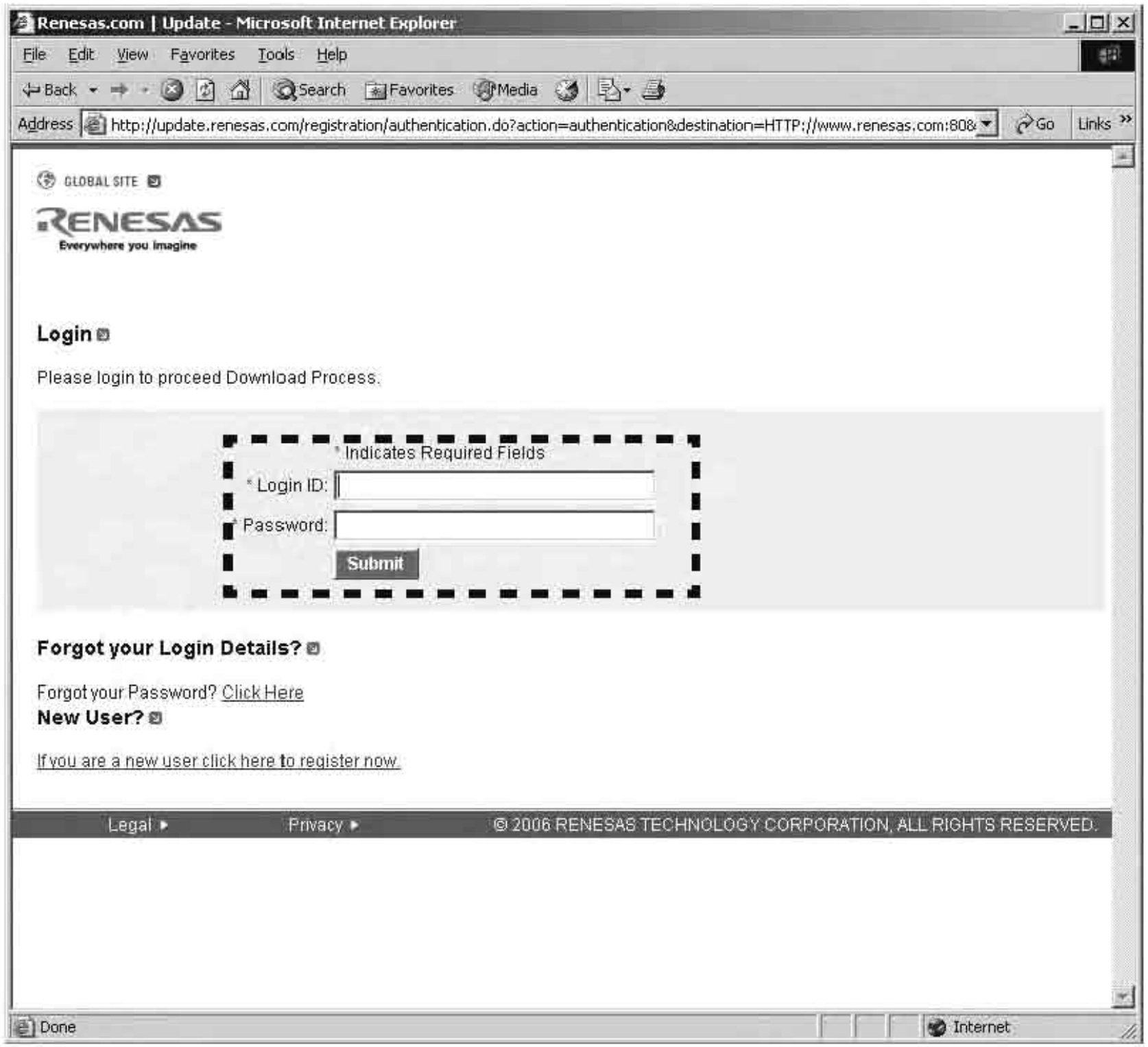
10. Click the **Submit**.

10. 送信をクリックします。



11. Immediately, an E-mail arrives from the RENESAS.
Click the link in the E-mail to go to the registration site, and input the Login ID and Password.
And Click the **Submit**.

11. 直ちに、RENESASからE-mailが届きます。
E-mail内に有る登録サイトへのリンクをクリックします。
Login IDとPasswordを入力し**Submit**をクリックします。



12. Registration is finished.
13. Open the RENESAS top page from registration page.

12. 登録が完了します。
13. 登録ページに有るリンクからRENESASのトップページに移動します。

14. Click the **GLOBAL SITE**.

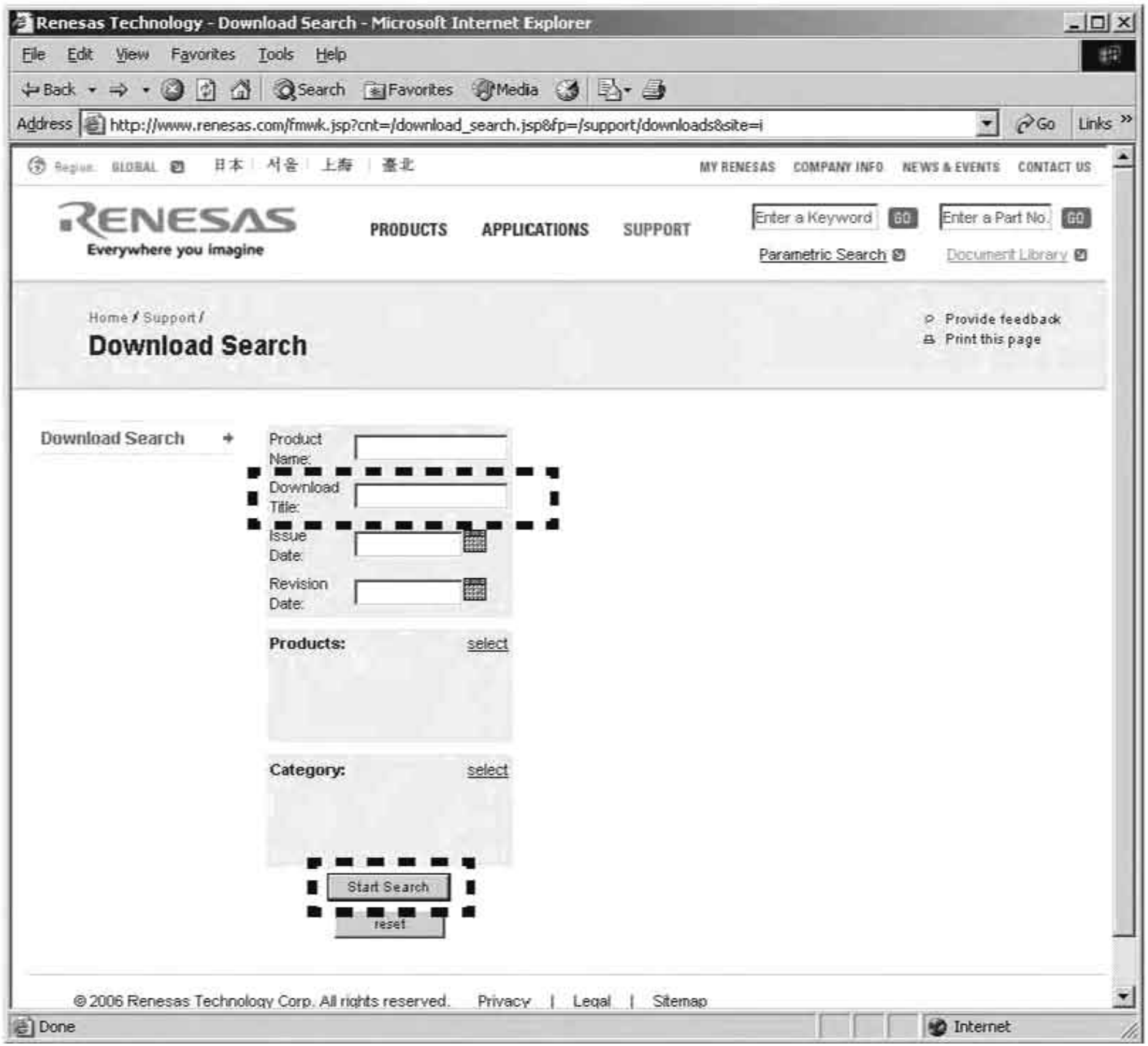
14. **GLOBAL SITE**をクリックします。

15. Click the **Downloads** in the DESIGN SUPPORT.

15. DESIGN SUPPORT内の**Downloads**をクリックします。

16. Type the "Flash Development toolkit" into the Download Title.
And click the **Start Search**.

16. Download Titleに"Flash Development toolkit"を入力します。
Start Searchをクリックします。

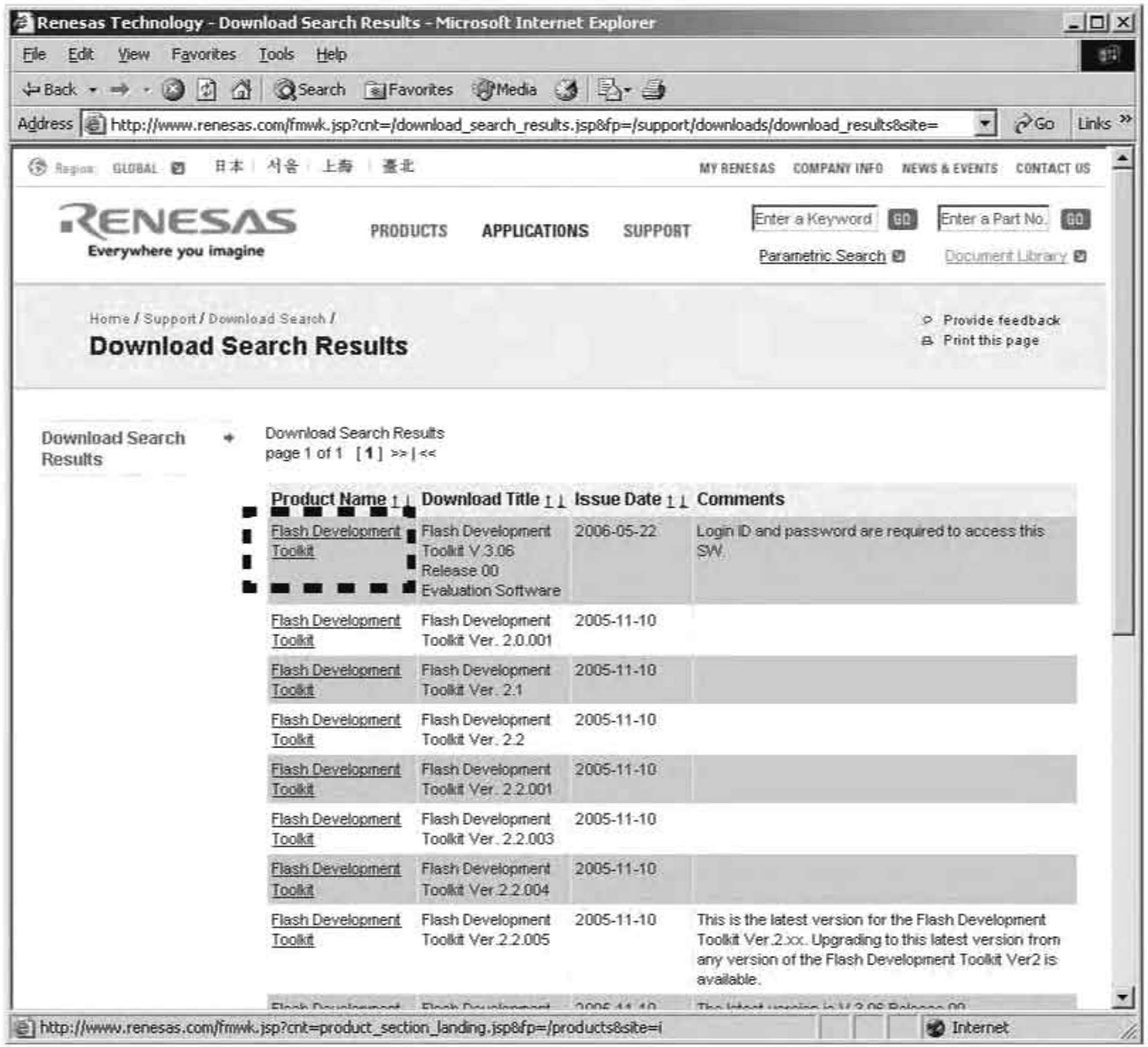


17. Click the **Flash Development Toolkit** of the top on the table.

NOTE : The latest edition is FDT V3.06 at present. (July, 2006) It is in FDT V3.06 as follows and explains it.

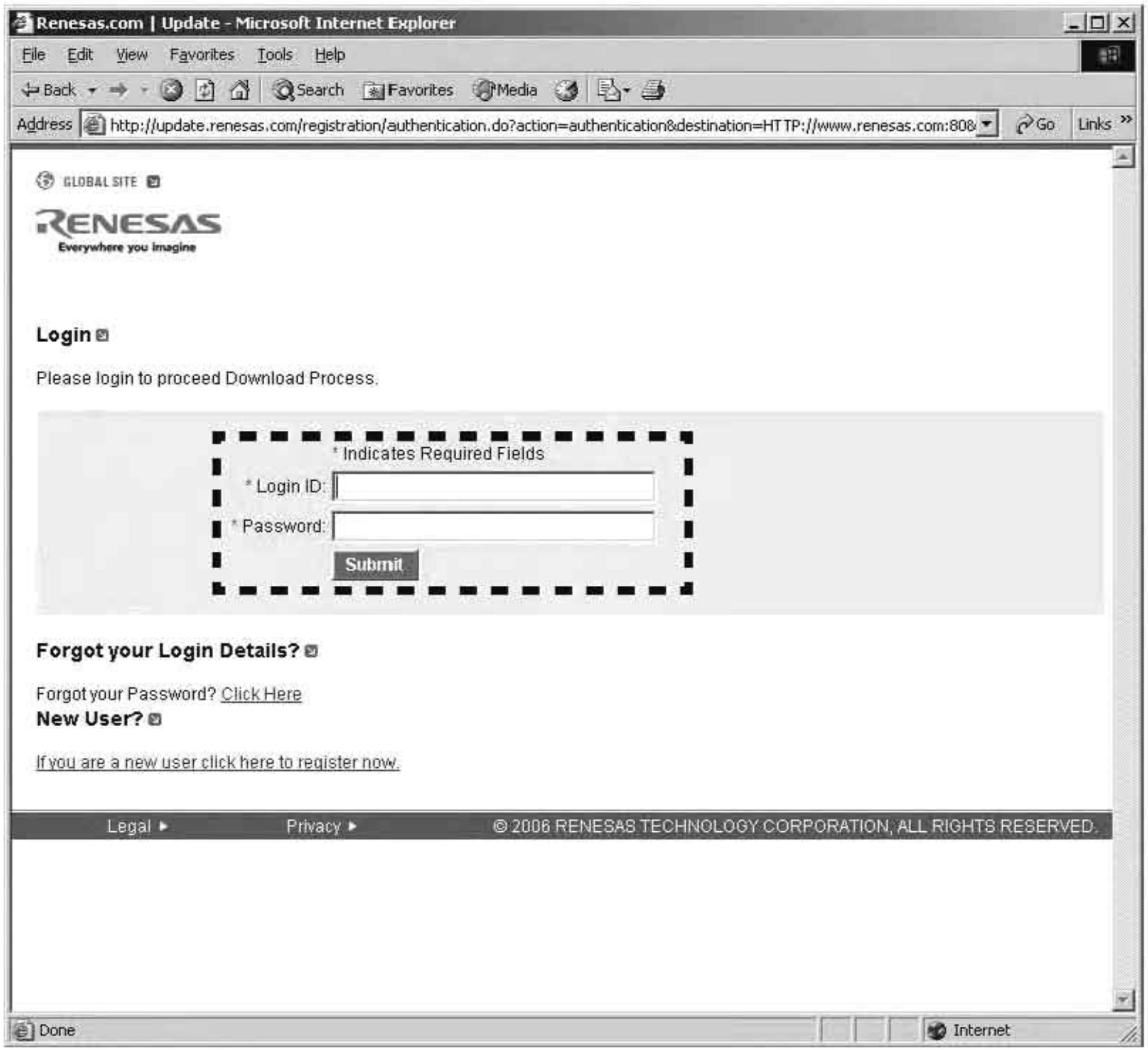
17. 検索結果の一番上の**Flash Development Toolkit**をクリックします。

注意: 現時点(2006年7月)での最新バージョンはV3.06になります。以下FDT V3.06で説明します。



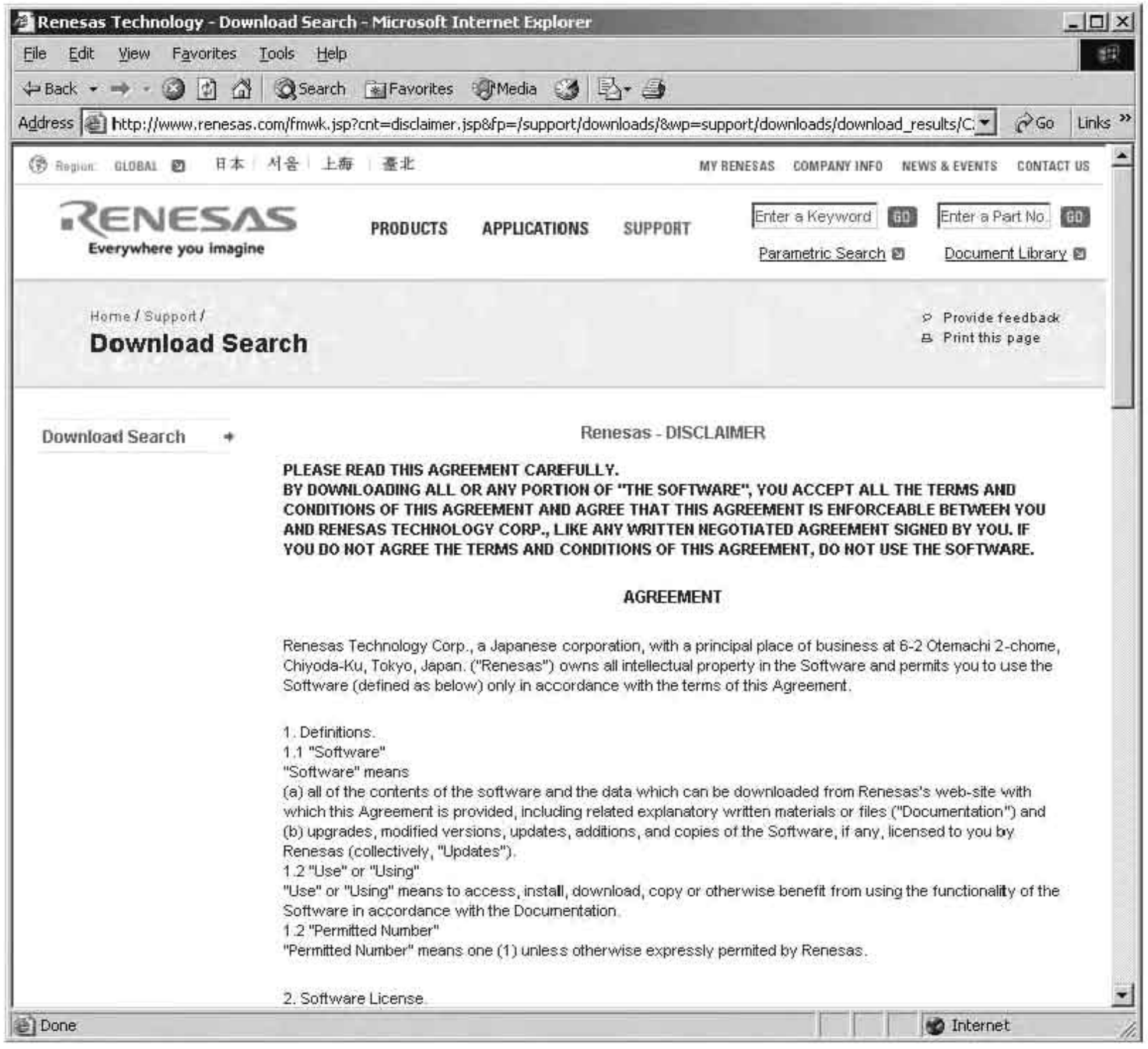
18. Input the Login ID and Password.
And click the **Submit**.

18. ダウンロードするためにLogin IDとPasswordを入力します。
Submit.をクリックします。



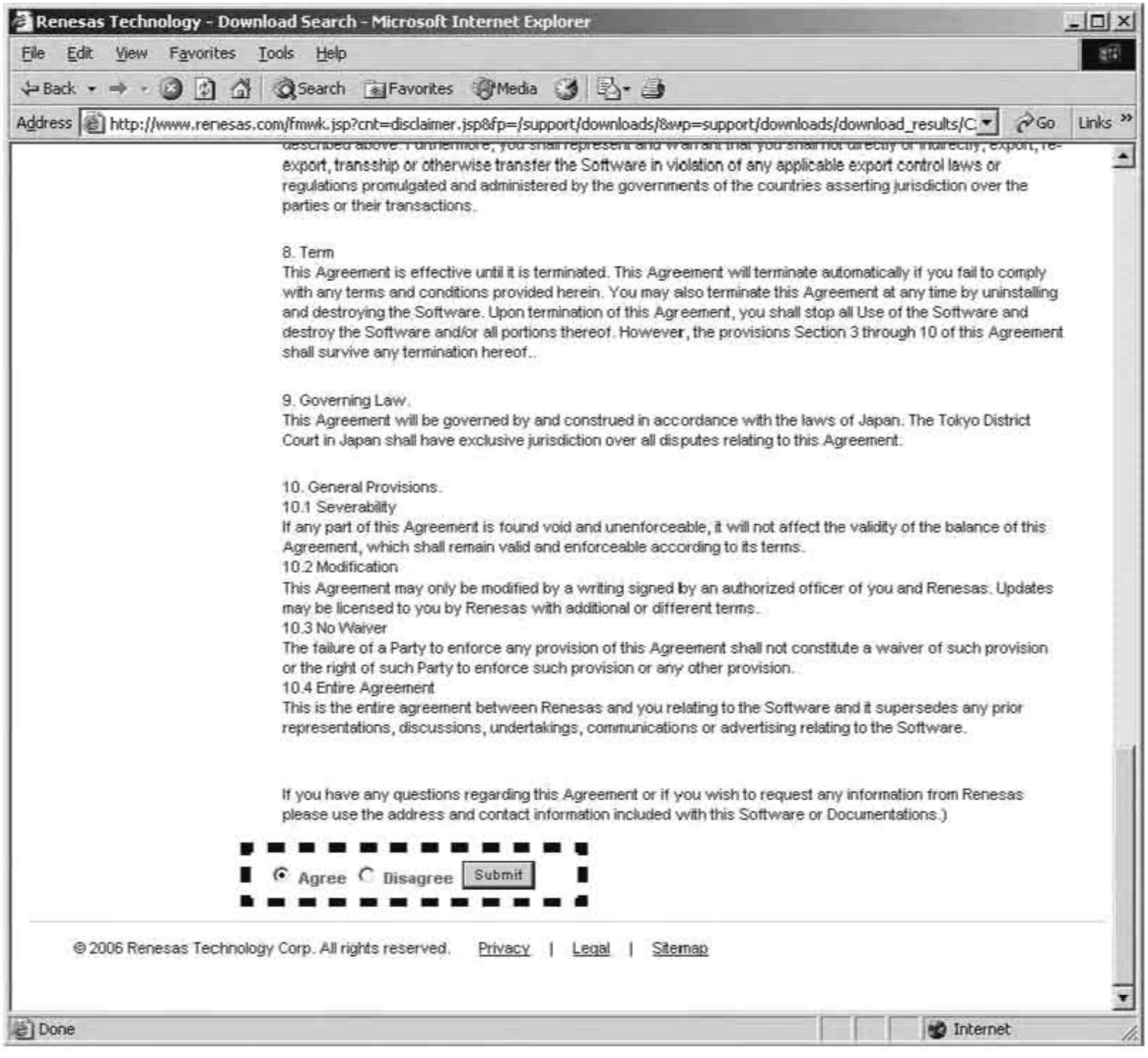
19. Scroll down the page.

19. ページをスクロールダウンします。



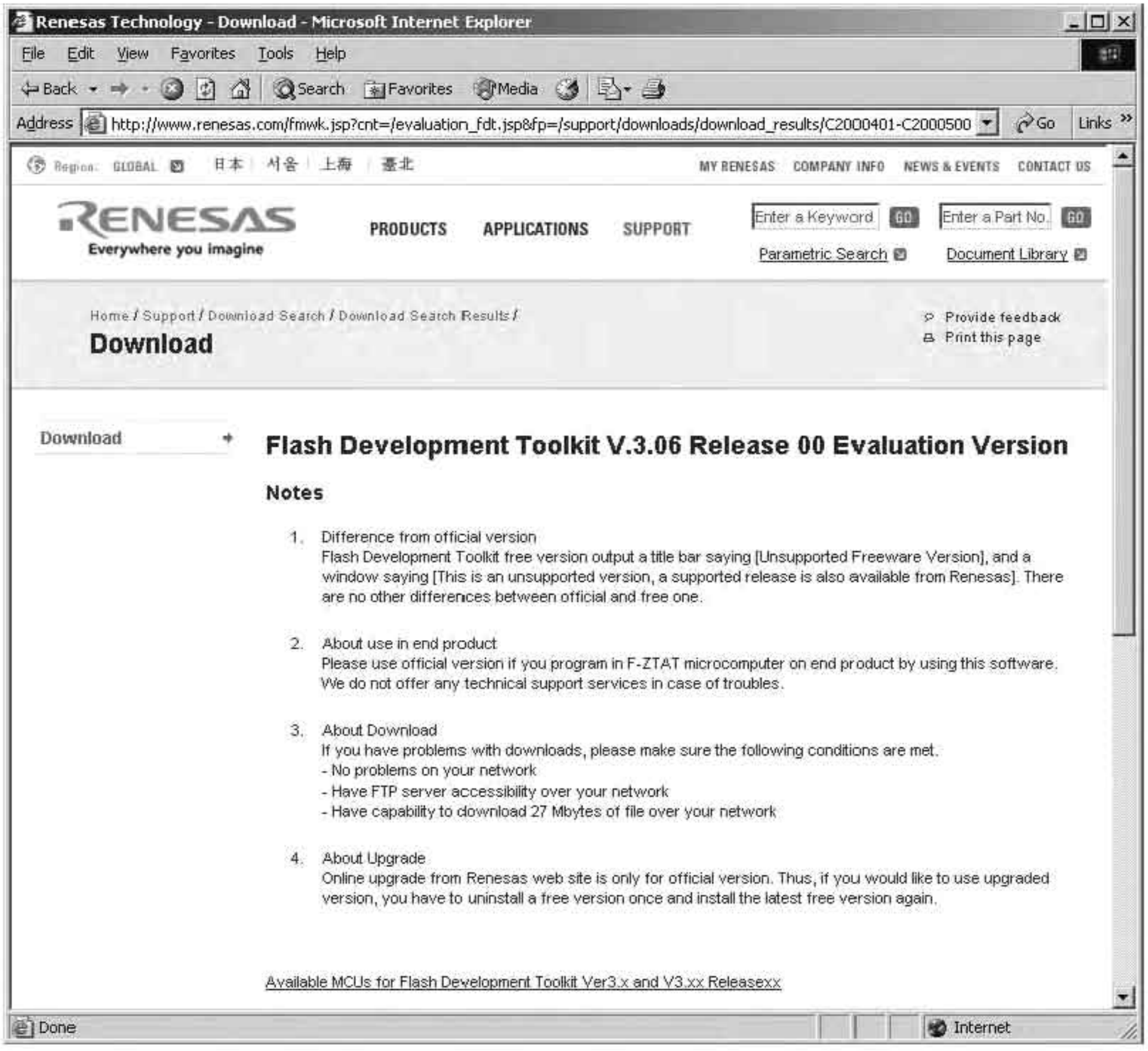
20. Check the **Agree**, and click the **Submit**.

20. **Agree**にチェックを入れ、**Submit**をクリックします。



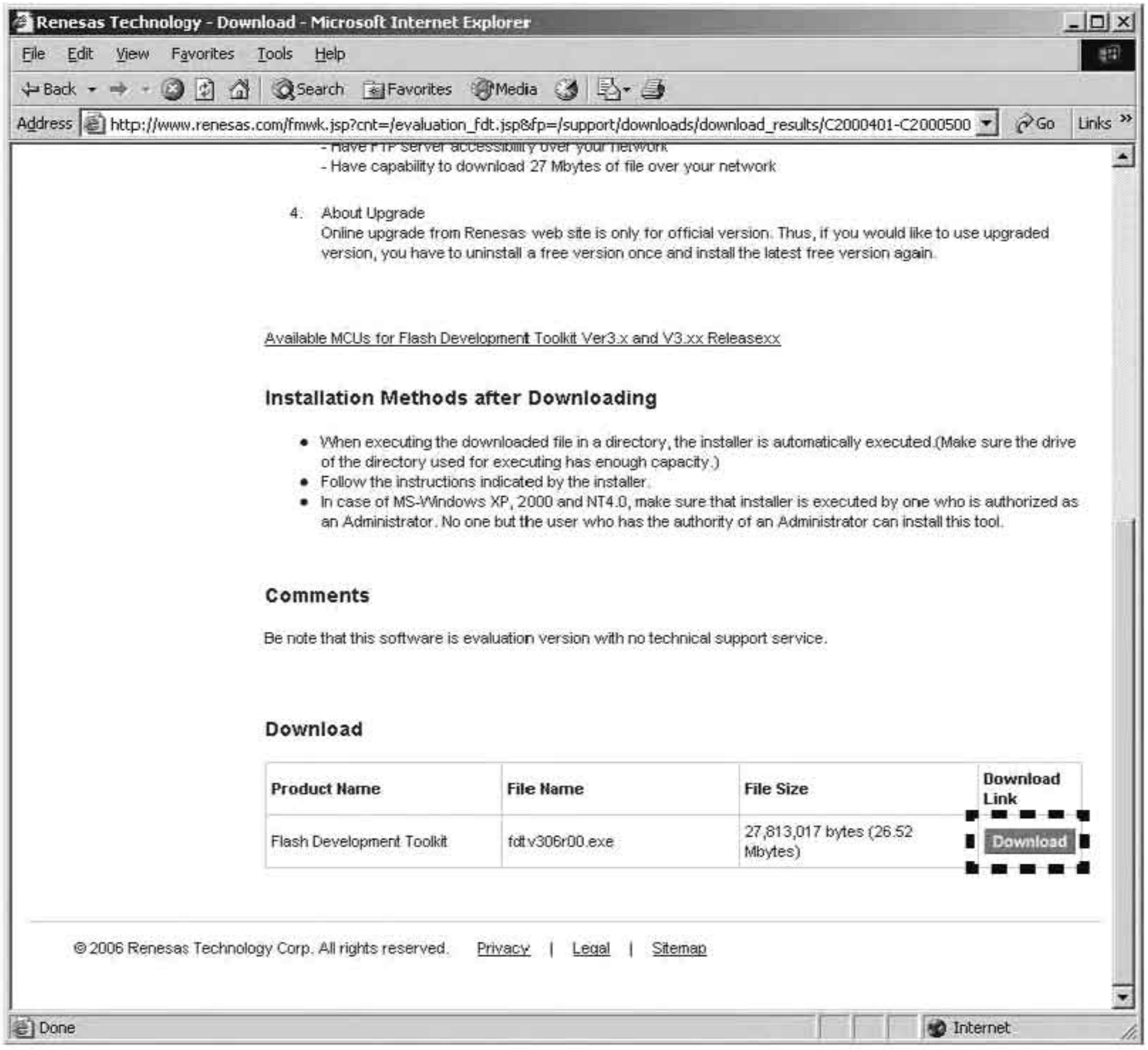
21. Scroll down the page.

21. ページをスクロールダウンします。



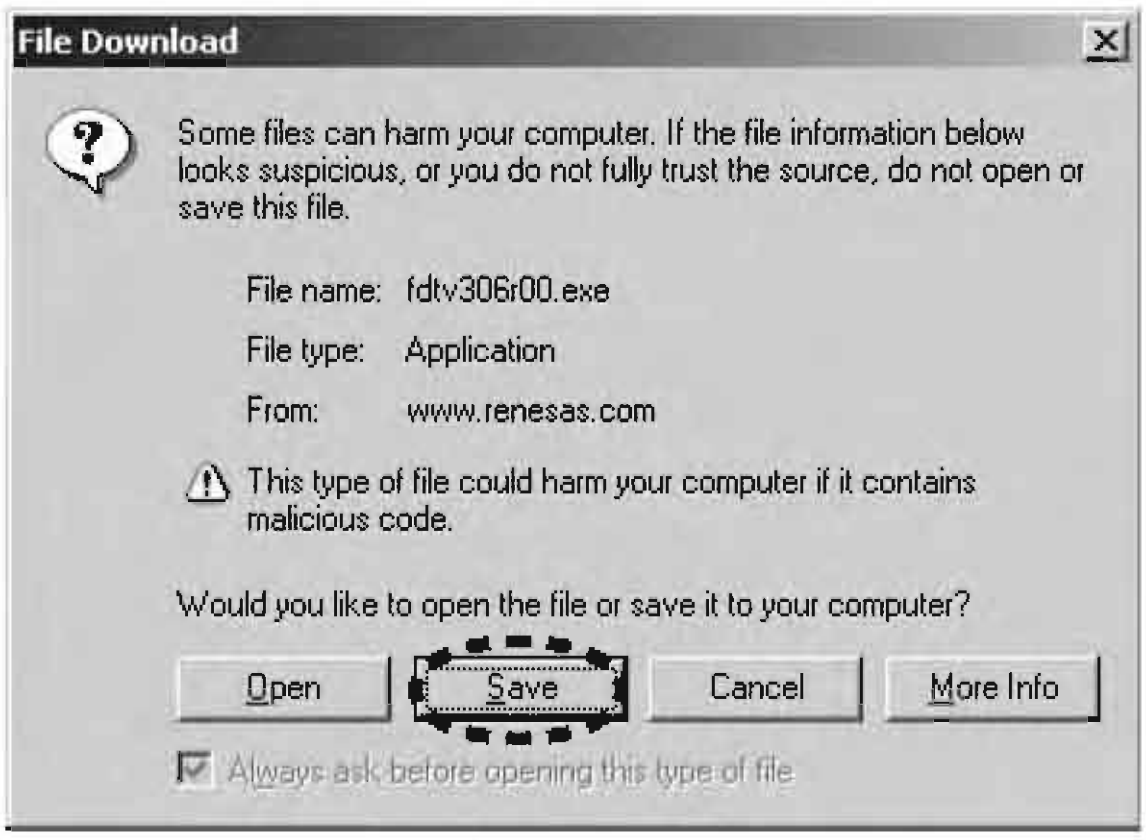
22. Click the **Download**.

22. **Download**をクリックします。



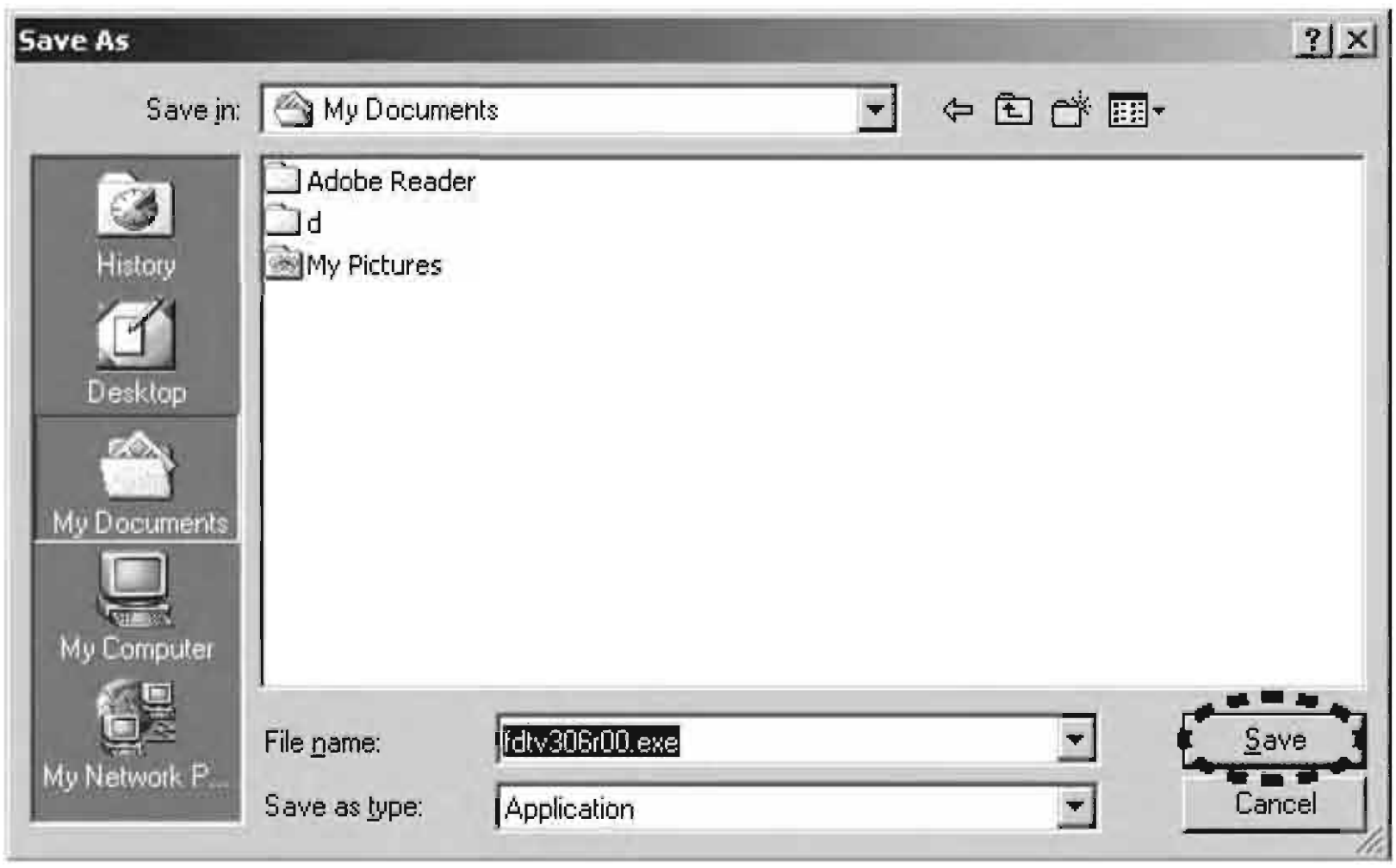
23. Click the **Save**.

23. **Save**をクリックします。



24. Save the fdtv306r00.exe on your PC's hard disc.
NOTE : A file name is change by improvement.

24. fdtv306r00.exeを任意のフォルダに保存します。
注意： ファイル名はバージョンにより変わります。

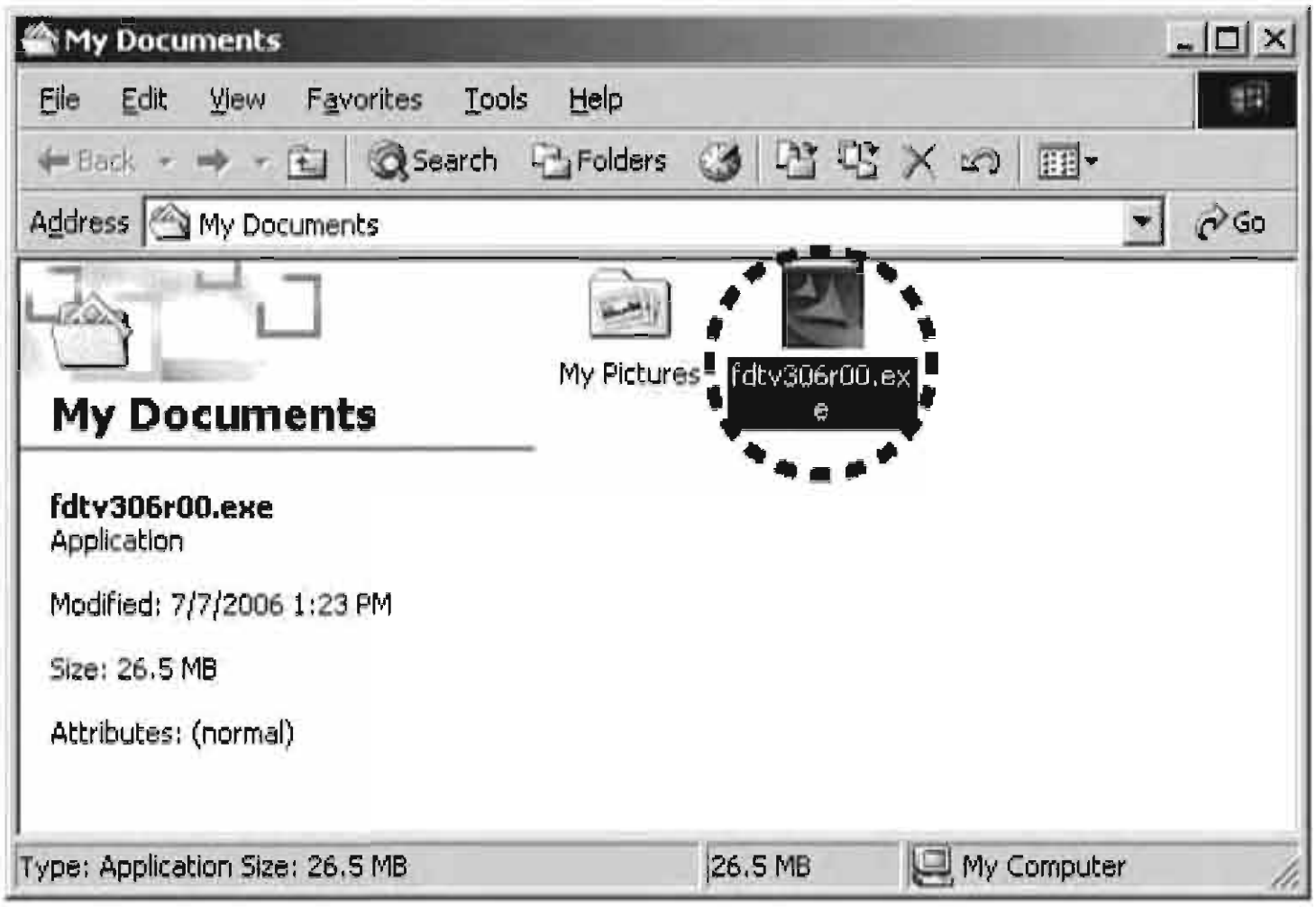


[A-2] INSTALLS OF THE SOFTWARE
(Flash Development Toolkit Ver.3.06)

1. Open the folder with the downloaded file.
2. And double click the **fdtv306r00.exe**.

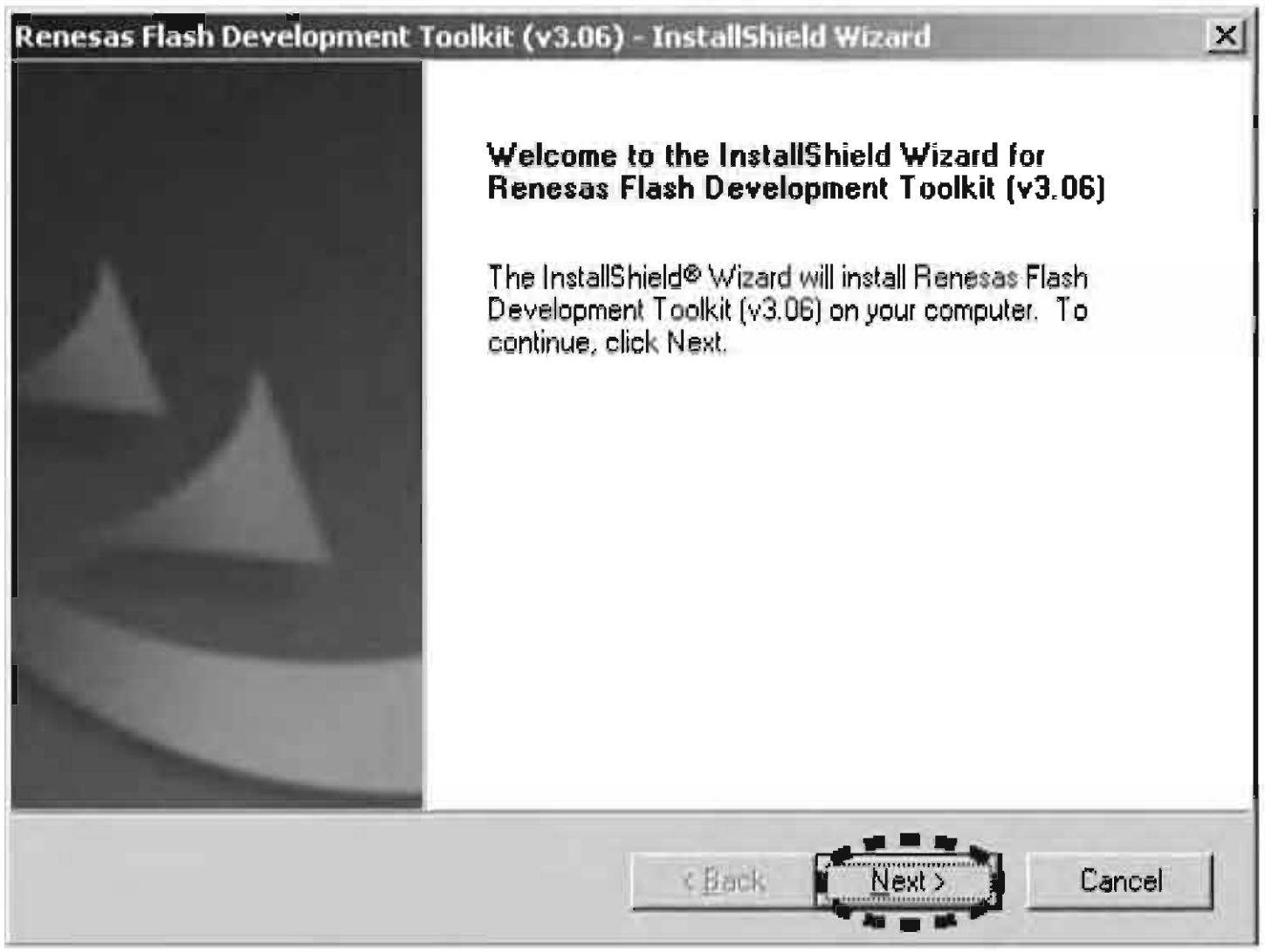
[A-2] INSTALLS OF THE SOFTWARE
(Flash Development Toolkit Ver.3.06)

1. ダウンロードしたファイルのあるフォルダを開きます。
2. **fdtv306r00.exe**をダブルクリックします。



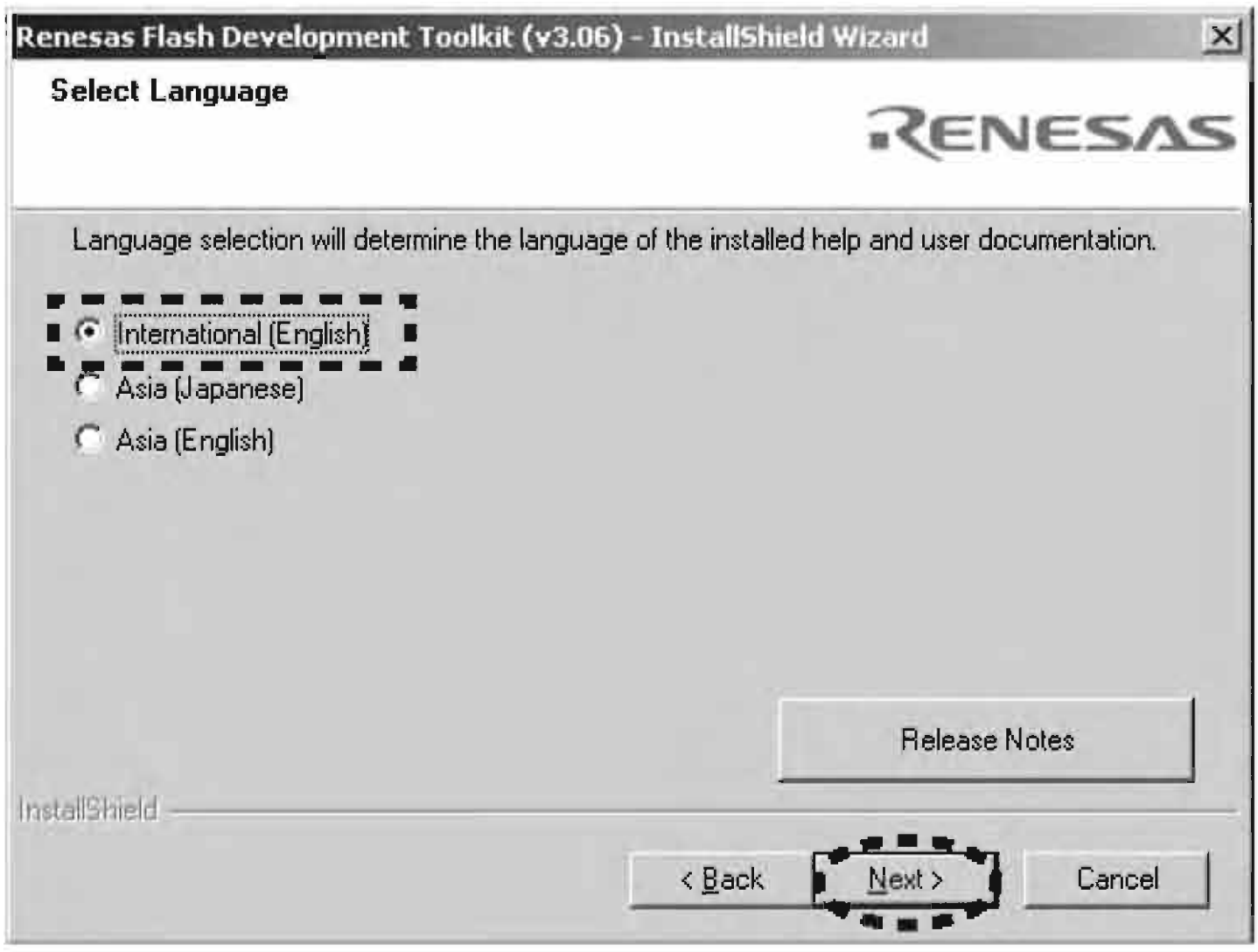
3. Click the **Next**.

3. **Next**をクリックします。



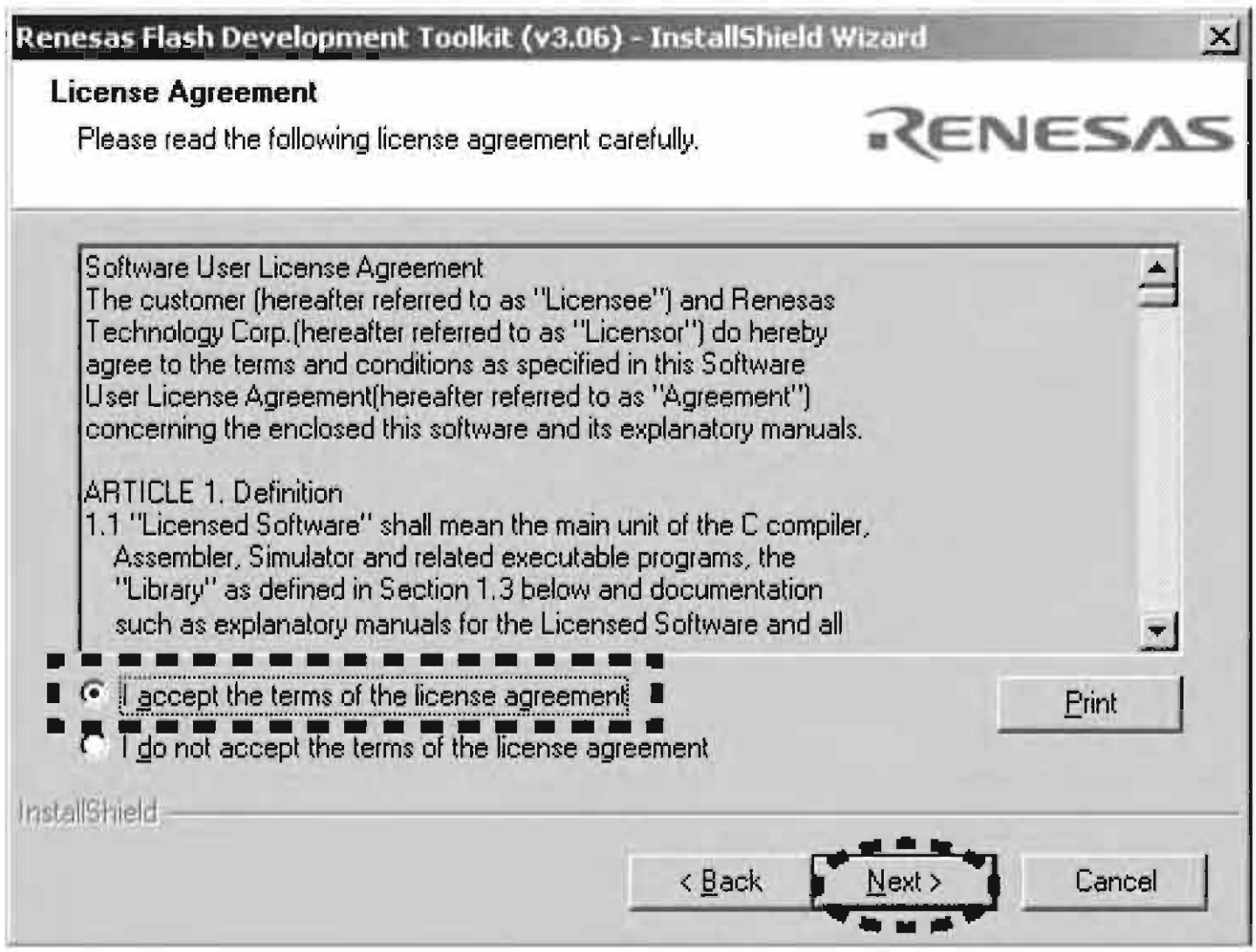
4. Check the **International [English]**, and click the **Next**.

4. **International [English]**にチェックを入れ**Next**をクリックします。



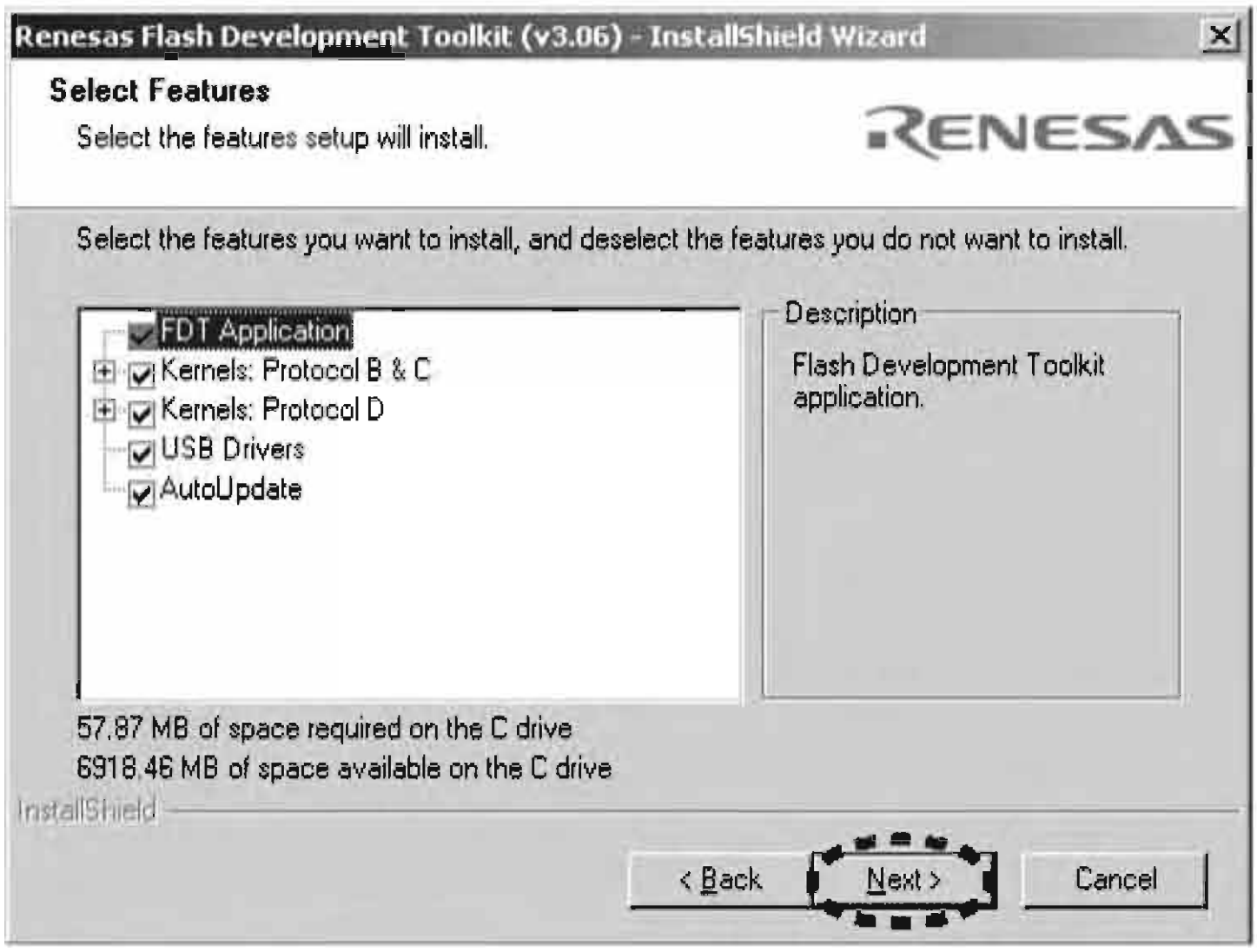
5. Check the **I accept the terms of the license agreement**, and Click the **Next**.

5. **I accept the terms of the license agreement**にチェックを入れ、**Next**をクリックします。



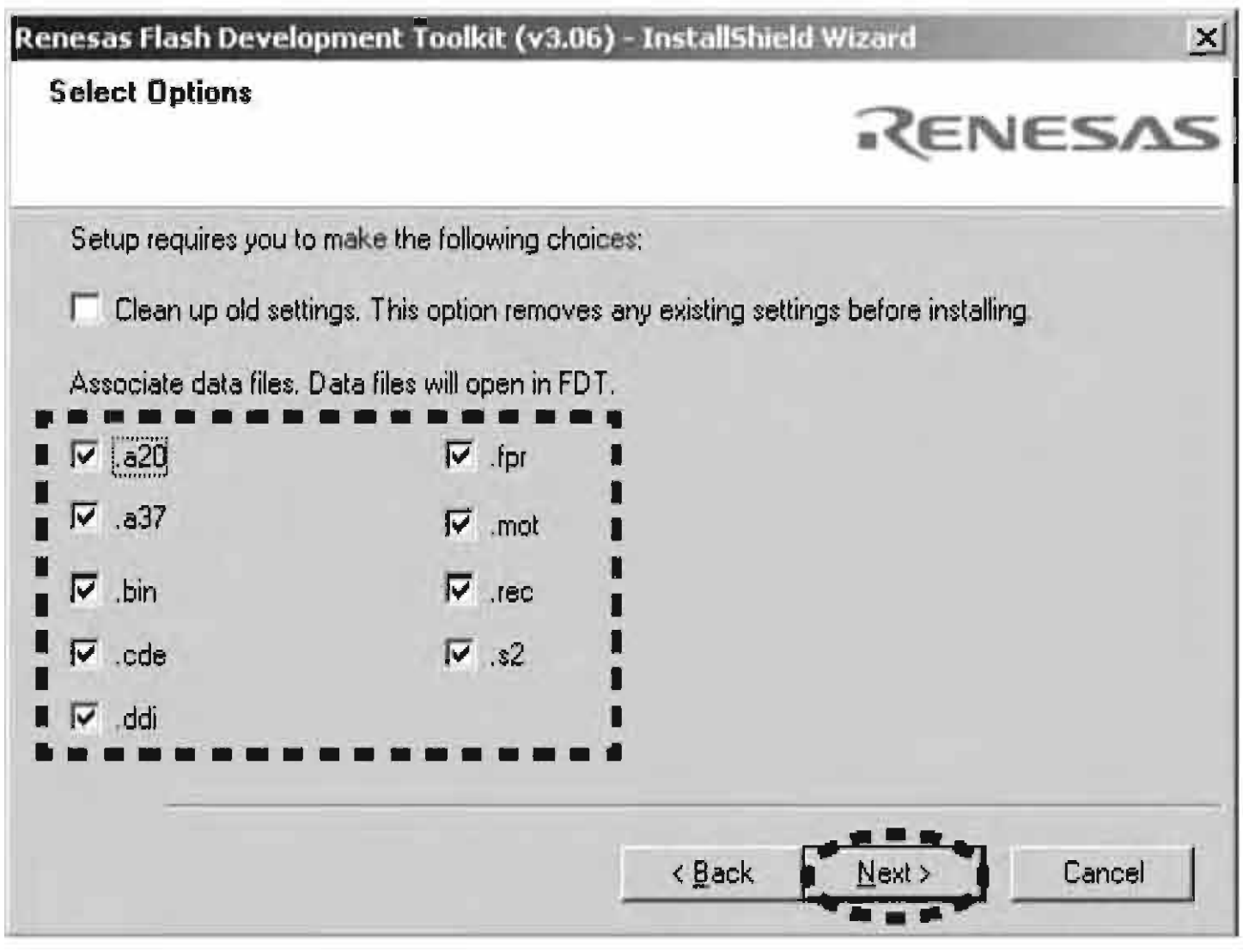
6 Click the **Next**.

6. **Next**をクリックします。



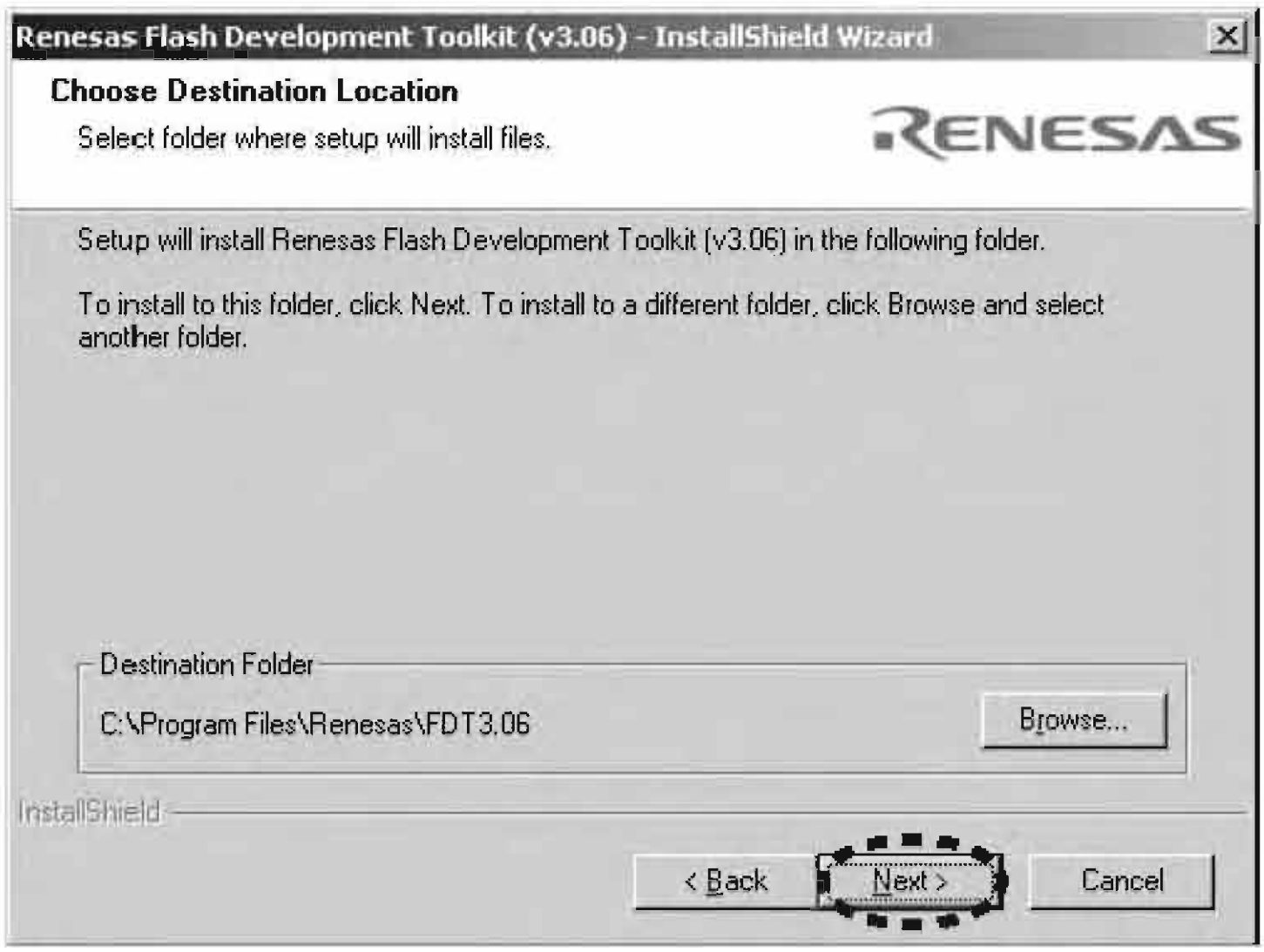
7. Check the all file type, and Click the **Next**.

7. 全てのファイルタイプにチェックを入れ、**Next**をクリックします。



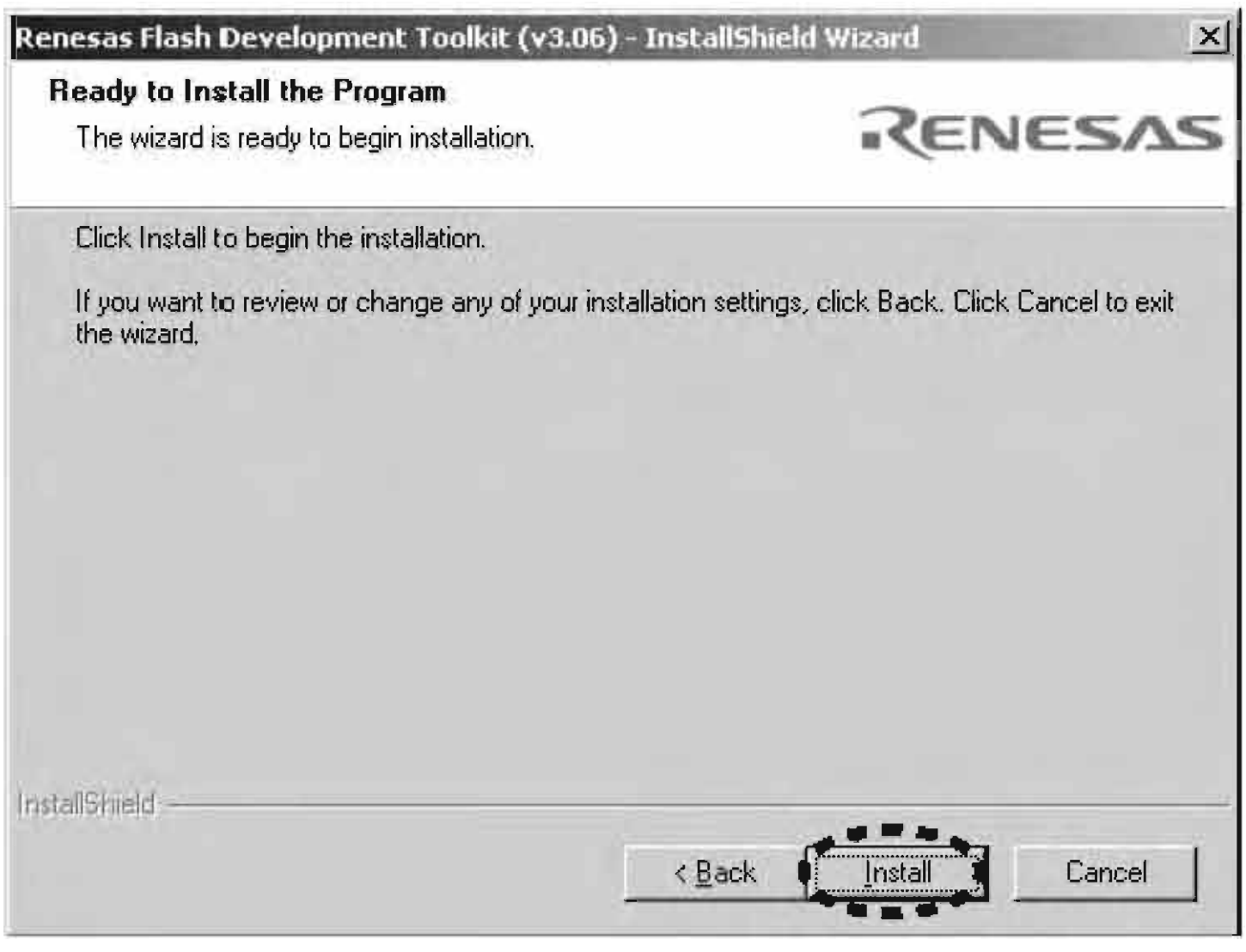
8. Click the **Next**.

8. **Next**をクリックします。



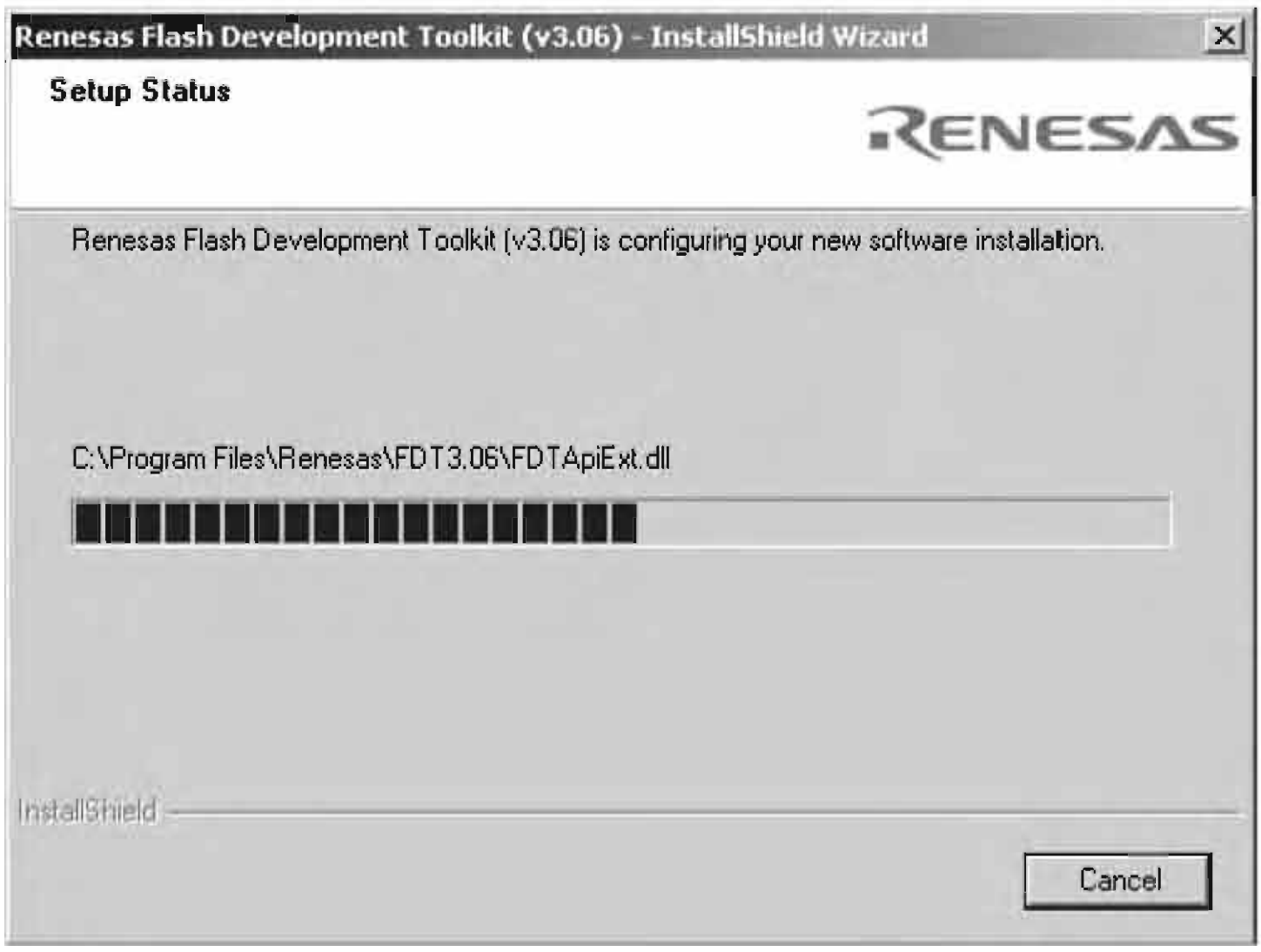
9. Click the **Install**.

9. **Install**をクリックします。



10. The Setup Status bar appears.

10. インストールの状態が表示されます。

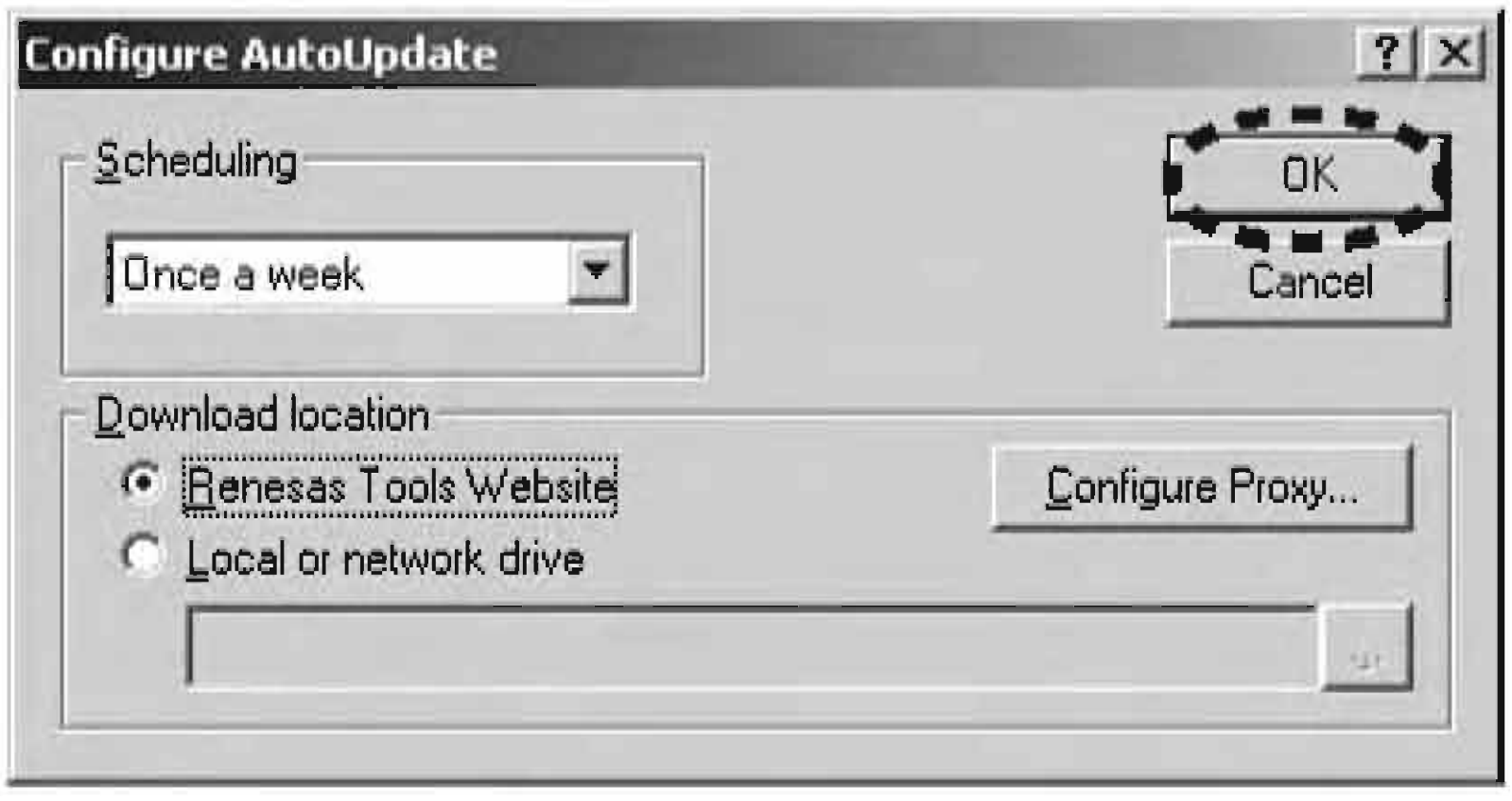


11. Click the **Finish**.

11. **Finish**をクリックします。

12. Click the **OK**.

12. **OK**をクリックします。



[B] WRITING AND UPDATE SOFTWARE

Software for MAIN CPU, flash ROM for DSP and HDMI CPU can be updated/downloaded.

Have update/download application software. ("H8Download.exe", "da708_writer.exe" and "fdtv306r00.exe (FDT3.06) or latest version")

There are three mode of download, regarding to the target of software as bellow.

Mode 1: Update/Download MAIN CPU's software to internal Flash-ROM.

This mode is to update/download the software for MAIN CPU.
The target devise is internal flash ROM of CPU (IC17) on CUP11872Z (DSP PWB).
The unit needs to be set to writing condition, by pushing internal switch from rear panel.
The updating of software takes about 2 minutes and 30 seconds.

Mode 2: Update/Download DSP's software to 8M Flash-ROM.

This mode is to update/download the software for DSP.
The target devise is 8M Flash-ROM (IC34) on CUP11872Z (DSP PWB).
The unit needs to be set writing condition, by three front buttons.
The updating of software takes about 2 minutes.

Mode 3: Update/Download HDMI CPU's software to internal Flash-ROM.

This mode is to update/download the software for HDMI CPU.
The target devise is internal flash ROM of CPU (IC90) on CUP11875Z (HDMI PWB).
The unit needs to be set writing condition, by three front buttons.
The updating of software takes about 45 seconds.

NECESSARY EQUIPMENT

The following items are required for updating/downloading.

Windows PC (OS: Windows2000 or WindowsXP) with Serial port.
RS-232C Dsub-9 pin cable (female to female/straight type)
Update software to MAIN CPU. (H8Download.exe, etc... in MAIN folder)
Update software to flash ROM for DSP. (da708_writer.exe, etc... in DSP folder)
Update software to HDMI CPU. (Writing data in HDMI folder)
Flash Development Toolkit 3.06 or latest version (fdtv306r00.exe or latest version)

Use RS232C Dsub-9 pin cable (female to female/straight type) to connect PC and the RS-232C port in rear panel of the unit, when updating/downloading MAIN CPU DSP and HDMI CPU.

[B] WRITING AND UPDATE SOFTWARE

MAINマイコン、**DSP**のフラッシュ**ROM**、および**HDMI**マイコンのソフトウェアは更新、および書き込みが出来ます。
更新および書き込みには書き込み用アプリケーションが必要です。("H8Download.exe"、“da708_writer.exe“、"fdtv306r00.exe (FDT3.06)または最新版")

書き込みには下記の3つのモードがあります。

Mode 1: Update/Download MAIN CPU's software to internal Flash-ROM.

このモードはMAINマイコンの更新および書き込み用です。
基板CUP11872Z (DSP PWB)のIC17のマイコン内部のフラッシュROMに書き込みます。
本機のリアパネルから内部スイッチを押し、書き込みモードにする必要があります。
書き込みにかかる時間は約2分30秒です。

Mode 2: Update/Download DSP's software to 8M Flash-ROM.

このモードはDSPのフラッシュROMの更新および書き込み用です。
基板CUP11872Z (DSP PWB)のIC34のフラッシュROMに書き込みます。
本機のフロントボタン3つから書き込みモードにする必要があります。
書き込みにかかる時間は約2分です。

Mode 3: Update/Download HDMI CPU's software to internal Flash-ROM.

このモードはHDMIマイコンの更新および書き込み用です。
基板CUP11875Z (HDMI PWB)のIC90のマイコン内部のフラッシュROMに書き込みます。
本機のフロントボタン3つから書き込みモードにする必要があります。
書き込みにかかる時間は約45秒です。

必要機器

下記は更新および書き込みに必要な機器です。

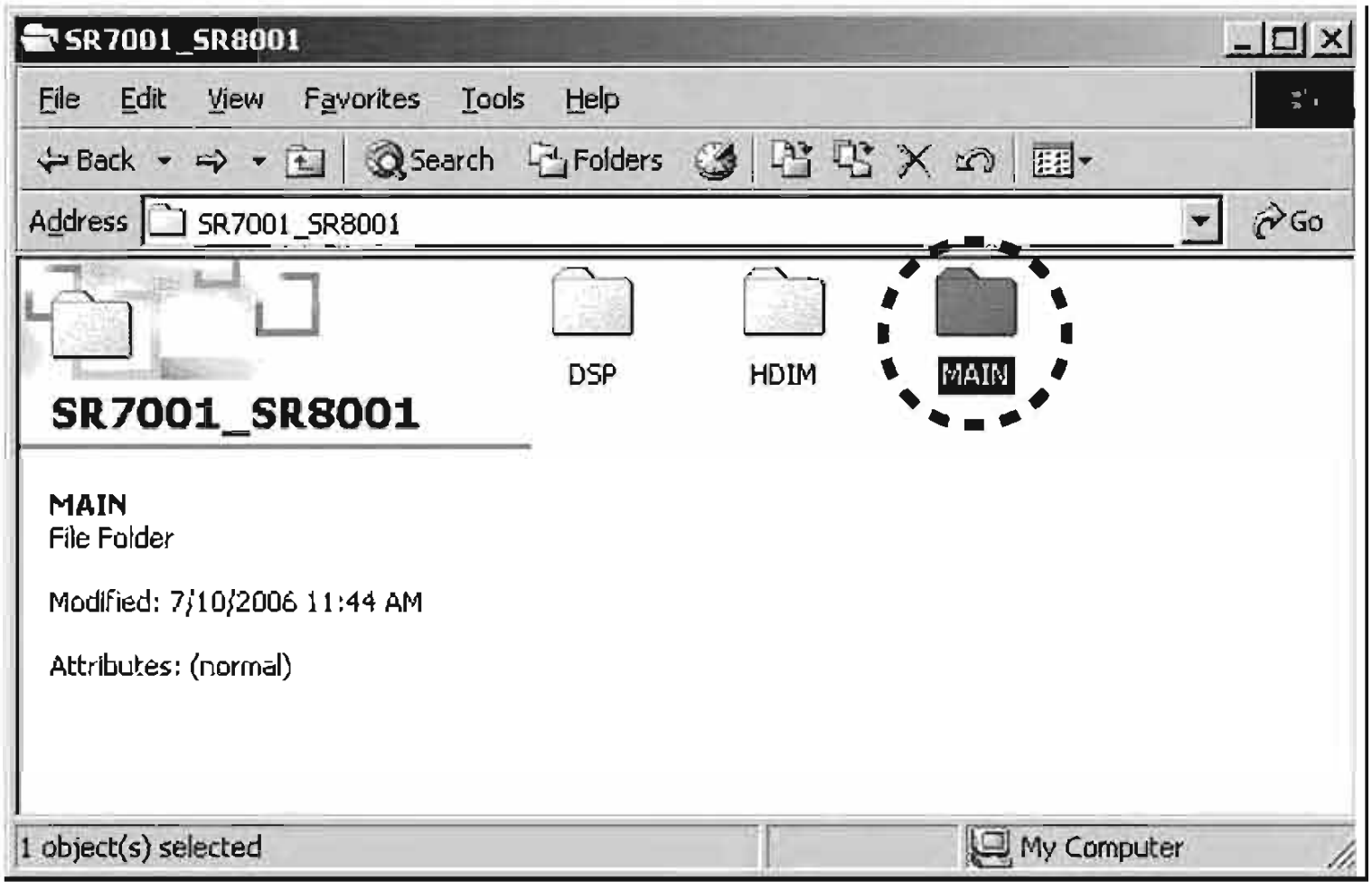
Windows PC (OS : Windows2000 またはWindowsXP) で Serial ポートのあるもの
RS-232C ストレートケーブル(9Pin メス-9Pin メス)
MAINマイコン用書き込みソフトウェア(MAINフォルダ内H8Download.exe、など)
DSPフラッシュROM用書き込みソフトウェア(DSPフォルダ内da708_writer.exe、など)
HDMIマイコン用書き込みソフトウェア(HDMIフォルダ内書き込み用データ)
Flash Development Toolkit 3.06または最新版 (fdtv306r00.exeまたは最新版)

MAINマイコン、DSPフラッシュROM、HDMIマイコンのソフトウェアを更新および書き込みする場合、RS-232Cケーブルで本機リアパネルのRS232Cコネクタと Windows PCのSerialポートを接続します。

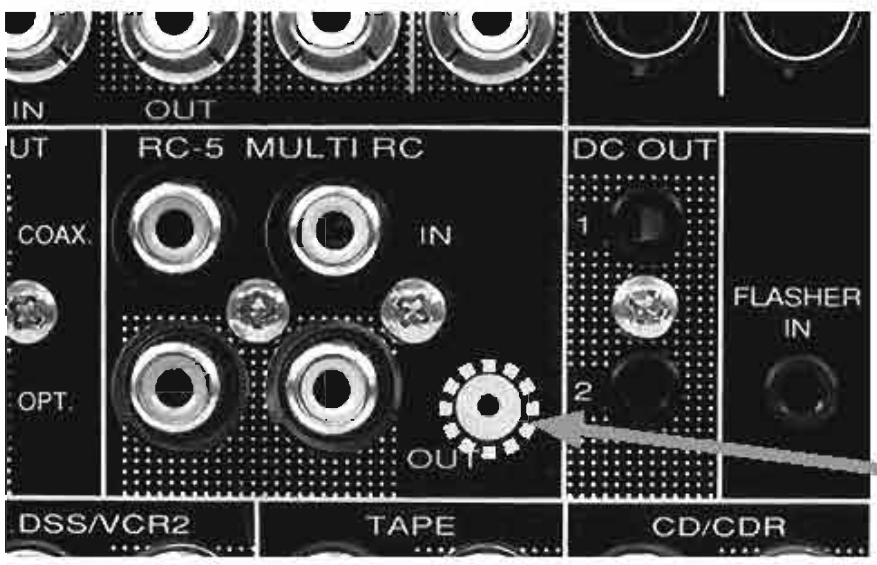
Mode 1: Update/Download MAIN CPU's software to internal Flash-ROM

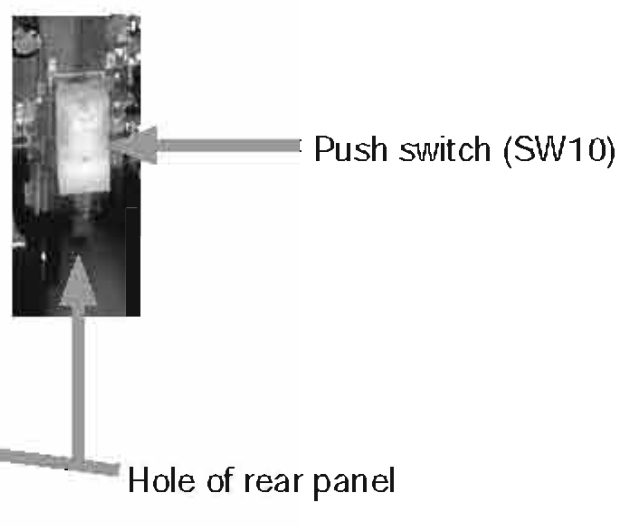
Update/Download software for MAIN CPU (Mode 1)

1. Put the "MAIN" folder into anywhere on your PC's hard disc.



2. Connect RS-232C on the rear panel of the unit and Serial Port of windows PC with RS-232C cable.
3. Insert a thin rot to the hole near the MULTI RC OUT terminal and push the switch (SW10) inside to turn on the switch.





4. Connect the mains cord into the unit. And press the **POWER ON/STANDBY** button for turn on the unit. (Except U1B)

NOTE : When the unit is into boot mode, STANDBY LED is lights at green.

Mode 1: Update/Download MAIN CPU's software to internal Flash-ROM

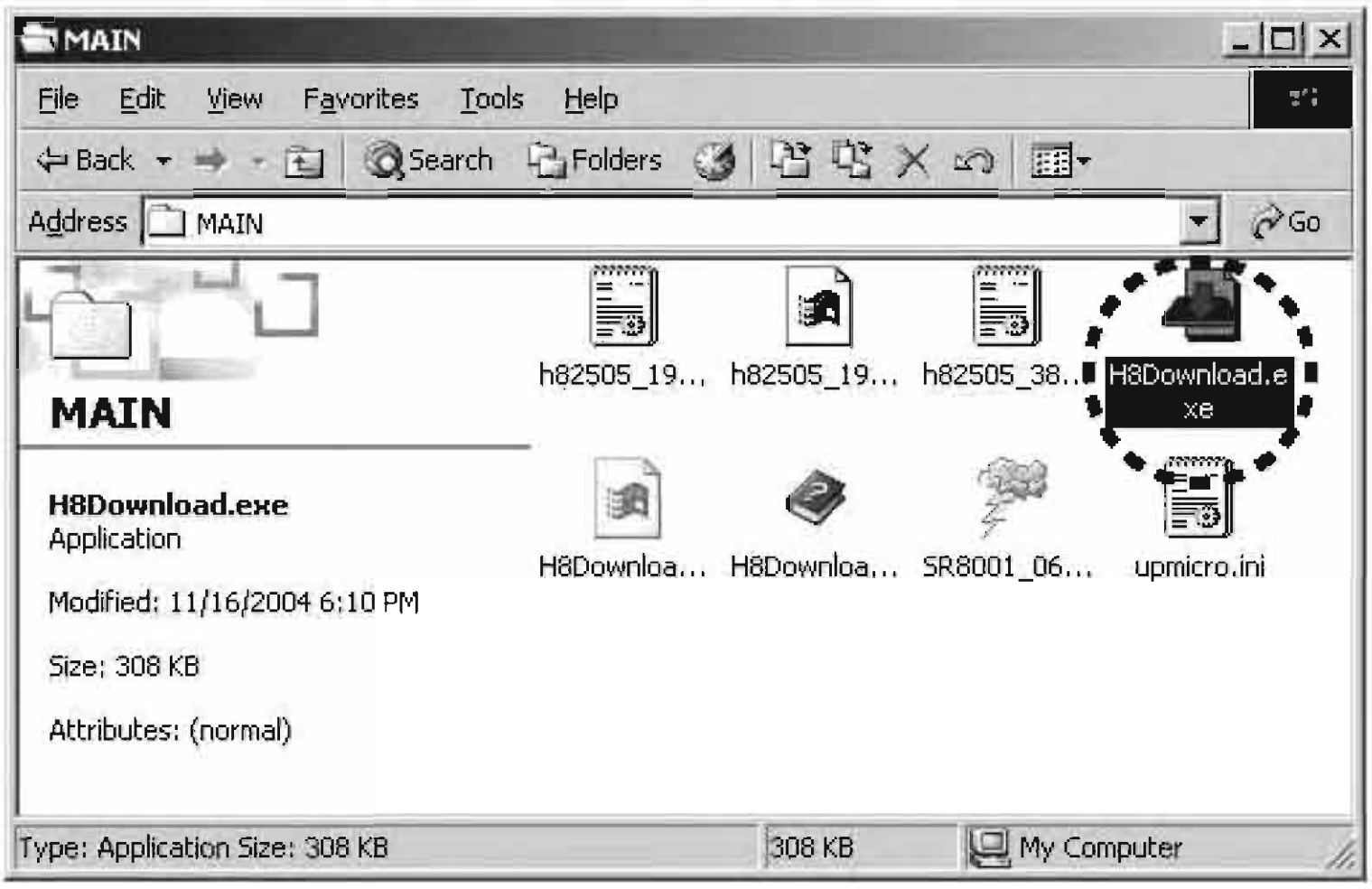
Update/Download software for MAIN CPU (Mode 1)

1. "MAIN"フォルダをPCの任意のフォルダにコピーします。
2. 本機のリアパネルにあるRS-232CコネクタとWindows PCのSerialポートをRS-232Cケーブルで接続します。
3. 細い棒を使い本機のMULTI RC OUT端子の右となりにある穴から内部スイッチ(SW10)を押して書き込みモードにします。
4. 本機に電源ケーブルを差し、**POWER ON/STANDBY**ボタンを押して電源を入れます。

注意: 本機が書き込みモードになるとSTANDBY LEDが緑色に点灯します。

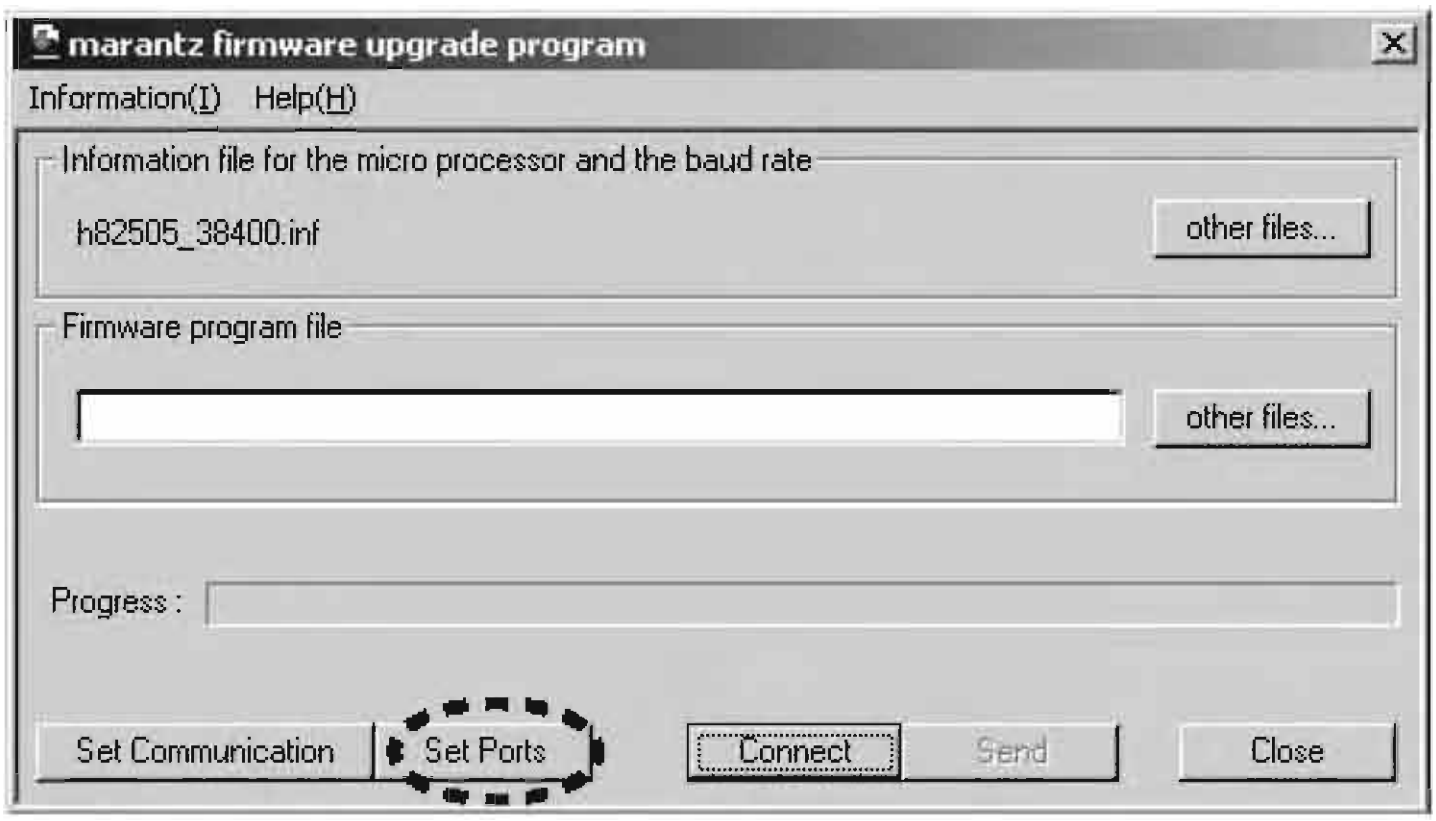
5. Double click the H8Download.exe. And launch the marantz firmware upgrade program.

5. H8Download.exeをダブルクリックし、marantz firmware upgrade programを起動します。



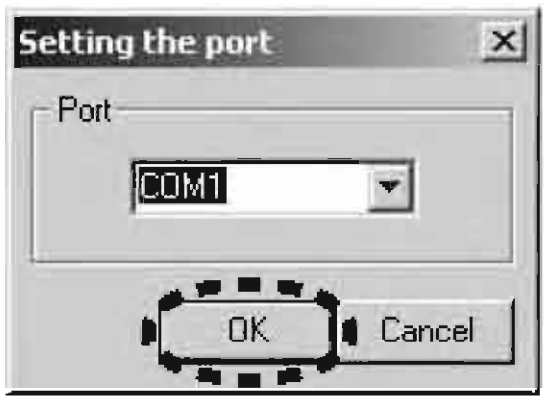
6. Click the **Set Ports**.

6. **Set Ports**をクリックします。



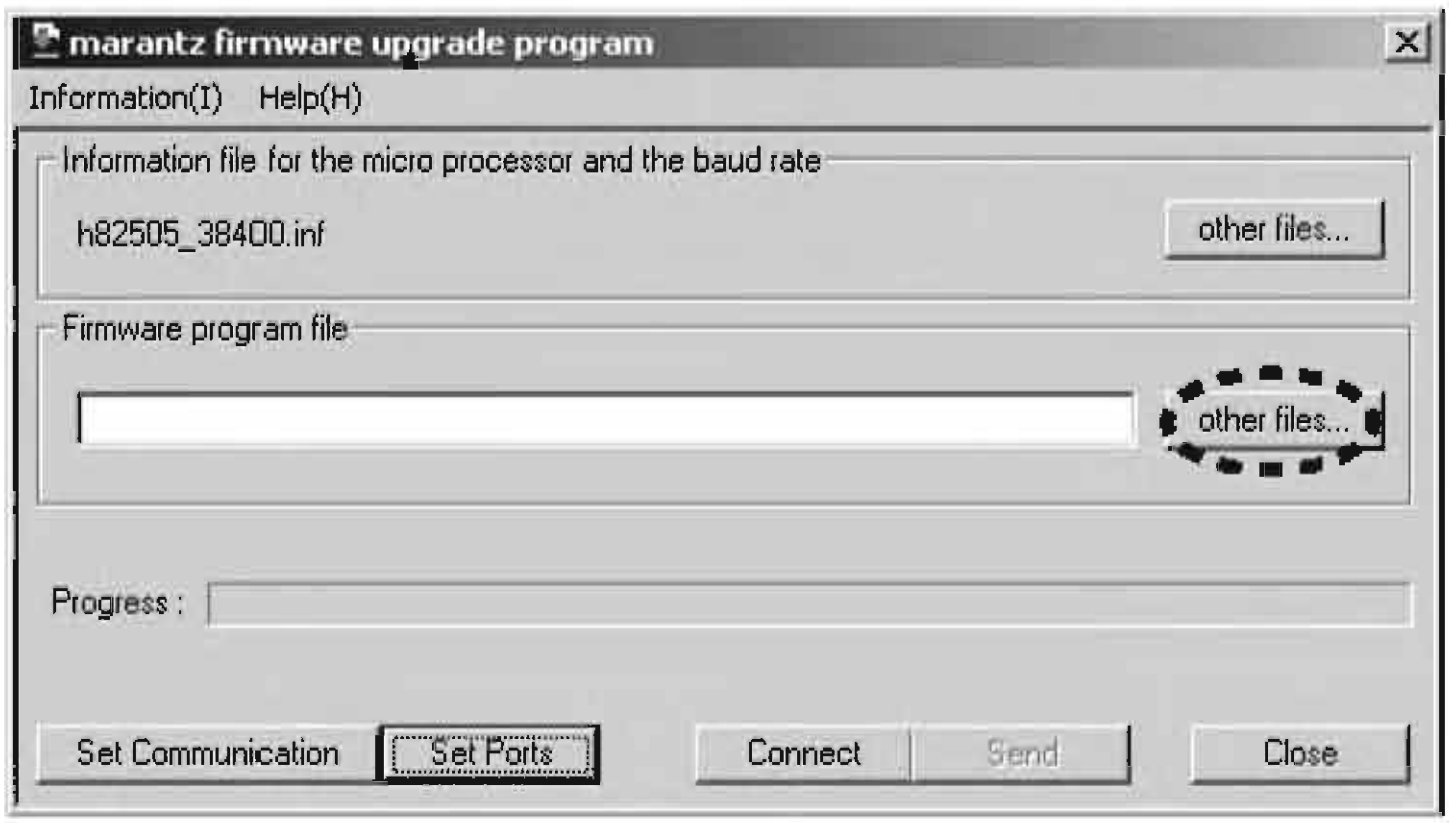
7. Choose the **COM Port number**. And Click the **OK**.

7. 使用する**COM**ポート 番号を選択し、**OK**をクリックします。



8. Click the **other files...** in the Firmware program file.

8. Firmware program file内の**other files...**をクリックします。

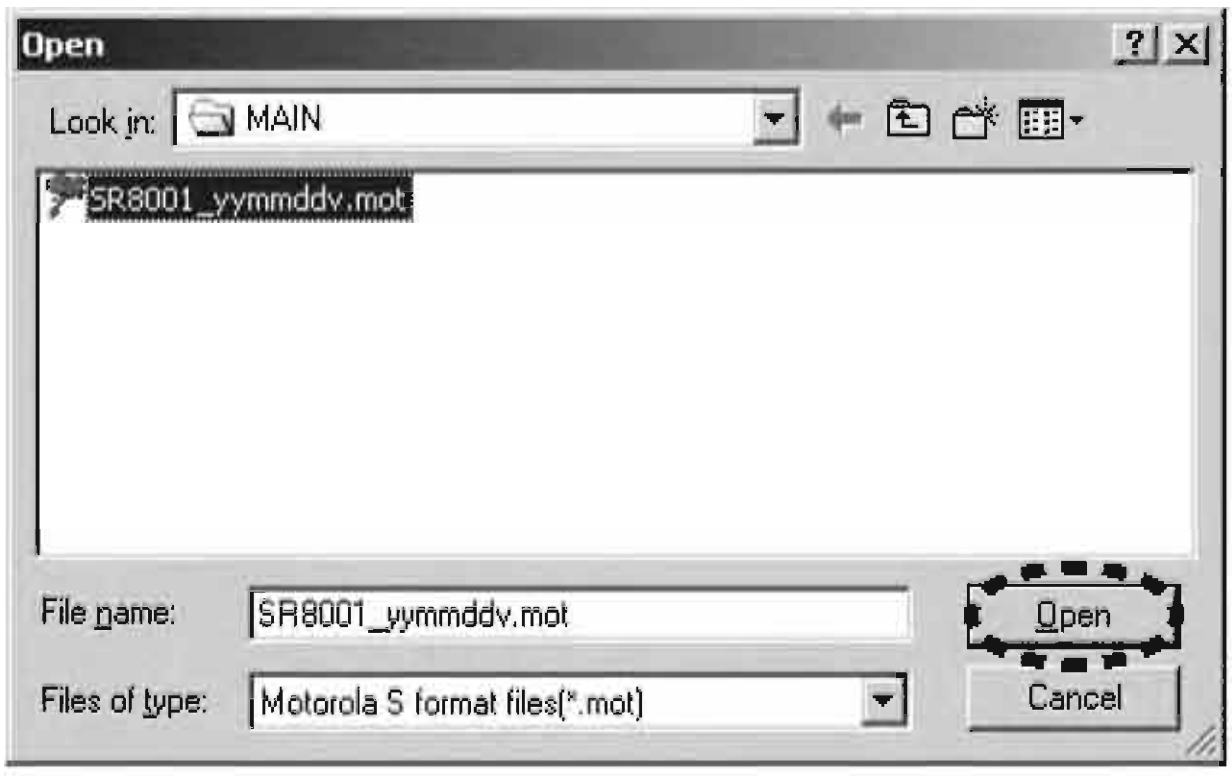


9. Choose the SR8001_yymmddv.mot. And click the **Open**.

NOTE : The yy is two digits of year. The mm is month. The dd is date. The v is release number.

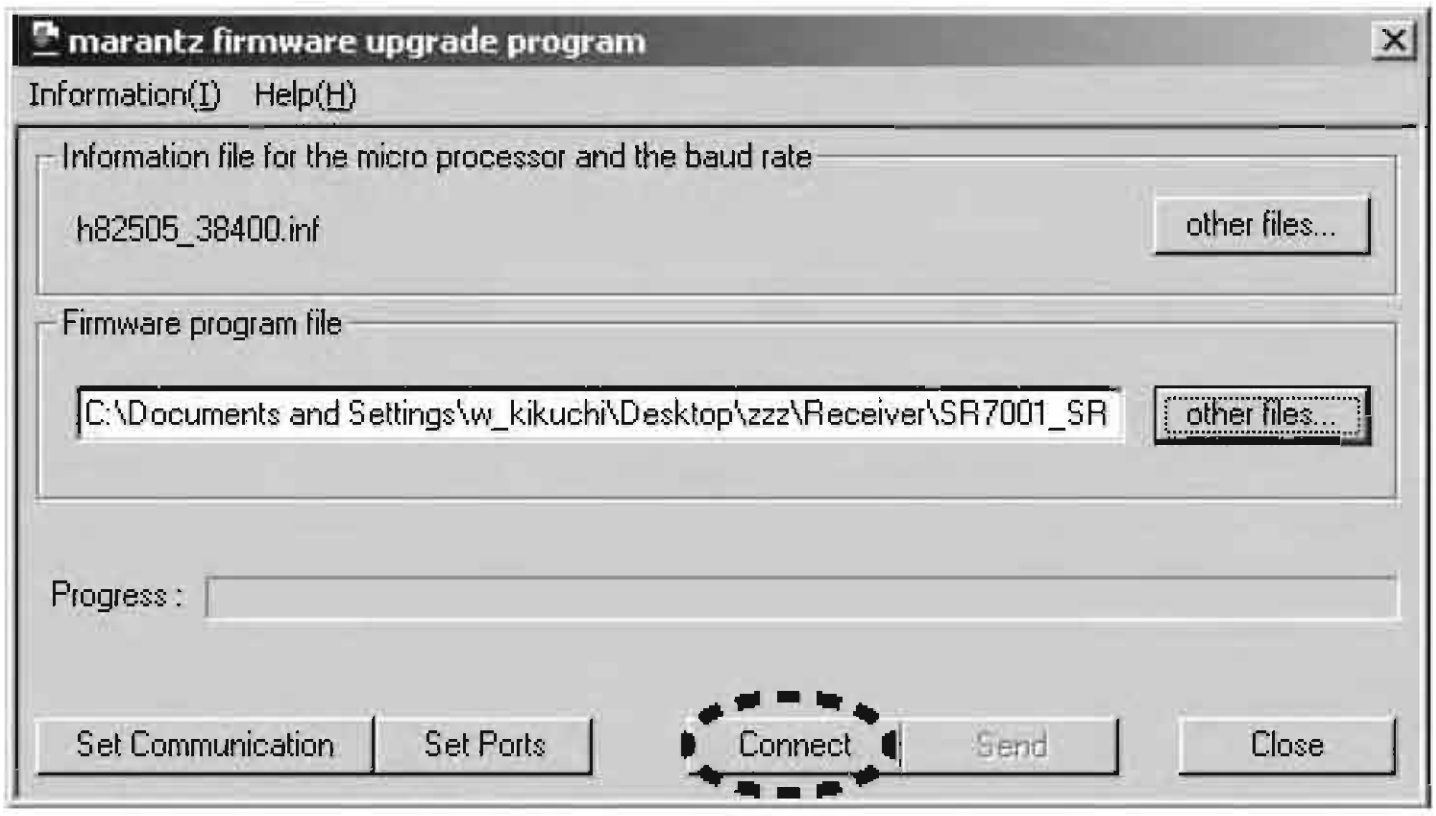
9. SR8001_yymmddv.motを選択し、**Open**をクリックします。

注意 : yyは年の下二桁、mmは月、ddは日、vはリリースナンバー



10. Click the **Connect**.

10. **Connect**をクリックします。

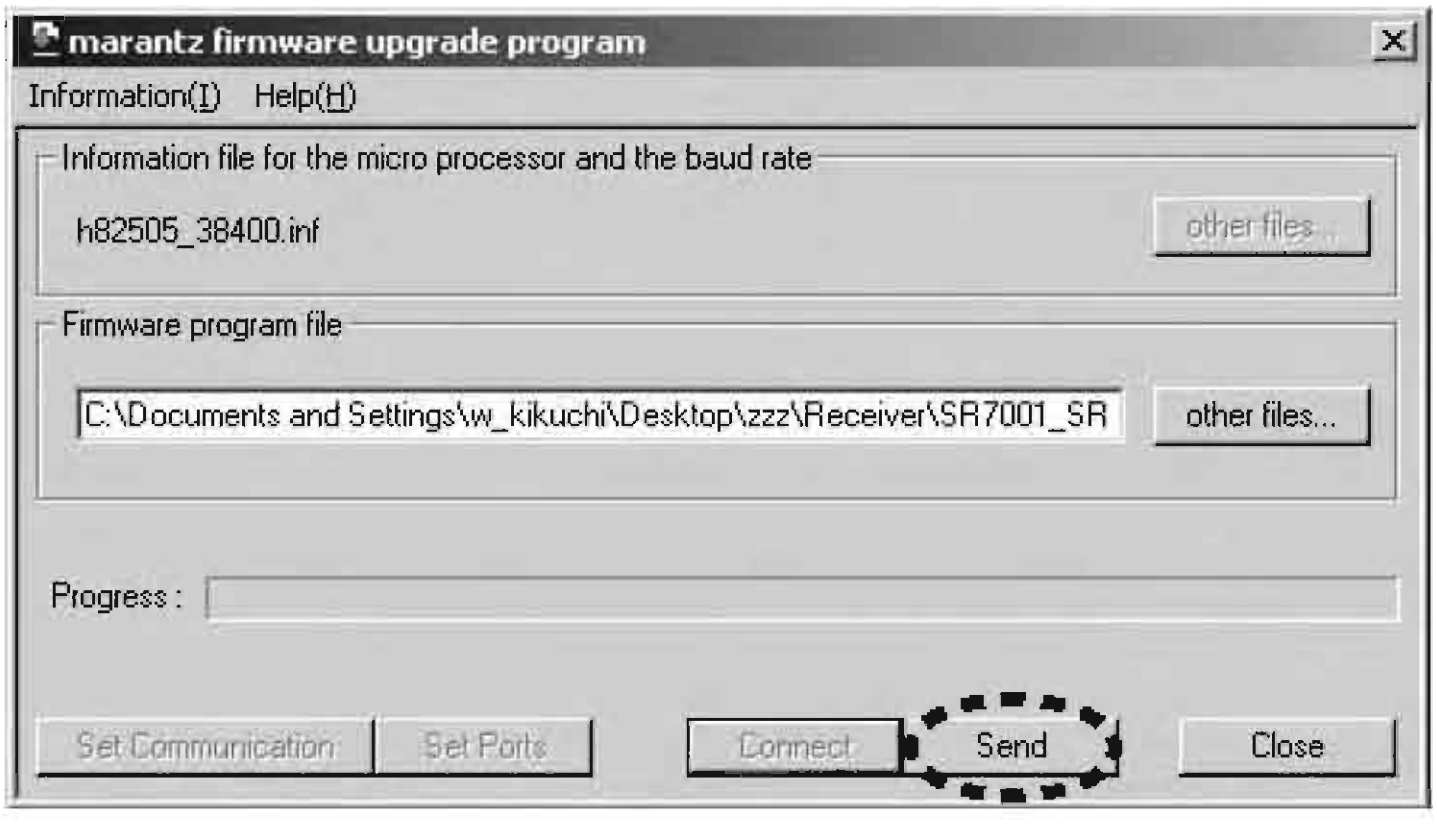


11. If the connection with the H8 µ-P is successfully made, a dialogue box saying "Success to the H8 micro processor connection" appears. If the connection fails, error message will appear.
Click the **OK**.

11. H8マイコンとの接続に成功すると"Success to the H8 micro processor connection"と表示したダイアログボックスが表示されます。接続に失敗するとエラーメッセージが表示されます。
OKをクリックします。

12. Click the **Send** to start update/download.
The writing of software takes about 2 minute and 30 seconds.

12. **Send**をクリックし書き込みを開始します。
書き込みにかかる時間は約2分30秒です。

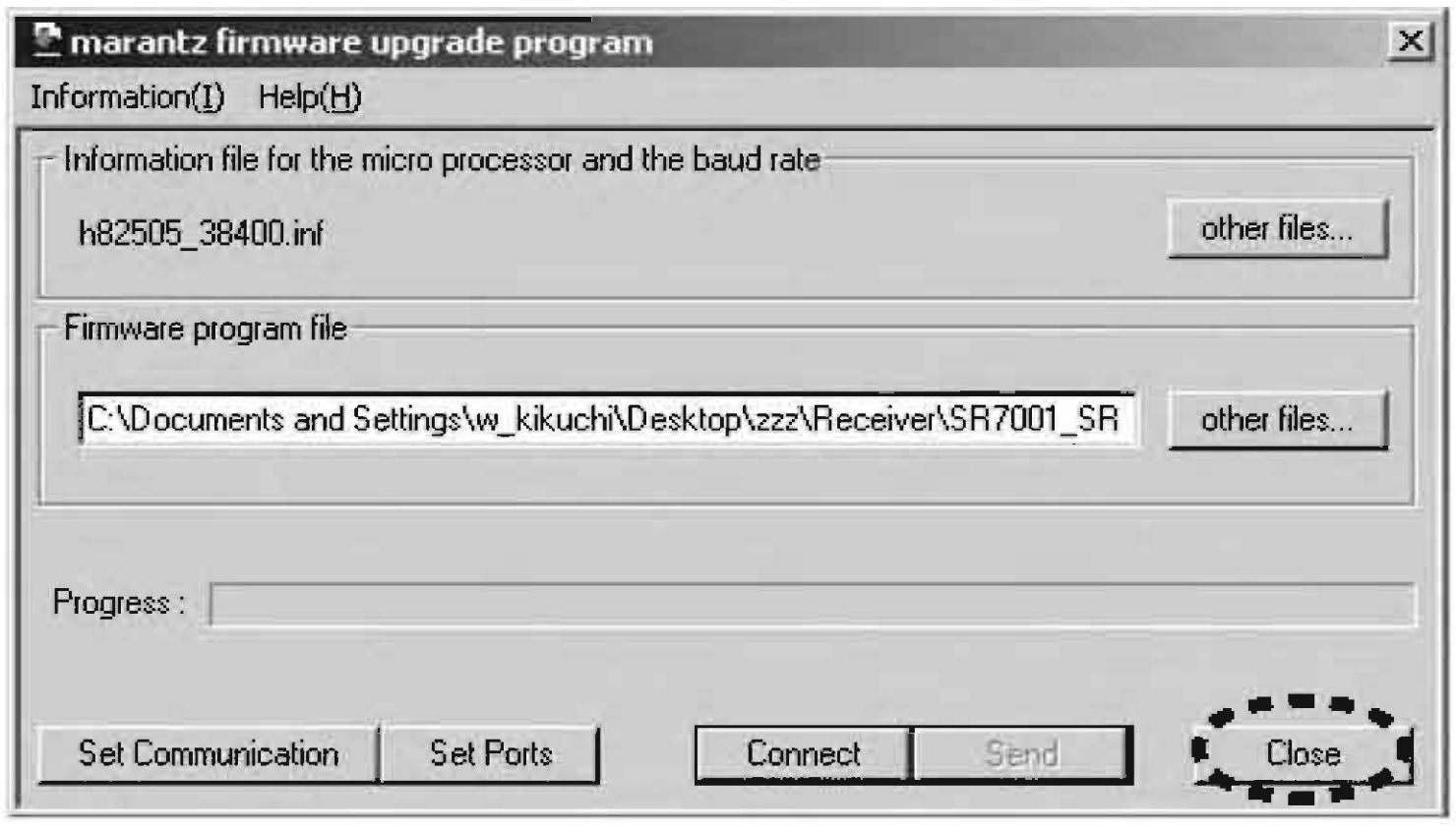


13. If the firmware is updated/downloaded successfully, a dialog box saying "Finished the firmware program sending" appears.
Click the **OK**.

13. 書き込みが成功すると"Finished the firmware program sending"と表示したダイアログボックスが表示されます。
OKをクリックします。

14. Click the **Close** to close the application.

14. **Close**をクリックしアプリケーションを閉じます。



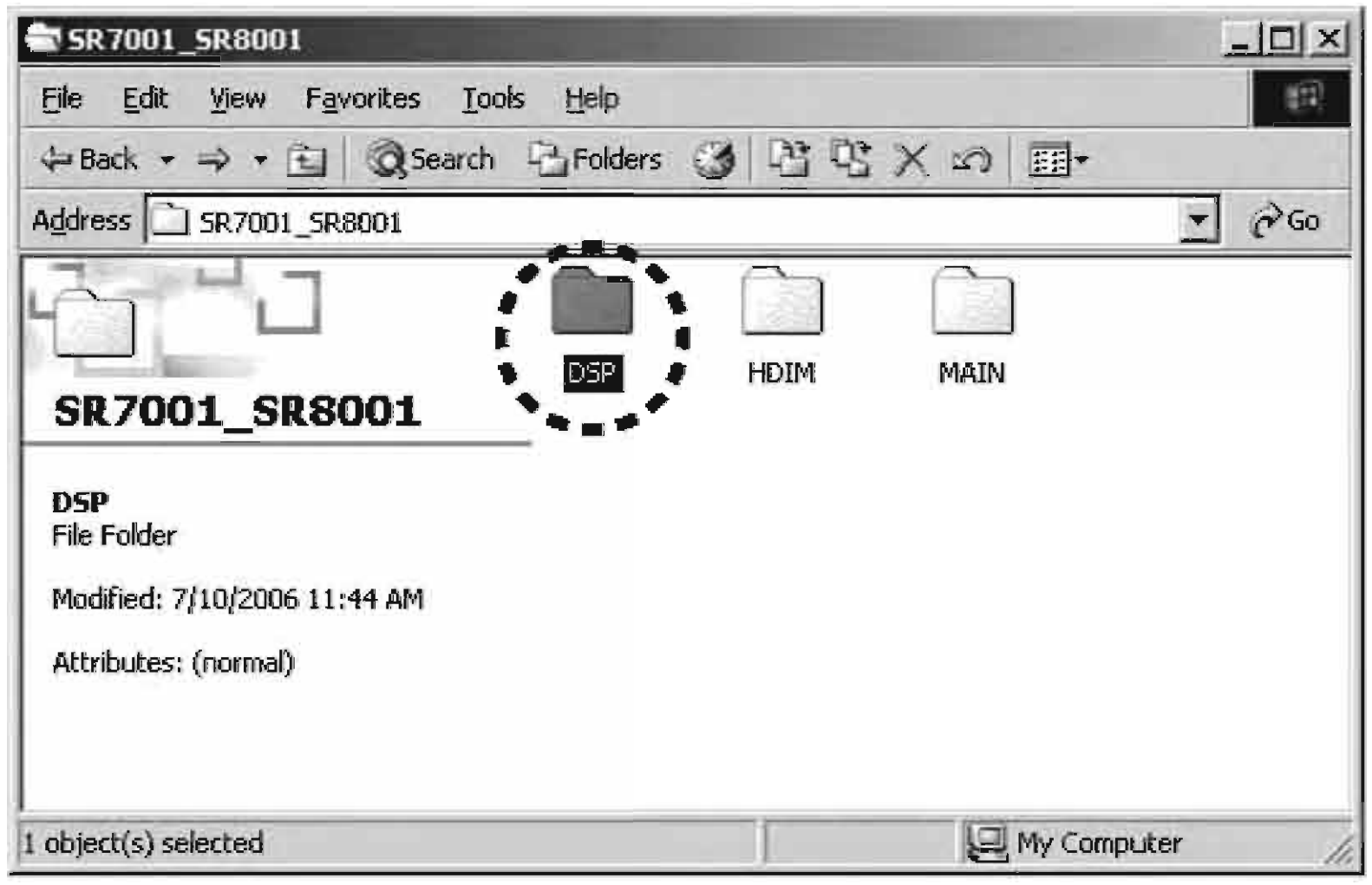
15. Press the **POWER ON/STANDBY** button for turn off the unit. (Except U1B)
16. Disconnect the mains cord and RS-232C cable from the unit.
17. Insert a thin rot to the hole and push the switch (SW10) inside to turn off the switch.

15. **POWER ON/STANDBY**ボタンを押して本機の電源を切ります。
16. 電源ケーブルとRS-232Cケーブルを本機から外します。
17. 細い棒を使い本機のMULTI RC OUT端子の右となりにある穴から内部スイッチ(SW10)を押して書き込みモードを解除します。

Mode 2 :Update/Download DSP's software to 8M Flash-ROM

Update/Download Software for DSP (Mode 2)

1. Put the "DSP" folder into anywhere on your PC's hard disc.



2. Connect the RS-232C on rear panel of the unit and the Serial Port of windows PC with RS-232C cable.
3. Connect the mains cord into the unit.
4. Press the **POWER ON/STANDBY** button for turn on the unit.
5. Press the **ENTER**, **SURROUND MODE** and **T-MODE** buttons simultaneously more than 3 seconds to turn the unit into Loading Mode.
6. The FLD shows "SELECT DSP" after showed "LOADING MODE".
7. Press the **ENTER** button.
8. "SELECTED DSP" shows on the FLD.

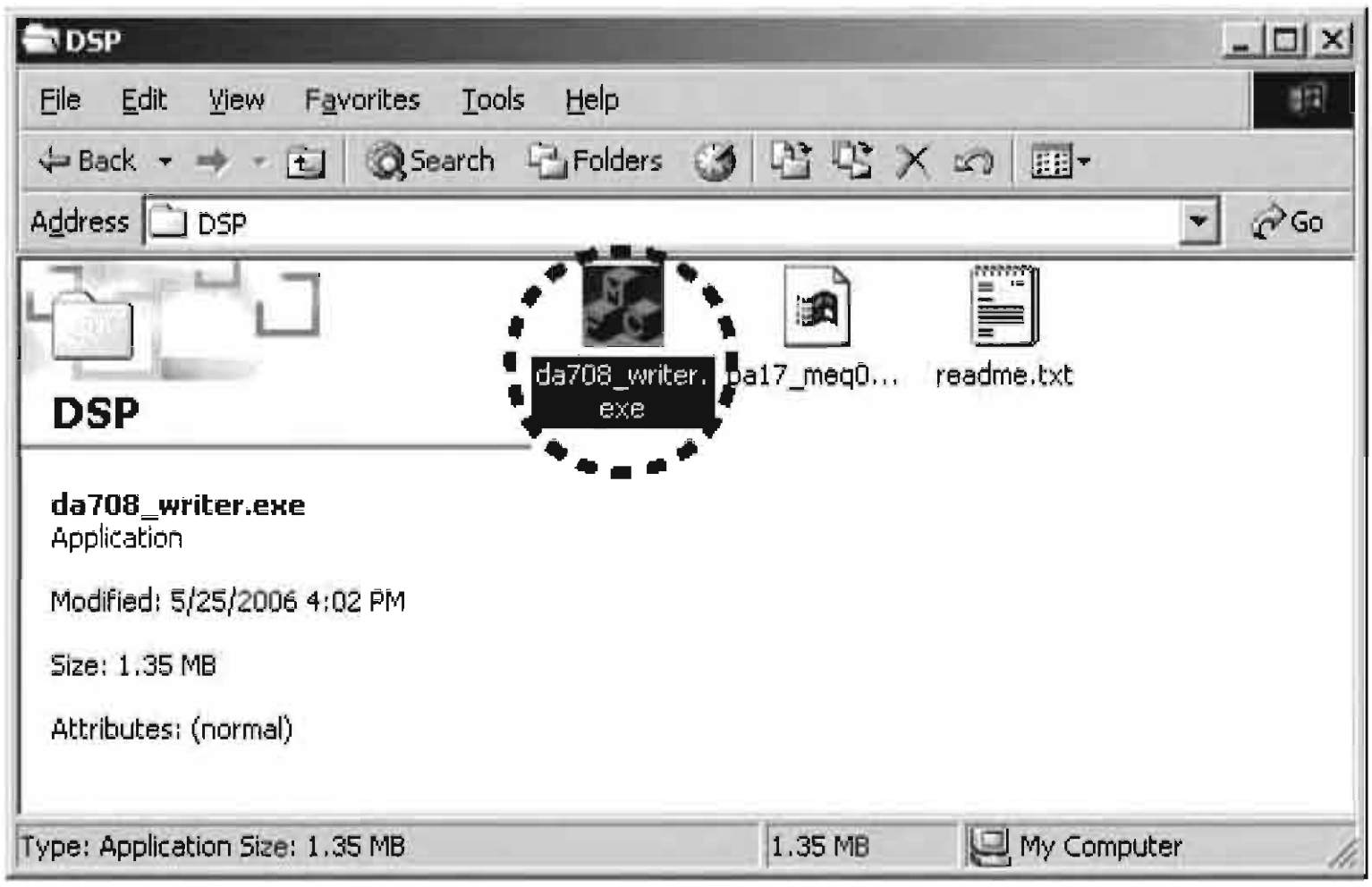
Mode 2: Update/Download DSP’s software to 8M Flash-ROM

Update/Download Software for DSP (Mode 2)

1. "DSP"フォルダをPCの任意のフォルダにコピーします。
2. 本機のリアパネルにあるRS-232Cコネクタと Windows PCのSeriaポートをRS-232Cケーブルで接続します。
3. 本機に電源ケーブルを差します。
4. **POWER ON/STANDBY**ボタンを押し、本機の電源を入れます。
5. **ENTER**, **SURROUND MODE**, **T-MODE**の3つボタンを同時に3秒以上押し続け、本機をローディングモードにします。
6. FLに"LOADING MODE"と表示された後、"SELECT DSP"と表示されます。
7. **ENTER**ボタンを押します。
8. FLの表示が"SELECTED DSP"に変わります。

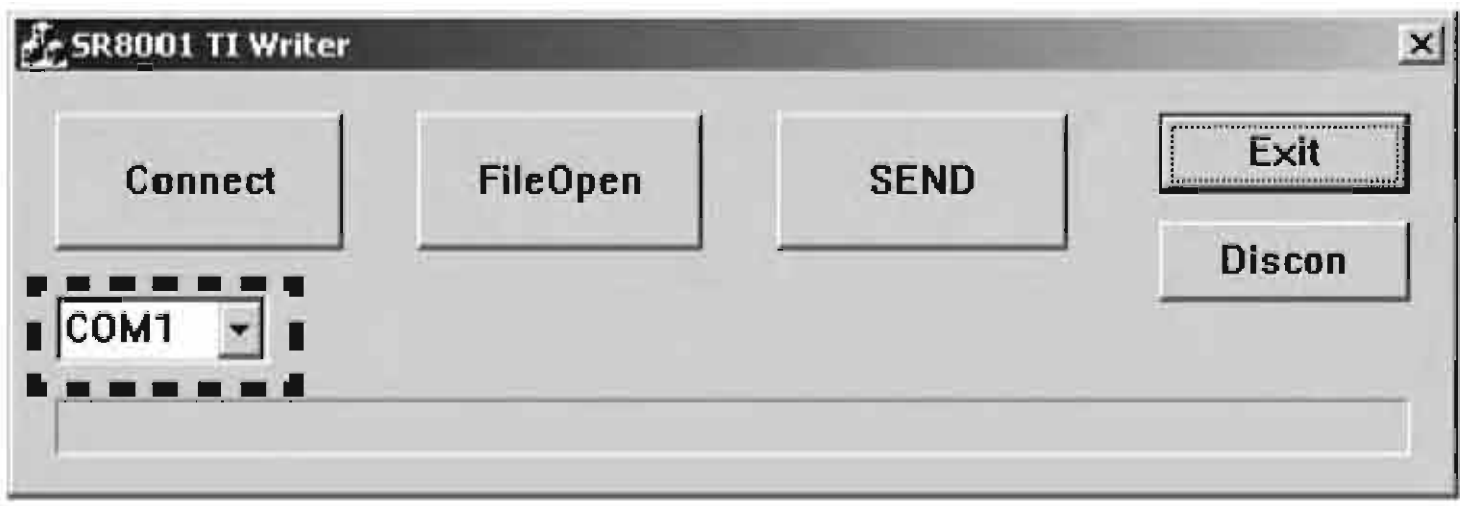
9. Double click the da708_writer.exe. And Launch the SR8001 TI Writer.

9. da708_writer.exeをダブルクリックし、SR8001 TI Writerを起動します。



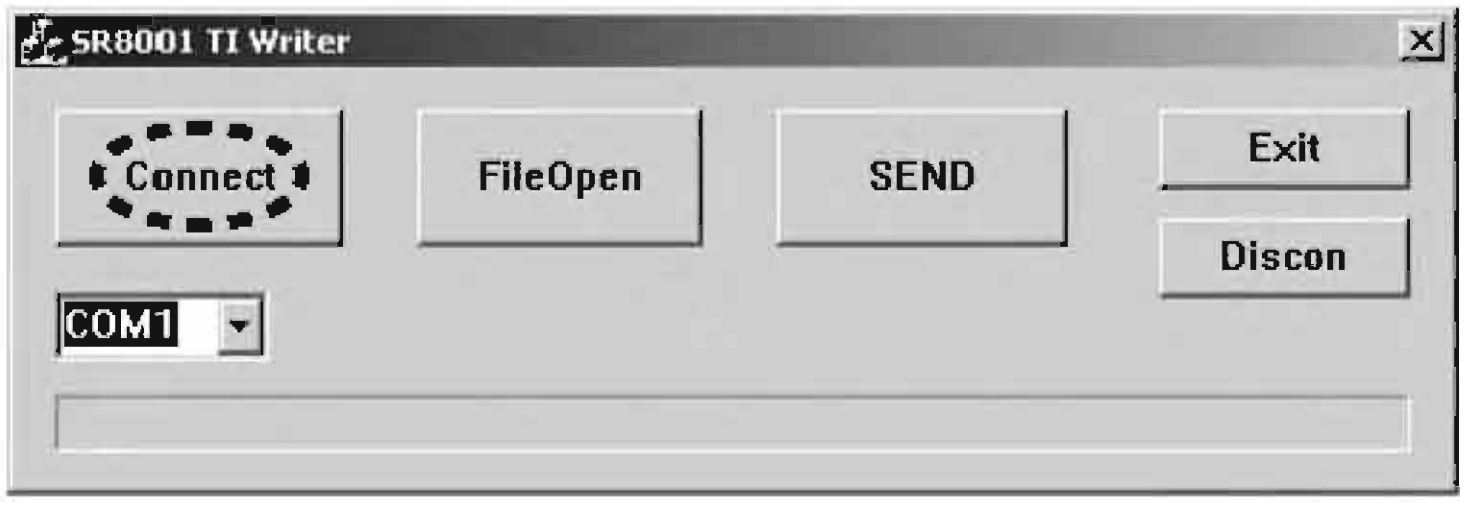
10. Choose the **COM Port number**.

10. 使用する**COM**ポート 番号を選択します。



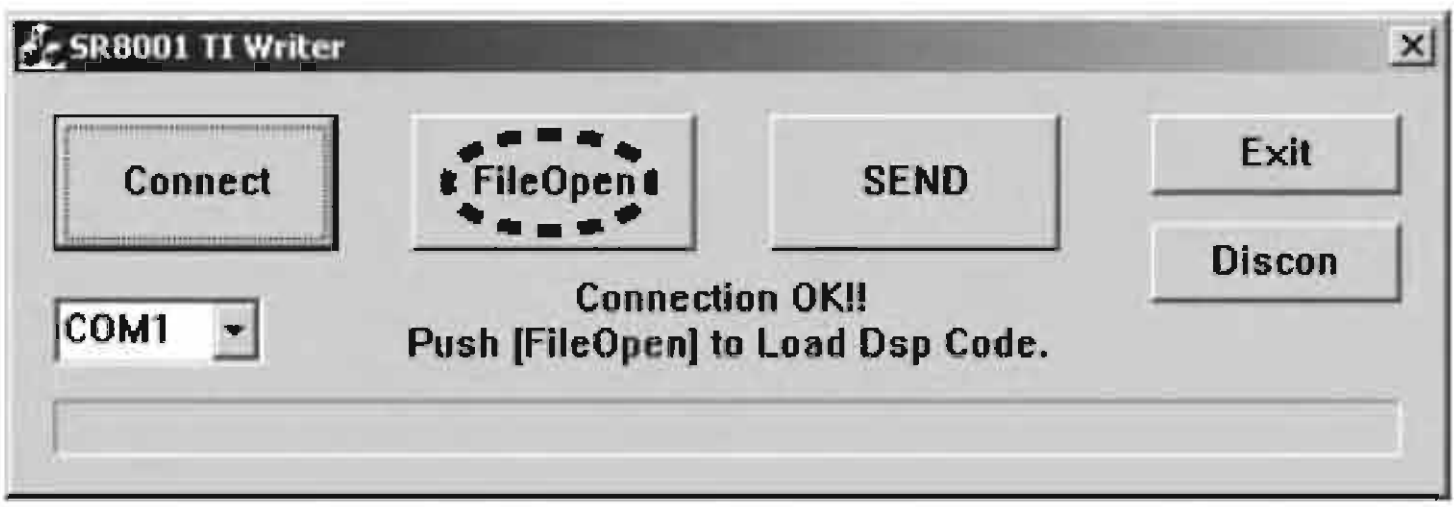
11. Click the **Connect**.

11. **Connect**をクリックします。



12. "Connection OK!!" appears on SR8001 TI Writer. And click the **FileOpen**.

12. SR8001 TI Writer上に"Connection OK!!"と表示されたら、**FileOpen**をクリックします。

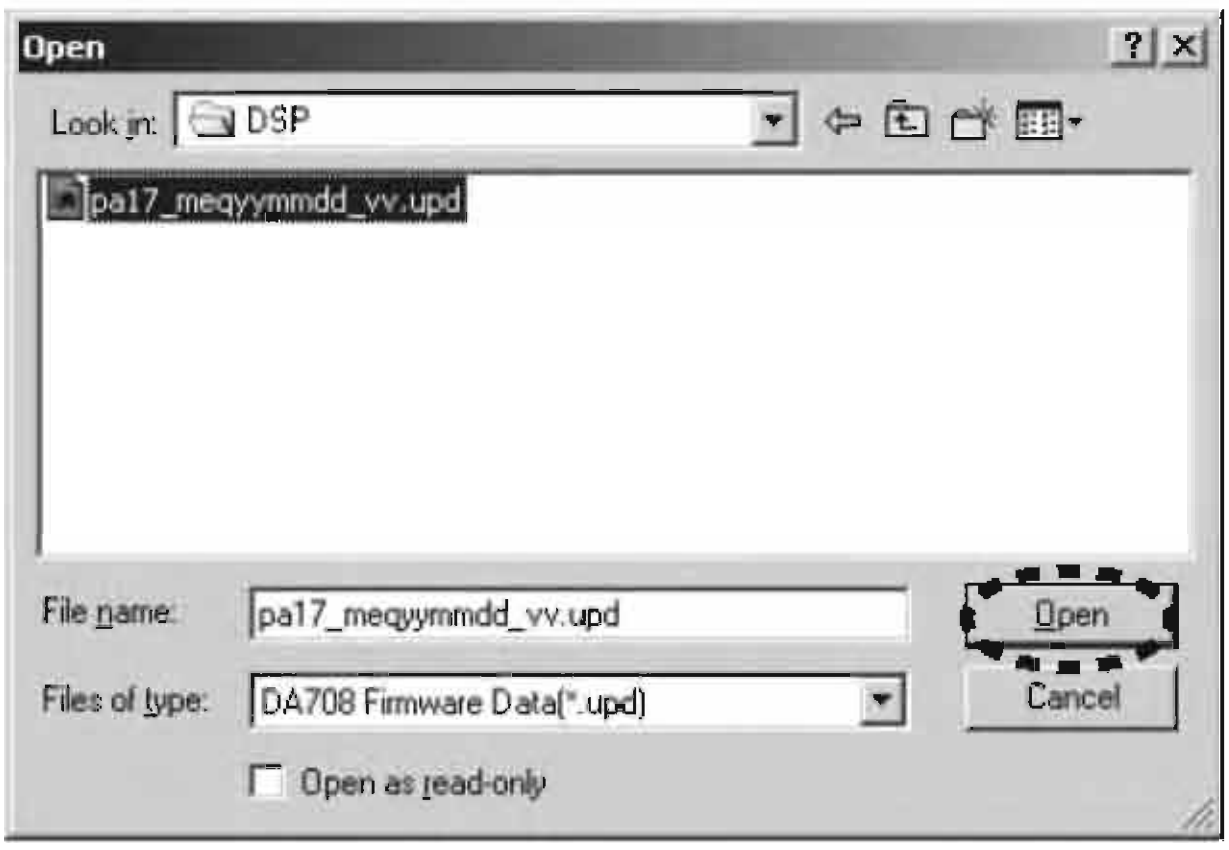


13. Choose the pa17_meqyymmdd_vv.upd. And click the **Open**.

NOTE : The yy is two digits of year. The mm is month. The dd is date. The vv is release number.

13. pa17_meqyymmdd_vv.updを選択し、**Open**をクリックします。

注意: yyは年の下二桁、mmは月、ddは日、vvはリリース番号

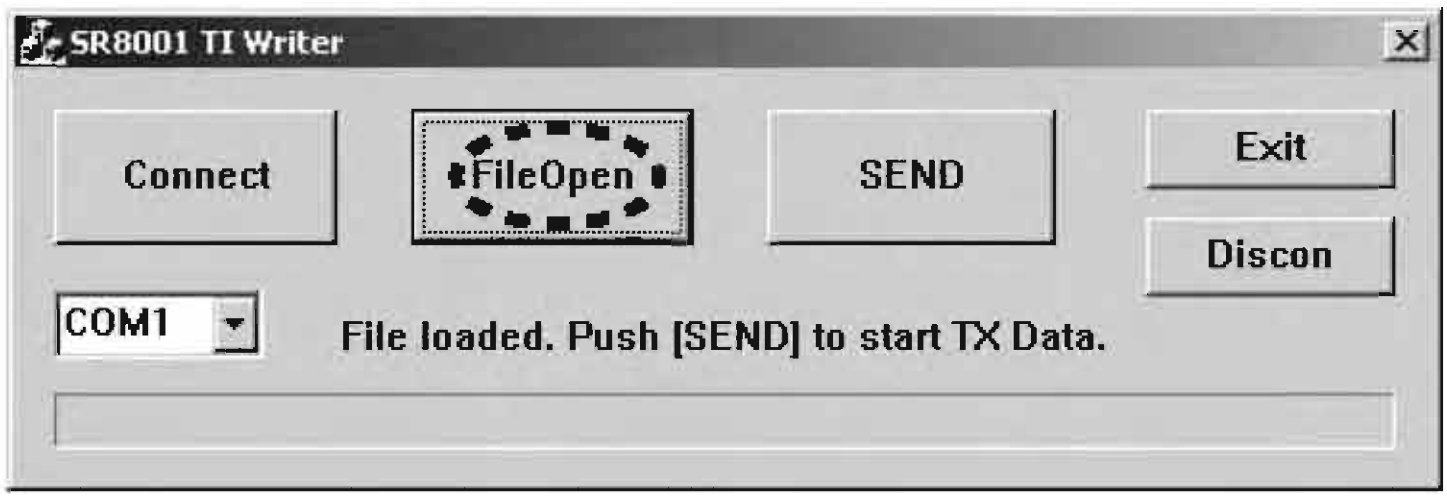


14. Click the **OK**.

14. **OK**をクリックします。

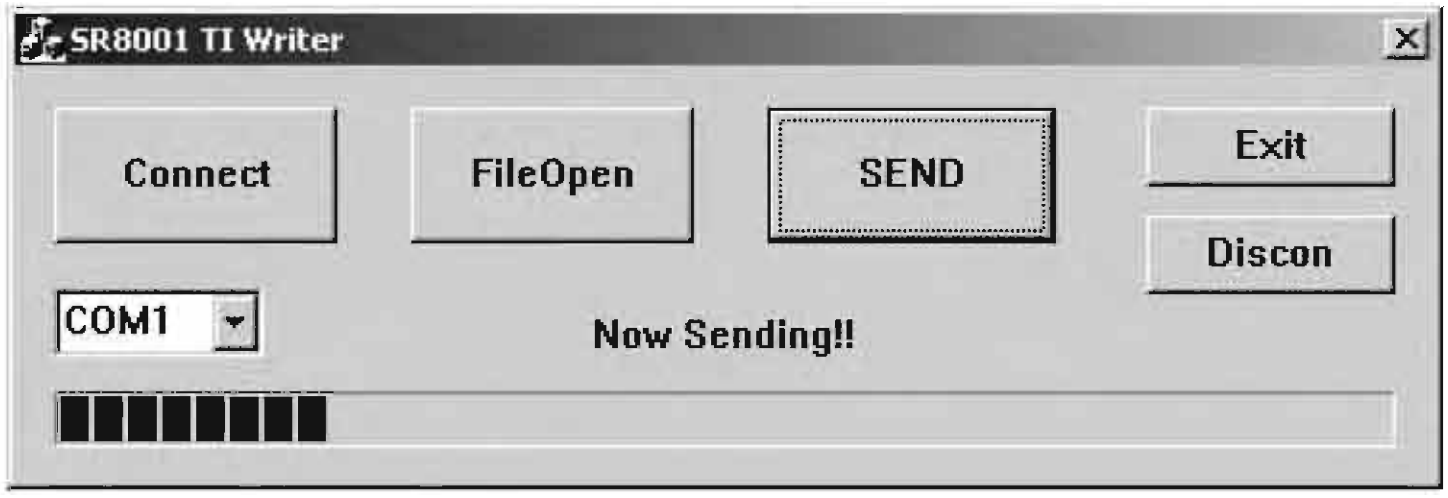
15. Click the **SEND**.

15. **SEND**をクリックします。



16. Software is written into the DSP Flash ROM.
The writing of software takes about 2 minute.

16. ソフトウェアがDSPフラッシュROMに書き込まれます。
書き込みにかかる時間は約2分です。



17. Click the **OK**.

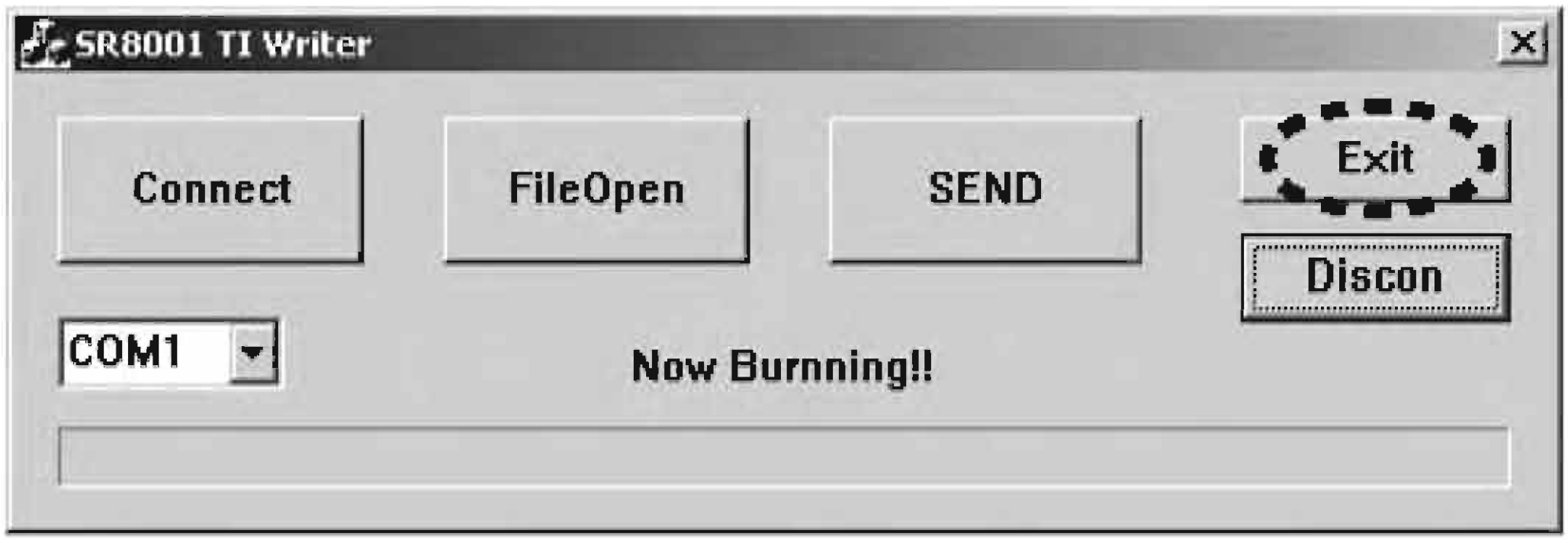
17. **OK**をクリックします。

19. Click the **Discon**.

18. **Discon**をクリックします。

19. Click the **Exit**.

19. **Exit**をクリックします。



20. Press the **POWER ON/STANDBY** button for turn off the unit.
21. Disconnect the mains cord and RS-232C cable from the unit.

20. **POWER ON/STANDBY**ボタンを押し、本機の電源を切ります。
21. 本機から電源コードとRS-232Cケーブルを外します。

Mode 3: Update/Download HDMI CPU's software to internal Flash-ROM.

Update/Download software for HDMI CPU (Mode 3)

[M3-1]The writing software setup procedure

1. Launch the Flash Development Toolkit v3.06 (FDT).

NOTE : Please refer to "[A] SOFTWARE (fdtv306r00.exe) DOWNLOAD AND INSTALL PROCEDURE", when you do not have FDT.
Can NOT update/download software by FDT ver.3.3.

2. Click Start, Programs, Renesas, Flash Development Toolkit 3.06 and Flash Development Toolkit 3.06.

3. Check the **Create a new project workspace**, and click the **OK**.

NOTE : It is needs setup for SR7001/SR8001. When you have already setup, please advance to "**[M3-2] Writing Procedure for HDMI CPU**".

Mode 3: Update/Download HDMI CPU's software to internal Flash-ROM.

Update/Download software for HDMI CPU (Mode 3)

[M3-1]The writing software setup procedure

1. Flash Development Toolkit v3.06 (FDT)を起動します。

注意: FDTを持っていない方は"[A] SOFTWARE (fdtv306r00.exe) DOWNLOAD AND INSTALL PROCEDURE"を参照してダウンロードしてください。
この書き込みはFDT ver.3.3では出来ません。

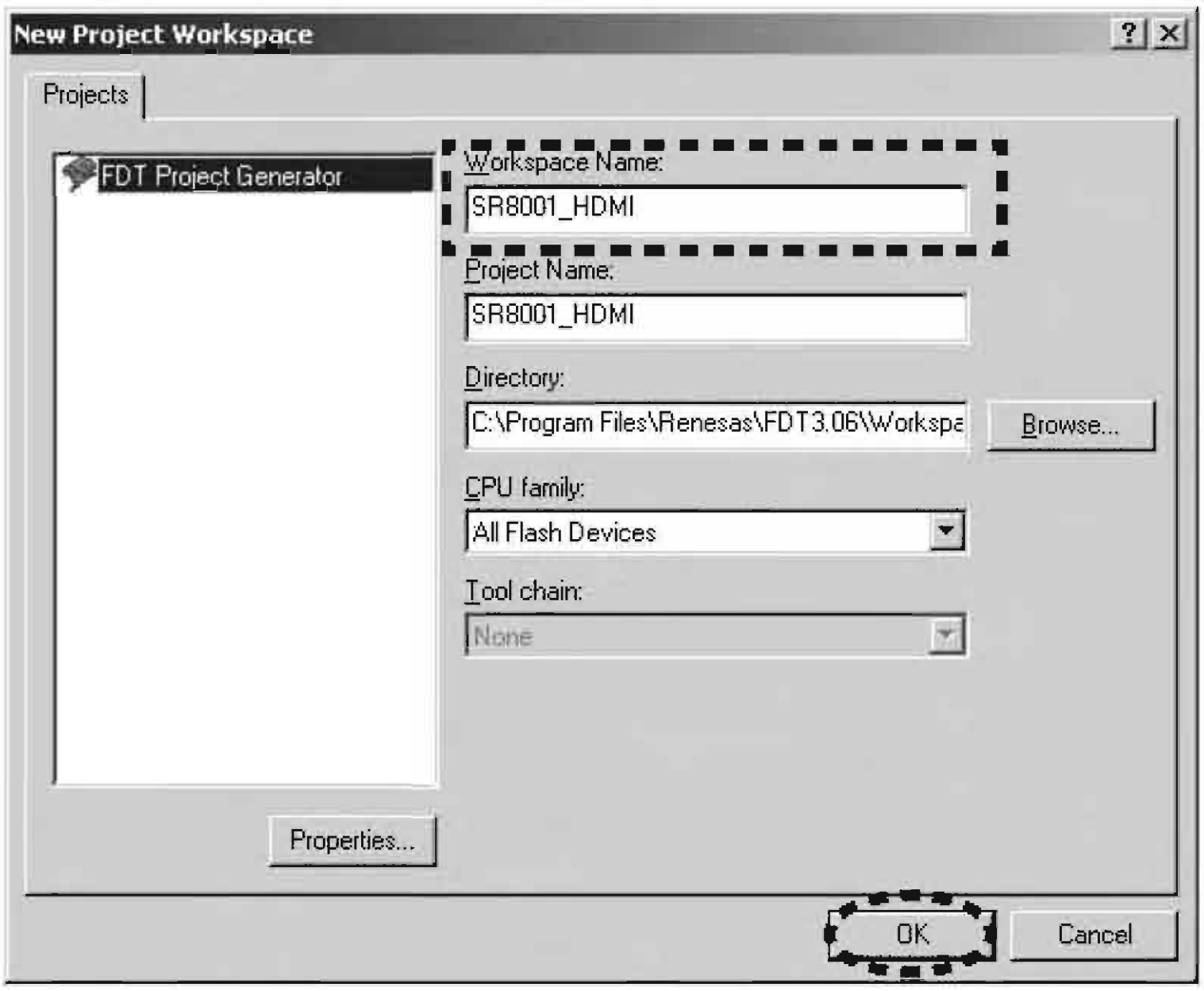
2. Start, Programs, Renesas, Flash Development Toolkit 3.06, Flash Development Toolkit 3.06をクリックします。

3. **Create a new project workspace**をチェックし、**OK**をクリックします。

注意: SR7001/SR8001用の設定が必要です。既に設定が終わっている方は"**[M3-2] Writing Procedure for HDMI CPU**"へ進んでください。

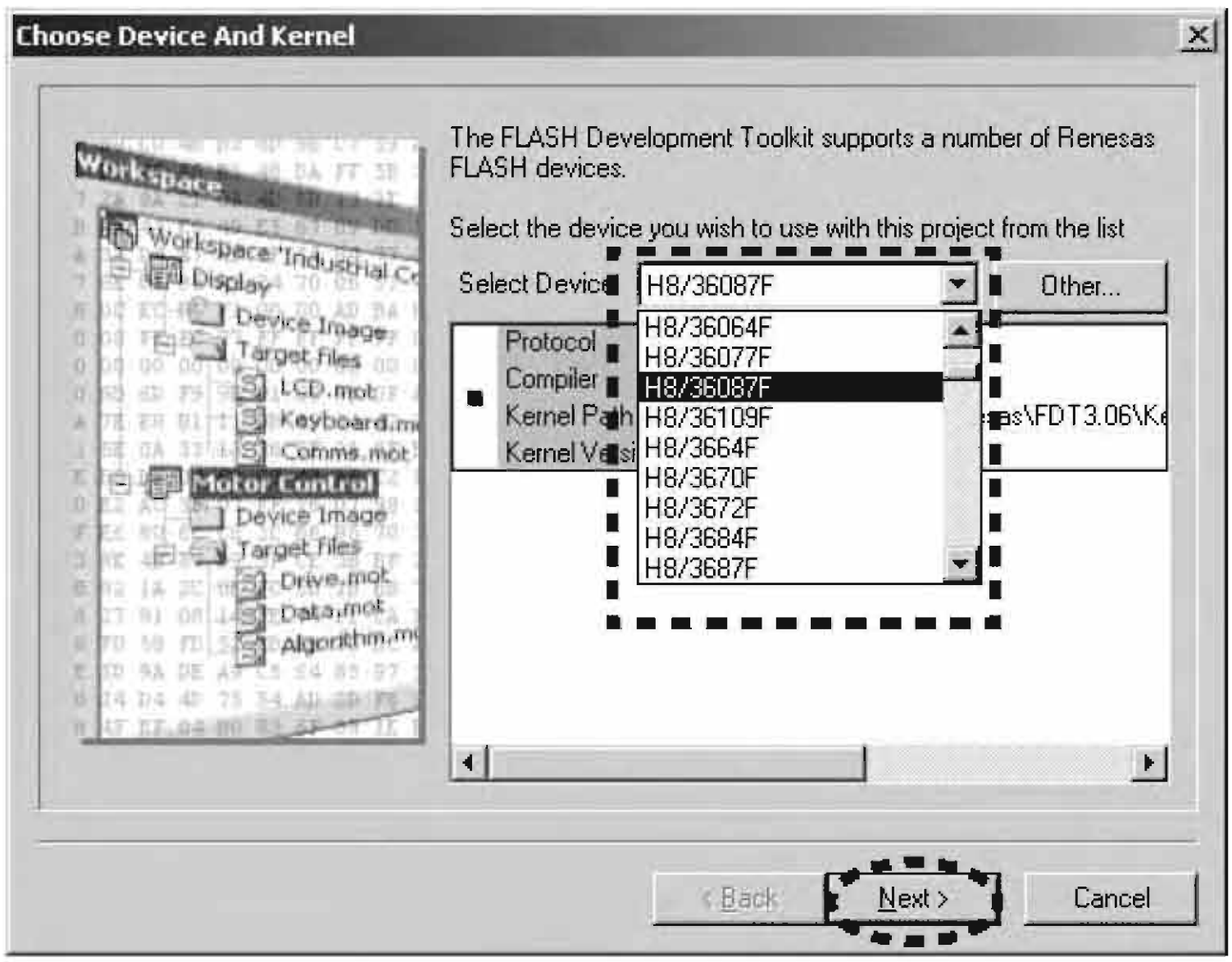
4. **SR8001_HDMI** is inputted into the Workspace Name. (It is simultaneously inputted into Project Name.) Click the **OK**.

4. Workspace Name に**SR8001_HDMI**を入力します。(同時にProject Nameにも入力されます) **OK**をクリックします。



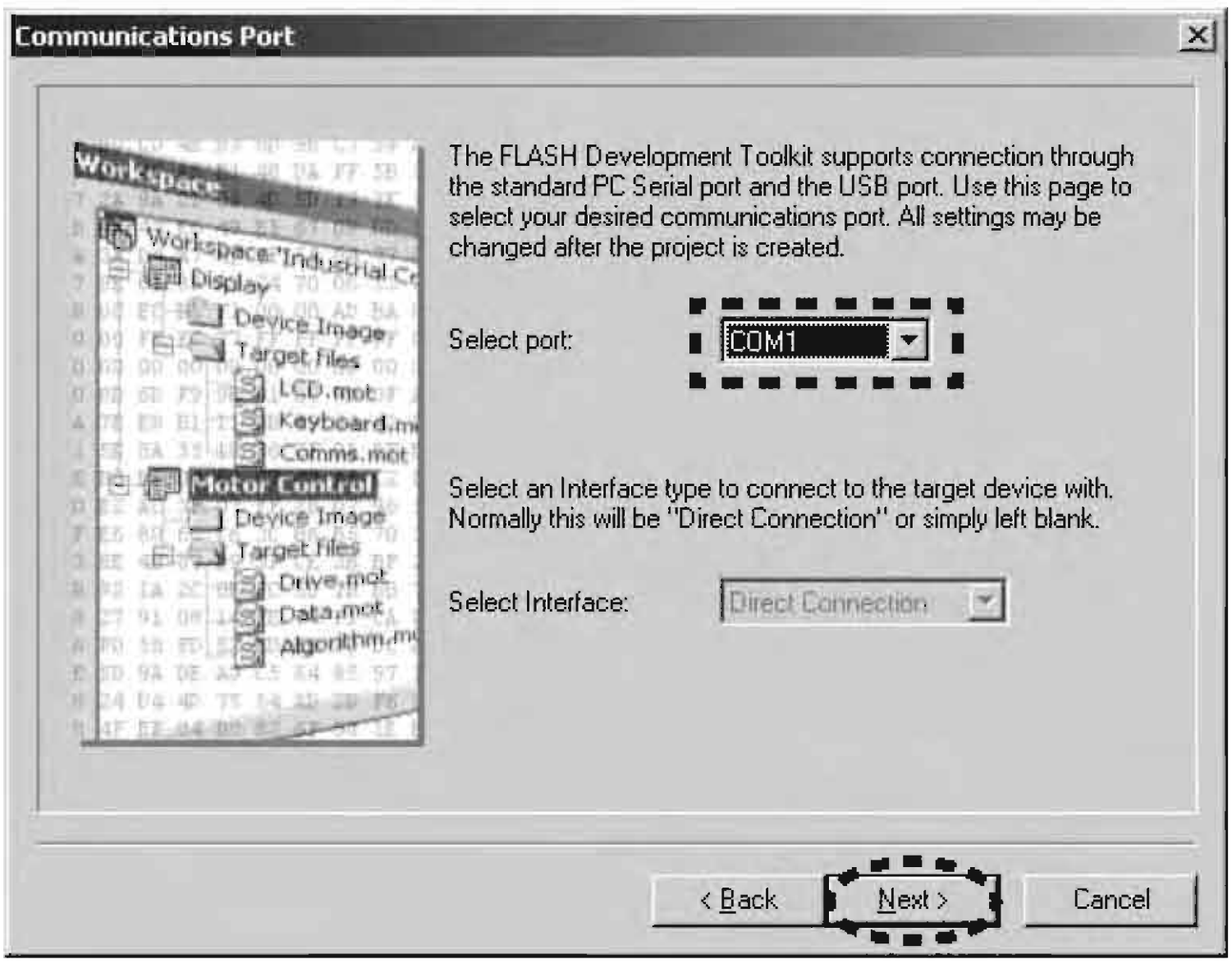
5. Choose the **H8/36087F** in Select Device. And click the **Next**.

5. Select Deviceから**H8/36087F**を選択し、**Next**をクリックします。



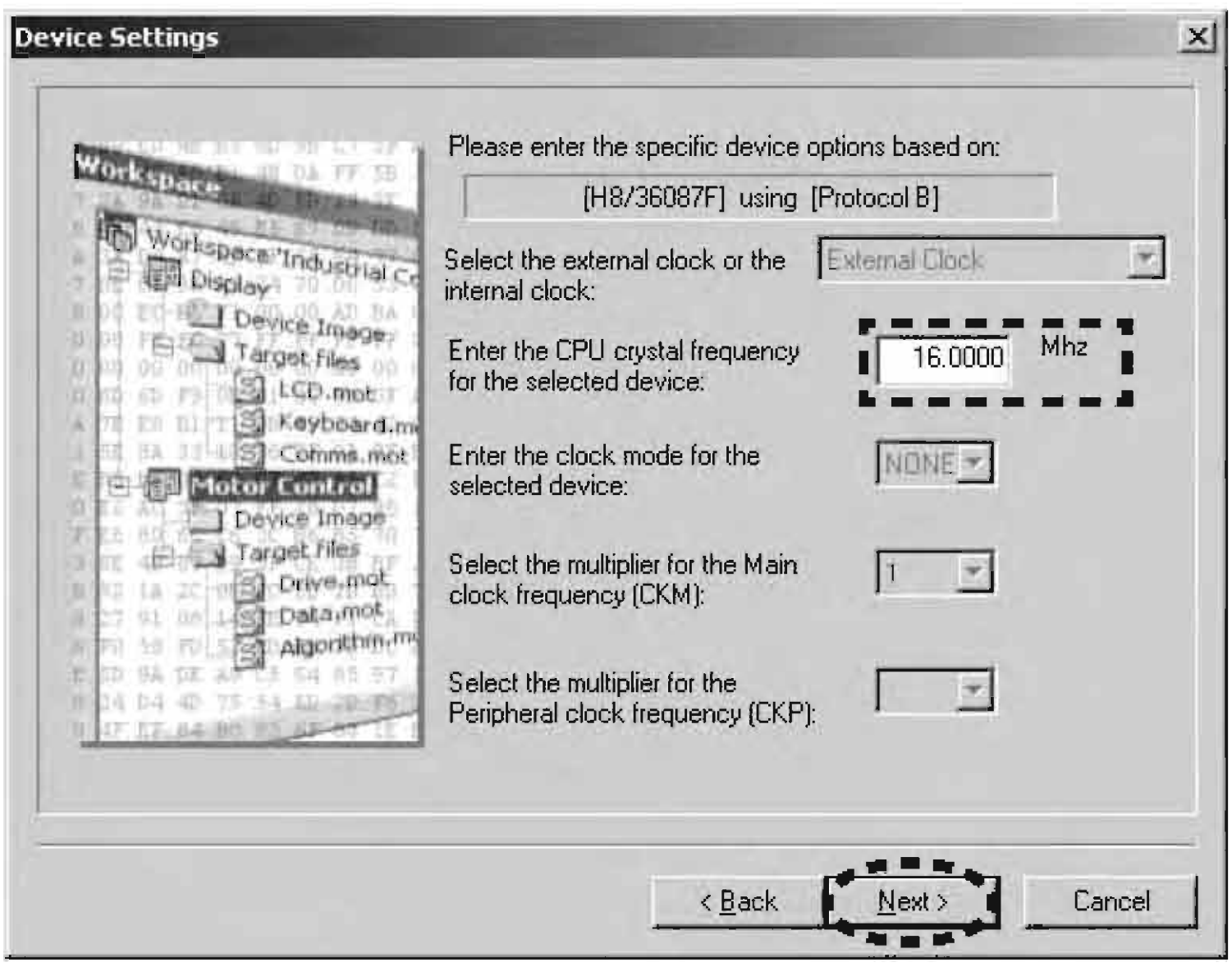
6. Choose the **Serial port number** in the Select Port. And click the **Next**.

6. Select Portから**Serial**ポート番号を選び、**Next**をクリックします。



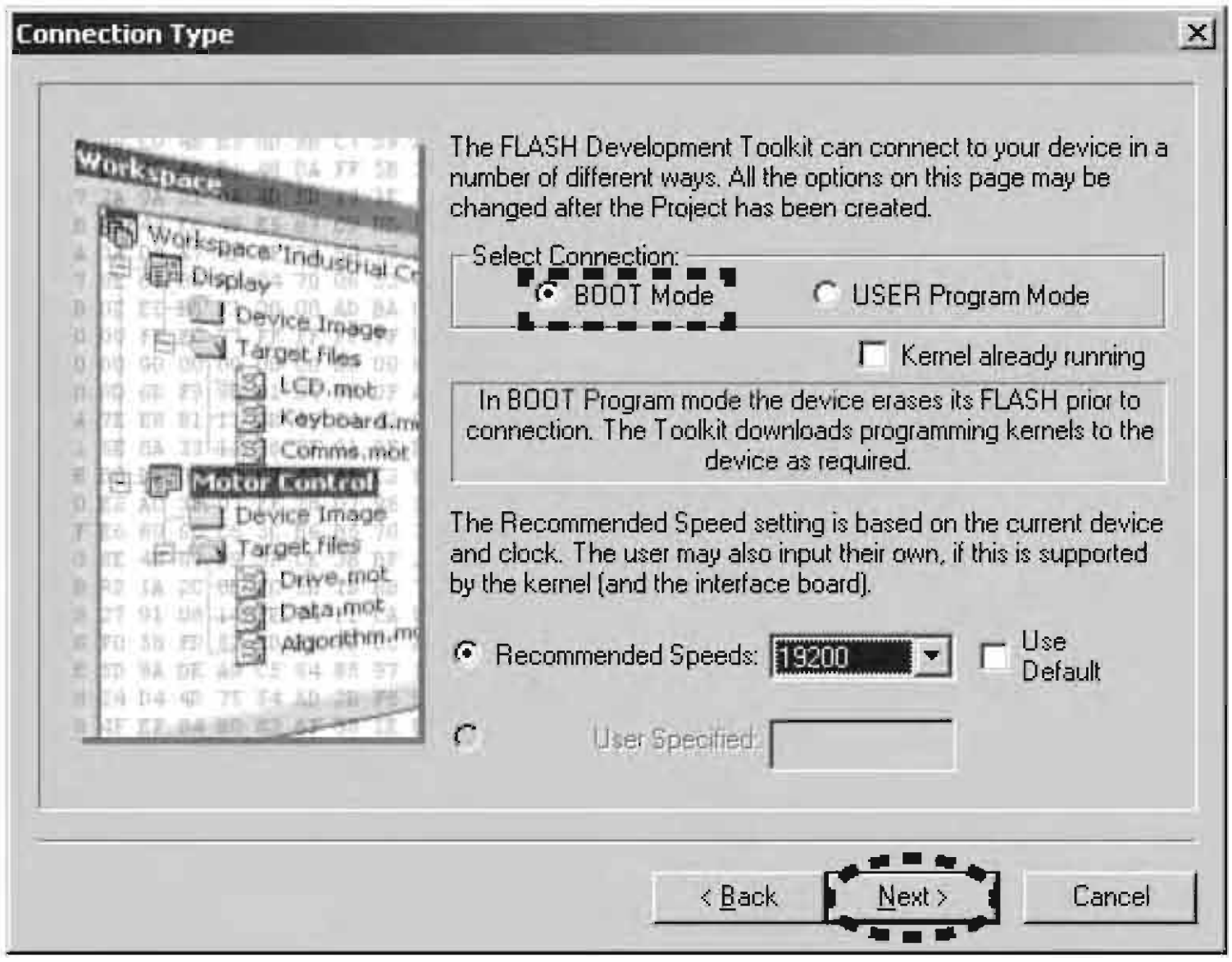
7. **16.0000** is inputted into the Enter the CPU crystal frequency for the selected device. And click the **Next**.

7. Enter the CPU crystal frequency for the selected device に**16.0000**を入力し、**Next**をクリックします。



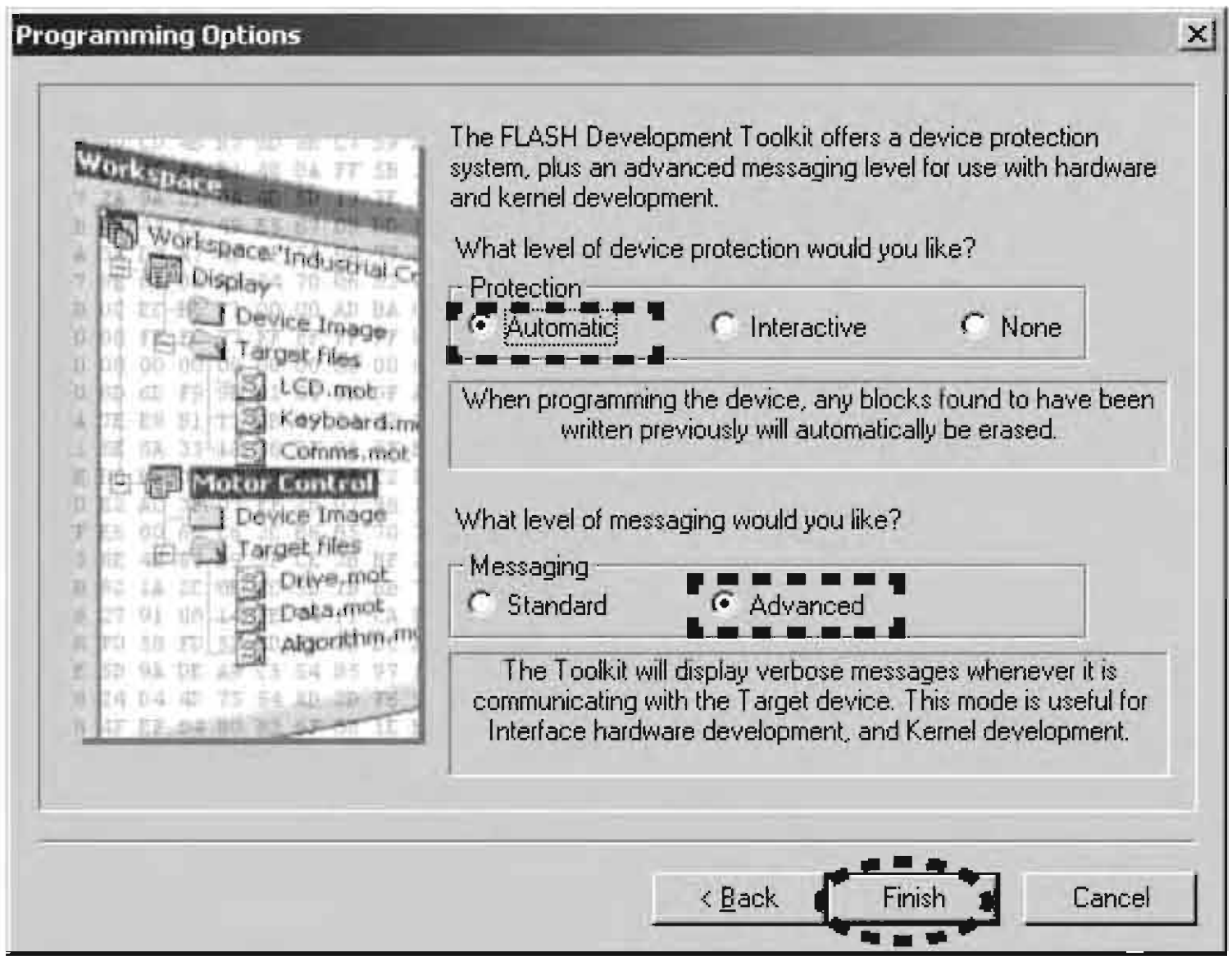
8. Check The **BOOT Mode** in Select Connection.
Un-check the **Use Default**, and choose the **19200** in Recommended Speeds.
Click the **Next**.

8. Select Connectionの**BOOT Mode**をチェックします。
Recommended Speedsの**Use Default**のチェックを外し、**19200**を選択します。
Nextをクリックします。



9. Check the **Automatic** in Protection.
Check the **Advanced** in Messaging.
Click the **Finish**.

9. Protectionの**Automatic**をチェックします。
Messagingの**Advanced**をチェックします。
Finishをクリックします。



[M3-2]Writing Procedure for HDMI CPU

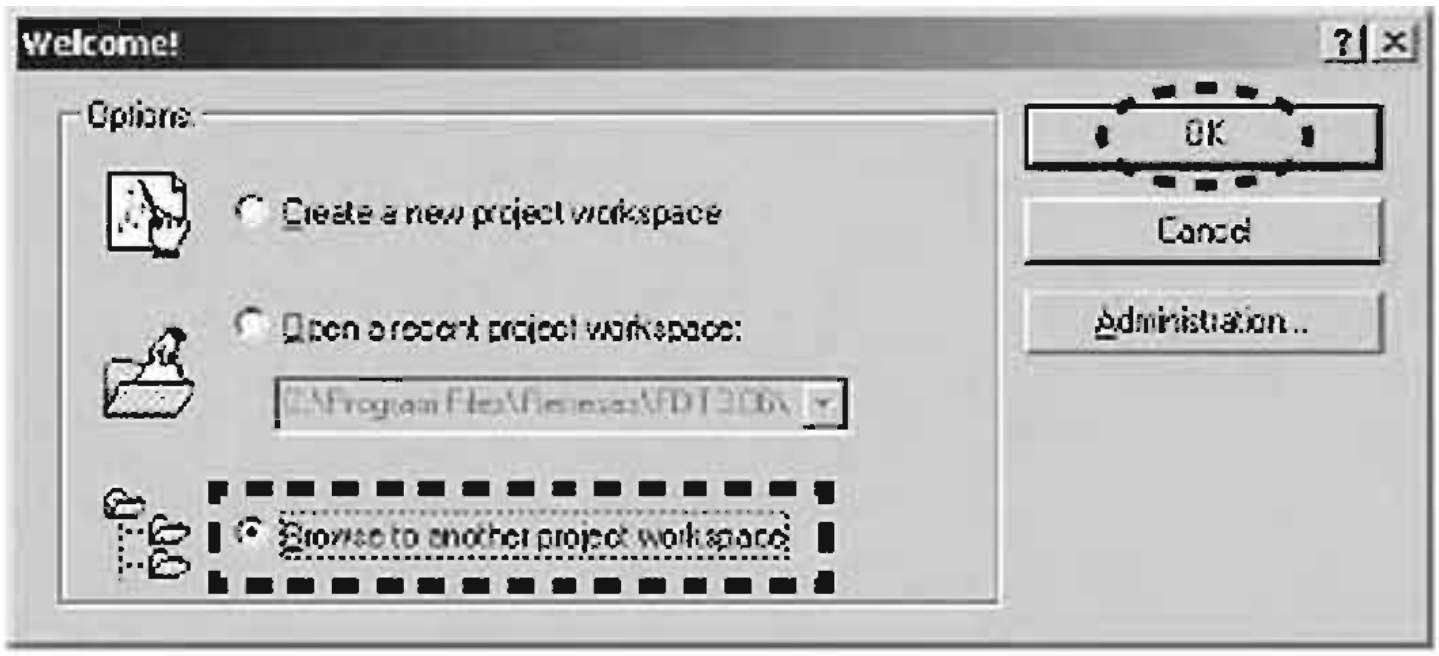
1. Connect the RS-232C on rear panel of the unit and the Serial Port of windows PC with RS-232C cable.
2. Connect the mains cord into the unit.
3. Launch the Flash Development Toolkit (FDT), When FDT is not launch.
   When FDT is already launch, please advance to step No.7.
4. Click Start, Programs, Renesas, Flash Development Toolkit 3.06 and Flash Development Toolkit 3.06.

[M3-2]Writing Procedure for HDMI CPU

1. 本機のリアパネルにあるRS-232CコネクタとWindows PCのSerialポートをRS-232Cケーブルで接続します。
2. 本機に電源コードを接続します。
3. Flash Development Toolkit v3.06(FDT)を起動していない場合は起動します。
   既にFDTを起動している方はステップ7に進んでください。
4. Start, Programs, Renesas, Flash Development Toolkit 3.06, Flash Development Toolkit 3.06をクリックします。

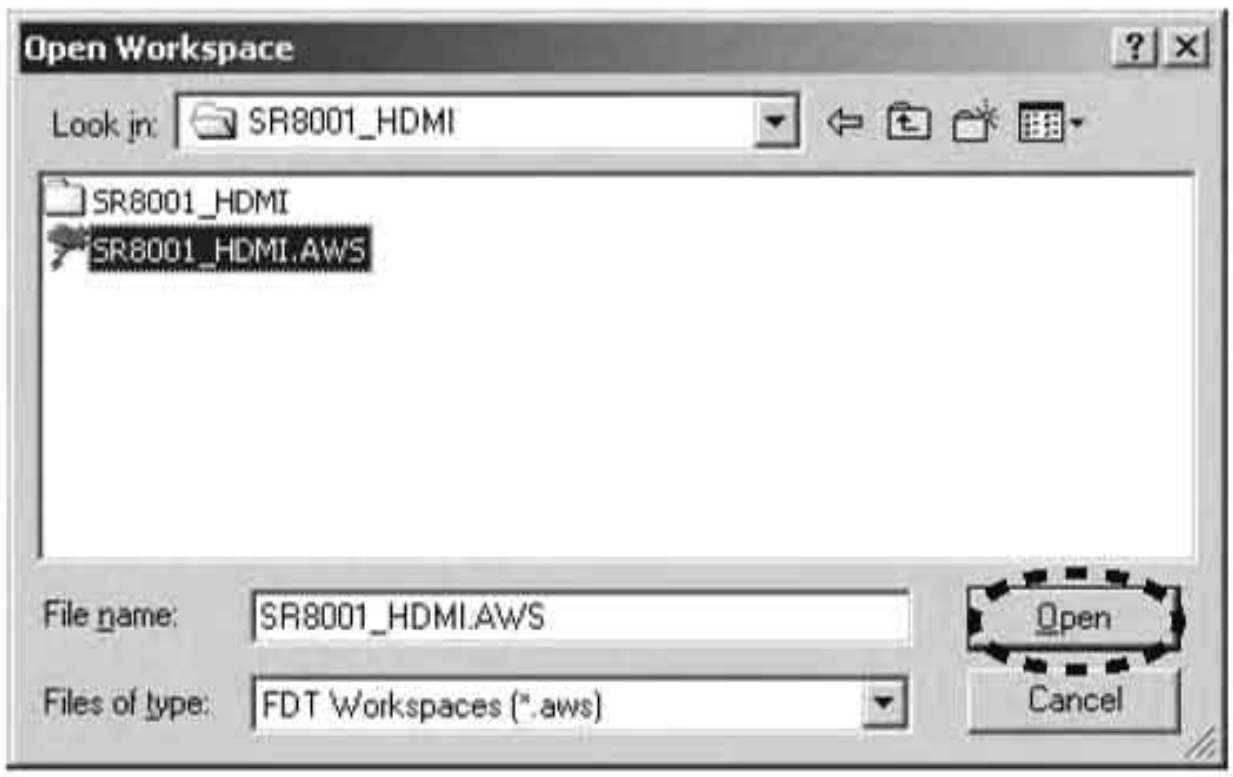
5. Check the Browse to another project workspace, and click OK.

5. Browse to another project workspaceをチェックし、OKをクリックします。



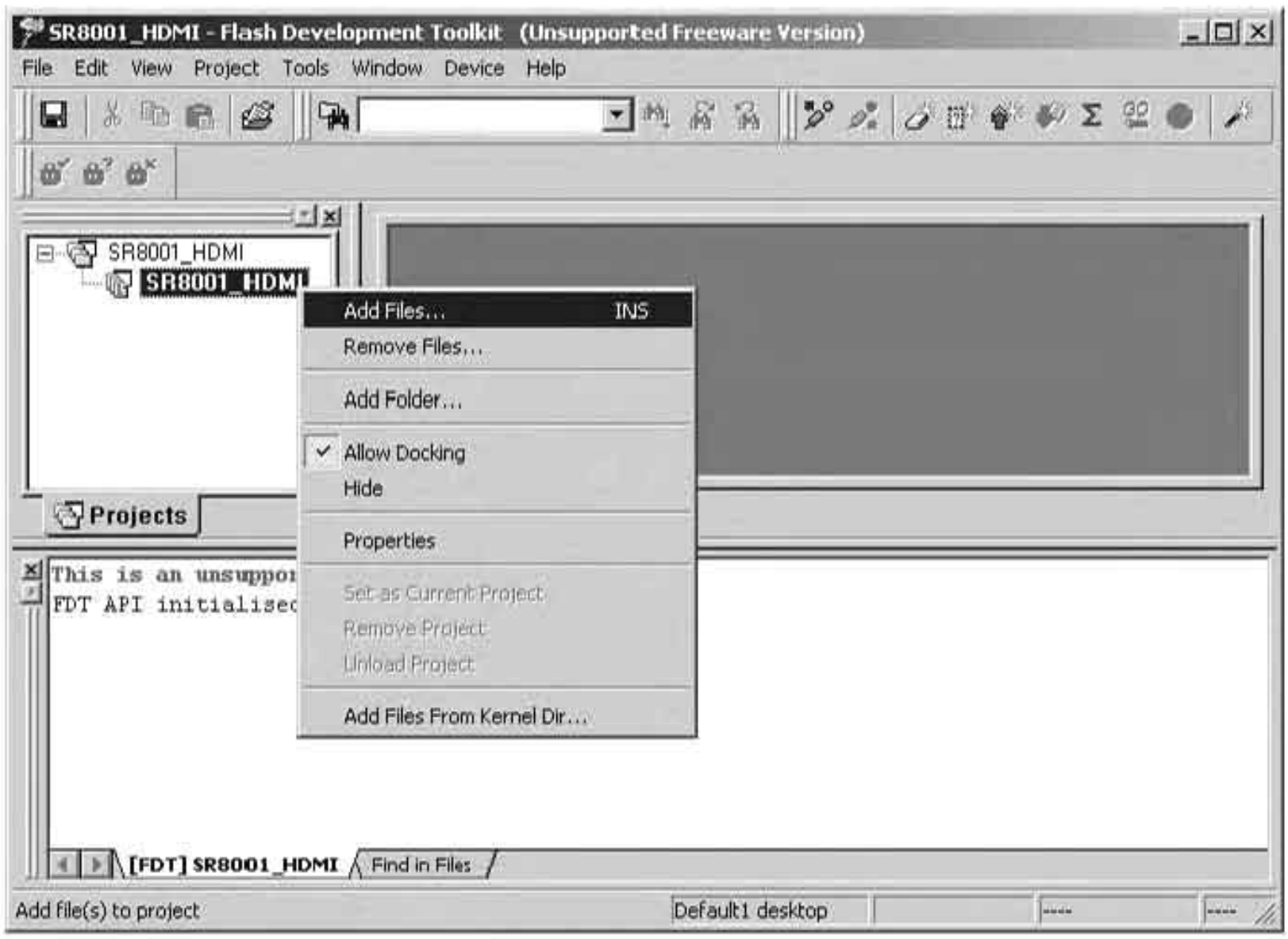
6. Choose **SP8001_HDMI.AWS** in SR8001_HDMI folder under workspase folder. And Click the **Open**.

6. workspaseフォルダの下の**SR8001_HDMI**フォルダ内のSP8001_HDMI.AWSを選択し、**Open**をクリックします。



7. Right button of mouse click on the **SR8001_HDMI**, and select the **Add Files...** in a menu.

7. **SR8001_HDMI**を右クリックし、メニューから**Add Files...**をクリックします。

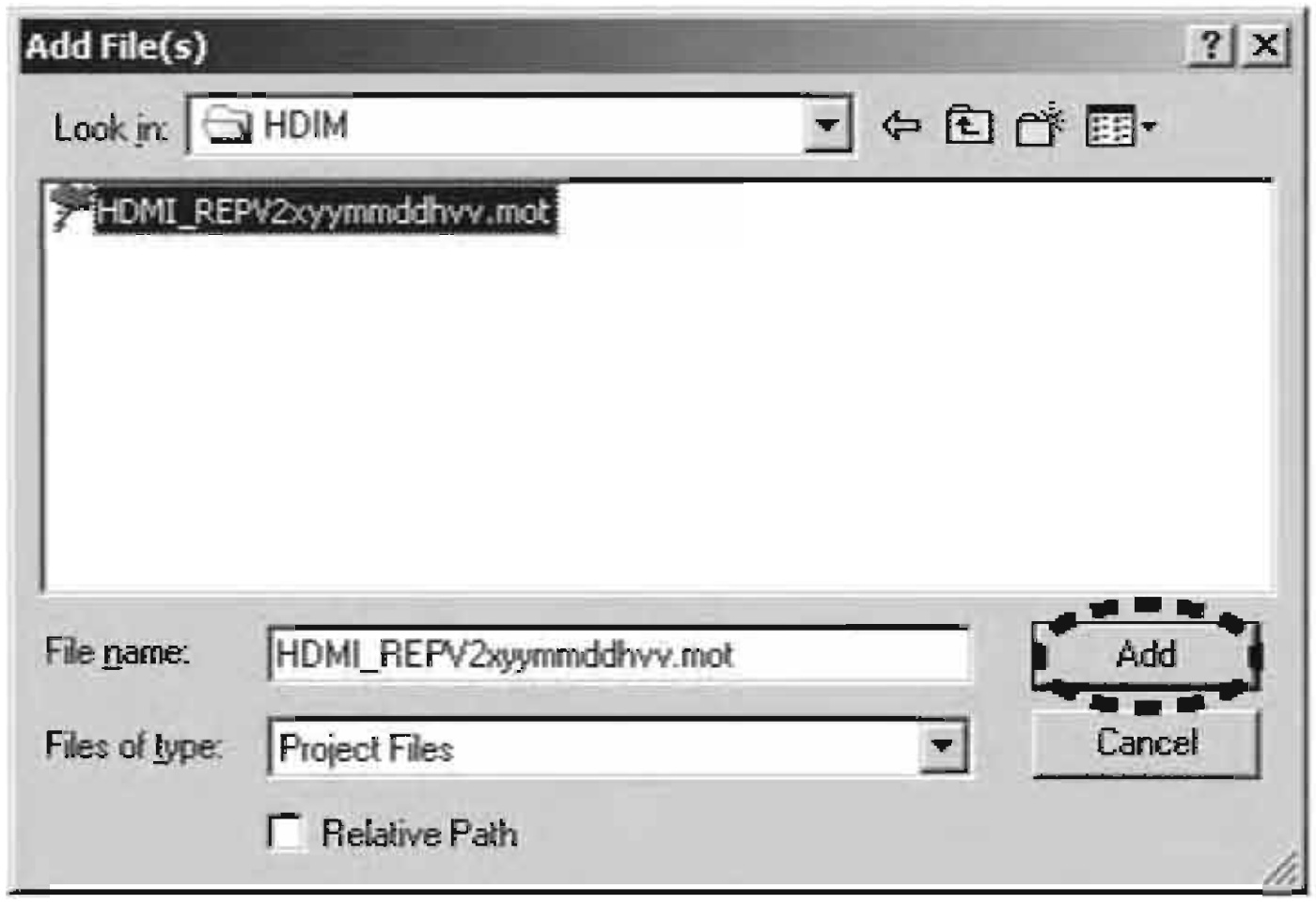


8. Choose the **HDMI_REPV2xyymmddvv.mot**, and click the **Add**.

NOTE : The yy is two digits of year. The mm is month. The dd is date. The vv is release number.

8. **HDMI_REPV2xyymmddvv.mot**を選択し、**Add**をクリックします。

注意: yyは年の下二桁、mmは月、ddは日、vvはリリースナンバー

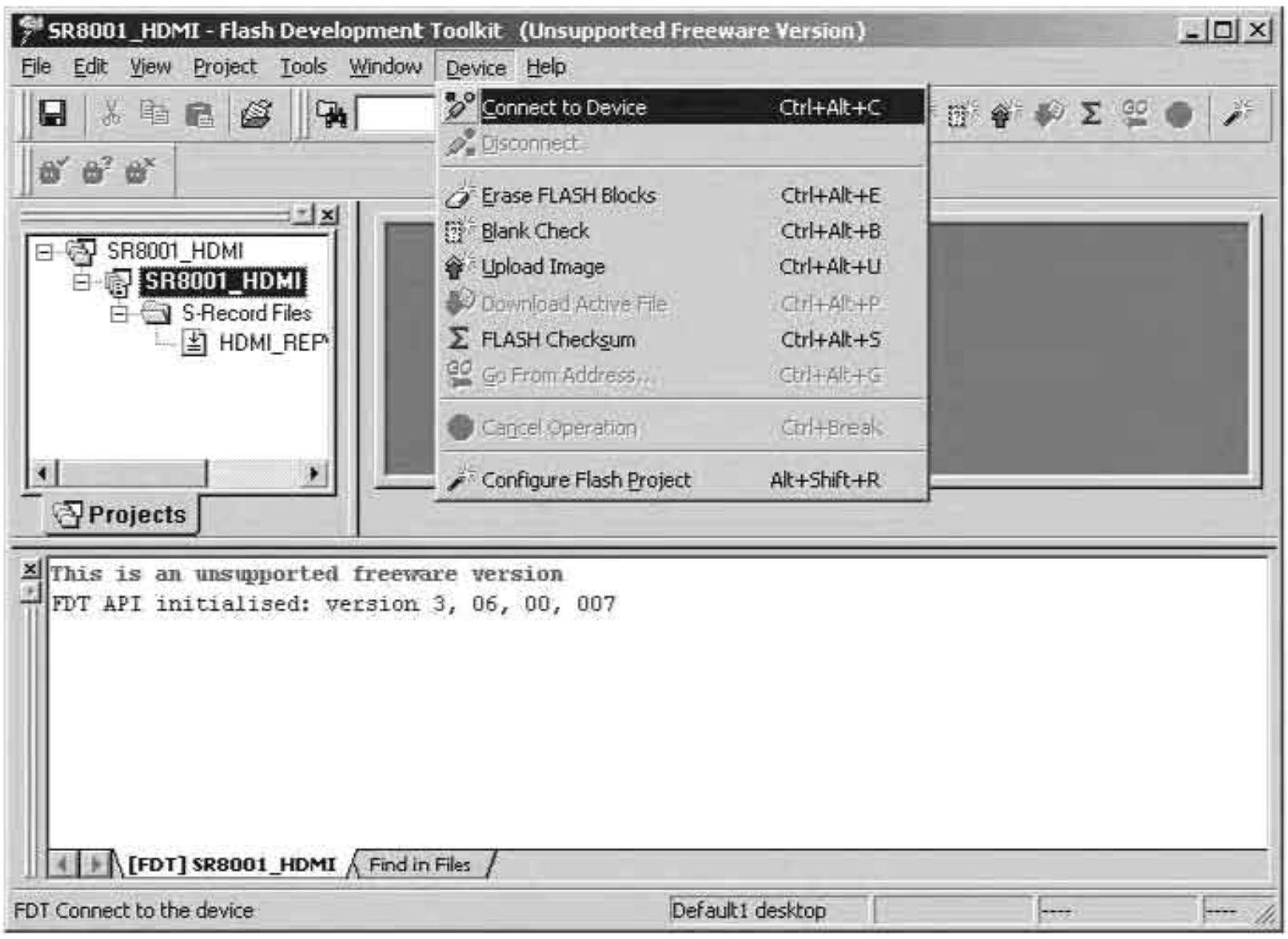


9. Press the **POWER ON/STANDBY** button for turn on the unit.
10. Press the **ENTER, SURROUND MODE** and **T-MODE** buttons simultaneously more than 3 seconds to turn the unit into Loading Mode.
11. The FLD shows "SELECT DSP" after showed "LOADING MODE".
12. Turn the **INPUT SELECTOR** to change display from "SELECT DSP" to "SELECT HDMI" on FLD.
13. Press the **ENTER** button.
14. "SELECTED HDMI" shows on the FLD.

9. **POWER ON/STANDBY**ボタンを押し、本機の電源を入れます。
10. **ENTER, SURROUND MODE, T-MODE**の3つボタンを同時に3秒以上押し続け、本機をローディングモードにします。
11. FLに"LOADING MODE"と表示された後、"SELECT DSP"と表示されます。
12. 本機の**INPUT SELECTOR**を回して、FLの表示が"SELECT DSP"から"SELECT HDMI"に換えます。
13. **ENTER**ボタンを押します。
14. FLの表示が"SELECTED HDMI"に変わります。

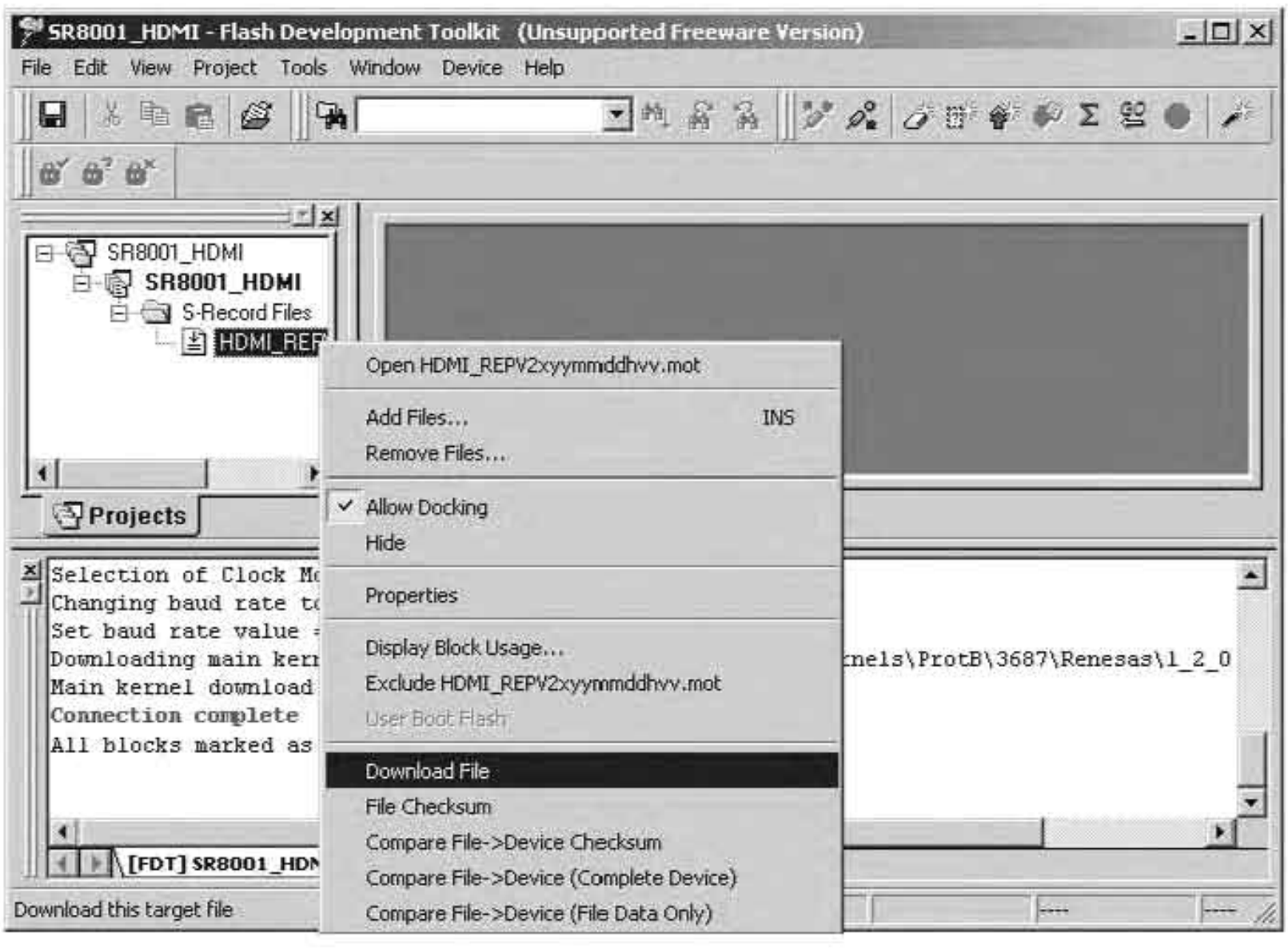
15. Click the **Device** in the menu bar and select the **Connect to Device**.

15. **Device**をクリックし、メニューから**Connect to Device**をクリックします。



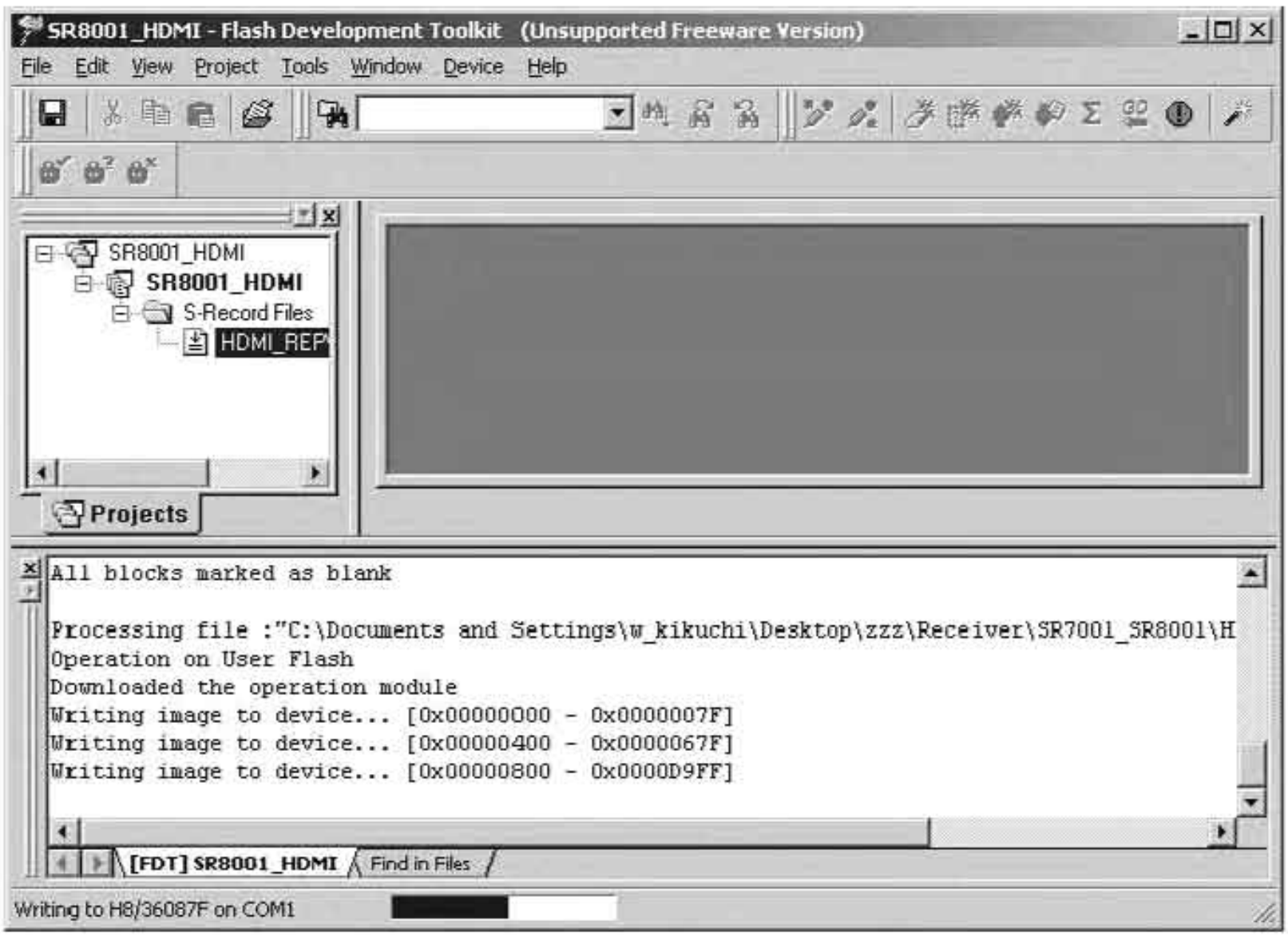
16. Press right button of mouse on the **HDMI_ REPV2xyymmddvv.mot**, and select the **Download File** in a menu.

16. **HDMI_REPV2xyymmddvv.mot**を右クリックし、メニューから**Download File**をクリックします。



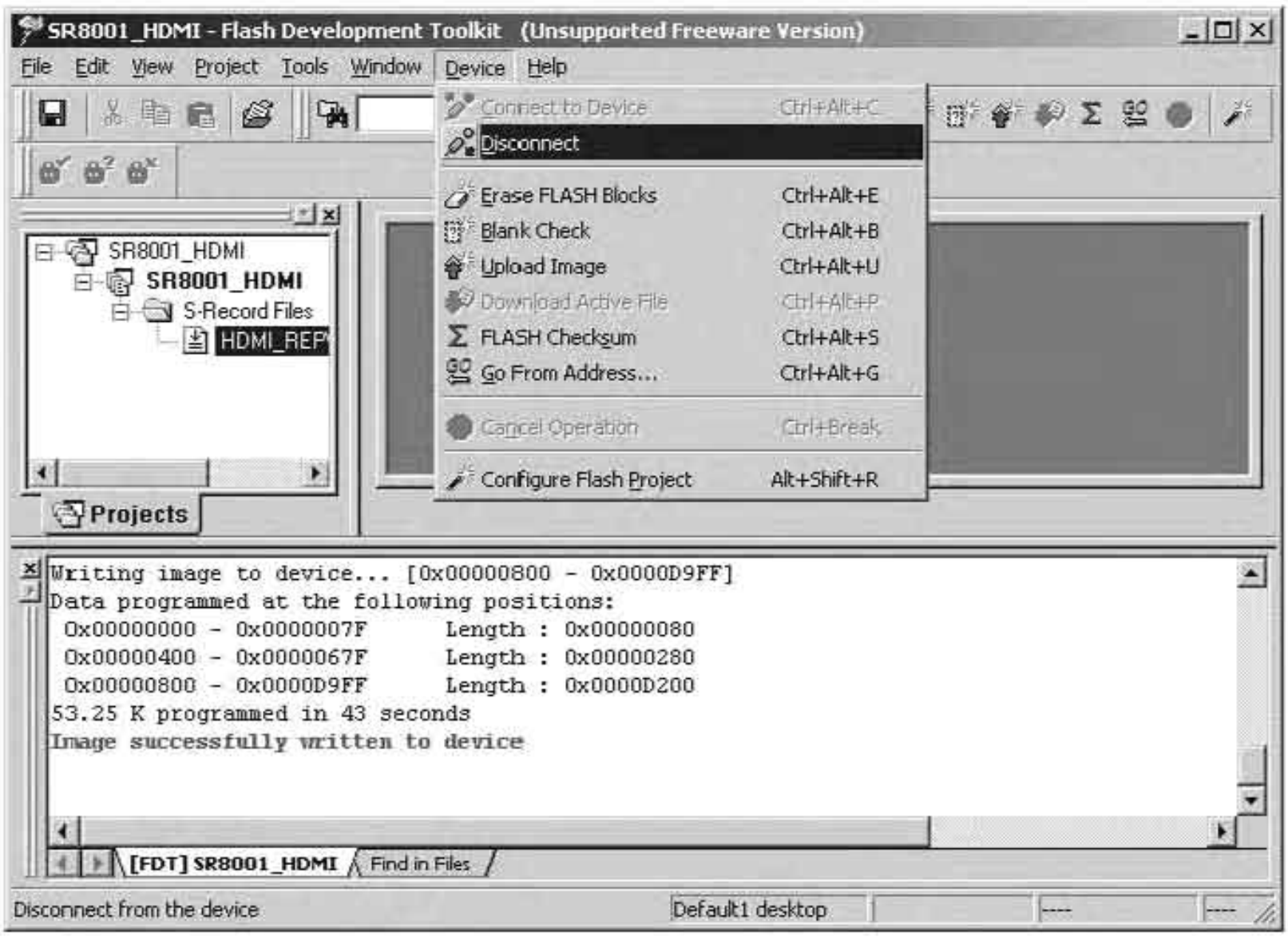
17. Software is written into the HDMI CPU.
The writing of software takes about 45 seconds.

17. ソフトウェアがHDMIマイコンに書き込まれます。
書き込みにかかる時間は約45秒です。



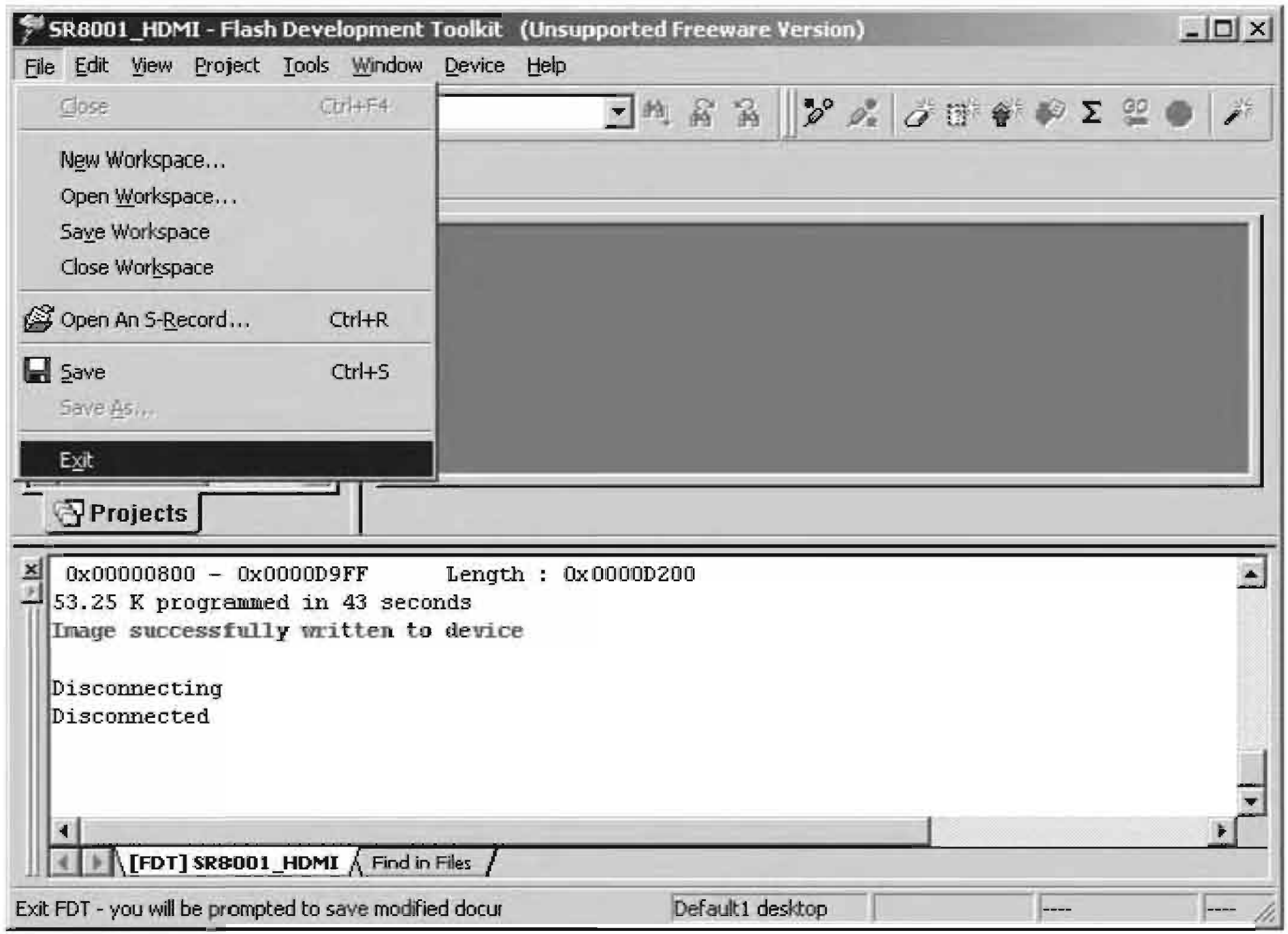
18. Click the **Device** in the menu bar and select the **Disconnect**.

18. **Device**をクリックし、メニューから**Disconnect**をクリックします。



19. Click the **File** and select the **Exit** in menu.

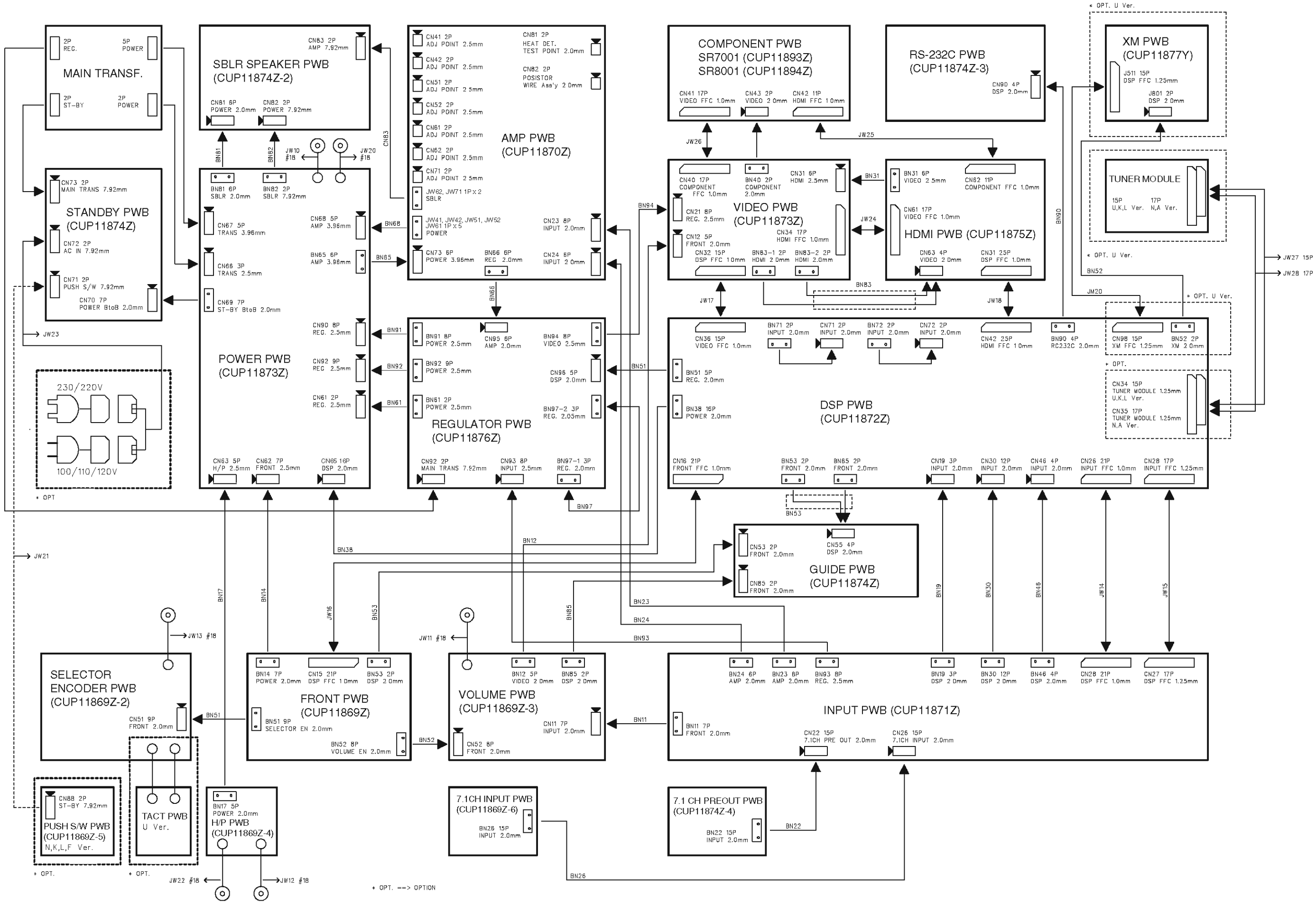
19. **File**をクリックし、メニューから**Exit**をクリックします。



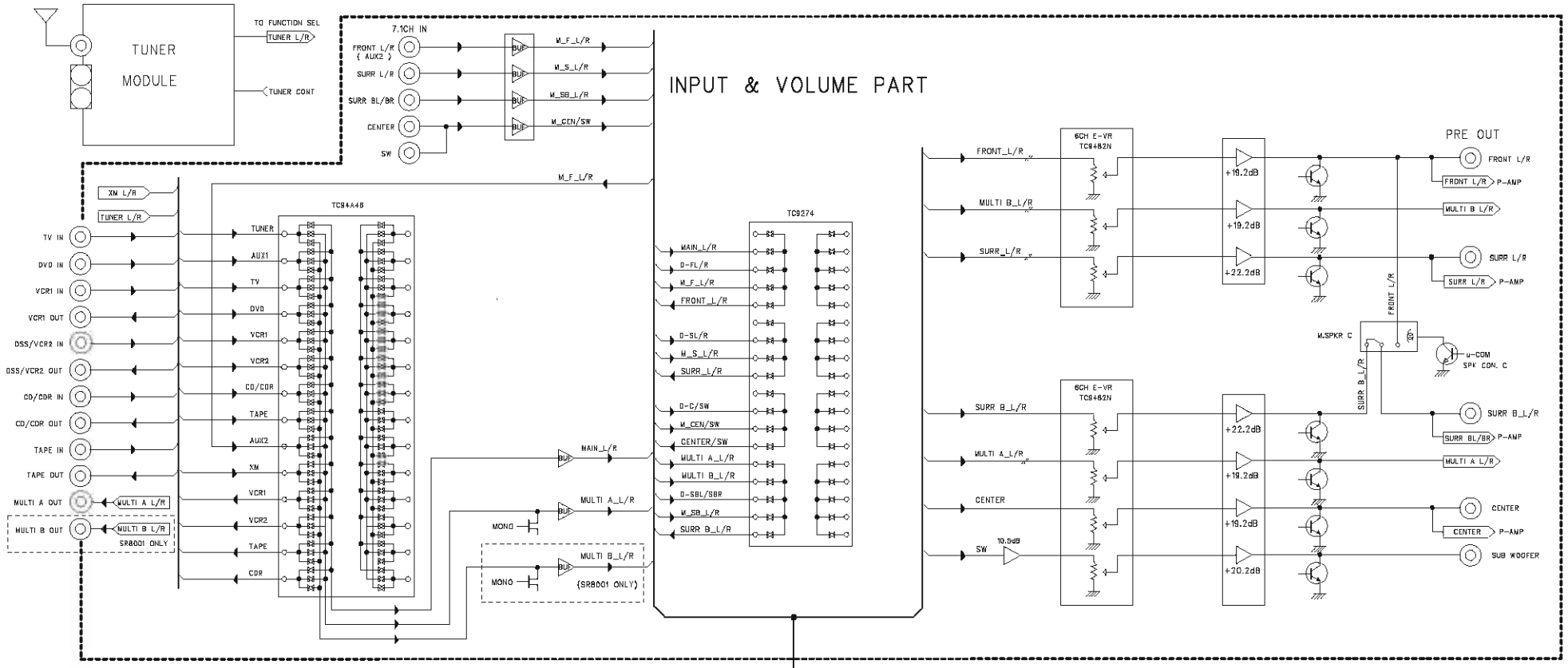
20. Press the **POWER ON/STANDBY** button for turn off the unit.
21. Disconnect the mains cord and RS-232C cable from the unit.

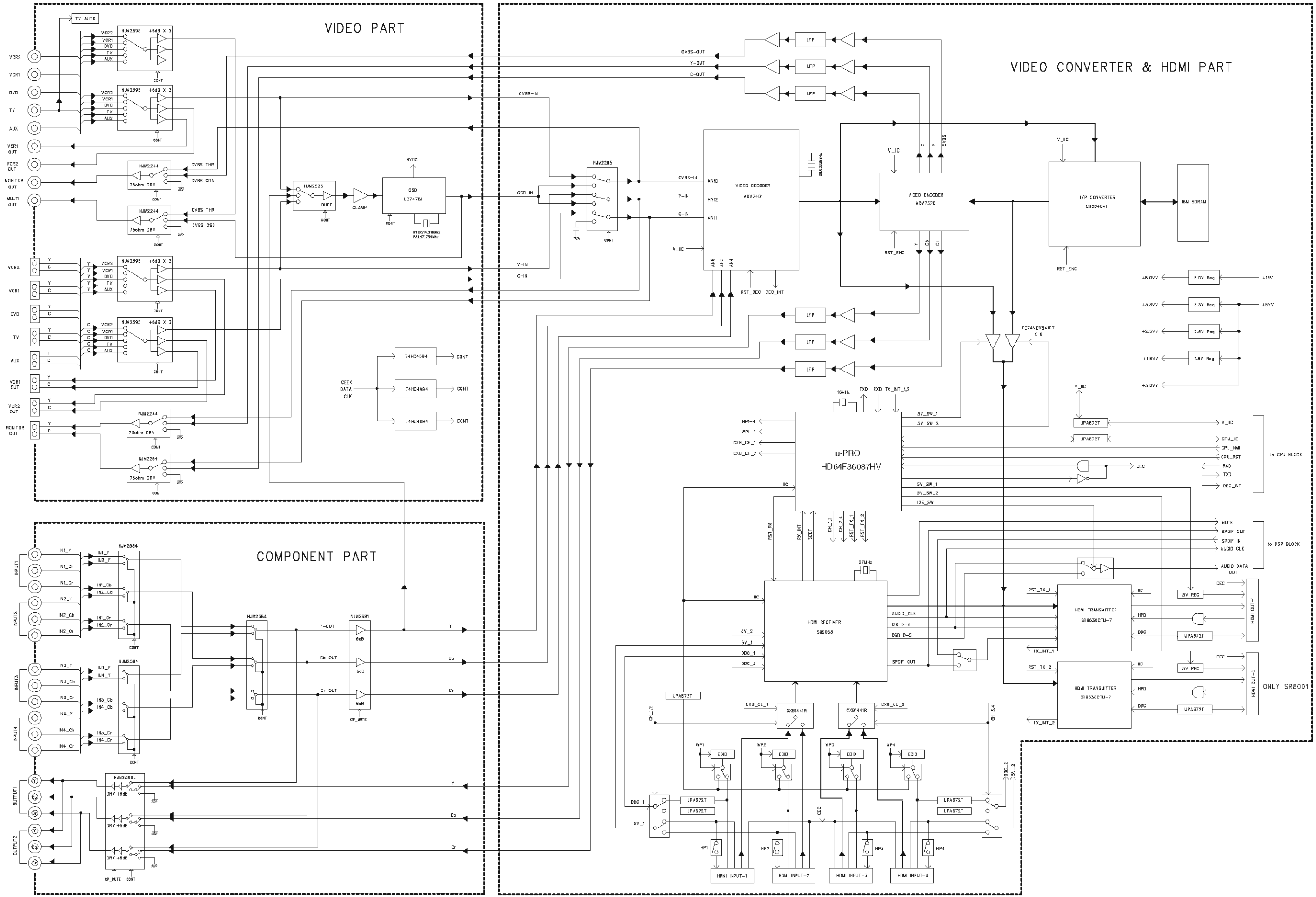
20. **POWER ON/STANDBY**ボタンを押し、本機の電源を切ります。
21. 本機から電源コードとRS-232Cケーブルを外します。

7. WIRING DIAGRAM

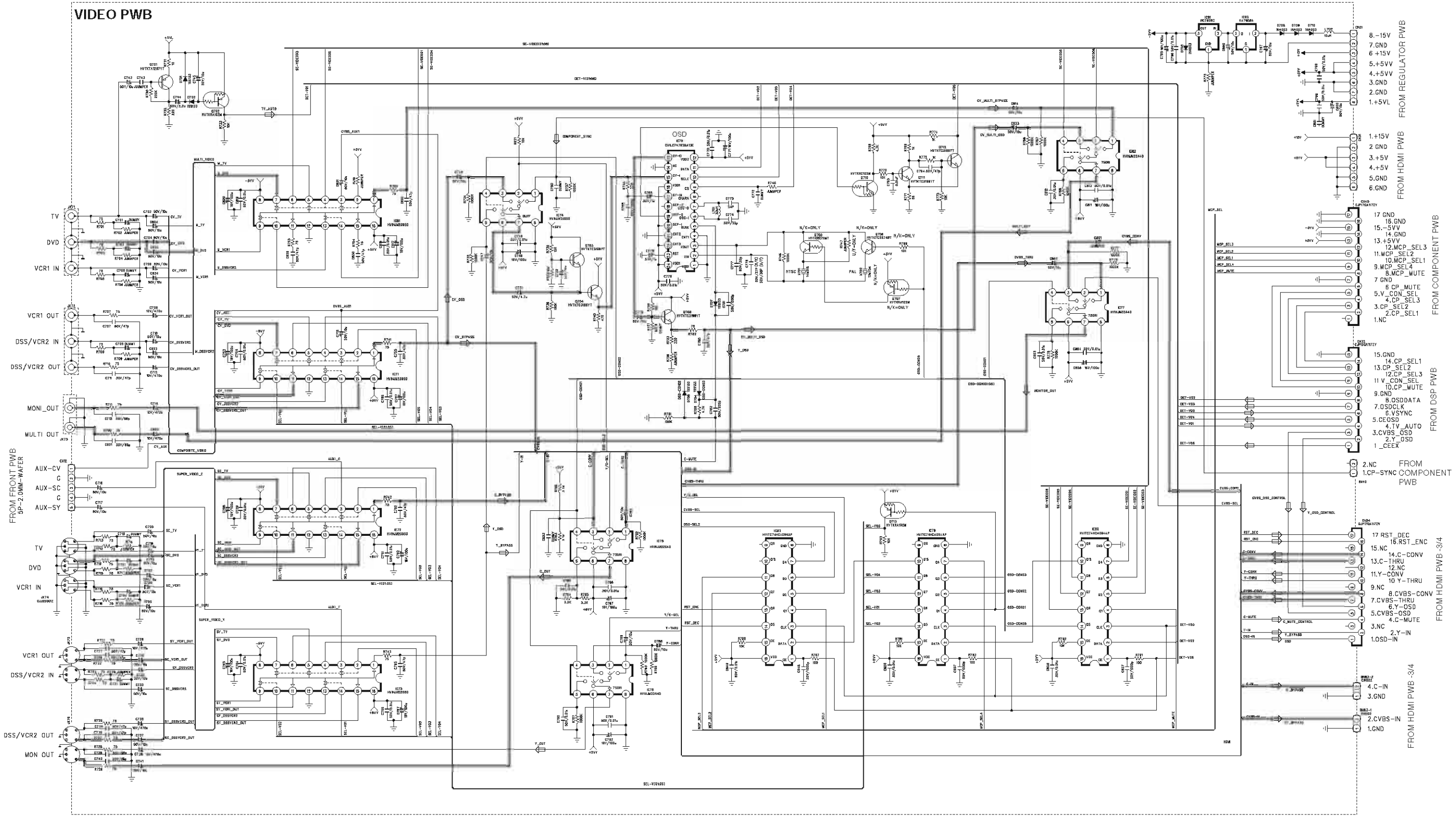


8. BLOCK DIAGRAM



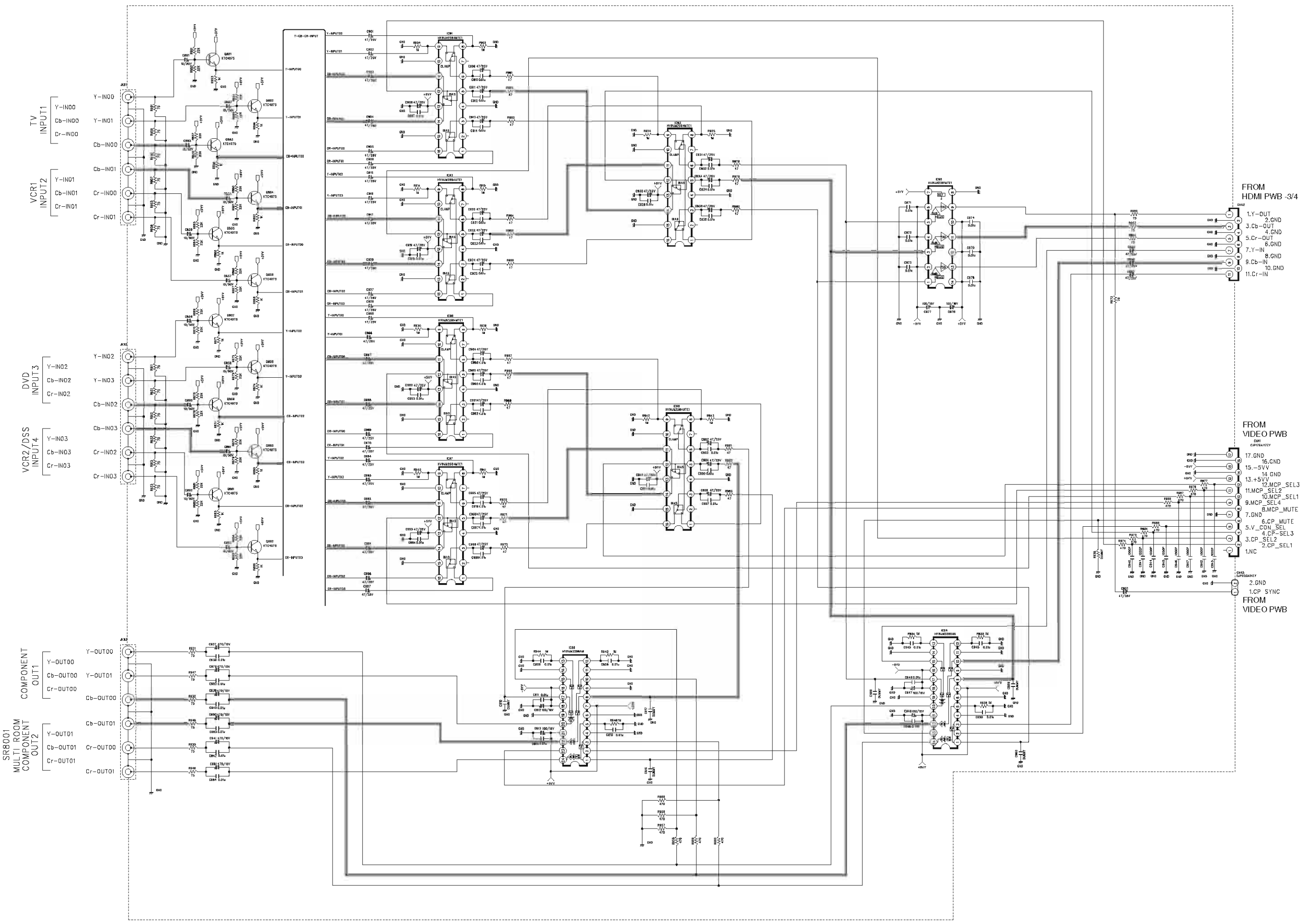

VIDEO PART
VIDEO CONVERTER & HDMI PART
COMPONENT PART
TV AUTO
VCR2
VCR1
DVD
TV
AUX
VCR1 OUT
VCR2 OUT
MONITOR OUT
MULTI OUT
NJM2595
+6dB X 3
CONT
NJM2244
75ohm DRV
CVBS THR
CVBS CON
CVBS OSD
NJM2535
BUFF
CLAMP
SYNC
OSD
LC74781
NTSC/14.318MHz
PAL/17.734MHz
CVBS-IN
Y-IN
C-IN
OSD-IN
NJM2285
CVBS-OUT
Y-OUT
C-OUT
LPF
VIDEO DECODER
ADV7401
AN10
AN12
AN11
AN6
AN5
AN4
V_IIC
RST_DEC
DEC_INT
VIDEO ENCODER
ADV7320
RST_ENC
I/P CONVERTER
CDD040AF
16M SDRAM
TC74VCX541FT
X 6
74HC4094
CEEX
DATA
CLK
u-PRO
HD64F36087HV
16MHz
TXD
RXD
TX_INT_1,2
HP1~4
WP1~4
CXB_CE_1
CXB_CE_2
5V_SW_1
5V_SW_2
I2S_SW
IIC
UPA672T
CEC
CPU_IIC
CPU_NMI
CPU_RST
RXD
TXD
DEC_INT
to CPU BLOCK
MUTE
SPDIF OUT
SPDIF IN
AUDIO CLK
AUDIO DATA OUT
to DSP BLOCK
RST_RV
RX_INT
SDDT
CH_1,2
CH_3,4
RST_TX_1
RST_TX_2
27MHz
HDMI RECEIVER
SII9033
AUDIO_CLK
I2S 0~3
DSD 0~5
SPDIF OUT
HDMI TRANSMITTER
SII9030CTU-7
5V REG
HDMI OUT-1
HDMI OUT-2
ONLY SR8001
TX_INT_1
TX_INT_2
CXB1441R
EDID
WP1
WP2
WP3
WP4
HP1
HP2
HP3
HP4
HDMI INPUT-1
HDMI INPUT-2
HDMI INPUT-3
HDMI INPUT-4
8.0V Reg
3.3V Reg
2.5V Reg
1.8V Reg
+15V
+5VV
+8.0VV
+3.3VV
+2.5VV
+1.8VV
+5.0VV
NJM2584
NJM2581
NJM2588L
DRV +6dB
6dB
CP_MUTE
INPUT1
INPUT2
INPUT3
INPUT4
OUTPUT1
OUTPUT2
IN1_Y
IN1_Cb
IN1_Cr
IN2_Y
IN2_Cb
IN2_Cr
IN3_Y
IN3_Cb
IN3_Cr
IN4_Y
IN4_Cb
IN4_Cr
Y-OUT
Cb-OUT
Cr-OUT

9. SCHEMATIC DIAGRAM



VERSION OPTION TABLE					
		N (EUR)	U (USA)	K (CHINA)	F (JAPAN)
C777	LOAD CAP	30p	30p	30p	30p
C778	LOAD CAP	27p	30p	27p	30p
Q705	KRC111M	○	×	○	×
Q706	KRC111M	○	×	○	×
Q707	KRA102M	○	×	○	×
R747	JUMPER	×	○	×	○
X702	17.7344MHz	○	×	○	×

COMPONENT PWB



HDMI PWB -1/4

INPUT-4

INPUT-3

INPUT-2

INPUT-1

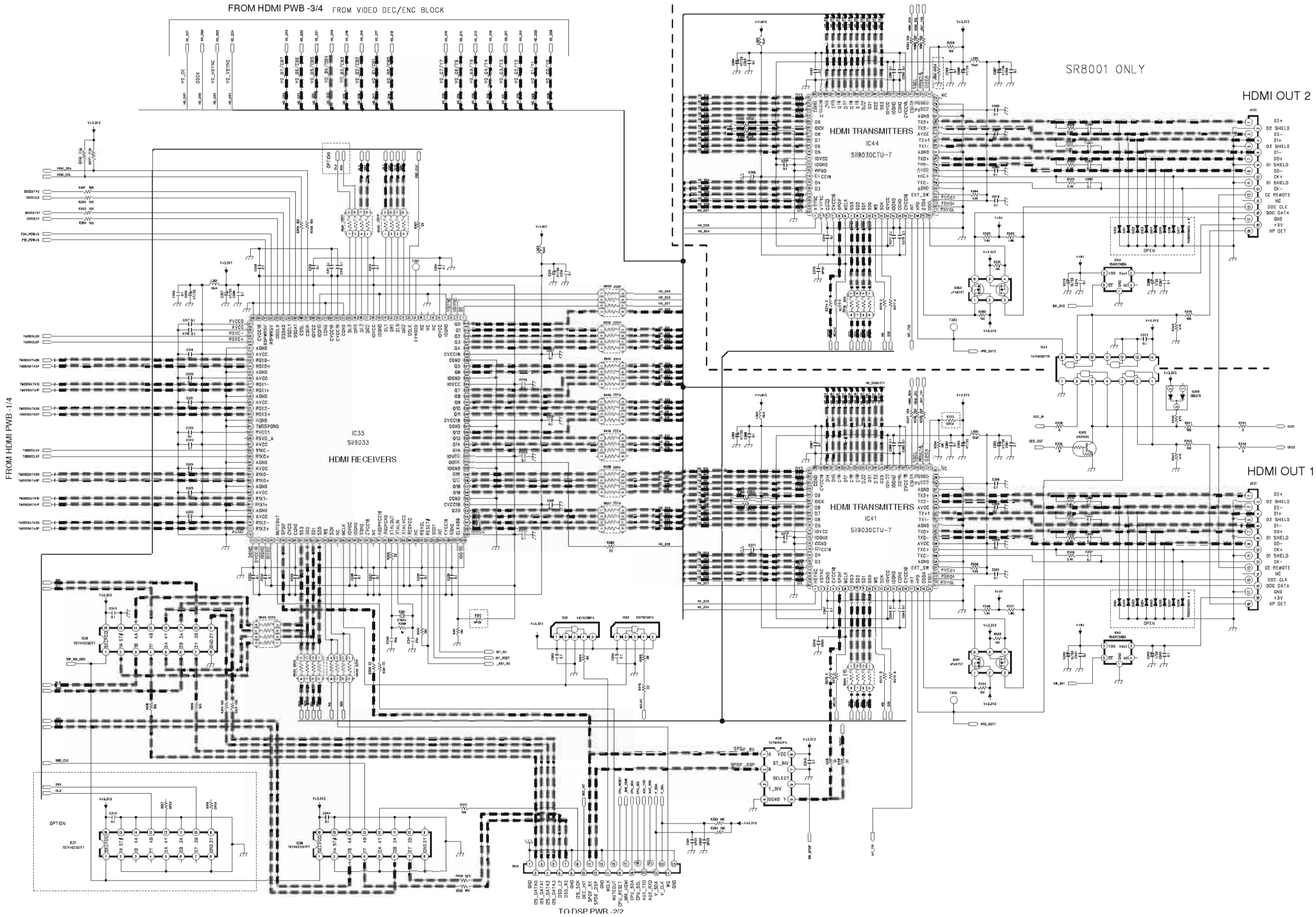
IC22
CXB1441R
Cable Equalizer with 2-system Switching Function

IC19
CXB1441R
Cable Equalizer with 2-system Switching Function

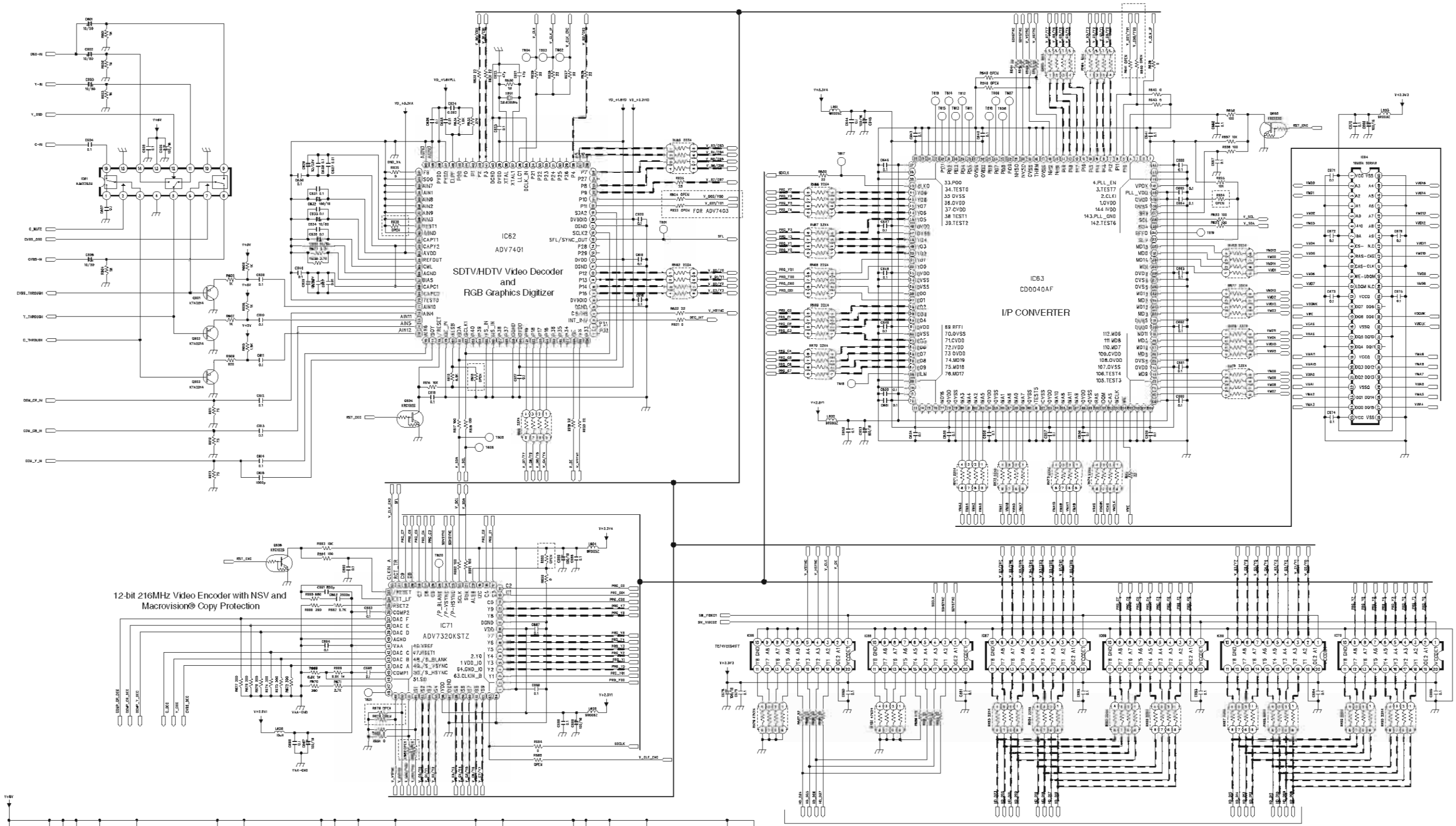
TO HDMI PWB -2/4

TO HDMI PWB -2/4

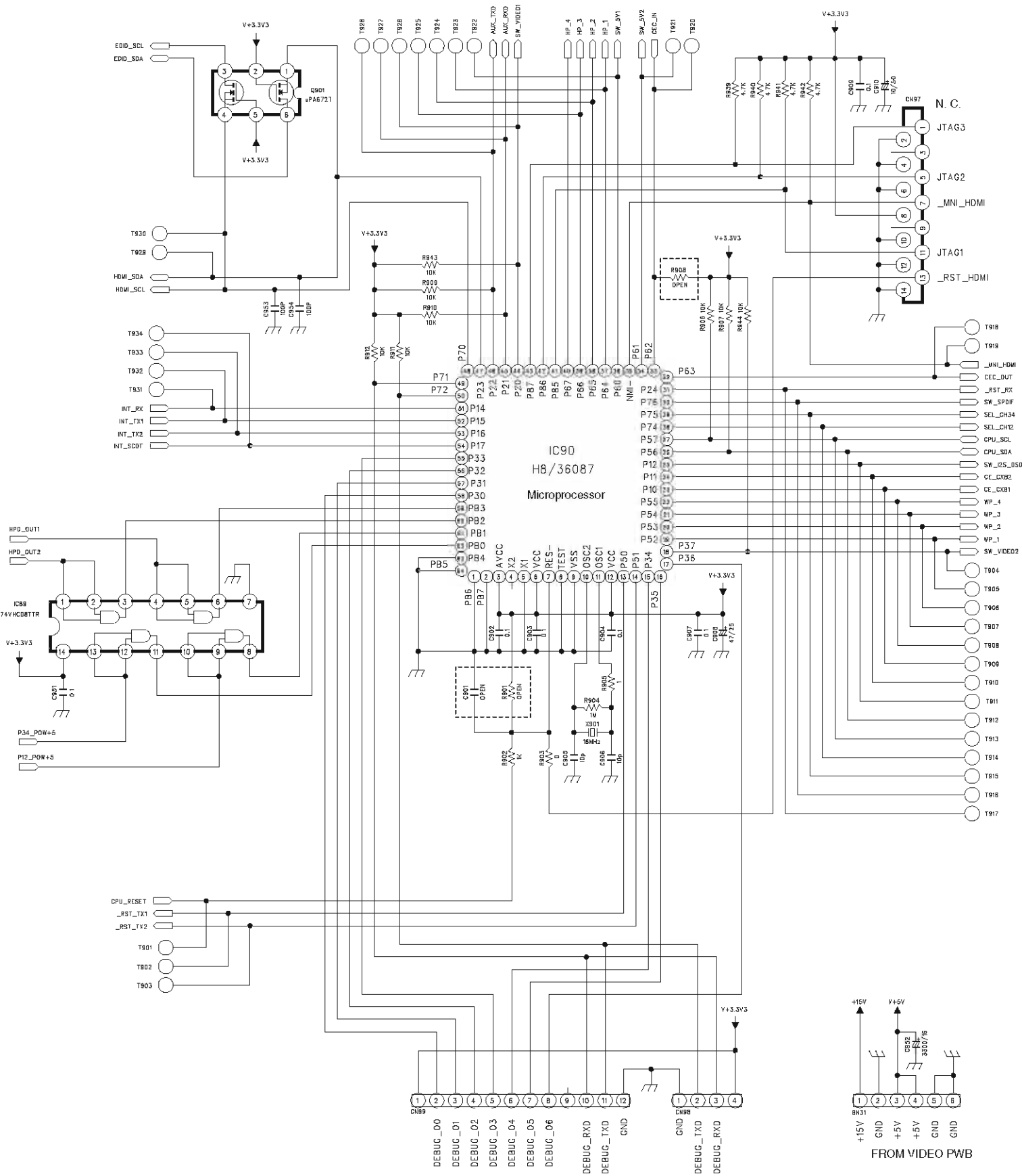
HDMI PWB -2/4

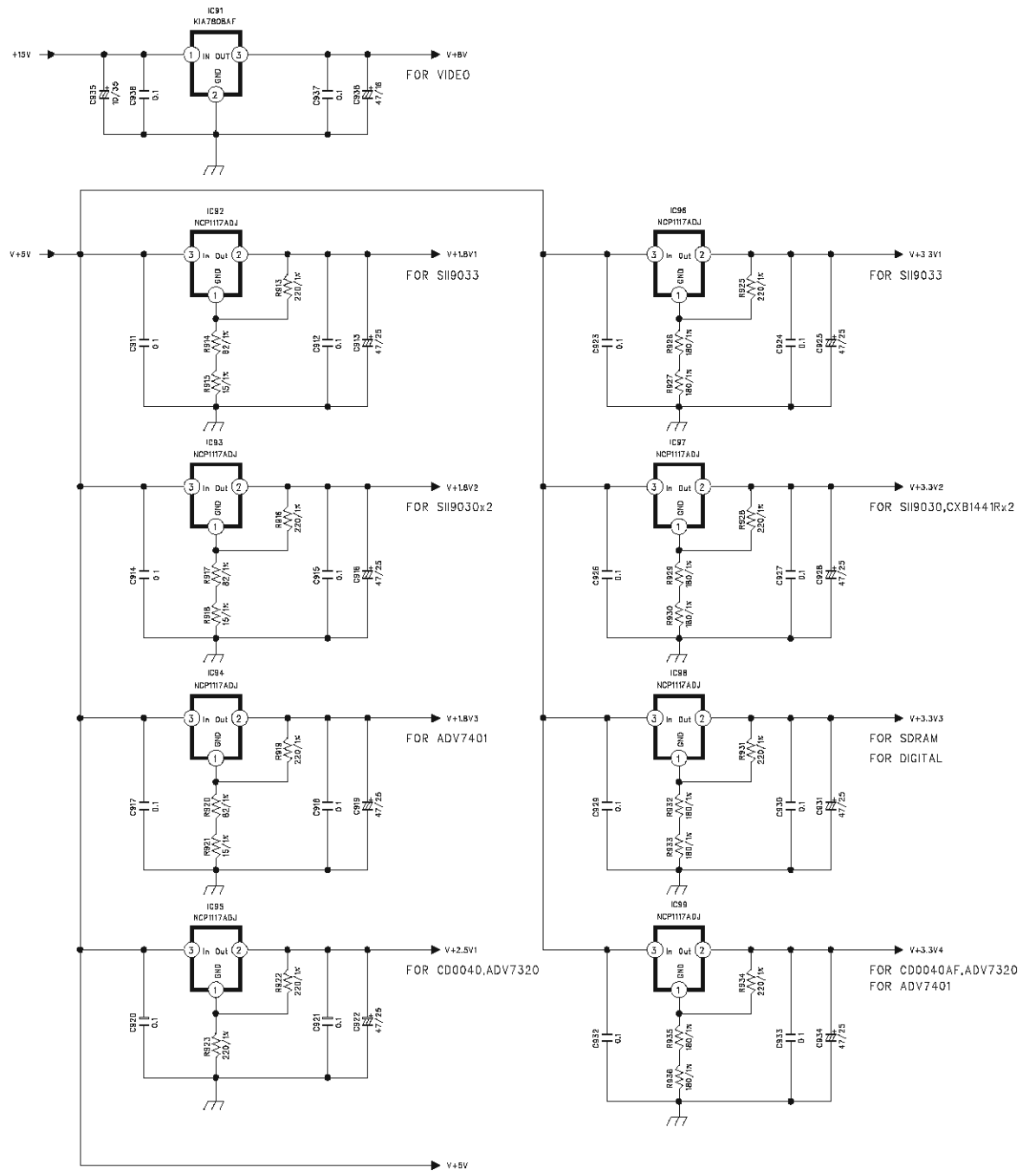

FROM HDMI PWB -3/4
FROM VIDEO DEC/ENC BLOCK
SR8001 ONLY
HDMI OUT 2
HDMI TRANSMITTERS
IC44
SII9030CTU-7
HDMI RECEIVERS
IC35
SII9033
HDMI TRANSMITTERS
IC41
SII9030CTU-7
HDMI OUT 1
OPTION
OPEN
FROM HDMI PWB -1/4
TO DSP PWB -2/2

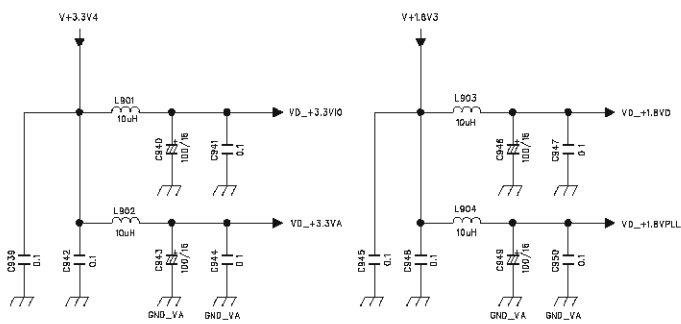
HDMI PWB -3/4

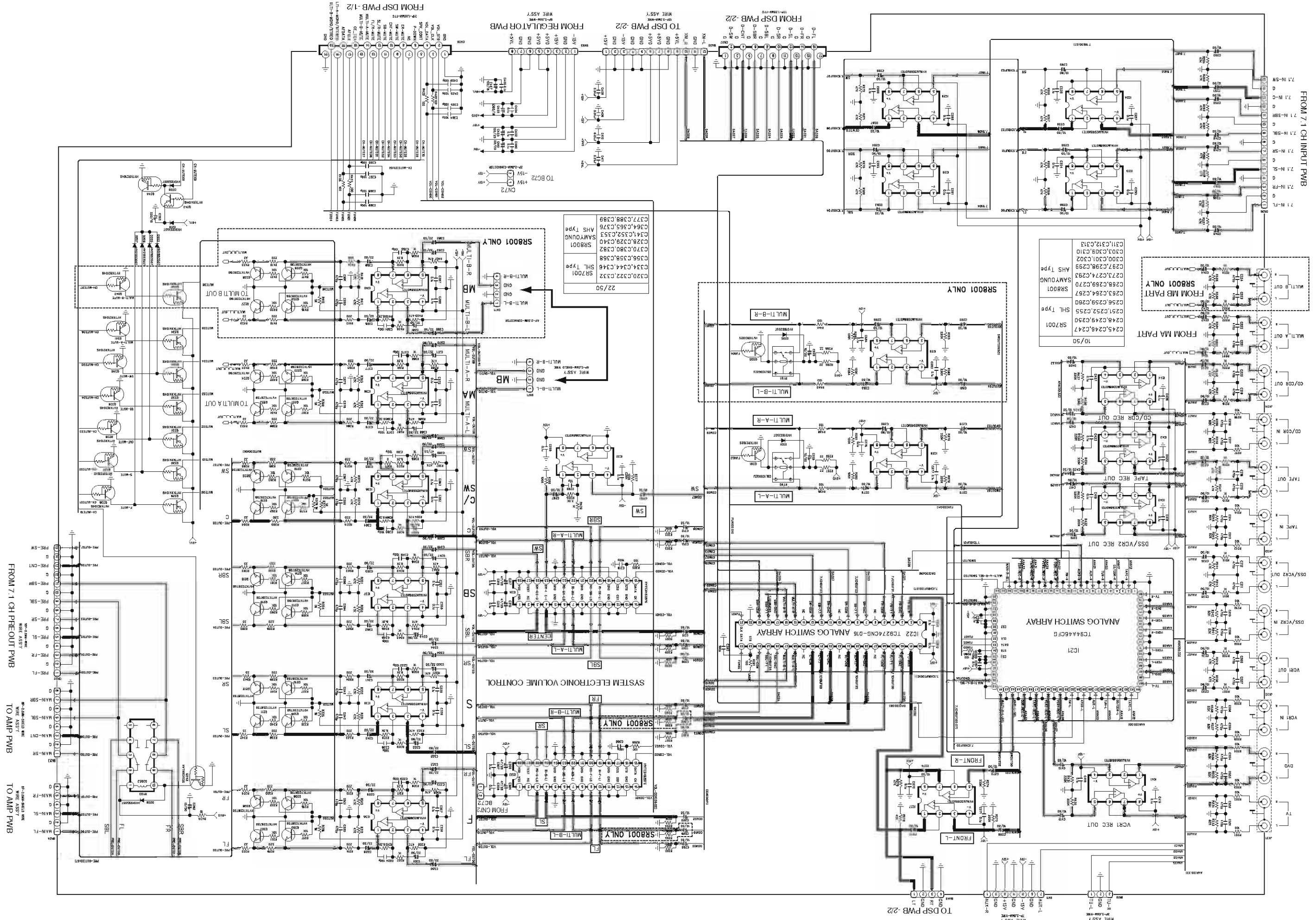

IC62
ADV7401
SDTV/HDTV Video Decoder
and
RGB Graphics Digitizer
IC63
CD0040AF
I/P CONVERTER
12-bit 216MHz Video Encoder with NSV and
Macrovision® Copy Protection
IC71
ADV7320KSTZ
TO HDMI PWB -2/4 TO HDMI-RX,TX BLOCK
TO VIDEO PWB
TO VIDEO PWB
TO COMPONENT PWB

HDMI PWB -4/4

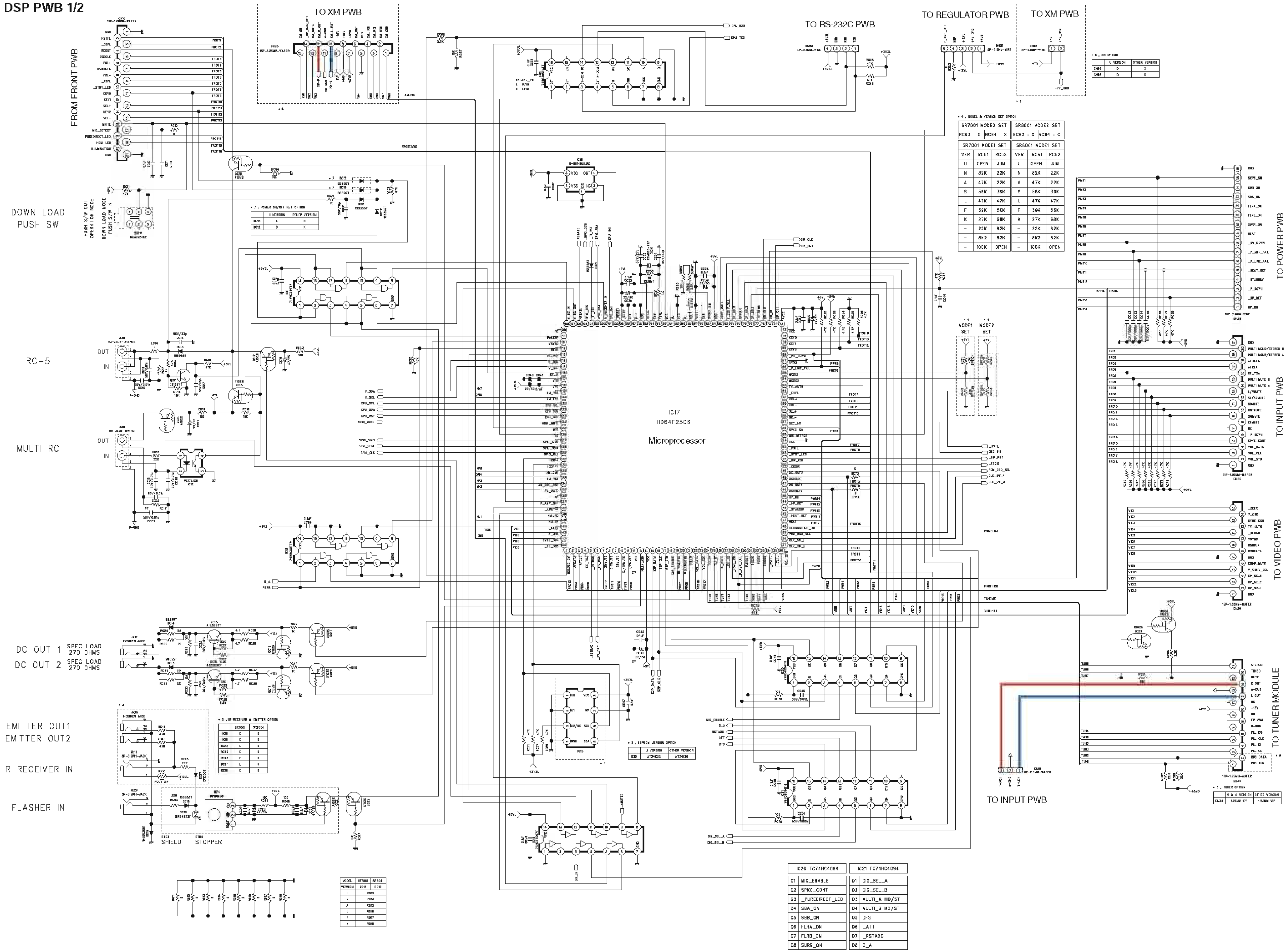

IC90
H8/36087
Microprocessor
Q901
UPA672T
IC89
74VHC08TTR
CN97
N. C.
JTAG3
JTAG2
_MNI_HDMI
JTAG1
_RST_HDMI
CN89
CN98
FROM VIDEO PWB
DEBUG_O0
DEBUG_O1
DEBUG_O2
DEBUG_O3
DEBUG_O4
DEBUG_O5
DEBUG_O6
DEBUG_RXD
DEBUG_TXD
GND
DEBUG_TXD
DEBUG_RXD


IC91
KIA78D8AF
FOR VIDEO
IC92
NCP1117ADJ
FOR SII9033
IC93
NCP1117ADJ
FOR SII9030x2
IC94
NCP1117ADJ
FOR ADV7401
IC95
NCP1117ADJ
FOR CD0040,ADV7320
IC96
NCP1117ADJ
FOR SII9033
IC97
NCP1117ADJ
FOR SII9030,CXB1441Rx2
IC98
NCP1117ADJ
FOR SDRAM
FOR DIGITAL
IC99
NCP1117ADJ
FOR CD0040AF,ADV7320
FOR ADV7401

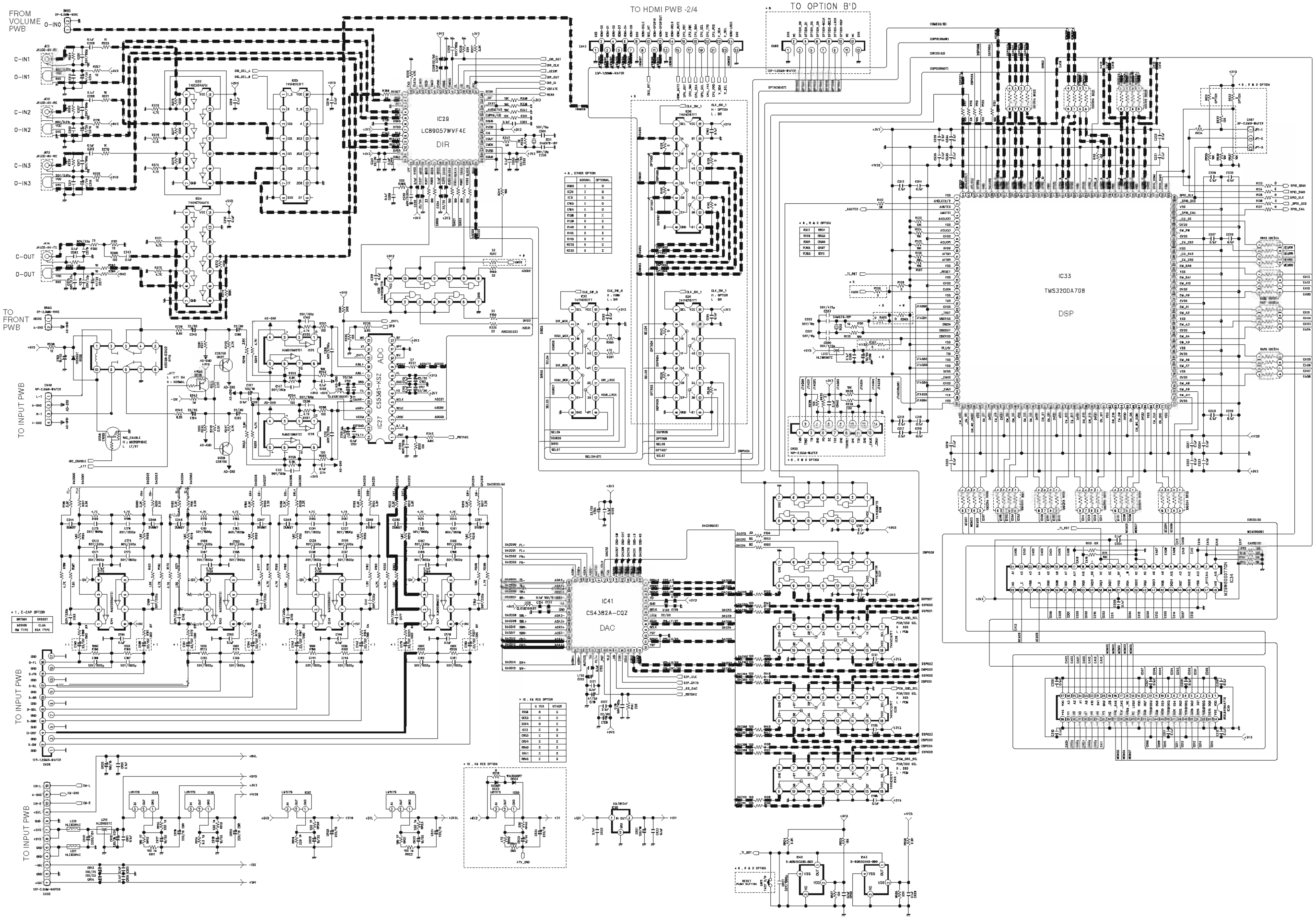

L901
10uH
L902
10uH
L903
10uH
L904
10uH
GND_VA


INPUT PWB
FROM 7.1 CH INPUT PWB
7.1 IN-FL
7.1 IN-FR
7.1 IN-SL
7.1 IN-SR
7.1 IN-SBL
7.1 IN-SBR
7.1 IN-C
7.1 IN-SW
FROM MB PART
SR8001 ONLY
FROM MA PART
SR8001 ONLY
SR7001 SHL Type
C247,C248,C249,C250
C251,C252,C255
C256,C259,C260
C263,C264,C267
C268,C269,C270
SR8001 SAWVOUNG AHS Type
C273,C274,C293
C297,C298,C299
C300,C301,C302
C303,C309,C310
C311,C312,C313
10/50
SR7001 SHL Type
C320,C322,C332
C334,C344,C346
C356,C358,C368
C370,C380,C382
C376,C378,C379
SR8001 SAWVOUNG AHS Type
C377,C388,C389
22/50
SR8001 ONLY
MULT-B-L
MULT-A-L
MULT-A-R
MULT-B-R
MB
MA
C/SW
SBR
SB
SBL
S
FR
FL
F
TO MULT B OUT
TO MULT A OUT
SYSTEM ELECTRONIC VOLUME CONTROL
CENTER
SW
FROM DSP PWB -1/2
FROM RE GLATOR PWB
TO DSP PWB -2/2
FROM DSP PWB -2/2
CN72
+15V
-15V
TO BC72
FROM BC72
CN72
ANALOG SWITCH ARRAY
IC21
TC9444CFG
IC22 TC9227ACNG-015 ANALOG SWITCH ARRAY
FRONT-R
FRONT-L
FROM FRONT PWB
TO DSP PWB -2/2
FROM DSP PWB -1/2
CD/CDR REC OUT
CD/CDR IN
TAPE REC OUT
TAPE OUT
TAPE IN
DSS/VCR2 REC OUT
DSS/VCR2 IN
VCR1 OUT
VCR1 IN
DVD
TV
VCR1 REC OUT
FROM PRE-OUT PWB
TO AMP PWB
TO AMP PWB
MAIN-FL
MAIN-FR
MAIN-SL
MAIN-SR
MAIN-SBL
MAIN-SBR
MAIN-CNT
PRE-FL
PRE-FR
PRE-SL
PRE-SR
PRE-SBL
PRE-SBR
PRE-CNT
PRE-SW

DSP PWB 1/2


FROM FRONT PWB
TO XM PWB
TO RS-232C PWB
TO REGULATOR PWB
TO XM PWB
DOWN LOAD PUSH SW
PUSH S/W OUT OPERATION MODE
DOWN LOAD MODE PUSH S/W IN
RC-5
OUT
IN
MULTI RC
OUT
IN
DC OUT 1 SPEC LOAD 270 OHMS
DC OUT 2 SPEC LOAD 270 OHMS
EMITTER OUT1
EMITTER OUT2
IR RECEIVER IN
FLASHER IN
SHIELD
STOPPER
IC17
HD64F2506
Microprocessor
MODE1 SET
MODE2 SET
TO POWER PWB
TO INPUT PWB
TO VIDEO PWB
TO TUNER MODULE
TO INPUT PWB
SR7001 MODE2 SET
RC63 O RC64 X
SR8001 MODE2 SET
RC63 : X RC64 : O
SR7001 MODE1 SET
VER RC61 RC62
U OPEN JUM
N 82K 22K
A 47K 22K
S 56K 39K
L 47K 47K
F 39K 56K
K 27K 68K
– 22K 82K
– 8K2 82K
– 100K OPEN
SR8001 MODE1 SET
VER RC61 RC62
U OPEN JUM
N 82K 22K
A 47K 22K
S 56K 39K
L 47K 47K
F 39K 56K
K 27K 68K
– 22K 82K
– 8K2 82K
– 100K OPEN
IC20 TC74HC4094
Q1 MIC_ENABLE
Q2 SPKC_CONT
Q3 _PUREDIRECT_LED
Q4 SBA_ON
Q5 SBB_ON
Q6 FLRA_ON
Q7 FLRB_ON
Q8 SURR_ON
IC21 TC74HC4094
Q1 DIG_SEL_A
Q2 DIG_SEL_B
Q3 MULTI_A MO/ST
Q4 MULTI_B MO/ST
Q5 DFS
Q6 _ATT
Q7 _RSTADC
Q8 D_A

DSP PWB 2/2


FROM VOLUME PWB
TO HDMI PWB -2/4
TO OPTION B'D
TO FRONT PWB
TO INPUT PWB
IC29
LC89057WVF4E
DIR
IC27
CS5361-KSZ
ADC
IC33
TMS320DA708
DSP
IC41
CS4382A-CQZ
DAC
C-IN1
D-IN1
C-IN2
D-IN2
C-IN3
D-IN3
C-OUT
D-OUT

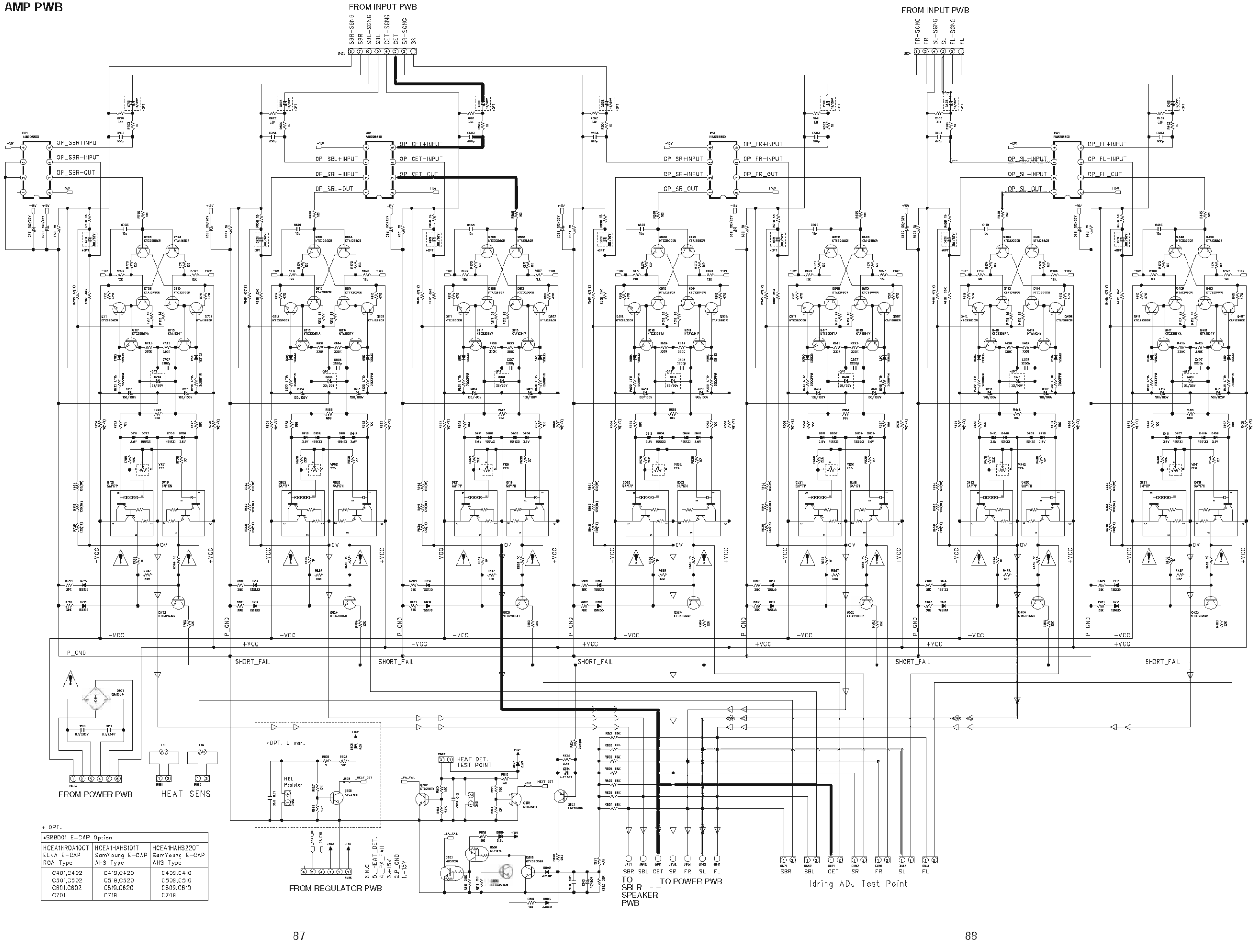
XM RADIO PWB

FROM DSP PWB -1/2

TO DSP PWB -1/2

N. C. BLOCK

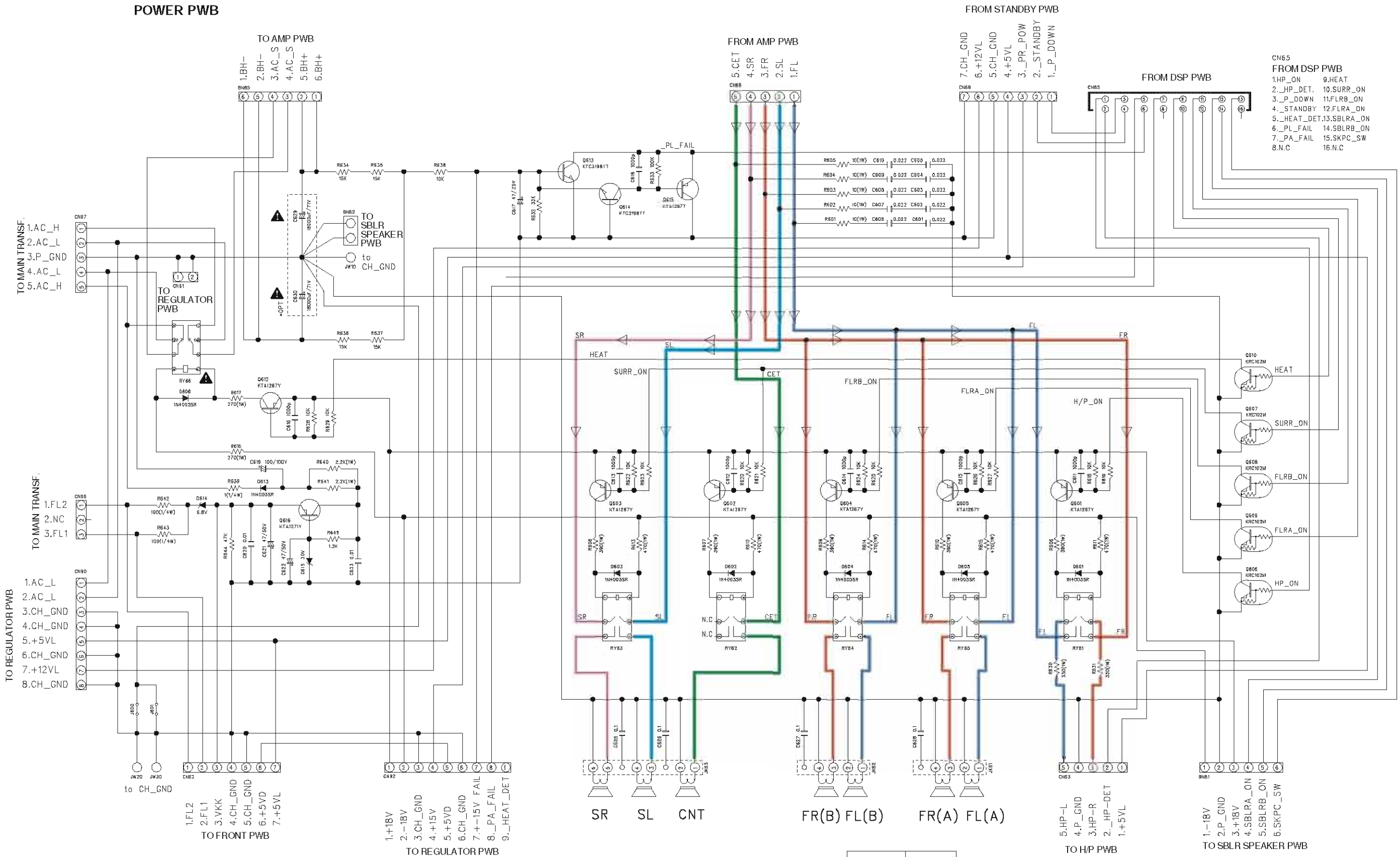
AMP PWB



* OPT.

*SRB001 E-CAP Option		
HCEA1HR0A100T ELNA E-CAP R0A Type	HCEA1HAHS101T SamYoung E-CAP AHS Type	HCEA1HAHS220T SamYoung E-CAP AHS Type
C401,C402 C501,C502 C601,C602 C701	C419,C420 C519,C520 C619,C620 C719	C409,C410 C509,C510 C609,C610 C709

POWER PWB



* OPTION	C629, C630
SR7001	LH6 TYPE 71V 18000uF
SR8001	LHO TYPE 71V 18000uF

SPK TERMINAL	COLOR
FR(A)	RED
FL(A)	WHITE
FL(B)	RED
FR(B)	WHITE
CENTER	GREEN
SR	GRAY
SL	BROWN

SELECTOR ENCODER PWB

FRONT PWB

FROM POWER PWB

FROM DSP PWB

FROM VOLUME PWB

FROM DSP PWB

FROM VIDEO PWB

VOLUME PWB

FROM INPUT PWB

TACT PWB
U VERSION ONLY

POWER ON/OFF

FRONT PANNEL AUX CONNECTION

7.1 CH INPUT PWB

TO INPUT PWB

7.1CH DIRECT IN

H/P PWB

FROM POWER PWB

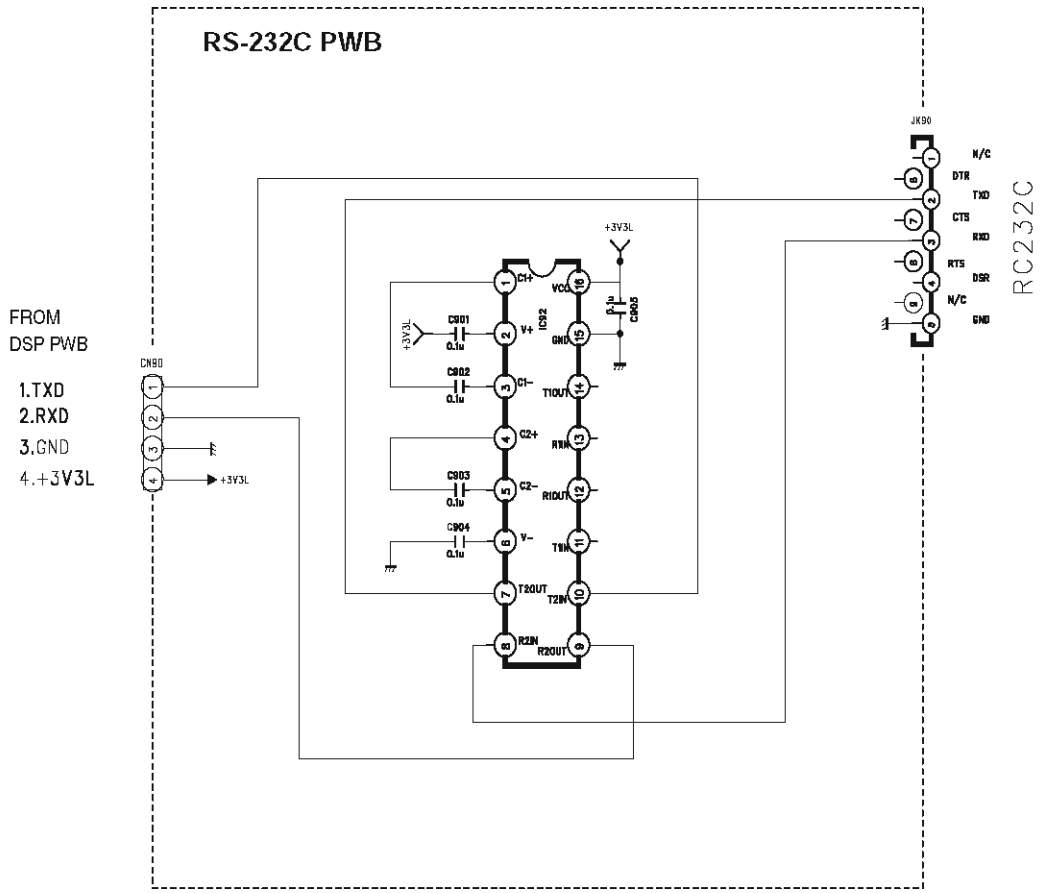
N,K,F VERSION ONLY

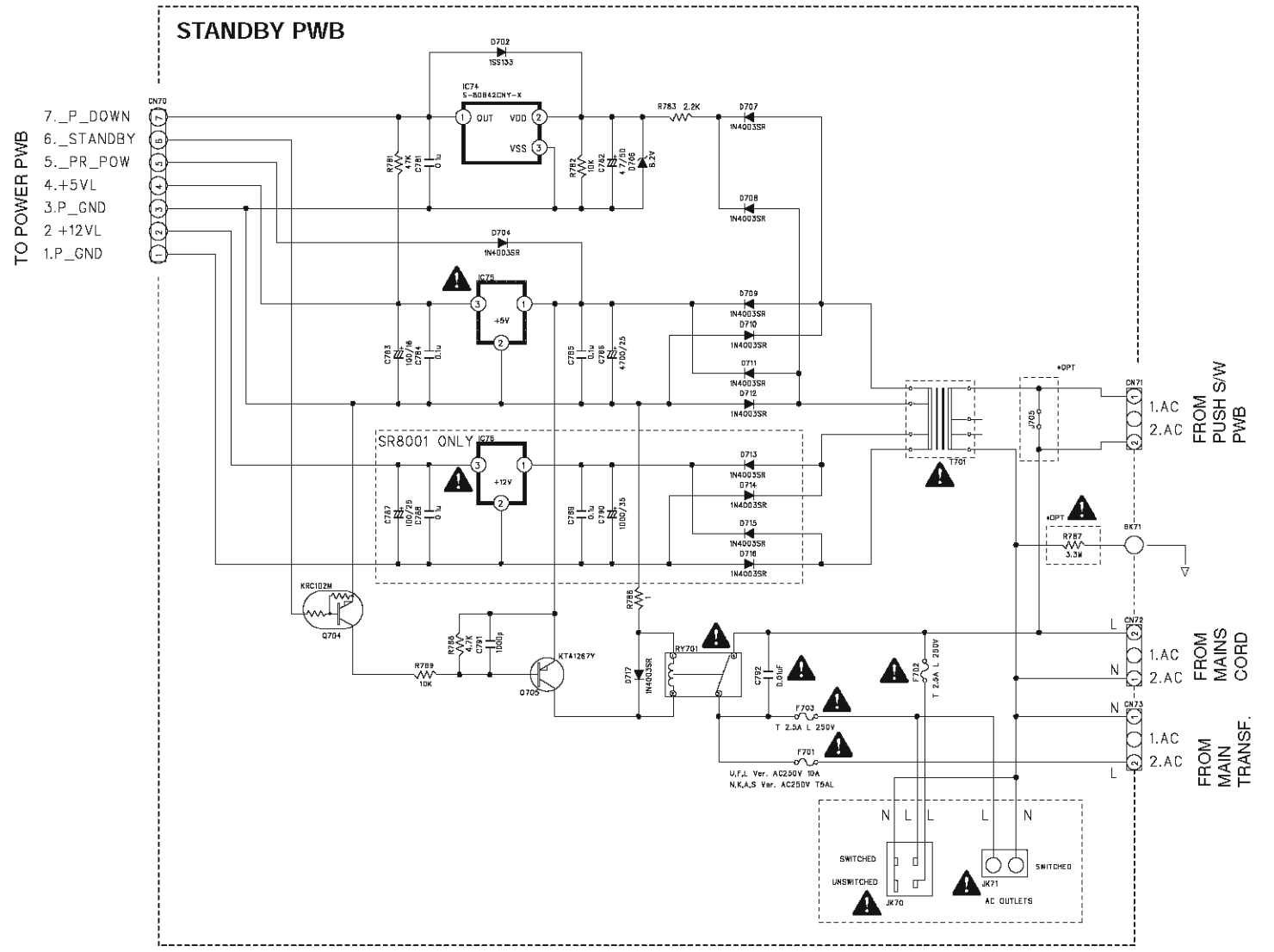
PUSH S/W PWB

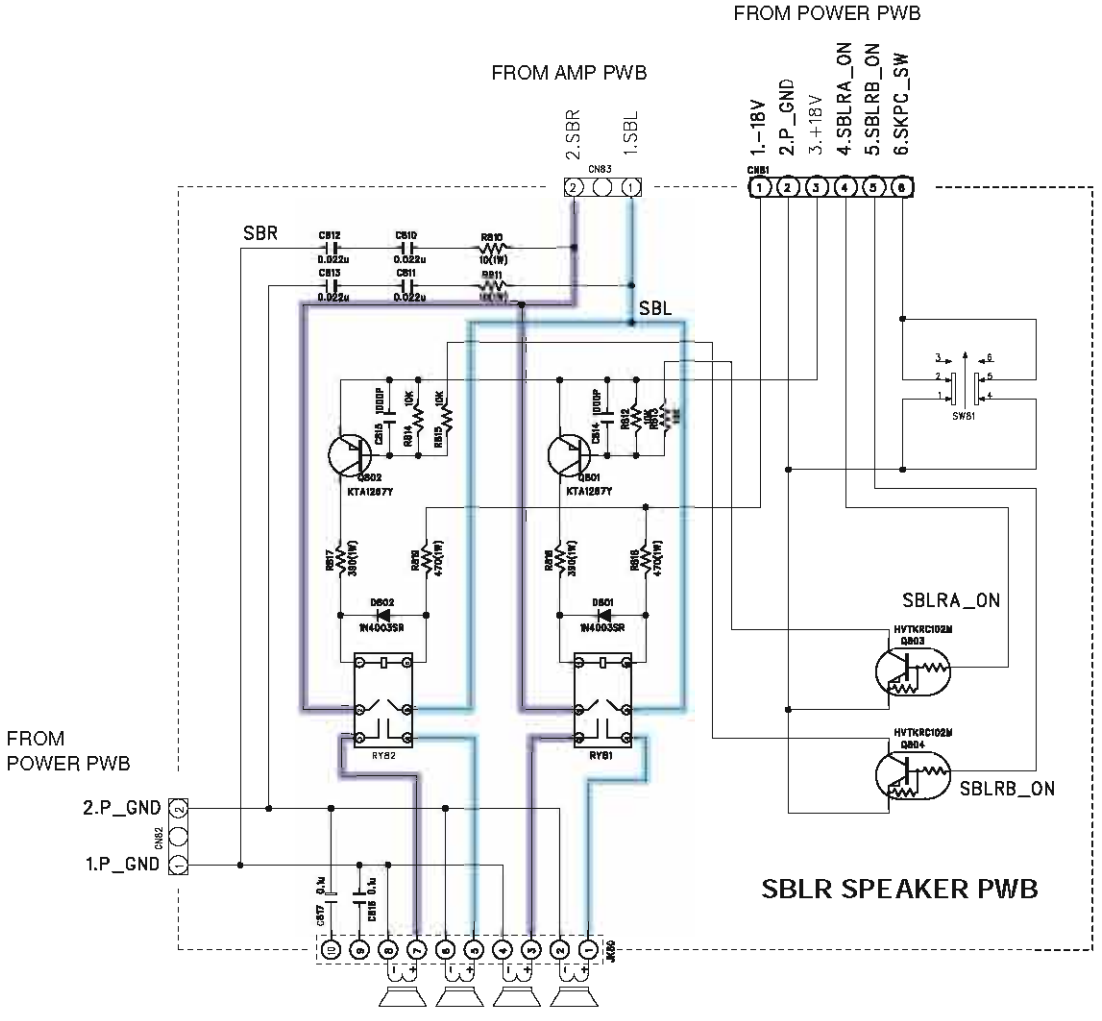
FROM STANDBY PWB

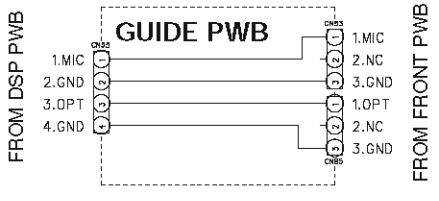
TO DSP PWB

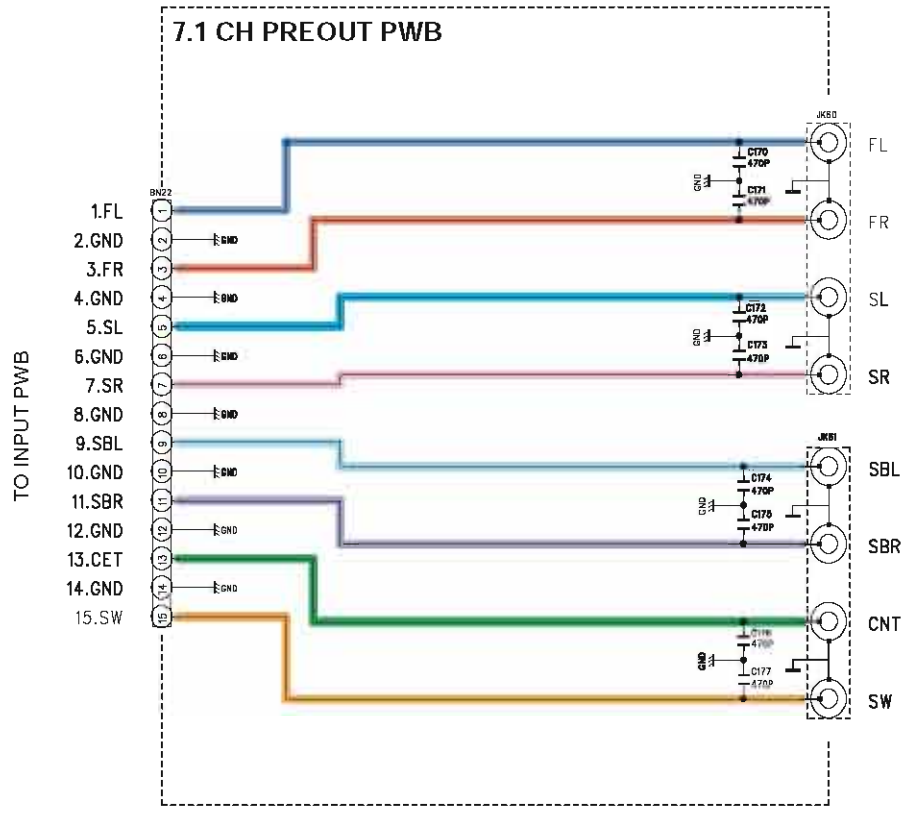
MIC


RS-232C PWB
FROM
DSP PWB
1.TXD
2.RXD
3.GND
4.+3V3L
CN80
JK90
RC232C
N/C
DTR
TXD
CTS
RXD
RTS
DSR
N/C
GND
+3V3L
IC92
C901
C902
C903
C904
C905
C+
V+
C-
V-
VCC
GND
T1OUT
R1IN
R1OUT
T1IN
T2OUT
R2IN
T2IN
R2OUT

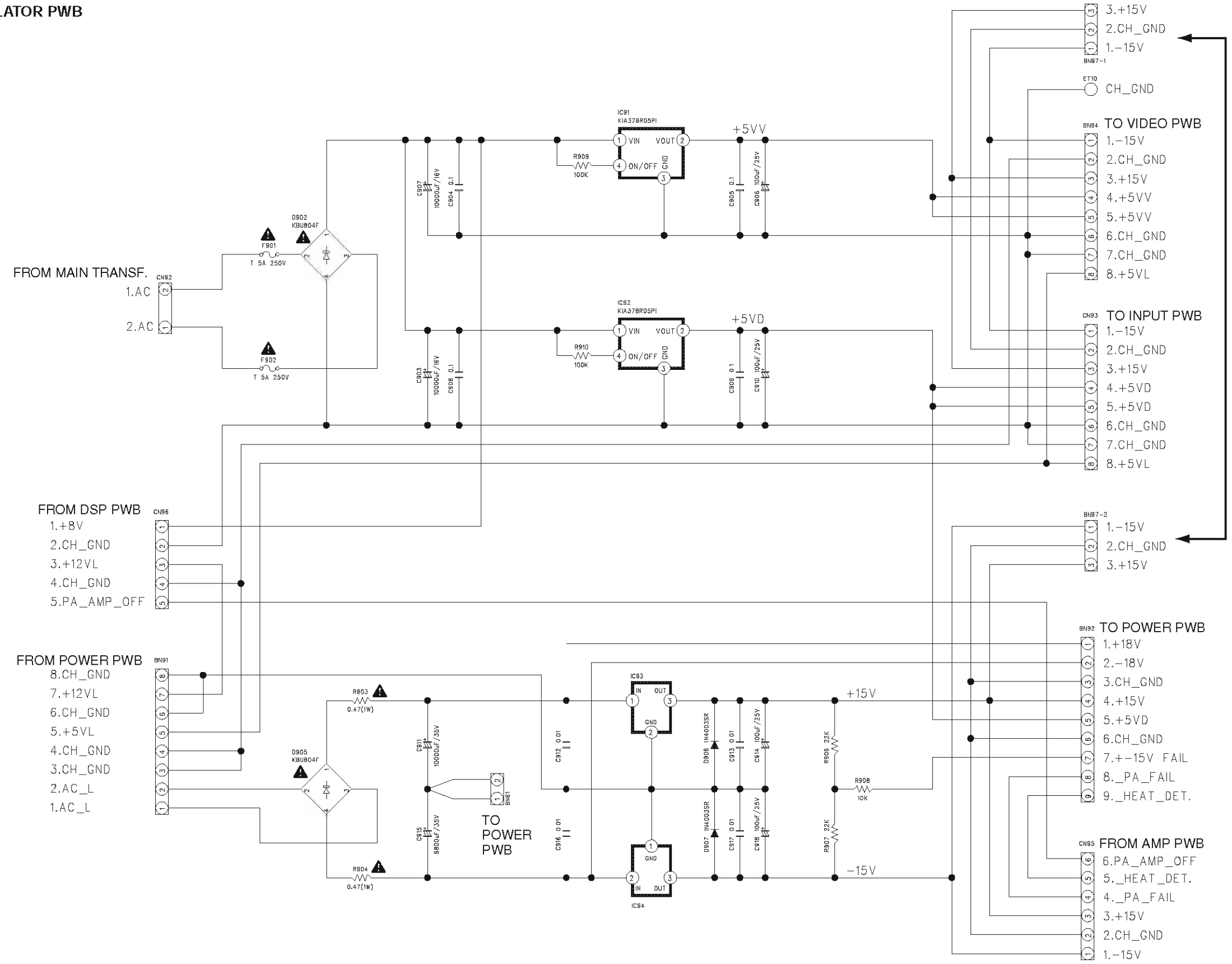

STANDBY PWB
TO POWER PWB
7._P_DOWN
6._STANDBY
5._PR_POW
4.+5VL
3.P_GND
2 +12VL
1.P_GND
CN70
IC74
S-80842CNY-X
OUT
VDD
VSS
IC75
+5V
+12V
SR8001 ONLY
D702
1SS133
D704
1N4003SR
D707
D708
D709
D710
D711
D712
D713
D714
D715
D716
KRC102M
Q704
KTA1267Y
Q705
RY701
T701
F703
T 2.5A L 250V
F701
U,F,L Ver. AC230V 10A
N,K,A,S Ver. AC250V T5AL
JK70
JK71
SWITCHED
UNSWITCHED
AC OUTLETS
FROM PUSH S/W PWB
FROM MAINS CORD
FROM MAIN TRANSF.
1.AC
2.AC


FROM POWER PWB
FROM AMP PWB
2.SBR
1.SBL
1.-18V
2.P_GND
3.+18V
4.SBLRA_ON
5.SBLRB_ON
6.SKPC_SW
CN83
CN81
SBR
SBL
SW51
SBLRA_ON
SBLRB_ON
HVTKRC102M
Q803
Q804
KTA1267Y
Q802
Q801
1N4003SR
D802
D801
RY82
RY81
FROM
POWER PWB
2.P_GND
1.P_GND
CN82
JK60
SBLR SPEAKER PWB

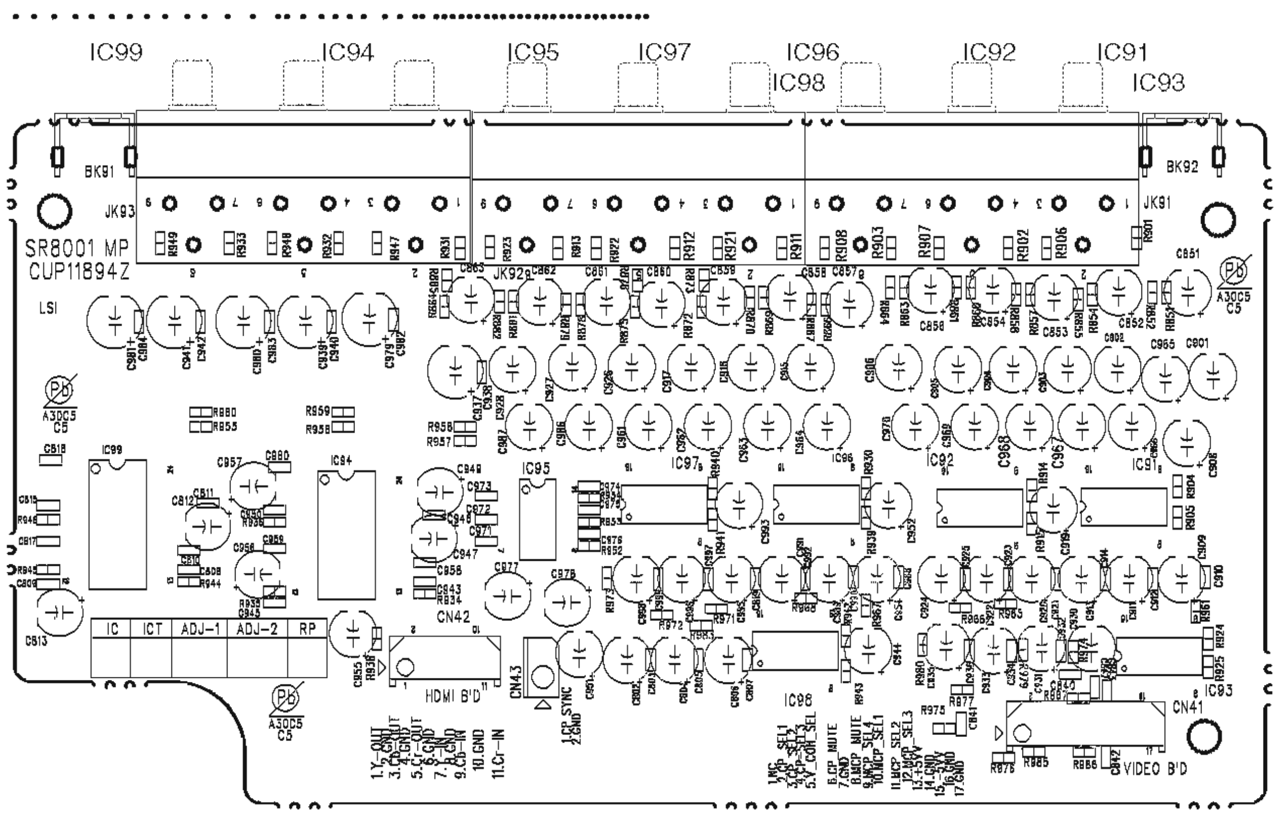

GUIDE PWB
FROM DSP PWB
1.MIC
2.GND
3.OPT
4.GND
CN55
CN53
1.MIC
2.NC
3.GND
1.OPT
2.NC
3.GND
FROM FRONT PWB

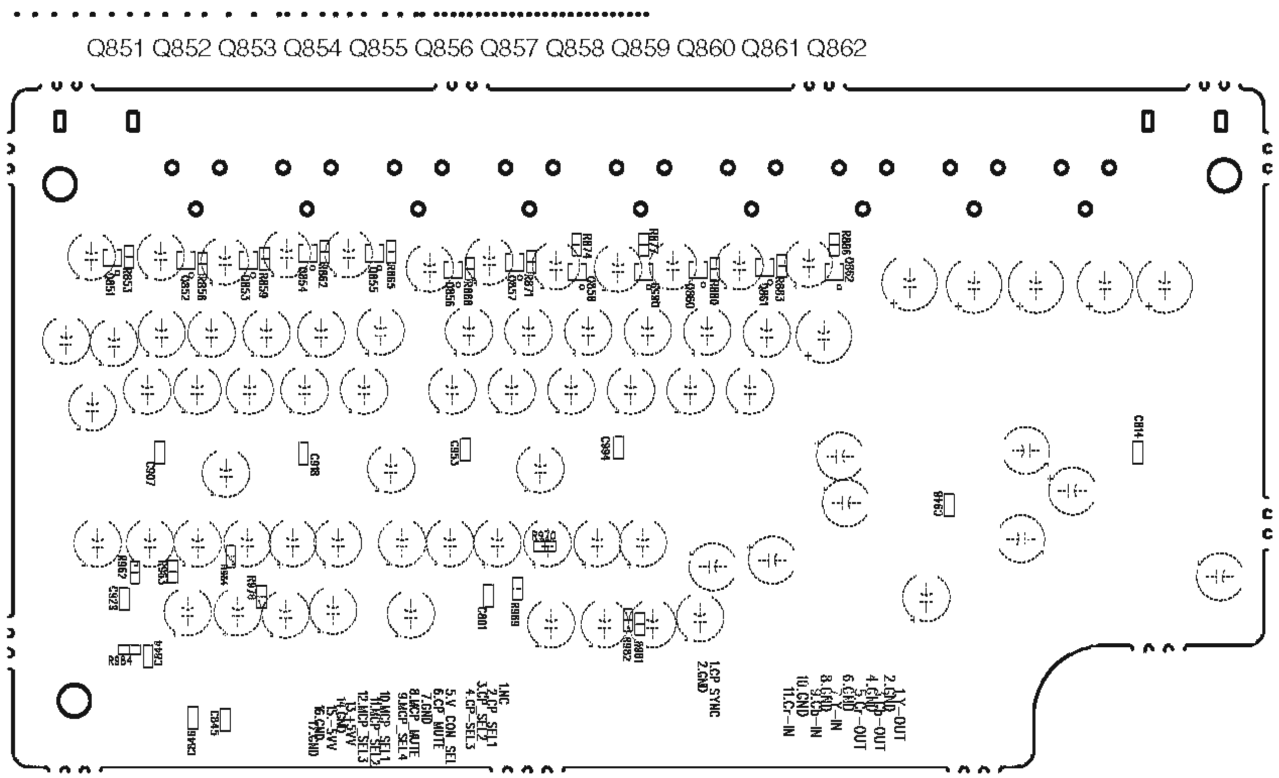

7.1 CH PREOUT PWB
TO INPUT PWB
1.FL
2.GND
3.FR
4.GND
5.SL
6.GND
7.SR
8.GND
9.SBL
10.GND
11.SBR
12.GND
13.CET
14.GND
15.SW
BN22
JK80
JK81
FL
FR
SL
SR
SBL
SBR
CNT
SW
GND

REGULATOR PWB

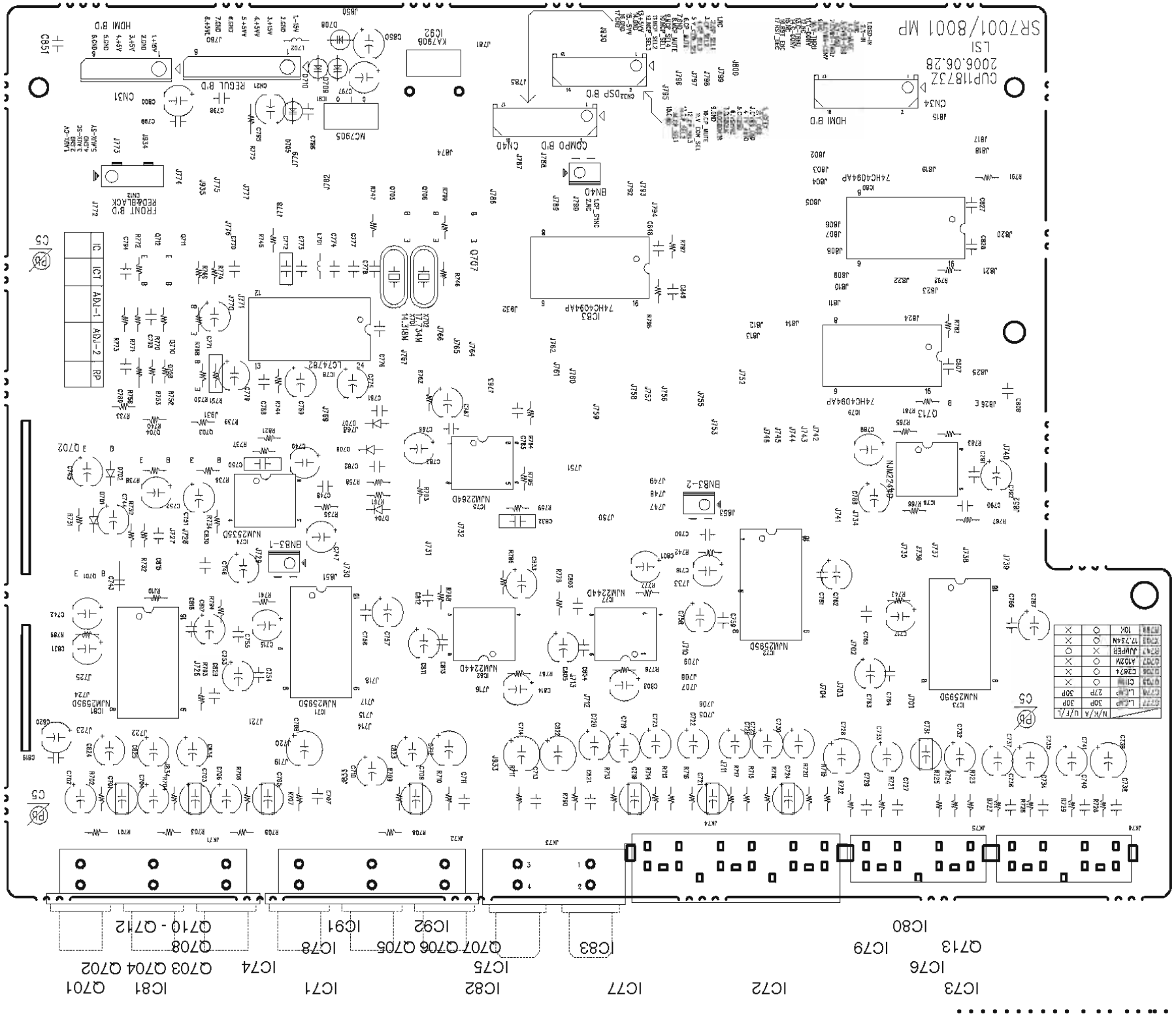


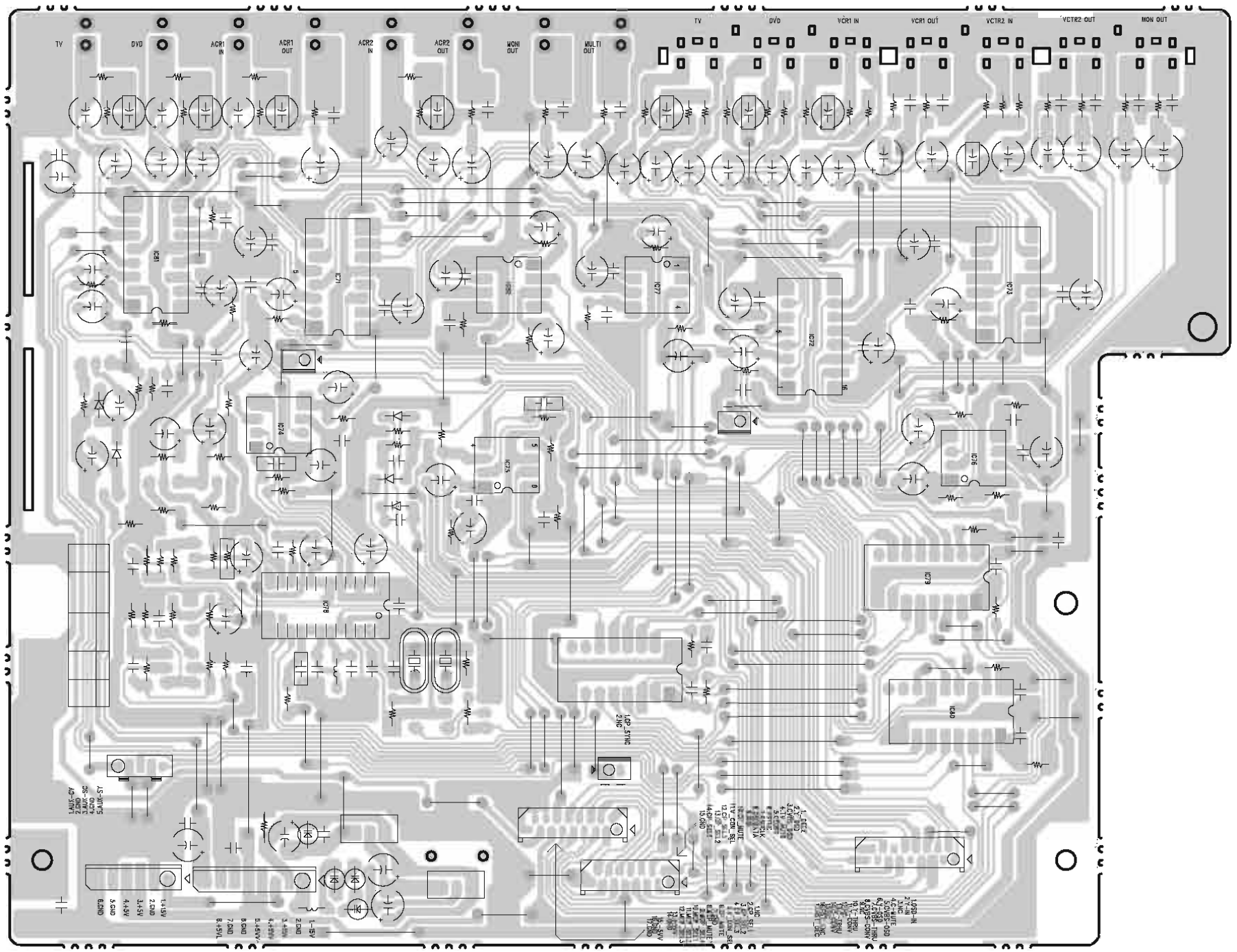
10. PARTS LOCATION





SR7001/8001 MP
LSI
2006.06.28
CUP1187J2




TV
DVD
AGR1 IN
AGR1 OUT
AGR2 IN
AGR2 OUT
MONI OUT
MULTI OUT
VCR1 IN
VCR1 OUT
VCTR2 IN
VCTR2 OUT
MON OUT

鉛フリ ー半田

半田付けには、鉛フリ ー半田 (Sn-Ag-Cu) を使用してください。

Lead-free Solder

When soldering, use the Lead-free Solder (Sn-Ag-Cu).

IC11 IC13 IC15 IC17 IC40

Q101 Q102 IC12 Q105 Q106 IC14 Q109 Q110 IC16 Q113 Q114 IC18 Q301 IC43

Q104 Q111 Q108 Q107 Q112 Q103 Q116 Q115 Q303

IC19 IC20 Q117 Q118 IC21 IC22 IC23 IC41 IC44

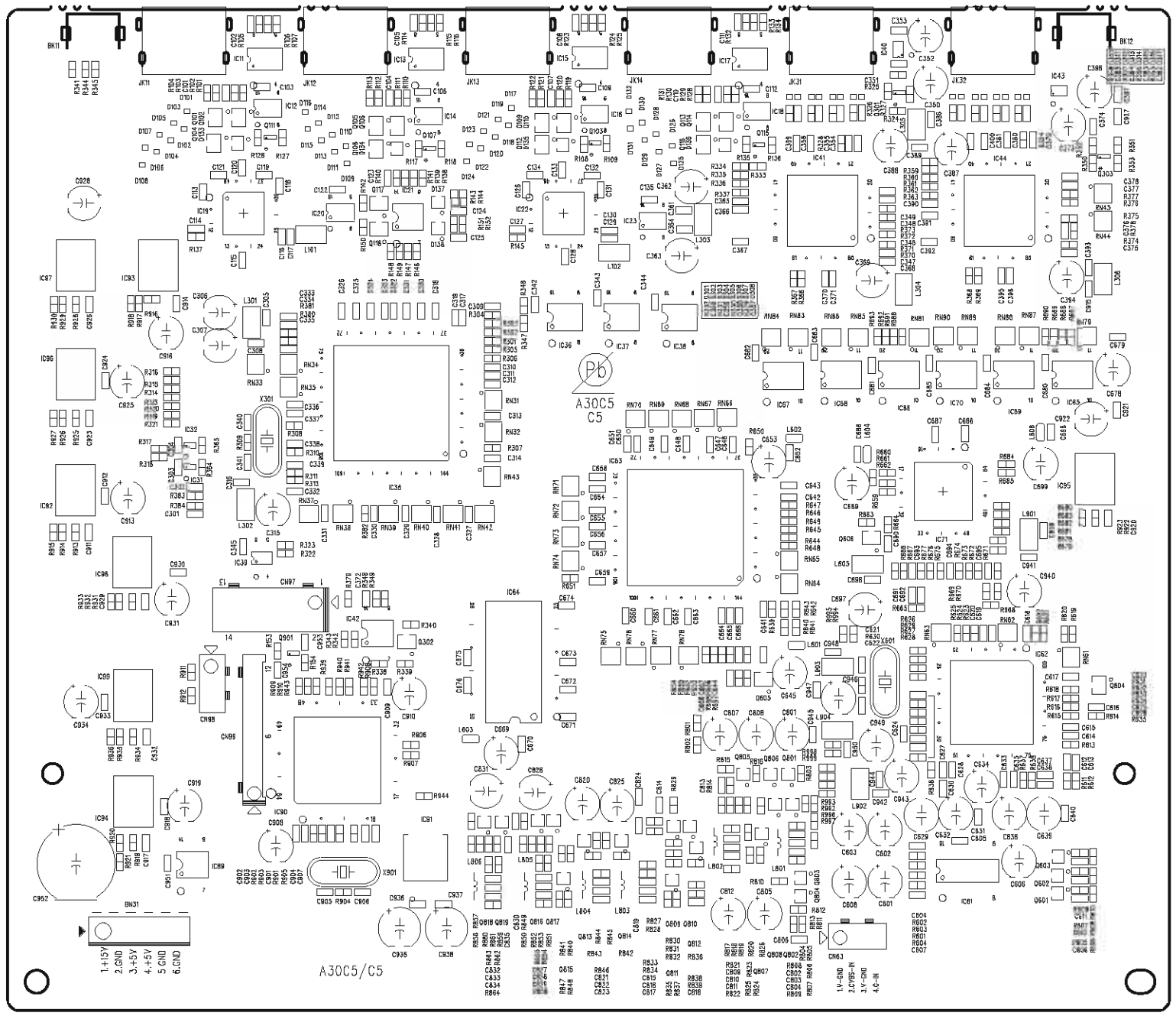
IC97 IC93 IC35 IC36 IC37 IC38 IC67 IC68 IC66 IC70 IC69 IC65

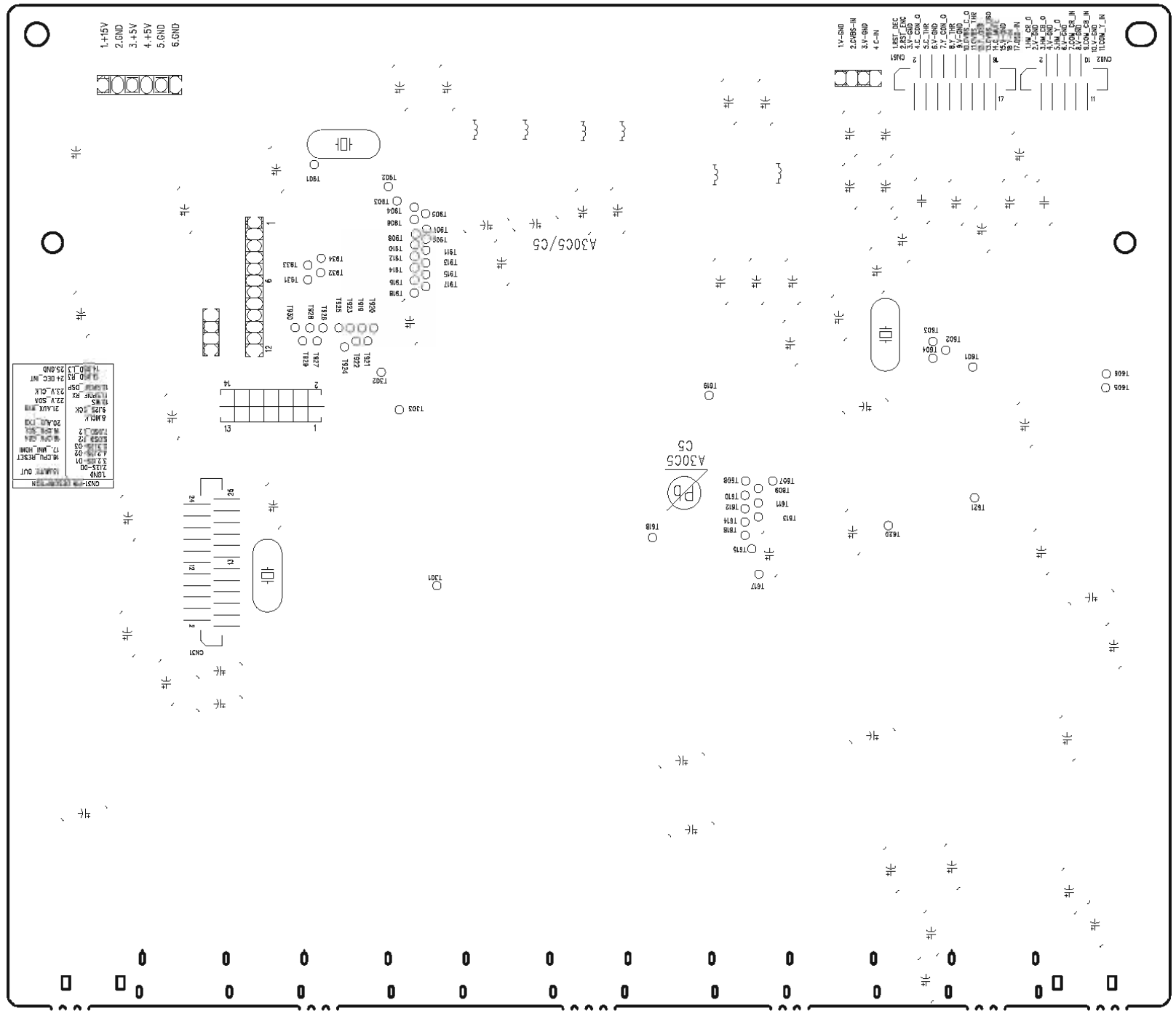
IC96 IC98 IC32 IC31 IC39 IC63 Q605 Q606 IC71 IC95

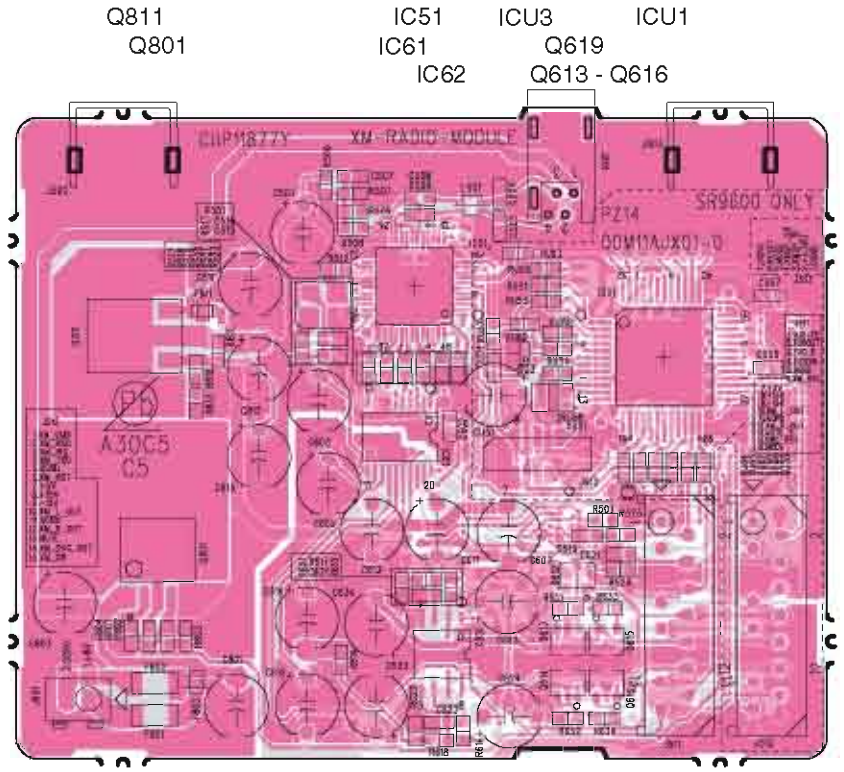
IC92 IC99 Q901 IC42 Q302 IC64 Q805 Q806 Q801 IC62 Q604

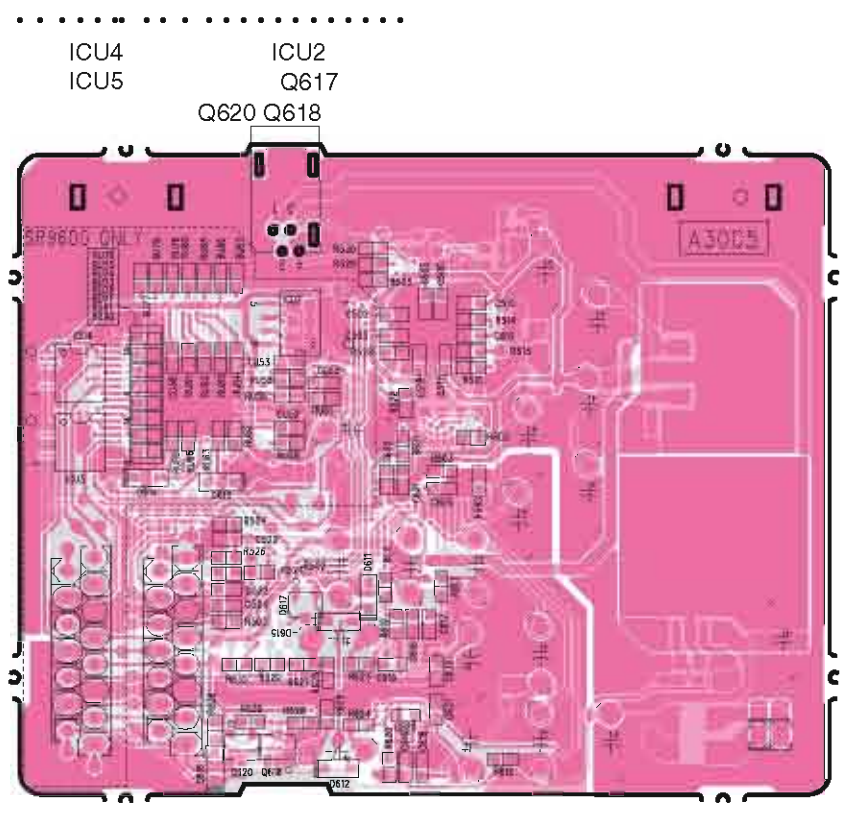
IC94 IC90 Q816 - Q819 Q809 Q810 Q808 Q802

IC89 IC91 Q815 Q813 Q814 Q811 Q812 Q807 Q803 Q804 IC61 Q603 - Q601




1.+15V
2.GND
3.+5V
4.+5V
5.GND
6.GND
A3CC5/C5
A3CC5
C5



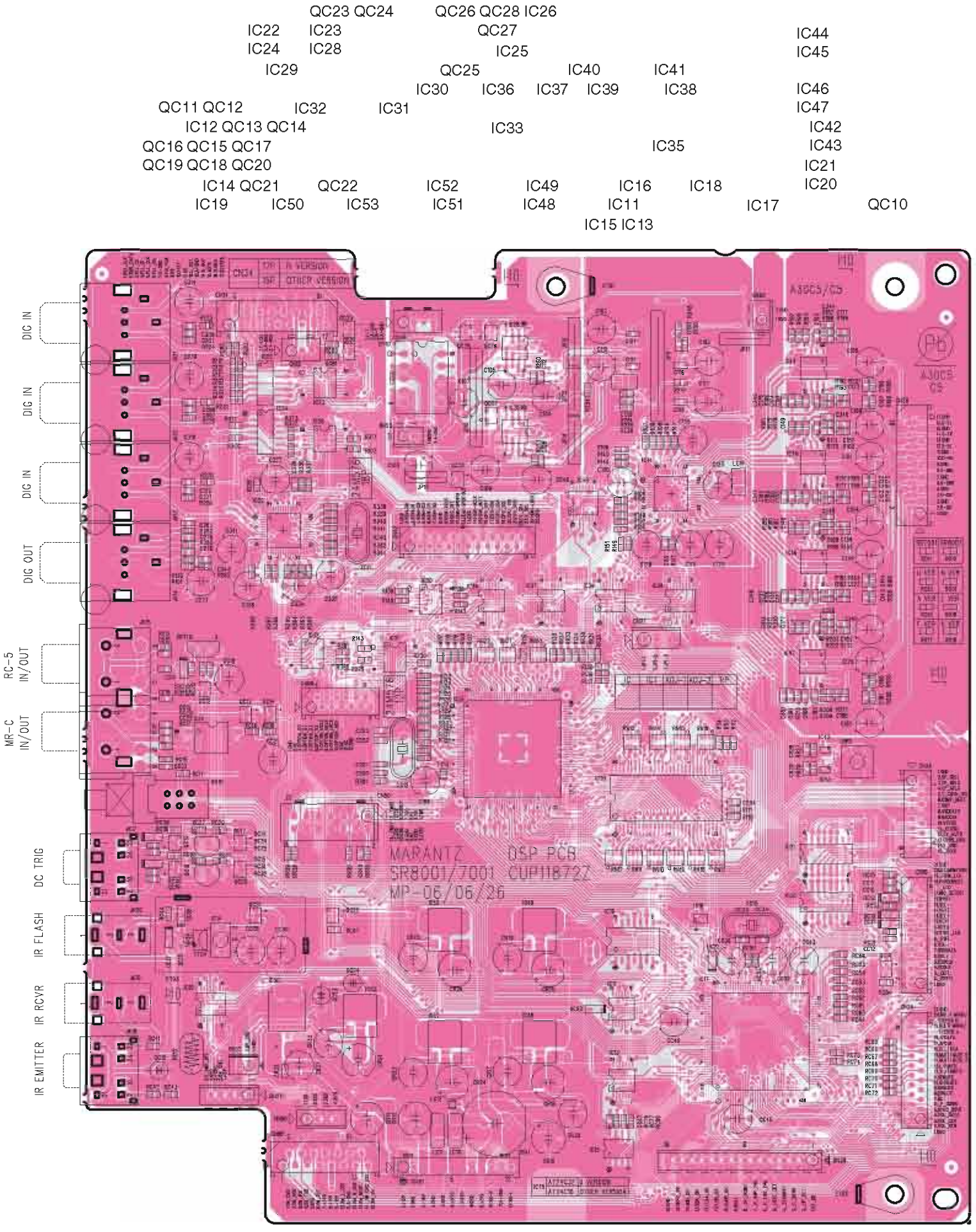


鉛フリ ー半田

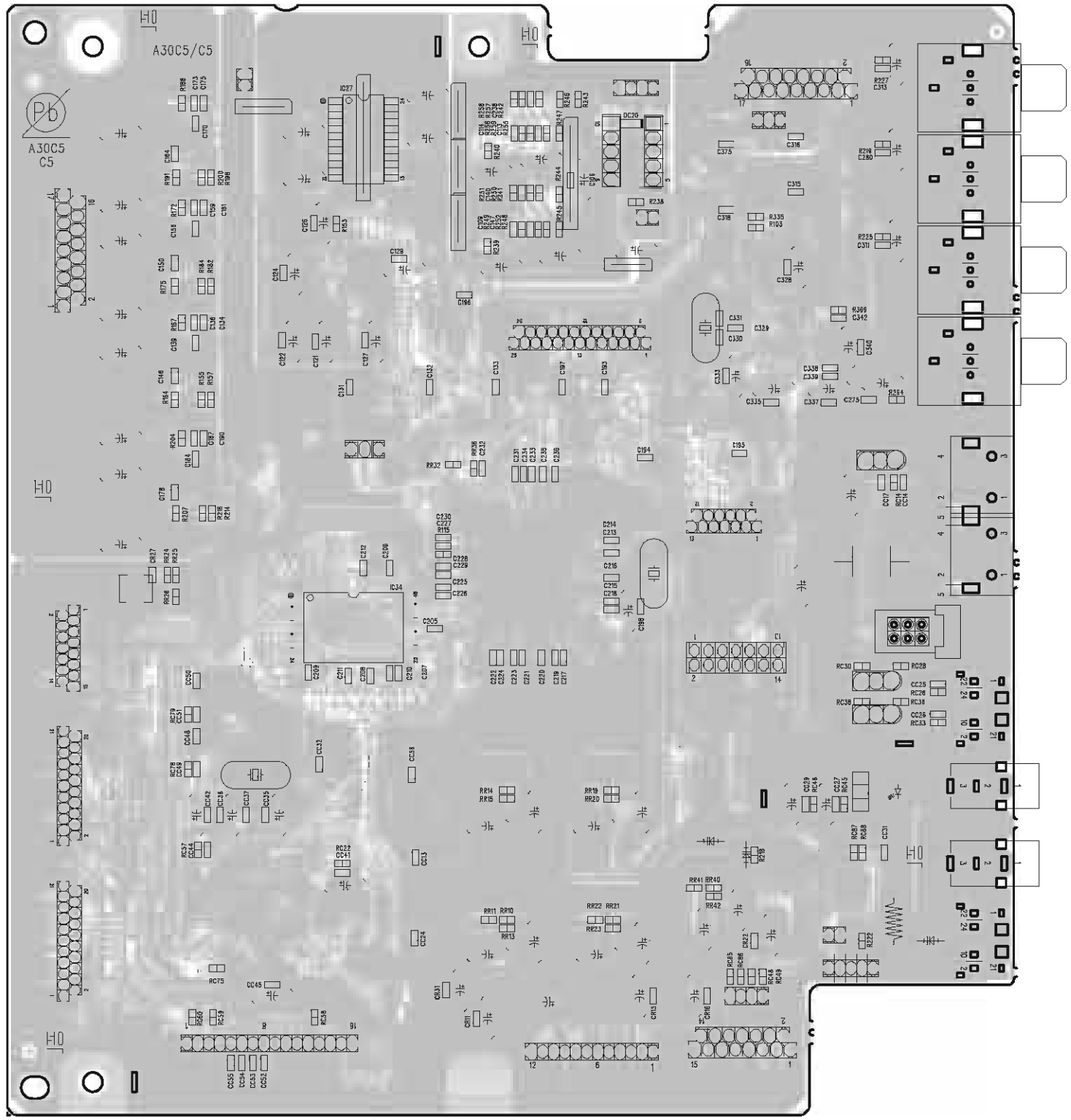
半田付けには、鉛フリ ー半田 (Sn-Ag-Cu) を使用してください。

Lead-free Solder

When soldering, use the Lead-free Solder (Sn-Ag-Cu).



IC27
IC34



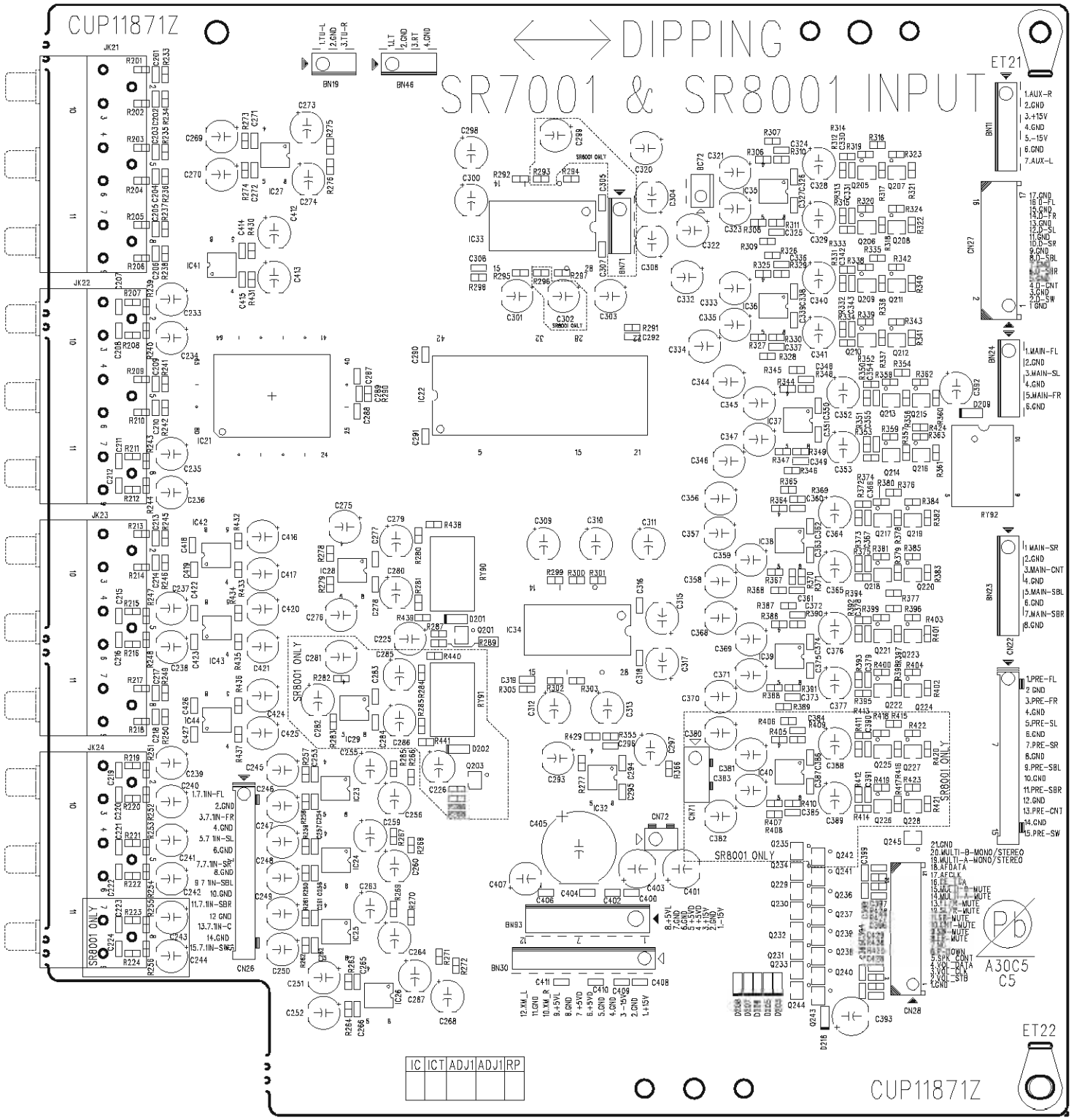
鉛フリー半田
半田付けには、鉛フリー半田 (Sn-Ag-Cu) を使用してください。

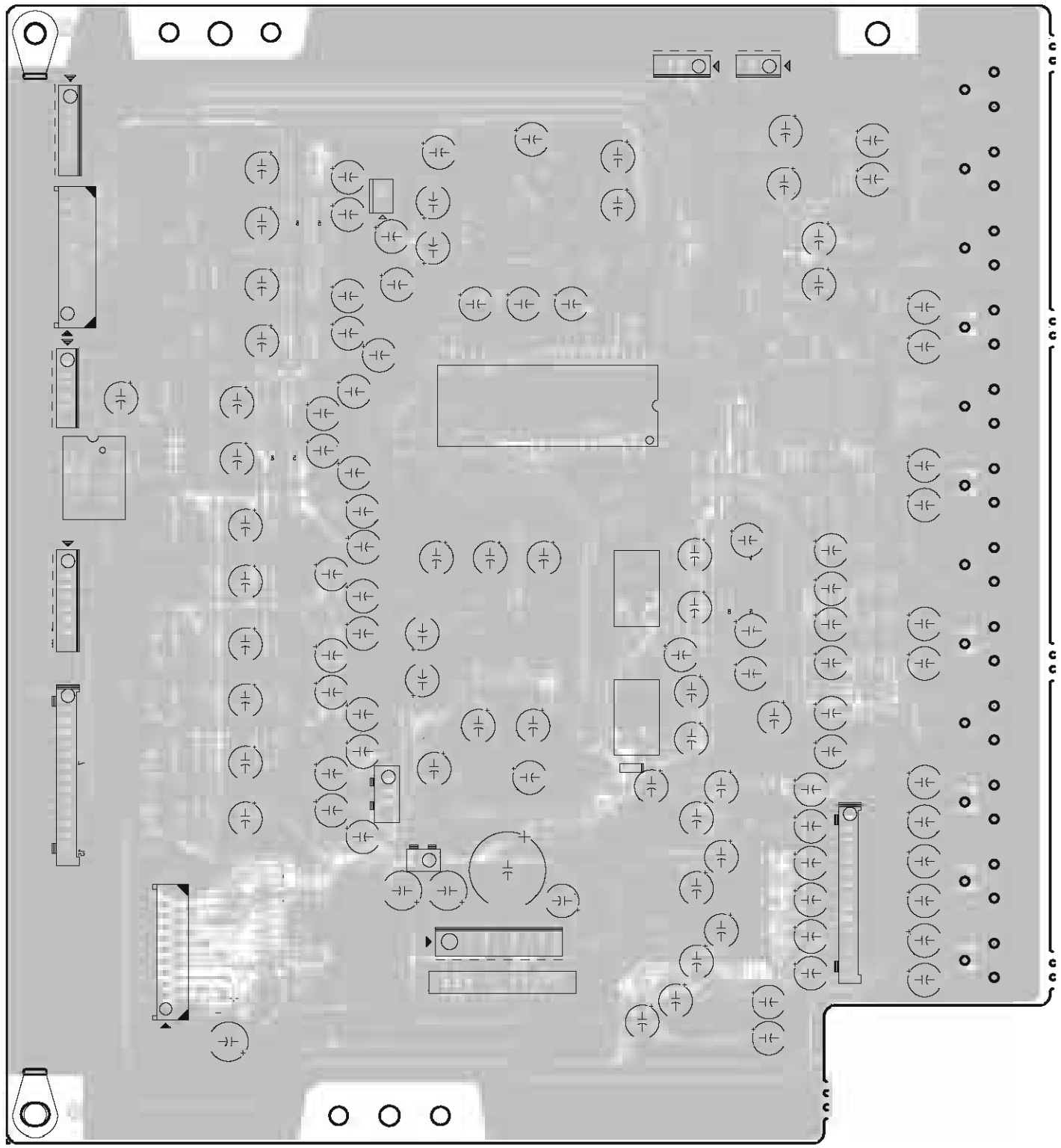
Lead-free Solder
When soldering, use the Lead-free Solder (Sn-Ag-Cu).

鉛フリ ー半田
半田付けには、鉛フリ ー半田 (Sn-Ag-Cu) を使用してください。

Lead-free Solder
When soldering, use the Lead-free Solder (Sn-Ag-Cu).

IC27 IC33 IC35 Q205 - Q208
IC41 IC36 Q209 - Q212
IC21 IC22 IC37 Q213 - Q216
IC42 IC28 IC38 Q217 - Q220
IC43 Q201 IC34 IC39 Q211 - Q224
IC44 IC29 Q203 IC32 IC40 Q225 - Q228
IC23 - IC26 Q229 - Q244 Q245

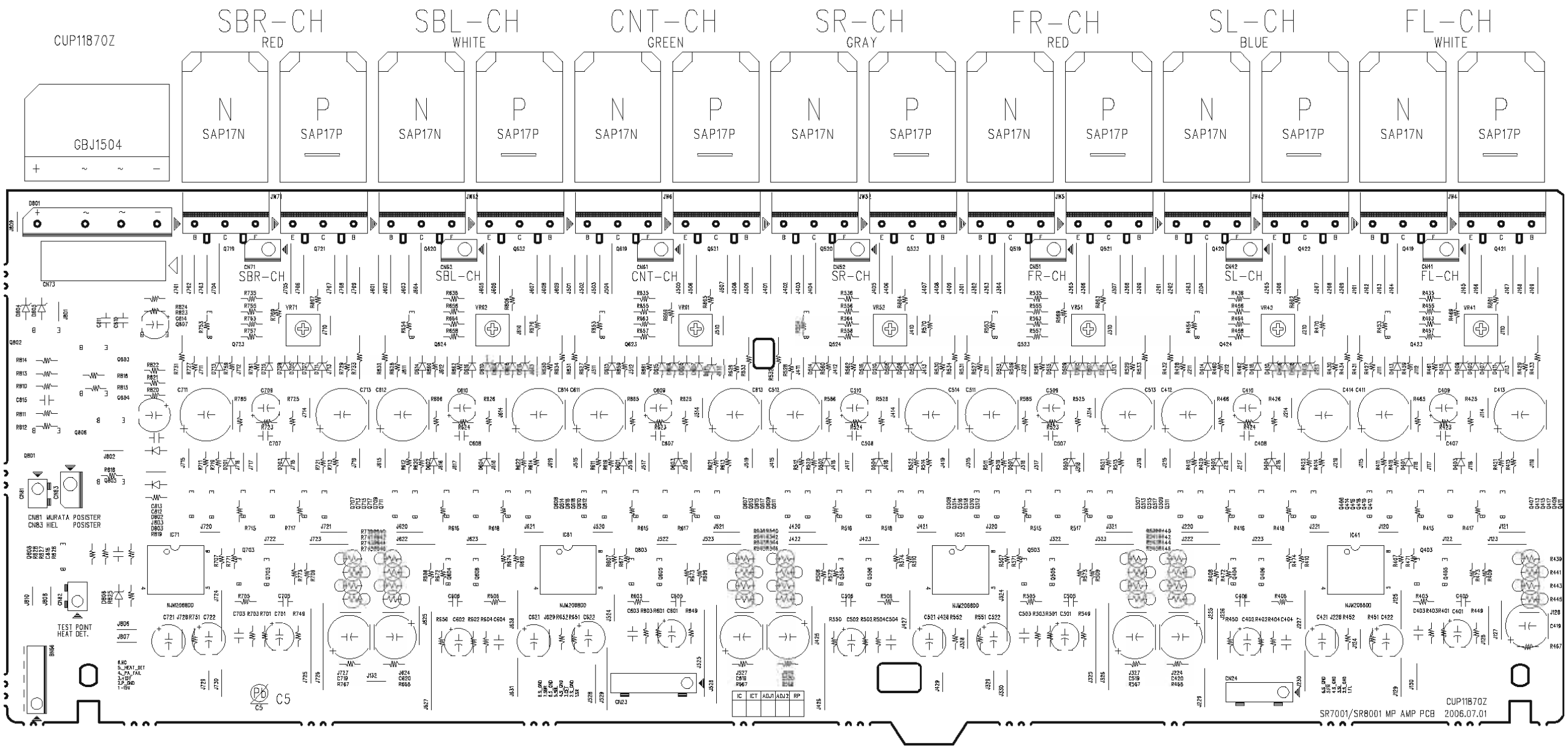


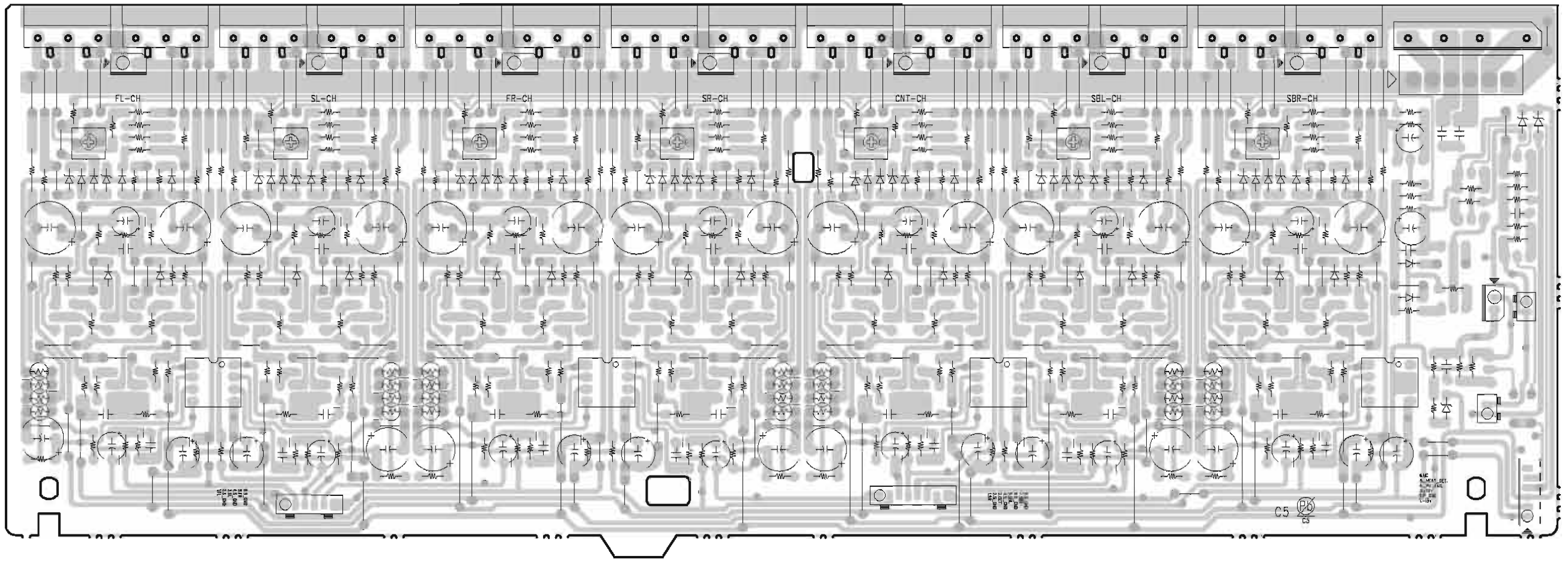


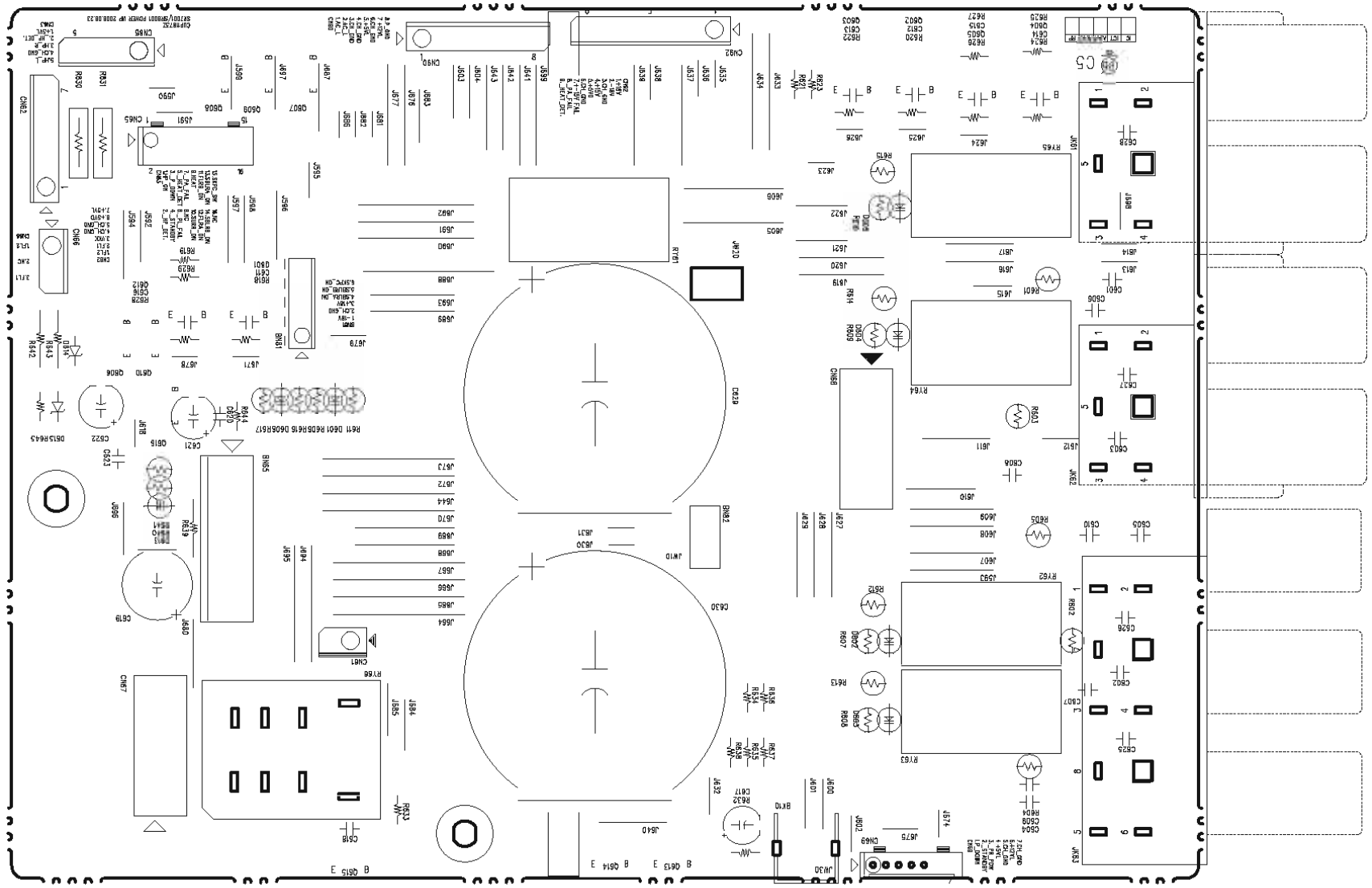
鉛フリ ー半田
半田付けには、鉛フリ ー半田 (Sn-Ag-Cu) を使用してく ださい。

Lead-free Solder
When soldering, use the Lead-free Solder (Sn-Ag-Cu).

Q719 Q721 Q620 Q622 Q619 Q621 Q520 Q522 Q519 Q521 Q420 Q422 Q419 Q421
Q802 Q803 Q807 Q723 Q624 Q623 Q524 Q523 Q424 Q423
Q801 Q804 Q806 Q707 Q715 Q709 Q608 Q616 Q610 Q607 Q615 Q609 Q508 Q516 Q510 Q507 Q515 Q509 Q408 Q416 Q410 Q407 Q415 Q409
Q805 Q713 Q717 Q711 Q614 Q618 Q612 Q613 Q617 Q611 Q514 Q518 Q512 Q513 Q517 Q511 Q414 Q418 Q412 Q413 Q417 Q411
Q808 IC71 Q703 Q705 Q604 Q606 IC61 Q603 Q605 Q504 Q506 IC51 Q503 Q505 Q404 Q406 IC41 Q403 Q405




FL-CH
SL-CH
FR-CH
SR-CH
CNT-CH
SBL-CH
SBR-CH
C5
P6
C5

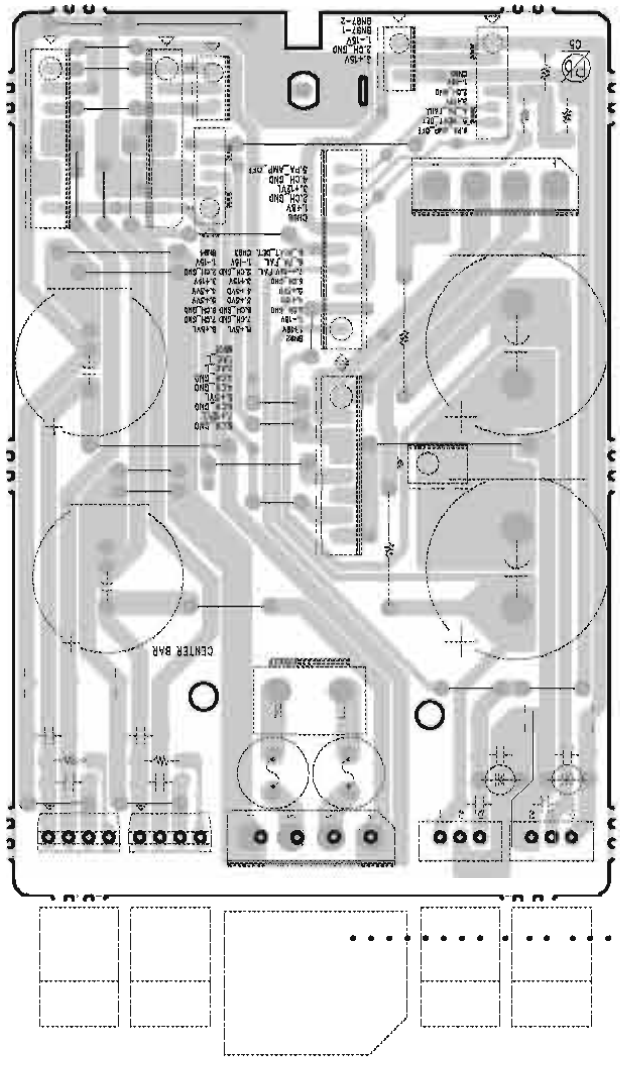


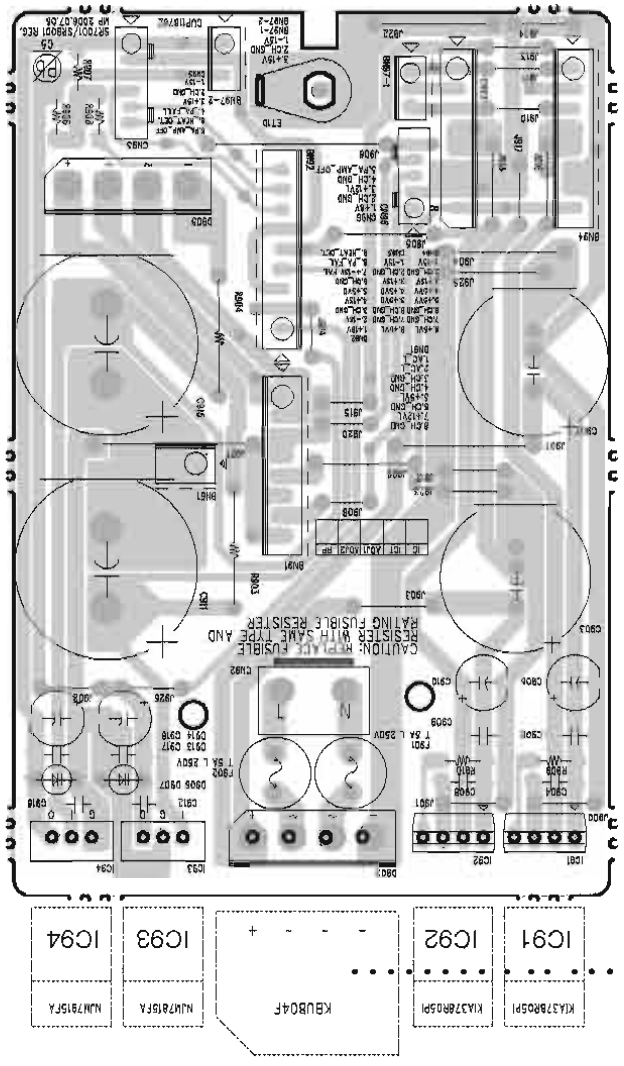
Q604 Q605 Q602 Q603

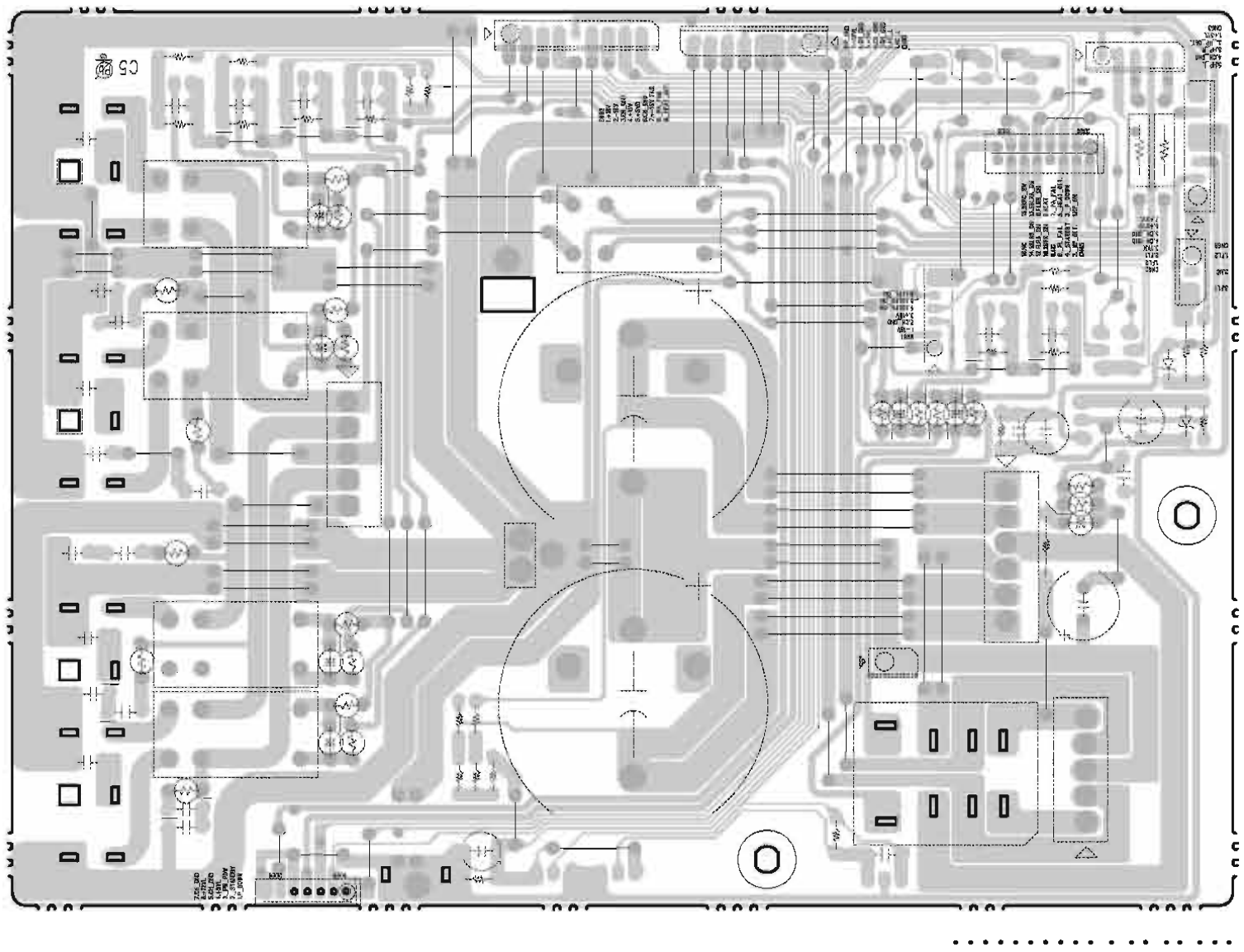
Q607 Q609 Q608

Q601 Q612 Q610 Q606

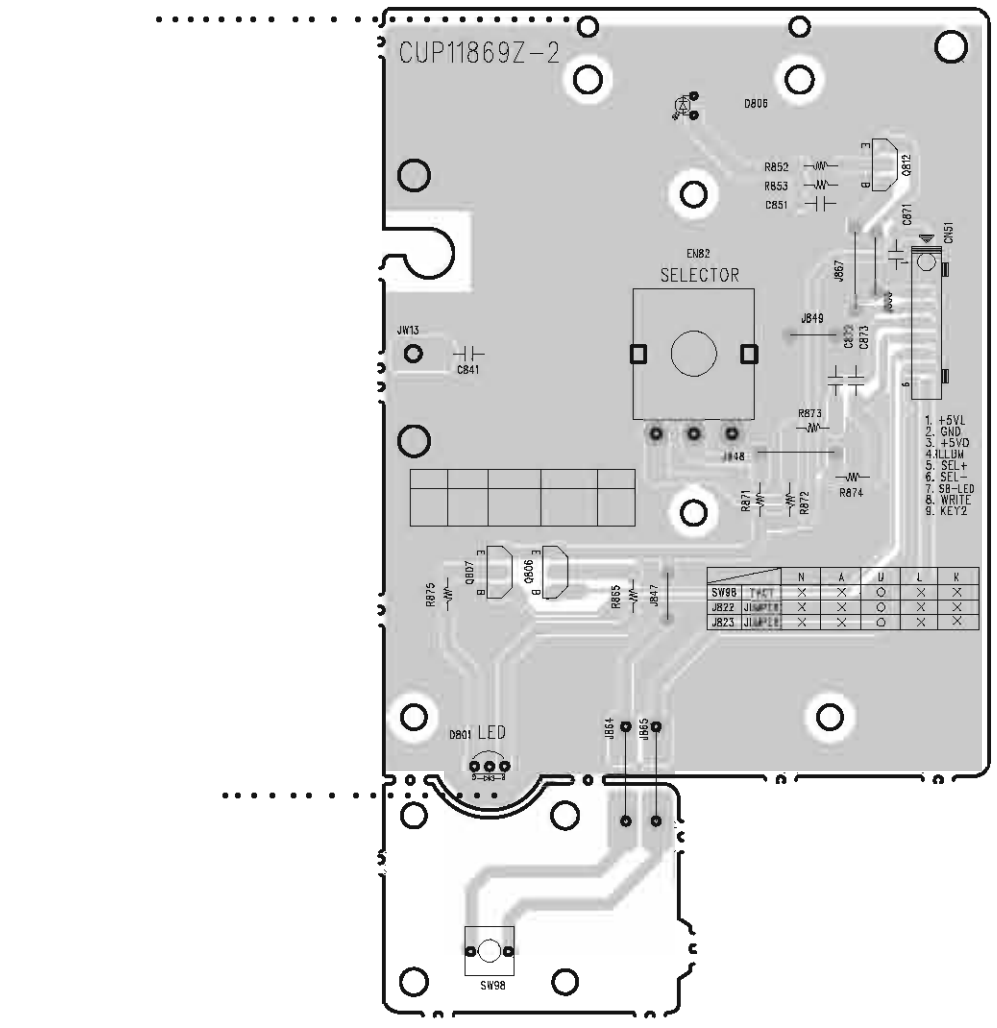
Q616 Q615 Q613 Q614

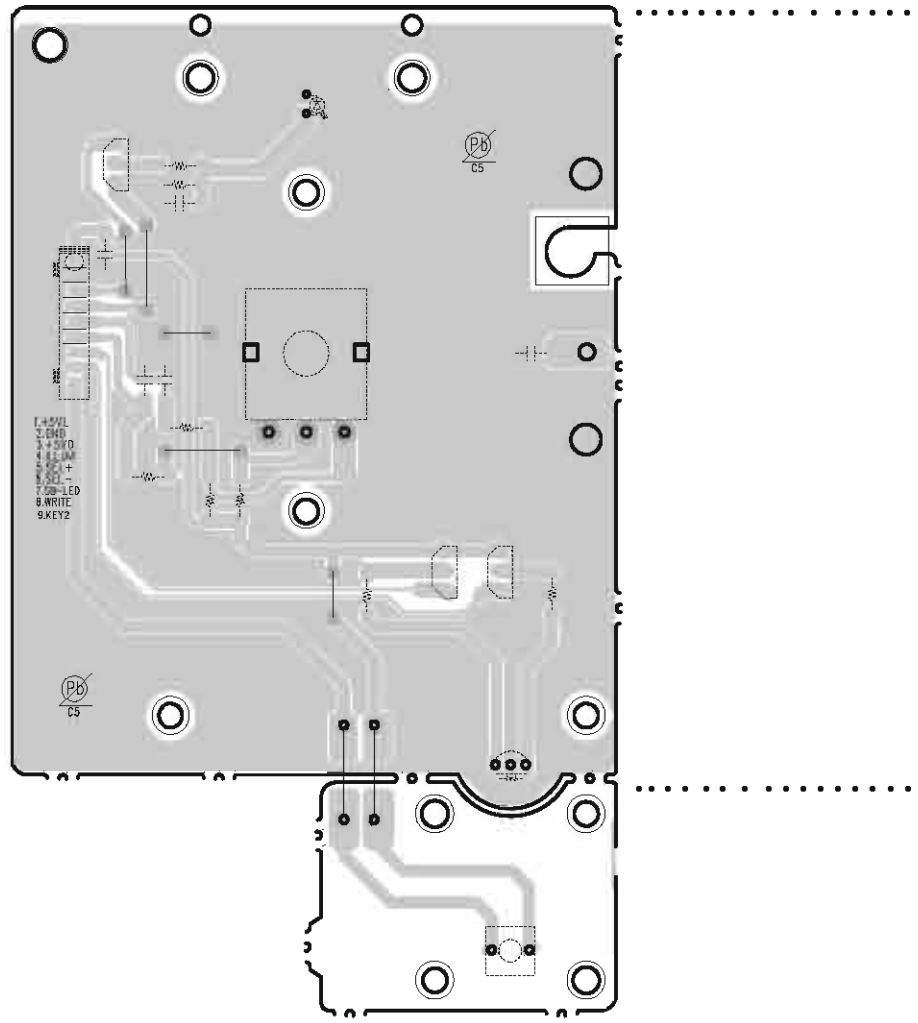

CENTER BAR

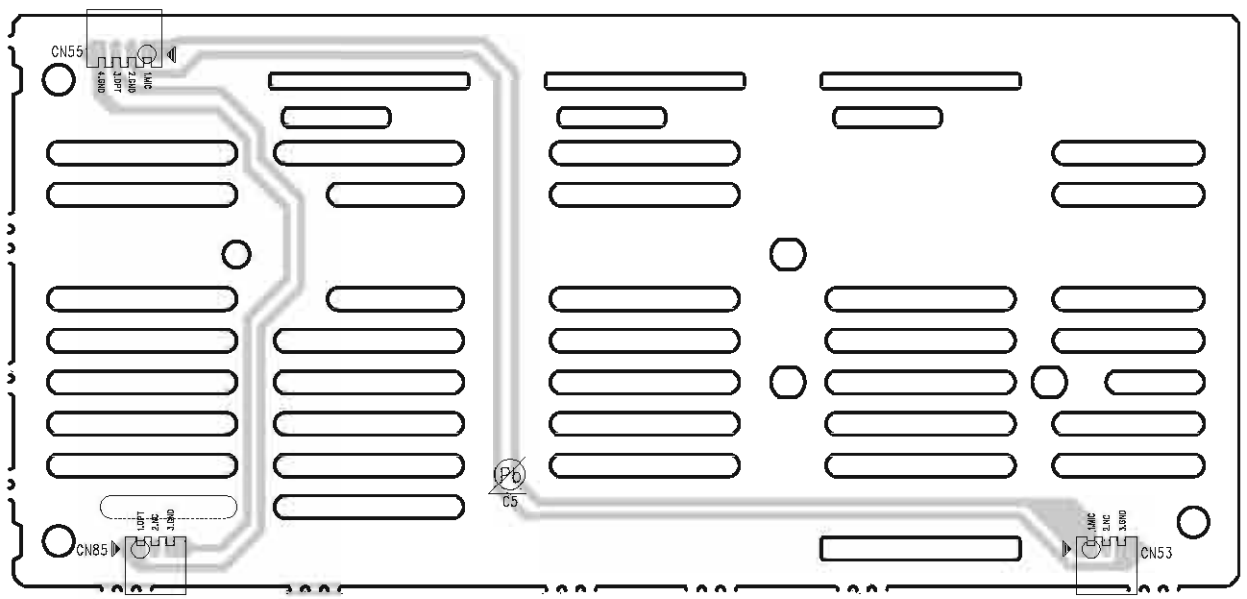

CAUTION: REPLACE FUSIBLE RESISTER WITH SAME TYPE AND RATING FUSIBLE RESISTER
KBU804F
IC91
IC92
IC93
IC94



Q807 Q806 Q812

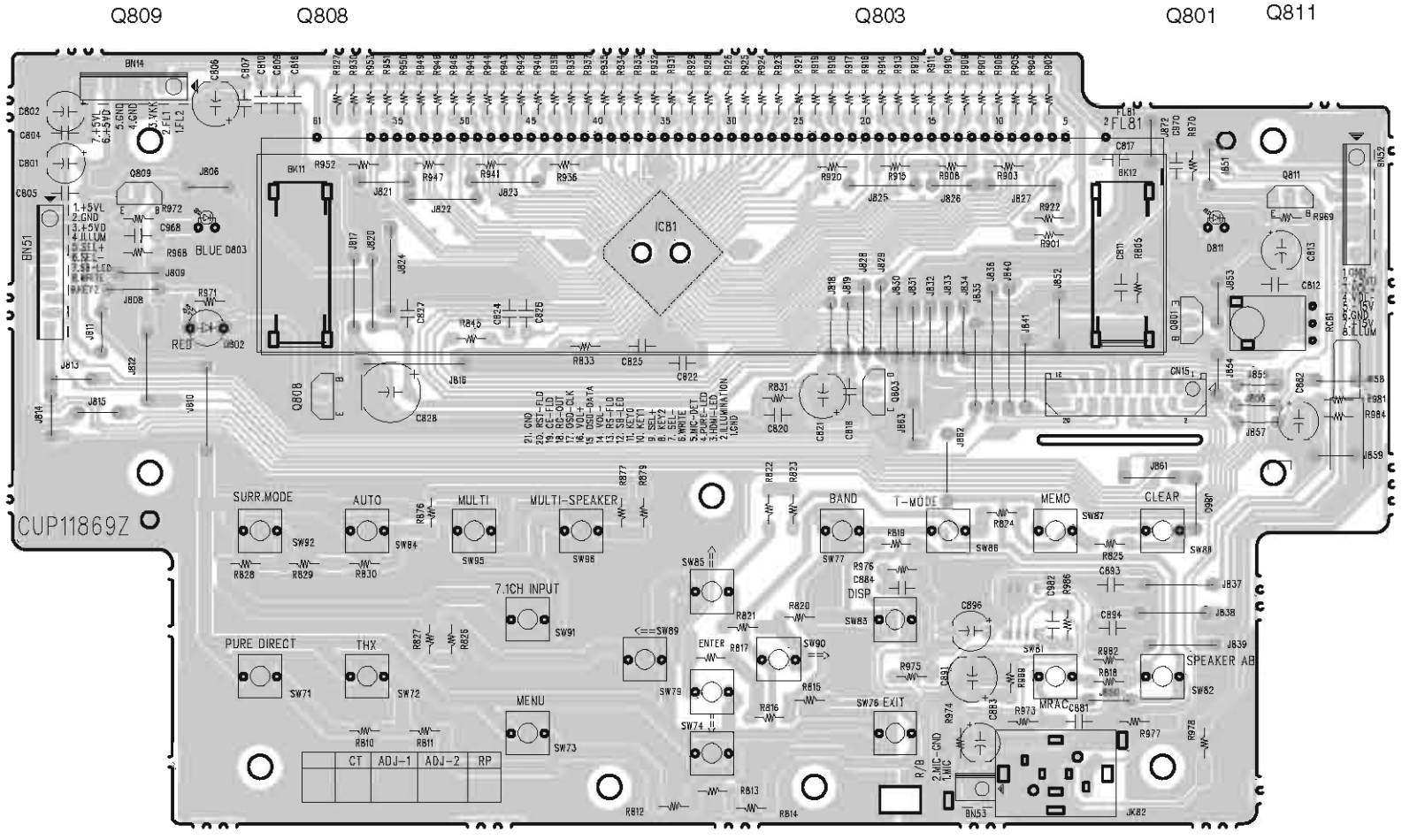


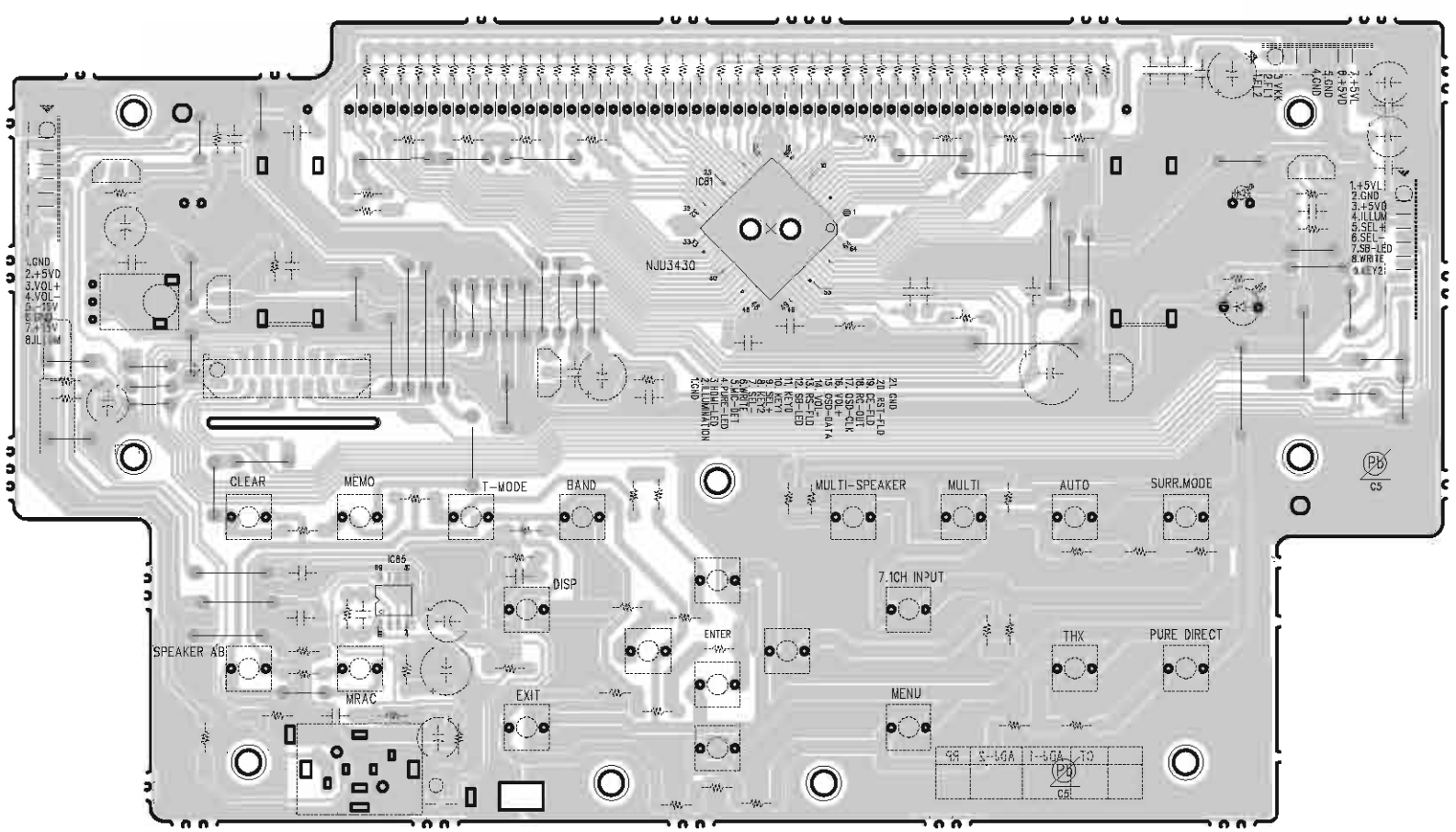




鉛フリ ー半田
半田付けには、鉛フリ ー半田 (Sn-Ag-Cu) を使用してください。

Lead-free Solder
When soldering, use the Lead-free Solder (Sn-Ag-Cu).



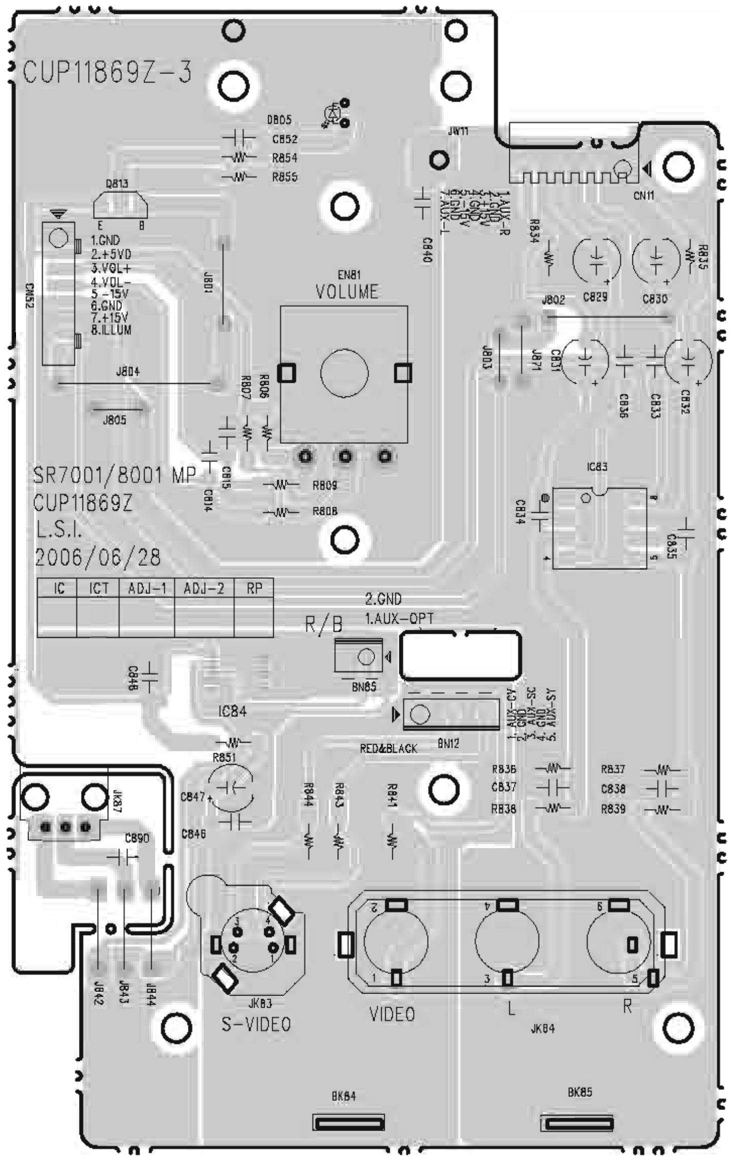


鉛フリー半田
半田付けには、鉛フリー半田 (Sn-Ag-Cu) を使用してください。

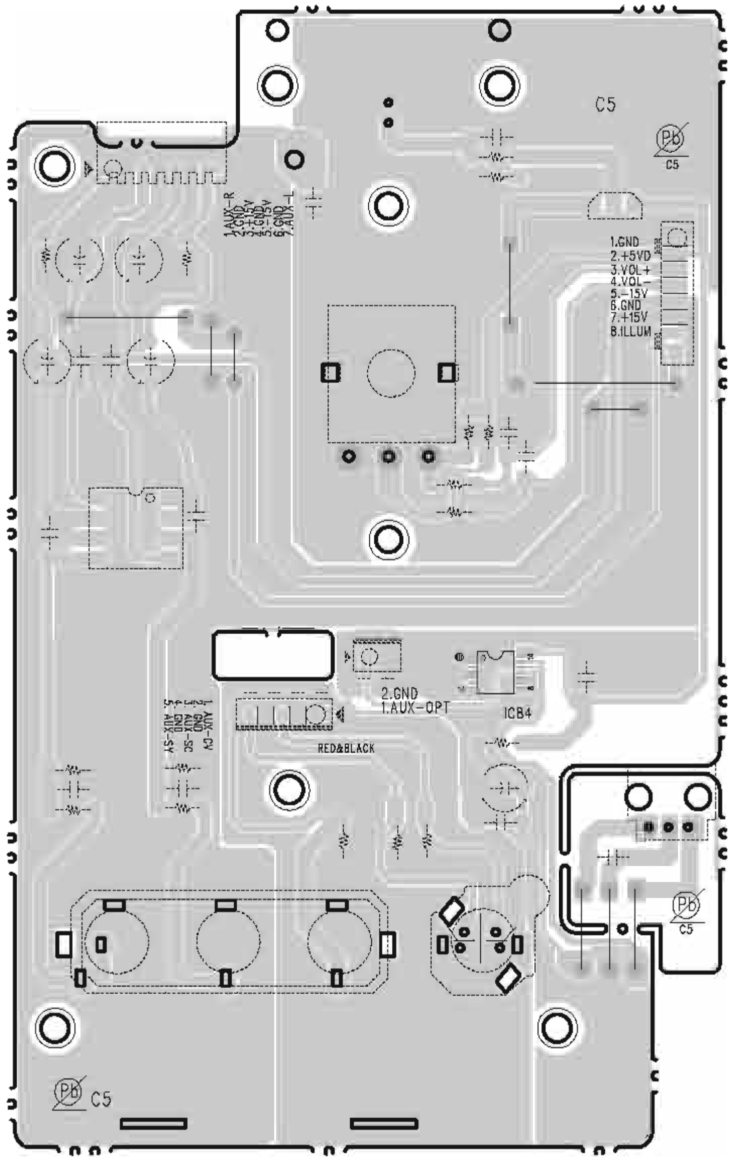
Lead-free Solder
When soldering, use the Lead-free Solder (Sn-Ag-Cu).

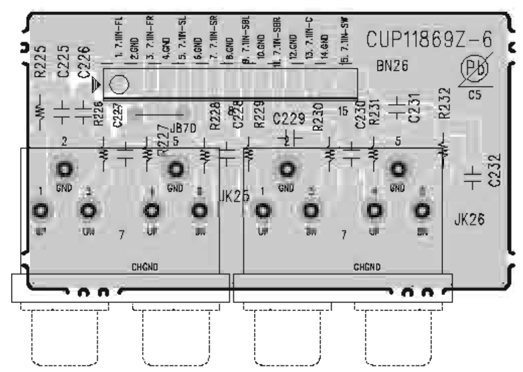
Q813

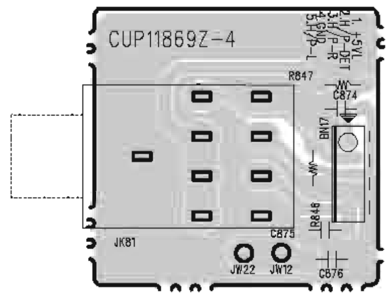
IC83

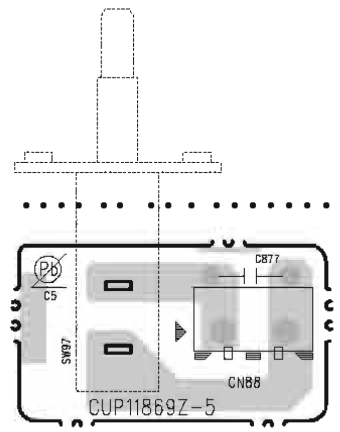


IC84

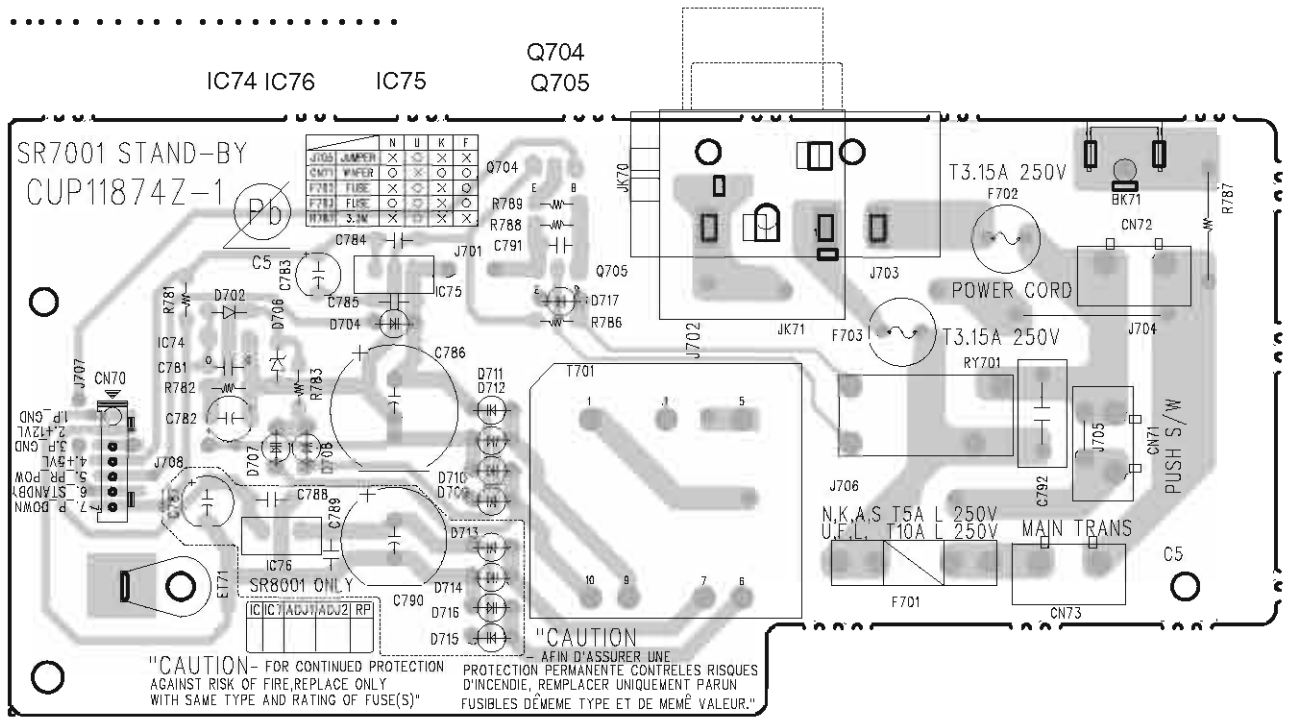




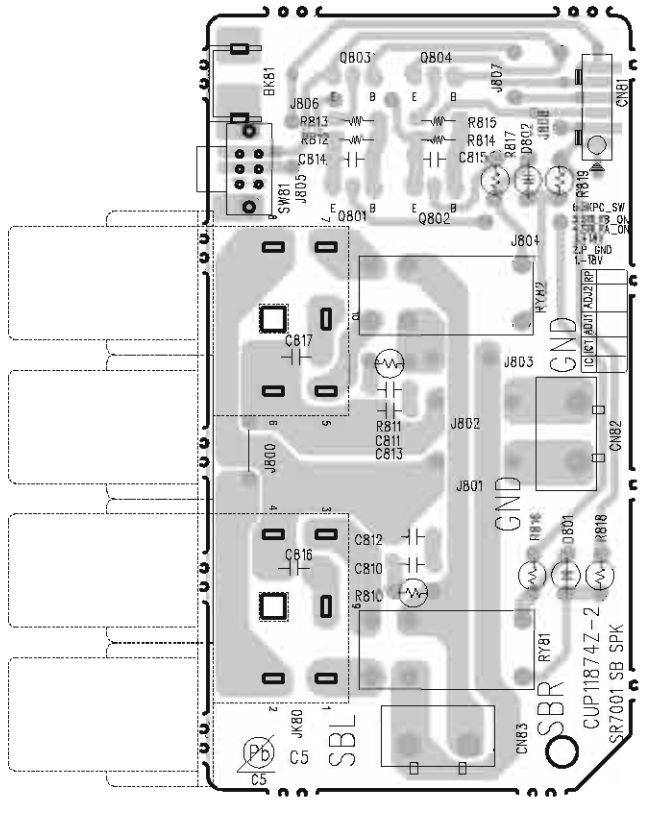


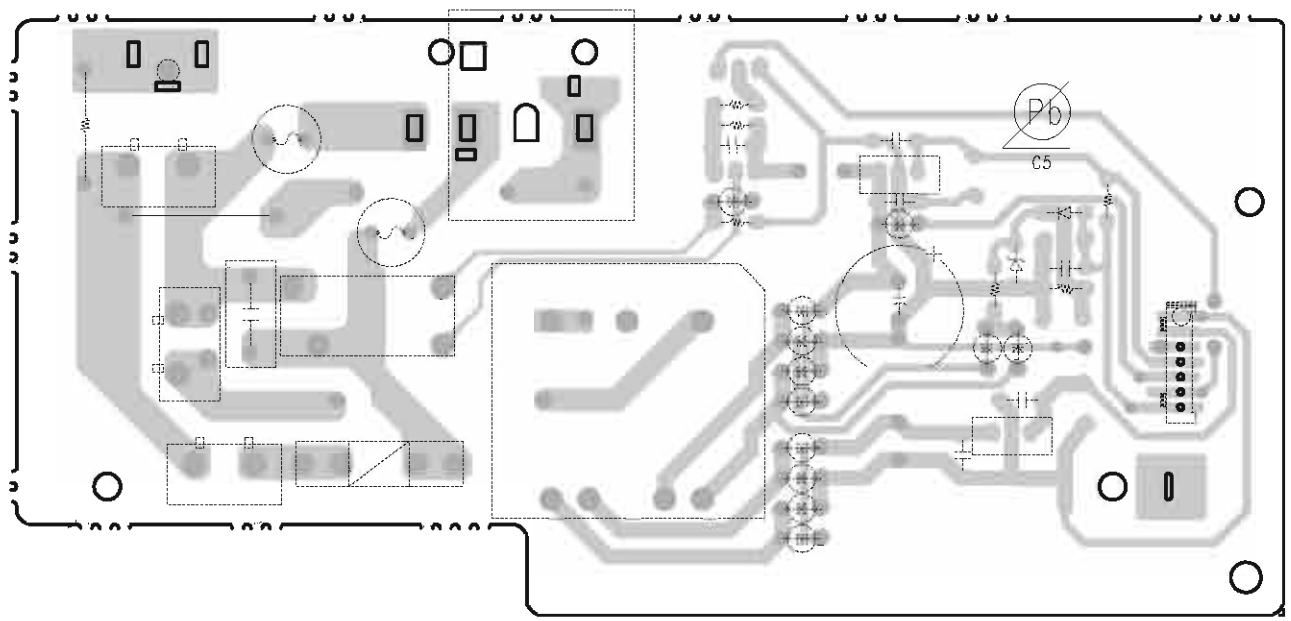


IC74 IC76 IC75 Q704 Q705

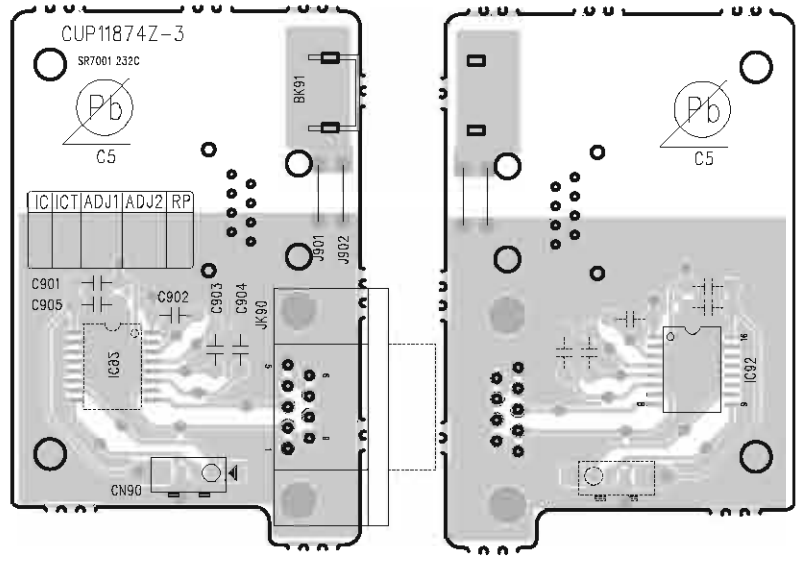


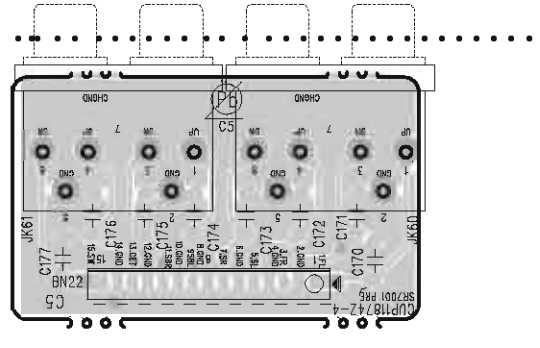
Q803 Q804
Q801 Q802





IC92

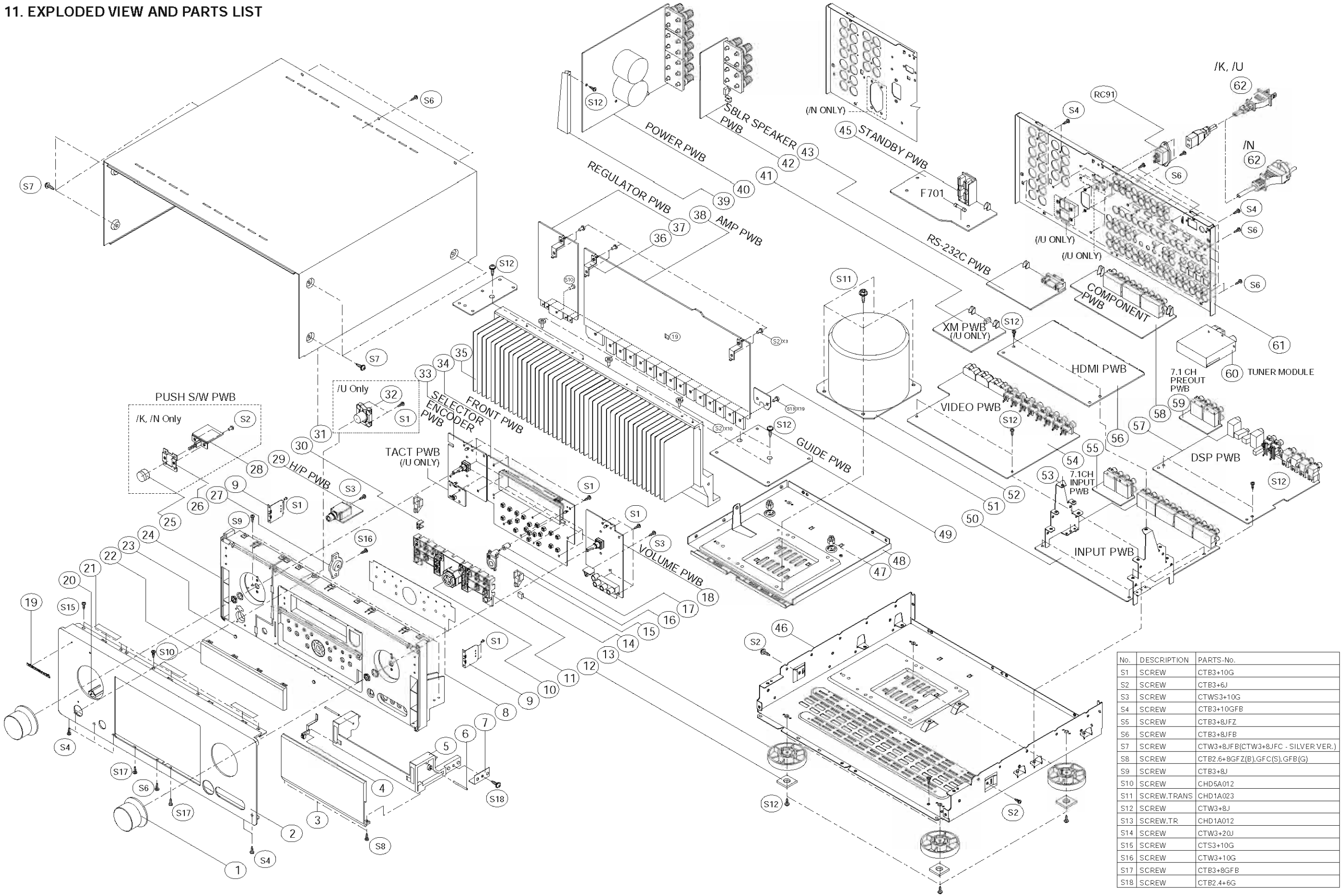




鉛フリ ー半田
半田付けには、鉛フリ ー半田 (Sn-Ag-Cu) を使用してく ださい。

Lead-free Solder
When soldering, use the Lead-free Solder (Sn-Ag-Cu).

11. EXPLODED VIEW AND PARTS LIST



No.	DESCRIPTION	PARTS-No.
S1	SCREW	CTB3+10G
S2	SCREW	CTB3+6J
S3	SCREW	CTWS3+10G
S4	SCREW	CTB3+10GFB
S5	SCREW	CTB3+8JFZ
S6	SCREW	CTB3+8JFB
S7	SCREW	CTW3+8JFB(CTW3+8JFC - SILVER VER.)
S8	SCREW	CTB2.6+8GFZ(B),GFC(S),GFB(G)
S9	SCREW	CTB3+8J
S10	SCREW	CHD5A012
S11	SCREW,TRANS	CHD1A023
S12	SCREW	CTW3+8J
S13	SCREW,TR	CHD1A012
S14	SCREW	CTW3+20J
S15	SCREW	CTS3+10G
S16	SCREW	CTW3+10G
S17	SCREW	CTB3+8GFB
S18	SCREW	CTB2.4+6G

P.W.B. NAME	POS. NO.	VERS. COLOR	PART NO. (FOR EUR)	PART NO. (MZ)	PART NAME	DESCRIPTION	
	1	/N1B	00M28AW154010	00M28AW154010	KNOB	MASTER KNOB (BLACK)	HGK1A090YA
	1	/N1G	00M28AW154020	00M28AW154020	KNOB	MASTER KNOB (GOLD)	HGK1A090ZA
	1	/N1S	00M28AW154030	00M28AW154030	KNOB	MASTER KNOB (SILVER)	HGK1A090XA
	1	/U1B	nsp	00M28AW154010	KNOB	MASTER KNOB (BLACK)	HGK1A090YA
	2	/N1B	00M06CW248010	00M06CW248010	PANEL	FRONT AL PANEL (BLACK)	CKM1A159QC23
	2	/N1G	00M06CW248110	00M06CW248110	PANEL	FRONT AL PANEL (GOLD)	CKM1A159QC24
	2	/N1S	00M06CW248210	00M06CW248210	PANEL	FRONT AL PANEL (SILVER)	CKM1A159QC40
	2	/U1B	nsp	00M06CW248020	PANEL	FRONT AL PANEL (BLACK)	CKM1A159PC23
	3	/N1B	00M05CW162010	00M05CW162010	DOOR	DOOR FRONT (AL) BLACK	CKM1A160ZC23
	3	/N1G	00M05CW162110	00M05CW162110	DOOR	DOOR FRONT (AL) GOLD	CKM1A160YC24
	3	/N1S	00M05CW162210	00M05CW162210	DOOR	DOOR FRONT (AL) SILVER	CKM1A160YC40
	3	/U1B	nsp	00M05CW162010	DOOR	DOOR FRONT (AL) BLACK	CKM1A160ZC23
	4		nsp	nsp	CONTACTOR	EARTH PLATE	CMC1A251
	5	/N1B	00M05CW271050	00M05CW271050	HOLDER	DOOR HOLDER BLACK	CKG2A046R4K92
	5	/N1G	00M05CW271110	00M05CW271110	HOLDER	DOOR HOLDER GOLD	CKG2A046RFD4
	5	/N1S	00M05CW271210	00M05CW271210	HOLDER	DOOR HOLDER SILVER	CKG2A046R6G13
	5	/U1B	nsp	00M05CW271050	HOLDER	DOOR HOLDER BLACK	CKG2A046R4K92
	6		00M10BW112010	00M10BW112010	SHAFT	SHAFT BASE	CDF1A018
	7		00M10BW104010	00M10BW104010	RETAINER	BRACKET BASE	CMD1A542
	8	/N1B	00M05CW063010	00M05CW063010	ESCUTCHEON	FRONT COVER BLACK	CGX1A358V
	8	/N1G	00M05CW063110	00M05CW063110	ESCUTCHEON	FRONT COVER GOLD	CGX1A358T
	8	/N1S	00M05CW063210	00M05CW063210	ESCUTCHEON	FRONT COVER SILVER	CGX1A358U
	8	/U1B	nsp	00M05CW063010	ESCUTCHEON	FRONT COVER BLACK	CGX1A358V
	9		nsp	nsp	BRACKET	SIDE BRACKET	CMD2A443
	10	/N1B	00M10BW270010	00M10BW270010	BUTTON	CURSOR BUTTON BLACK	CBT1A957ZK92
	10	/N1G	00M10BW270110	00M10BW270110	BUTTON	CURSOR BUTTON GLOD	CBT1A957RFZD4
	10	/N1S	00M10BW270210	00M10BW270210	BUTTON	CURSOR BUTTON SILVER	CBT1A957R6ZG13
	10	/U1B	nsp	00M10BW270010	BUTTON	CURSOR BUTTON BLACK	CBT1A957ZK92
	11	/N1B	00M10BW270020	00M10BW270020	BUTTON	FUNCTION BUTTON BLACK	CBT1A958K92
	11	/N1G	00M10BW270120	00M10BW270120	BUTTON	FUNCTION BUTTON GOLD	CBT1A958RFD4
	11	/N1S	00M10BW270220	00M10BW270220	BUTTON	FUNCTION BUTTON SILVER	CBT1A958R6G13
	11	/U1B	nsp	00M10BW270020	BUTTON	FUNCTION BUTTON BLACK	CBT1A958K92
	12		00M11BW056010	00M11BW056010	BUFFER	RUBBER CUSHION	KHG1A050
	13	/N1B	00M243W057010	00M243W057010	LEG	LEG GOLD/BLACK	CKL2A042H11
	13	/N1G	00M243W057010	00M243W057010	LEG	LEG GOLD/BLACK	CKL2A042H11
	13	/N1S	00M243W057210	00M243W057210	LEG	LEG FOR SILVER	CKL2A042H46
	13	/U1B	nsp	00M243W057010	LEG	LEG GOLD/BLACK	CKL2A042H11
	14		00M10BW305010	00M10BW305010	MAGNET	MAGNET BASE	CJC1A008
	15		00M05CW355050	00M05CW355050	LENS	INDICATOR VOL/SELECTOR	CGL1A249
	16		nsp	nsp	HOLDER	HOLDER INDICATOR VOL/SEL	CKG1A048R4K92
	17		00M03CW355010	00M03CW355010	LENS	HDMI INDICATOR	CGL1A245
	18	/N1B	nsp	nsp	PWB ASSY	VOLUME PWB ASSY	COP11869H
	18	/N1G	nsp	nsp	PWB ASSY	VOLUME PWB ASSY	COP11869H
	18	/N1S	nsp	nsp	PWB ASSY	VOLUME PWB ASSY	COP11869J
	18	/U1B	nsp	nsp	PWB ASSY	VOLUME PWB ASSY	COP11869I
	19	/N1B	00M24AW251010	00M24AW251010	BADGE	NEW MZ BADGE	CGB1A117
	19	/N1G	00M24AW251010	00M24AW251010	BADGE	NEW MZ BADGE	CGB1A117
	19	/N1S	00M24AW251020	00M24AW251020	BADGE	NEW MZ BADGE SILVER	CGB1A117G
	19	/U1B	nsp	00M24AW251010	BADGE	NEW MZ BADGE	CGB1A117
	20		00M10BW355010	00M10BW355010	LENS	INDICATOR POWER	CGL1A231
	21		nsp	nsp	TAPE	TAPE HEMELON	KHS1A032
	22		00M05CW158010	00M05CW158010	WINDOW	WINDOW FIP	CGU1A359Y
	23		00M446T056010	00M446T056010	BUFFER	CUSHION DOOR	CHG1A296Y
	24	/N1B	00M05CW105020	00M05CW105020	CHASSIS	FRONT MOLD CHASSIS (BLACK)	CGW2A390R4K92
	24	/N1G	00M05CW105120	00M05CW105120	CHASSIS	FRONT MOLD CHASSIS (GOLD)	CGW2A390RFD4
	24	/N1S	00M05CW105220	00M05CW105220	CHASSIS	FRONT MOLD CHASSIS (SILVER)	CGW2A390R6G13
	24	/U1B	nsp	00M05CW105020	CHASSIS	FRONT MOLD CHASSIS (BLACK)	CGW2A390R4K92
	25	/N1B	00M27AW270040	00M27AW270040	BUTTON	POWER SW BUTTON (BLACK)	CBC1A146K92
	25	/N1G	00M27AW270140	00M27AW270140	BUTTON	POWER SW BUTTON (GOLD)	CBC1A146RFD4
	25	/N1S	00M27AW270240	00M27AW270240	BUTTON	POWER SW BUTTON (SILVER)	CBC1A146R6G13
	26	/N1B	nsp	nsp	BRACKET	POWER SW BRACKET	CMD1A493
	26	/N1G	nsp	nsp	BRACKET	POWER SW BRACKET	CMD1A493
	26	/N1S	nsp	nsp	BRACKET	POWER SW BRACKET	CMD1A493
	27		00M391H130030	00M391H130030	DAMPER	DUMPER ASSY	KDG1A006Z
	28		nsp	nsp	PWB ASSY	PUSH S/W PWB ASSY	COP11869Z
	29		nsp	nsp	PWB ASSY	H/P PWB ASSY	CUP11869Z
	30		00M10BW355020	00M10BW355020	LENS	INDICATOR THX	CGL1A232

NOTE "nsp" PART IS LISTED FOR REFERENCE ONLY, MARANTZ WILL NOT SUPPLY THESE PARTS

P.W.B. NAME	POS. NO.	VERS. COLOR	PART NO. (FOR EUR)	PART NO. (MZ)	PART NAME	DESCRIPTION	
	32	/U1B	nsp	00M27AW270030	BUTTON	POWER SW BUTTON TACT (BLACK)	CBT1A877K92
	33	/N1B	nsp	nsp	PWB ASSY	SELECTOR ENCODER PWB ASSY	COP11869H
	33	/N1G	nsp	nsp	PWB ASSY	SELECTOR ENCODER PWB ASSY	COP11869H
	33	/N1S	nsp	nsp	PWB ASSY	SELECTOR ENCODER PWB ASSY	COP11869J
	33	/U1B	nsp	nsp	PWB ASSY	SELECTOR ENCODER PWB ASSY	COP11869I
	34	/N1B	nsp	nsp	PWB ASSY	FRONT PWB ASSY	COP11869H
	34	/N1G	nsp	nsp	PWB ASSY	FRONT PWB ASSY	COP11869H
	34	/N1S	nsp	nsp	PWB ASSY	FRONT PWB ASSY	COP11869J
	34	/U1B	nsp	nsp	PWB ASSY	FRONT PWB ASSY	COP11869I
	35		nsp	nsp	HEATSINK	HEATSINK	CMY1A263ZA
	36		nsp	nsp	BRACKET	BRACKET FOR POWER AMP PWB	CMD1A490
	37		nsp	nsp	PWB ASSY	REGULATOR PWB ASSY	COP11876B
	38		nsp	nsp	PWB ASSY	AMP PWB ASSY	COP11870H
	39		nsp	nsp	BRACKET	BRACKET PWB AG-D9320	CMD1A398
	40	/N1B	nsp	nsp	PWB ASSY	POWER PWB ASSY	COP11873H
	40	/N1G	nsp	nsp	PWB ASSY	POWER PWB ASSY	COP11873H
	40	/N1S	nsp	nsp	PWB ASSY	POWER PWB ASSY	COP11873H
	40	/U1B	nsp	nsp	PWB ASSY	POWER PWB ASSY	COP11873I
	41	/U1B	nsp	nsp	PWB ASSY	XM PWB ASSY	COP11877C
	42	/N1B	nsp	nsp	PWB ASSY	SBLR SPEAKER PWB ASSY	COP11874H
	42	/N1G	nsp	nsp	PWB ASSY	SBLR SPEAKER PWB ASSY	COP11874H
	42	/N1S	nsp	nsp	PWB ASSY	SBLR SPEAKER PWB ASSY	COP11874H
	42	/U1B	nsp	nsp	PWB ASSY	SBLR SPEAKER PWB ASSY	COP11874I
	43	/N1B	nsp	nsp	PWB ASSY	RS-232 PWB ASSY	COP11874H
	43	/N1G	nsp	nsp	PWB ASSY	RS-232 PWB ASSY	COP11874H
	43	/N1S	nsp	nsp	PWB ASSY	RS-232 PWB ASSY	COP11874H
	43	/U1B	nsp	nsp	PWB ASSY	RS-232 PWB ASSY	COP11874I
	45	/N1B	nsp	nsp	PWB ASSY	STANDBY PWB ASSY	COP11874H
	45	/N1G	nsp	nsp	PWB ASSY	STANDBY PWB ASSY	COP11874H
	45	/N1S	nsp	nsp	PWB ASSY	STANDBY PWB ASSY	COP11874H
	45	/U1B	nsp	nsp	PWB ASSY	STANDBY PWB ASSY	COP11874I
	46		nsp	nsp	CHASSIS	CHASSIS BOTTOM	CUA1A264CC
	47		nsp	nsp	HOLDER	HOLDER PWB	CHE170
	48		nsp	nsp	BRACKET	BRACKET MAIN TRANSF.	CMD1A581
	49		nsp	nsp	PWB ASSY	GUIDE PWB ASSY	
	50		nsp	nsp	PWB ASSY	INPUT PWB ASSY	COP11871H
	51		00M10BW109010	00M10BW109010	SHIELD	BRACKET SHIELD	CMC1A252Z
⚠	52	/N1B	90M-TS002960R	90M-TS002960R	TRANSF.	! TROIDAL POWER TRANSF. N	CLT5Z016ZE
⚠	52	/N1G	90M-TS002960R	90M-TS002960R	TRANSF.	! TROIDAL POWER TRANSF. N	CLT5Z016ZE
⚠	52	/N1S	90M-TS002960R	90M-TS002960R	TRANSF.	! TROIDAL POWER TRANSF. N	CLT5Z016ZE
⚠	52	/U1B	nsp	90M-TS002970R	TRANSF.	! TROIDAL POWER TRANSF. U	CLT5Z016ZU
	53		nsp	nsp	BRACKET	BRACKET MULTI PWB	CMD1A582
	54	/N1B	nsp	nsp	PWB ASSY	VIDEO PWB ASSY	COP11873H
	54	/N1G	nsp	nsp	PWB ASSY	VIDEO PWB ASSY	COP11873H
	54	/N1S	nsp	nsp	PWB ASSY	VIDEO PWB ASSY	COP11873H
	54	/U1B	nsp	nsp	PWB ASSY	VIDEO PWB ASSY	COP11873I
	55	/N1B	nsp	nsp	PWB ASSY	7.1CH PREOUT PWB ASSY	COP11874H
	55	/N1G	nsp	nsp	PWB ASSY	7.1CH PREOUT PWB ASSY	COP11874H
	55	/N1S	nsp	nsp	PWB ASSY	7.1CH PREOUT PWB ASSY	COP11874H
	55	/U1B	nsp	nsp	PWB ASSY	7.1CH PREOUT PWB ASSY	COP11874I
	56		nsp	nsp	PWB ASSY	HDMI PWB ASSY	COP11875H
	57	/N1B	nsp	nsp	PWB ASSY	DSP PWB ASSY	COP11872H
	57	/N1G	nsp	nsp	PWB ASSY	DSP PWB ASSY	COP11872H
	57	/N1S	nsp	nsp	PWB ASSY	DSP PWB ASSY	COP11872H
	57	/U1B	nsp	nsp	PWB ASSY	DSP PWB ASSY	COP11872I
	58		nsp	nsp	PWB ASSY	COMPONENT PWB ASSY	COP11894C
	59	/N1B	nsp	nsp	PWB ASSY	7.1CH INPUT PWB ASSY	COP11869H
	59	/N1G	nsp	nsp	PWB ASSY	7.1CH INPUT PWB ASSY	COP11869H
	59	/N1S	nsp	nsp	PWB ASSY	7.1CH INPUT PWB ASSY	COP11869J
	59	/U1B	nsp	nsp	PWB ASSY	7.1CH INPUT PWB ASSY	COP11869I
	60	/N1B	90M-AV000400R	90M-AV000400R	TUNER	TUNER MODULE (EUR)	CNVMB114MA18L
	60	/N1G	90M-AV000400R	90M-AV000400R	TUNER	TUNER MODULE (EUR)	CNVMB114MA18L
	60	/N1S	90M-AV000400R	90M-AV000400R	TUNER	TUNER MODULE (EUR)	CNVMB114MA18L
	60	/U1B	nsp	90M-AV000410R	TUNER	TUNER MODULE (USA)	CNVMB014MA08L
	61	/N1B	nsp	nsp	PANEL	REAR PANEL SR8001 N	CKF6A306Z
	61	/N1G	nsp	nsp	PANEL	REAR PANEL SR8001 N	CKF6A306Z
	61	/N1S	nsp	nsp	PANEL	REAR PANEL SR8001 N	CKF6A306Z

NOTE "nsp" PART IS LISTED FOR REFERENCE ONLY, MARANTZ WILL NOT SUPPLY THESE PARTS

P.W.B. NAME	POS. NO.	VERS. COLOR	PART NO. (FOR EUR)	PART NO. (MZ)	PART NAME	DESCRIPTION	
	61	/U1B	nsp	nsp	PANEL	REAR PANEL SR8001 U	CKF7A306Z
	JW14		90M-YU002390R	90M-YU002390R	FPC	21P 100MM FPC	CWC1B4A21A100B
	JW15		90M-YU002410R	90M-YU002410R	FPC	17P 100MM FPC	CWC1C4A17B100B
	JW16		90M-YU002400R	90M-YU002400R	FPC	21P 300MM FPC	CWC1B4A21A300A
	JW17		90M-YU002430R	90M-YU002430R	FPC	15P 100MM FPC	CWC3B4A15A100A
	JW18		90M-YU002450R	90M-YU002450R	FPC	25P 170MM FPC	CWC3B4A25A170B
	JW20	/U1B	nsp	90M-YU002460R	FPC	15P 150MM FPC	CWC3C4A15B150B
	JW21	/N1B	nsp	nsp	CORD	WIRE ASSY	CWB4F232500UU
	JW21	/N1G	nsp	nsp	CORD	WIRE ASSY	CWB4F232500UU
	JW21	/N1S	nsp	nsp	CORD	WIRE ASSY	CWB4F232500UU
	JW23		nsp	nsp	CORD	WIRE ASSY	CWZSR7001BN92A
	JW24		90M-YU002380R	90M-YU002380R	FPC	17P 80MM FPC	CWC1B4A17A080A
	JW25		90M-YU002420R	90M-YU002420R	FPC	11P 130MM FPC	CWC3B4A11A130A
	JW26		90M-YU002440R	90M-YU002440R	FPC	17P 170MM FPC	CWC3B4A17A170B
	JW27	/U1B	nsp	90M-YU001880R	FPC	15P 200MM FPC	CWC1C4A15B200B
	JW28	/N1B	90M-YU001890R	90M-YU001890R	FPC	17P 200MM FPC	CWC1C4A17B200B
	JW28	/N1G	90M-YU001890R	90M-YU001890R	FPC	17P 200MM FPC	CWC1C4A17B200B
	JW28	/N1S	90M-YU001890R	90M-YU001890R	FPC	17P 200MM FPC	CWC1C4A17B200B
	▲ RC91		90M-YJ002690R	90M-YJ002690R	TERMINAL	! R-301(187-2P) 10A/250V	HJJ8A001Z
			90M-FC500120R	90M-FC500120R	FERRITE CORE	FERRITE CORE	CLZ9Z070Z
			90M-FC500130R	90M-FC500130R	FERRITE CORE	FERRITE CORE	CLZ9Z071Z
			90M-FC500040R	90M-FC500040R	FERRITE CORE	FERRITE CORE(21.2X6.4X12.7) K5C T	CLZ9Z028Z
			90M-FC500030R	90M-FC500030R	FERRITE CORE	FERRITE RING 29X7.7X19	CLZ9W003Z
			nsp	nsp	CORD	WIRE ASSY	CWZSR7001BN92
PACKING							
		/N1B	00M06CW851310	00M06CW851310	USER GUIDE	USER GUIDE SR8001 N	CQX1A1093Z
		/N1G	00M06CW851310	00M06CW851310	USER GUIDE	USER GUIDE SR8001 N	CQX1A1093Z
		/N1S	00M06CW851310	00M06CW851310	USER GUIDE	USER GUIDE SR8001 N	CQX1A1093Z
		/U1B	nsp	00M06CW851250	USER GUIDE	USER GUIDE SR8001 U	CQX1A1094Z
			00MZK06CW0010	00MZK06CW0010	UNIT KIT	REMOTE CONTROLLER RC8001SR	CARTSR8001
	▲ 62	/N1B	90M-ZC000320R	90M-ZC000320R	MAINS CORD	! MAINS CORD 2WIRE 10A/250V	CJA2B054Z
	▲ 62	/N1G	90M-ZC000320R	90M-ZC000320R	MAINS CORD	! MAINS CORD 2WIRE 10A/250V	CJA2B054Z
	▲ 62	/N1S	90M-ZC000320R	90M-ZC000320R	MAINS CORD	! MAINS CORD 2WIRE 10A/250V	CJA2B054Z
	▲ 62	/U1B	nsp	90M-ZC000310R	MAINS CORD	! MAINS CORD UL 032508/12	CJA2A070Z
			00M05CW009010	00M05CW009010	MICROPHONE	MIC AUDYSSEY	CMICROSR8001
NOT STANDARD SPARE PART							
			nsp	00M06CW801010	PACKING CASE	PACKING CASE SR8001	CPG1A807W
		/N1B	nsp	00M06CW805010	MASS CARTON	SR8001 MASTER PKG	CPG1A808Y
		/N1G	nsp	00M06CW805010	MASS CARTON	SR8001 MASTER PKG	CPG1A808Y
		/N1S	nsp	00M06CW805010	MASS CARTON	SR8001 MASTER PKG	CPG1A808Y
			nsp	00M05CW809010	CUSHION	PAD SNOW L	CPS1A744
			nsp	00M05CW809020	CUSHION	PAD SNOW R	CPS1A745
	31	/N1B	nsp	00M05CW257010	LID	TOP COVER (BLACK)	CKC1A170K117
	31	/N1G	nsp	00M05CW257110	LID	TOP COVER (GOLD)	CKC1A170K118
	31	/N1S	nsp	00M05CW257210	LID	TOP COVER (SILVER)	CKC1A170G14
	31	/U1B	nsp	00M05CW257010	LID	TOP COVER (BLACK)	CKC1A170K117
			nsp	00M10BW067010	CAP	COVER FOR FRONT JACK	CGR1A344
			nsp	90M-ZA000240R	ANTENNA	AM LOOP ANT	CSA1A020Z
			nsp	90M-ZA000210R	ANTENNA	ANT FM WIRE (PIGTAIL)	CSA1A007

12. MICROPROCESSOR AND IC DATA

IC11 : HD64F2505

pin No	Port Name Mode7	I/O	use	STBY	Name	Port Setting		Note
						Act.	init	
1	PE5	I/O	O	I	RS232C_SW			RS232C Switch (Main CPU or HDMI CPU)
2	PE6	I/O	O	I	AFDATA	-	L	Analog Switch Data (TC94A46FG/TC9274N)
3	PE7	I/O	O	I	AFCLK	-	L	Analog Switch Clock (TC94A46FG/ TC9274N)
4	PD0	I/O	O	I	CE_TCA	H	L	Analog Switch (TC94A46FG/TC9274N)
5	PD1	I/O	O	I	_RSTDAC	L	L	Reset for DAC (CS4382)
6	PD2	I/O	O	I	_CS_DAC	L	H	DAC CHIP SELECTION (CS4382)
7	PD3	I/O	O	I	SWMUTE	H	H	SUB W SPK MUTE
8	PD4	I/O	O	I	CNTMUTE	H	H	CENTER SPK MUTE
9	PD5	I/O	O	I	SBMUTE	H	H	SRR B SPK MUTE
10	PD6	I/O	O	I	SL/SRMUTE	H	H	SL/SR SPK MUTE
11	PD7	I/O	O	I	L/RMUTE	H	H	FRONT L/R SPK MUTE
12	Vss	I	-	I	VSS	-	-	GND
13	PC0	I/O	O	I	KILLFLASH	H	L	Kill Flasher OUT
14	P1Vcc	I	YES	I	VCC	-	-	+5V'
15	PC1	I/O	O	I	S2P_DATA	-	L	4094 Data (74HC4094 x2pcs/CS4382)
16	PC2	I/O	O	I	S2P_CLK	-	L	4094 Clock (74HC4094 x2pcs/CS4382)
17	PC3	I/O	O	I	S2P_STB	-	H	4094 Strobe (74HC4094 x2pcs)
18	PC4	I/O	O	I	S2P__ENABLE	-	L	4094 Output Enable (Disable 4094 before strobe.) (74HC4094 x2pcs)
19	PC5	I/O	O	I	MULTIMUTEA	H	H	MULTI ROOM A MUTE
20	PC6	I/O	O	I	MULTIMUTEB	H	H	MULTI ROOM B MUTE
21	PC7	I/O	O	O	KILLIR	H	L	Kill to IR Input Signal
22	PB0	I/O	O	I	VOL_DATA	-	L	Ele Volume IC Data (TC9482)
23	PB1	I/O	O	I	VOL_CLK	-	L	Ele Volume IC Clock (TC9482)
24	PB2	I/O	I	I	_TU_SD	L	H	Tuner Tuned (Tuner Pack)
25	PB3	I/O	I	I	TU_ST	H		Tuner Stereo/_MONO (Tuner Pack)
26	PB4	I/O	O	I	TU_MUTE	H	H	Tuner MUTE (Tuner Pack)
27	PB5	I/O	O	I	_CE_TU	L	L	Tuner PLL CE (Tuner Pack)
28	PB6	I/O	O	I	_HDMI_LED	L	H	HDMI LED On
29	PB7	I/O	I	I	_P_AMP_FAIL	L	-	Power Amp Dectect (Open Collector)
30	PA0	I/O	O	I	TUDOUT	-	L	Tuner PLL Data Out (Tuner Pack)
31	PA1	I/O	O	I	TUCLK	-	L	Tuner PLL Clock (Tuner Pack)
32	PA2	I/O	I	I	TUDIN	-	L	Tuner PLL Data In (Tuner Pack)
33	PA3	I/O	I	I	RDS_DIN	-	L	Tuner RDS Data In (Tuner Pack)
34	PA4	I/O	O	I	_RSTFL	L	L	Front FL Driver Reset (NJU3430)
35	PA5	I/O	O	I	_CEFL	L	L	Front FL Driver Chip Select (NJU3430)
36	PA6	I/O	O	I	VOL_STB	H	L	Ele Volume IC Strobe (TC9482)
37	PA7	I/O	O	I	CLK_SW_0	-	L	_DIR/HDMI Audio Clock Select, L:DIR, H: HDMI (74VHC157)
38	PH7	I/O	O	I	CLK_SW_1	-	L	_DIR/Option Audio Clock Select, L:DIR, H: Opt (74VHC157)
39	PH6	I/O	O	I	_PCM_DSD_SEL	-	L	PCM/DSD DAC Audio input Select, L:PCM, H:DSD (74VHC157)
40	PH5	I/O	O	I	ILLUMINATION_ON_OFF	L	H	FRONT ILLUMINATION ON/OFF
41	PH4	I/O	O	I	HEAT	H	L	Power Amp±B AC_L Select
42	PH3	I/O	I	I	_HEAT_DET	H	-	Power Amp Heatsink Temp Detect
43	PH2	I/O	O	I	_STANDBY	L	L	Standby Power
44	PH1	I/O	I	I	_HP_DET	L	H	HP Jack Detect
45	PH0	I/O	O	I	HP_ON	H	L	HEAD PHONE ON
46	PJ7	I/O	SO	O	OSDDATA	-	L	Front FL, Video (OSD), 4094 Data (NJM3430/LC74781/74HC4094 x3pcs)
47	PJ6	I/O	O	I	DC_OUT1	L	H	DC Triger 1
48	PJ5	I/O	SC	I	OSDCLK	-	L	Front FL, Video (OSD), 4094 Clock (NJM3430/LC74781/74HC4094 x3pcs)
49	PJ4	I/O	O	I	DC_OUT2	L	H	DC Triger 2

IC11 : HD64F2505

pin No	Port Name Mode7	I/O	use	STBY	Name	Port Setting		Note
						Act.	init	
50	PJ3	I/O	O	I	_CEDIR	L	L	DIR Chip Enable (LC89057W)
51	PJ2	I/O	O	I	_DIR_RST	L	L	DIR Reset (LC89057W)
52	PJ1	I/O	O	O	_STBY_LED	L	H	Standby LED On
53	PJ0	I/O	O	I	_RSFL	L	L	Front FL Driver Register Selection (NJU3430)
54	Vss	I	-	I	VSS	-	-	GND
55	P97/AN15/ DA1	I,I,O	I	I	MIC_DETECT	L	H	MIC Jack Detection for MRAC
56	P96/AN14/ DA0	I,I,O	I	I	SPKC_SW	L	-	Speaker C Switch (Slide SW)
57	P95/AN13	I,I	I	I	DEC_INT	-	-	VIDEO DEC Interrupt (ADV7401)
58	P94/AN12	I,I	I	I	SEL-	L	H	Front Select Knob Encoder -
59	P93/AN11	I,I	I	I	SEL+	L	H	Front Select Knob Encoder +
60	P92/AN10	I,I	I	I	VOL-	L	H	Front Vol. Knob Encoder -
61	P91/AN9	I,I	I	I	VOL+	L	H	Front Vol. Knob Encoder +
62	P90/AN8	I,I	I	I	_OVFL	-	-	ADC Overflow for Peak Indicator (CS5361)
63	P47/AN7	I,I	I	I	TV_AUTO	-	-	TV Video Detect
64	P46/AN6	I,I	AD	AD	MODE2	-	-	CPU mode 2
65	P45/AN5	I,I	AD	AD	MODE1	-	-	CPU mode 1
66	P44/AN4	I,I	AD	AD	P_LINE_FAIL	-	-	Emergency Protection
67	AVss	I	-	I	AVSS	-	-	GND
68	P43/AN3	I,I	AD	AD	_5V_DOWN	-	-	Detect 5V
69	P42/AN2	I,I	AD	AD	KEY2	-	-	Front Button Key 2
70	P41/AN1	I,I	AD	AD	KEY1	-	-	Front Button Key 1
71	P40/AN0	I,I	AD	AD	KEY0	-	-	Front Button Key 0
72	Vref	I	YES	I	VCC	-	-	+5V'
73	AVcc	I	YES	I	AVCC	-	-	+5V'
74	P50/TxD2	I/O,O	O	I	DIR_OUT	-	-	Serial Data for DIR (LC89057W)
75	P51/RxD2	I/O,I	I	I	DIR_IN	-	-	Serial Data from DIR (LC89057W)
76	P52/SCK2	I/O,O	O	I	DIR_CLK	-	-	Serial Clock Out for DIR (LC89057W)
77	PF0/~IRQ2	I/O,I	INT	I	_P_DOWN	L	-	Power Down Detect
78	PF1/BUZZ	I/O,O	O	I	CP_SEL1			Component Video Input Select 1 (NJM2584) 1/3
79	PF2	I/O	O	I	CP_SEL2			Component Video Input Select 2 (NJM2584) 2/3
80	PF3/ ~ADTRG/ ~IRQ3	I/O,I,I	INT	I	RDS_CLK	-	-	Tuner RDS Clock (Tuner Pack)
81	PF4	I/O	O	I	CP_SEL3			Component Video Input Select 3 (NJM2584) 3/3
82	PF5	I/O	O	I	V_CONV_SEL			Component Video Monitor Select (NJM2586)
83	PF6	I/O	O	I	COMP_MUTE			Component Video Monitor Mute (NJM2586)
84	P1Vcc	I	YES	I	VCC	-	-	+5V'
85	PF7/	I/O,O	O	I	XPORT_SW			Switch of RS232C or X_PORT
86	Vss	I	-	I	VSS	-	-	GND
87	TEST	I	NO	I	TEST	-	-	GND
88	VCL	I	-	I	VCL	-	-	GND (0.47uF)
89	OSC2	I	NO	I	NC	-	-	OPEN
90	OSC1	I	NO	I	VSS	-	-	GND
91	NMI	I	NO	I	NMI	H	H	Fix : H
92	MD2	I	YES	I	MD2	H	H	Operation : H, Boot : L
93	XTAL	I	YES	I	XTAL	-	-	X'tal (20MHz)
94	Vss	I	NO	I	VSS	-	-	GND
95	EXTAL	I	YES	I	EXTAL	-	-	X'tal (20MHz)
96	Vcc	I	YES	I	VCC	-	-	+5V'
97	MD0	I	YES	I	MD0	H	H	Fix H
98	MD1	I	YES	I	MD1	H	H	Fix H
99	~STBY	I	NO	I	_STBY	L	H	Fix H

IC11 : HD64F2505

pin No	Port Name Mode7	I/O	use	STBY	Name	Port Setting		Note
						Act.	init	
100	~RES	I	YES	I	_RES	L	H	RESET
101	P20/TIOCA3	I/O,O	O	I	CPU_NMI			HDMI CPU WRITE MODE (H8/36087)
102	P21/TIOCB3	I/O,I/O	T_IN	I	IR_RECEIVER_IN	-	-	RFC
103	P22/TIOCC3	I/O,I/O	I	I	SPIO_ENA	L	H	Communication Enable from TI DSP (DA708)
104	P23/TIOCD3	I/O,I/O	O	I	_TI_RST	L	H	Reset for TI DSP (DA708)
105	P24/TIOCA4	I/O,I/O	O	I	_SPIO_SCS	L	H	Chip Select for TI DSP (DA708)
106	P25/TIOCB4	I/O,I/O	I	I	XSTATE	L	H	DIR CKST (LC89057W)
107	P26/TIOCA5	I/O,I/O	T_OUT	I	M_RC_OUT	-	L	RC BUS MULT OUT
108	P27/TIOCB5	I/O,I/O	T_IN	O	M_RC_IN	L	H	Multi RC5 In Detect Signal
109	P17/TIOCB2/ TCLKD	I/O,I/O,I/O	O	I	N.C	-	L	OPEN
110	P16/TIOCA2/ ~IRQ1	I/O,I/O,I	INT	INT	WAKEUP	↑	-	Standby Mode Release
111	P15/TIOCB1/ TCLKC	I/O,I/O,I/O	T_IN	I	VSYNC	↑	-	V-sync Det. & Change OSD (LC74781)
112	P14/TIOCA1/ ~IRQ0	I/O,I/O,I	INT	I	RERR	H	-	DIR Error (LC89057W)
113	P13/ TIOCD0/ TCLKB	I/O,I/O,I/O	T_OUT	O	RC_OUT	-	L	RC BUS OUT
114	P12/ TIOCC0/ TCLKA	I/O,I/O,I/O	O	I/O	V_SDA	-	H	I2C Data for VIDEO DEC/ENC (ADV7401/ ADV7320/CD0040AF)
115	P11/TIOCB0	I/O,I/O	O	O	V_SCL	-	H	I2C Clock for VIDEO DEC/ENC (ADV7401/ ADV7320/CD0040AF)
116	P10/TIOCA0	I/O,I/O	T_IN	I	RC_IN	↑↓	-	IR In for RC-5
117	Vss	I	YES	I	VSS	-	-	GND
118	P2Vcc	I	YES	I	VCC	-	-	+3.3V'
119	P37/TxD4	I/O,O	SO	O	XM_RXD	-	H	UART for XM Module
120	P36/RxD4	I/O,I	SI	I	XM_TXD	-	H	UART for XM Module
121	P35/SCK1/ SCK4/SCL0/ ~IRQ5	I/O,I/O,I/O,I/O,I	SC	I	CPU SCL	-	H	HDMI CPU I/F (H8/36087)
122	P34/RxD1/ SDA0	I/O,I,I/O	SIO	I	CPU SDA	-	H	HDMI CPU I/F (H8/36087)
123	P33/TxD1/ SCL1	I/O,O,I/O	O	I	CPU_RST	L	H	HDMI CPU Reset (H8/36087)
124	P32/SCK0/ SDA1/~IRQ4	I/O,I/O,I/O,I	INT	I	HDMI_MUTE	-	L	HDMI MUTE (Sil9033)
125	P31/RxD0	I/O,I	SI	I	RXD	-	H	UART for RS232C
126	P30/TxD0	I/O,O	SC	I	TXD	-	H	UART for RS232C
127	P77/TxD3	I/O,O	SO	I	SPIO_SIMO	-	H	Serilal Data Out for TI DSP (DA708)
128	P76/RxD3	I/O,I	SI	I	SPIO_SOMI	-	L	Serial Data In from TI DSP (DA708)
129	P75/TMO3/ SCK3	I/O,I/O,I/O	SC	I	SPIO_CLK	-	L	Serial Clock Out for TI DSP (DA708)
130	P74/TMO2/ ~MRES	I/O,O	O	O	IICCLK	-	L	I2C Clock for E2PROM (AT24C128)
131	P73/TMO1	I/O,O	I/O	I/O	IICDATA	-	L	I2C Data for E2PROM (AT24C128)
132	P72/TMO0	I/O,O	O	I	XM_CMD	H	L	DTIC mode select (XM Module)
133	P71/TMRI23/ TMCI23	I/O,O,O	O	I	XM_RST	L	L	Reset for XM DTIC (XM Module)
134	P70/TMRI01/ TMCI01	I/O,O,O	O	I	_XM_DAC_RST	L	L	DAC Reset for XM_Module (CS4392)
135	PG4	I/O	O	I	XM_MUTE	H	H	Mute On for XM Module
136	PG3	I/O	O	I	N.C	-	L	OPEN
137	PG2	I/O	O	O	N.C	-	L	OPEN
138	PG1/~IRQ7	I/O,I	INT	I	_AMUTE0	L	H	MUTE Contorol from TI DSP (DA708)
139	PG0/~IRQ6	I/O,I	INT	I	XM_IRQ	L	H	XM error detect (XM Module)
140	PE0	I/O	O		XM_ON	H	L	Control Power to XM/DT Bus (XM Module)
141	PE1	I/O	O	I	_CEEX	L	H	Serial to Parallel Expander for Video Strobe (74HC4094 x3pcs)
142	PE2	I/O	O	I	Y_OSD	H	L	Y/C_OSD_IC_BYPASS (NJM2595)
143	PE3	I/O	O	I	CVBS_OSD	H	L	CVBS_OSD_IC_BYPASS (NJM2595)
144	PE4	I/O	O	I	_CEOSD	L	H	Video Circuit (LC74781)

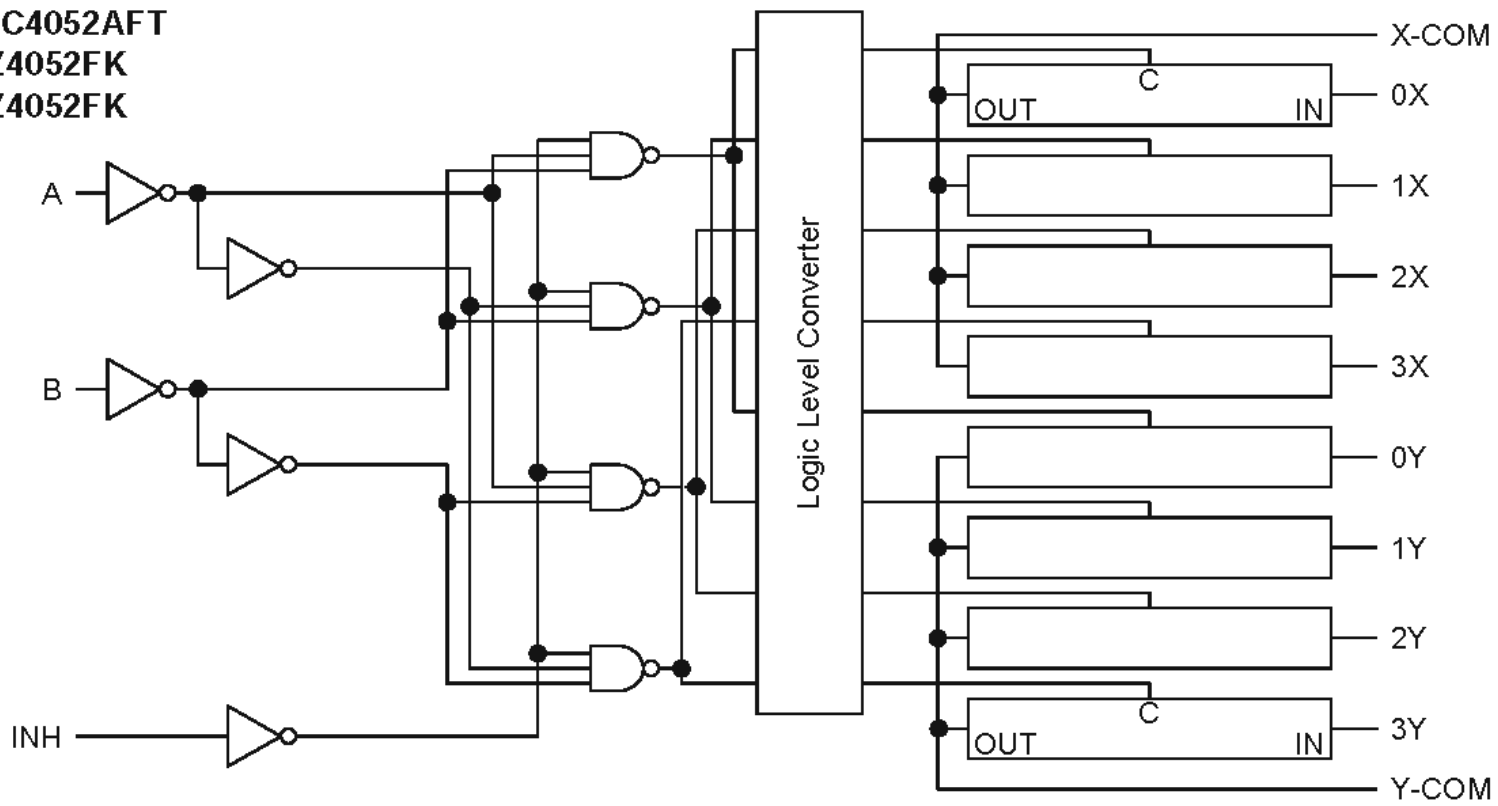
IC90 : HD64F36087HV

pin No	Port Name Mode7	I/O	use	STBY	Name	Port Setting		Note
						Act.	init	
1	PB6/AN6	I	I	I	SW6	-	-	to GND (or Temporary Pull up)
2	PB7/AN7	I	I	I	SW7	-	-	to GND (or Temporary Pull up)
3	Avcc	I	-	-				
4	X2	O	-	-				
5	X1	I	-	-				
6	Vcc	I	Vcc	-				
7	_RESET	I	_RES	-	_RST_HDMI			also use for JTAG
8	TEST	I	TEST	-				
9	Vss	I	Vss	-				
10	OSC2	O	OSC2	-	16MHz			
11	OSC1	I	OSC1	-	16MHz			
12	Vcc	I						
13	P50/_WKP0	I/O	O	I	_RST_TX1	L	H	HDMI Tx device1 Reset
14	P51/_WKP1	I/O	O	I	_RST_TX2	L	H	HDMI Tx device2 Reset
15	P34	I/O	O	I	DEBUG_O4	-	L	to Virtual Connector Land
16	P35	I/O	O	I	DEBUG_O5	-	L	to Virtual Connector Land
17	P36	I/O	O	I	DEBUG_O6	-	L	to Virtual Connector Land
18	P37	I/O	O	I	SW_VIDEO2	L	H	Select I/P Converter
19	P52/_WKP2	I/O	O	I	WP_4	L	L	Write Protect E2PROM4
20	P53/_WKP3	I/O	O	I	WP_3	L	L	Write Protect E2PROM3
21	P54/_WKP4	I/O	O	I	WP_2	L	L	Write Protect E2PROM2
22	P55/_WKP5	I/O	O	I	WP_1	L	L	Write Protect E2PROM1
23	P10/TMOW	I/O	O	I	CE_CXB2	H	L	CXB1441R 2 Chip Enable
24	P11/PWM	I/O	O	I	CE_CXB1	H	L	CXB1441R 1 Chip Enable
25	P12	I/O	O	I	SW_I2S_DSD			Switch I2S(L) or DSD(H)
26	P56/SDA	I/O	SDA	I	CPU_SDA			Commnunication to Main CPU
27	P57/SCL	I/O	SCL	I	CPU_SCL			Commnunication to Main CPU
28	P74/TMRIV	I/O	O	I	SEL_CH34	-	L	Select Input Ch. 3(L) or 4(H)
29	P75/TMCIV	I/O	O	I	SEL_CH12	-	L	Select Input Ch. 1(L) or 2(H)
30	P76/TMOV	I/O	O	I	SW_SPDIF			Sel. SPDIF Inp Rx(L) or DSP(H)
31	P24	I/O	O	I	_RST_RX	L	H	HDMI Rx device Reset
32	P63/FTIOD0	I/O	FTIOD	I	CEC_OUT	L	H	CEC Output
33	P62/FTIOC0	I/O	FTIOC	I	CEC_IN	L	-	CEC input
34	P61/FTIOB0	I/O	O	I	SW_5V2			+5V output to SINK2
35	_MNI	I	MNI		_MNI_HDMI			also use for JTAG
36	P60/FTIOA0	I/O	O	I	SW_5V1			+5V output to SINK1
37	P64/FTIOA1	I/O	O	I	HP_4			HPD switch for Input 4
38	P65/FTIOB1	I/O	O	I	HP_3			HPD switch for Input 3
39	P66/FTIOC1	I/O	O	I	HP_2			HPD switch for Input 2
40	P67/FTIOD1	I/O	O	I	HP_1			HPD switch for Input 1
41	P85	I/O			JTAG			use for JTAG (Pull up)
42	P86	I/O			JTAG			use for JTAG
43	P87	I/O			JTAG			use for JTAG
44	P20/SCK3	I/O	O	I	SW_VIDEO1	L	H	Select Video Decoder
45	P21/RXD	I/O	RXD	I	AUX_RxD			RS232C RxD for Host I/F
46	P22/TXD	I/O	TXD	I	AUX_TxD			RS232C TxD for Host I/F
47	P23	I/O	I/O	I	HDMI_SDA			I2C Line for HDMI Control
48	P70/SCK3_2	I/O	O	I	HDMI_SCL			I2C Line for HDMI Control

IC90 : HD64F36087HV

pin No	Port Name Mode7	I/O	use	STBY	Name	Port Setting		Note
						Act.	init	
49	P71/RXD_2	I/O	RXD	I	DEBUG_RxD			RS232C RxD for Debug
50	P72/TXD_2	I/O	TXD	I	DEBUG_TxD			RS232C TxD for Debug
51	P14/_IRQ0	I/O	INT	I	INT_RX	L	-	HDMI Rx device Int.
52	P15/_IRQ1	I/O	INT	I	INT_TX1	L	-	HDMI Tx device1 Int.
	/TMIB1							
53	P16/_IRQ2	I/O	INT	I	INT_TX2	L	-	HDMI Tx device2 Int.
54	P17/_IRQ3	I/O	INT	I	INT_SCDT	L	-	SCDT Int.
	/TRGV							
55	P33	I/O	O	I	DEBUG_O3	-	L	to Virtual Connector Land
56	P32	I/O	O	I	DEBUG_O2	-	L	to Virtual Connector Land
57	P31	I/O	O	I	DEBUG_O1	-	L	to Virtual Connector Land
58	P30	I/O	O	I	DEBUG_O0	-	L	to Virtual Connector Land
59	PB3/AN3	I	I	I	I_HPD_O1			HDP Input for Out1
60	PB2/AN2	I	I	I	I_HPD_O2			HDP Input for Out2
61	PB1/AN1	I	I	I	I_5V_CH34			5V Input for CH3,4
62	PB0/AN0	I	I	I	I_5V_CH12			5V Input for CH1,2
63	PB4/AN4	I	I	I	SW4			to GND (or Temporary Pull up)
64	PB5/AN5	I	I	I	SW5			to GND (or Temporary Pull up)

IC12 : TC7MZ4052FK
IC14 : TC7MZ4052FK
IC16 : TC7MZ4052FK
IC18 : TC7MZ4052FK
IC19 : TC74HC4052AFT
IC20 : TC7MZ4052FK
IC23 : TC7MZ4052FK



Control Inputs				"ON" Channel		
Inh bit	C*	B	A	MZ4051FK	MZ4052FK	MZ4053FK
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	—	0X, 0Y, 1Z
L	H	L	H	5	—	1X, 0Y, 1Z
L	H	H	L	6	—	0X, 1Y, 1Z
L	H	H	H	7	—	1X, 1Y, 1Z
H	X	X	X	None	None	None

X: Don't care, *: Except MZ4052FK

IC20 : TC74HC4094AFN
IC21 : TC74HC4094AFN
IC79 : TC74HC4094AFN
IC80 : TC74HC4094AFN
IC83 : TC74HC4094AFN

IC20

Port Name	Use	STBY	Name	V	PortSetup		Note
				Device	Act.	Int	
Q1	O	I	MIC_ENABLE	3.3-5.0V	H	L	MIC Enable for MRAC (Relay)
Q2	O	I	SPKC_CONT	5.0V	H	L	Speaker C Relay Control (Relay)
Q3	O	I	_PUREDIRECT_LED	5.0V	L	H	PURE DIRECT LED On
Q4	O	I	SBA_ON	3.3-5.0V	H	L	Surr-Back SPK A SELECT
Q5	O	I	SBB_ON	3.3-5.0V	H	L	Surr-Back SPK B SELECT
Q6	O	I	FLRA_ON	3.3-5.0V	H	L	SPK A SELECT
Q7	O	I	FLRB_ON	3.3-5.0V	H	L	SPK B SELECT
Q8	O	I	SURR_ON	3.3-5.0V	H	L	SURR/CNT SPK ON

IC21

Port Name	Use	STBY	Name	V	PortSetup		Note
				Device	Act.	Int	
Q1	O	I	DIG_SEL_A	3.3V(-5.0V)	-	L	DIGITAL INPUT SEL-A FOR DIR (74HC151 or 74VHC153)
Q2	O	I	DIG_SEL_B	3.3V(-5.0V)	-	L	DIGITAL INPUT SEL-B FOR DIR (74HC151 or 74VHC153)
Q3	O	I	Multi_A Mono/Stereo	3.3-5.0V	H	L	Multi Room Out A Mono/Stereo SELECT Mono :H Stereo : L
Q4	O	I	Multi_B Mono/Stereo	3.3-5.0V	H	L	Multi Room Out B Mono/Stereo SELECT Mono :H Stereo : L
Q5	O	I	DFS	3.3V	H	L	ADC Mode Selection 0 (CS5361)
Q6	O	I	_ATT	5.0V	L	H	Analog Audio (Lt/Rt) Input ATT
Q7	O	I	_RSTADC	3.3V	L	H	ADC Reset (CS5361)
Q8	O	I	D_A	3.3-5.0V	-	L	DIR or _ADC sel (Error Unsel) (74VHC08 to ERMUTE)

IC80

Port Name	Use	STBY	Name	V	PortSetup		Note
				Device	Act.	Int	
Q1	O	I	MCP_MUTE	5.0V	H	-	Multi Component MUTE
Q2	O	I	SE_VIDEO03	5.0V	H	-	CVBS Input Select 3 (VCR/DVD/TV/AUX) (NJM2595)
Q3	O	I	SE_VIDEO02	5.0V	H	-	CVBS Input Select 2 (VCR/DVD/TV/AUX) (NJM2595)
Q4	O	I	SE_VIDEO01	5.0V	H	-	CVBS Input Select 1 (VCR/DVD/TV/AUX) (NJM2595)
Q5	O	I	OSD_CON05	5.0V	H	-	
Q6	O	I	SE_VIDEO06	5.0V	H	-	CVBS Multi Monitor Select (Through/OSD) (NJM2244)
Q7	O	I	SE_VIDEO05	5.0V	H	-	CVBS Multi Monitor Select (Through/OSD) (NJM2244)
Q8	O	I	SE_VIDEO04	5.0V	H	-	CVBS Input Select 4 (VCR/DVD/TV/AUX) (NJM2595)

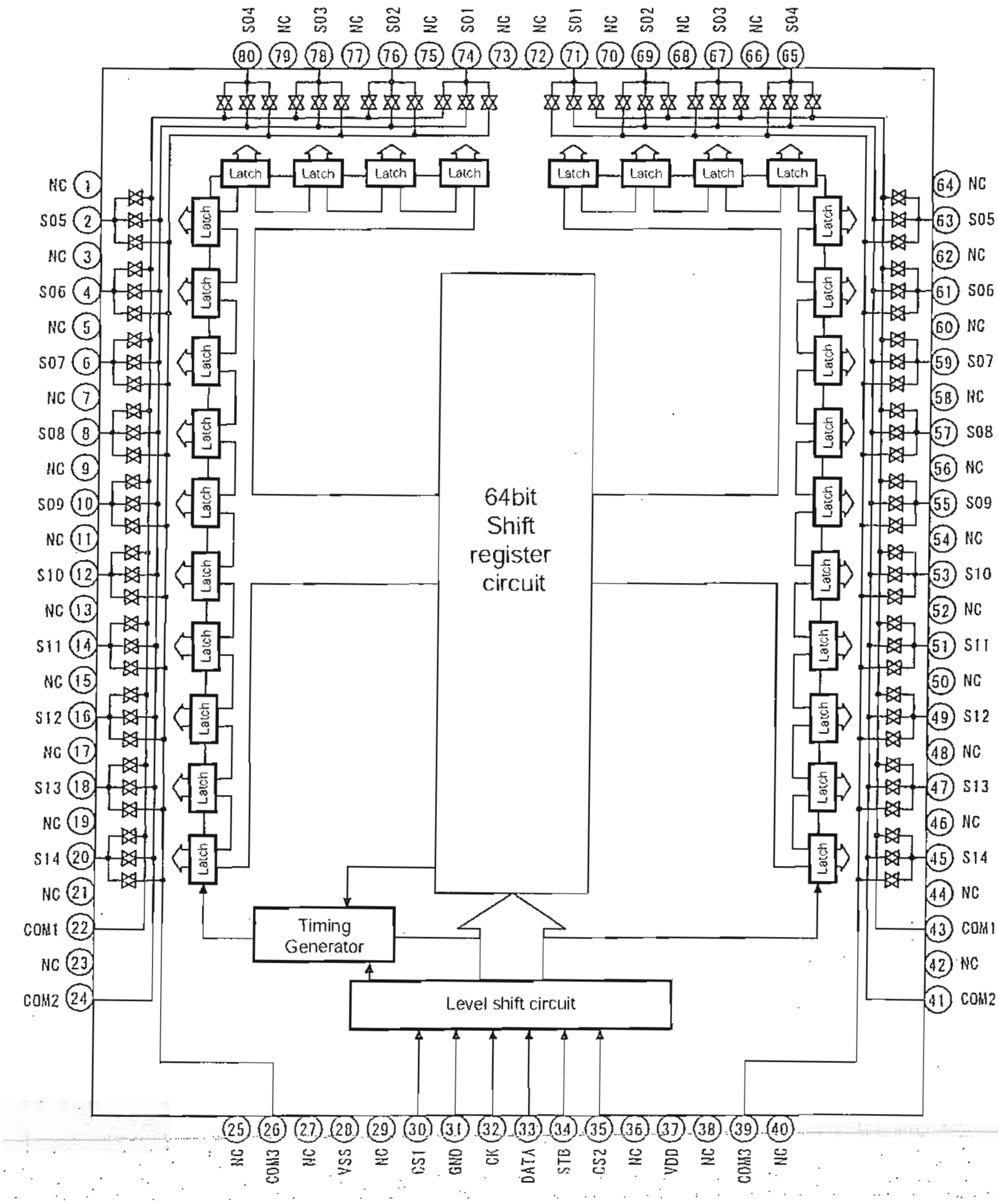
IC79

Port Name	Use	STBY	Name	V	PortSetup		Note
				Device	Act.	Int	
Q1	O	I	OSD_CON01	5.0V	H	-	CVBS & Y/C Monitor Select (Through/Converted) (NJM2244)
Q2	O	I	OSD_CON02	5.0V	H	-	OSD Sync Input Select (MJM2535/NJM2285)
Q3	O	I	OSD_CON03	5.0V	H	-	VIDEO DEC Input Select (MJM2285)
Q4	O	I	MCP_SEL4	5.0V	H	-	Multi Component SEL4
Q5	O	I	SEL_V02	5.0V	H	-	CVBS & Y/C Input Select 2 (VCR/DVD/TV/AUX) (NJM2595)
Q6	O	I	SEL_V01	5.0V	H	-	CVBS & Y/C Input Select 1 (VCR/DVD/TV/AUX) (NJM2595)
Q7	O	I	SEL_V03	5.0V	H	-	CVBS & Y/C Input Select 3 (VCR/DVD/TV/AUX) (NJM2595)
Q8	O	I	SEL_V04	5.0V	H	-	CVBS & Y/C Input Select 4 (VCR/DVD/TV/AUX) (NJM2595)

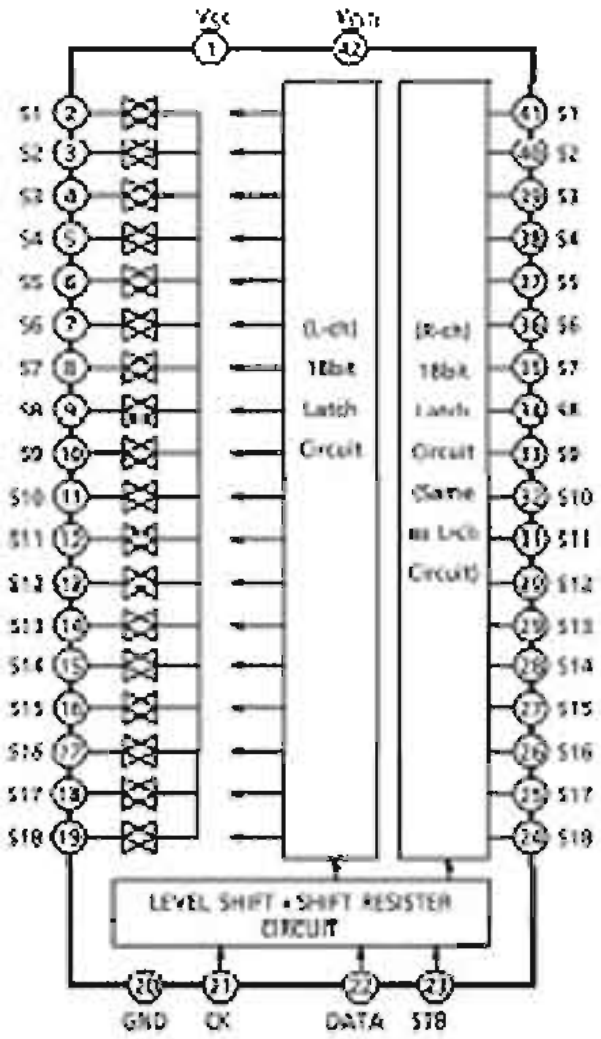
IC83

Port Name	Use	STBY	Name	V	PortSetup		Note
				Device	Act.	Int	
Q1	O	I	MCP_SEL1	5.0V	H	-	Multi Component SEL1
Q2	O	I	Y/C_SEL	5.0V	H	-	Y/C Monitor Select (Through/Converted) (NJM2244)
Q3	O	I	CVBS_SEL	5.0V	H	-	CVBS Monitor Select (Through/Converted) (NJM2244)
Q4	O	I	OSD_SEL	5.0V	H	-	SYNC SCAN Select
Q5	O	I	RST_DEC	5.0V	H	H	VIDEO DEC Reset
Q6	O	I	RST_ENC	5.0V	H	H	VIDEO ENC Reset
Q7	O	I	MCP_SEL2	5.0V	H	-	Multi Component SEL2
Q8	O	I	MCP_SEL3	5.0V	H	-	Multi Component SEL3

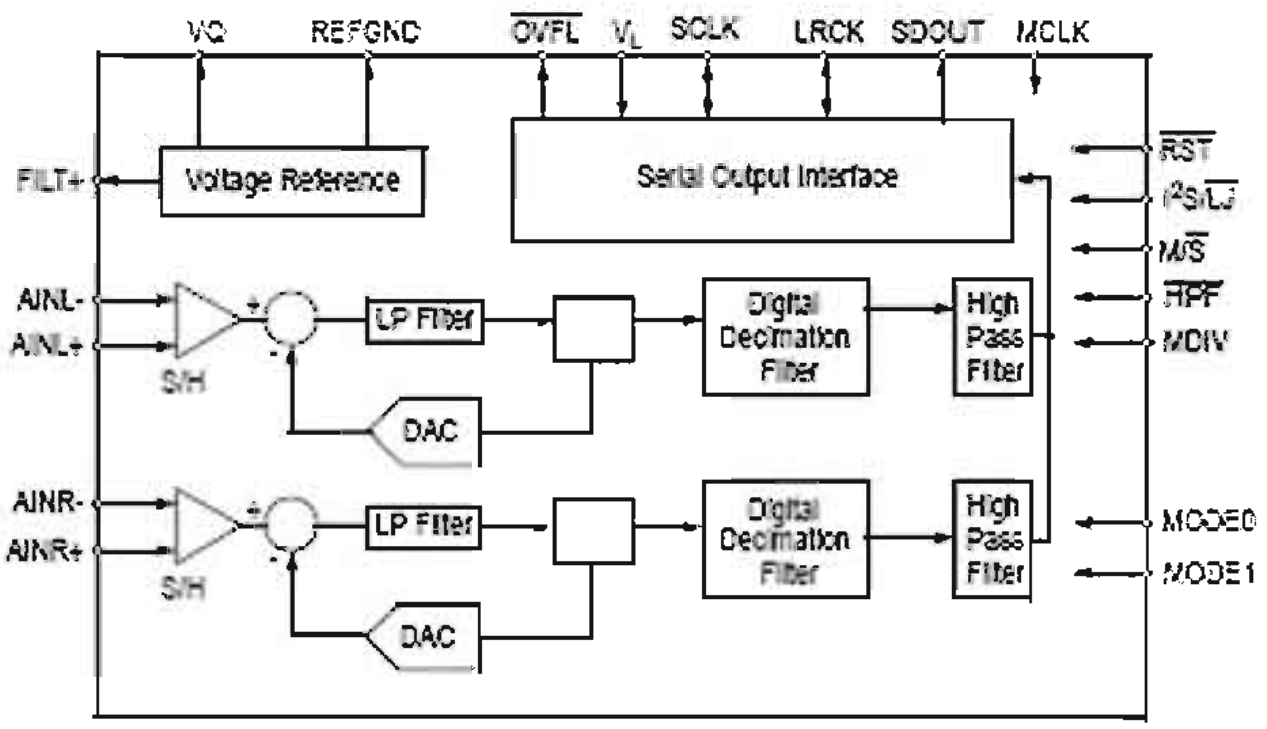
IC21 : TC94A46CFG



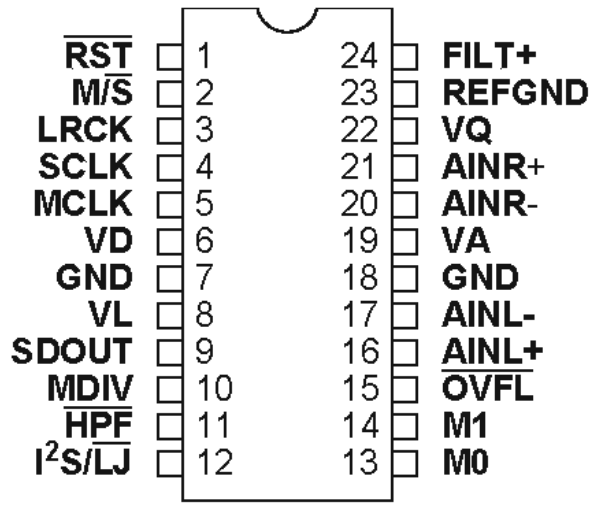
IC22 : TC9274CNG



IC27 : CS5361-KS

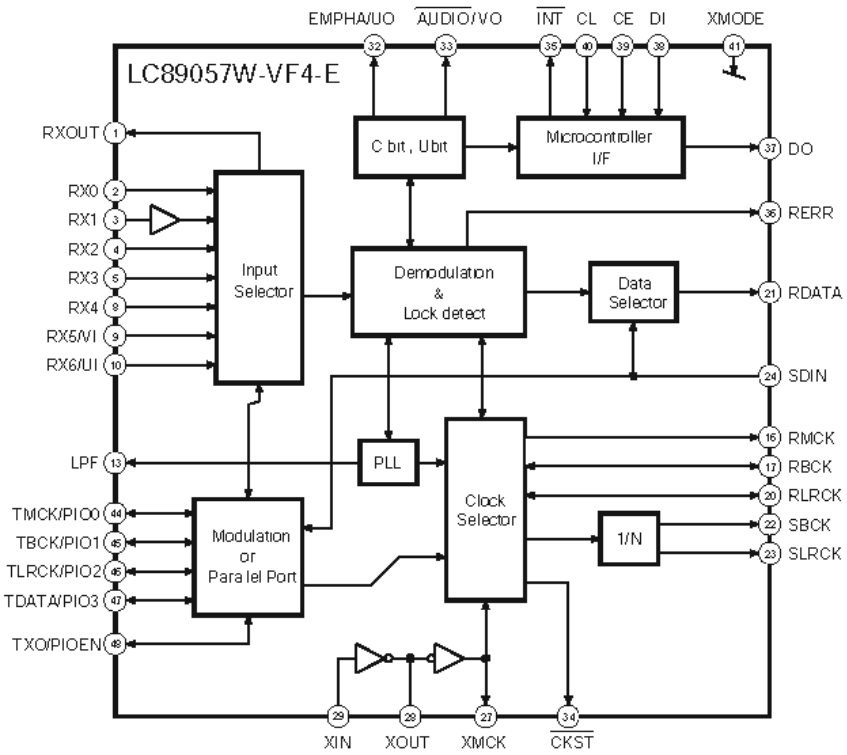


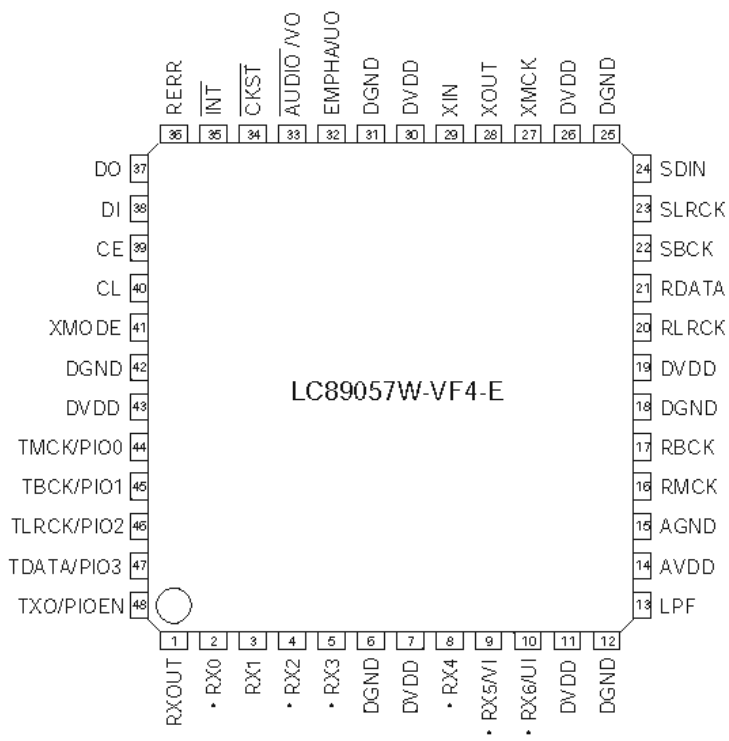
IC27 : CS5361-KS



Pin Name	#	Pin Description
RST	1	**Reset** (*Input*) - The device enters a low power mode when low.
M/S	2	**Master/Slave Mode** *(Input)* - Selects operation as either clock master or slave.
LRCK	3	**Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK	4	**Serial Clock** (*Input/Output*) - Serial clock for the serial audio interface.
MCLK	5	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VD	6	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
GND	7,18	**Ground** (*Input*) - Ground reference. Must be connected to analog ground.
VL	8	**Logic Power** (*Input*) **-** Positive power for the digital input/output.
SDOUT	9	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
MDIV	10	**MCLK Divider** *(Input)* **-** Enables a master clock divide by two function.
HPF	11	**High-pass Filter Enable** *(Input)* **-** Enables the Digital High-Pass Filter.
I²S/LJ	12	**Serial Audio Interface Format Select** (*Input*) -Selects either the left-justified or I²S format for the SAI.
M0 **M1**	13, 14	**Mode Selection** (*Input*) - Determines the operational mode of the device.
OVFL	15	**Overflow** *(Output, open drain)* **-** Detects an overflow condition on both left and right channels.
AINL+ **AINL-**	16, 17	**Differential Left Channel Analog Input** (*Input*) - Signals are presented differentially to the delta-sigma modulators via the AINL+/- pins.
VA	19	**Analog Power** (*Input*) **-** Positive power supply for the analog section.
AINR- **AINR+**	20, 21	**Differential Right Channel Analog Input** (*Input*) -Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
VQ	22	**Quiescent Voltage** *(Output)* **-** Filter connection for the internal quiescent reference voltage.
REF_GND	23	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
FILT+	24	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.

IC29 : LC89057W/VF4E

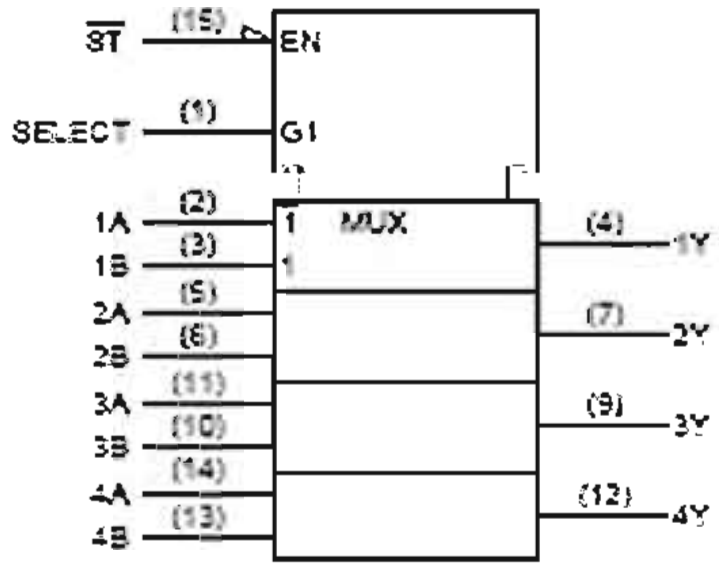




LC89057W

No.	Port name	I/O	Description
1	RXOUT	O	Data Output
2	RX0	I	Digital data Input (TTL)
3	RX1	I	Digital data Input (Coaxial)
4	RX2	I	Digital data Input (TTL)
5	RX3	I	Digital data Input (TTL)
6	DGND		Digital GND
7	DVDD		Digital VDD
8	RX4	I	Digital data Input (TTL)
9	RX5/VI	I	Digital data Input (TTL)
10	RX6/UI	I	Digital data Input (TTL)
11	DVDD		Digital GND for PLL
12	DGND		Digital VDD for PLL
13	LPF	O	Loop filter for PLL
14	AVDD		Analog VDD for PLL
15	AGND		Analog GND for PLL
16	RMCK	O	System clock Output for R (256fs, 512fs, XIN, VCO)
17	RBCK	O/I	Bit clock Output for R (64fs)
18	DGND		Digital GND
19	DVDD		Digital VDD
20	RLRCK	O/I	LR clock Input/Output for R
21	RDATA	O	Serial Audio data Input
22	SBCK	O	Bit clock Output for S (32fs, 64fs, 128fs)
23	SLRCK	O	LR clock Output for S (fs/2, fs, 2fs)
24	SDIN	I	Serial Audio data Input
25	DGND		Digital GND
26	DVDD		Digital VDD
27	XMCK	O	Oscillation amplifier
28	XOUT	O	XOUT
29	XIN	I	XIN or External clock Input (24.576MHz or 12.288MHz)
30	DVDD		Digital VDD
31	DGND		Digital GND
32	EMPHA/UO	I/O	Emphasis Information / U data Output / Set for chip address
33	AUDIO/VO	I/O	Detected non-PCM / V flag Output / Set for chip address
34	CKST	I/O	Clock timing Output / Switch to master or slave for demodulation
35	INT	I/O	Interrupt Output / Switch to Modulation or general-purpose I/O
36	RERR	O	Error Output (PLL lock, data error)
37	DO	O	IF, Read out data Output
38	DI	I	IF, Write data Input
39	CE	I	IF, Chip enable Input
40	CL	I	IF, Clock Input
41	XMODE	I	System reset Input
42	DGND		Digital GND
43	DVDD		Digital VDD
44	TMCK/PIO0	I/O	256fs system-clock Input for modulation / General-purpose I/O input/output
45	TBCK/PIO1	I/O	64fs bit-clock Input for modulation / General-purpose I/O input/output
46	TLRCK/PIO2	I/O	Fs clock Input for modulation / General-purpose I/O input/output
47	TDATA/PIO3	I/O	Serial audio data for modulation / General-purpose I/O input/output
48	TXO/PIOEN	O/I	Modulation data Output / General-purpose I/O enable input

IC32 : TC74VHC157FT



Inputs				Outputs
$\overline{ST}$	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X: Don't care

IC33 : TMS320DA708

1 Second Generation Aureus™ DSP

1.1 Features

DA708: 32-/64-Bit 250-MHz Floating-Point DSP

Upgrades to C67x+ CPU From DA6xx Family:
- 2X CPU Registers [64 General-Purpose]
- New Audio-Specific Instructions
- Compatible With the DA6xx C67x CPU

Enhanced Memory System
- 256K-Byte Unified Program/Data RAM
- 768K-Byte Unified Program/Data ROM
- Single-Cycle Data Access From CPU
- Large Program Cache (32K-Byte) Supports RAM, ROM, and External Memory

External Memory Interface (EMIF) Supports:
- 100-MHz SDRAM (16-Bit)
- Async Flash/SRAM (8- or 16-Bit)

Enhanced I/O System
- High-Performance Crossbar Switch
- Dedicated McASP DMA Bus
- Deterministic I/O Performance

dMAX Dual Data Movement Accelerator:
- Memory-to-Memory Transfers
- Memory-to-Peripheral Transfers
- Packing/Unpacking Delay Data
- Circular Addressing
- Non-Sequential Addressing for Reverb

Three Multichannel Audio Serial Ports
- Five Clock Zones and 16 Serial Data Pins
- Supports TDM, I2S, and Similar Formats
- DIT Only (McASP2)

Two SPI Ports With 3-, 4-, and 5-Pin Options

Two Inter-Integrated Circuit (I2C) Ports

Real-Time Interrupt Counter/Watchdog

Oscillator- and Software-Controlled PLL

Commercial or Extended Temperature

144-Pin, 0.5-mm, PowerPAD™ Thin Quad Flatpack (TQFP) [RFP Suffix]

Security Features Available

AUREUS DSP TEXAS INSTRUMENTS TECHNOLOGY

Applications
- A/V and DVD Receiver
- Multizone A/V Receiver
- HDD Jukebox
- Navigation Systems
- High-Speed Encode With Simultaneous Multichannel Decode

Software Support
- Dolby® Digital, Dolby® Digital EX, Dolby® Pro Logic® IIx, Dolby® Headphone, Dolby® Virtual Surround
- DTS® 5.1, DTS-ES™ 6.1, DTS Neo:6™, DTS 96/24™, DTS-ES 96/24™
- MPEG-2 AAC LC Decode
- THX® Select, THX® Ultra 2
- MP3 Encode, MP3 Decode
- WMA9 Encode, WMA9 Decode, WMA9 Pro Decode
- HDCD® Decode
- ATRAC3plus® Encode, ATRAC3plus® Decode
- Audyssey MultiEQ XT®, MultiEQ®, PreoEQ®
- SRS® Circle Surround™ II (CS II)
- Waves' MaxxBass® Technology
- TI Effects Library
- TI DSD-to-PCM Decode
- TI Filter Library
- TI Performance Audio Framework (PAF)
- TI DSP/BIOS™
- Chip Support Library and DSP Library

IC33 : TMS320DA708

Table 2-2. Terminal Functions

SIGNAL NAME	PIN NO.	TYPE(1)	PULL(2)	GPIO(3)	DESCRIPTION
External Memory Interface (EMIF) Address and Control					
EM_A[0]	91	O	-	N	EMIF Address Bus
EM_A[1]	89	O	-	N	
EM_A[2]	88	O	-	N	
EM_A[3]	86	O	-	N	
EM_A[4]	84	O	-	N	
EM_A[5]	83	O	-	N	
EM_A[6]	80	O	-	N	
EM_A[7]	79	O	-	N	
EM_A[8]	76	O	-	N	
EM_A[9]	75	O	-	N	
EM_A[10]	93	O	-	N	
EM_A[11]	74	O	-	N	
EM_BA[0]	96	O	-	N	SDRAM Bank Address and Asynchronous Memory Low-Order Address
EM_BA[1]	94	O	-	N	
$\overline{\text{EM\_CS[0]}}$	97	O	-	N	SDRAM Chip Select
$\overline{\text{EM\_CS[2]}}$	100	O	-	N	Asynchronous Memory Chip Select
$\overline{\text{EM\_CAS}}$	37	O	-	N	SDRAM Column Address Strobe
$\overline{\text{EM\_RAS}}$	98	O	-	N	SDRAM Row Address Strobe
$\overline{\text{EM\_WE}}$	38	O	-	N	SDRAM Write Enable
EM_CKE	71	O	-	N	SDRAM Clock Enable
EM_CLK	70	O	-	N	SDRAM Clock
EM_$\overline{\text{WE}}$_DQM[0]	39	O	-	N	Write Enable or Byte Enable for EM_D[7:0]
EM_$\overline{\text{WE}}$_DQM[1]	67	O	-	N	Write Enable or Byte Enable for EM_D[15:8]
$\overline{\text{EM\_OE}}$	104	O	-	N	SDRAM Output Enable
EM_R$\overline{\text{W}}$	102	O	-	N	Asynchronous Memory Read/not Write

(1) TYPE column refers to pin direction in functional mode. If a pin has more than one function with different directions, the functions are separated with a slash (/).
(2) PULL column:
IPD = Internal Pulldown resistor
IPU = Internal Pullup resistor
(3) If the GPIO column is 'Y', then in GPIO mode, the pin is configurable as an IO unless otherwise marked.

Table 2-2. Terminal Functions (continued)

SIGNAL NAME	PIN NO.	TYPE(1)	PULL(2)	GPIO(3)	DESCRIPTION
External Memory Interface (EMIF) Data Bus					
EM_D[0]	52	IO	-	N	EMIF Data Bus [Lower 16 Bits]
EM_D[1]	51	IO	-	N	
EM_D[2]	49	IO	-	N	
EM_D[3]	48	IO	-	N	
EM_D[4]	46	IO	-	N	
EM_D[5]	45	IO	-	N	
EM_D[6]	43	IO	-	N	
EM_D[7]	41	IO	-	N	
EM_D[8]	66	IO	-	N	
EM_D[9]	64	IO	-	N	
EM_D[10]	63	IO	-	N	
EM_D[11]	61	IO	-	N	
EM_D[12]	59	IO	-	N	
EM_D[13]	58	IO	-	N	
EM_D[14]	56	IO	-	N	
EM_D[15]	55	IO	-	N	

IC33 : TMS320DA708

Table 2-2. Terminal Functions (continued)

SIGNAL NAME	PIN NO.	TYPE[1]	PULL[2]	GPIO[3]	DESCRIPTION
McASP0, McASP1, McASP2, and SPI1 Serial Ports					
AHCLKR0/AHCLKR1	143	IO	-	Y	McASP0 and McASP1 Receive Master Clock
ACLKR0	139	IO	-	Y	McASP0 Receive Bit Clock
AFSR0	141	IO	-	Y	McASP0 Receive Frame Sync (L/R Clock)
AHCLKX0/AHCLKX2	2	IO	-	Y	McASP0 and McASP2 Transmit Master Clock
ACLKX0	142	IO	-	Y	McASP0 Transmit Bit Clock
AFSX0	144	IO	-	Y	McASP0 Transmit Frame Sync (L/R Clock)
AMUTE0	3	O	-	Y	McASP0 MUTE Output
AXR0[0]	113	IO	-	Y	McASP0 Serial Data 0
AXR0[1]	115	IO	-	Y	McASP0 Serial Data 1
AXR0[2]	116	IO	-	Y	McASP0 Serial Data 2
AXR0[3]	117	IO	-	Y	McASP0 Serial Data 3
AXR0[4]	119	IO	-	Y	McASP0 Serial Data 4
AXR0[5]/SPI1_$\overline{SCS}$	120	IO	-	Y	McASP0 Serial Data 5 ***or*** SPI1 Slave Chip Select
AXR0[6]/SPI1_$\overline{ENA}$	121	IO	-	Y	McASP0 Serial Data 6 ***or*** SPI1 Enable (Ready)
AXR0[7]/SPI1_CLK	122	IO	-	Y	McASP0 Serial Data 7 ***or*** SPI1 Serial Clock
AXR0[8]/AXR1[5]/ SPI1_SOMI	126	IO	-	Y	McASP0 Serial Data 8 ***or*** McASP1 Serial Data 5 ***or*** SPI1 Data Pin Slave Out Master In
AXR0[9]/AXR1[4]/ SPI1_SIMO	127	IO	-	Y	McASP0 Serial Data 9 ***or*** McASP1 Serial Data 4 ***or*** SPI1 Data Pin Slave In Master Out
AXR0[10]/AXR1[3]	130	IO	-	Y	McASP0 Serial Data 10 ***or*** McASP1 Serial Data 3
AXR0[11]/AXR1[2]	131	IO	-	Y	McASP0 Serial Data 11 ***or*** McASP1 Serial Data 2
AXR0[12]/AXR1[1]	134	IO	-	Y	McASP0 Serial Data 12 ***or*** McASP1 Serial Data 1
AXR0[13]/AXR1[0]	135	IO	-	Y	McASP0 Serial Data 13 ***or*** McASP1 Serial Data 0
AXR0[14]/AXR2[1]	137	IO	-	Y	McASP0 Serial Data 14 ***or*** McASP2 Serial Data 1
AXR0[15]/AXR2[0]	138	IO	-	Y	McASP0 Serial Data 15 ***or*** McASP2 Serial Data 0
ACLKR1	9	IO	-	Y	McASP1 Receive Bit Clock
AFSR1	12	IO	-	Y	McASP1 Receive Frame Sync (L/R Clock)
AHCLKX1	5	IO	-	Y	McASP1 Transmit Master Clock
ACLKX1	7	IO	-	Y	McASP1 Transmit Bit Clock
AFSX1	11	IO	-	Y	McASP1 Transmit Frame Sync (L/R Clock)
AMUTE1	4	O	-	Y	McASP1 MUTE Output
SPI0, I2C0, and I2C1 Serial Port Pins					
SPI0_SOMI/I2C0_SDA	111	IO	-	Y	SPI0 Data Pin Slave Out Master In ***or*** I2C0 Serial Data
SPI0_SIMO	110	IO	-	Y	SPI0 Data Pin Slave In Master Out
SPI0_CLK/I2C0_SCL	108	IO	-	Y	SPI0 Serial Clock ***or*** I2C0 Serial Clock
SPI0_$\overline{SCS}$/I2C1_SCL	107	IO	-	Y	SPI0 Slave Chip Select ***or*** I2C1 Serial Clock
SPI0_$\overline{ENA}$/I2C1_SDA	105	IO	-	Y	SPI0 Enable (Ready) ***or*** I2C1 Serial Data

IC33 : TMS320DA708

Table 2-2. Terminal Functions (continued)

SIGNAL NAME	PIN NO.	TYPE (1)	PULL (2)	GPIO (3)	DESCRIPTION
Clocks					
OSCIN	23	I	-	N	1.2-V Oscillator Input
OSCOUT	24	O	-	N	1.2-V Oscillator Output
$OSCV_{DD}$	25	PWR	-	N	Oscillator 1.2-V V_{DD} tap point (for filter only)
$OSCV_{SS}$	22	PWR	-	N	Oscillator V_{SS} tap point (for filter only)
CLKIN	17	I	-	N	Alternate clock input (3.3-V LVCMOS Input)
PLLHV	27	PWR	-	N	PLL 3.3-V Supply Input (requires external filter)
Device Reset					
$\overline{RESET}$	14	I	-	N	Device reset pin
Emulation/JTAG Port					
TCK	35	I	IPU	N	Test Clock
TMS	19	I	IPU	N	Test Mode Select
TDI	28	I	IPU	N	Test Data In
TDO	29	OZ	IPU	N	Test Data Out
$\overline{TRST}$	21	I	IPD	N	Test Reset
$\overline{EMU[0]}$	32	IO	IPU	N	Emulation Pin 0
$\overline{EMU[1]}$	34	IO	IPU	N	Emulation Pin 1
Power Pins					
Core Supply (CV_{DD})	8, 16, 20, 33, 44, 53, 57, 65, 77, 85, 90, 101, 123, 128, 132				
IO Supply (DV_{DD})	10, 31, 42, 50, 60, 68, 73, 81, 92, 103, 112, 125, 136				
Ground (V_{SS})	1, 6, 13, 15, 18, 26, 30, 36, 40, 47, 54, 62, 69, 72, 78, 82, 87, 95, 99, 106, 109, 114, 118, 124, 129, 133, 140				

2.15 Device Block Diagram

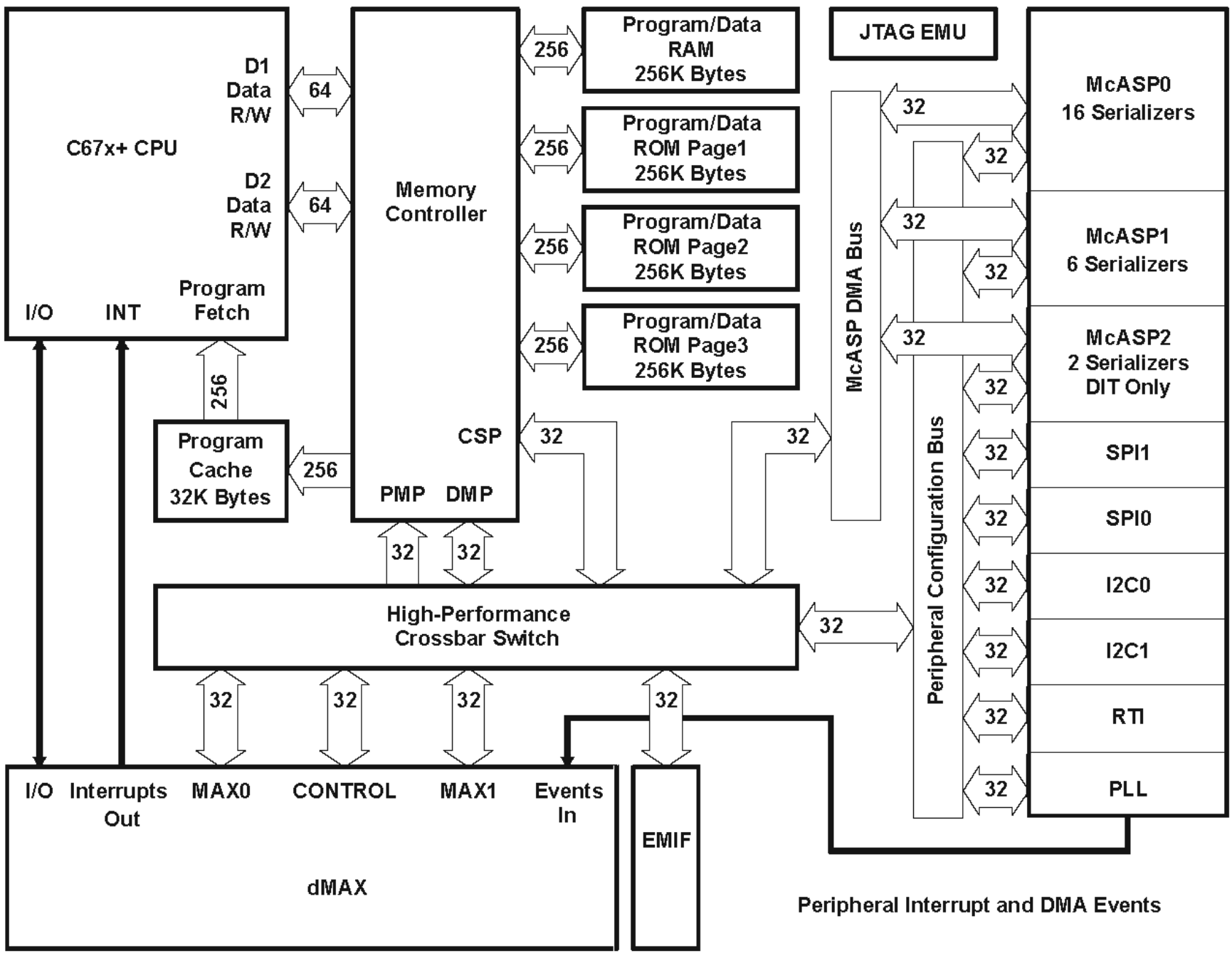
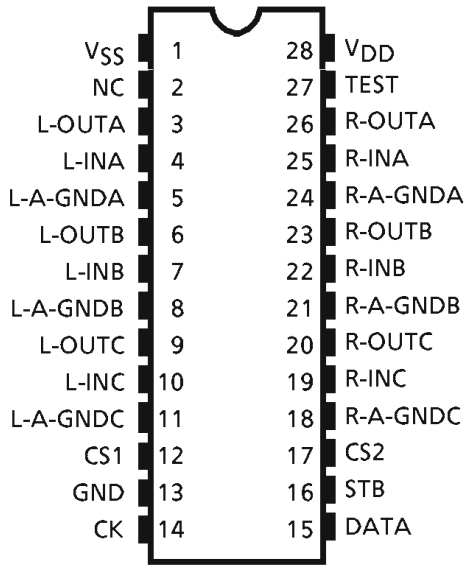


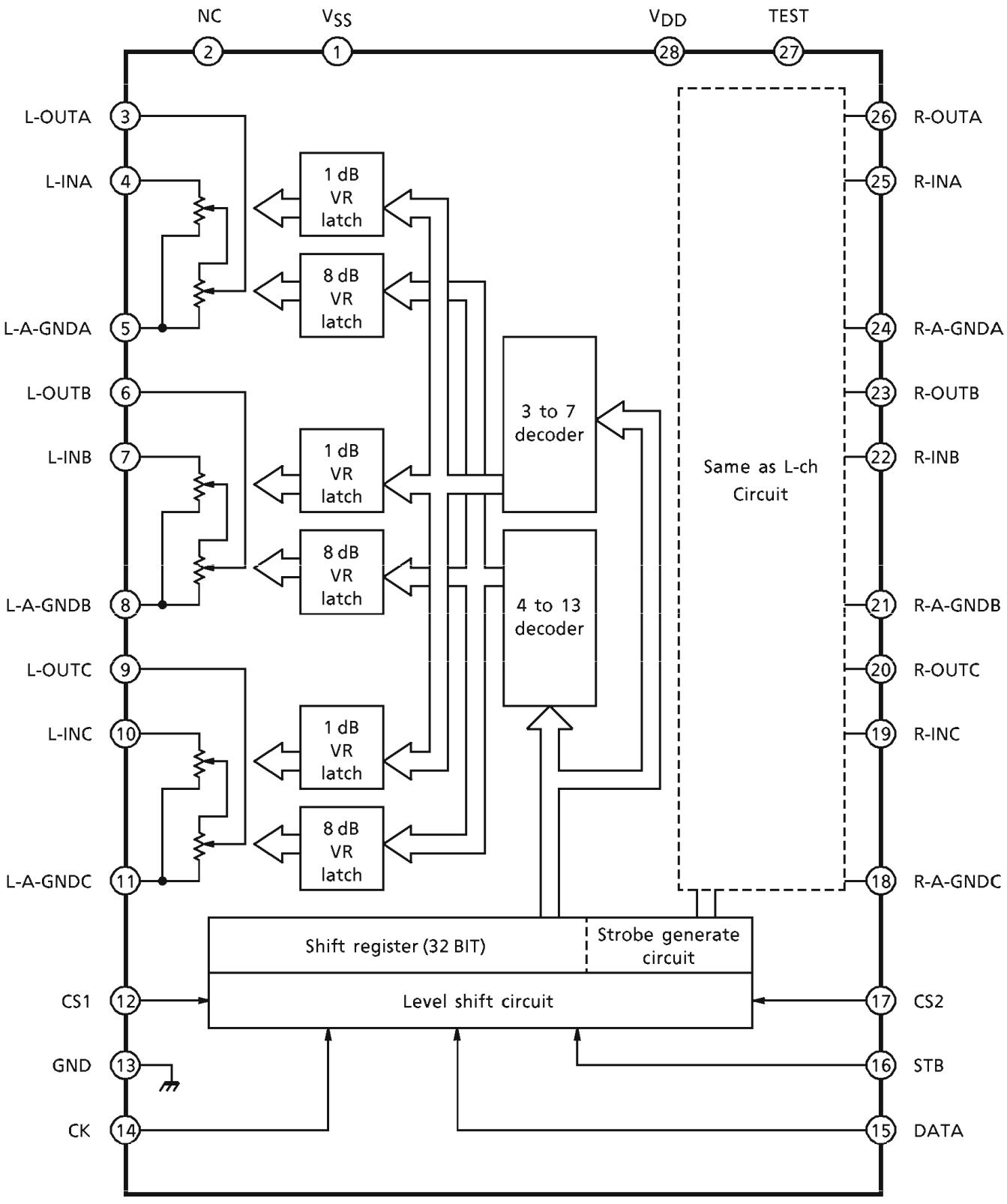
Figure 2-3. DA708 DSP Block Diagram

IC33 : TC9482BFG
IC34 : TC9482BFG

PIN CONNECTIONS

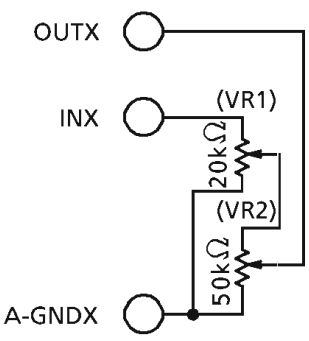


BLOCK DIAGRAM



IC33 : TC9482BFG
IC33 : TC9482BFG

PIN DESCRIPTION

PIN No.	SYMBOL	PIN NAME	FUNCTION	REMARK
1	V_{SS}	Negative power supply pin	● Power Supply Pins	—
28	V_{DD}	Positive power supply pin		
3	L-OUTA	Volume output pin	● Volume circuit 	—
26	R-OUTA			
6	L-OUTB			
22	R-OUTB			
9	L-OUTC			
19	R-OUTC			
4	L-INA	Volume input pin		
25	R-INA			
7	L-INB			
22	R-INB			
10	L-INC			
19	R-INC			
5	L-A-GNDA	Analog GND pin		
24	R-A-GNDA			
8	L-A-GNDB			
21	R-A-GNDB			
11	L-A-GNDC			
18	R-A-GNDC			
12	CS1	Chip select input pin	Up to 4 chips on the same bus can be used by switching over chip select code.	—
17	CS2			
14	CK	Clock input pin	Inputs clock for serial data transfer.	Low threshold value input pin
15	DATA	Data input pin	Inputs control data for setting volume.	
16	STB	Strobe input pin	Inputs strobe for writing data.	
13	GND	Digital GND pin	Digital ground pin	—
27	TEST	Test Pin	Normally connect to V_{DD} pin.	—
2	NC	No connection	—	—

IC34 : M29W800DT70N

Figure 2. Logic Diagram

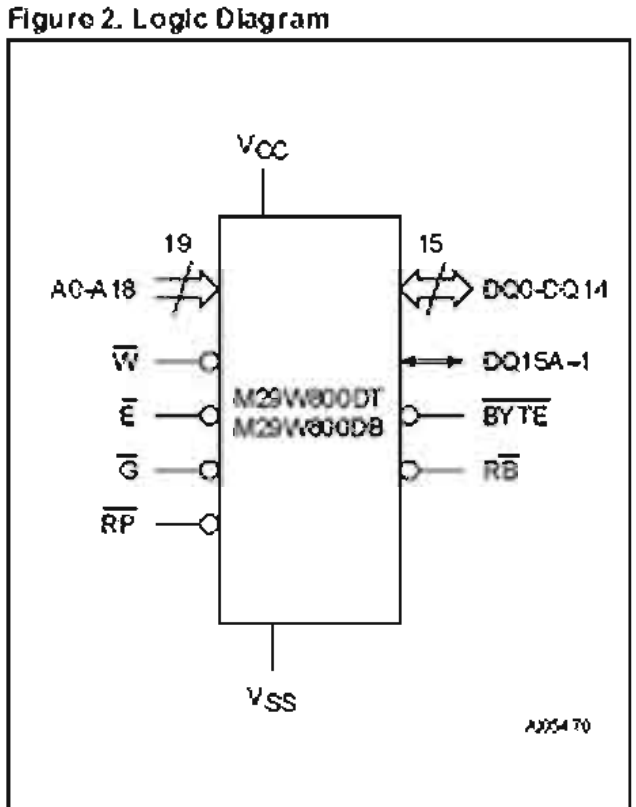
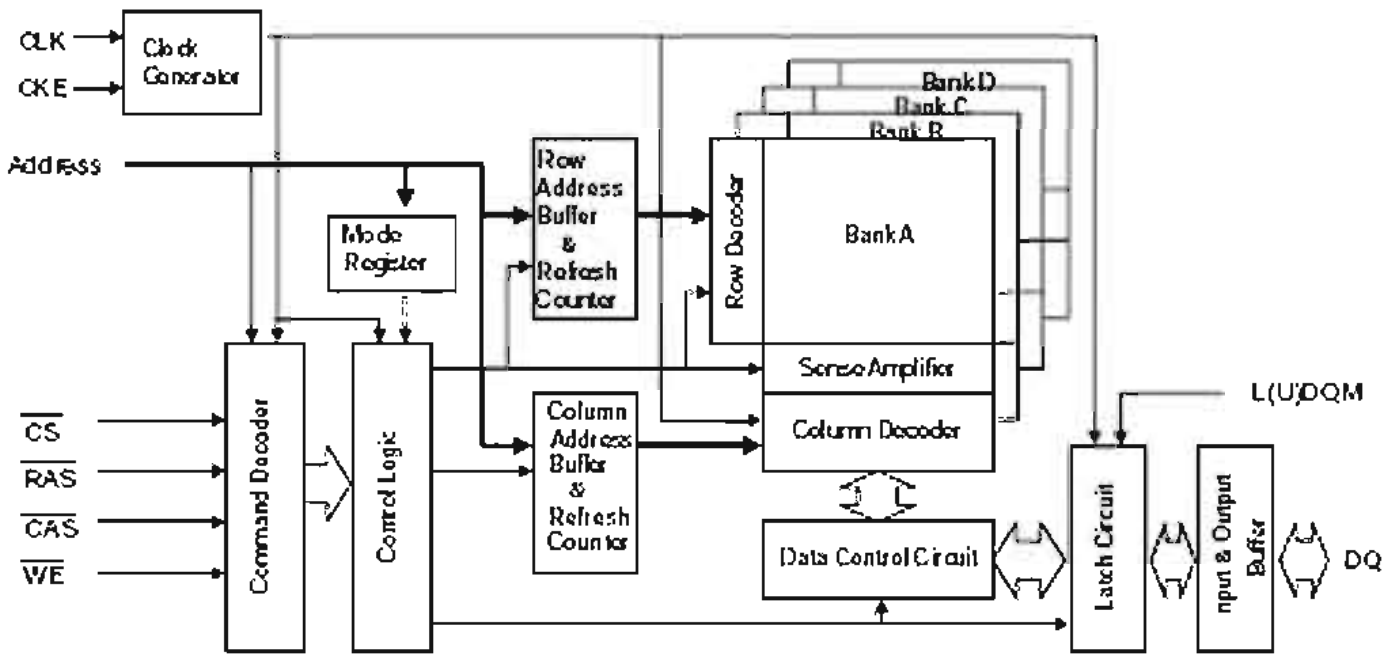


Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A-1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$\overline{RB}$	Ready/Busy Output (not available on SO44 package)
$\overline{BYTE}$	Byte/Word Organization Select
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

IC35 : M12L64164A7T

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK , CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row / column address are multiplexed on the same pins. Row address : RA0~RA11, column address : CA0~CA7
A12 , A13	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column address on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	Data Input / Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ DQ15	Data Input / Output	Data inputs / outputs are multiplexed on the same pins.
VDD / VSS	Power Supply / Ground	Power and ground for the input buffers and the core logic.
VDDQ / VSSQ	Data Output Power / Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left No Connection on the device.

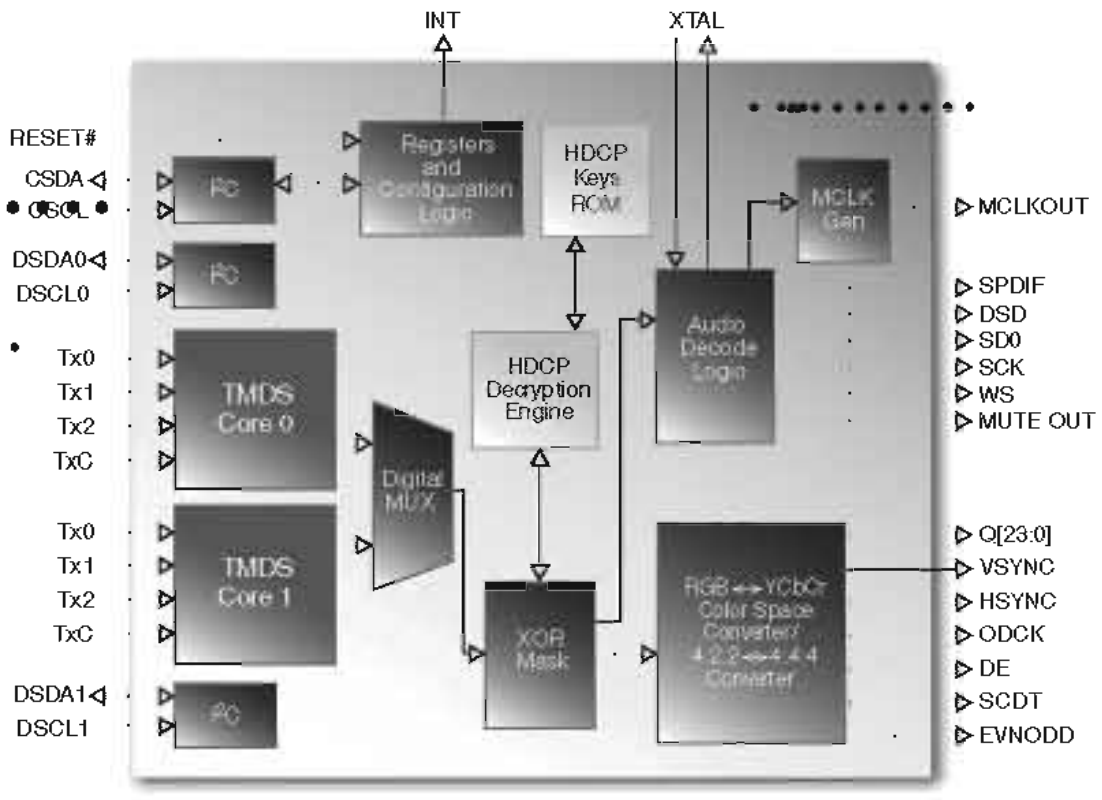
IC35 : Sil 9033CTU

HDMI Receiver

- HDMI 1.2
- DVI 1.0
- EIA/CEA-861C
- HDCP 1.1

- Dual integrated cores
- Supports DTV (480i/576i/480p/ 576p/720p/1080i/1080p) and PC (VGA/XGA/SXGA/WSXGA.UXGA) resolutions
- Flexible digital video interface
  - 24-bit RGB/YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YCbCr 4:2:2 (ITU-R BT.656)
  - 12-bit digital media interface
- Integrated RGB ↔ YCbCr color space conversion
- 4:2:2 ↔ 4:4:4 converter

- Industry-standard S/PDIF and I²S output
- Supports high-end audio including SACD and DVD-Audio
  - 2-ch. 32-192kHz or
  - 8-ch. 32-192kHz
- Programmable I²S output supports numerous low-cost audio DACs
- Supports IEC60958 2-channel PCM
- Capable of carrying IEC61937 compressed audio (Dolby Digital, DTS,etc.)



- Integrated HDCP cipher engine
- Built-in HDCP BIST
- Pre-programmed HDCP keys
  - Simplify manufacturing process
  - Most secure solution available
  - Lower system, manufacturing costs
- New built-in HDCP self-test
- Supports HDCP repeater capability
- Decrypts both video and audio

- Register-programmable via slave I²C interface
- Auto video mode simplifies design
- Auto audio mode allows more robust system
- Flexible interrupt registers with interrupt pin

- 1.8V core provides low-power operation
- Flexible power-down modes

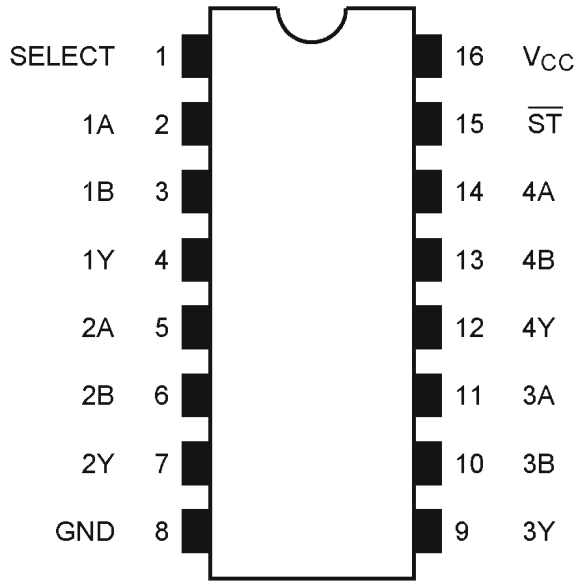
- Sil 9033 Receiver Daughter Board
- HDMI to HDMI cable

- HDMIGear Receiver Software Tool

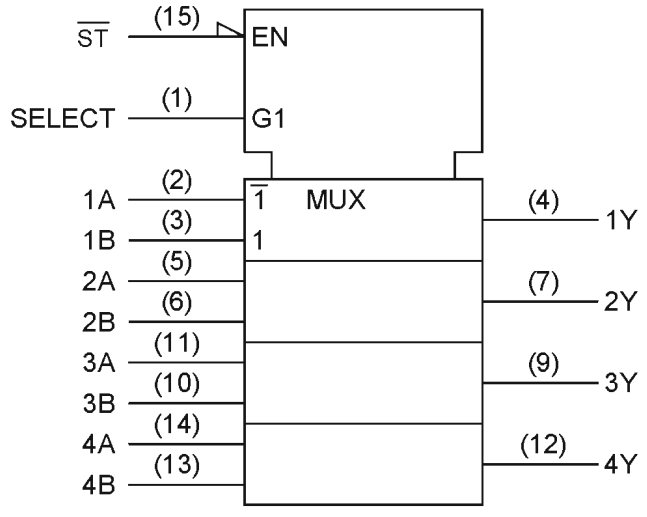
- User's Guide
- Schematics
- Bill of Materials (BOM)

IC36 : TC74VCX157FT
IC38 : TC74VCX157FT

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs				Outputs
$\overline{ST}$	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X: Don't care

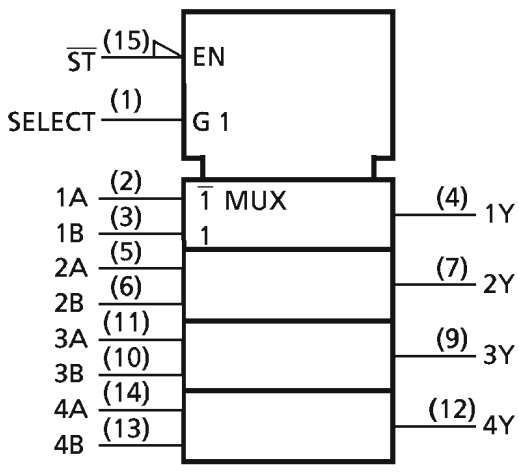
IC38 : TC74VHC157FT

TRUTH TABLE

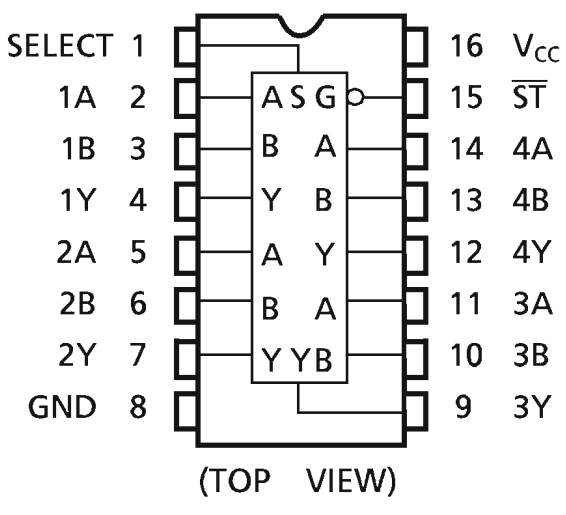
INPUTS				OUTPUT
$\overline{ST}$	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X : Don't Care

IEC LOGIC SYMBOL



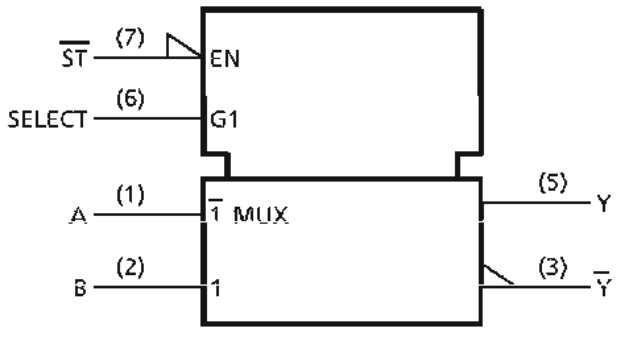
PIN ASSIGNMENT



(TOP VIEW)

IC39 : TC7WH157FU

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{ST}$	SELECT	A	B	Y	$\overline{Y}$
H	×	×	×	L	H
L	L	L	×	L	H
L	L	H	×	H	L
L	H	×	L	L	H
L	H	×	H	H	L

× : Don't care

IC41 : SiL 9030CTU-7

SiI 9030 Features

PanelLink Cinema Transmitter

Industry-Standard Compliance

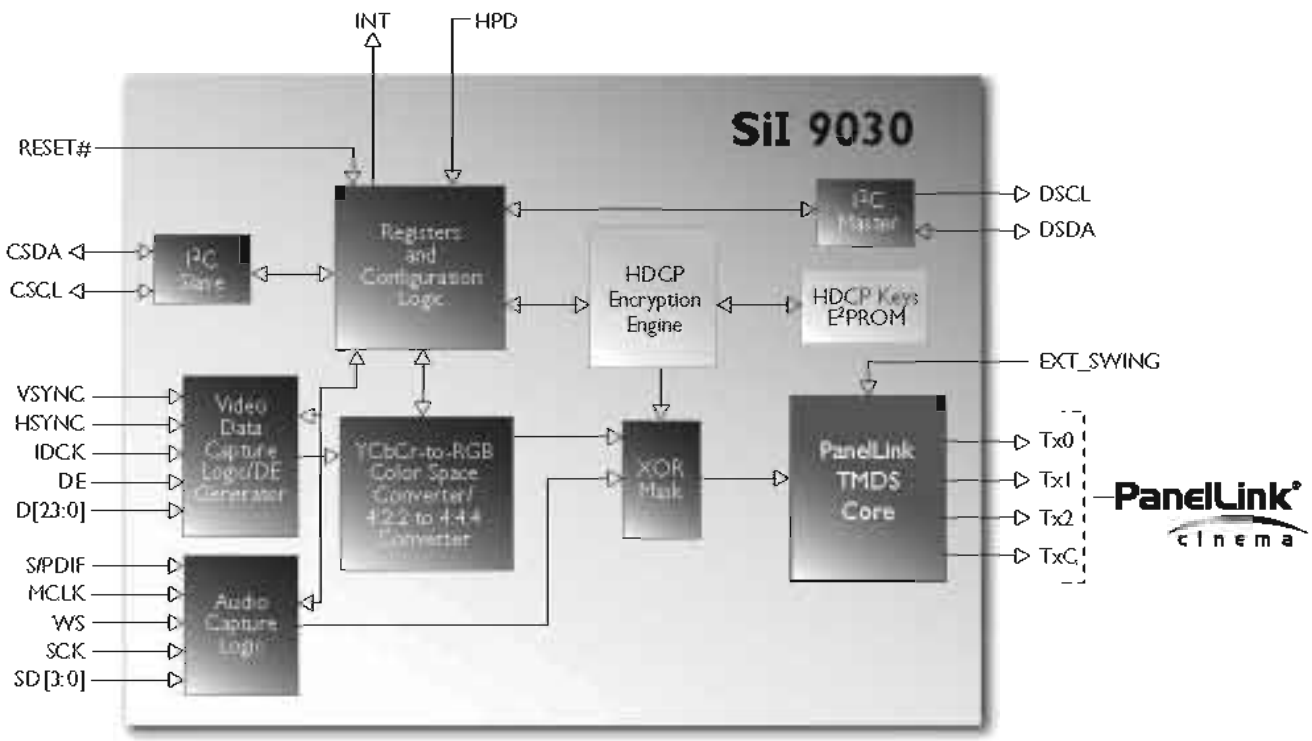
- HDMI 1.0
- DVI 1.0
- EIA/CEA-861B
- HDCP 1.1

Digital Video Output

- Integrated PanelLink® core
- Supports DTV (480i/576i/480p/576p/720p/1080i/1080p) and PC (VGA/XGA/SXGA/WSXGA) resolutions
- Flexible video interface supports DVD and HD MPEG decoders
  - 12/24-bit RGB YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YCbCr 4:2:2 (ITU-R BT.601 & BT.656)
- Integrated YCbCr ↔ RGB color space conversion
- 4:2:2↔ 4:4:4 up-converter
- Programmable Data Enable (DE) generator

Digital Audio Output

- DVD-Audio support thru 4xI²S inputs
- Supports 2-channel 192kHz or 8-channel 96kHz
- Supports IEC60958 2-channel PCM or IEC61937 compressed audio (Dolby Digital, DTS, etc.)
- Industry-standard S/PDIF input



Content Protection

- Integrated HDCP cipher engine
- Pre-programmed HDCP keys
  - Simplify manufacturing process
  - Most secure solution available
  - Lower system, manufacturing costs
- Encrypts both video and audio

System Operation

- Register-programmable via slave I²C interface
- Master I²C simplifies system design
- Flexible interrupt registers with interrupt pin
- Monitor detection supported through hot plug and receiver detection

Power Management

- 1.8V core provides low-power operation
- Flexible power-down modes

Silicon Image's SiI 9030 Starter Kit (CP9030HDMI)

Contents include:

Hardware

- SiI 9030 Transmitter Stand Alone Board
- HDMI to HDMI cable

Software

- HDMIGear Software Tool

Documentation

- User's Guide
- Schematics
- Bill of Materials (BOM)

IC41 : CS4382A-CQ

114 dB, 192 kHz 8-Channel D/A Converter

Features

- 24-bit Conversion
- Up to 192 kHz Sample Rates
- 114 dB Dynamic Range
- -100 dB THD+N
- Supports PCM and DSD Data Formats
- Selectable Digital Filters
- Volume Control with Soft Ramp
  - 1 dB Step Size
  - Zero Crossing Click-free Transitions
- Dedicated DSD inputs
- Low Clock Jitter Sensitivity
- Simultaneous Support for Two Synchronous Sample Rates for DVD Audio
- C or Stand-alone Operation

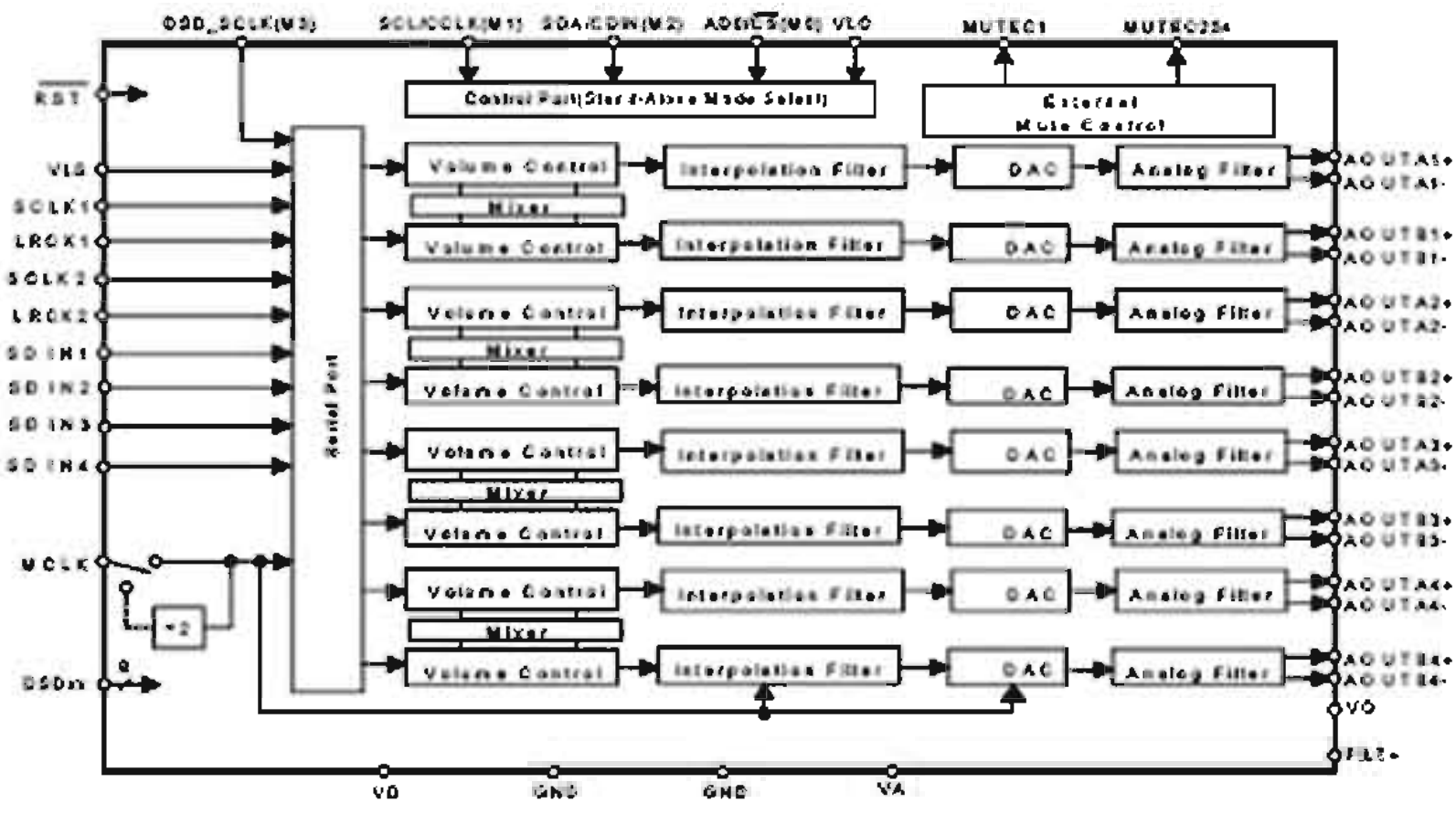
Description

The CS4382 is a complete 8-channel digital-to-analog system including digital interpolation, fifth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

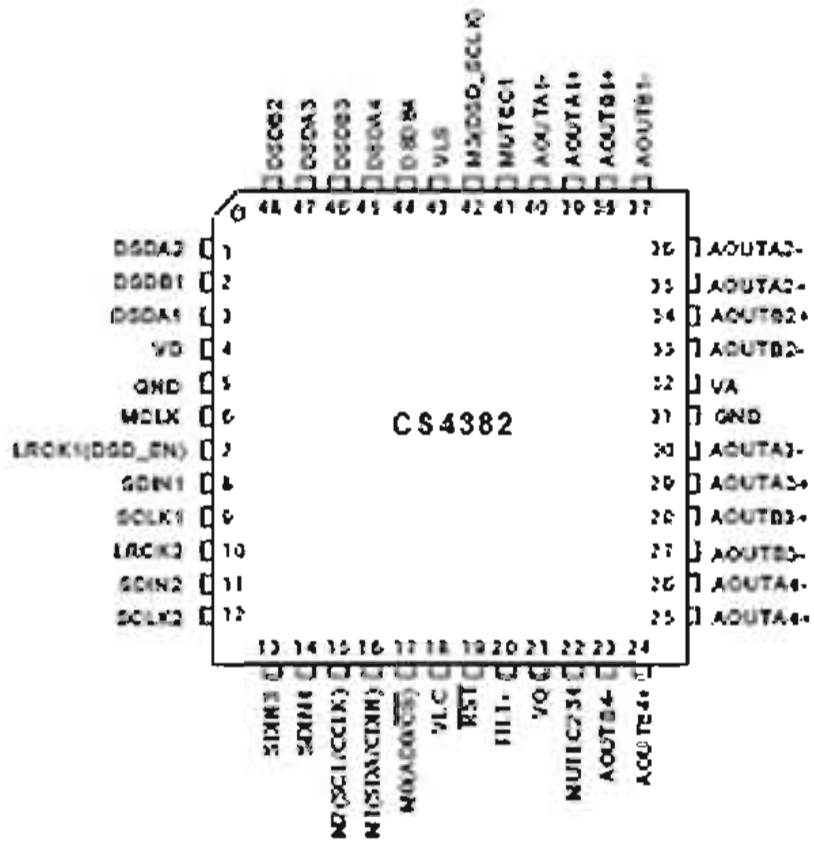
The CS4382 accepts PCM data at sample rates from 4 kHz to 192 kHz, DSD audio data, and operates over a wide power supply range. These features are ideal for multi-channel audio systems including DVD players, SACD players, A/V receivers, digital TV's, mixing consoles, effects processors, and automotive audio systems.

ORDERING INFORMATION

CS4382-KQZ, Lead Free	-10 to 70 °C	48-pin LQFP
CDB4382		Evaluation Board



IC41 : CS4382A-CQ

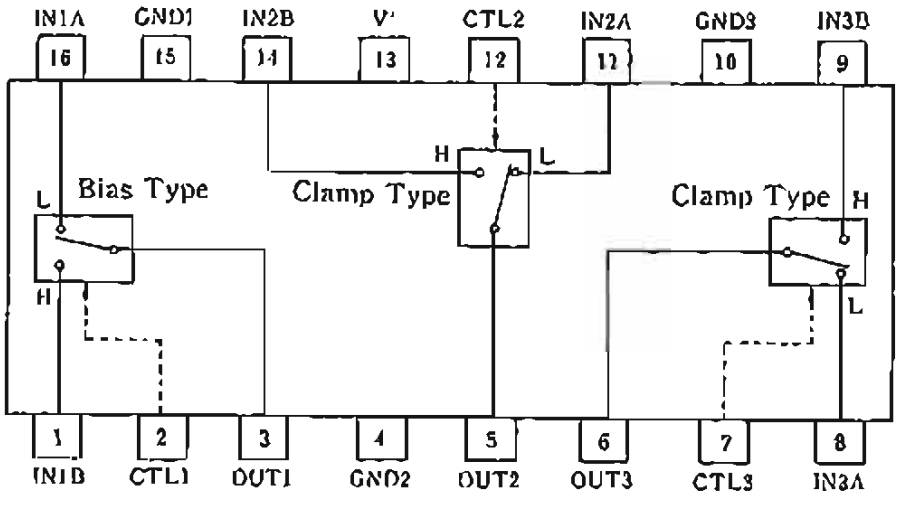


Pin Name	#	Pin Description
VD	4	**Digital Power** (*Input*) - Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	5 31	**Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MCLK	6	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters. Table 5 illustrates several standard audio sample rates and the required master clock frequency.
LRCK1 LRCK2	7 10	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SDIN1 SDIN2 SDIN3 SDIN4	8 11 13 14	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK1 SCLK2	9 12	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
VLC	18	**Control Port Power** (*Input*) - Determines the required signal level for the control port. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{\text{RST}}$	19	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
FILT+	20	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to analog ground, as shown in the Typical Connection Diagram.
VQ	21	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage. VQ must be capacitively coupled to analog ground, as shown in the Typical Connection Diagram. The nominal voltage level is specified in the Analog Characteristics and Specifications section. VQ presents an appreciable source impedance and any current drawn from this pin will alter device performance. However, VQ can be used to bias the analog circuitry assuming there is no AC signal component and the DC current is less than the maximum specified in the Analog Characteristics and Specifications section.

IC41 : CS4382A-CQ

Pin Name	#	Pin Description
MUTEC1 **MUTEC234**	41 22	**Mute Control** (*Output*) - The Mute Control pins go high during power-up initialization, reset, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect These pins are intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops
AOUTA1 +,- **AOUTB1 +,-** **AOUTA2 +,-** **AOUTB2 +,-** **AOUTA3 +,-** **AOUTB3 +,-** **AOUTA4 +,-** **AOUTB4 +,-**	39, 40 38, 37 35, 36 34, 33 29, 30 28, 27 25, 26 24, 23	**Differential Analog Output** (*Output*) - The full scale differential analog output level is specified in the Analog Characteristics specification table
VA	32	**Analog Power** (*Input*) **-** Positive power supply for the analog section Refer to the Recommended Operating Conditions for appropriate voltages
VLS	43	**Serial Audio Interface Power** (*Input*) **-** Determines the required signal level for the serial audio interface Refer to the Recommended Operating Conditions for appropriate voltages
Control Port Definitions		
SCL/CCLK	15	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port Requires an external pull-up resistor to the logic interface voltage in I^2C mode as shown in the Typical Connection Diagram
SDA/CDIN	16	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line in I^2C mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram CDIN is the input data line for the control port interface in SPI mode
AD0/$\overline{CS}$	17	**Address Bit 0 (I^2C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I^2C mode, $\overline{CS}$ is the chip select signal for SPI format
Stand-Alone Definitions		
M0 **M1** **M2** **M3**	17 16 15 42	**Mode Selection** (*Input*) - Determines the operational mode of the device as detailed in Tables 6 and 7
DSD Definitions		
DSD_SCLK	42	**DSD Serial Clock** (*Input*) - Serial clock for the Direct Stream Digital audio interface
DSD_EN	7	**DSD-Enable** *(Input)* - When held at logic '1' the device will enter DSD mode (Stand-Alone mode only)
DSDA1 **DSDB1** **DSDA2** **DSDB2** **DSDA3** **DSDB3** **DSDA4** **DSDB4**	3 2 1 48 47 46 45 44	**Direct Stream Digital Input** (*Input*) - Input for Direct Stream Digital serial audio data

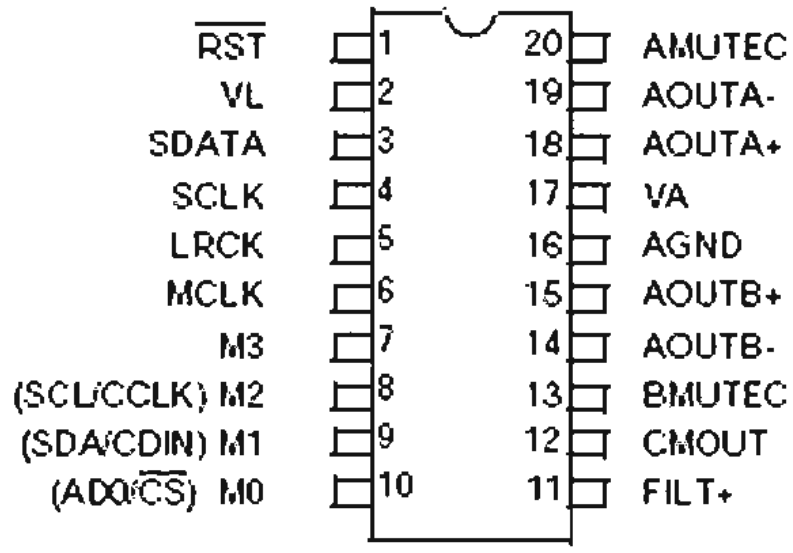
IC61 : NJM2285MTE1



NJM2285D
NJM2285M

IC61 : CS4392KZZ

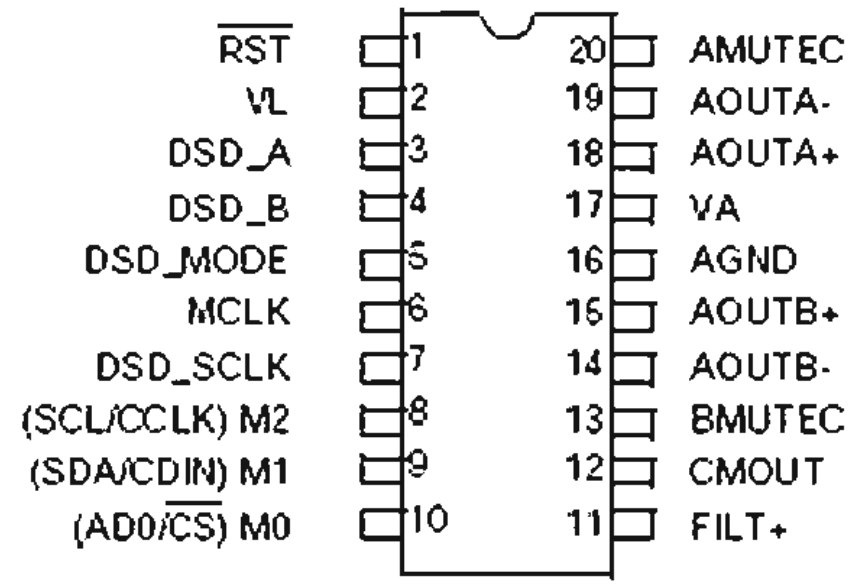
1. PIN DESCRIPTION - PCM DATA MODE



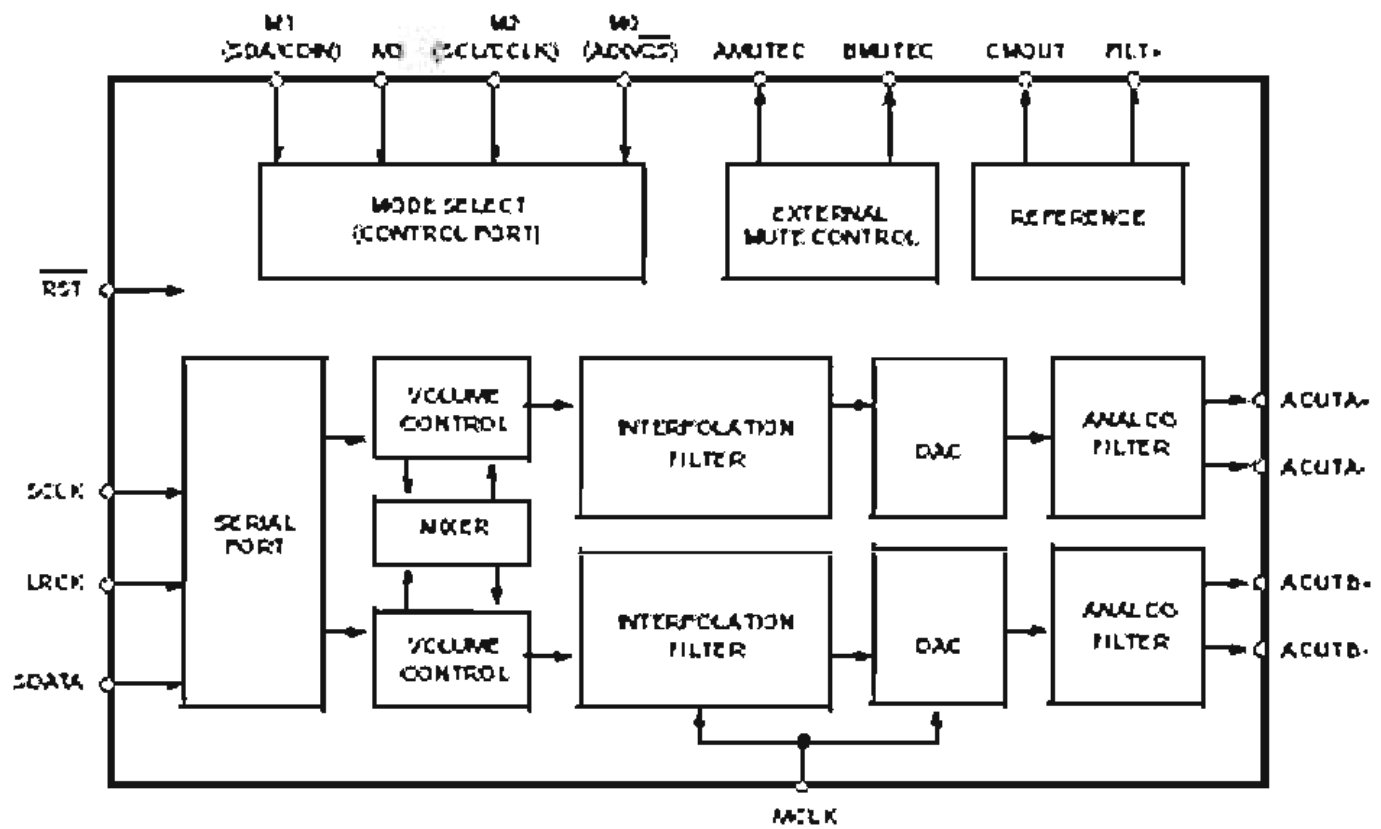
RST	1	Reset (Input) - Powers down device and resets all internal registers to their default settings.
VL	2	Logic Power (Input) - Positive power for the digital input/output.
SDATA	3	Serial Audio Data (Input) - Input for two's complement serial audio data.
SCLK	4	Serial Clock (Input/Output) - Serial clock for the serial audio interface.
LRCK	5	Left Right Clock (Input/Output) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	6	Master Clock (Input) - Clock source for the delta-sigma modulator and digital filters.
FILT+	11	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits.
CMOUT	12	Common Mode Voltage (Output) - Filter connection for internal quiescent voltage.
AMUTEC BMUTEC	20 13	Mute Control (Output) - The Mute Control pin goes high during power-up initialization, reset, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect.
AOUTB- AOUTB+ AOUTA+ AOUTA-	14 15 18 19	Differential Analog Output (Outputs) - The full scale differential analog output level is specified in the Analog Characteristics specification table.
AGND	16	Ground (Input)
VA	17	Analog Power (Input) - Positive power for the analog section.
Control Port Mode Definitions		
M3	7	Mode Selection (Input) - This pins should be tied to GND level during control port mode.
SCL/CCLK	8	Serial Control Port Clock (Input) - Serial clock for the serial control port.
SDA/CDIN	9	Serial Control Data (Input/Output) - SDA is a data I/O line in I^2C mode. CDIN is the input data line for the control port interface in SPI mode.
AD0/$\overline{CS}$	10	Address Bit 0 (I^2C) / Control Port Chip Select (SPI) (Input/Output) - AD0 is a chip address pin in I^2C mode. $\overline{CS}$ is the chip select signal for SPI format.
Stand-Alone Mode Definitions		
M3 M2 M1 M0	7 8 9 10	Mode Selection (Input) - Determines the operational mode of the device.

IC61 : CS4392KZZ

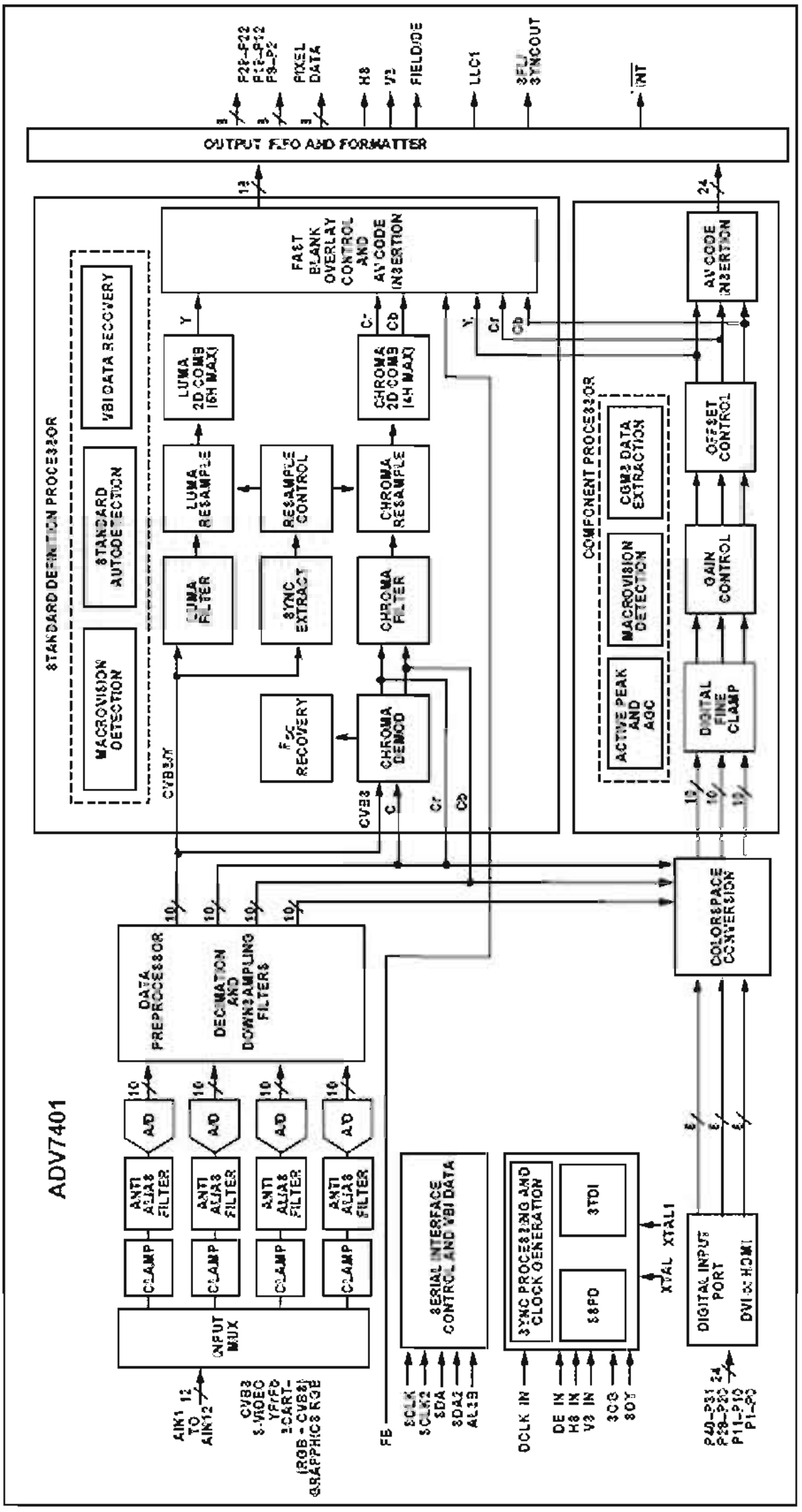
1.1 PIN DESCRIPTION - DSD mode



DSD_A	3	DSD Data (Input) - Input for Direct Stream Digital serial audio data.
DSD_B	4	
DSD_Mode	5	DSD Mode (Input) - In stand alone mode, this pin must be set to a logic 1 for operation of DSD Mode.
DSD_SCLK	7	DSD Serial Clock (Input/Output) - Serial clock for the Direct Stream Digital audio interface.



IC62 : ADV7401BS80



IC62 : ADV7401BS80

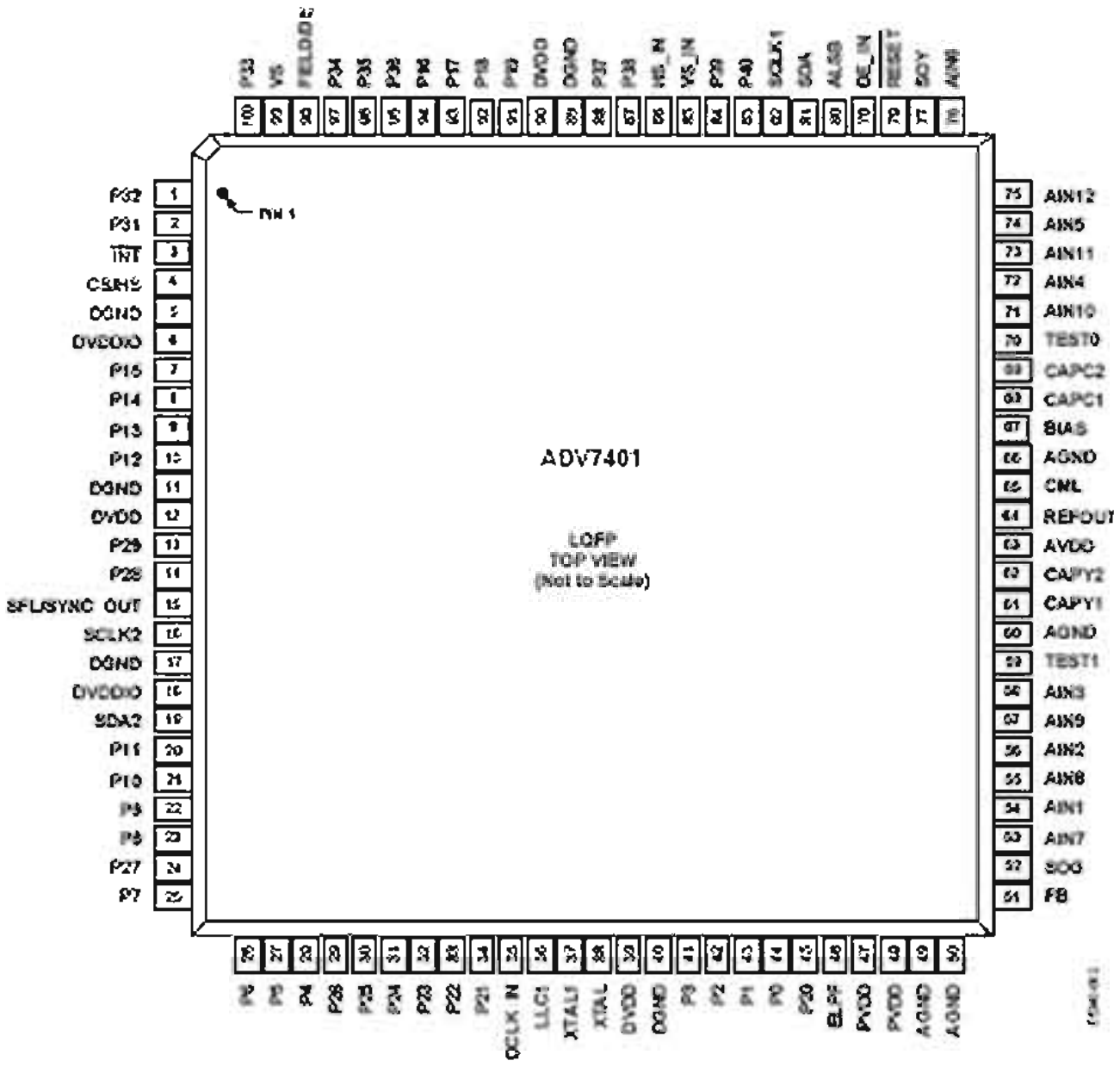


Figure 2.ADV7401 Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Function
5, 11, 17, 40, 89	DGND	G	Digital Ground.
49, 50, 60, 66	AGND	G	Analog Ground.
6, 18	DVDDIO	P	Digital I/O Supply Voltage (3.3 V).
12, 39, 90	DVDD	P	Digital Core Supply Voltage (1.8 V).
63	AVDD	P	Analog Supply Voltage (3.3 V).
47, 48	PVDD	P	PLL Supply Voltage (1.8 V).
51	FB	I	Fast Switch Overlay Input. This pin switches between CVBS and RGB analog signals.
54, 56, 58, 72, 74, 76, 53, 55, 57, 71, 73, 75	AIN1 to AIN12	I	Analog Video Input Channels.
42, 41, 28, 27, 26, 25, 23, 22, 10, 9, 8, 7, 94, 93, 92, 91	P2 to P9, P12 to P19	O	Video Pixel Output Port.
33, 32, 31, 30, 29, 24, 14, 13	P22 to P29	I/O	Video Input/Output Port
44, 43, 21, 20, 45, 34, 2, 1, 100, 97, 96, 95, 88, 87, 84, 83	P0 to P1, P10 to P11, P20 to P21, P31 to P40	I	Video Pixel Input Port.
3	$\overline{INT}$	O	Interrupt. This pin can be active low or active high. When SDP/CP status bits change this pin triggers. The set of events which triggers an interrupt are under user control.

IC62 : ADV7401BS80

Pin No.	Mnemonic	Type	Function
4	HS/CS	O	HS is a Horizontal Synchronization Output Signal (SDP and CP modes). CS is a Digital Composite Synchronization Signal (and can be selected while in CP mode).
99	VS	O	Vertical Synchronization Output Signal (SDP and CP modes).
98	FIELD/DE	O	Field Synchronization Output Signal (all interlaced video modes). This pin also can be enabled as a Data Enable signal (DE) in CP mode to allow direct connection to a HDMI/DVI Tx IC.
81, 19	SDA1, SDA2	I/O	I²C Port Serial Data Input/Output Pins. SDA1 is the data line for the Control port and SDA2 is the data line for the VBI readback port.
82, 16	SCLK1, SCLK2	I	I²C port serial clock input (max clock rate of 400 kHz). SCLK1 is the clock line for the Control port and SCLK2 is the clock line for the VBI data readback port.
80	ALSB	I	This pin selects the I²C address for the ADV7401 Control and VBI readback ports. ALSB set to a logic 0 sets the address for a write to control port of 0x40 and the readback address for the VBI port of 0x21. ALSB set to a logic high sets the address for a write to control port of 0x42 and the readback address for the VBI port of 0x23.
78	RESET	I	System reset input, active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7401 circuitry.
36	LLC1	O	LLC1 is a line locked output clock for the pixel data (range is 12.825 MHz to 140 MHz for ADV7401KSTZ-140; 12.825 MHz to 110 MHz for ADV7401BSTZ-110; 12.825 MHz to 80 MHz for ADV7401BSTZ-80).
38	XTAL	I	Input pin for 28.6363 MHz crystal, or can be overdriven by an external 3.3 V 28.6363 MHz clock oscillator source to clock the ADV7401.
37	XTAL1	O	This pin should be connected to the 28.6363 MHz crystal or left as a no connect if an external 3.3 V 28.6363 MHz clock oscillator source is used to clock the ADV7401. In crystal mode the crystal must be a fundamental crystal.
46	ELPF	O	The recommend external loop filter must be connected to this ELPF pin.
70	TEST0		This pin should be left unconnected or alternatively tied to AGND.
59	TEST1	O	This pin should be left unconnected.
15	SFL/SYNC_OUT	O	Subcarrier Frequency Lock (SFL). This pin contains a serial output stream which can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder. SYNC_OUT is the sliced sync output signal only available in CP mode.
64	REFOUT	O	Internal Voltage Reference Output.
65	CML	O	Common-Mode Level Pin (CML) for the internal ADCs.
61, 62	CAPY1 to CAPY2	I	ADC Capacitor Network.
68, 69	CAPC1 to CAPC2	I	ADC Capacitor Network.
67	BIAS	O	External Bias Setting Pin. Connect the recommended resistor (1.35k) between pin and ground.
86	HS_IN/CS_IN	I	Can be configured in CP mode to be either a digital HS input signal or a digital CS input signal used to extract timing in a 5-wire or 4-wire RGB mode.
85	VS_IN	I	VS input signal. Used in CP mode for 5-wire timing mode.
79	DE_IN	I	Data Enable Input Signal. Used in 24-bit digital input port mode (for example, processing 24-bit RGB data from a DVI Rx IC).
35	DCLK_IN	I	Clock Input Signal. Used in 24-bit digital input mode (for example, processing 24-bit RGB data from a DVI Rx IC) and also in digital CVBS input mode.
52	SOG	I	Sync on Green Input. Used in embedded sync mode.
77	SOY	I	Sync on Luma Input. Used in embedded sync mode.

IC63 : CD0040AF

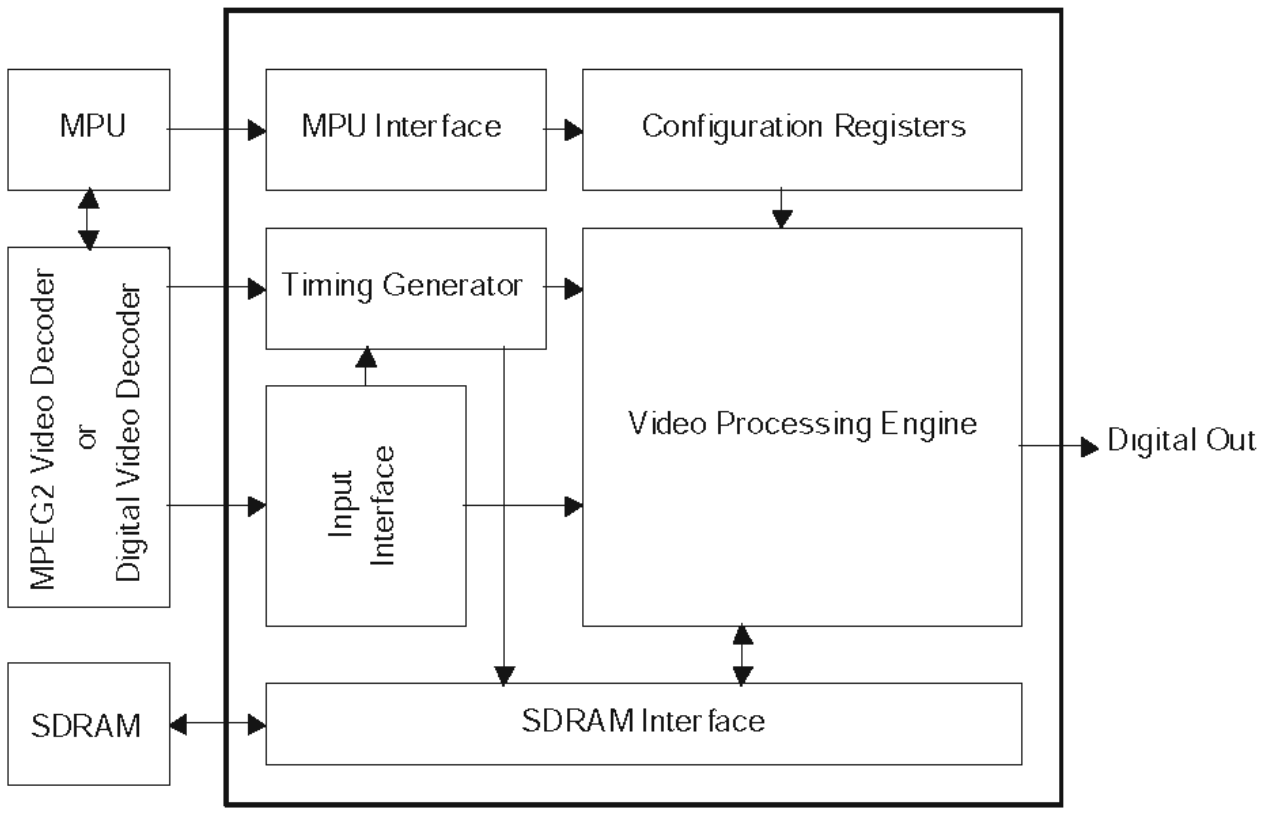
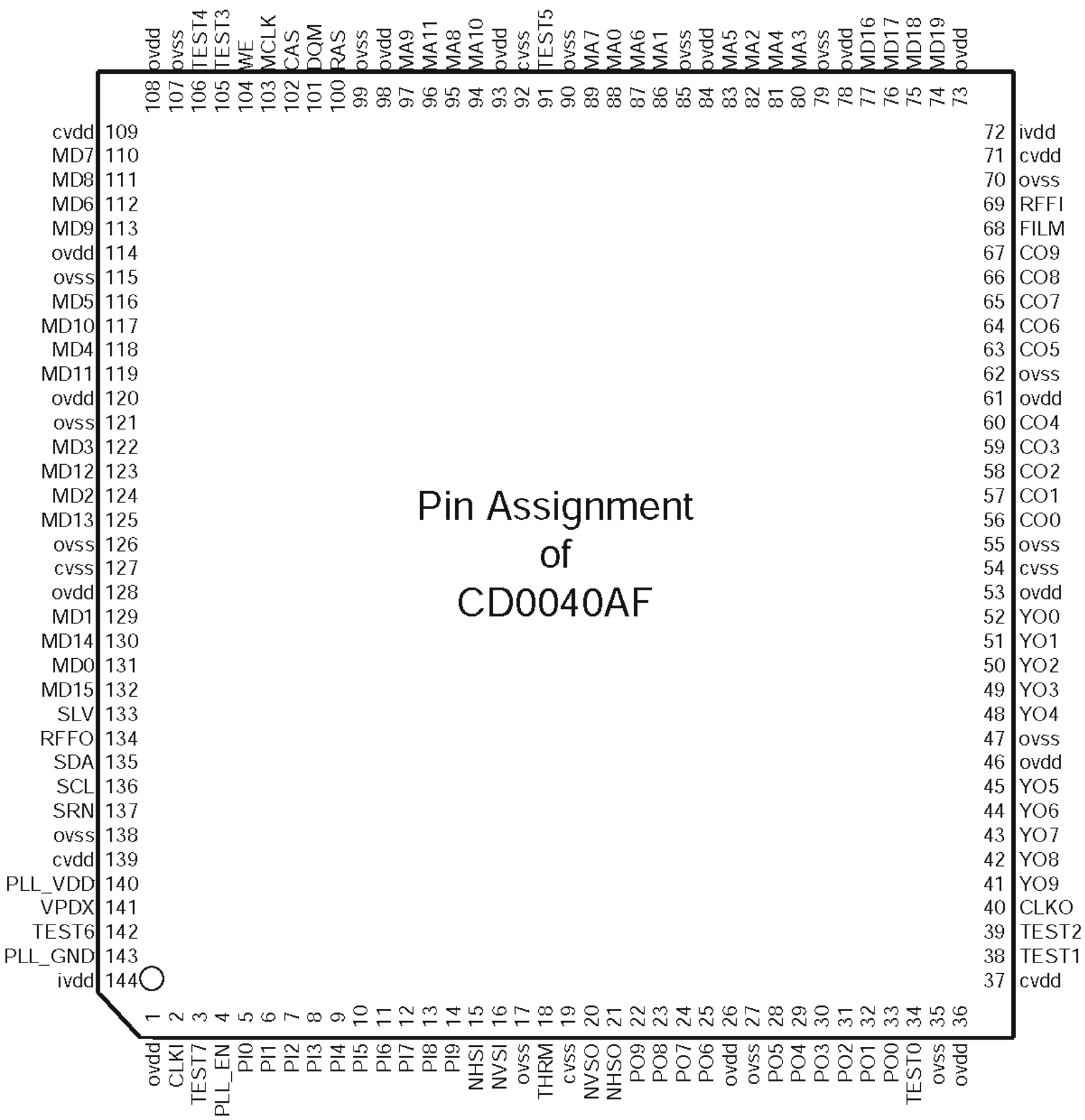


Fig. 2-1: System Block Diagram



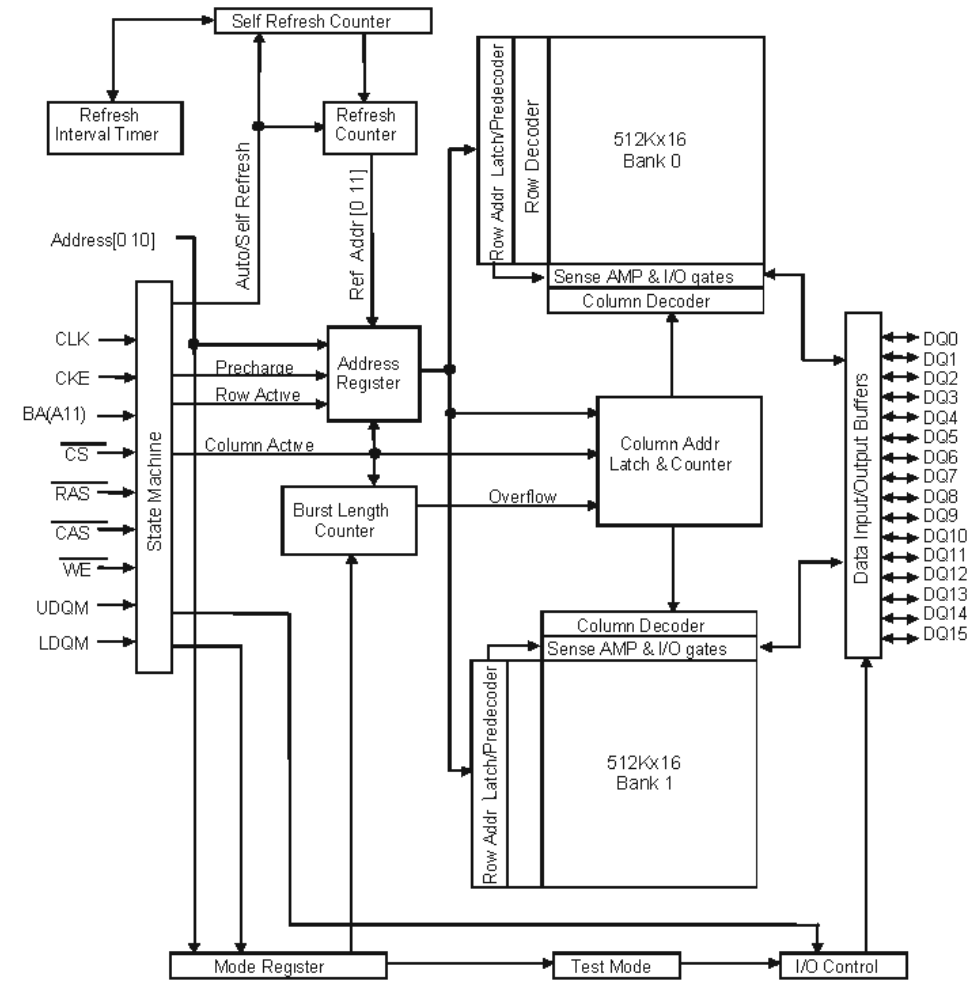
IC63 : CD0040AF

No	Name	I/O[1]	Attribute	Functional Description
1	OVDD	P	-	Positive supply voltage(+3.3V) for Pad Ring
2	CLKI	In	CMOS	System Clock Input (27MHz)
3	TEST7	In	CMOS	Test purpose only(must be connected to Ground)
4	PLL_EN	In	CMOS	PLL enable
5	PI0	In	CMOS	ITU-R BT 656/601 Input (LSB)
6	PI1	In	CMOS	ITU-R BT 656/601 Input
7	PI2	In	CMOS	ITU-R BT 656/601 Input
8	PI3	In	CMOS	ITU-R BT 656/601 Input
9	PI4	In	CMOS	ITU-R BT 656/601 Input
10	PI5	In	CMOS	ITU-R BT 656/601 Input
11	PI6	In	CMOS	ITU-R BT 656/601 Input
12	PI7	In	CMOS	ITU-R BT 656/601 Input
13	PI8	In	CMOS	ITU-R BT 656/601 Input
14	PI9	In	CMOS	ITU-R BT 656/601 Input (MSB)
15	NHSI	In	Schmitt	Active low horizontal sync input
16	NVSI	In	Schmitt	Active low vertical sync input
17	OVSS	P	-	Digital ground for Pad Ring
18	THMD	In	Schmitt	Through mode setting terminal Usually, this must be connected to ground
19	CVSS	P	-	Digital ground for Core
20	NVSO	Out	2mA	Active low vertical sync output (Interlace or Progressive) Refer 11.2Video Output
21	NHSO	Out	2mA	Active low horizontal sync output(Interlace or Progressive) Refer 11.2Video Output
22	PO9	Inout	CMOS / 2mA	ITU-R BT 656/601 output (MSB) / clamp signal output / ITU-R BT 601 Cb Cr input(MSB)
23	PO8	Inout	CMOS / 2mA	ITU-R BT 656/601 output / Video active signal output / ITU-R BT 601 CbCr input Refer 11.1Video Input 11.2Video Output 11.3Through Mode
24	PO7	Inout	CMOS / 2mA	ITU-R BT 656/601 output / Video blanking signal output / ITU-R BT 601 CbCr input Refer 11.1Video Input 11.2Video Output
25	PO6	Inout	CMOS / 2mA	ITU-R BT 656/601 output / ITU-R BT 601 CbCr input Refer 11.1Video Input 11.2Video Output 11.3Through Mode
26	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
27	OVSS	P	-	Digital ground for Pad Ring
28	PO5	Inout	CMOS / 2mA	ITU-R BT 656/601 output / ITU-R BT 601 CbCr input Refer 11.1Video Input 11.2Video Output 11.3Through Mode
29	PO4	Inout	CMOS / 2mA	ITU-R BT 656/601 output / ITU-R BT 601 CbCr input Refer 11.1Video Input 11.2Video Output 11.3Through Mode
30	PO3	Inout	CMOS / 2mA	ITU-R BT 656/601 output / ITU-R BT 601 CbCr input Refer 11.1Video Input 11.2Video Output 11.3Through Mode
31	PO2	Inout	CMOS / 2mA	ITU-R BT 656/601 output / ITU-R BT 601 CbCr input Refer 11.1Video Input 11.2Video Output 11.3Through Mode
32	PO1	Inout	CMOS / 2mA	ITU-R BT 656/601 output / ITU-R BT 601 CbCr input *2 Refer 11.1Video Input 11.2Video Output 11.3Through Mode
33	PO0	Inout	CMOS / 2mA	ITU-R BT 656/601 output (LSB) / ITU-R BT 601 CbCr input *2 Refer 11.1Video Input 11.2Video Output 11.3Through Mode
34	TEST0	In	CMOS	Test purpose only (must be connected to ground)
35	OVSS	P	-	Digital ground for Pad Ring
36	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
37	CVDD	P	-	Digital positive supply voltage (+2.5V) for core
38	TEST1	In	CMOS	Test purpose only (must be connected to ground)
39	TEST2	In	CMOS	Test purpose only (must be connected to ground)
40	CLKO	Out	2mA	Clock output(27MHz)
41	YO9	Out	4mA	ANSI/SMPTE 293M Y output(MSB)
42	YO8	Out	4mA	ANSI/SMPTE 293M Y output
43	YO7	Out	4mA	ANSI/SMPTE 293M Y output
44	YO6	Out	4mA	ANSI/SMPTE 293M Y output
45	YO5	Out	4mA	ANSI/SMPTE 293M Y output
46	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
47	OVSS	P	-	Digital ground for Pad Ring
48	YO4	Out	4mA	ANSI/SMPTE 293M Y output
49	YO3	Out	4mA	ANSI/SMPTE 293M Y output
50	YO2	Out	4mA	ANSI/SMPTE 293M Y output
51	YO1	Out	4mA	ANSI/SMPTE 293M Y output
52	YO0	Out	4mA	ANSI/SMPTE 293M Y output (LSB)
53	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
54	CVSS	P	-	Digital ground for core
55	OVSS	P	-	Digital ground for Pad Ring
56	CO0	Out	4mA	ANSI/SMPTE 293M Cb/Cr output
57	CO1	Out	4mA	ANSI/SMPTE 293M Cb/Cr output
58	CO2	Out	4mA	ANSI/SMPTE 293M Cb/Cr output
59	CO3	Out	4mA	ANSI/SMPTE 293M Cb/Cr output
60	CO4	Out	4mA	ANSI/SMPTE 293M Cb/Cr output
61	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
62	OVSS	P	-	Digital ground for Pad Ring
63	CO5	Out	4mA	ANSI/SMPTE 293M Cb/Cr output
64	CO6	Out	4mA	ANSI/SMPTE 293M Cb/Cr output
65	CO7	Out	4mA	ANSI/SMPTE 293M Cb/Cr output
66	CO8	Out	4mA	ANSI/SMPTE 293M Cb/Cr output
67	CO9	Out	4mA	ANSI/SMPTE 293M Cb/Cr output (MSB)
68	FILM	Out	2mA	Film sequence detection flag output. Refer 11.4.1.9Film detection Flag Output
69	RFFI	In	CMOS	MPEG flag (Repeat First Field) input port Refer 11.4.1.6Film I/P Conversion 11.4.1.8Film Sequence Flag Control Mode
70	OVSS	P	-	Digital ground for Pad Ring
71	CVDD	P	-	Digital positive supply voltage (+2.5V) for core
72	IVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
73	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
74	MD19	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
75	MD18	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
76	MD17	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
77	MD16	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
78	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
79	OVSS	P	-	Digital ground for Pad Ring
80	MA3	Out	4mA	Address output port for SDRAM
81	MA4	Out	4mA	Address output port for SDRAM
82	MA2	Out	4mA	Address output port for SDRAM
83	MA5	Out	4mA	Address output port for SDRAM
84	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
85	OVSS	P	-	Digital ground for Pad Ring
86	MA1	Out	4mA	Address output port for SDRAM
87	MA6	Out	4mA	Address output port for SDRAM
88	MA0	Out	4mA	Address output port for SDRAM (LSB)
89	MA7	Out	4mA	Address output port for SDRAM
90	OVSS	P	-	Digital ground for Pad Ring
91	IVSS	P	-	Digital ground for Pad Ring
92	CVSS	P	-	Digital ground for Pad Ring for Core
93	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
94	MA10	Out	4mA	Address output port for SDRAM
95	MA8	Out	4mA	Address output port for SDRAM
96	MA11	Out	4mA	Address output port for SDRAM (MSB)
97	MA9	Out	4mA	Address output port for SDRAM
98	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
99	OVSS	P	-	Digital ground for Pad Ring
100	RAS	Out	4mA	Row Address Strobe command output port for SDRAM
101	DQM	Out	4mA	DQM output port for SDRAM In addition, please connect the CKE terminal of SDRAM to the power supply of SDRAM
102	CAS	Out	4mA	Column Address Strobe command output port for SDRAM
103	MCLK	Out	4mA	Clock output port for SDRAM (54MHz)
104	WE	Out	4mA	Write Enable output port for SDRAM
105	TEST3	In	CMOS	Test purpose only (must be connected to ground)
106	TEST4	In	CMOS	Test purpose only (must be connected to ground)
107	OVSS	P	-	Digital ground for Pad Ring
108	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
109	CVDD	P	-	Digital positive supply voltage (+2.5V) for core
110	MD7	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
111	MD8	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
112	MD6	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
113	MD9	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
114	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
115	OVSS	P	-	Digital ground for Pad Ring
116	MD5	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
117	MD10	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
118	MD4	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
119	MD11	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
120	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
121	OVSS	P	-	Digital ground for Pad Ring
122	MD3	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
123	MD12	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
124	MD2	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
125	MD13	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
126	OVSS	P	-	Digital ground for Pad Ring
127	CVSS	P	-	Digital ground for core
128	OVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring
129	MD1	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
130	MD14	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
131	MD0	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
132	MD15	Inout	CMOS, pull-up / 4mA	Data input/output port for SDRAM
133	SLV	In	CMOS	Slave address selection input for I2C Slave address is set up to 0x72 when SLV is 0 , 0x70 when 1
134	RFFO	Out	2mA	MPEG flag (Repeat First Field) output port If not used, leave open
135	SDA	Inout	Schmitt, 3.3V / 4mA	Data input/output of MPU interface
136	SCL	In	Schmitt, 3.3V	Clock input of MPU interface
137	SRN	In	Schmitt	System reset input(negative)
138	OVSS	P	-	Digital ground for Pad Ring
139	CVDD	P	-	Digital positive supply voltage (+2.5V) for core
140	PLL_VDD	P	-	Digital positive supply voltage (+2.5V) for PLL
141	VPDX	In	CMOS	Must be connected to ground
142	TEST6	In	CMOS	Test purpose only (must be connected to ground)
143	PLL_GND	P	-	Ground for PLL
144	IVDD	P	-	Positive supply voltage (+3.3V) for Pad Ring

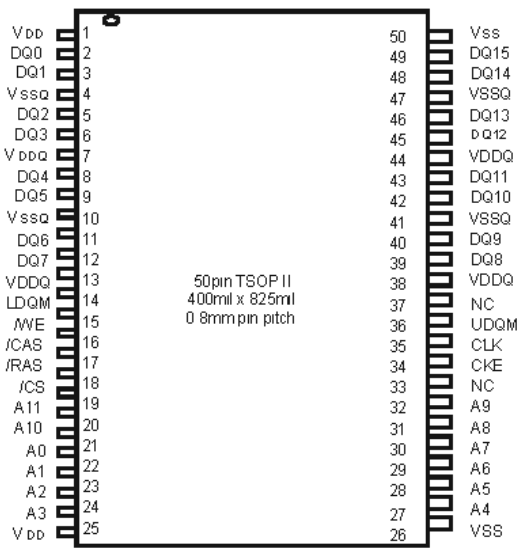
Note *1 P10 and P11 should be connected to GND at the time of 8bit input
*2 PO0 and PO1 should connected to GND at the time of 8bit input
*3 Although the same bidirectional buffer as PO is used in order to unite PO and timing at the time of PO input, it is always fixed as an input
*4 The initial-setting value or the initial state in a reset period and after reset release

IC64 : HY57V161610ET-7

1Mx16 Synchronous DRAM



PIN CONFIGURATION

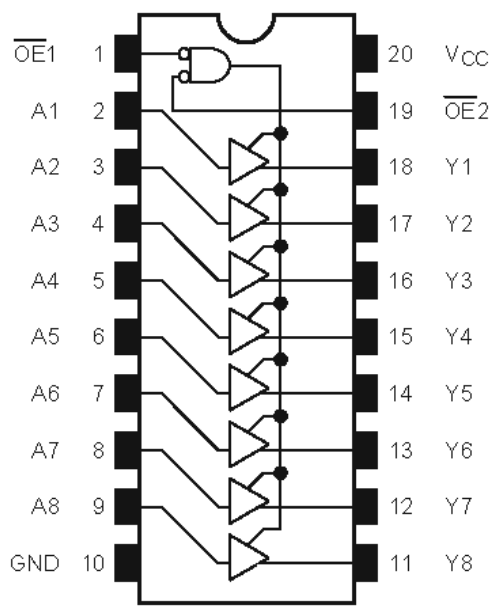


PIN DESCRIPTION

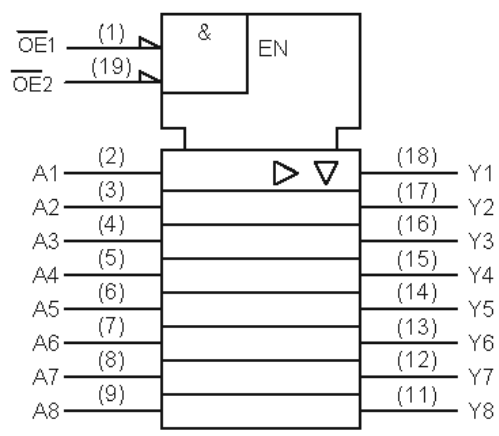
PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are referenced to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Command input enable or mask except CLK, CKE and DQM
BA	Bank Address	Select either one of banks during both $\overline{RAS}$ and $\overline{CAS}$ activity
A0 ~ A10	Address	Row Address : RA0 ~ RA10, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	DQM control output buffer in read mode and mask input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuit and input buffer
VDDQ/VSSQ	Data Output Power/Ground	Power supply for DQ
NC	No Connection	No connection

IC65 : TC74VCX541FT
IC66 : TC74VCX541FT
IC67 : TC74VCX541FT
IC68 : TC74VCX541FT
IC69 : TC74VCX541FT
IC70 : TC74VCX541FT

Pin Assignment (top view)



IEC Logic Symbol



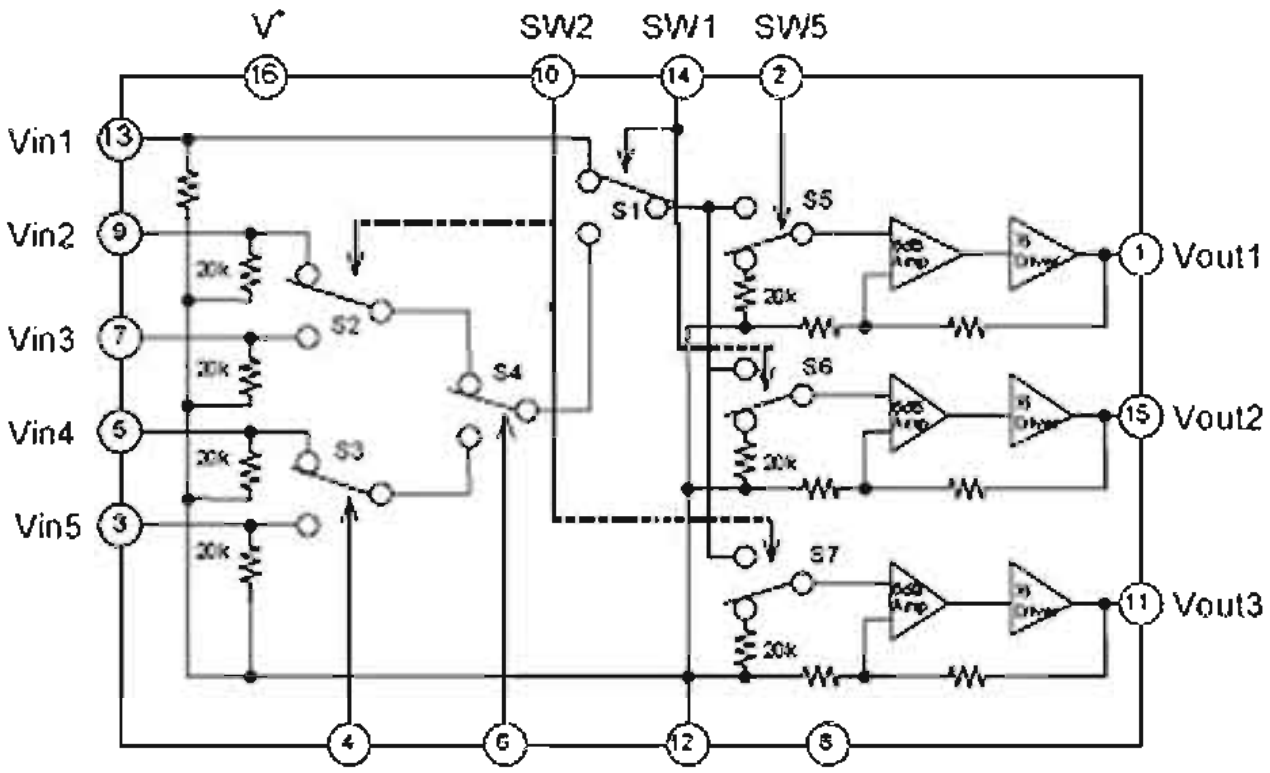
Truth Table

Inputs			Outputs
$\overline{OE1}$	$\overline{OE2}$	An	
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

X: Don't care

Z: High impedance

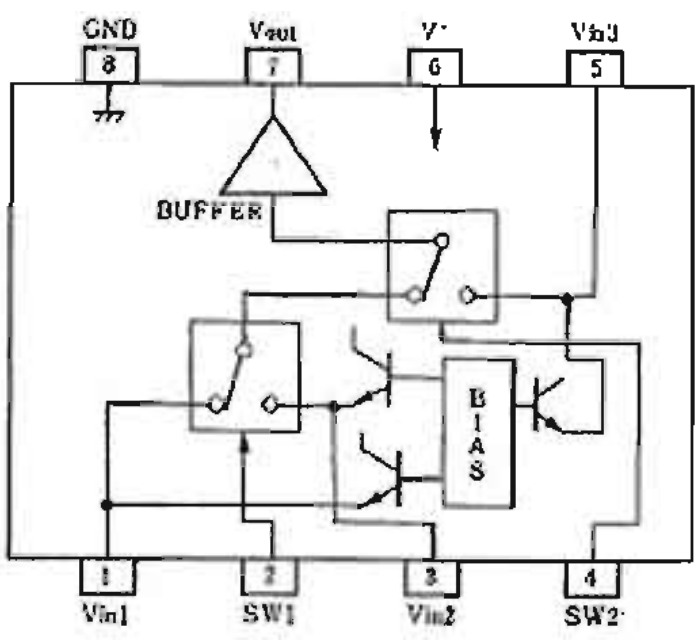
IC71 : NJM2595MTE1
IC72 : NJM2595MTE1
IC73 : NJM2595MTE1
IC81 : NJM2595MTE1



Control Signal vs. Output Signal (L=V_{SS}, H=V_{DD}, X=L or H)

SW1	SW2	SW3	SW4	SW5	Vout1	Vout2	Vout3
L	H	X	X	H	Vin1	MUTE	Vin1
	L			H	Vin1	MUTE	MUTE
	H			L	MUTE	MUTE	Vin1
H	L	X	L	H	Vin2	Vin2	MUTE
				L	MUTE	Vin2	MUTE
H	H	X	L	H	Vin3	Vin3	Vin3
				L	MUTE	Vin3	Vin3
H	H	L	H	H	Vin4	Vin4	Vin4
	H			L	MUTE	Vin4	Vin4
	L			H	Vin4	Vin4	MUTE
	L			L	MUTE	Vin4	MUTE
H	H	H	H	H	Vin5	Vin5	Vin5
	H			L	MUTE	Vin5	Vin5
	L			H	Vin5	Vin5	MUTE
	L			L	MUTE	Vin5	MUTE
L	L	X	X	L	MUTE	MUTE	MUTE

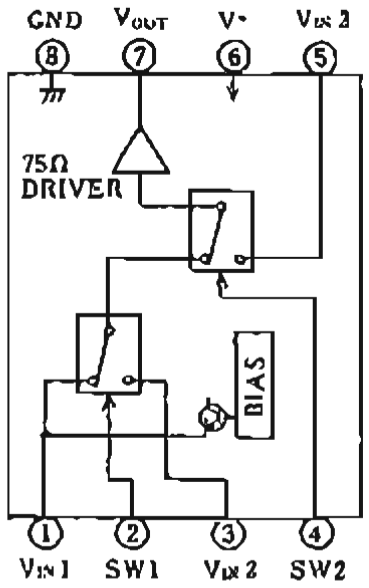
IC74 : NJM2535D



PIN FUNCTION
1 : Vin1
2 : SW1
3 : Vin2
4 : SW2
5 : Vin3
6 : V'
7 : V_{OUT}
8 : GND

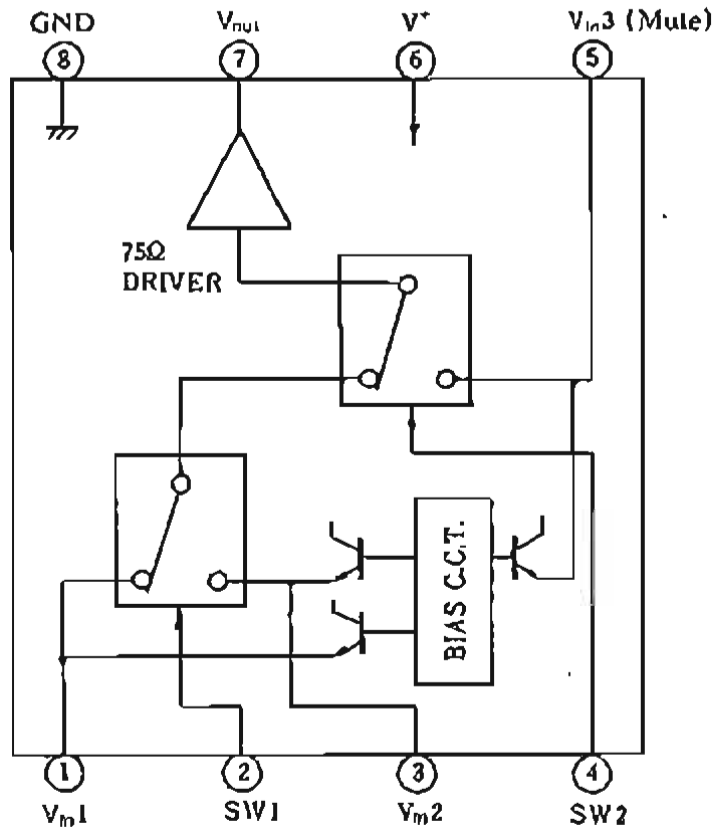
SW1	SW2	OUTPUT SIGNAL
L	L	$V_{IN}1$
H	L	$V_{IN}2$
L/H	H	$V_{IN}3$

IC75 : NJM2264D



SW 1	SW 2	OUTPUT SIGNAL
L	L	V_{IN} 1
H	L	V_{IN} 2
L/H	H	V_{IN} 3

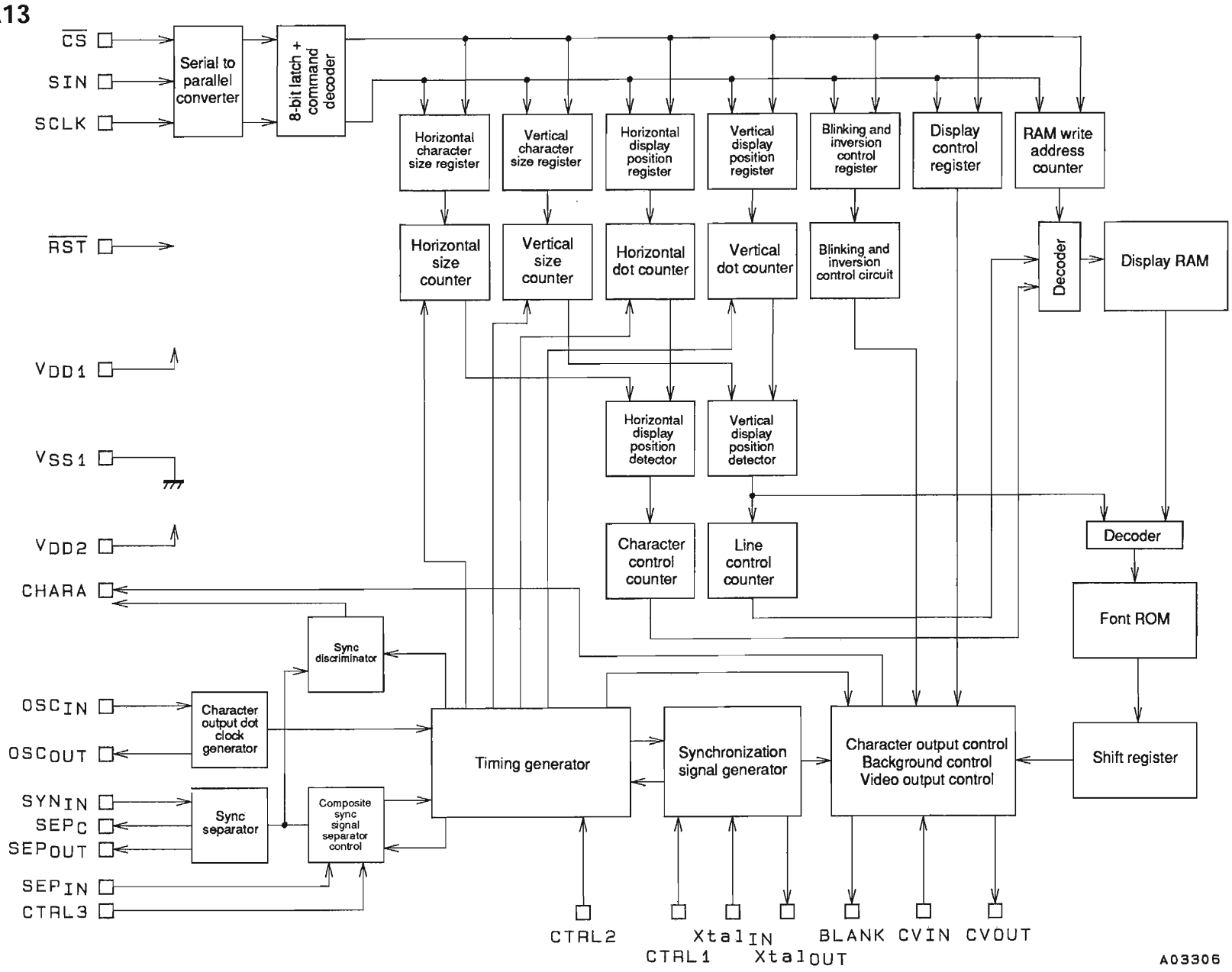
IC76 : NJM2244D
IC77 : NJM2244D
IC82 : NJM2244D



SW 1	SW 2	OUTPUT SIGNAL
L	L	V_{IN} 1
H	L	V_{IN} 2
L/H	H	V_{IN} 3

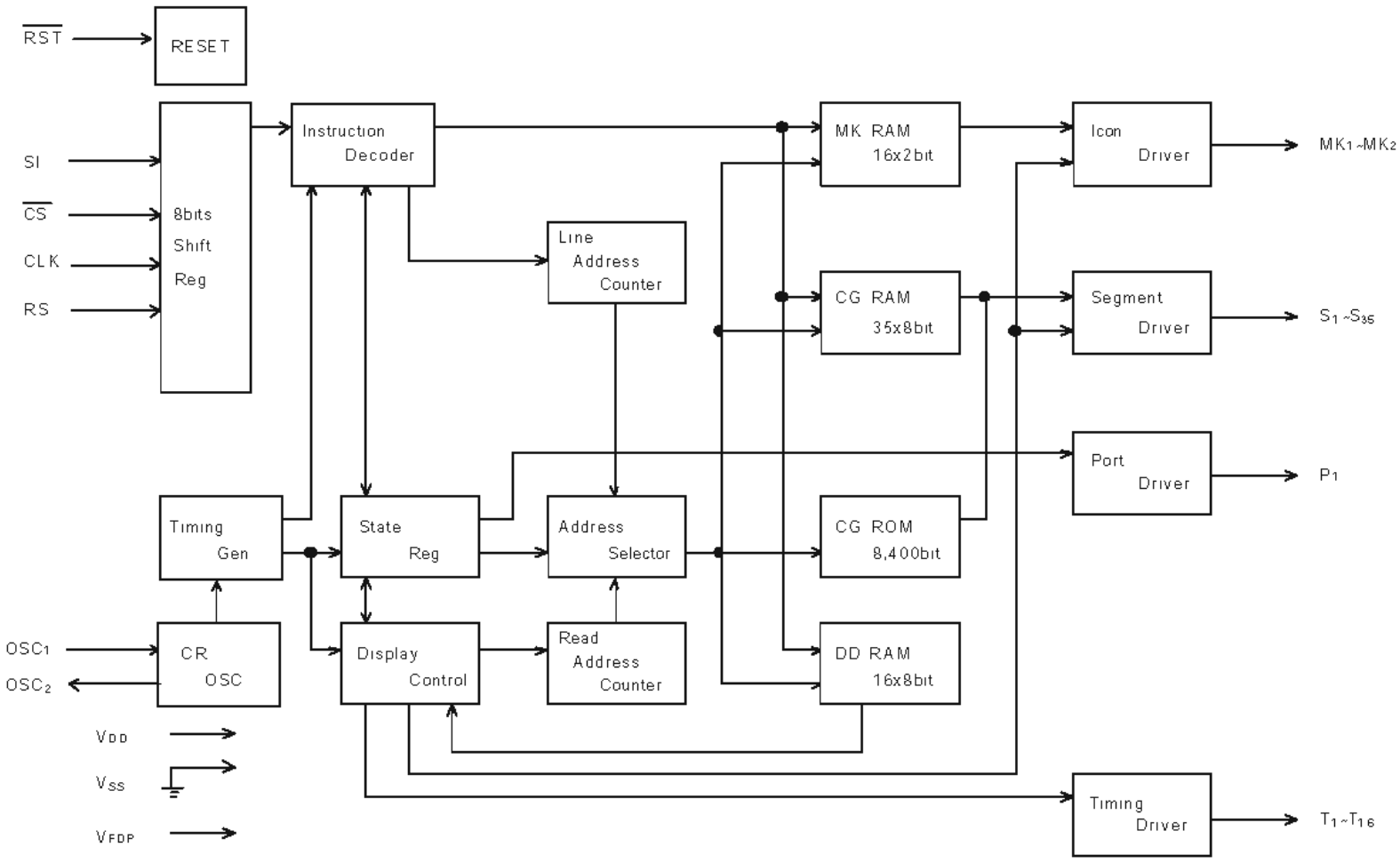
note): Input clamp voltage is about 2/5 of supply voltage.

IC78 : LC747828A13



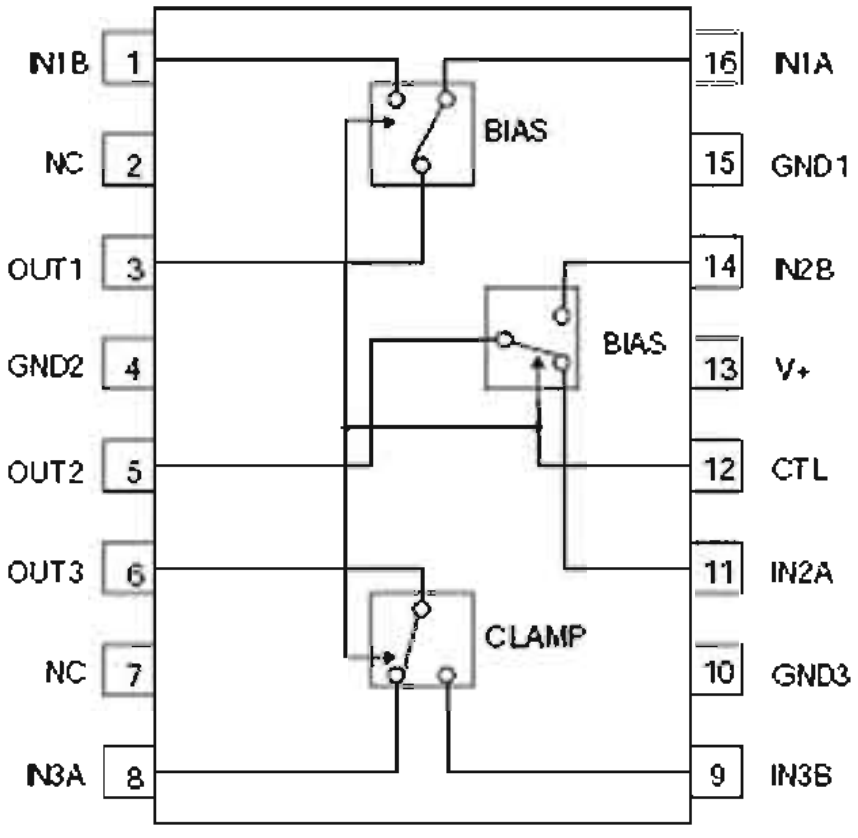
Pin No.	Symbol	Function	Description
1	$V_{SS}1$	Ground	Ground connection (digital system ground)
2	$Xtal_{IN}$	Crystal oscillator connection	Used to connect the crystal oscillator and capacitor used to generate the internal synchronization signal, or to input an external clock (2fsc or 4fsc).
3	$Xtal_{OUT}$		
4	CTRL1	Crystal oscillator input switching	Switches between external clock input mode and crystal oscillator mode. Low = crystal oscillator mode, high = external clock mode
5	BLANK	Blanking output	Outputs the blank signal (the OR of the character and border signals). (Outputs a composite sync signal when MOD0 is high.) Outputs the crystal oscillator clock during reset (when the $\overline{RST}$ pin is low), but can be set up to not output this signal by microprocessor command.
6	OSC_{IN}	LC oscillator connection	Connections for the coil and capacitor that form the oscillator that generates the character output dot clock.
7	OSC_{OUT}		
8	CHARA	Character output	Outputs the character signal. (Functions as the external synchronization signal discrimination signal output pin when MOD0 is high, and outputs the state of the judgment as to whether the external synchronization signal is present or not. Outputs a high level when the synchronization signal is present.) Outputs the dot clock (LC oscillator) during reset, but can be set up to not output this signal by microprocessor command.
9	CS	Enable input	Serial data input enable input. Serial data input is enabled when low. A pull-up resistor is built in (hysteresis input).
10	SCLK	Clock input	Serial data input clock input. A pull-up resistor is built in (hysteresis input).
11	SIN	Data input	Serial data input. A pull-up resistor is built in (hysteresis input).
12	$V_{DD}2$	Power supply	Composite video signal level adjustment power supply pin (analog system power supply).
13	CV_{OUT}	Video signal output	Composite video signal output
14	NC		Must be either connected to ground or left open.
15	CV_{IN}	Video signal input	Composite video signal input
16	$V_{DD}1$	Power supply	Power supply (+5 V: digital system power supply)
17	SYN_{IN}	Sync separator circuit input	Video signal input for the built-in sync separator circuit (Used for either horizontal synchronization signal or composite sync signal input when the built-in sync separator circuit is not used.)
18	SEP_C	Sync separator circuit bias voltage	Built-in sync separator circuit bias voltage monitor pin
19	SEP_{OUT}	Composite sync signal output	Built-in sync separator circuit composite sync signal output. (When MOD1 is high, outputs a high level during internal synchronization and a low level during external synchronization.) (Outputs the SYN_{IN} input signal when the internal sync separator circuit is not used.)
20	SEP_{IN}	Vertical synchronization signal input	Inputs a vertical synchronization signal created by integrating the SEP_{OUT} pin output signal. An integrator must be attached at the SEP_{OUT} pin. This pin must be tied to $V_{DD}1$ if unused.
21	CTRL2	NTSC/PAL-M switching input	The setting indicated by this pin takes priority in switching between the NTSC, PAL, PAL-M and PAL-N formats. A low level selects NTSC after a reset. The microprocessor command NTSC, PAL, PAL-M, or PAL-N setting is valid. High = PAL-M format.
22	CTRL3	SEP_{IN} input control	Controls whether or not the $\overline{VSYNC}$ signal is input to the SEP_{IN} input. Low = $\overline{VSYNC}$ input, high = $\overline{VSYNC}$ not input.
23	$\overline{RST}$	Reset input	System reset input. A pull-up resistor is built in (hysteresis input).
24	$V_{DD}1$	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

IC81 : NJU3430F



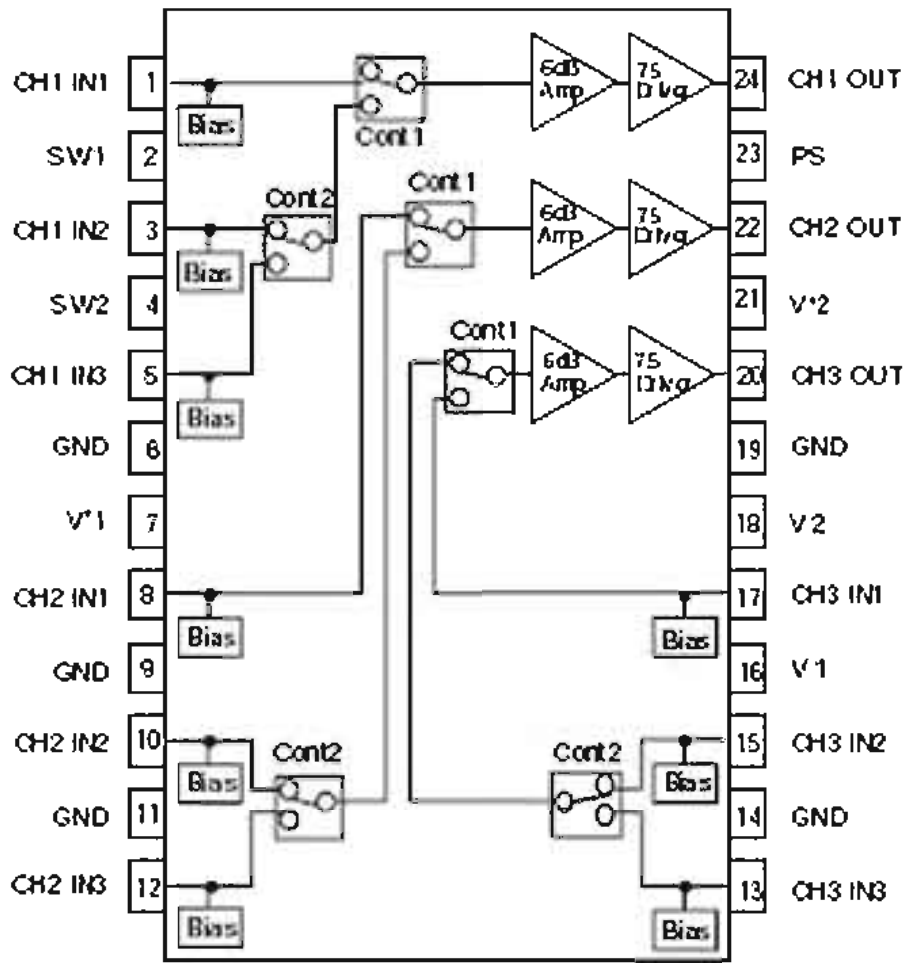
No.	SYMBOL	I/O	F U N C T I O N
57	VDD	-	Power Source : VDD=+3.0 to 5.5V
49	VSS	-	GND : VSS=0V
48	VFDP	-	VFD Driving Power Sourse VDD-20V to VDD-45V
50	OSC1	I	CR Oscillation Terminal External R and C connect to these terminals. (Target fOSC=360kHz)
51	OSC2	O	
54	CLK	I	Serial Clock Input Terminal The serial data input synchronizing the rise edge of this terminal.
53	$\overline{CS}$	I	Chip Select Terminal When the CS terminal is "H" the serial data input is not available.
55	SI	I	Serial Data Input Terminal The data input is MSB first.
56	RS	I	Register Selection Signal Input Terminal RS="0" : Instruction Register RS="1" : Data Register
52	$\overline{RST}$	I	Reset Terminal RST="L" : Reset -Each Address : (00)H -Each RAM Data : Unfixed -Display Digits : 16-digit -Contrast Control : 8/16 Dury -All Display Off -All Outputs are "L"
61 to 64, 1 to 31	S1 to S35	O	Segment Output Terminals (Internal Pull-down Resistance)
32 to 47	T1 to T16	O	Timing Output Terminals (Internal Pull-down Resistance)
60 59	MK1 MK2	O	Icon Output Terminals (Internal Pull-down Resistance)
58	P1	O	Output Port Terminal This terminal is suitable for LED.

IC91 : NJM2584M
IC92 : NJM2584M
IC93 : NJM2584M
IC96 : NJM2584M (SR8001 only)
IC97 : NJM2584M (SR8001 only)
IC98 : NJM2584M (SR8001 only)



PIN	MODE	NOTES
Control	H	B channel output
	L	A channel output
	OPEN	A channel output

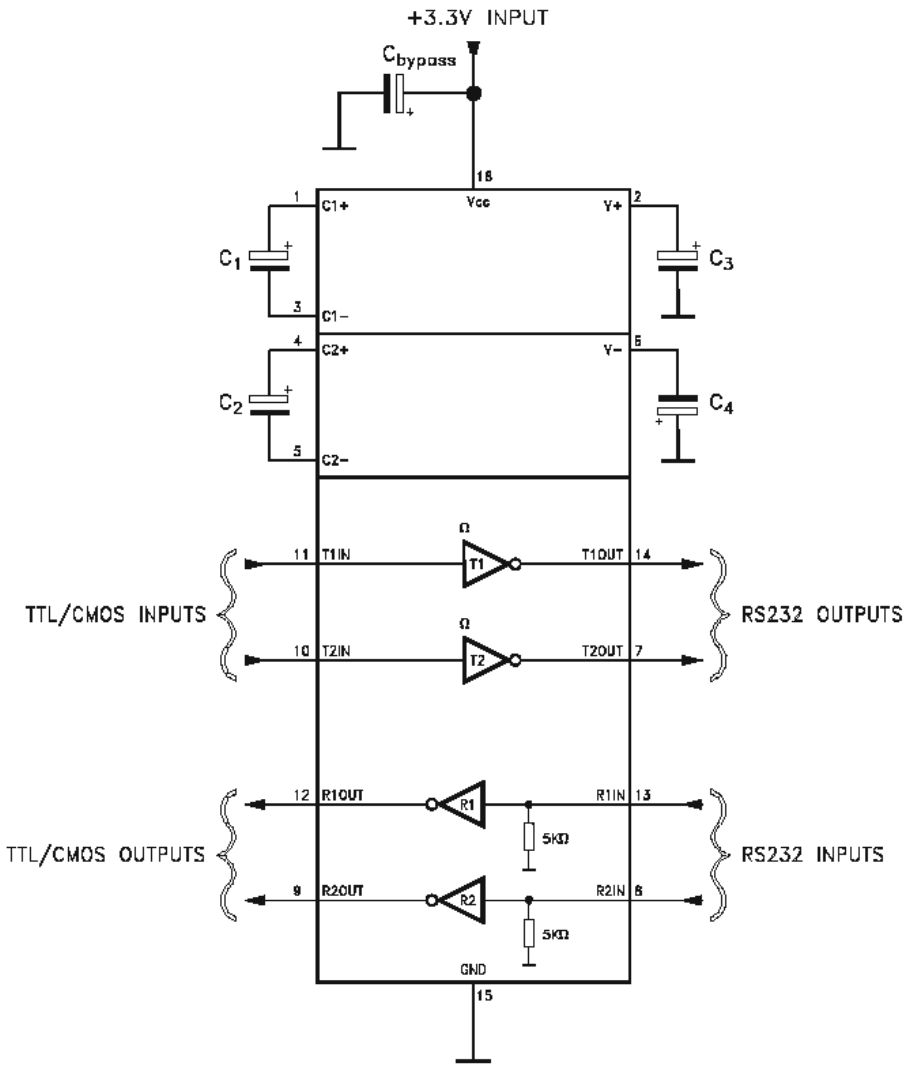
IC94 : NJM2586AM
IC99 : NJM2586AM (SR8001 only)



PARAMETER	STATUS	NOTE
PS	H	Power Save OFF
	L	Power Save ON
	OPEN	Power Save ON

PARAMETER	STATUS		NOTE
	SW1	SW2	
SW1, SW2I	L, OPEN	X	IN1 (X=don't care)
	H	L, OPEN	IN2
	H	H	IN3

IC92 : ST3232ECWR



PIN DESCRIPTION

PIN N°	SYMBOL	NAME AND FUNCTION
1	C_1+	Positive Terminal for the first Charge Pump Capacitor
2	V+	Doubled Voltage Terminal
3	C_1-	Negative Terminal for the first Charge Pump Capacitor
4	C_2+	Positive Terminal for the second Charge Pump Capacitor
5	C_2-	Negative Terminal for the second Charge Pump Capacitor
6	V-	Inverted Voltage Terminal
7	$T2_{OUT}$	Second Transmitter Output Voltage
8	$R2_{IN}$	Second Receiver Input Voltage
9	$R2_{OUT}$	Second Receiver Output Voltage
10	$T2_{IN}$	Second Transmitter Input Voltage
11	$T1_{IN}$	First Transmitter Input Voltage
12	$R1_{OUT}$	First Receiver Output Voltage
13	$R1_{IN}$	First Receiver Input Voltage
14	$T1_{OUT}$	First Transmitter Output Voltage
15	GND	Ground
16	V_{CC}	Supply Voltage