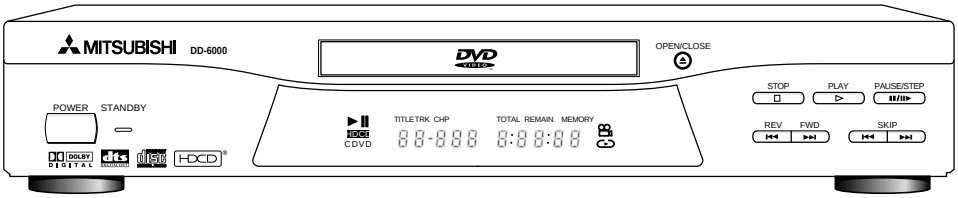
2000

MITSUBISHI ELECTRIC

Service Manual

DVD Player

Model
DD-6000



This service manual contains the differences between models DD-5000 and DD-6000. It also includes information for the DD-6000 that is identical to the DD-5000.

CAUTION

Before servicing this chassis, it is important that the service person reads all SAFETY PRECAUTIONS and the SAFETY NOTICE in this manual.

SPECIFICATIONS

Power Supply:	120V AC, 60 Hz
Power Consumption:	19W
Weight:	6.8 lb.
External Dimensions:	17"x 3-1/4"x12-1/4" (W/H/D)
Signal System:	Standard NTSC
Laser:	Semiconductor laser, wavelength 650 nm
Frequency Range:	(Digital Audio)
Audio CD:	4 Hz to 20 kHz
DVD Linear -	
48 kHZ Sampling:	4 Hz to 22 kHz
96 kHZ Sampling:	4 Hz to 44 kHz
Signal-To-Noise Ratio:	More than 112 dB (EIAJ)
Audio Dynamic Range:	More than 106 dB (EIAJ)
Harmonic Distortion:	Less than 0.001%
Wow and flutter:	Below measurable level (less than ± 0.001% (W.PEAK)) (EIAJ)
Operating conditions:	Temperature: 5°C to 35°C
Operation status:	Horizontal
Video output:	1.0 V (p-p), 75Ω, negative sync., pin jack x 1
S Video output:	(Y) 1.0 V (p-p), 75Ω, negative sync., Mini DIN 4-pin x 1 (C) 0.286 V (p-p), 75Ω
Color Difference outputs:	(Y) 1.0 V (p-p), 75Ω,
(1 Interlaced)	negative sync., pin jack x 1
(1 Progressive)	(Cr, Pr)/(Cb, Pb) 0.7 V (p-p), 75Ω, pin jack x 2
Digital Audio output:	(Bitstream/PCM) 0.5 V (p-p), 75Ω, pin jack x 1, Optical connector x 1
Analog Audio output:	2.0 V (rms), 220Ω, pin jack 2 CH L R x 2, 5.1 CH SURROUND x 6

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SAFETY PRECAUTIONS

LEAKAGE CURRENT CHECK

Plug the AC line cord directly into a 120V AC outlet (do not use an isolation transformer for this check). Use an AC voltmeter, having 5000 Ω per volt or more sensitivity.

Connect a 1500 Ω 10 W resistor, paralleled by a 0.15 µF 150V AC capacitor between a known good earth ground (water pipe, conduit, etc.) and all exposed metal parts of the cabinet (antennas, handle bracket, metal cabinet screwheads, metal overlays, control shafts, etc.).

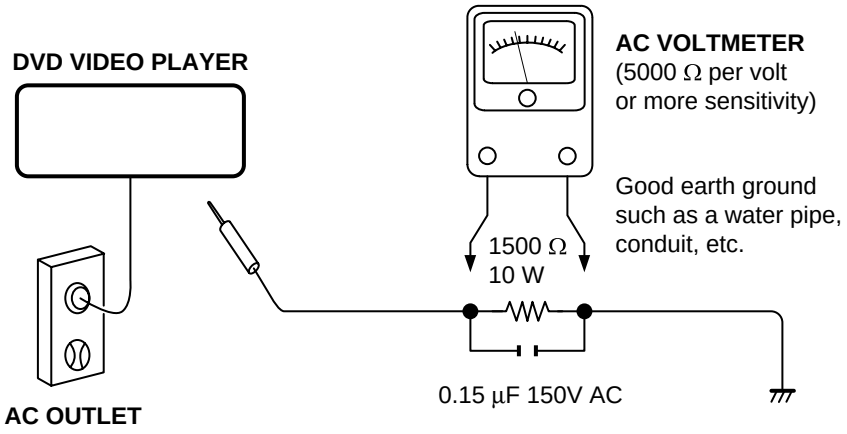
Measure the AC voltage across the 1500 Ω resistor.

The test must be conducted with the AC switch on and then repeated with the AC switch off. The AC voltage indicated by the meter may not exceed 0.3 V. A reading exceeding 0.3 V indicates that a dangerous potential exists, the fault must be located and corrected.

Repeat the above test with the DVD VIDEO PLAYER power plug reversed.

NEVER RETURN A DVD VIDEO PLAYER TO THE CUSTOMER WITHOUT TAKING NECESSARY CORRECTIVE ACTION.

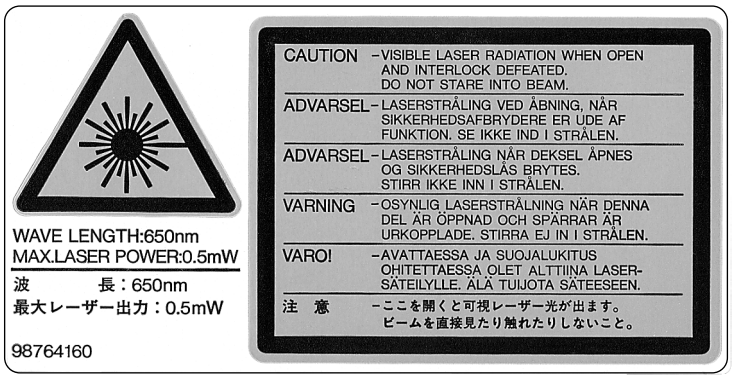
READING SHOULD NOT EXCEED 0.3V



Test all exposed metal.

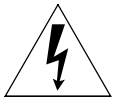
Voltmeter Hook-up for Leakage Current Check

LASER BEAM CAUTION LABEL



When the power supply is on, do not remove this laser caution label. If it is removed, laser radiation may be recceived.

SAFETY NOTICE



The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated “dangerous voltage” within the product’s enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

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SECTION 1
GENERAL DESCRIPTIONS

General descriptions such as preparation for servicing, location of mechanical parts and troubleshooting are the same as model DD-5000.

The pages from model DD-5000, Section 1, are included in this text.

SECTION 2
PART REPLACEMENT AND ADJUSTMENT PROCEDURES

Part replacement and adjustment procedures are the same as DD-5000.

The pages from model DD-5000, Section 2, are included in this text.

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   - 1-2. Solid Resistor Indication
   - 1-3. Capacitance Indication
   - 1-4. Inductor Indication
   - 1-5. Waveform and Voltage Measurement
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NOTICE
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   2. Capacitor (Cap)
   3. Resistor (Res)
4. EXPLODED VIEWS
   - 4-1. Packing Assembly
   - 4-2. Chassis Assembly
   - 4-3. Mechanism Assembly
5. PARTS LIST

SECTION 1
General Descriptions

1. PREPARATION FOR SERVICING

The Pickup Head consists of a laser diode that is very susceptible to external static electricity.

Although it may operate properly after replacement, if subjected to electrostatic discharge during replacement, its life may be shortened. When replacing the laser diode, LSI's and IC's, use a conductive mat, soldering iron with ground wire, etc. to protect against damage from static electricity.

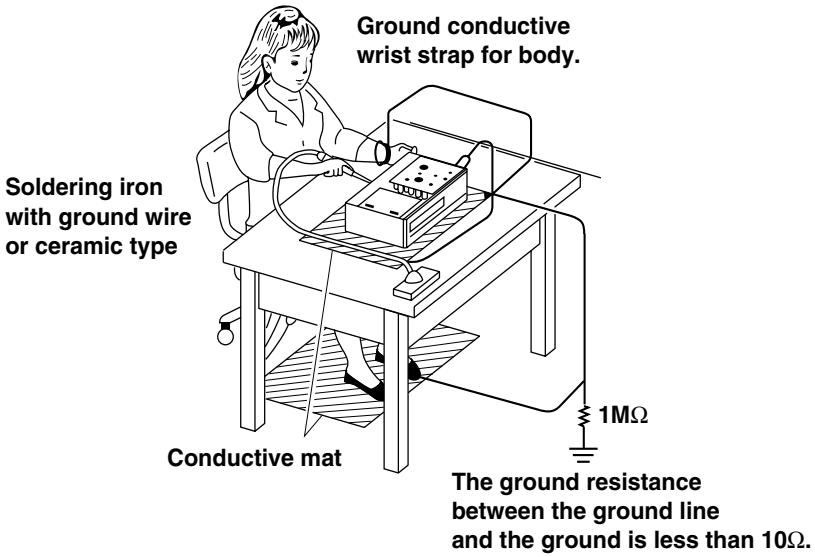


Fig. 1-1-1

2. LOCATION OF MAIN PARTS AND MECHANISM PARTS

2-1. Location of Main Parts

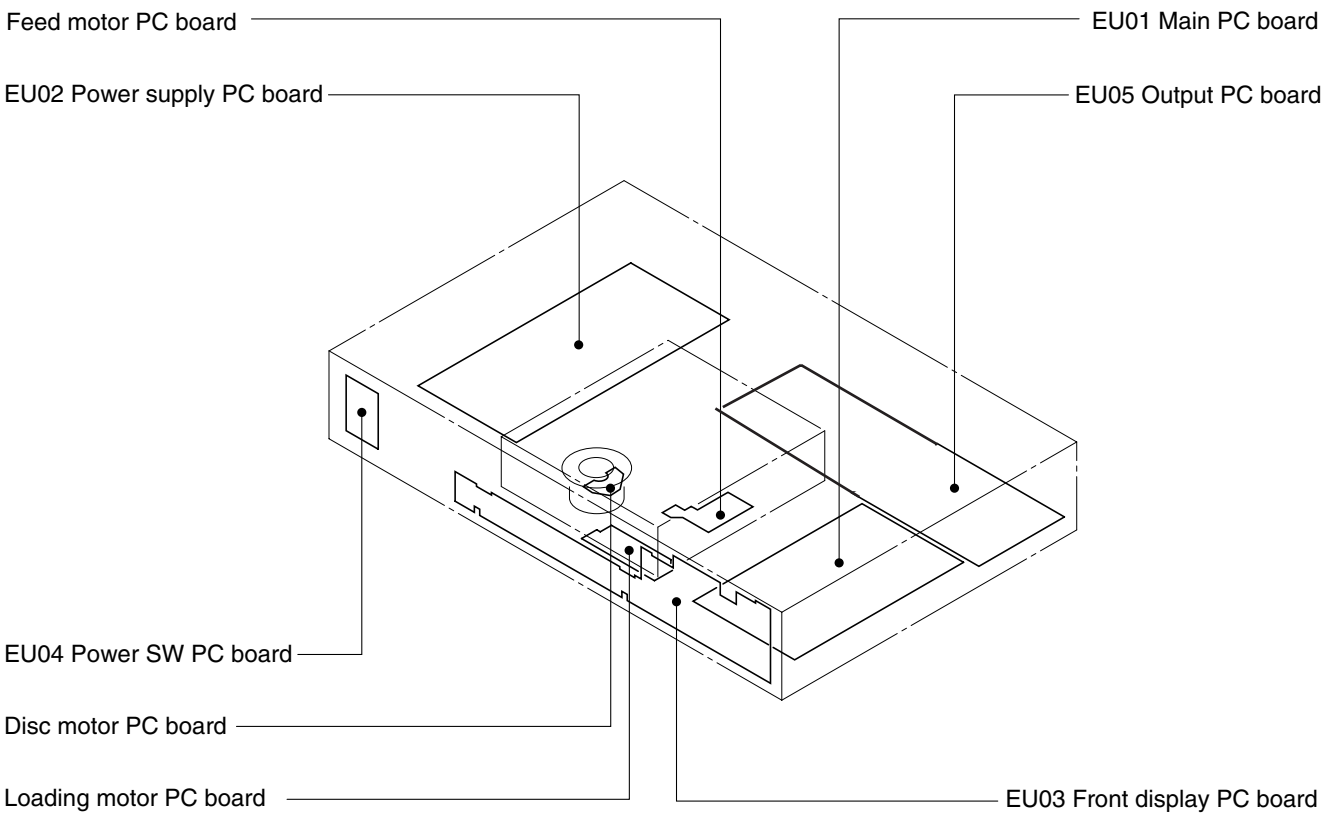


Fig. 1-2-1

2-2. Location of Mechanism Parts

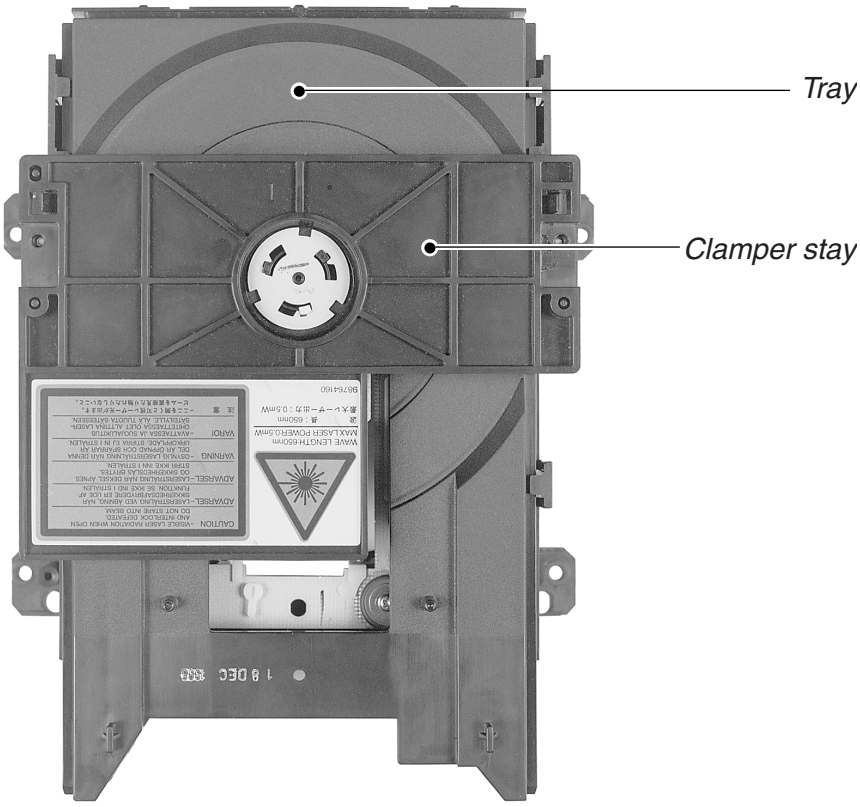


Fig. 1-2-2 Mechanism chassis assembly (Top side)

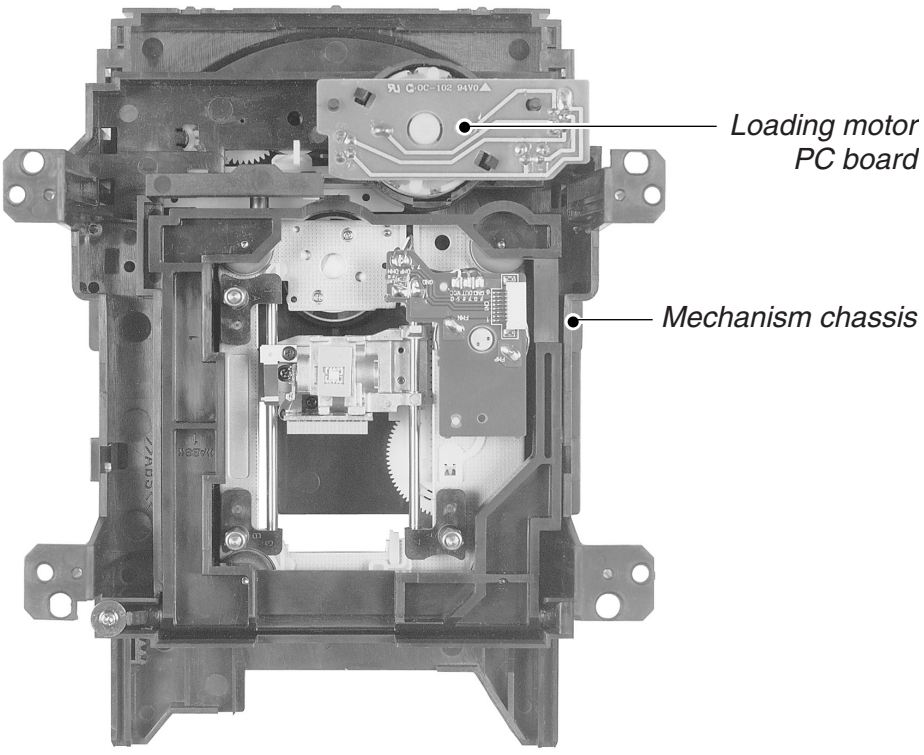


Fig. 1-2-3 Mechanism chassis assembly (Bottom side)

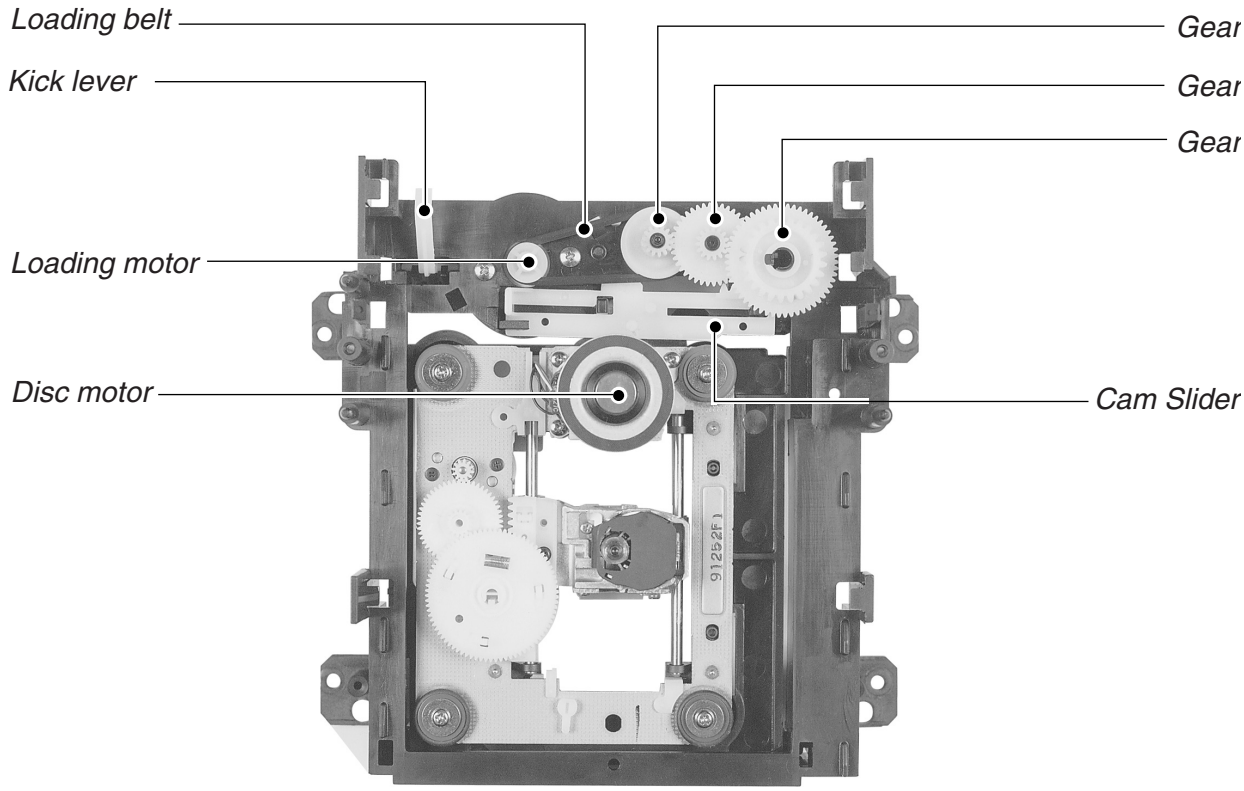


Fig. 1-2-4 Mechanism chassis assembly (Internal side)

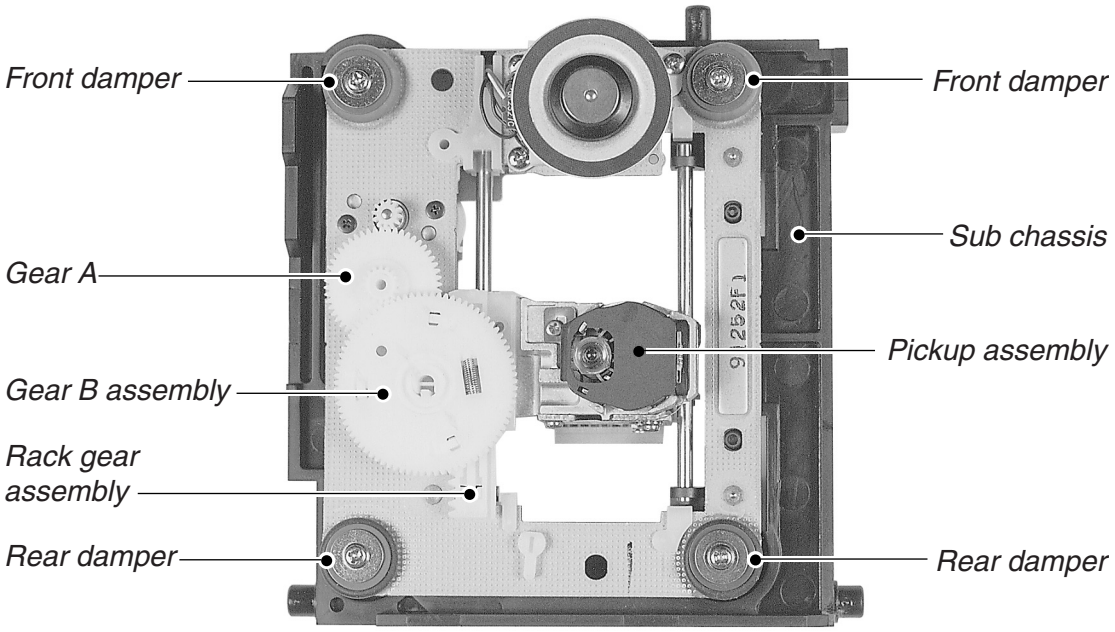


Fig. 1-2-5 Pickup mechanism chassis assembly (Top side)

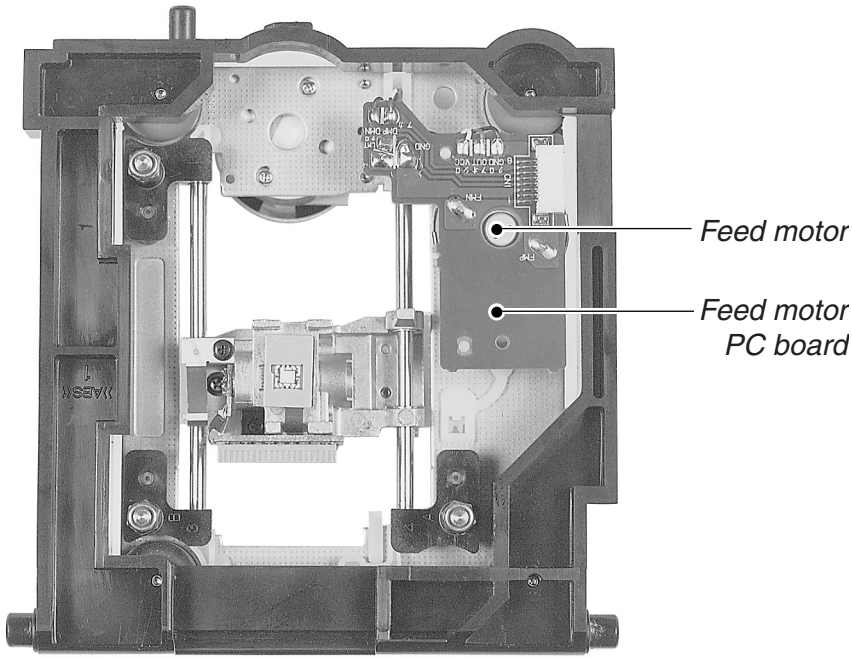


Fig. 1-2-6 Pickup mechanism chassis assembly (Bottom side)

3. TROUBLESHOOTING

3-1. Main Circuit

3-1-1. Servo System

(1) Initial Operation after Power ON

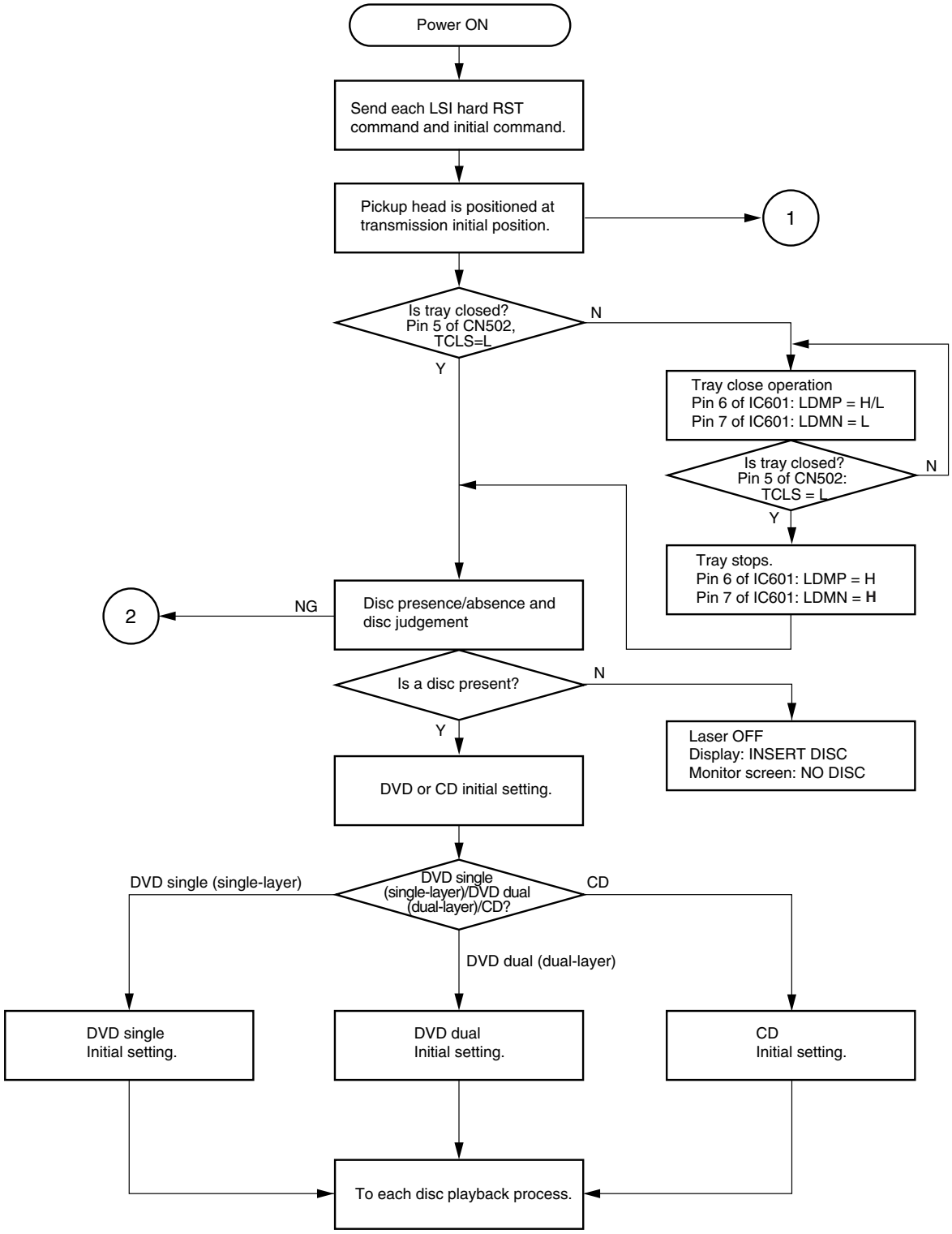


Fig. 1-3-1

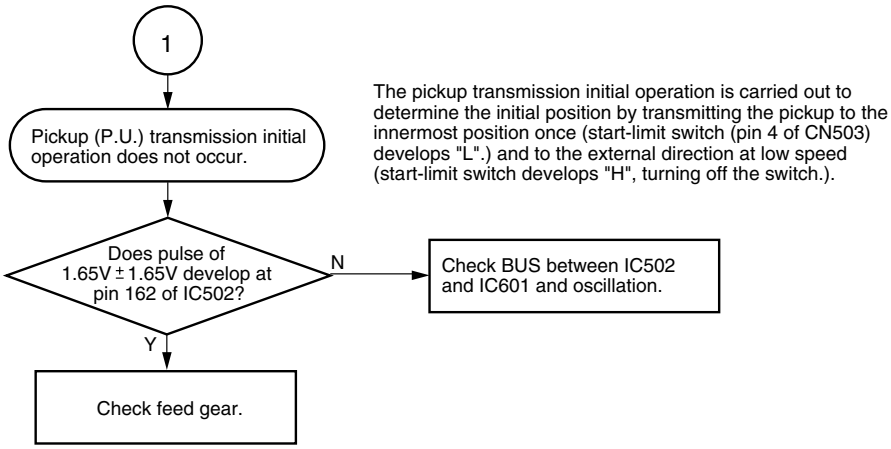


Fig. 1-3-2

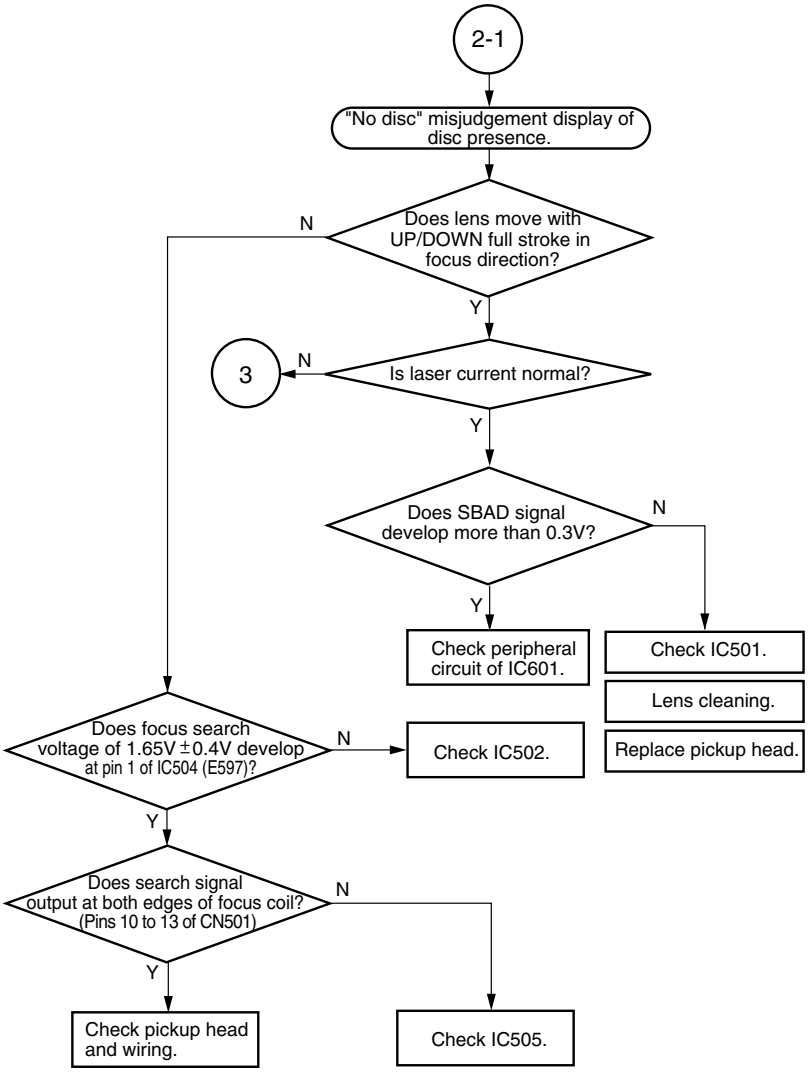


Fig. 1-3-3

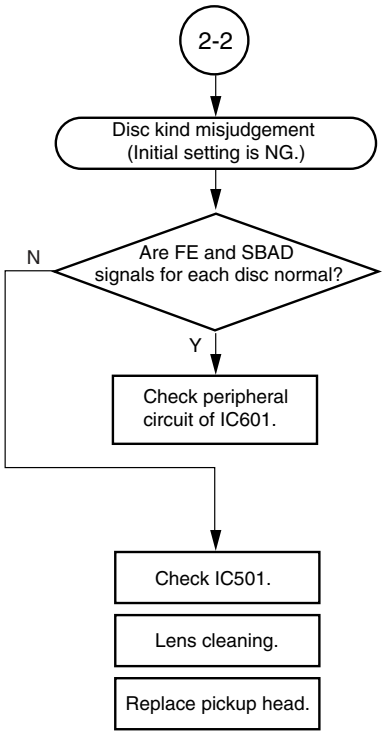


Fig. 1-3-4

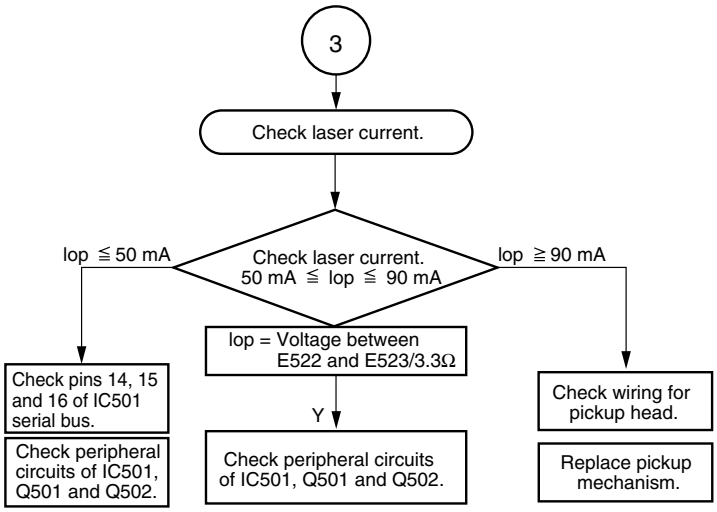


Fig. 1-3-5

DVD single (single-layer) disc detection waveform

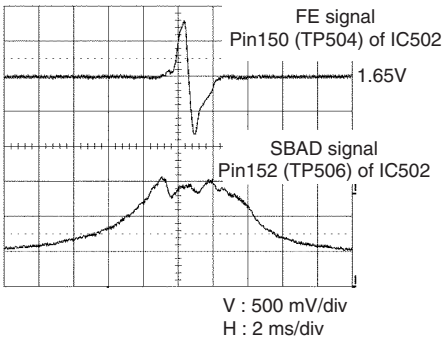


Fig. 1-3-6

DVD dual (dual-layer) disc detection waveform

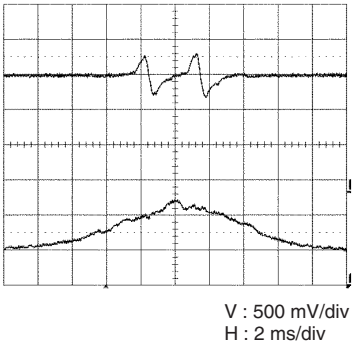


Fig. 1-3-7

CD disc detection waveform

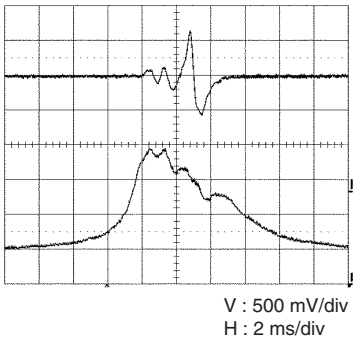


Fig. 1-3-8

(2) Picture appears (PLAY)

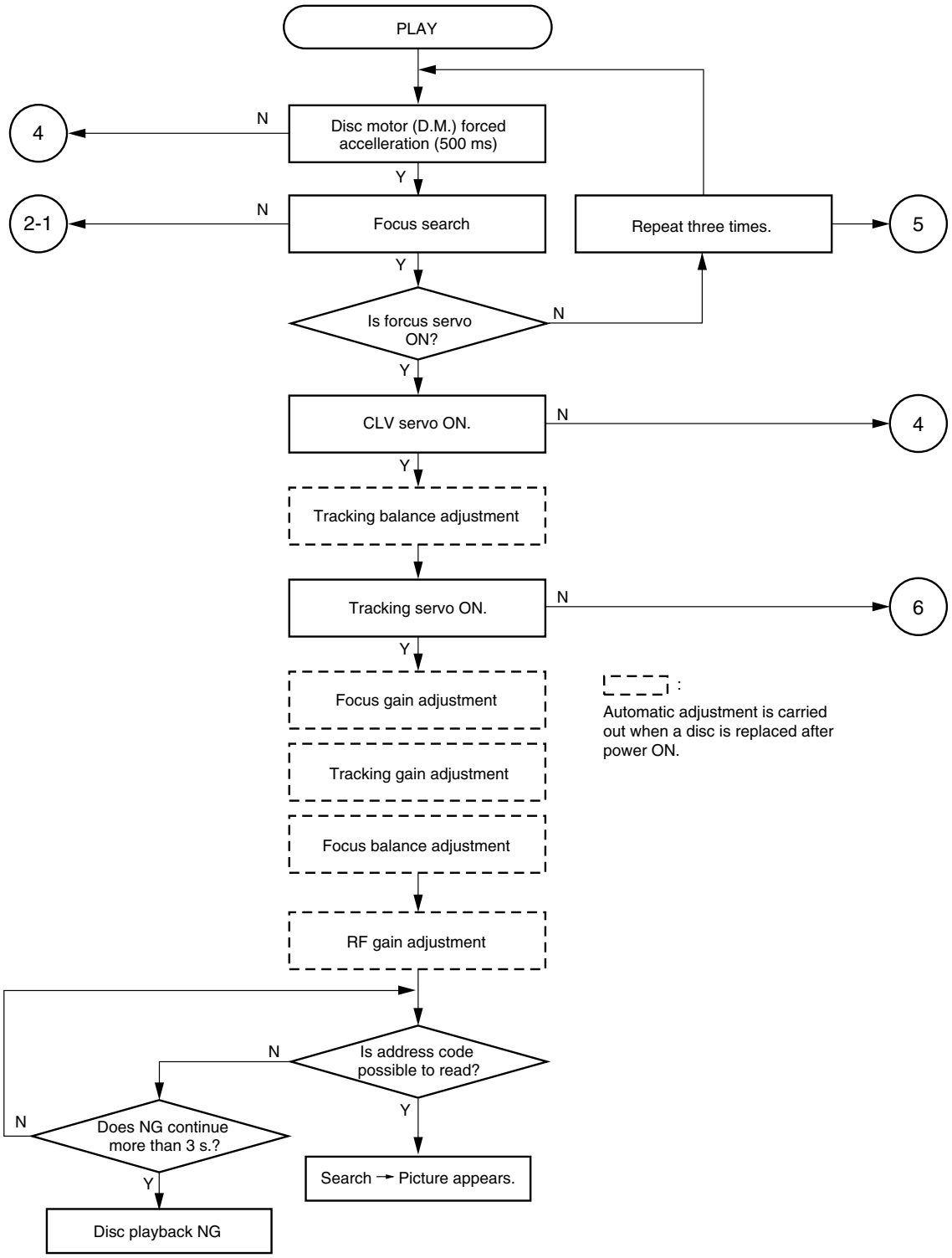


Fig. 1-3-9

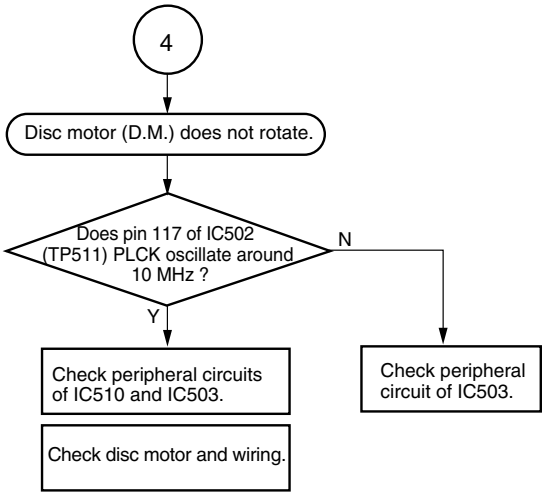


Fig. 1-3-10

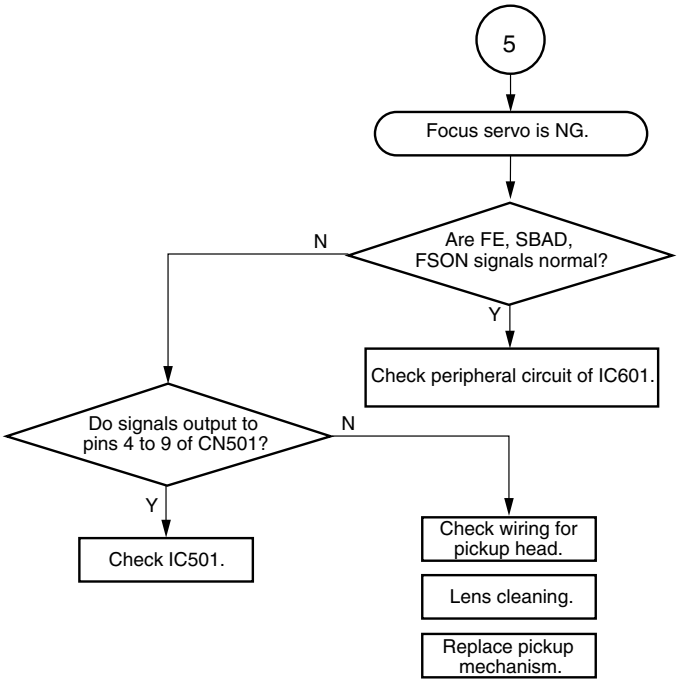


Fig. 1-3-11

Focus servo ON signal waveform

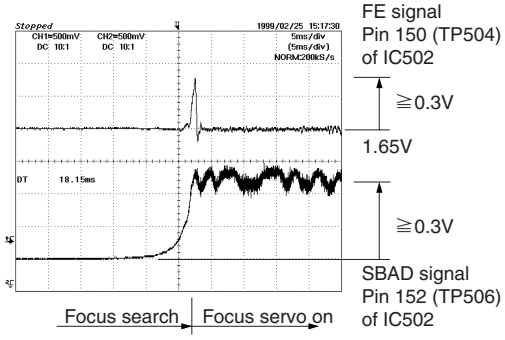


Fig. 1-3-12

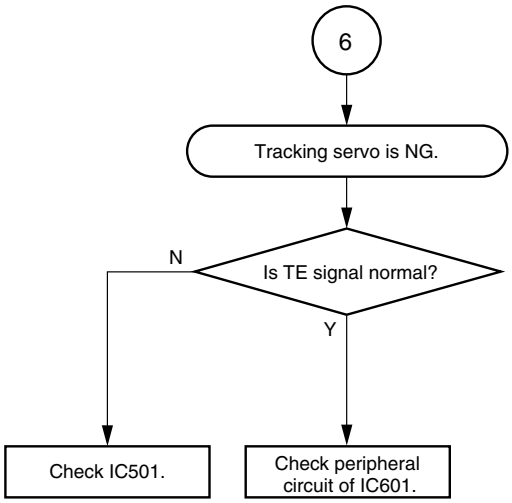
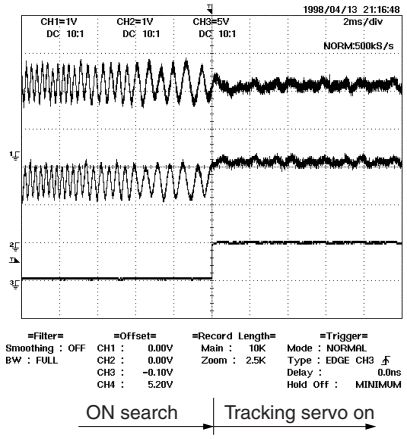


Fig. 1-3-13

Signal waveform at tracking servo ON (CD)



TE signal
Pin 151 (TP503) of IC502
1.65V

RFRP signal
Pin 153 (TP501) of IC502

Search ON (SRCH)
Pin 38 (TP508) of IC502

Fig. 1-3-14

Signal waveform at tracking servo ON (DVD)

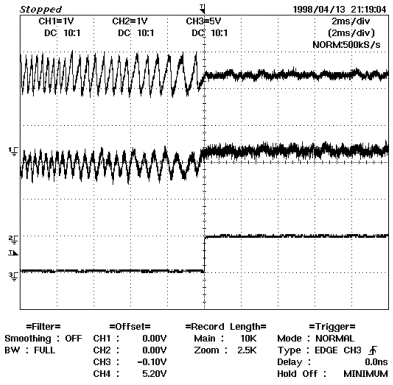


Fig. 1-3-15

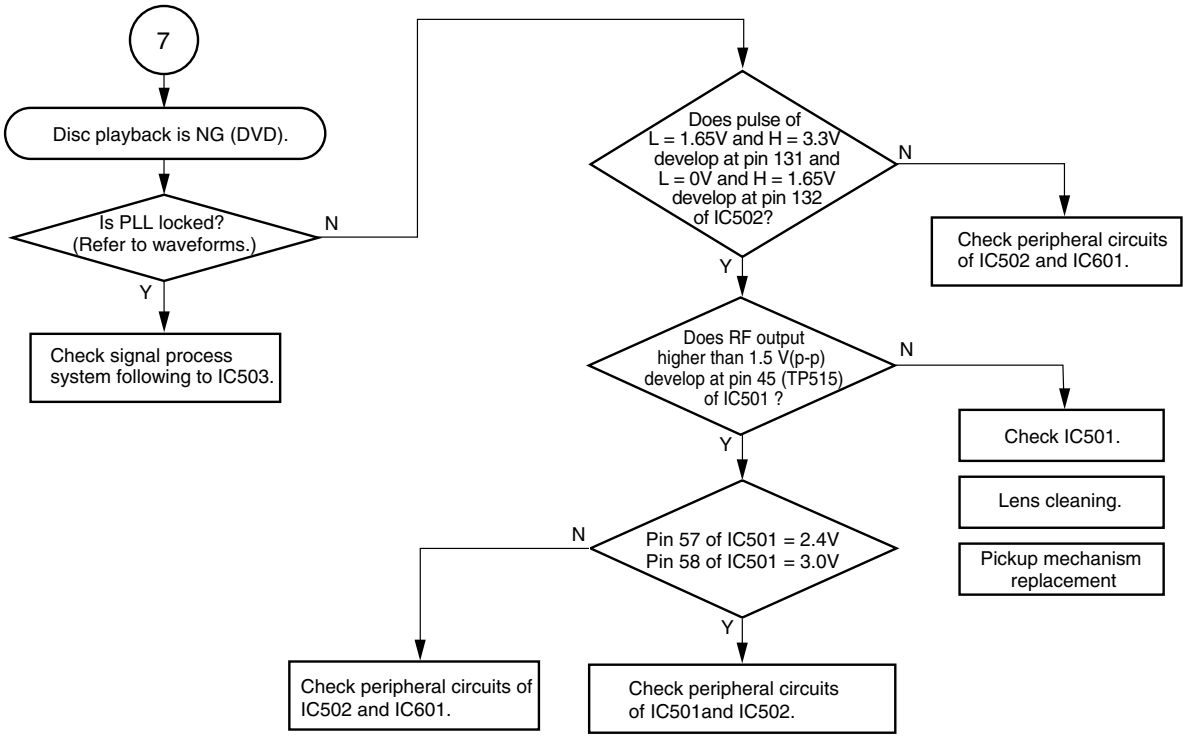
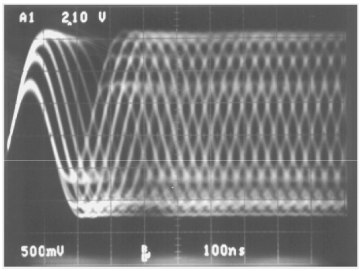


Fig. 1-3-16

PLL works as a servo loop to generate a clock signal for reading RF signal binary data. With the PLL locked, the eye pattern is identified clearly when triggered with the read clock PLCK.

DVD RF signal

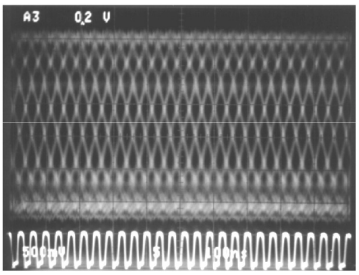


DVD RF signal
Pin 45 (TP515) of IC501

V : 500 mV/div
H : 50 ns/div

Fig. 1-3-17

DVD playback waveform



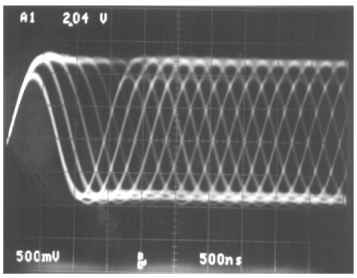
DVD RF signal
Pin 45 (TP515) of IC501

DVD PLCK
Pin 117 (TP511) of IC502

CH1 : TP515 DVDRF 500 mV/div
CH2 : TP511 DVDPLCK 5 V/div
50 ns/div

Fig. 1-3-19

CD RF signal

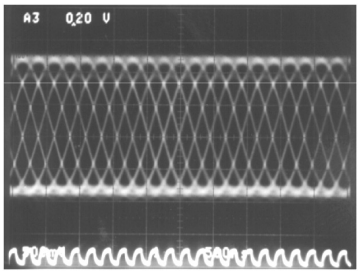


CD RF signal
Pin 45 (TP515) of IC501

V : 500 mV/div
H : 100 ns/div

Fig. 1-3-18

CD playback waveform



CD RF signal
Pin 45 (TP515) of IC501

CD PLCK
Pin 117 (TP511) of IC502

CH1 : TP515 CDRF 500 mV/div
CH2 : TP511 CDPLCK 5 V/div
100 ns/div

Fig. 1-3-20

3-1-2. Location Diagram of Servo Test Point

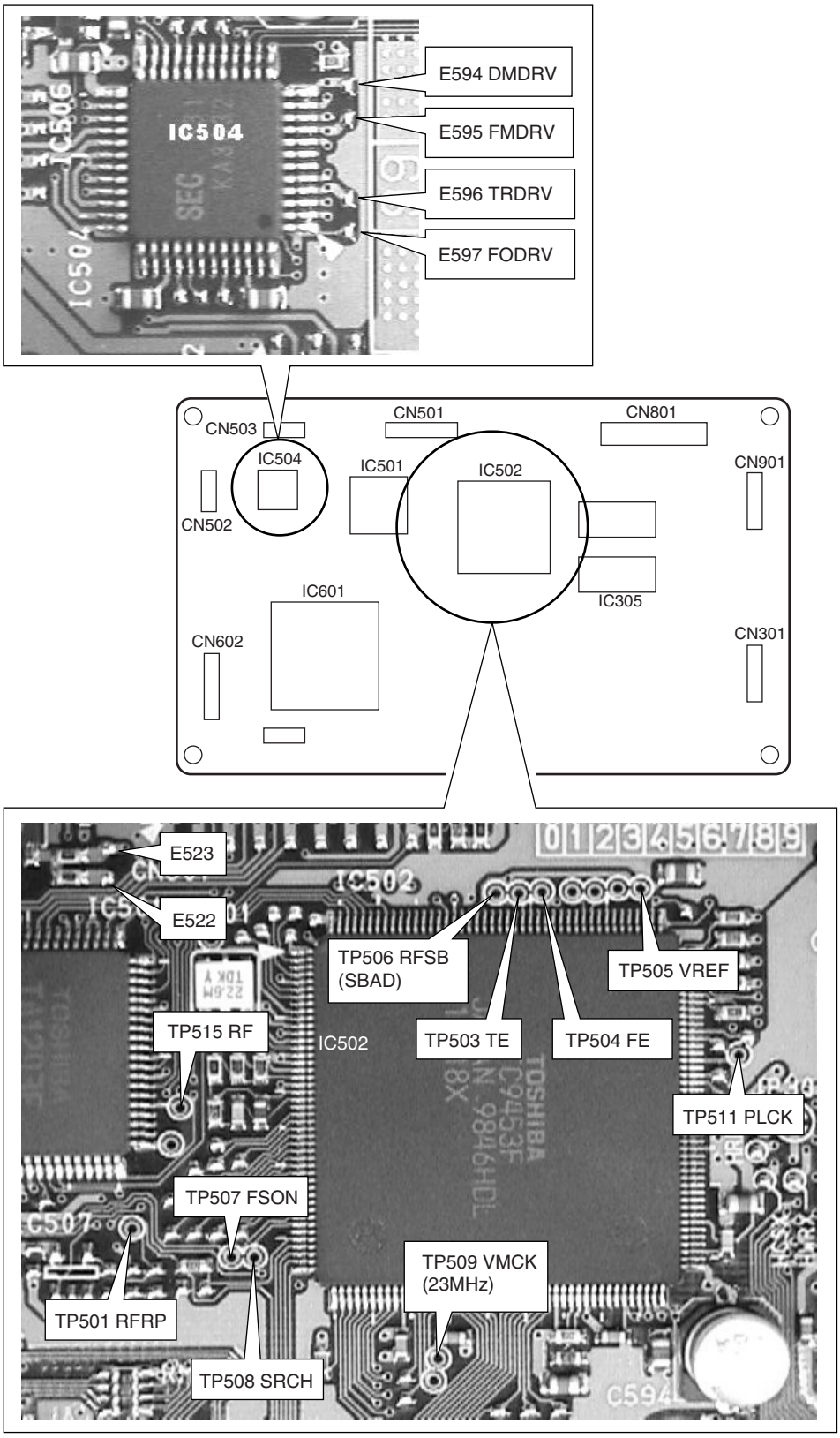


Fig. 1-3-21

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SECTION 2
PART REPLACEMENT AND ADJUSTMENT PROCEDURES

CAUTIONS BEFORE STARTING SERVICING

Electronic parts are susceptible to static electricity and may easily damaged, so do not forget to take a proper grounding treatment as required.

Many screws are used inside the unit. To prevent missing, dropping, etc. of the screws, always use a magnetized screwdriver in servicing. Several kinds of screws are used and some of them need special cautions. That is, take care of the tapping screws securing molded parts and fine pitch screws used to secure metal parts. If they are used improperly, the screw holes will be easily damaged and the parts can not be fixed.

1. REPLACEMENT OF MECHANICAL PARTS

1-1. Cabinet Replacement

1-1-1. Top Cover

1. Remove five screws (1) and remove the top cover (2).

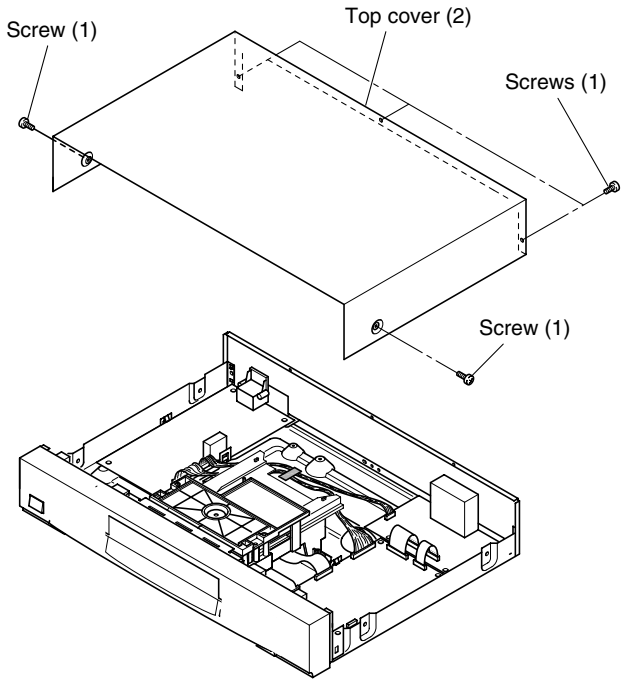

Fig. 2-1-1

1-1-2. Clamper Stay

<Removal>

1. Remove two screws (1).
2. Release two claws and remove the clamper stay (2).

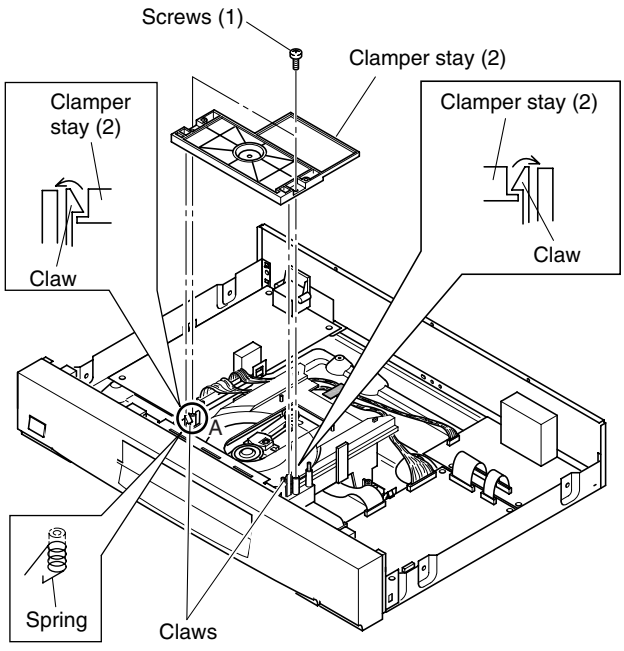

Fig. 2-1-2

<Mounting >

1. The spring for tray side pressure is inserted into the portion “A”. (Refer to Fig. 2-1-2.)
2. By referring to Fig. 2-1-3, insert the spring normally and mount the clamper stay.

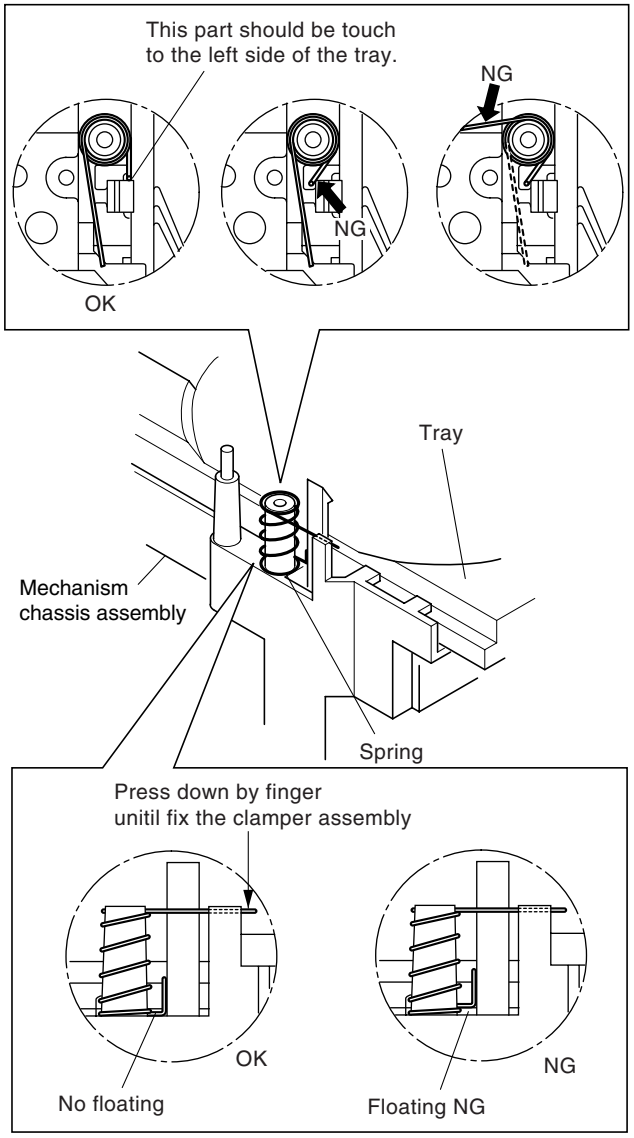

Fig. 2-1-3

1-1-3. Tray Panel

<Tray Ejection>

1. Slide the slider (2) of the mechanism chassis assembly (1) with a screwdriver, etc. in the arrow direction, so that the tray (3) is ejected.

Note:

- Take care not to damage the pickup and other parts.

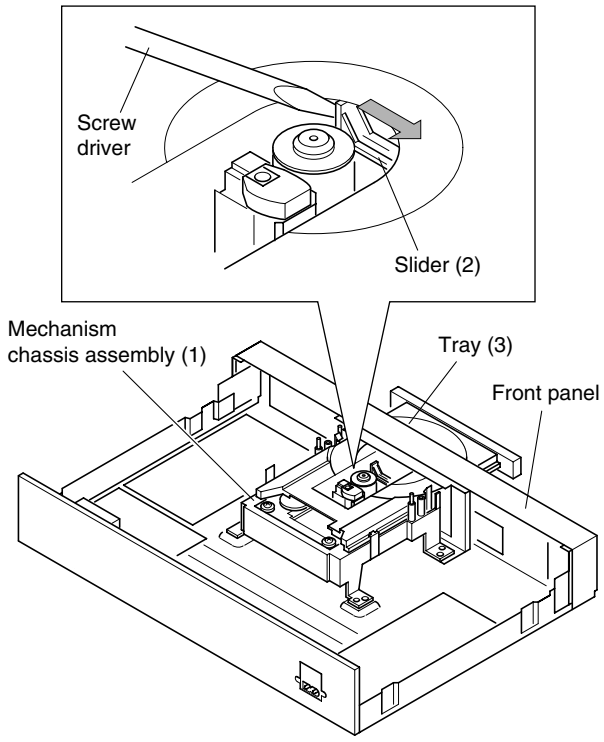

Fig. 2-1-4

<Tray Panel Removal>

1. Eject the tray (3).
2. Twist the tray panel (4) a little in the arrow A direction with the tray (3) hold by hand to release two claws and lift up the tray panel (4) in the arrow B direction, then the tray panel (4) is removed. (Refer to Fig. 2-1-5.)
3. When mounting the tray panel (4), insert the tray panel (4) along the grooves of the both sides of the tray (3) until clicking.

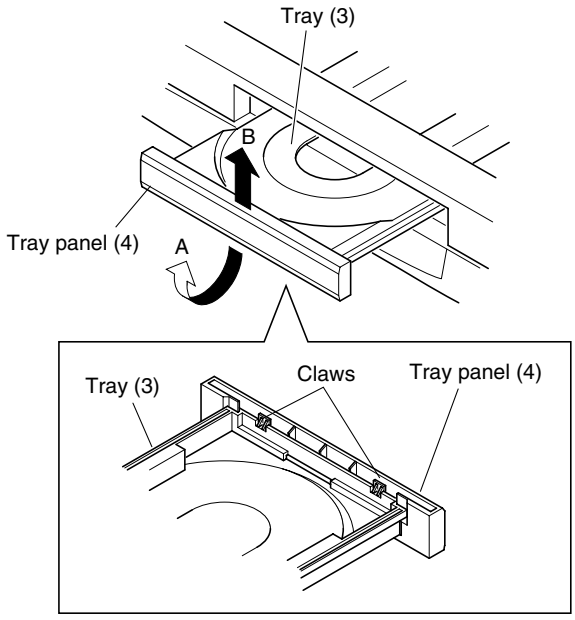

Fig. 2-1-5

1-1-4. Front Panel and Tray

1. Remove the flexible cable (1).
2. Release four claws and remove the front panel (2).
3. Pull out the tray (3) to this side.

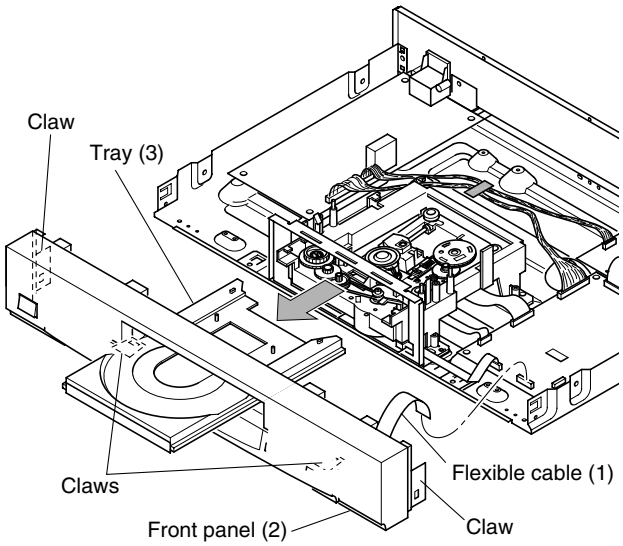

Fig. 2-1-6

Note:

- Insert the tray (3) with the front side of the pickup mechanism assembly descended. (The slider positions to the left side.)
- The gears are required to match their phases each other. After setting the gear (4) as shown in the figure "A", insert the tray (3). When inserting a tray (3), push the rack gear side shown by the arrow.
- After inserting the tray (3), confirm that the mark of the gear (4) matches with that of the rack gear on the tray (first tooth of the gear). (Refer to Fig. B.)

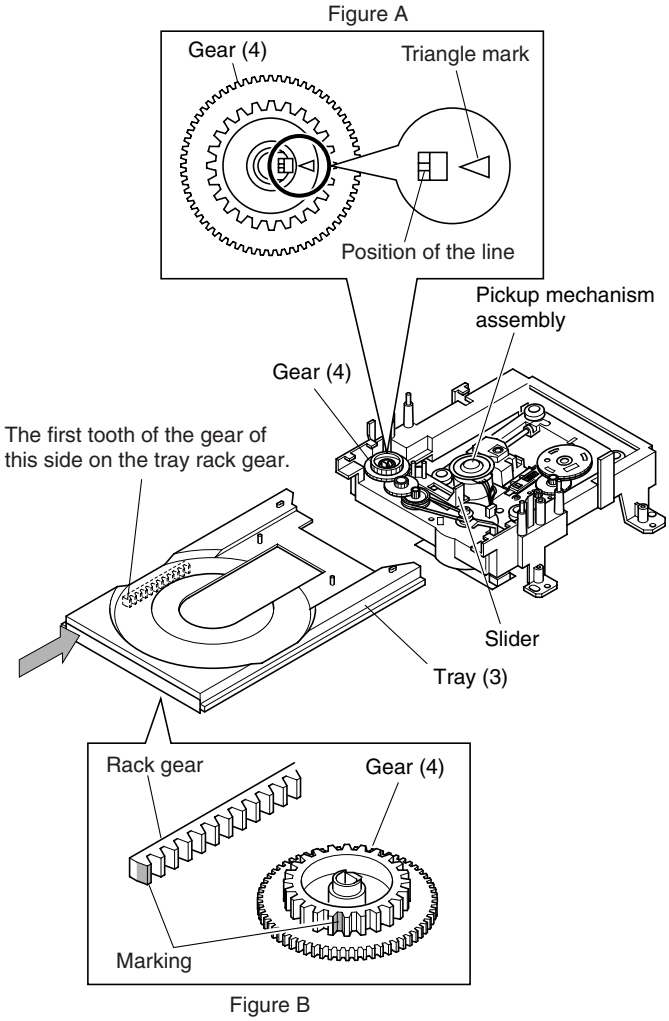

Fig. 2-1-7

1-1-5. Rear Panel

1. Remove three screws (1) and remove the rear panel (2).

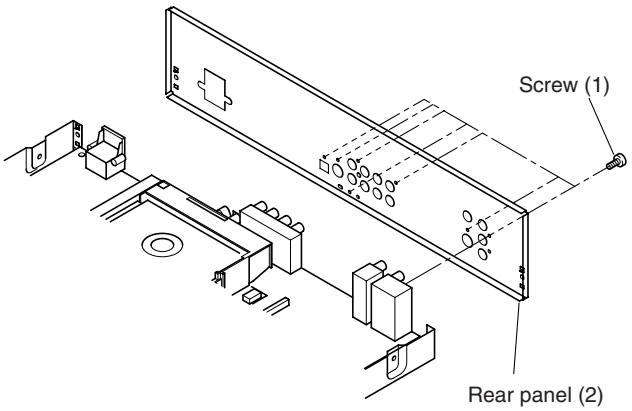

Fig. 2-1-8

1-2. PC Board Replacement

1-2-1. Main PC Board

Note:

- Before removing the main PC board (4), be sure to short-circuit the laser diode output land.

  After replacing, open the land as it was after inserting the flexible cables (1).

1. Remove the top cover. (Refer to item 1-1-1.)
2. Remove six flexible cables (1) and remove one connector (3).
3. Remove four screws (2).
4. Release two claws and remove the main PC board (4).

Note:

- When mounting, be sure to twist the wire for the connector (3) several times.

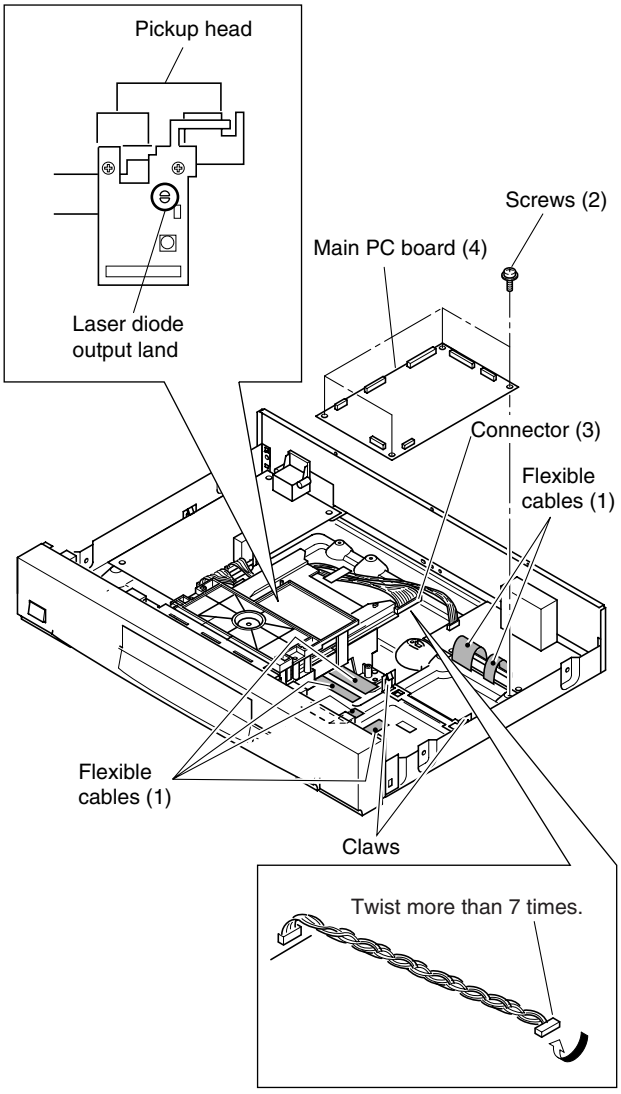

Fig. 2-1-9

1-2-2. Output PC Board

1. Remove the rear panel. (Refer to item 1-1-4
2. Peel off the tape (1).
3. Remove the connector (2).
4. Disconnect two flexible cables (3).
5 Remove the wire part of the connector (5) from the binding band (4).
6. Remove three screws (6) and remove the output PC board (7).

Note:

- When mounting, keep the wire part of the connector

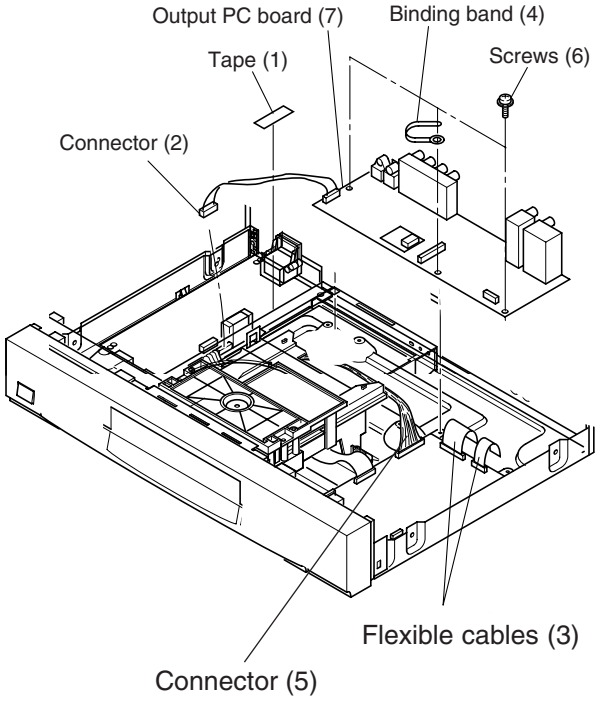

Fig. 2-1-10

1-2-3. Power PC board

1. Peel off the tape (1).
2. Remove the connectors (2) and (3).
3. Release the wire part of the connector with the binding band (4) tightened.
4. Remove three screws (5).
5. Remove two screws (6).
6. Release two claws and remove the power supply PC board (7).

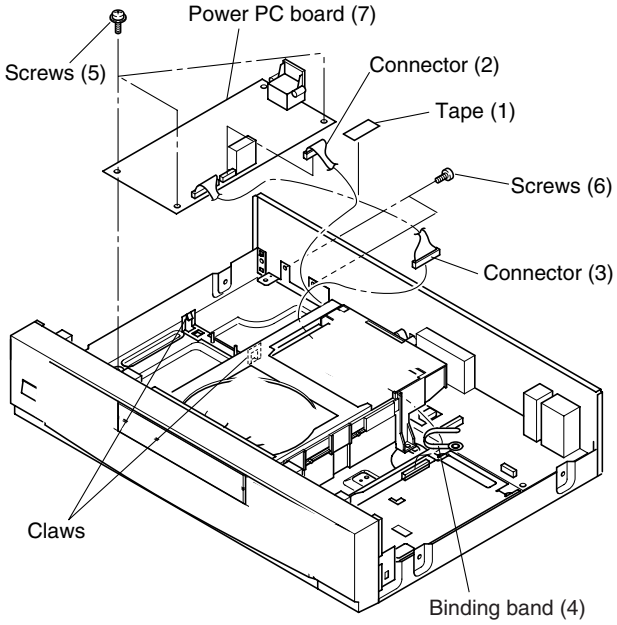

Fig. 2-1-11

1-2-4. Front PC Board

1. Remove the front panel. (Refer to item 1-1-4.)
2. Remove four screws (1) and remove the front display PC board (2)
3. Remove two screws (3) and remove the power switch PC board (4).

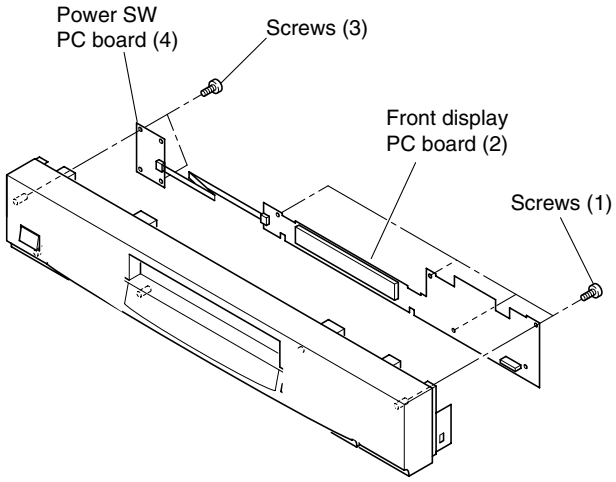

Fig. 2-1-12

1-3. Mechanism Parts

1-3-1. Mechanism Chassis Assembly

Note:

- When removing the mechanism chassis assembly (3), be sure to short-circuit the laser diode output land before removing the connector and the flexible cables.

  After replacing, open the land as it was after inserting the connector and flexible cables.

1. Remove the tray. (Refer to items 1-1-3 and 1-1-4.)
2. Remove three flexible cables (1).
3. Remove four screws (2) and remove the mechanism chassis assembly (3).

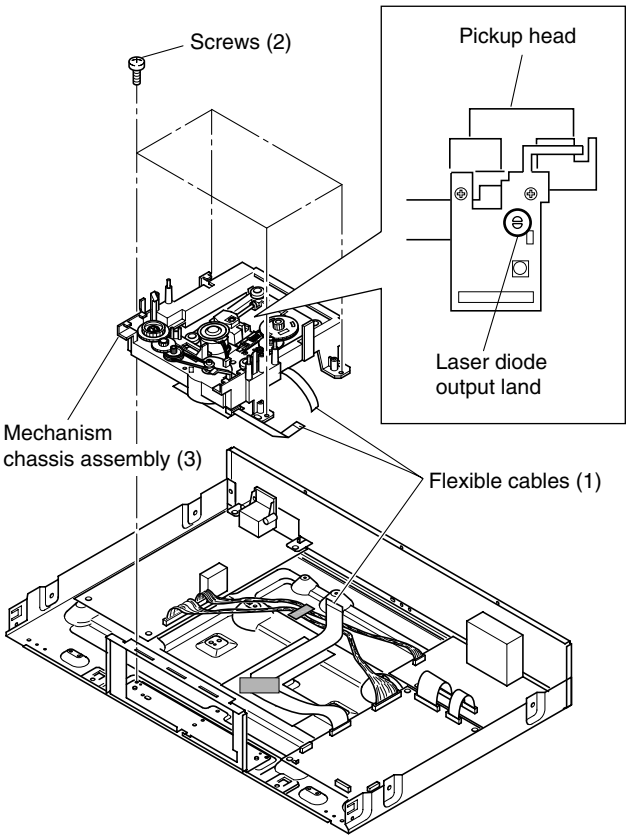

Fig. 2-1-13

1-3-2. Loading Belt

1. Remove the gear (1) by releasing the claw.
2. Remove the gear (2).
3. Remove the gear (3) and the loading belt (4).
4. Replace the loading belt (4) with a new one.
5. When mounting, perform the reverse order of the removal.

Note:

- When mounting the loading belt (4), twisting and attaching of a grease, etc. are not allowed.

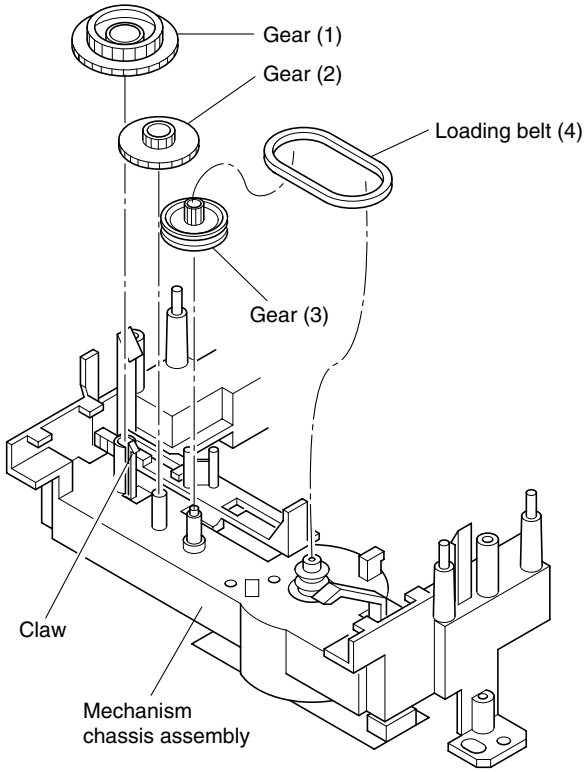

Fig. 2-1-14

1-3-3. Loading Motor

1. Remove the loading belt. (Refer to item 1-3-2.)
2. Remove two screws (1) and two claws. Then remove the loading motor (2) (with the loading motor PC board (3) attached).
3. Desolder the terminal section of the loading motor (2) and remove the loading motor PC board (3).
4. Replace the loading motor (2) with a new one.
5. When mounting, perform the reverse order of the removal.

Note:

- When replacing the loading motor, meet the polarity phase of the terminals. (Mount the motor with the label positioned as shown in Fig. 2-1-15.)

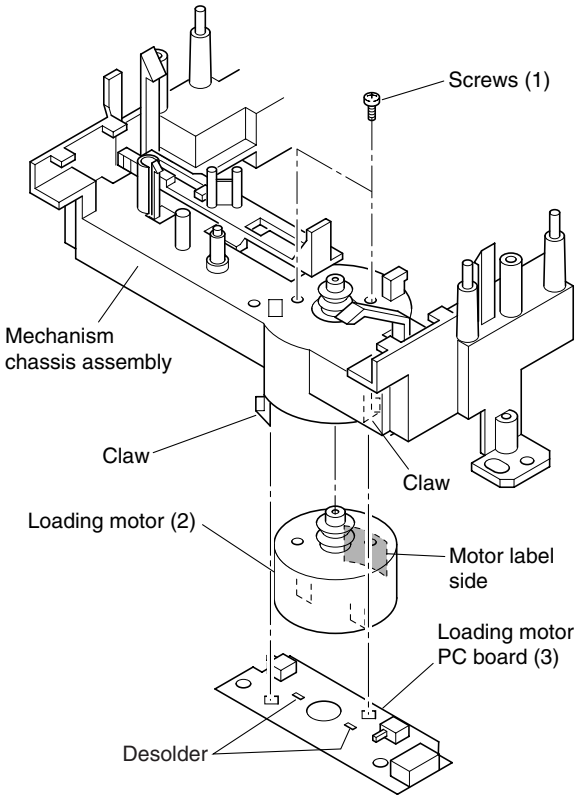

Fig. 2-1-15

1-3-4. Sub Chassis (with a pickup mechanism)

1. Turn the mechanism chassis assembly (1) upside down.
2. Remove one screw (2) and release the boss "A" from the claw. Then remove the sub chassis (3) (with the pickup mechanism) by sliding in the arrow direction.
3. When mounting, perform the reverse order of the removal.

Note:

- When mounting the sub chassis (3) (with the pickup mechanism), first, insert the boss "C" along the groove of the cam slider up/down cam (4) and next, the boss "B" and "A".
- The boss "A" and "B" may be used with washers. (One or two washers are used to prevent from the slust rattling. In some cases, no washer is used.)

  When the washer(s) is used, be sure to assemble as it was without losing.

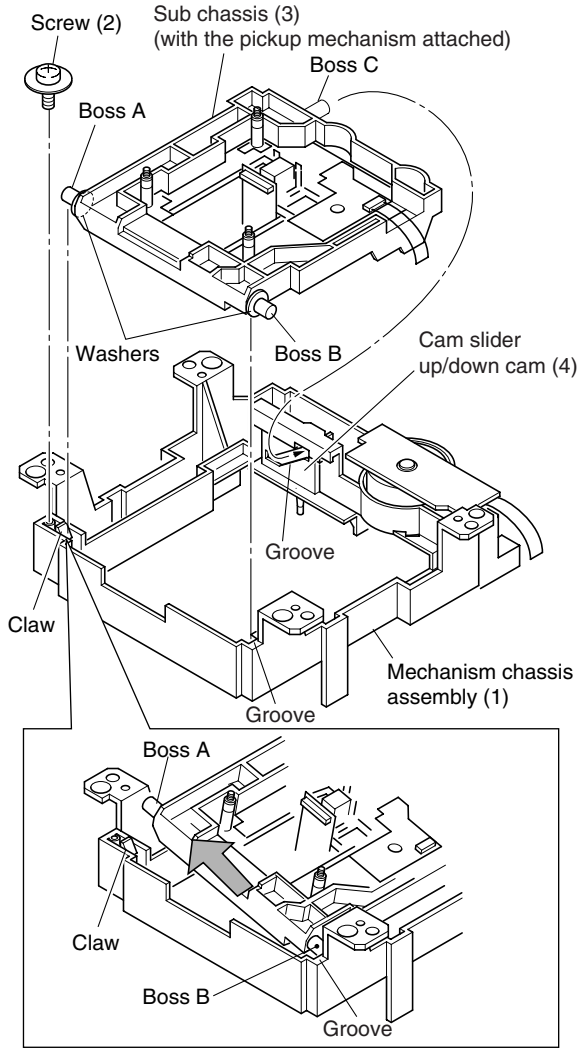

Fig. 2-1-16

1-3-5. Pickup Mechanism Assembly

<Removal>

1. Remove four screws (1) and four washers (2) and then remove the pickup mechanism assembly (3).

<Mounting>

1. Replace the pickup mechanism assembly (3) with a new one.
2. When mounting, perform the reverse order of the removal.

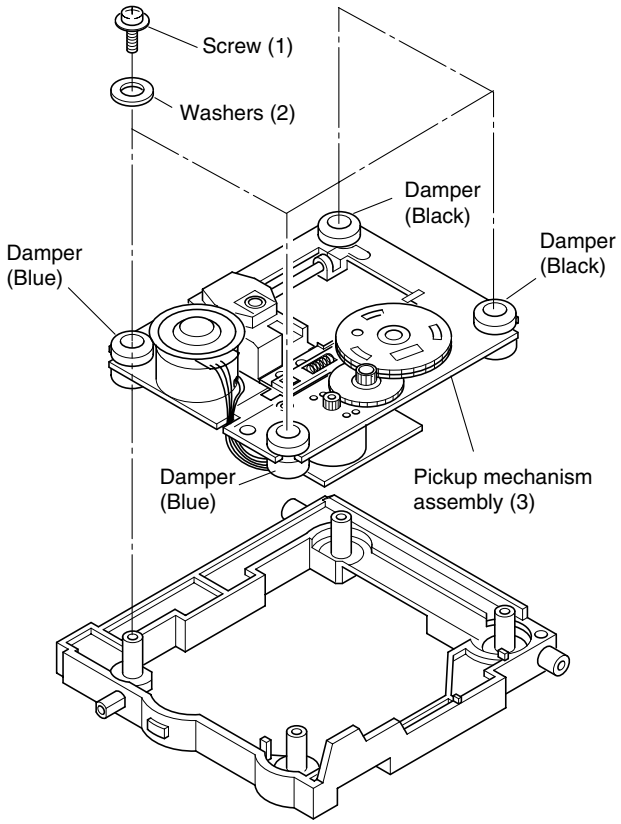

Fig. 2-1-17

Note:

- The dampers' color differs when used for the front side and the rear.
- When mounting the pickup mechanism assembly (2) with the screws (1), push the pickup mechanism assembly (2) downward without being caught and tighten the screws (1) after placing the washer with the damper bent.

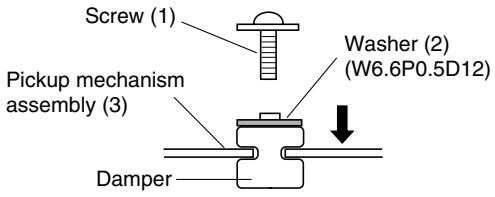

Fig. 2-1-18

1-3-6. Gear B Assembly, Gear A and Rack Gear Assembly

<Removal>

1. Remove one screw (5) and remove the gear B assembly (1).
2. Remove the gear A (2).
3. Remove one screw (3) and remove the rack gear assembly (4).

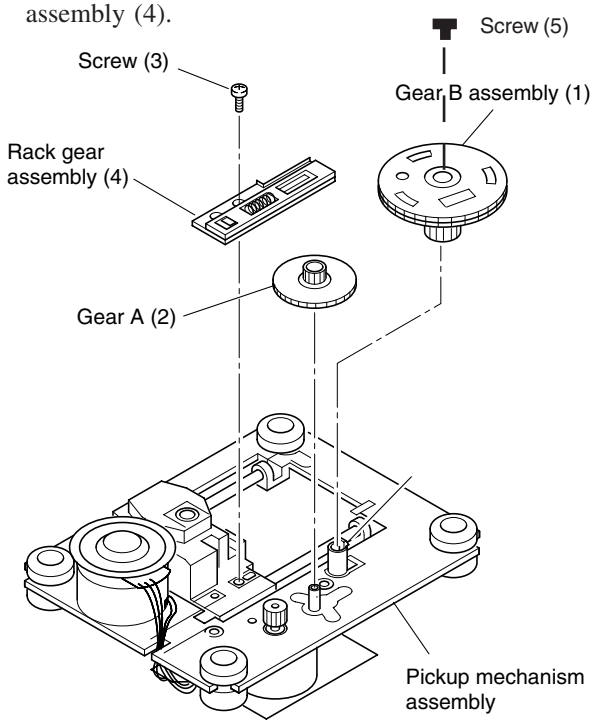

Fig. 2-1-19

<Mounting>

1. When mounting, perform the reverse order of the removal.
2. Mount the gear B assembly (1) by pushing the pickup head (5) to the disc motor side (arrow A direction) and shifting the upper gear of the rack gear assembly (4) in the arrow B direction. (Refer to Fig. 2-1-20.)
3. Fit the positioning holes on the upper gear and lower gear of the gear B assembly (1) and mount on the pickup mechanism assembly with the phase matched.

   At this time, note that the phase of the gear B assembly (1) and the gear A (2) shows the status in the Fig. 2-1-21.

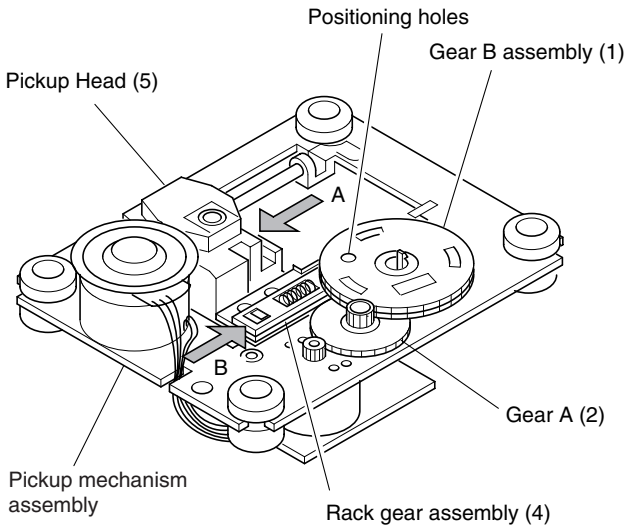

Fig. 2-1-20

Note:

- Mount the gear B assembly (1) and the gear A (2) with their gear teeth placed more than one tooth at least inside the shaded portion.

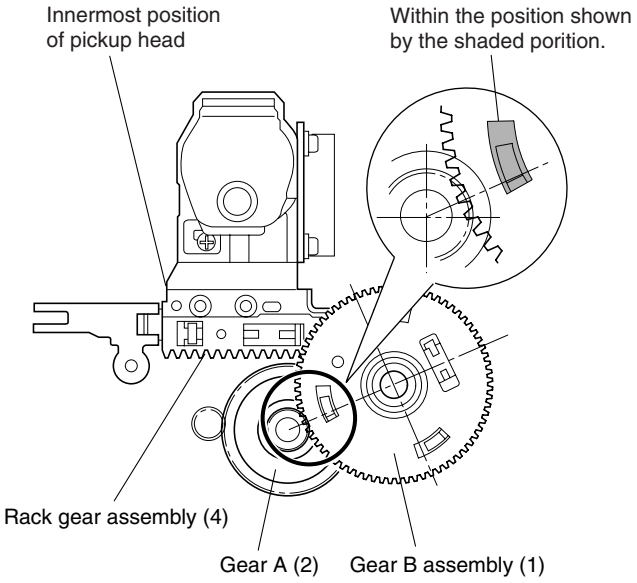

Fig. 2-1-21

1-3-7. Feed Motor

<Removal>

1. Remove the gear B assembly (1) and the gear A (2). (Refer to item 1-3-6.)
2. Remove two screws (1) and remove the feed motor (2) (with the feed motor PC board (3) attached). (Refer to Fig. 2-1-22.)
3. Desolder the terminals of the feed motor (2) and remove the feed motor PC board (3).

<Mounting>

1. Tighten the feed motor (2) on the pickup mechanism assembly with two screws (1).
2. Insert the feed motor PC board (3) with the positioning pin on the chassis matched and solder the terminals.
3. Perform the reverse order of the removal.

Note:

- After mounting, put the lead wires through the notch of the pickup mechanism assembly.
- When replacing the loading motor, meet the polarity phase of the terminals. (Mount the motor with the label positioned as shown in Fig. 2-1-22.)

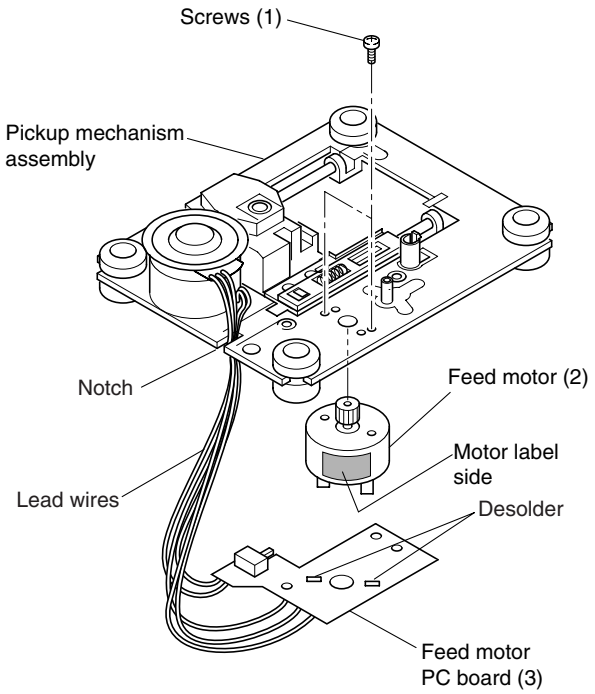

Fig. 2-1-22

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SECTION 3
SERVICING DIAGRAMS

1. CIRCUIT SYMBOLS AND SUPPLEMENTARY EXPLANATION

1-1. Precautions for Part Replacement

- In the schematic diagram, parts marked ⚠ (ex. ⚠ F801) are critical part to meet the safety regulations, so always use the parts bearing specified part codes (SN) when replacing them.
- Using the parts other than those specified shall violate the regulations, and may cause troubles such as operation failures, fire etc.

1-2. Solid Resistor Indication

Unit	None .....Ω K .....kΩ M .....MΩ
Tolerance	None .....±5% B .....±0.1% C .....±0.25% D .....±0.5% F .....±1% G .....±2% K .....±10% M .....±20%
Rated Wattage	(1) Chip Parts None .....1/16W (2) Other Parts None .....1/6W Other than above, described in the Circuit Diagram.
Type	None .....Carbon film S .....Solid R .....Oxide metal film W .....Metal film W .....Cement FR .....Fusible

Eg. 1

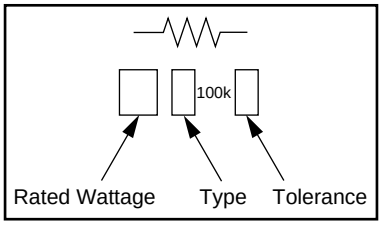


Fig. 3-1-1

1-3. Capacitance Indication

Symbol	.....Electrolytic, Special electrolytic .....Non polarity electrolytic .....Ceramic, plastic .....Film .....Trimmer
Unit	None .....F μ .....μF p .....pF
Rated voltage	None .....50V For other than 50V and electrolytic capacitors, described in the Circuit Diagram.
Tolerance	(1) Ceramic, plastic, and film capacitors of which capacitance are more than 10 pF. None .....±5% or more B .....±0.1% C .....±0.25% D .....±0.5% F .....±1% G .....±2% (2) Ceramic, plastic, and film capacitors of which capacitance are 10 pF or less. None .....more than ±5% pF B .....±0.1 pF C .....±0.25 pF (3) Electrolytic, Trimmer Tolerance is not described.
Temperature characteristic (Ceramic capacitor)	None .....SL For others, temperature characteristics are described. (For capacitors of 0.01 μF and no indications are described as F.)
Static electricity capacity (Ceramic capacitor)	Sometimes described with abbreviated letters as shown in Eg. 3.

Eg. 2

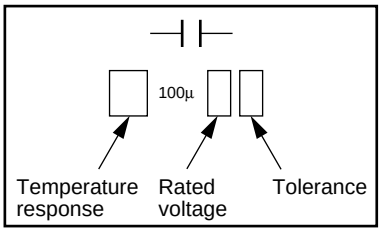


Fig. 3-1-2

Eg. 3

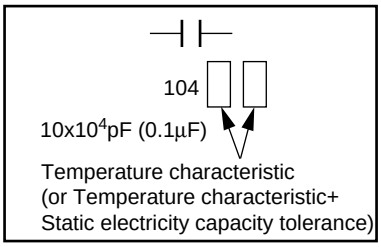


Fig. 3-1-3

1-4. Inductor Indication

Unit	None	.....H
	μ	.....μH
	m	.....mH
Tolerance	None	.....±5%
	B	.....±0.1%
	C	.....±0.25%
	D	.....±0.5%
	F	.....±1%
	G	.....±2%
	K	.....±10%
	M	.....±20%

Eg. 4

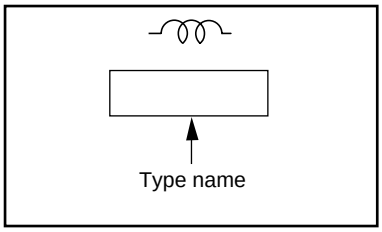


Fig. 3-1-4

Eg. 5

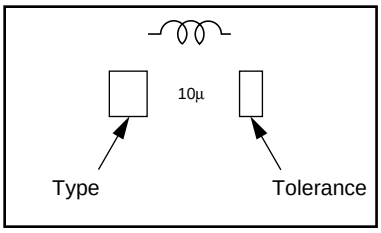


Fig. 3-1-5

1-5. Waveform and Voltage Measurement

- The waveforms for CD/DVD and RF shown in the circuit diagrams are obtained when a test disc is played back.
- All voltage values except the waveforms are expressed in DC and measured by a digital voltmeter.

1-6. Others

- The parts marked with “NC” or “KETU” in the circuit diagrams are not used for this model.

1-7. When Replaced ROM ICs or Upgraded Firmware

1. When replaced the following ROM ICs, it is necessary to write the data into the new ICs.
   1) IC615 (firmware)
   2) IC613 (Setup default data and other information)
2. When the firmware is upgraded, rewriting the new firmware into IC615 may be requested for servicing.
3. Connect a computer to the main PC board of the DVD video player with using DATA UPDATE KIT (P/No. 79080074). (Fig. 3-2-6)
4. Writing operation

   Refer to the instruction attached to the data floppy disc.

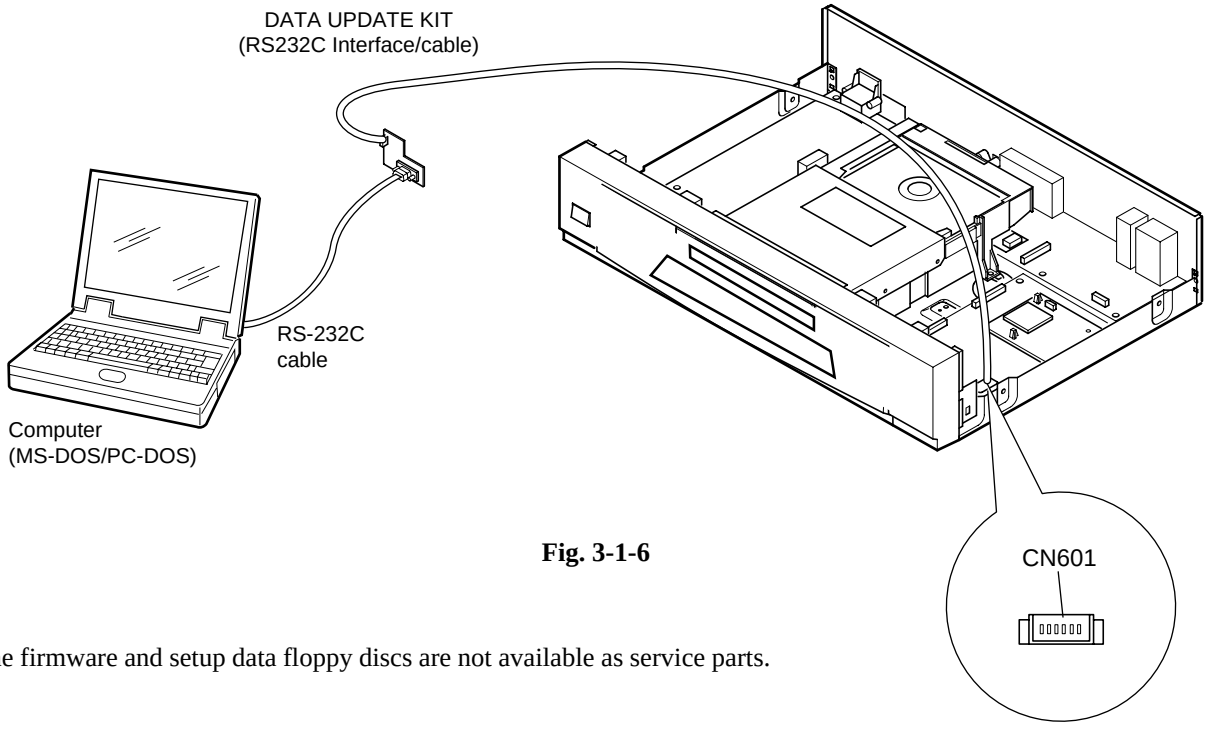


Fig. 3-1-6

Note:

- The firmware and setup data floppy discs are not available as service parts.

2. PRINTED WIRING BOARD AND SCHEMATIC DIAGRAM

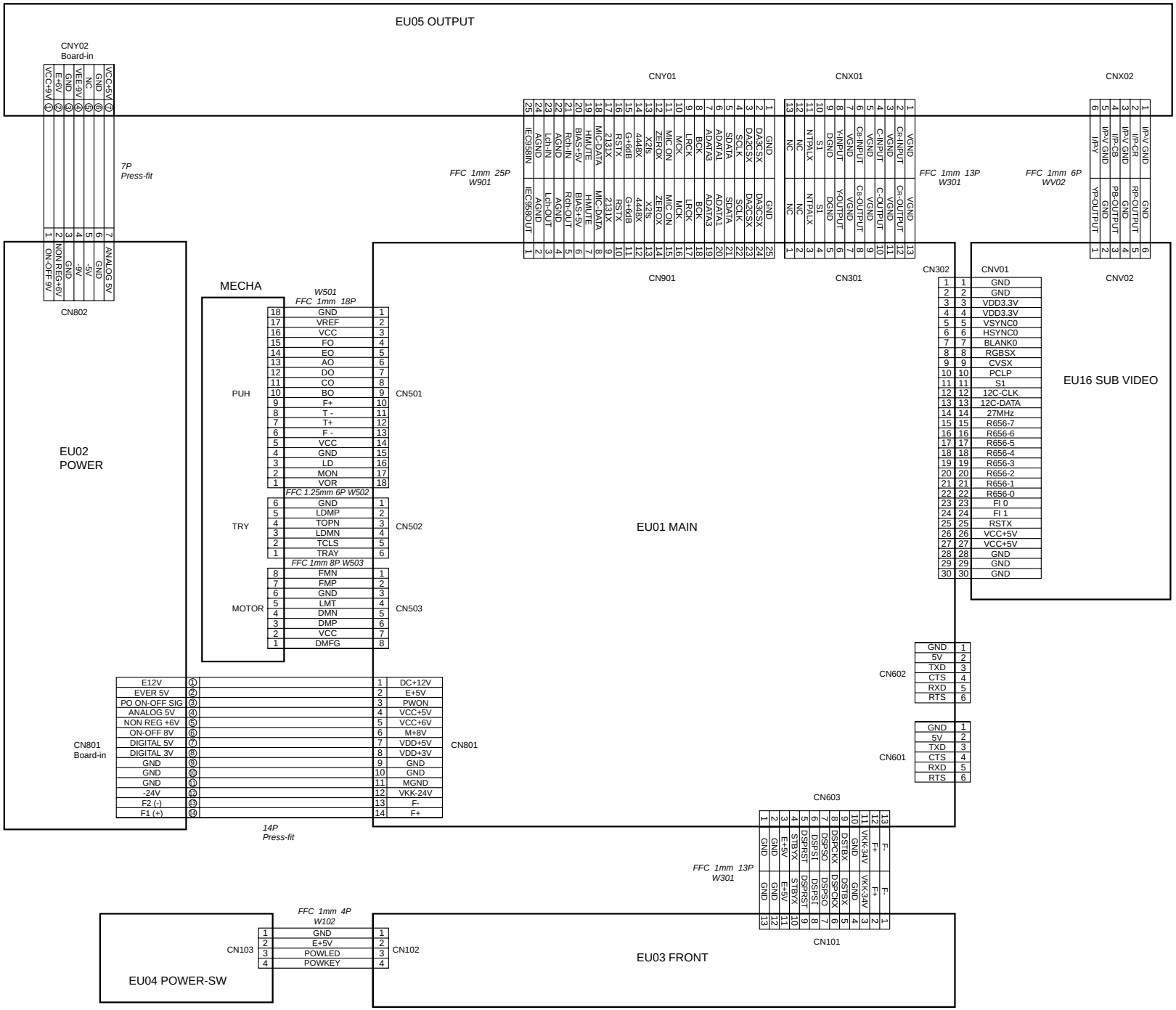


Fig. 3-2-1

3. BLOCK DIAGRAMS

3-1. Overall Block Diagram

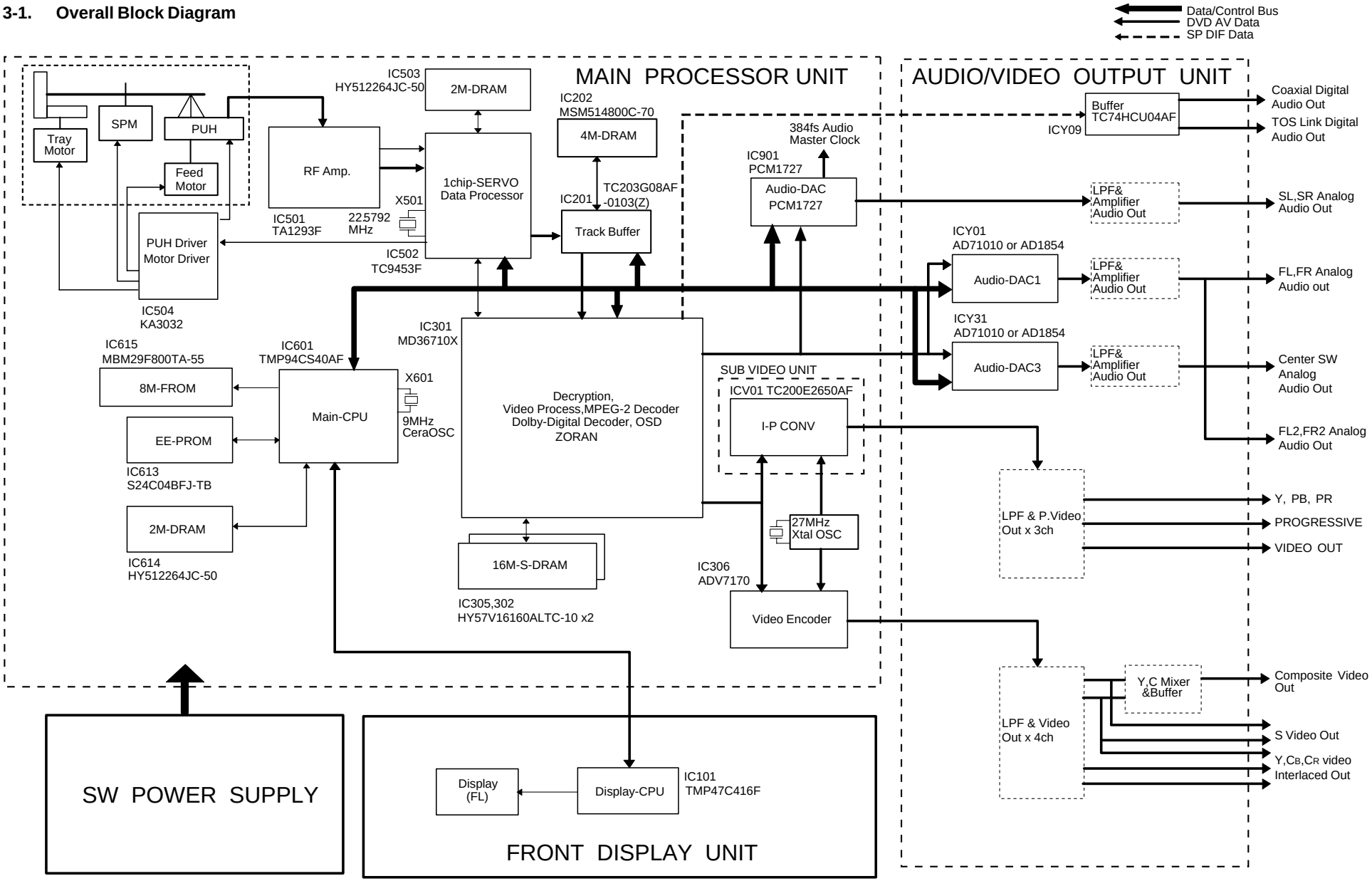


Fig.3-3-1

3-2. Main Block Diagrams

3-2-1. Logical System Block Diagram

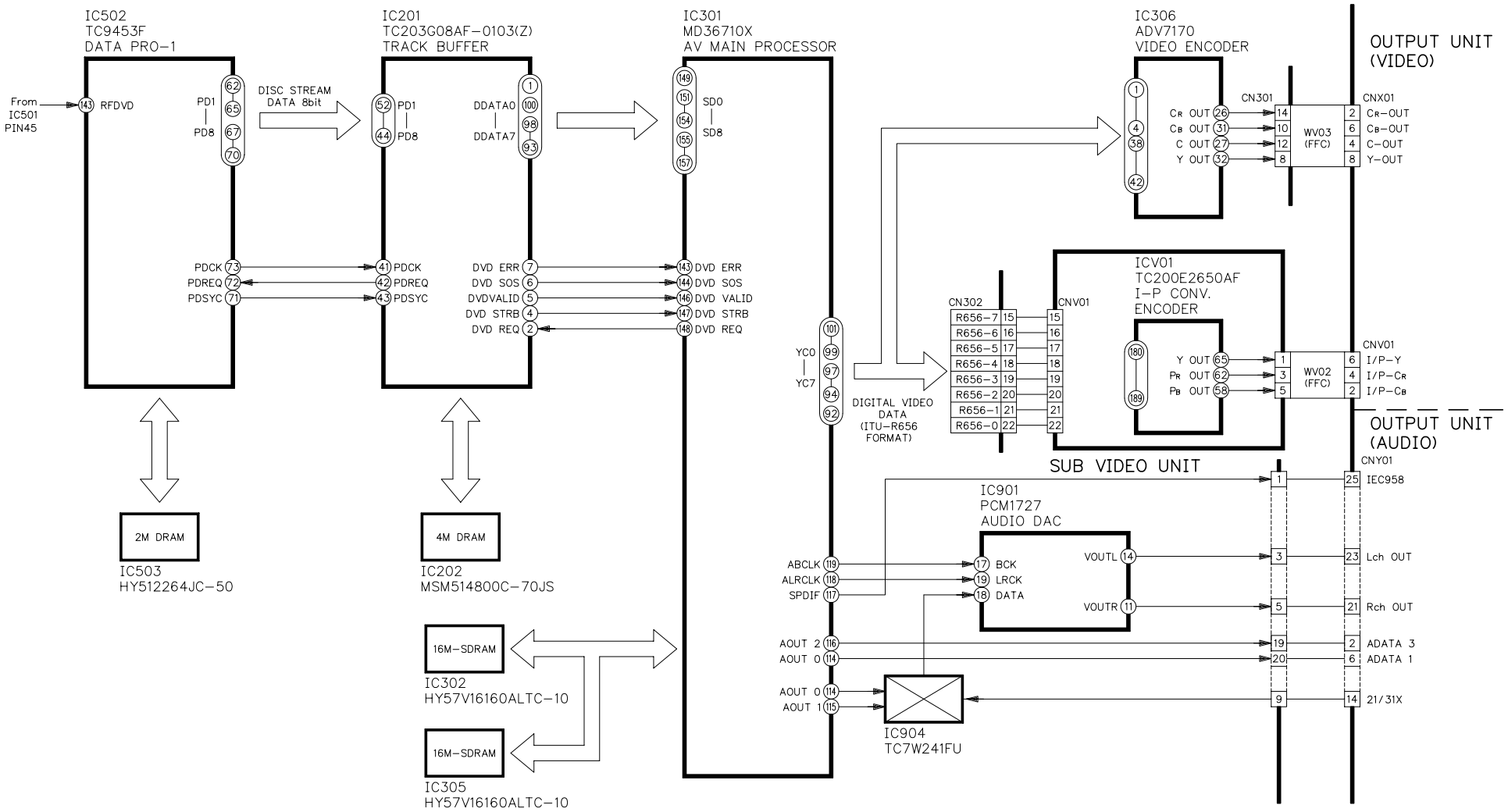


Fig. 3-3-2

3-3. Output Block Diagram

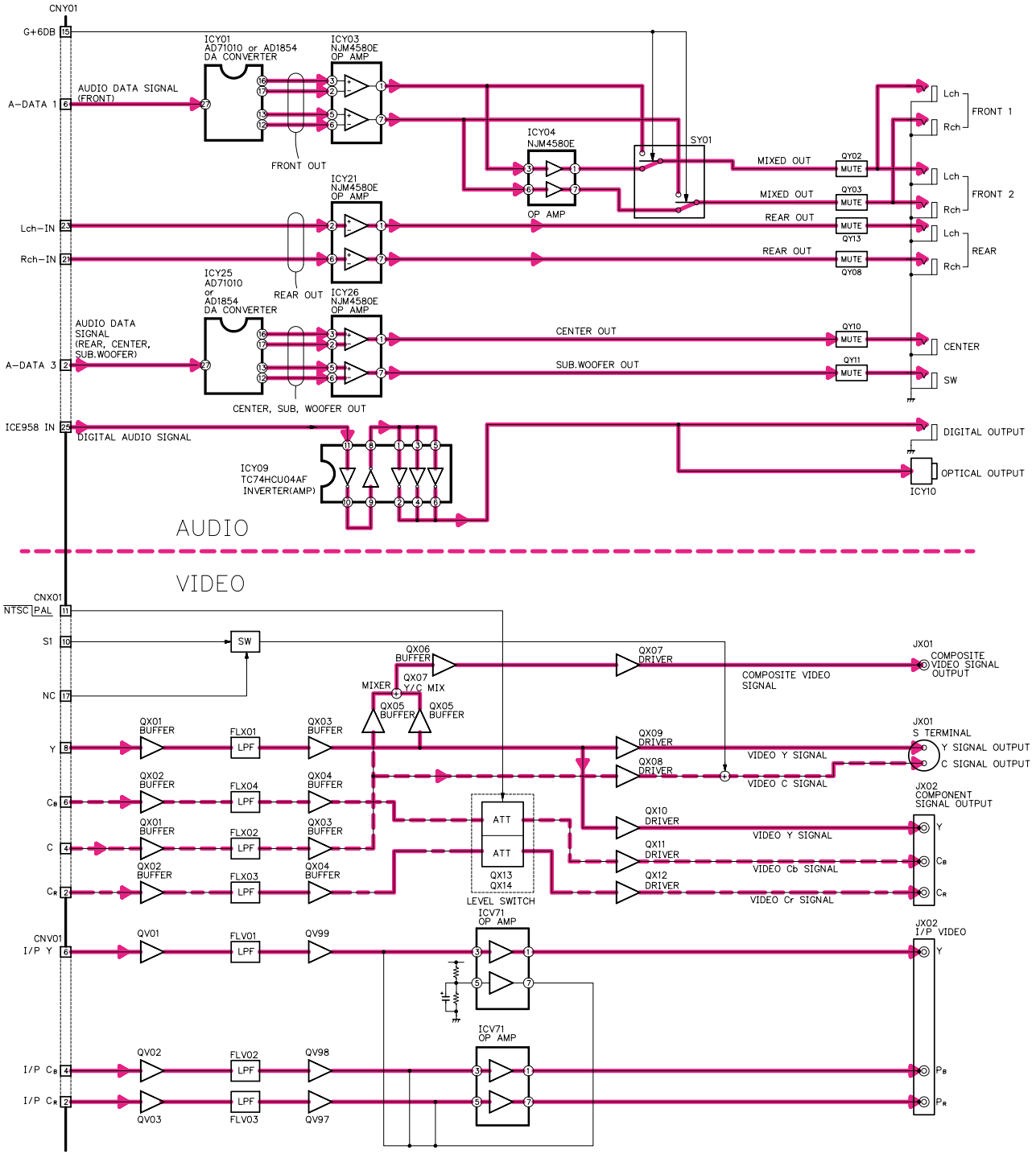
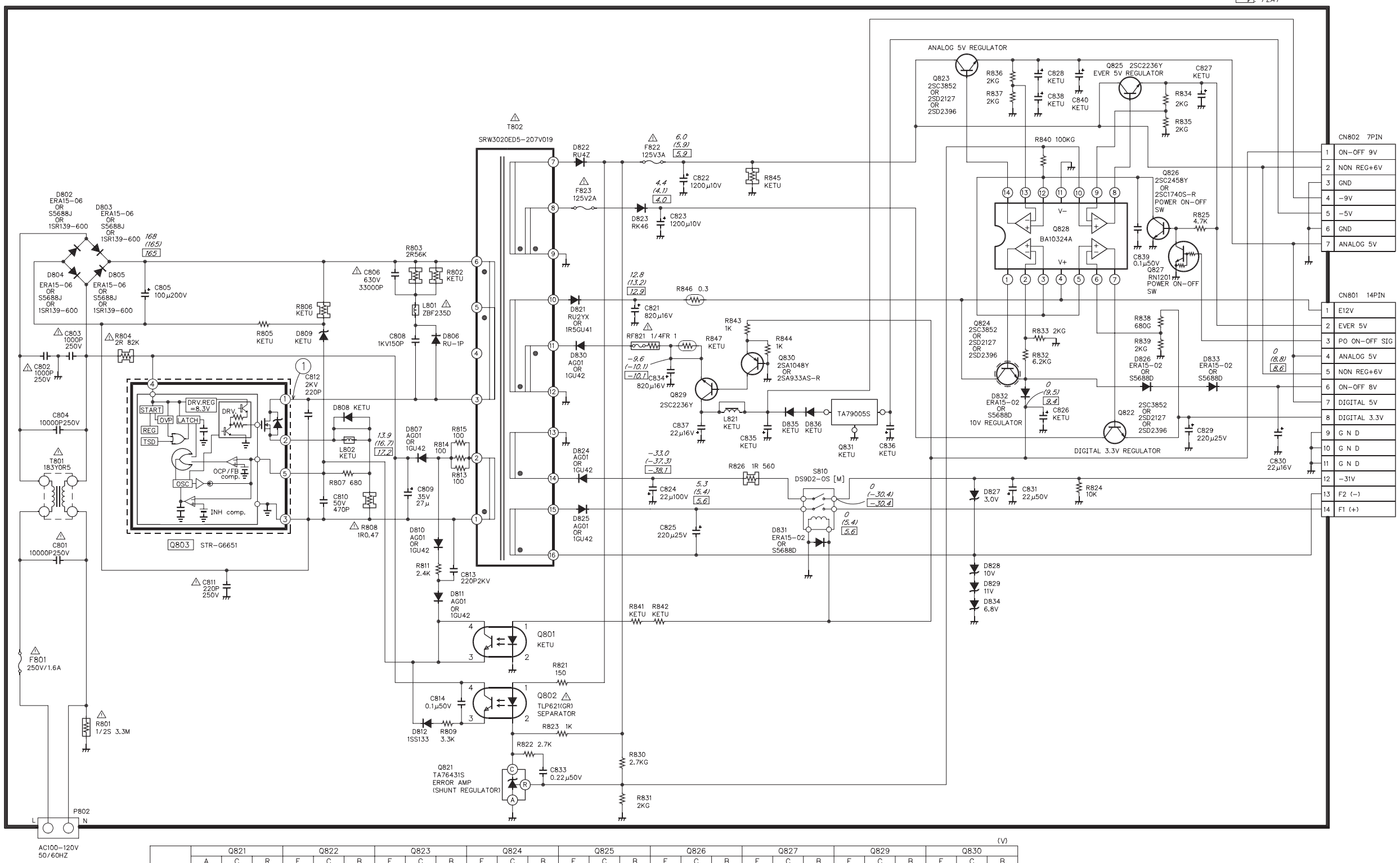


Fig. 3-3-3

EU02 POWER

V: OFF (STANDBY)
(V): ON
[V]: PLAY



(V)

	Q821			Q822			Q823			Q824			Q825			Q826			Q827			Q829			Q830		
	A	C	R	E	C	B	E	C	B	E	C	B	E	C	B	E	C	B	E	C	B	E	C	B	E	C	B
OFF	0	4.8	2.5	0	4.4	0	0	6.0	0	0	12.8	0	5.0	6.0	5.6	0	0	0.7	0	0.7	0	−9.6	0	−8.8	0	−8.8	0
ON	0	4.8	2.5	3.3	4.1	4.0	4.9	5.9	5.6	10.2	13.2	10.8	5.0	5.9	5.6	0	2.5	0	0	0	4.6	−10.1	−10.0	−9.4	0.7	−9.4	0
PLAY	0	4.8	2.5	3.3	4.1	4.0	4.9	5.9	5.6	10.2	12.8	10.8	5.0	5.9	5.6	0	2.5	0	0	0	4.6	−10.1	−10.0	−9.4	0.7	−9.4	0

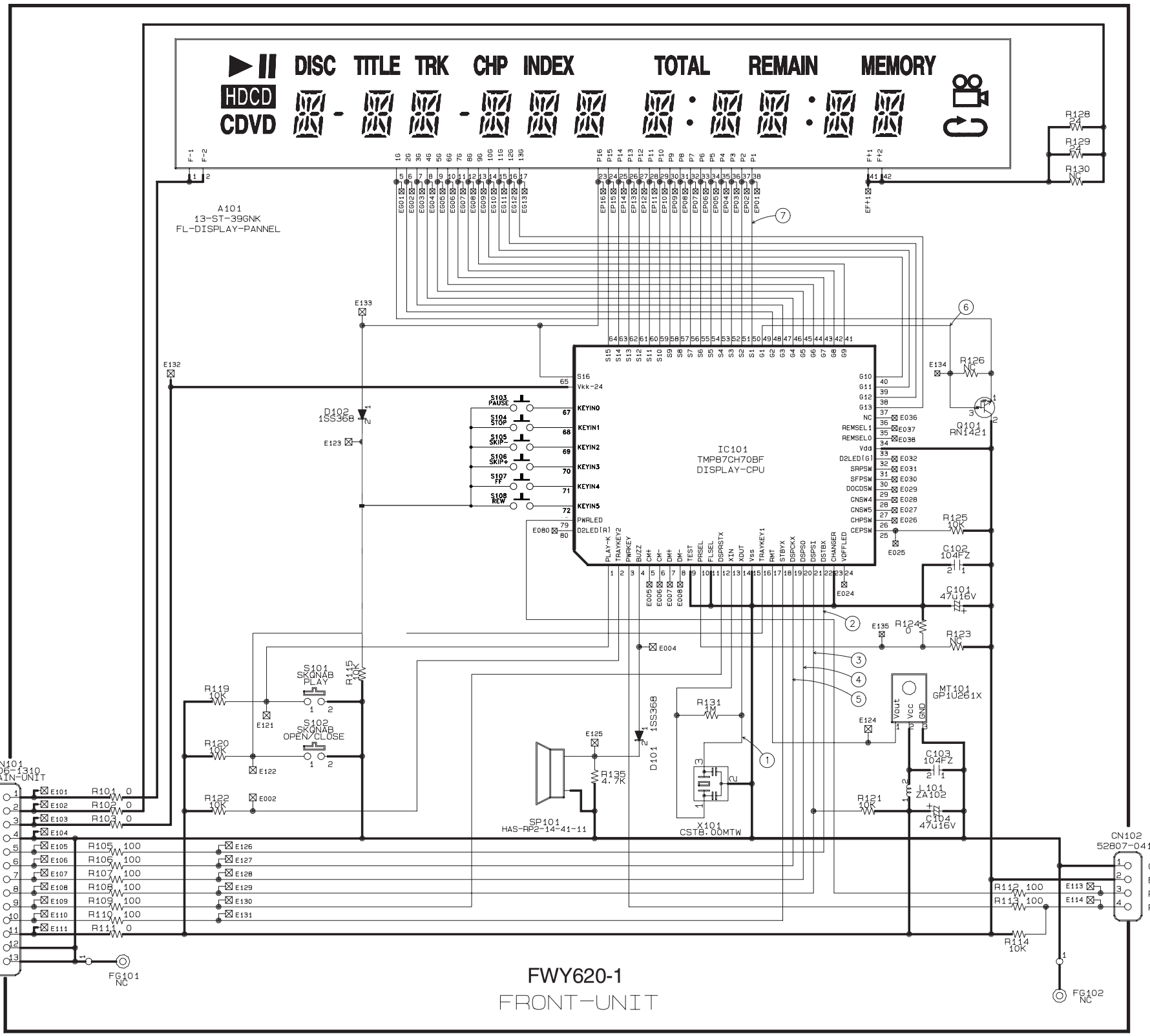
(V)

	Q828													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
OFF	0	0	0	12.8	0	0	0	5.6	2.5	2.5	0	0	0	0
ON	10.8	2.5	2.5	13.2	2.5	2.5	4.0	5.6	2.5	2.5	0	2.5	2.5	5.6
PLAY	10.8	2.5	2.5	12.8	2.5	2.5	4.0	5.6	2.5	2.5	0	2.5	2.5	5.6

Fig. 3-5-2

5-2. Front Display, Power Switch Circuit Diagram

EU03 FRONT



EU04 POWER SWITCH

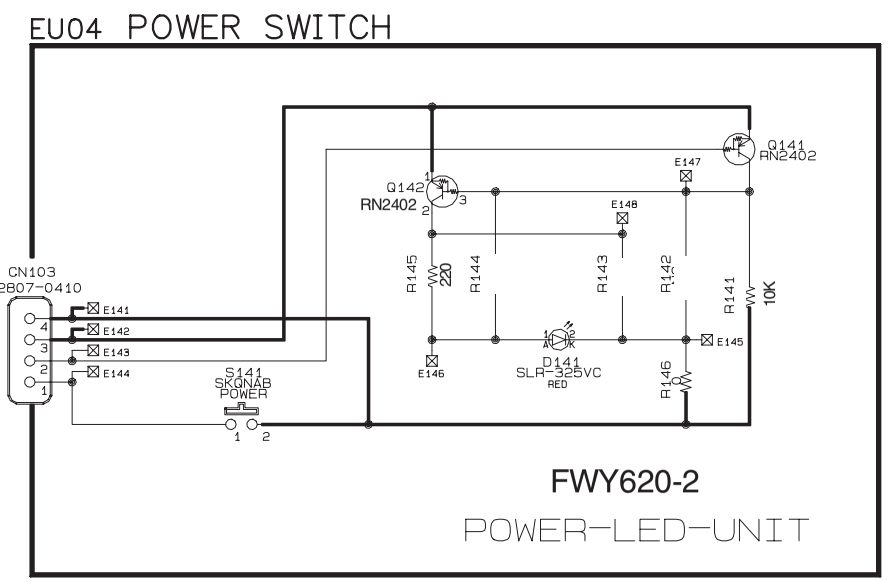


Fig. 3-5-3

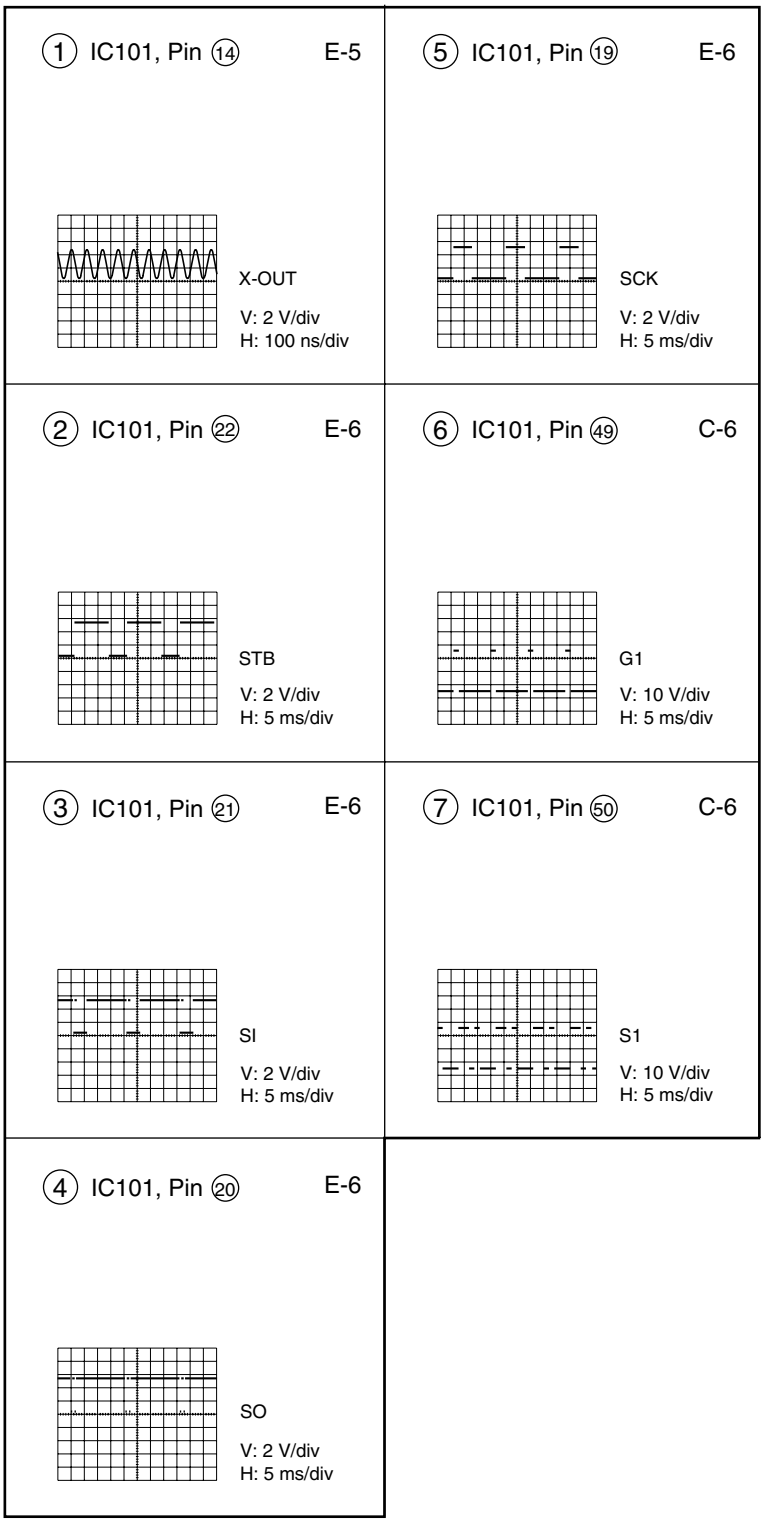


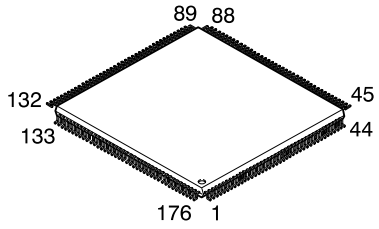
Fig. 3-5-4

Part No.	Location	Part No.	Location
A101	B2	EG03	B3
C101	E6	EG04	B3
C102	D6	EG05	B3
C103	F6	EG06	B4
C104	F6	EG07	B4
CN101	F1	EG08	B4
CN102	F7	EG09	B4
CN103	F8	EG10	B4
D101	F5	EG11	B4
D102	D3	EG12	B4
D141	F9	EG13	B4
E002	F3	EP01	B5
E004	E5	EP02	B5
E005	E5	EP03	B5
E006	E5	EP04	B5
E007	E5	EP05	B5
E008	E5	EP06	B5
E025	D6	EP07	B5
E026	D6	EP08	B5
E027	D6	EP09	B5
E028	D6	EP10	B5
E029	D6	EP11	B5
E030	D6	EP12	B5
E031	D6	EP13	B4
E032	D6	EP14	B4
E036	D6	EP15	B4
E037	D6	EP16	B4
E038	D6	FG101	G2
E071	D4	FG102	G7
E072	D4	IC101	D5
E073	D4	L101	F6
E074	D4	MT101	E6
E075	D4	Q101	D6
E076	D4	Q141	F10
E077	D4	Q142	F9
E078	D4	R101	F2
E080	D4	R102	F2
E101	F1	R103	F2
E102	F1	R105	F2
E103	F1	R106	F2
E104	F1	R107	F2
E105	F1	R108	F2
E106	F1	R109	F2
E107	F1	R110	F2
E108	F1	R112	F7
E109	F1	R113	F7
E110	F1	R114	G7
E111	G1	R115	E3
E113	F7	R119	E2
E114	F7	R120	E2
E121	E3	R121	F6
E122	F3	R122	F2
E123	D3	R123	E6
E124	E6	R124	E6
E125	E4	R125	D6
E126	F2	R126	C6
E127	F2	R128	B7
E128	F2	R129	B7
E129	F2	R130	B7
E130	F2	R131	E5
E131	F2	R135	F4
E132	C2	R141	F10
E133	C3	R142	F10
E134	C6	R143	F10
E135	E6	R144	F9
E141	F8	R145	F9
E142	F8	R146	F10
E143	F8	S101	E3
E144	F8	S102	E3
E145	F10	S103	D3
E146	F9	S104	D3
E147	F10	S105	D3
E148	F10	S106	E3
EF+1	B6	S141	F8
EG01	B3	SP101	F4
EG02	B3	X101	F5

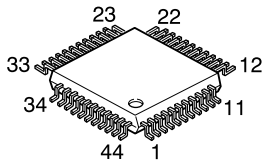
5-3. Main Circuit Diagrams

5-3-1. Main ICs Information

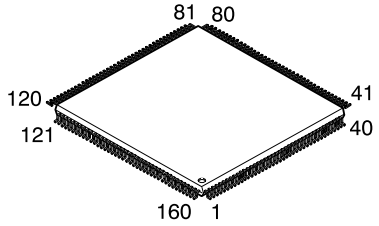
TC9453F



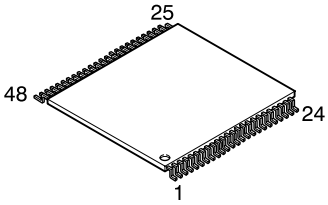
ADV7170



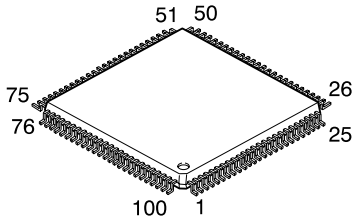
MD36710X, TMP94CS40AF



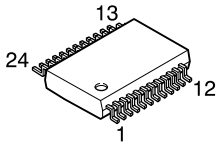
MBM29F800TA-55



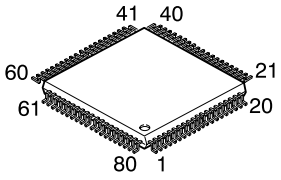
TC203G08AF



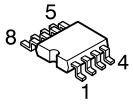
PCM1727



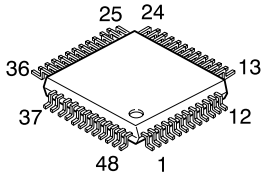
TA1293F



S24C01AFJ-TB



KA3032



Main ICs Function

Table 3-5-1

Ref. No.	IC Name	Function	Detail
IC613	S24C01AFJ-TB	EE-PROM	Setup default, memorization of specification setting.
IC306	ADV7170	Video Encorder	Built-in D/A converter. Encodes digital video signal to analog video signal of NTSC/PAL system.
IC301	MD36710X	AV Decorder	Decryption, MPEG-2 Decode, Audio Decode, Sub Picture Decode, OSD.
IC502	TC9453F	SERVO & Data Processor	Performs servo control of DVD or CD, and performs demodulation and correction of RF signal.
IC501	TA1293F	RF Signal processing IC	Equalizes of playback RF signal and generates error detection signal required for each servo operation.
IC504	KA3032	5-CH Motor Driver	5ch driver for motor driving.
IC901	PCM1727	DA Converter	Stereo audio DA converter with a dual PPL built-in.
IC601	TMP94CS40AF-0103(Z)	Main Micro Processor	Performs system control for all circuits.
IC201	TC203G08AF	Track Buffer	Rate control and Buffer control.
IC615	MBM29F800TA-55	Flash ROM	Memorization for firmware.
IC309	TC203G08AF-0101(Z)	3D DNR	3 Dimension Digital Noise Reduction.

Table 3-5-2 (1/2) ADV7170

Pin No.	Name	Function
1	V_{AA}	Power supply
2 3 4 5 6 7 8 9	P5-P12	8 bit, 4:2:2 Multiplexed Y/Cr/Cb pixel port (P7-P0) or 16 bit Y/Cr/Cb pixel port (P15-P0). P0 represents the LSB.
10	GND	Ground
11	V_{AA}	Power supply
12 13 14	P13-P15	8 bit, 4:2:2 Multiplexed Y/Cr/Cb pixel port (P7-P0) or 16 bit Y/Cr/Cb pixel port (P15-P0). P0 represents the LSB.
15	HSYNC	HSYNC (Modes 1 & 2) control signal. Master Mode: control signal output Slave Mode: control signal acceptance
16	FIELD/ VSYNC	Dual function field (Mode 1) and VSYNC (mode 2) control signal. Master Mode: control signal output Slave Mode: control signal acceptance
17	BLANK	Video blanking control signal. The pixel inputs are ignored when this is logic level "0". This signal is optional.
18	ALSB	TTL address input. This signal set up the LSB of the MPU address.
19	GND	Ground pin
20	V_{AA}	Power supply
21	GND	Ground pin
22	RESET	This pin resets the on-chip timing generator and sets the ADV7170 into default mode. NTSC operation, timing slave mode 0, 8 bit operation, 2 x composite & S VHS OUT.
23	SCLOCK	MPU port serial interface clock input
24	SDATA	MPU port serial data input/output
25	COMP	Compensation pin. Connect a 0.1μF capacitor from COMP to V_{AA}. For optimum dynamic performance in low power mode, the value of the COMP capacitor can be varied as described in low power mode section.

Table 3-5-2 (2/2) ADV7170

Pin No.	Name	Function
26	RED/ CHROMA/V	RED/S-VHS C/V analog output.
27	GREEN/ LUMA/Y	Green/S-VHS Y/Y analog output.
28	V_{AA}	Power supply
29	GND	Ground pin
30	V_{AA}	Power supply
31	BLUE/ CVBS/U	Blue/Composite/U analog output
32	COMPO-SITE (CVBS)	PAL/NTSC composite video output.
33	V_{REF}	Voltage reference input for DACs or voltage reference output.
34	R_{SET}	A 150 ohm resistor connected from this pin to GND is used to control full scale amplitudes of the video signal.
35	SCRESET/ RTC	This pin can be configured as an input by setting MR22 and MR21 of mode register 2. It can be configured as a subcarrier reset pin, in which case a high to low transition on this pin will reset the subcarrier to field 0. Alternately it may be configured as a real time control (RTC) input.
36	TTX REQ	Teletext data request signal Defaults to GND when teletext not selected (enables backward compatibility to ADV7175/ADV7176).
37	TTX V_{AA}	Teletext data Defaults to V_{AA} when teletext not selected (enables backward compatibility to ADV7175A/ADV7176.)
38 39 40 41 42	P0-P4	8 bit, 4:2:2 Multiplexed Y/Cr/Cb pixel port (P7-P0) or 16 bit Y/Cr/Cb pixel port (P15-P0). P0 represents the LSB.
43	GND	Ground pin
44	CLOCK	TTL clock input.

Table 3-5-3 KA3032

Pin No.	Name	Function
1	OUT1	CH1 OP-AMP output
2	IN2.1	CH2 OP-AMP input (+)
3	IN2.2	CH2 OP-AMP input (-)
4	OUT2	CH2 OP-AMP output
5	IN3.1	CH3 OP-AMP input (+)
6 7	GND	Ground
8	IN3.2	CH3 OP-AMP input (-)
9	OUT3	CH3 OP-AMP output
10	IN4.1	CH4 OP-AMP input (+)
11	IN4.2	CH4 OP-AMP input (-)
12	OUT4	CH4 OP-AMP output
13	CTL	CH5 motor speed control
14	FWD1	CH5 forward input
15	REV1	CH5 reverse input
16	SGND	Signal ground
17	OPOUT	OP-AMP output
18 19	GND	Ground
20	OPIN(+)	OP-AMP input (+)
21	IPIN(-)	OP-AMP input (-)
22	MUTE4	CH4 mute
23	MUTE3	CH3 mute
24	MUTE1,2	CH1,2 mute
25	PVCC1	Power supply voltage (for CH5)
26	DO5.2	CH5 drive output
27	DO5.1	CH5 drive output
28	DO4.2	CH4 drive output
29	DO4.1	CH4 drive output
30 31	GND	Ground
32	DO3.2	CH3 drive output
33	DO3.1	CH3 drive output
34	PGND	Power ground
35	DO2.2	CH2 drive output
36	DO2.1	CH2 drive output
37	DO1.2	CH1 drive output
38	DO1.1	CH1 drive output
39	PVCC2	Power supply voltage (for CH1, CH2, CH3, CH4)
40	GEG50	Regulator output
41	REG050	Regulator 5V output
42 43	GND	Ground
44	RES50	Regulator reset
45	SVCC	Signal supply voltage
46	REF	Bias voltage input
47	IN1.1	CH1 OP-AMP input (+)
48	IN1.2	CH1 OP-AMP input (-)

Table 3-5-4 MBM29F800TA-55

Pin No.	Name	Function
1 | 8 16 | 24 25 45 48	A_{-1}, A_0 - A_{18}	Address input
29 | 36 38 | 45	DQ_0 - DQ_{15}	Data I/O
26	$\overline{CE}$	Chip enable
28	$\overline{OE}$	Output enable
11	$\overline{WE}$	Write enable
12	$\overline{RESET}$	Hardware reset
15	RY/$\overline{BY}$	Ready/busy output
47	$\overline{BYTE}$	8 bit, 16 bit mode switch
27	V_{SS}	Ground
37	V_{CC}	Power supply
9 10 13 14	N.C.	Not connected.

Table 3-5-5 MD36710X (1/5)

Pin No.	Name	Function
Host Interface, CD-DSP interface, Sub ode interface (32 pins)		
	HD [15:12]	When connecting HWID to V_{DD}, become data lines 15:12 of 16 bit host data bus. When connecting HWID to GND, the lines become CD-DSP serial input port pins defined as below.
3	CDERR (HD [15])	CD-DSP data error input
4	CDFRM (HD [14])	CD-DSP LR clock (frame) input
5	CDDAT (HD [13])	CD-DSP data input
6	CDDAT (HD [12])	CD-DSP bit clock input
	HD [11:8]	When connecting HWID to V_{DD}, become data lines 11:8 of 16 bit host data bus. When connecting HWID to GND, the lines become sub code port pins defined as below.
7	SCCLK (HD [11])	Sub code bit clock output
9	SCDAT (HD [10])	Sub code bit clock input
10	SCSYN (HD [9])	Sub code sync signal display input
11	SCFRM (HD [8])	Sub code frame sync input
12 14 | 16 19 | 21	HD [7:0]	8 l.s. host data bus. When connecting HWID to GND, only the 8 l.s. signal is defined as a host data signal. When connecting HWID to V_{DD}, 8 l.s. line is used for of 16 bit data bus.
22 24 25 26	HA [3:0]	Host address input. Inputs address signal that specifies physical address inside MD36710X.
27	HWR# (HR/W#)	Host protocol, type A (HTYPE=GND): HR/W#. Decides direction of host access. Host protocol, type B (HTYPE=V_{DD}): HWR#. Host writing input (active low).
29	HCS#	Host chip select input. Active low.
30	HRD# (HDS#)	Host protocol, type A (HTYPE=GND): HDS#. Data strobe input (active low). Host protocol, type B (HTYPE=V_{DD}): HRD#. Host writing input (active low).
31	HRDY	Host ready output (active high). Use this signal to transmit bit stream via host bus. External pull-up resistor is required. Transmission of CodBurstLen byte length is determined as 1 packet. Check that the signal is active before transmitting each packet. Possible to write the bit stream serially up to CodBurstLen byte to MD36710X.
32	HACK#	Host acknowledge output (active low). Protocol is type A, MD36710X asserts this output and notify completion of reading or writing cycle. If this signal is not active, 3-state condition occurs (External pull-up resistor is required.). If protocol is type B, the signal functions as wait output signal. When high speed host (microprocessor) is used, this signal may not be used.
34	HIRQ#	Interruption requirement (active low). Deassert when host reads interruption status resister of MD36710X. Also deassert after host masks interruption in the interrupt mask resister of MD36710X or reseting. If HIRQ# is not asserted, 3-state condition occurs (External pull-up resistor is required.)

Table 3-5-5 MD36710X (2/5)

Pin No.	Name	Function
35	HWID	Determines data bus width of host interface. It can be changed only during reset. Host interface of MD36710X is set to 8 bit width at low level (GND) and set to 16 bit width at high level (V_{DD}).
36	HORD	Determines byte order for data bus of host interface in 16 bit width setting. (HWID: V_{DD}). It can be changed only during reset. Set MD36710X to obtain I/O signals of m.s. byte in HD [15:8] at low level (GND) and those in HD [7:0] at high level. If HWID is GND level, connect to GND.
37	HTYPE	Determines protocol of host bus. It can be changed only during reset. Sets MD36710X to type A at low level and type B at High level.
130	STNDBY#	Standby input (active low). All output pins and bidirectional pins become float state if asserting with RESET# and MD36710X is cut electrically from peripheral circuits. All internal operation stop and power consumption is confined to the minimum. Contents of SDRAM are not stored at stanby.
141	RESET#	Reset input (active low). Initializing process of MD36710X starts at the time deasserting is carried out from assert state.
142	IDLE	Idle, init or reset states display output (active high).
GPI/O signal (4 pins)		
2	GPSI	General input controlled by DVP micro code.
122 123	GPAI/O [1:0]	General bidirectional pin controlled by ADP micro code. After resetting, this pin is defined as an input pin. ADP command specifies the setting.
159	GPSO	General output conrolled by DVP micro code.
PLL signal (6 pins)		
126	GCLK1	Master clock input for audio. Must be connected to GCLK for usual operation.
128	XO	Output to the crystal connected to GCLK. If the crystal is not used for GCLK, XO is not connected.
129	GCLK	Clock for main processor or crystal input.
135 137	PLLCFG [1:0]	PLL configuration input. It can be changed only during reset. Both pins must be connected to GND (digital) for usual operation.
136	PLLCA	Capacitor connection pin for PLL. Connect the other terminal of the capacitor to PLLGND.

Table 3-5-5 MD36710X (3/5)

Pin No.	Name	Function
Digital video port (24 pins)		
84	VCLK	VCLKx2 signal is divided by 2. Used as a qualifier of data and sync signal.
85	VMASTER	Video master/slave selection input. At high level, video sync in MD36710X enters master mode. (Video sync and clock signals are developed.) After low level, video sync enters slave mode. (Video sync and clock signals are entered.) Only during reset, setting of terminal can be changed.
87	VDEN#	Video enable input (active low). When active, MD 36710X develops video data. When deasserting, pixel output becomes 3-state condition. (But sync and clock signals are kept to be active.) Input is changeable at any time but becomes effective at the next VCLKx2.
89	VSYNC	Vertical sync bidirectional signal pin. Polarity and length are programmable.
90	HSYNC	Horizontal sync bidirectional signal pin. Polarity and length are programmable.
91	FI	Field identification bidirectional signal pin. Polarity is programmable.
92 94 | 97 99 | 101	Y [7:0]	At 16 bit video mode (Video 8=0), develop luminance signals. At 8 bit mode (Video 8=1), develop luminance and color difference signals multiplexed in time sequence according to the ITU-R656 standard (in no relation to presence of SAV and EAV sync code).
98	CBLANK	Composite blank output. Waveforms are programmable other than polarity.
102 104 105 106 107 109 | 111	C [7:0] OSDPLT (C [4]) OSDPEL [3:0] (C [3:0])	At 16 bit video mode (Video 8=0), develop color difference signal. At 8 bit mode (Video 8=1), m.s. line 3 pin (c [7:5]) is not used, l.s.5 pin (C [4:0]) is used as input from external OSD device. On-chip OSD palette selector. Selects OSD Palette0 at low level and OSD Plette1 at high level. OSD pixel input. Used as an entry signal to on-chip OSD palette.
124	VCLKx2	Main video clock input or output.
Digital audio port (8 pins)		
112	AIN	Serial input of PCM stereo audio for ADC
114 115 116	AOUT [2:0]	Serial output of PCM stereo audio for DAC. After reset, develop signals of low level. Only AOUT [0] supports 24 bit sample width.
117	S/PDIF (AOUT [3])	S/PDIF transmitter output. Possible to connected to DAC as the forth audio output (AOUT [3]). After reset, develop signal of low level.
118	ALRCLK	LR clock output of AOUT [3..0] and AIN. Becomes square waveform in sampling frequency. Polarity of LR is programmable.
119	ABCLK	Bit clock output of AOUT [3..0] and AIN. At rising/falling edges (programmable) AOUT is developed and AIN is latched.

Table 3-5-5 MD36710X (4/5)

Pin No.	Name	Function
132	AMCLK	Audio master clock I/O. 384 fs, 256 fs, 192 fs and 128 fs of sampling frequency can be selected (programmable).
DVD-DSP interface (13 pins)		
143	DVDERR	DVD-DSP error input (Polarity programmable)
144	DVDSOS	DVD-DSP data selector start input (Polarity programmable)
146	DVDVALID	DVD-DSP data effective input (Polarity programmable)
147	DVDSTRB	DVD-DSP data bit strobe (clock) input. Polarity programmable.
148	DVDREQ	DVD-DSP data requirement output (Polarity programmable)
149 151 | 154 156 | 158	DVDDAT [7:0]	DVD-DSP data input bus
SDRAM interface (35 pins)		
38 39 42 | 47 49 | 52	RAMADD [11:0]	SDRAM address bus output
54	RAMCS0#	SDRAM chip select (active low) output. Lower bit for 2 Mbyte device.
55	RAMCS1#	SDRAM ship select (active low). Upper bit for 2 Mbyte device.
56	RAMRAS#	Row selection of SDRAM (active low) output
57	PCLK	SDRAM clock output (same as internal process clock).
59	RAMCAS#	Column selection of SDRAM (active high) output
60	RAMWE#	SDRAM write enable (active low) output
61	RAMDQM	SDRAM data masking (active high) output
62 64 | 67 69 | 72 74 | 79 82	RAMDAT [15:0]	SDRAM bidirectional data bus
TEST signal (3 pins)		
83	TESTMODE	Test pin. Connects to V_{DD} for normal.
127	SCNENBL	Test pin. Connects to GND for normal.
139	ICEMODE	Test pin. Connects to V_{DD} for normal.

Table 3-5-5 MD36710X (5/5)

Pin No.	Name	Function
Power signal (35 pins)		
1 40 41 53 68 80 81 93 108 120 121 125 131 145 160	GND	Digital GND
8 28 33 48 58 63 73 86 78 113 133 140 150 155	VDD	Digital power supply (3.3V)
134	PLLGND (GNDA)	GND of internal PLL circuit
138	$PLLV_{DD}$ ($V_{DD}A$)	Power supply of internal PLL circuit

Table 3-5-6 PCM1727

Pin No.	Name	Function
1	XT1	PLL master clock input or crystal connector terminal
2	PGND	PLL GND
3	V_{CP}	PLL power supply
4	MCKO	Master clock buffer output
5	RSV	Not connected. Use the pin with open.
6	SCKO3	PLL-2 generation system clock output.
7	ML	Serial control data enable input.(1)
8	MC	Serial control data clock input.(1)
9	MD	Serial control data, data input.(1)
10	$\overline{RSTB}$	External reset input, reset at L.(1)
11	$V_{OUT}R$	Rch analog audio output
12	AGND	Analog GND
13	V_{CA}	Analog power supply
14	$V_{OUT}L$	Lch analog audio output
15	CAP	Internal analog bias (connected with a bypass capacitor)
16	$\overline{ZERO}$	Infinity zero detection output.(2)
17	BCK	PCM audio data, bit clock input.(3)
18	DATA	PCM audio data, data input.(3)
19	LRCK	PCM audio data, LRCK input (f_S)(3)
20	SCKO2	PLL-1 generation system clock output
21	SCKO1	PLL-1 generation system clock output
22	V_{DD}	Digital power supply
23	DGND	Digital GND
24	XT2	Crystal oscillator connection terminal, connected to GND at external clock input.

Note:
(1) With internal pull-up. Schmitt trigger input.
(2) Open drain output.
(3) Schmitt trigger input.

Table 3-5-7 S-24C01AFJ-TB-01

Pin No.	Name	Function
1	A0	Address input
2	A1	Address input
3	A2	Address input
4	GND	Ground
5	SDA	Serial data I/O
6	SCL	Serial clock input
7	TEST	Connect to GND.
8	V_{CC}	Power supply

Table 3-5-8 (1/2) TA1293F

Pin No.	Name	Function
1	GNDP	GND terminal
2	LDO2	Drive terminal
3	MDI2	Monitor terminal
4 5	NC	- - -
6	VrA	Analog V_{REF}
7	Vrfi	Filter capacity for reference
8	VrD	Digital V_{REF}
9	Vdd	Power supply terminal
10	DPAC	DPD AC coupling capacity 1
11	DPBD	DPD AC coupling capacity 2
12	DPD1	DPD integration capacity 1
13	DPD2	DPD integration capacity 2
14	SCB	Control line (bit clock)
15	SCL	Control line (latch signal)
16	SCD	Control line (serial data)
17	VRCK	Reference clock input
18 19	NC	- - -
20	VCKF	Capacity for time constant adjustment
21	VccP	Power supply terminal
22 23 24 25	NC	- - -
26	RFSW	RFO control terminal
27	VccS	Power supply terminal
28 29 30	NC	- - -
31	LVL	Servo addition output
32	NC	- - -
33	TEO	TE output
34	FEO	FE output
35 36 37 38 39	NC	- - -
40	DFTN	DPD defect
41	RPZ	RF ripple center output
42	RPO	RF ripple output
43	RPB	Bottom of RF ripple
44	RPP	Peak of RF ripple
45	RFO	Equivalent RF output
46	VccR	Power supply terminal (RF)
47	DPDB	Pit depth adjustment
48	TEB	TE balance
49	FEB	FE balance
50	PSC	VRCK dividing ON/OFF
51	VccO	Power supply terminal
52	Vcc2	Power supply terminal
53	NC	- - -
54	EQD	Group delay correction
55	GND2	GND terminal

Table 3-5-8 (2/2) TA1293F

Pin No.	Name	Function
56	RFDC	DC feed back capacity
57	EQB	Boost adjustment
58	EQF	Frequency adjustment
59	MDI1	Monitor input
60	LDO1	Drive output
61	P1TN	TE- input (DVD)
62	P1TP	TE+ input (DVD)
63	P1FN	FE- input (DVD)
64	P1FP	FE+ input (DVD)
65	LDP1	APC polarity 1
66	GNDR	GND terminal
67	P1DI	D input (DVD)
68	P1CI	C input (DVD)
69	P1BI	B input (DVD)
70	P1AI	A input (DVD)
71	LDP2	APC polarity 2
72	P2AI	A input (CD)
73	P2BI	B input (CD)
74	P2CI	C input (CD)
75	P2DI	D input (CD)
76	GNDS	GND terminal
77	P2FP	FE+ input (CD)
78	P2FN	FE- input (CD)
79	P2TP	TE+ input (CD)
80	P2TN	TE- input (CD)

Table 3-5-9 (1/4) TC9453F

Pin No.	Name	Function
1 2	NC	- - -
3	DVSS	Exclusive ground for DAC
4	RO	R-ch output signal
5	DVDD	Exclusive power supply for DAC
6	DVR	Amplifier reference signal output
7	LO	L-ch output signal
8	DVSS	Exclusive ground for DAC
9	XVSS	Exclusive ground for oscillator
10	XI	Crystal oscillation input
11	XO	Crystal oscillation output
12	XVDD	Exclusive power supply for oscillator
13 14 15	TESM0 TESM1 TESM2	Test terminal
16	VDD3	Digital power supply
17	VSS3	Digital ground
18	VPFC	Clock PLL phase/frequency comparison output
19	TEST0	Test mode terminal
20	VLPFI	VCO filter input for clock PLL
21	VLPFO	VCO filter output for clock PLL
22	VSS3	Digital ground
23 24 25 26 27 28 29 30 31 32	MON0 MON1 MON2 MON3 MON4 MON5 MON6 MON7 MON8 MON9	Test monitor
33	VDD3	Digital power supply
34 35	NC	- - -
36	TEST1	Test mode terminal
37	FLGA	General I/O or flag monitor
38	FLGB	General I/O or flag monitor
39	VSS3	Digital ground
40	/RST	Reset terminal
41	/MA	Microprocessor address enable signal
42	/MRD	Microprocessor data read signal
43	/MWR	Microprocessor data write signal
44	/MCE	Microprocessor chip enable signal
45	/MINT	Microprocessor interrupt signal
46 47 48 49 50 51 52 53	MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7	Microprocessor data bus
54	VDD5	Power supply
55 56	NC	- - -
57	SMCK	Clock output
58	VMCK	Data output (signal process) clock output

Table 3-5-9 (2/4) TC9453F

Pin No.	Name	Function
59	VDD3	Digital power supply
60	PD0	DVD/CD data output
61	VSS5	Ground
62 63 64 65	PD1 PD2 PD3 PD4	DVD/CD data output
66	VSS3	Digital ground
67 68 69 70	PD5 PD6 PD7 PD8	DVD/CD data output
71	/PSYC	DVD data sector sync signal
72	/PDRQ	DVD data transfer block
73	PDCK	DVD data transfer clock
74	VDD5	Power supply for 5V
75	TESM3	Test terminal
76	DIGI	1 bit DAC digital IN input
77	TESM4	Test terminal
78	VDD3	Digital power supply
79 80 81 82	BA0 BA1 BA2 BA3	External RAM address output
83	VSS5	Ground
84 85 86 87 88	BA4 BA5 BA6 BA7 BA8	External RAM address output
89	VDD3	Digital power supply
90	/BOE	External RAM/OE signal
91	/BRAS	External RAM/RAS signal
92	/BCAS	External RAM/CAS signal
93	/BWL	External RAM Lower/WE signal
94	/BWU	External RAM Upper/WE signal
95	VDD5	Power supply
96 97 98 99 100 101 102 103 104	BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7 BD8	External RAM data I/O
105	VSS3	Digital ground
106 107 108 109	BD9 BD10 BD11 BD12	External RAM data I/O
110	VSS5	Ground
111 112 113	BD13 BD14 BD15	External RAM data I/O
114 115	NC	- - -
116	VDD3	Digital power supply
117	PLCK	PLL clock I/O

Table 3-5-9 (3/4) TC9453F

Pin No.	Name	Function
118 119 120 121	TESM5 TESM6 TESM7 TESM8	Test terminal
122	VSS3	Digital ground
123	CFC1	VCO frequency control signal
124	CFC2	VCO frequency control signal
125	PPW	Phase comparator offset adjustment voltage output
126	PESV	Phase comparator offset adjustment signal input
127	PVSS	Exclusive ground for PLL
128	PESP	Phase comparator offset adjustment signal output
129	PDOP1	DVD/CD phase control signal (Positive polarity)
130	PDON1	DVD/CD phase control signal (Negative polarity)
131	PDOP2	DVD/CD phase control signal (Positive polarity)
132	PDON2	DVD/CD phase control signal (Negative polarity)
133	LPFN	Data PLL low pass filter inverted input
134	LPFO	Data PLL low pass filter output
135	PVREF	Exclusive reference power supply for data PLL
136	VCOREF	VCO reference
137	VCOF	VCO automatic adjustment filter output
138	PVDD	Exclusive power supply for PLL
139	SLCO1	Data slice 6 bit DAC output
140	TESM9	Test terminal
141	TEST2	Test mode terminal
142	RFCD	CD RF signal input
143	RFDVD	DVD RF signal input
144	AVDD	Exclusive power supply for analog
145	RFCT	RFRP center voltage input (zero cross)
146	RFZI	RFRP signal input (zero cross)
147	TEZI	Tracking error signal input (zero cross)
148	AWIN	Active wide PLL control signal input
149	AVSS	Exclusive ground for analog
150	FEI	Focus error signal input
151	TEI	Tracking error signal input
152	RFSB	RF level or sub beam signal addition input
153	RFRP	RFRP signal input
154	AVSS	Exclusive ground for analog
155	TESM10	Test terminal
156	EXTAD	General external ADC input
157	VREF	Exclusive reference power supply for analog
158	FOO	Focus EQ output
159	TRO	Tracking EQ output
160	AVDD	Exclusive power supply for analog
161	AWCTL	Active wide PLL control output
162	FMO	Focus EQ output
163	DMO	Disc EQ output

Table 3-5-9 (4/4) TC9453F

Pin No.	Name	Function
164	TEBC	Tracking balance control signal
165	FEBC	Focus balance control signal
166	DPDC	DPD error signal pit depth adjustment signal
167	EQBC	RF wide range boost adjustment signal
168	ANMON	General PWM output
169	/DFCT	Black dot detection signal
170	VRCK	RF EQ characteristic control clock
171	VSS3	Digital ground
172	SCD	Head amplifier serial data
173	SCL	Head amplifier serial data latch pulse
174	SCB	Head amplifier serial data clock
175	FGIN	Disc FG signal input (with self-bias circuit)
176	NC	- - -

* " / " indicated at the head of pin name means active "L" pin.

Table 3-5-10 (1/5) TMP94CS40AF

Pin No.	Name	Function
77 | 84	P00 - P07 D0 - D7	Port 0: I/O port. Data 0-7: data bus 0-7. Function is selectable by setting of AM0/1 terminal. It becomes high impedance at no external memory access.
86 | 93	P10 - P17 D8 - D15	Port 1: I/O port. Data 8-15: data bus 8-15. Function is selectable by setting of AM0/1 terminal. It becomes high impedance at no external memory access.
95 | 102	P20 - P27 D16 - D23	Port 2: I/O port. Data 16-23: data bus 16-23. Function is selectable by setting of AM0/1 terminal. It becomes high impedance at no external memory access.
104 | 111	P30 - P37 D24 - D31	Port 3: I/O port. Data 24-31: data bus 24-31. Function is selectable by setting of AM0/1 terminal. It becomes high impedance at no external memory access.
113 | 120	P40 - P47 A0 - A7	Port 4: I/O port. Address 0-7: address bus 0-7. Function is selectable by setting of AM0/1 terminal. Signal does not change at no external memory access.
122 | 129	P50 - P57 A8 - A15	Port 5: I/O port. Address 8-15: address bus 8-15. Function is selectable by setting of AM0/1 terminal. Signal does not change at no external memory access.
131 | 138	P60 - P67 A16 - A23	Port 6: I/O port. Address 16-23: address bus 16-23. Function is selectable by setting of AM0/1 terminal. Signal does not change at no external memory access.
75	P70 $\overline{RD}$	Port 70: output port. (Initializes to "1" output.) Read: strobe signal reading external memory. Function is selectable by setting of AM0/1 terminal. Strobe signal is not developed at no external memory access.
74	P71 $\overline{WRLL}$	Port 71: output port. (Initializes to "1" output.) Write: strobe signal writing D0-D7 of external memory. Strobe signal is not developed at no external memory access.
73	P72 $\overline{WRLH}$	Port 72: output port. (Initializes to "1" output.) Write: strobe signal writing D8-D15 of external memory. Strobe signal is not developed at no external memory access.
72	P73 $\overline{WRHL}$	Port 73: output port. (Initializes to "1" output.) Write: strobe signal writing D16-D23 of external memory. Strobe signal is not developed at no external memory access.
71	P74 $\overline{WRHH}$	Port 74: output port. (Initializes to "1" output.) Write: strobe signal writing D24-D31 of external memory. Strobe signal is not developed at no external memory access.

Table 3-5-10 (2/5) TMP94CS40AF

Pin No.	Name	Function
70	P75 $\overline{BUSRQ}$	Port 75: I/O port. Bus request: signal with memory interface terminal requested to be high impedance. The following pins become high impedance, but no change is made when used as a port. A0 - A23, D0 - D31, $\overline{RD}$, $\overline{WRLL}$, $\overline{WRLH}$, $\overline{WRHL}$, $\overline{WRHH}$, $\overline{CS0}$ - $\overline{CS5}$, $\overline{OE0}$ - $\overline{OE1}$, $\overline{WE0}$-$\overline{WE1}$, $\overline{RAS}$ group, $\overline{CAS}$ group
69	P76 $\overline{BUSAK}$	Port 75: output port. (Initializes to "1" output.) Bus acknowledge: signal, that indicates request of $\overline{BUSRQ}$ received.
67	P80 $\overline{CS0}$	Port 80: output port. (Initializes to "1" output.) Chip select 0: "L" level is developed if address is within the assigned address range.
66	P81 $\overline{CS1}$ $\overline{RAS0}$	Port 81: output port. (Initializes to "1" output.) Chip select 1: "L" level is developed if address is within the assigned address range. Low address strobe 0: $\overline{RAS}$ strobe signal for DRAM is developed if address is within the assigned address range.
65	P82 $\overline{CS2}$	Port 82: output port. (Initializes to "0" output.) Chip select 2: "L" level is developed if address is within the assigned address range.
64	P83 $\overline{CS3}$ $\overline{RAS1}$	Port 83: output port. (Initializes to "1" output.) Chip select 3: "L" level is developed if address is within the assigned address range. Low address strobe 1: $\overline{RAS}$ strobe signal for DRAM is developed if address is within the assigned address range.
63	P84 $\overline{CS4}$	Port 84: output port. (Initializes to "1" output.) Chip select 4: "L" level is developed if address is within the assigned address range.
62	P85 $\overline{CS5}$	Port 85: output port. (Initializes to "1" output.) Chip select 5: "L" level is developed if address is within the assigned address range.
49	P86 $\overline{WAIT}$	Port 86: I/O port. Wait: Bus wait request signal
60	PA0 $\overline{CAS0}$ $\overline{LCAS0}$	Port A0: output port. (Initializes to "1" output.) Column address strobe 0: $\overline{CAS}$ strobe signal for DRAM is developed if address is within the assigned address range. Lower column address strobe 0: lower $\overline{CAS}$ strobe signal for DRAM is developed if address is within the assigned address range.
59	PA1 $\overline{UCAS0}$	Port A1: output port. (Initializes to "1" output.) Upper column address strobe 0: upper $\overline{CAS}$ strobe signal for DRAM is developed if address is within the assigned address range.
58	PA2 $\overline{OE0}$	Port A2: output port. (Initializes to "1" output.) Out enable 0: out enable signal for DRAM is developed.
57	PA3 $\overline{OE1}$	Port A3: output port. (Initializes to "1" output.) Out enable 1: out enable signal for DRAM is developed.
56	PA4 $\overline{WE0}$	Port A4: output port. (Initializes to "1" output.) Write enable 0: write enable signal for DRAM is developed.

Table 3-5-10 (3/5) TMP94CS40AF

Pin No.	Name	Function
55	PB0 $\overline{CAS1}$ $\overline{LCAS1}$ $\overline{LLCAS1}$	Port B0: output port. (Initializes to "1" output.) Column address strobe 1: $\overline{CAS}$ strobe signal for DRAM is developed if address is within the assigned address range. Lower column address strobe 1: lower $\overline{CAS}$ strobe signal for DRAM is developed if address is within the assigned address range. Lower-lower column address strobe 1: lower-lower $\overline{CAS}$ strobe signal for DRAM is developed if address is within the assigned address range.
54	PB1 $\overline{UCAS1}$ $\overline{LUCAS1}$	Port B1: output port. (Initializes to "1" output.) Upper column address strobe 1: upper $\overline{CAS}$ strobe signal for DRAM is developed if address is within the assigned address range. Lower-upper column address strobe 1: lower-upper $\overline{CAS}$ strobe signal for DRAM is developed if address is within the assigned address range.
53	PB2 $\overline{HLCAS1}$	Port B2: output port. (Initializes to "1" output.) Upper-lower column address strobe 1: upper lower $\overline{CAS}$ strobe signal for DRAM is developed if address is within the assigned address range.
52	PB3 $\overline{HUCAS1}$	Port B3: output port. (Initializes to "1" output.) Upper-upper column address strobe 1: upper-upper $\overline{CAS}$ strobe signal for DRAM is developed if address is within the assigned address range.
51	PB4 $\overline{WE1}$	Port B4: output port. (Initializes to "1" output.) Write enable 1: write enable signal for DRAM is developed.
140	PC0 TO1 TO7	Port C0: I/O port. Timer output 1: 8 bit timer 0 or timer 1 is developed. Timer output 7: 16 bit timer 7 is developed.
141	PC1 TO3 TOB	Port C1: I/O port. Timer output 3: 8 bit timer 2 or timer 3 is developed. Timer output B: 16 bit timer B is developed.
17	PD0 TO4	Port D0: I/O port. Timer output 4: 16 bit timer 4 is developed.
18	PD1 TI4 INT4	Port D1: I/O port. Timer input 4: 16 bit timer 4 is entered. Interrupt request terminal 4: programmable at rising/falling edges.
19	PD2 TI5 INT5	Port D2: I/O port. Timer input 5: 16 bit timer 4 is entered. Interrupt request terminal 5: Interrupt request terminal at rising edge.
20	PD4 TO6	Port D4: I/O port Timer output 6: 16 bit timer 6 is developed.
21	PD5 TI6 INT6	Port D5: I/O port. Timer input 6: 16 bit timer 6 is entered. Interrupt request terminal 6: programmable at rising/falling edges.
22	PD6 TI7 INT7	Port D6: I/O port. Timer input 7: 16 bit timer 6 is entered. Interrupt request terminal 7: Interrupt request terminal at rising edge.
24	PE0 TO8	Port E0: I/O port. Timer output 8: 16 bit timer 8 is developed.
25	PE1 TI8 INT8	Port E1: I/O port. Timer input 8: 16 bit timer 8 is entered. Interrupt request terminal 8: programmable at rising/falling edges.
13	PE2 TI9 INT9	Port E2: I/O port. Timer input 9: 16 bit timer 8 is entered. Interrupt request terminal 9: Interrupt request terminal at rising edge.

Table 3-5-10 (4/5) TMP94CS40AF

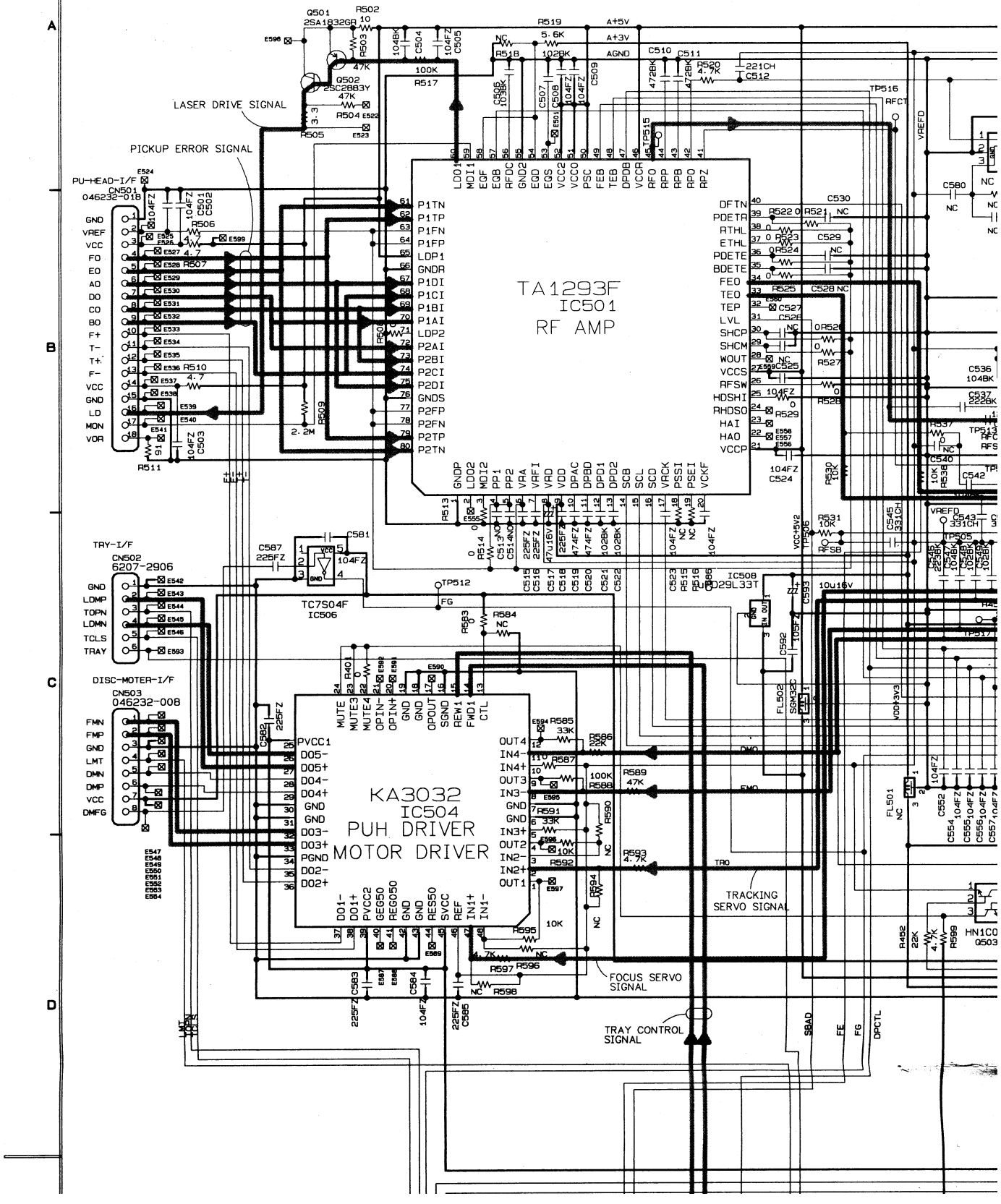
Pin No.	Name	Function
14	PE4 TOA	Port E4: I/O port. Timer output A: 16 bit timer A is developed.
15	PE5 TIA INTA	Port E5: I/O port. Timer input A: 16 bit timer A is entered. Interrupt request terminal A: programmable at rising/falling edges.
16	PE6 TIB INTB	Port E6: I/O port. Timer input B: 16 bit timer A is entered. Interrupt request terminal B: Interrupt request terminal at rising edge.
24	PF0 TXD0	Port F0: I/O port. Serial transfer data 0 (open drain output capability)
25	PF1 RXD0	Port F1: I/O port. Serial reception data 0
26	PF2 $\overline{CTS0}$ SCLK0	Port F2: I/O port. Serial transfer capability 0 Serial clock I/O 0
27	PF4 TXD1	Port F4: I/O port. Serial transfer data 1 (open drain output capability)
28	PF5 RXD1	Port F5: I/O port. Serial reception data 1
29	PF6 $\overline{CTS1}$ SCLK1	Port F6: I/O port. Serial transfer capability 1 Serial clock I/O 1
152 to 159	AN0 – AN7	Analog input: input of 10 bit A/D converter.
6	PH0 TC0	Port H0: I/O port. Terminal count 0: Strobe output signal is developed at "H" level when count value of micro DMA channel 0 is 0.
7	PH1 TC1	Port H1: I/O port. Terminal count 1: Strobe output signal is developed at "H" level when count value of micro DMA channel 1 is 0.
8	PH2 TC2	Port H2: I/O port. Terminal count 2: Strobe output signal is developed at "H" level when count value of micro DMA channel 2 is 0.
9	PH3 TC3	Port H3: I/O port Terminal count 3: Strobe output signal is developed at "H" level when count value of micro DMA channel 3 is 0.
10	PH4 INT0	Port H4: I/O port (schmitt input) Interrupt request terminal 0: programmable at level/rising edge. (Schmitt input)
31	$\overline{NMI}$	Nonmaskable interrupt request terminal: interrupt request terminal at falling edge. Available at rising edge by using a program.
32	$\overline{WDTOUT}$	Watchdog timer output terminal
4 5	AM0,1	Address mode: selects start-up external data bus width after releasing reset. AM1= "0" AM0= "0": starts with 8 bit external data bus AM1= "0" AM0= "1": starts with 16 bit external data bus AM1= "1" AM0= "0": starts with 32 bit external data bus AM1= "1" AM0= "1": starts from internal ROM
43 48	TEST0,1	Test: used with "GND" fixed.
36	CLK	Clock: develops system clock.
38 40	X1/X2	Oscillation connection terminal

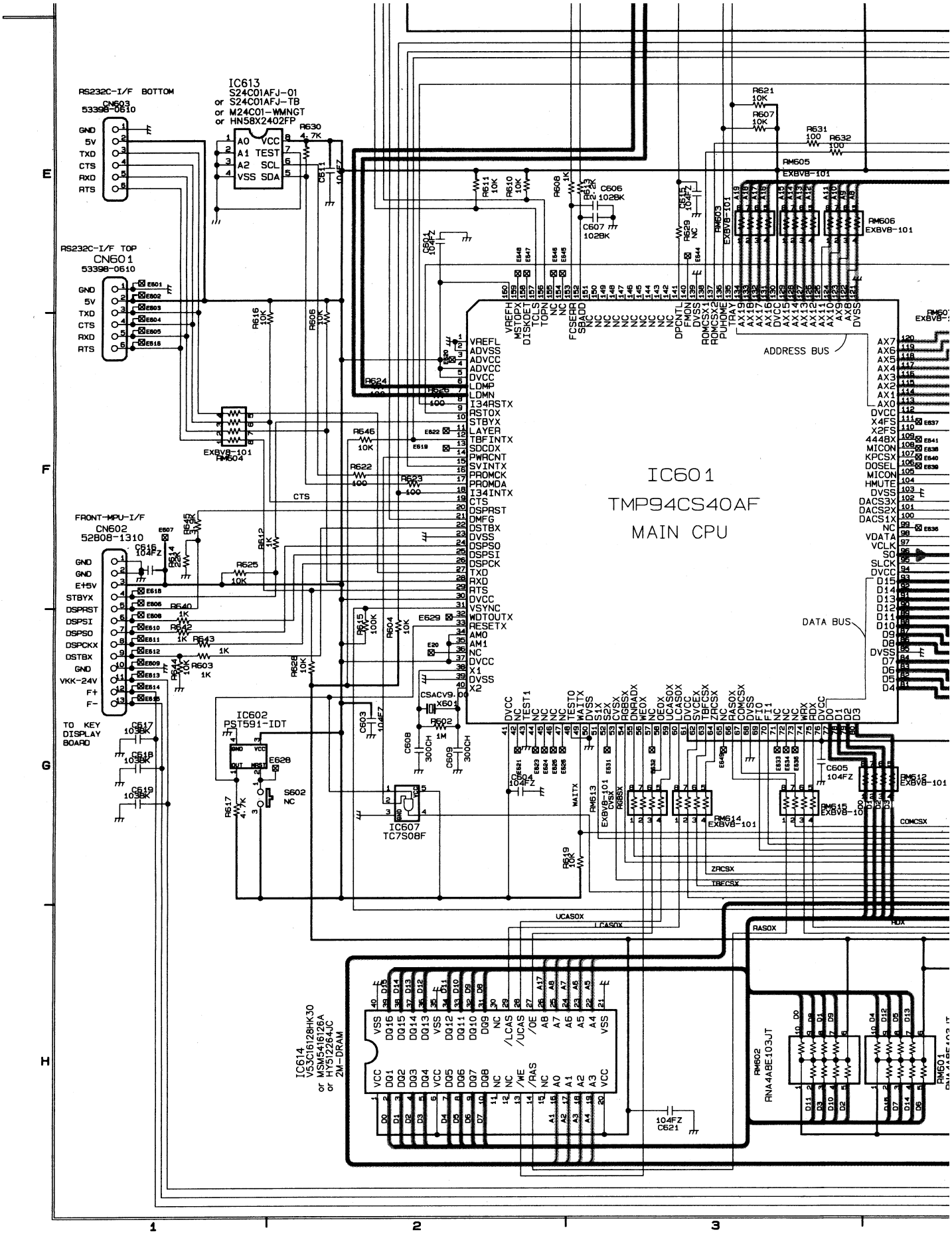
Table 3-5-10 (5/5) TMP94CS40AF

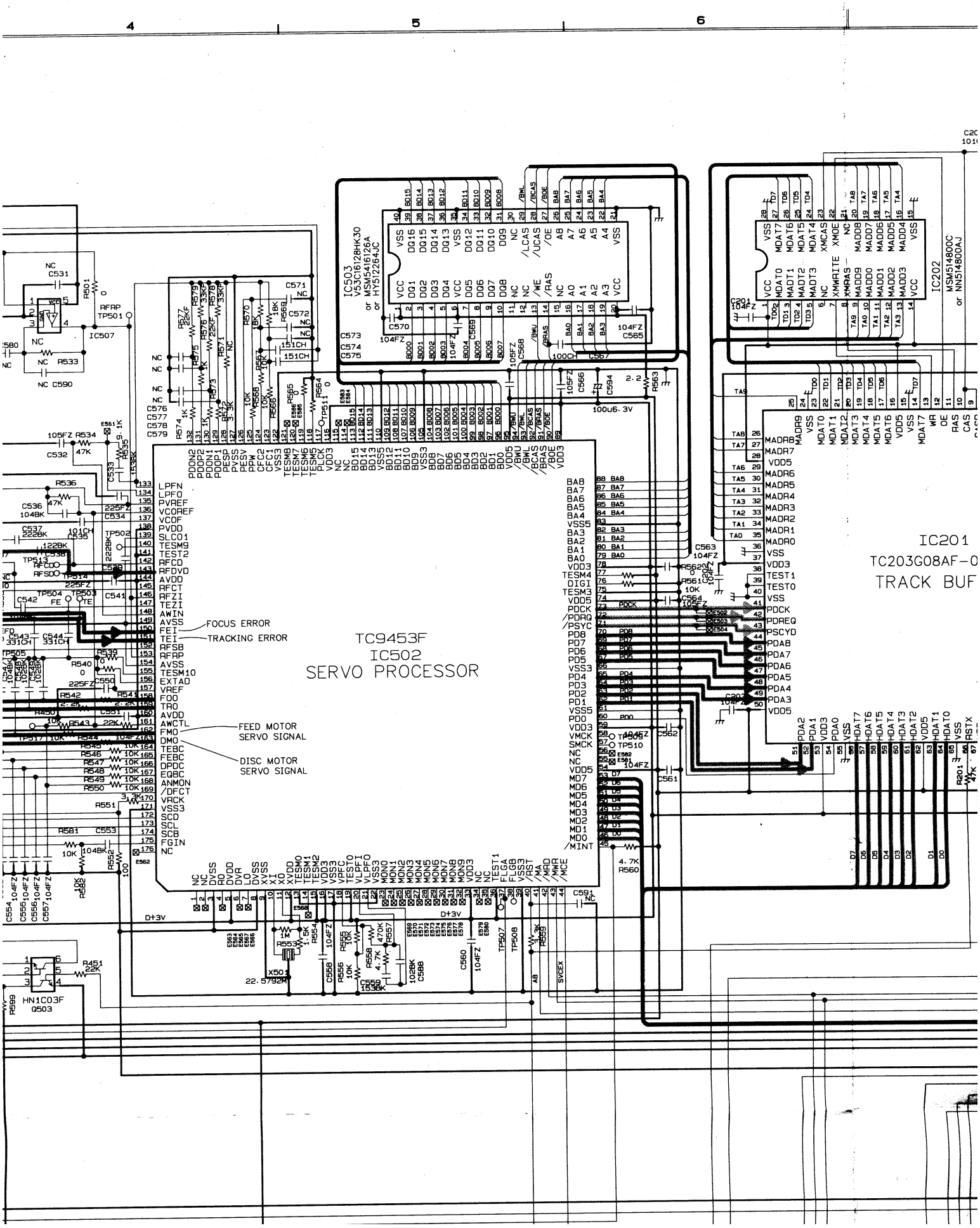
Pin No.	Name	Function
33	$\overline{\text{RESET}}$	Reset: initializes device (with pull-up resistance) (schmitt input)
160	VREFH	Reference voltage input terminal (H) for 10 bit A/D converter
1	VREFL	Reference voltage input terminal (L) for 10 bit A/D converter
4	ADVCC	10 bit A/D converter power supply terminal
2	ADVSS	10 bit A/D converter GND terminal
37	CLVCC	Power supply terminal for clock doubler
39	CLVSS	GND terminal for clock doubler
30	DVCC	Digital power supply terminal
23	DVSS	Digital GND terminal

5-3-2. Main Circuit Diagram

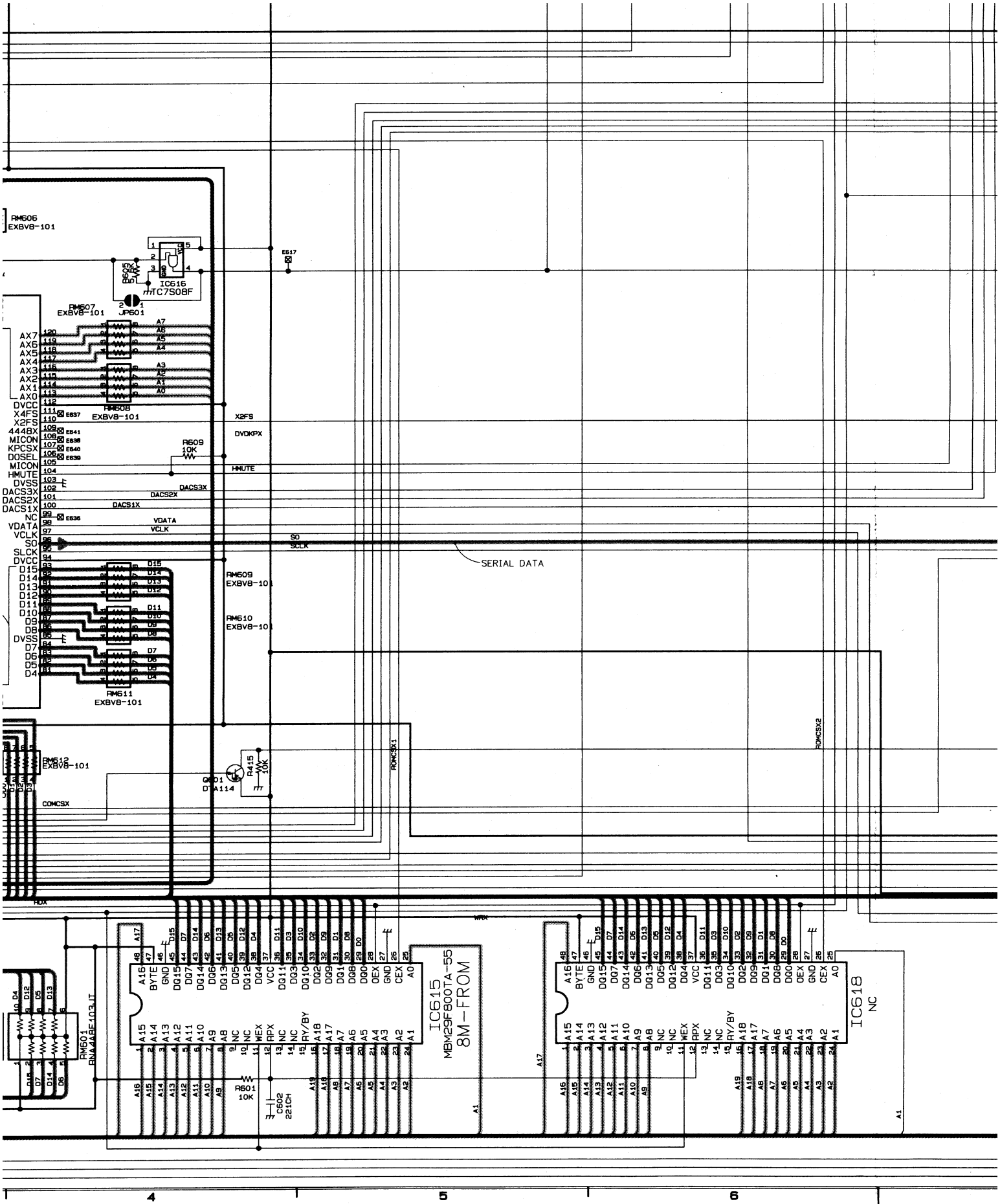
Part No.	Location
C201	A6
C202	B6
C203	C6
C204	B8
C205	A7
C301	G8
C302	G8
C303	F9
C304	E9
C305	E9
C306	E8
C307	G8
C308	E10
C309	E10
C310	F11
C311	F11
C312	F10
C313	F11
C314	F10
C315	F10
C316	H12
C317	B8
C318	C8
C319	C9
C320	E10
C321	B10
C322	G10
C323	E11
C335	F11
C336	F11
C337	G12
C338	G12
C339	G11
C340	H11
C341	H12
C344	G11
C345	G11
C347	C9
C349	A9
C350	A9
C351	B11
C352	C11
C501	B1
C502	B1
C503	B1
C504	A2
C505	A2
C506	A2
C507	A2
C508	A2
C509	A2
C510	A3
C511	A3
C512	A3
C513	C2
C514	C2
C515	C2
C516	C2
C517	C2
C518	C2
C519	C2
C520	C2
C521	C2
C522	C2
C523	C3
C524	B3
C525	B3
C526	B3
C527	B3
C528	B3
C529	B3
C530	B3
C531	A4
C532	B4
C533	B4
C534	B4
C535	B4
C536	B4
C537	B4
C538	B4
C539	B4
C540	B3
C541	B4
C542	B4
C543	C4
C544	C4
C545	C3
C546	C3
C547	C4
C548	C4
C549	C4
C550	C4
C551	C4
C552	C4
C553	C4
C554	C4
C555	C4
C556	C4
C557	C4
C558	D5
C559	D5
C560	D5
C561	C6
C562	C6
C563	B6
C564	B6
C565	A6
C566	B6
C567	B6
C568	B5
C569	A5
C570	A5
C571	A5
C572	A5
C573	A5
C574	B5
C575	B5
C576	B4
C577	B4
C578	B4
C579	B4
C580	A4
C581	C2
C582	C1
C583	D2
C584	D2
C585	D2
C586	C2
C587	C1
C588	D5
C590	B4
C591	C6
C592	C3
C593	C3
C594	B6
C601	E2
C602	H4
C603	G2
C604	G2
C605	G3
C606	E3
C607	E3
C608	G2
C609	G2
C610	G10
C611	E2
C615	E3
C616	F1
C617	G1
C618	G1
C619	G1
C621	H3
C622	H12
C623	H12
C624	H12
C901	A11
C902	A11
C903	A11
C904	A11
C905	A11
C906	B11
C907	A10
C908	A10
C909	A11
C910	B12
C911	A11
C912	A11
C913	A11
C914	B11
CN301	F12
CN302	D12
CN501	B1
CN502	C1
CN503	C1
CN601	E1
CN602	F1
CN603	E1
CN801	G12
CN901	B12
E20	G2
E303	F12
E304	F12
E305	F12
E306	F12
E307	F12
E308	F12
E309	F12
E310	F12
E311	F12
E312	F12
E313	F12
E314	F12
E315	F10
E316	F10
E317	F10
E318	F10
E319	F10
E320	F10
E321	F10
E322	F10
E323	F10
E324	F12
E326	E12
E327	E12
E328	E12
E329	E12
E330	B11
E331	C11
E332	E12
E333	D12
E334	D12
E335	D12
E336	D12
E337	D12
E338	E12
E339	E12
E340	B11
E341	E12
E501	A2
E502	B6
E503	B6
E504	C6
E522	A2
E523	A2
E524	A1
E525	B1
E526	B1
E527	B1
E528	B1
E529	B1
E530	B1
E531	B1
E532	B1
E533	B1
E534	B1
E535	B1
E536	B1
E537	B1
E538	B1
E539	B1
E540	B1
E541	B1
E542	C1
E543	C1
E544	C1
E545	C1
E546	C1
E547	D1
E548	D1
E549	D1
E550	D1
E551	D1
E552	D1
E553	D1
E554	D1
E555	C2
E556	B3
E557	B3
E558	B3
E559	B3
E560	B3
E561	B4
E562	C4
E563	D4
E564	D4
E565	D4
E566	D4
E567	D4
E568	C5
E569	D5
E570	D5
E571	D5
E572	D5
E573	D5
E574	D5
E575	D5
E576	D5
E577	D5
E578	D5
E579	D5
E580	D5
E581	C6
E582	C6
E583	B5
E584	B5
E585	B5
E586	B5
E587	D2
E588	D2
E589	D2
E590	C2
E591	C2
E592	C2
E593	C1
E594	C2
E595	C2
E596	D2
E597	D2
E598	A1
E599	B1
E601	E1
E602	E1
E603	E1
E604	F1
E605	F1
E606	F1
E607	F1
E608	G1
E609	G1
E610	G1
E611	G1
E612	G1
E613	G1
E614	G1
E615	G1
E616	F1
E617	E4
E618	F1
E619	F2
E620	F2
E621	G2
E622	F2
E623	G2
E624	G2
E625	G2
E626	G2
E628	G2
E629	G2
E631	G3
E632	G3
E633	G3
E634	G3
E635	G3
E636	F4
E637	F4
E639	F4
E640	F4
E641	F4
E644	E3
E645	E2
E646	E2
E647	E2
E648	E2
E649	G3
E801	G12
E802	G12
E803	G12
E804	G12
E805	G12
E806	G12
E807	H12
E808	H12
E810	H12
E811	H12
E812	H12
E813	H12
E814	H12
E815	G12
E816	G11
E817	G11
E818	G11
E819	H11
E901	B12
E902	B12
E903	C12
E904	C12
E905	C12
E906	C12
E907	C12
E908	C12
E909	C12
E910	C12
E911	C12
E912	C12
E913	C12
E914	C12
E915	C12
E916	C12
E917	C12
E918	C12
E919	C12
E920	C12
E921	C12
E922	C12
E923	C12
E924	C12
E925	C12
E926	A11
FL301	G12
FL302	G12
FL303	G11
FL304	G12
FL305	H12
FL308	F11
FL501	C3
FL502	C3
IC201	B7
IC202	A7
IC301	B9
IC302	C10
IC305	C8
IC306	F10
IC307	E10
IC308	E11
IC309	F9
IC310	G9
IC311	B10
IC312	B11
IC313	B11
IC314	B11
IC501	B2
IC502	C5
IC503	A5
IC504	C2
IC506	C2
IC507	A4
IC508	C3
IC601	F3
IC602	G1
IC607	G2
IC613	E1
IC614	H2
IC615	H5
IC616	E4
IC617	G10
IC618	H6
IC901	A11
IC902	A12
IC903	A10
IC904	A10
JP301	C8
JP601	F4
Q501	A2
Q502	A2
Q503	D4
Q601	G4
R201	C7
R301	F11
R302	F11
R303	F8
R305	F11
R306	F11
R307	F11
R308	F11
R309	F11
R310	F11
R311	C10
R312	C12
R313	C10
R314	B10
R315	F10
R316	E12
R317	E12
R319	F11
R320	A9
R321	A9
R323	G10
R324	G10
R325	B11
R326	E12
R327	E12
R328	F12
R329	A9
R401	C2
R415	G4
R450	C4
R451	D4
R452	D3
R501	A4
R502	A2
R503	A2
R504	A2
R505	A2
R506	B1
R507	B1
R508	B2
R509	B2
R510	B1
R511	B1
R513	C2
R514	C2
R515	C3
R516	C3
R517	A2
R518	A2
R519	A2
R520	A3
R521	B3
R522	B3
R523	B3
R524	B3
R525	B3
R526	B3
R527	B3
R528	B3
R529	B3
R530	B3
R531	C3
R533	B4
R534	B4
R535	B4
R536	B4
R537	B3
R538	B4
R539	C4
R540	C4
R541	C4
R542	C4
R543	C4
R544	C4
R545	C4
R546	C4
R547	C4
R548	C4
R549	C4
R550	C4
R551	C4
R552	C4
R553	D4
R554	D5
R555	D5
R556	D5
R557	D5
R558	D5
R559	D5
R560	C6
R561	B6
R562	B6
R563	B6
R564	B5
R565	B5
R566	B4
R567	B4
R568	B4
R569	A5
R570	A4
R571	B4
R572	B4
R573	B4
R574	B4
R575	B4
R576	A4
R577	A4
R578	A4
R579	A4
R581	C4
R582	C4
R583	C2
R584	C2
R585	C2
R586	C2
R587	C2
R588	C2
R589	C3
R590	C2
R591	C2
R592	D2
R593	D3
R594	D2
R595	D2
R596	D2
R597	D2
R598	D2
R599	D4
R601	H4
R602	G2
R603	G1
R604	G2
R605	E4
R606	F2
R607	E3
R608	E2
R609	F4
R610	E2
R611	E2
R612	F1
R613	E2
R614	F1
R615	G2
R616	F1
R617	G1
R618	H11
R619	G3
R620	G10
R621	E3
R622	F2
R623	F2
R624	F2
R625	F1
R626	F2
R628	G2
R629	E3
R630	E2
R631	E3
R632	E3
R640	F1
R642	G1
R643	G1
R644	G1
R645	F1
R646	F2
R901	B12
R902	A10
R903	C12
R904	C12
R905	C12
R906	C12
R907	C12
R908	A10
R909	A10
R910	A10
R911	C12
R912	A10
R913	A11
R914	B11
R915	B11
R916	B11
RM303	F10
RM304	E10
RM601	H4
RM602	H3
RM603	E3
RM604	F1
RM605	E3
RM606	E4
RM607	F4
RM608	F4
RM609	F4
RM610	G4
RM611	G4
RM612	G4
RM613	G3
RM614	G3
RM615	G3
RM903	C12
RM904	C12
RM905	C12
S602	G2
SD0	B8
SD1	B8
SD2	B8
SD3	B8
SD4	B8
SD5	B8
SD6	B8
SD7	B8
TP301	B9
TP302	C9
TP303	A9
TP304	A9
TP305	A10
TP306	A10
TP307	G10
TP308	G10
TP309	G11
TP501	A4
TP502	B4
TP503	B4
TP504	B4
TP505	C4
TP506	C3
TP507	D5
TP508	D5
TP509	C6
TP510	C6
TP511	B5
TP512	C2
TP513	B4
TP514	B4
TP515	A3
TP516	A3
TP517	C4
X301	E10
X501	D4
X601	G2

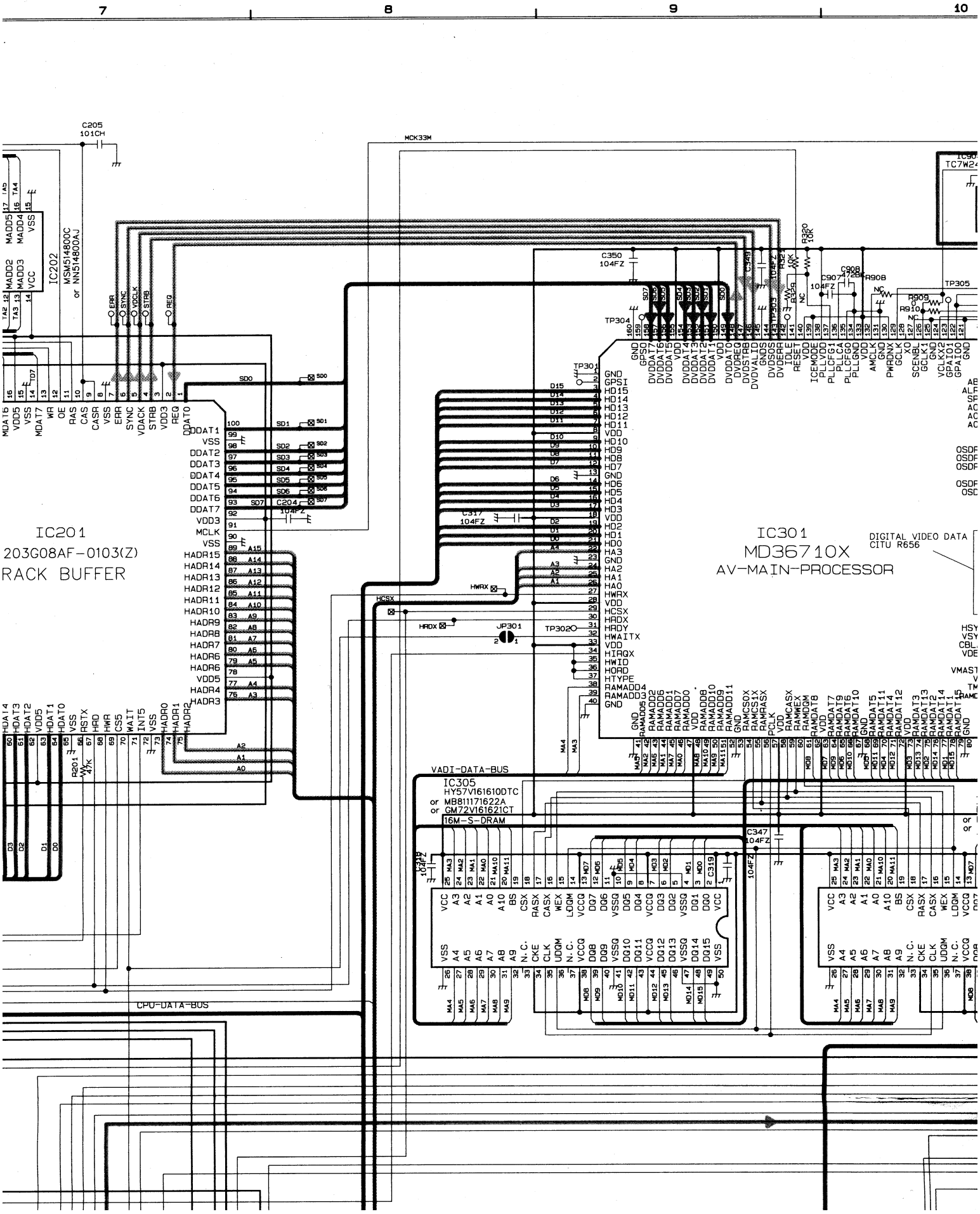

TA1293F
IC501
RF AMP
KA3032
IC504
PUH DRIVER
MOTOR DRIVER
TC7S04F
IC506
LASER DRIVE SIGNAL
PICKUP ERROR SIGNAL
TRACKING SERVO SIGNAL
FOCUS SERVO SIGNAL
TRAY CONTROL SIGNAL
PU-HEAD-I/F
CN501
046232-018
TRY-I/F
CN502
6207-2906
DISC-MOTER-I/F
CN503
046232-008
A+5V
A+3V
AGND
VREFD
RFCT


IC601
TMP94CS40AF
MAIN CPU
IC613
S24C01AFJ-01
or S24C01AFJ-TB
or M24C01-WMNGT
or HN58X2402FP
RS232C-I/F BOTTOM
CN603
53398-0610
RS232C-I/F TOP
CN601
53398-0610
FRONT-MPU-I/F
CN602
52808-1310
TO KEY DISPLAY BOARD
IC602
PST591-IDT
IC607
TC7S08F
IC614
V53C16128HK30
or MSM5416126A
or HY512264JC
2M-DRAM
RM602
RNA4A8E103JT
ADDRESS BUS
DATA BUS
RM605
EXBV8-101
RM606
EXBV8-101
RM604
EXBV8-101
RM613
EXBV8-101
RM614
EXBV8-101
RM615
EXBV8-101
RM612
EXBV8-101
CSACV9.00
X601
S602
NC
CTS
COMCSX
ZRCSX
TBFCSX
UCASOX
LCASOX
RASOX
RDX
WAITX
104FZ
C621
E
F
G
H
1
2
3

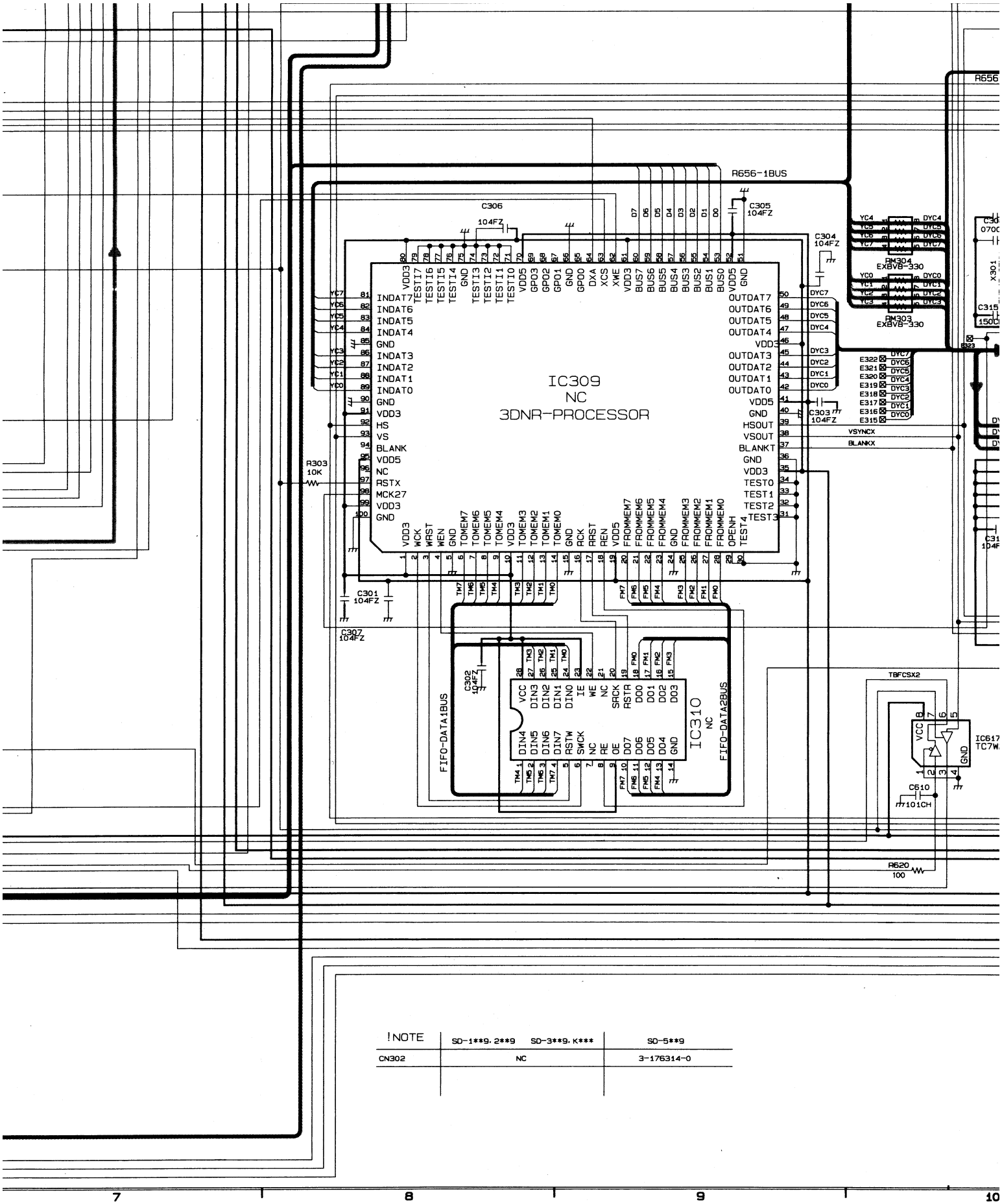


4
5
6
IC503
V53C16128HK30
or MSM5416126A
or HY5I2264JC
IC202
MSM514800C
or NN514800AJ
IC201
TC203G08AF-0
TRACK BUF
TC9453F
IC502
SERVO PROCESSOR
FOCUS ERROR
TRACKING ERROR
FEED MOTOR
SERVO SIGNAL
DISC MOTOR
SERVO SIGNAL
HN1C03F
Q503
IC507

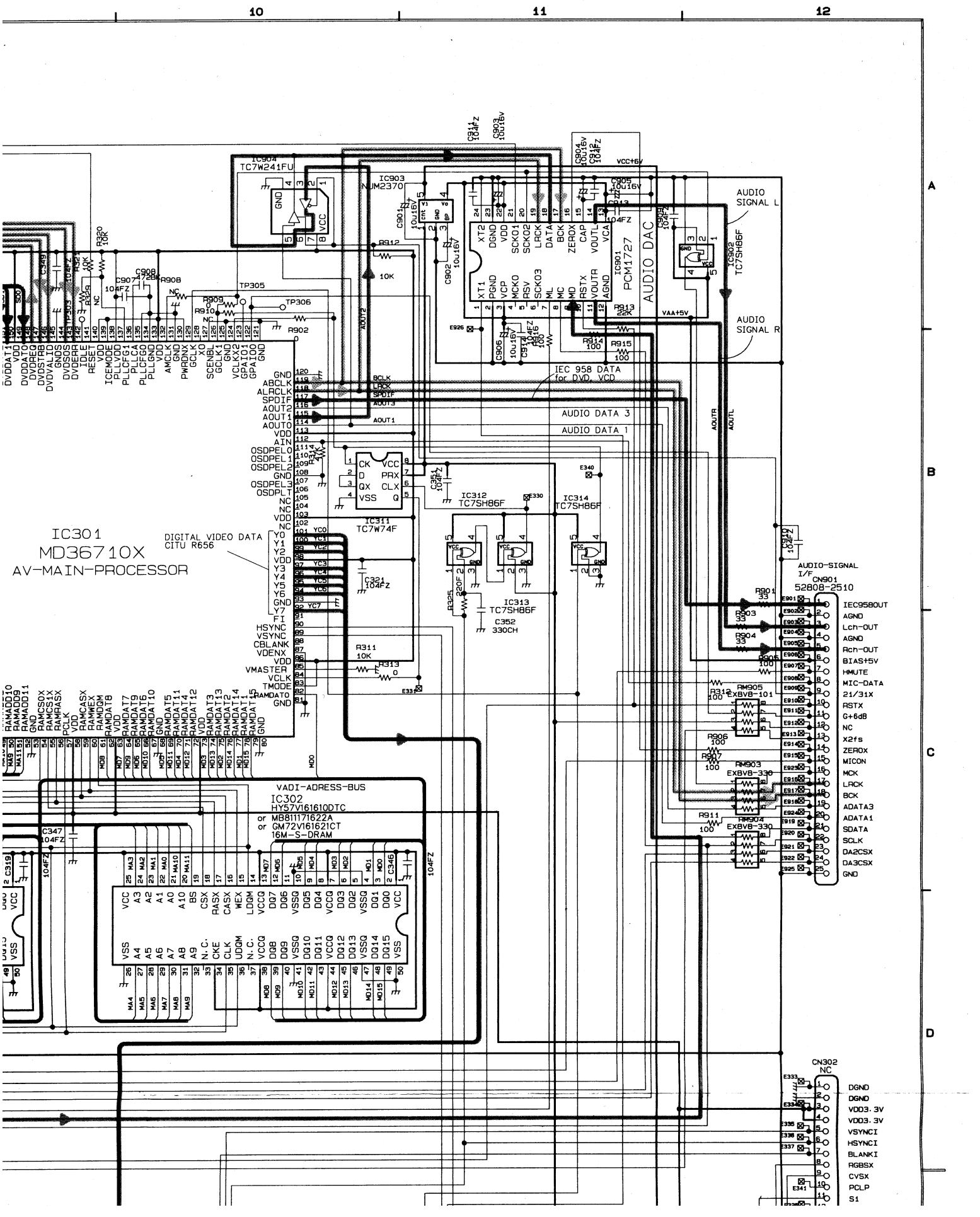

RM606 EXBV8-101
IC616 TC7S08F
JP601
RM607 EXBV8-101
RM608 EXBV8-101
AX7 AX6 AX5 AX4 AX3 AX2 AX1 AX0
DVCC X4FS X2FS 4448X MICON KPCSX DOSEL MICON HMUTE DVSS DACS3X DACS2X DACS1X NC VDATA VCLK SO SLCK DVCC
D15 D14 D13 D12 D11 D10 D9 D8 DVSS D7 D6 D5 D4
RM609 EXBV8-101
RM610 EXBV8-101
RM611 EXBV8-101
R609 10K
X2FS
DVDKPX
HMUTE
DACS3X
DACS2X
DACS1X
VDATA
VCLK
SO
SCLK
SERIAL DATA
RM612 EXBV8-101
COMCSX
Q601 DTA114
R415 10K
ROMCSX1
ROMCSX2
RDX
WRX
IC615 MBM29F800TA-55 8M-FROM
IC618 NC
RM601 RNA4ABE-103JT
R601 10K
C602 221CH
4
5
6

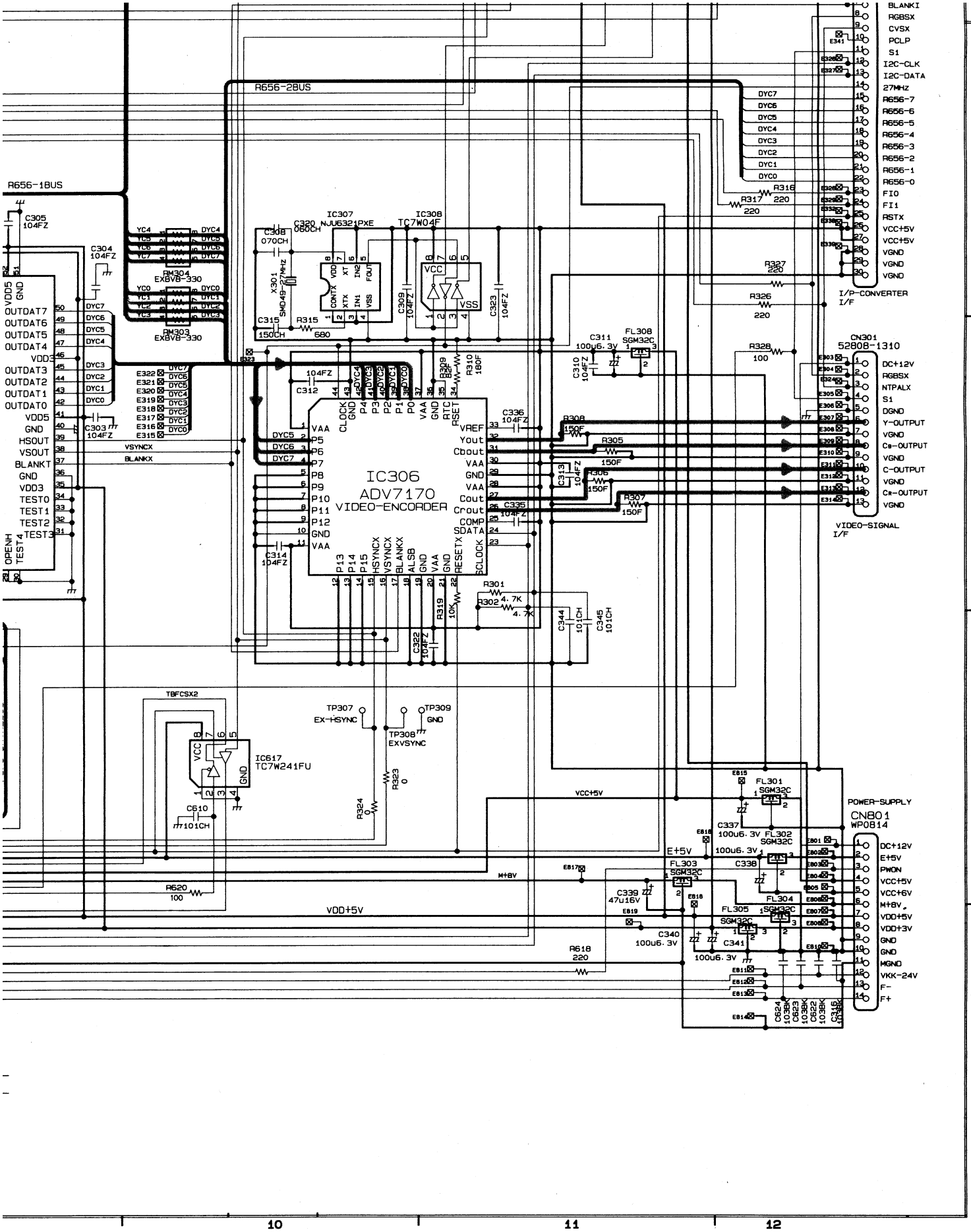


7
8
9
10
IC201
203G08AF-0103(Z)
RACK BUFFER
IC301
MD36710X
AV-MAIN-PROCESSOR
DIGITAL VIDEO DATA
CITU R656
IC202
MSM514800C
or NN514800AJ
IC305
HY57V161610DTC
or MB811171622A
or GM72V161621CT
16M-S-DRAM
VADI-DATA-BUS
CPU-DATA-BUS
MCK33M
C205
101CH
C350
104FZ
C317
104FZ
C204
104FZ
C347
104FZ
C318
104FZ
C319
104FZ
JP301
TP302
TP304
TP305
TP301
TP303
R201
47K
R320
10K
R321
10K
R329
R908
R909
R910
C907
104FZ
C908
472BK



!NOTE	SD-1**9, 2**9 SD-3**9, K***	SD-5**9
CN302	NC	3-176314-0


10
11
12
A
B
C
D
IC301
MD36710X
AV-MAIN-PROCESSOR
DIGITAL VIDEO DATA
CITU R656
IC904
TC7W241FU
IC903
NJM2370
PCM1727
AUDIO DAC
IC902
TC7SH86F
AUDIO SIGNAL L
AUDIO SIGNAL R
IEC 958 DATA
for DVD, VCD
AUDIO DATA 3
AUDIO DATA 1
IC311
TC7W74F
IC312
TC7SH86F
IC313
TC7SH86F
IC314
TC7SH86F
AUDIO-SIGNAL
I/F
CN901
52808-2510
IEC958OUT
AGND
Lch-OUT
AGND
Rch-OUT
BIAS+5V
HMUTE
MIC-DATA
21/31X
RSTX
G+6dB
NC
X2fs
ZEROX
MICON
MCK
LRCK
BCK
ADATA3
ADATA1
SDATA
SCLK
DA2CSX
DA3CSX
GND
VADI-ADRESS-BUS
IC302
HY57V161610DTC
or MB811171622A
or GM72V161621CT
16M-S-DRAM
CN302
NC
DGND
DGND
VDD3.3V
VDD3.3V
VSYNCI
HSYNCI
BLANKI
RGBSX
CVSX
PCLP
S1


R656-28US
R656-18US
IC306
ADV7170
VIDEO-ENCORDER
IC307
NJU6321PXE
IC308
TC7W04F
IC617
TC7W241FU
CN301
52808-1310
I/P-CONVERTER
I/F
VIDEO-SIGNAL
I/F
POWER-SUPPLY
CN801
WP0814
VCC+5V
E+5V
VDD+5V
M+8V
VSYNCX
BLANKX
TBFCSX2
TP307
EX-HSYNC
TP308
EXVSYNC
TP309
GND
BLANKI
RGBSX
CVSX
PCLP
S1
I2C-CLK
I2C-DATA
27MHz
FIO
FI1
RSTX
DC+12V
NTPALX
DGND
Y-OUTPUT
Cb-OUTPUT
C-OUTPUT
Cr-OUTPUT
PWON
VCC+6V
VDD+3V
MGND
VKK-24V
F-
F+
E
F
G
H
10
11
12

4-1. Output Circuit Diagram

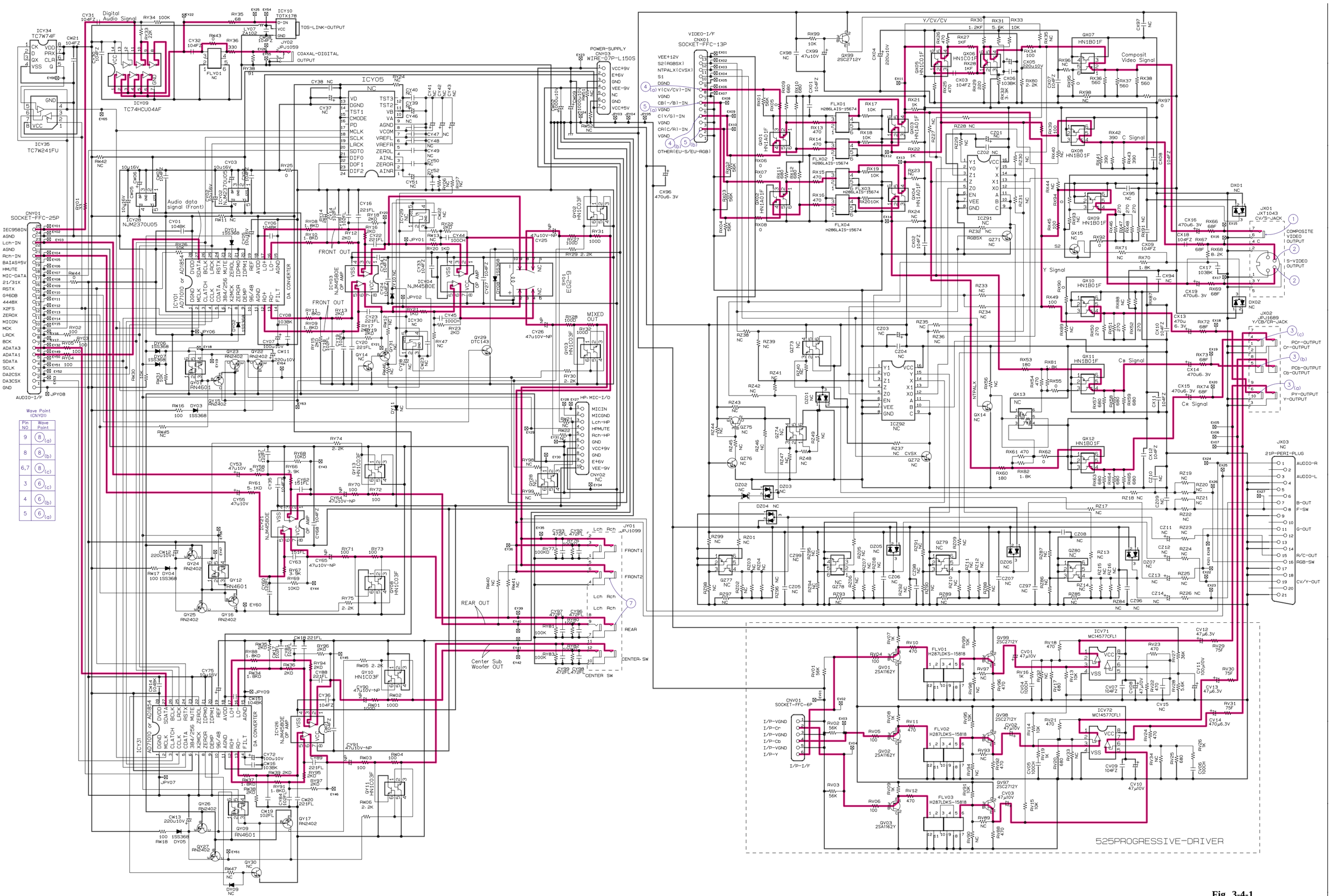
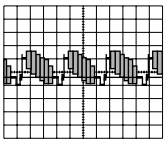


Fig. 3-4-1

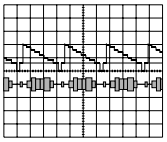
① JX01 Composite video output C-16



CVBS output
75Ω terminated
100% color bar

V: 500 mV/div
H: 20 μs/div

② JX01 S-video output D-16



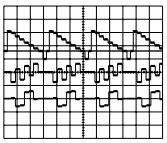
Y
C

S-Y/C
75Ω terminated
100% color bar

V: 500 mV/div
H: 20 μs/div

③ JX02 Y/CB/CR output E-16

(a) Pin ⑥ (Y)
(b) Pin ⑤ (Cb)
(c) Pin ④ (Cr)



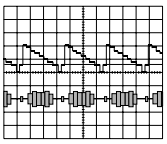
(a)
(b)
(c)

Component output
75Ω terminated
100% color bar (Play)

V: 500 mV/div
H: 20 μs/div

④ CNX01

(a) Pin ⑧ (Y) B-8
(b) Pin ④ (C) C-9



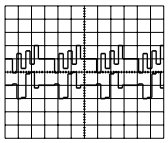
(a)
(b)

100% color bar (Play)

V: 1 V/div
H: 20 μs/div

⑤ CNX01

(a) Pin ⑥ (CB) B-8
(b) Pin ② (CR) C-9



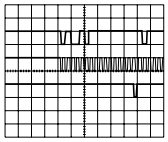
(a)
(b)

100% color bar (Play)

V: 1 V/div
H: 20 μs/div

⑥ CNY01

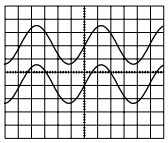
(a) Pin ③ (S DATA) G-1
(b) Pin ④ (S CLOCK) G-1
(c) Pin ⑤ (DA2CSX) G-1



(a)
(b)
(c)

V: 5 V/div
H: 20 μs/div

⑦ JY01 L ch output / R ch output H-8



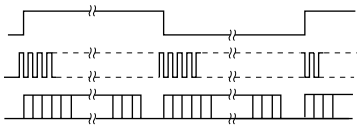
L ch output

R ch output

V: 2 V/div
H: 200 μs/div

⑧ CNY01

(a) Pin ⑨ (LRCK) F-1
(b) Pin ⑧ (BCK) F-1
(c) Pin ⑦ (ADATA3) F-1
⑥ (ADATA1) F-1



(a)
(b)
(c)

Fig. 3-4-2

IC

ICY01
DA CONVERTER

1	0
2	2.5
3	4.9
4	3.2
5	3.5
6	0
7	0
8	0
9	0
10	0
11	0
12	2.3
13	2.4
14	2.4
15	0
16	2.4
17	2.3
18	4.9
19	3.3
20	0
21	0
22	0
23	0
24	4.9
25	2.4
26	2.4
27	1.3
28	4.9

ICY02
REGURATOR

1	6.5
2	0
3	1.2
4	4.9
5	6.5

ICY03
OP AMP

1	4.9
2	4.9
3	4.9
4	4.9
5	4.9
6	4.9
7	4.9
8	9.2

ICY04
OP AMP

1	4.9
2	4.9
3	4.9
4	0
5	4.9
6	4.9
7	4.9
8	9.2

ICY09
INVERTER

1	2.5
2	2.5
3	2.5
4	2.5
5	2.5
6	2.5
7	0
8	2.5
9	2.5
10	2.5
11	2.0
12	2.6
13	2.0
14	4.9

ICY21
OP AMP

1	4.9
2	4.9
3	4.9
4	0
5	4.9
6	4.9
7	4.9
8	9.2

ICY31
DA CONVERTER

1	0
2	2.5
3	4.9
4	3.2
5	3.5
6	0
7	0
8	0
9	0
10	0
11	0
12	2.3
13	2.4
14	2.4
15	0
16	2.4
17	2.3
18	4.9
19	3.3
20	0
21	0
22	0
23	0
24	4.9
25	2.4
26	2.4
27	1.3
28	4.9

ICY26
OP AMP

1	4.9
2	4.9
3	4.9
4	0
5	4.9
6	4.9
7	4.9
8	9.2

ICY28
REGURATOR

1	6.5
2	0
3	1.2
4	4.9
5	6.5

ICY34
D-FLIP-FLOP

1	2.6
2	2.5
3	2.5
4	0
5	2.5
6	4.9
7	4.9
8	4.9

ICY35
3-STATE
BUFFER

1	0
2	0
3	0
4	0
5	0
6	2.5
7	4.9
8	4.9

Transistor

QY01
SWITCH

1	4.9
2	4.9
3	4.9
4	0
5	0
6	0

QY02
SWITCH

1	0
2	0
3	0
4	0
5	0
6	0

QY03
SWITCH

1	0
2	0
3	0
4	0
5	0
6	0

QY08
SWITCH

1	0
2	0
3	0
4	0
5	0
6	0

QY09
SWITCH

1	4.9
2	4.9
3	4.9
4	0
5	0
6	0

QY10
SWITCH

1	0
2	0
3	0
4	0
5	0
6	0

QY11
SWITCH

1	0
2	0
3	0
4	0
5	0
6	0

QY12
SWITCH

1	4.9
2	4.9
3	4.9
4	0
5	0
6	0

QY13
SWITCH

1	0
2	0
3	0
4	0
5	0
6	0

QX01
BUFFER

1	1.8
2	1.1
3	0
4	2.1
5	1.4
6	0

QX02
BUFFER

1	2.1
2	1.4
3	0
4	2.1
5	1.4
6	0

QX03
BUFFER

1	2.7
2	2.0
3	0
4	2.4
5	1.7
6	0

QX04
BUFFER

1	2.7
2	2.0
3	0
4	2.7
5	2.0
6	0

QX05
BUFFER

1	9.2
2	2.7
3	2.1
4	9.2
5	2.4
6	1.8

QX06
MIX AMP
BUFFER

1	9.2
2	1.6
3	1.0
4	6.0
5	6.0
6	5.5

QX07
DRIVER

1	Ð
2	5.4
3	9.2
4	4.7
5	5.4
6	0

QX08
DRIVER

1	3.4
2	2.7
3	0
4	0
5	0
6	0

QX09
DRIVER

1	3.1
2	2.4
3	0
4	0
5	0
6	0

QX10
SWITCH

1	3.1
2	2.4
3	0
4	0
5	0
6	0

QX11
DRIVER

1	2.6
2	2.6
3	0
4	0
5	0
6	0

QX12
DRIVER

1	2.6
2	2.0
3	0
4	0
5	0
6	0

QY15
SWITCH

E	4.9
C	0
B	4.9

QY16
SWITCH

E	4.9
C	0
B	4.9

QY17
SWITCH

E	4.9
C	0
B	4.9

QY22
SWITCH

E	4.9
C	0
B	4.9

QY23
SWITCH

E	4.9
C	0
B	4.9

QY24
SWITCH

E	4.9
C	0
B	4.9

QY25
SWITCH

E	4.9
C	0
B	4.9

QY26
SWITCH

E	4.9
C	0
B	4.9

QY27
SWITCH

E	4.9
C	0
B	4.9

QY29
SWITCH

E	0
C	0
B	4.7

Output Circuit Diagram (With Sub Output Circuit)

Sub output circuit is provided depending on units. For more information, please refer to the circuits below.

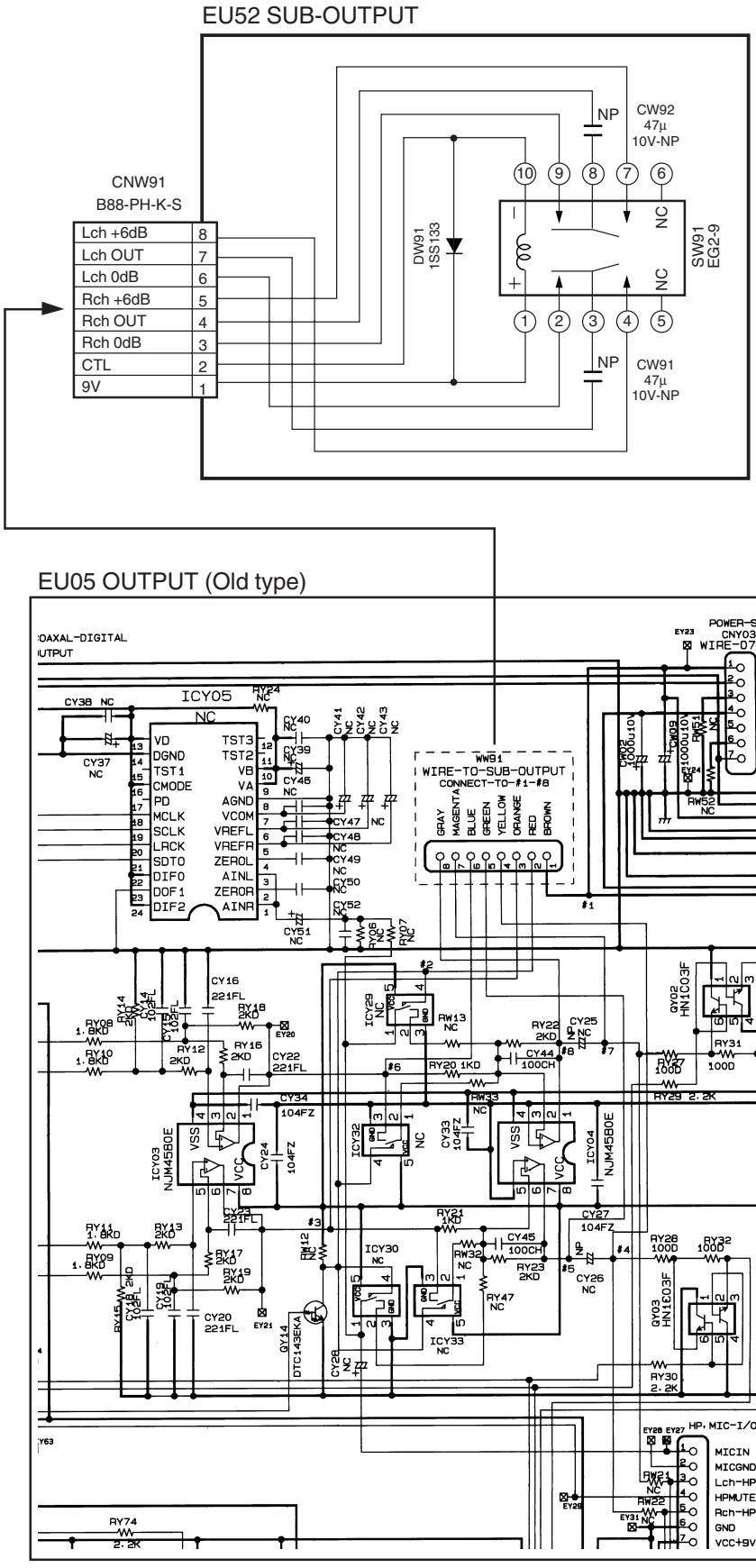


Fig. 3-5-8

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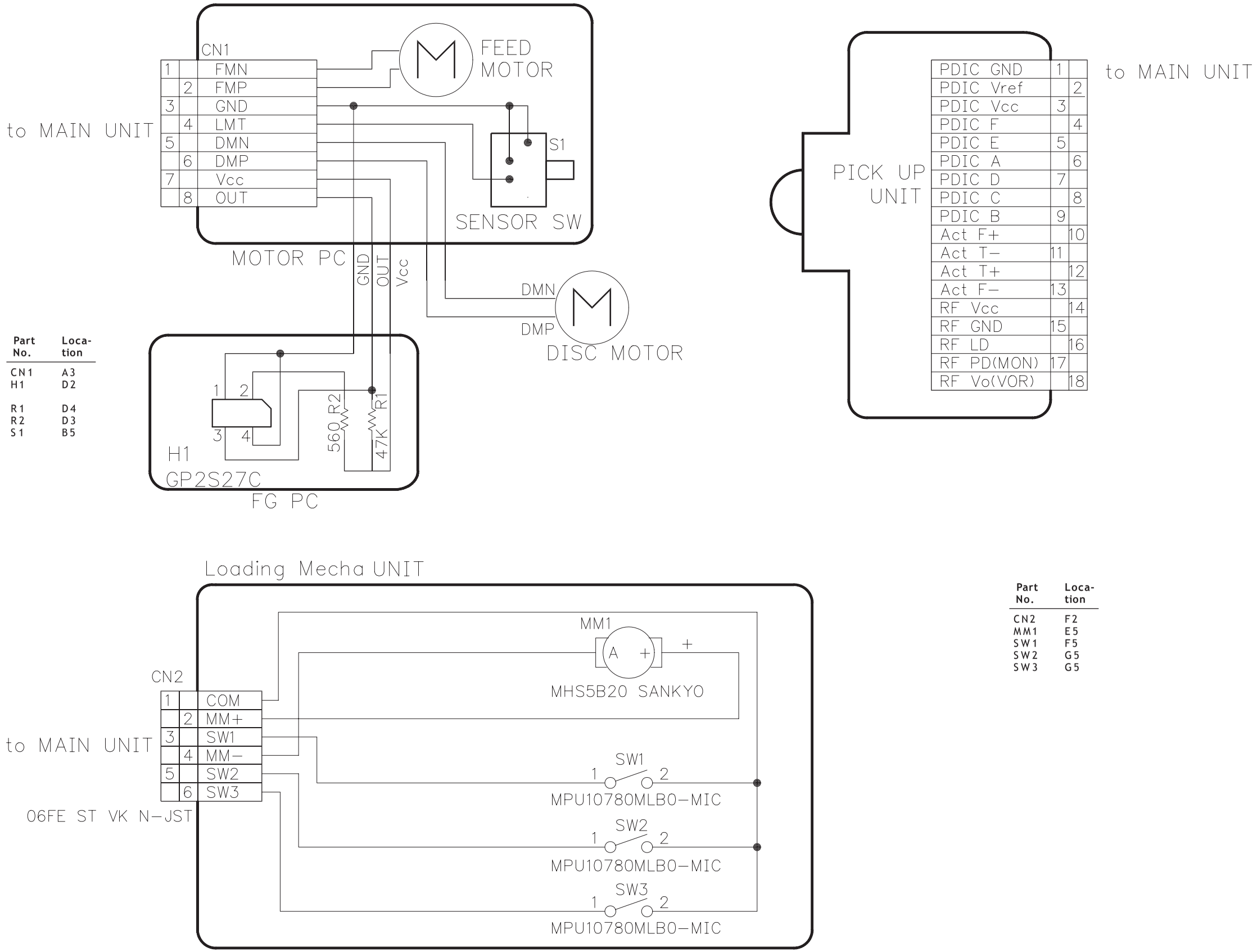
5-5. Motor System Circuit Diagram



Part No.	Location
CN1	A3
H1	D2
R1	D4
R2	D3
S1	B5

Part No.	Location
CN2	F2
MM1	E5
SW1	F5
SW2	G5
SW3	G5

Fig. 3-5-9

SECTION 4
PARTS LIST

SAFETY PRECAUTION

The parts identified by ⚠mark are critical for safety. Replace only with part number specified.

The mounting position of replacement is to be identical with originals.

The substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire or other hazards.

NOTICE

The part number must be used when ordering parts in order to assist in processing, be sure to include the model number and description.

Parts marked # are of chip type and mounted on original PC boards.

However, when they are placed for servicing works, use discrete parts listed on the parts list.

ABBREVIATIONS

1. Integrated Circuit (IC)

2. Capacitor (Cap)

- **Capacitance Tolerance (for Nominal Capacitance more than 10pF)**

Table 4-2-1

Symbol	B	C	D	F	G	J	K	M	N
Tolerance %	± 0.1	± 0.25	± 0.5	± 1	± 2	± 5	± 10	± 20	± 30

Symbol	P	Q	T	U	V	W	X	Y	Z
Tolerance %	+ 100 0	+ 30 – 10	+ 50 – 10	+ 75 – 10	+ 20 – 10	+ 100 – 10	+ 40 – 20	+ 150 – 10	+ 80 – 20

Ex. 10µF J = 10µF ± 5%

- **Capacitance Tolerance (for Nominal Capacitance 10pF or less)**

Table 4-2-2

Symbol	B	C	D	F	G
Tolerance pF	± 0.1	± 0.25	± 0.5	± 1	± 2

Ex. 10pF G = 10pF ± 2pF

3. Resistor (Res)

- **Resistance tolerance**

Table 4-3-1

Symbol	B	C	D	F	G	J	K	M
Tolerance %	± 0.1	± 0.25	± 0.5	± 1	± 2	± 5	± 10	± 20

Ex. 470ΩJ = 470Ω± 5%

4. EXPLODED VIEWS

4-1. Packing Assembly

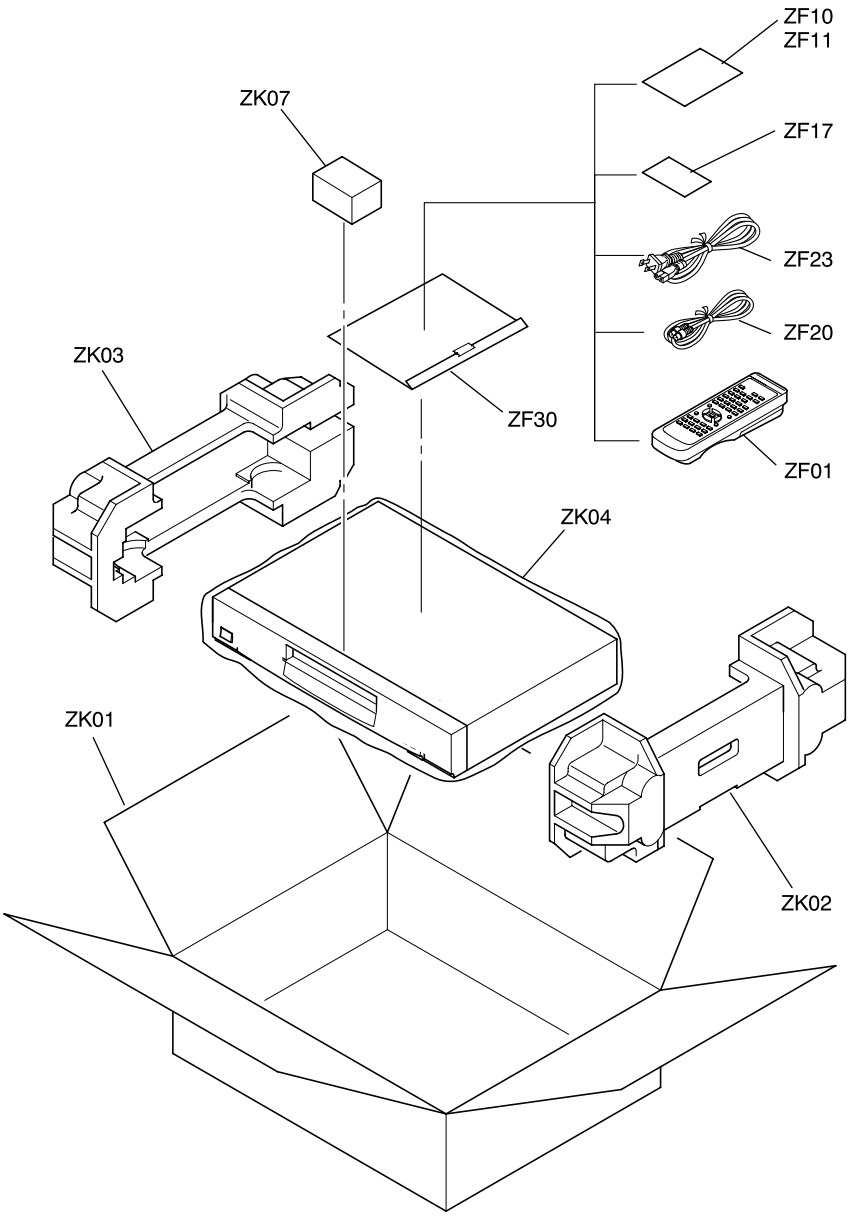


Fig. 4-4-1

4-2. Chassis Assembly

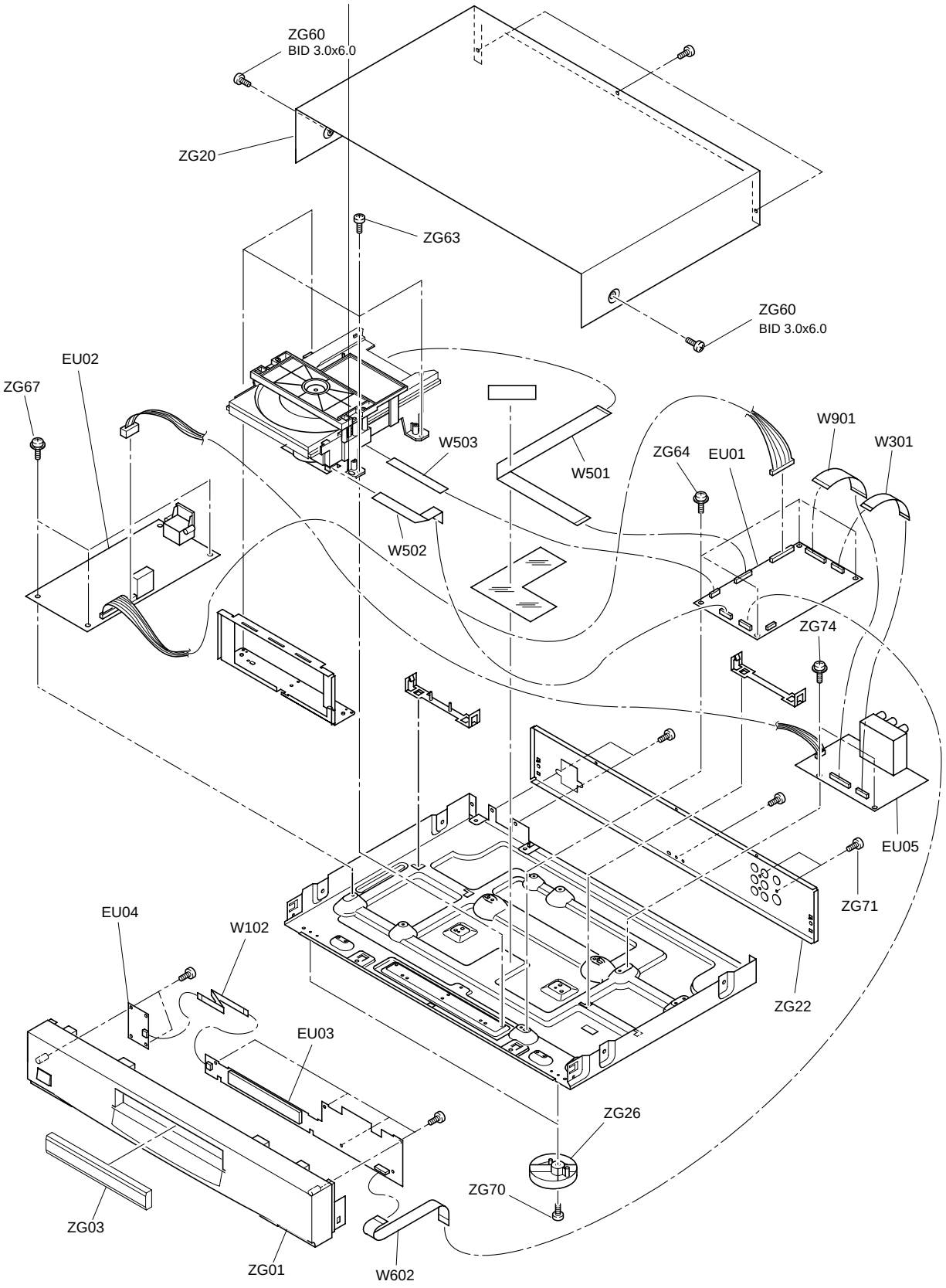


Fig. 4-4-2

4-3. Mechanism Assembly

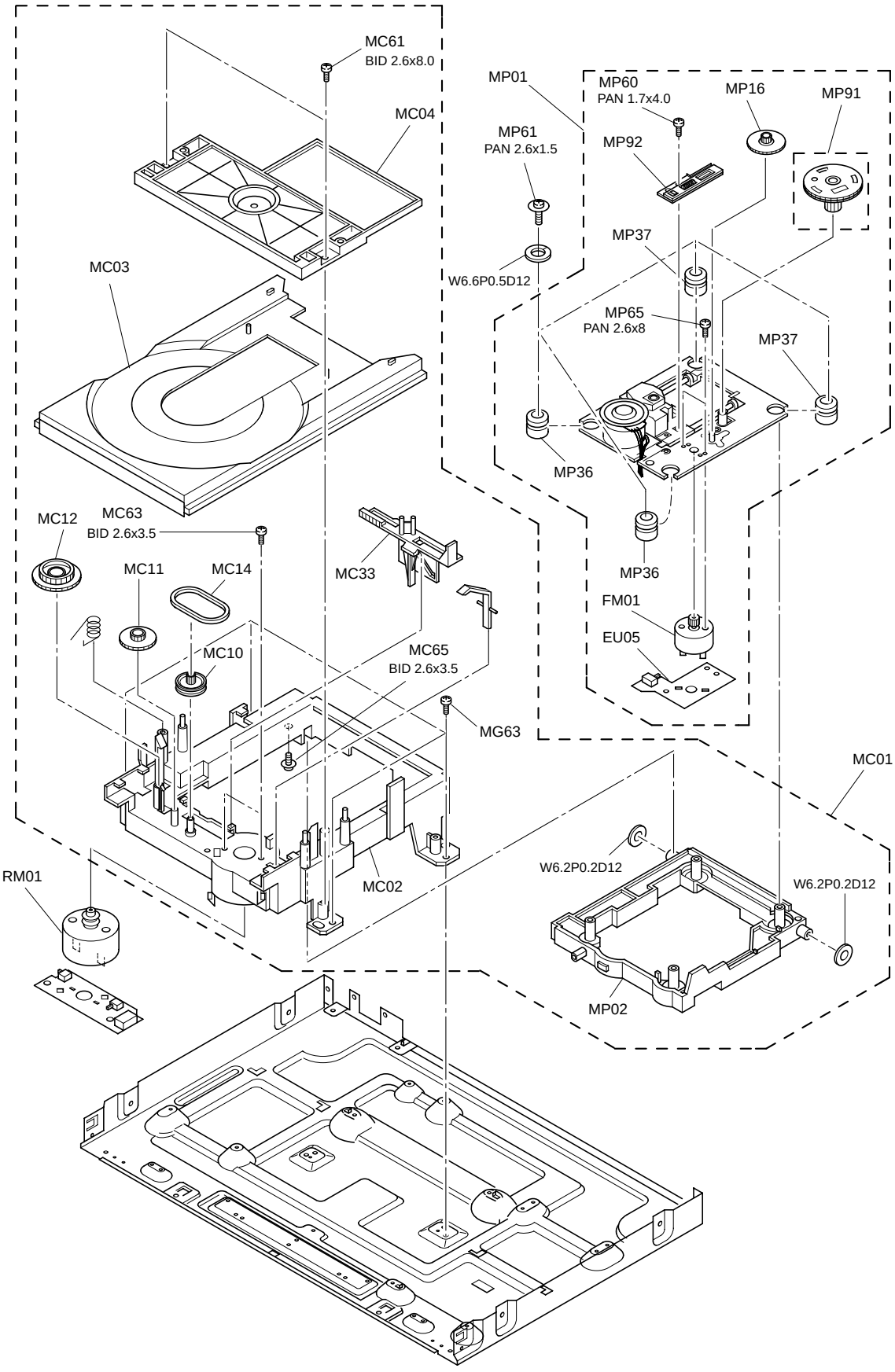


Fig. 4-4-3

5. PARTS LIST

DD-6000 Parts List

Part Number	Description
79070428	BELT-LOAD
79080197	CABLE (13 pin main-assy front)
79080194	CABLE (13 pin main-assy output)
79080145	CABLE (18 pin assy front-assy power sw)
79080191	CABLE (18 pin main-mechanism)
79080196	CABLE (25 pin main-output)
79080192	CABLE (6 pin main-chassis mech)
79080182	CABLE (6 pin)
79080193	CABLE (8 pin main-chassis)
79070037	CABLE-AV
79070049	CABLE-S
79070416	CHASSIS ASSY MECHANISM
79088007	CORD-POWER
79050041	COUPLER-PHOTO (TLP621)
79073035	COVER-TOP
79089034	DISPLAY FL
79080055	FILTER-LINE
79073038	FOOT,ASSY FRONT
79087002	FUSE-(1.6A/250)
79070055	FUSE-(125V 2.0A)
79070061	FUSE-(125V 3.0A)
79070422	GEAR A
79070420	GEAR-RACK ASSY
79040105	IC-BA10324A
79040147	IC-STR-G6651LF1105
79040146	IC-TA76431S
I/B DD6000	I/B DD6000
79089023	JACK,AC INLET
79080074	KIT-DATA UPDATE
79070419	KIT-GEAR B ASSY
79060035	LED
79070415	MECHA-PU ASSY
79089035	MODULE, REMOTE
79070421	MOTOR-ASSY, FEED
79070427	MOTOR-ASSY, LOADING
79071099	PANEL-FRONT
79071076	PANEL-TRAY
79081034	PCB-FRONT ASSY
79083040	PCB-MAIN (T/A REQUIRED)
79085038	PCB-OUTPUT (T/A REQUIRED)
79085017	PCB-POWER (T/A REQUIRED)
79086007	PCB-PROGRESSIVE (T/A REQUIRED)
79081033	PCB-SWITCH POWER
79089018	RELAY, DS9D2-0S
79080018	RELAY, EG2-9
79078023	REMOTE
79030054	Res, Fusible 1 ohm J 1/4W
79050040	TR-2SA1048-Y
79050036	TR-2SA1832 GR
79050042	TR-2SC2883-Y
79089024	TERMINAL,OPT
79010015	TRANSF-(SRW3020ed5-207)