Service Information

Model: OMS-1/1A/1E (Compact Disc Player)
Serial No.: from –

Subject: Principle of Operation

Nakamichi

No. OOD-SI-3110 (1/36)
Date 31 May 1988

CONTENTS

1. Introduction

Fig. 1 shows the block diagram of the OMS-1, and Fig. 2 shows its timing chart. Though being Nakamichi low-cost version CD player, the OMS-1 incorporates a variety of technology developed for Nakamichi's high-grade models and demonstrates high-grade sound quality.

The OMS-1 employs a 3-beam laser pickup. In circuit construction, third-generation LSIs particularly developed for CD players, 2-times oversampling digital filter, up-to-date D/A (digital-to-analog) converter technology, and 5th-order active low-pass filter are employed. In mechanism, the floating disc drive with precision centering is adopted for protection against disturbance. Using the Remote Control Unit attached to the OMS-1 enables F. Fwd. and Rev. operation which cannot be executed on the OMS-1 itself.

G-880505A Printed in Japan

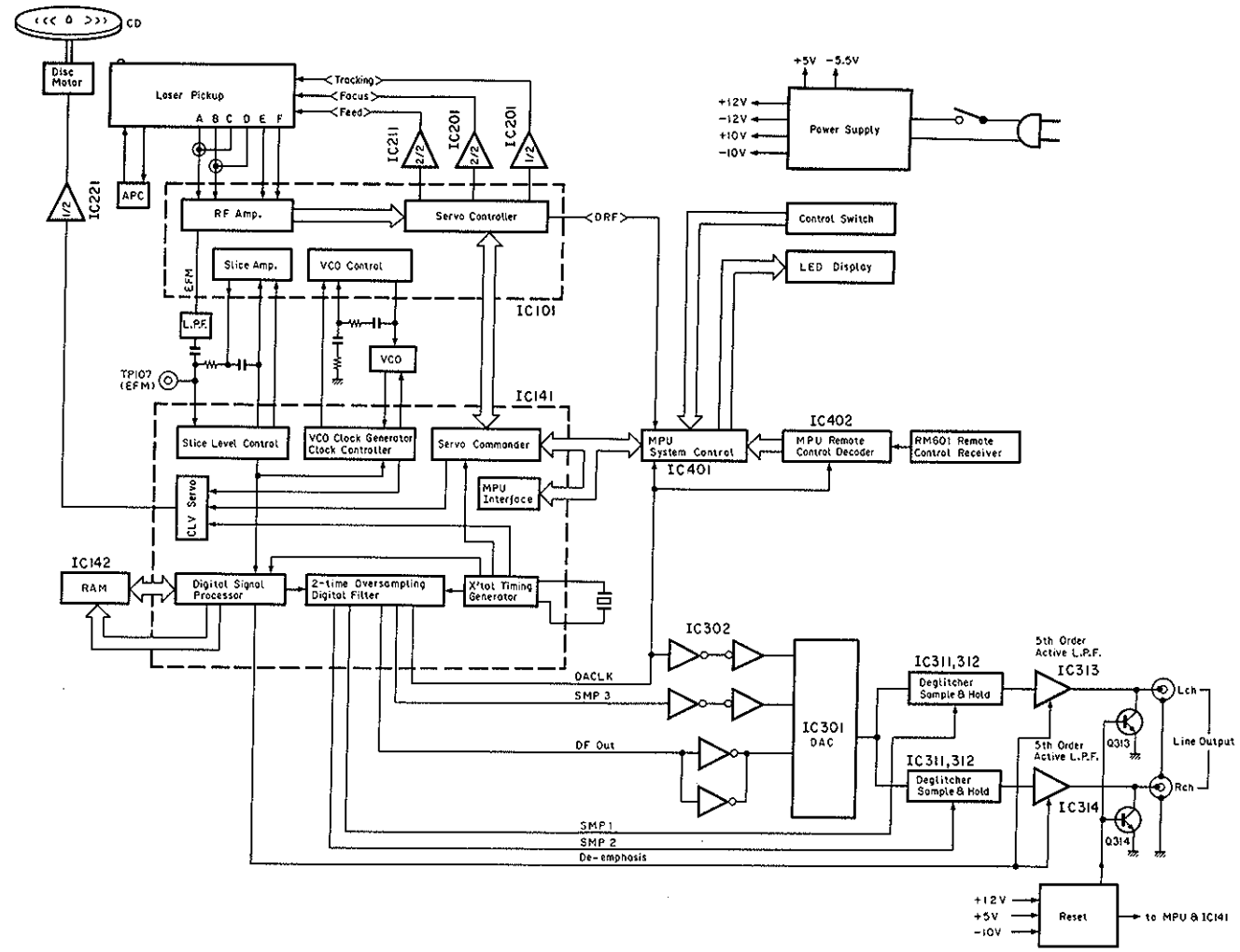
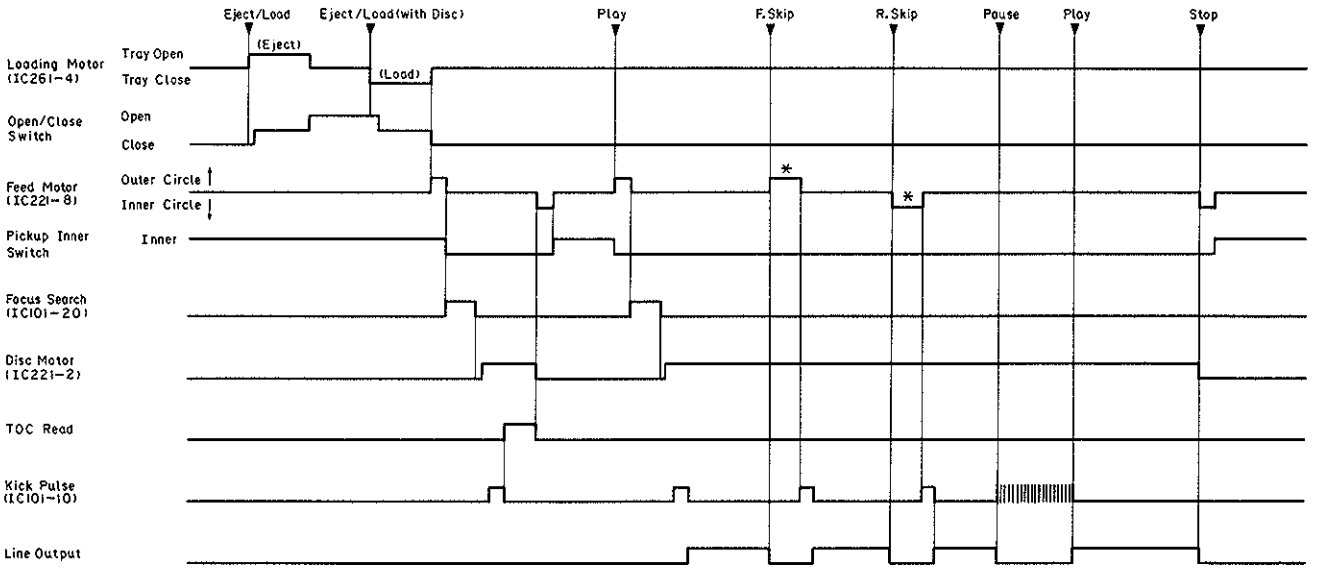


Fig. 1 Block Diagram



Notes: 1. This timing chart starts from Standby mode without putting a disc.
2. Signal marked with * is not a continuous signal.
3. Disc Motor signal shows a CLV servo signal.
4. Kick pulse is a complex signal of JP+ and JP— signals.

Fig. 2 Timing Chart

2. Power Supply Circuit

Fig. 3 shows the power supply circuit of the OMS-1. In the power supply circuit of the OMS-1, the power transformer has two windings on its secondary side. One is used for the digital circuit and another is for the analog circuit to avoid interference between the digital and analog circuits.

Ground lines of the digital circuit and analog circuit are connected contiguous to a point where the power transformer is connected to the Main P.C B. Ass'y. The P.C.B. patterns are also designed to eliminate interference between ground lines following the connection point. The DC power supply for the digital circuit provides non-regulated ±12 V as well as regulated +5 V and −5.5 V. The DC power supply for the analog circuit provides regulated ±10 V.

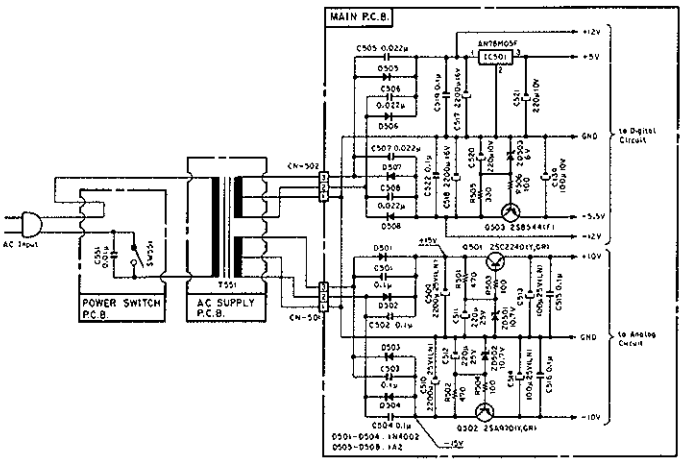


Fig. 3 Power Supply Circuit

3. Control System

Two MPUs (microprocessing units; IC401 and IC402) are incorporated on the Main P.C.B. Ass'y of the OMS-1. Fig. 4 shows the keyboard and display control circuit. IC401 (LC6520H-3527) on the Main P.C.B. Ass'y is an MPU for system control. IC402 (LC6528C-3509) receives and decodes command signals sent by the Remote Control Unit RM-1CD, and then transmits them to IC401. Each command entered from the key is input into IC401 to select each mode.

IC401 outputs display control signal corresponding to each mode to turn ON the LED on the Control P.C.B. Ass'y.

Fig. 5 shows the system control circuit.

IC401 decodes signals entered from keys on the Control P.C.B. Ass'y, and transmits them to the Digital Signal Processor IC (IC141; LC7860N).

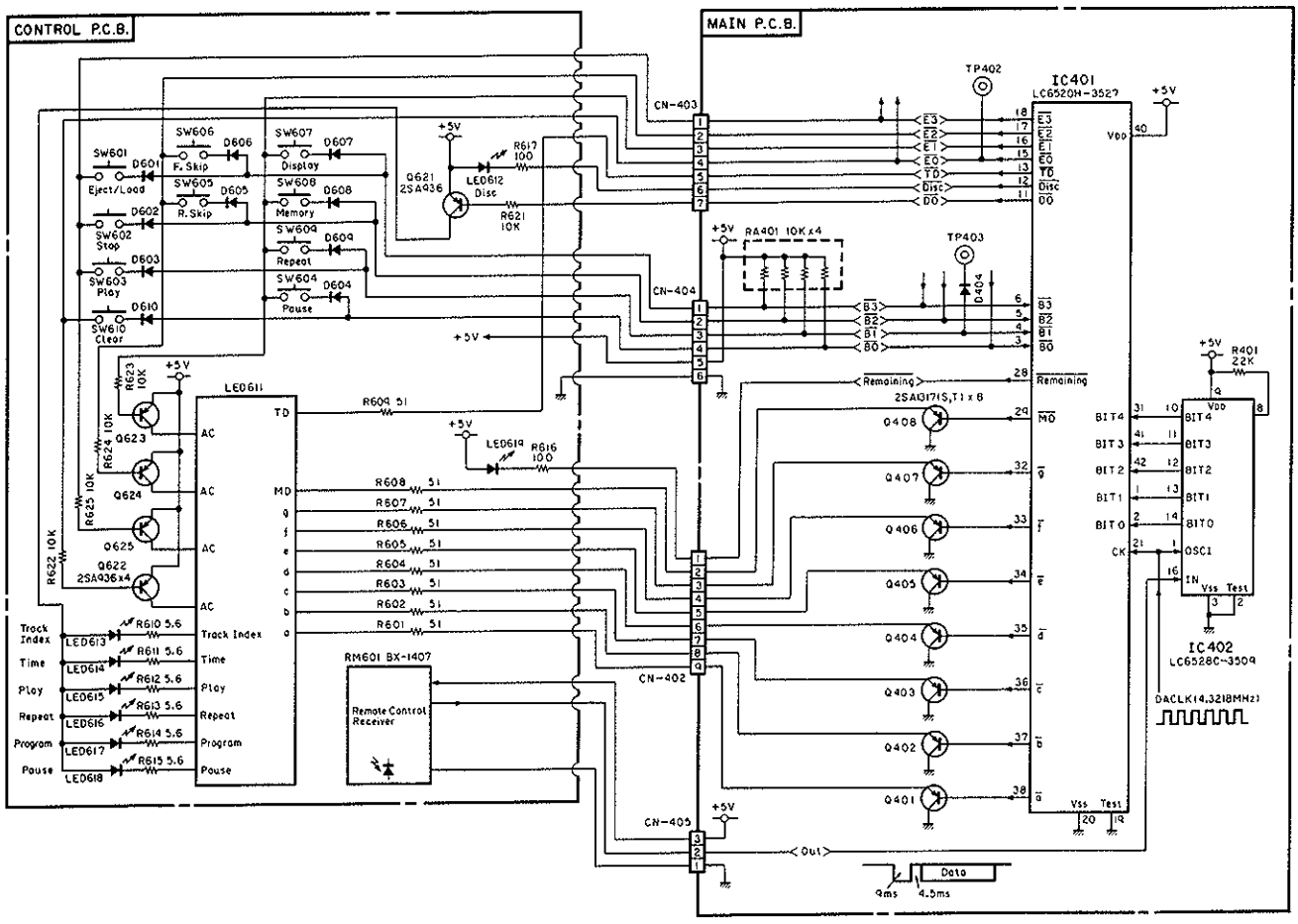


Fig. 4 Keyboard and Display Control Circuit

The servo commander in IC141 is controlled by $\overline{\text{CQCK}}$ (IC401-26), COIN (IC401-25), and RWC (IC401-30) output by IC401.

8-bit 1-word data is output from COIN of IC401 synchronously with $\overline{\text{CQCK}}$ when RWC is set to "H". This data is output in LSB first order.

Four kinds of commands are output from IC401. They are Focus Start command, Disc Motor command, Track Jump command, and Mute command. Table 1 shows command codes.

Fig. 6 shows the timing chart of RWC, $\overline{\text{CQCK}}$, and COIN.

The command is executed from trailing edge of RWC. As Mute and Disc Motor commands are latched to the registers, the command type varies according to the other commands input. When IC401 and IC141 are reset by $\overline{\text{Reset}}$ signal, Mute command is $-\infty$ dB and Disc Motor command is in Stop mode.

Although approximate 25ms is needed for execution of the Track Jump command, the next Track Jump command can be given during execution of the previous one. The Focus Start command requires more time, but other commands cannot be input during execution of this command. Thus when more than one command is to be input, the Mute or Disc Motor command is input first followed by input of the Focus Start or Track Jump command.

DACLK (4.3218 MHz) generated by the crystal timing generator in IC141 is input into clock circuits of IC401 and IC402. IC401, IC402, and IC141 are reset by the $\overline{\text{Reset}}$ signal generated when the Power switch of the OMS-1 is turned ON or OFF.

Table 1 Command Codes

MSB Code LSB	Command
00000000	Nothing
00010001	1 Track Jump In #1
00010010	1 Track Jump In #2
00010011	4 Track Jump In
00010100	16 Track Jump In
00010101	64 Track Jump In
00011001	1 Track Jump Out #1
00011010	1 Track Jump Out #2
00011011	4 Track Jump Out
00011100	16 Track Jump Out
00011101	64 Track Jump Out
00010110	256 Track Check
00000001	Mute 0 dB
00000010	Mute −12 dB
00000011	Mute $-\infty$ dB
00000100	Disc Motor Start
00000101	Disc Motor CLV
00000110	Disc Motor Brake
00000111	Disc Motor Stop
00001000	Focus Start

#1 JP Pulse width 233 μs + 233 μs.

#2 Switching from acceleration pulse to deceleration pulse is made by detecting the intermediate point of the track.

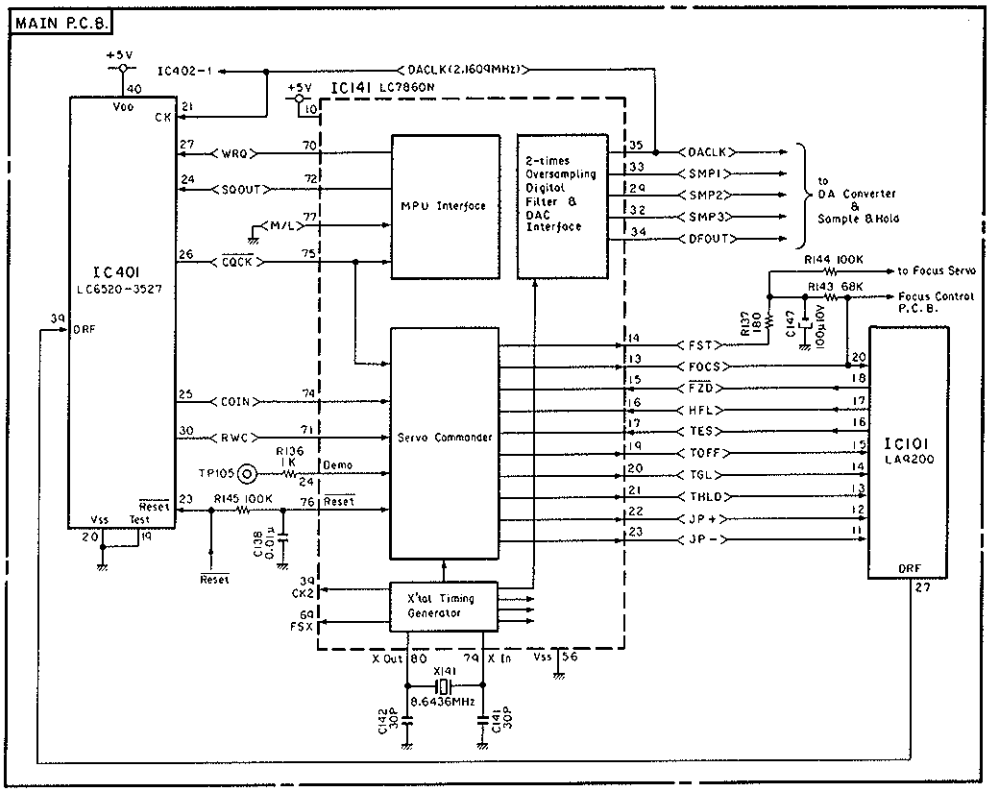


Fig. 5 System Control Circuit

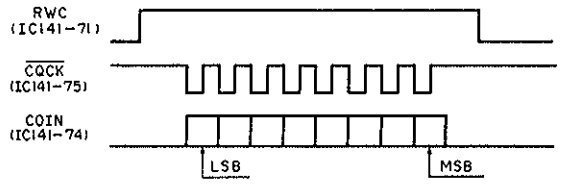


Fig. 6 Servo Command Timing (from IC401)

Fig. 7 shows the wireless remote control receiver circuit.

This is a circuit for receiving commands sent from the Remote Control Unit RM-1CD. Signals are received by photodiode D1 (PH302B) in the remote control receiver unit RM601 (BX-1407), and amplified through current-to-voltage conversion by the head amplifier section in IC CX20106A.

Then, the limiter amplifier section limits surplus parts of signal waves, and the band-pass filter whose center frequency is 40 kHz suppresses out-of-band noise component. Then, the detector detects signal component, the integrator integrates it, and the hysteresis comparator outputs rectangular waveform command signal. Fig. 8 shows output waveform at pin 7 of CX-20106A.

Then, the waveform is input into pin 16 of IC402 and decoded. Decoded command signal is transmitted to IC401 to control the OMS-1.

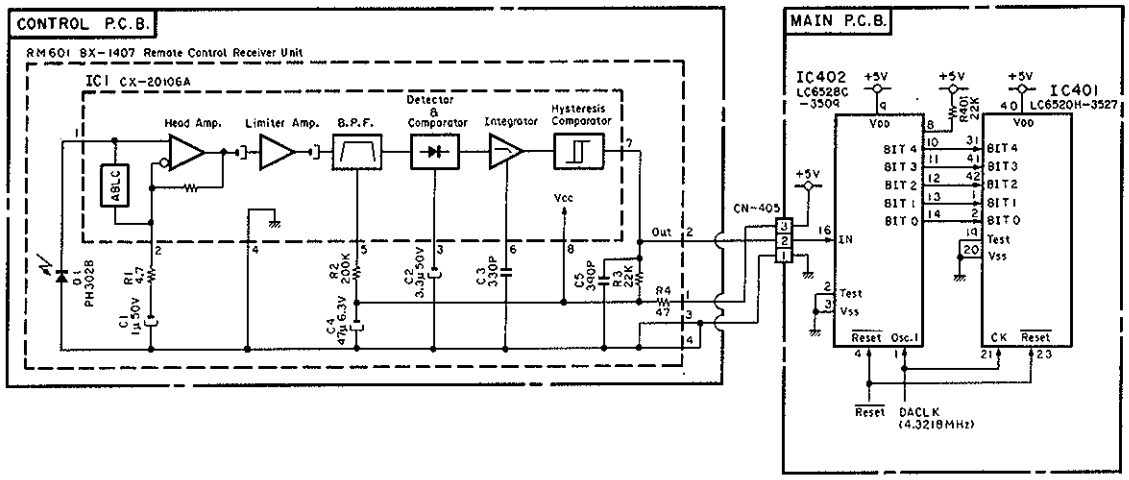


Fig. 7 Wireless Remote Control Receiver Circuit

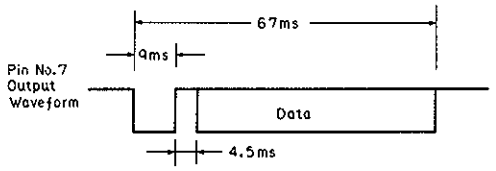


Fig. 8 Wireless Remote Control Receiver Output

4. Reset Circuit

Fig. 9 shows the reset circuit of the OMS-1.

This circuit is provided to prevent MPUs and IC141 from malfunctioning as well as to prevent any noises from being output from line output terminals when the Power switch of the OMS-1 is turned ON or OFF.

Setting the OMS-1's Power switch to ON rises the power supplies in the DC power supply of the Main P.C.B. Ass'y. When +12 V is output, emitter voltage of Q531 reaches approx. 6 V. Since base voltage of Q531 is lower than the emitter voltage while C533 is being charged, Q531 is turned ON during the charging.

When Q531 is turned ON, Q313 and 314 are turned ON to mute line output terminals. When Q531 is turned ON and its collector voltage exceeds 3 V, ZD141 is turned ON, Q141 is turned ON, and the $\overline{\text{Reset}}$ signal = L is input into IC401, IC402, and IC141 to reset them.

When C533 has been charged, base voltage of Q531 reaches approx. +6 V; consequently, Q531 is cut off and collector voltage of Q531 lowers up to approx. −5 V. By this, Q141 is cut off, and IC401 and IC402 are released from the reset state after C154 has been charged. Further, IC141 is released from the reset state after C138 has been charged. Now the OMS-1 is ready for operation.

When the Power switch is turned OFF, C533 is immediately discharged through D532. Since emitter voltage of Q531 is approx. +6 V by voltage charged in C532, Q531 is turned ON, and its collector voltage rises up to approx. +6 V. Thus, similarly to turning ON the Power switch, $\overline{\text{Reset}}$ signal = L is applied to IC401, IC402, and IC141, and line output terminals are muted.

Fig. 10 shows the timing chart of the reset circuit.

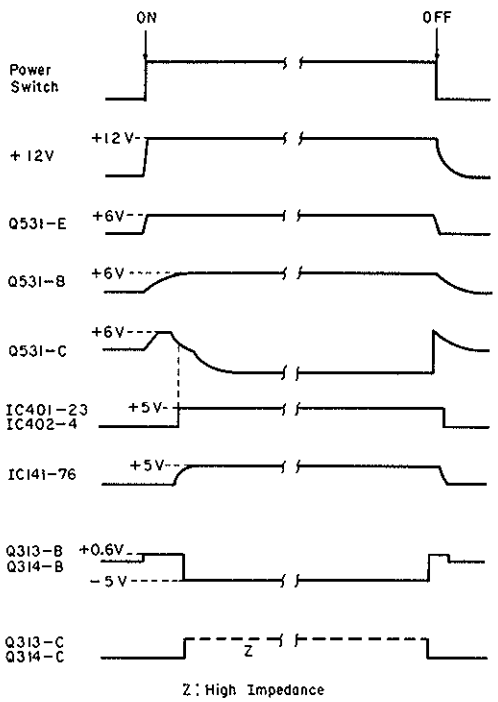


Fig. 10 Reset Timing Chart

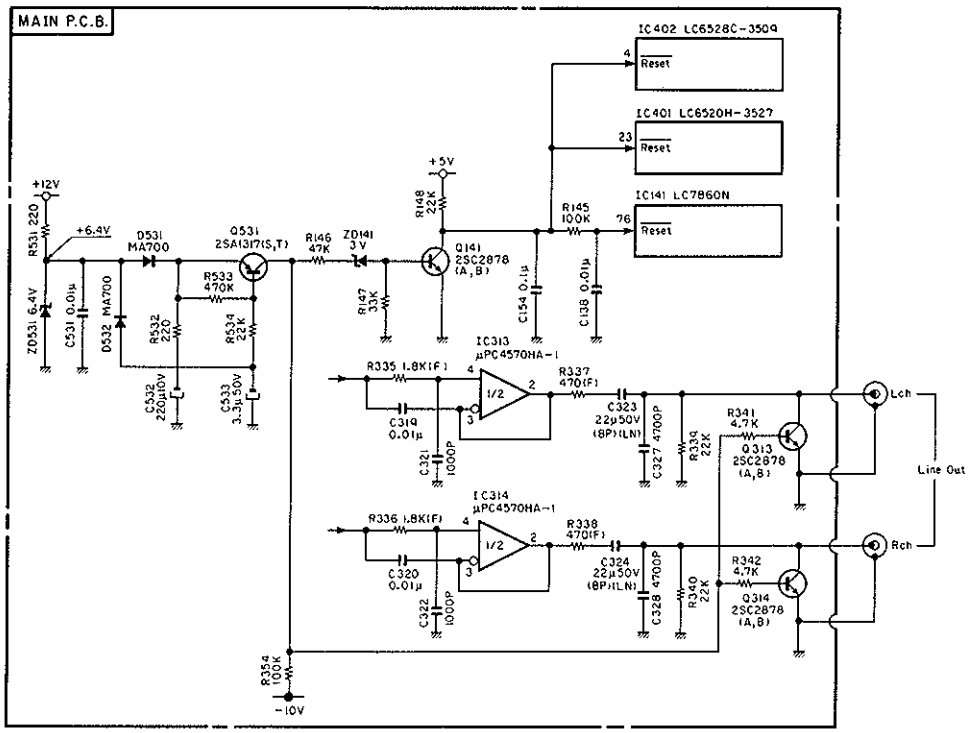


Fig. 9 Reset Circuit

5. Eject/Load Operations

Eject/load operations take place when a CD is loaded or unloaded.

Fig. 11 shows the eject/load circuit.

Usually, eject/load operations are triggered by press of the Eject/Load button on the Front Panel Ass'y.

When loading a CD, however, the Play button may be pressed to permit direct operation. In this case, the Play mode is automatically entered after loading.

(1) Eject Opeation

Pressing the Eject/Load button with the Disc Tray Ass'y closed starts eject operation and moves the Disc Tray Ass'y out. Upon press of the Eject/Load button, the signal $\overline{\text{Eject/Load}}$ = L is input to pin 6 of the IC401 (LC6520H-3527) on the Main P.C.B. Ass'y.

Receiving the signal $\overline{\text{Eject/Load}}$ = L, IC401 outputs "H" from pin 8 (LM−). Since this upsets the input balance of IC261 (LA6500), positive voltage is output at pin 4 of IC261. The Loading Motor is applied with approx. +4.5 V, so it rotates in the reverse direction to move the Disc Tray Ass'y out. When the outward movement of the Disc Tray Ass'y actuates the Open/Close switch, the signal $\overline{\text{Open}}$ = L is input to pin 6 of IC401 and pin 9 (LM+) changes from "H" to "L". Because the input balance of IC261 is now restored, the Loading Motor stops, and the eject operation is over with the Disc Tray Ass'y left out. The eject operation can be entered from any mode. Fig. 12 shows the timing chart of the eject operation.

(2) Load Operation

Refer to Figs. 13 and 14.

Pressing the Eject/Load button or the Play button with the Disc Tray Ass'y open starts load operation and closes the Disc Tray Ass'y.

When the Eject/Load button is pressed, the signal $\overline{\text{Eject/Load}}$ = L is input to pin 6 of IC401 on the Main P.C.B. Ass'y.

When the Play button is pressed, the signal $\overline{\text{Play}}$ = L is input to pin 4 of IC401. Upon receipt of this signal, IC401 outputs "H" level from pin 8 (LM−).

Since this upsets the input balance of IC261, a negative voltage is output at pin 4 of IC261. The Loading Motor is applied with approx. −4.5 V, so it rotates in the forward direction to close the Disc Tray Ass'y.

When the closing motion of the Disc Tray Ass'y actuates the Open/Close switch, the signal $\overline{\text{Close}}$ = L is input to pin 5 of IC401, and pin 8 (LM−) changes from "H" to "L" level. Because the input balance of IC261 is now restored, the Loading Motor stops and the Disc Tray Ass'y closes.

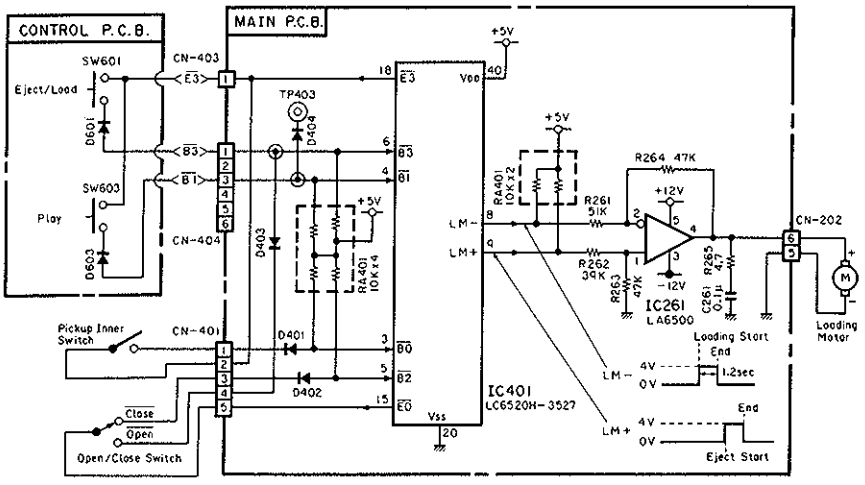


Fig. 11 Eject/Load Circuit

Then, when pin 3 (Pickup Inner) of IC401 is at "H" level, the Feed Motor is rotated, and after the $\overline{\text{Pickup Inner}}$ signal is changed to "L", the Read-In area is read to terminate the load operation.

If the $\overline{\text{Pickup Inner}}$ signal is already at "L" level, the Feed Motor is rotated slightly to make the pickup direction forward, so that the $\overline{\text{Pickup Inner}}$ signal is set to "H" level. Then the Feed Motor is rotated in the reverse direction to set the $\overline{\text{Pickup Inner}}$ signal to "L" level. Now the Read-In area is read to terminate the load operation. If the load operation was started with the Play button instead of the Eject/Load button, the Play mode is entered after the load operation.

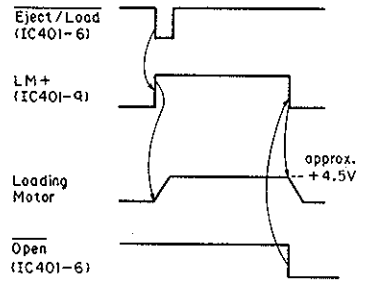


Fig. 12 Eject Timing Chart

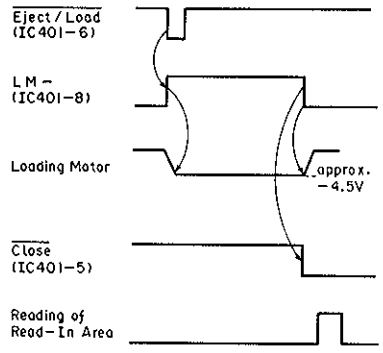


Fig. 13 Loading Timing Chart (When Eject/Load switch is pressed)

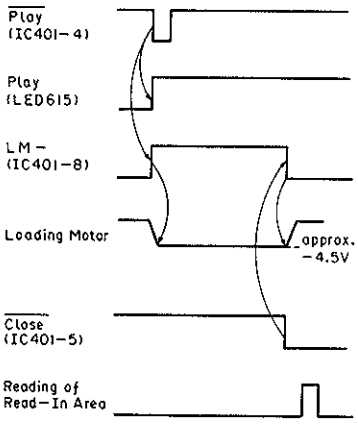


Fig. 14 Loading Timing Chart (When Play switch is pressed)

6. Auto Power Control

Fig. 15 shows the auto power control circuit of the OMS-1 which mounted on the Laser Pickup Ass'y. The auto power control circuit has two functions: (1) control of the laser diode so that the amount of light emission is not affected by temperature changes, etc., and (2) protection of the laser diode against overcurrent.

Overcurrent into the laser diode leads to breakdown or deterioration of the laser diode. The semi-fixed volume is incorporated in the Auto Power Control P.C.B. Ass'y of the Laser Pickup Ass'y. This volume must never be adjusted because it has been exactly adjusted in our factory.

The laser diode of the OMS-1 emits light if:

(1) The Disc Tray Ass'y is loaded.

(2) The OMS-1 is in Play or Pause mode.

However, during reading of the Read-In area at the load time, the laser diode emits light even if the OMS-1 is not in Play or Pause mode.

When the Disc Tray has been loaded, the Open/Close switch on the CD Mechanism Ass'y is switched to close side, so that the signal $\overline{\text{Close}}$ = L is input to pin 5 of IC401. Then, pressing SW603 (Play) or SW604 (Pause) on the Control P.C.B. Ass'y causes input of the signal $\overline{\text{Play}}$ = L or $\overline{\text{Pause}}$ = L to pin 4 or 3 of IC401, so that pin 10 ($\overline{\text{LSON}}$) of IC401 outputs the signal $\overline{\text{LSON}}$ = L. Since the $\overline{\text{LSON}}$ = L signal enters pin 38 ($\overline{\text{LDSW}}$) of IC101 (LA9200), the laser ON/OFF circuit is turned ON and approx. −5.5 V is output at pin 39 (LDD) of IC101. Then this voltage enters the APC (auto power control) circuit and turns ON Q2, Q3, and Q1, so that the laser diode of the Laser Pickup Ass'y emits light.

The amount of light emission from the laser diode is detected by the monitor diode of the Laser Pickup Ass'y and fed back to base of Q2 in the APC circuit. This feedback signal is compared with the −2.3 V reference voltage at emitter of Q2. If the feedback signal is lower than −2.3 V, the current flowing in the laser diode increases. If the feedback signal is higher than −2.3 V, the current flowing in the laser diode decreases. Thus, the laser diode is controlled to emit a constant amount of light.

When pin 10 ($\overline{\text{LSON}}$) of IC401 is set at "H" level, the laser diode does not emit light, because Q2, Q3, and Q1 are cut off.

To measure the current flowing in the laser diode, determine the voltage across R2 (22Ω) in the APC circuit using a DC voltmeter. Then calculate the current from the formula I = V/22.

The timing chart related to laser diode light emission is given in Fig. 16.

For measuring the laser power of the OMS-1, it is not necessary to bring the OMS-1 into Play mode or Pause mode. It can be measured easily only by grounding TP401 on the Main P.C.B. Ass'y, causing the laser diode to emit light.

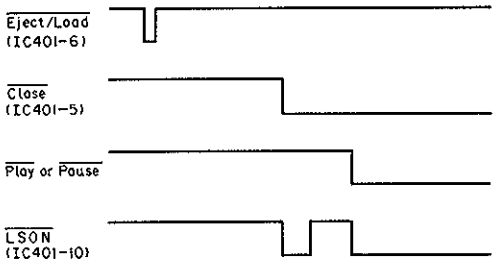


Fig. 16 Laser ON/OFF Timing Chart

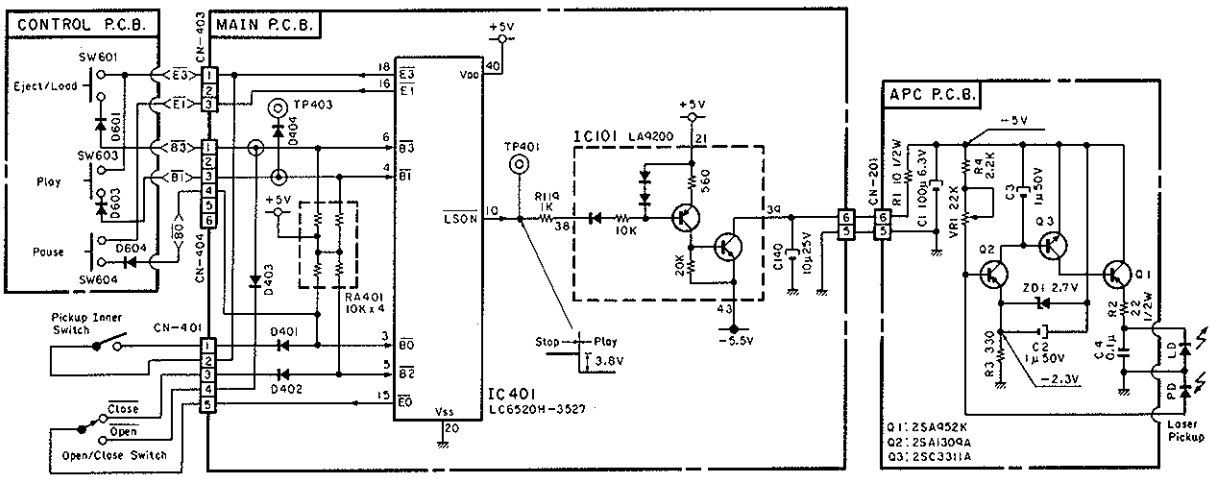


Fig. 15 Auto Power Control Circuit

7. Focus Servo System

Fig. 17 shows a block diagram of the focus servo system. The focus servo has the function of maintaining a fixed distance between the laser pickup's object lens and the CD's signal surface.

As the CD begins rotation, the focus servo shifts the object lens of the laser pickup vertically so that the distance to the signal surface is constant at any given time. The vertical deviation of a CD is specified to be within ±0.5 mm. The focus servo of the OMS-1 uses the astigmatism method. This method is illustrated in Fig. 18 showing the construction and in Fig. 19 showing the principle of operation.

The cylindrical lens shown in Fig. 18 plays an important role in the astigmatism approach. This lens acts as a lens only in one direction (x-direction in Fig. 18), but it does nothing in the other direction (y-direction in Fig. 18). Therefore, at point B, the light is condensed into a vertical (y-direction) line, and at point A, into a horizontal (x-direction) line. An enlarged view of optical path between points A and B is presented in Fig. 19. At the midpoint J between points A and B, the beam takes a circular form. At points nearer to point B (farther from point J), the beam shape becomes a progressively longer ellipse extending in the vertical direction. At points nearer to point A, the beam shape becomes a progressively longer ellipse extending in the horizontal direction.

In the astigmatism method, the object lens is adjusted so that the image of CD's signal surface is formed at point J when the signal surface is on the focal plane of the optical system. With a quarter-split PIN photodiode placed at point J as shown in Fig. 19, the four outputs are arithmetically operated in the formula "(A + C) — (B + D)". The result of this arithmetic operation, which is zero, serves as the focus error signal.

When the CD is nearer to the object lens, the image on the quarter-split photodiode at point J becomes a vertically longer ellipse, giving a positive focus error signal. When the CD is farther from the object lens, the image becomes a horizontally longer ellipse, giving a negative focus error signal. Thus the focus error signal is bipolar.

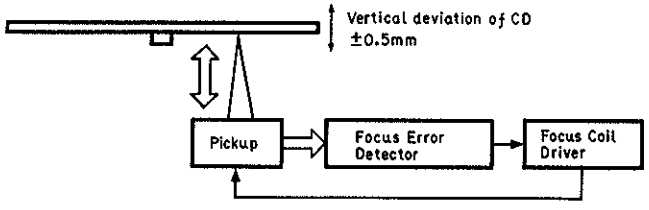


Fig. 17 Focus Servo System Block Diagram

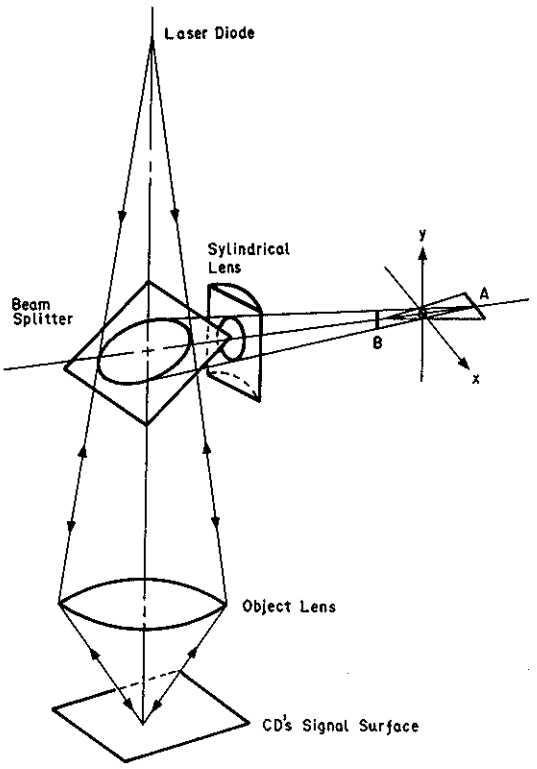
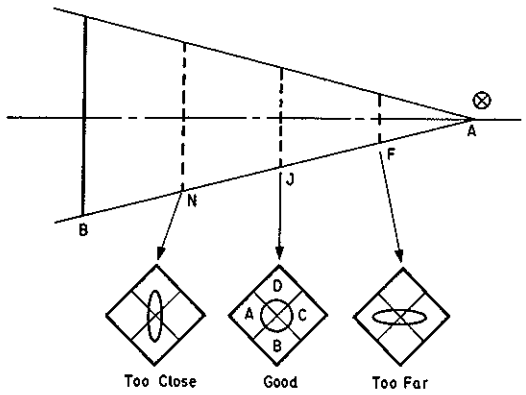


Fig. 18 Astigmatism Method



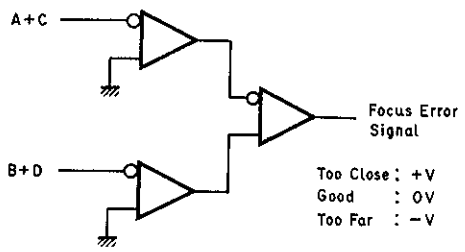


Fig. 19

Fig. 20 shows the focus servo circuit of the OMS-1.
The focus servo circuit of the OMS-1 is located in the Main P.C.B. Ass'y. It consists of IC401 (LC6520H-3257), IC141 (LC7860N), IC101 (LA9200), IC201-2/2 (LA6510), focus control circuit, and peripheral circuitry. The focus servo is controlled primarily by IC401 and IC141.
Fig. 21 shows the RF amplifier circuit for the focus servo and the EFM signal. This circuit performs current-to-voltage conversion of output from the quarter-split photodiode.
Output of the quarter-split photodiode is input into the Main P.C.B. Ass'y first: Through A + C and B + D accumulation it is input into pins 41 and 42 of IC101. IC101 amplifies input signals through current-to-voltage (I – V) conversion. –(A + C) signal and –(B + D) signal processed through current-to-voltage conversion are wired-ORed by resistors of 10 kΩ, inverted and amplified by the RF summing amplifier, and output from pin 36 of IC101 as the EFM signal (A + B + C + D). On the other hand, the I-V processed signals are differentially amplified by the focus error amplifier and output from pin 31 of IC101 as the focus error signal [(A + C) – (B + D)]
In general, the focus servo circuit executes focus searching first. When the focus zero detector signal is detected, focus searching terminates, and focus servo is activated. Further control is in accordance with the focus error signal.
Fig. 22 shows the focus search circuit.

When the Focus Search command is transmitted from IC401 to the servo commander in IC141, IC141 causes the servo commander to output the $\overline{FST}$ signal (from pin 14), and discharges C147 (100 μF, 10 V) through R137 (180 Ω). At this time, the object lens of the Laser Pickup Ass'y lowers.
Then, IC141 causes the servo commander to output the FOCS signal (from pin 13) to pin 20 of IC101 (FOCS) and the Focus Control P.C.B. Ass'y to deactivate the focus servo.
Simultaneously, it charges C147 (100 μF, 10 V) through R143 (68 kΩ). At this time, the object lens of the Laser Pickup Ass'y rises slowly.
The focus zero detector section in IC101 detects the S-curve of the focus error signal (as shown in Fig. 23). This S-curve is detected when it gets almost in focus.

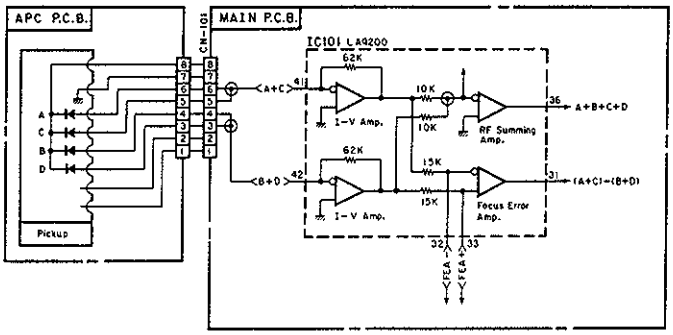


Fig. 21 RF Amp. Circuit

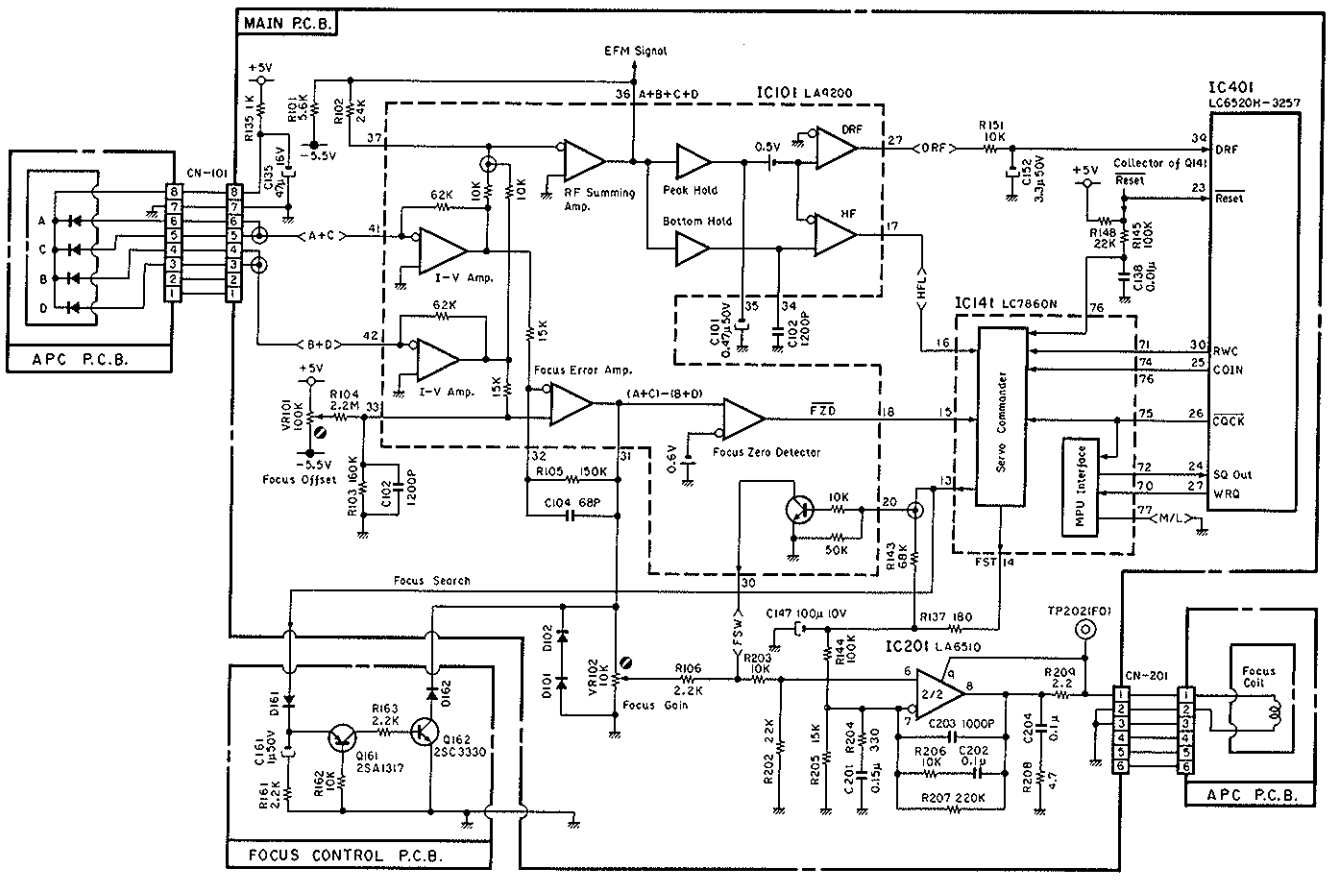


Fig. 20 Focus Servo Circuit

When the S-curve signal lowers than −0.6 V, $\overline{FZD}$ = L signal is output from pin 18 of IC101 and input into pin 15 of IC141. For generation of $\overline{FZD}$ signal, refer to Fig. 24.

When the $\overline{FZD}$ = L signal is input, the servo commander in IC141 resets the FOCS signal. By this, FOCS = L signal is output from pin 13 of IC141. This signal is input into pin 20 of IC101. Since pin 30 of IC101 (FSW) is consequently brought into the high-impedance state, focus error signal is input into the focus coil driver, activating focus servo, and the focus error signal controls the focus coil.

After outputting the Focus Search command, IC401 examines input signal into pin 39 (DRF) to check whether focus servo is activated. If focus servo is not activated during charging C147, IC401 outputs the Focus Search command again.

The DRF signal is generated in IC101. Output signals from the quarter-split photodiode are summed and amplified by the RF summing amplifier in IC101 to be the EFM signal, and is input into the peak hold section and bottom hold section. The DRF signal is set to "H" if voltage at pin 35 (PHLD) is 0.45 V. It is set to "L" if PHLD voltage is 0.42 V.

The object lens of the Laser Pickup Ass'y is located at the mechanical zero point, i.e., in the lower position when the Power switch of the OMS-1 is set to OFF. When the Power switch is turned ON, it moves up to the electrical zero point, i.e., a point where 0.5 V is applied across the focus coil. Based on this point as the center, the object lens moves up and down for focusing.

VR101 (100 kΩ) is for adjusting offset of the focus error amplifier, and VR102 (10 kΩ) is for adjusting focus gain.

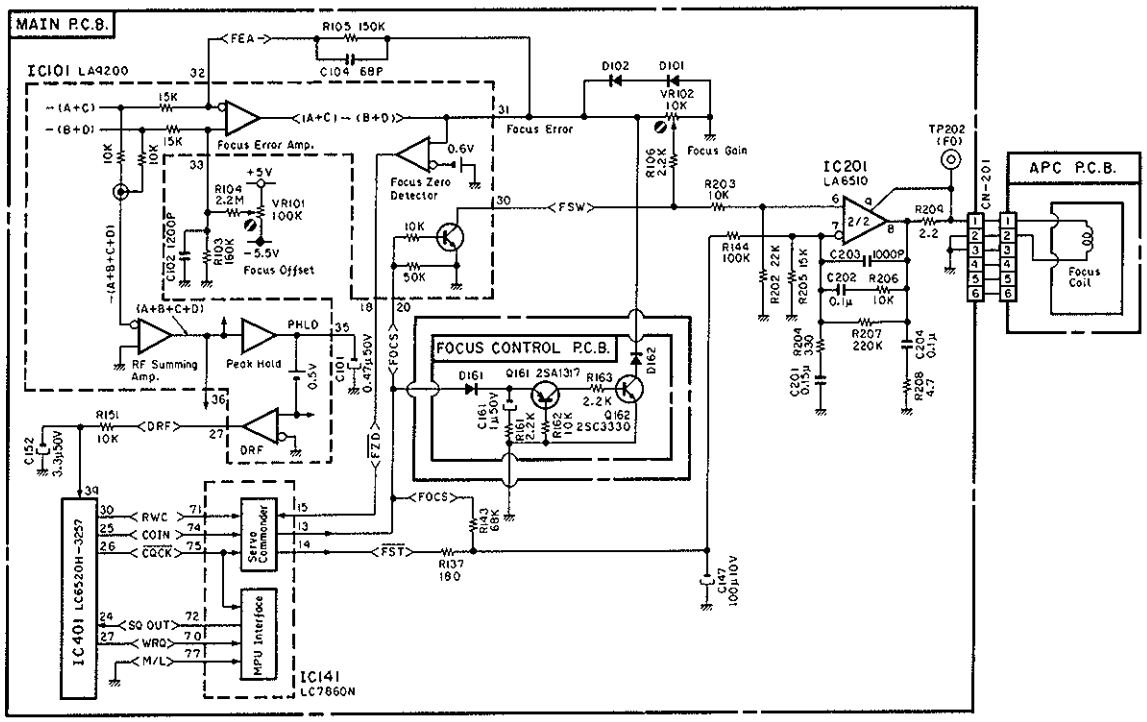


Fig. 22 Focus Search Circuit

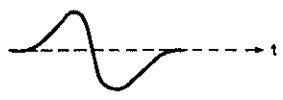


Fig. 23 Focus S-Curve

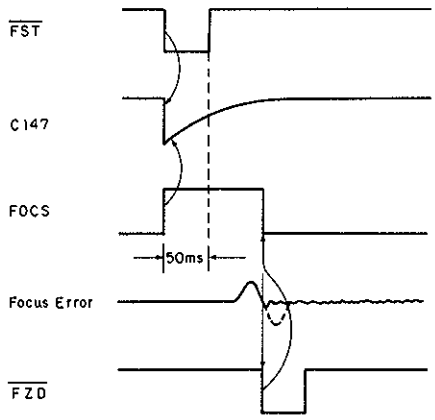


Fig. 24 Timing Chart

8. Tracking Servo System

Fig. 25 shows a block diagram of the tracking servo system. The tracking servo moves the object lens in the pickup in right-left direction to compensate for eccentricity of the CD itself or for the eccentricity of the CD produced by chucking at loading time of CD into CD player.

The eccentricity of the CD itself is specified to be within ±70 μm.

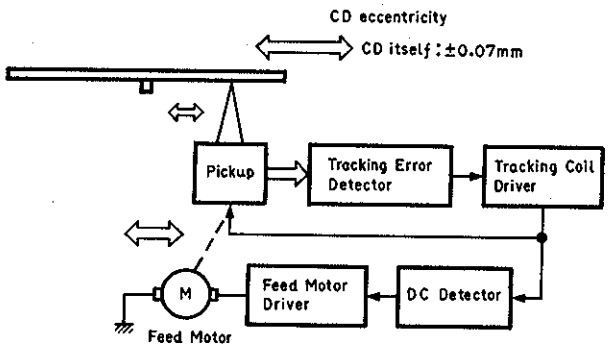


Fig. 25 Tracking Servo System Block Diagram

In the OMS-1, the object lens in the pickup is designed to follow up only quick displacements such as eccentricity. To have the whole pickup follow the track, the feed servo system is used. The feed servo detects the DC component in the tracking error signal and drives the feed motor to shift the pickup itself.

The tracking servo of the OMS-1 uses three-beam method. Fig. 26 illustrates the principle of producing three beam spots. The main-beam spot (zeroth order diffracted light) and two sub-beam spots (first order diffracted light) are separated by a grating plate.

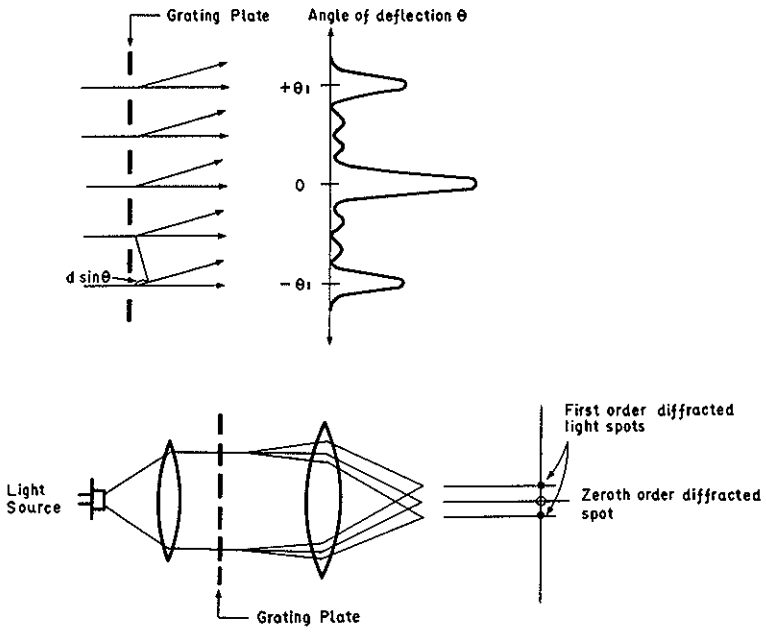


Fig. 26 3-Beam Method

The second and higher order diffracted light rays are also produced, but these are not used as they are extremely small in light quantity; in fact, these rays are unnecessary for the purpose.

The intensity of diffracted light increases with light traveling angles as follows:

$$d\sin\theta = n\lambda$$

The beam traveling in the direction such that n=1 is called the zeroth order diffracted light.

As illustrated in Fig. 27, the three-beam method projects three spots — the main spot and two sub spots on its sides — onto the pit surface of the CD in such an arrangement that the three spots form a line at a small angle with the track. Fig. 28 shows basic principle how to generate a tracking error signal.

The beams of light reflected by the sub spots are detected by separate PIN photodiodes, and the balance between these beams are processed to generate a tracking error signal.

If the object lens is displaced to the right, the sub spot E is off the track, so the tracking error amplifier is unbalanced in inputs and develops positive voltage at its output. If the object lens is displaced to the left, the sub spot F is off the track, so the tracking error amplifier is unbalanced in inputs and develops negative voltage. Thus the resultant tracking error signal is bipolar. That is, the error signal indicates the displacement side (right or left) relative to the track and the amount of displacement.

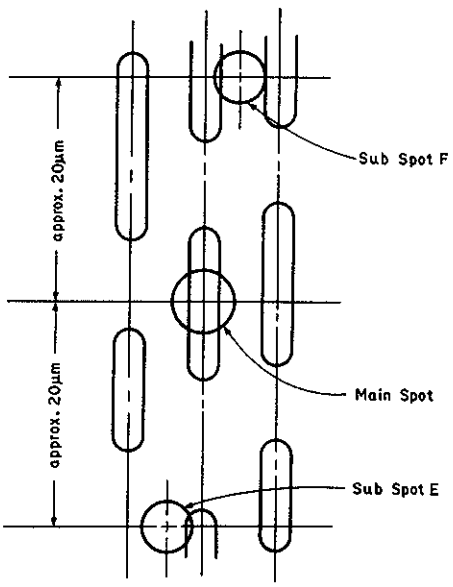


Fig. 27 3-Beam Spots on the Pits

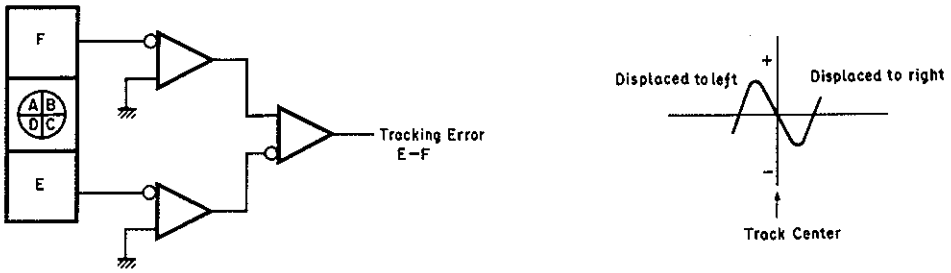


Fig. 28 Basic Principles How to Generate a Tracking Error Signal

Fig. 29 shows the tracking servo circuit of the OMS-1. Sub beams reflected by a CD are received by PIN photodiodes E and F in the laser pickup. Signals of the PIN photodiodes E and F are input into pins 47 (E) and 48 (F) of IC101 on the Main P.C.B. Ass'y respectively, and amplified through current-to-voltage conversion by the I−V amplifiers.

Signals processed through current-to-voltage conversion become −E and −F, and are differentially amplified by the tracking error amplifier in IC101, which outputs E − F signal, i.e., tracking error signal. This signal is input into two circuits. One is input into VR122 (30 kΩ), which adjusts tracking gain, and is input into the TE-preamplifier. Another is once output from pin 2 of IC101 (TEAO), and then input into pin 3 (TESI) of IC101 again through C123 (0.1 μF), R126 (2.2 kΩ), and C124 (1000 pF). This signal is used to detect the S-curve of tracking error signal in the TES section in IC101.

Output signal of the TE-preamplifier from pin 7 (TPRO) is input into the tracking coil driver composed of IC201-1/2 (LA6510) and its peripheral circuits, which drives the tracking coil in accordance with tracking error signal to control it so that the tracking error signal is always set to zero.

If the tracking error signal cannot be controlled by the tracking coil, DC voltage at output terminal of the tracking coil driver is supplied to the feed servo circuit to move the laser pickup itself so that the object lens is located at the center.

VR123 (10 kΩ) is used to adjust offset of the tracking servo circuit.

IC201-1/2 is also used for track jump. For details, refer to "10. Track Jump System".

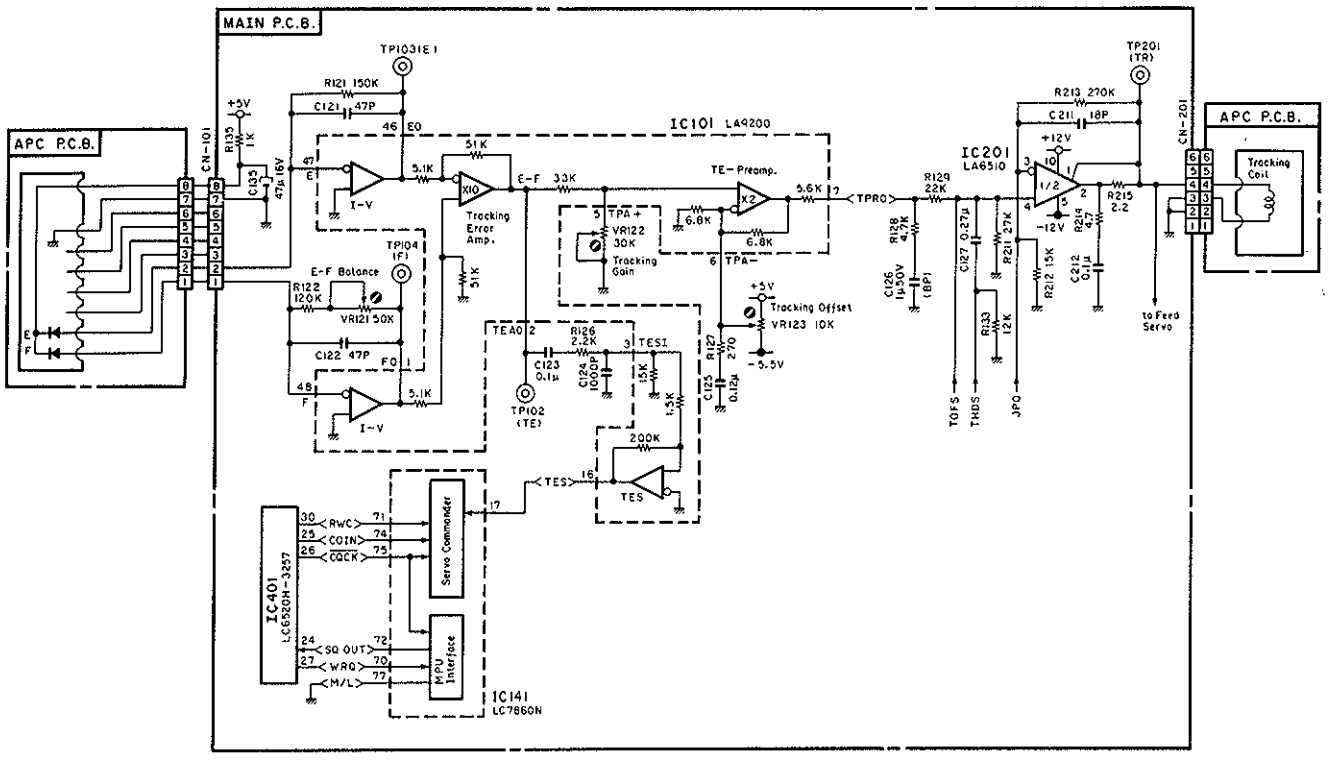


Fig. 29 Tracking Servo Circuit

9. Feed Servo System

The tracking servo follows up deviations quickly by moving the object lens, but the lens moving range is small (approx. ±0.8 mm). Because music tracks run a wide range from the inside to outside of the CD, they must be followed up by moving the laser pickup itself. And this is done by the feed servo system.

Fig. 30 shows the feed servo circuit of the OMS-1. If music is played back with the laser pickup fixed, the object lens in the laser pickup goes after the track toward the limit of its movable range. The closer to the limit of the movable range, the larger the DC component in the tracking error signal. The feed servo circuit moves the laser pickup by driving the feed motor so that the DC component becomes 0 V.

The feed servo circuit is controlled by the tracking error signal and FM+ signal or FM– signal from IC401. When the feed servo is active, if the object lens in the laser pickup shifts off center, the tracking error signal has an increasing quantity of DC component. The tracking error signal is integrated by R251 (10 kΩ) and C244 (2.2 μ 50V), then it passes through the high-cut filter (R246 and C243) so that only the DC omponent remains unremoved. This DC component is amplified by the feed motor driver (IC221-2/2) to drive the feed motor.

On the other hand, when fast-feeding the laser pickup, this is done according to the FM+ signal or FM– signal from IC401, so the feed servo circuit operation must be stopped. To do this, IC141 outputs the THLD signal. As a result, Q242 (RN1207) is turned OFF, and Q241 (2SC2878) is turned ON to short the feed servo circuit to ground. Then the FM+ signal from IC401 moves the laser pickup in the forward direction; the FM– signal from IC401 moves the laser pickup in the reverse direction.

When, the Power switch is set to ON or the OMS-1 is set to Stop mode, IC401 outputs FM– signal to return the laser pickup toward the inner perimeter of the CD. A provision is made to prevent the laser pickup from returning more than necessary. Specifically, as the pickup reaches the Read-In area, which extends 2 mm from the CD's innermost perimeter, the Pickup Inner switch works so that the signal $\overline{\text{Inner-End}}$ = L is input to pin 3 of IC401 via D401 and FM– signal is reset. Thus the feed motor is stopped.

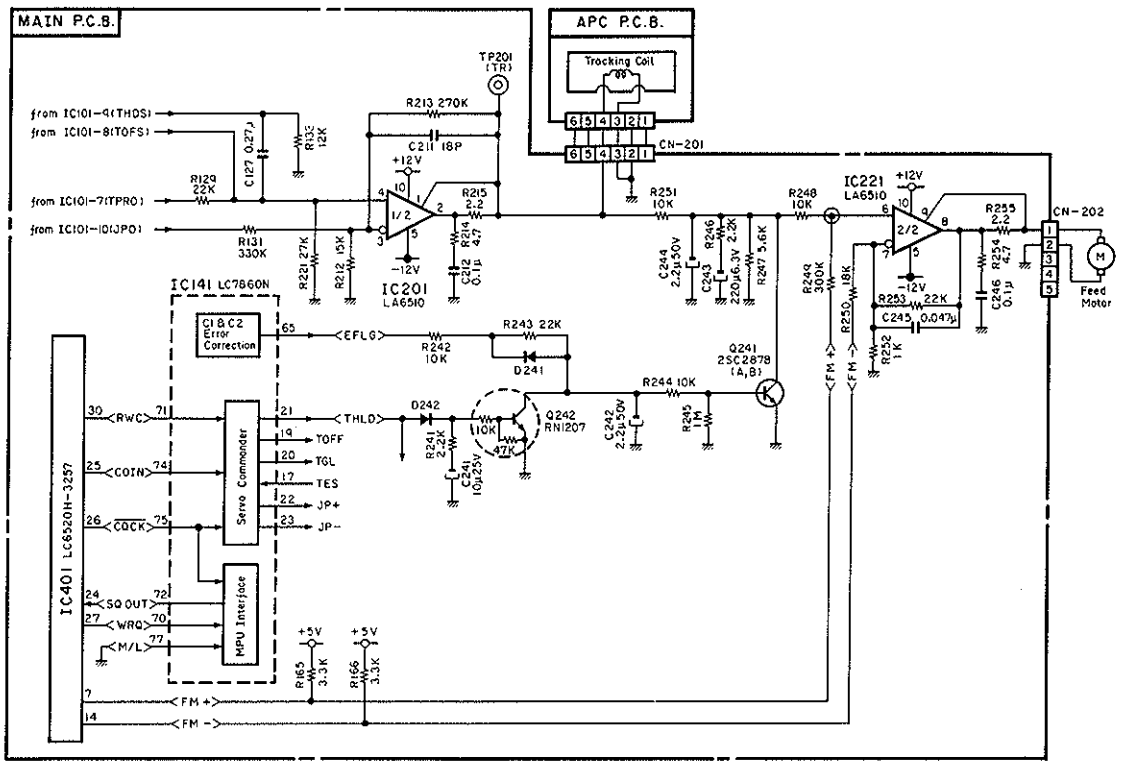


Fig. 30 Feed Servo Circuit

10. Track Jump System

Track jump of the OMS-1 consists of four types; 1-track jump, 4-track jump, 16-track jump, and 64-track jump. Fig. 34 shows Track Jump commands and their timing chart.

Signals HFL, TES, TOFF, TGL, THLD, JP+, and JP– are used for track jump. Functions of these signals are as follows:

HFL: This function detects track jumps. Brake timing information is sent to the IC141 (LC7860N) together with the TES signal.

TES: The level of TES drops when S-curve of the tracking error detection signal (TE output) drops. TES is a schmitt-type circuit which eliminates improper operation caused by noise present in the output. Brake timing information is sent to the IC141 together with the HFL signal.

TOFF: This signal is used to turn ON and OFF the tracking servo.

TGL: This signal is used to reduce gain of the tracking servo.

THLD: This signal is used to hold the tracking servo output voltage at the THLD ON voltage.

JP+/JP–: These signals are generated according to Track Jump command. A jump of the prescribed number of tracks is 1, 4, 16, or 64.

Fig. 31 shows the HFL signal and TES signal generating circuit.

Output of the RF summing amplifier is input into the peak hold section and bottom hold section.

The bottom hold is at a time constant that enables following as high as 30 kHz of traversing, while the peak hold is at another that enables following even the rotary frequency envelop fluctuations. Then the signals enter the HF comparator, and from pin 17 (HFL), it is output as a HFL signal to pin 16 (HFL) of IC141.

On the other hand, the tracking error signal is fed to pin 3 (TESI) of IC101.

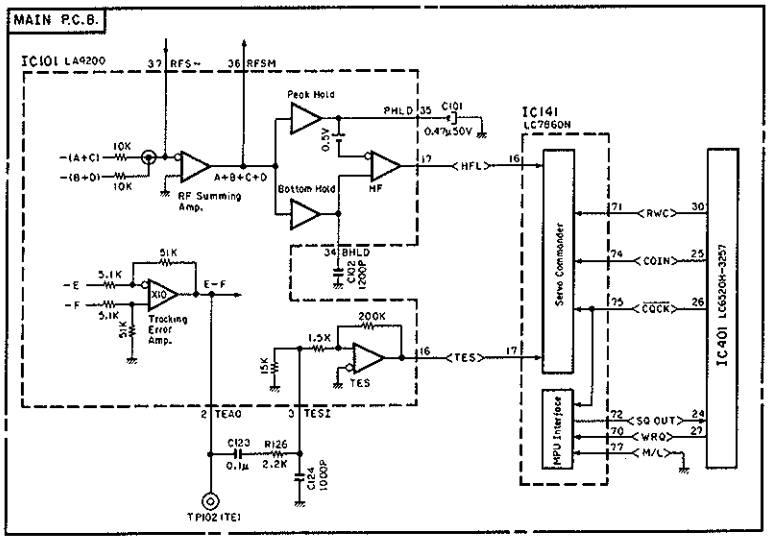


Fig. 31 HFL Signal and TES Signal Generating Circuit

This signal is waveform-shaped in the TES amplifier, output from pin 16 as the TES signal, and input into pin 17 (TES) of IC141.

Fig. 32 shows the timing chart of this circuit.

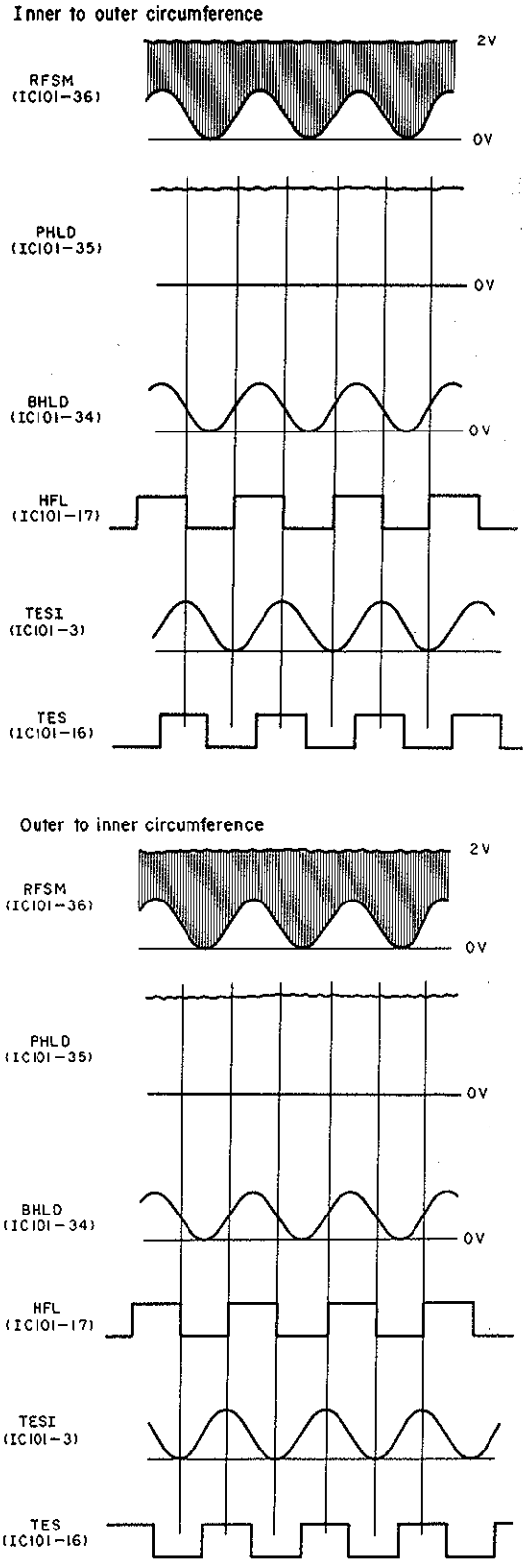


Fig. 32 HFL and TES Signals

Fig. 33 shows the track jump circuit. Fig. 34 shows the track jump pulse timing chart.

When the Track Jump command is input to the servo commander of IC141, acceleration pulses are issued followed by deceleration pulses, the braking period elapses, and the prescribed jump is completed.

The brake period is determined by the TES and HFL signals.

The beam is detected in the slit direction, the section in the tracking error signal enhancing the slit is cut by TOFF signal, and the track destination after jumping is determined by raising the servo gain by the TGL signal.

The TOFF signal goes "H" when the CLV Servo command is stop.

Normal 1-track jump, 4-track jump, 16-track jump, and 64-track jump are executed based on the JP+ signal from pin 22 of IC141 and the JP– signal from pin 23.

For jumping 256 tracks or more, information is transmitted to IC401 to move the laser pickup a lot using the FM+ signal from pin 7 and FM– signal from pin 14. While 256 tracks are jumping, the THLD signal is set to "H".

For 1-track jump, the JP– (or JP+) signal is output from pin 23 (or 22) of IC141 as 0.5-track jump period worth of acceleration signal to drive the actuator (laser pickup), and the JP+ (or JP–) signal is output from pin 22 (or 23) of IC141 as 233 μs worth of deceleration signal to brake the actuator.

For 4-track jump, 2-track jump period worth of acceleration signal is output, and then 446 μs worth of deceleration signal is output.

For 16-track jump, 9-track jump period worth of acceleration signal is output, and then 7-track jump period worth of deceleration signal is output.

Likewise, for 64-track jump, 36-track jump period worth of acceleration signal is output, and then 28-track jump period worth of deceleration signal is output.

For 256-track jump, the FM+ (or FM–) signal is output from pin 7 (or 14) of IC401 and, at the same time, the 256-track jump command is issued from IC401 to the servo commander of IC141. By this command, the THLD signal is set to "H", TGL signal is set to "L", and TOFF signal is set to "H".

Immediately after counting 256 tracks, IC141 sets the TOFF and THLD signals to "L" to enter the track-complement operation.

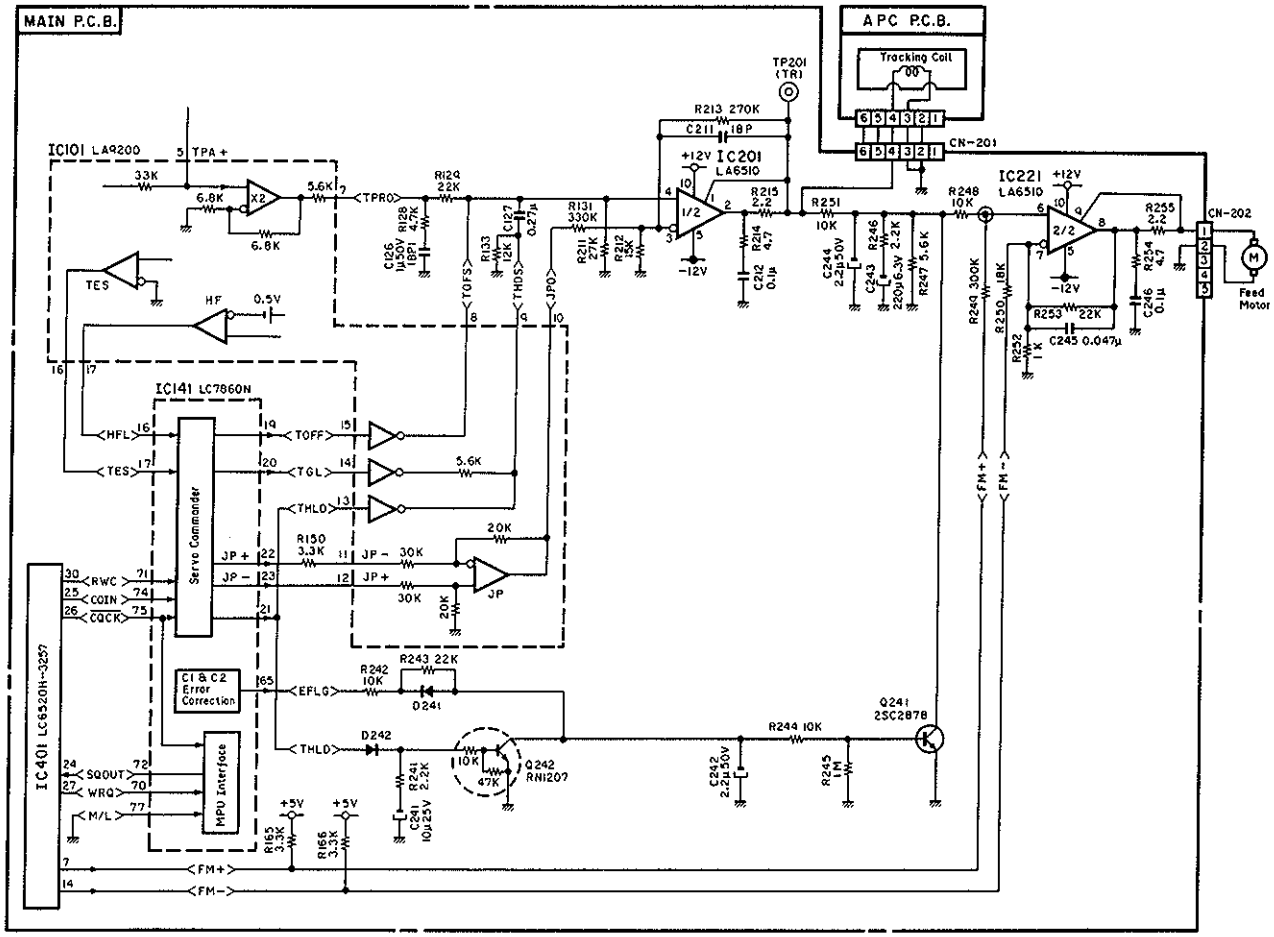
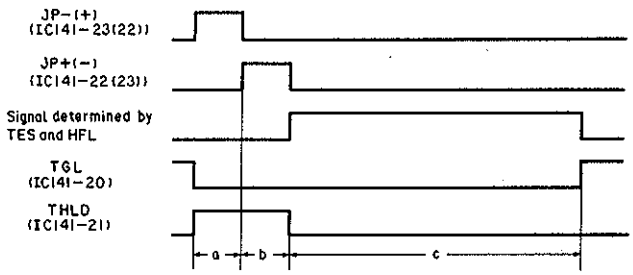


Fig. 33 Track Jump Circuit



Command	a	b	c
1 Track Jump In (Out) No. 1	233 μs	233 μs	17ms
1 Track Jump In (Out) No. 2	0.5 Track Jump period	233 μs	17ms
4 Track Jump In (Out)	2 Track Jump period	466 μs	17ms
16 Track Jump In (Out)	9 Track Jump period	7 Track Jump period	17ms
64 Track Jump In (Out)	36 Track Jump period	28 Track Jump period	17ms
256 Track Check	When 256 tracks elapse, THLD signal goes Low.		

Fig. 34 Track Jump Pulse Timing Chart

Fig. 35 shows the 256-track jump timing chart. A large scratch, etc., on the disc surface may cause the feed servo to run away because of disorder of the tracking error signal. To prevent this, the error flag signal output from pin 65 (EFLG) of IC141 is input to the base of Q241 after integration.

Note that the THLD signal is input to the base of Q242 so that Q241 is not turned ON even if the tracking error increases in the track search or track jump mode. When Q241 is cut off, the tracking error signal is input to the feed servo circuit, and the control is made by the JP+ or JP− signal output from IC141.

One-track jump is normally performed by applying acceleration pulse first, then applying deceleration pulse for a fixed period of time after a tracking error signal passed zero cross point. Refer to Fig. 36.

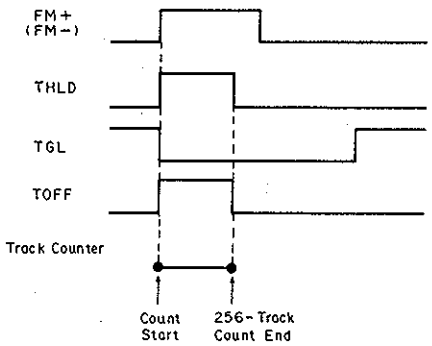


Fig. 35 256-track Jump Timing Chart

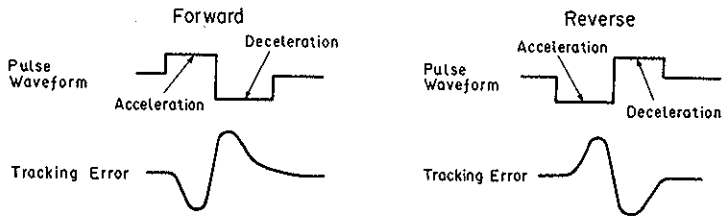


Fig. 36 Tracking Error Signal

11. CLV (Constant Linear Velocity) Servo System

The rotational frequency of CD is 500 rpm for the innermost perimeter and 200 rpm for the outermost perimeter. The CLV servo provides control to give a constant linear speed.

The frame sync. signal read from the CD is locked in the PLL (phase locked loop). The disc motor rotational frequency is controlled so that 1/588 of the frame sync. signal frequency matches the 7.35 kHz that is made by dividing the crystal oscillator frequency. Fig. 37 shows a CD player frequency system diagram and Fig. 38 shows the processing of signals to be recorded on the CD.

The CLV servo circuit of the OMS-1 is built on the Main P.C.B. Ass'y. It is composed primarily of IC101, IC141, IC221-1/2, and peripheral circuitry (refer to Figs. 39, 40 and 42).

The CLV servo circuit is basically controlled through comparison of frame sync. signal created from data read on a CD with signal from the crystal timing generator. Thus, this section describes circuits on the order of the data processing circuit for read data (this circuit is also used in "12. Signal System"), PLL circuit, and CLV servo circuit.

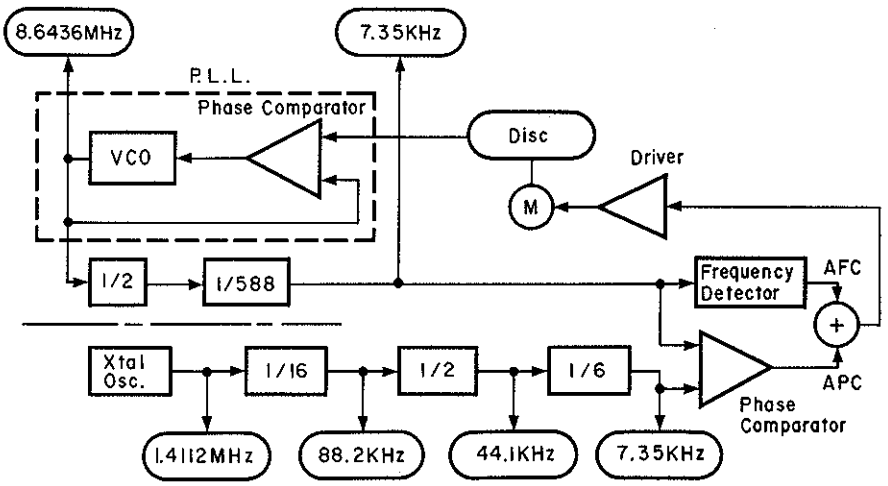


Fig. 37 CD Player Frequency System Diagram

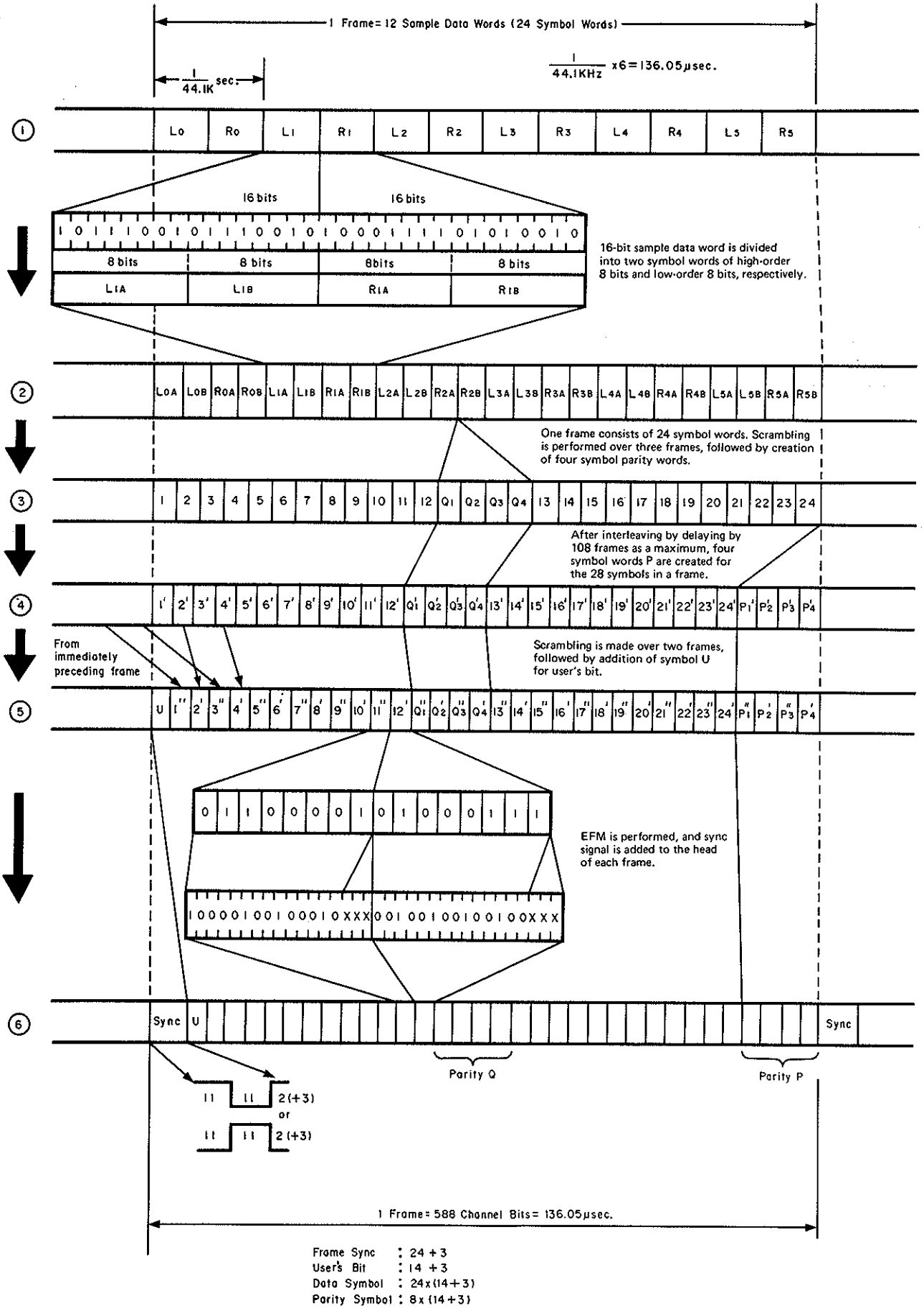


Fig. 38 Processing of Signals to be Recorded CD

(1) EFM Auto Slice Circuit

Fig. 39 shows the EFM auto slice circuit.

Light reception signals from the quarter-split photodiodes A, B, C, and D in the laser pickup are ORed by the Main P.C.B. Ass'y to create (A + C) signal and (B + D) signal. These signals are input into pins 41 and 42 of IC101 respectively, and converted and amplified through current-to-voltage conversion by the I–V amplifier. –(A + C) signal and –(B + D) signal processed through current-to-voltage conversion pass through resistors (10 kΩ), and are wired-ORed to be –(A + B + C + D) signal. Then, it is inverted and amplified by the RF summing amplifier, and output from pin 36 (RFSM) of IC101 as (A + B + C + D) signal.

This RFSM signal is the EFM signal, which passes through LPF101 to eliminate high-frequency noises. LPF101 also increases 3T component level. Then the signal is input into pin 8 (EFMIN) of IC141. The EFM signal is brought into binary-coded EFM signal by the auto slice circuit composed of the slice level controller in IC141, slice amplifier in IC101, and peripheral circuits.

The center of the EFM signal does not always coincide with the center of amplitude. This center-to-center disagreement is known as asymmetry (which is due largely to the CD itself). The specific condition of asymmetry depends on CD mastering laser power, development and all other processes, and the wavelength of laser beam used in playback.

In the OMS-1, an EFM auto slice circuit is employed to eliminate the effects of asymmetry. The EFM auto slice circuit serves for converting EFM signals into binary code.

The EFM signal is input to pin 8 (EFMIN) of IC141, inverted and waveform-shaped by the inverter in IC141, and output from pin 7 ($\overline{\text{EFMO}}$). The inverted and waveform-shaped signal is further inverted by the inverter in IC141 and output from pin 6 (EFMO). The $\overline{\text{EFMO}}$ and EFMO signals are converted into DC signals through integrated circuits composed of R114 and C109, and R113 and C108, respectively.

When the slice level is proper, both DC converted signals at pins 23 and 24 of IC101 coincide with the half level (2.5 V) of peak value (5 V) at pins 7 and 6 of IC141, so that no output appears at pin 22 of IC101.

If the slice level at point 8 of IC141 shifts to the positive side, the slice level at pin 7 shifts to the negative side and the slice level at pin 6 shifts to the positive side. Accordingly, the voltage at pin 23 of IC101 is lowered than 2.5 V and the voltage at pin 24 is higher than 2.5 V. As a result, the voltage at pin 22 shifts to the negative side and the DC signal at pin 8 of IC141 is lowered through R112 so that the slice level is maintained properly.

On the other hand, if the slice level at pin 8 of IC141 shifts to the negative side, inverse operation is performed and the voltage at pin 22 of IC101 shifts to the positive side. Consequently, the DC signal at pin 8 of IC141 become higher through R112 so that the proper slice level is maintained.

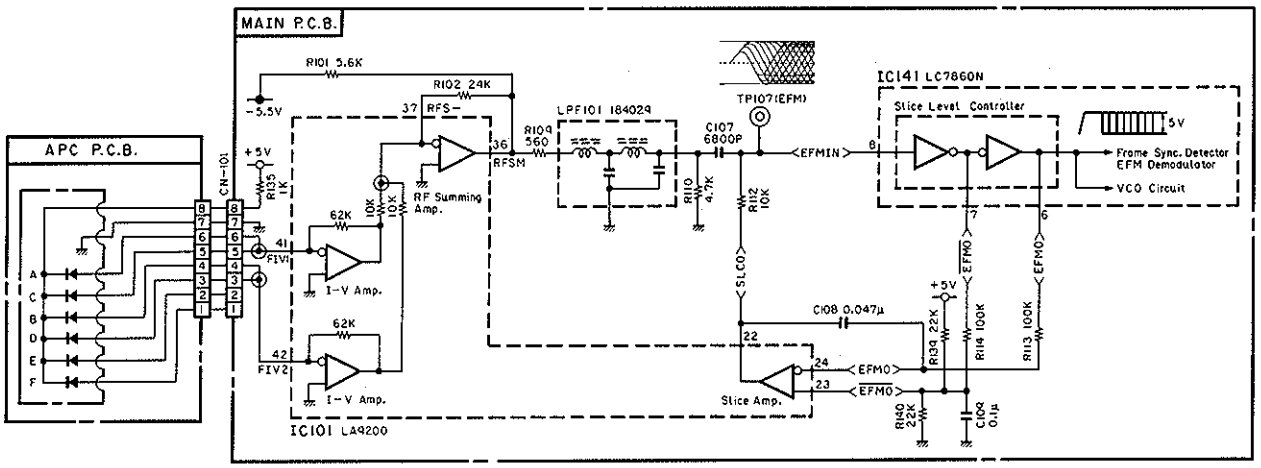


Fig. 39 EFM Auto Slice Circuit

(2) PLL Circuit

Figs. 40 and 41 show the PLL circuit and the timing chart, respectively. The binary-coded EFM signal enters the phase comparator circuit. Here, phase comparison is made of the binary-coded EFM signal at its each edge with respect to the PCK that is one half of VCO. The comparison result output from pin 4 of IC141 is a tri-state PDO signal.

When the binary-coded EFM signal and the PCK signal are synchronous, the mean voltage level at the PDO pin is approx. +2.5 V. When the VCO is at a higher frequency, the mean voltage level drops; when the VCO is at a lower frequency, the mean voltage level rises.

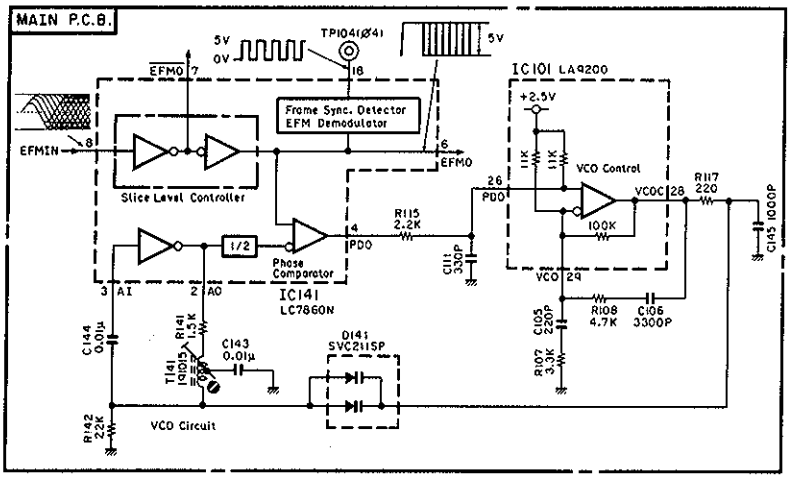
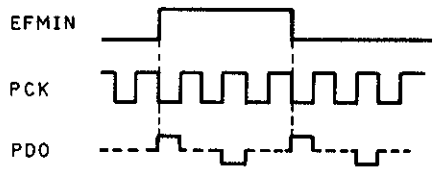


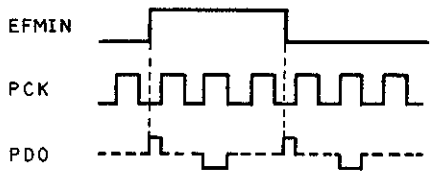
Fig. 40 PLL Circuit

The PDO signal comes to pin 26 of IC101. When it is higher than the reference voltage at the inverting input of the VCO controller in IC101, positive voltage appears at pin 28; when it is lower than the reference voltage, negative voltage appears at pin 28. Based on this, the VCO oscillating frequency is controlled to synchronize the binary-coded EFM signal and the PCK signal.

When EFM signal and VCO synchronize together



When VCO is higher than EFM signal



When VCO is lower than EFM signal

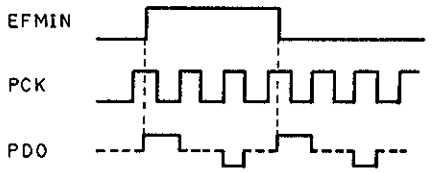


Fig. 41 Timing Charts at PDO Pin

(3) CLV Servo Circuit

Fig. 42 shows the CLV servo circuit of the OMS-1.

Internal mode of the CLV servo circuit in IC141 consists of four modes as shown in Table 2. Upon receiving a command from IC401, IC141 selects a corresponding mode by observing the crystal timing generator, binary-coded EFM signal, and the PCK signal.

At first (in Play mode), IC141 selects Low Speed Rotation, then Rough Servo, and PLL Servo at last.

The disc motor is controlled by signals output from pins 11 (CLV+) and 12 (CLV–) of IC141.

The CLV+ is a signal for accelerating the disc motor in the forward direction and the CLV– is a deceleration signal. One of the four modes, Acceleration, Deceleration, CLV, and Stop, is selected by a command from IC401.

The CLV+ and CLV– outputs in each of these modes are shown in Table 3.

Signal output from pins 11 (CLV+) and 12 (CLV–) of IC141 is input into pins 4 and 3 of IC221-1/2 through the integration circuit composed of R221, C221, R224, and C222. IC221 outputs signal corresponding to these signals from pin 2 to drive the disc motor.

Table 3

MODE	CLV+	CLV–
Acceleration	H	L
Deceleration	L	H
CLV	*	*
Stop	L	L

* In the CLV mode, the disc rotation is detected from the EFM signal, the internal mode of IC141 is changed, and normal linear speed rotation is adopted by control of each signal. The cycle of PWM is 7.35 kHz and the 1/64 duty cycle is 1.114 sec.

Table 2

Internal Mode	CLV+	CLV–
Rough Servo (judged as low speed rotation)	H	L
Rough Servo (judged as high speed rotation)	L	H
PLL Servo (PCK is locked)	PWM	PWM
Low Speed Rotation (when no HF signal)	1/64 DUTY	L

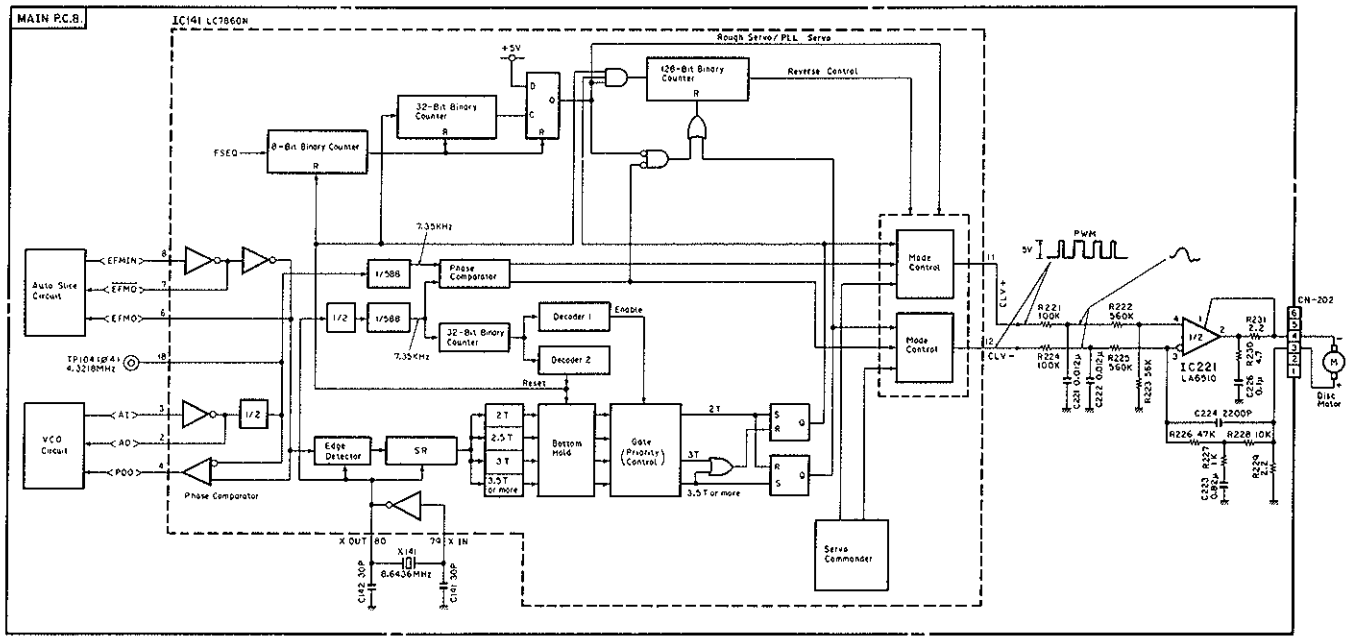


Fig. 42 CLV Servo Circuit

12. Signal System

Fig. 43 shows the digital signal processing circuit.

Digital signal processing of the OMS-1 is performed by IC141 (LC7860N), IC142 (LC3517AS-15), IC101 (LA9200), IC401, and peripheral circuits.

EFM signal output from IC101 is brought into the binary-coded EFM signal by the slice level controller in IC141.

Digital signal processing is based on this signal.

(1) Frame Sync. Detector and EFM Demodulator

Since the EFM signal read out of the quarter-split PIN photodiode in the laser pickup contains a 2.1609 MHz clock component, the 4.3218 MHz bit clock (PCK) that synchronizes with the clock component may be fetched with the PLL circuit. During recording on CD, no pattern will be identical to the frame sync. signal, but due to dropouts, jitters, etc., the same pattern is sometimes detected in the playback data.

Conversely, the original frame sync. signal sometimes fails to be detected for similar reasons.

After converting just the edge portion of PCK-latched EFM signals (EFMO) to "1" and the remaining portion to "0", the signals will be input to a frame sync. detector for detection of the frame sync. signal.

In IC141, 14-bit data will be demodulated into 8-bit data by the EFM demodulator through 14-bit to 8-bit conversion.

Next, a write request signal will be output to the RAM Interface block. Then, by an OENB signal conveyed from the block, the demodulated 8-bit data will be output to the RAM data bus (pins DB7 through DB0).

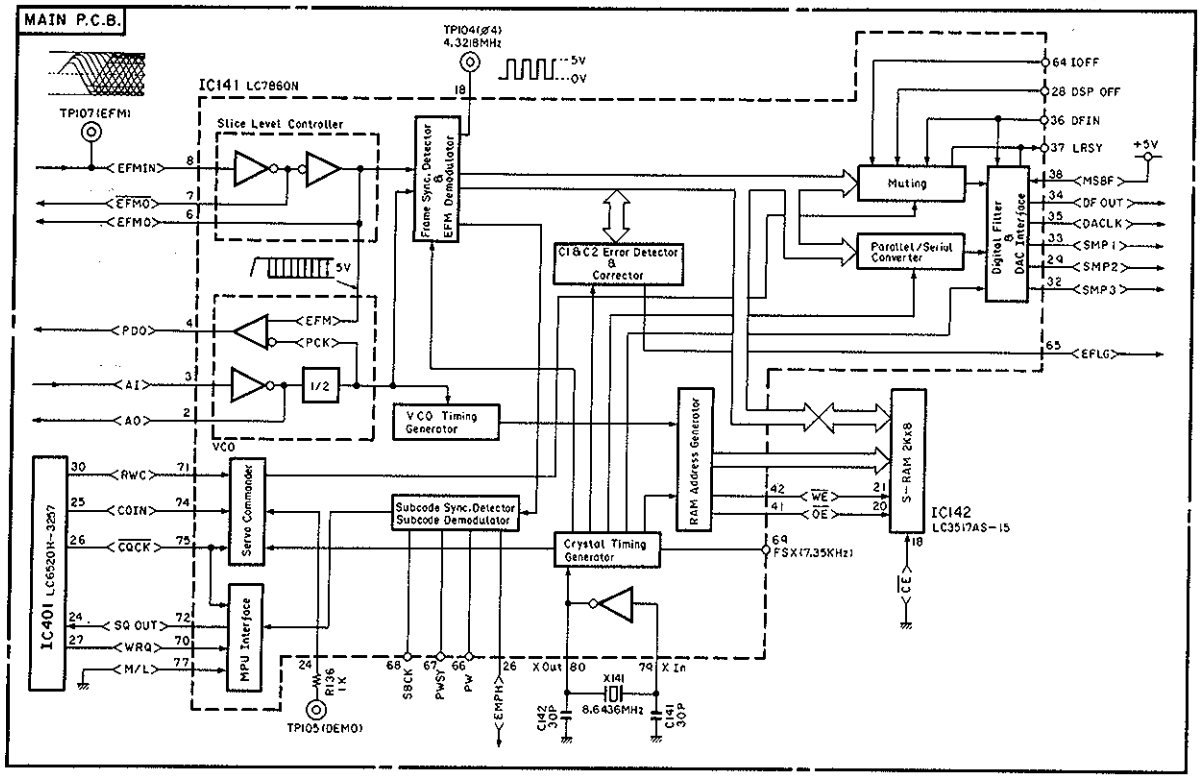


Fig. 43 Digital Signal Processing Circuit

(2) Subcode Demodulation

A CD may be divided into 99 portions, meaning it may record up to 99 small pieces of music. To accommodate 99 music pieces, the CD player must be able to detect each pieces automatically and play back according to the user-specified program. Subcoding P and Q are used to find the start of a music piece.

Subcoding P has the only function of indicating the start of a music piece. It is coded to "1" at the start of a piece, and "0" for the rest of the music. The time allocated for "1" must be at least two seconds. Upon simply looking at "1", the laser pickup moves fast to search for the start.

Fig. 44 shows the subcoding frame format.

Subcoding P is the leftmost 1-bit column in the 8-bit subcoding data.

Subcoding Q (the second leftmost column in Fig. 44) provides even higher functions to the CD player.

The general format of subcoding Q is shown in Fig. 45.

In the figure, S0 and S1 are subcoding sync. signals, with the following patterns:

S0 = "00100000000001"

S1 = "00000000010010"

The WRQ signal from IC401 goes "H" when the CRC check results in success as well as only when address is 1.

The data from SQOUT (pin 72 of IC141) signal can be read in order if IC401 detects this "H" state and sends $\overline{CQCK}$ signal to pin 75 of IC141. When $\overline{CQCK}$ signal output starts, updating of data in the registers of IC141 is prohibited. When IC401 completes reading of the data, RWC signal is driven once to "H" and permission to update data is given.

At this time, WRQ signal drops to "L".

As WRQ signal drops to "L" 11.2 ms after going to "H", transmission of $\overline{CQCK}$ signal starts while it is "H".

The data can be read with in the LSB first out.

Fig. 46 shows data contents of subcoding Q. Fig. 47 shows its timing chart.

The control field consists of four bits for indicating the number of audio channels and the emphasis ON/OFF state. The pre-emphasis characteristics of CD are specified as shown in Fig. 48. In the OMS-1, de-emphasis is automatically turned ON/OFF by detecting the signals in subcoding Q. De-emphasis (EMPH) signal is output from pin 26 of IC141.

The contents of the 4-bit control field are as follows:

"0000": 2-channel audio signal without pre-emphasis.

"1000": 4-channel audio signal without pre-emphasis.

"0001": 2-channel audio signal with pre-emphasis.

"1001": 4-channel audio signal with pre-amphasis.

The CRC (cyclic redundancy code) is an error detection code consisting of 16 bits. Its role is important: It judges whether the received subcoding Q data is right or wrong and reads only right data.

The address field consists of four bits. It may take one of three possible codes, but in most cases, it is coded as "0001".

For ten successive subcoding Q formats shown in Fig. 45, at least nine of them must have the address pattern "0001". The two patterns other than "0001" have little meaning for the CD player. When the address is "0001", the data contents are as shown in Fig. 49. This data is updated every 1/75 second. Delivered to pin 24 of IC401, subcoding Q controls time display and the laser pickup.

On the OMS-1, the Read-In area of CD is read to read TOC (table of contents) at CD load time.

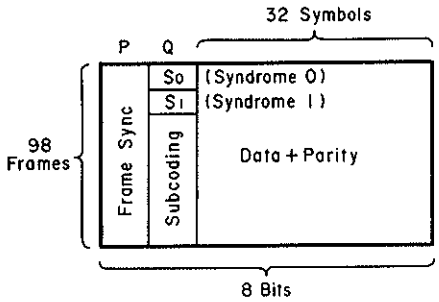


Fig. 44 Subcoding Frame Format

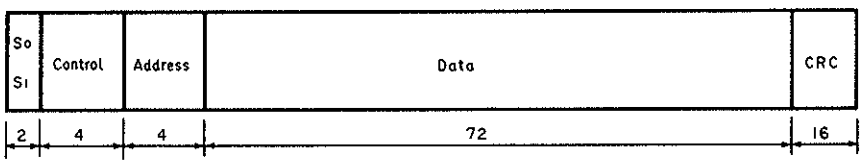


Fig. 45 Subcoding Q Format

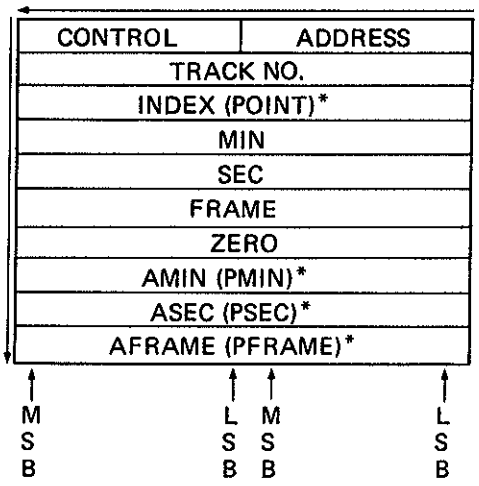


Fig. 46 Data Contents of Subocoding Q

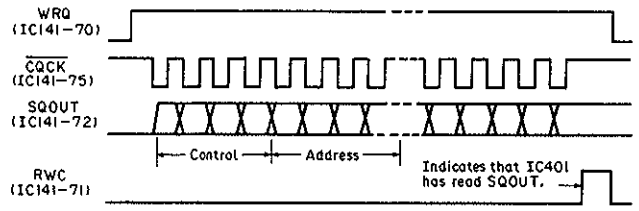


Fig. 47 Timing Chart

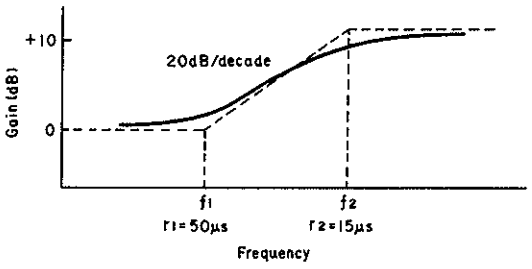


Fig. 48 Pre-emphasis Characteristics

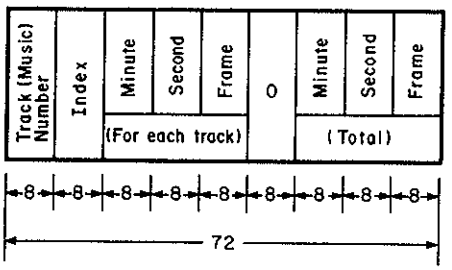


Fig. 49 Data Contents of Subcoding Q (for Address "0001")

(3) RAM Interface (External RAM Address Generation)

(a) Requests from EFM demodulator block (write requests to RAM)

As the whole symbol of demodulated data has been made ready, the EFM demodulator block will issue a request to the RAM interfacing block to write the data in the external RAM. This request is a WREQ signal. The RAM interfacing block assigns priority levels to the requests from other blocks for the orderly processing thereof.

Upon receiving an EFM write request, the block will generate an address to the RAM and engage write enable mode. It will also issue a data outputting instruction to the EFM demodulator block. This instruction is an OENB signal.

For the EFM block and the requests therefrom (WREQ), a PLL type clock is used. For subsequent processings, a crystal type will be used.

(b) RAM address generation and jitter margin

IC141 performs de-interleave processing of EFM demodulated data by address generation of 8-bit/2K words of external RAM IC.

For de-interleaving, 108 frames of data will be required. In other words, to obtain one frame of audio data for playback at given point in time, 108 frames of post-EFM demodulation data will be required.

The C1/C2 type of data is a data train in the middle of an interleaving process, so that it will be included in the 108 frames. Actual data is generated continuously. Accordingly, de-interleaving will have to be updated in frame increments. For this reason, read/write base counters will be required.

The base counter takes counts for each and every frame. The write base counter will be used only when writing EFM data. The address output to an external RAM will be determined by the amount of delay relative to the EFM demodulated data and the number of its frames.

As EFM demodulated data synchronizes with the data regenerating circuit (PLL), it contains disturbances in the disc revolution servo (CLV servo) and the like (wow & flutter, for example). The data will be fetched into the external RAM, but since the data fetched out of the RAM will be in synchronization with the crystal circuit clock, the RAM will in effect be exercising time axis correction.

The jitter absorption capabilities of the input data is +4 frames as the buffer memory capability. The remaining buffer space is constantly checked and the data write address is controlled to the center of the buffer by fine-tuning the division ratio on the CLV servo circuit PCK side. If the +4 frames buffer capacity is exceeded, the write address is forcibly set to +0. This means that the errors occurring cannot be processed by flags and muting is applied for a 128 frames period. Table 4 shows jitter margin.

Table 4 Jitter Margin

Position	Division Ratio or Action
Less than −4	Forcibly moved to ±0
−3	589 (Advance division)
−2	589 (Advance division)
−1	589 (Advance division)
±0	588 — Standard division
+1	587 (Retard division)
+2	587 (Retard division)
+3	587 (Retard division)
+4 or greater	Forcibly moved to ±0

(c) Requests from error corrector block (C1/C2 corrections and R/W pointer)

The error corrector block requests the data located on the train to be corrected (C1/C2). It also issues requests to rewrite erroneous data into valid ones, as well as those for R/W pointers that indicate the reliability of data.

These requests will be made with the 8-bit data that are output by the error corrector block to the RAM interfacing block.

The RAM will output data to the error corrector block. This block will then generate an address for the data requested, and also control R/W of the RAM at the same time.

(4) Error Correction

At the error correction block in IC141, up to double errors will be corrected for the C1 correction and C2 correction individually.

The EFM demodulated data is written to the external RAM (IC142), jitter absorption is made, and the following processing is made at fixed timing set by the crystal circuit clock.

First, error checking and correction is made for C1 block, and the C1 flag is determined and written to the C1 flag register. Next, error checking and correction is made for the C2 block, and the C2 flag is determined and written to the external RAM IC.

Table 5 shows C1 check, correction, and flag processing.
Table 6 shows C2 check, correction, and flag processing.

(5) Playback Flag Determination and Interpolation

(a) Interpolator block

By a read request to D/A converter, 3 bytes of data will be fetched. They will each consists of a C2 flag, 8 lower bits, and 8 upper bits. The upper and lower bits together will represent 16 bits of data fetched with a single sampling.

Since the C2 flag indicates lack of the 16-bit data reliability, data containing C2 flag will be subjected to interpolation in this block.

Table 7 shows relationship between C2 flag and playback flag.

Fig. 50 shows an example of interpolation.

Table 5 C1 Check, Correction, and Flag Processing

C1 Check	Correction and Flag Processing	
No Errors	Correction unnecessary	Flag reset
1 Error	Correction made	Flag reset
2 Errors	Correction made	Flag set
3 Errors or more	Correction impossible	Flag set

Table 6 C2 Check, Correction, and Flag Processing

C2 Check	Correction and Flag Processing	
No Errors	Correction unnecessary	Flag reset
1 Error	Correction made	Flag reset
2 Errors	Reference to C1 flag *1	
3 Errors or more	Reference to C1 flag *2	

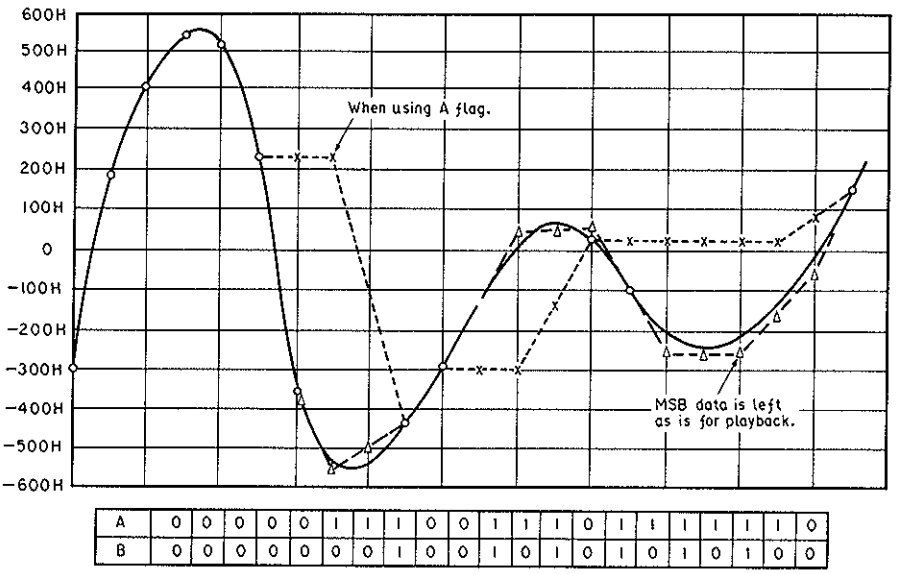
*1 When the error position determined by C2 check and C1 flag are the same, correction is made and the flag is reset. However, when the number of C1 flags is 3 or more, the possibility of improper correction exists and correction is not made. The C1 flag remains as it is and the C2 flag is set. When one of the error positions is the same and the other does not match, correction is not possible. Furthermore, when the number of C1 flags is less than 5, the C1 check results are thought to be suspect and the flag is set. 6 or more errors is handled in the same manner as correction impossible; the C1 flag remains as it is and the C2 flag is set. Correction is of course not possible if none of the error positions match. When the number of C1 flag is less than 2, the data evaluated as OK by the C1 check is probably incorrect and the flag is set. In all other cases, the C1 flag remains as it is and C2 flag is set.

*2 When correction impossible is evaluated with 3 or more errors, correction is of course not possible. When the number of C1 flags is less than 2, the data evaluated as OK by the C1 check is probably incorrect and the flag is set. In all other cases, the C1 flag remains as it is and C2 flag is set.

Table 7 Playback Flag

C2 Flag		Playback Flag
Upper	Lower	
0	0	Reset
0	1	*
1	0	Set
1	1	Set

*: Reset performed if amplitude of previous 8 samples is 200H or greater. Set performed if not. The data up to the C2 block is treated as symbols in 8-bit units with each sample of an upper and lower symbol for a total of 16 bits. Thus, each sample has two C2 flags. Data manipulation such as average value interpolation and previous value hold, etc., can be made by attempting to infer a value as close to the true value as possible from the surrounding samples and substituting this for the error sample. The error in this is low when the signal level is low, but becomes large when the amplitude becomes larger. For a sample in which the upper symbol is no-error and only the lower sample contains an error, adopting a procedure of substituting 80H for the lower, symbol will limit the error to 80H, a relatively low level. Thus in this case, the playback flag is reset if the amplitude of the previous 8 samples is 200H or greater. Previous value hold occurs for interpolation when there is an error in only one sample and for the average value when there are consecutive errors in two or more samples.



A: OR obtained from upper and lower C2 flags to obtain playback flag.
B: C2 flag of upper symbol used as playback flag of IC141.

Fig. 50 Interpolation Example

(b) Muting and attenuation

At the muting block, audio signal outputs can be either muted or attenuated by the Mute signal from the servo commander block. When the F. FWD and REV buttons of the RM-1CD are pressed together, OMS-1 enters Half Mute mode and the digital signal outputs will be attenuated by 12 dB.

Mute (−∞ dB) and Half Mute (−12 dB) are executed through 4 steps, step 0 → 1 → 2 → 3, as shown in Table 8.

Table 8

ATTENUATION \ STEP	0	1	2	3
−∞ dB	1	3/4	1/4	0 (−∞ dB)
−12 dB	1	3/4	2/4	1/4 (−12 dB)

(6) Digital Filter and DAC (D/A Converter) Interface

The digital filter and DAC interface of the OMS-1 are incorporated in IC141.

Main function of the digital filter is over-sampling, i.e., conversion of sampling frequency. In the OMS-1, 2-times over-sampling is performed.

On a CD, audio signals with limited frequency bandwidth of 20 kHz are recorded as 16-bit quantized PCM signals at a sampling frequency fs = 44.1 kHz. As shown in Fig. 51, frequency spectrum of this sampled signal demonstrates distribution where the spectrum of the original audio signal turns over at integral multiple frequencies of fs as the center. Spectra whose center frequencies are nfs (n ⩾ 2; n = integer) are called image spectra.

These are spectrum components not included in the analog signals before sampling. Thus, to reproduce the original audio signal from sampled signals, it is necessary to remove the image spectra added in sampling. Since the upper limit of audio signals on CDs is 20 kHz, the lower limit of the image spectra is 44.1 kHz − 20 kHz = 24.1 kHz.

Therefore, audio signals can be reproduced from sampled signals through filtering with a low-pass filter which passes signals lower than 20 kHz and attenuates those higher than 24.1 kHz as shown in Fig. 52.

As the low-pass filter, an analog filter with sharp roll-off characteristics within the 4.1 kHz band will provide sufficient performance. However, even if such an analog filter can be designed almost ideally in its frequency characteristics, its phase sharply shifts close to the cutoff frequency, resulting in bad group delay characteristics.

Purpose of the over-sampling filter is to cover the non-ideal characteristics of analog low-pass filters. The over-sampling filter is a kind of sampling frequency converters, which can be regarded as a digital computing element multiplying the sampling frequency into its integral multiples. Through computing operation, it can create digital data which could be obtained by sampling at a frequency several times as high as the original sampling frequency.

Fig. 53 shows conceptual drawings of the 2-times over-sampling filter.

The FIR type digital filter provided with low-pass filter characteristics attenuates image spectrum whose center frequency is 44.1 kHz. Different from the analog filter, the digital filter has filtering characteristics repeating cyclically. Therefore, components higher than the image spectrum with a center frequency fs2 = 88.2 kHz remain.

Since over-sampling leaves wide range of bandwidth between the upper limit of audio signals and lower limit of image spectra as shown above, a low-pass filter with gentle roll-off characteristics as shown in Fig. 54 can remove image spectra. Consequently, group delay characteristics of the analog filter becomes approximate flat within the audio band, resulting in little sound deterioration in mid and high frequency bands.

After digital filtering, signals are output from the DAC interface block.

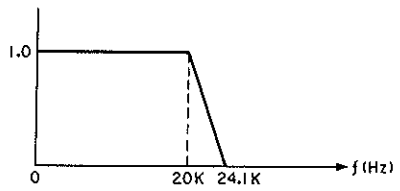
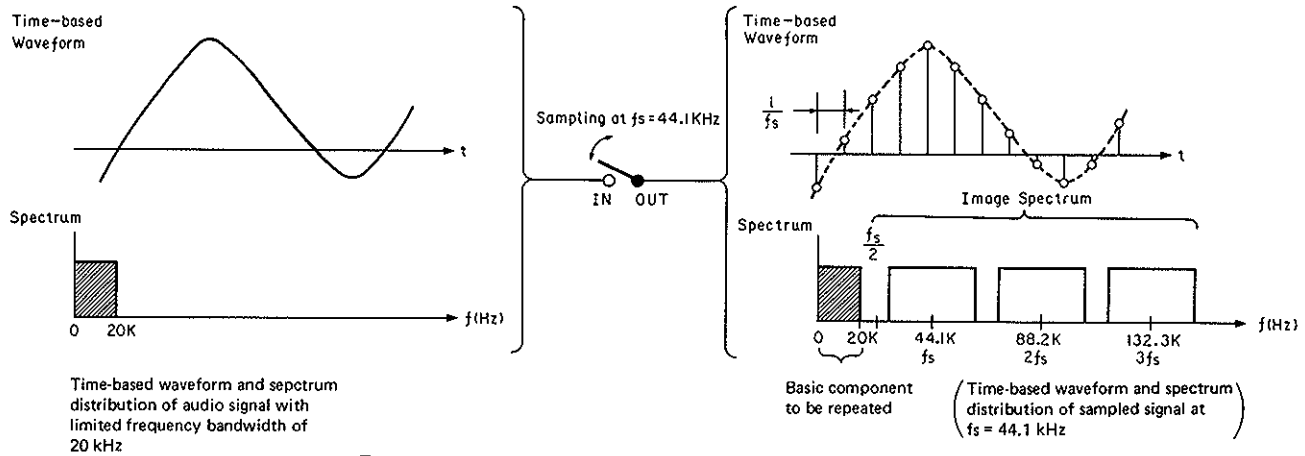


Fig. 52 Frequency Response of LPF for Reproducing Audio Signal



Time-based waveform and sepctrum distribution of audio signal with limited frequency bandwidth of 20 kHz

Fig. 51 Audio Signal & Time-Based Waveform and Spectrum Distribution of its Sampled Signal

Fig. 55 shows the timing chart of the DAC interface block. The DFOUT signal from pin 34 of IC141 is output in serial form, data of which is output in MSB first out order synchronously with the trailing edge of the DACLK signal. Pin numbers, signal names, and contents of the signals are as follows:

Pin No.	Signal Name	Contents
34	DFOUT	Serial data output with MSB first
35	DACLK	4.3218 MHz clock signal
33	SMP1	Switching and sample hold of the 88.2 kHz left channel
29	SMP2	Switching and sample hold of the 88.2 kHz right channel
32	SMP3	176.4 kHz strobe signal

(7) DEMO (Pin 24 of IC141) Signal

Has sound output adjustment function. Even if no command is sent from IC401, setting this pin to "H" will set muting to 0 dB and the disc motor to CLV, and will perform the focus search operation.

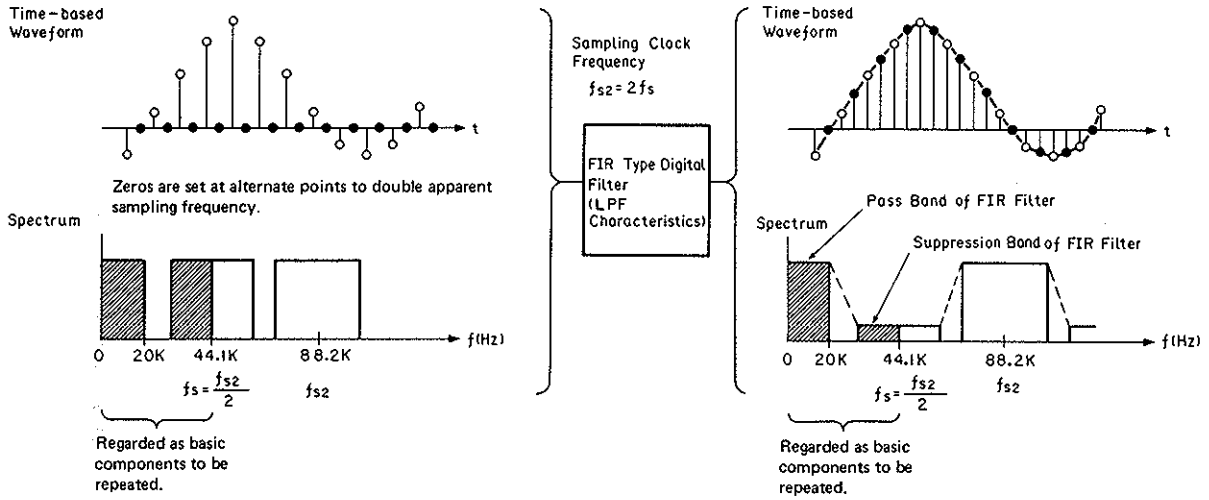


Fig. 53 Conceptual Drawing of 2-times Over-sampling Filter

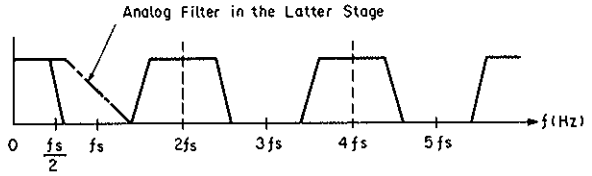


Fig. 54 Characteristics of 2-times Over-sampling Filter

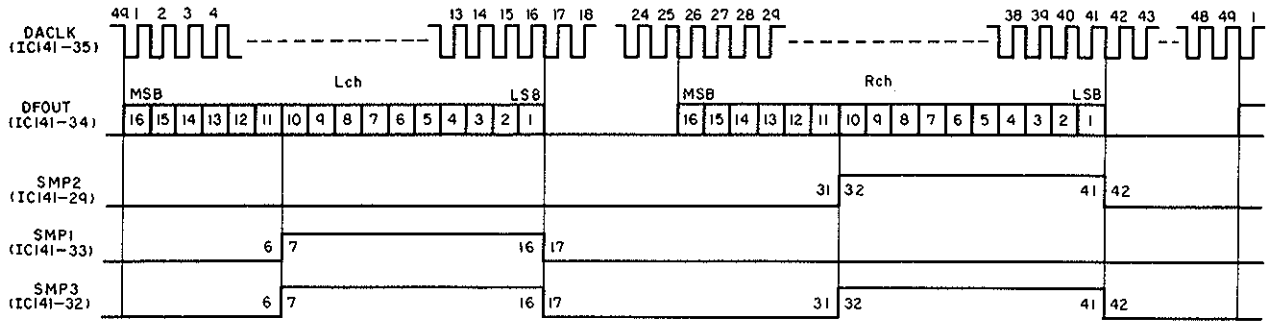


Fig. 55 Timing Chart of DAC Interface Block

(8) D/A Converter and Following Circuits

Fig. 56 shows the D/A converter and the following circuits of the OMS-1.

These circuits are roughly divided into the D/A converter, deglitcher/sample & hold section, and 5th-order active low-pass filter. They convert PCM-recorded signals on a CD into audio signals.

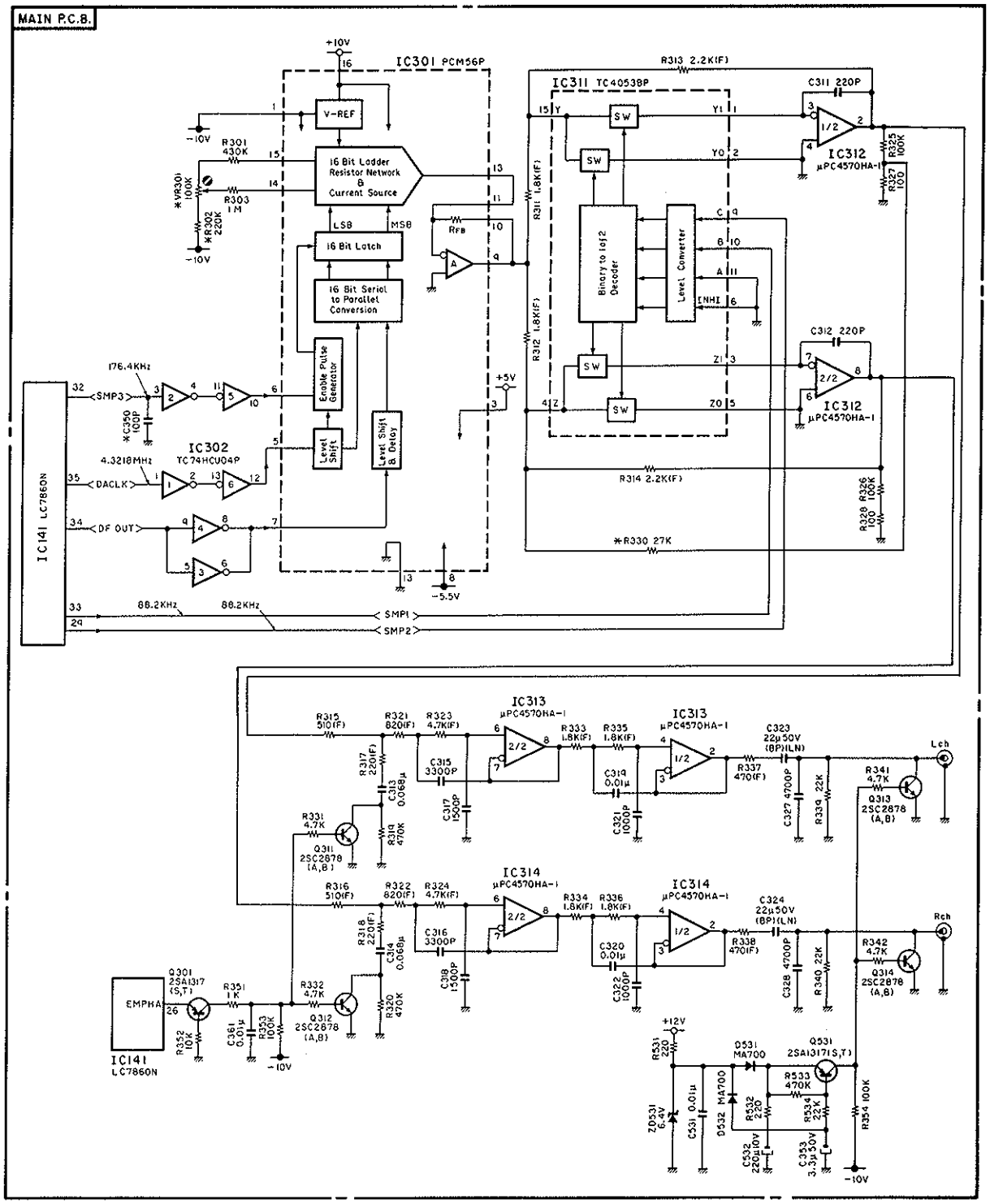


Fig. 56 Audio Signal Circuit

(a) D/A converter

Fig. 57 shows the D/A converter circuit of the OMS-1. The OMS-1 employs a D/A converter IC PCM56P. PCM56P has a serial input terminal for D/A conversion. PCM56P is designed based on the PCM54, used in the OMS-7II, etc., and has additional serial-to-parallel conversion function.

The DFOUT signal from pin 34 of IC141 is input into IC301, and is converted into 16-bit parallel data in the serial-to-parallel conversion section in IC301 based on the DACLK signal (4.3218 MHz) output from pin 35 of IC141. The 16-bit parallel data enters the 16-bit latch section.

Data input into the 16-bit latch section are output to the 16-bit ladder resistor network & current source section at the falling edge of a pulse output from the enable pulse generator in IC301. This pulse is generated when the SMP3 signal (176.4 kHz) is input from pin 33 of IC141. Fig. 58 shows the timing chart. Current of ±1 mA is output from the 16-bit ladder resistor network & current source section. Then, it is converted from current to voltage by the operational amplifier A in IC301, and is output from pin 9 as voltage output of ±3 V.

IC301 reduces zero-cross distortion in the MSB correction circuit with external-mount resistor as shown in Fig. 59. This distortion correction is more effective in low-level output (−20 dB to −60 dB) than full-scale output.

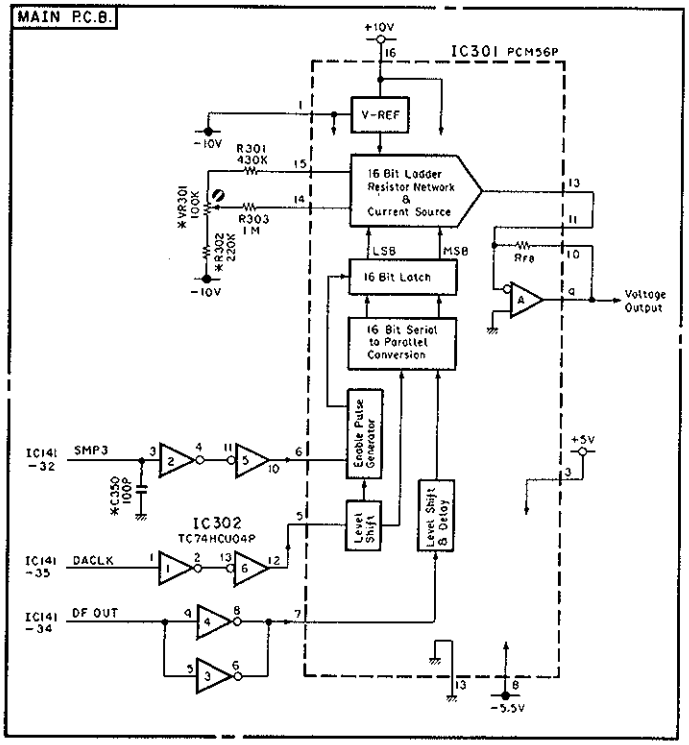


Fig. 57 D/A Converter Circuit

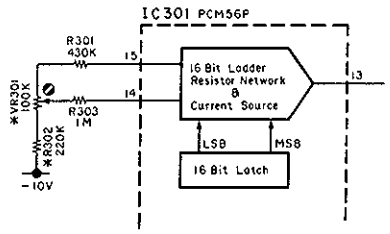


Fig. 59 MSB Correction Circuit

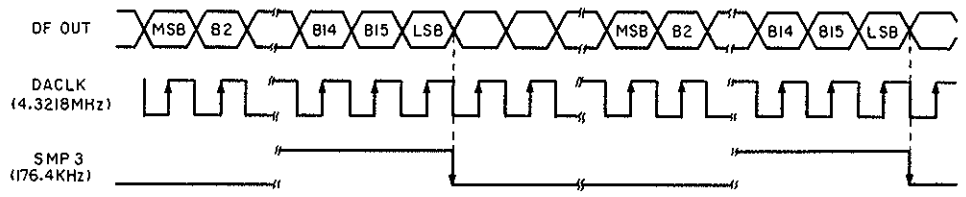


Fig. 58 Timing Chart

(b) Deglitcher/sample & hold circuit

Fig. 60 shows the deglitcher/sample & hold circuit of the OMS-1.

This circuit separates L-ch and R-ch signals output from IC301 to create sampled signals, and outputs them to the following 5th-order active low-pass filter. IC311 receives SMP2 signal (88.2 kHz) and SMP1 signal (88.2 kHz) output from IC141, and executes deglitching/sampling & holding. IC311 is a triple 2-channel multiplexer/demultiplexer IC. Since pins 11 (A) and 6 (INHI) of this IC are grounded, its truth values are as shown in Table 9. Actually, only circuits Y and Z function.

The circuit Y is used for L channel, and circuit Z is used for R channel.

The deglitch circuit is composed of R311, R312, R313, R314, C311, C312, IC311 and IC312.

Table 9 Truth Table of TC4053BP

Control Input				"ON" Channel		
Inhibit	C	B	A	Z	Y	X
L	L	L	L	Z_0	Y_0	X_0
L	L	H	L	Z_0	Y_1	X_0
L	H	L	L	Z_1	Y_0	X_0
L	H	H	L	Z_1	Y_1	X_0

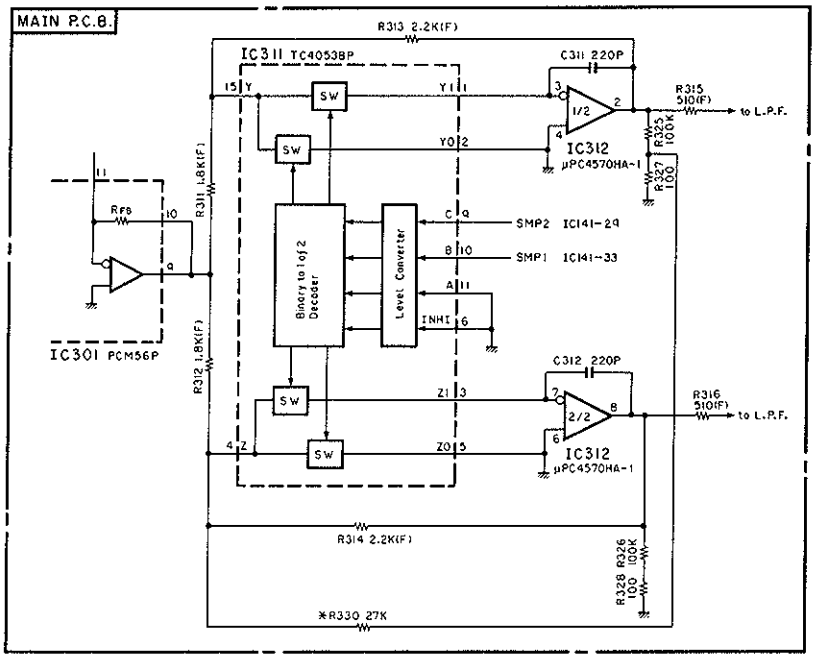


Fig. 60 Deglitcher/Sample & Hold Circuit

(c) 5th-order active LPF circuit

Fig. 61 shows the 5th-order active LPF circuit of the OMS-1. This circuit is the last stage of the OMS-1, and its output signals are output from the line output terminals of the OMS-1.

The output from IC312 includes a low-frequency component and sideband components as shown in Fig. 62. Therefore, only the low-frequency component must be extracted using a low-pass filter. The low-pass filter in the OMS-1 is a 5th-order active filter, which consists of two operational amplifier ICs. The low-frequency component having passed through the low-pass filter is sent to the outside via the line output terminals.

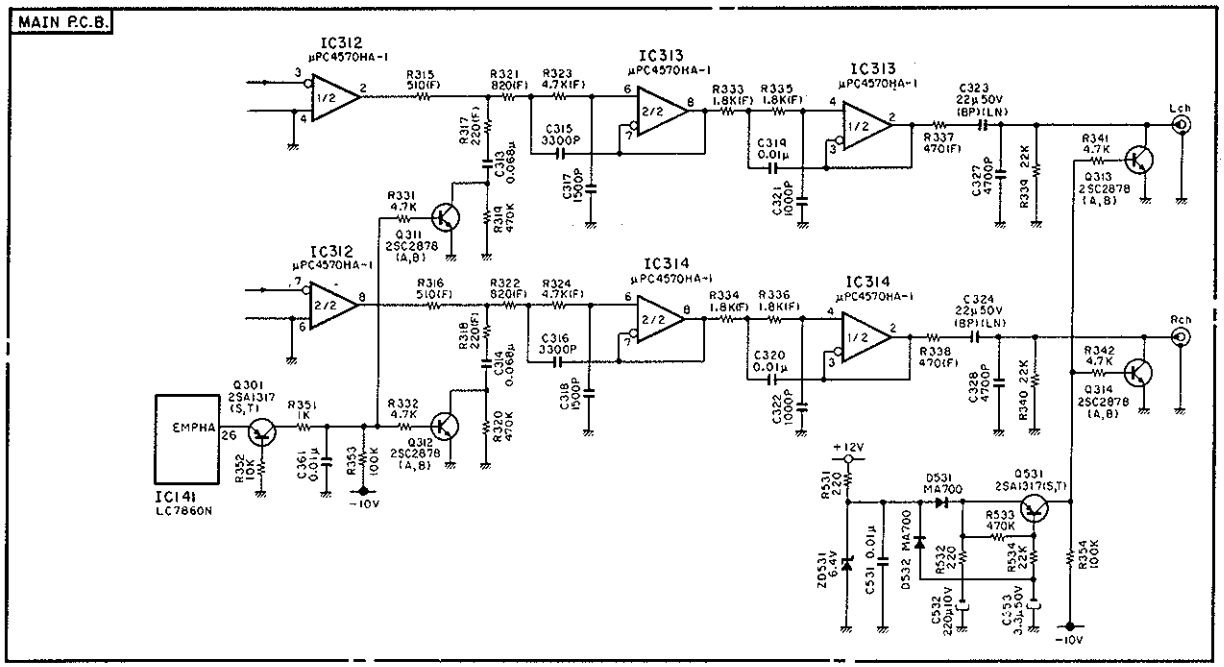


Fig. 61 5th-order Active Low Pass Filter Circuit

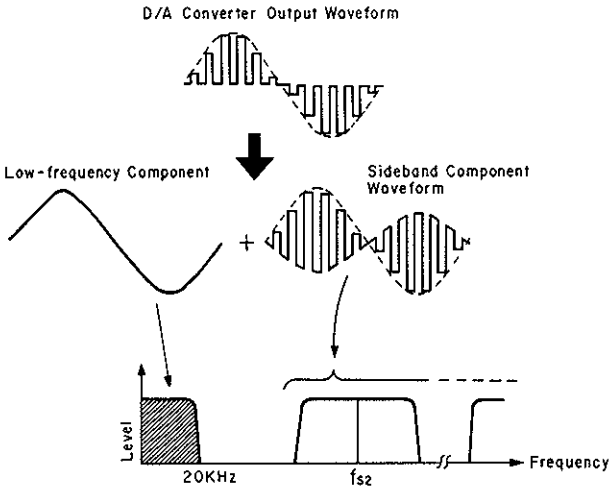


Fig. 62 D/A Converter Output Waveform and Low-frequency Component

(d) De-emphasis circuit

Fig. 63 shows the de-emphasis circuit of the OMS-1. Some CDs are recorded with pre-emphasis. The OMS-1 distinguishes possible emphasis when reading the CD's Read-In area. For music pieces recorded with pre-emphasis, the EMPH signal is output from pin 26 of IC141.

If the EMPH = H signal is output, Q301 is turned ON; consequently, Q311 and Q312 are turned ON; a set of R317 (220 Ω) and C313 (0.068 μF) and a set of R318 (220 Ω) and C314 (0.068 μF) are grounded through Q311 and Q312 respectively, providing in de-emphasis characteristics shown in Fig. 64. The time constant can be found as follows:

$$R317\ (R318) \times C313\ (C314) = 220 \times 0.068 \times 10^{-6}$$
$$= 14.96\ \mu s$$
$$\fallingdotseq 15\ \mu s$$
$$(R315\ (R316) + R317\ (R318)) \times C313\ (C314)$$
$$= (510 + 220) \times 0.068 \times 10^{-6}$$
$$= 49.64\ \mu s$$
$$\fallingdotseq 50\ \mu s$$

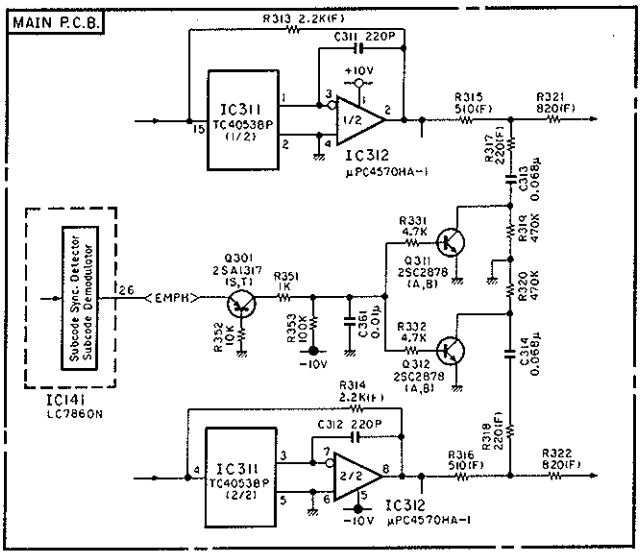


Fig. 63 De-emphasis Circuit

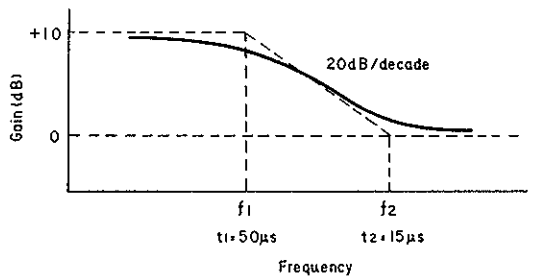


Fig. 64 De-emphasis Characteristics

(e) Reset circuit for line output terminals

Fig. 65 shows the reset circuit of line output terminals of the OMS-1.

Reset is performed by using the Reset signal generated in the reset circuit mentioned in item 4. When the Power switch of the OMS-1 is turned ON or OFF, Q531 is turned ON; consequently, Q313 and Q314 are turned ON, and line output terminals are grounded to prevent noises from being output to external devices.

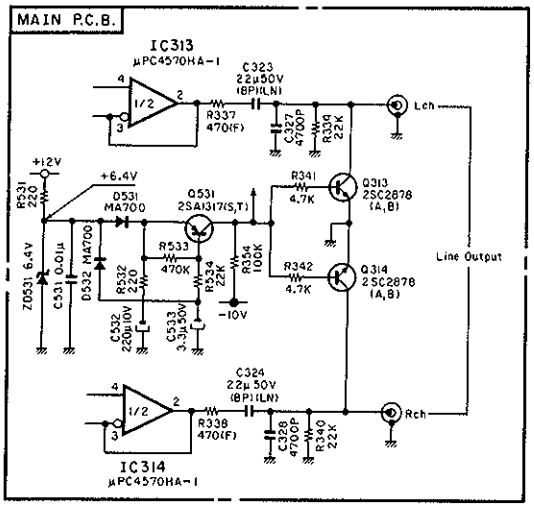


Fig. 65 Reset Circuit of Line Output Terminals