

SERVICE MANUAL

MODEL A401M  
MODEL A201S  
MODEL 401S

P.O. Box 389  
1840 Bradshaw Ct.  
Walled Lake, MI 48390  
USA

TABLE OF CONTENTS

<u>SECTION</u>	<u>TITLE</u>	<u>PAGE</u>
1.0	INTRODUCTION	1
2.0	CIRCUIT DESCRIPTION	2
2.1	AMPLIFIER BOARD, ASSEMBLY NO. 100016	2
2.2	PROTECTION BOARD, ASSEMBLY NO. 100017	6
2.3	DISTRIBUTION BOARD, ASSEMBLY NO.'s 100018 (MONO) AND 100019 (STEREO)	8
2.4	HEAT SINK ASSEMBLY, NO.'s 100020 (N CHANNEL) AND 100021 (P CHANNEL)	9
3.0	AMPLIFIER SERVICE	10
3.1	GENERAL PRECAUTIONS	11
3.2	LIST OF DRAWINGS	12
3.3	BOARD REPLACEMENT	13
3.3.1	PROTECTION BOARD ASSEMBLY	13
3.3.1.1	SELECTION	13
3.3.1.2	CALIBRATION	13
3.3.1.3	REPLACEMENT PROCEDURE	13
3.3.2	AMPLIFIER BOARD ASSEMBLY	14
3.3.2.1	SELECTION	14
3.3.2.2	CALIBRATION	14
3.3.2.2.1	FUSE RELACEMENT	16
3.3.2.3	REPLACEMENT PROCEDURE	16
3.3.3.	DISTRIBUTION BOARD ASSEMBLY	22
3.3.3.1	SELECTION	22
3.3.3.2	CALIBRATION	23
3.3.3.3	REPLACEMENT PROCEDURE	24
3.3.4	HEAT SINK ASSEMBLY	24
3.3.4.1	SELECTION	24
3.3.4.2	CALIBRATION	25
3.3.4.3	REPLACEMENT PROCEDURE	25

<u>SECTION</u>	<u>TITLE</u>	<u>PAGE</u>
4.0	AMPLIFIER DIAGNOSTICS	27
4.1	NORMAL AMPLIFIER OPERATION	27
4.1.1	AMPLIFIER BOARD ASSEMBLY	27
4.1.2	PROTECTION BOARD ASSEMBLY	30
4.1.3.	DISTRIBUTION BOARD ASSEMBLY	32
4.1.4.	HEAT SINK ASSEMBLY	34
4.2	TROUBLE SHOOTING	34
4.2.1.	AMPLIFIER BOARD ASSEMBLY	35
4.2.2.	PROTECTION BOARD ASSEMBLY	36
4.2.3.	DISTRIBUTION BOARD ASSEMBLY	37
4.2.4.	HEAT SINK ASSEMBLY	37
APPENDIX A	D.C. OFFSET VOLTAGE ADJUSTMENT PROCEDURE	
APPENDIX B	AMPLIFIER BOARD CLAMPING VOLTAGE ADJUSTMENT PROCEDURE	
APPENDIX C	AMPLIFIER BOARD BIAS VOLTAGE ADJUSTMENT PROCEDURE (WITH POWER FETs WIRED)	
APPENDIX D	QUICK CHECK FOR POWER FET DAMAGE	
APPENDIX E	AMPLIFIER POWER UP WITHOUT THE PROTECTION BOARD ASSY.s	



## 1.0 INTRODUCTION

The Models A401M, A201S, and 401S are high frequency, high powered precision Class A audio amplifiers. All three units utilize the same chassis and the same basic circuitry. These units utilize MOSFETS in the output stages as well as in many of the low level stages. Therefore, service people must follow strict electrostatic discharge control procedures.

All amplifiers are burned in at the factory for at least 20 hours. This should significantly reduce the likelihood of early failure due to infant mortality or latent defects. The components used in the amplifier circuit are of the highest quality. They are tested for functionality and matched to their counterparts. The supporting protection circuitry uses high reliability industrial grade components. In this circuitry accuracy is not as significant an issue as it is in the audio stages, but reliability is.

Due to the complexity of the circuitry in these amplifiers, they are designed to be serviced in a modular fashion. When an assembly is not functioning properly the whole assembly should be replaced. In most cases attempts to service each separate assembly will not be cost effective. This is especially true in the amplifier circuitry where a failure in one device may cause damage to another device. This damage may not be apparent to the technician. Such damage, if it is not found and corrected, may result in another failure after the amplifier has been returned to the customer. If the unit is serviced in a modular fashion and the service procedures outlined in the following pages are adhered to, this should not occur.

This service manual is arranged in the following manner.

<u>Section</u>	<u>Subject matter</u>
2	Circuitry Description and Amplifier Functions
3	Amplifier Service, Component Replacement, and Calibration
4	Amplifier Diagnostics - Description of Normal Operation and Problem/Cause Table

The service technician should review all of sections 2, 3.0, 3.1, 3.2, 3.3.1.1., 3.3.1.2., 3.3.2.1., 3.3.2.2., 3.3.3.1., 3.3.3.2., 3.3.4.1., and 3.3.4.2. before performing any work or diagnostics on the amplifier. This will familiarize the technician with all the modes of amplifier operation as well as all the calibration procedures and how to perform them. Section 4 should be used to help identify the source of a problem. Once the problem is identified the appropriate procedure from section 3 should be followed if one of these major components requires replacement.

## 2.0 CIRCUIT DESCRIPTION

The overall amplifier circuitry consists of:

1. **LOW LEVEL AMPLIFIER CIRCUIT** - This is the voltage multiplication stages and the driver stage. This circuitry is contained on the Amplifier Board, assembly number 100016.
2. **AMPLIFIER OUTPUT CIRCUIT** - This is the power FETS and the power distribution circuitry. This circuitry is contained in part on the Heat Sink Assemblies, number 100020 (N channel power FET, type IRF230) and 100021 (P channel power FET, type IRF9230) and in part on the Distribution Board, assembly numbers 100018 (Mono - A401M) and 100019 (Stereo - A201S, 401S).
3. **POWER SUPPLY CIRCUIT** - This includes both the low level and the high level power supplies. This circuitry is divided between the Protection Board, assembly number 1000017, and the Amplifier Board, assembly number 100016.
4. **PROTECTION CIRCUIT** - This is the monitoring circuitry which performs power up and power down mute, overload detection and shutdown, heat sink temperature control, and input/output differential (clipping) detection.

An overall functional schematic is given in drawing 300018 accompanying this manual. The drawing shows the interaction of all the different circuitry. Each amplifier channel consists of identical circuitry. The monaural amplifiers use one channel of this circuitry to drive all the power FETS. In the stereo amplifiers each channel drives one half of the power FETS.

With the exception of the amplifier low level board, each circuit board is dedicated to only one of the above primary circuit functions. The overall amplifier wiring is given on the "Power Wiring Diagram", drawing number 300012, and the "Interconnection Wiring Diagram", drawing numbers 300013 (A401M) and 300014 (A201S and 401S). The interconnection of the different boards can be seen in these drawings. A more detailed breakdown of the functions of the amplifier board and the protection board are given in drawings 300016 and 300017 respectively. These are functional block diagrams for each board. The following describes the purpose and the circuitry of each board assembly used in the amplifier.

### 2.1 AMPLIFIER BOARD, ASSEMBLY NUMBER 100016

The amplifier board contains the following circuitry:

1. Low Level Amplifier Stages.
2. Amplifier Bias Adjust Circuitry (maintains the output FETS at 50°C).
3. Input/Output Comparator and the 1 Percent Distortion Detection/Hold Circuit.
4. LED Drive Circuitry.
5. Input Monitor/Amp Reset Circuit (Resets overload protection circuitry when the amplifier input signal is reduced to zero).



6. Regulated +/- 15V and -12V D.C. Supplies.
7. High Frequency Roll Off Input Filter/Select Switch.

The functional block diagram, drawing 300016, shows the interaction of these circuits in detail. Drawing 100016 shows the board layout for the major components.

The amplifier circuitry on the board consists of two voltage multiplication stages and one unity gain current buffering stage. The input stage is a differential J-FET stage cascoded by two high frequency, low level MOSFETs. This drives a differential predriver stage with a current mirror on the negative side of the differential amp. The predriver stage utilizes medium power high frequency NPN and PNP transistors. The output of the noninverting side of the differential predriver stage and the current mirror output are summed together at an adjustable bias network. The output of the biasing network drives the gates of two N channel and two P channel power driver MOSFETs. The MOSFETs are configured as unity gain source followers. The output of their sources go through FU1 and FU2. This signal exits the amplifier board and is carried to the distribution board where it is routed out to drive the gates of the output power MOSFETs. An adjustable bias voltage clamping network runs across the outputs of FU1 to FU2. This network is set to clamp the output bias voltage at a level which will protect the power MOSFETs from overbias in the case of a low level amplifier board failure. In the event of this the fuses FU1 and FU2 will blow and the power output stage will remain undamaged. FU1 and FU2 also prevent damage to the driver stage from high frequency, high power oscillations. Such oscillations draw large amounts of current from the driver stage. These fuses will blow before damage occurs. Such oscillations are caused by poor wiring techniques. See the Owners Manual for instructions on proper wiring. The symptoms of a blown fuse are described in section 3.3.2.2.1. "Fuse Replacement".

The amplifier board regulates the output stage, the power FET temperature and the heat sink temperature. The power FET temperature is communicated to the amplifier board from the protection board. The protection board monitors the power FET temperature via thermistors T1 and T2 (see drawings C300013 and D300014). The amplifier board compares the power FET temperature to a set point of 50°C (122°F). The circuitry on the amplifier board adjusts the bias voltage (which adjusts the idle bias current of the power FETs) either up or down as necessary to maintain the power FETs at 50°C. The range of bias adjustment which the amplifier board can perform is limited to approximately +/- 50% of the nominal bias current for power FETs. This is sufficient to allow the amplifier to warm up quickly and maintain the power FETs at their proper temperature under normal use. It does not allow the amplifier to reduce the bias to the point where the unit is no longer in class A operation.

The amplifier board contains the input/output (I/O) comparator circuitry and part of the distortion detection and display hold circuitry. The LED drive circuit is on the amplifier board. The LED drive signal is routed to the protection board via the ribbon cable. This signal is connected to the LED's by a terminal block on the protection board.

The I/O comparator is a simple differential circuit whose output is proportional



to the difference between the two inputs. The positive input of this differential amp is the amplifier input signal. The negative input of this differential amp is the amplifier output (degaigned to the level of the amplifier input). If there is a difference between the input and the (gain corrected) output waveforms of the amplifier this circuit will put out a voltage proportional to this difference. Such differences correspond either to a linear difference (such as an incorrect amplifier gain) or a nonlinear difference (distortion). If the protection circuitry has shut the amplifier off and there is an input, or if the amplifier is clipping (distorting) for some reason the circuit will provide an output signal proportional to the difference between the two inputs. It is noteworthy that D.C. voltage at the amplifier input will be detected as an input/output difference resulting in LED green or red indication. This is because the amplifier gain rolls off to unity gain at D.C. The I/O detection circuit compares the amplifier input to the amplifier output degaigned by 31.18. The unity gain of the amplifier at D.C. appears to be a gain error to the I/O detection circuit.

The output of the I/O comparator is routed to two distortion detection hold circuits. These circuits consist of a comparator with a preset trip level. The output of the comparators switch to a high voltage when the input from the I/O comparator exceeds this level. One of these circuits is set for any distortion level (or difference) exceeding 1% of the maximum amplifier output level. This circuit is very fast and can detect 1% distortion for a duration as short as 20 microseconds. This circuit also has a hold function which will continue to latch the output for 1 second after the distortion exceeds the comparator's "trip" level. The other distortion detect/hold circuit is slightly more complex and contains an integrator as well as a holding comparator. This circuit does not latch until the distortion time product exceeds 5 percent seconds (of the maximum amplifier output). This circuit also latches the output for 1 second after its "trip" level is exceeded. The output of these two distortion detect hold circuits is routed to the LED drive circuitry. The output of the 1% distortion detect/hold circuit commands the LED driver to display green. The output of the 5 percent-seconds detect/hold circuit commands the LED driver to display red. In the event both circuits are indicating the LED will display red. In most cases green indication caused by clipping is totally inaudible or barely audible. This is mainly because this circuit is much faster than the human ear. Red indication is definitely audible and can be dangerous to the speakers in the system. It is acceptable to play the amplifier at levels where green indication is occurring (even as much as 50% of the time) provided the speakers can handle the power level. If red indication occurs the volume should be reduced.

The protection board assembly contains all the circuitry associated with amplifier overload monitoring and amplifier shutdown. The amplifier board contains the circuitry which commands the amplifier shutdown circuit to reset. This "reset" circuit consists of a high gain op-amp circuit routed to a comparator. The high gain op-amp receives its input from the power amplifier input. The normal output of the comparator (with no input) commands the amplifier shut down circuit to reset. If the input of the comparator exceeds its trip level the comparator stops commanding the shut down circuit to reset. The net result is that the amplifier shut down circuit will reset as long as the input to the amplifier is less than that required to drive 0.1 volts RMS out of the amplifier. If

the input to the amplifier exceeds this level the shut down circuit will not reset. Thus, when an amplifier overload occurs the amplifier may be reset by turning the input signal all the way down to zero volts.

The amplifier board contains a high frequency roll off filter which has a selectable cut-off frequency. This circuit may be set (via switch SW1, see section 3.3.2.) to roll off all input signals above either 200 kilohertz or 3 megahertz at 6 dB/octave. The purpose of this circuit is to prevent unwanted RF from entering the amplifier input. Due to the wide bandwidth of this amplifier such signals will be amplified if permitted to enter the unit. The 3 megahertz setting is the normal input filter intended to be used when the amplifier is wired properly to a preamplifier or line input source compatible with the wide bandwidth of the amplifier. The 200 kilohertz setting is intended to be used when input or output wiring schemes are less than ideal or when the amplifier is to be used with a preamplifier which is not compatible with the full bandwidth of the amplifier. Proper amplifier wiring practices are described in the Owners Manual.

Preamplifiers which are incompatible with the full bandwidth of the amplifier typically do not have internal wiring sufficient for performance in the megahertz frequency range. At these high frequencies the channel to channel grounding scheme becomes critical. The loop area between a conductor and its ground (return path) must be minimized. Usually the most common problem with preamplifiers incompatible with this wide bandwidth is the presence of high frequency oscillations when in the mute mode of the preamplifier. This is because most mute circuits short the preamplifier output to the incorrect ground. On many preamplifiers the circuit designer simply selects the nearest ground. If the ground selected is not the same ground point as that routed to the output phono jack for that channel the result is a large antenna loop which picks up RF and causes oscillations. Note, a preamplifier which does not have a manual mute circuit (user selectable) does still contain a mute circuit. The mute circuit is automatically activated at preamplifier power up and power down.

Preamplifiers with a compatibility problem with the amplifier's full bandwidth will typically show the following symptoms when the input roll off filter is set for 3 megahertz.

1. In the manual mute mode or at preamplifier power up and power down the amplifier LED(s) will cycle on and off either green or red several times a second.
2. The cycling described in 1. will be accompanied by an audible popping from the speakers.
3. The amplifier may blow the amplifier board fuses, FU1 and FU2, on a regular basis (see section 3.3.2.2.1.)
4. The amplifier may sound harsh in the treble range when played at loud levels or may display green clipping earlier than expected.

If any or all of these symptoms is present when used with a specific preamplifier



the high frequency roll off switch on the amplifier boards, SW1, should be set in the 200 kilohertz position in accordance with section 3.3.2.2., item 4.

Finally, the amplifier board contains three potentiometers for board calibration. These potentiometers are used to manually adjust the amplifier board bias voltage, the amplifier board bias clamping voltage (described earlier in this section), and the amplifier output D.C. offset voltage. The adjustment of these potentiometers is described in section 3.3.2.2.

## 2.2. PROTECTION BOARD, ASSEMBLY NUMBER 100017

The Protection board contains the following circuitry:

1. Output FET Power Monitor/Overload Shutdown.
2. Output FET Temperature Monitor.
3. Power Up and Inrush Time Delay.
4. Distortion Detection Circuit, 5 Percent-Seconds and the LED Output Terminal Block.

The functional block diagram, drawing 300017, shows the interaction of these circuits. Drawing 100017 shows the board layout for the major components.

The majority of the components on the protection board are associated with the amplifier overload protection circuit. The purpose of this circuit is to monitor the power loading on the output FETs at all times. If the loading on the output FETs exceeds their capabilities, the overload protection circuit shuts the amplifier output down. This is accomplished by shutting off the bias current to the predriver stage. This effectively reduces the amplifier voltage gain to zero and turns off the output FET bias current. This shutdown scheme results in a protection circuit which has absolutely no effect on amplifier sound until shutdown has occurred. Once the protection circuit is triggered the shutdown circuit latches in the amplifier off condition. The circuit will not reset (and allow the amplifier to turn on again) until it receives a command from the amplifier board indicating the amplifier input signal has been reduced to an acceptable level (see section 2.1). A more complete description of how the overload protection circuit operates is given in the following paragraphs.

The power loading across the output FETs is calculated by multiplying the voltage across the output FETs by the current flowing through the output FETs. The voltage across the output FETs is obtained by subtracting the output voltage of the amplifier from the supply voltage. This operation is performed by a differential amplifier. The supply voltage for both the positive and negative supplies are stepped down to approximately +/- 4 volts. These voltages are routed into a selection switch which decides which supply voltage to monitor (dependent upon which FET type, N channel or P channel, is conducting the current to the load). This voltage is routed into the positive input of the differential amplifier. The negative input of the differential amplifier receives a stepped down version of the amplifier output voltage. This results in an output from

the differential amplifier which is proportional to the voltage across either the P channel or the N channel output FETs.

The current through the output FETs is determined by another differential amplifier. This differential amp receives its input from the milliohm shunt on the distribution board. The shunt is in series with the signal return from the load (speaker). The output of the differential amplifier monitoring this current shunt is proportional to the current being conducted through the output FETs.

A comparator circuit monitors the output FET current signal and determines the polarity of the output FET current. A positive polarity indicates the N channel output FETs are conducting the current to the load. A negative polarity indicates the P channel output FETs are conducting the current to the load. It is the output of this polarity detector which drives the solid state switches which select what output FET type (N channel or P channel) to monitor for voltage across the output FETs and for power loading of the output FETs.

The signal proportional to the voltage across the output FETs and the signal proportional to the current through the output FETs are routed to an analog multiplier. The output of the multiplier is proportional to the power loading of either the P channel or the N channel output FETs. This signal is sent to another signal routing select switch. This switch routes the signal to either the N channel or the P channel output FET monitor circuitry. The selection of where to route the signal is based on whether the signal exiting the multiplier corresponds to the power loading across the N channel output FETs or the P channel output FETs.

The N channel and P channel output FET monitor circuits are both identical. Each circuit begins with an analog circuit which mimics the time dependent thermal resistance characteristics of the output FETs. The signal representing the power across the output FETs is routed into this circuit. The output of the circuit is proportional to the temperature rise from the case to the junction of the output FETs. This temperature rise calculation takes into account the thermal time transient characteristics of the output FETs. If a short term power load transient occurs the circuit will lower the temperature rise calculated for the same power load as the duration of the power loading becomes shorter. For example, assume a 100 watt load on the output FETs corresponds to a 1 volt output from this circuit when the load is continuous. When the same load is applied for 10 milliseconds the circuit output would be 1/4 volt.

The signal which corresponds to the temperature rise from the case to the junction of the output FETs is routed to a comparator. The trip point of the comparator corresponds to the maximum allowable case to junction temperature rise for the output FETs. If this value is exceeded the comparator trips. The output from the comparators for both the N channel and the P channel output FET monitor circuits are sent through an OR Gate to a set/reset circuit. If either comparator trips, the set/reset circuit latches to an output which shuts the amplifier circuit off. The set/reset is only reset if the input to the amplifier is lowered to a level corresponding to an amplifier output voltage of 0.1 vrms (see Section 2.1).

The output of the set/reset is routed to an OR Gate. The output of the OR



Gate drives a transistor which produces the signal which commands the amplifier circuit into the "ON" state. If the OR Gate receives an overload signal from the set/reset the amplifier "ON" signal is discontinued and the amplifier circuit shuts down (see Section 2.1.). The OR Gate also receives an input from the power up time delay circuit and the circuit which monitors the supply voltage (to determine if a brown out condition is present on the AC power line). The net result is that the amplifier circuit will also shut down for the first 7 seconds at power up and whenever the AC line voltage falls below approximately 80% of the line voltage at which the amplifier is set to operate.

The power up time delay circuit also powers the coil to the inrush limiter bypass relay. This relay is open at power up. In this condition the only power provided to the large power transformer is through two 50 ohm, 20 watt resistors. This limits the maximum inrush current from the AC line to several amperes. Five seconds after the power switch is turned on the power up time delay circuit closes the inrush limiter bypass relay. This allows full power to flow to the large power transformer. Two seconds after this relay closes the power up time delay circuit turns the amplifier circuit on. This assures the amplifier circuit is not turned on until all the power supplies are fully charged. This minimizes the thump produced at the speakers when the amplifier is turned on.

The protection board monitors the temperature of the cases of the output FETs via thermistors T1 and T2. This signal is buffered by an operational amplifier. The output of this op. amp is routed to the amplifier board (see Section 2.1) and to the circuit which determines the maximum allowable temperature rise from the junction to the case of the output FETs. The maximum allowable temperature rise corresponds to  $150^{\circ}\text{C}$  minus the actual case temperature. (The maximum allowable junction temperature for the output FETs is  $150^{\circ}\text{C}$ ).

The protection board contains the circuit which drives the light in the power switch. This circuit consists of a circuit in series with the light which causes it to flash several times a second. This flashing circuit is bypassed by an optically coupled triac. The optically coupled triac is driven by the Q output from the overload set/reset circuit. If the amplifier is not in overload the triac bypasses the flashing circuit and the power switch light is steady.

The last set of circuitry contained in the protection board is the 5 percent-seconds distortion detection and hold circuit associated with the input/output comparator LEDs. The functional description of this circuit has already been given in Section 2.1.

### 2.3 DISTRIBUTION BOARD ASSEMBLY NUMBERS 100018 (A401M) AND 100019 (A201S, 401S)

The function of the distribution board assembly is to:

1. Distribute the power and the drive signal to the heat sink assemblies and to collect and route their outputs to the output binding post assemblies.
2. Monitor load current with a current shunt.

3. Provide a central ground point and a feedback signal for the amplifier board.
4. Decouple the power supplies and damp inductive ringing of the power supply wiring.

Drawing 300010 is the circuit schematic for the distribution board assembly. Drawings 100018 and 100019 are the board layout for the major components of the distribution board assembly.

The distribution board consists of two double sided PC boards combined together to provide a very low inductance distribution network for the ground, power, and output signals. The chassis ground is provided through the standoff mounts of the distribution board assembly.

#### 2.4 HEAT SINK ASSEMBLY, NUMBERS 100020 (IRF230) AND 100021 (IRF9230)

The functions of the heat sink assembly follows:

1. To provide the necessary heat sinking for the power FETs.
2. To provide a low inductance path for the gate drive, power supply, and power output signals of the power FETs.
3. To provide further damping of supply and ground noise ringing due to wiring inductances.
4. To provide a mounting location for the power FET source degradation resistors and gate stability resistors.

Drawing 300011 is the circuit schematic and drawing 100020/21 is the assembly drawing for the heat sink assembly.

Each heat sink assembly contains a single PC board which is mounted by the same screws which mount the power FETs. The board is insulated from the heat sink assembly by fiber shoulder washers. Each FET is insulated from the heat sink by special low dielectric constant mounting insulators. The cable used on these assemblies is a custom low inductance triaxial configuration.



### 3.0 AMPLIFIER SERVICE

The Amplifier is intended to be serviced in a modular fashion. If an assembly is not functioning properly it is to be replaced by a new assembly. A list of all the basic electrical and electromechanical assemblies follows:

<u>ASSEMBLY NO.</u>	<u>DESCRIPTION</u>
100016	Low Level Amplifier Board
100017	Protection Board
100018	Distribution Board, Mono
100019	Distribution Board, Stereo
100020	Heat Sink Assembly, IRF230
100021	Heat Sink Assembly, IRF9230
100022	Cable Assembly, Triaxial (power FET drive)
100023	Thermistor Assembly
100024	Cable Assembly, Ribbon
100025	Cable Assembly, Coaxial (Dist. board to amp. board)
100030	Set of 4 Matched Heat Sink Assemblies
100031	Set of 8 Matched Heat Sink Assemblies
100033	Transformer Assembly, Low Level
100034	Binding Post Assembly, Output

The heat sink assemblies are typically purchased in sets of 4 or 8 which include the FET drive cables and the thermistor assemblies. The following sections describe the selection and replacement procedures for each of the major assemblies.

### 3.1 GENERAL PRECAUTIONS

1. Be sure amplifier A.C. Power cord is unplugged.
2. Be sure main power supplies are discharged. If the amplifier has been powered up recently the power supplies take at least 15 minutes to discharge. If they are not discharged they may be discharged by shorting each supply terminal to ground (the bus bar) with a 20 watt or larger power resistor between 10 and 50 ohms. Be sure to check each supply after this operation to see if it has been properly discharged.
3. Follow standard precautions for working on static discharge sensitive devices when servicing the amplifier. Be sure the service technician is grounded to the amplifier ground or chassis with a wrist strap at all times when working on the amplifier. NOTE: The amplifier output devices as well as many of the devices on both the amplifier boards (assembly No. 100016) and the protection boards (assembly No. 100017) are static sensitive. The boards should be handled following ESD precautions both in and out of the amplifier.
4. The terminal block pins which solder to the PC board are sensitive to over torquing. Use the following procedure when tightening or loosening the PC board mounted terminal blocks:
  - a. Always hold the body of 2 point terminal blocks when tightening or loosening them to prevent rotation.
  - b. Tighten PC board mounted terminal blocks to 3 inch-pounds of torque. Do not exceed 4 inch-pounds of torque.
  - c. Always tighten terminals twice - First initially, then once again after 5 to 10 minutes. This prevents the terminal block from loosening due to relaxation of the metal in the wire lead tip.
  - d. The operator should always be aware that the terminal block leads to the board can break and should watch for this. A broken connection to the gate or the source of a power FET can destroy the device.
5. The stand-offs used to mount the PC boards should be tightened to 3 inch-pounds of torque and should not exceed 4 inch-pounds. Overtorquing these units can result in breaking them.
6. The service technician working on the amplifier should always have another service technician check his wiring connections for conformance to the prints when he is finished. An incorrect wire termination can cause destruction of the amplifier.
7. When working on the amplifier boards (assembly No. 100016) or the protection boards (assembly No. 100017) always check the ribbon cable connections to PLL at both ends to be sure they have not been pulled out of their plug connections.



8. Do not connect or disconnect the amplifier inputs while the unit is on. This promotes input/output coupling which can cause high frequency oscillations and may blow the amp board fuses.(See owners manual).

9. Always short the heat sink assembly leads together for each assembly if they are disconnected from the distribution board. This prevents the possibility of damage from static discharge.

10. Do not touch any components while the amplifier is on, especially the power FETs. Many of the component cases are at high voltage while the power supplies are charged.

11. Do not operate the amplifiers at high frequency at high power. This will overpower the output stability network. The maximum allowable frequency at full power is 60KHZ for sine waves and 20KHZ for square waves. For lower power levels the maximum frequency may be determined from the waveform peak voltage,  $V_{peak}$  by:

SINE WAVE:

$$\text{Maximum frequency(KHZ)}=60 \times (80/V_{peak})^2$$

SQUARE WAVE:

$$\text{Maximum frequency(KHZ)}=20 \times (80/V_{peak})^2$$

### 3.2 LIST OF DRAWINGS

The following list gives the drawing numbers and titles of all the drawings required to service the A201S, A401M, and 401S amplifiers. One copy of each drawing is provided with this service manual. The drawings are listed in numerical order.

<u>DRAWING NO.</u>	<u>TITLE</u>	<u>USED ON</u>
B100016	Board Layout, Amplifier Board Assembly.	All
B100017	Board Layout, Protection Board Assembly.	All
A100018	Board Layout, Mono Distribution Board Assembly.	A401M
A100019	Board Layout, Stereo Distribution Board Assembly.	A201S, 401S
B100020/21	Assembly, Heat Sink.	All
C300010	Circuit Schematic, Distribution Board.	All
A300011	Circuit Schematic, Heat Sink Assembly.	All
C300012	Power Wiring, Amplifier Assembly.	All

<u>DRAWING NO.</u>	<u>TITLE</u>	<u>USED ON</u>
C300013	Interconnection Wiring Diagram, Amplifier Assembly (mono).	A401M
D300014	Interconnection Wiring Diagram, Amplifier Assembly (stereo).	A201S, 401S
A300015	Line Voltage Selection Wiring, TB2 and TB5.	All
B300016	Block Diagram, Assembly No. 100016 Low Level Amplifier Board.	All
B300017	Block Diagram, Assembly No. 100017 Protection Board.	All
B300018	Block Diagram (simplified), Overall Amplifier Assembly.	All

### 3.3 BOARD REPLACEMENT

#### 3.3.1. BOARD REPLACEMENT, PROTECTION BOARD ASSEMBLY NO. 100017

3.3.1.1. BOARD SELECTION: There are two types of protection boards. They differ from one another by the amount of voltage step down they use in the circuits which monitor the amplifier output and the supply voltages. One is intended to be used with the higher voltage 400 watt amplifiers and the other with the 200 watt amplifiers. Protection board assembly selection should be in accordance with the following.

<u>ASSEMBLY NUMBER</u>	<u>USE WITH AMPLIFIER MODEL NUMBER</u>
100017-1	A401M and 401S
100017-2	A201S

3.3.1.2. BOARD CALIBRATION: All protection board assemblies are calibrated at the factory. No further calibration is required when they are installed in the amplifier. Do not attempt to adjust any of the potentiometers on the board without consulting the factory.

#### 3.3.1.3. PROTECTION BOARD REPLACEMENT PROCEDURE

1. Configure T13 and T14 on the protection board in accordance with the appropriate interconnection wiring diagram 300013 for the model A401M and 300014 for the models A201S and 401S.



2. Follow the general precautions of section 3.1. Wire the new protection board into the amplifier in accordance with the following drawings.

<u>DRAWING NO.</u>	<u>DESCRIPTION</u>
B100017	Major Component Layout, Protection Board Assembly
C300013	Interconnection Wiring Diagram - A401M
D300014	Interconnection Wiring Diagram - A201S, 401S

3. Have another technician verify all wiring and connections made.

4. If no other boards were replaced perform the amplifier power up procedure given in Steps 14 thru 21 of Section 3.3.2.3. "AMPLIFIER BOARD REPLACEMENT PROCEDURE". If any other boards were replaced perform the amplifier power up described in section 3 of this manual for the board type of the other board which was replaced. The burn in described in Item 22 of Section 3.3.2.3 is optional if the protection board assembly was the only board replaced.

### 3.3.2 BOARD REPLACEMENT, AMPLIFIER BOARD ASSY. NO. 100016

3.3.2.1. BOARD SELECTION: The same amplifier board is used in all models. The Assembly number is 100016.

3.3.2.2. BOARD CALIBRATION: The amplifier board has three potentiometers and one switch which require adjustment. These are:

- P1 DC Offset Voltage, Amplifier Output
- P2 Bias Voltage, Power FETs
- P3 Clamping Voltage, Output Bias
- SW1 Frequency Select, Input Filter

See Drawing 100016, board layout, for the location of the devices and Drawing 300016 block diagram for a functional description of the circuits. These values should be adjusted in accordance with the following either before or during installation and power up.

1. DC OFFSET VOLTAGE, P1 - This pontentiometer will come preadjusted from the factory, but it may require some fine trimming. This should be done during preliminary power up without the power FETs wired to the distribution board when possible (See Section 3.3.2.3.). Adjustment may also be done with the power FETs connected. To adjust the offset voltage perform the procedure listed in Appendix A.

2. OUTPUT BIAS CLAMPING VOLTAGE, P3 - This pontentiometer must be adjusted to match the board to the output power FETs with which the board will be used. If the board clamping voltage has already been set at the factory, the value to which it is set will be written on

a sticker on top of one of the two large heat sinks (For Q14 thru Q17) at the front of the amplifier board assembly (see Drawing 100016). The value to which the clamping voltage is to be set for is determined from the gate to source bias voltages of the power FETs with which the board will be used. The correct clamping voltage is determined as follows:

$$V_{\text{clamp}} = \text{Average of the IRF230 } V_{\text{gs}} \text{ (gate to source matching voltage)} + \text{Average of the IRF9230 } V_{\text{gs}} + 0.8 \text{ volts}$$

The gate to source matching voltage of the power FETs are labeled on each FET with a small stick-on label. The values in any matched group (per channel or per amplifier) are typically within 0.04 volts of each other. An example of the determination of the correct clamping voltage for an amplifier board follows:

If IRF230  $V_{\text{gs}} = 3.41$  to  $3.45$  volts  
IRF9230  $V_{\text{gs}} = 3.96$  to  $4.00$  volts

Then  $V_{\text{clamp}} = 3.43 + 3.98 + 0.8$   
 $= 8.21$  volts

Determine the correct value of the clamping voltage for the board from the  $V_{\text{gs}}$  of the FETs with which the board will be used. For the stereo models the heat sinks associated with the right channel are the center four heat sinks. The two front and two rear heat sinks are associated with the left channel of the stereo models (see dwg. D300014). If the clamping voltage labeled on the board is incorrect or if the board has no clamping voltage labeled on it follow the procedure in Appendix B and adjust the clamping voltage.

3. POWER FET BIAS VOLTAGE, P2 - The power FET bias voltage should always be checked when putting in a new board and should be adjusted as necessary. The adjustment should be made during the preliminary power up without the power FETs wired to the distribution board where ever possible (see Section 3.3.2.3). The procedure for the adjustment with the power FETs wired to the distribution board is given in Appendix C.

4. INPUT FREQUENCY SELECT SWITCH, SW1 - This switch selects the cut off frequency for the low pass input filter. This filter may be adjusted to roll off all input signals above either 200 Kilohertz or 3 Megahertz. The switch should be adjusted to the desired setting whenever installing a new amplifier board. The switch comes preset from the factory to the 200 Kilohertz position. A more complete description of this circuit and its purpose is given in section 2.1. If this switch is to be adjusted with the amplifier board mounted in the amplifier this must be done with the amplifier off. The switch is located underneath the protection board(s) when the amplifier board is mounted in the amplifier. The switch may be accessed from the front of the amplifier with a long insulated shaft probe or a similar device such as a pencil. The correct position is shown on drawing 100016 for each setting. If the equipment with which the amplifier is to be used is unknown the 200 Kilohertz setting is preferred.



#### 3.3.2.2.1. FUSE REPLACEMENT

The low level amplifier board fuses FU1 and FU2 are located at the front of the amplifier board in accordance with the component layout drawing Bl00016. The purpose of these fuses is described in Section 2.1 of this Manual.

An amplifier with one blown fuse will show the following symptoms:

1. With no signal an audible hum and increased noise will be present at the output. This hum and noise will still be fairly quiet.
2. The amplifier channel will sound harsh and somewhat lacking in dynamics.
3. The amplifier channel will clip early (From 1/2 to 1/10 the normal clipping level depending on speaker load and frequency).
4. The heat sinks associated with the channel will not warm up at idle. On a stereo amp the center four heat sinks are used for the right channel and the front and rear sets of heat sinks are used for the left channel. Note, some warming of the heat sinks may be caused by high power operation or convective heating from the other channel heat sinks.

An amplifier with two blown fuses will show the following symptoms:

1. Significant audible hum and noise will be present on the the affected channel at all times.
2. The channel will not put out any signal.
3. Clipping will occur almost immediately due to the lack of output.
4. The heat sinks on the channel will not warm up at idle.

If a blown fuse is suspected the fuse continuity should be checked. A good fuse will measure about 1.5 to 3 ohms resistance for the 1/8 amp fuses. Some early amplifiers used 1/16 amp fuses. The resistance of these fuses is 5 to 10 ohms. Verification of continuity may be done directly in the fuse mount by measuring from one of the fuse holder mounting posts to the other. If a fuse is blown replace it. If the fuse(s) continue to blow on power-up something is wrong with the amplifier or the equipment hook-up. Consult the diagnostic section of this Service Manual.

#### 3.3.2.3. AMPLIFIER BOARD REPLACEMENT PROCEDURE

1. If necessary, adjust the clamping voltage of the new amplifier board. See Section 3.2.2. Step 2 and Appendix B.
2. Follow the General Precautions in Section 3.1. Wire the new amplifier board into the amplifier in accordance with the following drawings:

<u>DRAWING NO.</u>	<u>DESCRIPTION</u>
B100016	Major Component Layout, Amplifier Board
C300013	Interconnection Wiring Diagram - A401M
D300014	Interconnection Wiring Diagram - A201S, 401S

Be certain to bend the ribbon cable connecting the right channel amplifier board to the right channel protection board in a manner to prevent contact between the bottom of the protection board and the cable.

3. Have another technician verify all wiring and connections made.
4. Disconnect the power FET heat sink assemblies from the distribution board for the channel being serviced.

Reference the following drawings:

<u>DRAWING NO.</u>	<u>DESCRIPTION</u>
A100018	Major Component Layout, Distribution Board - A401M
A100019	Major Component Layout, Distribution Board - A201S, 401S
C300013	Interconnection Wiring Diagram - A401M
C300014	Interconnection Wiring Diagram - A201S, 401S

Short the exposed leads of each of the disconnected heat sink assemblies together with an insulated wire nut or some other insulated shorting device. This will protect these assemblies from static electricity. If there is any possibility the damage on the amp board being replaced could have damaged the power FETs the heat sink assemblies should be checked. (For example, if the amp board fuses FU1 and FU2 blew). A quick check to verify whether there is power FET damage is outlined in Appendix D.

5. Using a small piece of bus wire, short TB2-2 to TB2-3 on the distribution board assembly (Assy No. 100018 for A401M and 100019 for A201S or 401S). This bypasses the output FETs and allows the amplifier board to operate with feedback as a low power amplifier. Be sure the jumper is placed correctly. Incorrect placement will destroy the amplifier board.



6. With the amplifier off connect the following test equipment to the channel for the unit being serviced.

<u>EQUIPMENT</u>	<u>SETTING</u>	<u>CONNECT TO</u>
*Signal Generator	1KHZ SINE WAVE Min Amplitude	Amplifier Input
Oscilloscope	0.2 Milliseconds/Div. 50 Volts/Div D.C. coupled.	Amplifier Output binding posts.(Gnd to "-", Signal Probe to "+")
D.C. Volt Meter with probe tip test leads with an insulated probe shaft	200, 20, 2 or .2 volt range depending on Proc. Step No. (or range sufficient to measure supply voltages and FET bias voltage).	Monitor test points specified in following steps.

NOTE - If the signal generator has a D.C. offset voltage at the output greater than 0.1 VDC this will cause the amplifier clipping indication to illuminate green or red. This will not harm the unit.

7. Leave the signal generator off. Power up the Amplifier. Monitor the amplifier output of the channel being serviced on the oscilloscope. The inrush limiter bypass relay should close in about 5 seconds after power up. Another 5 seconds after the relay closes the amplifier output should power up. The scope trace should jump slightly (up to possibly 20 volts) and then settle back to zero volts D.C.

8. Set the volt meter for the 200 volt range. Monitor the main power supplies. The two large capacitors in the front section of the unit are C1 and C2. The two large capacitors on the shelf in the low level section of the unit (with the amplifier boards) are C3 and C4. The supply voltages should agree with the following:

<u>MODEL</u>	<u>C1</u>	<u>C2</u>	<u>C3</u>	<u>C4</u>
A201S	+65	-65	+90	-90
A401M, 401S	+90	-90	+115	-115

NOTE - If your A.C. line voltage is not equal to the amplifier setting for A.C. line voltage the above voltages will change.

9. Set the volt meter to the 20 volt range. Monitor the FET bias voltage at the amplifier board being serviced. This reading is made from TB3-1 (volt meter positive lead) to TB3-4 (volt meter negative lead) on the amplifier board, Assy. No. 100016. The bias voltage should initially read between 0.6 and 1.0 volts less than the amplifier board clamping voltage (labeled on top of the heat sinks for Q14 thru Q17 on the amplifier board assembly). This value will be increasing slowly due to component warm up. If the bias voltage is within less than 0.6

volts of the clamping voltage while the board is still cold adjust P2 on the amplifier board with an insulated adjustment tool until the bias voltage is 0.8 volts less than the clamping voltage. For example, if the amp board being serviced is labeled with a clamping voltage of 7.8 volts the bias voltage should read between 6.8 and 7.2 volts when the amp is first powered up. If the bias voltage reads greater than 7.2 volts initially adjust P2 until the bias voltage reads 7.0 volts. This adjustment is not critical since the adjustment will be repeated once the board is warm (Approx. ½ hour after power up). See Appendix B if this adjustment is to be made with the power FETs connected.

10. Remove the volt meter leads from the amplifier. Change the volt meter scale to 2VDC. Monitor the amplifier offset voltage at the output binding posts of the amplifier channel being serviced. The D.C. offset voltage should be no more than +/- 0.02 VDC. If the offset is greater than this adjust P1 on the amplifier board in accordance with Appendix A. Note, the D.C. offset voltage on the amplifier board comes preadjusted from the factory. If the D.C. offset voltage of a new board is greater than +/- 0.1 VDC something is probably wrong.

11. Set the volt meter on the 200 millivolt range. Be certain the probes being used have an insulated shaft with only the last 0.1 inches or less of probe exposed. Locate R44, R45, R49 and R50 on the amplifier board being serviced (refer to drawing 100016 for the location of these resistors). Make the following measurements across these resistors being very careful not to short the probe tips to any other components or heat sinks. The location of the amp board top, bottom, front, and rear are defined on drawing 100016.

Measure

<u>From</u>	<u>To</u>	<u>Correct Reading</u> (in millivolts)
Rear lead of R45	Front lead of R45	0.0
Rear lead of R45	Bottom lead of R44	0.0
Rear lead of R49	Front lead of R49	0.0
Rear lead of R49	Bottom lead of R50	0.0

12. Remove the volt meter leads from the output binding posts. Monitor the amplifier output on the oscilloscope. Turn the signal generator on. Increase the signal generator until the sine wave on the scope visibly clips. The waveform should clip first on the negative half of the wave. The amplifier L.E.D. on the front panel should illuminate green. Increase the level until the positive half of the waveform shows visible clipping on the scope. The front panel L.E.D. should light red. The peak voltages of the waveform on the scope at clipping should roughly agree with the following:



<u>AMPLIFIER MODEL NO.</u>	<u>NEGATIVE HALF OF WAVEFORM</u>	<u>POSITIVE HALF OF WAVEFORM</u>
A401M, 401S	- 90 volts	+ 110 volts
A201S	- 70 volts	+ 90 volts

Note, these voltages are dependent on the supply voltages and will shift if the supply (or A.C. line) voltage changes.

13. Turn the signal generator amplitude all the way down and turn it off. Let the amplifier warm up for at least  $\frac{1}{2}$  hour. Once the amplifier board is warm monitor the FET bias voltage in accordance with Step 9. The bias voltage of the warm amplifier board should be 0.3 volts lower than the clamping voltage labeled on the board. Adjust P1 following the procedure outlined in Step 9 until the bias voltage is 0.3 volts less than the clamping voltage (i.e. If the clamping voltage is 7.4 volts adjust the bias voltage to 7.1 volts D.C.).

14. Turn the amplifier off and disconnect the test equipment. Discharge the power supplies (See Item 2 of Section 3.1 "GENERAL PRECAUTIONS"). Remove the jumper from TB2-2 to TB2-3 of the distribution board. Connect the heat sink assembly cables to the distribution board in accordance with the following drawings:

MONO AMPLIFIER - A401M

<u>DRAWING NO.</u>	<u>DESCRIPTION</u>
A100018	Major Component Layout, Distribution Board, Mono
C300013	Interconnection Wiring Diagram, Mono

STEREO AMPLIFIERS - A201S, 401S

<u>DRAWING NO.</u>	<u>DESCRIPTION</u>
A100019	Major Component Layout, Distribution Board, Stereo
D300014	Interconnection Wiring Diagram, Stereo

Have another technician check the wiring to be sure there are no errors.

15. Disconnect the inrush limiter bypass relay, K1, from the protection board assembly, 100017. (See Dwgs. B100017 and C300013 (Mono) or D300014 (Stereo)). Insulate the loose lead ends to prevent them from shorting to anything. Disconnecting the relay will prevent it from closing and bypassing the inrush limiters. If there is a mistake or problem the current provided to the power FETs will be limited to a low enough level to prevent damage to them at the expense of the inrush limiters.

16. Connect the oscilloscope and the signal generator to the amplifier again (see Step 6). Leave the signal generator off.

17. Perform this step quickly because the inrush limiters will overheat if the amplifier is on with the relay disconnected for longer than several minutes.

Power up the amplifier monitoring the scope. The trace should jump slightly about 10 seconds after the unit is powered up. This indicates the amplifier channel is on. Verify the following with the volt meter:

- Output offset voltage is less than +/- 0.04 VDC (see Step 10)
- The FET bias voltage is between 0.6 and 1.0 volts less than the clamping voltage (See Step 9, measure from TB3-1 to TB3-4 on the amplifier board).

Remove the volt meter leads from the amplifier. Turn the signal generator on. Increase the signal generator amplitude until the signal on the oscilloscope visibly clips. This should occur at approximately +/- 70 to 80 volts for the A401M or the 401S and approximately +/- 50 to 60 volts for the A201S. The clipping value is degraded by the current limiting of the inrush limiters. Verify the LED on the front panel lights green for mild clipping red for severe clipping. Turn the signal generator amplitude all the way down and turn the amplifier and signal generator off.

NOTE - If there is a problem in this step typically the amplifier output will have a large D.C. offset voltage which can be seen on the scope. If a large D.C. offset appears quickly shutting off the power may save the inrush limiters from burning up. At power up D.C. offset voltages up to 3 volts are normal for the first 10 seconds of operation if there is no load connected to the amplifier. After the first 10 seconds the D.C. offset should jump to zero as the amplifier circuit turns on.

18. Disconnect the test equipment. Discharge the main power supplies. Reconnect the relay leadwires, K1, to the protection board 100017. (See Step 15).

19. If possible connect a load bank to the output of the amplifier. The load size should be in accordance with the following:

<u>AMPLIFIER MODEL NO.</u>	<u>LOAD SIZE</u>
A201S, A401M	2 ohm, 400 watts min.
401S	4 ohm, 200 watts min.

If a load bank of higher resistance (for example 8 ohms) is all that is available this may be used. In this case the load bank should be capable of handling 1/4 the rated output of the amplifier into the impedance of the load bank. Connect the scope and signal generator to the amplifier again. If a load bank is not available perform the following steps without a load except skip the burn in.



20. With the signal generator off power up the amplifier. Verify the D.C. offset voltage (Step 10) and the FET bias voltage (Step 9) again with the volt meter. Let the amplifier idle with no signal for about ½ hour. Monitor the D.C. offset voltage and use P1 to adjust the offset voltage to zero. Disconnect the volt meter leads. Place your hand on each heat sink assembly one at a time and verify they are all warm and producing heat (a cold heat sink assembly means the power FETs are not conducting current or receiving a supply voltage. In this case there is probably a wiring error).

21. Turn the signal generator on. Turn the amplitude up until the waveform on the oscilloscope clips. Do this quickly to prevent the load bank from over heating. Verify both green and red indication of the L.E.D. on the front panel. Turn the signal generator amplitude down all the way.

22. To burn in the amplifier adjust the signal generator amplitude until the waveform peak voltage agrees with the following:

<u>MODEL NO.</u>	<u>PEAK WAVEFORM VOLTAGE</u>	<u>RMS EQUIVALENT</u> (for reference only)
A201S	30V	21V
A401M & 401S	40V	28V

Leave the amplifier at this level for burn in for 4 to 8 hours. Upon completion disconnect all equipment. The amplifier is ready for use.

### 3.3.3. BOARD REPLACEMENT, DISTRIBUTION BOARD ASSEMBLY NUMBERS 100018 (MONO) and 100019 (STEREO)

#### 3.3.3.1. BOARD SELECTION.

There are two major assembly numbers for the distribution board assembly. They differ from one another in the number of heat sink assemblies they accommodate. Distribution board assembly selection should be in accordance with the following:

<u>ASSEMBLY NUMBER</u>	<u>USE WITH AMPLIFIER MODEL NUMBER</u>
100018 - 0.83	A401M
100019 - 1.3	A201S
100019 - 1.7	401S

The base assembly number indicates whether the distribution board is mono, 100018, or stereo, 100019. The dash number after the main assembly number indicates the current shunt resistance in milliohms. All mono distribution boards, Assy. No. 100018, come precalibrated from the factory to 0.83 milliohms. The stereo distribution boards may be purchased either precalibrated or as the basic assembly 100019. In the latter case the assembly must be calibrated before use. Assemblies which have already been calibrated may be readjusted to a new shunt resistance also. See the following section for the calibration procedure.

### 3.3.3.2 BOARD CALIBRATION

Perform the following procedure on the distribution board assembly to be calibrated with a precision  $1 \pm 0.02$  amp DC current supply and a millivolt meter capable of at least 1/10th of a millivolt resolution.

1. Connect the millivolt meter across the last two terminals of TBl (TBl-11 and TBl-12 for Assembly Number 100018, TBl-10 and TBl-11 for Assembly Number 100019).
2. Connect the DC current supply from TBl-2 to TB4-1.
3. The shunt will be trimmed to the correct value by cutting through part of the shunt trace with a utility knife or a razor blade. Refer to drawing 100016 Note 2 for the location in which this cutting will be performed. See section 3.3.3.1 of this manual and determine the correct value, in milliohms, for which the shunt will be trimmed.
4. Turn on the D.C. current supply. Monitor the voltage reading on the DC millivolt meter. The reading on the meter in millivolts corresponds to the shunt resistance in milliohms. Note, the shunt trimming is performed in two cuts through the trace. Refer to drawing 100016. One cut is from the center of the trace to the edge of the trace. The other cut is along the center of the trace beginning at the first cut. See the old distribution board for reference if necessary.
5. Perform the cut from the center of the trace to the edge with the utility knife. Start the cut in the trace center to avoid overcutting. Be sure the cut goes all the way through the copper of the trace. Run the knife along the cut several times to be certain of this. The reading on the millivolt meter should not change significantly during this operation.
6. Monitoring the millivolt meter very carefully perform the second cut along the trace center in accordance with the following. Begin the cut at the center on the end point of the first cut. Be certain no trace metal bridges from one side to the other side of either cut, especially where two cuts intersect. As the cut is performed the value on the millivolt meter should increase with cut length. Periodically stop and run the utility knife along both cuts to be sure no metal is bridging across the cuts. Continue performing the cut along the trace center until the millivolt meter reads the desired resistance in milliohms. At this point the trimming is complete.  
  
If the second cut is made too long by mistake use solder or a combination of solder and copper foil tape to shorten the length of the cut along the center by filling in the end of this cut. Be sure to let the trace cool before remeasuring the value of the shunt on the millivolt meter. The hot trace has a higher resistance reading. Perform recutting and resoldering of the center cut until the correct shunt resistance value is obtained.
7. Disconnect the test equipment. Using a permanent marker, write the resistance value to which the shunt is calibrated on the board in milliohms.



Note, if the board in stock is already calibrated to the wrong resistance value the board may be recalibrated using the same technique described to correct errors in Step 6. of the Calibration Procedure. Use acetone to wash off the old calibration number when complete and write the new value on the board.

### 3.3.3.3. DISTRIBUTION BOARD REPLACEMENT PROCEDURE

Follow the general precautions of Section 3.1. Wire the new distribution board into the amplifier in accordance with the following Drawings, except DO NOT wire the heat sink cable assemblies to the board.

<u>DRAWING NO.</u>	<u>DESCRIPTION</u>
A100018	Major Component Layout, Distribution Board Assembly - A401M
A100019	Major Component Layout, Distribution Board Assembly - A201S, 401S
C300013	Interconnection Wiring Diagram - A401M
D300014	Interconnection Wiring Diagram - A201S, 401S

2. Have another technician verify all wiring and connections made.
3. Perform the amplifier power up procedure given in Steps 4 thru 22 of Section 3.3.2.3. "AMPLIFIER BOARD REPLACEMENT PROCEDURE".

### 3.3.4. BOARD REPLACEMENT, HEAT SINK ASSEMBLY NUMBERS 100020 (N CHANNEL MOSFET) AND 100021 (P CHANNEL MOSFET).

#### 3.3.4.1. ASSEMBLY SELECTION.

The heat sink assemblies are grouped according to MOSFET type (N channel and P channel) and amplifier power into 8 ohms (200 watts or 400 watts). Heat sink assembly selection should be in accordance with the following:

<u>*BASIC HEAT SINK ASSEMBLY PART NUMBER</u>		<u>PART NUMBER FOR A SET OF MATCHED ASSEMBLIES</u>		<u>USE WITH AMPLIFIER MODEL NUMBER</u>
N CHANNEL MOSFETS (IRF230)	P CHANNEL MOSFETS (IRF9230)	2 N CHANNEL AND 2 P CHANNEL MOSFET ASSEMBLIES (1 STEREO AMPLIFIER CHANNEL)	4 N CHANNEL AND 4 P CHANNEL MOSFET ASSEMBLIES (1 ENTIRE AMP.)	
100020-.47	100021-.47	100031-.47	100030-.47	A201S
100020-.82	100021-.82	100031-.82	100030-.82	401S
100020-.82	100021-.82	NOT APPLICABLE	100030-.82	A401M

\* These part numbers are given for reference to the amplifier assembly

drawings only. The heat sink assemblies are to be ordered by the matched set part numbers (Basic P/N 100030 and 100031, see Table).

The heat sink assemblies on each amplifier channel must be matched to one another. Sets of 4 and 8 matched heat sink assemblies can be purchased from the factory. The part number required to order a matched set of either 4 heat sink assemblies (one stereo channel) or 8 heat sink assemblies (one entire amplifier) is given in the heat sink assembly selection table listed previously in this section. Once replaced the remaining damaged heat sink assemblies should be returned to the factory for rework provided the condition of the heat sinks themselves are physically good (no severe scratches or dents).

#### 3.3.4.2. ASSEMBLY CALIBRATION.

The heat sink assemblies require no calibration; however, the amplifier board assembly to be used with the new heat sink assemblies must be calibrated in accordance with section 3.3.2.2, item 2. This is required to match the amplifier board clamping voltage with that required for the new heat sink assemblies.

#### 3.3.4.3. HEAT SINK ASSEMBLY REPLACEMENT PROCEDURE.

1. Remove the old heat sink assemblies. Save the mounting hardware and the FET covers. Be careful not to scratch the old heat sink assemblies so they may be returned for rework. Be sure to follow the general precautions listed in section 3.1.
2. Using a scribe or an equivalent tool, open up all the terminals in TB2 and TB3 on the distribution board so the new heat sink assembly leads may be installed easily.
3. This step is only to be performed if the new set of heat sinks is the matched set of 8, 100030-.82. This set may be used in either the model A401M or the model 401S. This set of assemblies includes the cable tags for both types of amplifiers on the end of the cables. It also includes both stereo amplifier thermistor assemblies. See the Interconnection Wiring Diagrams C300013 (mono) and D300014 (stereo).

For the matched set of assemblies 100030-.82 remove the cable tags which are not associated with the assembly being serviced. If the heat sinks are to be used on a mono amplifier A401M remove the stereo thermistor cable assembly T2 in accordance with the following:

- 3a. Pick up the heat sink assembly which has thermistor T2 mounted on it. Hold the heat sink assembly horizontal with the power FETs facing down. Keep the heat sink assembly in this position during the entire operation. This prevents the washers which are placed between the heat sink board and the heat sink itself from sliding out of place while the screw mounting the thermistor is removed (reference drawing 100020/21).



3b. With one finger over the head of the screw mounting the thermistor assembly T2 use a nut driver to remove the nut from the other side of the screw. Be careful to grab the nut once removed so it does not slip under the board.

3c. Carefully pull the loose screw out of the heat sink and out of the ring lug on the thermistor T2. The thermistor is free now to be removed. Replace the screw into the heat sink without the ring lug of the thermistor attached. Be sure the lock washer on the screw remains in place.

3d. Again with one finger over the head of the screw put the nut back on the other side and hand tighten it. The heat sink may now be held in any orientation.

3e. Using a torque screwdriver and a nut driver (or a torque nut driver and a screwdriver) tighten the nut on the screw to 4 inch-lbs of torque.

3f. Remove the loose thermistor from the heat sink assembly.

4. Again following the general precautions of section 3.1 mount the new heat sink assemblies onto the amplifier in accordance with the following drawings. Do not wire the cables of these assemblies into the distribution board.

<u>Drawing</u>	<u>Description</u>
C300013	Interconnection Wiring Diagram, Mono
D300014	Interconnection Wiring Diagram, Stereo

Be careful when routing the cables not to rip through the outer jacket of the cable assemblies. A short between the conductor under this jacket and the chassis will cause amplifier damage. Using cable ties, tie the cables down in a manor to prevent any of the cables from pressing against any sharp objects or high voltage conductors. Be especially careful of the small power transformer in the front section, the inrush limiting relay, and the power distribution terminal block mounted on the case inside wall adjacent to the distribution board assemblies.

5. Perform the amplifier power up procedure in accordance with steps 4 thru 22. of section 3.3.2.3 "AMPLIFIER BOARD REPLACEMENT PROCEDURE"

#### 4.0 AMPLIFIER DIAGNOSTICS

The amplifier is intended to be service in a modular fashion. If any board is damaged the entire board must be replaced. This section is to be used as a guide for isolating and identifying damaged boards. Once a damaged board is identified it should be replaced in accordance with the procedures given in Section 3 of this manual. Be sure to follow the general precautions listed in Section 3.1 whenever servicing the amplifier.

#### 4.1 NORMAL AMPLIFIER OPERATION

This section defines the voltages and voltage waveforms which are present at each connection point of each assembly during normal amplifier operation. The servicing technician should read all of Section 2 of the manual prior to attempting to diagnose a problem in the amplifier. This will familiarize him with all the functions of the amplifier and each assembly within it.

##### 4.1.1 AMPLIFIER BOARD, ASSEMBLY NO. 100016

Refer to the following drawings for the functional and interconnection schematics for the amplifier board assembly:

<u>DRAWING NUMBER</u>	<u>TITLE</u>	<u>USED ON</u>
B100016	MAJOR COMPONENT LAYOUT, AMPLIFIER BOARD	ALL
C300013	INTERCONNECTION WIRING DIAGRAM	A201S, 401S
D300014	INTERCONNECTION WIRING DIAGRAM	A401M
B300016	BLOCK DIAGRAM ASSY. NO. 100016	ALL

These drawings will aid in the understanding of the amplifier board operating characteristics.

The following lists the normal operating voltages or voltage waveforms for each interconnection point of the amplifier board, Assembly No. 100016.

Tbl-1: Ground



- TB1-2: Amplifier input signal. No waveform or DC offset voltage should be present here if no input signal is connected.
- TB2-1: Ground
- TB2-2: Feedback signal. Same waveform that is present at the amplifier output for the same channel.
- TB3-1: Gate drive signal for the N channel output FETs. This signal should correspond to the amplifier output signal,  $V_{out}$ , plus the N channel FET gate to source voltage. This is approximately  $V_{out} + 4V_{dc}$ .
- TB3-2: Ground
- TB3-3: Ground
- TB3-4: Gate drive signal for the P channel output FETs. This signal should correspond to the amplifier output signal,  $V_{out}$ , plus the P channel FET gate to source voltage. This is approximately  $V_{out} - 4V_{dc}$ .
- TB4-1: The low level, high voltage positive supply,  $+V_{cc2}$ . The approximate value for the positive and negative supplies  $\pm V_{cc2}$  are listed below:

<u>AMPLIFIER MODEL NO.</u>	<u>SUPPLY VOLTAGE, <math>\pm V_{cc2}</math></u>
A201S	$\pm 90 V_{dc}$
A401M, 401S	$\pm 115 V_{dc}$

- TB4-2: The low level, high voltage negative supply,  $-V_{cc2}$ . See TB4-1 above.
- TB5-1: Ground
- TB5-2: Stereo amplifier bridging connection, approximately equal to the amplifier output degained by 31.18 ( $V_{out} / 31.18$ ).
- TB6-1: Unregulated +24 Vdc supply.
- TB6-2: Ground
- TB6-3: Unregulated -24 Vdc supply.
- PL1-1: Regulated +15 Vdc supply.
- PL1-2: Ground

- PLl-3: Regulated -15 Vdc supply.
- PLl-4: Unregulated +24 Vdc supply.
- PLl-5: L.E.D. drive signal. Approximately 0 volts for no indication, +2 Vdc for red indication, and - 2 Vdc for green indication.
- PLl-6: Overload circuit reset signal. The approximate voltages are Reset = +14 Vdc; No Reset = +2 Vdc. Reset occurs when the amplifier output is reduced to less than 0.1 Volts RMS.
- PLl-7: Input/output comparator difference signal. The difference signal,  $V_{diff}$ , is based on the amplifier input signal,  $V_{in}$ , and the amplifier output signal,  $V_{out}$ , as follows:  
 $V_{diff} = (V_{in} - V_{out}/31.18) \times 5.06$ . LED indication occurs whenever the peak value of  $V_{diff} \geq 0.6$  volts.
- PLl-8: L.E.D. red indication over-ride,  $V_{red}$ . The voltage at this point is in accordance with the following:  
 $V_{red} = 0$ , No Indication;  
 $-0.6$  volts peak  $\geq V_{red} \geq -0.15$  volts peak, Green Indication;  
 $V_{red} = +14$  Vdc, Red Indication.
- PLl-9: Amplifier output voltage monitor signal. This pin carries the signal which monitors the amplifier output voltage. The voltage at this pin is the result of a current source whose current is proportional to the output voltage of the amplifier. This current source is driving a low source impedance circuit. The actual voltage waveform does not look like the amplifier output signal. This signal equals +3 to +4 Vdc when the current to the load (speakers) is positive and -3 to -4 Vdc when the current to the load is negative. With a sine wave driving the load, this signal appears to be a square wave at the same frequency as the amplifier output signal with a peak voltage of 3 to 4 volts. Note, if the current to the amplifier load becomes too small this signal discontinues switching with the current. This occurs at current values less than approximately 1 ampere.
- PLl-10: Output FET temperature monitor signal, Voltage at PLl-10 =  $12 \times (1.059 - 0.007286T)$  VDC where T is the output FET temperature in degrees centigrade. Under normal conditions this voltage is between 7.5 to 9 VDC when the amplifier is warm.
- PLl-11: Regulated -12 VDC supply.
- PLl-12: Amplifier on command. This point is at -15 VDC (Same as PLl-3) when the amplifier circuit is off and at -14.3 VDC (The voltage at PLl-3 plus 0.7 VDC) when the amplifier circuit is on.



4.1.2. PROTECTION BOARD, ASSEMBLY NO. 100017

Refer to the following drawings for the functional and interconnection schematics for the protection board assembly:

<u>DRAWING NUMBER</u>	<u>TITLE</u>	<u>USED ON</u>
B100017	MAJOR COMPONENT LAYOUT, PROTECTION BOARD	ALL
C300013	INTERCONNECTION WIRING DIAGRAM	A401M
D300014	INTERCONNECTION WIRING DIAGRAM	401S, A201S
B300017	BLOCK DIAGRAM, ASSEMBLY No.100017	ALL

These Drawings will aid in the understanding of the protection board operating characteristics.

The following lists the normal operating voltages or voltage waveforms for each interconnection point of the amplifier board, Assembly No. 100017.

- TB7-1: Negative input to protection board for current shunt from distribution board. This point is at ground potential when it is connected to the distribution board. See TB7-2.
- TB7-2: Positive input to protection board for current shunt from distribution board. This point is at ground potential when it is connected to the distribution board. The differential signal from TB7-1 to TB7-2 equals the current to the load (speakers) multiplied by the shunt resistance (A401M = 0.00083 OHMS, A201S = 0.0013 OHMS, 401S = 0.0017 OHMS).
- TB8-1: Ground, L.E.D. Drive return.
- TB8-2: L.E.D. Drive Signal.  
0 VDC = No Indication  
-2 VDC = Green Indication  
+2 VDC = Red Indication
- TB9-1: +24VDC, Power source for inrush limiter relay coil.
- TB9-2: Inrush limiter relay coil drive signal. +24VDC = relay contacts open, +0.1VDC = relay contacts closed. The relay contacts should only be open for the first 5 seconds after amplifier power-up.
- TB10-1: Power switch light drive signal return. The light in the power switch receives the hot A.C. line voltage, Vline, at its input. This terminal corresponds to the return path for the light. This terminal returns the light drive current to VLine - 100 VAC (the light is a 100 VAC neon light). If the light is on steady the voltage at this terminal will be 100 VAC relative to TB10-3.

If the light is flashing the voltage from TB10-1 to TB10-3 will read approximately 5 VAC (The actual waveform is approximately 0 volts for  $\frac{1}{2}$  second and 100 volts for several milliseconds. The volt meter averages this signal to result in a low A.C. voltage reading). The flashing light means the amplifier is in overload and at least one of the two channels has shut down. If the input to this channel is reduced to zero the overload circuit should reset and the light should become steady.

TB10-2: Hot A.C. line voltage. This terminal is connected to the voltage of the A.C. power line to which the amplifier is connected.

TB10-3: Hot A.C. line voltage minus 100 VAC. This terminal is connected to the primary tap on the small power transformer which corresponds to 100 volts less than the A.C. power line voltage (i.e. If the A.C. power line is at 220 VAC, TB10-3 will be at 120 VAC).

TB11-1: High power positive supply monitor +Vccl. This terminal is at +Vccl. The approximate voltages of +/- Vccl are listed below for the various model numbers.

<u>AMPLIFIER MODEL NO.</u>	<u>SUPPLY VOLTAGE, +/- Vccl</u>
A201S	+/- 64 VDC
A401M, 401S	+/- 84 VDC

TB11-2: High power negative supply monitor, -Vccl. This terminal is at -Vccl. See TB11-1 above.

For the normal operating voltages of PLL-1 thru PLL-12 see Section 4.1.1, Amplifier Board, Assembly No. 100016.



4.1.3. DISTRIBUTION BOARD, ASSEMBLY NO'S 100018 (A401M)  
AND 100019 (A201S, 401S)

Refer to the following drawings for the electrical and interconnection schematics of the distribution board assemblies:

<u>DRAWING NUMBER</u>	<u>TITLE</u>	<u>USED ON</u>
A100018	MAJOR COMPONENT LAYOUT, DISTRIBUTION BOARD	A401M
A100019	MAJOR COMPONENT LAYOUT DISTRIBUTION BOARD	A201S, 401S
C300010	CIRCUIT SCHEMATIC, DISTRIBUTION BOARD	ALL
C300013	INTERCONNECTION WIRING DIAGRAM	A401M
C300014	INTERCONNECTION WIRING DIAGRAM	A201S, 401S

These drawings will aid in understanding the distribution board assembly.

The following lists the normal operating voltages and voltage waveforms for each interconnection point of the distribution boards, Assembly Numbers 100018 and 100019:

TBl-1: Feedback signal. Same waveform that is present at the amplifier output for the same channel.

TBl-2: Ground.

TBl-3: Gate drive signal for P channel output FETs. This signal should correspond to the amplifier output signal,  $V_{out}$ , plus the P channel FET gate to source voltage. This is approximately  $V_{out} - 4$  VDC.

TBl-4: Ground.

TBl-5: High power negative supply,  $-V_{cc1}$ . The approximate voltages of  $\pm V_{cc1}$  are listed below for the various model numbers.

<u>AMPLIFIER MODEL NO.</u>	<u>SUPPLY VOLTAGE, <math>\pm V_{cc1}</math></u>
A201S	$\pm 64$ VDC
A401M, 401S	$\pm 84$ VDC

TBl-6: Ground.

TB1-7 (A401M ONLY): Ground.

TB1-8 (A401M) OR TB1-7 (A201S, 401S): High power positive supply, +Vccl.  
See TB1-5.

TB1-9 (A401M) OR TB1-8 (A201S, 401S): Ground.

TB1-10 (A401M) OR TB1-9 (A201S, 401S): Gate drive signal for N channel output FETs. This signal corresponds to the amplifier output signal, Vout, plus the N channel FET gate to source voltage. This is approximately Vout + 4 VDC.

TB1-11 (A401M) OR TB1-10 (A201S, 401S): Negative signal from current shunt. This point is essentially at ground potential.

TB1-12 (A401M) OR TB1-11 (A201S, 401S): Positive signal from current shunt. This point is essentially at ground potential. The difference between the positive and the negative current shunt signals equals the current to the load (speakers) multiplied by the shunt resistance (A401M = 0.00083 Ohms, A201S = 0.0013 Ohms, 401S = 0.0017 Ohms).

TB2-1, TB2-4, TB2-7 (A401M ONLY), AND TB2-10 (A401M ONLY): Positive high power supply, +Vccl. See TB1-5 for voltages. These terminals provide the supply voltage to the N channel output FET heat sink assemblies.

TB2-2, TB2-5, TB2-8 (A401M ONLY), AND TB2-11 (A401M ONLY): Amplifier output signal (connected to the sources of the N channel output FETs).

TB2-3, TB2-6, TB2-9 (A401M ONLY), AND TB2-12 (A401M ONLY): Gate drive signal for N channel output FETs. See TB1-10 (A401M) or TB1-9 (A201S, 401S).

TB3-1, TB3-4, TB3-7 (A401M ONLY), AND TB3-10 (A401M ONLY): Negative high power supply, -Vccl. See TB1-5 for voltages. These terminals provide the supply voltage to the P channel output FET heat sink assemblies.

TB3-2, TB3-5, TB3-8 (A401M ONLY), AND TB3-11 (A401M ONLY): Amplifier output signal (connected to the sources of the P channel output FETs).

TB3-3, TB3-6, TB3-9 (A401M ONLY), AND TB3-12 (A401M ONLY): Gate drive signal for P channel output FETs. See TB1-3.



4.1.4. HEAT SINK ASSEMBLIES, NUMBERS 100020 (N CHANNEL FET)  
AND 100021 (P CHANNEL FET)

The heat sink assemblies each have one cable with three lead wires exiting them. These leadwires correspond to the three device connections to the output FETs. The FETs on each assembly are wired in parallel. The following identifies which leadwire color code corresponds to what FET terminal connection:

<u>LEADWIRE COLOR</u>	<u>CORRESPONDING FET TERMINAL</u>
WHITE	DRAIN (SUPPLY VOLTAGE)
RED	SOURCE (UNITY GAIN OUTPUT SIGNAL)
BLACK	GATE (DRIVE SIGNAL)

Be sure to follow the General Precautions identified in Section 3.1 whenever handling the heat sink assemblies. The output FETs are very sensitive to electrostatic discharge.

4.2. TROUBLE SHOOTING

Section 4.1 defines all the normal operating voltages for the interconnection points of each assembly within the amplifier. This information is intended as an aid in identifying which assemblies are not functioning properly. When this information is used in conjunction with proper trouble shooting techniques the identification of damaged assemblies and the repair of amplifiers is possible.

The purpose of this section of the Service Manual is to define a systematic approach to the trouble shooting of the amplifier as well as to identify specific trouble shooting procedures which simplify problem identification for each assembly. The subsections will deal with specific trouble shooting procedures for each assembly.

Amplifier trouble shooting should be performed utilizing the following guidelines:

1. Define the problem. Based on the problem definition try to identify which assemblies are associated with the amplifier functions affected. Use Section 2 and Drawings 300012 through 300018 as a guide in identifying the affected assemblies (see Section 3.2 for drawing list).
2. If the damage is catastrophic and it is suspected that the output FETs are damaged, trouble shooting should be performed after replacement of assemblies which are obviously damaged. Amplifier power up should be in accordance with Section 3.3.2.3. and should initially be performed without the output FETs.

3. Trouble shooting of suspected assemblies should be performed by first verifying all the assembly inputs (supply voltages, input signals, etc.). If there are incorrect input voltages the source of the problem should be identified and corrected before verifying the board outputs. Inputs and outputs for the amplifier and protection board assemblies are identified on Drawings 300016 and 300017 by the direction of the arrows on the associated trace.

If it is unknown what assembly is the cause of a problem then the technician should begin with the overall amplifier inputs (all power supplies and input signals to the amplifier).

4. Once the inputs to an assembly are correct the outputs should be verified. If the outputs are incorrect either the assembly is faulty or the assembly to which the bad output is connected is faulty. In most cases if the assembly to which the output is connected is faulty this will show up as a short to one of the supplies or ground. If the two assemblies can be disconnected and the amplifier will still operate this should be done. In many cases assembly interconnections cannot be broken without affecting the performance of the amplifier. In this case the suspected assemblies must be replaced one at a time to identify which assembly is the problem. The rules for stand alone operation of assemblies within the amplifier are given in the subsections of this section. Refer to these subsections for aid in trouble shooting each specific assembly.

5. Once the damaged assembly is identified, replace it with a new assembly. Follow the board replacement procedures given in Section 3.3. for the specific assembly being replaced. If there is any possibility the output FETs could have been damaged by the problem found, they should be verified in accordance with Section 4.2.4.

Trouble shooting of the power wiring which is not directly associated with a specific board or assembly should be performed referring to the Power Wiring Diagram, Drawing Number 300012. The chassis mounted terminal blocks are identified by a label on the side. In some of the earlier amplifiers, these terminal blocks were not numbered. In these cases the terminal blocks may be identified by the assemblies wired to them. The terminal numbering of all chassis mounted terminal blocks is from the amplifier rear to the amplifier front (i.e. terminal 1 is the terminal closest to the rear of the amplifier).

#### 4.2.1. AMPLIFIER BOARD, ASSEMBLY NO. 100016.

Many of the interconnection points on the amplifier board assembly are difficult to access when it is installed in the amplifier. If the amplifier board is suspected as the cause of the problem it should be disconnected from the heat sink assemblies and powered up without them. This is to avoid any damage on the amplifier board from damaging the output FETs. The procedure to power up the amplifier board without the heat sinks is



given in Section 3.3.2.3., Items 4 thru 13. Note, always verify the fuses FU1 and FU2 on the amplifier board are not blown before searching elsewhere for the problem (see Drawing 100016 for fuse locations).

If the amplifier board continues to operate incorrectly when powered up without the heat sinks the source of the problem could either be in the board or the result of an incorrect signal from one of the board's interconnection points. The amplifier board may be powered up without its protection board. This will do two things: 1. It will allow access to the terminals on the amplifier board which could not be accessed with the protection board in place, and 2. It will verify whether the cause of the problem is on the protection board.

To power up the amplifier board without the protection board(s) refer to the procedure given in Appendix E. Monitor each interconnection point for the proper voltages or voltage waveforms in accordance with Section 4.1.1. with either a volt meter or an oscilloscope as appropriate. Follow the general trouble shooting guidelines defined in Section 4.2. along with the information contained in 4.1.1. to identify the source of the problem.

#### 4.2.2. PROTECTION BOARD, ASSEMBLY NO. 100017

The protection board assemblies for the A401M and the left channel of the A201S or 401S are easily accessed since they are on the top. These boards may be trouble shot while installed.

The right channel protection board on the A201S and 401S is below the left channel board. Direct access to this board is not possible without removing the left channel board. If the right channel protection board is suspected as the culprit, carefully remove the left channel board following the precautions outlined in Section 3.1. in accordance with the following:

1. Remove the left channel protection board assembly.
2. Install the leads from the inrush relay, K1 (blue and black) into TB9 on the right channel protection board in accordance with Drawing B100017.
3. Short the leads of CA9 (blue and white) together and insulate the shorted end with electrical tape or equivalent.
4. Insulate all the remaining leads which are exposed with electrical tape or equivalent. Do not short any of them together since some of these leads carry power voltages.
5. Disconnect the input source from the left channel of the amplifier.

The amplifier may now be powered up. The left channel amplifier board will remain off since its protection board is no longer connected. The right channel protection board is now accessible for trouble shooting. Once the problem is found replace the appropriate assembly in accordance with the board replacement procedures of Section 3.3. When rewiring in the left channel protection board remember to remove the inrush relay cable,

the left channel protection board remember to remove the inrush relay cable, K1 from the right channel board.

Monitor each interconnection point for the proper voltages or voltage waveforms in accordance with Section 4.1.2. with either a volt meter or an oscilloscope as appropriate. Follow the general Trouble Shooting guidelines defined in Section 4.2. along with the information in 4.1.2. to identify the source of the problem.

#### 4.2.3. DISTRIBUTION BOARD, ASSEMBLY NUMBERS 100018 (A401M) AND 100019 (A201S, 401S)

The distribution board assemblies on the A401M and the right channel of the A201S and 401S are easily accessed without board removal or any special provisions. The left channel of the A201S and 401S is hidden by the right channel board and is, therefore, much more difficult to access. With care, however, all the interconnection points on this board may be accessed where the cable leadwires terminate into each terminal block. This must be done leaving the right channel distribution board assembly in place. The amplifiers should not be powered up without a distribution board connected. The boards also should not be disconnected from their mounting standoffs when powered up. The ground connection to the chassis from these boards is through the standoffs.

If damage is suspected on the distribution board the heat sink assemblies should be disconnected from the suspect distribution board before power up. This will prevent the possibility of damage to the output FETs from the distribution board. Follow the general precautions of Section 3.1. To perform power up of an amplifier channel without the heat sink assemblies follow the procedure given in Section 3.3.2.3., Items 4 thru 14. One of the most important types of damage to look for is broken or incorrectly terminated terminals on the distribution board terminal blocks. See the following Section, 4.2.4., for an explanation. If it is still uncertain whether the distribution board is damaged, simply replace the distribution board with a new assembly. Follow the replacement procedure given in Section 3.3.3. for this operation.

#### 4.2.4. HEAT SINK ASSEMBLY, NUMBERS 100020 (N CHANNEL MOSFET) AND 100021 (P CHANNEL MOSFET).

There are only three leads exiting the cable from the heat sink assembly. These leads can be accessed while connected to the distribution board. None of these leads should be disconnected from the distribution board when the amplifier is powered up unless all the heat sink assemblies are disconnected from the distribution board. This should only be done in accordance with the procedure given in Section 3.3.2.3., Items 4 thru 14.



If a heat sink assembly is suspected of being damaged, the procedure given in Appendix D should be followed to verify this. If any heat sink assemblies are damaged and the source of the problem is unknown all the gate and source connections to the heat sinks on the distribution board assembly should be checked. See Section 4.1.4. If a gate or a source connection to a heat sink assembly is open circuited (due to a poor connection or a broken terminal on a terminal block) the FETs will be damaged. The level of damage can vary anywhere from minor gate leakage to complete destruction of the output stage. Therefore, it is very important to properly terminate all gate and source connections to the heat sinks and find any broken terminal blocks. Follow the general precautions of Section 3.1.

It should also be noted that the gate drive signals for the N and P channel MOSFETs coming from the amplifier board assembly can not be open circuited. These connections correspond to TB3-1 and TB3-4 on the amplifier board (Assy. 100016) and TBL-3 and TBL-9 (A201S, 401S) or TBL-10 (A401M) on the distribution board assemblies (ref. Section 4.1.1. and 4.1.3). If any of these interconnections are not terminated properly the output FETs will be damaged.

APPENDIX A  
DC OFFSET VOLTAGE ADJUSTMENT PROCEDURE

1. With the amplifier off, locate P1 on the amplifier board, Assy. No. 100016, for the channel to be adjusted. (The right board is the right channel, etc.). Select an adjustment. Tool with an insulated shaft and a blade fine enough to fit into the adjustment screw head on P1. P1 is accessed through a hole in each protection board, Assy. No. 100017, which is mounted directly above P1. Before powering up the amplifier and making the adjustment be sure you can access P1 with the tool selected. If there are any cables blocking the path to P1, use the tool to carefully move them aside far enough to make the adjustment. If the cable interfering with the adjustment is the ribbon cable be careful not to disengage its connector at either termination point when moving it. If a second tool needs to be used to hold the interfering cable back be sure it is not conductive.
2. Turn the amplifier on. Monitor the amplifier output with a DC voltmeter at the output binding posts of the channel to be adjusted. This measurement should be made with an input source with no DC offset or with no input source at all.
3. Adjust P1 on the amplifier board until the DC offset voltage is less than +/- 0.02 VDC. Give the volt meter sufficient time to settle each time the potentiometer is turned.

You may notice the DC offset will drift some as the amplifier warms up. This drift should not exceed about +/- 0.03 volts.



## APPENDIX B

### AMPLIFIER BOARD CLAMPING VOLTAGE ADJUSTMENT PROCEDURE

Section 2.1 contains a functional description of this circuit. Section 3.3.2.2, Item 2, describes how to determine the correct value for the clamping voltage. The adjustment procedure follows:

1. Connect an ohm meter set on the 1000 ohm scale from the rear of R45 to the cathode of D15 on the amplifier board to be calibrated (See Drawing 100016). Adjust P2 until the ohm meter reads 250 +/- 20 ohms. Disconnect the ohm meter from the amplifier board.
2. Remove the fuses FU1 and FU2 from the amplifier board assembly to be calibrated. See DWG 100016
3. Insert a small piece of 24 AWG Solid Bus Wire into the front socket of the fuse mounts for FU1 and FU2. (The front socket is the socket for the fuse lead closest to the board edge).
4. With the DC supply off, connect the following test equipment to the Bus Wire leads in accordance with figure 1 on the following page.

<u>QTY</u>	<u>DESC.</u>
1.	DC supply (adjusted) to 20VDC
1	100 Ohm, 2 watt or greater power resistor
1	DC volt meter set on 20 volt scale (or sufficient to monitor clamping voltage to 0.01 volts accuracy)

5. Turn the DC supply on and adjust P3 until the volt meter reads the correct clamping voltage within +/- 0.02 volts.
6. Disconnect the test equipment. Remove the leads from the front of the fuse mounts and replace the fuses. Label the board with the new clamping voltage on the top of the heat sink for Q14 and Q15 (see drawing 100016)

#### Notes:

1. The value of  $V_{clamp}$  decreases slightly as the circuit warms with time. It is the cold value which should be adjusted to  $V_{clamp}$ , but this drift will usually fall within the +/- 0.02 volt tolerances.
2. If P3 is adjusted to too low a value of  $V_{clamp}$  the circuit will saturate and actually begin to increase in voltage with further turning. If this occurs just back off until the circuit is no longer saturated. The point of saturation typically occurs at a clamping voltage of about 6 volts.

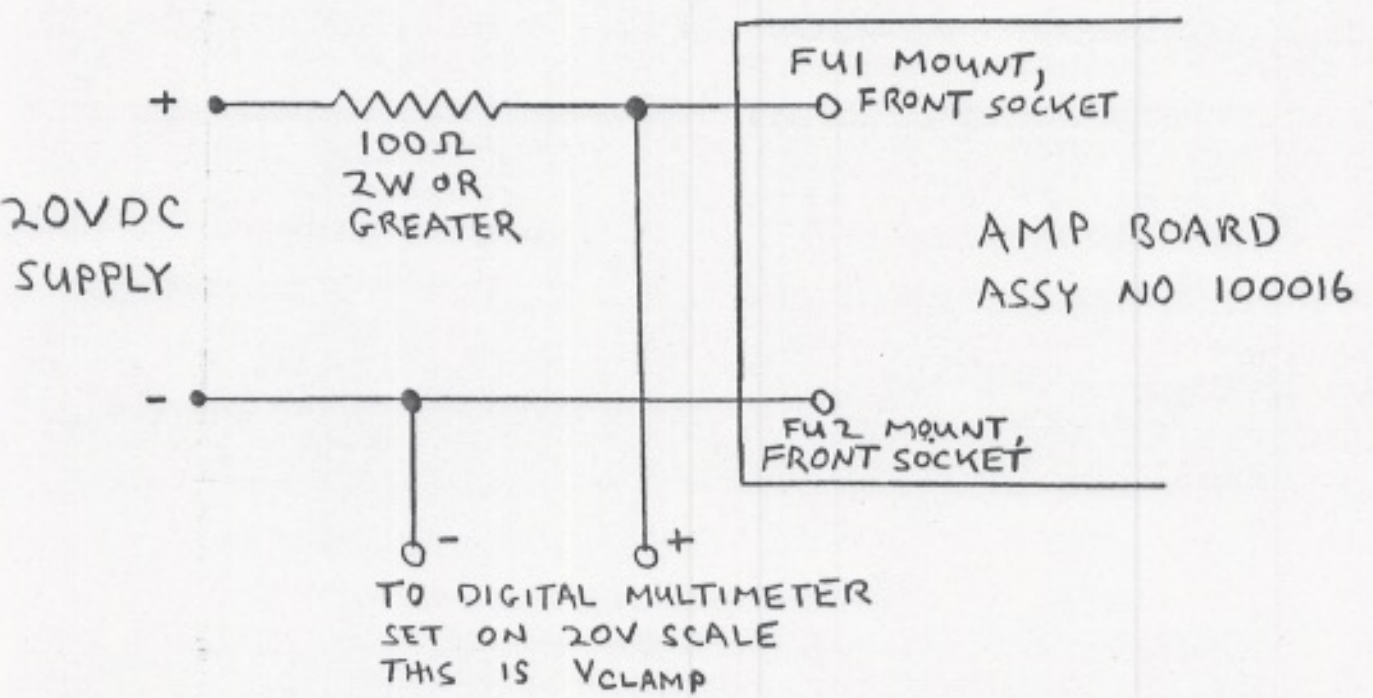


Figure 1. Test Equipment Wiring Schematic



## APPENDIX C

### AMPLIFIER BOARD BIAS VOLTAGE ADJUSTMENT PROCEDURE WITH THE POWER FETS WIRED TO THE DISTRIBUTION BOARD

The simplest and most accurate way to adjust the bias voltage of the amplifier board, Assy. No. 100016, is to disconnect the thermistor from the protection board corresponding to the amplifier channel to be adjusted. This eliminates the temperature monitoring circuitry for the power FETs. With the thermistor disconnected the protection board defaults to a steady temperature reading of 8°C (46°F). This cold temperature reading forces the amplifier board to a high bias voltage condition in an attempt to heat up the output FETs. The adjustment procedure follows:

1. With the amplifier off, disconnect the thermistor from the protection board, Assy. No. 100017, for the amplifier channel to be adjusted. See Drawings 100017 and 300013 (A401M) or 300014 (A201S, 401S). Insulate the exposed thermistor leads to prevent them from shorting to anything.
2. Turn the amplifier on. Monitor the bias voltage from TB3-1 (Positive) to TB3-4 (Negative) on the amplifier board, Assembly No. 100016, with a volt meter. Be sure the amplifier board being monitored corresponds to the correct amplifier channel. The bias voltage should start out at about 0.8 volts less than the clamping voltage labeled on the amplifier board (see section 3.3.2.2). As the board warms up the bias voltage will increase.
3. Allow the amplifier board to warm up for one hour periodically monitoring the bias voltage. If the bias voltage exceeds the clamping voltage minus 0.3 volts adjust P2 such that the bias voltage remains at or below this value. At the end of one hour adjust P2 until the bias voltage reads 0.3 volts less than the clamping voltage.
4. Turn the amplifier off and disconnect the A.C. power cord from the power line. Allow the power supply to discharge for at least 15 minutes or manually discharge the power capacitors. Reconnect the thermistor to the protection board in accordance with Drawings 100017 and 300013 (A401M) or 300014 (A201S, 401S).
5. Power up the amplifier and verify it is operating correctly.

## APPENDIX D

### QUICK CHECK FOR POWER FET DAMAGE

The power FETs which are mounted on the heat sink assemblies may incur damage if there is a failure of the amplifier board (Assy. No. 100016) or the distribution board (Assy. No's 100018 and 100019). If catastrophic damage is caused this will be easy to identify from simple resistance measurements between the three leads of the heat sink assembly. In the FET off state the resistance between any pair of these three leads should be a very high value (in excess of 1 megohm). All the power FETs are wired in parallel on each heat sink assembly. The three leads exiting each heat sink assembly correspond to one of the three terminals of the power FETs. These terminals are identified below:

<u>HEAT SINK LEAD COLOR CODE</u>	<u>CORRESPONDING FET TERMINAL</u>
WHITE	DRAIN (SUPPLY VOLTAGE)
RED	SOURCE (UNITY GAIN OUTPUT)
BLACK	GATE (DRIVE SIGNAL)

The two FET types used are IRF9230 which is a P channel power FET and IRF230 (or IRF232) which is an N channel power FET.

If minor damage has been caused to the power FETs on a heat sink the unit may pass a simple lead to lead resistance check. This kind of damage is dangerous because if it goes unnoticed it can result in an amplifier failure later.

In most cases any power FET damage which could cause a catastrophic failure later will show up in the form of current leakage at the gate of the power FET. This leakage can be quite small, but if it grows, with time it can also be quite dangerous. Since all the power FETs are in parallel, if the device eventually fails completely by gate punch through to the drain, it will overvoltage the gates of all the other power FETs. The net result may be destruction of the entire output stage.

A quick check for gate leakage which can detect very small values of gate leakage current follows. Be sure to follow the precautions of Section 3.1.

1. Connect a 1 kilohm resistor in series with the black (gate) lead of the heat sink to be tested.
2. Short the red and the white leads together.
3. Connect the negative terminal of a 10 VDC supply to the shorted leads and the positive terminal of the supply



to the resistor in series with the black lead.

4. Turn on the supply and measure the voltage drop across the resistor with a volt meter set for millivolts DC. Record this voltage.
5. Turn the supply off. Reverse the supply terminals (so the positive terminal is connected to the shorted heat sink leads and the negative terminal is connected to the resistor in series with the black lead).
6. Repeat step 4.
7. Turn the supply off and disconnect the leads. Repeat the procedure on the next heat sink assembly.

The voltage drop across the 1 kilohm resistor should ideally be 0.0 millivolts. The leakage can be somewhat higher because humidity absorbs into the solder flux on the back of the heat sink board which cannot be cleaned off after the final solder operation. Normal values could go as high as 5 millivolts. Anything in excess of this indicates a potential problem. The device which is the source of the problem may be identified by measuring the voltage drop (in millivolts) across each of the 49.9 OHM,  $\frac{1}{4}$  watt resistors mounted in the heat sink board while performing the previously described procedure. These resistors are wired in series with the gate of each power FET.

## APPENDIX E

### AMPLIFIER POWER UP WITHOUT THE PROTECTION BOARD ASSEMBLIES

Each channel of the amplifier may be powered up without its protection board assembly (No. 100017). This may be useful to identify if a protection board is the source of the problem or to allow easier access to the terminal blocks on the amplifier board which are below the protection board.

The amplifier board assembly is in the "off" state if it is not given the power up command signal from the protection board (reference Sections 2.1. and 2.2. and Drawings No. 300016 and 300017). If the protection board is disconnected from the amplifier board, the amplifier board will not power up. The amplifier board needs to receive an "on" command to power up. The following procedure describes how to power up the amplifier board without a protection board and simulate the protection board "on" command.

1. Disconnect and remove one or both protection boards as necessary. Follow the general precautions given in Section 3.1.
2. Insulate all the exposed leadwires with electrical tape or equivalent. Be sure not to short any of the leadwires together (many of these carry power voltages).
3. Perform the following steps on the amplifier channel which is to be inspected. The other channel may be left alone. It simply will not power up without the protection board.
  - 3a. With the ribbon cable still connected to the amplifier board, wire a ten (10) kilohm,  $\frac{1}{4}$  watt resistor from PLL-1 (+15 vdc) to PLL-12 (Amplifier "ON" Command) in the connector. Refer to Drawing 300016, Block Diagram. If you solder 18 AWG solid bus wire onto the two leads of the resistor, this will interface quite well with the sockets of the connector. This way the resistor may be removed and installed easily. Bend the leads appropriately so all the other sockets within the connector can still be accessed when the resistor is installed. Place shrink tubing or some other form of insulation over the exposed lead length not in the socket to avoid the possibility of shorts to the leads during the following operations. The installation of this resistor commands the amp board into the "on" state without the protection board.
  - 3b. Wire a one (1) kilohm,  $\frac{1}{4}$  watt resistor from PLL-2 (GND) to PLL-10 (Temperature Monitor) in the connector in a manner similar to that described in Step 1. See Drawing 300016. Be sure the lead connected to PLL-2 may be removed and reconnected to PLL-11 (-12VDC) easily without any danger of shorts to it while the amplifier is on. The ground connection simulates a hot temperature from the thermistor, the -12 volts simulates a cold temperature reading from the thermistor. It is the voltage that is being monitored. The resistor installed in series is simply to minimize current



flow if one of the two points being connected is damaged.

4. Disconnect the heat sink assemblies from both distribution board assemblies. Follow the procedure given in Section 3.3.2.3., Steps 4,5, and 6. Turn the amplifier on with these connections in place. Monitor the bias voltage on the amplifier board being inspected (TB3-1 to TB3-4) with the resistor described in Step 3. installed from PLL-2 to PLL-10. The bias voltage should be approximately 0.5 to 0.6 volts lower than that expected in Step 9. of Section 3.3.2.3 Remove the resistor lead from PLL-2 and place it in the socket for PLL-11. This should be done without disturbing the resistor lead in PLL-10. The bias voltage should increase by approximately 0.5 volts. If the amplifier board appears to be operating properly perform Steps 9. thru 12. in Section 3.3.2.3. Leave the 1 kilohm resistor wired from PLL-10 to PLL-11 for this operation.

If a problem is not found the amplifier channel should be inspected further. Trouble shooting should be performed in accordance with the steps outlined in Section 4.2. and 4.2.1. as necessary. Once all board inspection is complete, the amplifier should be shut off and all supplies allowed to discharge. The resistors installed in the ribbon cable should be removed.

Any damaged assemblies should be replaced following the appropriate procedures from Section 3.3. and the protection board assemblies should be reinstalled following the procedure given in Section 3.3.1.3.