SERVICE MANUAL

DT9904S

CONTENTS

1. SAFETY PREAUTIONS

1.1 GENERAL GUIDELINES

1. When servicing, observe the original lead dress. if a short circuit is found, replace all parts which have been overheated or damaged by the short circuit.

2. After servicing, see to it that all the protective devices such as insulation barrier, insulation papers shields are properly installed.

3. After servicing, make the following leakage current checks to prevent the customer from being exposed to shock hazards.

2.PREVENTION OF ELECTRO STATIC DISCHARGE(ESD)TO ELECTROSTATICALLY SENSITIVE(ES)DEVICES

Some semiconductor(solid state)devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive(ES)Devices. Examples of typical ES devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by electro static discharge(ESD).

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any ESD on your body by touching a known earth ground. Alternatively, obtain and wear a commercially availabel discharging ESD wrist strap, which should be removed for potential shock reasons prior to applying power to the unit under test.

2. After removing an electrical assembly equipped with ES devices,place the assembly on a conductive surface such as alminum foil, to prevent electrostatic charge buildup or exposure of the assembly.

3. Use only a grounded-tip soldering iron to solder or unsolder ES devices.

4. Use only an anti-static solder removal device. Some solder removal devices not classified as anti-static (ESD protected)can generate electrical charge sufficient to damage ES devices.

5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ES devices.

6. Do not remove a replacement ES device from its protective package until immediately before you are ready to install it. (Most replacement ES devices are packaged with leads electrically shorted together by conductive foam, alminum foil or comparable conductive material).

7. Immediately before removing the protective material from the leads of a replacement ES device, touch the protective material to the chassis or circuit assembly into which the device will be installed.

Caution

Be sure no power is applied to the chassis or circuit, and observe all other safety precautions.

8. Minimize bodily motions when handling unpackaged replacement ES devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity(ESD).

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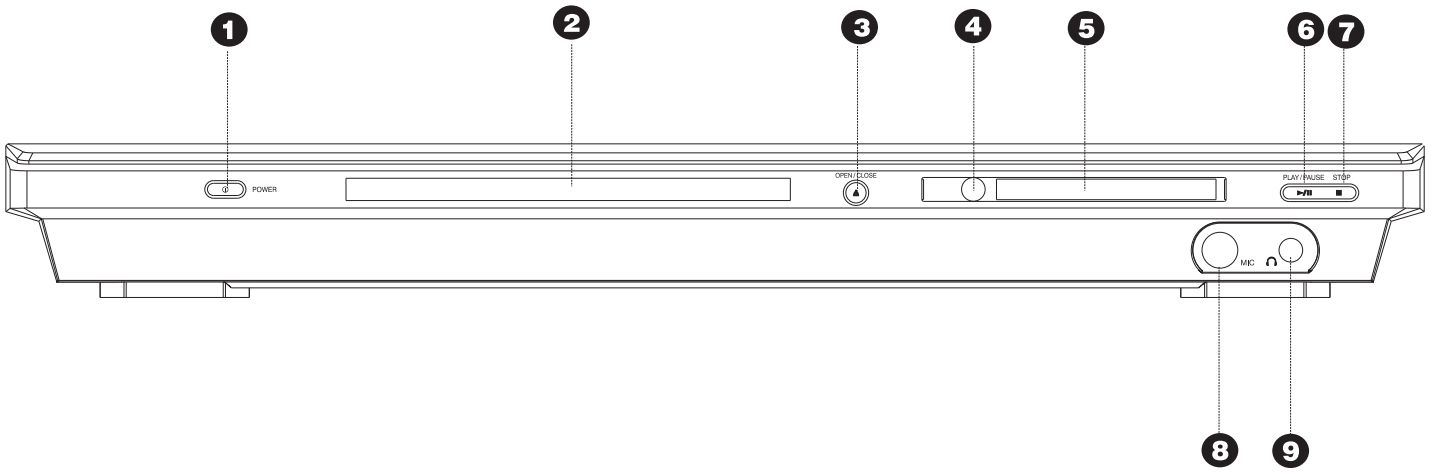
IMPORTANT SAFETY NOTICE

There are special components used in this equipment which are imporant for safety.
These parts are marked by ⚠ in the schematic diagrams, Exploded Views and replacement parts list. It is essential that these critical parts should be replaced with manufacturer's specified parts to prevent shock, fire, or other hazards. Do not modify the original design without permission of manufacturer.

▪ Front Panel Illustration



❶ POWER switch

❷ Disc tray

❸ OPEN/CLOSE button

❹ Remote control signal sensor

❺ LED display window

❻ PLAY/PAUSE button

❼ STOP button

❽ MIC jack

❾ Headphone jack

4.PREVENTION OF STATIC ELECTRICITY DISCHARGE

The laser diode in the traverse unit (optical pickup)may brake down due to static electricity of clothes or human body. Use due caution to electrostatic breakdown when servicing and handling the laser diode.

4.1.Grounding for electrostatic breakdown prevention

Some devices such as the DVD player use the optical pickup(laser diode)and the optical pickup will be damaged by static electricity in the working environment.Proceed servicing works under the working environment where grounding works is completed.

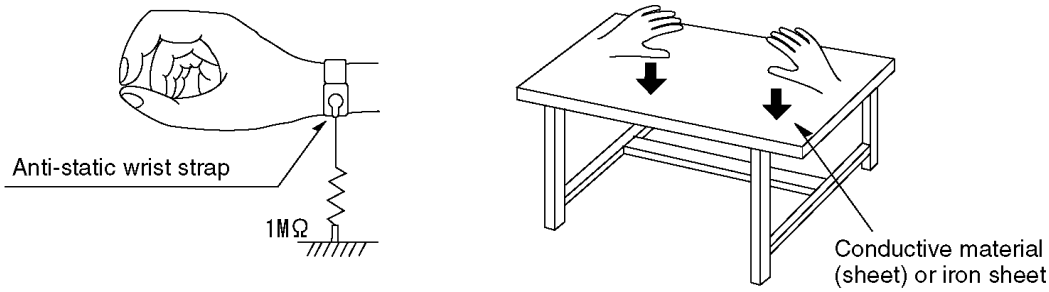
4.1.1. Worktable grounding

1. Put a conductive material(sheet)or iron sheet on the area where the optical pickup is placed,and ground the sheet.

4.1.2.Human body grounding

1 Use the anti-static wrist strap to discharge the static electricity from your body.

safety_3 (1577x409x2 tiff)



4.1.3.Handling of optical pickup

1. To keep the good quality of the optical pickup maintenance parts during transportation and before installation, the both ends of the laser diode are short-circuited.After replacing the parts with new ones, remove the short circuit according to the correct procedure. (See this Technical Guide).

2. Do not use a tester to check the laser diode for the optical pickup .Failure to do so willdamage the laser diode due to the power supply in the tester.

4.2. Handling precautions for Traverse Unit (Optical Pickup)

1. Do not give a considerable shock to the traverse unit(optical pickup)as it has an extremely high-precise structure.

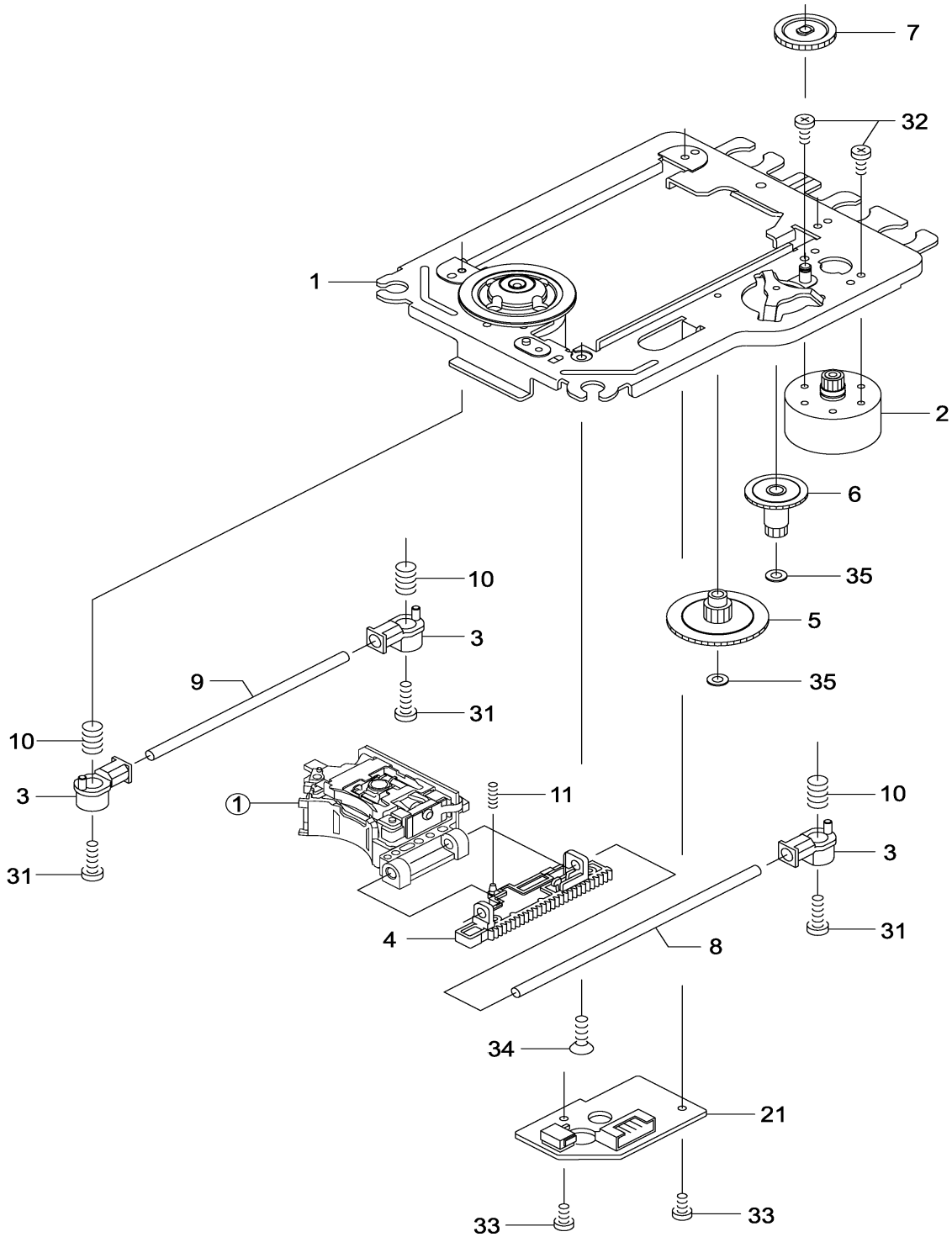
2. When replacing the optical pickup, install the flexible cable and cut is short land with a nipper. See the optical pickup replacement procedure in this Technical Guide. Before replacing the traverse unit, remove the short pin for preventingstatic electricity and install a new unit.Connect the connector as short times as possible.

3. The flexible cable may be cut off if an excessive force is applied to it.Use caution when handling the cable

4. The half-fixed resistor for laser power adjustment cannot be adjusted. Do not turn the resistor.

5. Assembling and disassembling the mechanism unit

5.1 Optical pickup Unit Explosed View and Part List



Pic (1)

Materials to Pic (1)

No.	PARTS CODE	PARTS NAME	Q'ty
①	14692200	SF-HD60	1
1	1EA0311A06300	ASSY, CHASSIS, COMPLETE	1
2	1EA0M10A15500	ASSY, MOTOR, SLED	1
Or	1EA0M10A15501	ASSY, MOTOR, SLED	1
3	1EA2451A24700	HOLDER, SHAFT	3
4	1EA2511A29100	GEAR, RACK	1
5	1EA2511A29200	GEAR, DRIVE	1
6	1EA2511A29300	GEAR, MIDDLE, A	1
7	1EA2511A29400	GEAR, MIDDLE, B	1
8	1EA2744A03000	SHAFT, SLIDE	1
9	1EA2744A03100	SHAFT, SLIDE, SUB	1
10	1EA2812A15300	SPRING, COMP, TYOUSEI	3
11	1EA2812A15400	SPRING, COMP, RACK	1
21	1EA0B10B20100	ASSY, PWB	1
Or	1EA0B10B20200	ASSY, PWB	1
31	SEXEA25700---	SPECIAL SCREW BIN+-M2X11	3
32	SEXEA25900---	SPECIAL SCREW M1.7X2.2	2
33	SFBPN204R0SE-	SCR S-TPG PAN 2X4	2
34	SFSFN266R0SE-	SCR S-TPG FLT 2.6X6	1
35	SWXEA15400---	SPECIAL WASHER 1.8X4 X0.25	2

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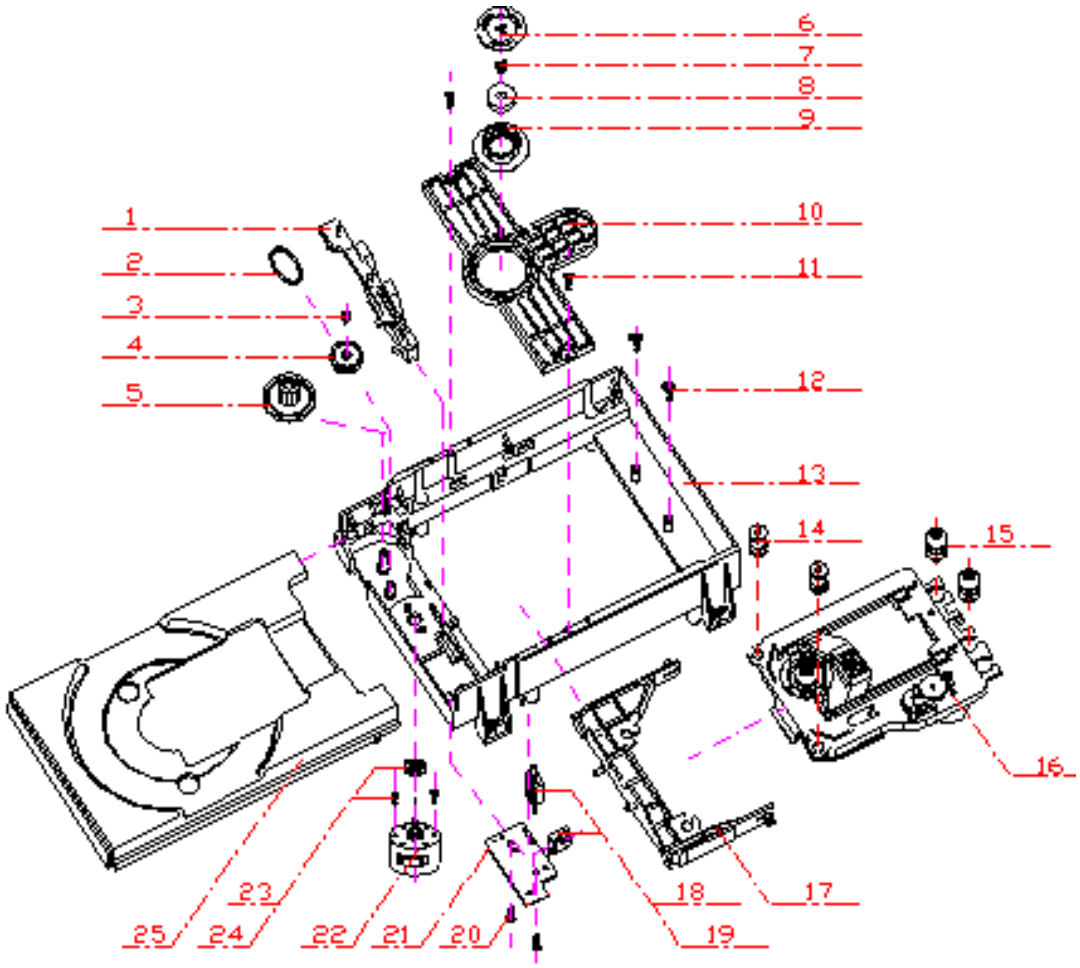
Note : This parts list is not for service parts supply.

5.2 Bracket Explosed View and Part List



Pic (2)

Materials to Pic(2)

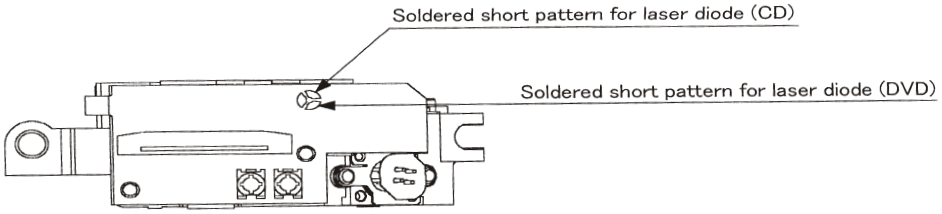
1.bracket
2.belt
3.screw
4.belt wheel
5.gearwheel
6.iron chip
7. Immobility mechanism equipment
8. Magnet
9. Platen
10. Bridge bracket
11. screw
12. screw
13. Big bracket
14. front silicon rubber
15. Back silicon rubber
16. Pick-up
17. Pick-up
18. switch
19. Five-pin flat plug
20. screw
21. PCB
22. motor
23. Motor wheel
24. screw
25.tray

Before going process with disassembly and installation, please carefully both peruse the chart and confirm the materials.

5.3 MISCELLANEOUS

5.3.1 Protection of the LD(Laser diode)

Short the parts of LD circuit pattern by soldering.



5.3.2 Cautions on assembly and adjustment

Make sure that the workbenches,jigs,tips,tips of soldering irons and measuring instruments are grounded,and that personnel wear wrist straps for ground.

Open the LD short lands quickly with a soldering iron after a circuit is connected.

Keep the power source of the pick-up protected from internal and external sources of electrical noise.

Refrain from operation and storage in atmospheres containing corrosive gases (such as H2S,SO2, NO2 and Cl2)or toxic gases or in locations containing substances(especially from the organic silicon,cyan, formalin and phenol groups)which emit toxic gases.It is particularly important to ensure that none of the above substances are present inside the unit.Otherwise,the motor may no longer run.

6.Electrical Confirmation

6.1. Video Output (Luminance Signal) Confirmation

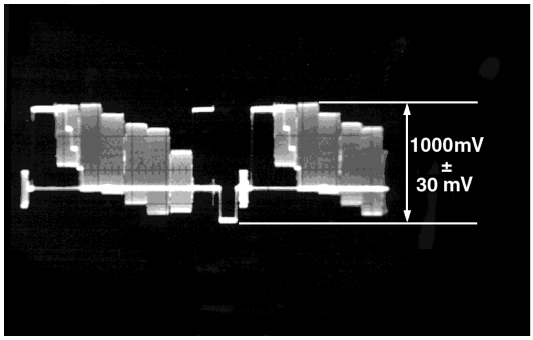
DO this confirmation after replacing a P.C.B.

Measurement point	Mode	Disc
Video output terminal	Color bar 75% PLAY(Title 46):DVDT-S15 PLAY(Title 12):DVDT-S01	DVDT-S15 or DVDT-S01
Measuring equipment,tools	Confirmation value	
200mV/dir,10 μ sec/dir	1000mVp-p±30mV	

Purpose:To maintain video signal output compatibility.

1.Connect the oscilloscope to the video output terminal and terminate at 75 ohms.

2.Confirm that luminance signal(Y+S)level is 1000mVp-p±30mV



6.2 Video Output(Chrominance Signal) Confirmation

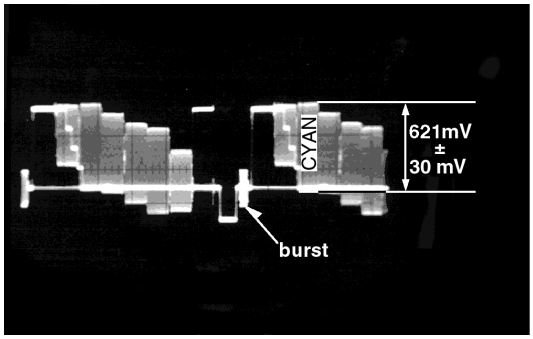
Do the confirmation after replacing P.C.B.

Measurement point	Mode	Disc
Video output terminal	Color bar 75% PLAY(Title 46):DVDT-S15 PLAY(Title 12):DVDT-S01	DVDT-S15 or DVDT-S01
Measuring equipment,tools	Confirmation value	
Screwdriver,Oscilloscope 200mV/dir,10 μ sec/dir	621mVp-p±30mV	

Purpose:To maintain video signal output compatibility.

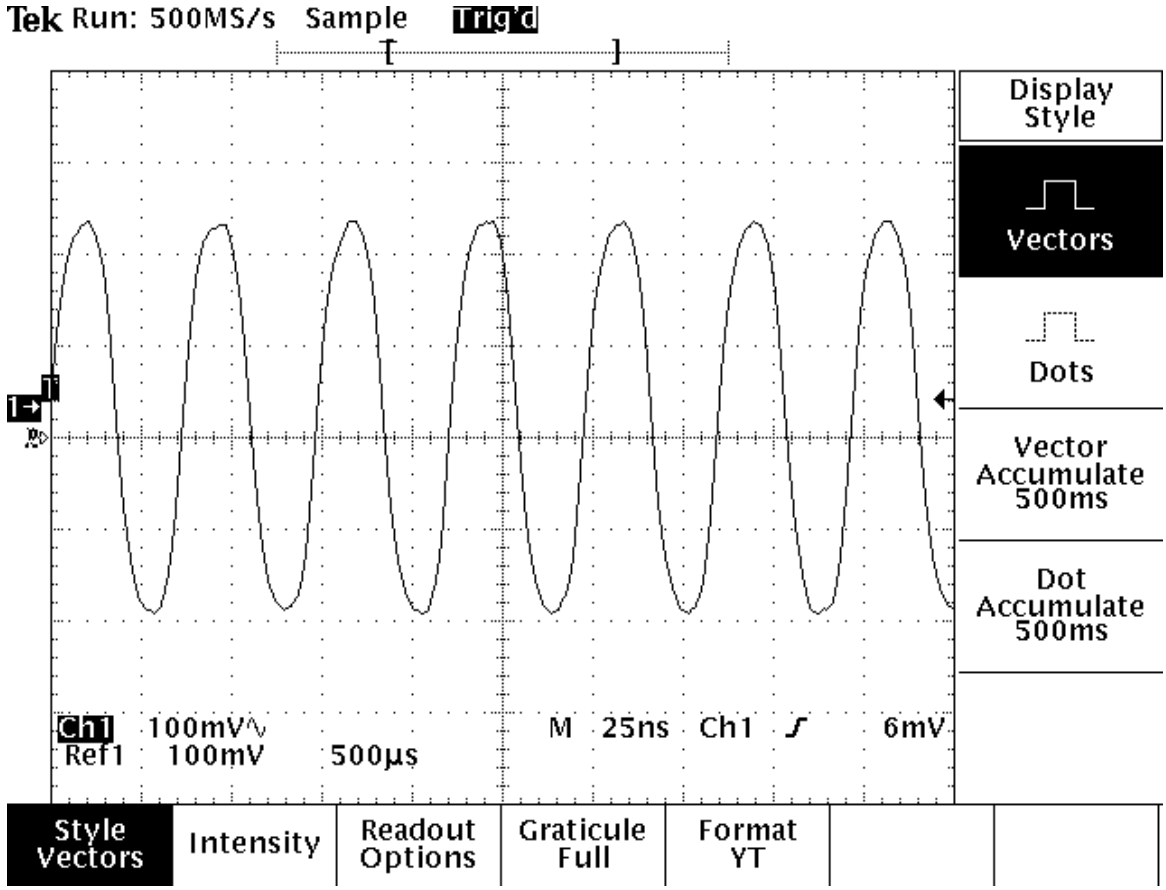
1.Connect the oscilloscope to the video output terminal and terminate at 75 ohme.

2.Confirm that the chrominance signal(C)level is 621 mVp-p±30mV

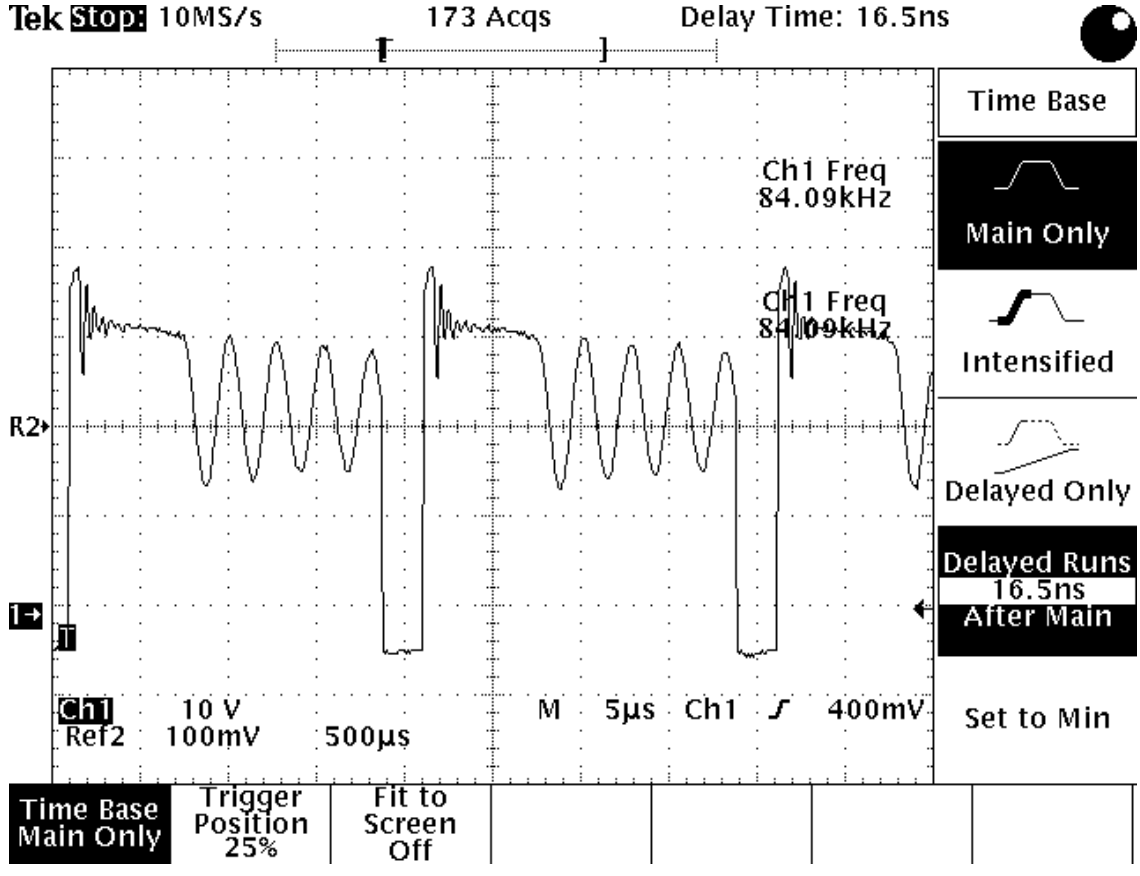


7.MPEG BOARD CHECK WAVEFORM

7.1 27MHz WAVEFORM



7.2 IC5L0380R PIN.2 WAVEFORM DIAGRAM



16 Megabit (2 M x 8-Bit/1 M x 16-Bit) CMOS 3.0 Volt-only Boot Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Manufactured on 0.23 µm process technology**
  - — Fully compatible with 0.32 µm Am29LV160B device
- **High performance**
  - — Access times as fast as 70 ns
- **Ultra low power consumption (typical values at 5 MHz)**
  - — 200 nA Automatic Sleep mode current
  - — 200 nA standby mode current
  - — 9 mA read current
  - — 20 mA program/erase current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and thirty-one 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-system or via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write cycle guarantee per sector**
- **20-year data retention at 125°C**
  - — Reliable operation for the life of the system
- **Package option**
  - — 48-ball FBGA
  - — 48-pin TSOP
  - — 44-pin SO
- **CFI (Common Flash Interface) compliant**
  - — Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion (not available on 44-pin SO)
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device to reading array data

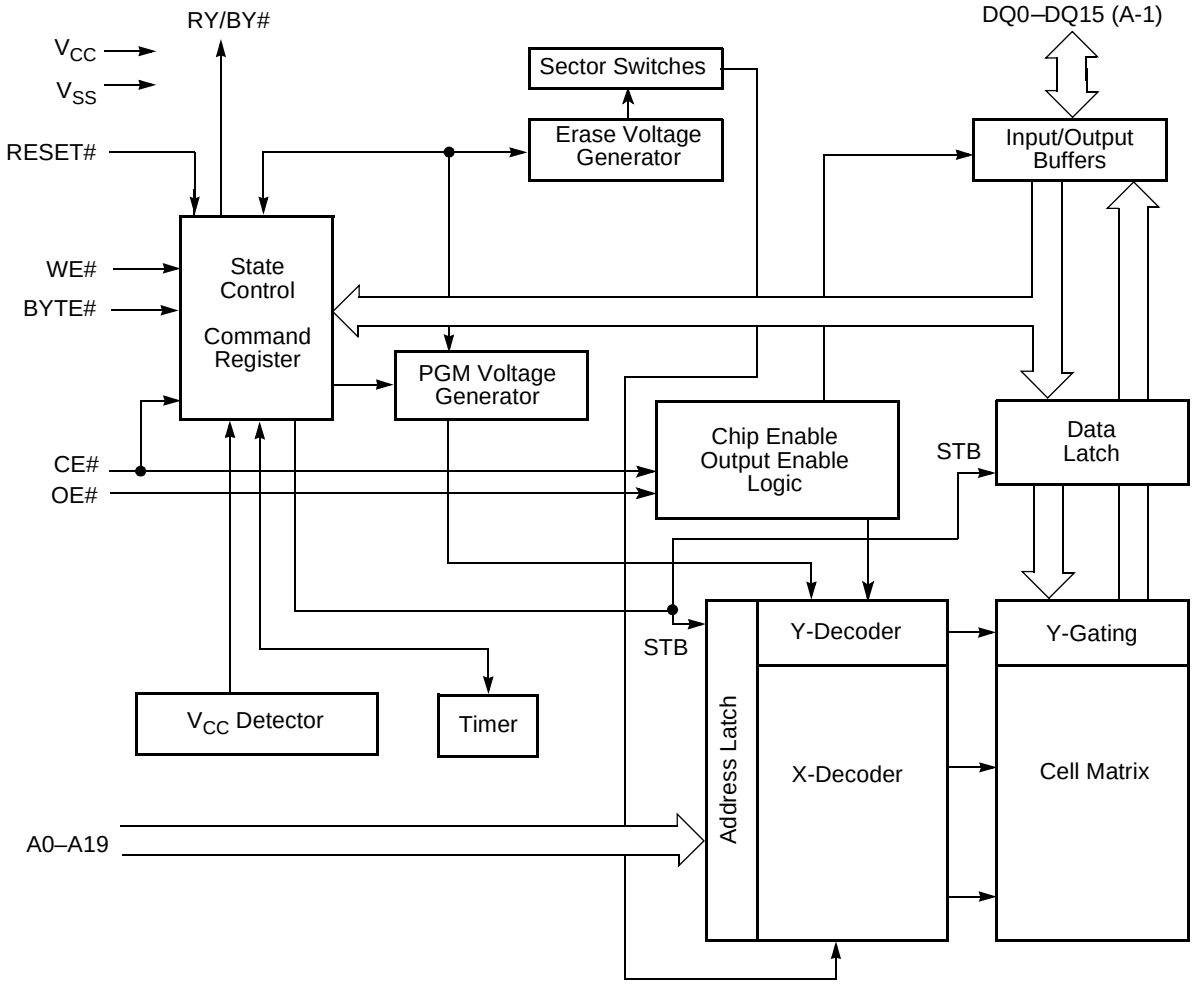
Publication# **22358** Rev: **B** Amendment/**+3**
Issue Date: **November 10, 2000**

PRODUCT SELECTOR GUIDE

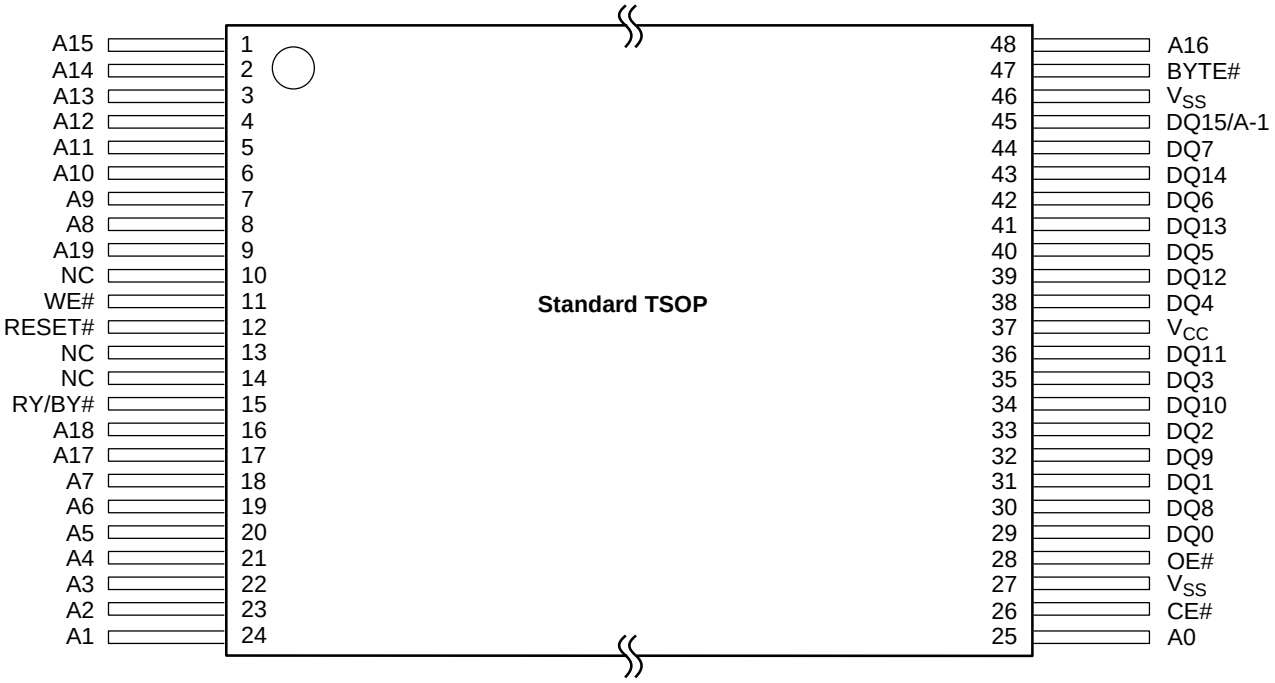
Family Part Number		Am29LV160D		
Speed Option	Voltage Range: V_{CC} = 2.7–3.6 V	**-70**	**-90**	**-120**
Max access time, ns (t_{ACC})		70	90	120
Max CE# access time, ns (t_{CE})		70	90	120
Max OE# access time, ns (t_{OE})		30	35	50

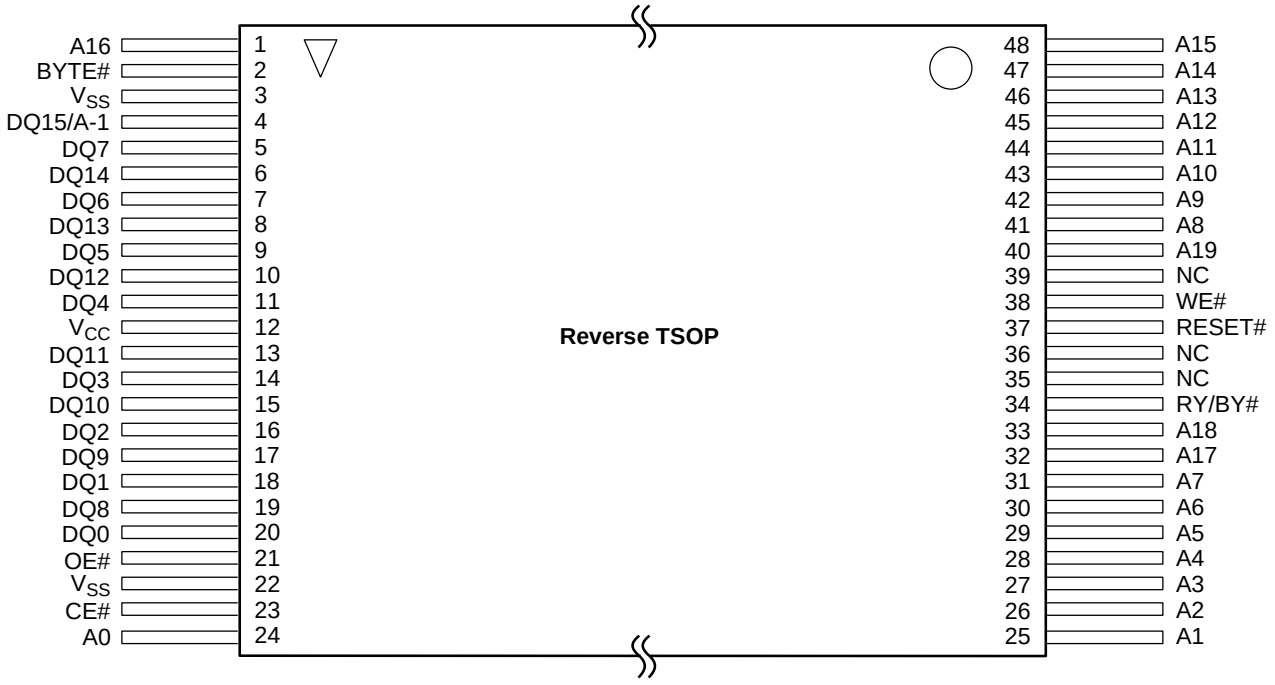
Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM

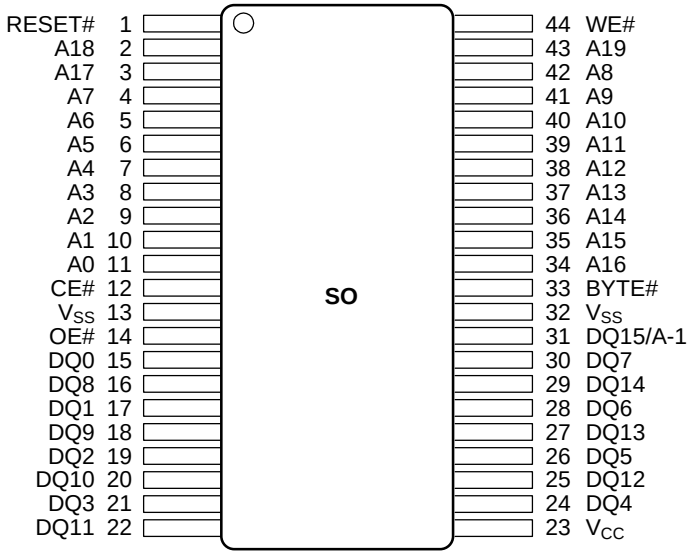


CONNECTION DIAGRAMS





CONNECTION DIAGRAMS



FBGA
Top View, Balls Facing Down

A6	B6	C6	D6	E6	F6	G6	H6
A13	A12	A14	A15	A16	BYTE#	DQ15/A-1	V_{SS}
A5	B5	C5	D5	E5	F5	G5	H5
A9	A8	A10	A11	DQ7	DQ14	DQ13	DQ6
A4	B4	C4	D4	E4	F4	G4	H4
WE#	RESET#	NC	A19	DQ5	DQ12	V_{CC}	DQ4
A3	B3	C3	D3	E3	F3	G3	H3
RY/BY#	NC	A18	NC	DQ2	DQ10	DQ11	DQ3
A2	B2	C2	D2	E2	F2	G2	H2
A7	A17	A6	A5	DQ0	DQ8	DQ9	DQ1
A1	B1	C1	D1	E1	F1	G1	H1
A3	A4	A2	A1	A0	CE#	OE#	V_{SS}

Special Handling Instructions

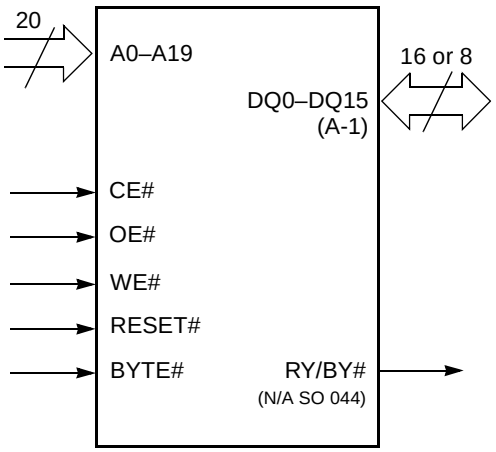
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN CONFIGURATION

A0–A19	=	20 addresses
DQ0–DQ14	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	=	Selects 8-bit or 16-bit mode
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin
RY/BY#	=	Ready/Busy output (N/A SO 044)
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

LOGIC SYMBOL



8.1 HY57V641620HG

DESCRIPTION

The Hyundai HY57V641620HG is a 67,108,864-bit CMOS Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth. HY57V641620HG is organized as 4banks of 1,048,576x16.

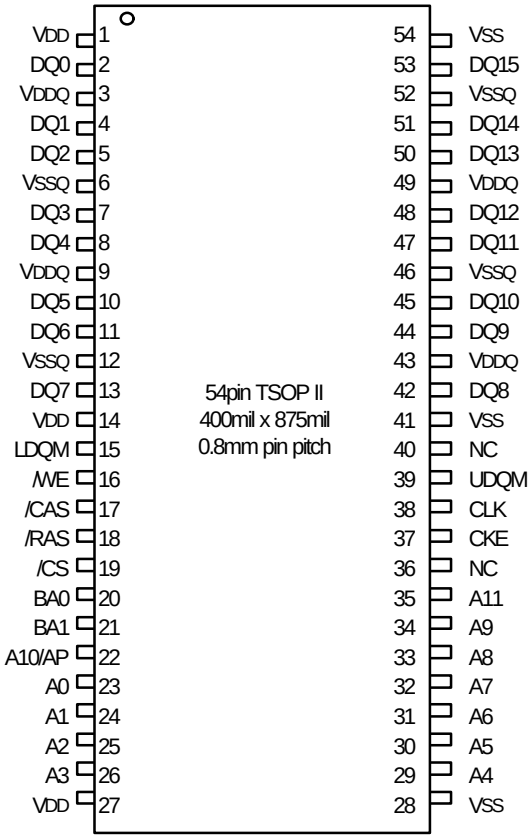
HY57V641620HG is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or Full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

FEATURES

- Single 3.3±0.3V power supply Note)
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 54pin TSOP-II with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM or LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or Full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 2, 3 Clocks

PIN CONFIGURATION

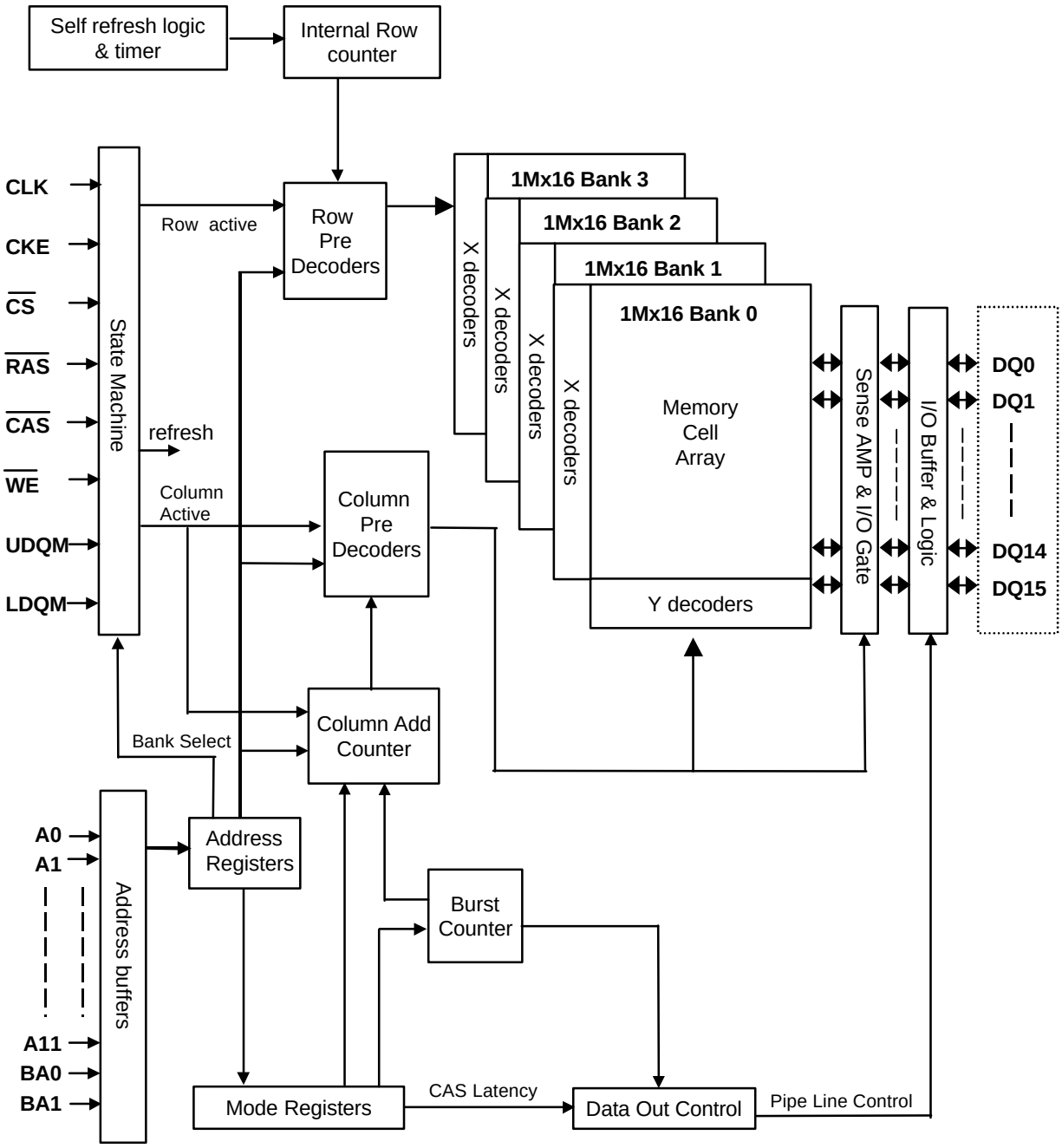


PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0,BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM

1Mbit x 4banks x 16 I/O Synchronous DRAM



MT1389

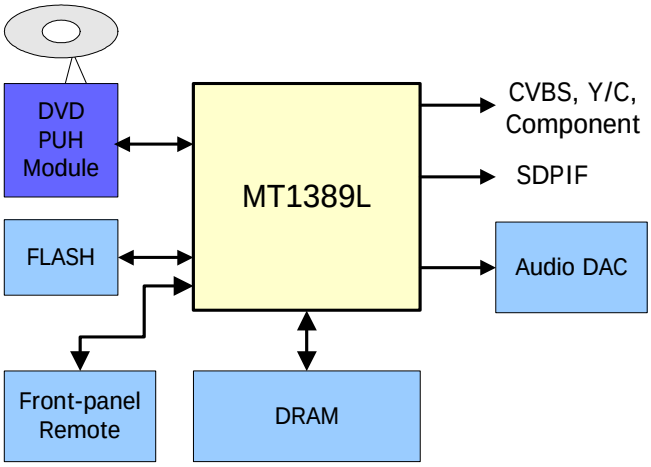
Progressive-Scan DVD Player SOC

Specifications are subject to change without notice

MediaTek MT1389 is a DVD player system-on-chip (SOC) which incorporates advanced features like high quality TV encoder and state-of-art de-interlace processing. The MT1389 enables consumer electronics manufacturers to build high quality, cost-effective DVD players, portable DVD players or any other home entertainment audio/video devices.

Based on MediaTek's world-leading DVD player SOC architecture, the MT1389 is the 3rd generation of the DVD player SOC. It integrates the MediaTek 2nd generation front-end analog RF amplifier and the Servo/MPEG AV decoder.

The progressive scan of the MT1389 utilized a proprietary advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. It can easily detect 3:2/2:2 pull down source and restore the correct original pictures. It also supports a patent-pending edge-preserving algorithm to remove the saw-tooth effect.



DVD Player System Diagram Using MT1389

Key Features

- RF/Servo/MPEG Integration
- High Performance Audio Processor
- Motion-Adaptive, Edge-Preserving De-interlace
- 108MHz/12-bit, 6 CH TV Encoder

Applications

- Standard DVD Players
- Portable DVD Players

General Feature List

- Super Integration DVD player single chip
  - High performance analog RF amplifier
  - Servo controller and data channel processing
  - MPEG-1/MPEG-2/JPEG video
  - Dolby AC-3/DTS/DVD-Audio
  - Unified memory architecture
  - Versatile video scaling & quality enhancement
  - OSD & Sub-picture
  - 2-D graphic engine
  - Built-in clock generator
  - Built-in high quality TV encoder
  - Built-in progressive video processor
  - Audio effect post-processor
  - Audio input port

- High Performance Analog RF Amplifier
  - Programmable fc
  - Dual automatic laser power control
  - Defect and blank detection
  - RF level signal generator

- Speed Performance on Servo/Channel Decoding
  - DVD-ROM up to 4XS
  - CD-ROM up to 24XS

- Channel Data Processor
  - Digital data slicer for small jitter capability
  - Built-in high performance data PLL for channel data demodulation
  - EFM/EFM+ data demodulation
  - Enhanced channel data frame sync protection & DVD-ROM sector sync protection

- Servo Control and Spindle Motor Control
  - Programmable frequency error gain and phase error gain of spindle PLL to control spindle motor on CLV and CAV mode
  - Built-in ADCs and DACs for digital servo control
  - Provide 2 general PWM
  - Tray control can be PWM output or digital output

- Embedded Micro controller
  - Built-in 8032 micro controller
  - Built-in internal 373 and 8-bit programmable lower address port
  - 1024-bytes on-chip RAM
  - Up to 4M bytes FLASH-programming interface
  - Supports 5/3.3-Volt. FLASH interface
  - Supports power-down mode
  - Supports additional serial port

- DVD-ROM/CD-ROM Decoding Logic
  - High-speed ECC logic capable of correcting one error per each P-codeword or Q-codeword
  - Automatic sector Mode and Form detection
  - Automatic sector Header verification
  - Decoder Error Notification Interrupt that signals various decoder errors
  - Provide error correction acceleration

- Buffer Memory Controller
  - Supports 16Mb/32Mb/64Mb/128Mb SDRAM
  - Supports 16-bit SDRAM data bus
  - Provide the self-refresh mode SDRAM
  - Block-based sector addressing
  - Support 3.3 Volt. DRAM Interface

- Video Decode
  - Decodes MPEG1 video and MPEG2 main level, main profile video (720/480 and 720x576)
  - Smooth digest view function with I, P and B picture decoding
  - Baseline, extended-sequential and progressive JPEG image decoding
  - Support CD-G titles

- Video/OSD/SPU/HLI Processor
  - Arbitrary ratio vertical/horizontal scaling of video, from 0.25X to 256X
  - 65535/256/16/4/2-color bitmap format OSD,
  - 256/16 color RLC format OSD
  - Automatic scrolling of OSD image
  - Slide show transition as DVD-Audio Specification

- 2-D Graphic Engine
  - Support decode Text and Bitmap
  - Support line, rectangle and gradient fill
  - Support bitblt
  - Chroma key copy operation
  - Clip mask

- Audio Effect Processing
  - Dolby Digital (AC-3)/EX decoding
  - DTS/DTS-ES decoding
  - MLP decoding for DVD-Audio
  - MPEG-1 layer 1/layer 2 audio decoding
  - MPEG-2 layer1/layer2 2-channel audio
  - High Definition Compatible Digital (HDCD)
  - Windows Media Audio (WMA)
  - Advanced Audio Coding (AAC)
  - Dolby ProLogic II
  - Concurrent multi-channel and downmix out
  - IEC 60958/61937 output
    - PCM / bit stream / mute mode
    - Custom IEC latency up to 2 frames
  - Pink noise and white noise generator
  - Karaoke functions
    - Microphone echo
    - Microphone tone control
    - Vocal mute/vocal assistant
    - Key shift up to +/- 8 keys
    - Chorus/Flanger/Harmony/Reverb
  - Channel equalizer
  - 3D surround processing include virtual surround and speaker separation

- TV Encoder
  - Six 108MHz/12bit DACs
  - Support NTSC, PAL-BDGHINM, PAL-60
  - Support 525p, 625p progressive TV format
  - Automatically turn off unconnected channels
  - Support PC monitor (VGA)
  - Support Macrovision 7.1 L1, Macrovision 525P and 625P
  - CGMS-A/WSS
  - Closed Caption

- Progressive Output
  - Automatic detect film or video source
  - 3:2 pull down source detection
  - Advanced Motion adaptive de-interlace
  - Edge Preserving
  - Minimum external memory requirement

- Audio Input
  - Line-in/SPDIF-in for versatile audio processing

- Outline
  - 256-pin LQFP package
  - 3.3/1.8-Volt. Dual operating voltages

Data sheet acquired from Harris Semiconductor
SCHS047D

August 1998 - Revised March 2000

CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to $20V_{P-P}$ can be achieved by digital signal amplitudes of 4.5V to 20V (if V_{DD}-V_{SS} = 3V, a V_{DD}-V_{EE} of up to 13V can be controlled; for V_{DD}-V_{EE} level differences above 13V, a V_{DD}-V_{SS} of at least 4.5V is required). For example, if V_{DD} = +4.5V, V_{SS} = 0V, and V_{EE} = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic “1” is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the “CHANNEL IN/OUT” terminals are the outputs and the “COMMON OUT/IN” terminals are the inputs.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD4051BF, CD4052BF, CD4053BF	-55 to 125	16 Ld CERAMIC DIP
CD4051BE, CD4052BE, CD4053BE	-55 to 125	16 Ld PDIP
CD4051BM, CD4051BNS	-55 to 125	16 Ld SOIC
CD4051BPW, CD4052BPW, CD4053BPW	-55 to 125	16 Ld TSSOP

Features

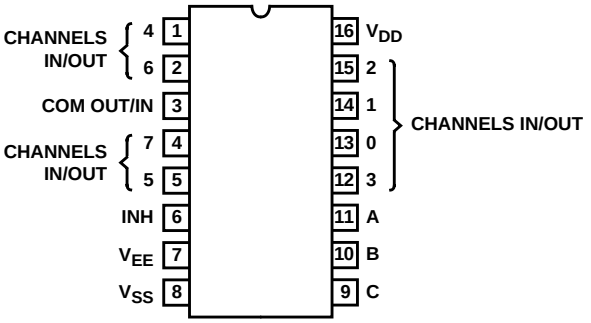
- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . . 3V to 20V
  - Analog. . . . . $\leq 20V_{P-P}$
- Low ON Resistance, 125Ω (Typ) Over $15V_{P-P}$ Signal Input Range for V_{DD}-V_{EE} = 18V
- High OFF Resistance, Channel Leakage of ±100pA (Typ) at V_{DD}-V_{EE} = 18V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V_{DD}-V_{SS} = 3V to 20V) to Switch Analog Signals to $20V_{P-P}$ (V_{DD}-V_{EE} = 20V)
- Matched Switch Characteristics, r_{ON} = 5Ω (Typ) for V_{DD}-V_{EE} = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2μW (Typ) at V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25^oC
- Break-Before-Make Switching Eliminates Channel Overlap

Applications

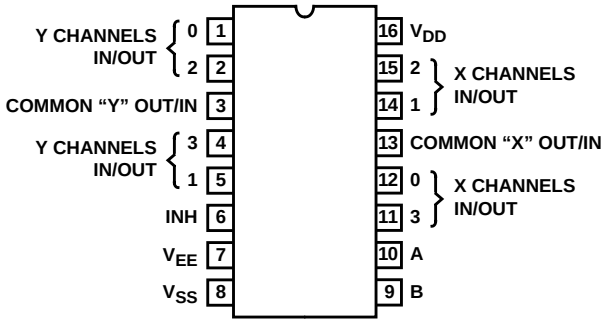
- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

Pinouts

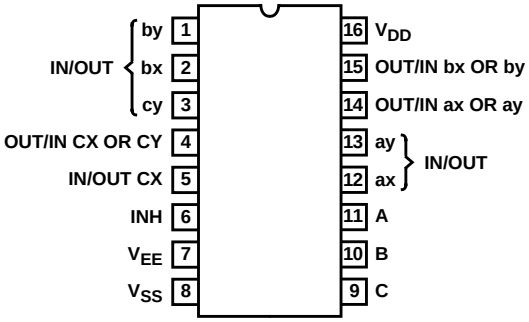
CD4051B (PDIP, CDIP, SOIC, TSSOP)
TOP VIEW



CD4052B (PDIP, CDIP, TSSOP)
TOP VIEW

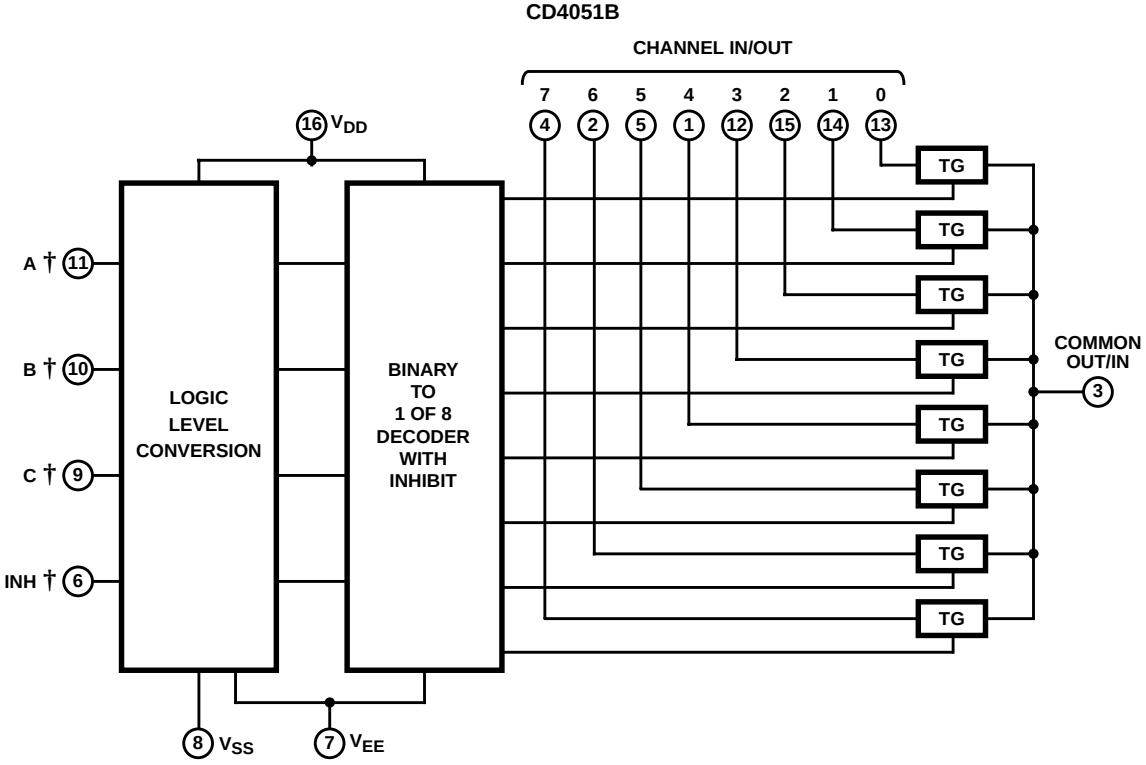


CD4053B (PDIP, CDIP, TSSOP)
TOP VIEW



Functional Block Diagrams

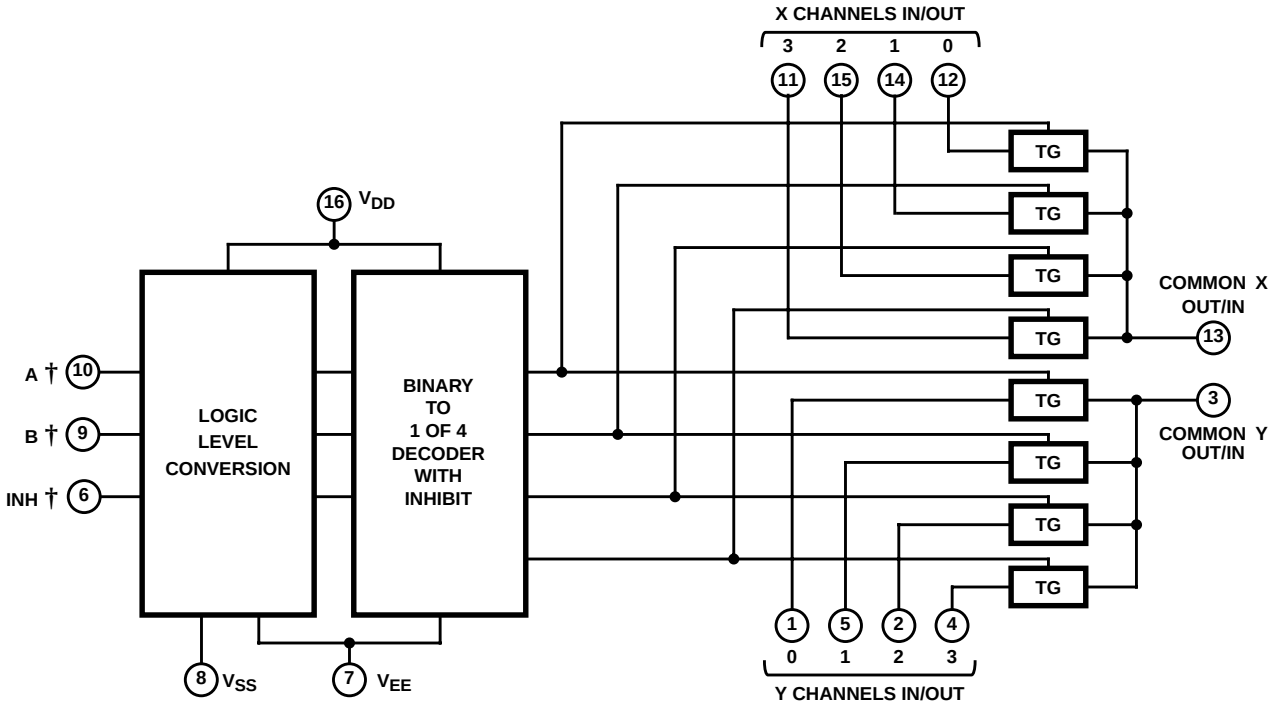
CD4051B



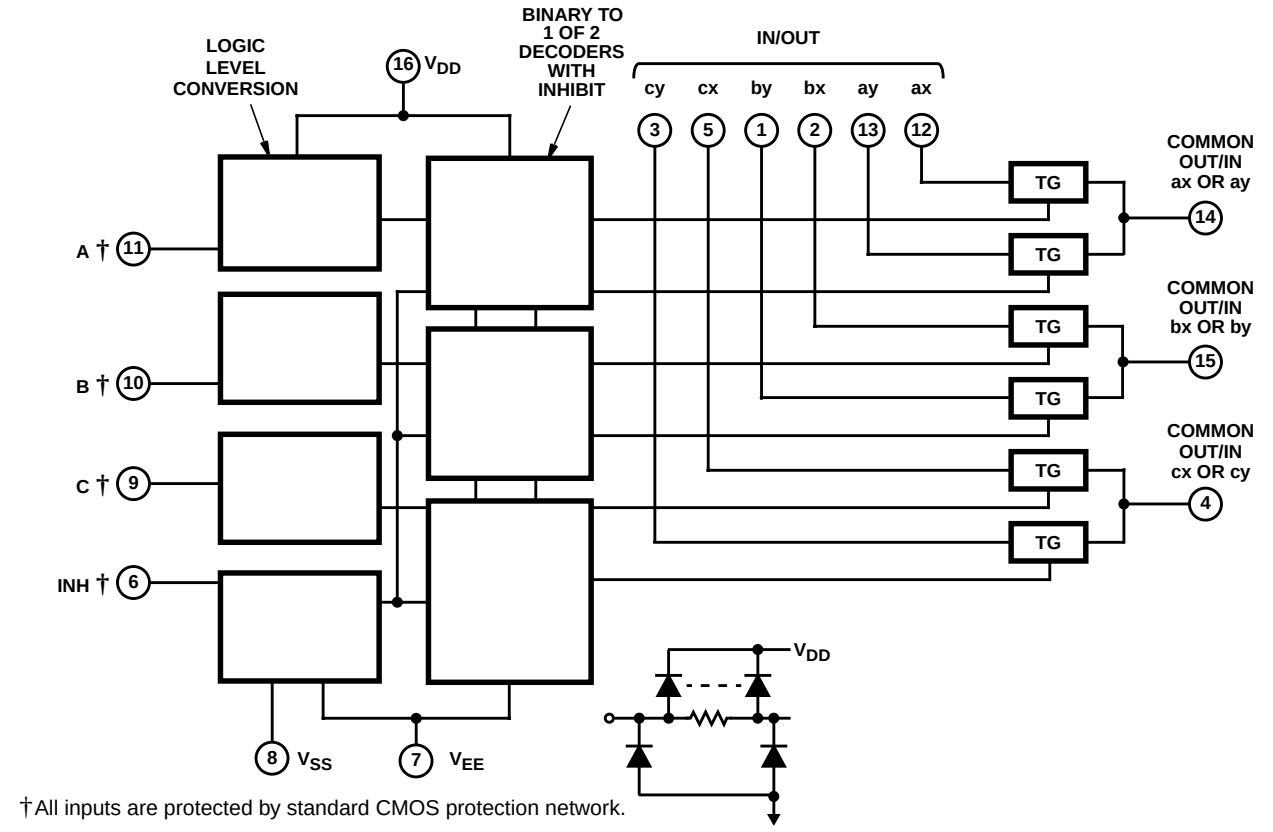
†All inputs are protected by standard CMOS protection network.

Functional Block Diagrams (Continued)

CD4052B



CD4053B



†All inputs are protected by standard CMOS protection network.

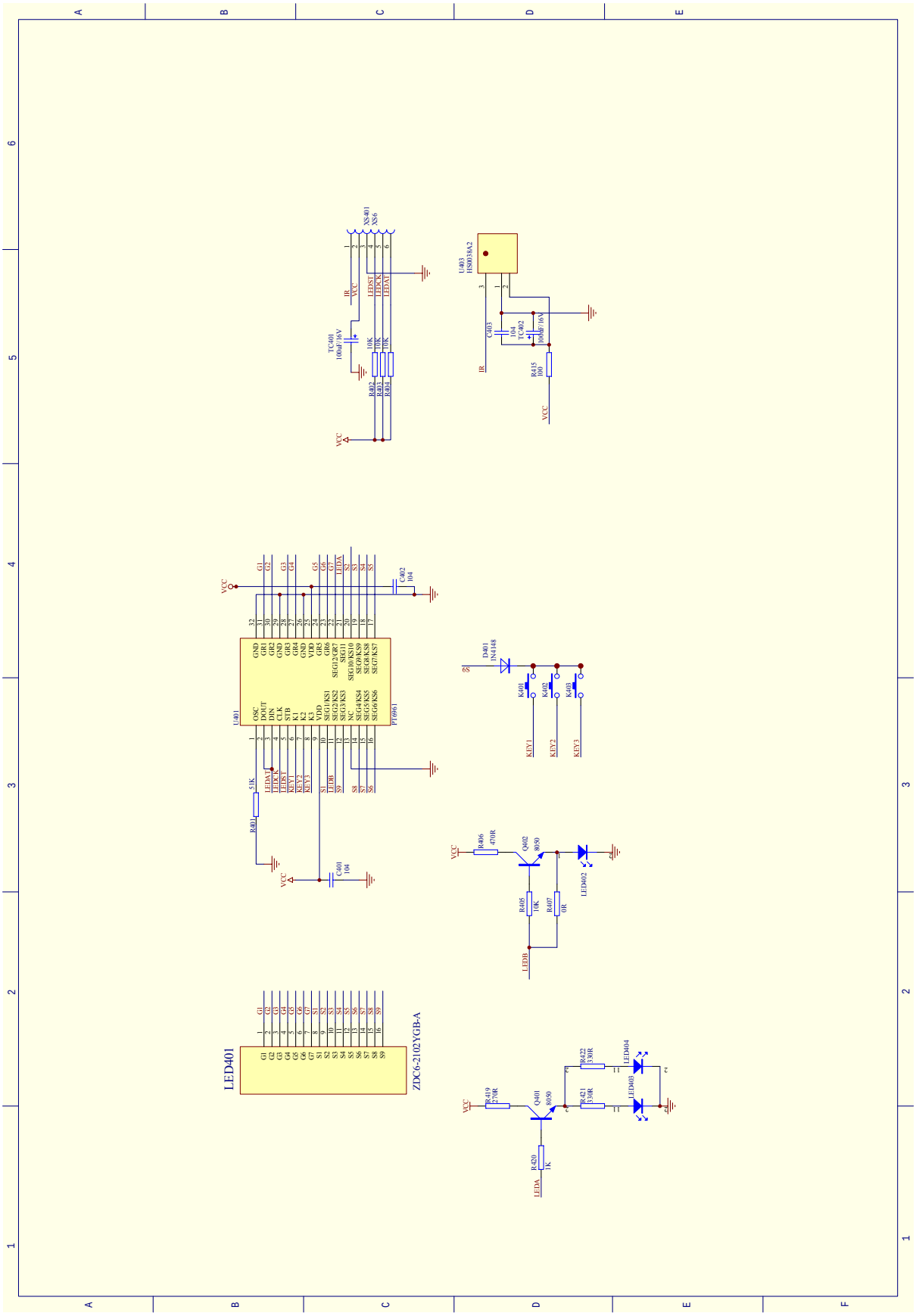
TRUTH TABLES

INPUT STATES				
INHIBIT	**C**	**B**	**A**	**“ON” CHANNEL(S)**
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
CD4052B				
INHIBIT	**B**		**A**	
0	0		0	0x, 0y
0	0		1	1x, 1y
0	1		0	2x, 2y
0	1		1	3x, 3y
1	X		X	None
CD4053B				
INHIBIT	**A OR B OR C**			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			None

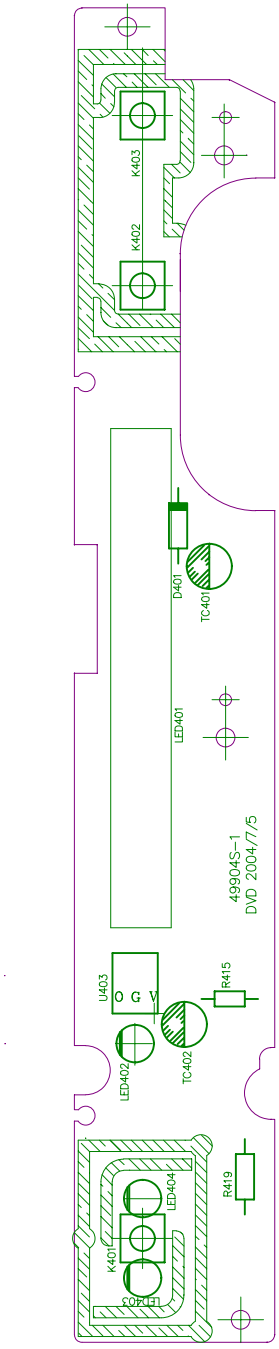
X = Don’t Care

9. SCHEMATIC & PCB WIRING DIAGRAM

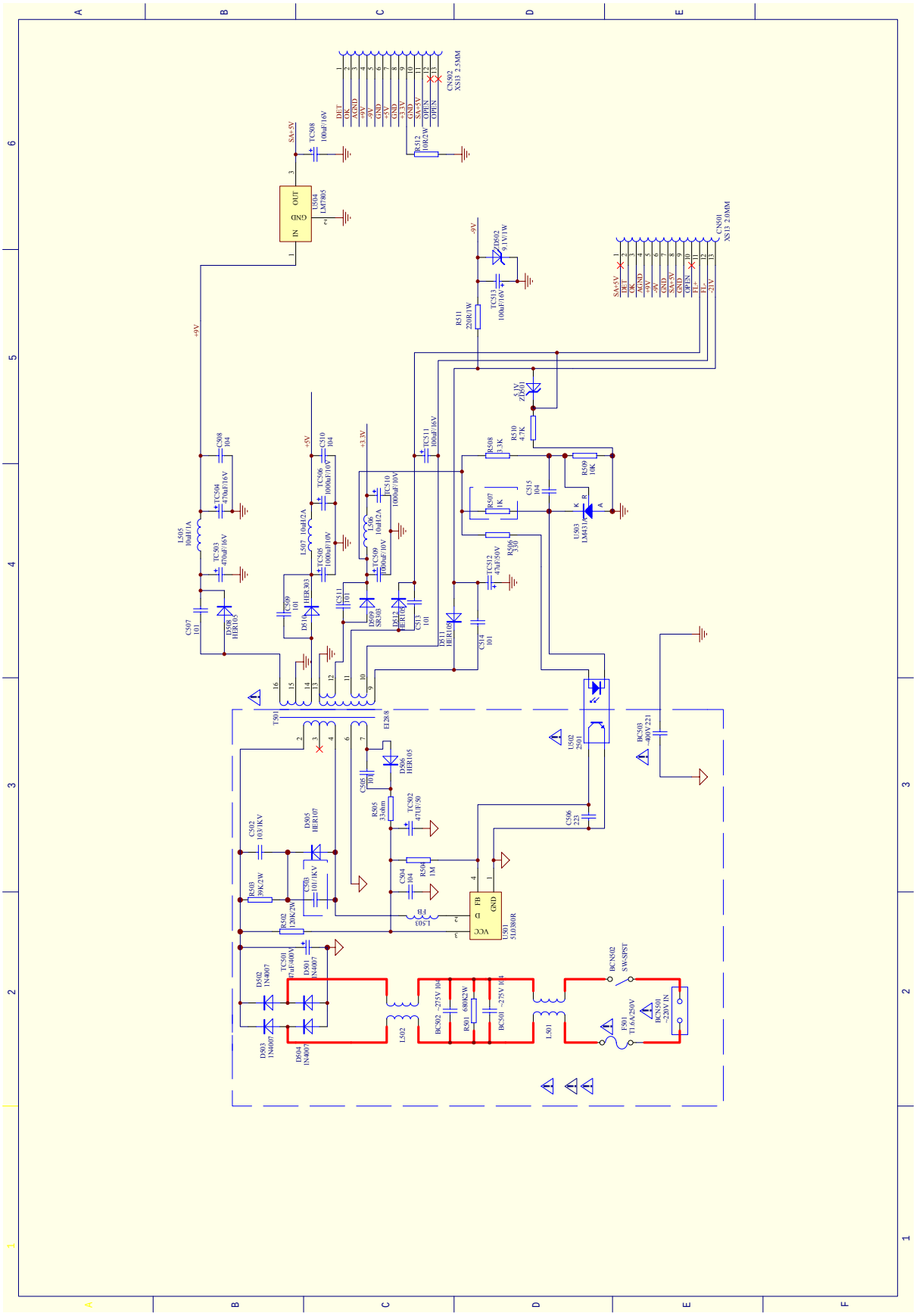
FRONT SCHEMATIC DIAGRAM



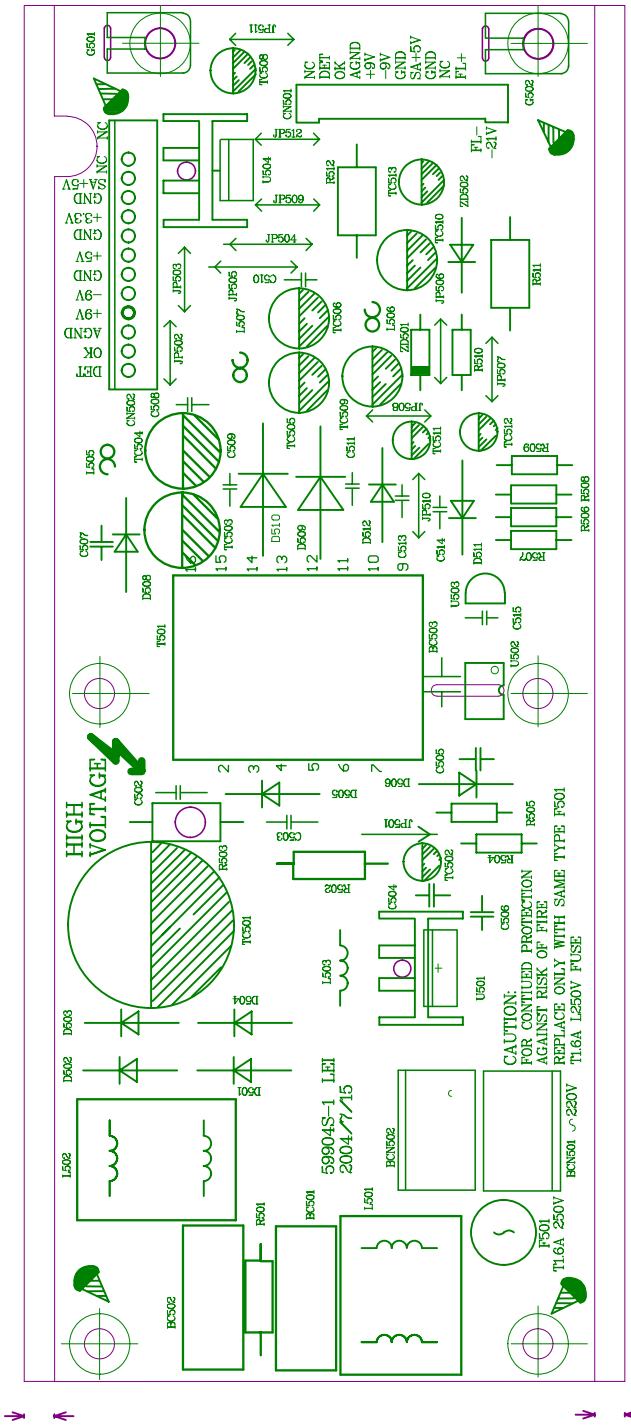
FRONT SCHEMATIC DIAGRAM



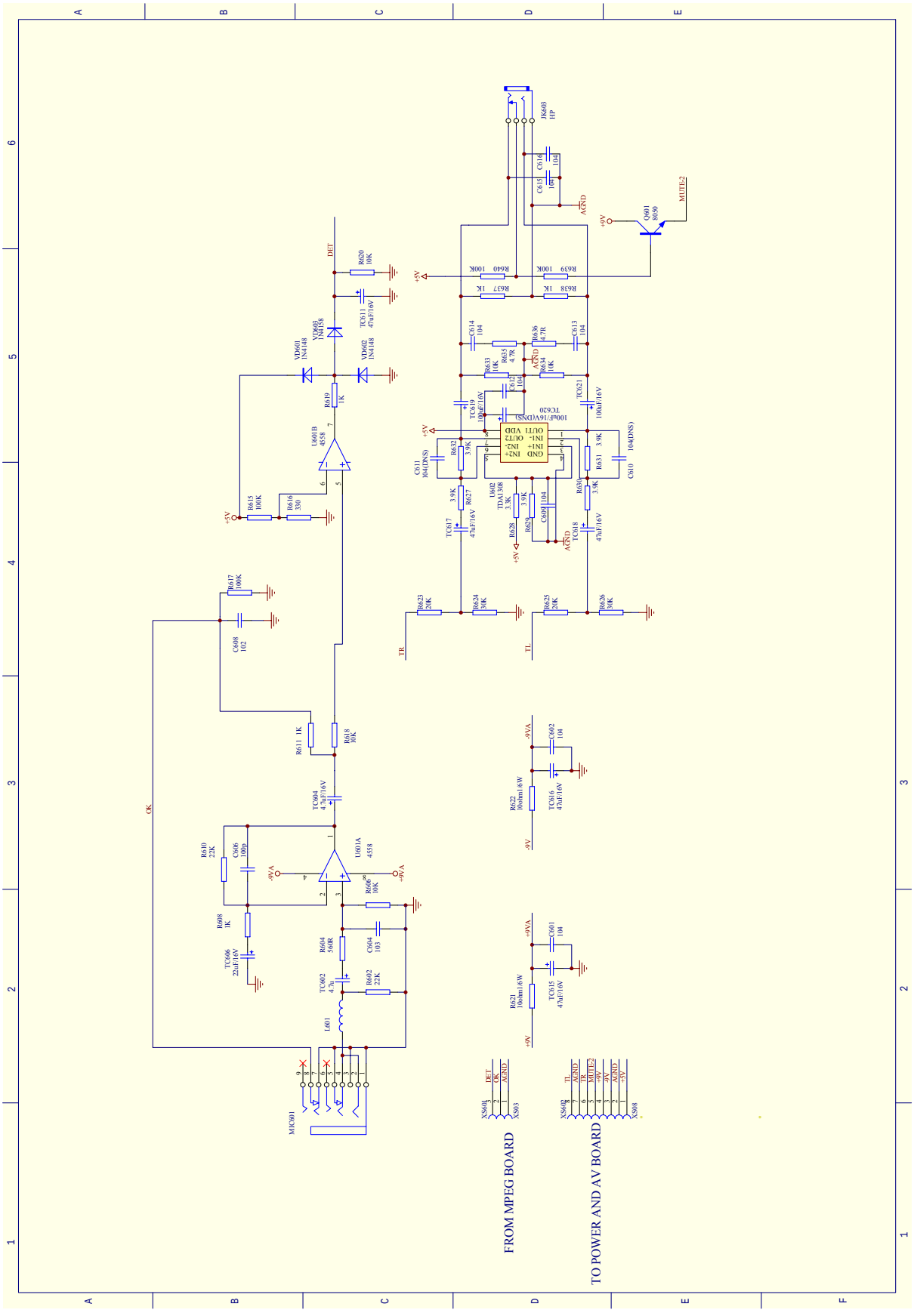
POWER BOARD SCHEMATIC DIAGRAM



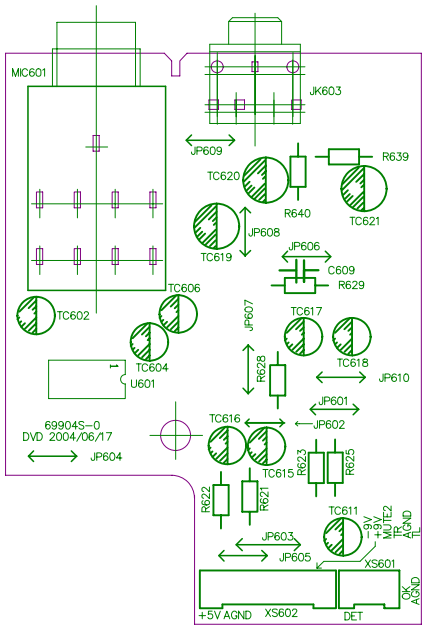
POWER BOARD SCHEMATIC DIAGRAM



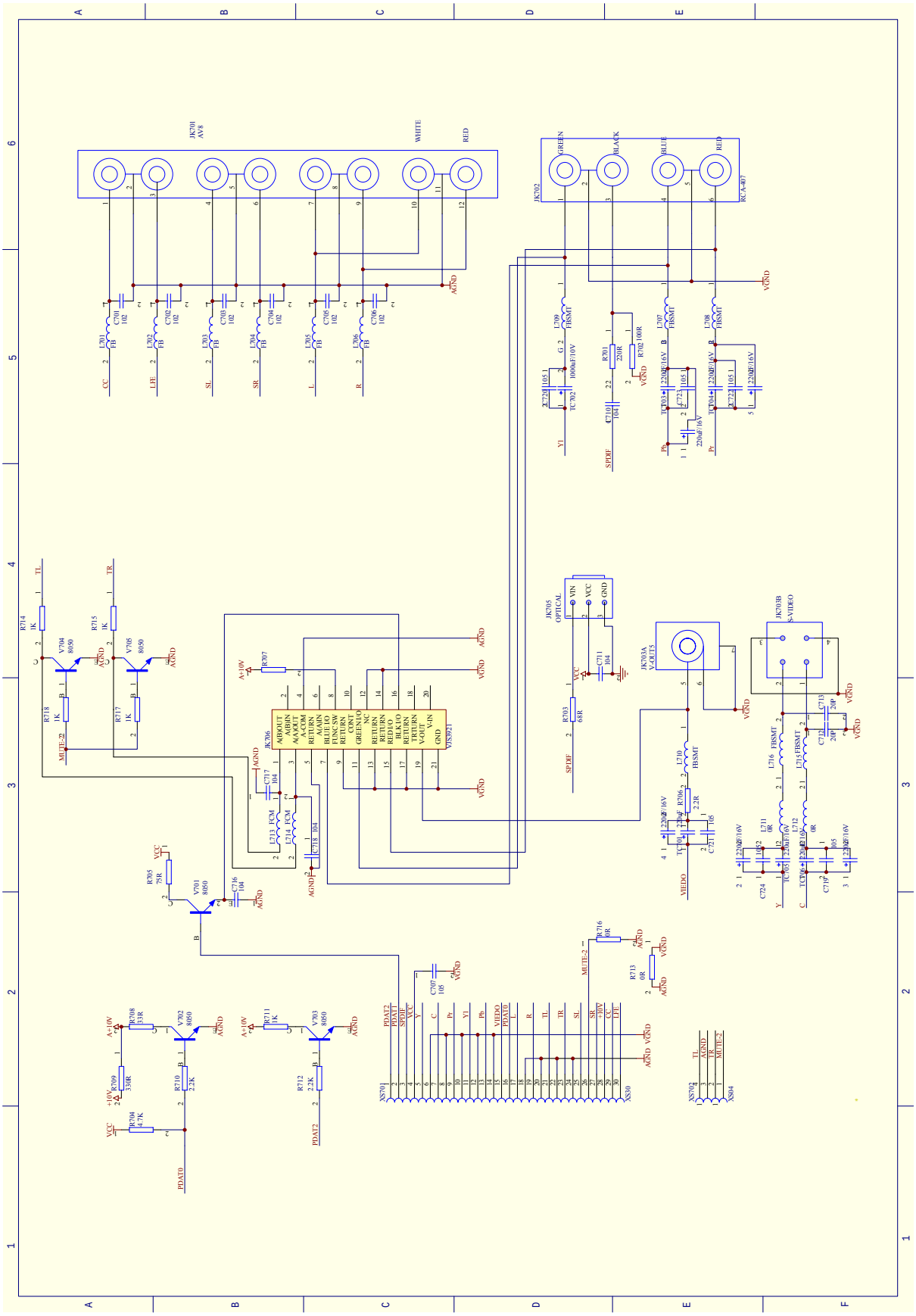
OK SCHEMATIC DIAGRAM



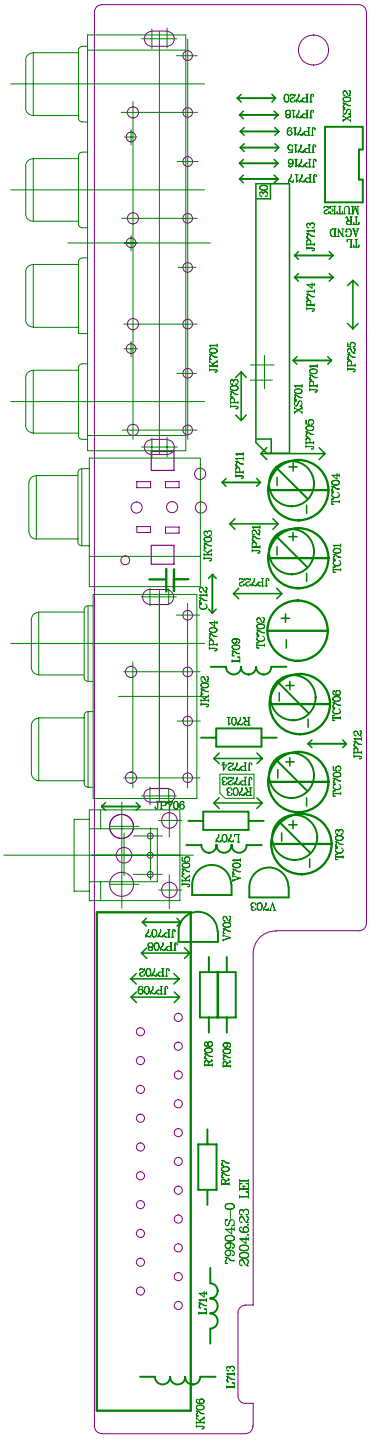
OK SCHEMATIC DIAGRAM



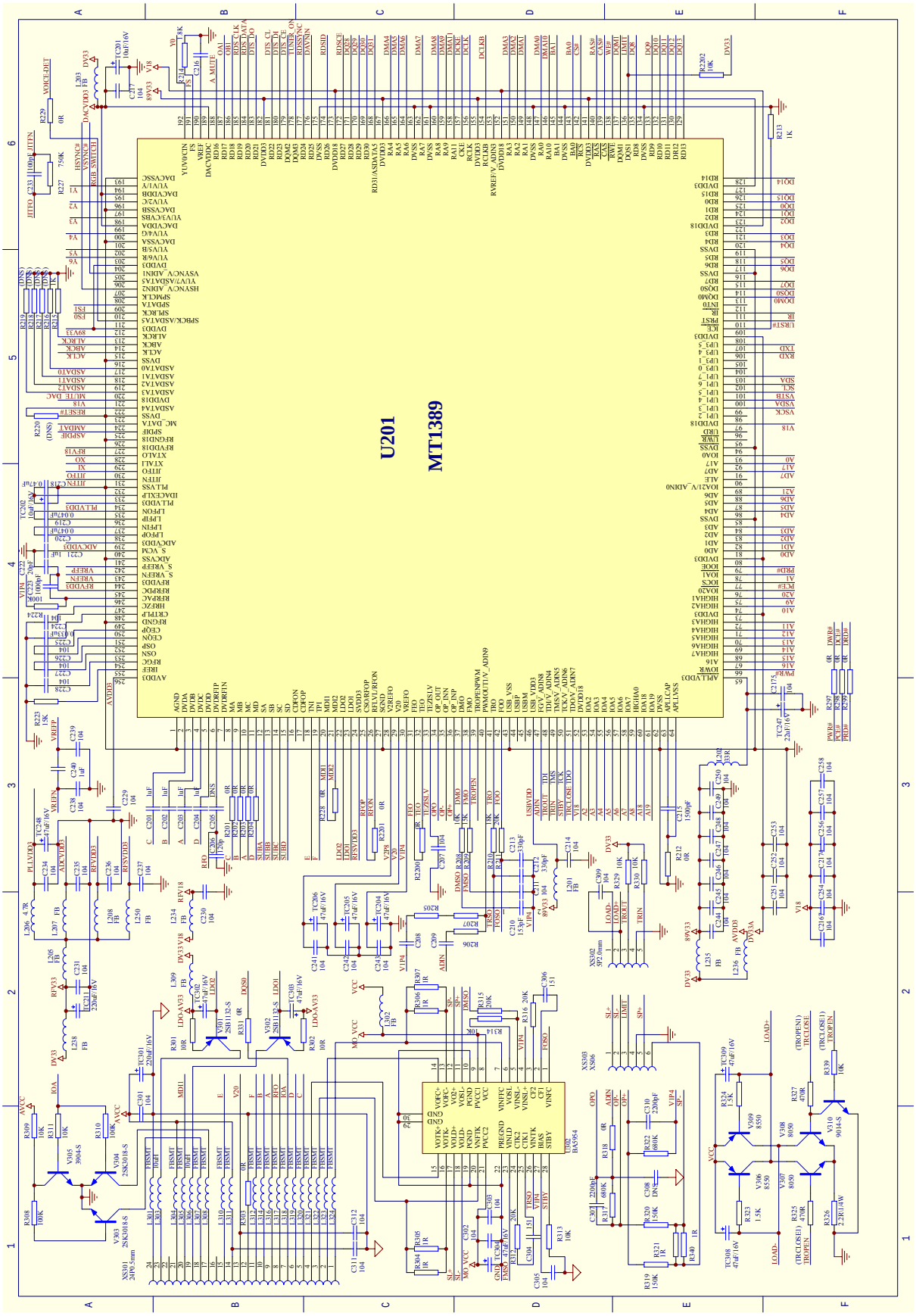
OUTPUT BOARD SCHEMATIC DIAGRAM



OUTPUT BOARD SCHEMATIC DIAGRAM



MIAN SCHEMATIC DIAGRAM



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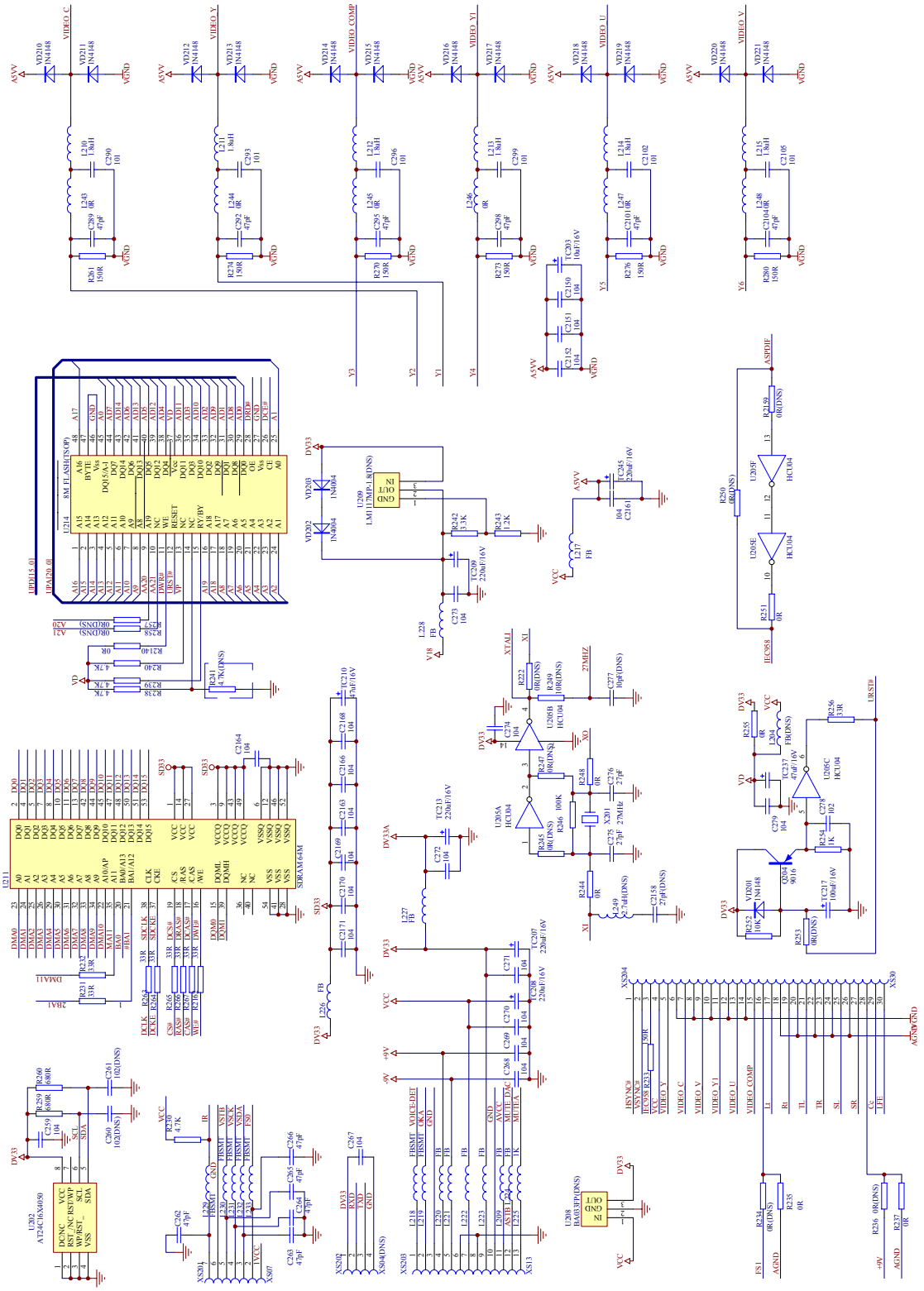

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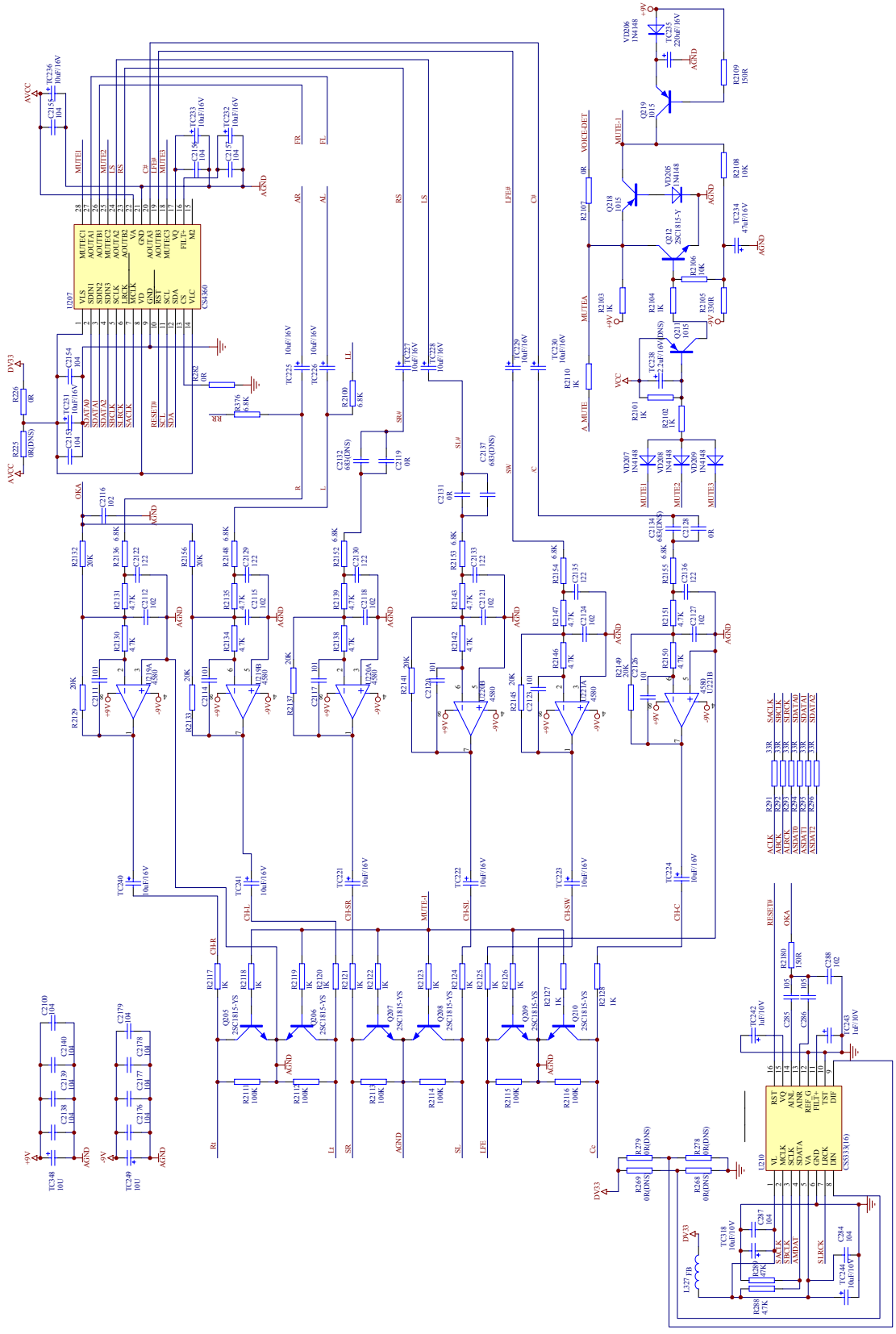

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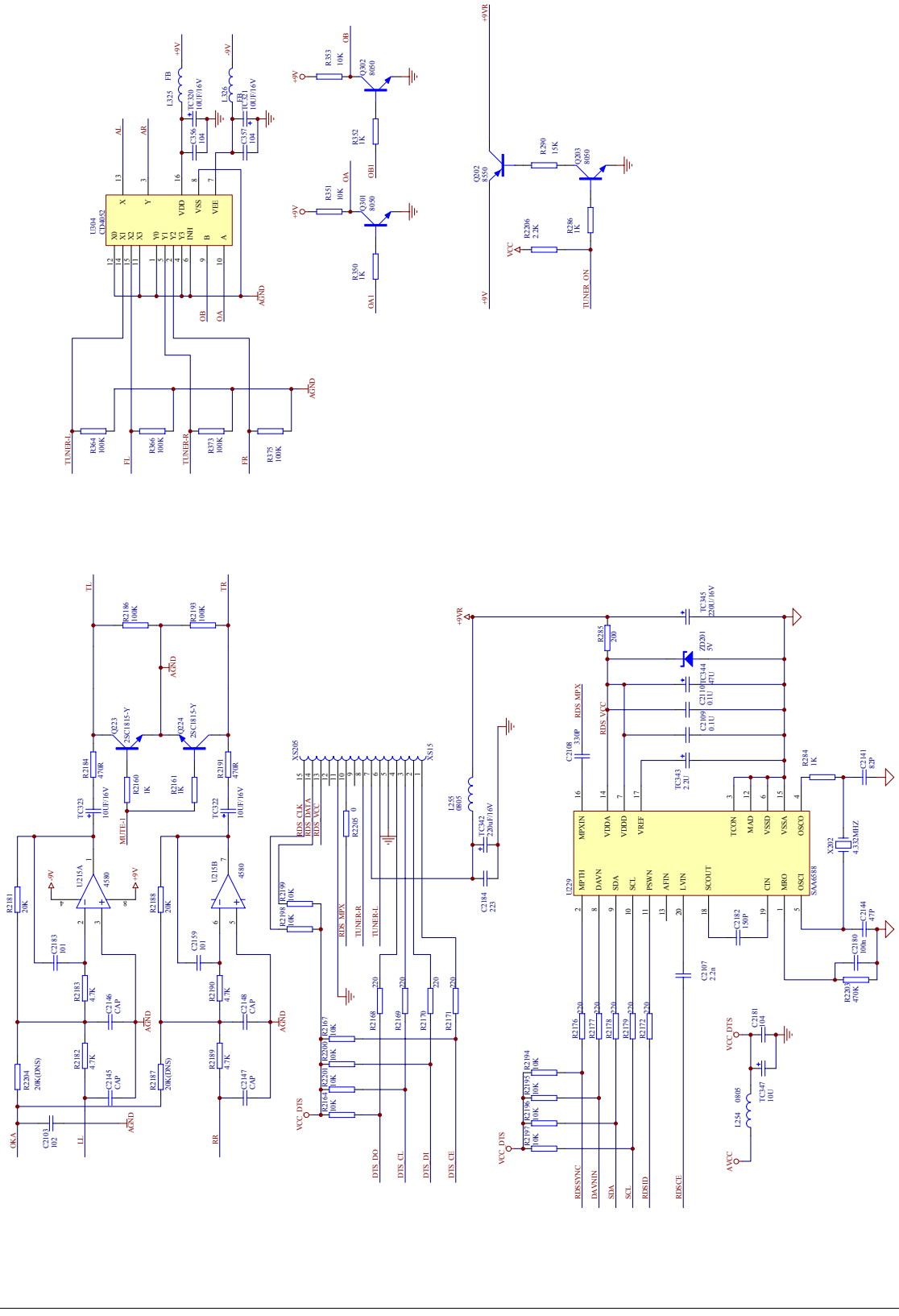
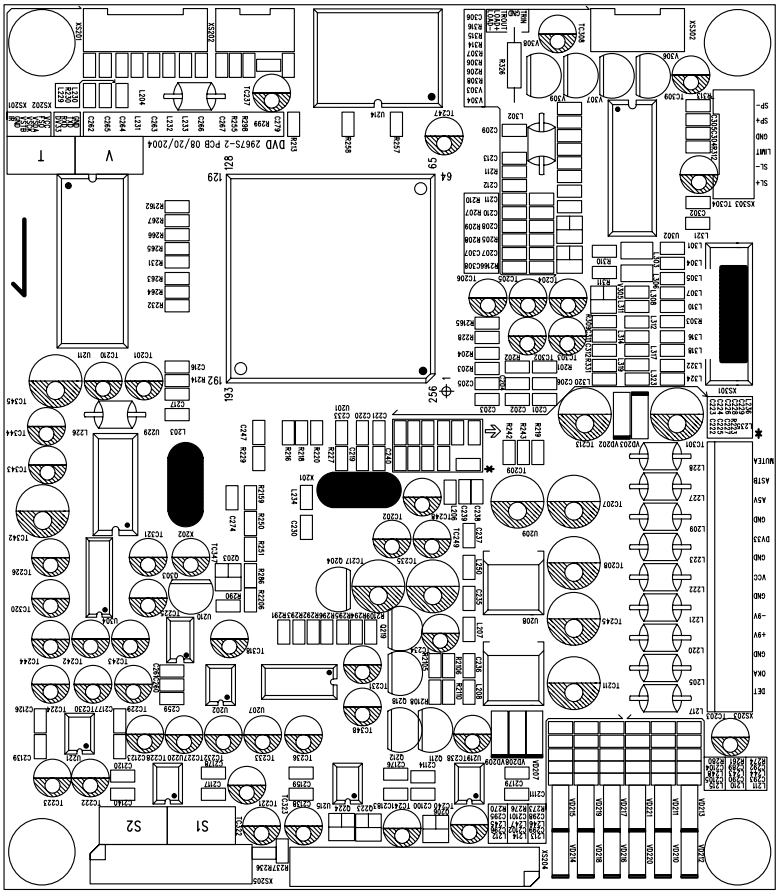


MIAN SCHEMATIC DIAGRAM



10. SPARE PARTS LIST

DT9904S MATERIAL LIST

1. Power board

NO		MATERIAL	SPECIFICATIONS/PART NUMBER	QUANTITY
1		CARBON FILM RESISTOR	1/4W33Ω±5%SHAPED10	1
2		CARBON FILM RESISTOR	1/4W330Ω±5%SHAPED10	1
3		CARBON FILM RESISTOR	1/4W10K±5%SHAPED10	1
4		CARBON FILM RESISTOR	1/4W4.7K±5%SHAPED10	1
5		CARBON FILM RESISTOR	1/4W1MΩ±5%SHAPED10	1
6		METAL FILM RESISTOR	1/4W 3.9K ±1% SHAPED10	1
7		METAL FILM RESISTOR	1/4W12K±1% SHAPED10	1
8		METAL OXIDE FILM RESISTOR	1W330Ω±5%R-SHAPED15×8	1
9		METAL OXIDE FILM RESISTOR	2W39K±5% FLAT-SHAPED15×9	1
	9.1	METAL OXIDE FILM RESISTOR	2W39K±5%FLAT-SHAPED15×7	1
10		METAL OXIDE FILM RESISTOR	2W120K±5%FLAT-SHAPED15×7	1
11		METAL OXIDE FILM RESISTOR	2W10Ω±5%FLAT-SHAPED15×7	1
12		HIGH VOLTAGE RESISTOR	1/2W680K±5%	1
13		PORCELAIN CAPACITOR	50V 100P ±10% 5mm	6
14		PORCELAIN CAPACITOR	50V 104 ±20% 5mm	4
15		PORCELAIN CAPACITOR	1000V 101 +80%-20% 7.5mm	1
	15.1	PORCELAIN CAPACITOR	1000V 101 ±10% 7.5mm	1
16		PORCELAIN CAPACITOR	1000V 103 +80%-20% 7.5mm	1
17		CERAMIC CAPACITOR	CT81 250VAC221±20% 10mm	1
	17.1	CERAMIC CAPACITOR	CT81 250VAC221±10% 10mm	1
18		TERYLENNE	100V 223 ±10% 5mm	1
19		TERYLENNE	275V 104 ±20% 15mm	1
	19.1	TERYLENNE	275V 104 ±10% 15mm	1
20		ANTI-JAMMING CAPACITOR	MKP41 275VAC 103 ±20% 10	1
21		CD	CD11T 16V100u±20%6×12 2.5	3
22		CD	CD11T 25V470u±20%10×16 5	2
23		CD	CD11T 50V47u±20%6×12 2.5	2
24		CD	CD11T 10V1000u±20%8×16 3.5	4
25		CD	CD294 400V47U±20%22×25 10	1
26		MAGNETIC BEADS INDUCTOR	RH354708	1
27		CHOKE COIL	VERTICAL 10UH 1A 5mm	1
28		CHOKE COIL	VERTICAL 10UH 2A 5mm	2
29		SWITCHING POWER TRANSFORME	BCK-28-0286	1
	29.1	SWITCHING POWER TRANSFORME	BCK2801-624	1
30		DIODE	HER105	4
31		DIODE	HER306	1
32		SCHOTTKEY DIODE	SR360	1
33		DIODE	HER107	1
34		VOTAGE REGULATOR DIODE	5.1V 1/2W	1
35		VOTAGE REGULATOR DIODE	9.1V 1W	1
36		DIODE	1N4007	4
37		IC	5L0380R YDTU	1
38		IC	LM431ACZ TO-92	1
	38.1	IC	TL431C TO-226AA(LP)	1
	38.2	IC	431L TO-92	1
	38.3	IC	KA431AZ TO-92	1
39		POWER GRID FILTER	UT-20 40mH ±20% 10×13	2
40		PHOTOELECTRIC COUPLER	HS817	1
41		IC	LM7805 GOLDEN SEALED TO-220	1
42		SOCKET	4-CORE 2.0mm	1

43		SOCKET	10-CORE2.5mm	1
44		SOCKET	2-CORE 8.0mm 2#	2
45		CONNECTION CORDS	Φ0.6 SHAPED10mm	9
46		CONNECTION CORDS	Φ0.6 SHAPED12.5mm	2
47		FUSE	T1.6AL 250V WITH CONDUCTION PIN	1
48		HEAT RADIATOR BOARD	11×15×25 AB009K	2
	48.1	HEAT RADIATOR BOARD	11×15×25 WHITE AB905	2
49		PCB	59904S-1	1
50		POWER BOARD GROUND PIECE	AB903	2
51		TAPPING SCREW	BT 3×8 BLACK	2

2. MAIN FRONT PANEL

NO			SPECIFICATIONS/PART NUMBER	QUANTITY
1		CARBON FILM RESISTOR	1/6W100Ω±5%	1
2		SMD RESISTOR	1/16W 10K ±5% 0603	3
3		SMD RESISTOR	1/16W 51K ±5% 0603	1
4		SMD RESISTOR	25V 104 +80%-20% 0603	3
5		CD	CD11C 10V100U±20%5×7 2	2
6		DIODE	1N4148	1
7		PCB	49904S-1	1
8		LED	ZDC6-2102YGB-A	1
	8.1	LED	TOS-2601BG-B29	1
9		IR SENSOR	AT138BV3 PIN LENGTH27mm	1
10		LIGHT TOUCH RESTORE SWITCH	6×6×1	3
11		IC	PT6961 SOP	1
12		SOFT SPONGE SPACER	20×7×18 DOUBLE FACED, HARD	2
13		SOFT SPONGE SPACER	7×7×10 DOUBLE FACED, HARD	2
14		FLAT CABLE	6-7P 100 2.0 2PLUG, WITH L-SHAPE NEEDLI	1

3. OUTPU

NO			SPECIFICATIONS/PART NUMBER	QUANTITY
1		SMD RESISTOR	1/16W 100Ω ±5% 0603	1
2		CORBON FILM RESISTOR	1/4W68Ω±5%	1
3		SMD RESISTOR	1/16W 2.2Ω ±5% 0603	1
4		CORBON FILM RESISTOR	1/4W220Ω±5%	1
5		SMD CAPACITOR	50V 102 ±10% 0603	6
6		SMD CAPACITOR	25V 104 +80%-20% 0603	2
	6.1	SMD CAPACITOR	50V 104 +80%-20% 0603	2
7		SMD CAPACITOR	50V104 ±20% 0603	1
8		MAGNETIC BEAD INDUCTOR	RH354708	2
9		PHOTOELECTRIC TRANSFORMER	TX179ATW	1
	9.1	PHOTOELECTRIC TRANSFORMER	TX179AT	1
10		OUTJACK	AV4-8.4-6G-3	1
11		OUTJACK	SA-001-012 BLACK	1
12		OUTJACK	AV8-8.4-6G-3	1
13		CABLE SOCKET	15CORE 1.0mm STRAIGHT DUAL LINE PLU	1
14		CONNECTION CORDS	Φ0.6 SHAPED5mm	14
15		CONNECTION CORDS	Φ0.6 SHAPED10mm	4
16		SCART SOCKET	SCART-01	1
17		CONNECTION CORDS	Φ0.6 SHAPED7.5mm	9
18		SMD MAGNETIC BEADS	FCM1608K-221T05	10

19		SMD CAPACITOR	50V 20P ±5% NPO 0603	1
20		PORCELAIN CAPACITOR	50V 20P ±10% NPO 5mm	1
21		DYNATRON	S8050D	3
22		SMD RESISTOR	1/16W 4.7K ±5% 0603	1
23		CARBON FILM RESISTOR	1/4W330Ω±5%	1
24		CARBON FILM RESISTOR	1/4W33Ω±5%	1
25		SMD RESISTOR	1/16W 1K ±5% 0603	1
26		SMD RESISTOR	1/16W 2.2K ±5% 0603	2
27		SMD RESISTOR	1/16W 75Ω ±5% 0603	1
28		SMD RESISTOR	1/16W 0Ω ±5% 0603	11
29		SMD RESISTOR	16V 105 +80%-20% 0603	1
30		PCB	79904S-0	1
31		SOCKET	4-CORE 2.0mm	1

4. OK BOARD

NO			SPECIFICATIONS/PART NUMBER	QUANTITY
1		CARBON FILM RESISTOR	1/6W10Ω±5%SHAPED7.5	2
2		SMD RESISTOR	1/16W 330Ω ±5% 0603	1
3		SMD RESISTOR	1/16W 560Ω ±5% 0603	1
4		SMD RESISTOR	1/16W 1K ±5% 0603	3
5		CARBON FILM RESISTOR	1/6W1K±5%SHAPED7.5	2
6		SMD RESISTOR	1/16W 10K ±5% 0603	5
7		SMD RESISTOR	1/16W 22K ±5% 0603	2
8		SMD RESISTOR	1/16W 100K ±5% 0603	2
9		SMD CAPACITOR	50V 47P ±5% NPO 0603	1
10		SMD CAPACITOR	50V 103 ±10% 0603	1
11		SMD CAPACITOR	50V 104 +80%-20% 0603	3
	11.1	SMD CAPACITOR	25V 104 +80%-20% 0603	3
12		CD	CD110 16V47U±20%5×11 2	3
	12.1	CD	CD11 16V47U±20%5×11 2	3
	12.2	CD	CD11C 16V47U±20%5×7 2	3
13		CD	CD11 16V4.7U±20%5×11 2	2
14		CD	CD11 16V22U±20%5×11 2	1
	14.1	CD	CD11 25V22U±20%5×11 2	1
15		SMD MAGNETIC BEADS	FCM1608K-221T05	1
16		SMD DIODE	1N4148	3
17		IC	NJM4558D DIP	1
	17.1	IC	KA4558 DIP	1
18		MICROPHONE SOCKET	CK3-6.35-106	1
19		SOCKET	8-CORE 2.0mm	1
20		SOCKET	3-CORE 2.0mm	1
21		PCB	69904S-0	1
22		CONNECTION CORDS	Φ0.6 SHAPED7.5mm	8
23		CONNECTION CORDS	Φ0.6 SHAPED5mm	1
24		CONNECTION CORDS	Φ0.6 SHAPED10mm	1
25		CARBON FILM RESISTOR	1/6W3.3K±5%	1
26		SMD RESISTOR	1/16W 3.9K ±5% 0603	4
27		CARBON FILM RESISTOR	1/4W3.9K±5%SHAPED10	1
28		SMD RESISTOR	1/16W 4.7Ω ±5% 0603	2
29		CD	CD11 25V47U±20%5×11 2	2
30		CD	CD11C 16V100U±20%6×7 2.5	3
31		SMD CAPACITOR	50V104 ±20% 0603	5

32		PORCELAIN CAPACITOR	50V 104 ±20% 5mm	1
33		IC	TDA1308 SOP	1
34		EARPHONE SOCKET	2SJ-05231N23	1
	34.1	EARPHONE SOCKET	2SJ-05232N23	1
35		SMD RESISTOR	1/16W 56K ±5% 0603	2

5. DECODE BOARD

NO		SPECIFICATIONS/PART NUMBER	QUANTITY
1		SMD RESISTOR	1/16W 0Ω ±5% 0603	37
2		SMD RESISTOR	1/16W 75Ω ±5% 0603	7
3		CARBON FILM RESISTOR	1/4W2.2Ω±5%	1
4		SMD RESISTOR	1/16W1Ω±5% 0603	6
5		SMD RESISTOR	1/16W 10Ω ±5% 0603	2
6		SMD RESISTOR	1/16W 33Ω ±5% 0603	16
7		SMD RESISTOR	1/16W 150Ω ±5% 0603	1
8		SMD RESISTOR	1/16W 220Ω ±5% 0603	4
9		SMD RESISTOR	1/16W 330Ω ±5% 0603	1
10		SMD RESISTOR	1/16W 470Ω ±5% 0603	2
11		SMD RESISTOR	1/16W 680Ω ±5% 0603	2
12		SMD RESISTOR	1/16W 1K ±5% 0603	27
13		SMD RESISTOR	1/16W 2K ±5% 0603	1
14		SMD RESISTOR	1/16W 1.5K ±5% 0603	3
15		SMD RESISTOR	1/16W 510Ω ±5% 0603	1
16		SMD RESISTOR	1/16W 3.3K ±5% 0603	1
17		SMD RESISTOR	1/16W 4.7K ±5% 0603	21
18		SMD RESISTOR	1/16W 6.8K ±5% 0603	8
19		SMD RESISTOR	1/16W 10K ±5% 0603	22
20		SMD RESISTOR	1/16W 15K ±5% 0603	2
21		SMD RESISTOR	1/16W 20K ±5% 0603	4
22		SMD RESISTOR	1/16W24K±5% 0603	8
23		SMD RESISTOR	1/16W 18K ±5% 0603	1
24		SMD RESISTOR	1/16W 47K ±5% 0603	1
25		SMD RESISTOR	1/16W 150K ±5% 0603	2
26		PRECISION SMD RESISTOR	1/16W 680K ±1% 0603	2
27		PRECISION SMD RESISTOR	1/16W 750K ±1% 0603	1
28		SMD RESISTOR	1/16W 100K ±5% 0603	16
29		CD	CD11 16V10U±20%5×11 2	29
30		CD	CD11 16V1U±20%5×11 2	2
31		CD	CD11 16V220U±20%6×12 2.5	10
32		CD	CD11 16V47U±20%5×11 2	13

33		SMD RESISTOR	50V 20P ±5% NPO 0603	1
34		SMD RESISTOR	50V 27P ±5% NPO 0603	2
35		SMD RESISTOR	50V 47P ±5% NPO 0603	17
36		SMD RESISTOR	50V 101 ±5% NPO 0603	10
37		SMD RESISTOR	50V 331 ±5% NPO 0603	2
38		SMD RESISTOR	50V 151 ±5% NPO 0603	2
39		SMD RESISTOR	50V 104 +80%-20% 0603	84
	39.1	SMD RESISTOR	25V 104 +80%-20% 0603	84
40		SMD RESISTOR	16V 105 +80%-20% 0603	8
41		SMD RESISTOR	50V 102 ±10% 0603	11
42		SMD RESISTOR	50V 122 ±10% 0603	8
43		SMD RESISTOR	50V 152 ±10% 0603	1
44		SMD RESISTOR	50V 222 ±10% 0603	2
45		SMD RESISTOR	50V 153 ±10% 0603	1
46		SMD RESISTOR	50V 223 ±10% 0603	1
47		SMD RESISTOR	16V 333 ±10% 0603	1
48		SMD RESISTOR	16V 473 ±10% 0603	2
49		SMD RESISTOR	16V474 +80%-20% 0603	1
50		SMD RESISTOR	10UH ±10% 2012	2
51		SMD RESISTOR	1.8UH ±10% 1608	6
52		MAGNETIC BEAD INDUCTOR	RH354708	11
53		SMD MAGNETIC BEAD	FCM1608K-221T05	39
54		SMD MAGNETIC BEAD	FCM2012V-221T07	2
55		SMD RESISTOR	1/16W 4.7Ω ±5% 0603	1
56		SMD DIODE	1N4148	18
	56.1	SMD DIODE	LS4148	18
	56.2	SMD DIODE	LL4148	18
57		SMD DYNATRON	8050D	3
58		DYNATRON	C8050	2
59		DYNATRON	8550C	3
60		SMD DYNATRON	9014C	1
61		DYNATRON	9015C	1
62		DYNATRON	C1815Y	1
63		SMD DYNATRON	C1815	8
64		DYNATRON	2SA1015	3

65		SMD DYNATRON	3904	1
66		SMD DYNATRON	2SK3018	2
67		SMD DYNATRON	2SB1132	2
68		IC	NJM4558M SOP	4
	68.1	IC	4580 SOP	4
	68.2	IC	4558 SOP	4
69		IC	MM74HCU04M SOP	1
	69.1	IC	HCU04 SOP	1
70		IC	HY57V641620HGT-7 TSOP	1
	70.1	IC	KSV464P4JA-70 TSOP	1
71		IC	LM1117MP-ADJ SOT-223	1
72		IC	CS4360 SSOP	1
73		IC	CS5333 SSOP	1
74		IC	24C02N SOP	1
75		IC	MT1389EE QFP	1
	75.1	IC	MT1389FE QFP	1
76		IC	BA5954FP HSOP	1
77		IC	36C7T 3MCD4052BM SOP	1
78		CRYSTAL OSCILLATOR	27.00MHz 49-S	1
79		CABLE SOCKET	6/5 P1.25mm STRAIGHT DUAL LINE PLUG	1
80		CABLE SOCKET	15P 1.0mm STRAIGHT DUAL TOUCH PLUG	1
81		PCB	2967S-2	1
82		SOCKET	5 P 2.0mm	1
83		SOCKET	7P 2.0mm	1
84		SOCKET	6P 2.0mm	1
85		SOCKET	13 P 2.5mm	1
86		CABLE SOCKET	24P 0.5mm SMD UP CONNECT WITH BUTTC	1

11. APPENDIX-AM/FM Tuner Specificadtion

AM/FM Tuner Specification

イホソシ

			TFCF1U800A
END CUST	CUST	CUST MODEL NO.	ALPS MODEL NO.

					APPD	CHKD	DSGD	
								TITLE PRODUCT **TFCF1U** SPECIFICATION
					DOCUMENT NO.			
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				0/11

AM/FM Tuner Specification

1.Application product P/N TFCF1U TYPE FM/AM TUNER

1-1.Manufacturing location Japan and People Republic of China and Malaysia

2.Specification Customer Specification USA / CND Version

3.Test conditions

Usual standard test with next condition

Measurement shall be started to minutes after power applied

The apply voltege must be regulated +9 v ± 2%

Condition Temperature :5。ｵ35。

Humidity :45。ｵ85 % Rh

If there is an objection to test result, they set up with next test condition

Condition Temperature :20±2。

Humidity :60。ｵ70 % Rh

Unit: Scale / Tolerance

	Components	Materials Finish/ Specifications				Components	Materials Finish/ Specifications		
1			6						
2			7						
3			8						
4			9						
5			1		0				

					DSGD.			
					CHKD.	TITLE PRODUCT		
						TFCF1U SPECIFICATION		
					APPD			
						(1/11)		
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

4.General Specifications

4-1.FM Tuner General Specifications

Frequency Range	87.5MHz。ォ108.0MHz
STEP Frequency	50KHz/100KHz
Intermediate Frequency	10.7MHz(Upper Heterodyne)
Operating Temperature	ィC20。ォ」ォ70。
ANT Input Impedance	75 Unbalanced

4-2. PLL General Specifications

Cutout port function		B01	B02					
		FM/AM	。ェ					
Seral date	0	AM	。ェ					
	1	FM	。ェ					

Crystal Frequency :75KHz

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			(2/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

4-3.AM Tuner General Specifications

Frequency Range	530KHz｡ｵ1710KHz
STEP Frequency	10KHz or 9KHz
Intermediate Frequency	450KHzｺﾕ(Upper Heterodyne)
Operating Temperature	ｲC20｡ｵﾚｵ70｡
ANT Input Impedance	Use Dummy antenna which specified If there hanppened,should use loop antenna

5.Machanical specifications

Dimensions	See Assembly drawing
Core torque	3｡ｵ30mN·m
Variable Resistor Torque	3｡ｵ30mN·m
Antenna Connector	FMﾚﾕSticker S DIN 45325/F AMﾚﾕSMK LPR0210-XX09 or ﾏ犒高ｱﾆｷ

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(3/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

6-1.Terminal load connections」ユ

Specified jig should be used for measurement

Jig circuit follows 10-2

During FM measurement,use specified by IHF T-200(200Hz。ォ15KHz B.P.F)

Filter for audio output of filer *Less than 200Hz 」ユ18dB/act.out

*220Hz and 15KHz」ユ-3dB MIN

19KHz」ユ-30dB MAX

6-2.Standard connection diagram

FM section」ユ

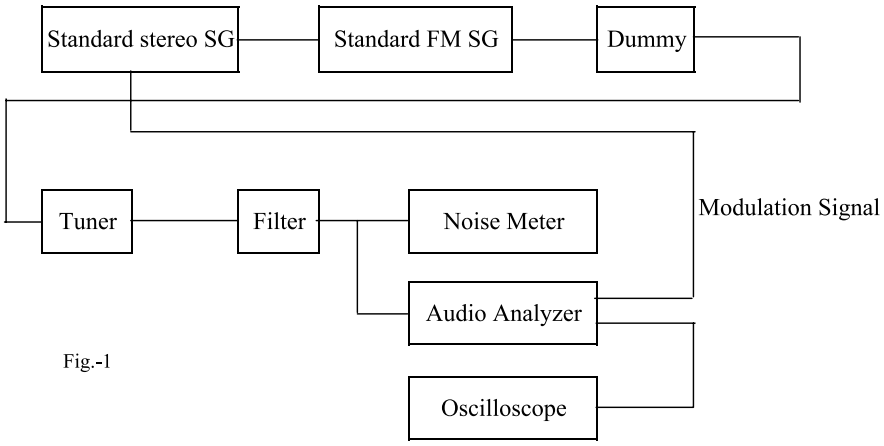


Fig.-1

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(4/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

6-3.Test Modulation

FM」ｺMONO 1KHz 75.0KHz dev

STEREO 1KHz L」ｵR 67.5KHz dev

PILOT 7.5KHz dev

Antenna Input 75ﾗｸ Opened SSG-Dunmy los

RF Input Level 60dBu

AM」ｺ400hz 30% mod

Use Dunmy antenna which specified by ALPS.

RF Input level」ｺ94dBu(ANT Input)

7.DC Specification

ITEM	TEST Condition	SPEO ｹ貂			UNIT
		MIN	TYP	MAX	ｵ･ﾎｻ
Supply Voltage 」ｵ9v	Off Station	8.5	9	9.5	V
Supply Currant 」ｵ9v	Off Station	。I	65	90	mA

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(5/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

8.FM Tuner Electrical Specification (Measurement Points Unless Otherwise Stated are 87.5,98,100MHz.
Concerning MONORAL test shall be at L out terminal)

ITEM	TEST Condition			SPEC ヶ貂			UNITヶ貂
				MIN	TYP	MAX	
50dB S/N Sensitivity			87.5MHz	。I	17	25	dBu
			98.0MHz	—	15	25	
			106.0MHz	。I	17	25	
IHF Sensitivity	Distortion 3%		87.5MHz	。I	14	20	dBu
			98.0MHz	。I	12	20	
			106.0MHz	。I	14	20	
Max S/N Ratio		MONO	98.0MHz	65	72	。I	dB
		STEREO	98.0MHz	60	67	。I	
Distortion		MONO	98.0MHz	。I	0.2	1.5	%
		STEREO	98.0MHz	。I	0.3	2	
Distortion with strong signal	120dBu	MONO	98.0MHz	。I	0.2	2	%
		STEREO	98.0MHz	。I	0.3	2.5	
Audio Output Level	L and R out	MONO	98.0MHz	0	3	6	dBs
		STEREO	98.0MHz	-1	2	5	
Stereo Separation			98.0MHz	25	40	—	dB
Stereo Work Level	SDCOJ⊐0 SDCTJ⊐0		98.0MHz	10	18	27	dBu
Tuned Level	SDCOJ⊐0 SDCTJ⊐0		98.0MHz	10	18	27	dBu
Auto Stop Level	SDCOJ⊐0 SDCTJ⊐0		98.0MHz	10	20	33	dBu

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(6/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

ITEM	TEST Condition		SPEC ケ貂			UNITケ貂
			MIN	TYP	MAX	
Image Rejection	MONO	98.0MHz	17	23	—	dB
Carrier Leak		98.0MHz	28	33	—	dB
Emphasis	-12.29 IHF Filter Off	98.0MHz	-3	0	3	dB
Pilot Margin		98.0MHz	4	10	—	dB
Adjacent Channel Selectivity	±400KHz	98.0MHz	20	30	—	dB
AM Rejection		98.0MHz	40	60	—	dB
I.F. Rejection		98.0MHz	60	90	—	dB
Spurious Response Patio		98.0MHz	40	50	—	dB
Spurious Radiation	Meat FOC Requirements Note1.		3	10	—	dB
Antenna Leakage	Meat FOC Requirements Note1.		3	8	—	dB

Note1.Spurlous Radiation and Antenna Leakage 」ヨUse Radio Set Provided by CUSTMOR

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			(7/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

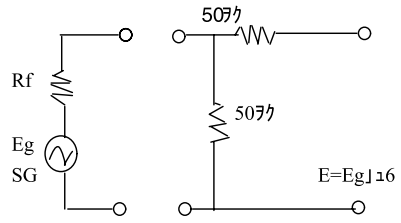
9.AM Tuner Electrcical Specification (Test shall be at L out Terminal)

ITEM	TEST Condition		SPEC ㄅ貂			UNITㄅ貂
			MIN	TYP	MAX	
S/N 20dB Sensitivity		620KHz	—	54	61	dBu
		1050KHz	—	48	57	
		1490KHz	—	48	56	
Max S/N		1050KHz	43	54	—	dB
Distortion		1050KHz	—	1.3	2.5	%
Distortion with Strong Signal	104dBu RF Input Level	1050KHz	—	1.3	2.5	%
Audio Output Level	L.R OUT	1050KHz	-11	-7	—	dBs
One Signal Selectivity	±10KHz	1050KHz	18	27	—	dB
Image Rejection		1050KHz	30	36	—	dB
I.F. Rejection		1050KHz	45	55	—	dB
AGC Form		1050KHz	44	50	—	dB
Audio Frequency Response	O Point 400Hz 100Hz	1050KHz	-10	-5.5	—	dB
	Refㄱ400Hz 4KHz	1050KHz	-22	-16	—	
Auto stop level		1050KHz	—	50	66	dBu
Tuned Level		1050KHz	—	52	61	dBu

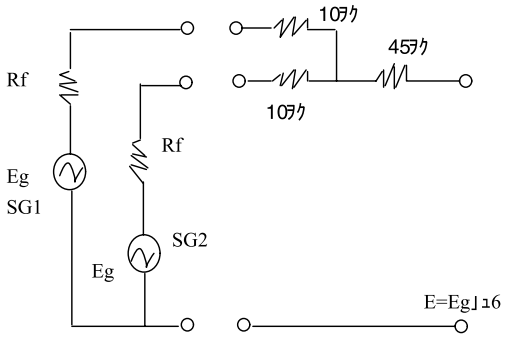
					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
							(8/11)	
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

10-1.ANT PAD

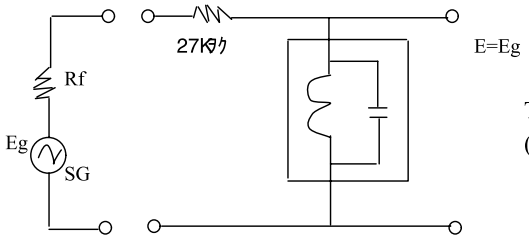
(1).FM1 SIGNAL



(2).FM2 SIGNAL



(3).AM1 SIGNAL



Trans mand TOKO
(LイP15.2uH , C=30PF)

ANT Input Signal Voltage is Open Voltage ON SSG

NOTE」ユUse Test jig which specified

Rf = 50ヲク

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			(9/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

11.Printed-Wiring Board Material

ITEM	Contants		
Material Suppliar	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD
Trade Name	MCL － 437F	MCL － 437F	MCL － 437F
UL Grade	94V － 0	94V － 0	94V － 0
Edging Supplier	NIPPON ELEC Co.,LTD	NIPPON ELEC Co.,LTD	PNE PCB LTD.
UL Type Designation	NE 49S△	NE M PF2△	PNE － 1B
UL File NO.	E41166 (S)	E41166 (S)	E67640

Material Suppliar	SUZHOU Matsushita Electric Work Co.,LTD	Suzhou Matsushita Electric Work Co.,LTD
Trade Name	R8700	R8700
UL Grade	94V － 0	94V － 0
Etching Supplier	Yamanashi Matsushita Elactic Work Co.,LTD	Suzhou Matsushita Electric Works(PWB) Co.,LTD
UL Type Designation	NTP－N870A－T YMEW－N870A－T	SMEW－N870A－T
UL File NO.	E107496 (S)	E164387 (S)

Dimension of Print-Wiring Board	56 × 49

					DSGD.			
					CHKD.	TITLE		PRODUCT
						TFCF1U		SPECIFICATION
					APPD			
								(11/E)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

Description of DI control Data

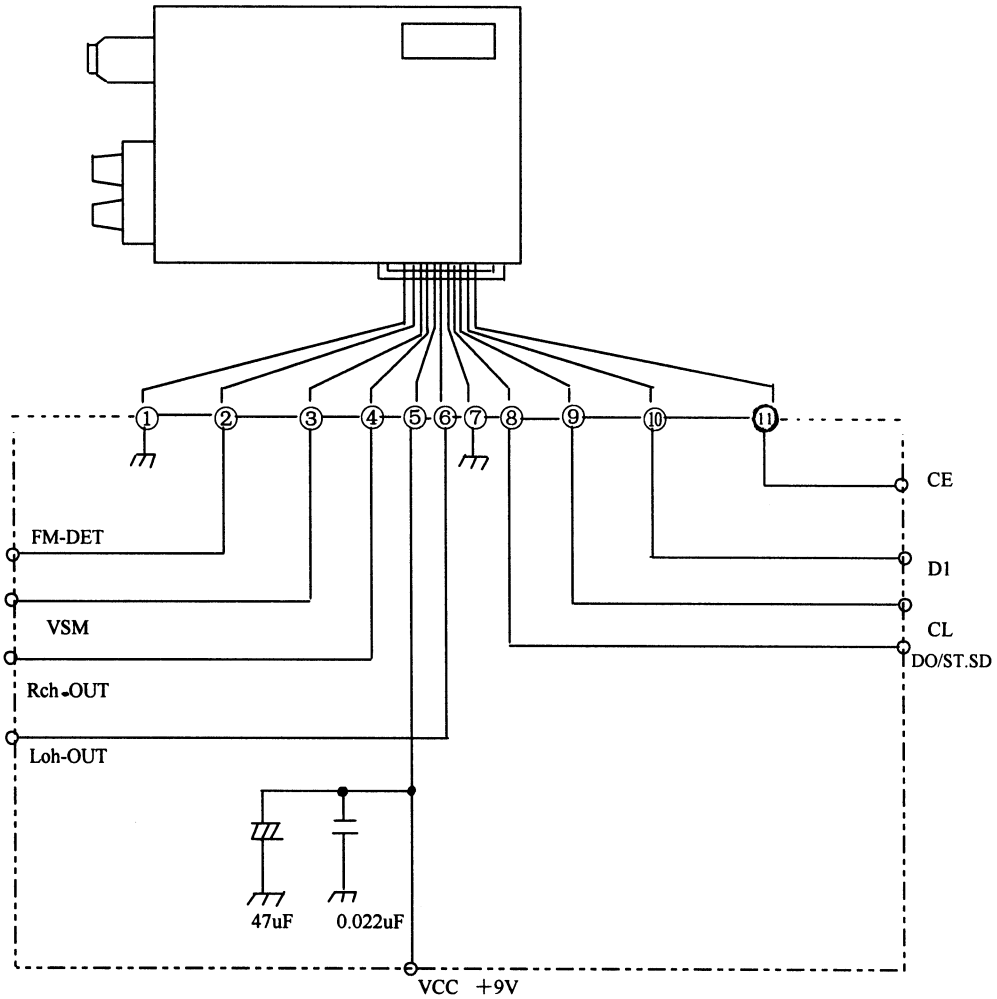
<table>
<tr><th>No.</th><th>Control block data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data

P0 to P15
DVS,SNS</td><td>
• Data to set the dividing number of programmable divider
Binary value with P15 assued to be MSB. LSB varies according to DVS and SNS.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>set dividing number(N)</th><th>actual dividing number</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the set value</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>Set value</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>Set value</td></tr>
</table>
* P0 to P3 invalid when LSB:P4
• To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input</th><th>Operation frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr>
</table>
</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data

R0 to R3</td><td>
• Reference frequency (fref) selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25 kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
* PLL INHIBIT
• The programmable divider and IF counter stop, with FMIN,AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance.
</td><td></td></tr>
</table>

10-2. TEST JIG

NOTE: Use Test jig which specified



					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			(10/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

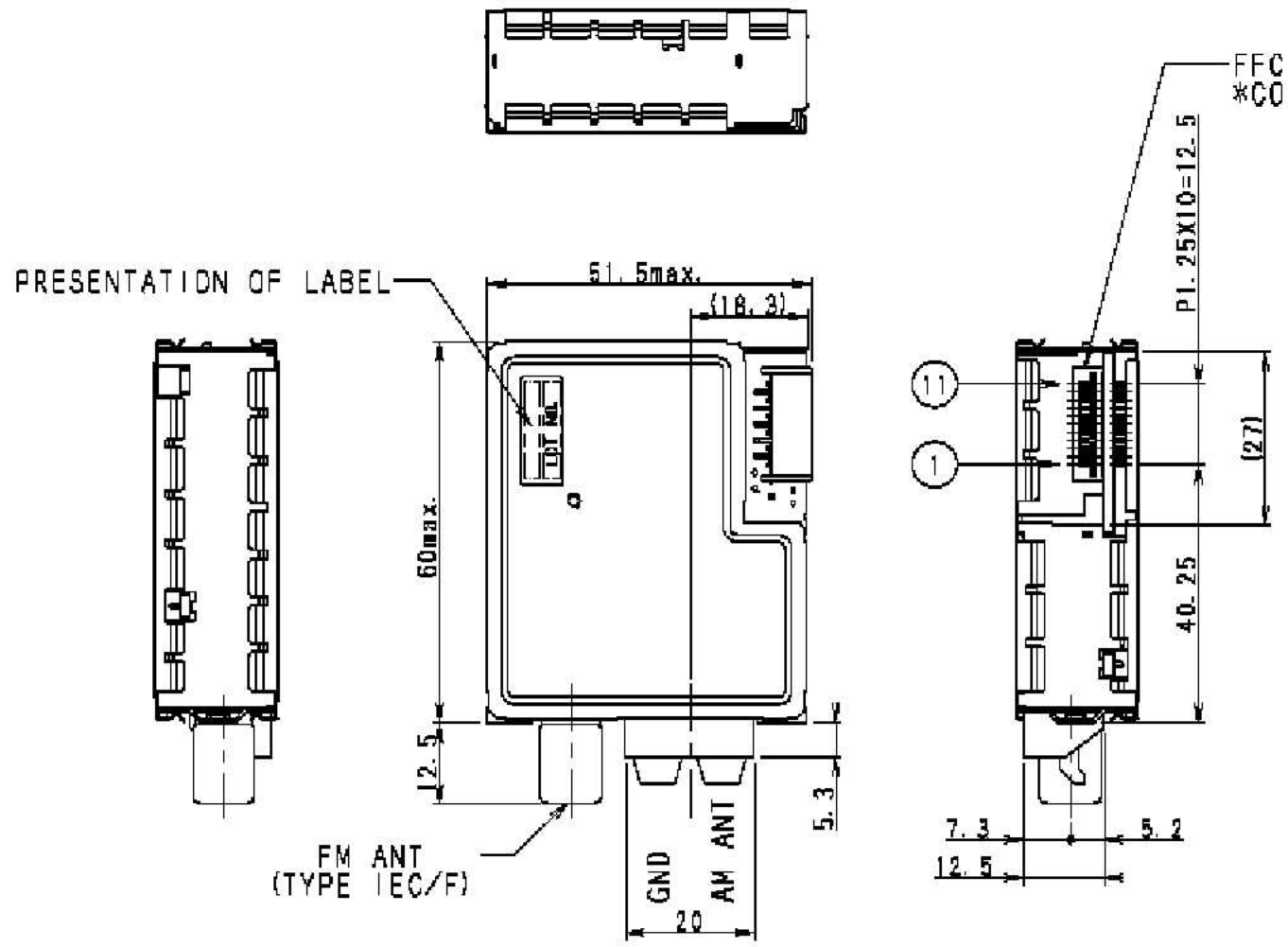
11.Printed-Wiring Board Material

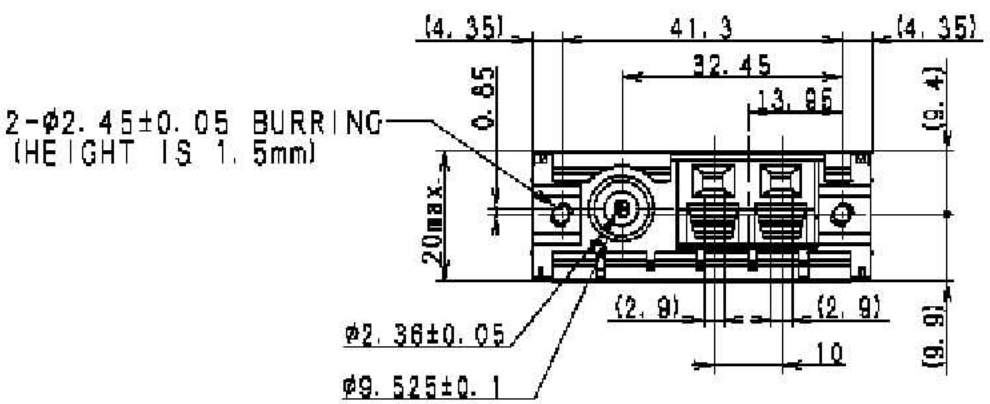
ITEM	Contants		
Material Suppliar	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD
Trade Name	MCL ｣ｪ 437F	MCL ｣ｪ 437F	MCL ｣ｪ 437F
UL Grade	94V ｣ｪ 0	94V ｣ｪ 0	94V ｣ｪ 0
Edging Supplier	NIPPON ELEC Co.,LTD	NIPPON ELEC Co.,LTD	PNE PCB LTD.
UL Type Designation	NE 49S。	NE M PF2。	PNE ｣ｪ 1B
UL File NO.	E41166 (S)	E41166 (S)	E67640

Material Suppliar	SUZHOU Matsushita Electric Work Co.,LTD	Suzhou Matsushita Electric Work Co.,LTD
Trade Name	R8700	R8700
UL Grade	94V ｣ｪ 0	94V ｣ｪ 0
Etching Supplier	Yamanashi Matsushita Elactic Work Co.,LTD	Suzhou Matsushita Electric Works(PWB) Co.,LTD
UL Type Designation	NTP｣ｪN870A｣ｪT YMEW｣ｪN870A｣ｪT	SMEW｣ｪN870A｣ｪT
UL File NO.	E107496 (S)	E164387 (S)

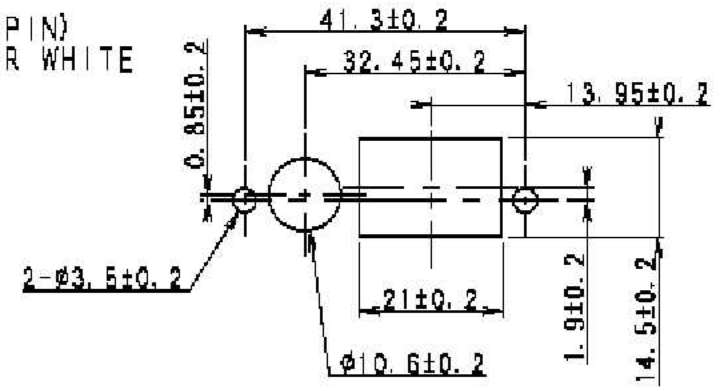
Dimension of Print-Wiring Board	56 × 49

					DSGD.			
					CHKD.	TITLE PRODUCT **TFCF1U** SPECIFICATION		
					APPD	(11/E)		
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

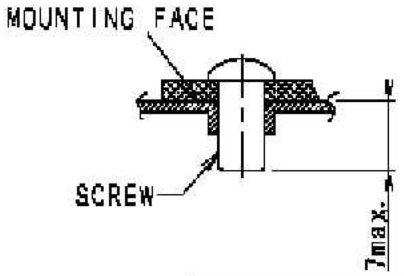




RECOMMENDED MOUNTING HOLE(REFERENCE ONLY)



NOTE 1. TOLERANCES ARE ±0.5mm.
UNLESS OTHERWISE SPECIFIED.
2. ALPS CAN ALTER COVER HOLE DESIGN
WITHOUT NOTICE IF NO ELECTRICAL DEGRADATION.
3. SCREW LENGTH FROM MOUNTING FACE IS 8mm MAX.



No.	NAME
①	GND
②	FM DET
③	VSM
④	Rch OUT
⑤	Vcc
⑥	Lch OUT
⑦	GND
⑧	DO
⑨	CL
⑩	DI
⑪	CE

		TFCF1U
PRESENTATION OF LABEL	CUST PARTS NO.	ALPS MODEL NO.

PART NO.	NAME	MATERIAL	SPEC.	FINISH

ZONE	SYMB.	DATE OR NO.	APPD.	CHKD.	DSGD.
C-5	B1	Sep. 9.'02	M. K	Y. S	J. K
D-1	A1	K020108	H. O	Y. S	J. K

DSGD. CHKD. APPD.

SCALE 1:1

UNIT mm

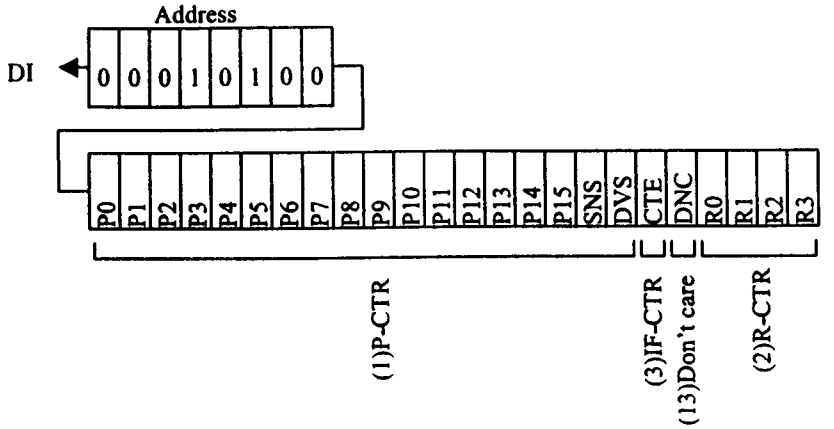
TITLE TFCF1 ASSEMBLY DRAWING

KEY NO. U111A6 (A3・■■用紙)

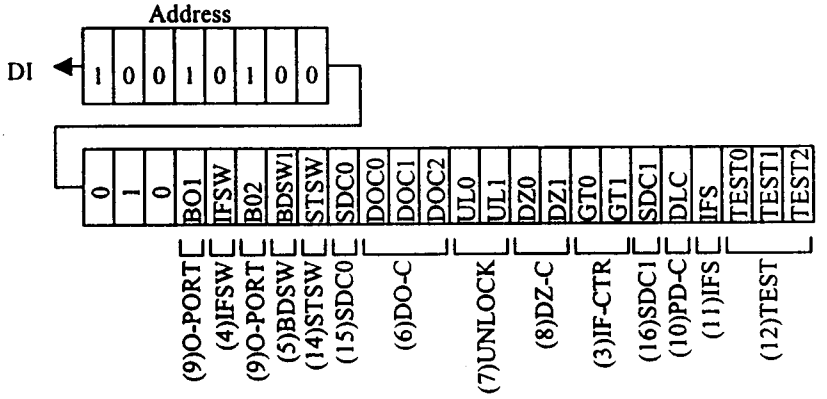
59

Composition of DI control data (serial data input)

(1) IN mode



(2) IN2 mode



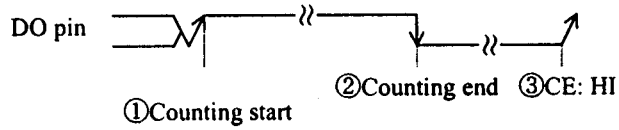
Description of DI control Data

<table>
<tr><th>No.</th><th>Control block data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data

P0 to P15
DVS,SNS</td><td>
• Data to set the dividing number of programmable divider
Binary value with P15 assued to be MSB. LSB varies according to DVS and SNS.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>set dividing number(N)</th><th>actual dividing number</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the set value</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>Set value</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>Set value</td></tr>
</table>
* P0 to P3 invalid when LSB:P4
• To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input</th><th>Operation frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr>
</table>
</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data

R0 to R3</td><td>
• Reference frequency (fref) selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25 kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
* PLL INHIBIT
• The programmable divider and IF counter stop, with FMIN,AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance.
</td><td></td></tr>
</table>

<table>
<tr><td>(3)</td><td>CTE
GT0,GT1</td><td>
<table>
<tr><th>GT1</th><th>GT0</th><th>Counting time</th><th>Wait time</th></tr>
<tr><td>0</td><td>0</td><td>4 ms</td><td>3 to 4 ms</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr>
<tr><td>1</td><td>0</td><td>16</td><td>3 to 4</td></tr>
<tr><td>1</td><td>1</td><td>32</td><td>3 to 4</td></tr>
</table>
</td><td>IFS</td></tr>
<tr><td>(4)</td><td>MUTE control data
IFSW</td><td>• Data to determine the output of output port IFSW, controlling the MUTE function.
"Data"=0: at receiving
1: MUTE</td><td></td></tr>
<tr><td>(5)</td><td>FM/AM BAND selection control data
BDSW</td><td>• Data to determine the output of output port BDSW, controlling selection of BAND.
"Data"=0: AM
1: FM</td><td></td></tr>
<tr><td>(6)</td><td>DO pin control data

DOC0
DOC1
DOC2</td><td>• Data to control DO pin output
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin condition</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when unlock is detected.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC(See the item with asterisk below)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Low when SDON</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Low when stereo</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
• The open condition is selected at power ON/reset.
* IF counter counting end check
 

① With end-UC set and IF counter starting (CTE=0→1), DO pin opens automatically.
② At end of counting of the IF counter, DO pin goes LOW and check on counting end can be made.
③ DO pin opens when serial data is entered/output (CE pin: Hi)
Note: DO pin is always in the open condition during data input (IN1 and IN2 modes, during CE: Hi period), regardless of DO pin control data (DOC0 to 2). In the DO pin condition during data output (OUT mode, CE-Hi period), the content of internal DO serial data is output in synchronization with CL, regardless of DO pin control data (DOC).</td><td>UL0,UL1
CTE</td></tr>
</table>

<table>
<tr><th>No.</th><th>Control block data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(7)</td><td>Unlock detection data

UL0,UL1</td><td>• Phase error (ϕE) detection width selection data to judge if PLL is locked.
Phase error exceeding the detection width is judged that PLL is locked
(*:don't care)
<table><tr><th>UL1</th><th>UL0</th><th>ΦE Detection width</th><th>Detection output</th></tr><tr><td>0</td><td>0</td><td>Stop</td><td>Open</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Direct output of ϕE</td></tr><tr><td>1</td><td>*</td><td>±6.67μ</td><td>ϕE extended by 1 to 2 ms</td></tr></table>* DO pin is LOW. Serial data output: UL = 0.</td><td>DOC0
DOC1
DOC2</td></tr>
<tr><td>(8)</td><td>Phase comparator control data

DZ0,DZ1</td><td>• Data to control the dead zone of phase comparator
<table><tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr><tr><td>0</td><td>0</td><td>DZA</td></tr><tr><td>0</td><td>1</td><td>DZB</td></tr><tr><td>1</td><td>0</td><td>DZC</td></tr><tr><td>1</td><td>1</td><td>DZD</td></tr></table>Dead zone width: DZA<DZB<DZC<DZD</td><td></td></tr>
<tr><td>(9)</td><td>Output port data

$\overline{BO1}$,$\overline{BO2}$</td><td>• Data to determine the output of output ports $\overline{BO1}$ and $\overline{BO2}$
"Data"=0: OPEN
1: Low</td><td></td></tr>
<tr><td>(10)</td><td>Charge pump control data

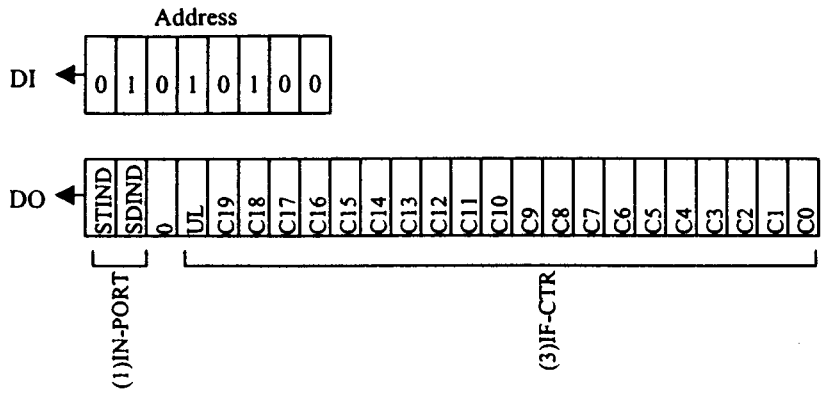
DLC</td><td>• Data to enforce control of charge pump output
<table><tr><th>DLC</th><th>Charge pump output</th></tr><tr><td>0</td><td>Normal</td></tr><tr><td>1</td><td>Forced to LOW</td></tr></table>In case of dead lock because of VCO oscillation stop when the VCO control voltage (Vtune) is 0 V, it is possible to clear dead lock by setting the charge pump output to LOW and V tune to Vcc. (Dead lock clear circuit)</td><td></td></tr>
<tr><td>(11)</td><td>IFS</td><td>• Normally, set Data = 1. Setting Data = 0 causes the input sensitivity worsening mode and the sensitivity decreases by about 10 to 30mVrms.</td><td></td></tr>
<tr><td>(12)</td><td>LSI test data
TEST0 to 2</td><td>• LSI test data
TEST0
TEST1] All to be set to "0"
TEST2
All set to zero at power ON/reset</td><td></td></tr>
<tr><td>(13)</td><td>DNC</td><td>• Set data = 0.</td><td></td></tr>
<tr><td>(14)</td><td>Forced monaural control data

STSW</td><td>• Data to determine the output of output port STSW, controlling the forced stereo functions.
"Data"=0: MONO
1: STEREO</td><td></td></tr>
<tr><td>(15)
(16)</td><td>SD sensitivity control data

SDC0
SDC1</td><td>• Data to determine the output of output ports SDC0 and SDC1, controlling the SD sensitivity
"Data"=SDC0: 0, SDC1: 0 → SD sensitivity = 42dBuV (Typ)
SDC0: 0, SDC1: 1 → SD sensitivity = 45dBuV (Typ)
SDC0: 1, SDC1: 0 → SD sensitivity = 51dBuV (Typ)
SDC0: 1, SDC1: 1 → SD sensitivity = 56dBuV (Typ)</td><td></td></tr>
</table>

DO control data (serial data output) composition

(1) OUT mode

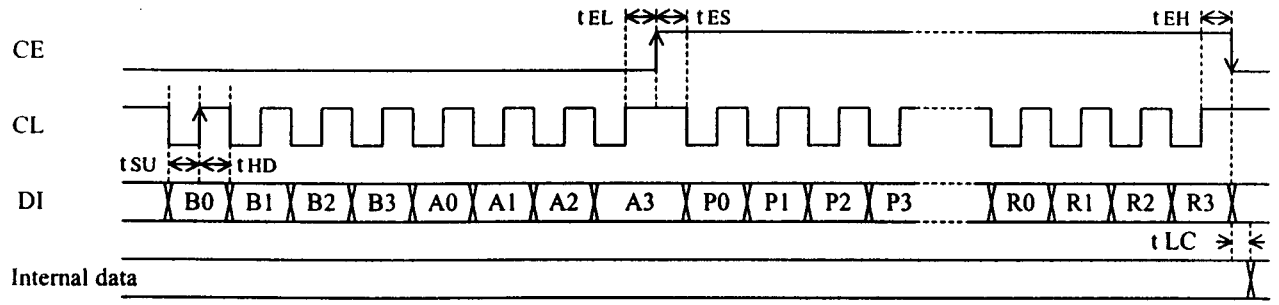


Description of the DO output data

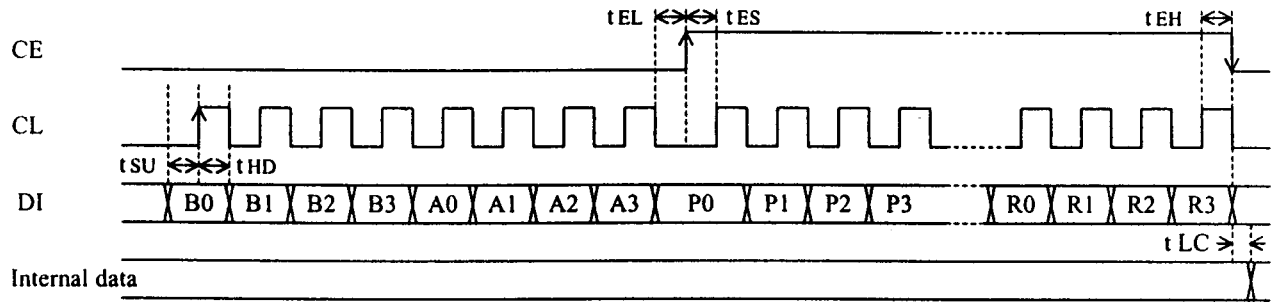
No.	Control block data	Description	Related data
(1)	Stereo and SD indicators control data STIND, SDIND	• Data latching stereo and SD indicator conditions. Latching made in the data output (OUT) mode. STIND ← Stereo indicator condition 0: ST ON, 1: ST OFF SDIND ← SD indicator condition 0: SD ON, 1: SD OFF	
(2)	PLL unlock data UL	• Data latching the content of unlock detection circuit UL ← 0: At unlock 1: At lock or detection stop mode	UL0 UL1
(3)	IF counter, binary counter C19 to C0	• Data latching the content of IF counter (20-bit binary counter) C19 ← MSB of binary counter C0 ← LSB of binary counter	CTE GT0 GT1

Serial data input (IN1/IN2) t SU, tHD, tEL, tES, tEH ≧ 0.75 μs t LC < 0.75 μs

① CL: Normally HI

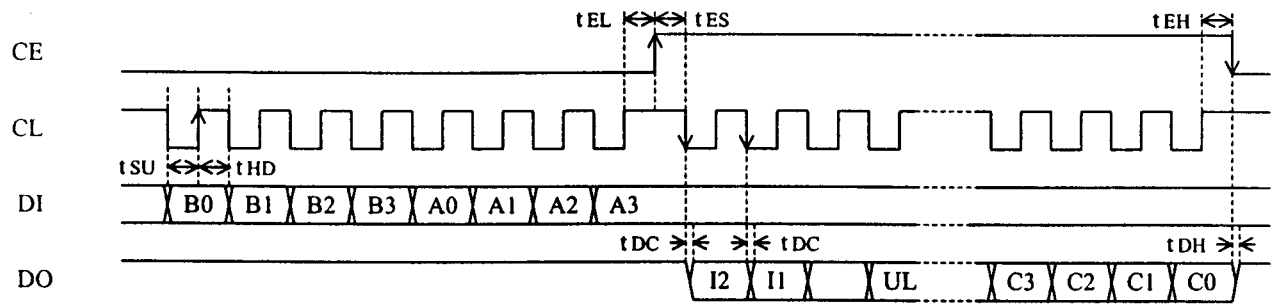


② CL: Normally LOW

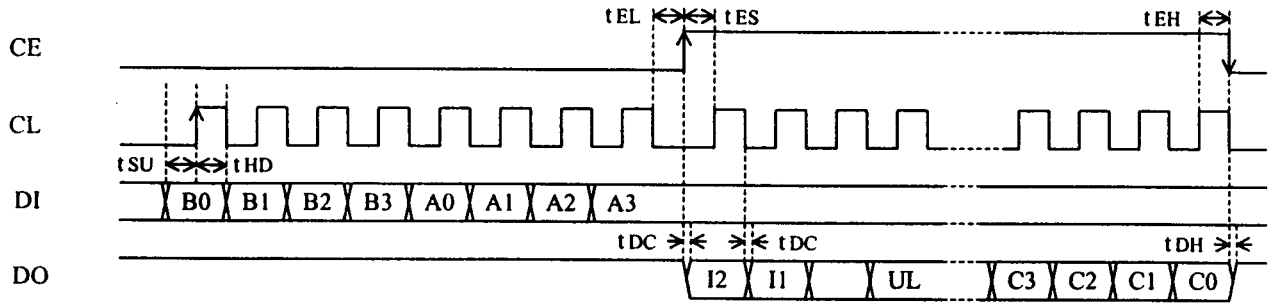


Serial data output (OUT)tSU, tHD, tEL, tES, tEH ≧ 0.75 μs tDC, tDH < 0.35 μs

① CL: Normally Hi

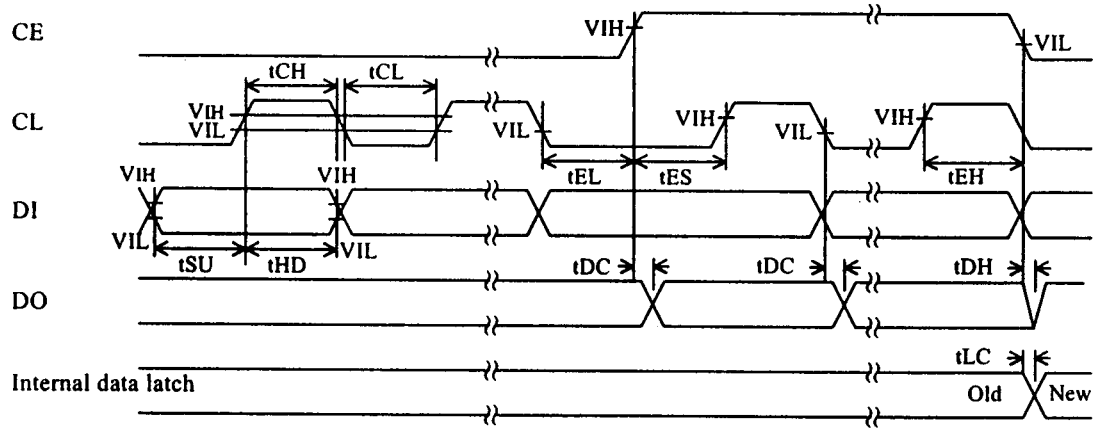


② CL: Normally low

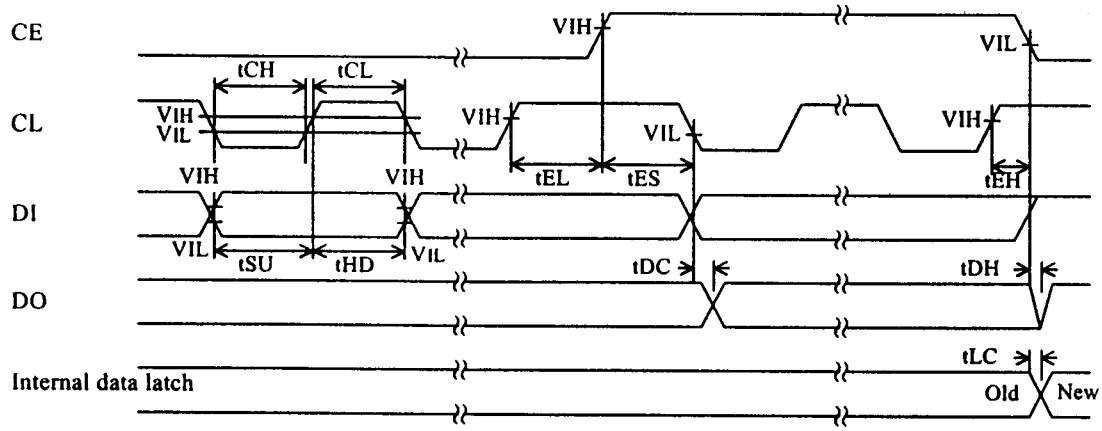


(Note) DO pin is an Nch open drain pin, so that the data varying time (tDC and tDH) differs depending on the pull-up resistance and substrate capacity.

Serial data timing



<< When CL stops at the "L" level >>



<< When CL stops at the "H" level >>

Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	tSU	DI,CL		0.75			μs
Data hold time	tHD	DI,CL		0.75			μs
Clock "L" level time	tCL	CL		0.75			μs
Clock "H" level time	tCH	CL		0.75			μs
CE wait time	tEL	CE,CL		0.75			μs
CE setup time	tES	CE,CL		0.75			μs
CE hold time	tEH	CE,CL		0.75			μs
Data latch change time	tLC					0.75	μs
Data output time	tDC	DO,CL	Differs depending on the pull-up resistance and substrate capacity			0.35	μs
	tDH	DO,CE					

最新カスタムIC搭載により容積30%減（当社従来品比）の小形化を実現。
30 % less volume than our traditional models thanks to state-of-the-art customized IC.

■特長
- 独自開発のICを搭載し、当社従来品容積比約30%減の小形化（60ml）を達成。
- ANTコネクタ部を直出構造とし、内部をフルシールド化することにより、優れたノイズ除去能力を発揮。

■用途
- マイクロコンポーネントステレオ、MDラジカセ、DVD、オーディオレシーバなど多機能化、小形化傾向の進む、各種オーディオ機器、ミニコンポーネントステレオ、各種多機能オーディオ機器。

■Features
- Uniquely developed IC has achieved a small volume of 60 ml, 30 % less than our traditional models.
- Fully shielded structure with ANT connector effectively filters out noise.

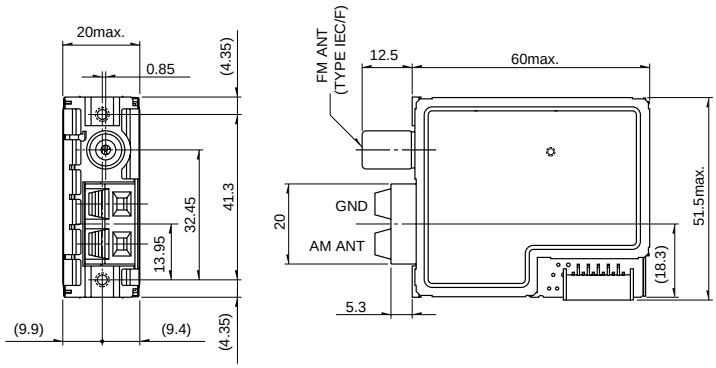
■Applications
- Offers a wide range applications to audio equipment, especially multi-functional, compact audio equipment, such as mini- and micro-component stereo equipment, MD radio cassette recorders, DVDs and audio receivers.

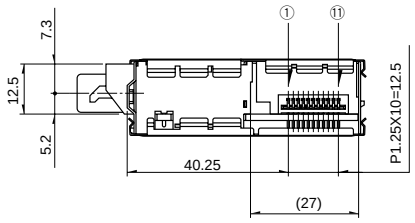
■主な仕様　Typical Specifications

Items			Specifications
Receiving frequency range	AM	(kHz)	530 to 1710
	FM	(MHz)	87.5 to 108
Input impedance (Ω)	AM		—
	FM		75
Receive sensitivity (dBμ)	AM@SN20dB		51
	FM@SN50dB		15
Stereo separation (dB)	FM		45
Output level (dBs)	AM		−7.5
	FM		2.5
Total harmonic distortion (%)	AM		1.2
	FM		0.25
Power consumption		(V/W)	9/500
Volume		(ml)	60

■外形図　Dimensions

Unit : mm





Terminal No.	Terminal name
①	GND
②	FM DET
③	VSM
④	Rch OUT
⑤	Vcc
⑥	Lch OUT
⑦	GND
⑧	DO
⑨	CL
⑩	DI
⑪	CE

■回路ブロックダイヤグラム　Circuit Block Diagram