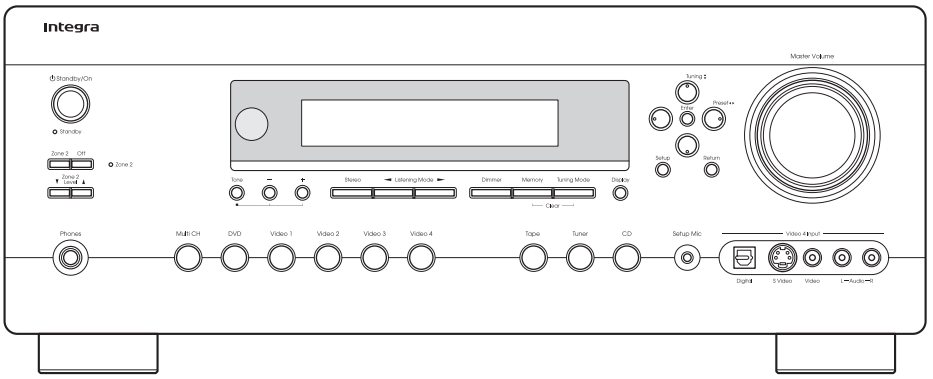
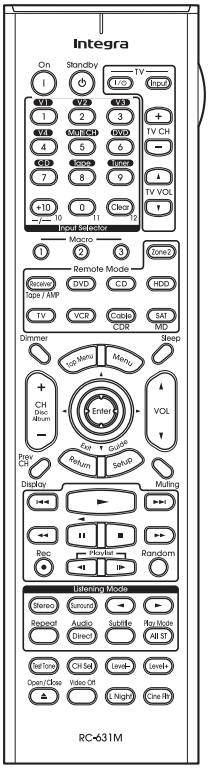
Ref. No. 3916
Nov., 2005

Integra SERVICE MANUAL

AV RECEIVER
MODEL DTR-5.6





RC-631M

Black model

BMDD	120V AC, 60Hz
BMPA	230V~240V AC, 50Hz

SAFETY-RELATED COMPONENT WARNING!!

THE MARK ⚠ FOUND ON SOME COMPONENT PARTS INDICATES THE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK.
WHEN REPLACING, BE SURE TO USE PARTS OF IDENTICAL DESIGNATION.
MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

SPECIFICATIONS

Amplifier Section

Power Output	
2 channels driven:	**90 W + 90 W (8Ω , 20 Hz~20 kHz, FTC)**
Dynamic Power	225 W + 225 W (3Ω , Front) 170 W + 170 W (4Ω , Front) 105 W + 105 W (8Ω , Front)
THD (Total Harmonic Distortion)	0.08% (Power Rated)
Damping Factor	60 (Front, 1 kHz, 8Ω)
Input Sensitivity and Impedance	200 mV/ 47 kΩ (LINE)
Output Level and Impedance	200 mV/ 470Ω (REC OUT)
Frequency Response	5 Hz~100 kHz/ +1 dB-3 dB (LINE)
Tone Control	±10 dB, 50 Hz (BASS) ±10 dB, 20 kHz (TREBLE)
Signal to Noise Ratio	106 dB (LINE, IHF-A) 80 dB (PHONO, IHF-A)
Speaker Impedance	6Ω~

Video Section

Input Sensitivity/Output Level and Impedance	1 Vp-p /75Ω (Component and S-Video Y) 0.7 Vp-p /75Ω (Component Pb/Cb,Pr/Cr) 0.28 Vp-p /75Ω (S-Video C) 1 Vp-p /75Ω (Composite)
Component Video Frequency Response	5 Hz ~ 50 MHz

Tuner Section

FM

Tuning Frequency Range	87.5 MHz~107.9 MHz
Usable Sensitivity	Stereo: 22.2 dBf (75Ω IHF) Mono: 15.2 dBf (75Ω IHF)
Signal to Noise Ratio	Stereo: 67 dB (IHF-A) Mono: 73 dB (IHF-A)
THD	Stereo: 0.5% (1 kHz) Mono:0.3% (1 kHz)
Frequency Response	30 Hz~15 kHz / ±1 dB
Stereo Separation	40 dB (1 kHz)

AM

Tuning Frequency Range	North American: 530 kHz~1710 kHz Australian: 522/530 kHz~1611/1710 kHz
Usable Sensitivity	300 µV/m
Signal to Noise Ratio	40 dB
THD	0.70%

General

Power Supply	North American: AC 120 V, 60 Hz Australian: AC 230-240 V, 50 Hz
Power Consumption	North American: 6.7 A Australian: 570 W
Standby Power Consumption	North American: 0.1 W Australian: 0.5 W
Dimensions (W × H × D)	435 × 173.5 × 428.5 mm 17-1/8" × 6-13/16" × 16-7/8"
Weight	11.9 kg 26.2 lbs.

Video Inputs

Component	IN1, IN2, IN3
S-Video	DVD, VIDEO1, VIDEO2, VIDEO3, VIDEO4
Composite	DVD, VIDEO1, VIDEO2, VIDEO3, VIDEO4

Video Outputs

Component	OUT
S-Video	MONITOR OUT, VIDEO1, VIDEO2
Composite	MONITOR OUT, VIDEO1, VIDEO2

Audio Inputs

Digital Inputs	Optical: 5 (1 on Front Panel) Coaxial: 2
Analog Inputs	DVD (MULTICHANNEL), VIDEO1, VIDEO2, VIDEO3, VIDEO4, TAPE, CD, PHONO
Multichannel Input	7.1 ch (DVD)

Audio Outputs

Digital Output	Optical: 1
Analog Outputs	TAPE, VIDEO1, VIDEO2, ZONE2 L/R/SUBWOOFER
Multichannel Pre Outputs	7.1 ch
Speaker Outputs	L, R, C, SL, SR, SBL, SBR ZONE2 (L, R)
Phones	1
RS232	1
IR Input/Output	2/1
12 V Trigger Out	A, B, C

Specifications and features are subject to change without notice.

SERVICE PROCEDURES

1. Replacing the fuses

 This symbol located near the fuses indicates that the fuse used is fast operating type. For continued protection against fire hazard, replace with same type fuse. For fuse rating refer to the marking adjacent to the symbol.

 Ce symbole indique que le fusible utlise est a rapide. Pour une protection permanente, n'untiliser que fusibles de meme type. Ce darnier est la qu le present symbol est appse.

CIRCUIT NO.	PART NO.	DESCRIPTION
F6901,F6902	252301GR	12A-TUL-250V,Fuse
F901	252078GR	5A-SE-EAK,Fuse <A>
	252330GR	10A-UL/T-233,Fuse <D>
F903	252075GR	2.5A-SE-EAK,Fuse <A>
	252326GR	5A-UL/T-233,Fuse <D>
F931,F932	252073GR	1.6A-SE-EAK,Fuse
F951,F952	252257GR	4A-T/UL-ST2,Fuse

Note: <D>:120V model only
<A>: Australian model only

2. To initialize the unit

This device employs a microprocessor to perform various functions and operations. If interference generated by an external power supply, radio wave, or other electrical source results in accident which causes the specified operations and functions to operate abnormally.
To perform a result, please follow the procedure below.
1.Press and hold down the VIDEO-1 button, then press the STANDBY button.
2.After "Clear" is displayed, the preset memory and each mode stored in the memory, such as surround, are initialized and will return to the factory setting.

3. Safety-check out

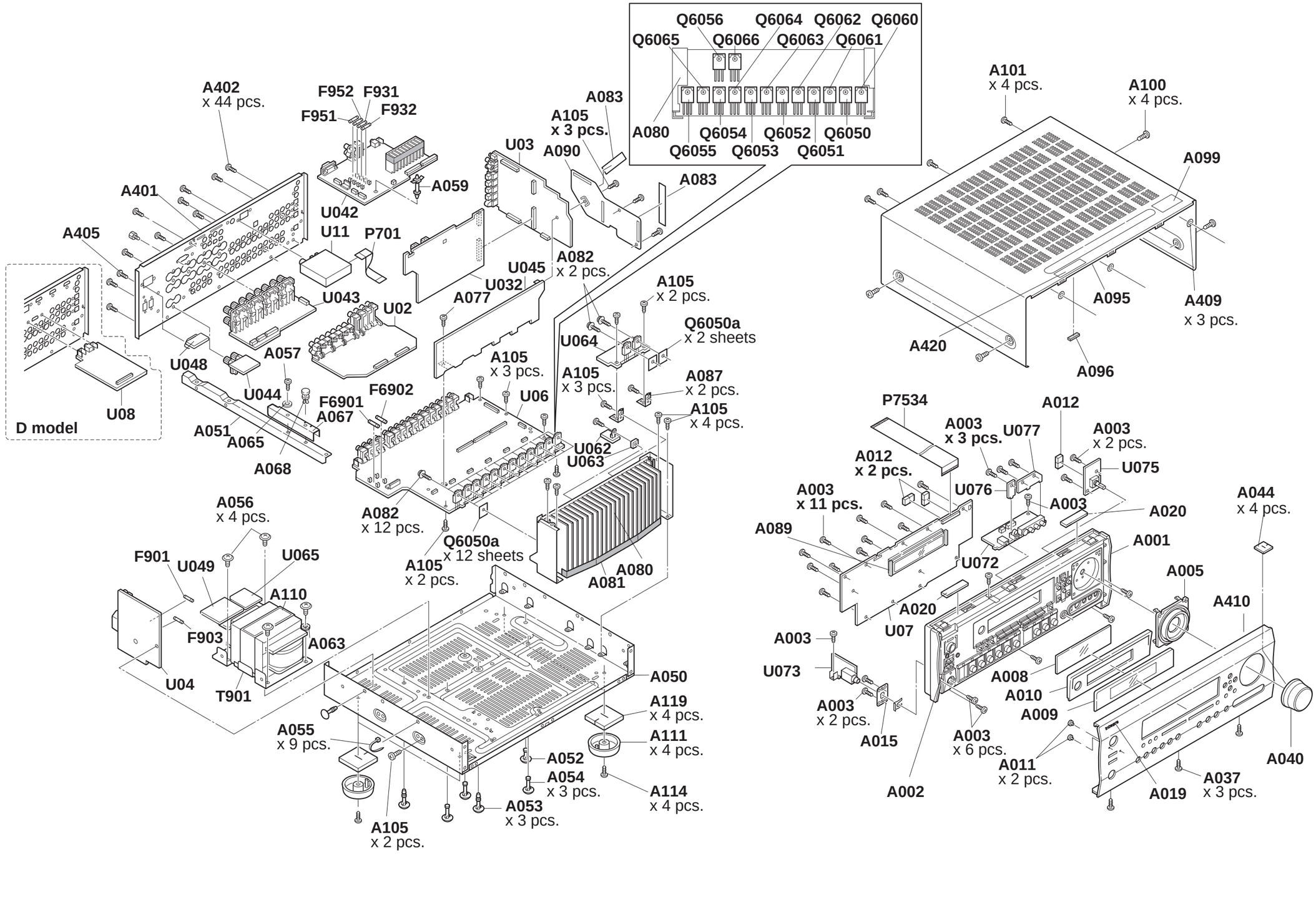
(U.S.A. model only)
After correcting the original service problem, perform the following safety check before releasing the set to the customer.
Leakage Current Check
Measure leakage current to a known earth ground(water pipe, conduit, etc.) by connecting a leakage current tester between the earth ground and exposed metal parts of the appliance (input/output terminals, screwheads,metal overlays, etc.).

4. Changing the AM band step

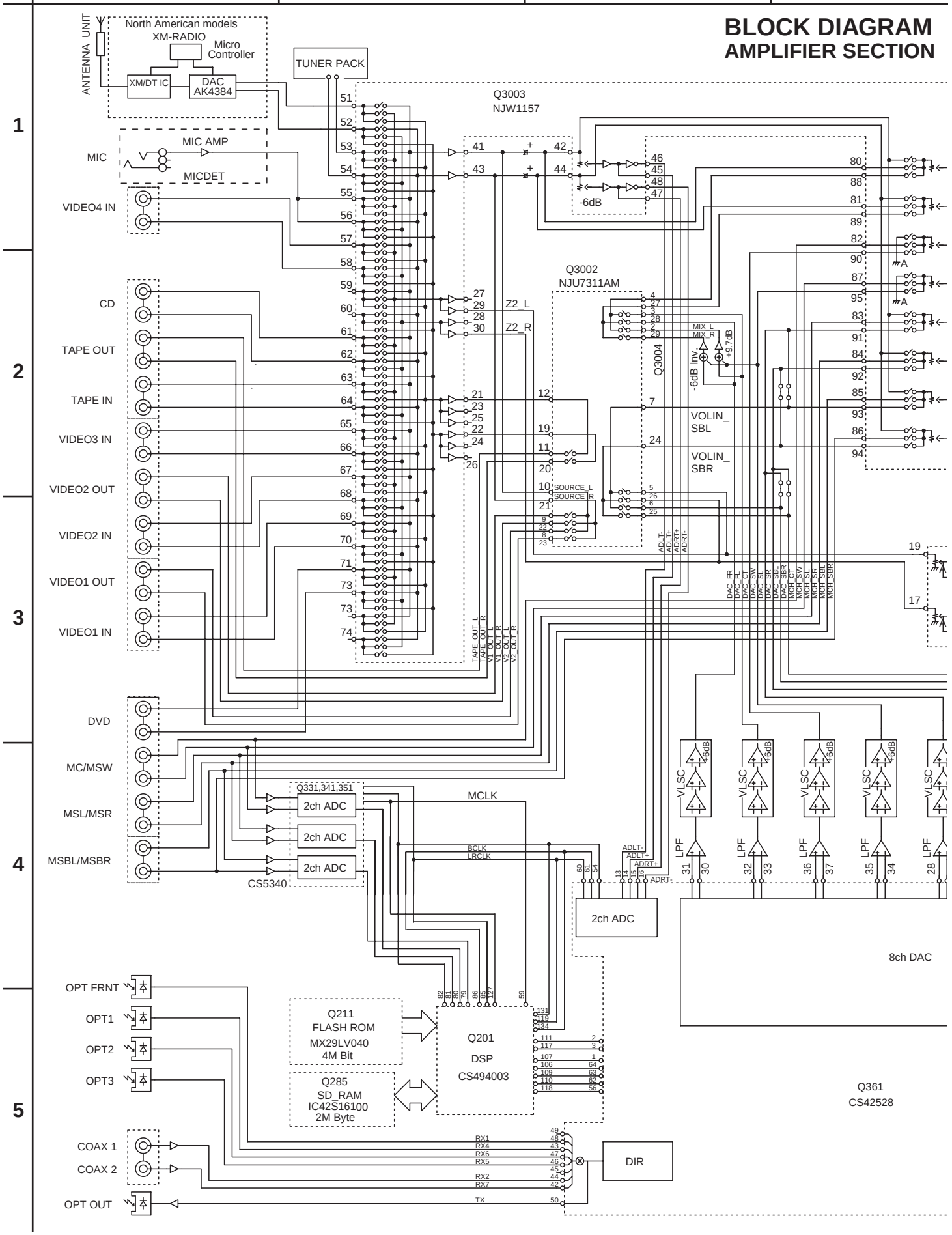
With the exception of the worldwide models, a tuning step selector switch is not provided. When you change the band step, change the parts as shown below.

	To 10kHz	To 9kHz
R714	Open	10 k

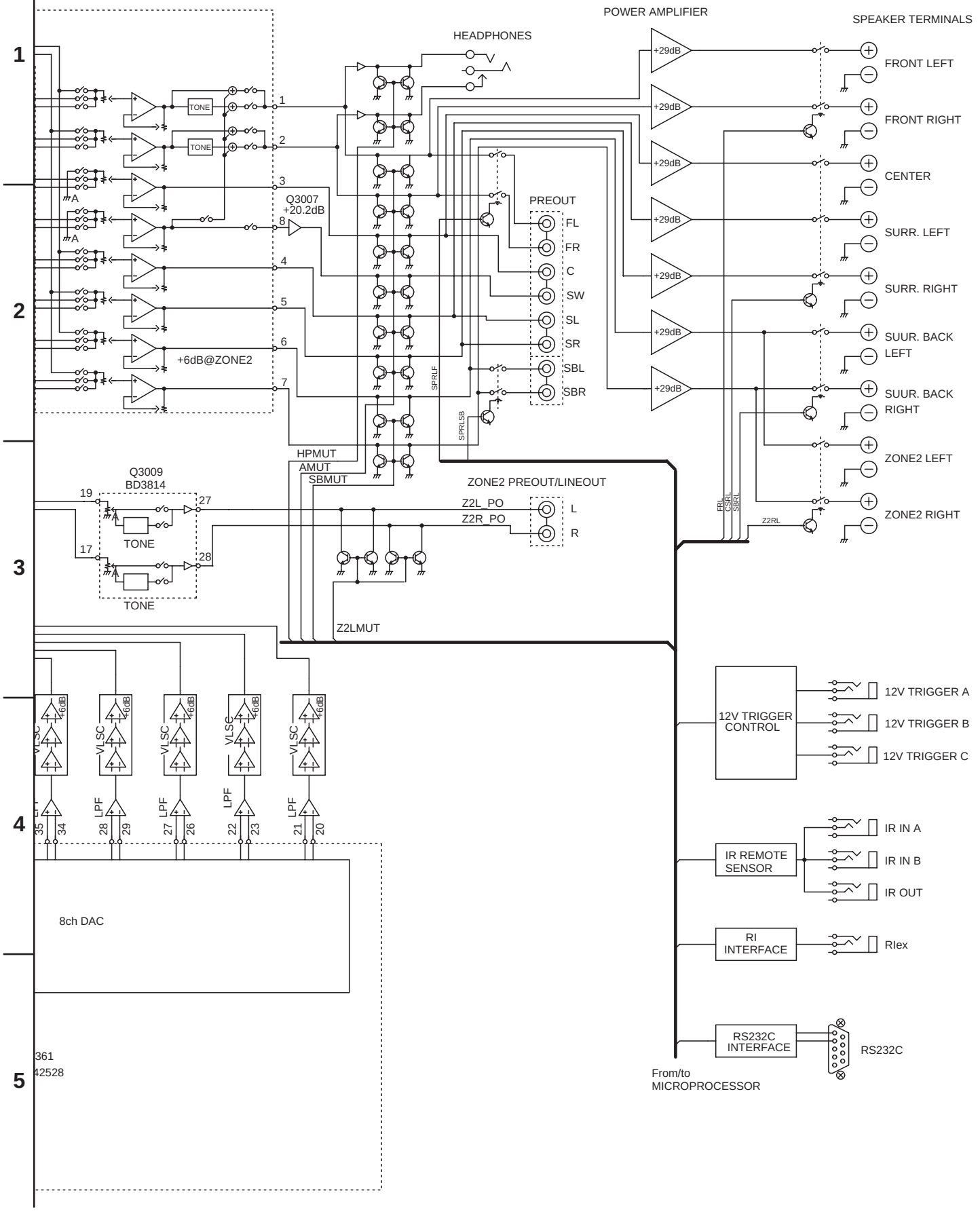
EXPLODED VIEW



BLOCK DIAGRAM
AMPLIFIER SECTION



BLOCK DIAGRAM
AMPLIFIER SECTION



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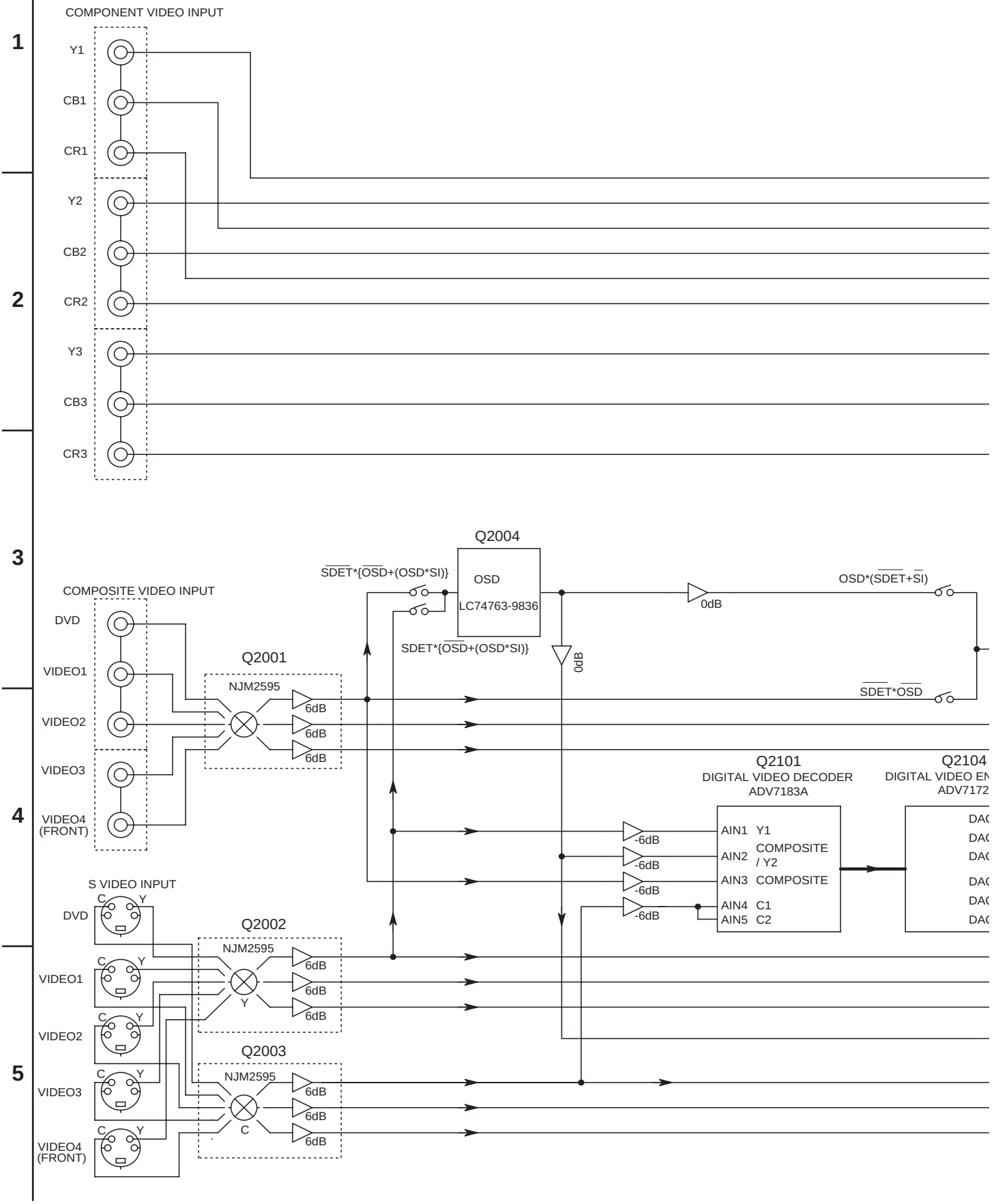

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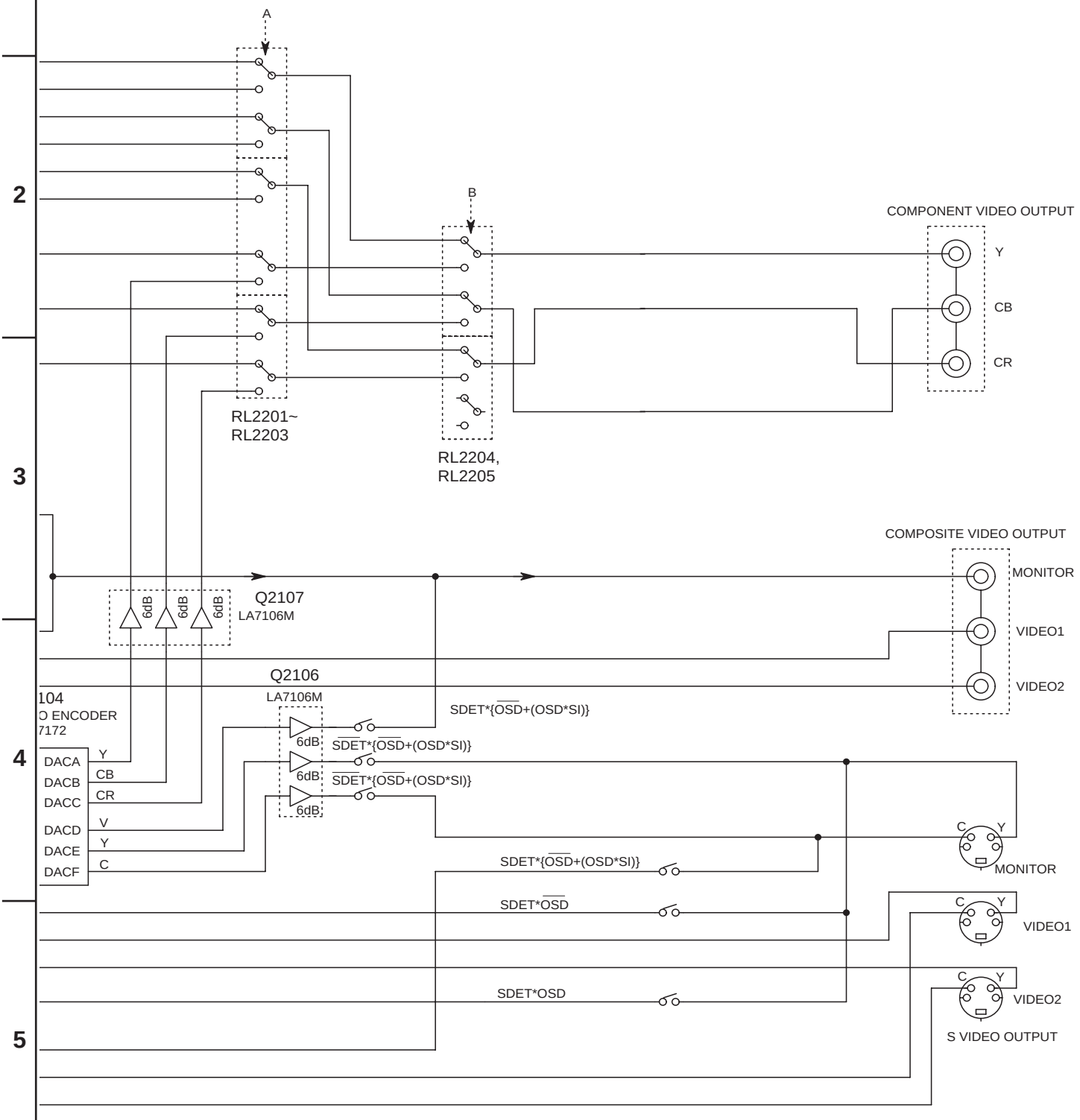


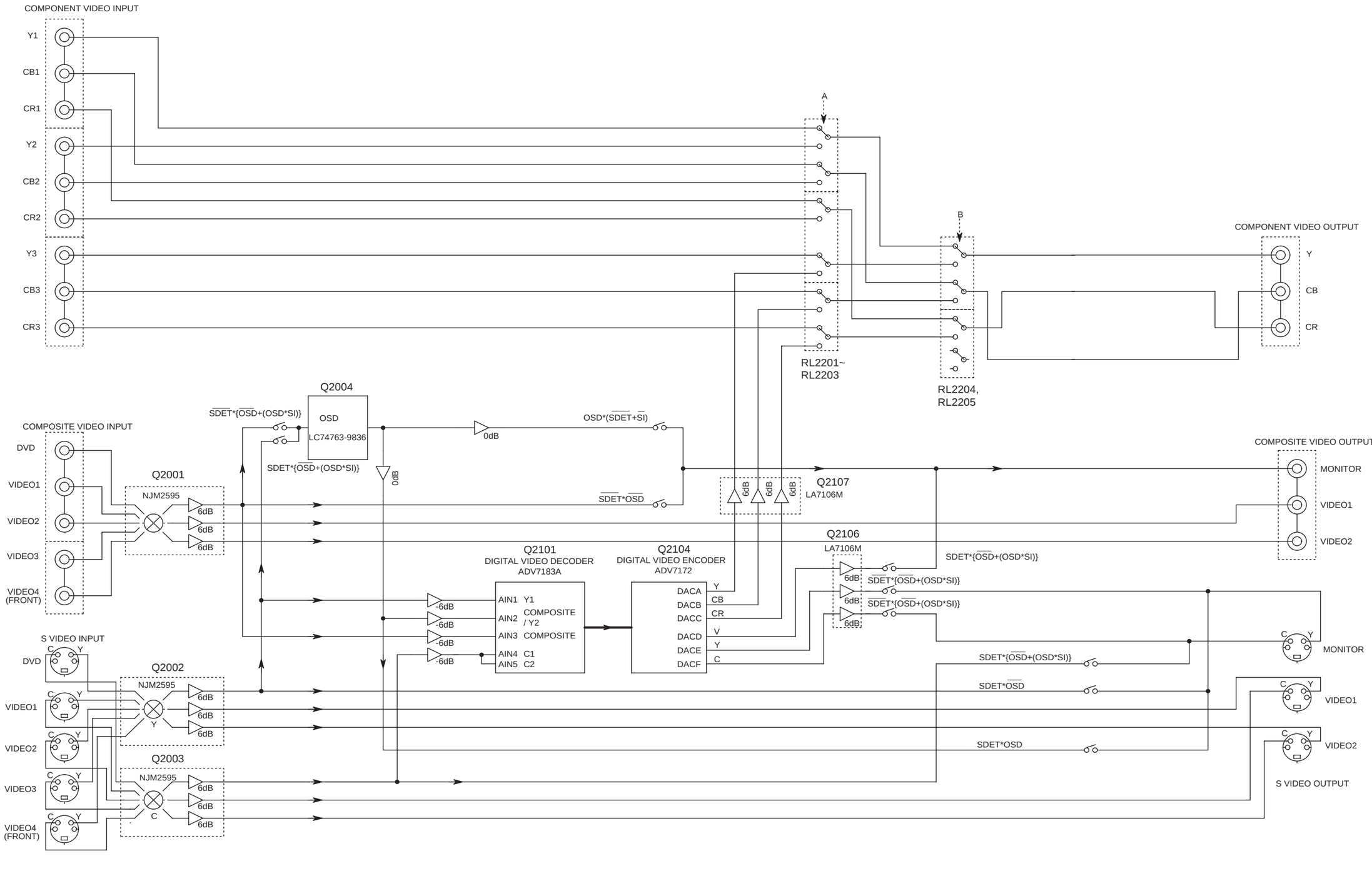
BLOCK DIAGRAM
AMPLIFIER SECTION

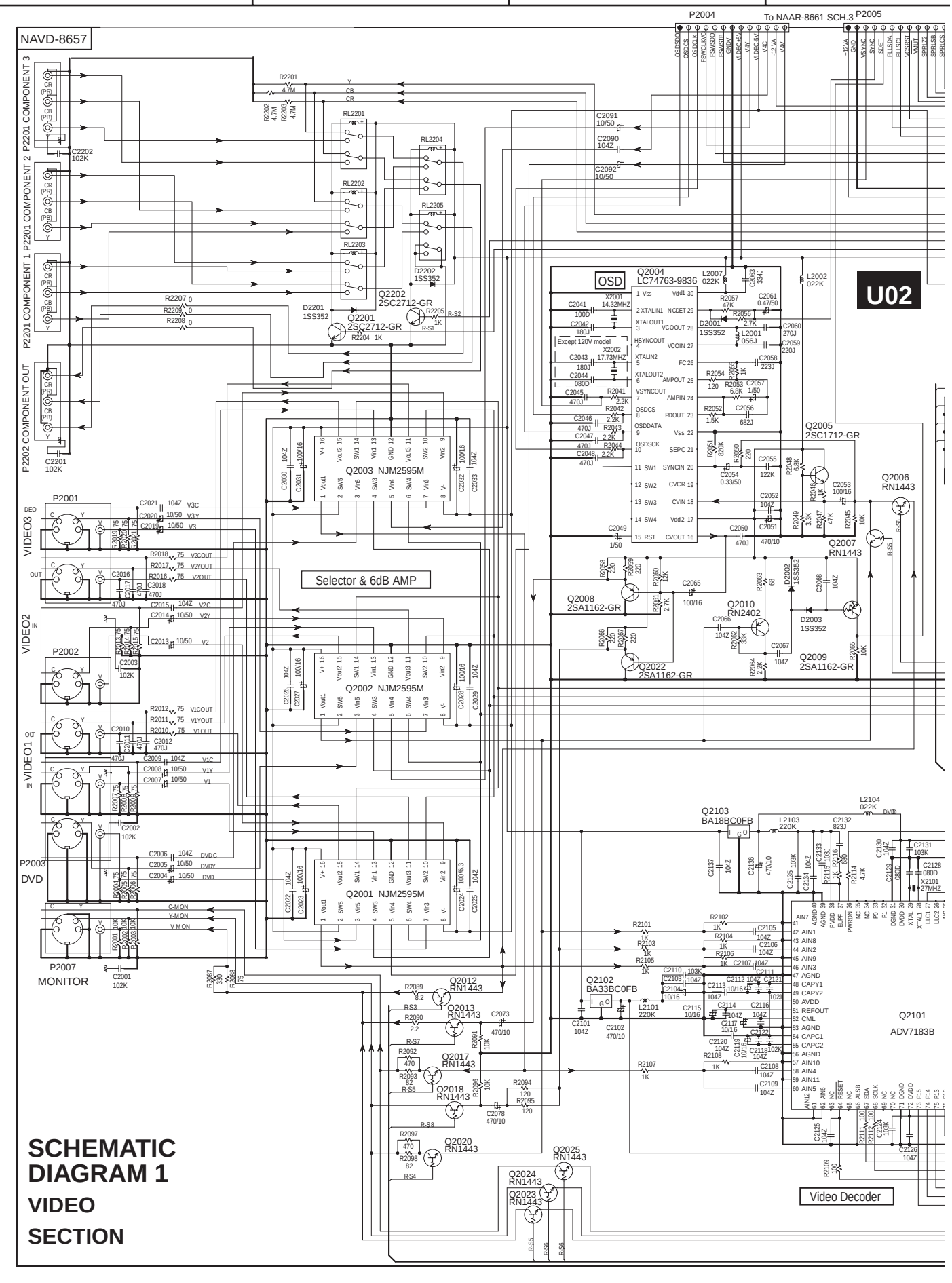
A B C D E F G H

1 2 3 4 5

ANTENNA UNIT
North American models
XM-RADIO
Micro Controller
XM/DT IC
DAC AK4384
TUNER PACK
MIC
MIC AMP
MICDET
VIDEO4 IN
CD
TAPE OUT
TAPE IN
VIDEO3 IN
VIDEO2 OUT
VIDEO2 IN
VIDEO1 OUT
VIDEO1 IN
DVD
MC/MSW
MSL/MSR
MSBL/MSBR
CS5340
Q331,341,351
2ch ADC
Q3003
NJW1157
Q3002
NJU7311AM
Q3004
-6dB
-6dB Inv.
+9.7dB
VOLIN_SBL
VOLIN_SBR
Z2_L
Z2_R
SOURCE_L
SOURCE_R
MCLK
BCLK
LRCLK
TONE
+6dB@ZONE2
Q3007
+20.2dB
HEADPHONES
POWER AMPLIFIER
+29dB
SPEAKER TERMINALS
FRONT LEFT
FRONT RIGHT
CENTER
SURR. LEFT
SURR. RIGHT
SUUR. BACK LEFT
SUUR. BACK RIGHT
ZONE2 LEFT
ZONE2 RIGHT
PREOUT
FL
FR
C
SW
SL
SR
SBL
SBR
SPRLF
SPRLSB
HPMUT
AMUT
SBMUT
ZONE2 PREOUT/LINEOUT
Z2L_PO
Z2R_PO
L
R
Z2LMUT
Q3009
BD3814
TONE
VLSC
6dB
LPF
8ch DAC
Q361
CS42528
Q211
FLASH ROM
MX29LV040
4M Bit
Q285
SD_RAM
IC42S16100
2M Byte
Q201
DSP
CS494003
OPT FRNT
OPT1
OPT2
OPT3
COAX 1
COAX 2
OPT OUT
DIR
12V TRIGGER CONTROL
12V TRIGGER A
12V TRIGGER B
12V TRIGGER C
IR REMOTE SENSOR
IR IN A
IR IN B
IR OUT
RI INTERFACE
RIex
RS232C INTERFACE
RS232C
From/to MICROPROCESSOR

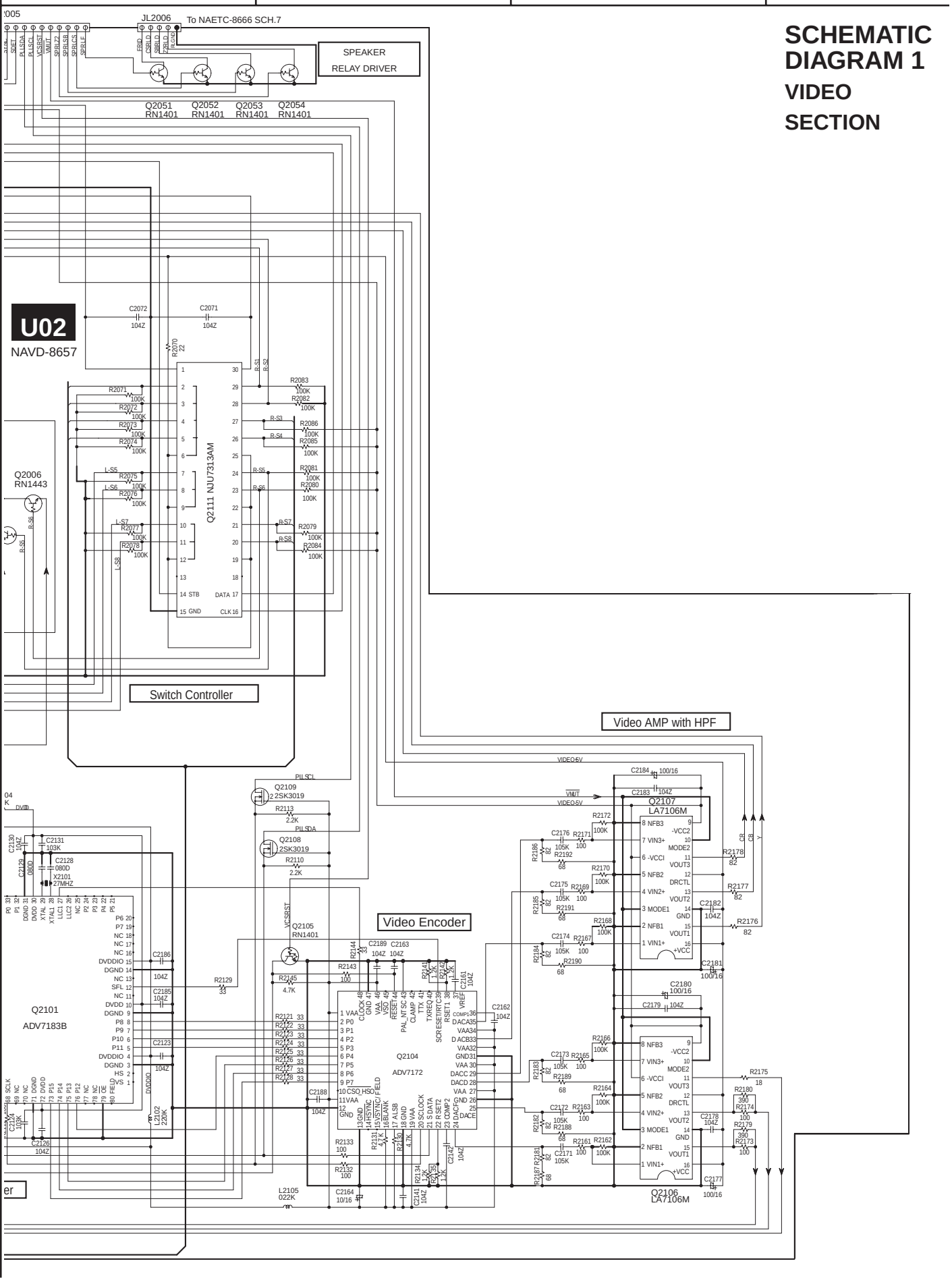
BLOCK DIAGRAM VIDEO SECTION



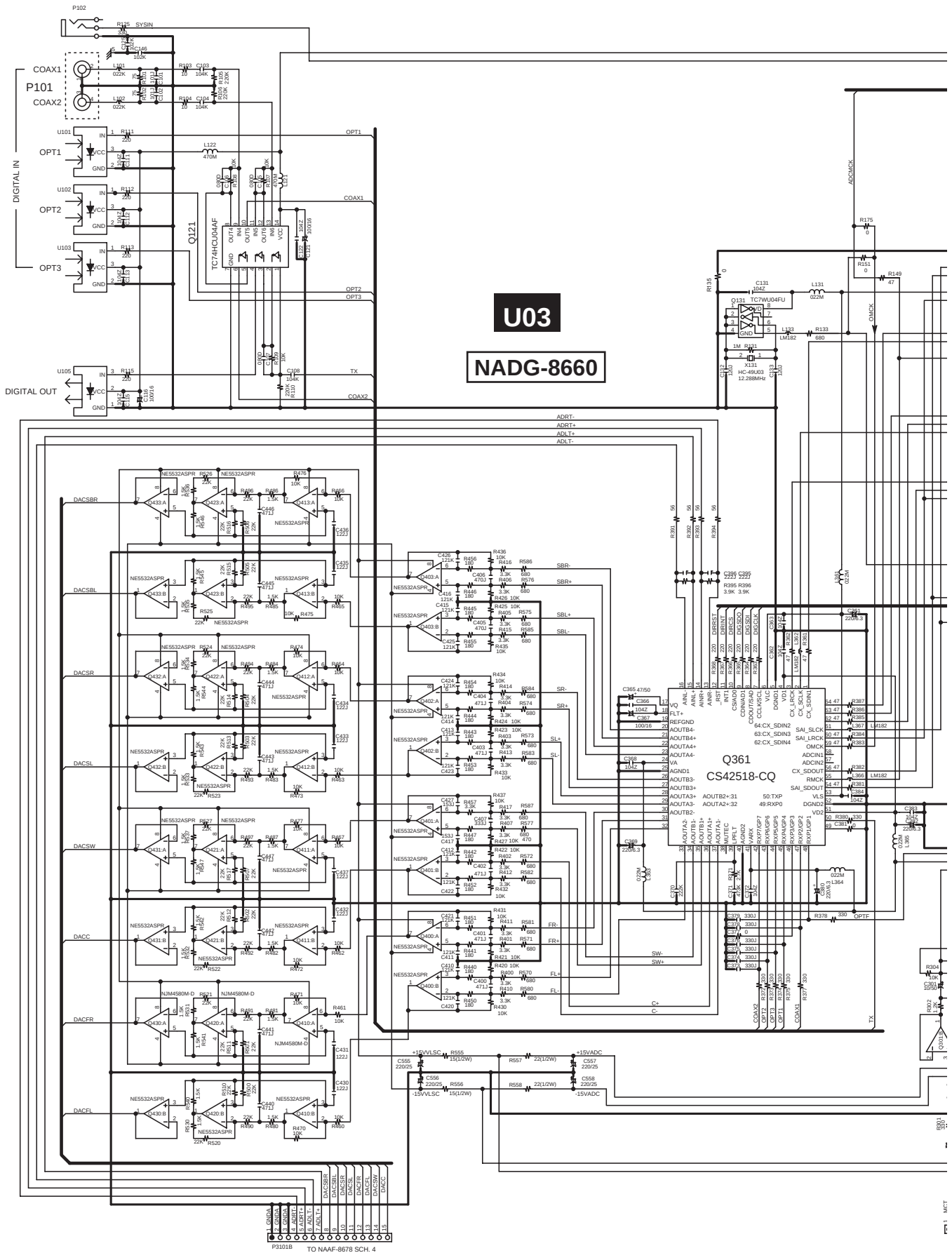

A
B
C
D
1
2
3
4
5
NAVD-8657
P2004
To NAAR-8661 SCH.3
P2005
U02
OSD
Q2004
LC74763-9836
Selector & 6dB AMP
Video Decoder
Q2101
ADV7183B
Q2003 NJM2595M
Q2002 NJM2595M
Q2001 NJM2595M
P2001
P2002
P2003
DVD
P2007
MONITOR
VIDEO3
VIDEO2
VIDEO1
P2201 COMPONENT 3
P2201 COMPONENT 2
P2201 COMPONENT 1
P2202 COMPONENT OUT
SCHEMATIC DIAGRAM 1
VIDEO
SECTION

SCHEMATIC DIAGRAM 1

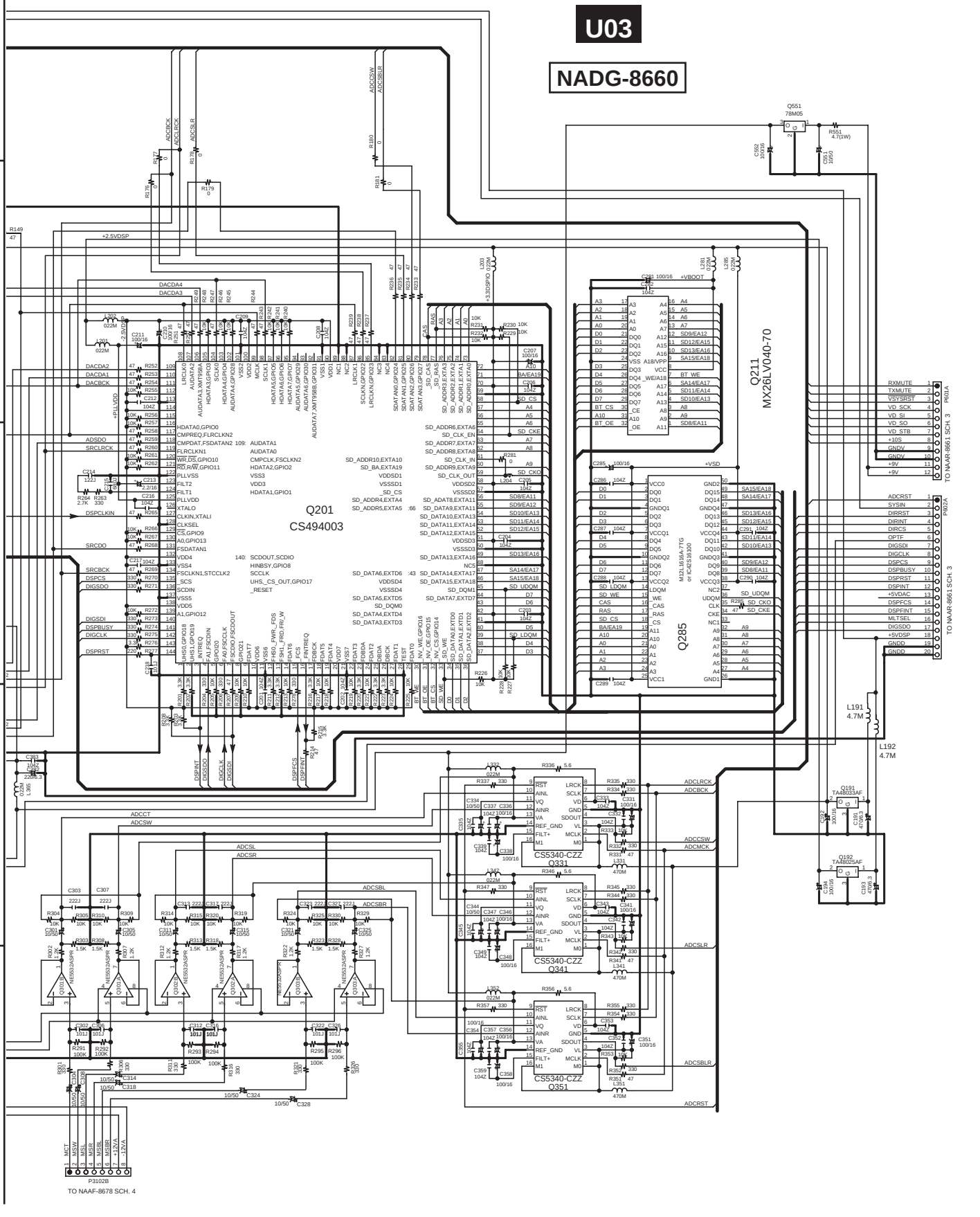
VIDEO SECTION



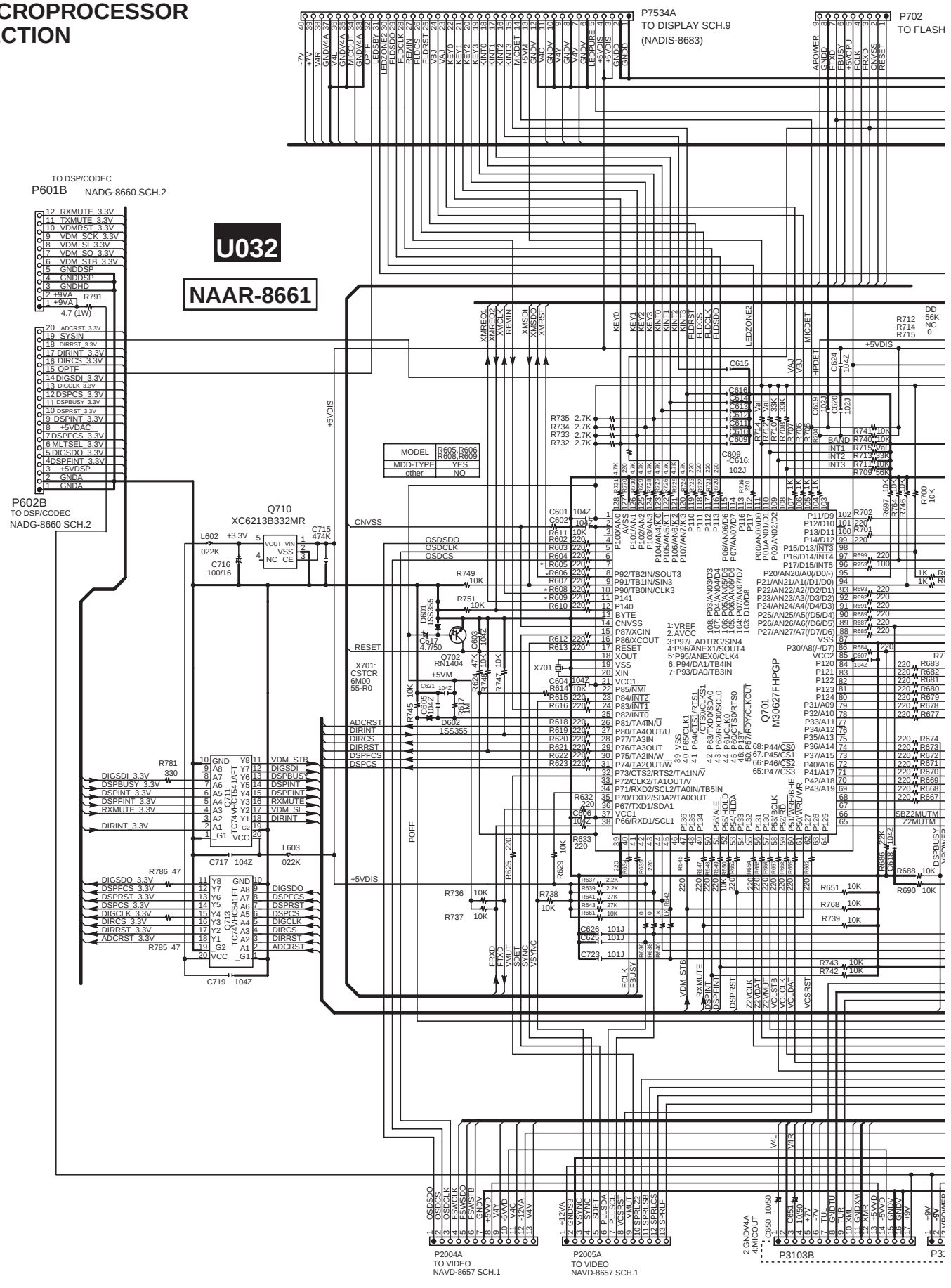
SCHEMATIC DIAGRAM 2 DSP SECTION

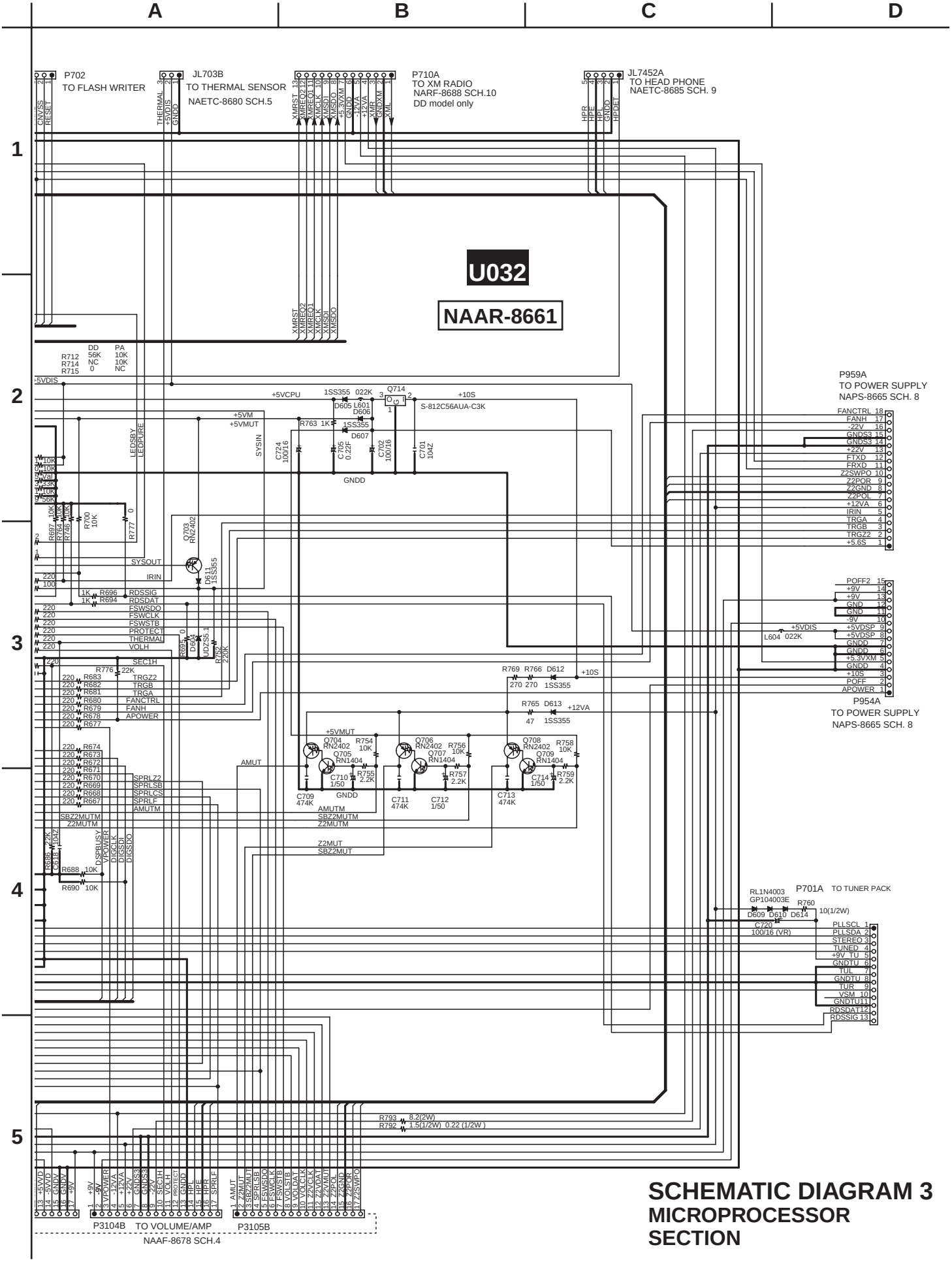


SCHEMATIC DIAGRAM 2 DSP SECTION



SCHEMATIC DIAGRAM 3
MICROPROCESSOR SECTION

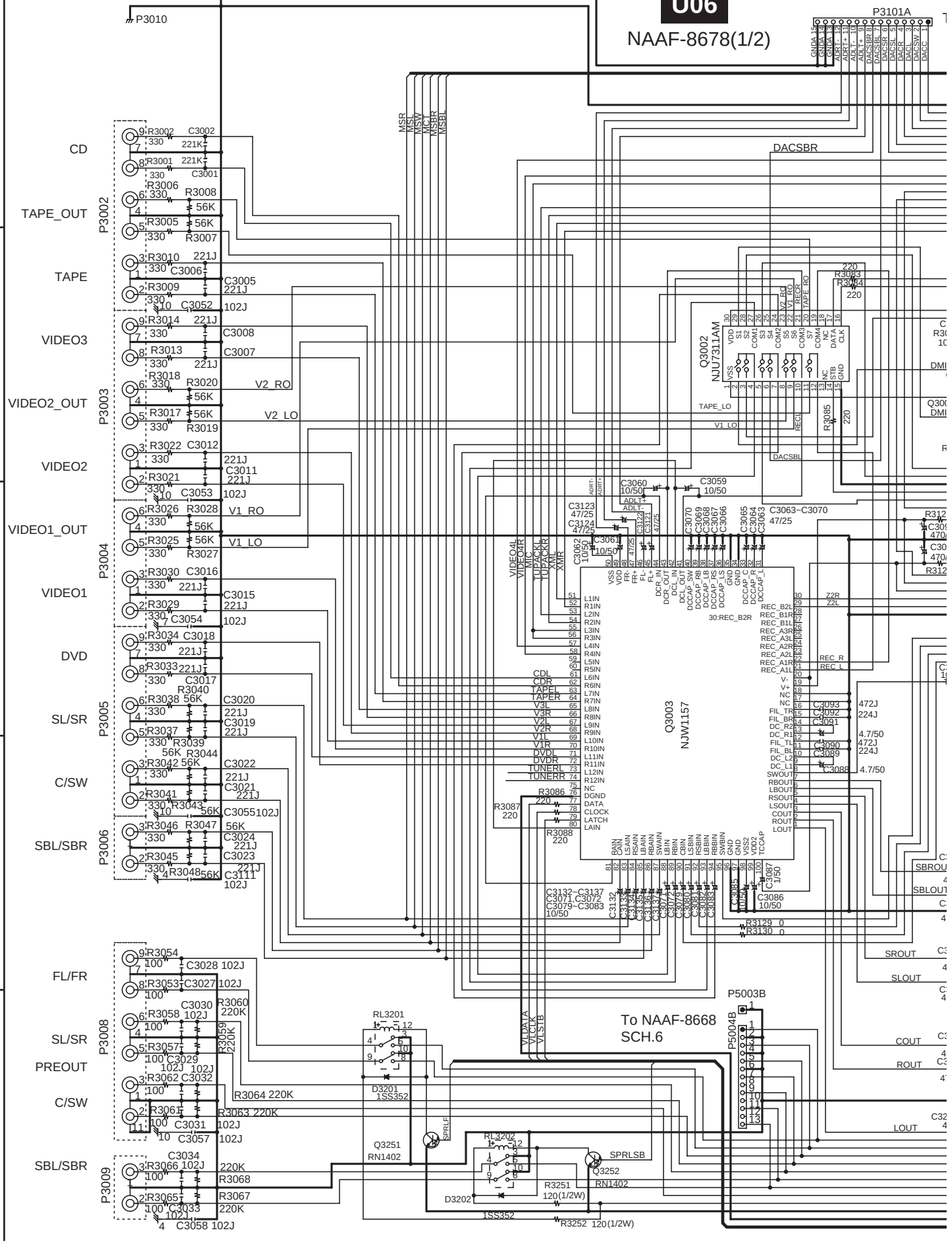



A
B
C
D
1
2
3
4
5
P702
TO FLASH WRITER
JL703B
TO THERMAL SENSOR
NAETC-8680 SCH.5
P710A
TO XM RADIO
NARF-8688 SCH.10
DD model only
JL7452A
TO HEAD PHONE
NAETC-8685 SCH. 9
U032
NAAR-8661
P959A
TO POWER SUPPLY
NAPS-8665 SCH. 8
P954A
TO POWER SUPPLY
NAPS-8665 SCH. 8
P701A TO TUNER PACK
P3104B TO VOLUME/AMP
NAAF-8678 SCH.4
P3105B
SCHEMATIC DIAGRAM 3
MICROPROCESSOR
SECTION

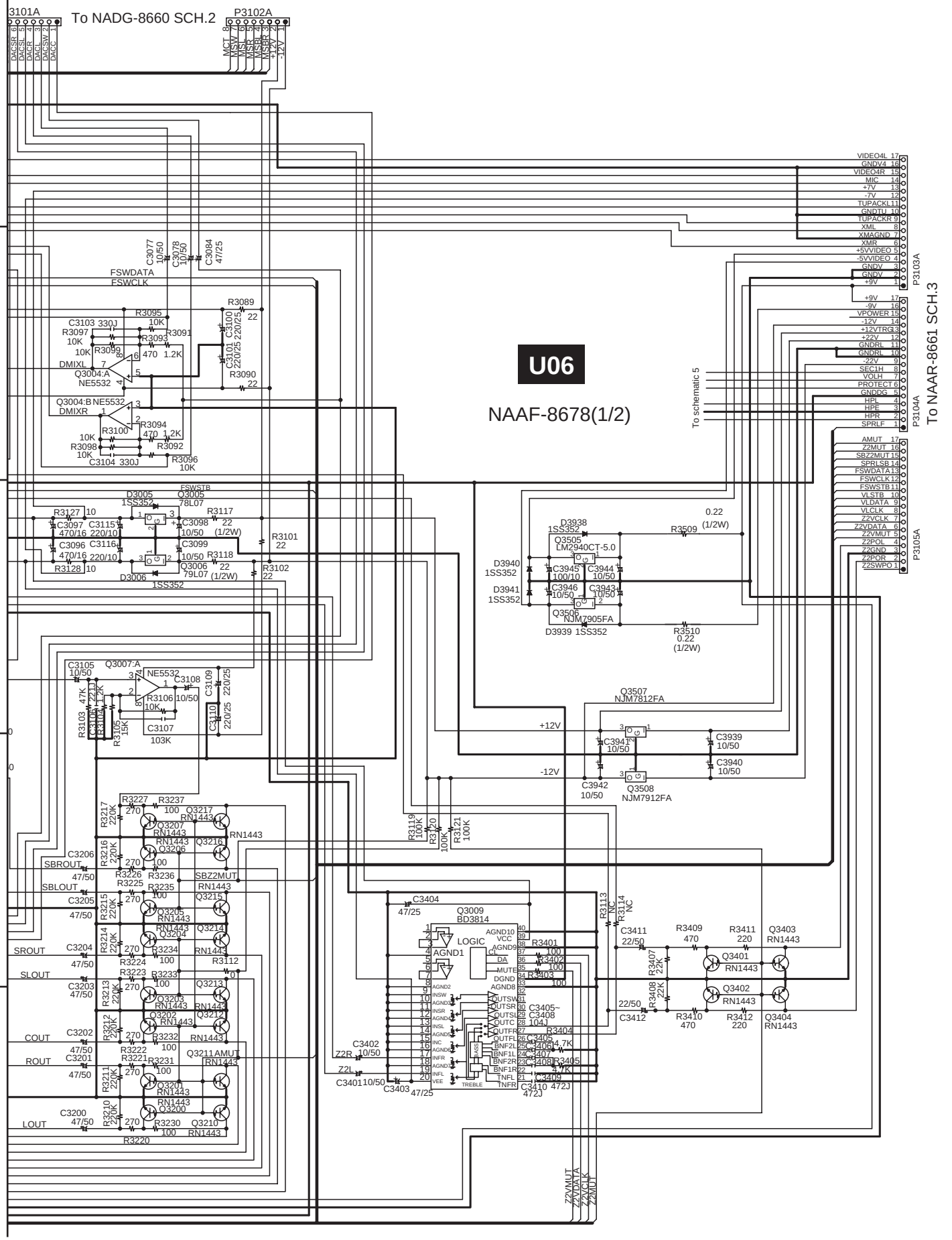
SCHEMATIC DIAGRAM 4 PREAMPLIFIER SECTION

U06

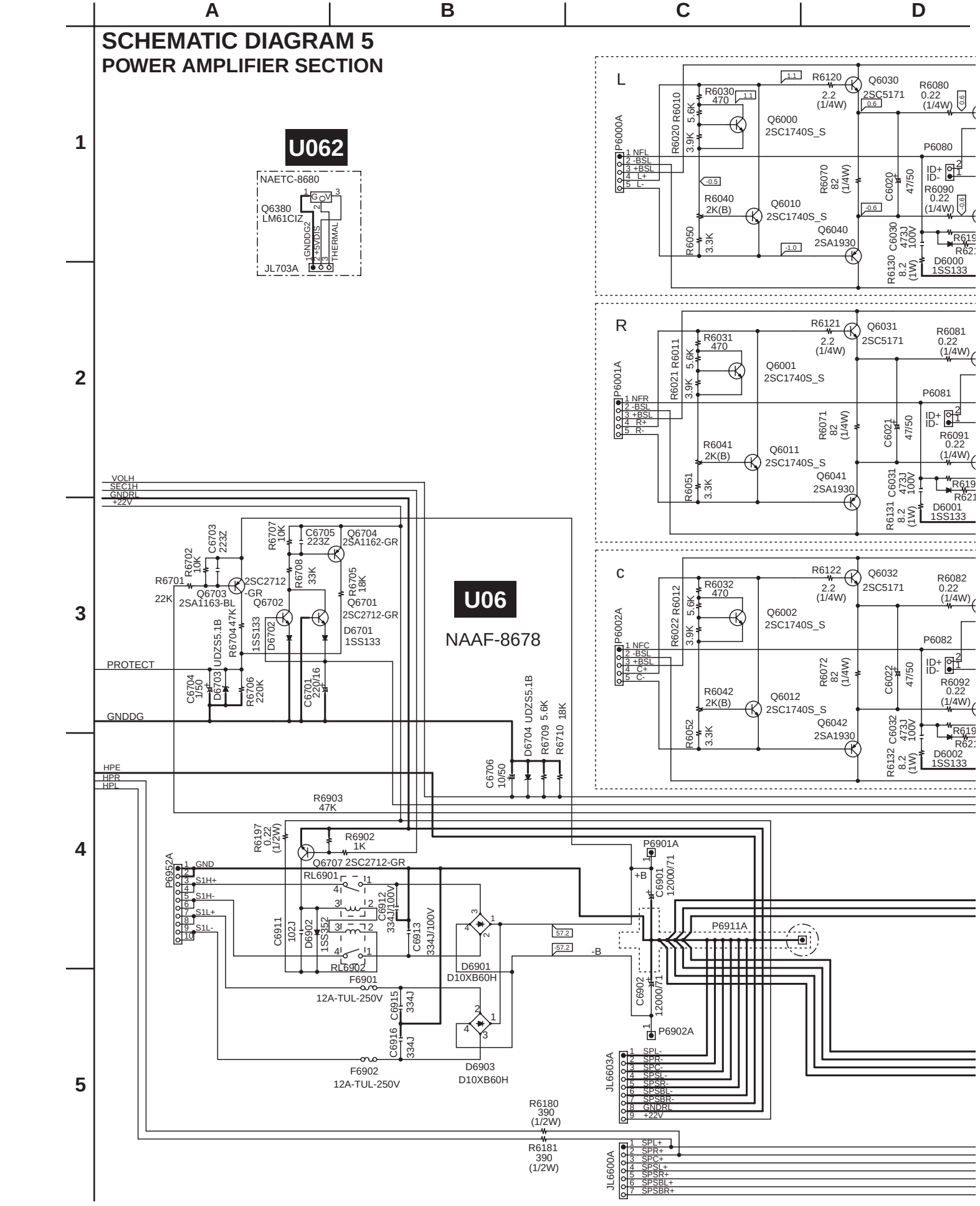
NAAF-8678(1/2)

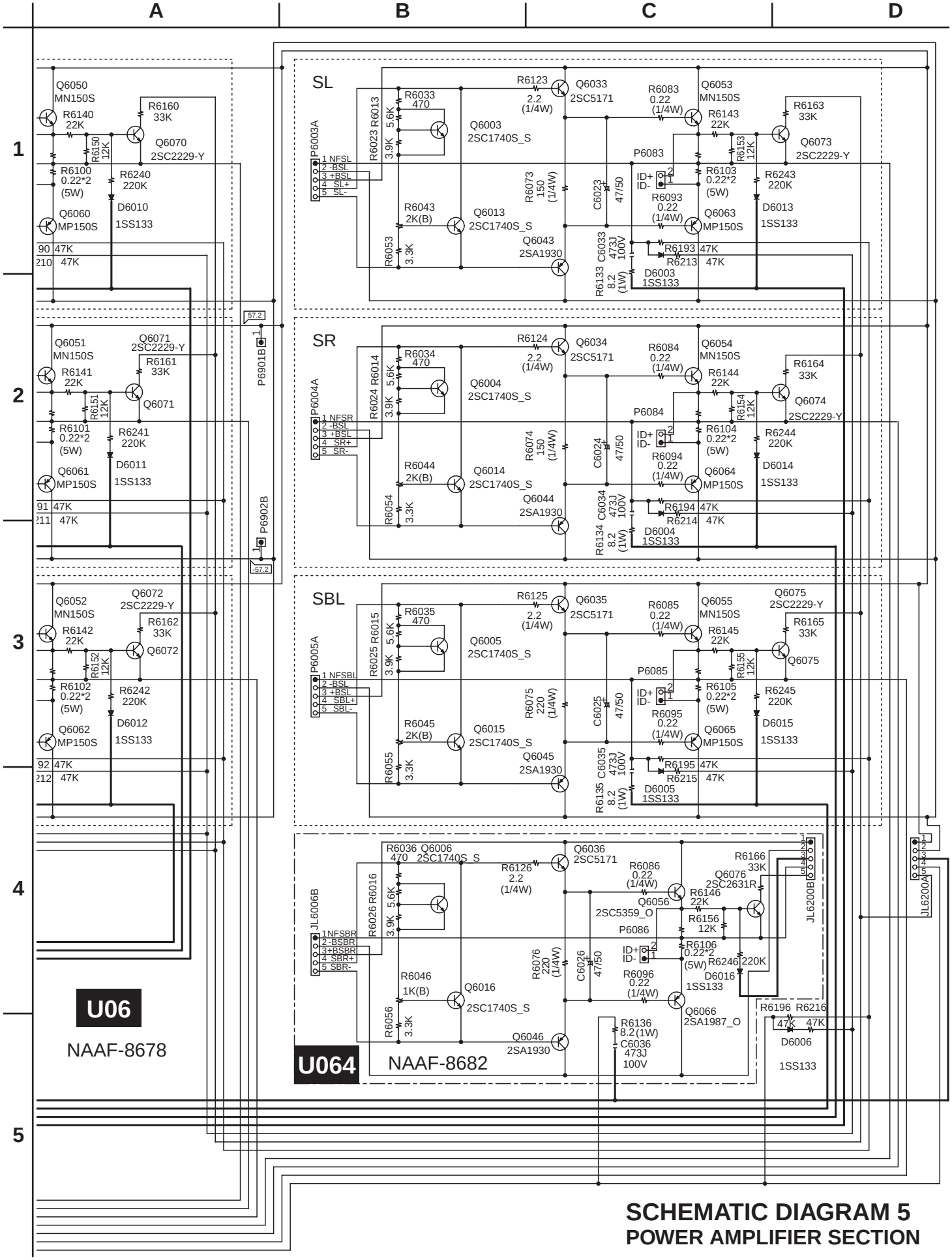


SCHEMATIC DIAGRAM 4 PREAMPLIFIER SECTION



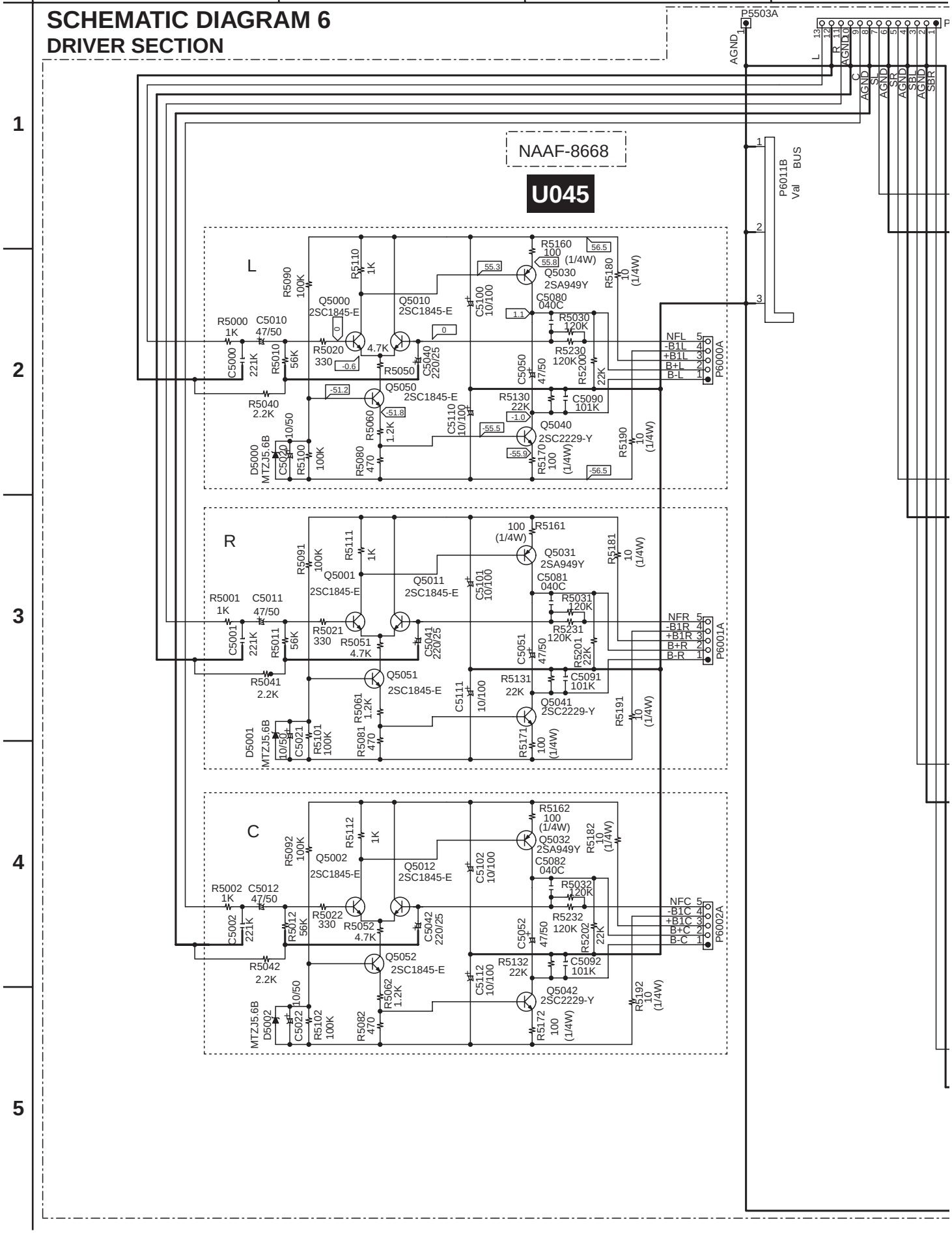
SCHEMATIC DIAGRAM 5
POWER AMPLIFIER SECTION



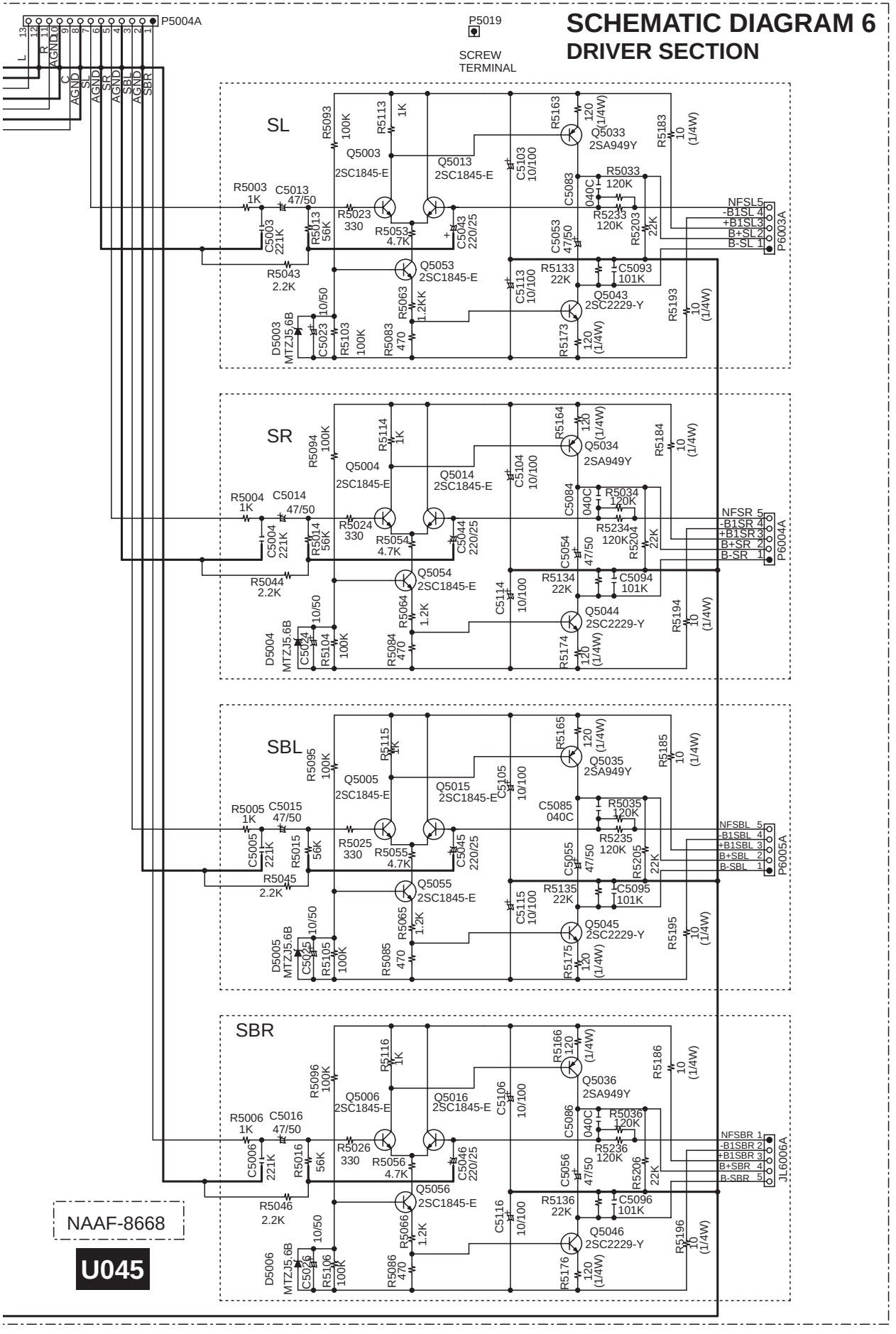


SCHEMATIC DIAGRAM 5
POWER AMPLIFIER SECTION

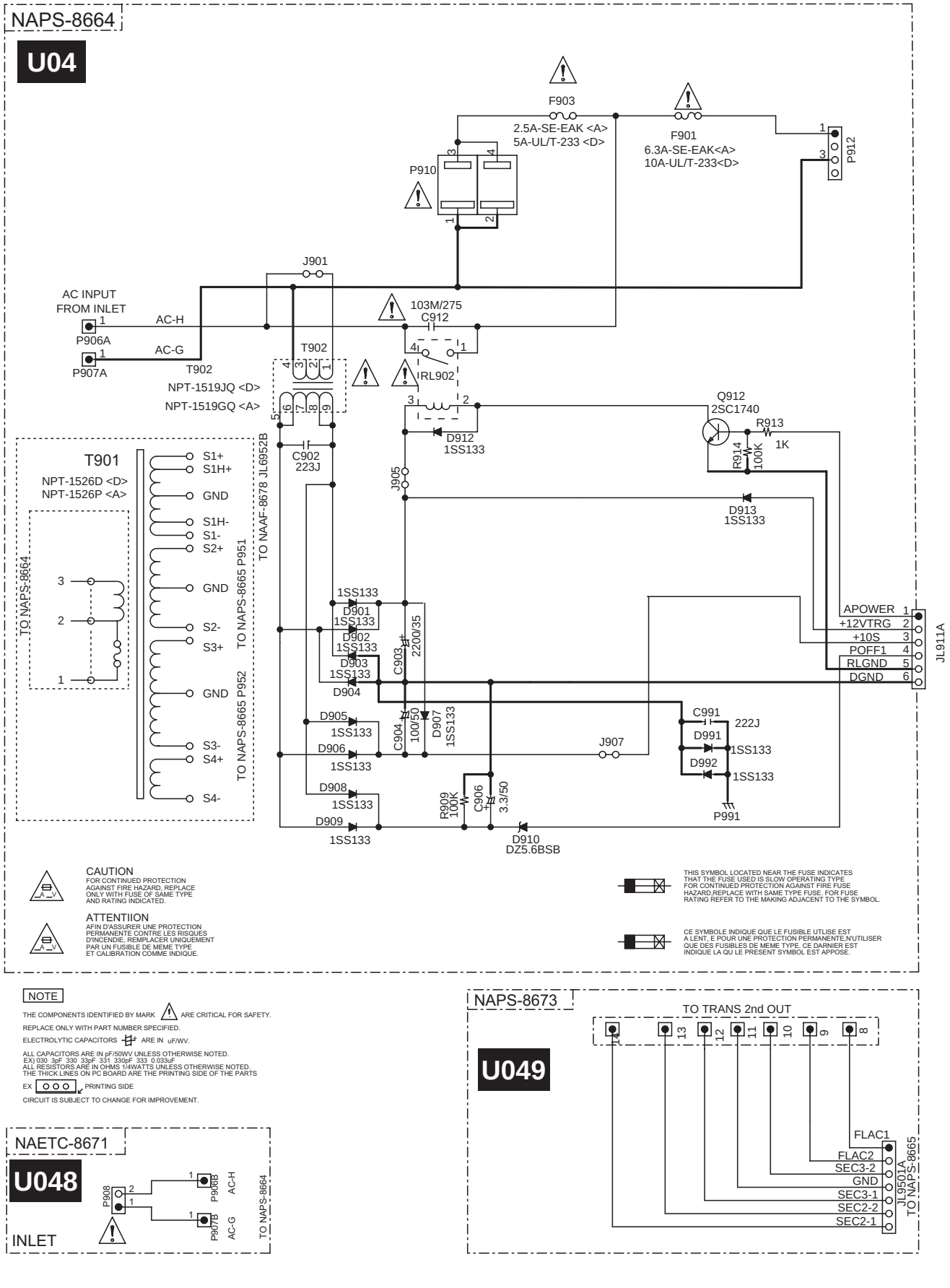
SCHEMATIC DIAGRAM 6
DRIVER SECTION



SCHEMATIC DIAGRAM 6
DRIVER SECTION



SCHEMATIC DIAGRAM 7
POWER SUPPLY SECTION

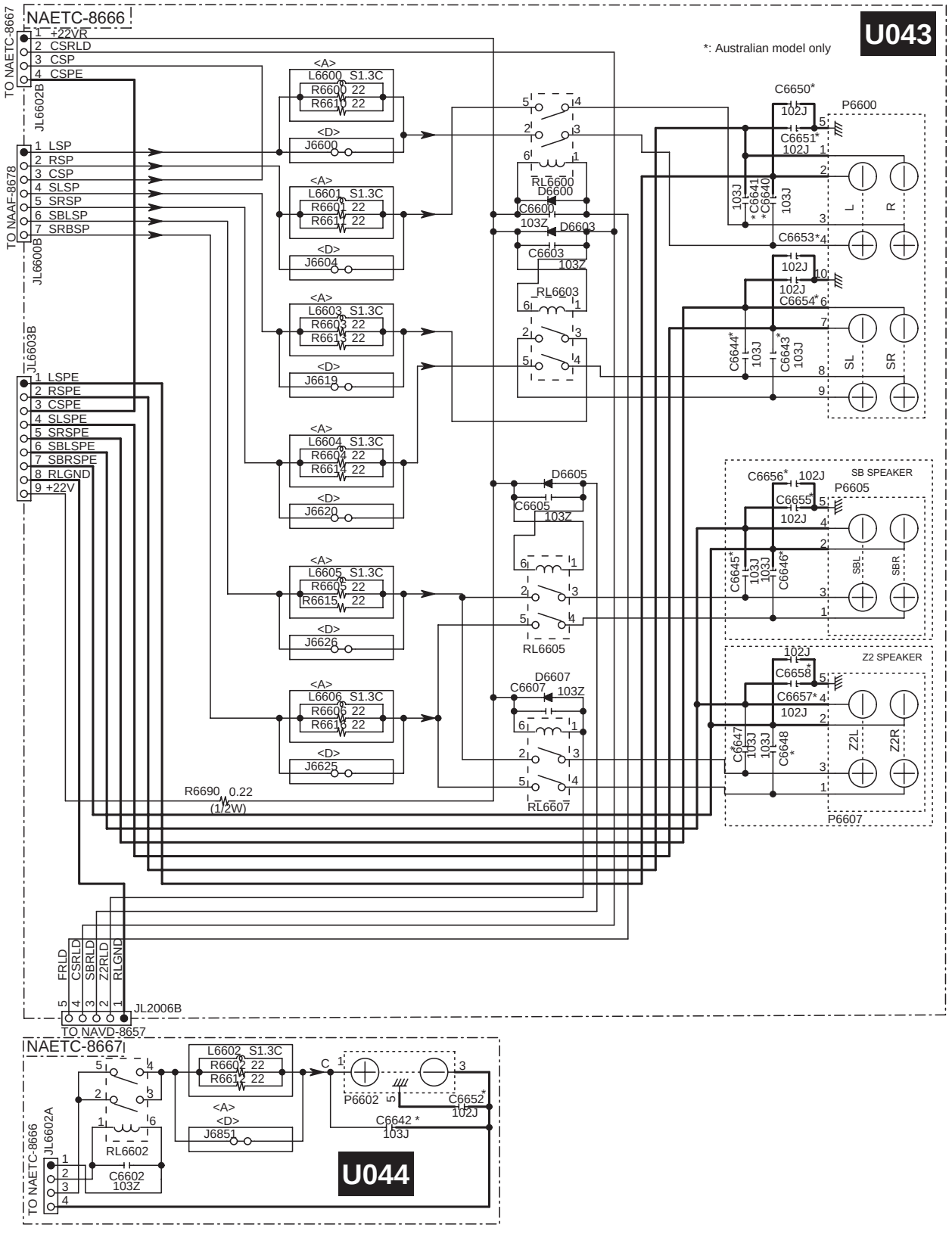


NOTE

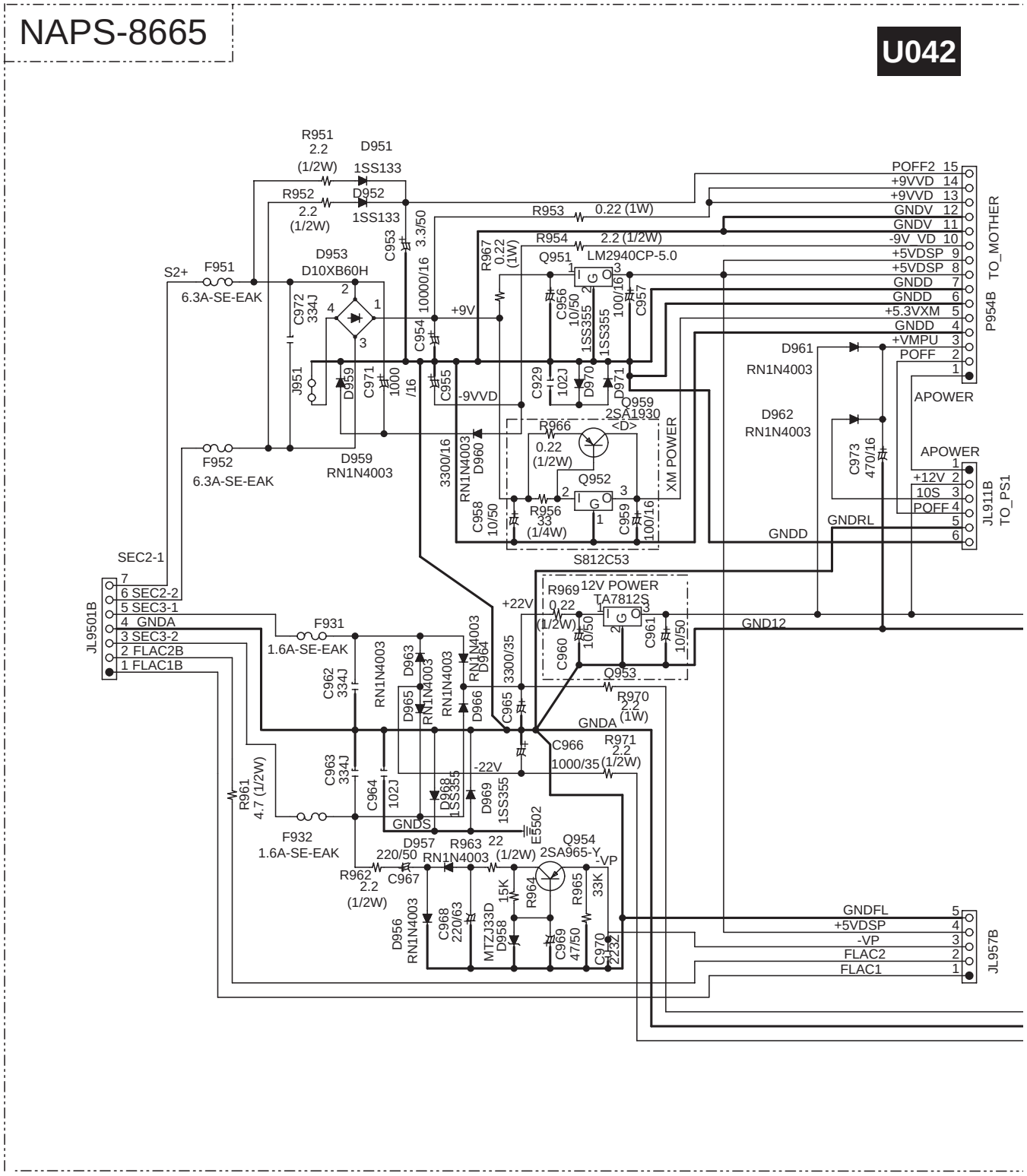
THE COMPONENTS IDENTIFIED BY MARK ⚠ ARE CRITICAL FOR SAFETY.
REPLACE ONLY WITH PART NUMBER SPECIFIED.
ELECTROLYTIC CAPACITORS ARE IN uF/WV.

ALL CAPACITORS ARE IN pF/50WV UNLESS OTHERWISE NOTED.
EX) 030 3pF 330 33pF 331 330pF 333 0.033uF
ALL RESISTORS ARE IN OHMS 1/4WATTS UNLESS OTHERWISE NOTED.
THE THICK LINES ON PC BOARD ARE THE PRINTING SIDE OF THE PARTS
EX PRINTING SIDE
CIRCUIT IS SUBJECT TO CHANGE FOR IMPROVEMENT.

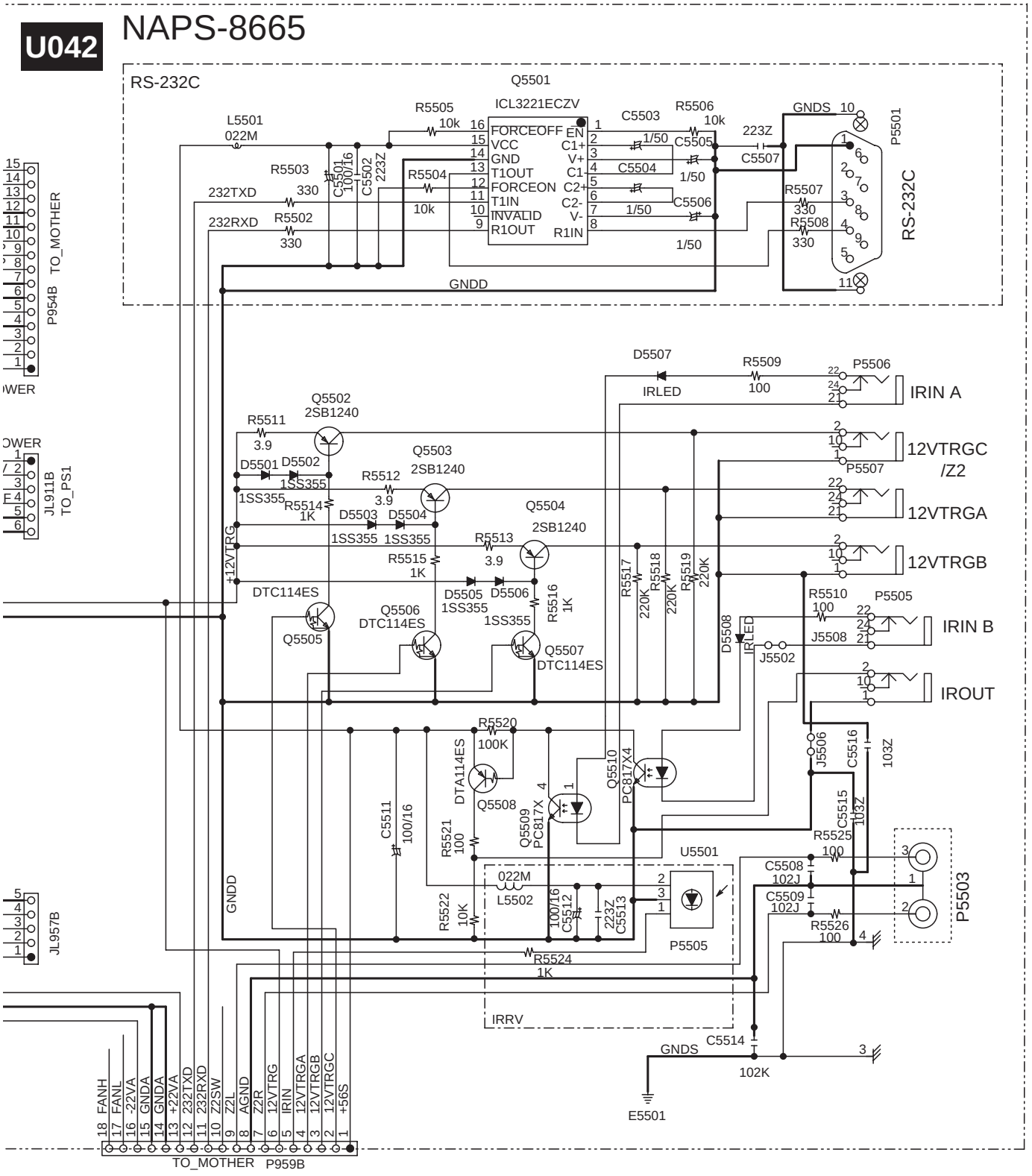
SCHEMATIC DIAGRAM 7
POWER SUPPLY SECTION



SCHEMATIC DIAGRAM 8
POWER SUPPLY SECTION



SCHEMATIC DIAGRAM 8
POWER SUPPLY SECTION



SCHEMATIC DIAGRAM 9
DISPLAY SECTION

NADIS-8683

U07

Q7501 HNA-16SM10T

Q7502 M66005

Q7503 2SC2712

D7501 UDZS8.2B

D7502 STBY

D7503 ZONE2

Q7506 RN1402

Q7509 RN2402

U7501

LEDSBY

LEDZONE2

VAJ

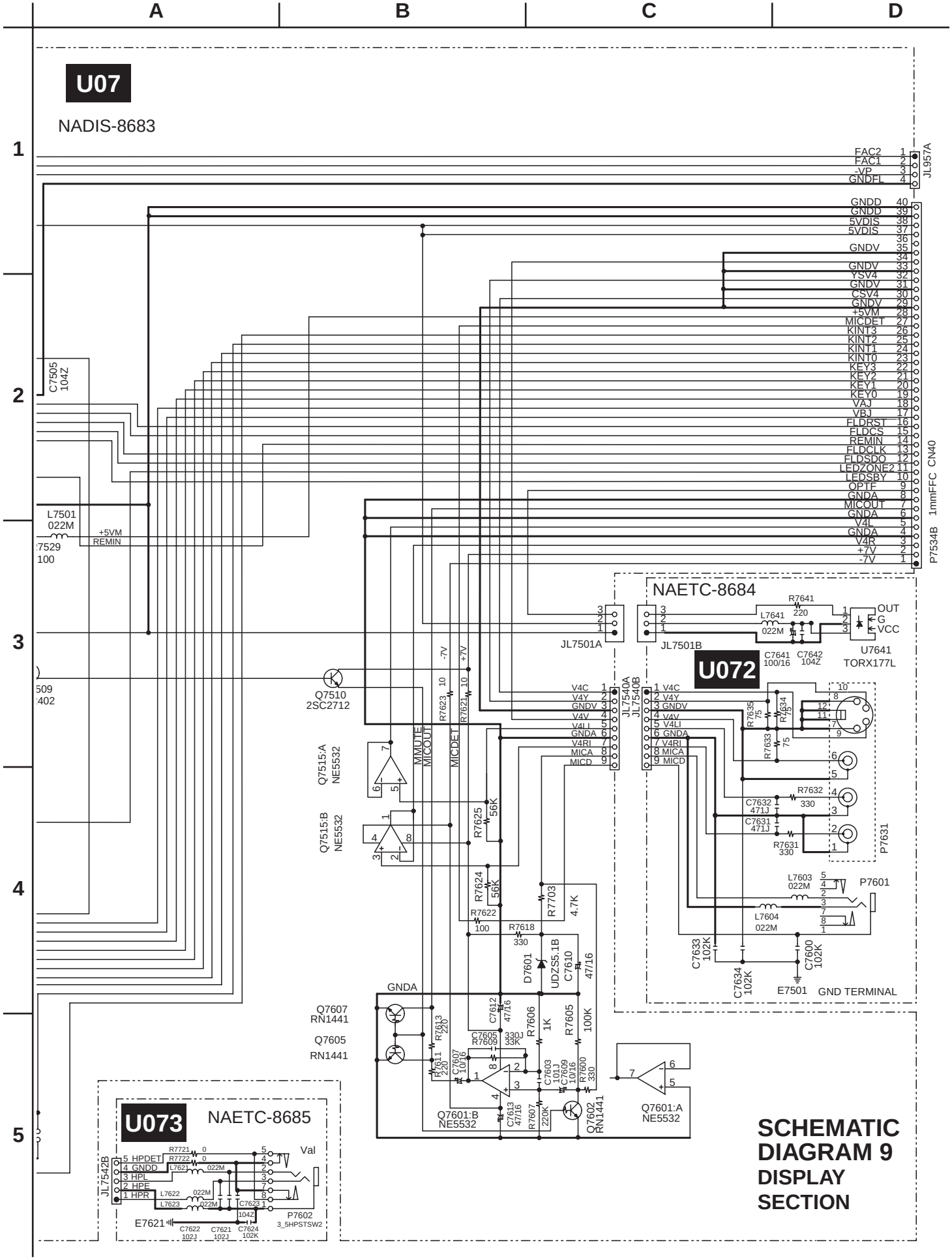
VBJ

JL7503A

JL7503B

S7591

U075 NAETC-8687

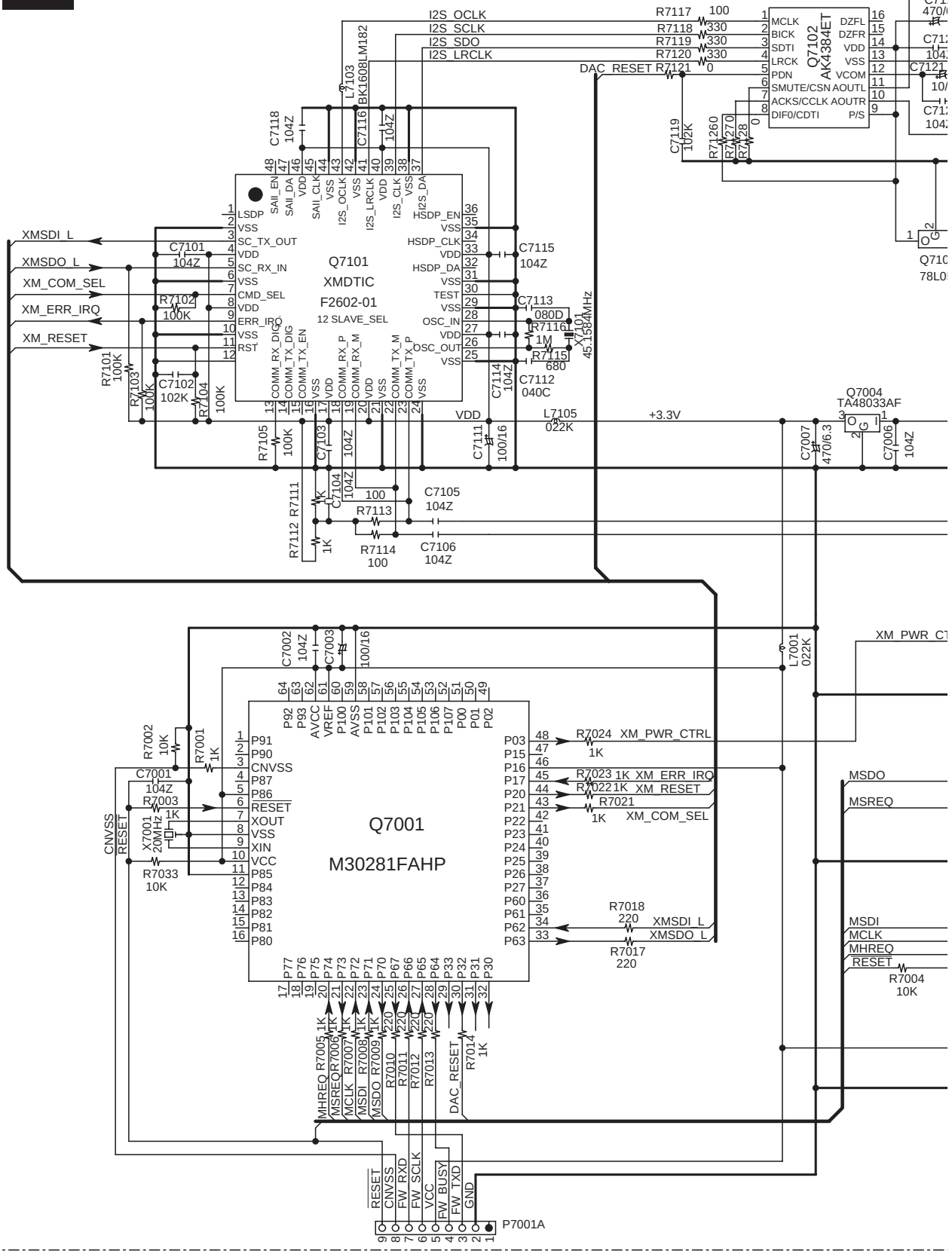

A
B
C
D
1
2
3
4
5
U07
NADIS-8683
FAC2 1
FAC1 2
-VP 3
GNDFL 4
JL957A
GNDD 40
GNDD 39
5VDIS 38
5VDIS 37
36
GNDV 35
34
GNDV 33
YSV4 32
GNDV 31
CSV4 30
GNDV 29
+5VM 28
MICDET 27
KINT3 26
KINT2 25
KINT1 24
KINT0 23
KEY3 22
KEY2 21
KEY1 20
KEY0 19
VAJ 18
VBJ 17
FLDRST 16
FLDCS 15
REMIN 14
FLDCLK 13
FLDSDO 12
LEDZONE2 11
LEDSBY 10
OPTF 9
GNDA 8
MICOUT 7
GNDA 6
V4L 5
GNDA 4
V4R 3
+7V 2
-7V 1
P7534B 1mmFFC CN40
C7505 104Z
L7501 022M
+5VM
REMIN
7529
100
509
402
Q7510 2SC2712
-7V
+7V
R7623 10
R7621 10
MMUTE
MICOUT
MICDET
Q7515:A NE5532
Q7515:B NE5532
R7625 56K
R7624 56K
R7622 100
R7703 4.7K
R7618 330
D7601 UDZS5.1B
C7610 47/16
GNDA
Q7607 RN1441
Q7605 RN1441
R7613 220
R7611 220
C7612 47/16
C7607 100
C7605 330J
R7609 33K
R7606 1K
R7605 100K
C7603 101J
C7609 101J
R7600 330
C7613 47/16
R7607 220K
Q7602 RN1441
Q7601:B NE5532
Q7601:A NE5532
NAETC-8684
JL7501A
JL7501B
R7641 220
L7641 022M
OUT
G
VCC
U7641 TORX177L
C7641 100/16
C7642 104Z
U072
JL7540A
JL7540B
V4C 1
V4Y 2
GNDV 3
V4V 4
V4LI 5
GNDA 6
V4RI 7
MICA 8
MICD 9
R7635 75
R7634 75
R7633 75
R7632 330
C7632 471J
C7631 471J
R7631 330
P7631
L7603 022M
P7601
L7604 022M
C7633 102K
C7634 102K
C7600 102K
E7501
GND TERMINAL
U073
NAETC-8685
JL7542B
5 HPDET
4 GNDD
3 HPL
2 HPE
1 HPR
R7721 0
R7722 0
L7621 022M
L7622 022M
L7623 022M
C7623 1
104Z
C7622 102J
C7621 102J
C7624 102K
E7621
P7602 3_5HPSTSW2
Val
SCHEMATIC DIAGRAM 9
DISPLAY SECTION

SCHEMATIC DIAGRAM 10

XM RADIO SECTION (North American models)

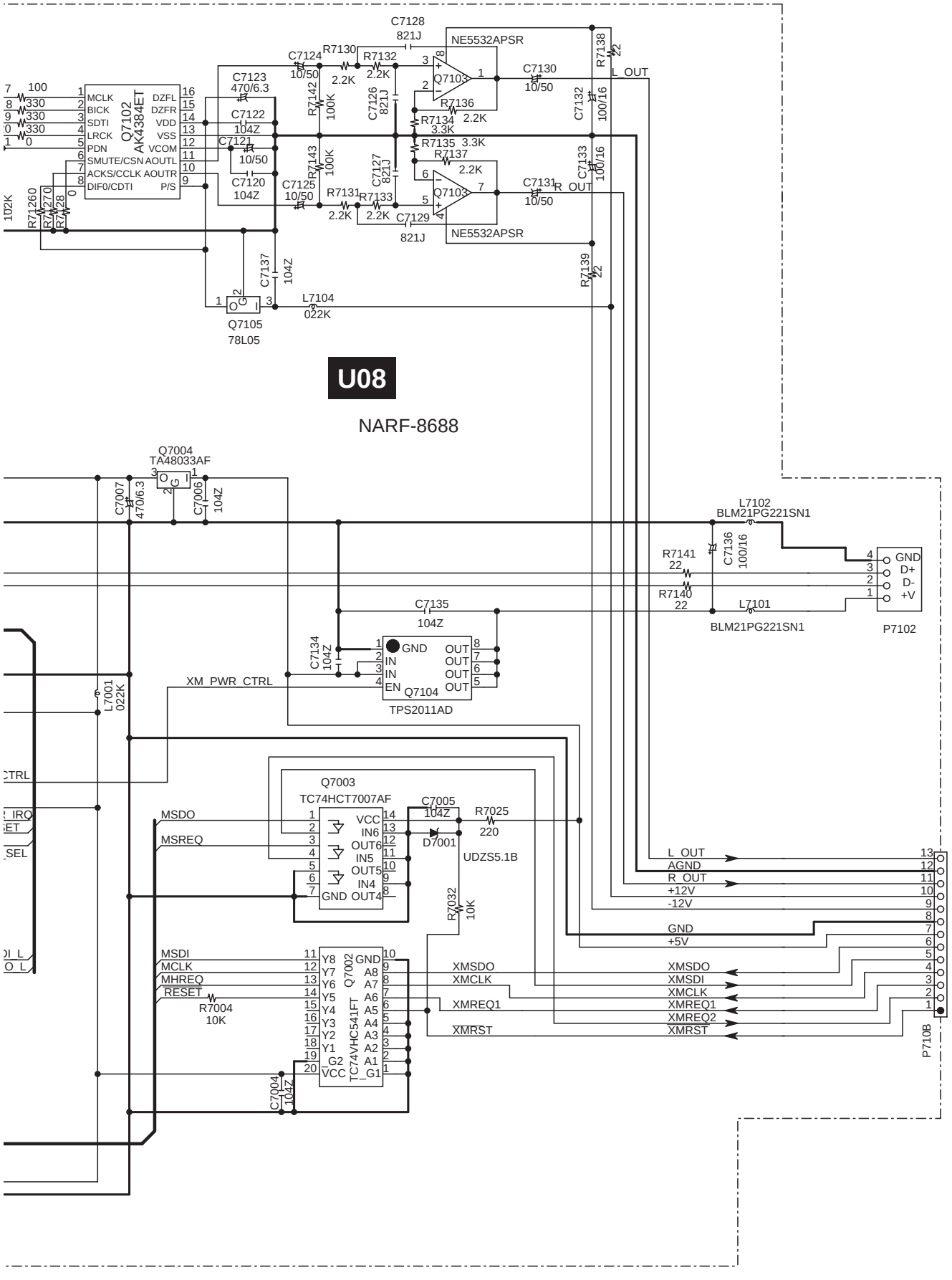
NARF-8688

U08



SCHEMATIC DIAGRAM 10

XM RADIO SECTION (North American models)



SCHEMATIC DIAGRAM 1

VIDEO SECTION

NAVD-8657

U02

Selector & 6dB AMP

Switch Controller

Video Decoder

Video Encoder

Video AMP with HPF

SPEAKER RELAY DRIVER

SCHEMATIC DIAGRAM 2

DSP SECTION

U03

NADG-8660

Q201 CS494003

Q361 CS42518-CQ

Q211 MX26LV040-70

Q285 M13S1616A-7TG or K4S511632D

Q331 CS5340-CZZ

Q341 CS5340-CZZ

Q351 CS5340-CZZ

P101 COAX1 COAX2 DIGITAL IN OPT1 OPT2 OPT3 DIGITAL OUT

P102 SYSIN

P3101B TO NAAF-8678

P3102B TO NAAF-8678

P301A TO NAAR-8661

P301A TO NAAR-8661

SCHEMATIC DIAGRAM 3
MICROPROCESSOR SECTION

U032

NAAR-8661

P7534A TO DISPLAY (NADIS-8683)

P702 TO FLASH WRITER

JL703B TO THERMAL SENSOR NAETC-8680

P710A TO XM RADIO NARF-8688 DD model only

JL7452A TO HEAD PHONE NARF-8688

P959A TO POWER SUPPLY NAPS-8665

TO POWER SUPPLY NAPS-8665 P954A

TO DSP/CODEC P601B NADG-8660

P602B TO DSP/CODEC NADG-8660

Q710 XC6213B332MR

Q702 RN1404

Q703 RN2402

Q704 RN2402

Q705 RN1404

Q706 RN2402

Q707 RN1404

Q708 RN2402

Q709 RN1404

Q701 M30627FHPGP

MODEL	R605 R606 R608 R609
MDD-TYPE	YES
other	NO

P2004A TO VIDEO NAVD-8657

P2005A TO VIDEO NAVD-8657

P3103B P3104B TO VOLUME/AMP NAAF-8678 P3105B

P701A TO TUNER PACK

RL1N4003 GP104003E

SCHEMATIC DIAGRAM 4
PREAMPLIFIER SECTION

A B C D E F G H

1 2 3 4 5

CD
TAPE_OUT
TAPE
VIDEO3
VIDEO2_OUT
VIDEO2
VIDEO1_OUT
VIDEO1
DVD
SL/SR
C/SW
SBL/SBR
FL/FR
SL/SR
PREOUT
C/SW
SBL/SBR

P3002 P3003 P3004 P3005 P3006 P3008 P3009

P3010 P3101A P3102A

DACSBR DACSBL

Q3002 NJU7311AM

Q3003 NJW1157

FSWDATA FSWCLK FSWSTB

Q3004:A NE5532 Q3004:B NE5532

Q3005 78L07 Q3006 79L07 Q3007:A NE5532

D3005 1SS352 D3006 1SS352 D3938 1SS352 D3939 1SS352 D3940 1SS352 D3941 1SS352

Q3505 LM2940CT-5.0 Q3506 NJM7905FA Q3507 NJM7812FA Q3508 NJM7912FA

+12V -12V

U06

NAAF-8678(1/2)

To schematic 5

P3103A P3104A P3105A

Q3009 BD3814

LOGIC AGND1 DA MUTE DGND AGND2 INSW AGND3 INSB AGND4 INC AGND5 INFR AGND6 VEE TREBLE

P5003B P5004B

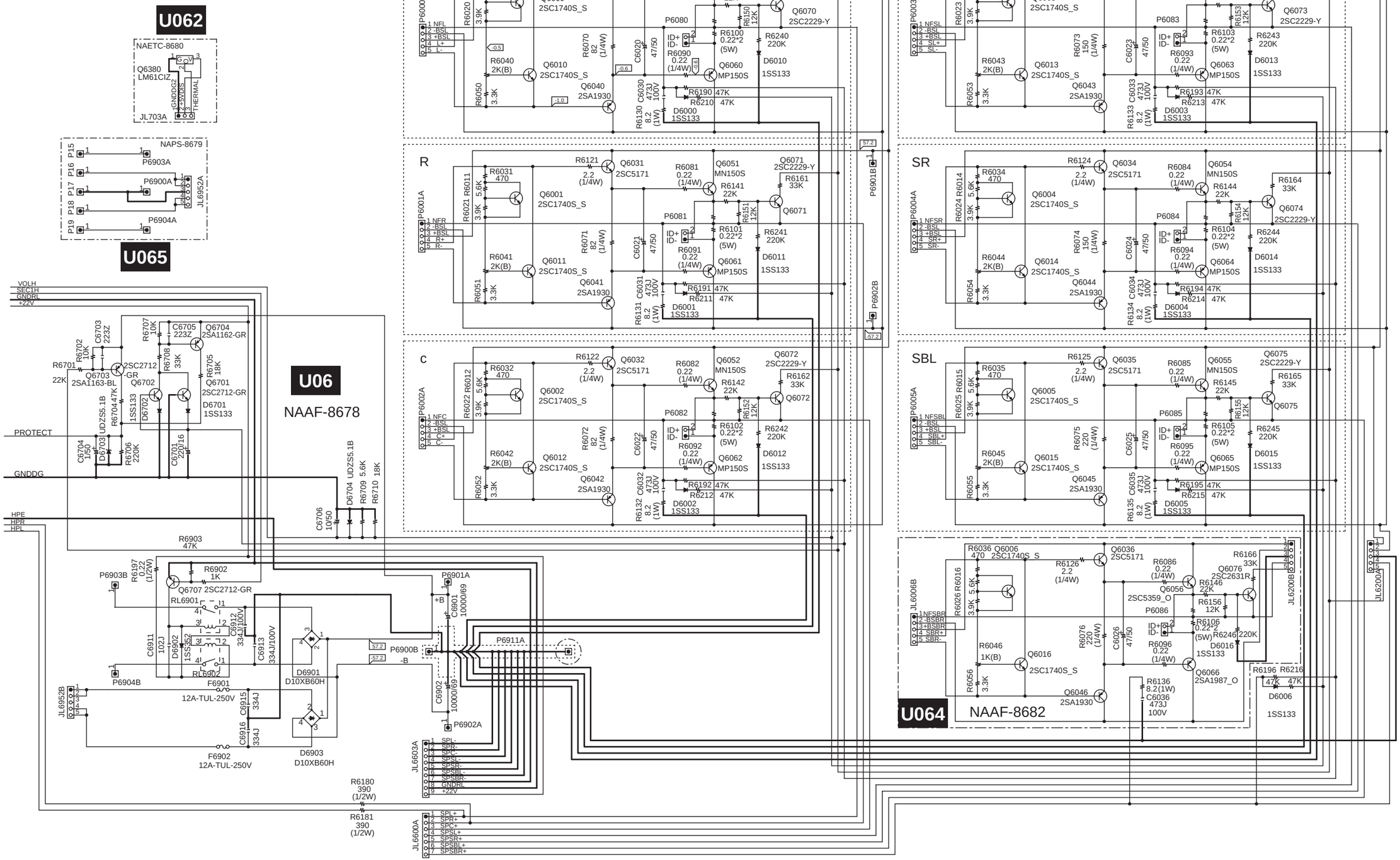
RL3201 RL3202 D3201 1SS352 D3202 1SS352 Q3251 RN1402 Q3252 RN1402

SPRLF SPRLSB

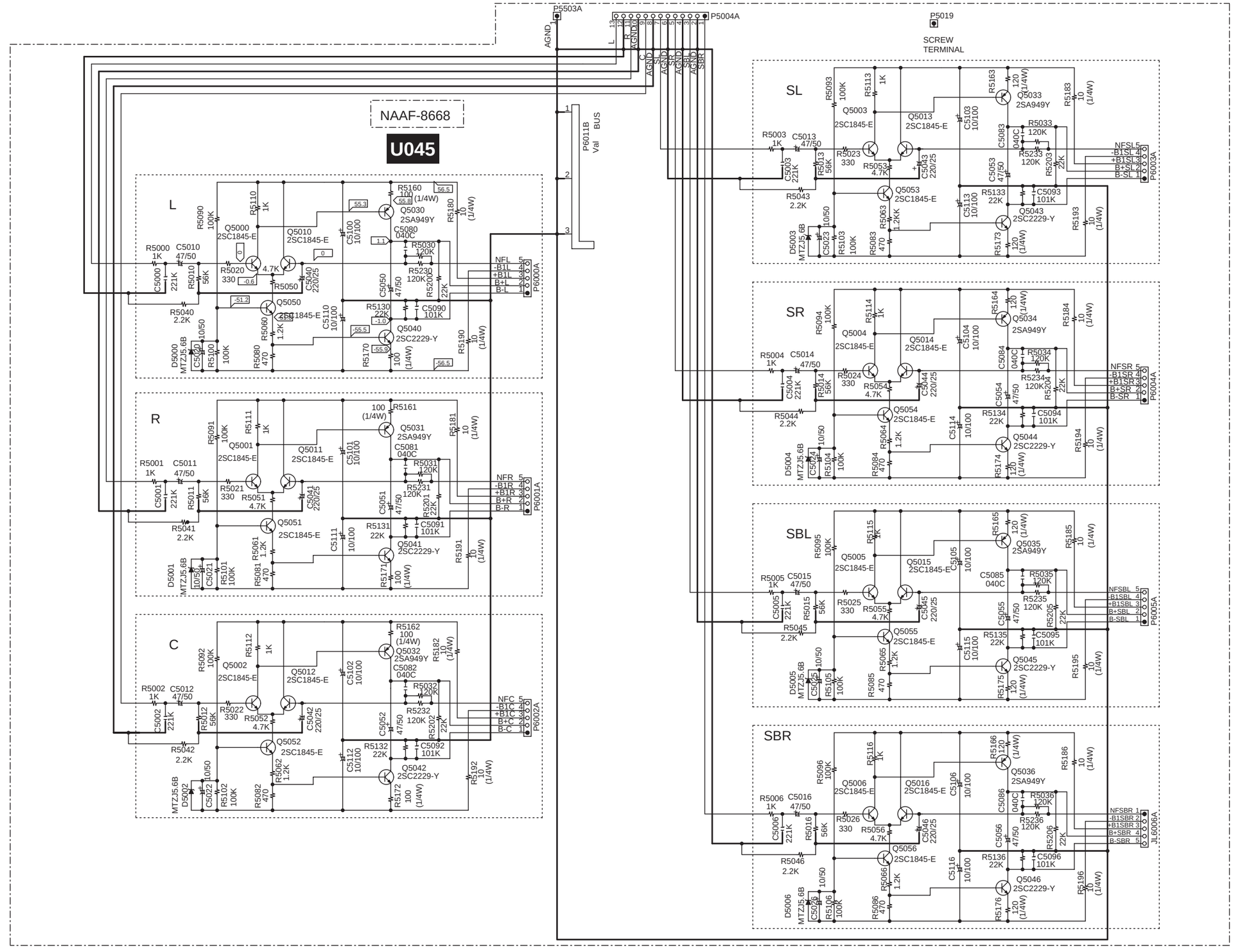
VLDATA VLCLK VLSTB

Z2VMUT Z2VDATA Z2VCLK Z2VLAT

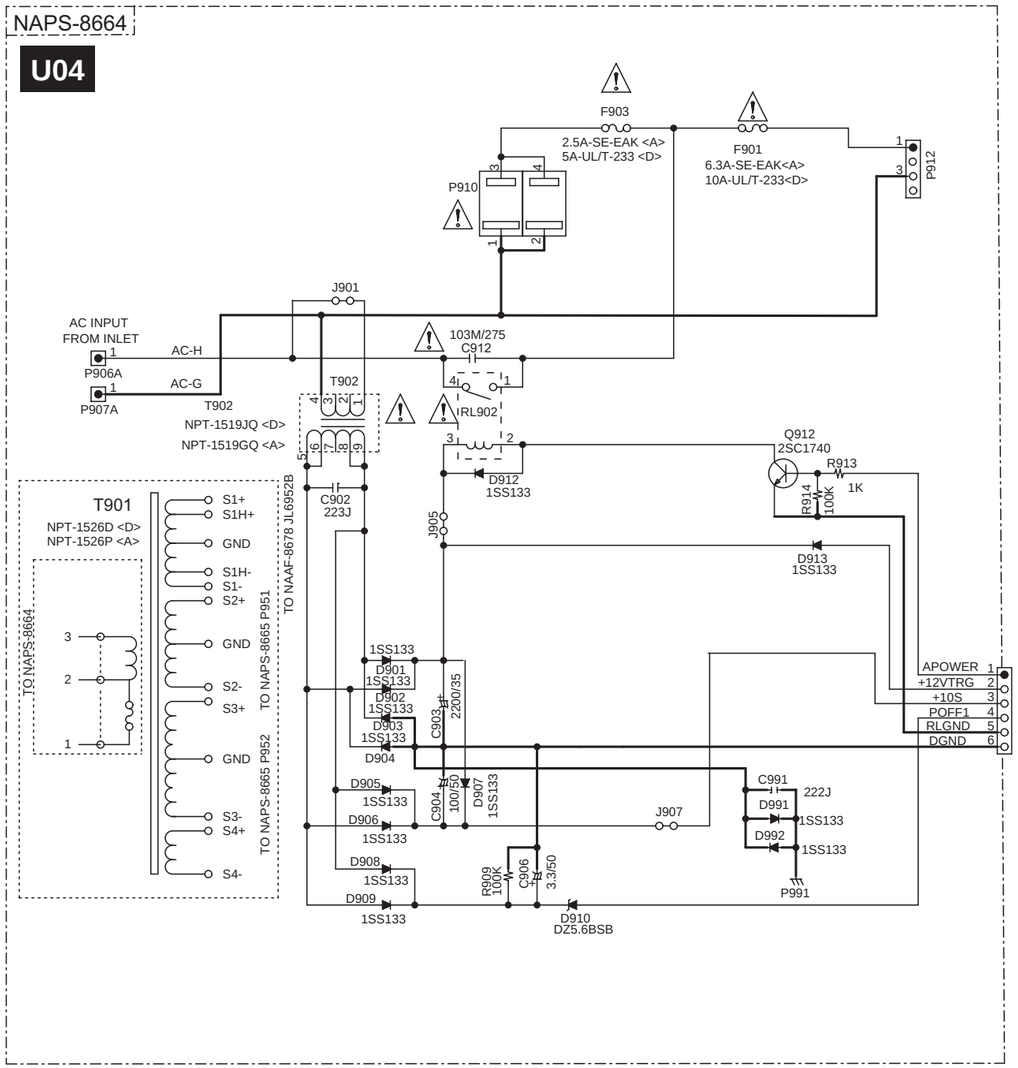
SCHEMATIC DIAGRAM 5
POWER AMPLIFIER SECTION

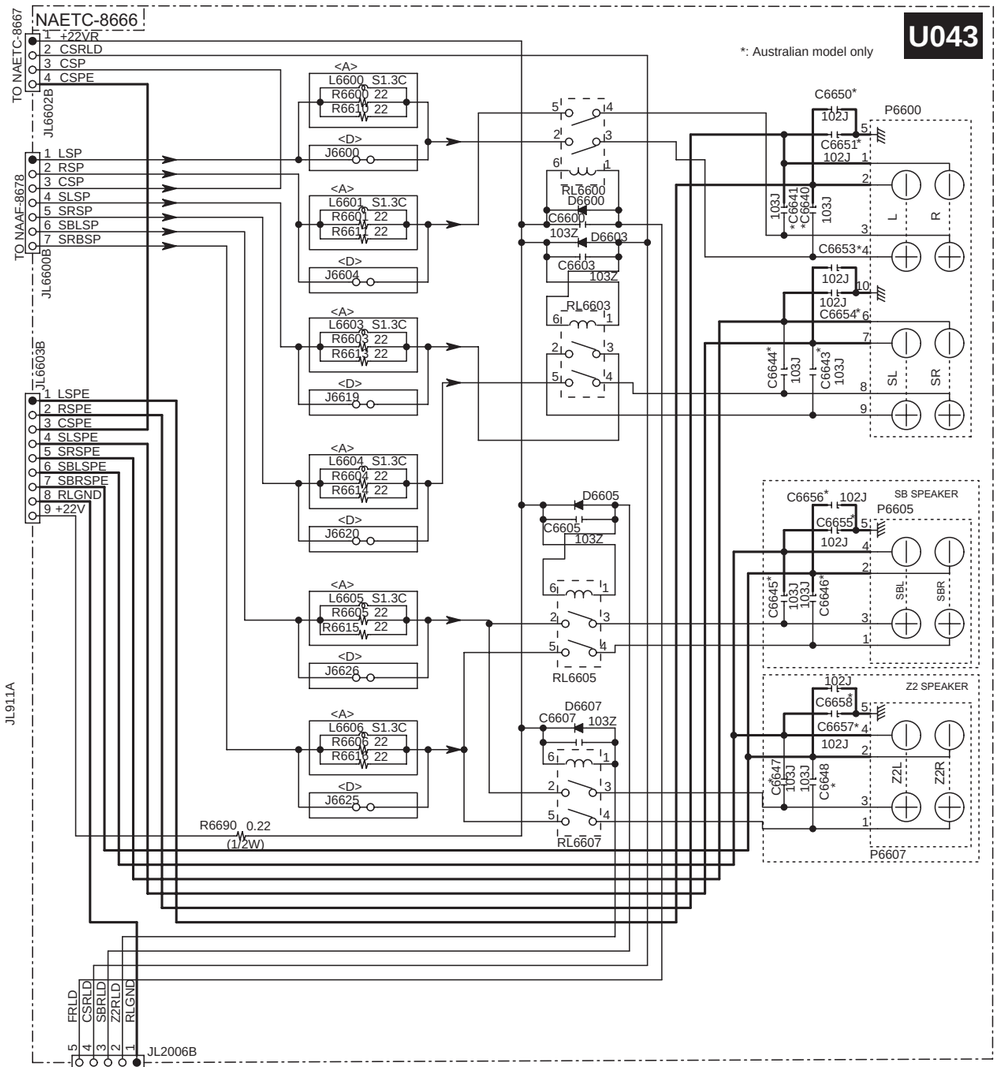


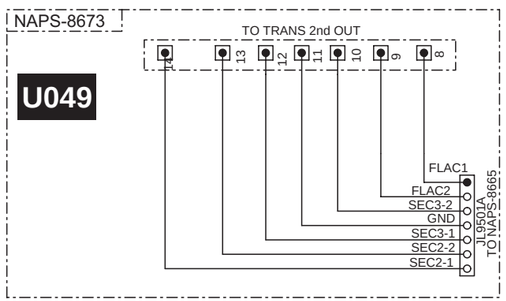
SCHEMATIC DIAGRAM 6
DRIVER SECTION

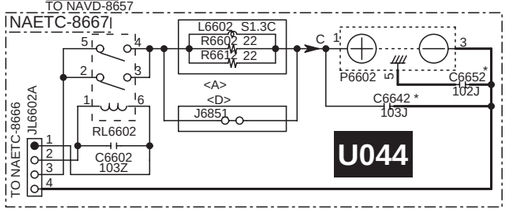


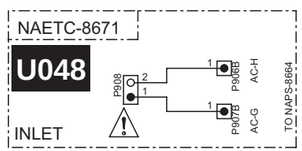
SCHEMATIC DIAGRAM 7
POWER SUPPLY SECTION











CAUTION
FOR CONTINUED PROTECTION AGAINST FIRE HAZARD, REPLACE ONLY WITH FUSE OF SAME TYPE AND RATING INDICATED.

ATTENTIION
AFIN D'ASSURER UNE PROTECTION PERMANENTE CONTRE LES RISQUES D'INCENDIE, REMPLACER UNIQUEMENT PAR UN FUSIBLE DE MEME TYPE ET CALIBRATION COMME INDIQUE.

THIS SYMBOL LOCATED NEAR THE FUSE INDICATES THAT THE FUSE USED IS SLOW OPERATING TYPE. FOR CONTINUED PROTECTION AGAINST FIRE FUSE HAZARD,REPLACE WITH SAME TYPE FUSE. FOR FUSE RATING REFER TO THE MAKING ADJACENT TO THE SYMBOL.

CE SYMBOLE INDIQUE QUE LE FUSIBLE UTLISE EST A LENT. E POUR UNE PROTECTION PERMANENTE.NUTILISER QUE DES FUSIBLES DE MEME TYPE. CE DARNIER EST INDIQUE LA QU LE PRESENT SYMBOL EST APPOSE.

NOTE

THE COMPONENTS IDENTIFIED BY MARK ⚠ ARE CRITICAL FOR SAFETY.
REPLACE ONLY WITH PART NUMBER SPECIFIED.
ELECTROLYTIC CAPACITORS ⊣⊢ ARE IN uF/WV.
ALL CAPACITORS ARE IN pF/50WV UNLESS OTHERWISE NOTED.
EX) 032 3pF 330 33pF 331 330pF 333 0.033uF
ALL RESISTORS ARE IN OHMS 1/4WATTS UNLESS OTHERWISE NOTED.
THE THICK LINES ON PC BOARD ARE THE PRINTING SIDE OF THE PARTS
EX ○○○ PRINTING SIDE
CIRCUIT IS SUBJECT TO CHANGE FOR IMPROVEMENT.

SCHEMATIC DIAGRAM 8
POWER SUPPLY SECTION

NAPS-8665

U042

SCHEMATIC DIAGRAM 9
DISPLAY SECTION

NADIS-8683

U07

Q7501 HNA-16SM10T

Q7502 M66005

Q7503 2SC2712

Q7506 RN1402

Q7509 RN2402

Q7510 2SC2712

D7501 UDZS8.2B

D7502 STBY

D7503 ZONE2

U7501

LEDSBY

LEDZONE2

VAJ

VBJ

JL7503A

JL7503B

S7591

U075 NAETC-8687

U073 NAETC-8685

JL7542B

E7621

P7602 3_5HPSTSW2

JL7501A

JL7501B

U072 NAETC-8684

U7641 TORX177L

JL7540A

JL7540B

Q7515:A NE5532

Q7515:B NE5532

Q7601:B NE5532

Q7601:A NE5532

Q7607 RN1441

Q7605 RN1441

Q7602 RN1441

D7601 UDZS5.1B

E7501 GND TERMINAL

P7534B 1mmFFC CN40

P7631

P7601

+5VM REMIN

-7V

+7V

MMUTE

MICOUT

MICDET

GNDA

STANDBY S7501

ZONE2 S7502

ZONE2 OFF S7503

ZONE 2V S7504

ZONE 2V+ S7505

MULTI S7506

DVD S7534

TUNER S7508

TAPE S7509

CD S7511

VIDEO4 S7512

VIDEO3 S7513

VIDEO2 S7514

S7533 VIDEO1

TUN MODE S7515

MEMORY S7516

DIMMER S7517

LIS MODE+ S7518

LIS MODE- S7519

STEREO S7520

TONE+ S7530

TONE- S7531

TONE S7532

SETUP S7521

RETURN S7522

PRESET FR S7523

PRESET DOWN S7524

PRESET UP S7525

PRESET FF S7526

ENTER S7527

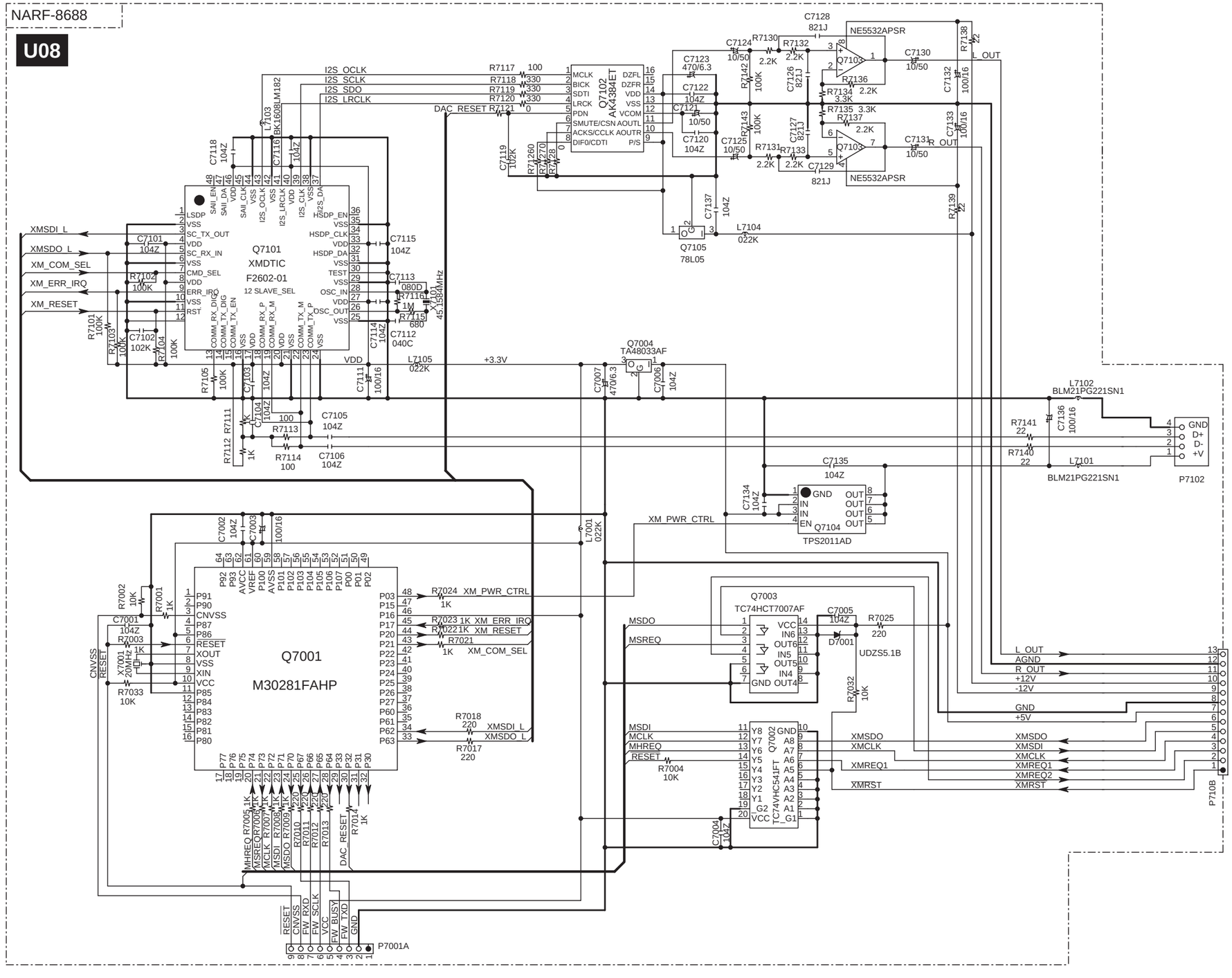
DISPALY S7528

SCHEMATIC DIAGRAM 10

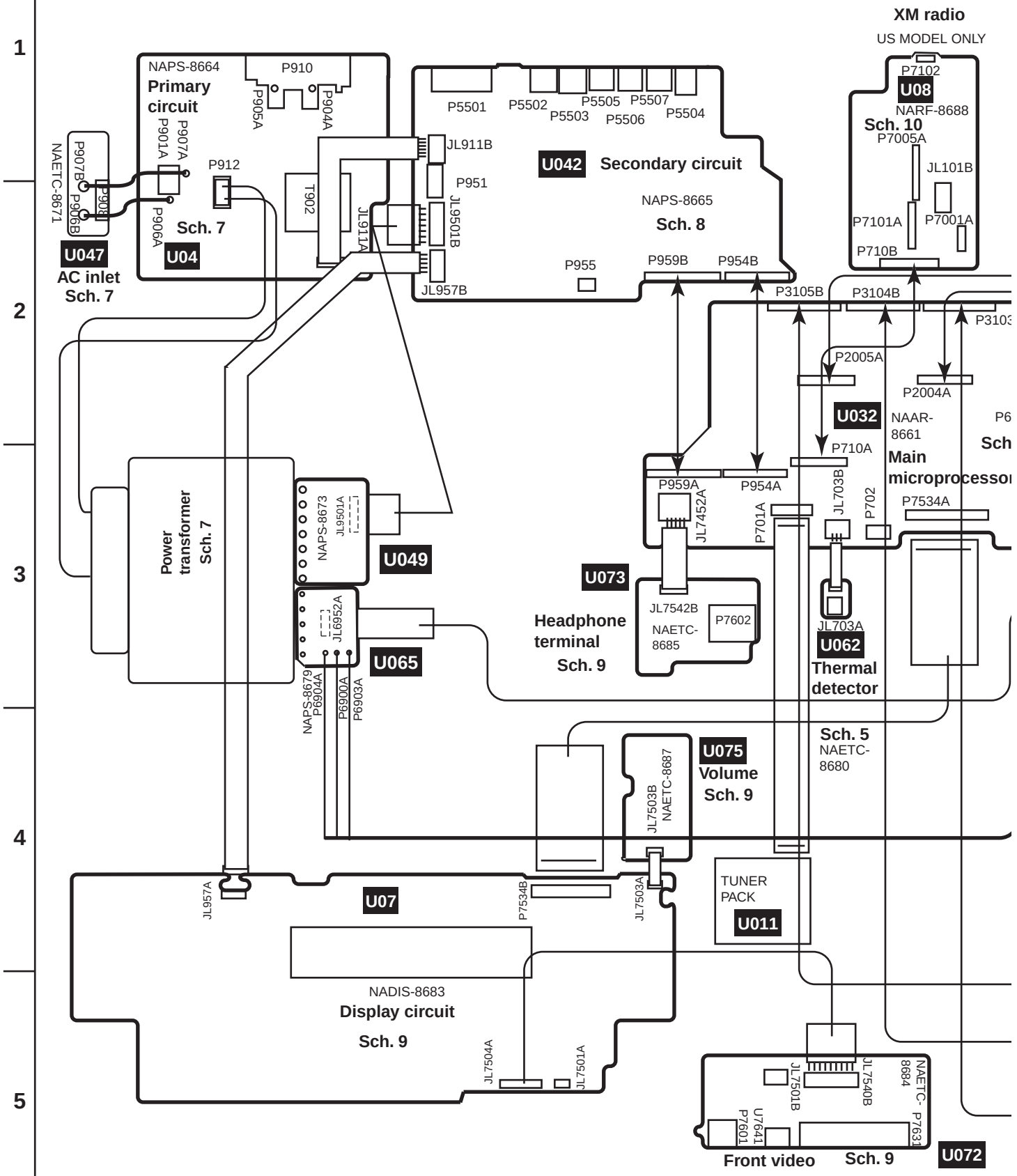
XM RADIO SECTION (North American models)

NARF-8688

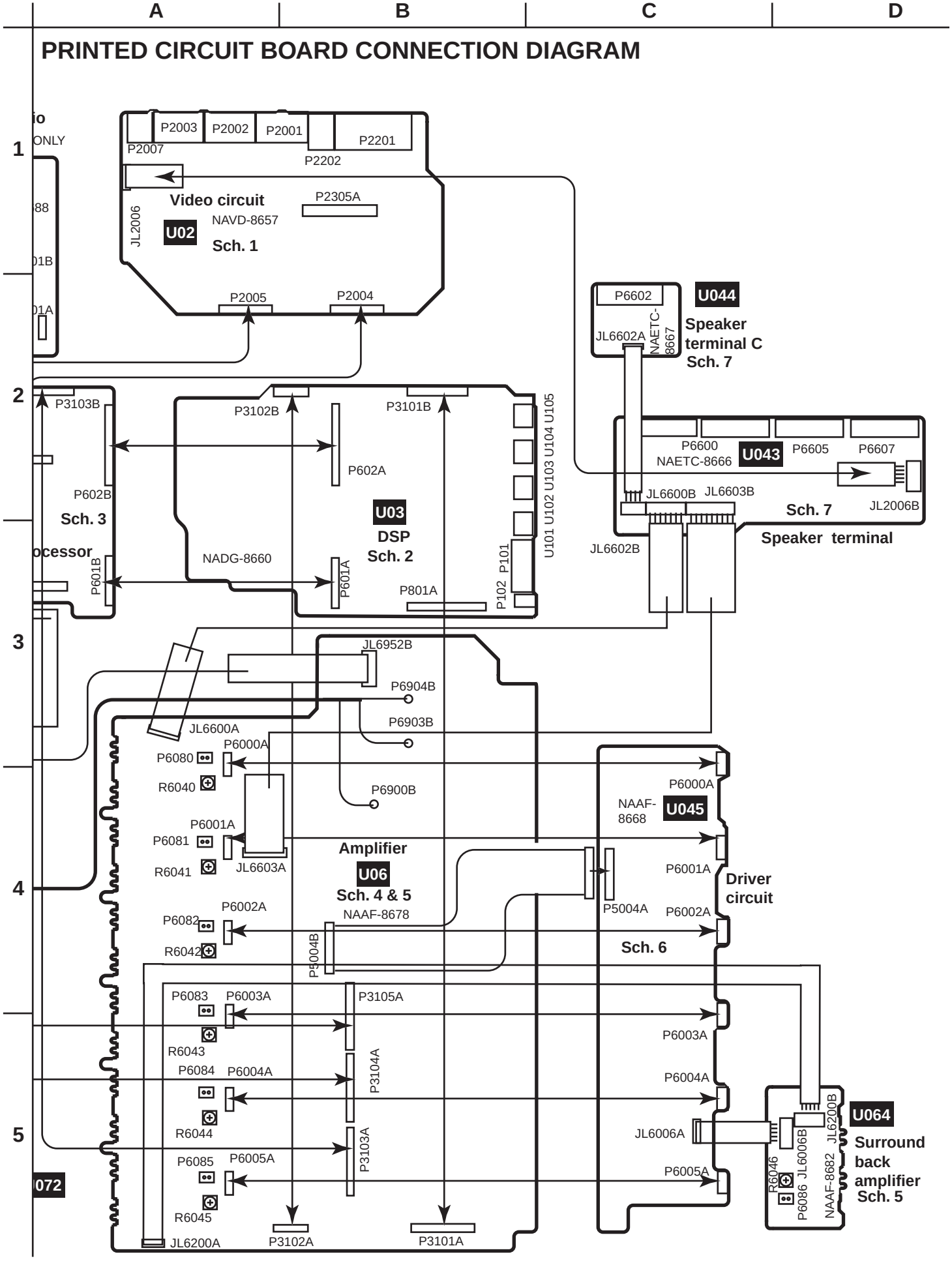
U08



PRINTED CIRCUIT BOARD CONNECTION DIAGRAM



PRINTED CIRCUIT BOARD CONNECTION DIAGRAM



PRINTED CIRCUIT BOARD CONNECTION DIAGRAM

A B C D E F G H

1 2 3 4 5

NAPS-8664
Primary circuit
P910
P905A P904A
P901A P907A
P912
P907B P906B P906A
NAETC-8671
Sch. 7
U047
AC inlet
Sch. 7
U04

P5501 P5502 P5503 P5505 P5506 P5507 P5504
JL911B
P951
JL9501B
JL911A
T902
U042 Secondary circuit
NAPS-8665
Sch. 8
P955
P959B P954B
JL957B

XM radio
US MODEL ONLY
P7102
U08
NARF-8688
Sch. 10
P7005A
JL101B
P7101A P7001A
P710B

P2003 P2002 P2001 P2201
P2007
P2202
Video circuit
P2305A
JL2006
U02
NAVD-8657
Sch. 1
P2005 P2004

P6602
JL6602A NAETC-8667
U044
Speaker terminal C
Sch. 7

P3105B P3104B P3103B
P2005A
P2004A
U032
NAAR-8661
Main microprocessor
P710A
P959A P954A
JL7452A
P701A
JL703B
P702
P7534A
P601B
Sch. 3

P3102B P3101B
P602A
U03
DSP
Sch. 2
NADG-8660
P601A
P801A
P102 P101
U101 U102 U103 U104 U105

P6600
NAETC-8666
U043
P6605 P6607
JL6600B JL6603B
Sch. 7
JL2006B
JL6602B
Speaker terminal

Power transformer Sch. 7

NAPS-8673
JL9501A
U049

NAPS-8679
JL6952A
P6904A P6900A P6903A
U065

U073
Headphone terminal
Sch. 9
JL7542B
NAETC-8685
P7602

JL703A
U062
Thermal detector
Sch. 5
NAETC-8680

U075
Volume
Sch. 9
JL7503B NAETC-8687

JL6952B
P6904B
P6903B
JL6600A
P6000A
P6080
R6040
P6900B
P6001A
P6081
R6041
JL6603A
Amplifier
U06
Sch. 4 & 5
NAAF-8678
P6002A
P6082
R6042
P5004B
P6083 P6003A
R6043
P6084 P6004A
R6044
P6085 P6005A
R6045
JL6200A
P3102A
P3101A
P3105A
P3104A
P3103A

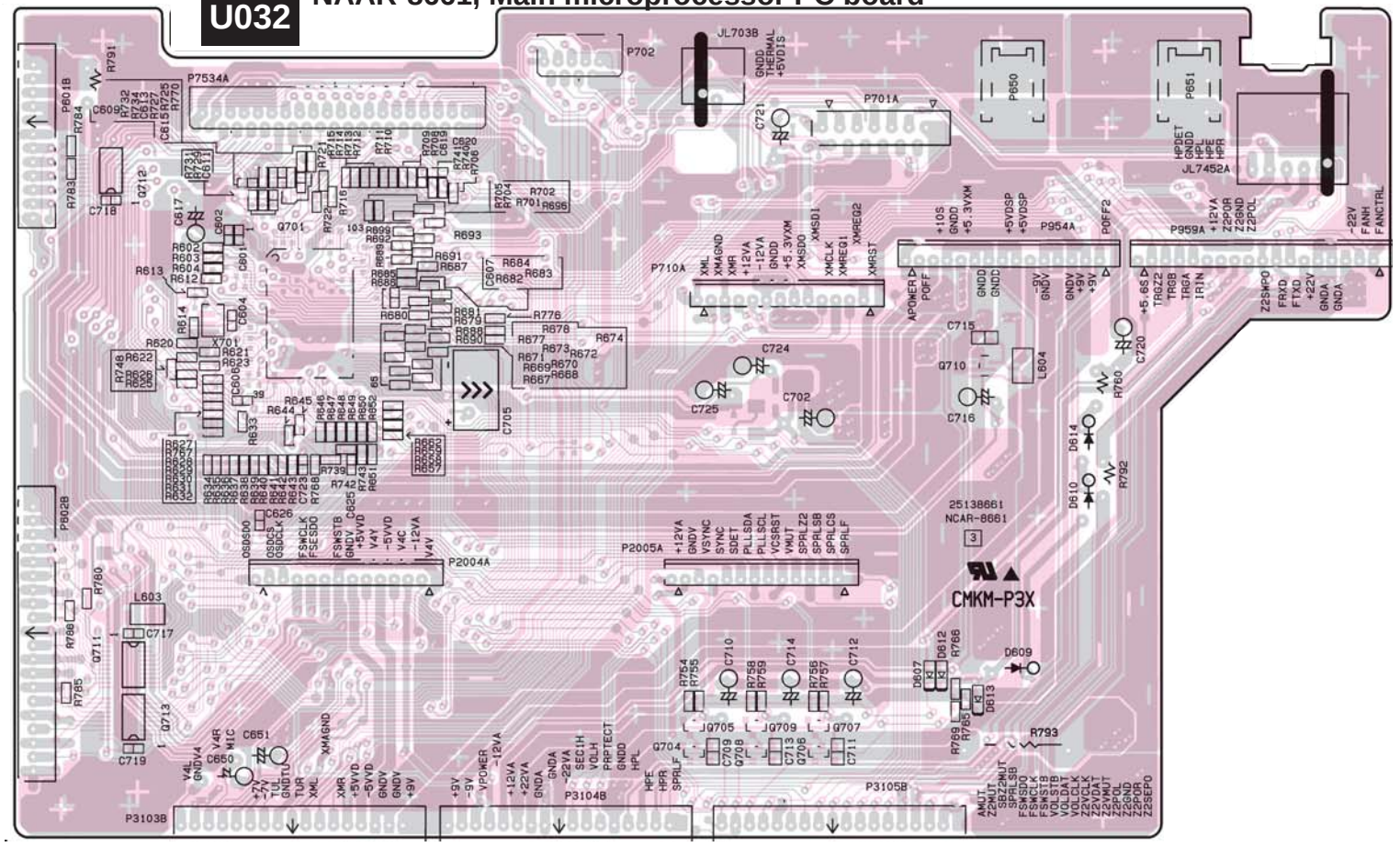
P6000A
NAAF-8668
U045
P6001A
P5004A
P6002A
Driver circuit
Sch. 6
P6003A
P6004A
JL6006A
P6005A
U064
JL6200B
JL6006B
R6046
P6086
NAAF-8682
Surround back amplifier
Sch. 5

JL957A
U07
P7534B
JL7503A
TUNER PACK
U011
NADIS-8683
Display circuit
Sch. 9
JL7504A
JL7501A

JL7501B
JL7540B
NAETC-8684
P7631
U7941
P7601
Front video
Sch. 9
U072

PRINTED CIRCUIT BOARD VIEW 1-1
Digital section

U032 NAAR-8661, Main microprocessor PC board



A	B	C	D	E

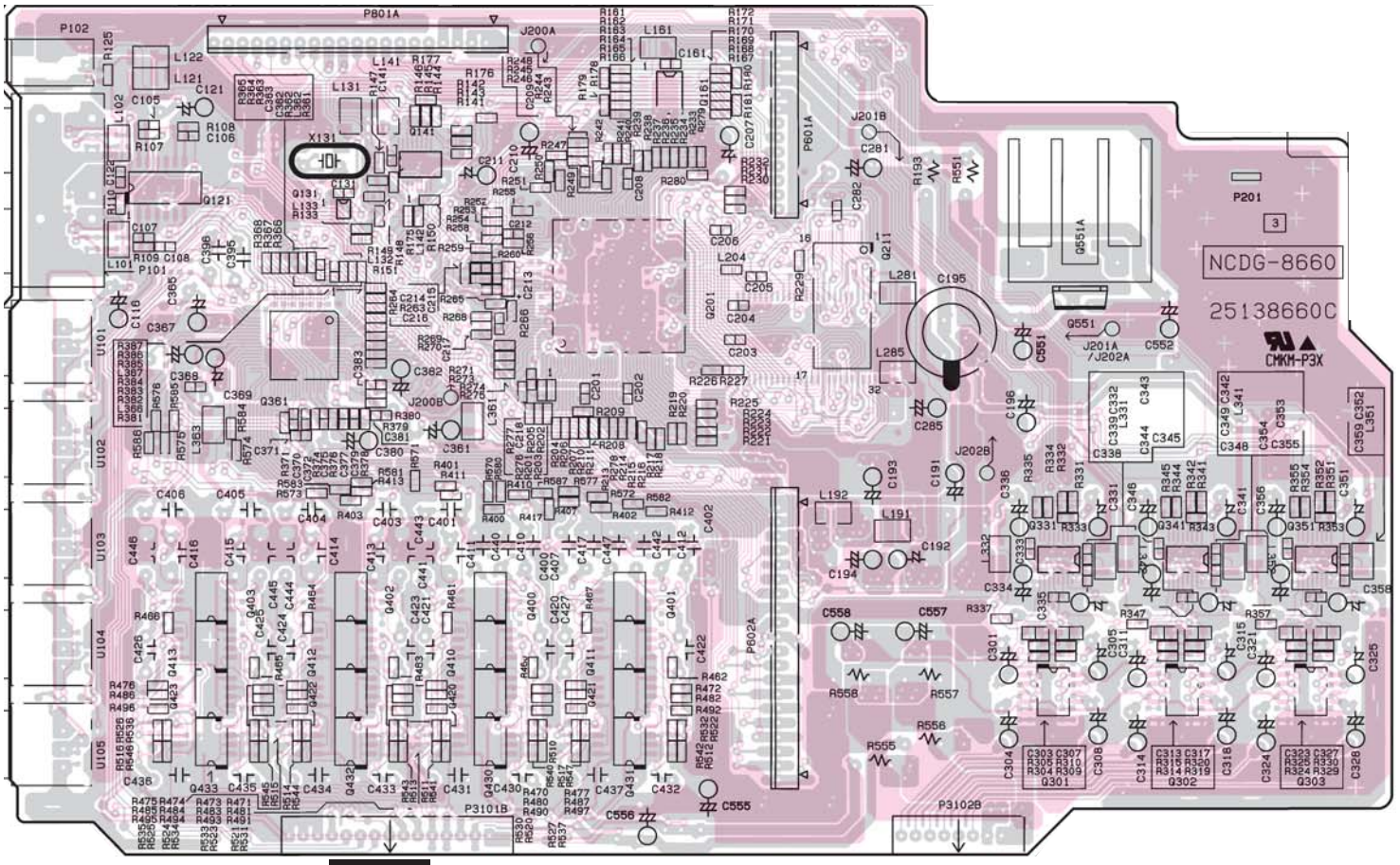
1

2

3

4

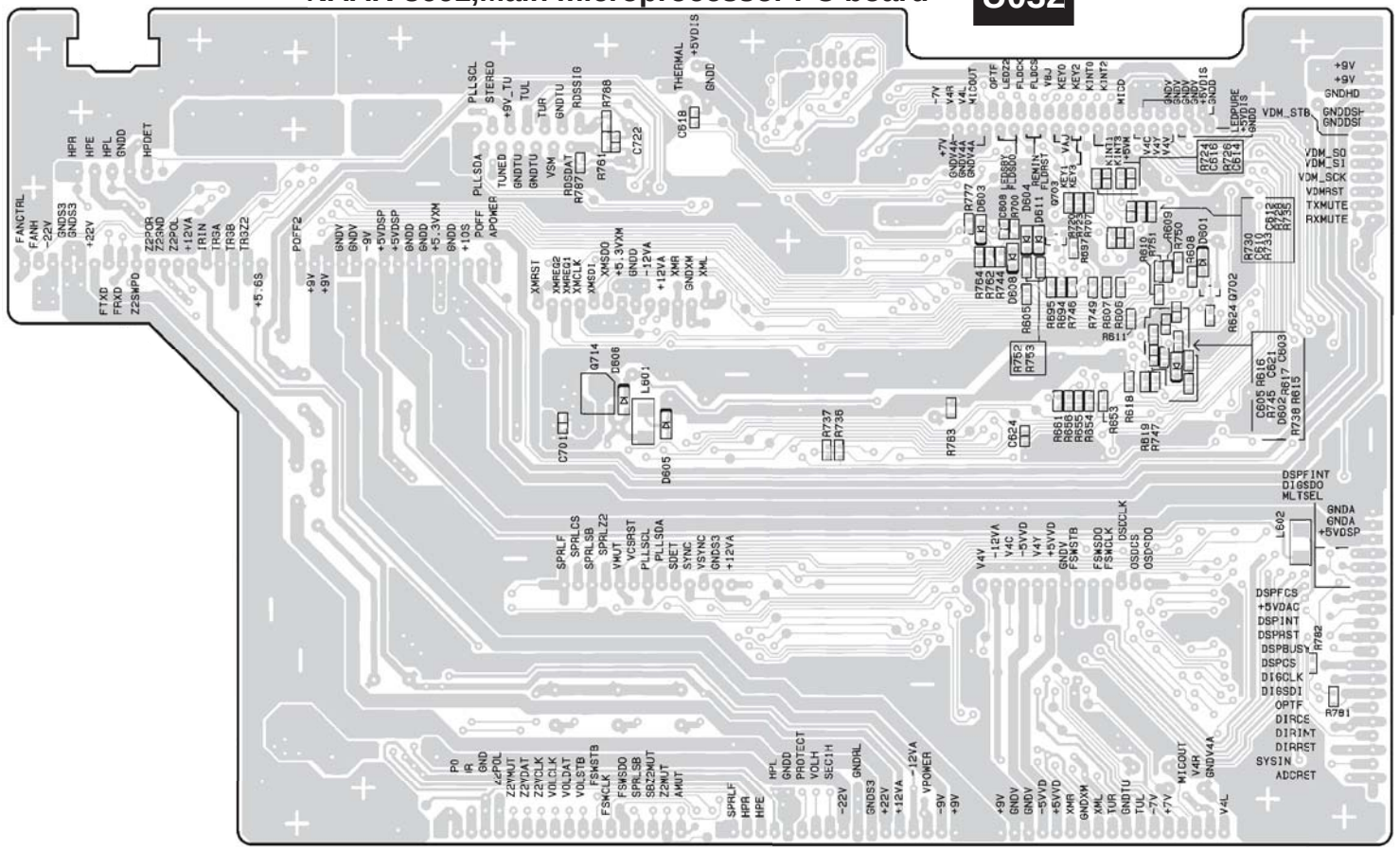
PRINTED CIRCUIT BOARD VIEW 1-1
Digital section



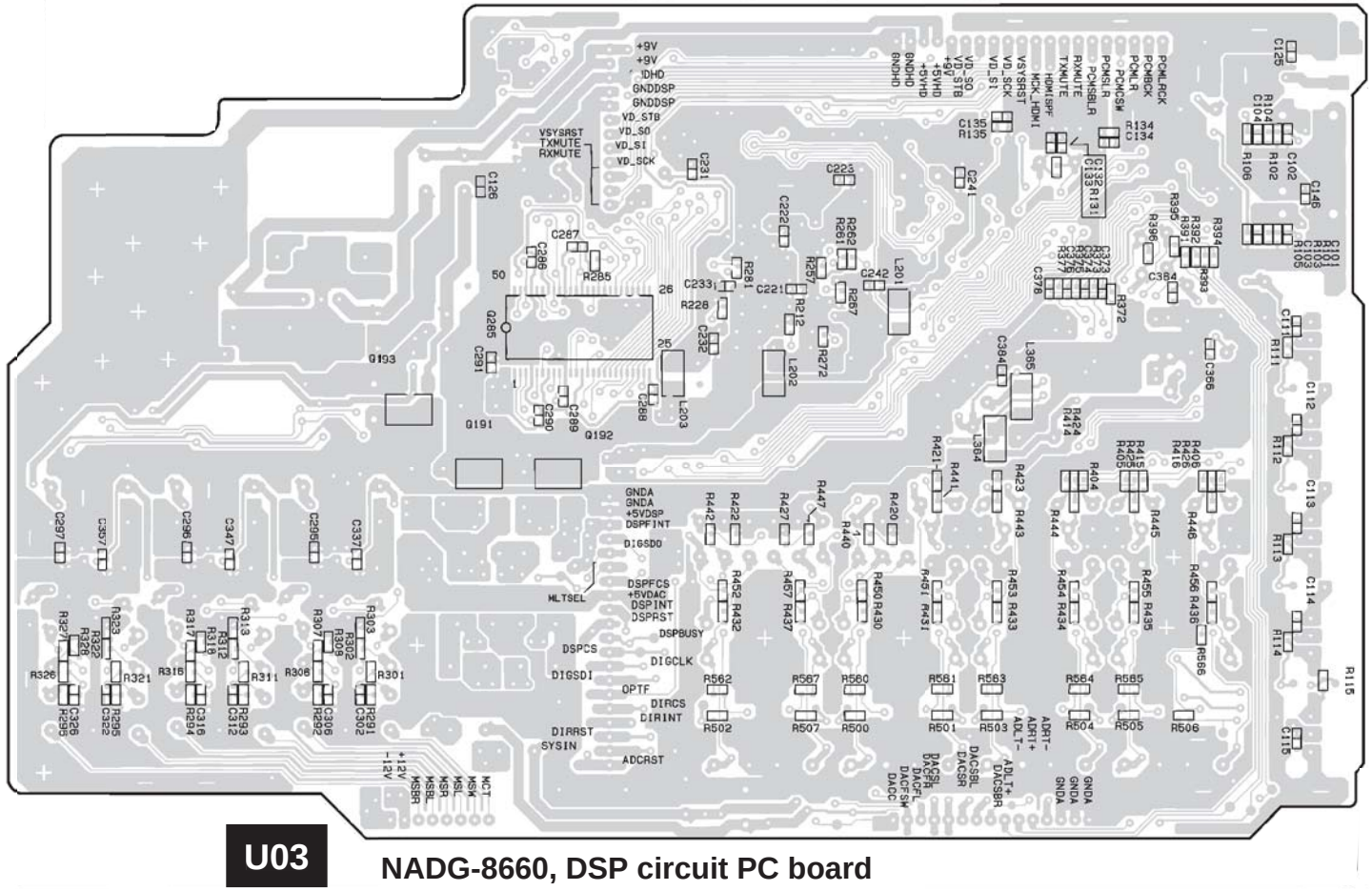
U03 NADG-8660, DSP circuit PC board

PRINTED CIRCUIT BOARD VIEW 1-2
Digital section

NAAR-8661,Main microprocessor PC board **U032**



PRINTED CIRCUIT BOARD VIEW 1-2
Digital section

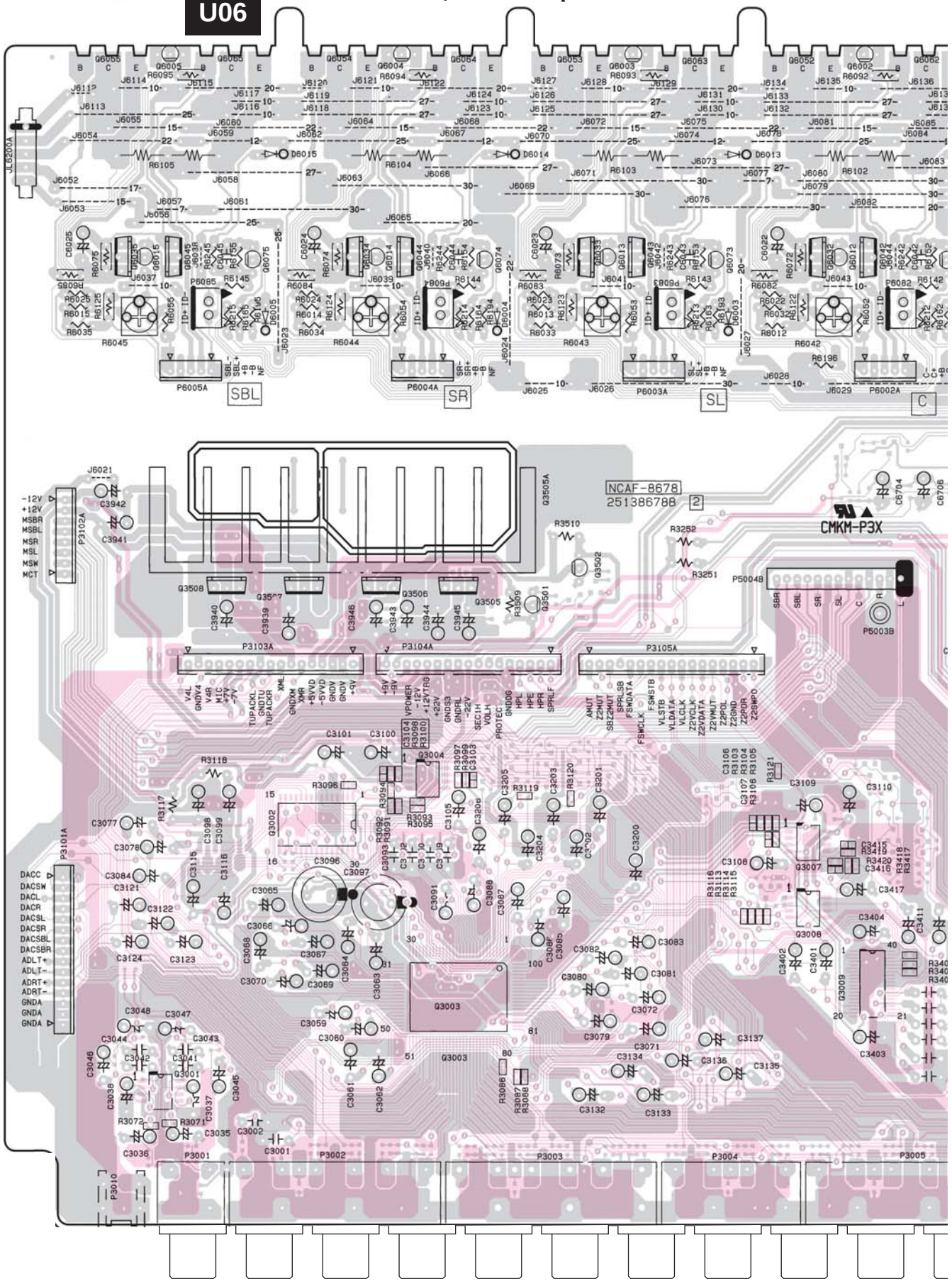


U03 NADG-8660, DSP circuit PC board

PRINTED CIRCUIT BOARD VIEW 2 Amplifier section

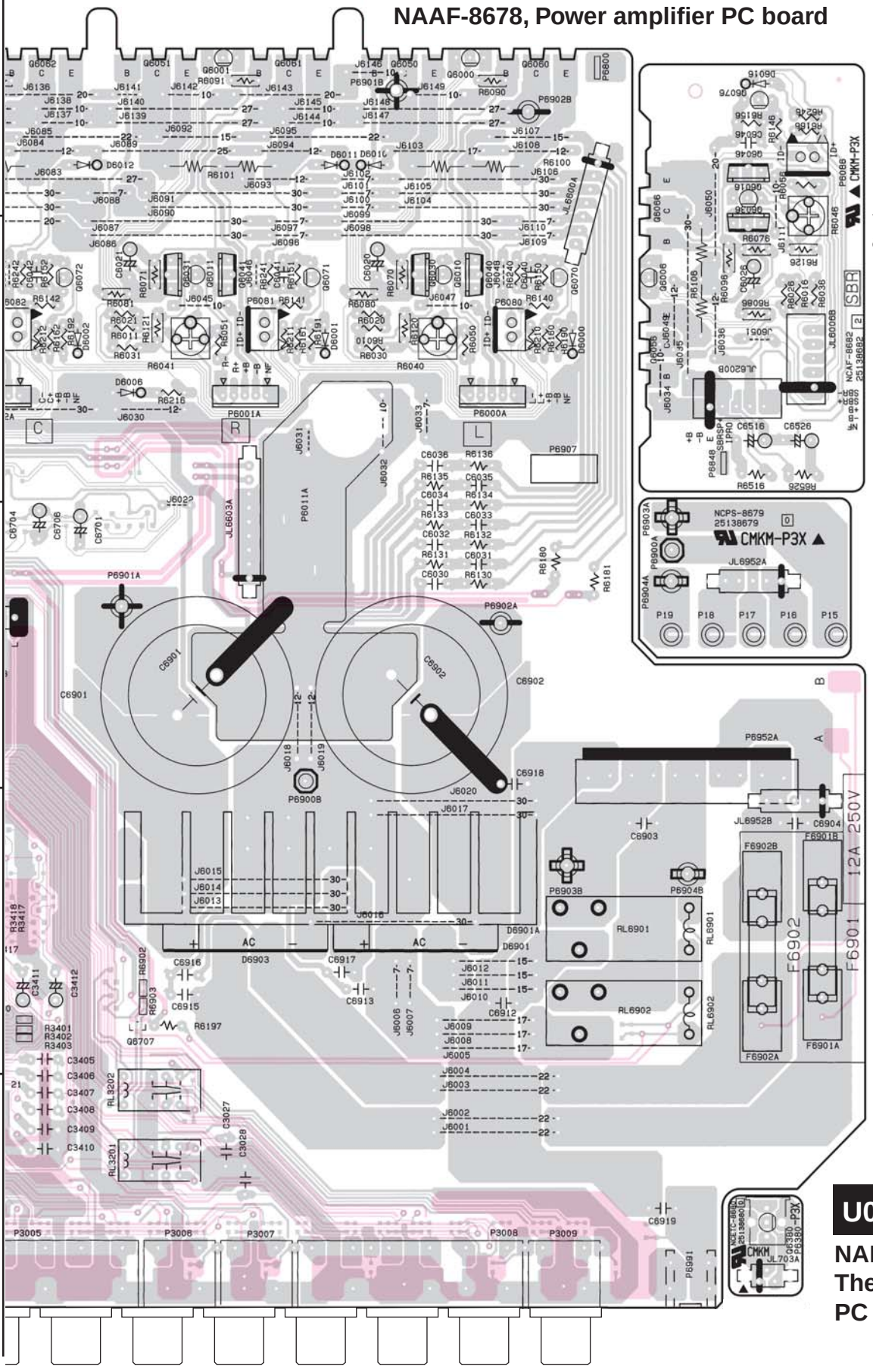
NAAF-8678, Power amplifier PC board

U06



PRINTED CIRCUIT BOARD VIEW 2 Amplifier section

NAAF-8678, Power amplifier PC board



U064

NAAF-8682, Surround back amplifier PC board

U061

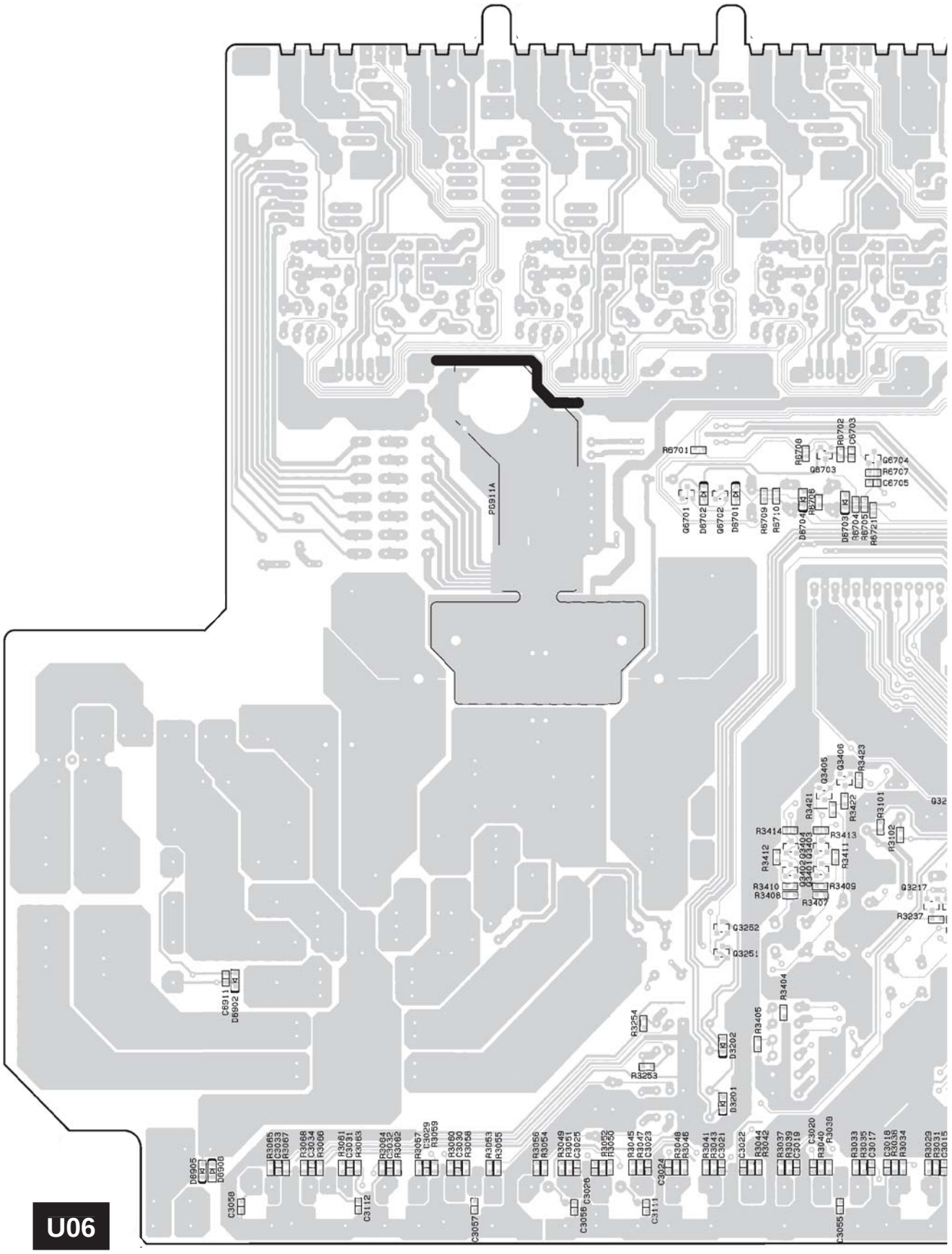
NAPS-8679, Power transformer PC board

U06

U062

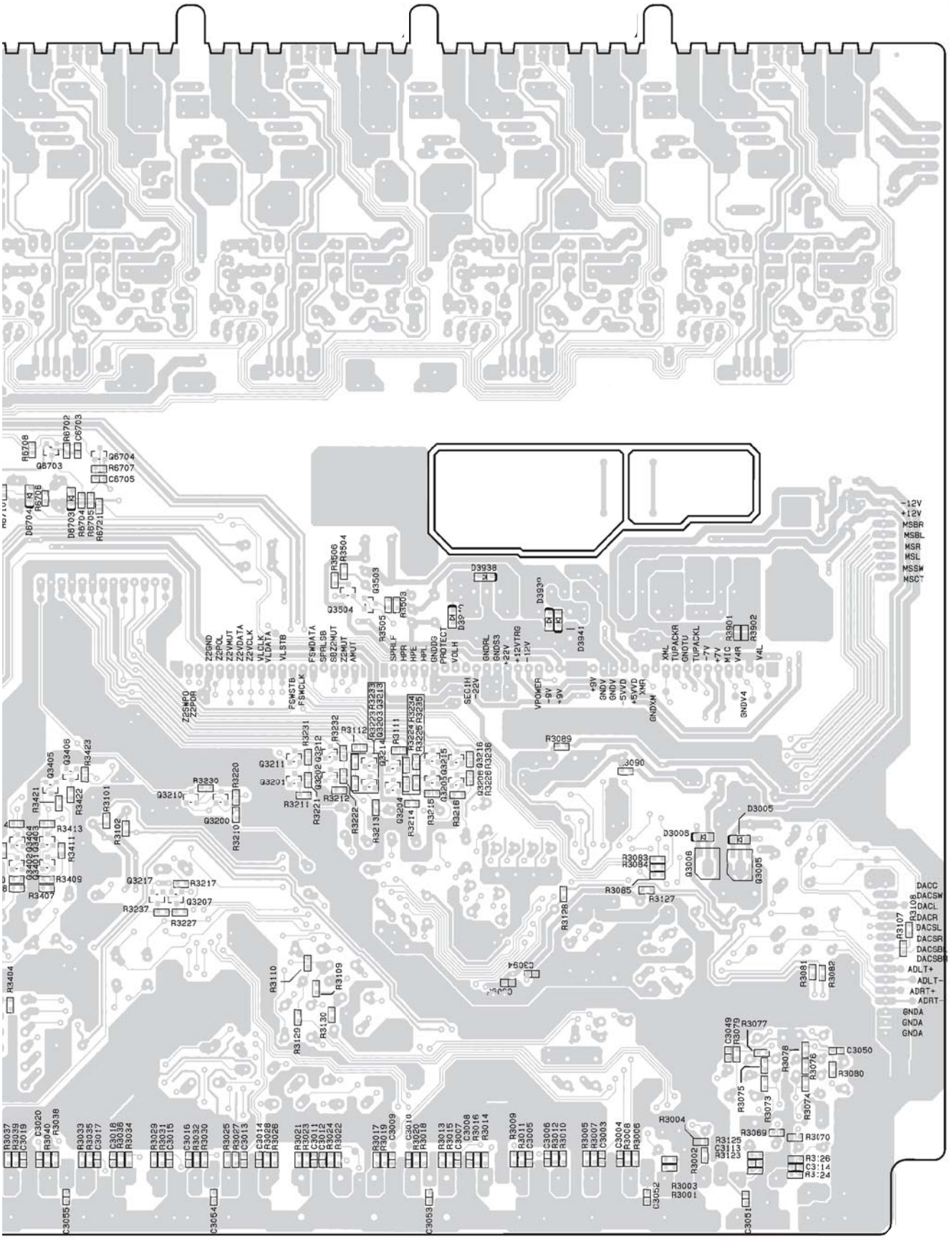
NAETC-8680, Thermal detector PC board

PRINTED CIRCUIT BOARD VIEW 2-2 Amplifier section



NAAF-8678, Power amplifier PC board

PRINTED CIRCUIT BOARD VIEW 2-2 Amplifier section



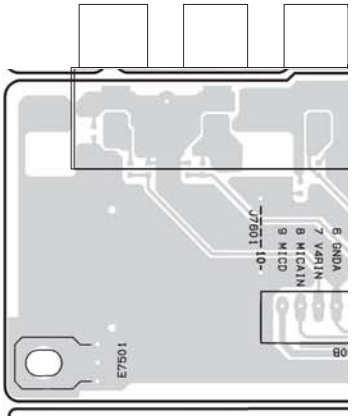
A B C D

1 2 3 4 5

PRINTED CIRCUIT BOARD VIEW 3
DISPLAY SECTION

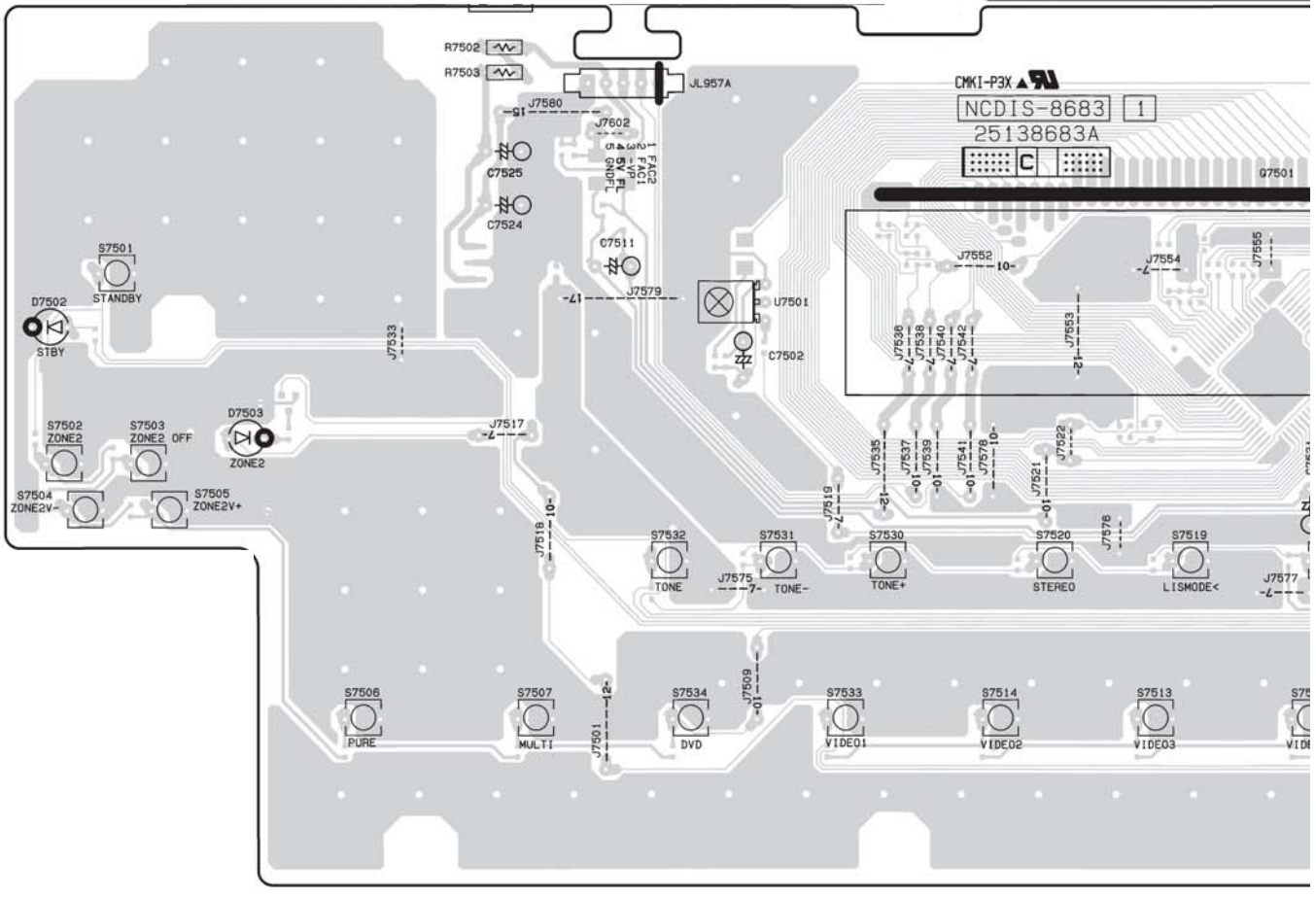
U072

NAETC-8684,
Front video PC b



U07

NADIS-8683,
Display circuit PC board

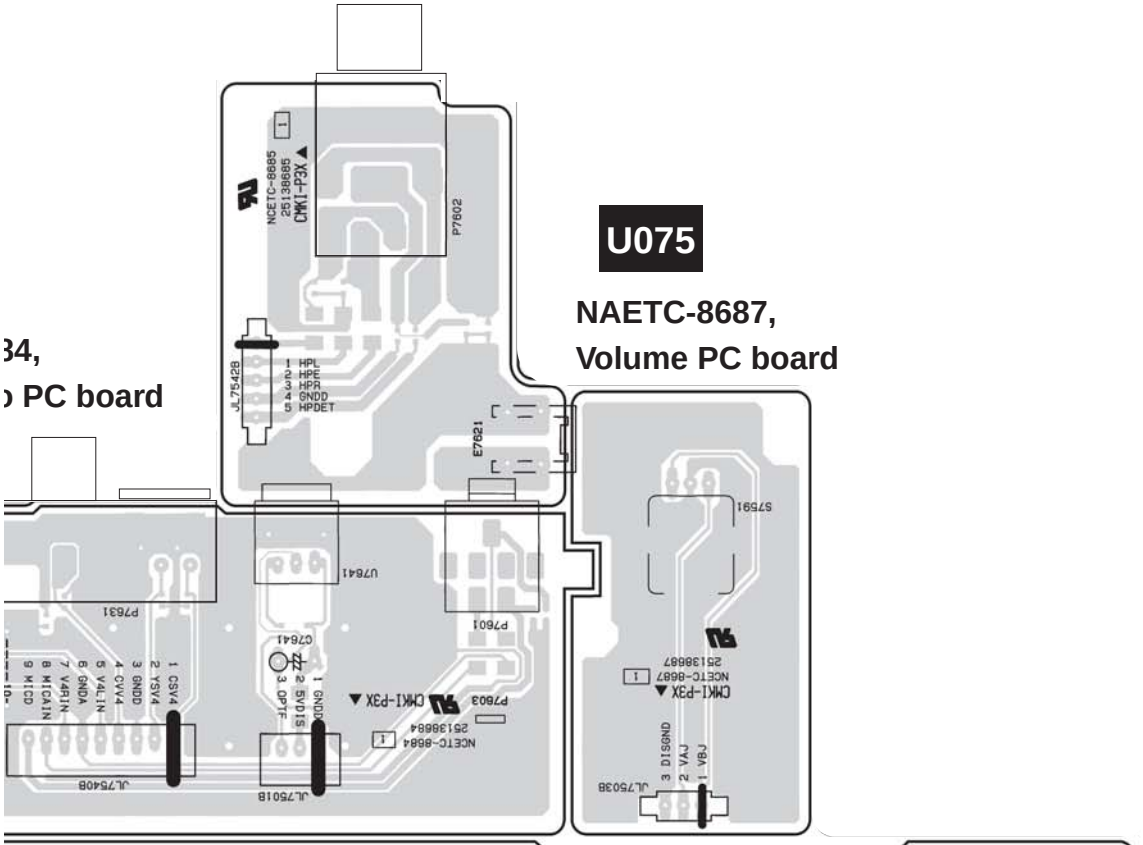


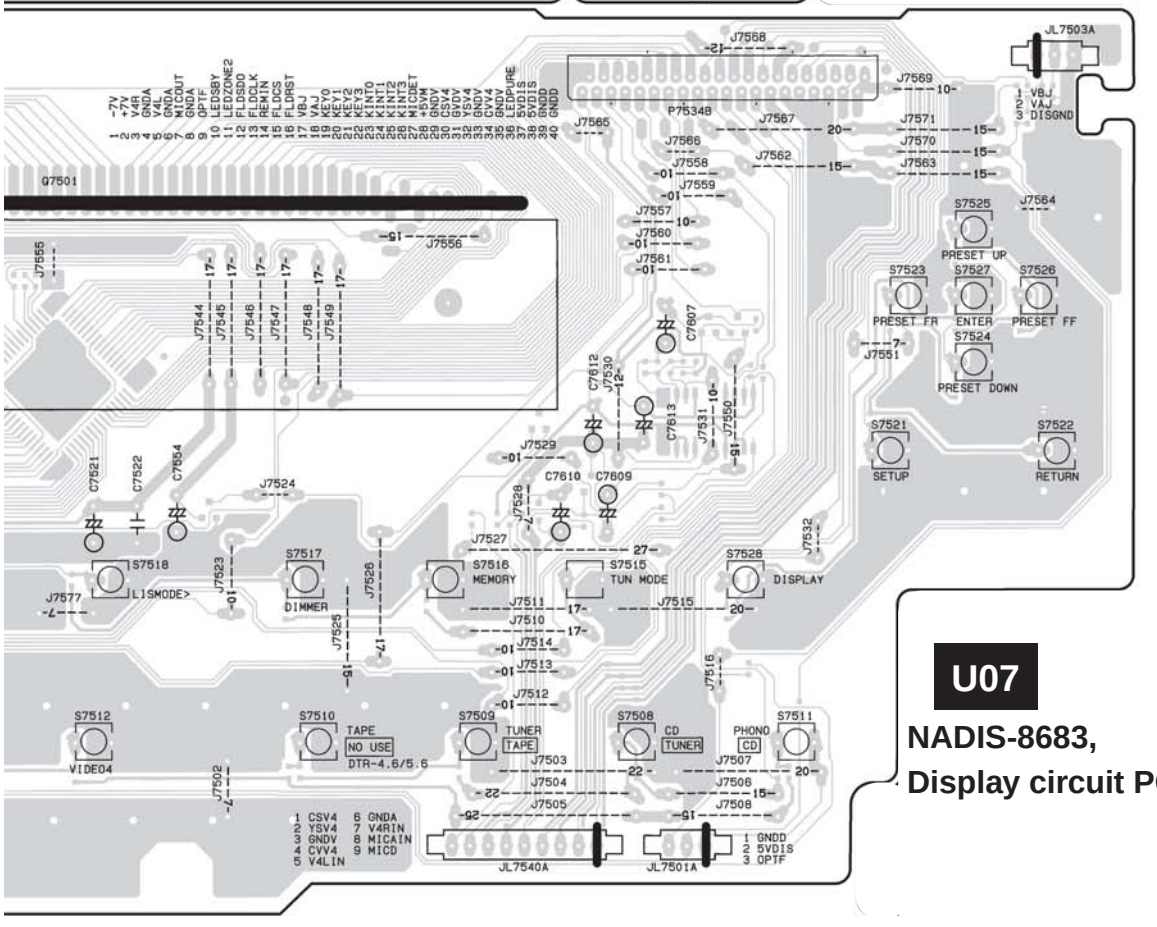
PRINTED CIRCUIT BOARD VIEW 3
DISPLAY SECTION

U073
NAETC-8685,
Headphone terminal PC board

U075
NAETC-8687,
Volume PC board

34,
PC board





U07
NADIS-8683,
Display circuit PC board

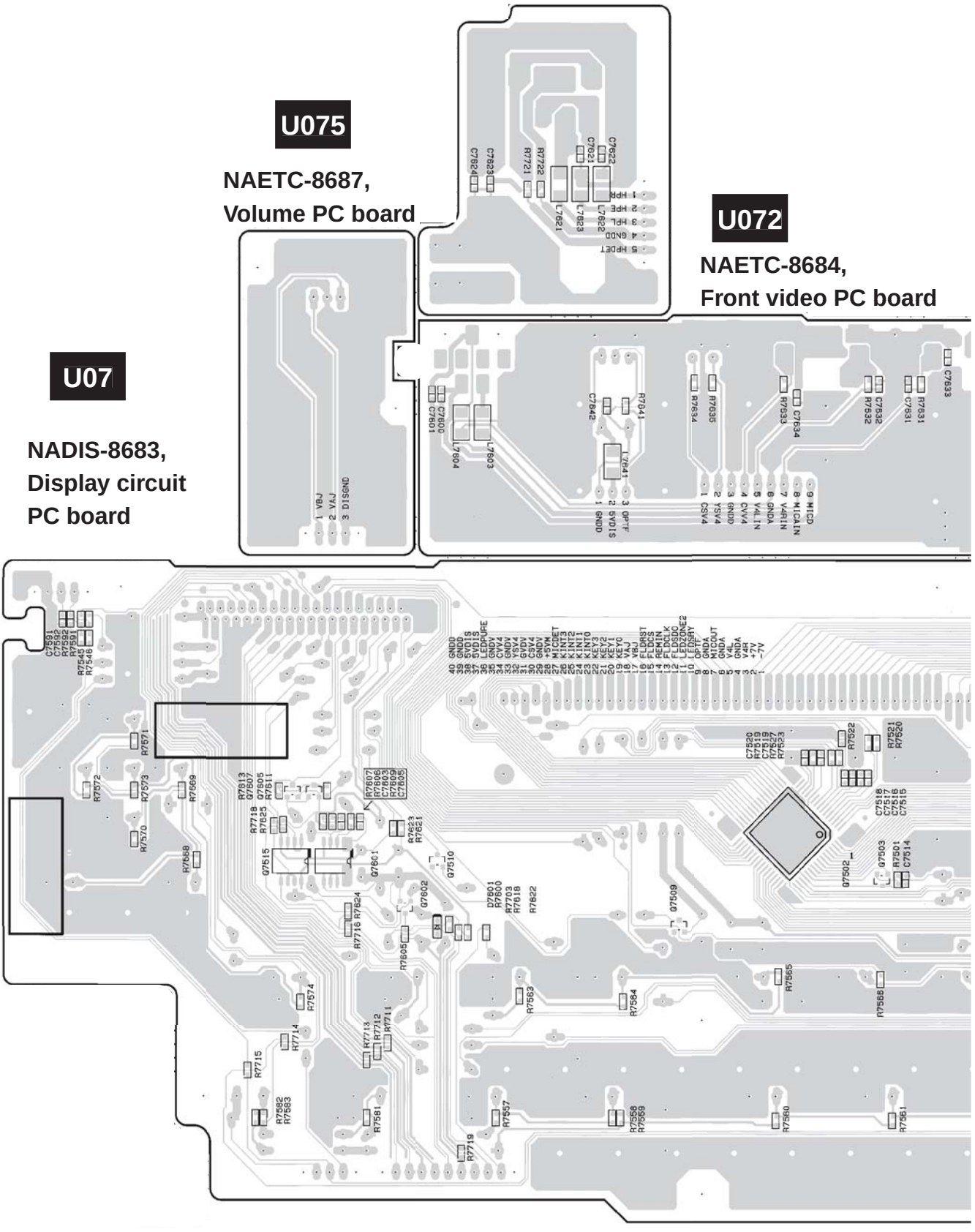
PRINTED CIRCUIT BOARD VIEW 3 DISPLAY SECTION

U073
NAETC-8685,
Headphone terminal
PC board

U075
NAETC-8687,
Volume PC board

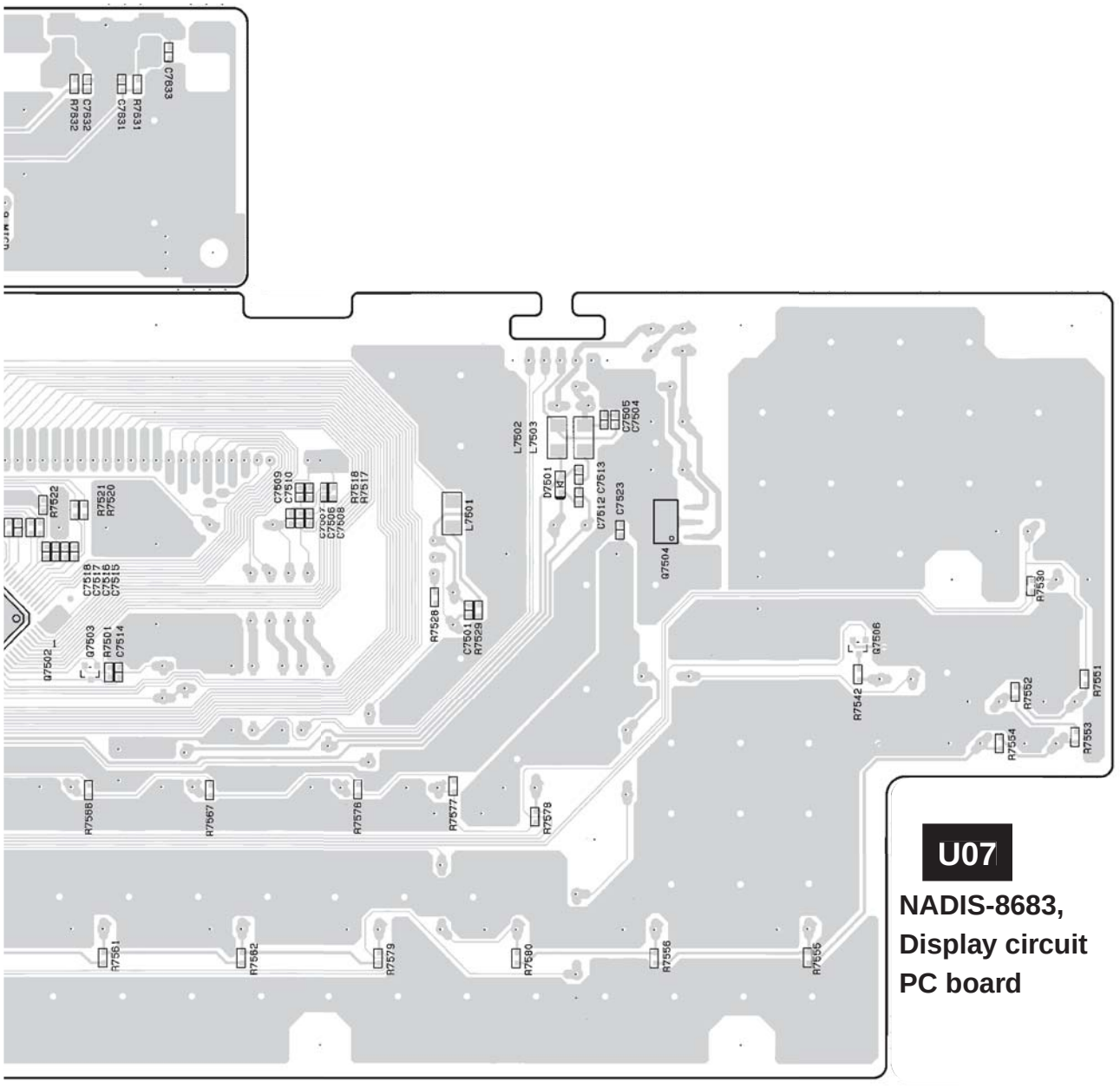
U072
NAETC-8684,
Front video PC board

U07
NADIS-8683,
Display circuit
PC board



PRINTED CIRCUIT BOARD VIEW 3 DISPLAY SECTION

684,
eo PC board



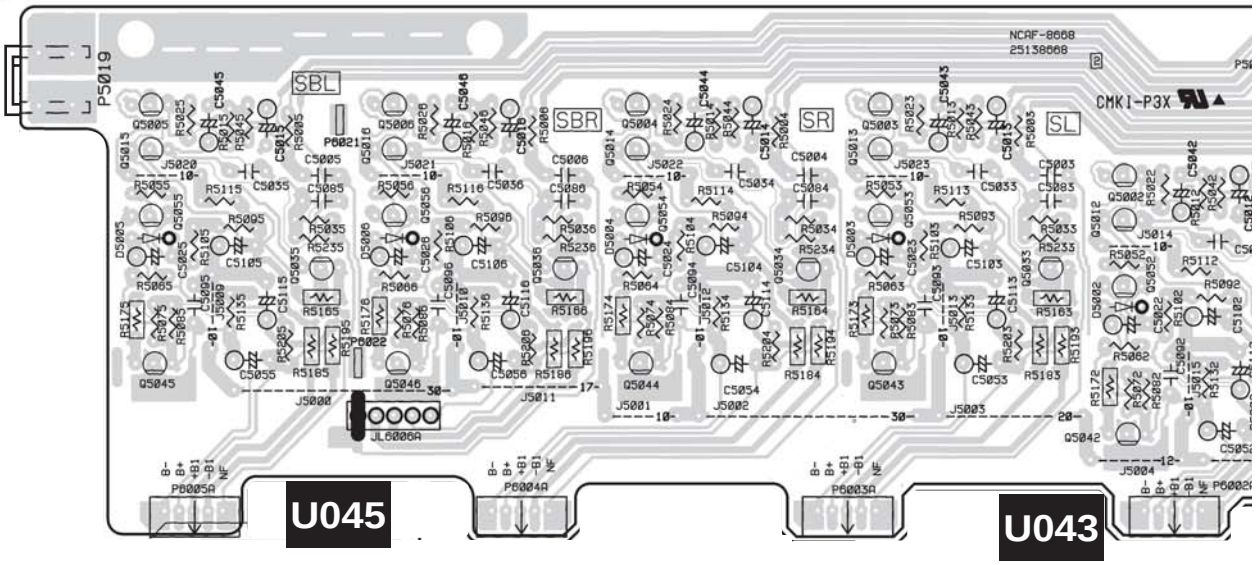
U07

NADIS-8683,
Display circuit
PC board

A B C D

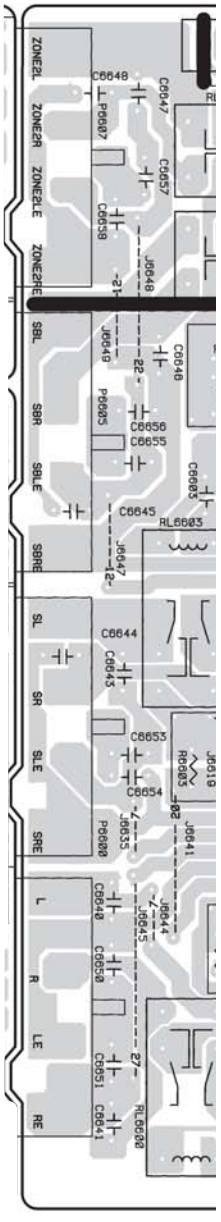
1 2 3 4 5

PRINTED CIRCUIT BOARD VIEW 4 Power supply and Driver sections



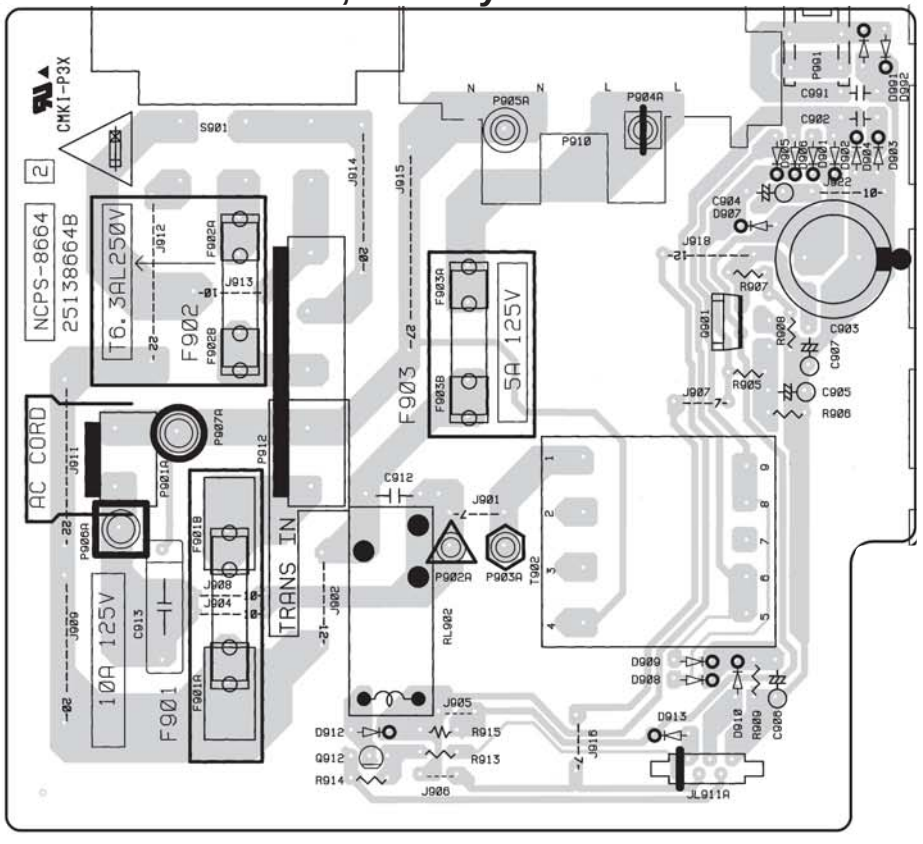
NAAF-8668, Driver circuit PC board

NAETC-8666, Spea

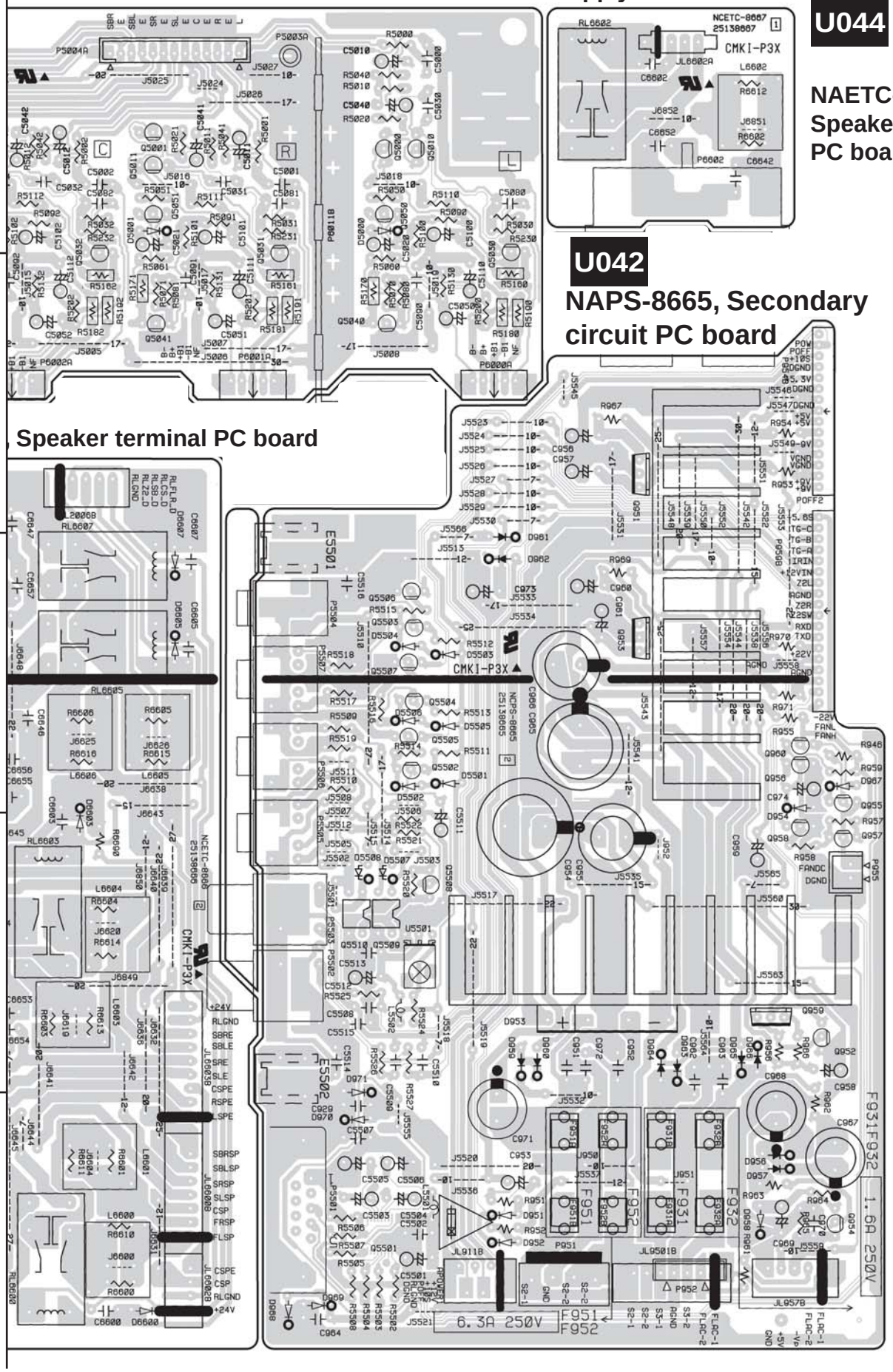


U04

NAPS-8664, Primary circuit PC board



PRINTED CIRCUIT BOARD VIEW 4 Power supply and Driver sections



PRINTED CIRCUIT BOARD VIEW

DIGITAL AND MAIN MICRO-PROCESSOR PC BOARD

U032

NADG-8660, DSP circuit PC board

U03

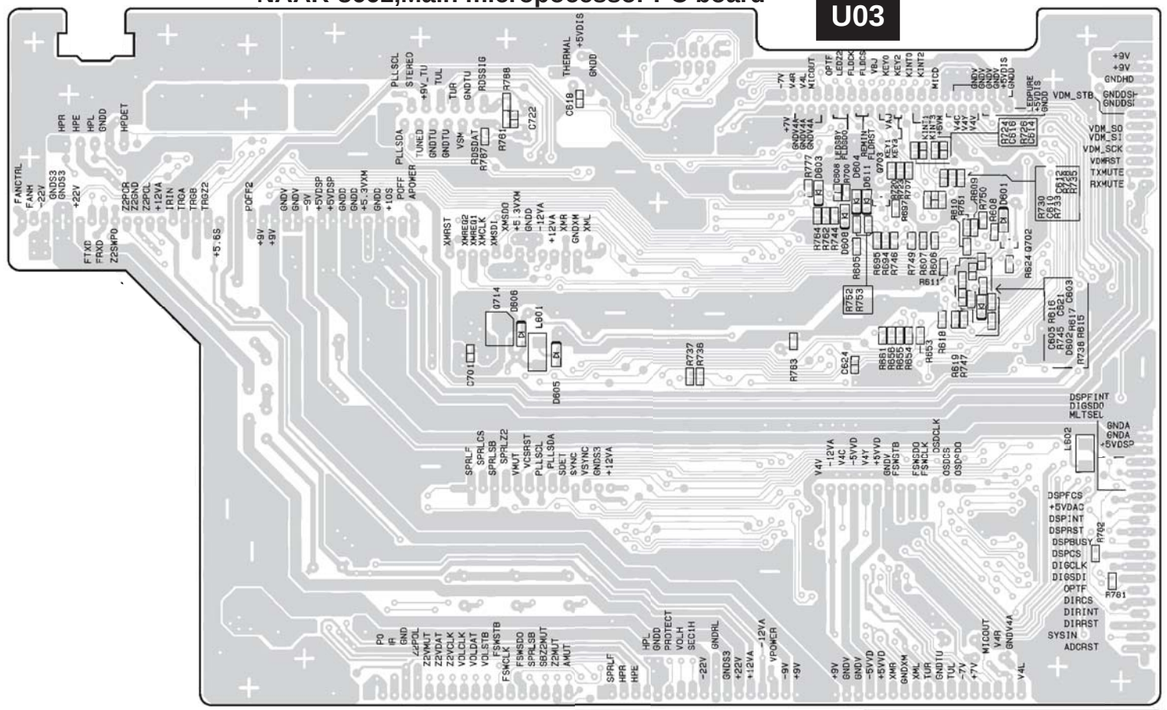
NAAR-8661,Main micropocessor PC board

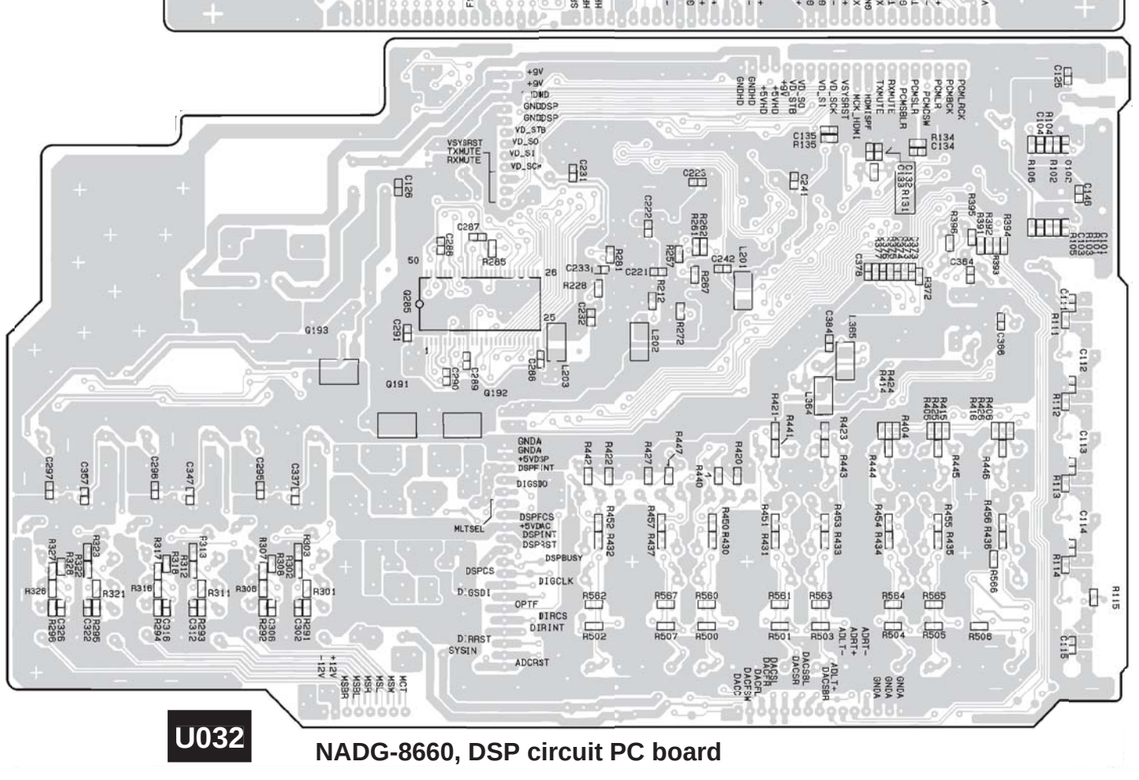
PRINTED CIRCUIT BOARD VIEW

DIGITAL AND MAIN MICRO-PROCESSOR PC BOARD

NAAR-8661,Main micropocessor PC board

U03



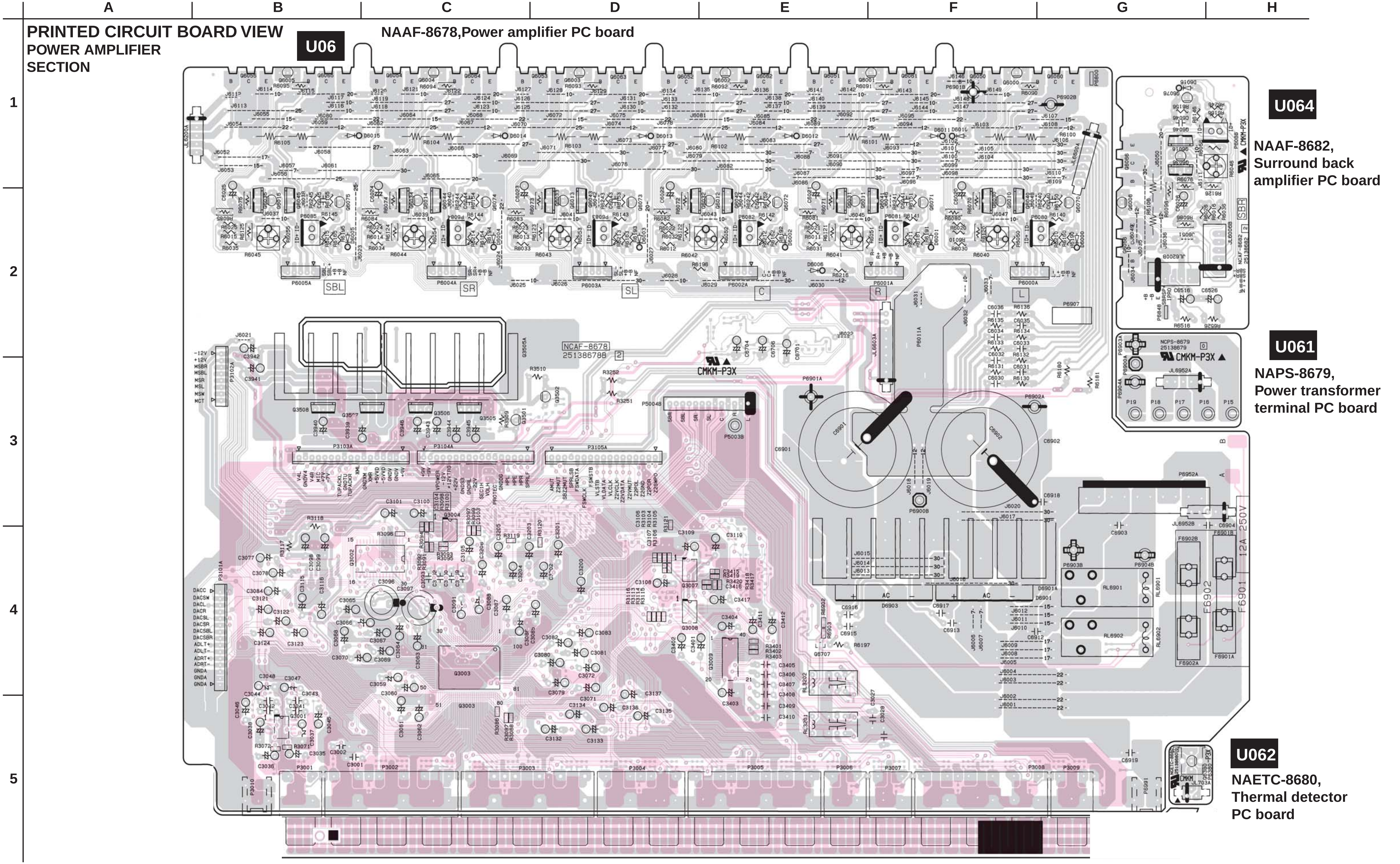


U032

NADG-8660, DSP circuit PC board

PRINTED CIRCUIT BOARD VIEW

POWER AMPLIFIER SECTION



A B C D E F G H

1

2

3

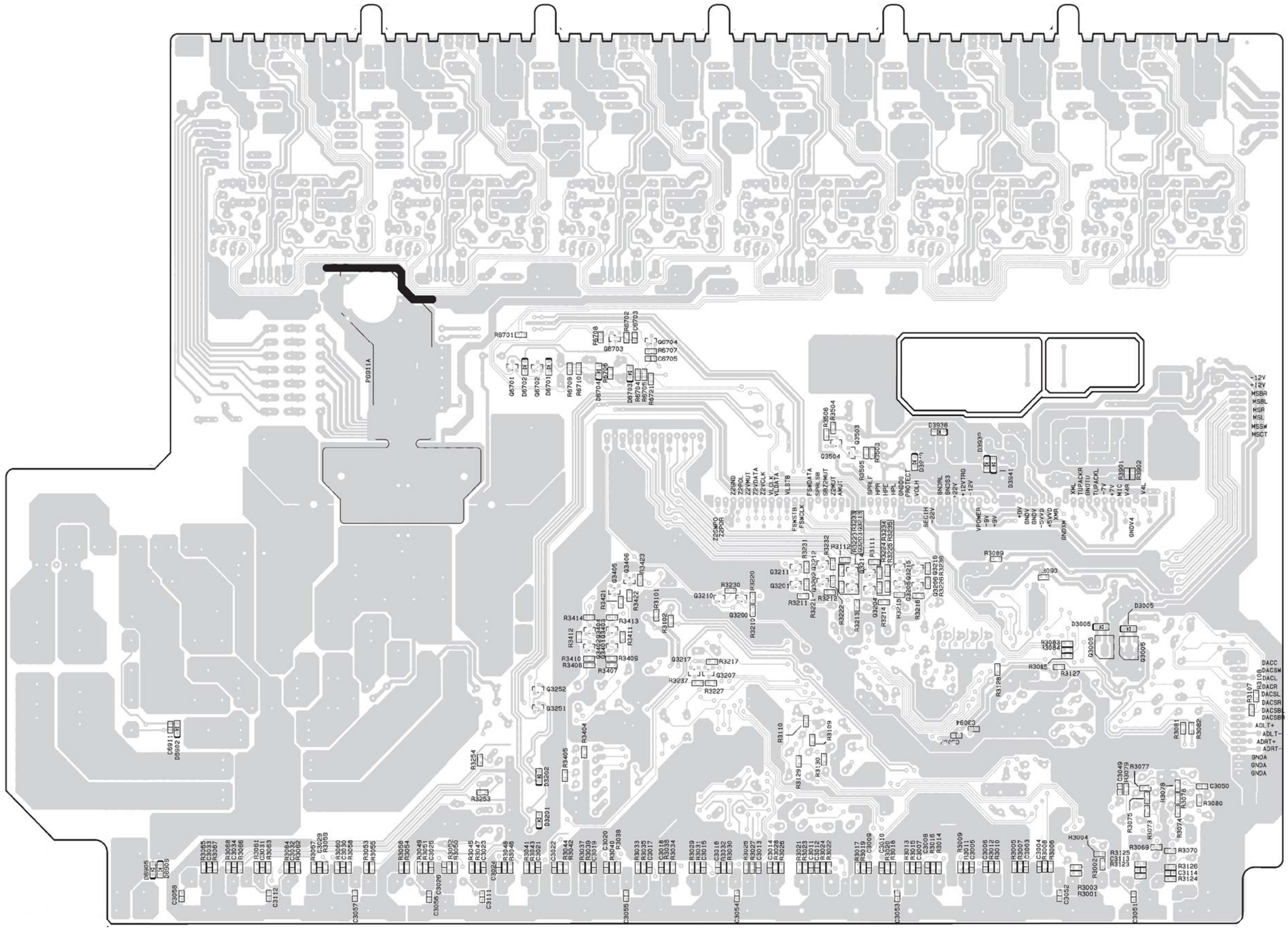
4

5

PRINTED CIRCUIT BOARD VIEW

AMPLIFIER SECTION

PC BOARD



U06

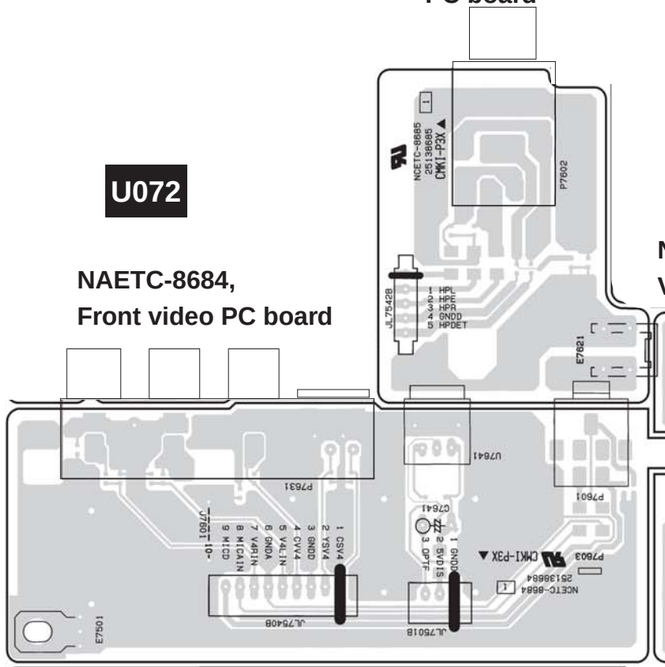
NAAF-8678,Power amplifier PC board

PRINTED CIRCUIT BOARD VIEW

DISPLAY CIRCUIT PC BOARD

U073

NAETC-8685,
Headphone terminal
PC board

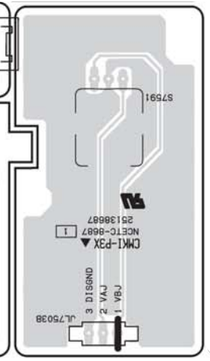


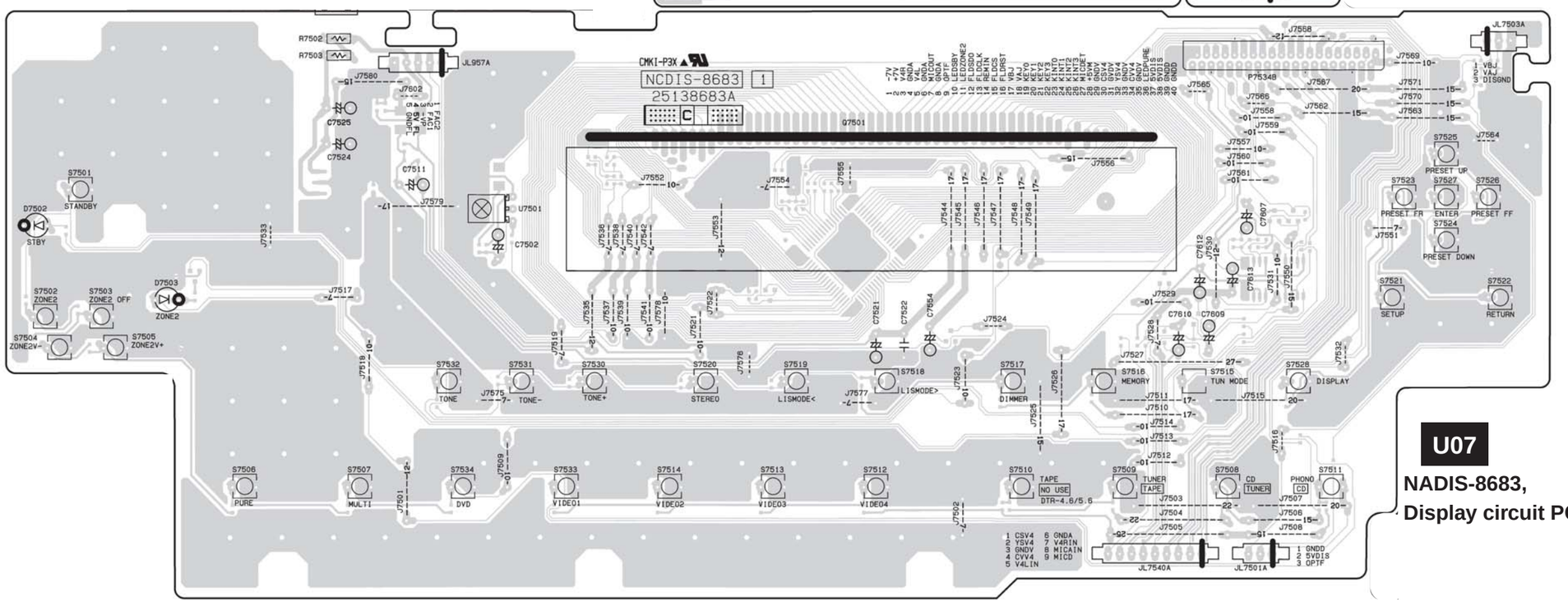
U072

NAETC-8684,
Front video PC board

U075

NAETC-8687,
Volume PC board





U07

NADIS-8683,
Display circuit PC board

A B C D E F G H

1 2 3 4 5

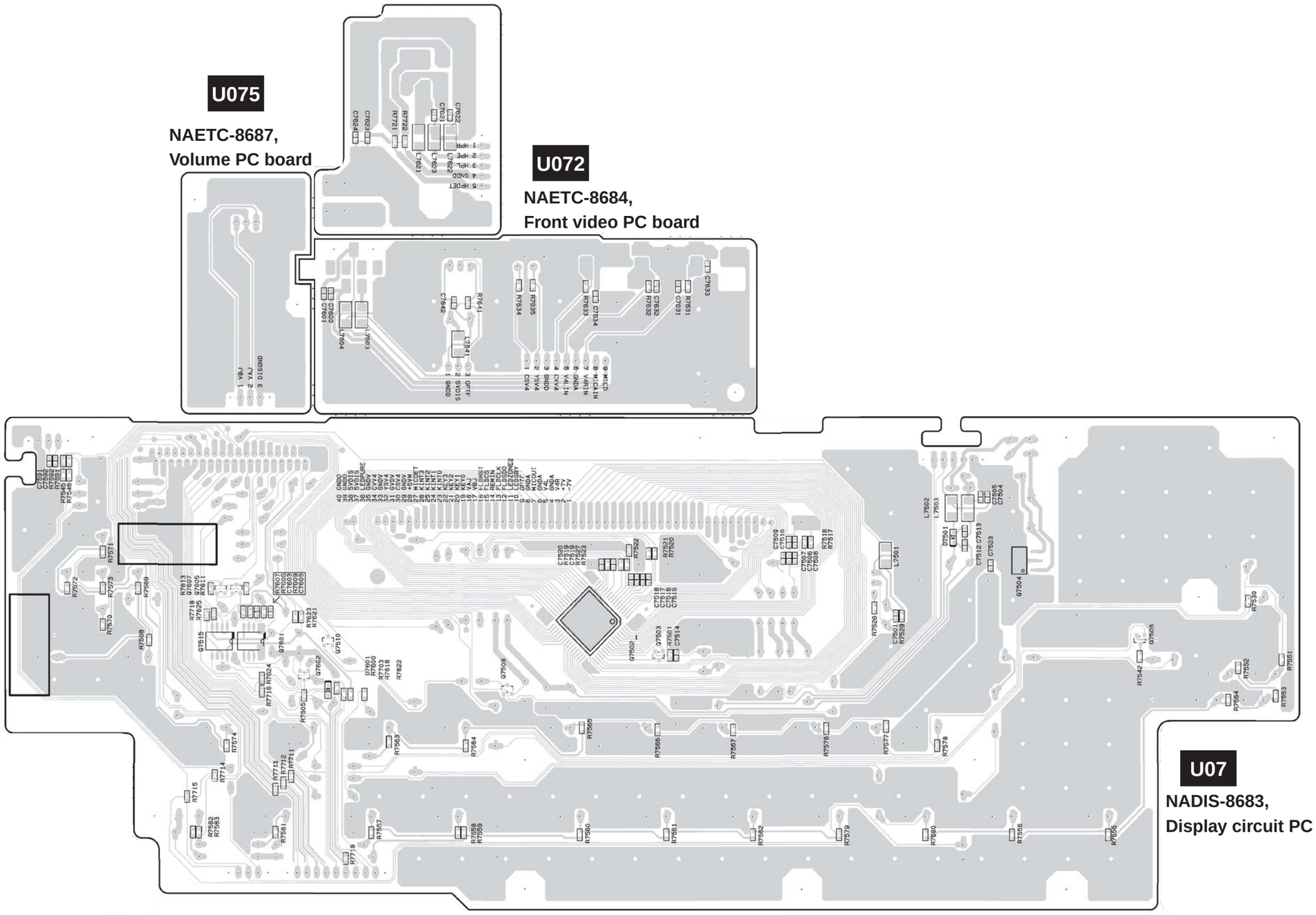
PRINTED CIRCUIT BOARD VIEW

DISPLAY CIRCUIT PC BOARD

U073
NAETC-8685,
Headphone terminal
PC board

U075
NAETC-8687,
Volume PC board

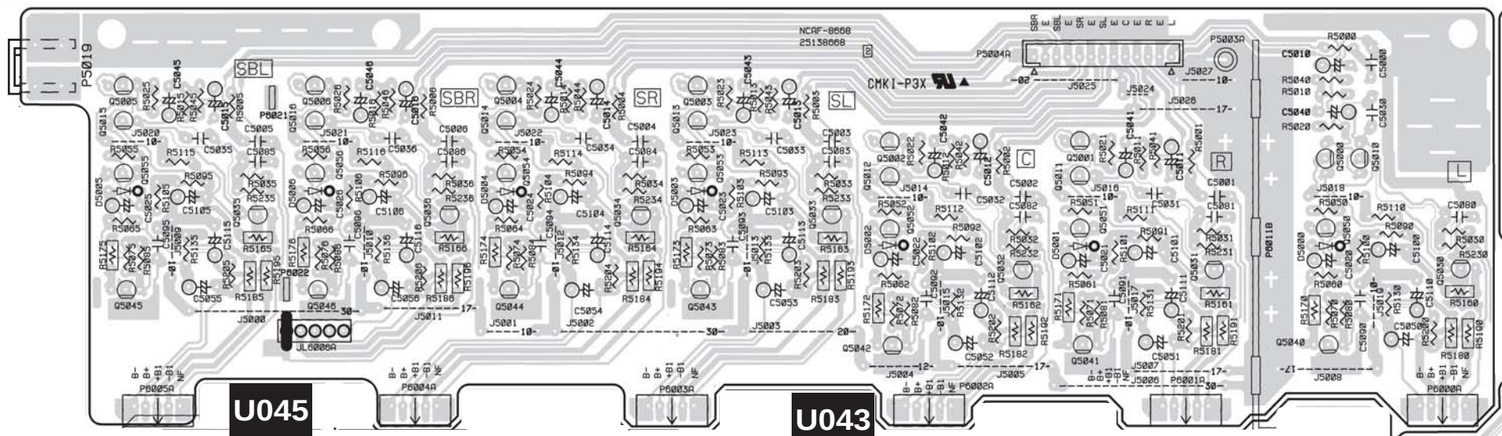
U072
NAETC-8684,
Front video PC board



U07
NADIS-8683,
Display circuit PC board

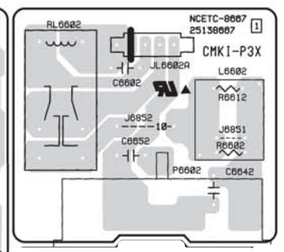
PRINTED CIRCUIT BOARD VIEW

Power supply and Driver sections



U045

NAAF-8668, Driver circuit PC board

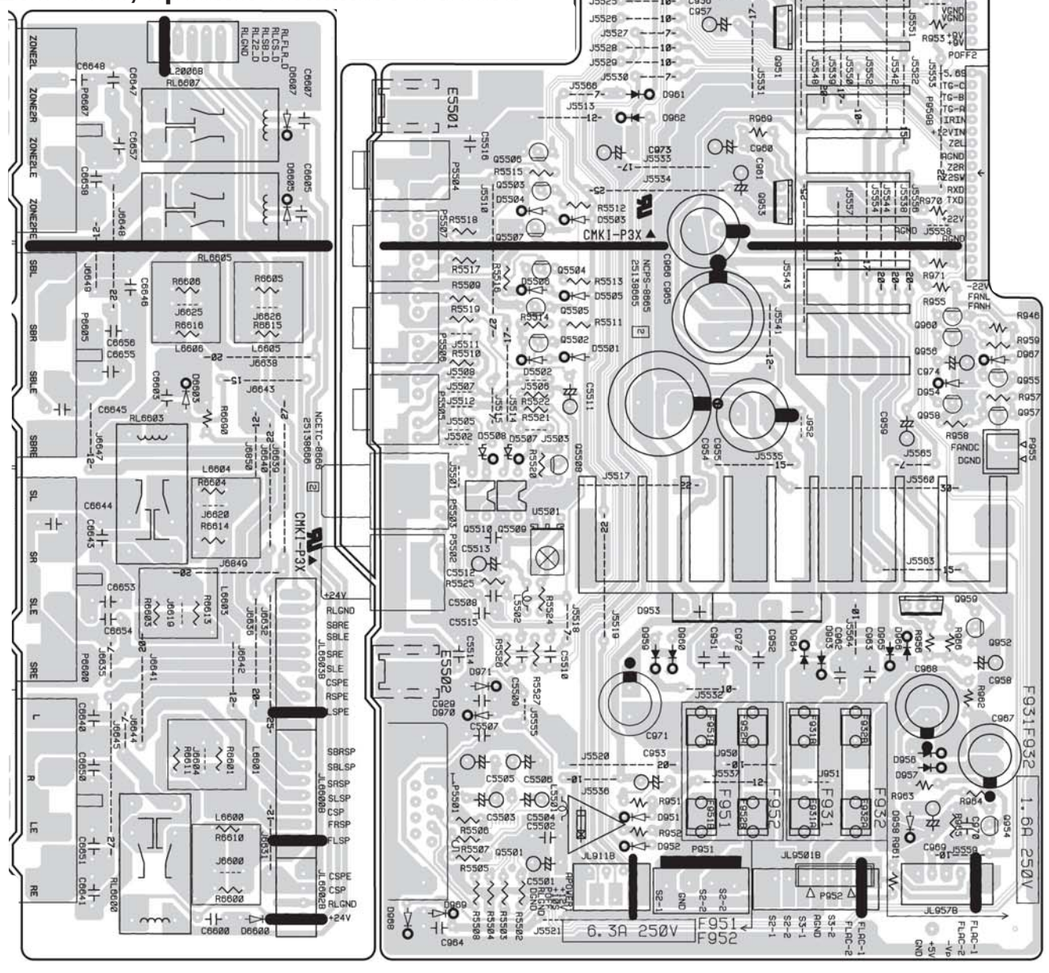


U044

NAETC-8667, Speaker terminal C PC board

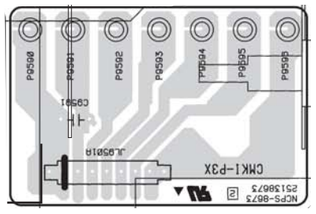
U042

NAPS-8665, Secondary circuit PC board



U043

NAETC-8666, Speaker terminal PC board

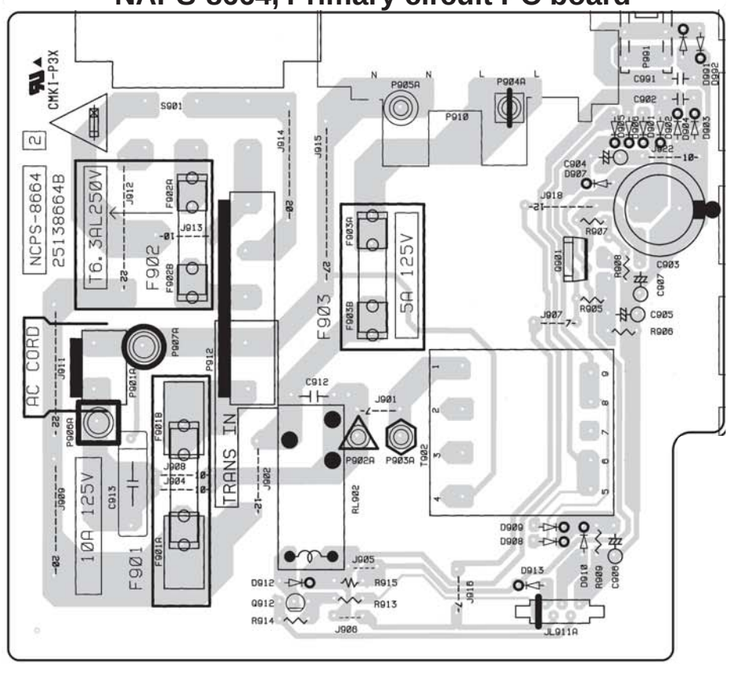


U049

NAETC-8673, Transfomer terminal PC board

U04

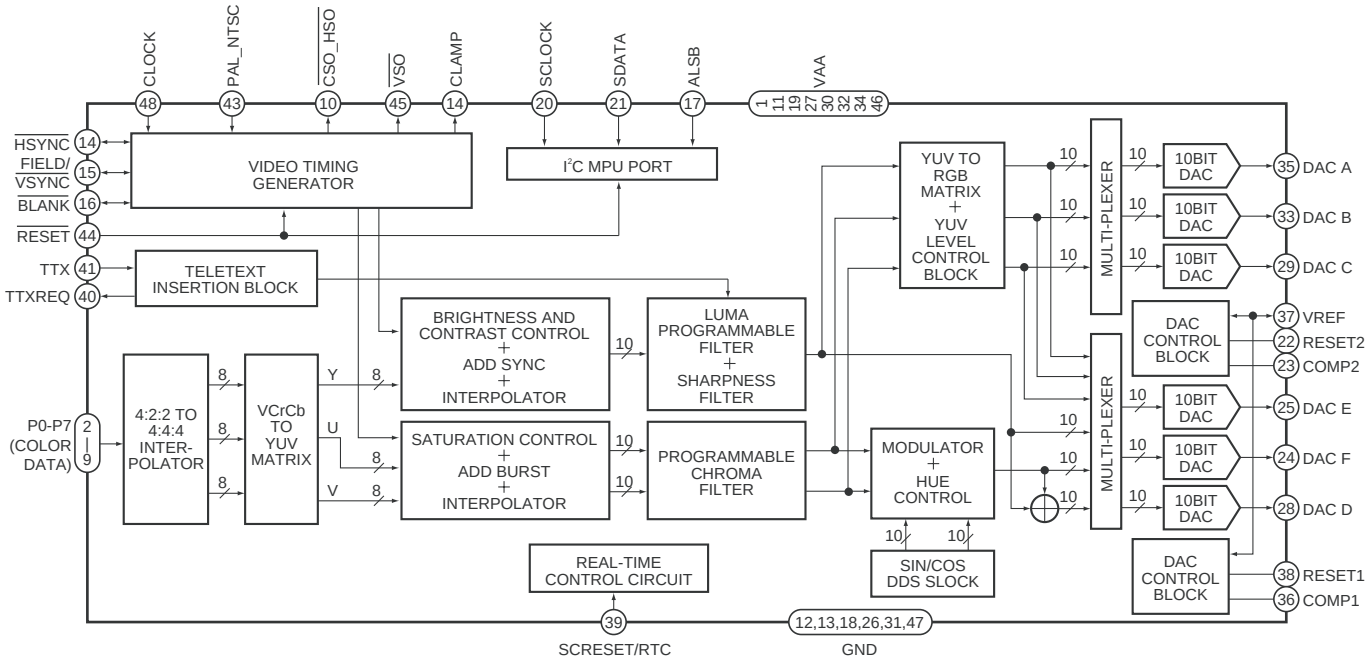
NAPS-8664, Primary circuit PC board



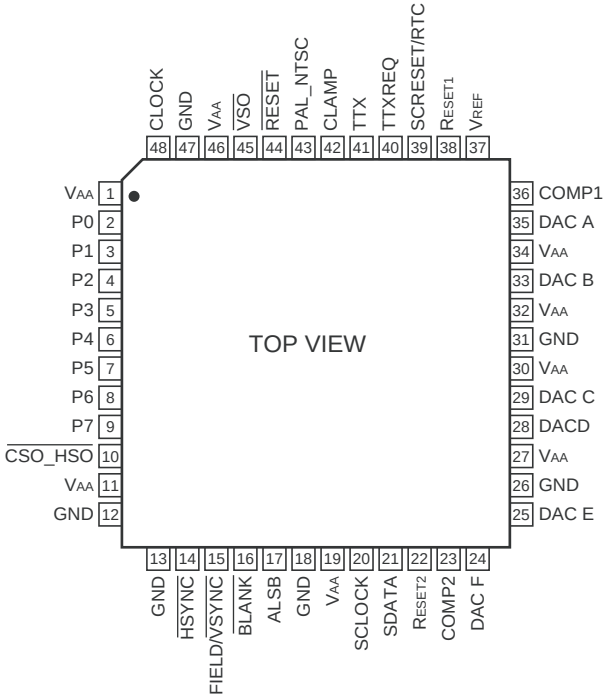
IC BLOCK DIAGRAMS AND DESCRIPTIONS

ADV7172 (Digital PAL/NTSC Video Encoder with Six DACs (10-Bits))

BLOCK DIAGRAM



PIN LAYOUT



IC BLOCK DIAGRAMS AND DESCRIPTIONS

ADV7172 (Digital PAL/NTSC Video Encoder with Six DACs (10-Bits))

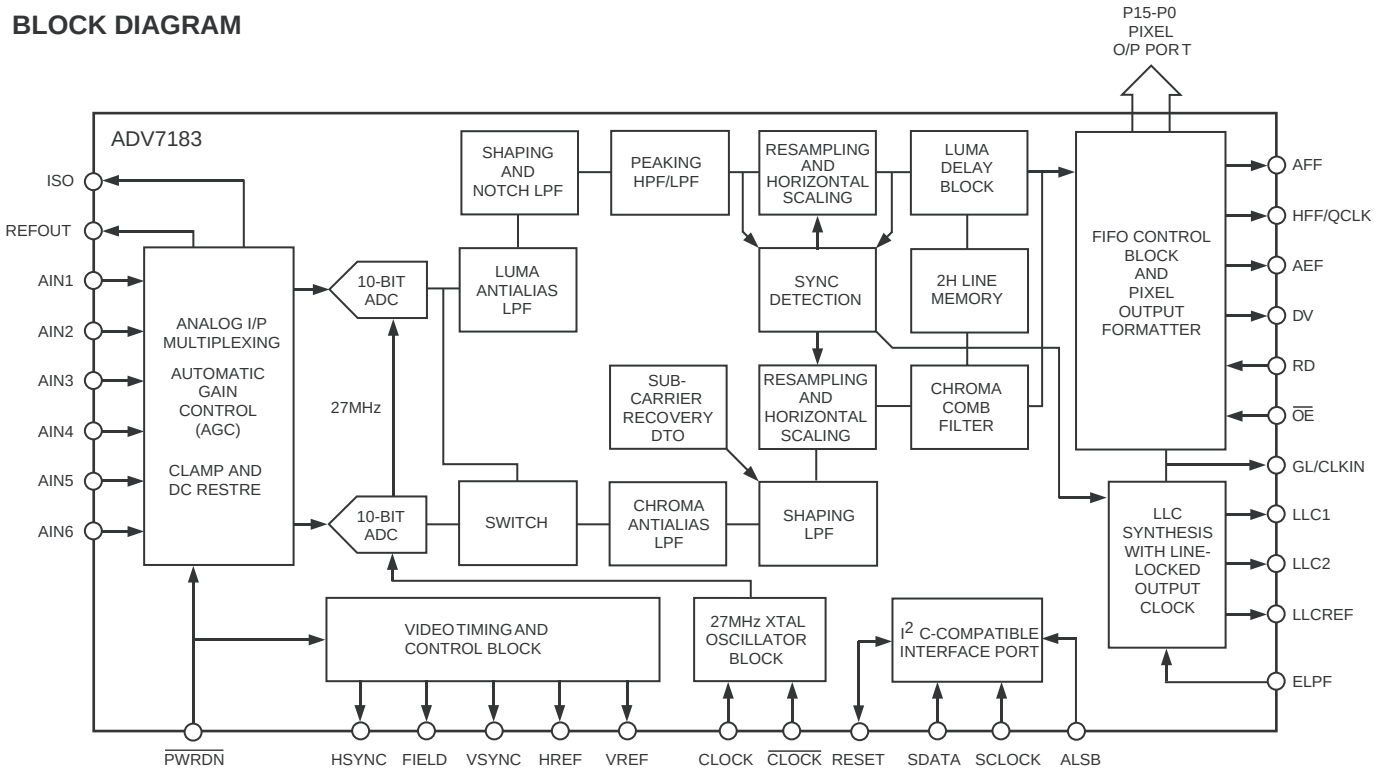
TERMINAL DESCRIPTION

No.	Name	I/O	Description
9-2	P7-P0	I	8-Bit 4:2:2 Multiplexed YCrCb Pixel Port (P7-P0) P0 represents the LSB.
48	CLOCK	I	TTL Clock Input. Requires a stable 27 MHz reference clock for standard operation. Alternatively, a 24.5454 MHz (NTSC) or 29.5 MHz (PAL) can be used for square pixel operation.
14	$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1 and 2) Control Signal. This pin may be configured to output (Master Mode) or as an input and accept (Slave Mode) Sync signals.
15	FIELD/$\overline{\text{VSYNC}}$	I/O	Dual Function FIELD (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin may be configured to output (Master Mode) or as an input (Slave Mode) and accept these control signals.
16	$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is Logic Level "0" This signal is optional.
39	SCRESET/RTC	I	This pin can be configured as an input by setting MR42 and MR41 of Mode Register 4. It can be configured as a subcarrier reset pin, in which case a low-to-high transition on this pin will reset the subcarrier phase to Field 0. Alternatively it may be configured as a Real-Time Control (RTC) Input.
37	V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
38	R_{SET1}	I	A 150 ohms resistor connected from this pin to GND is used to control full-scale amplitudes the Video Signals from DACs A, B, and C (the "large" DACs).
22	R_{SET2}	I	A 600 ohms resistor connected from this pin to GND is used to control full-scale amplitudes the Video Signals from DACs D, E, and F (the "small" DACs).
36	COMP1	O	Compensation Pin for DACs A, B, and C. Connect a 0.1 uF Capacitor from COMP to V_{AA}. For Optimum Dynamic Performance in Low Power Mode, the value of the COMP1 capacitor can be lowered to as low as 2.2 nF.
23	COMP2	O	Compensation Pin for DACs D, E, and F. Connect a 0.1 uF Capacitor from COMP to V_{AA}.
35	DAC A	O	GREEN/Composite/Y Analog Output. This DAC is capable of providing 34.66 mA output.
33	DAC B	O	BLUE/S-Video Y/U Analog Output. This DAC is capable of providing 34.66 mA output.
29	DAC C	O	RED/S-Video C/V Analog Output. This DAC is capable of providing 34.66 mA output.
28	DAC D	O	GREEN/Composite/Y Analog Output. This DAC is capable of providing 8.66 mA output.
25	DAC E	O	BLUE/S-Video Y/U Analog Output. This DAC is capable of providing 8.66 mA output.
24	DAC F	O	RED/S-Video C/V Analog Output. This DAC is capable of providing 8.66 mA output.
20	SCLOCK	I	MPU Port Serial Interface Clock Input.
21	SDATA	I/O	MPU Port Serial Data Input/Output.
42	CLAMP	O	TTL Output Signal to external circuitry to enable clamping of all video signals.
43	PAL_NTSC	I	Input signal to select PAL or NTSC mode of operation, pin set to Logic "1" selects PAL.
45	$\overline{\text{VSO}}$	O	$\overline{\text{VSO}}$ TTL Output Sync Signal.
10	$\overline{\text{CSO\_HSO}}$	O	Dual Function $\overline{\text{CSO}}$ or $\overline{\text{HSO}}$ TTL Output Sync Signal.
17	ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address.
44	$\overline{\text{RESET}}$	I	The input resets the on-chip timing generator and sets the ADV7172/ADV7173 into default mode. This is NTSC operation, Timing Slave Mode 0, DACs A, B, and C powered OFF, DACs D, E, and F powered ON, Composite and S-Video out.
41	TTX	I	Teletext Data Input Pin.
40	TTXREQ	O	Teletext Data Request output signal used to control teletext data transfer.
1, 11, 19, 27, 30, 32, 34, 46	V_{AA}	P	Power Supply (3 V to 5 V).
12, 13, 18, 26, 31, 47	GND	G	Ground Pin.

IC BLOCK DIAGRAMS AND DESCRIPTIONS

ADV7183 (Advanced Video Decoder with 10-Bit ADC and Component Support)

BLOCK DIAGRAM



TERMINAL DESCRIPTION

Pin	Mnemonic	Input/Output	Function
1	VS/VACTIVE	O	VS or Vertical Sync. A dual-function pin, (OM_SEL[1:0] = 0, 0) is an output signal that indicates a vertical sync with respect to the YUV pixel data. The active period of this signal is six lines of video long. The polarity of the VS signal is controlled by the PVS bit. VACTIVE (OM_SEL[1:0] = 1, 0 or 0, 1) is an output signal that is active during the active/viewable period of a video field. The polarity of VACTIVE is controlled by PVS bit.
2	HS/HACTIVE	O	HS or Horizontal Sync. A dual-function pin, (OM_SEL[1:0] = 0, 0) is a programmable horizontal sync output signal. The rising and falling edges can be controlled by HSB[9:0] and HSE[9:0] in steps of 2 LLC1. The polarity of the HS signal is controlled by the PHS bit. HACTIVE (OM_SEL[1:0]= 1, 0 or 0, 1) is an output signal that is active during the active/viewable period of a video line. The active portion of a video line is programmable on the ADV7183. The polarity of HACTIVE is controlled by PHS bit.
3, 14	DVSSIO	G	Digital I/O Ground
4, 15	DVDDIO	P	Digital I/O Supply Voltage (3.3 V)
5-8, 19-24, 32, 33, 73-76	P15-P0	O	Video Pixel Output Port. 8-bit multiplexed YCrCb pixel port (P15-P8), 16-bit YCrCb pixel port (P15-P8 = Y and P7-P0 = Cb,Cr).
9, 31, 71	DVSS1-3	G	Ground for Digital Supply
10, 30, 72	DVDD1-3	P	Digital Supply Voltage (3.3 V)
11	AFF	O	Almost Full Flag. A FIFO control signal indicating when the FIFO has reached the almost full margin set by the user (use FFM[4:0]). The polarity of this signal is controlled by the PFF bit.
12	HFF/QCLK/GL	I/O	Half Full Flag. A multifunction pin, (OM_SEL[1:0] = 1, 0) is a FIFO control signal that indicates when the FIFO is half full. The QCLK (OM_SEL[1:0] = 0, 1) pin function is a qualified pixel output clock when using FIFO SCAPI mode. The GL (OM_SEL[1:0] = 0, 0) function (Genlock output) is a signal that contains a serial stream of data that contains information for locking the subcarrier frequency. The polarity of HFF signal is controlled by PFF bit.
13	AEF	O	Almost Empty Flag. A FIFO control signal, it indicates when the FIFO has reached the almost empty margin set by the user (use FFM[4:0]). The polarity of this signal is controlled by PFF bit.
16	CLKIN	I	Asynchronous FIFO Clock. This asynchronous clock is used to output data onto the P19-P0 bus and other control signals.
17, 18, 34, 35	GPO[3:0]	O	General-Purpose Outputs controlled via I^2C

IC BLOCK DIAGRAMS AND DESCRIPTIONS

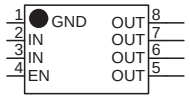
ADV7183 (Advanced Video Decoder with 10-Bit ADC and Component Support)

TERMINAL DESCRIPTION

Pin	Mnemonic	Input/Output	Function
25	LLCREF	O	Clock Reference Output. This is a clock qualifier distributed by the internal CGC for a data rate of LLC2. The polarity of LLCREF is controlled by the PLLCREF bit.
26	LLC2	O	Line-Locked Clock System Output Clock/2 (13.5 MHz)
27	LLC1/PCLK	O	Line-Locked Clock System Output Clock. A dual-function pin (27 MHz ± 5%) or a FIFO output clock ranging from 20 MHz to 35 MHz.
28	XTAL1	O	Second terminal for crystal oscillator; not connected if external clock source is used.
29	XTAL	I	Input terminal for 27MHz crystal oscillator or connection for external oscillator with CMOS-compatible square wave clock signal
36	$\overline{\text{PWRDN}}$	I	Power-Down Enable. A logical low will place part in a power-down status.
37	ELPF	I	This pin is used for the External Loop Filter that is required for the LLC PLL.
38	PVDD	P	
39	PVSS	G	
40, 47, 53, 56, 63	AVSS	G	Ground for Analog Supply
41, 43, 45, 57, 59, 61	AVSS1-6	G	Analog Input Channels. Ground if single-ended mode is selected. These pins should be connected directly to REFOUT when differential mode is selected.
42, 44, 46, 58, 60, 62	AIN1-6	I	Video Analog Input Channels
48, 49	CAPY1-2	I	ADC Capacitor Network
50	AVDD	P	Analog Supply Voltage (5 V)
51	REFOUT	O	Internal Voltage Reference Output
52	CML	O	Common-Mode Level for ADC
54, 55	CAPC1-2	I	ADC Capacitor Network
64	$\overline{\text{RESET}}$	I/O	System Reset Input. Active Low.
65	ISO	I	Input Switch Over. A low to high transition on this input indicates to the decoder core that the input video source has been changed externally and configures the decoder to reacquire the new timing information of the new source. This is useful in applications where external video muxes are used. This input gives the advantage of faster locking to the external muxed video sources. A low to high transition triggers this input.
66	ALSB	I	TTL Address Input. Selects the MPU address: MPU address = 88h ALSB = 0, disables I^2C filter MPU address = 8Ah ALSB = 1, enables I^2C filter
67	SDATA	I/O	MPU Port Serial Data Input/Output
68	SCLK	I	MPU Port Serial Interface Clock Input
69	VREF/$\overline{\text{VRESET}}$	O	VREF or Vertical Reference Output Signal. Indicates start of next field. $\overline{\text{VRESET}}$ or Vertical Reset Output is a signal that indicates the beginning of a new field. In SCAPI/CAPI mode this signal is one clock wide and active low relative to CLKIN. It immediately follows the $\overline{\text{HRESET}}$ pixel, and indicates that the next active pixel is the first active pixel of the next field.
70	HREF/$\overline{\text{HRESET}}$	O	HREF or Horizontal Reference Output Signal. A dual-function pin (enabled when Line-Locked Interface is selected, OM_SEL[1:0] = 0,0), this signal is used to indicate data on the YUV output. The positive slope indicates the beginning of a new active line; HREF is always 720 Y samples long. $\overline{\text{HRESET}}$ or Horizontal Reset Output (enabled when SCAPI or CAPI is selected, OM_SEL[1:0] = 0, 1 or 1, 0) is a signal that indicates the beginning of a new line of video. In SCAPI/CAPI this signal is one clock cycle wide and is output relative to CLKIN. It immediately follows the last active pixel of a line. The polarity is controlled via PHVR.
77	RD	I	Asynchronous FIFO Read Enable Signal. A logical high on this pin enables a read from the output of the FIFO.
78	DV	O	DV or Data Valid Output Signal. In SCAPI/CAPI mode, DV performs to functions, depending on whether SCAPI or CAPI is selected. It toggles high when the FIFO has reached the AFF margin set by the user, and remains high until the FIFO is empty. The alternative mode is where it can be used to control FIFO reads for bursting information out of the FIFO. In API mode DV indicates valid data in the FIFO, which includes both pixel information and control codes. The polarity of this pin is controlled via PDV.
79	OE	I	Output Enable Controls Pixel Port Outputs. A logic high will three-state P19-P0.
80	FIELD	O	ODD/EVEN Field Output Signal. An active state indicates that an even field is being digitized. The polarity of this signal is controlled by the PF bit.

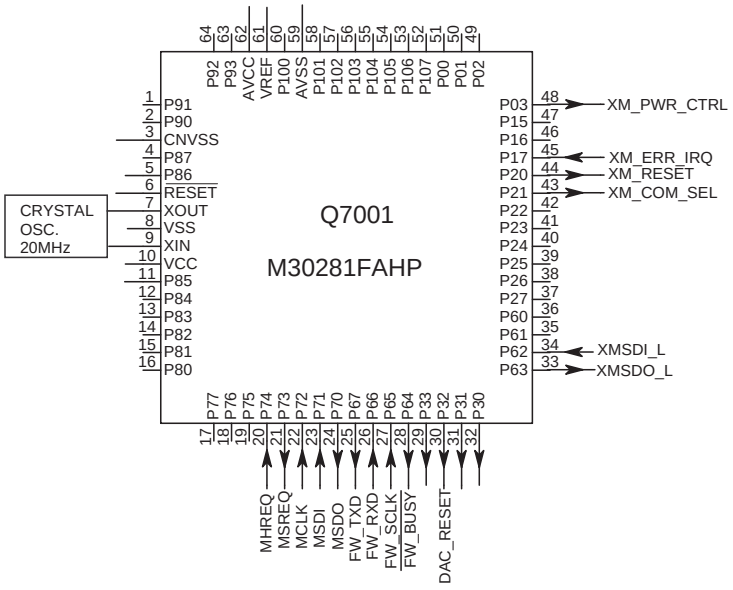
IC BLOCK DIAGRAMS AND DESCRIPTIONS(XM radio only)

TPS2012AD/MAX1930ESA(POWER-DISTRIBUTION)



1	EN	Enable input. Logic low turns power switch on.
2,3	IN	Input voltage
4	GND	Ground
5~8	OUT	Power switch output

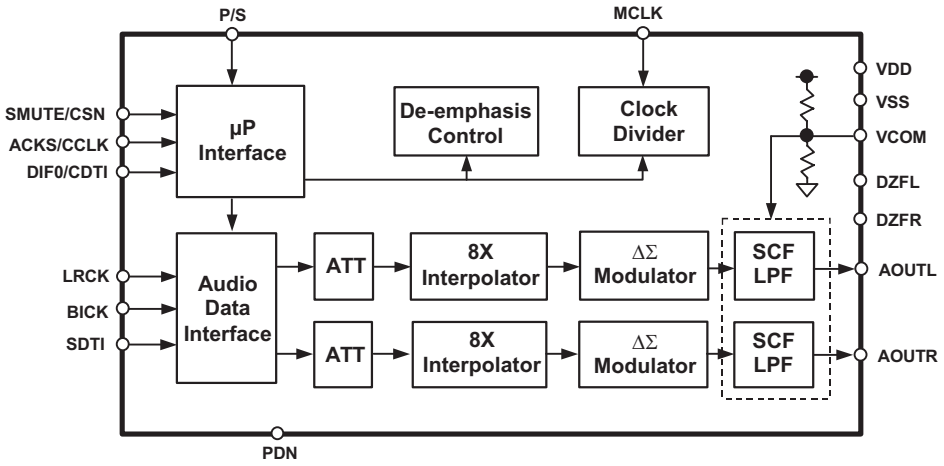
M30281FAHP(XM MICROPROCESSOR)

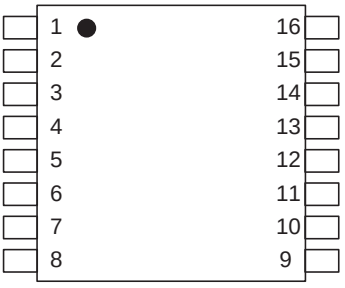


No.	PIN NAME	I/O	DESCRIPTION
3	Cnvss		Connect to Vcc.
5	FW_CE	I	Port for writing flash.
6	~RESET	I	Reset input
7	Xout		Connect to the crystal oscillator.
8	Vss		Ground for power supply
9	Xin		Connect to the crystal oscillator.
10	Vcc		Power supply Vcc
20	MHREQ	I	Request signal to transfer the serial data from main microprocessor. (System)
21	MSREQ	O	Request signal to transfer the serial data to main microprocessor. (Local)
22	MCLK	I	Serial clock input from main microprocessor.
23	MSDI	I	Serial data input from main microprocessor.
24	MSDO	O	Serial data output to main microprocessor.
25	FW_TXD	O	Port for writing flash.
26	FW_RXD	I	Port for writing flash.
27	FW_SCLK	I	Port for writing flash.
28	FW_BUSY	O	Port for writing flash.
29	DACSDO	O	Serial data output for DAC.
30	DACRESET	O	Reset output for DAC.
31	DACCS	O	Serial communication chip select for DAC.
32	DACCLK	O	Serial communication clock for DAC.
33	XMSDO	O	Serial data output for XM IC.
34	XMSDI	I	Serial data input for XM IC.
43	XM_COM_SEL	O	Command select output for XM IC.
44	XM_RESET	O	Reset output for XM IC.
45	XM_ERR_IRQ	I	Error interrupt request line for XM IC.
46	FW_P16	I	Port for writing flash.
48	XM_PWR_CTRL	O	Power supply control for XM IC.
59	AVSS		Ground for A/D converter.
61	Vref		Reference power supply for A/D converter.
62	AVcc		Power supply for A/D converter.

IC BLOCK DIAGRAMS AND DESCRIPTIONS

AK4384(106dB 192kHz 24-Bit 2ch ΔΣ DAC)





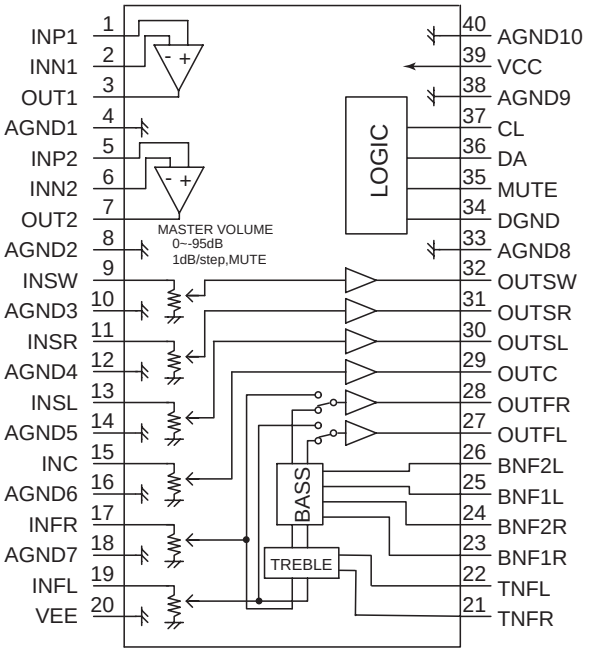
Pin Layout

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin
5	PDN	I	Power-Down Mode Pin When at "L", the AK4384 is in the power-down mode and is held in reset. The AK4384 should always be reset upon power-up.
6	SMUTE	I	Soft Mute Pin in parallel mode "H": Enable, "L": Disable
	CSN	I	Chip Select Pin in serial mode
7	ACKS	I	Auto Setting Mode Pin in parallel mode "L": Manual Setting Mode, "H": Auto Setting Mode
	CCLK	I	Control Data Clock Pin in serial mode
8	DIF0	I	Audio Data Interface Format Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial mode
9	P/S	I	Parallel/Serial Select Pin (Internal pull-up pin) "L": Serial control mode, "H": Parallel control mode
10	AOUTR	O	Rch Analog Output Pin
11	AOUTL	O	Lch Analog Output Pin
12	VCOM	O	Common Voltage Pin, VDD/2 Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
13	VSS	-	Ground Pin
14	VDD	-	Power Supply Pin
15	DZFR	O	Rch Data Zero Input Detect Pin
16	DZFL	O	Lch Data Zero Input Detect Pin

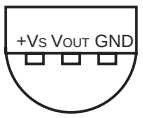
Note: All input pins except pull-up pin should not be left floating.

IC BLOCK DIAGRAMS AND DESCRIPTIONS

BD3814FV(5.1ch Electronic Volume)



LM61C1Z(Temperature Sensor)

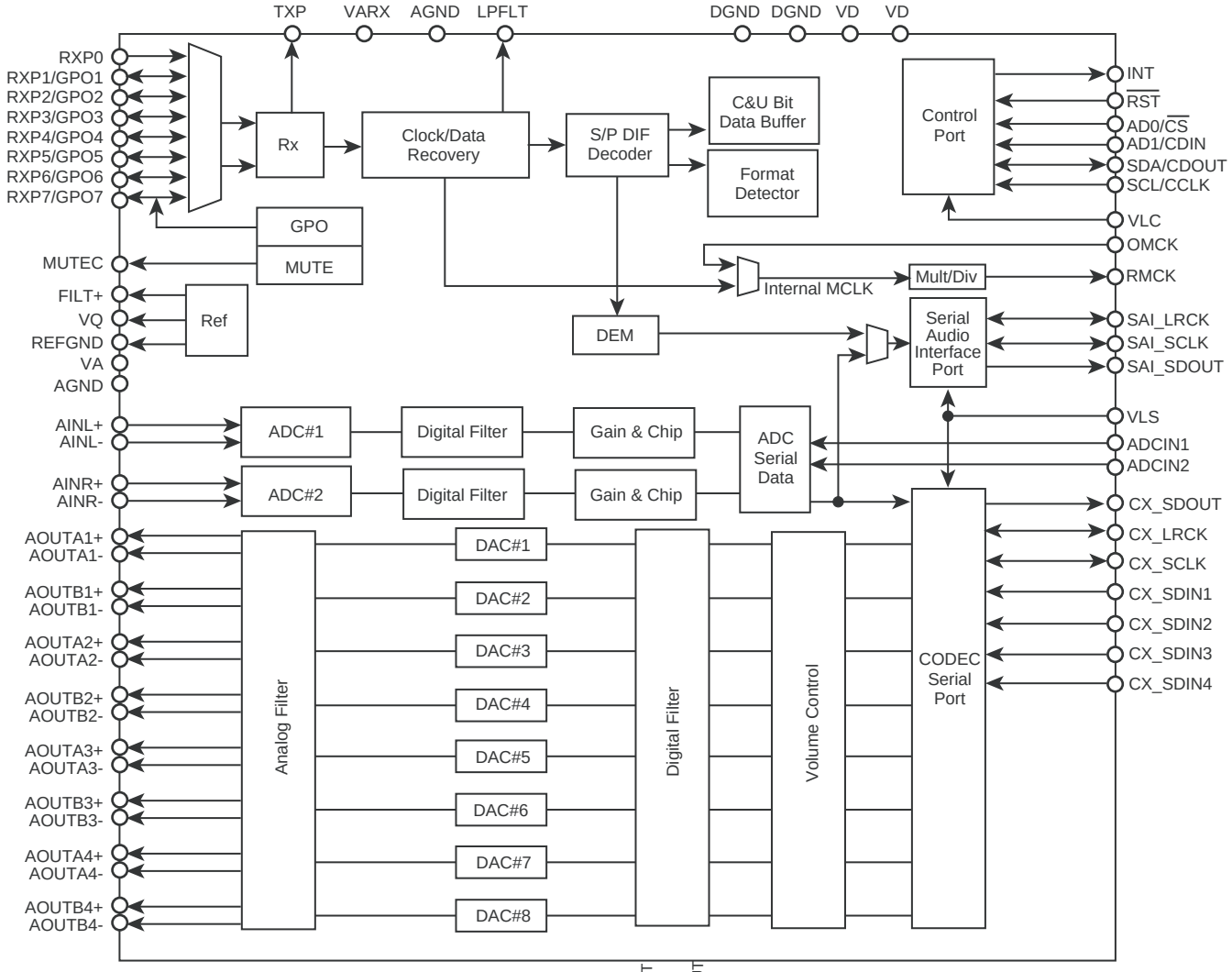


+Vs=+2.7 to +10V
VOUT=10mV x T℃+600mV
T:Temperature

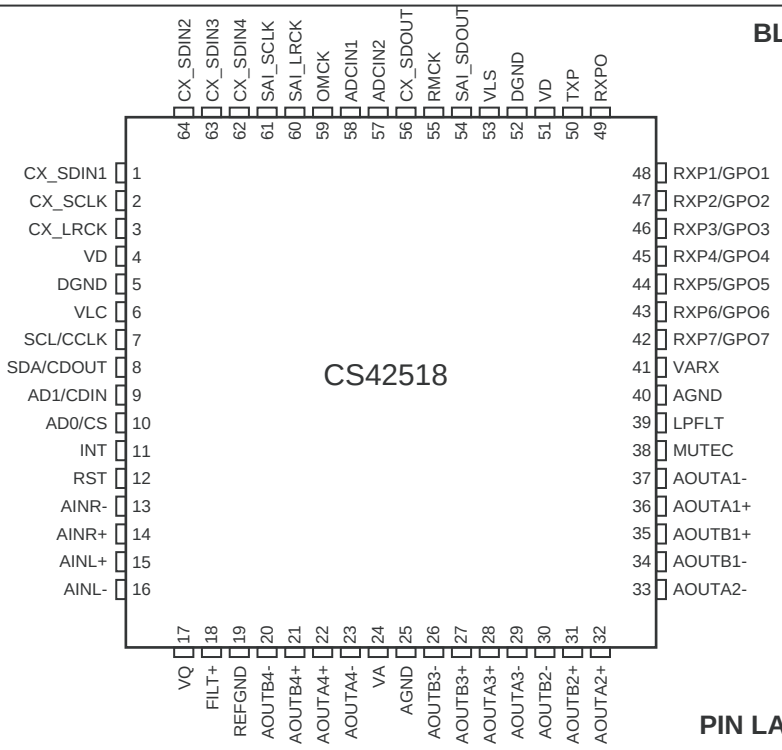
No.	Terminal	Description	No.	Terminal	Description
1	INP1	Input terminal 1	21	TNFR	Rch treble filter terminal
2	INN1	Input terminal 1	22	TNFL	Lch treble filter terminal
3	OUT1	Output terminal 1	23	BNF1R	Rch bass filter terminal 1
4	AGND1	Analog ground terminal 1	24	BNF2R	Rch bass filter terminal 2
5	INP2	Input terminal 2	25	BNF1L	Lch bass filter terminal 1
6	INN2	Input terminal 2	26	BNF2L	Lch bass filter terminal 2
7	OUT2	Output terminal 2	27	OUTFL	Front Lch output terminal
8	AGND2	Analog ground terminal 2	28	OUTFR	Front Rch output terminal
9	INSW	Subwoofer input terminal	29	OUTC	Center ch output terminal
10	AGND3	Analog ground terminal 3	30	OUTSL	Surround Lch output terminal
11	INSR	Surrond Rch input terminal	31	OUTSR	Surround Rch output terminal
12	AGND4	Analog ground terminal 4	32	OUTSW	Subwoofer output terminal
13	INSL	Surround Lch input terminal	33	AGND8	Analog ground terminal 8
14	AGND5	Analog ground terminal 5	34	DGND	Digital ground terminal
15	INC	Center channel input terminal	35	MUTE	Mute temrinal
16	AGND6	Analog ground terminal 6	36	DA	Serial data and latch input terminal
17	INFR	Front Rch input terminal	37	CL	Serial clock input terminal
18	AGND7	Analog ground terminal 7	38	AGND9	Analog ground terminal 9
19	INFL	Front Lch input terminal	39	VCC	Power supply trerminal +
20	VEE	Power supply terminal -	40	AGND10	Analog ground terminal 10

IC BLOCK DIAGRAMS AND DESCRIPTIONS

CS42518 (8-Ch Codec with S/PDIF Receiver)



BLOCK DIAGRAM



PIN LAYOUT

IC BLOCK DIAGRAMS AND DESCRIPTIONS

CS42528 (8-Ch Codec with S/PDIF Receiver)

TERMINAL DESCRIPTION

Pin Name	#	Pin Description
CX_SDIN1 CX_SDIN2 CX_SDIN3 CX_SDIN4	1 64 63 62	Codec Serial Audio Data Input (Input) - Input for two's complement serial audio data.
CX_SCLK	2	CODEC Serial Clock (Input/Output) - Serial clock for the CODEC serial audio interface
CX_LRCK	3	CODEC Left Right Clock (Input/ Output) - Determines which channel, Left or Right, is currently active on the CODEC serial audio data line.
VD	4 51	Digital Power (Input) - Positive power supply for the digital section.
DGND	5 52	Digital Ground (Input) - Ground reference. Connects to digital ground.
VLC	6	Control Port Power (Input) - Determines the required signal level for the control port.
SCL/CCLK	7	Serial Control Port Clock (Input) - Serial clock for the serial control port.
SDA/CDOUT	8	Serial Control Data (Input/Output) - SDA is a data I/O line in IC mode and requires an external pull-up resistor to the logic interface voltage. CDOUT is the output data line for the control port interface in SPI mode.
AD1/CDIN	9	Address Bit 1 (I^2C)/Serial Control Data (SPI) (Input) - AD1 a chip address pin in I^2C mode; CDIN is the input data line for control port interface in SPI mode.
AD0/$\overline{CS}$	10	Address Bit 0 (I^2C)/Control Port Chip Select (SPI) (Input) - AD0 is a chip address pin in I^2C mode; CS is the chip select signal in SPI mode.
INT	11	Interrupt (Output) - The CS42518 will generate an interrupt condition as per the Interrupt Mask register.
$\overline{RST}$	12	Reset (Input) - The device enters a low power mode and all internal registers are reset to their default settings when low.
AINR- AINR+	13 14	Differential right Channel Analog Input (Input) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
AINL- AINL+	15 16	Differential right Channel Analog Input (Input) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
VQ	17	Quiescent Voltage (Output) - Filter connection for internal quiescent reference voltage.
FILT+	18	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits.
REFGND	19	Reference Ground (Input) - Ground reference for the internal sampling circuits.
AOUTA1 +, - AOUTB1 +, - AOUTA2 +, - AOUTB2 +, - AOUTA3 +, - AOUTB3 +, - AOUTA4 +, - AOUTB4 +, -	36, 37 35, 34 32, 33 31, 30 28, 29 27, 26 22, 23 21, 20	Differential Analog Output (Output) - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
VA VARX	24 41	Analog Power (Input) - Positive power supply for the analog section.
AGND	25 40	Analog Ground (Input) - Ground reference. Connectes to analog ground.

IC BLOCK DIAGRAMS AND DESCRIPTIONS

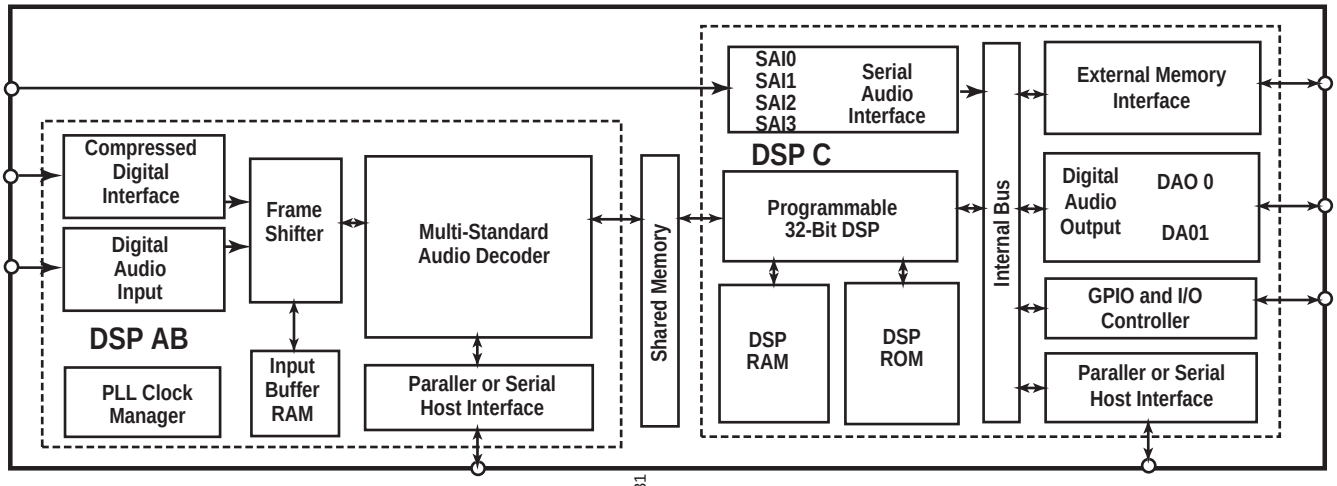
CS42518 (8-Ch Codec with S/PDIF Receiver)

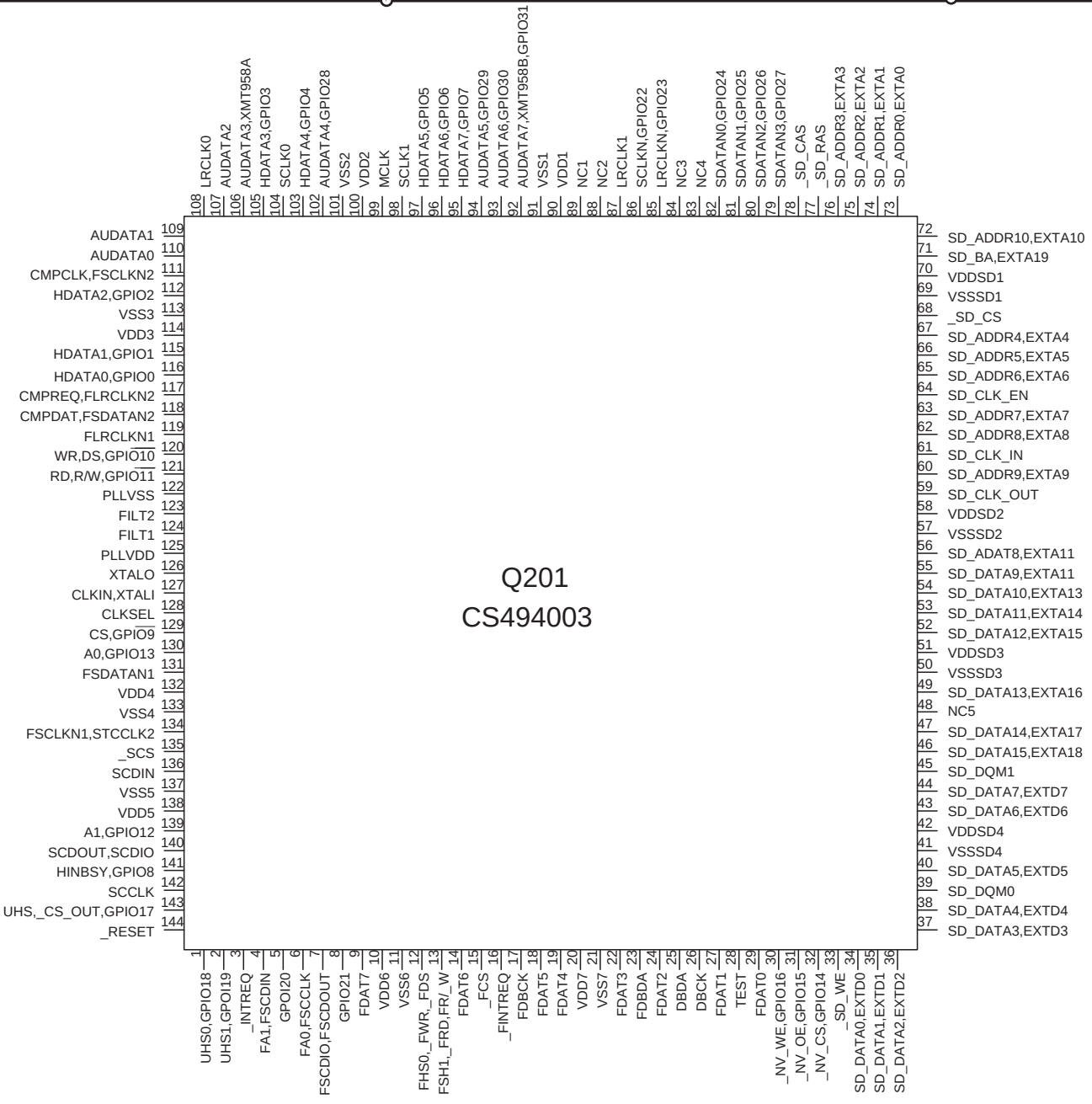
TERMINAL DESCRIPTION

Pin Name	#	Pin Description
VA VARX	24 41	Analog Power (Input) - Positive power supply for the analog section.
AGND	25 40	Analog Ground (Input) - Ground reference. Connects to analog ground.
MUTEC	38	Mute Control (Output) - The Mute Control pin outputs high impedance following an initial power -on condition or whenever the PDN bit is set to a "1", forcing the codec into power -down mode. The signal will remain in a high impedance state as long as the part is in power-down mode. The Mute Control pin goes to the selected "active" state during reset, muting, or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatoy but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
LPFLT	39	PLL Loop Filer (Output) - An RC network should be connected between this pin and ground.
RXP7/GPO7 RXP6/GPO6 RXP5/GPO5 RXP4/GPO4 RXP3/GPO3 RXP2/GPO2 RXP1/GPO1	42 43 44 45 46 47 48	S/PDIF Receiver Input/ General Purpose Output (Input/ Output) - Receiver inputs for S/PDIF encoded data. The CS42518 has an internal 8:2 multiplexer to select the active receiver port, according to the Receiver Mode Control 2 resister. These pins can also be configured as general purpose output pins, ADC Overflow indicators or Mute Control outputs according to the RXP/General Purpose Pin Control resisters.
RXP0	49	S/PDIF Receiver Input (Input) - Dedicated receiver input for S/PDIF encoded data.
TXP	50	S/PDIF Transmitter Output (Output) - S/PDIF encoded data output, mapped directly from one of the receiver inputs as indicated by the Receiver Mode Control 2 resister.
VLP	53	Serial Port Interface Power (Input) - Determines the required signal level for the serial port interfaces.
SAI_SDOUT	54	Serial Audio Interface Serial Data Output (Output) - Output for two's complement serial audio PCM data from the S/PDIF incoming stream. This pin can also be configured to transmit the output of the internal and external ADCs.
RMCK	55	Recovered Master Clock (Output) - Recovered master clock output from the External Clock Reference
CX_SDOUT	56	CODEC Serial Data Output (Output) - Output for two's complement serial audio data the internal and external ADCs.
ADCIN1 ADCIN2	58 57	External ADC Serial Input (Input) - The CS42528 provides for up two external stereo analog to digital converter inputs to provide a maximum of six channels on serial data output line when the CS42528 is placed in One Line mode.
OMCK	59	External Reference Clock (Input) - External clock reference that must be within the ranges specified in currently active on the serial audio data line.
SAI_LRCK	60	Serial Audio Interface Left/Right Clock (Input/Output) - Determines which channel, Left of Right, is currently active on the serial audio data line.
SAI_SCLK	61	Serial Audio Interface Serial Clock (Input/Output) - Serial clock for the Serial Audio Interface

IC BLOCK DIAGRAMS AND DESCRIPTIONS

CS494003(Audio Decoder DSP)





IC BLOCK DIAGRAMS AND DESCRIPTIONS

CS494003(Audio Decoder DSP)

PIN NO.	TERMINAL NAME/DESCRIPTION
1	UHS0, GPIO18 :DSPC control mode select Bit 0, General Purpose I/O
2	UHS1, GPIO19 :DSPC control mode select Bit 1, General Purpose I/O
3	INTREQ:Control Port Interrupt Request
4	FA1, FSCDIN:Host parallel address bit zero or SPI rerial control data input
5	GPIO20:General Purpose I/O can be individually configured and controlled by DSPC.
6	FAO, FSCCLK:Host Parallel Address Bit Zero or Serial Control Port Clock
7	FHS2, FSCDIO, FSCDOUT:Mode select bit 2 or serial control port data input and output,parallel porttype select
8	GPIO21:General Purpose I/O can be individually configured and controlled by DSPC.
9	FDAT7:DSPAB Bidirectional Data Bus input
10	VDD6:2.5V supply voltage.
11	VSS6:2.5V ground.
12	FHS0, FWR, FDS:Mode select bit 0 or host write strobe or host data strobe
13	FHS1, FRD, FR/W:Mode select bit 1 or host parallel output enable or host parallel R/W
14	FDAT6:DSPAB Bidirectional Data Bus input
15	FCS:Host parallel chip select,Host serial SPI chip select
16	FINTREQ:Control port interrupt request
17	FDBCK:Reversed input:This pin is reversed and is pulled up with an external resistor.
18	FDAT5:DSPAB Bidirectional Data Bus input
19	FDAT4:DSPAB Bidirectional Data Bus input
20	VDD7:2.5V supply voltage.
21	VSS7:2.5V ground.
22	FDAT3:DSPAB Bidirectional Data Bus input
23	FDBDAReversed input:This pin is reversed and is pulled up with an external resistor.
24	FDAT2:DSPAB Bidirectional Data Bus input
25	DBDA:Debug data
26	DBCK:Debug clock
27	FDAT1:DSPAB Bidirectional Data Bus input
28	TEST:This pin is connected low for normal operation.
29	FDAT0:DSPAB Bidirectional Data Bus input
30	NV_WE, GPIO16:SRAM write enable output, General Purpose I/O
31	NV_OE, GPIO15:SRAM output Enable output, General Purpose I/O
32	NV_CS, GPIO14:SRAM Chip Select output, General Purpose I/O
33	SD_WE :SDRAM write enable output.
34	SD_DATA0, EXTD0:SDRAM data bus. SRAM external data bus input.
35	SD_DATA1, EXTD1:SDRAM data bus. SRAM external data bus input.
36	SD_DATA2, EXTD2:SDRAM data bus. SRAM external data bus input.
37	SD_DATA3, EXTD3:SDRAM data bus. SRAM external data bus input.
38	SD_DATA4, EXTD4:SDRAM data bus. SRAM external data bus input.
39	SD_DQM0:SDRAM data mask 0 output.
40	SD_DATA5, EXTD5:SDRAM data bus. SRAM external data bus input.
41	VSSSD4:3.3V SDRAM / SRAM / EPROM Interface ground.
42	VDDSD4:3.3V SDRAM / SRAM / EPROM Interface supply
43	SD_DATA6, EXTD6:SDRAM data bus. SRAM external data bus input.
44	SD_DATA7, EXTD7:SDRAM data bus. SRAM external data bus input.
45	SD_DQM1:SDRAM data mask 1 output.
46	SD_DATA15, EXTA18:SDRAM data bus output, SRAM external address bus output
47	SD_DATA14, EXTA17:SDRAM data bus output, SRAM external address bus output
48	NC5:No connect. Connect to ground.

IC BLOCK DIAGRAMS AND DESCRIPTIONS

CS494003(Audio Decoder DSP)

PIN NO.	TERMINAL NAME/DESCRIPTION
49	SD_DATA13, EXTA16:SDRAM data bus output, SRAM external address bus output
50	VSSSD3:3.3V SDRAM / SRAM / EPROM Interface ground.
51	VDDSD3:3.3V SDRAM / SRAM / EPROM Interface supply
52	SD_DATA12, EXTA15:SDRAM data bus output, SRAM external address bus output
53	SD_DATA11, EXTA14:SDRAM data bus output, SRAM external address bus output
54	SD_DATA10, EXTA13:SDRAM data bus output, SRAM external address bus output
55	SD_DATA9, EXTA12:SDRAM data bus output, SRAM external address bus output
56	SD_DATA8, EXTA11:SDRAM data bus output, SRAM external address bus output
57	VSSSD2:3.3V SDRAM / SRAM / EPROM Interface ground.
58	VDDSD2:3.3V SDRAM / SRAM / EPROM Interface supply
59	SD_CLK_OUT:SDRAM clock output.
60	SD_ADDR9, EXTA9:SDRAM address bus output. SRAM external address output.
61	SD_CLK_IN:SDRAM re-timing clock input.
62	SD_ADDR8, EXTA8:SDRAM address bus output. SRAM external address output.
63	SD_ADDR7, EXTA7:SDRAM address bus output. SRAM external address output.
64	SD_CLK_EN:SDRAM clock enable output.
65	SD_ADDR6, EXTA6:SDRAM address bus output. SRAM external address output.
66	SD_ADDR5, EXTA5:SDRAM address bus output. SRAM external address output.
67	SD_ADDR4, EXTA4:SDRAM address bus output. SRAM external address output.
68	SD_CS:SDRAM Chip select
69	VSSSD1:3.3V SDRAM / SRAM / EPROM Interface ground.
70	VDDSD1:3.3V SDRAM / SRAM / EPROM Interface supply
71	SD_BA, EXTA19:SDRAM bank address select, SRAM external address bus 19.
72	SD_ADDR10, EXTA10:SDRAM address bus output. SRAM external address output.
73	SD_ADDR0, EXTA0:SDRAM address bus output. SRAM external address output.
74	SD_ADDR1, EXTA1:SDRAM address bus output. SRAM external address output.
75	SD_ADDR2, EXTA2:SDRAM address bus output. SRAM external address output.
76	SD_ADDR3, EXTA3:SDRAM address bus output. SRAM external address output.
77	SD_RAS:SDRAM row address strobe output.
78	SD_CAS:DRAM column address strobe output.
79	SDATAN3, GPIO27:Digital-audio PCM data input. General purpose I/O
80	SDATAN2, GPIO26:Digital-audio PCM data input. General purpose I/O
81	SDATAN1, GPIO25:Digital-audio PCM data input. General purpose I/O
82	SDATAN0, GPIO24:Digital-audio PCM data input. General purpose I/O
83	NC4:No connect. Connect to ground.
84	NC3:No connect. Connect to ground.
85	LRCLKN, GPIO23:PCM Audio Input Sample Rate Clock, General Purpose I/O
86	SCLKN, GPIO22:PCM Audio Input Bit Clock, General Purpose I/O
87	LRCLK1:Audio Output Sample Rata Clock
88	NC2:No connect. Connect to ground.
89	NC1:No connect. Connect to ground.
90	VDD1:2.5V supply voltage.
91	VSS1:2.5V ground
92	AUDATA7, XMT958B, GPIO31:PCM digital-audio data output 7, S/PDIF Transmitter, General Purpose I/O
93	AUDATA6, GPIO30:PCM digital-audio data output 6, General Purpose I/O
94	AUDATA5, GPIO29:PCM digital-audio data output 5, General Purpose I/O
95	HDATA7, GPIO7:DSPC Bidirectional Data Bus, General Purpose I/O
96	HDATA6, GPIO6:DSPC Bidirectional Data Bus, General Purpose I/O

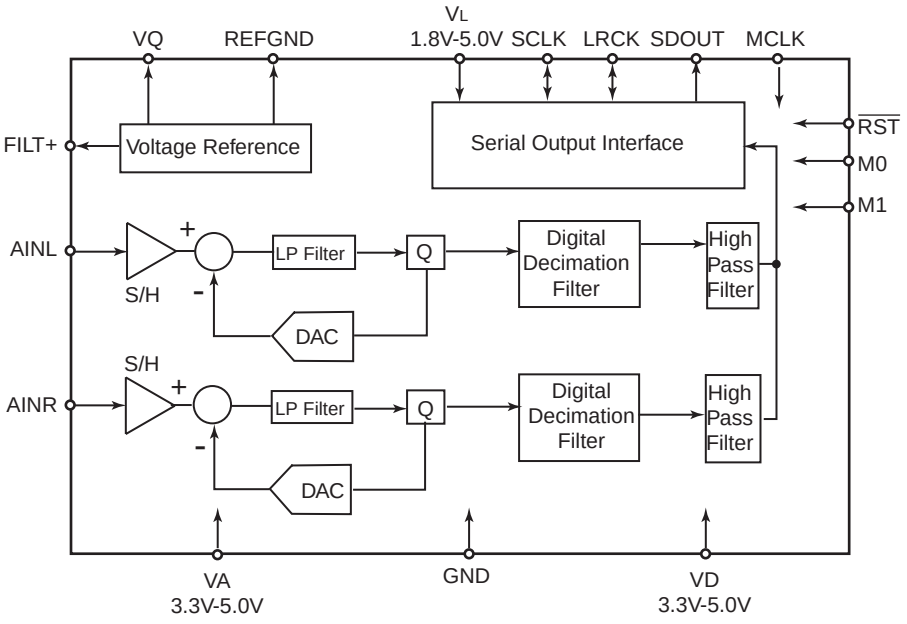
IC BLOCK DIAGRAMS AND DESCRIPTIONS

CS494003(Audio Decoder DSP)

PIN NO.	TERMINAL NAME/DESCIPTION
97	HDATA5, GPIO5:DSPC Bidirectional Data Bus, General Purpose I/O
98	SCLK1 :Audio Output Bit Clock:Bidirectional digital-audio output bit clock for AUDATA4, to AUDATA7.
	As an output, SCLK1 can provide 32 fs, 64 fs, 128 fs, 256 fs, or 512 fs frequencies and is synchronous to MCLK.
99	MCLK:Bidirectional master audio clock. As an output, MCLK provides a low jitter oversampling clock.
100	VDD2:2.5V supply voltage.
101	VSS2:2.5V ground.
102	AUDATA4, GPIO28:Digital Audio Output 4, General Purpose I/O.PCM digital-audio data output.
103	HDATA4, GPIO4:DSPC Bidirectional Data Bus, General Purpose I/O
104	SCLK0 :Audio Output Bit Clock:Bidirectional digital-audio output bit clock for AUDATA0, to AUDATA3.
105	HDATA3, GPIO3:DSPC Bidirectional Data Bus, General Purpose I/O
106	AUDATA3, XMT958A:Digital Audio Output 3, S/PDIF Transmitter
107	AUDATA2:PCM digital-audio data output.
108	LRCLK0:Audio Output Sample Rate Clock
109	AUDATA1:PCM digital-audio data output.
110	AUDATA0:PCM digital-audio data output.
111	CMPCLK, FSCLKN2:PCM Audio Input Bit Clock:Digital- audio bit clock input.
112	HDATA2, GPIO2:DSPC Bidirectional Data Bus, General Purpose I/O
113	VSS3:2.5V ground.
114	VDD3:2.5V supply voltage.
115	HDATA1, GPIO1:DSPC Bidirectional Data Bus, General Purpose I/O
116	HDATA0, GPIO0:DSPC Bidirectional Data Bus, General Purpose I/O
117	CMPREQ, FLRCLKN2:PCM audio input request
118	CMPDAT, FSDATAN2:Digital-audio data input that can accept either one compressed line or 2 channels of PCM data.
119	FLRCLKN1:Digital-audio frame clock input.
120	WR, DS, GPIO10:Host Write Strobe, Host Data Strobe, General Purpose I/O
121	RD, R/W, GPIO11:Host Parallel Output Enable, Host Parallel R/W, General Purpose I/O
122	PLLVSS :PLL Ground Voltage
123	FILT2: Phase-Locked Loop Filter. Connects to an external filter for the phase-locked loop.
124	FILT1: Phase-Locked Loop Filter. Connects to an external filter for the phase-locked loop.
125	PLLVDD:2.5V PLL supply voltage.
126	XTALO: Crystal oscillator output.
127	CLKIN, XTALI:External Clock input / Crystal Oscillator input:12MHz crystal oscillator is connected.
128	CLKSEL:DSP Clock select input
129	CS, GPIO9:Host Parallel Chip Select, General Purpose I/O
130	A0, GPIO13:Host Address Bit 0, General Purpose I/O
131	FSDATAN1:Digital-audio data input can accept from one compressed line or 2 channels of PCM data.
132	VDD4:2.5V supply voltage.
133	VSS4:2.5V ground.
134	FSCLKN1, STCCLK2:Digital audio bit clock input.
135	SCS:Host Serial SPI Chip Select:SPI mode active-low chip-select input signal.
136	SCDIN:SPI Serial Control Data Input:In SPI mode this pin serves as the data input pin.
137	VSS5:2.5V ground.
138	VDD5:2.5V supply voltage.
139	A1, GPIO12:Host Address Bit 1, General Purpose I/O
140	SCDOUT, SCDIO:Serial Control Port Data Input and Output:In SPI mode this pin serves as the data output pin.
141	HINBSY, GPIO8: Input host Message Status, General Purpose I/O. This pin is indicates that serial or parallel communication data written to the DSP has not been read yet.
142	SCCLK :This pin serves as the serial SPI clock input.
143	UHS2, CS_OUT, GPIO17:Mode Select Bit 2, External Serial Memory Chip Select,General Purpose I/O
144	RESET :Master Reset Input:Asynchronous active-low master reset input.

IC BLOCK DIAGRAMS AND DESCRIPTIONS

CS5340-CZZ(101dB,192kHz, Multi-Bit Audio A/D Converter)

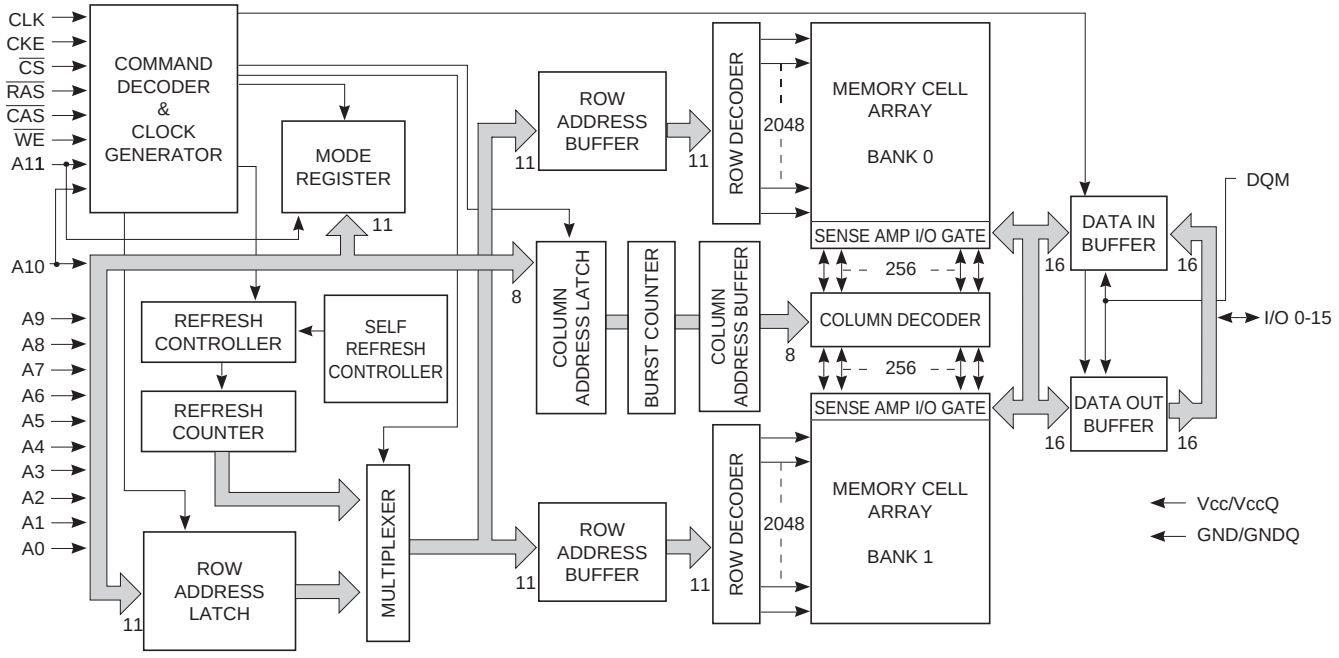


Pin	Pin Name	I/O	Description
1	M0	I	Mode Selection-Determines the operational mode of the device.
16	M1	I	
2	MCLK	I	Master Clock-Clock source for the delta-sigma modulator and digital filters.
3	VL		Logic Power-Positive power supply for digital input/output.
4	SDOUT	O	Serial Audio Data Output-Output for two's complement serial audio data.
5,14	GND		Ground-Connect to the analog ground.
6	VD	I	Digital Power-Positive power supply for the digital section.
7	SCLK	I/O	Serial Clock-Serial clock for the serial audio interface.
8	LRCK	I/O	Left Right Clock-Determines which channel, Left and Right, is currently active on the serial audio data line.
9	RST	I	Reset-The device enters a low power mode when low.
10 12	AINL AINR	I I	Analog Input-The full scale analog input level is 0.56Vp-p.
11	VQ	O	Quiescent Voltage-Filter connection for the internal quiescent reference voltage.
13	VA		Analog Power-Positive power supply for the analog section.
15	FILT+	O	Positive Voltage Reference-Positive reference voltage for the internal sampling circuits.

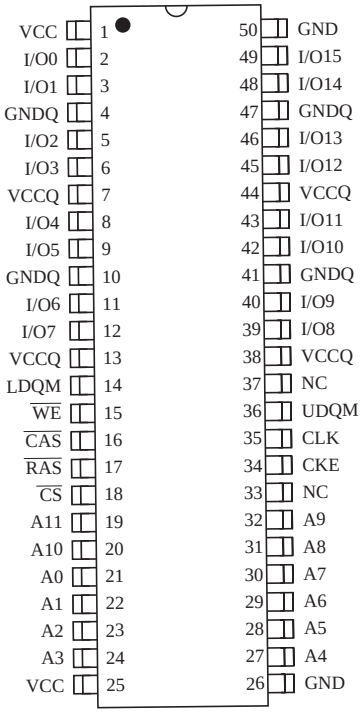
IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS

IC42S16100 (16-Mbit Synchronous Dynamic RAM)

BLOCK DIAGRAM



PIN LAYOUT

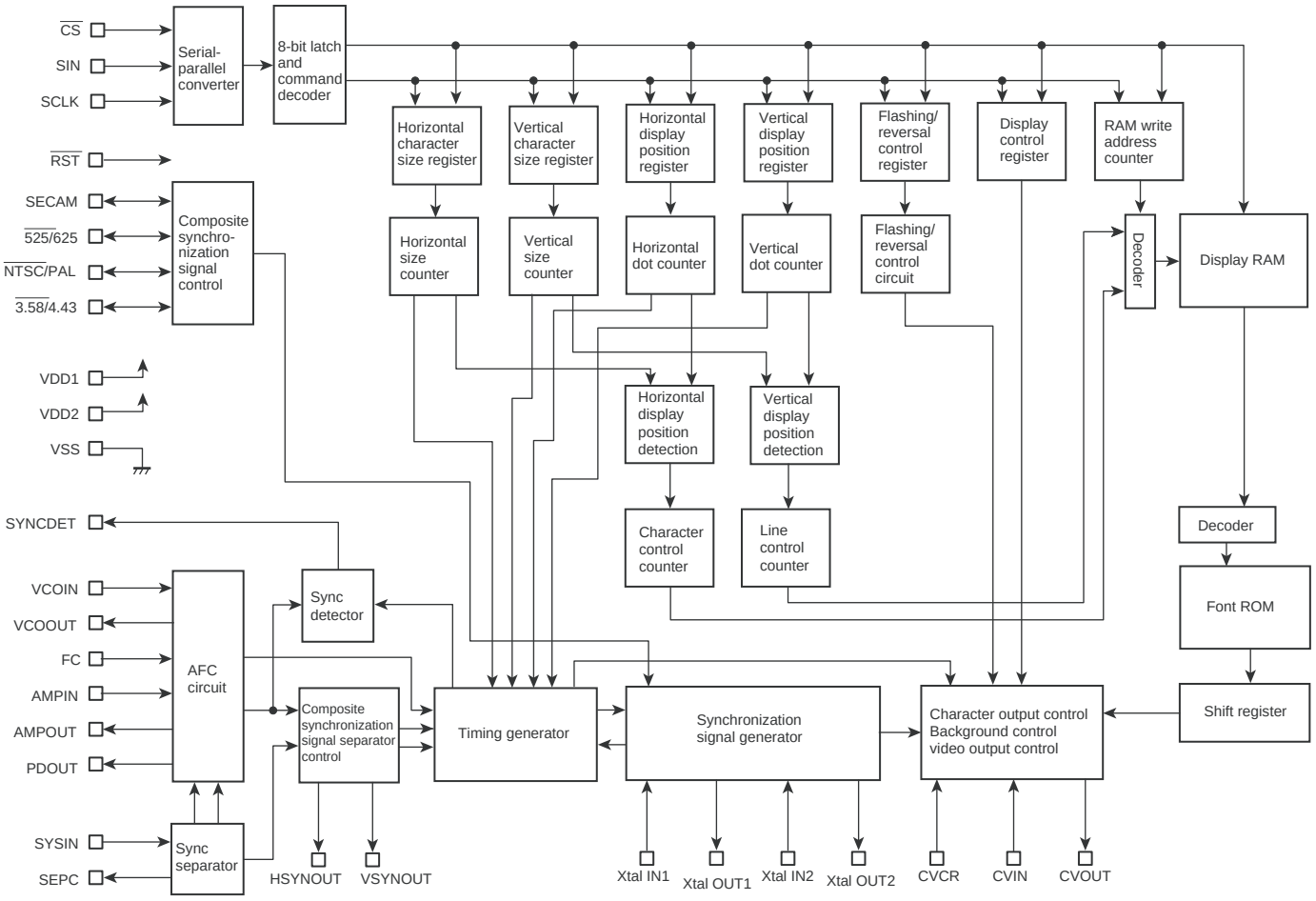


Pin No.	Pin name	Function
20 to 24 27 to 32	A0-A10	A0 to A10 are address inputs. A0-A10 are used as row address inputs during active command input and A0-A7 as column address inputs during read or write command input. A10 is also used to determine the precharge mode during other commands. If A10 is LOW during precharge command, the bank selected by A11 is precharged, but if A10 is HIGH, both banks will be precharged. When A10 is HIGH in read or write command cycle, the precharge starts automatically after the burst access. These signals become part of the OP CODE during mode register set command input.
19	A11	A11 is the bank selection signal. When A11 is LOW, bank 0 is selected and when high, bank 1 is selected. This signal becomes part of the OP CODE during mode register set command input.
16	$\overline{CAS}$	$\overline{CAS}$, in conjunction with the $\overline{RAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
34	CKE	The CKE input determines whether the CLK input is enabled within the device. When is CKE HIGH, the next rising edge of the CLK signal will be valid, and when LOW, invalid. When CKE is LOW, the device will be in either the power-down mode, the clock suspend mode, or the self refresh mode. The CKE is an asynchronous input.
35	CLK	CLK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
18	$\overline{CS}$	The $\overline{CS}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{CS}$ is LOW, and disabled with $\overline{CS}$ is HIGH. The device remains in the previous state when $\overline{CS}$ is HIGH.
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	I/O0 to I/O15	I/O00 to I/O15 are I/O pins. I/O through these pins can be controlled in byte units using the LDQM and UDQM pins.
14, 36	LDQM, UDQM	LDQM and UDQM control the lower and upper bytes of the I/O buffers. In read mode, LDQM and UDQM control the output buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and when HIGH, disabled. The outputs go to theHIGH impedance state when LDQM/UDQM is HIGH. This function corresponds to $\overline{OE}$ in conventional DRAMs. In write mode, LDQM and UDQM control the input buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and data can be written to the device. When LDQM or UDQM is HIGH, input data is masked and cannot be written to the device.
17	$\overline{RAS}$	$\overline{RAS}$, in conjunction with $\overline{CAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
15	$\overline{WE}$	$\overline{WE}$, in conjunction with $\overline{RAS}$ and $\overline{CAS}$, forms the device command. See the "Command Truth Table" item for details on device commands.
7, 13, 38, 44	$V_{CC}Q$	$V_{CC}Q$ is the output buffer power supply.
1, 25	V_{CC}	V_{CC} is the device internal power supply.
4, 10, 41, 47	GNDQ	GNDQ is the output buffer ground.
26, 50	GND	GND is the device internal ground.

IC BLOCK DIAGRAMS AND DESCRIPTIONS

LC74763-9836 (On-Screen Display IC)

BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND DESCRIPTIONS

LC74763-9836 (On-Screen Display IC)

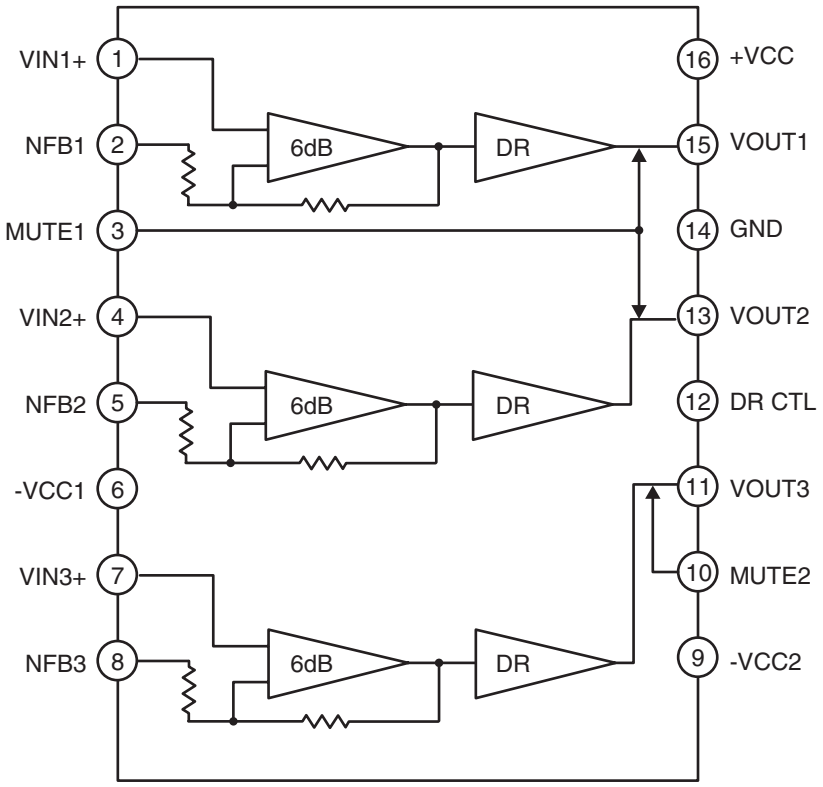
TERMINAL DESCRIPTION

Pin No.	Symbol	Function	Description
1	V_{SS}	Ground	Ground connection
2	$Xtal_{IN1}$	Crystal oscillator connection	Connection for the crystal and capacitor used to form the crystal oscillator that generates the internal synchronization signal. The oscillator can be selected with a command switch.
3	$Xtal_{OUT1}$		
4	$HSYNC_{OUT}$	Horizontal synchronization output	Outputs the horizontal synchronization signal (AFC). The output polarity can be selected (metal option). Also functions as general output port (command switch).
5	$Xtal_{IN2}$	Crystal oscillator connection	Connection for the crystal and capacitor used to form the crystal oscillator that generates the internal synchronization signal.
6	$Xtal_{OUT2}$		
7	$VSYNC_{OUT}$	Vertical synchronization output	Outputs the vertical synchronization signal. The output polarity can be selected (metal option). Also functions as general output port (command switch).
8	$\overline{CS}$	Enable input	Enables/disables serial data input. Serial data is enabled when this pin is low (hysteresis input). Pull-up resistor built in (metal option).
9	SIN	Data input	Serial data input (hysteresis input). Pull-up resistor built in (metal option).
10	SCLK	Clock input	Clock input for serial data input (hysteresis input). Pull-up resistor built in (metal option).
11	SECAM	SECAM mode switch input/ output (command switch)	During input, switches between SECAM and other modes. During output, functions as general output port or internal V output (command switch). Low = other modes, high = SECAM mode
12	$\overline{525}$/625	525/625 switch input/output (command switch)	During input, switches between 525 scan lines and 625 scan lines. During output, functions as general output port or character data output (command switch). Low = 525 lines, high = 625 lines
13	$\overline{NTSC}$/PAL	NTSC/PAL switch input/output (command switch)	Switches the color mode between NTSC and PAL. During output, functions as general output port or frame data output (command switch). Low = NTSC, high = PAL
14	$\overline{3.58}$/4.43	3.58/4.43 switch input/output (command switch)	Switch FSC between 3.58 MHz and 4.43 MHz. During output, functions as general output port or halftone output (command switch). Low = 3.58, high = 4.43
15	$\overline{RST}$	Reset input	System reset input pin, low is active (hysteresis input). Pull-up resistor built in (metal option).
16	CV_{OUT}	Video signal output	Composite video output
17	V_{DD2}	Power supply connection	Power supply connection for composite video signal level generation
18	CV_{IN}	Video signal input	Composite video input
19	CV_{CR}	Video signal input	SECAM chroma signal input
20	$SYNC_{IN}$	Sync separator circuit input	Built-in sync separator circuit video signal input
21	SEP_{C}	Sync separator circuit	Built-in sync separator circuit
22	V_{SS}	Ground	Ground connection
23	PD_{OUT}	Control voltage output	AFC control voltage output
24	AMP_{IN}	AFC filter connection	Filter connection
25	AMP_{OUT}		
26	FC	Control voltage input	AFC control voltage input
27	VCO_{IN}	LC oscillator connection	VCO LC oscillator circuit coil and capacitor connection
28	VCO_{OUT}		
29	$SYNC_{DET}$	External synchronization signal detection output	Outputs the exclusive NOR of the horizontal synchronization signal (AFC) and CSYNC (sync separator). The output polarity can be selected (metal option). Also functions as general output port (command switch).
30	V_{DD1}	Power supply connection	Power supply connection (+5 V: digital system power supply)

IC BLOCK DIAGRAM AND TERMINAL DESCRIPTIONS

LA7106M (6ch AMP + Driver)

BLOCK DIAGRAM



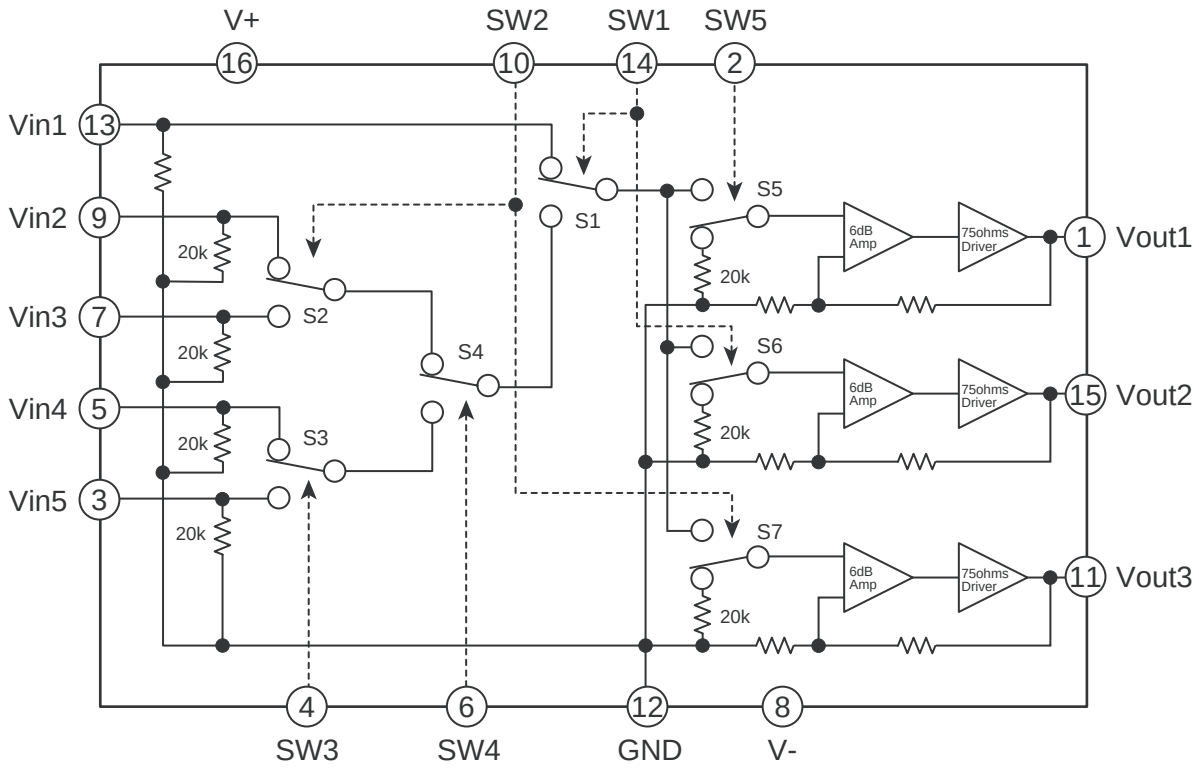
TRUTH TABLE

	Pins 3 , 10	Pin 12
H	Through	150 ohm Drive
L	Mute	75 ohm Drive

IC BLOCK DIAGRAMS AND DESCRIPTIONS

NJM2595M(5-INPUT 3-OUTPUT VIDEO SWITCH)

BLOCK DIAGRAM



TRUTH TABLE

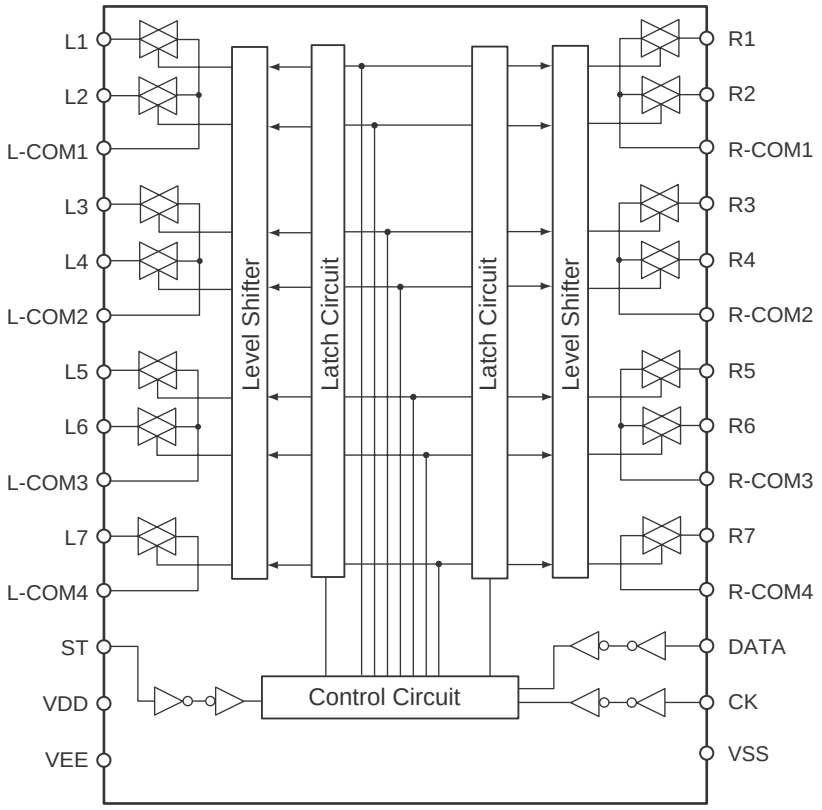
Control Signal vs. Output Signal (L=VCL, H=VCH, X=L or H)

SW1	SW2	SW3	SW4	SW5	Vout1	Vout2	Vout3
L	H	X	X	H	Vin1	MUTE	Vin1
	L			H	Vin1	MUTE	MUTE
	H			L	MUTE	MUTE	Vin1
H	L	X	L	H	Vin2	Vin2	MUTE
				L	MUTE	Vin2	MUTE
H	H	X	L	H	Vin3	Vin3	Vin3
				L	MUTE	Vin3	Vin3
H	H	L	H	H	Vin4	Vin4	Vin4
	H			L	MUTE	Vin4	Vin4
	L			H	Vin4	Vin4	MUTE
	L			L	MUTE	Vin4	MUTE
H	H	H	H	H	Vin5	Vin5	Vin5
	H			L	MUTE	Vin5	Vin5
	L			H	Vin5	Vin5	MUTE
	L			L	MUTE	Vin5	MUTE
L	L	X	X	L	MUTE	MUTE	MUTE

IC BLOCK DIAGRAMS AND DESCRIPTIONS

NJU7311AM (Analog Function Switch)

BLOCK DIAGRAM



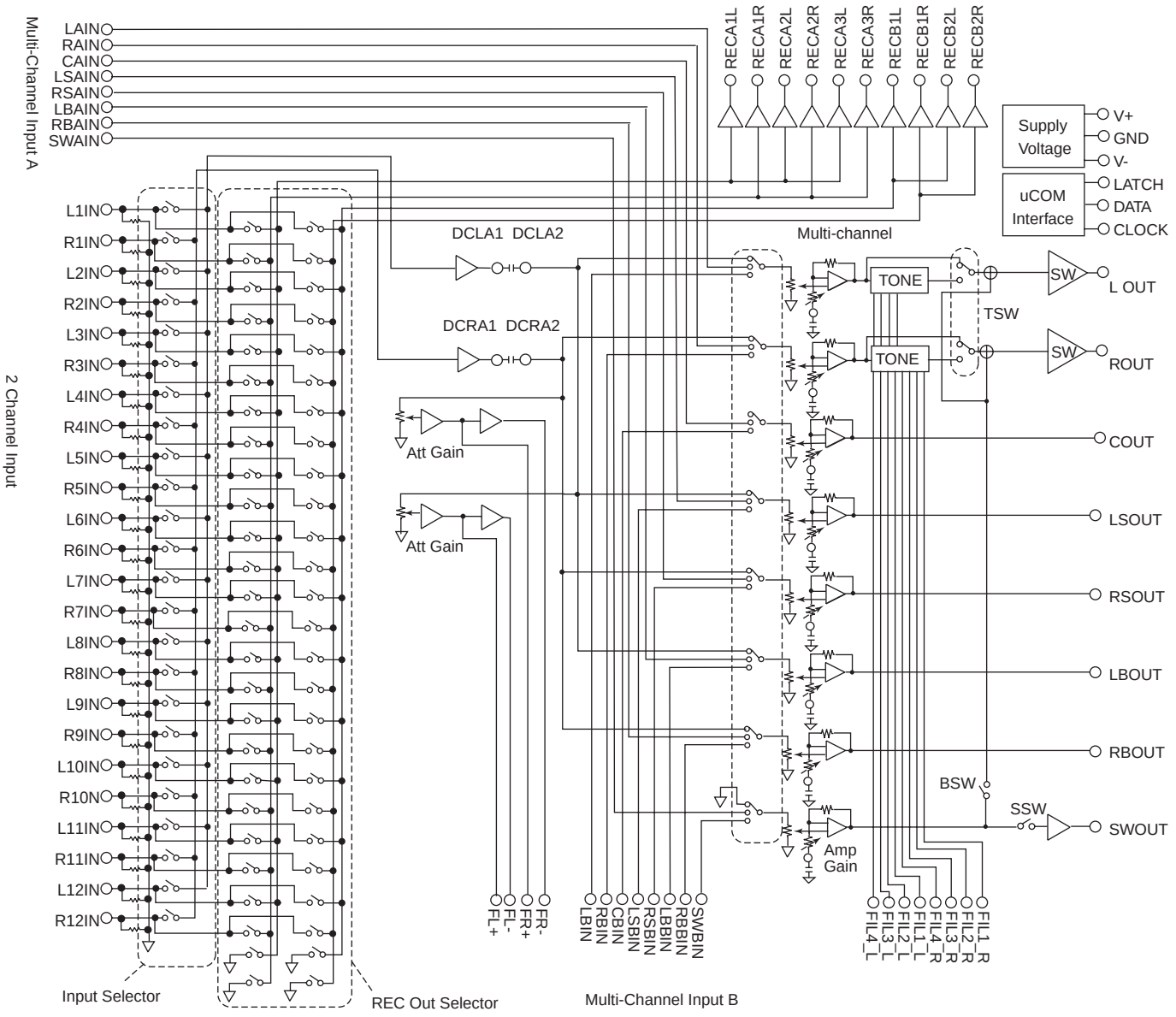
TERMINAL DESCRIPTION

Pin No.	Pin Name	Description
1	VEE	Negative Voltage Supply
2	L1	Analog switch input/output
3	L2	Analog switch input/output
4	L-COM1	L1, L2, Common
5	L3	Analog switch input/output
6	L4	Analog switch input/output
7	L-COM2	L3, L4 common
8	L5	Analog switch input/output
9	L6	Analog switch input/output
10	L-COM3	L5, L6 Common
11	L7	Analog switch input/output
12	L-COM4	L7 Common
13	ST	Chip enable
14	VSS	GND

Pin No.	Pin Name	Description
15	CK	Clock input
16	DATA	Data input
17	R-COM4	R7 Common
18	R7	Analog switch input/output
19	R-COM3	R5, R6 Common
20	R6	Analog switch input/output
21	R5	Analog switch input/output
22	R-COM2	R3, R4 Common
23	R4	Analog switch input/output
24	R3	Analog switch input/output
25	R-COM1	R1, R2, Common
26	R2	Analog switch input/output
27	R1	Analog switch input/output
28	VDD	Positive voltage supply

IC BLOCK DIAGRAMS AND DESCRIPTIONS

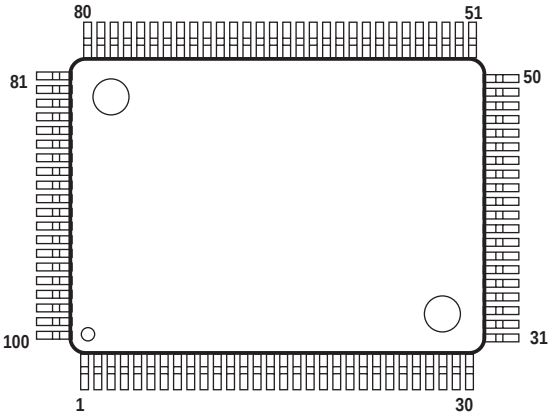
NJW1157(8-Channel Electronic Volume with Input Selector)



IC BLOCK DIAGRAMS AND DESCRIPTIONS

NJW1157(8-Channel Electronic Volume with Input Selector)

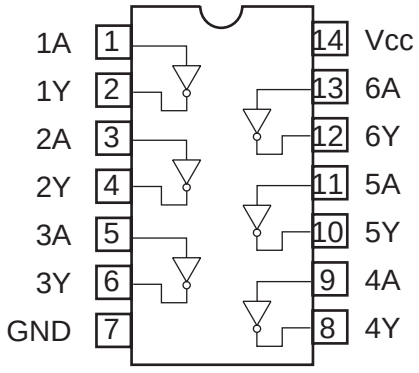
PIN FUNCTION



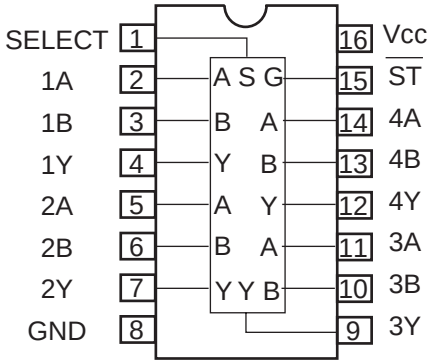
No.	SYMBOL	FUNCTION	No.	SYMBOL	FUNCTION
1	LOUT	Lch output	51	L1IN	"Input selector" Lch input 1
2	ROUT	Rch output	52	R1IN	"Input selector" Rch input 1
3	COUT	Cch output	53	L2IN	"Input selector" Lch input 2
4	LSOUT	LSch output	54	R2IN	"Input selector" Rch input 2
5	RSOUT	RSch output	55	L3IN	"Input selector" Lch input 3
6	LBOUT	LBch output	56	R3IN	"Input selector" Rch input 3
7	RBOUT	RBch output	57	L4IN	"Input selector" Lch input 4
8	SWOUT	SWch output	58	R4IN	"Input selector" Rch input 4
9	DC_L1	Lch Bass filter DC cut capacitor output terminal	59	L5IN	"Input selector" Lch input 5
10	DC_L2	Lch Bass filter DC cut capacitor input terminal	60	R5IN	"Input selector" Rch input 5
11	FIL_BL	Lch Bass filter terminal	61	L6IN	"Input selector" Lch input 6
12	FIL_TL	Lch Treble filter terminal	62	R6IN	"Input selector" Rch input 6
13	DC_R1	Rch Bass filter DC cut capacitor output terminal	63	L7IN	"Input selector" Lch input 7
14	DC_R2	Rch Bass filter DC cut capacitor input terminal	64	R7IN	"Input selector" Rch input 7
15	FIL_BR	Rch Bass filter terminal	65	L8IN	"Input selector" Lch input 8
16	FIL_TR	Rch Treble filter terminal	66	R8IN	"Input selector" Rch input 8
17	N.C.	No connect	67	L9IN	"Input selector" Lch input 9
18	N.C.	No connect	68	R9IN	"Input selector" Rch input 9
19	V+	+ Power supply voltage input	69	L10IN	"Input selector" Lch input 10
20	V-*	- Power supply voltage input	70	R10IN	"Input selector" Rch input 10
21	REC_A1L	"Input selector" Lch REC output A1	71	L11IN	"Input selector" Lch input 11
22	REC_A1R	"Input selector" Rch REC output A1	72	R11IN	"Input selector" Rch input 11
23	REC_A2L	"Input selector" Lch REC output A2	73	L12IN	"Input selector" Lch input 12
24	REC_A2R	"Input selector" Rch REC output A2	74	R12IN	"Input selector" Rch input 12
25	REC_A3L	"Input selector" Lch REC output A3	75	NC	No connect
26	REC_A3R	"Input selector" Rch REC output A3	76	DGND	Digital Ground
27	REC_B1L	"Input selector" Lch REC output B1	77	DATA	Control data signal input
28	REC_B1R	"Input selector" Rch REC output B1	78	CLOCK	Clock signal input
29	REC_B2L	"Input selector" Lch REC output B2	79	LATCH	Latch signal input
30	REC_B2R	"Input selector" Rch REC output B2	80	LAIN	Multi-channel Lch input A
31	DCCAP_L	Switching noise rejection capacitor	81	RAIN	Multi-channel Rch input A
32	DCCAP_R	Switching noise rejection capacitor	82	CAIN	Multi-channel Cch input A
33	DCCAP_C	Switching noise rejection capacitor	83	LSAIN	Multi-channel LSch input A
34	GND	Ground	84	RSAIN	Multi-channel RSch input A
35	GND	Ground	85	LBAIN	Multi-channel LBch input A
36	DCCAP_LS	Switching noise rejection capacitor	86	RBAIN	Multi-channel RBch input A
37	DCCAP_RS	Switching noise rejection capacitor	87	SWAIN	Multi-channel SWch input A
38	DCCAP_LB	Switching noise rejection capacitor	88	LBIN	Multi-channel Lch input B
39	DCCAP_RB	Switching noise rejection capacitor	89	RBIN	Multi-channel Rch input B
40	DCCAP_SW	Switching noise rejection capacitor	90	CBIN	Multi-channel Cch input B
41	DCL_OUT	"Input selector" Lch output	91	LSBIN	Multi-channel LSch input B
42	DCL_IN	"Multi-channel selector" Lch output	92	RSBIN	Multi-channel RSch input B
43	DCR_OUT	"Input selector" Rch output	93	LBBIN	Multi-channel LBch input B
44	DCR_IN	"Multi-channel selector" Rch output	94	RBBIN	Multi-channel RBch input B
45	FL+	"Input selector gain control" Lch no-inverted output	95	SWBIN	Multi-channel SWch input B
46	FL-	"Input selector gain control" Lch inverted output	96	GND	Ground
47	FR+	"Input selector gain control" Rch no-inverted output	97	GND	Ground
48	FR-	"Input selector gain control" Rch inverted output	98	VSSOUT2	Internal Digital -Power Supply Output 2
49	VDDOUT	Internal Digital +Power Supply Output	99	VDDOUT2	Internal Digital +Power Supply Output 2
50	VSSOUT	Internal Digital -Power Supply Output	100	TCCAP	Switching noise rejection capacitor

IC BLOCK DIAGRAMS AND DESCRIPTIONS

74HC04F(Hex Inverter)



TC74VHC157FT(Quad 2-channel Multiplexer)

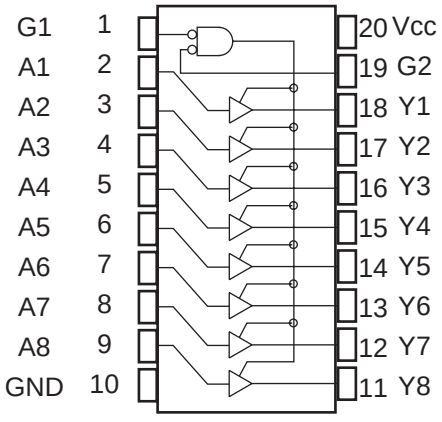


Truth Table

INPUTS				OUTPUT
ST	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X:Don't care

TC74VHC541FT/T541AFT(Octal buss buffer)

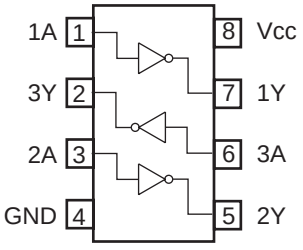


Truth Table

INPUTS			OUTPUT
G1	G2	An	Yn
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

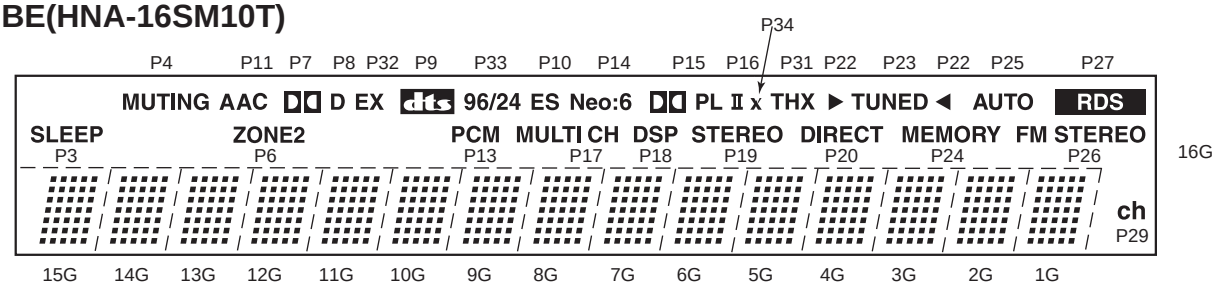
X:Don't care
Z:High Impedance

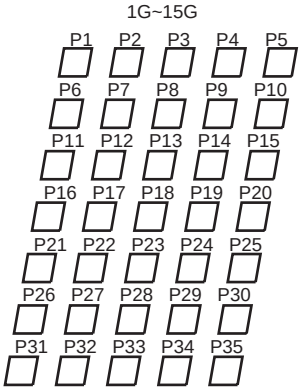
TC7WU04FU(3 Inverter)



IC BLOCK DIAGRAM AND DESCRIPTION

FL TUBE(HNA-16SM10T)



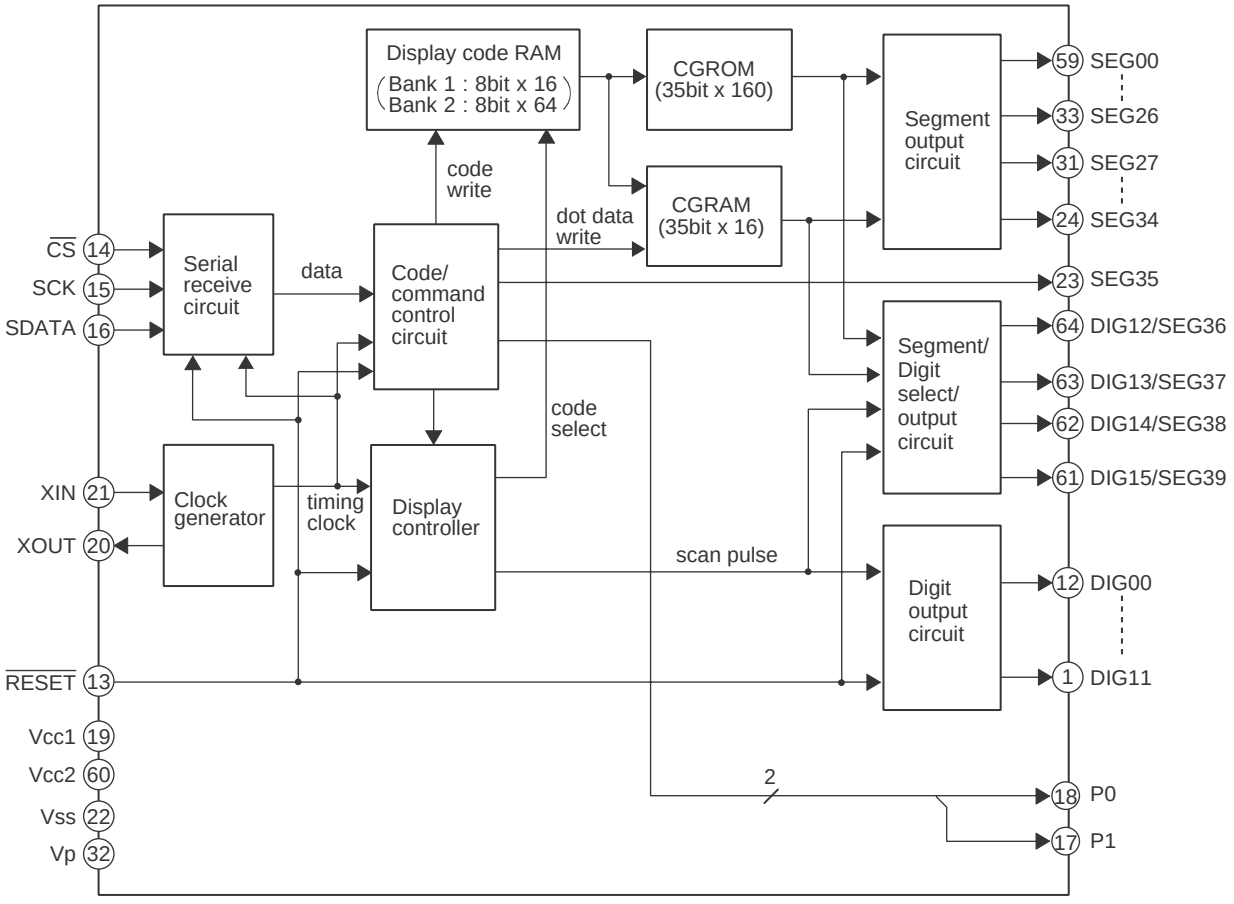


M66005 TERMINAL DESCRIPTION

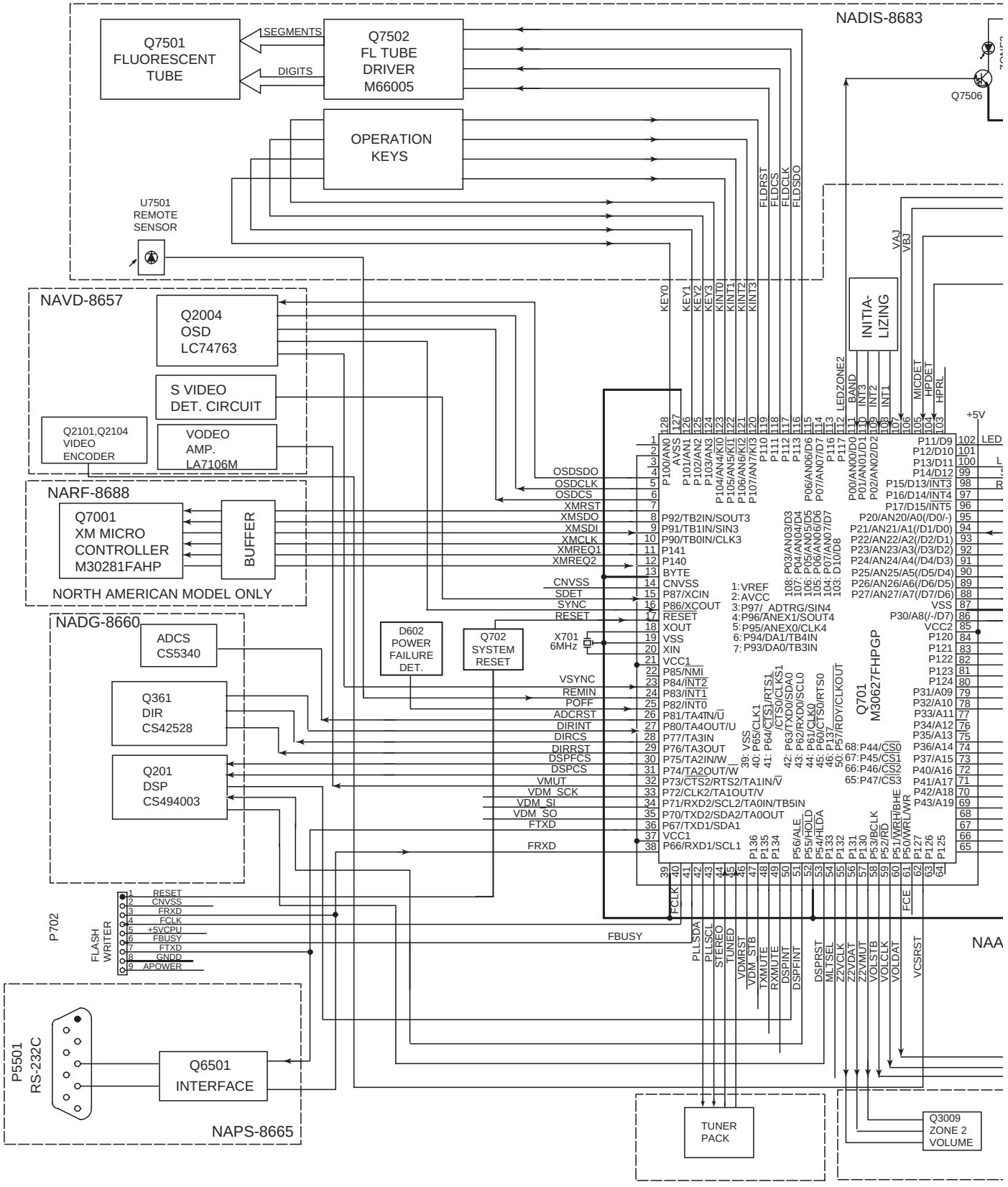
PIN NO.	SYMBOL	PIN NAME	DESCRIPTION
13	$\overline{\text{RESET}}$	Reset input	This pin is used to initialize the internal state of the M66005.
14	$\overline{\text{CS}}$	Chip select input	"L" : Communication with the MCU is possible. "H" : Any instruction from the MCU is neglected.
15	SCK	Shift clock input	At the rising edge from "L" to "H", input data is shifted.
16	SDATA	Serial data input	Character code or command data to display is input from MSB.
21, 20	XIN, XOUT	Clock input Clock output	This pin is used to connect a resister and a capacitor externally to set oscillation frequency.
1~12 61~64	DIG00 ~ DIG15	Digit output	These pins are used to connect to digit pins of VFD.
23~31 33~59	SEG00 ~ SEG39	Segment output	These pins are used to connect to segment pins of VFD.
17, 18	P0, P1		Output port (static operation)
19	VCC1		Positive power supply for internal logic.
60	VCC2		Positive power supply for high-pressure-resistant output port.
22	VSS		GND
32	VP		Negative power supply for VFD drive.

M66005 (FL tube driver)

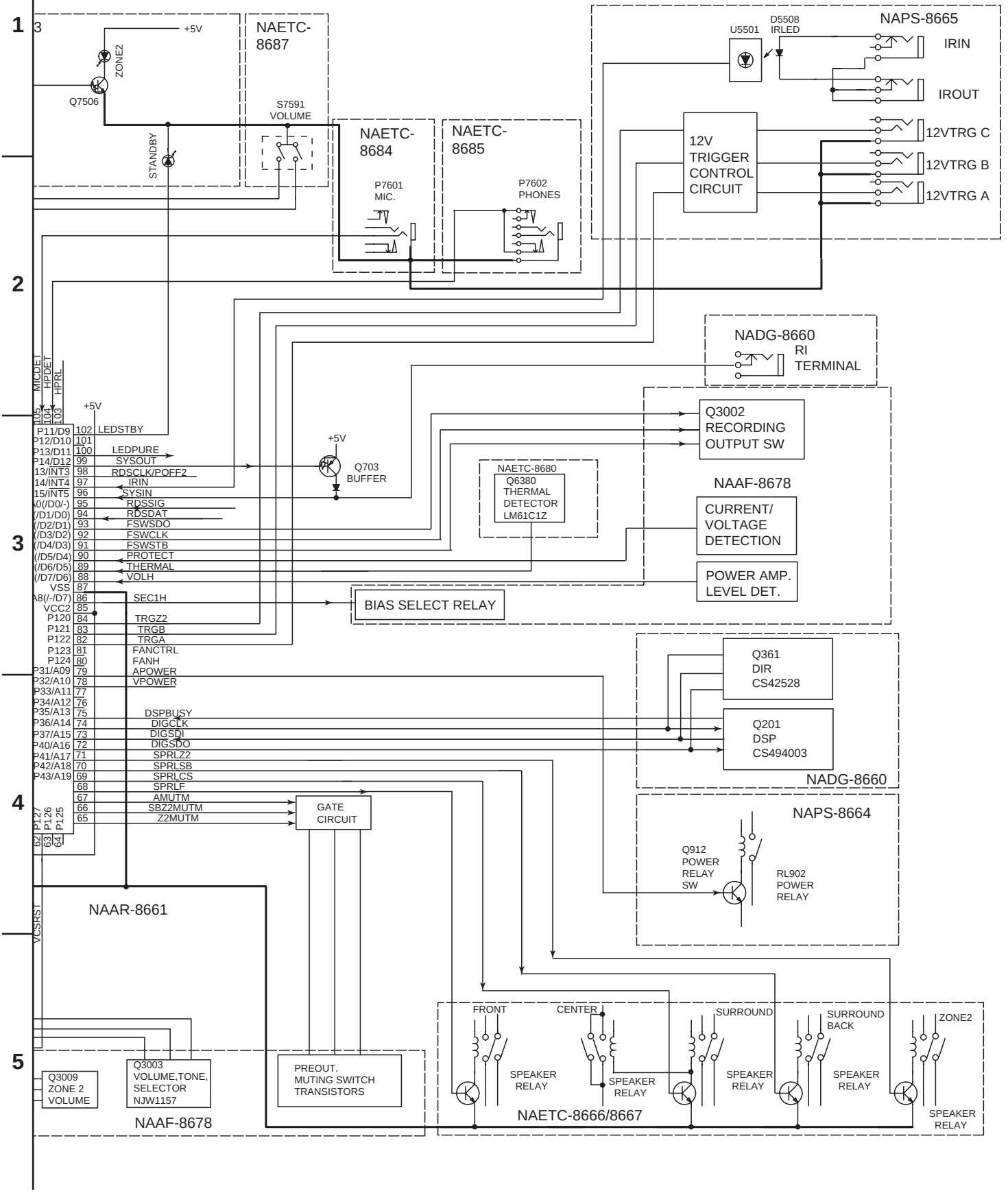
BLOCK DIAGRAM



MICROPROCESSOR-CONNECTION DIAGRAM



MICROPROCESSOR-CONNECTION DIAGRAM



MICROPROCESSOR-CONNECTION DIAGRAM

A B C D E F G H

1 2 3 4 5

Q7501 FLUORESCENT TUBE
SEGMENTS
DIGITS
Q7502 FL TUBE DRIVER M66005
OPERATION KEIES
U7501 REMOTE SENSOR
FLDRST FLDCS FLDCLK FLDSDO
KEY0 KEY1 KEY2 KEY3 KINT0 KINT1 KINT2 KINT3

NADIS-8683
+5V
ZONE2
Q7506
STANDBY
S7591 VOLUME
NAETC-8687
NAETC-8684
P7601 MIC.
NAETC-8685
P7602 PHONES
VAJ VBJ
INITIA-LIZING
LEDZONE2 BAND INT3 INT2 INT1 MICDET HPDET HPRL

NAPS-8665
U5501
D5508 IRLED
IRIN
IROUT
12V TRIGGER CONTROL CIRCUIT
12VTRG C
12VTRG B
12VTRG A

NAVD-8657
Q2004 OSD LC74763
S VIDEO DET. CIRCUIT
Q2101,Q2104 VIDEO ENCODER
VODEO AMP. LA7106M

NADG-8660
RI TERMINAL

NARF-8688
Q7001 XM MICRO CONTROLLER M30281FAHP
BUFFER
NORTH AMERICAN MODEL ONLY

Q3002 RECORDING OUTPUT SW
NAAF-8678
CURRENT/ VOLTAGE DETECTION
POWER AMP. LEVEL DET.

NADG-8660
ADCS CS5340
Q361 DIR CS42528
Q201 DSP CS494003
D602 POWER FAILURE DET.
Q702 SYSTEM RESET
X701 6MHz

OSDSDO OSDCLK OSDCS XMRST XMSDO XMSDI XMCLK XMREQ1 XMREQ2
CNVSS SDET SYNC RESET XOUT VSS XIN VCC1
VSYNC REMIN POFF ADCRST DIRINT DIRCS DIRRST DSPFCS DSPCS VMUT VDM_SCK VDM_SI VDM_SO FTXD FRXD

P11/D9 LEDSTBY
P12/D10 LEDPURE
P13/D11 SYSOUT
P14/D12 RDSCLK/POFF2
P15/D13/INT3 IRIN
P16/D14/INT4 SYSIN
P17/D15/INT5 RDSSIG
P20/AN20/A0(/D0/-) RDSDAT
P21/AN21/A1(/D1/D0) FSWSDO
P22/AN22/A2(/D2/D1) FSWCLK
P23/AN23/A3(/D3/D2) FSWSTB
P24/AN24/A4(/D4/D3) PROTECT
P25/AN25/A5(/D5/D4) THERMAL
P26/AN26/A6(/D6/D5) VOLH
P27/AN27/A7(/D7/D6) SEC1H
P30/A8(/-/D7) TRGZ2
P120 TRGB
P121 TRGA
P122 APOWER
P123 VPOWER
P124 DSPBUSY
P31/A09 DIGCLK
P32/A10 DIGSDI
P33/A11 DIGSDO
P34/A12 SPRLZ2
P35/A13 SPRLSB
P36/A14 SPRLCS
P37/A15 SPRLF
P40/A16 AMUTM
P41/A17 SBZ2MUTM
P42/A18 Z2MUTM
P43/A19

Q701 M30627FHPGP

1:VREF 2:AVCC 3:P97/ ADTRG/SIN4 4:P96/ANEX1/SOUT4 5:P95/ANEX0/CLK4 6:P94/DA1/TB4IN 7:P93/DA0/TB3IN
39: VSS 40: P65/CLK1 41: P64/CTS1/RTS1 /CTS0/CLKS1 42: P63/TXD0/SDA0 43: P62/RXD0/SCL0 44: P61/CLK0 45: P60/CTS0/RTS0 46: P57/RDY/CLKOUT
68:P44/CS0 67:P45/CS1 66:P46/CS2 65:P47/CS3
P00/AN00/D0 P01/AN01/D1 P02/AN02/D2 P03/AN03/D3 P04/AN04/D4 P05/AN05/D5 P06/AN06/D6 P07/AN07/D7 P10/D8 P11/D9
P100/AN0 P101/AN1 P102/AN2 P103/AN3 P104/AN4/KI0 P105/AN5/KI1 P106/AN6/KI2 P107/AN7/KI3 P110 P111 P112 P113 P114 P115 P116 P117
KEY0 KEY1 KEY2 KEY3 KINT0 KINT1 KINT2 KINT3
P92/TB2IN/SOUT3 P91/TB1IN/SIN3 P90/TB0IN/CLK3 P141 P140 BYTE CNVSS P87/XCIN P86/XCOUT RESET XOUT VSS XIN VCC1
P85/NMI P84/INT2 P83/INT1 P82/INT0 P81/TA4IN/U P80/TA4OUT/U P77/TA3IN P76/TA3OUT P75/TA2IN/W P74/TA2OUT/W P73/CTS2/RTS2/TA1IN/V P72/CLK2/TA1OUT/V P71/RXD2/SCL2/TA0IN/TB5IN P70/TXD2/SDA2/TA0OUT P67/TXD1/SDA1 VCC1 P66/RXD1/SCL1
P136 P135 P134 P56/ALE P55/HOLD P54/HLDA P133 P132 P131 P130 P53/BCLK P52/RD P51/WRH/BHE P50/WRL/WR P127 P126 P125
FCLK FBUSY PLLSDA PLLSCL STEREO TUNED VDMRST VDM_STB TXMUTE RXMUTE DSPINT DSPFINT DSPRST MLTSEL Z2VCLK Z2VDAT VOLSTB VOLCLK VOLDAT FCE VCSRST

NAAR-8661

P702 FLASH WRITER
1 RESET
2 CNVSS
3 FRXD
4 FCLK
5 +5VCPU
6 FBUSY
7 FTXD
8 GNDD
9 APOWER

Q703 BUFFER
NAETC-8680 Q6380 THERMAL DETECTOR LM61C1Z
BIAS SELECT RELAY
GATE CIRCUIT
PREOUT. MUTING SWITCH TRANSISTORS

Q361 DIR CS42528
Q201 DSP CS494003
NADG-8660

NAPS-8664
Q912 POWER RELAY SW
RL902 POWER RELAY

P5501 RS-232C
Q6501 INTERFACE
NAPS-8665

TUNER PACK
Q3009 ZONE 2 VOLUME
Q3003 VOLUME,TONE, SELECTOR NJW1157
NAAF-8678

FRONT CENTER SURROUND SURROUND BACK ZONE2
SPEAKER RELAY
NAETC-8666/8667

MICROPROCESSOR TERMINAL DESCRIPTIONS

No.	Pin Name	Function	I/O	Act.	Description
1	Vref	Vref			A/D Reference Vltage (Vcc)
2	AVcc	AVcc			A/D Power supply
3	P97/~ADTRG/SIN4		O	H	No connect
4	P96/ANEX1/SOUT4	OSDSDO	O	H	Data output for on-screen display.
5	P95/ANEX0/CLK4	OSDCLK	O	CLK	OSD IC Serial Communication Clock Output.
6	P94/DA1/TB4IN	OSDCS	O	H	OSD IC Chip Select Output
7	P93/DA0/TB3IN	XMRST	O	L	Reset output to XM microprocessor.
8	P92/TB2IN/SOUT3	XMSDO	O	H	Serial data output to XM microprocessor.
9	P91/TB1IN/SIN3	XMSDI	I	H	Serial data input from XM microprocessor.
10	P90/TB0IN/CLK3	XMCLK	O	CLK	Serial clock output to XM microprocessor.
11	P141	~XMREQ1	I	L	Serial data chip request input from XM microprocessor.
12	P140	~XMREQ2	O	H	Serial data chip request output to XM microprocessor.
13	BYTE	BYTE			External bus width select pin. Connects to the ground.
14	CNVSS	CNVss			Processor mode select pin. Connects to the ground via resistor.
15	P87/XCIN	~SDET	I	L	S Video input detection pin.
16	P86/XCOUT	~SYNC	I	L	Sync. detection pin.
17	~RESET	~RESET	I	L	Reset input
18	XOUT	Xout			Ceramic oscillator connection pin.
19	VSS	Vss			Power supply Ground
20	XIN	Xin			Ceramic oscillator connection pin.
21	VCC1	Vcc1			Power supply Vcc.
22	P85/~NMI	~NMI	I	L	Connect the pull-up resistor.
23	P84/~INT2	~VSYNC	I	L	Vertical sync signal detection input.
24	P83/~INT1	~REMIN	I	L	Remote control input.
25	P82/~INT0	POFF	I	H	Power failure detection input pin.
26	P81/TA4IN/~U	~ADCRST	O	L	Multi channel AD Reset output
27	P80/TA4OUT/U	DIRINT	I	H	DIR interrupt request detection pin.
28	P77/TA3IN	~DIRCS	O	L	DIR/CODEC chip select output pin.
29	P76/TA3OUT	~DIRRST	O	L	DIR/CODEC reset output pin.
30	P75/TA2IN/~W	~DSPFCS	O	L	Chip select output pin for DSP AB
31	P74/TA2OUT/W	~DSPCS	O	L	Chip select output pin for DSP C
32	P73/~CTS2/~RTS2/TA1IN/~V	~VMUT	O	L	Video mute control output pin
33	P72/CLK2/TA1OUT/V	VDM_SCK	O	H	Clock output pin to Video microprocessor.
34	P71/RXD2/SCL2/TA0IN/TB5IN	VDM_SI	I	H	Data output pin to Video microprocessor.
35	P70/TXD2/SDA2/TA0OUT	VDM_SO	O	H	Data input pin from Video microprocessor.
36	P67/TXD1/SDA1	FTXD	O	H	Port for writing Flash./RS232 port output.
37	Vcc1				Power supply
38	P66/RXD1/SCL1	FRXD	I	H	Port for writing Flash./RS232 port input.
39	Vss				Ground
40	P65/CLK1	FCLK	O	CLK	Port for writing Flash.
41	P64/~CTS1/~RTS1/~CTS0/CLKS1	FBUSY	O	H	Port for writing Flash.
42	P63/TXD0/SDA0	PLLSDA/VCSDA	I/O	H	Tuner I2C bus data pin/Video Dec/Enc serial communication data output pin
43	P62/RXD0/SCL0	PLLSCL/VCSCL	O	CLK	Tuner I2C bus clock output pin/Video Dec/Enc serial communication clock output pin
44	P61/CLK0	~STEREO	I	L	FM stereo broadcast defection input
45	P60/~CTS0/~RTS0	~TUNED	I	L	Tuner tuned detection input pin
46	P137	~VDMRST	O	H	Reset output pin to video microprocessor.
47	P136	VDM_STB	I	H	Strobe input pin from video microprocessor.
48	P135	TXMUTE	O	H	Muting output pin to video microprocessor.
49	P134	RXMUTE	I	H	Muting input pin from video microprocessor.
50	P57/~RDY/CLKOUT	~DSPINT	I	L	Interrupt request detection pin for DSP C.
51	P56/ALE	~DSPFINT	I	L	Interrupt request detection pin for DSP AB.
52	P55/~HOLD				Connect to the ground.
53	P54/~HLDA	~DSPRST	O	L	DSP reset output pin
54	P133	MLTSEL	O	H	Multi Ch AD and HDMI(I2S) select pin
55	P132	Z2VCLK	O	H	Serial clock output pin for Zone2 Volume IC.
56	P131	Z2VDAT	O	H	Serial data output pin for Zone2 Volume IC.
57	P130	Z2VMUT	O	H	Mute control output pin for Zone2 Volume IC.
58	P53/BCLK	VOLSTB	O	H	Strobe output for Volume
59	P52/~RD	VOLCLK	O	CLK	Serial clock output for Volume
60	P51/~WRH/~BHE	VOLDAT	O	H	Serial data output for Volume
61	P50/~WRL/~WR	~FCE	I	H	Port for writing Flash.
62	P127	~VCRST	O	L	Video Dec/Enc reset control pin
63	P126				
64	P125				

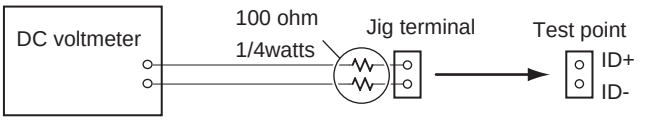
MICROPROCESSOR TERMINAL DESCRIPTIONS

No.	Pin Name	Function	I/O	Act.	Description
65	P47/~CS3	Z2MUT	O	H	Zone2 Out mute control pin
66	P46/~CS2	SBZ2MUT	O	H	Surround back/Zone2 mute control.
67	P45/~CS1	AMUT	O	H	Audio mute control pin
68	P44/~CS0	SPRLF	O	H	Front speaker relay control pin
69	P43/A19	SPRLCS	O	H	Center/Surround back speaker relay control pin.
70	P42/A18	SPRLSB	O	H	Surround back speaker relay control pin.
71	P41/A17	SPRLZ2	O	H	Zone2 speaker relay control pin
72	P40/A16	DIGSDO	O	H	Serial communication data output pin for DIR/CODEC/DSP.
73	P37/A15	DIGSDI	I	H	Serial communication data input pin for DIR/CODEC/DSP.
74	P36/A14	DIGCLK	O	CLK	Serial communication clock output pin for DIR/CODEC/DSP.
75	P35/A13	DSPBUSY	I	H	Busy detection pin for DSP C.
76	P34/A12	DGSW1	O	H	DIGITAL AUDIO MCK select 1. Not used.
77	P33/A11	DGSW2	O	H	DIGITAL AUDIO MCK select 2. Not used.
78	P32/A10	VPOWER	O	H	Power control output for video section
79	P31/A09	APOWER	O	H	Power source control output
80	P124	FANH	O	L	Fan speed control pin. High: Low speed Low: High speed
81	P123	FANCTRL	O	L	Fan operation control pin. High: Stop Low: Rotation
82	P122	TRGA	O	H	12V trigger output A
83	P121	TRGB	O	H	12V trigger output B
84	P120	TRGZ2	O	H	12V trigger output ZONE2
85	VCC2	Vcc2			Power supply
86	P30/A8(/-/D7)	SEC1H	O	H	Voltage select control pin
87	VSS	Vss			Ground
88	P27/AN27/A7(/D7/D6)	VOLH	I	A/D	Signal level detection circuit
89	P26/AN26/A6(/D6/D5)	THERMAL	I	A/D	Thermal detection pin
90	P25/AN25/A5(/D5/D4)	PROTECT	I	H	Protection circuit detection circuit
91	P24/AN24/A4(/D4/D3)	FSWSTB	O	H	Strobe output pin for function switch
92	P23/AN23/A3(/D3/D2)	FSWCLK	O	H	Serial clock output pin for function switch
93	P22/AN22/A2(/D2/D1)	FSWSDO	O	H	Serial data output pin for function switch
94	P21/AN21/A1(/D1/D0)	RDSDAT	I	H	Serial data input pin for RDS
95	P20/AN20/A0(/D0/-)	RDSSIG	I	H	Demodulator data input pin for RDS
96	P17/D15/~INT5	SYSIN	I	H	RI input pin
97	P16/D14/~INT4	~IRIN	I	L	IRIN remote control input pin
98	P15/D13/~INT3	~RDSCLK/POFF2	I	L	Serial clock input pin for RDS
99	P14/D12	~SYSOUT	O	L	RI output pin
100	P13/D11	LEDPURE	O	H	Pure Audio LED control output pin
101	P12/D10				
102	P11/D9	LEDSTBY	O	H	STANDBY LED control pin
103	P10/D8	HPRL	O	H	Headphone relay control pin
104	P07/AN07/D7	HPDET	I	H	Headphone detection input
105	P06/AN06/D6	~MICDET	I	L	Microphone detection input
106	P05/AN05/D5	VOLB	I	CLK	Rotary encoder input for Volume
107	P04/AN04/D4	VOLA	I	CLK	Rotary encoder input for Volume
108	P03/AN03/D3	INIT3	I	A/D	Initializing pin 3
109	P02/AN02/D2	INIT2	I	A/D	Initializing pin 2
110	P01/AN01/D1	INIT1	I	A/D	Initializing pin 1
111	P00/AN00/D0	BAND	I	A/D	Initializing pin for tuner section
112	P117	LEDZONE2	O	H	Zone2 LED control pin
113	P116				
114	P115				
115	P114				
116	P113	FLDSDO	O	H	Serial data output for FL driver
117	P112	FLDCLK	O	H	Serial clock output for FL driver
118	P111	FLDCS	O	H	Chip select output for FL driver
119	P110	~FLDRST	O	L	Reset output for FL driver
120	P107/AN7/~KI3	~KEYINT3	I	L	Key input interrupt 3
121	P106/AN6/~KI2	~KEYINT2	I	L	Key input interrupt 2
122	P105/AN5/~KI1	~KEYINT1	I	L	Key input interrupt 1
123	P104/AN4/~KI0	~KEYINT0	I	L	Key input interrupt 0
124	P103/AN3	KEY3	I	A/D	Key input 3
125	P102/AN2	KEY2	I	A/D	Key input 2
126	P101/AN1	KEY1	I	A/D	Key input 1
127	AVSS	AVss			Ground for A/D
128	P100/AN0	KEY0	I	A/D	Key input 0

ADJUSTMENT AND CONFIRMATION PROCEDURES 1

Idling current adjustment

Before Idling current adjustment, turn the trimming resistors R6040 to R6046 to counter-clockwise.
Connect the DC voltmeter at the sockets P6080 to P6086 via the carbon resistors 100 ohm 1/4W.



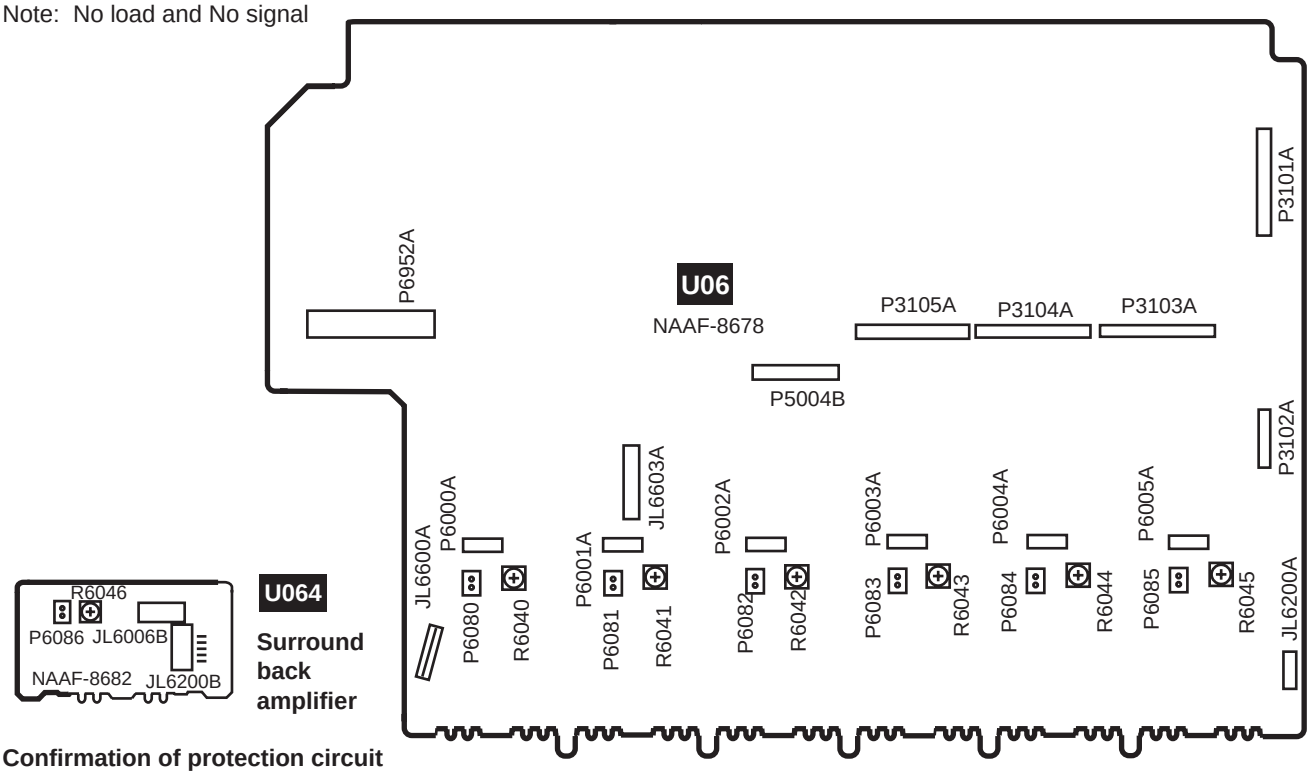
After turn POWER to ON, adjust the trimming resistors R6040, R6041 and R6042 so that the reading of voltmeter becomes 2.5 mV. (Front and center channels)
Adjust the trimming resistors R6043, R6044, R6045 and R6046 so that the reading of voltmeter becomes 1.5 mV. (Surround and surround back channels)
After adjustment, attach the top cover.
Confirm the voltage of points above after about five minutes.

Front and center channels

When less than 9.0 mV, readjust the resistors above so that the voltage becomes 9.0 mV.
When 9.0 mV to 11.0 mV, you are not necessary to adjust.
When more than 11.0 mV, readjust the resistors above so that the voltage becomes 11.0 mV.

Surround and surround back channels

When less than 6.0 mV, readjust the resistors above so that the voltage becomes 6.0 mV.
When 6.0 mV to 8.0 mV, you are not necessary to adjust.
When more than 6.0 mV, readjust the resistors above so that the voltage becomes 8.0 mV.
Note: No load and No signal



Confirmation of protection circuit

1. Confirmation of operation of speaker relay

Confirm that the speaker relays turn ON approximate 5 seconds after the power switch is turned ON.
Confirm that the speaker relays turn OFF immediately after the power switch is turned OFF.

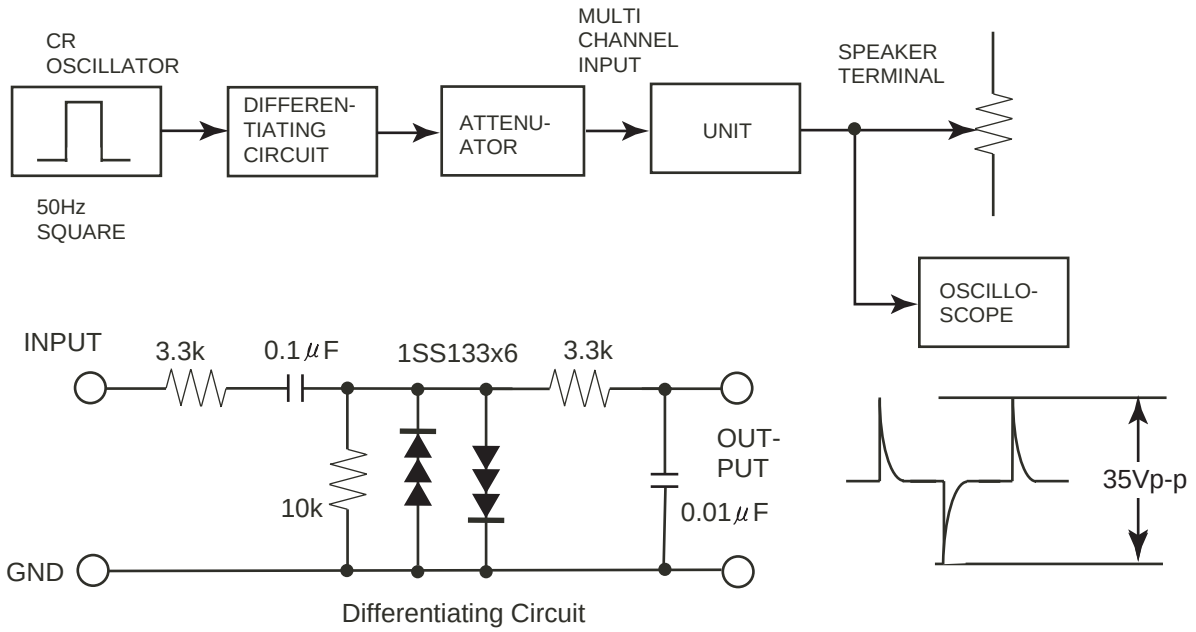
2. Confirmation of DC detection circuit

Press and hold down CD button, then press STANDBY/ON button to set the unit to "Test- 1".
After "Test- 1" on the FL tube light on, press DVD button to set the unit to "Test- 1-00".
Apply DC 1.5 to 3.5V to the MULTI-CH INPUT terminal with no load.
Confirm that the speaker relay turns OFF.
Apply DC -1.5 to -3.5 V to the MULTI-CH INPUT terminal with no load.
Confirm that the speaker relay turns OFF.
Caution: Don't apply DC voltage more than 1 sec..

ADJUSTMENT AND CONFIRMATION PROCEDURES 2

3. Confirmation of Current detection circuit

Set the unit to "Test- 1-00".
Connect the differentiating circuit and apply the 50Hz square signal to MULTI CHANNEL INPUT terminal of each channel.
Adjust the attenuator or Volume so that the output level becomes 35V p-p.
Confirm that the speaker relay does not turn OFF when a 3.0 ohm load is connected.
Confirm that the speaker relay turns OFF when a 1.0 ohm load is connected.



Differentiating Circuit

Test Mode

1. Turn POWER button on.
2. Press and hold down CD button, then press STANDBY/ON button.
3. After "Test - " on the FL tube is displayed, press CD button to set the unit to the test mode of FL tube.
   Note: DVD :Test- 1 VIDEO 1 :Test- 2
   VIDEO 2 :Test- 3 VIDEO 3:Test- 4

Change of item
Tone + ...UP
Tone - .....DOWN

Check of unit by test mode

Voltage detection circuit

Set the unit to "Test- 4-21".
The microprocessor checks the output voltage of all channels automatically
When the output voltage is abnormal, "Protect NG" is displayed on FL tube.
When the voltage of all channels is normal, "Test- 4-35" is displayed on FL tube.
4-21:FL 4-22:FR 4-23:C 4-24:SL 4-25:SR 4-26:SBL 4-27:SBR

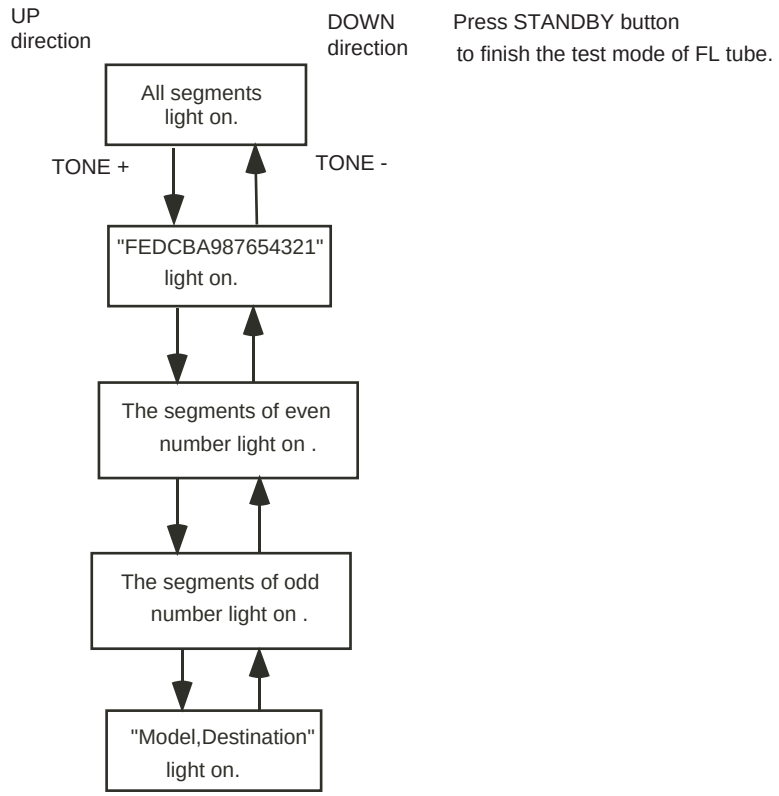
Current detection circuit

Set the unit to "Test- 4-35".
Connect the hollow resistor 3 ohm across the speaker terminal.
Check that the speaker relay turn On.
When connect the hollow resistor 1.5 ohm, check that the speaker relay turn Off.
Note: Check the all channels.

ADJUSTMENT AND CONFIRMATION PROCEDURES 3

FL tube

Press and hold down CD button, then press STANDBY/ON button.
After "Test - " on the FL tube is displayed, press CD button to set the unit to the test mode of FL tube.



Confirmation of voltage sensor and thermal protector

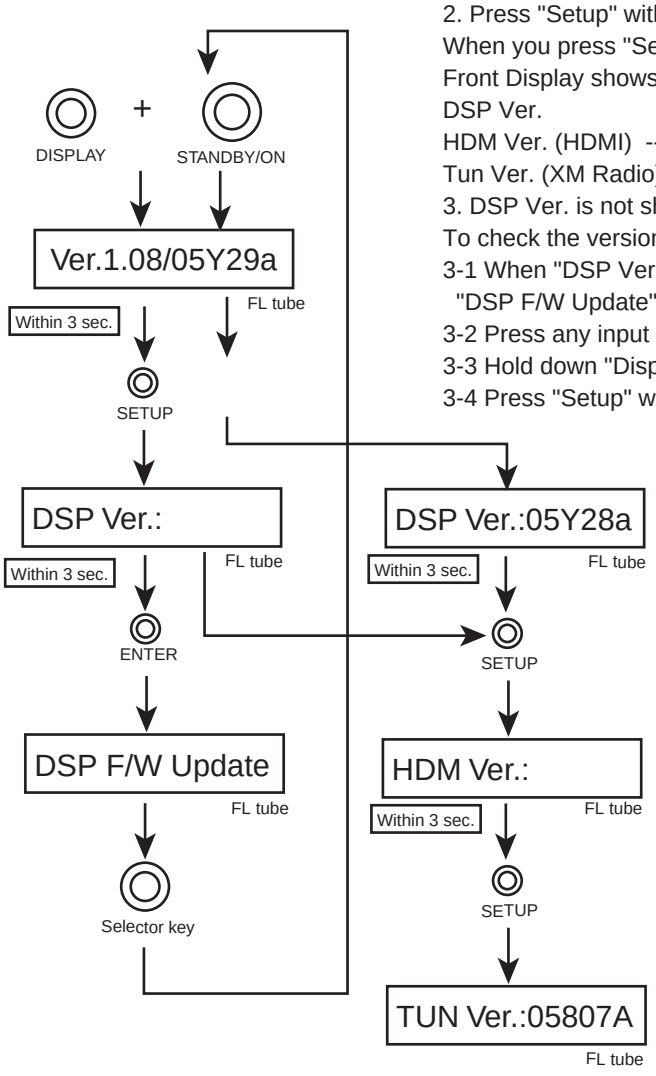
1. Set the unit to "Test- 4-36 " and "4-37".
   Confirm that FM STEREO is displayed and Speaker relays RL6901 and RL6902 turn Off.
2. Set the unit to "Test- 4-38 ".
   Confirm that FM STEREO is displayed and Speaker relays RL6901 and RL6902 turn Off.

Confirmation of cooling fan

1. Confirm that the fan does not rotate when no input signal.
2. Set the unit to "Test- 4-36 " and "4-37".
   Confirm that the fan rotates at a low speed.
3. Set the unit to "Test- 4-39 ".
   Confirm that the fan rotates at a high speed.

FW UPGRADE

How to check version



1. Hold down "Display" and then press "Standby" button to show Main version.
2. Press "Setup" within 3 seconds.
When you press "Setup", another version of program is shown.
Front Display shows each version of programs in the following order:
DSP Ver.
HDM Ver. (HDMI) -- blank
Tun Ver. (XM Radio) -- blank except MDD
3. DSP Ver. is not shown easily.
To check the version of DSP FW,
3-1 When "DSP Ver. " is shown, press "Enter" within 3 seconds.
"DSP F/W Update" will be shown.
3-2 Press any input selector button to exit "DSP F/W Update".
3-3 Hold down "Display" and then press "Standby" button to show Main version.
3-4 Press "Setup" within 3 seconds.

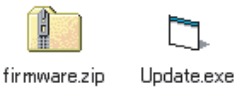
Main FW and DSP FW

1) **If both FWs need to be upgraded, DSP FW Upgrade should be done first.**
2) If either of Main Board or DSP Board is replaced, certain combinations of Main-DSP FW versions do not allow you to upgrade DSP FW.
In that case, rewrite a compatible version of Main FW, upgrade DSP FW, and then upgrade Main FW.
DSP: Ver.05723a - Main: Ver. 1.04/05921a,1.06/05X06b,
DSP: Ver. 05Y28a - Main: Ver. 1.08/05Y25a

FW UPGRADE

DSP/Video FW Upgrade

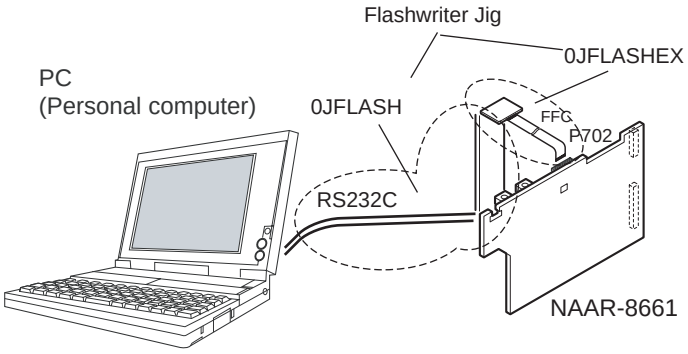
o. Unzip “firmware.zip” and store the unzipped folder & files and "Update.exe" as below.

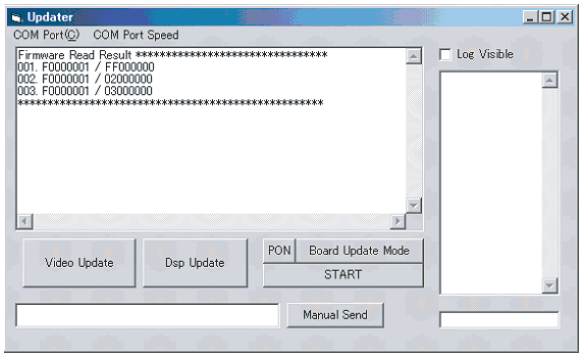


\Updater_SR803\Update.exe
\firmware\SR803\fdist.fdf
\FW803.dcf
\DSP7803_05Y28A.s28
\05X04B_video803.hex

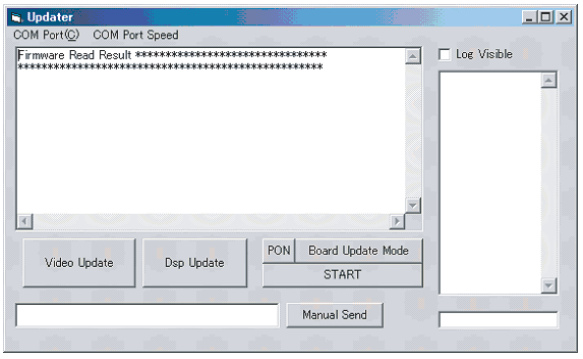
You can name the uppermost folder "\Updater_SR803" as you like.

1. Hold down "Display" and then press "Standby" button to show Main version.
2. Press "Setup" within 3 seconds.
3. Press "Enter" while DSP version is shown to enter Setup mode. "DSP F/W Update" will be shown.
4. Connect your unit and PC with Flashwriter Jig and put the unit into Standby mode.
5. Double-click "Update.exe".

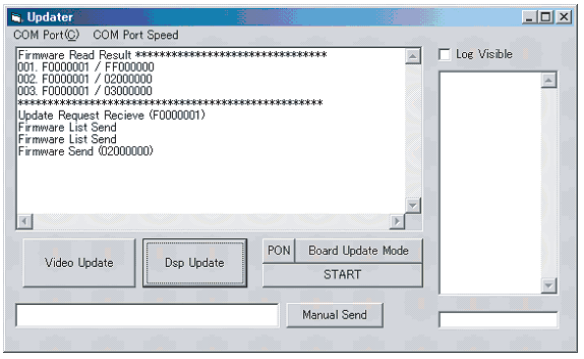




If you get the message like below, FW files are not properly stored. Check the path.



6. Click "DSP Updade" .
DSP

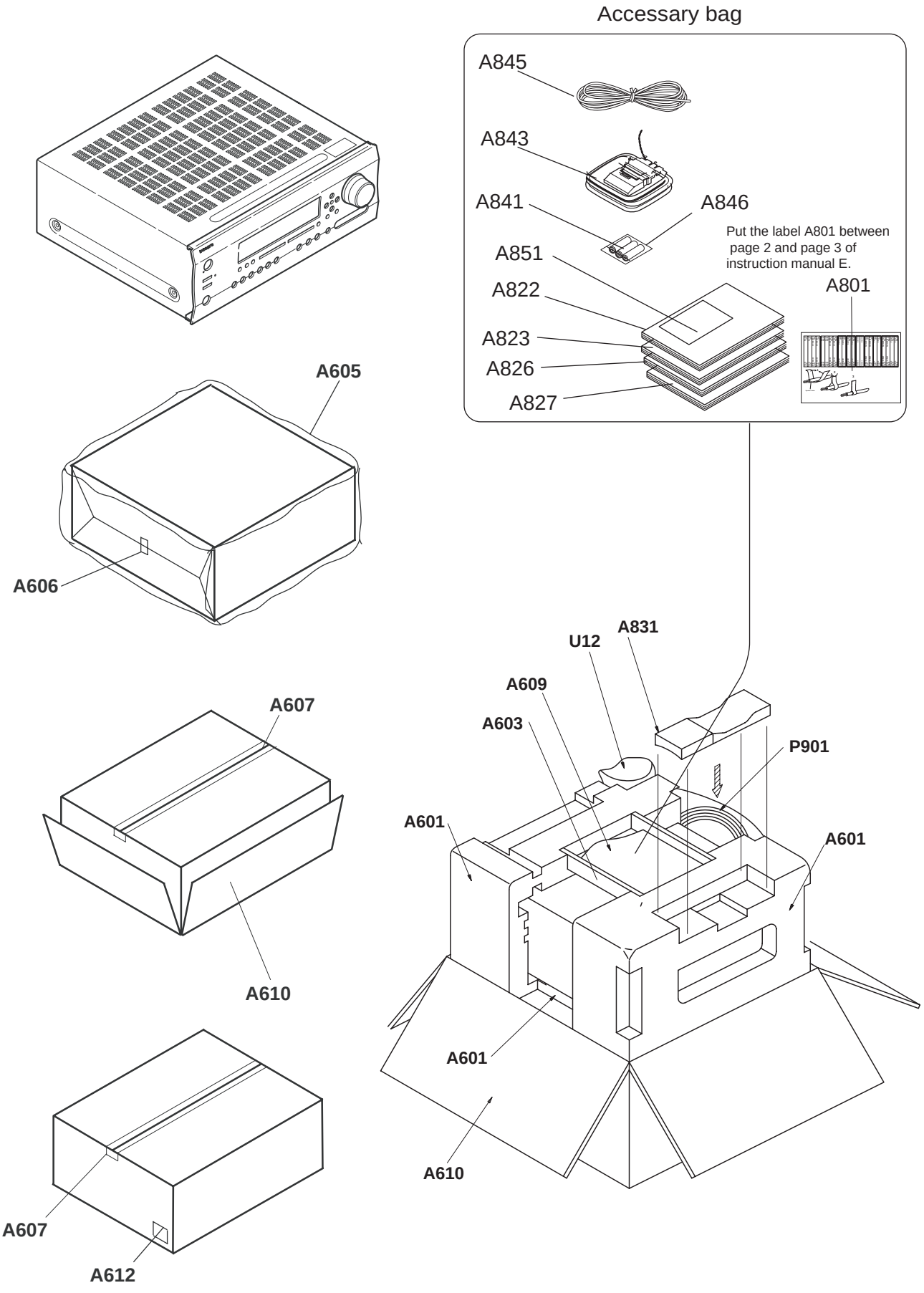


7. Update completes when Front Display stops showing the progress.

Note: Even if you try to check the DSP version, you might not be able to get is due to the wrong combination of DSP and Main.
In this case, check the version after upgrading Main FW.

Main FW Upgrade
Write the latest main program using FlashSta.exe.

PACKING VIEW



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Tel: 201-785-2600 Fax: 201-785-2650 http://www.integrahometheater.com

EXPLODED VIEW-PARTS LIST

NOTE: THE COMPONENTS IDENTIFIED BY MARK ! ARE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK. REPLACE ONLY WITH PART NUMBER SPECIFIED.

CAUTION: Replacement for transistor of mark *, if necessary must be made from the same beta group (h_{FE}) as the original type.

NOTE: <D>: USA model only <A>:Australian model only

REF.NO.	PART NO.	DESCRIPTION
A001	27111427A	Front bracket
A002	28325756	Knob, standby
A003	801618	3TTB+8B(CU)SR,Screw
A005	27268164	Guide, volume
A008	28133418	Back plate
A009	28192078	Clear plate
A010	27215377	Decorative frame
A011	28198905	Facet
A012	28141650	Cushion
A015	27141787	Retainer HP
A019	28135278	Badge
A020	28141562	t5*30*5,Cushion
A037	838430088GR	3TTB+8B(3BC),Screw
A040	28326231	Knob, volume
A044	28141637	Cushion
A050	27100468A	Chassis
A051	27130991A	Bracket FR
A052	27190470	KGLS-18S,Holder
A053	27190524	KGLS-14RT,Holder

A054	27190991	Holder
A055	260208	BSK-1,Wire tie
A056	830440089GR	4TTC+8C(3BC),Screw
A059	27190802	KGPS-14RF,Holder
A063	27270439	Spacer
A064	27190608-1	UA-0 V0,Clamp
A065	27270147	8X3X0.188,Spacer
A067	27131004	Bracket U
A068	880009	NRP-345,Plastic rivet
A077	801618	3TTB+8B(CU)SR,Screw
A080	27160565A	Heat sink
A081	29110083	Cloth tape
A082	801606	3SMH10W.SW+15B(CU),Screw
A083	29110083	Cloth tape
A087	27130745	Bracket
A089	28141585	W15*3t,Cushion
A090	27150507	Shield plate FFC
A095	28184952	Top cover
A096	28141563	t3*50*10,Cushion

A099	29364123	Label, cover
A100	838440089GR	4TTB+8C(3BC),Screw
A101	838430088GR	3TTB+8B(3CM),Screw
A105	801618	3TTB+8B(CU)SR,Screw
A110	29364345	Label PT
A111	27175418	Leg
A114	838430088GR	3TTB+8B(3BC),Screw
A115	27255004	CS-1U,Clip
A119	28141647	Cushion
A401	27123488	Rear panel <D>
	27123489	Rear panel <A>
A402	838430088GR	3TTB+8B(3BC),Screw
A405	838440089GR	4TTB+8C(3BC),Screw
A409	27270463	T0.5*Φ8*Φ3.5,Spacer
A410	27212844	Front panel <D>
	27212845	Front panel <A>

REF.NO.	**PART NO.**	**DESCRIPTION**
A420	29363195	Label, hookup <D>

F6901,F6	252301GF	!	12A-TUL-250V,Fuse <D>
F901	252078GF	!	5A-SE-EAK,Fuse <A>
	252330GF	!	10A-UL/T-233,Fuse <D>
F903	252075GF	!	2.5A-SE-EAK,Fuse <A>
	252326GF	!	5A-UL/T-233,Fuse <D>
F931,F93	252073GF	!	1.6A-SE-EAK,Fuse
F951,F95	252257GF	!	4A-T/UL-ST2,Fuse
P701	2047131012		NCFC7-131012,FFC
P7534	2045405512		NCFC5-405012,FFC
Q6050,Q6	2203666 (	*	MN130S-P or
Q6052,Q6	2202842 (	*	2SC5242-R or
Q6054	2202843 (	*	2SC5242-O or
Q6055	2203663 (	*	MN130S-O or
Q6056	2203664	*	MN130S-Y,Transistor
Q6050A	223024		AC238,Isolated plate
Q6060,Q6	2203676 (	*	MP130S-P or
Q6062,Q6	2202832 (	*	2SA1962-R or

Q6064	2202833 (	*	2SA1962-O or
Q6065	2203673 (	*	MP130S-O or
Q6066	2203674	*	MP130S-Y,Transistor
T901	2301806	!	NPT-1518P,Power transformer <A>
	2301828	!	NPT-1525D,Power transformer <D>
U02	1B104557-1D		NAVD-8657-1D, Video circuit PC board ass'y <D>
	1B104557-1H		NAVD-8657-1H, Video circuit PC board ass'y <A>
U03	1B104560-1P		NADG-8660-1P, DSP circuit PC board ass'y <D>

	1B104560-1Q	NADG-8660-1Q, DSP circuit PC board ass'y <A>
U032	1B104561-1P	NAAR-8661-1P,Main microprocessor PC board ass'y <D>
	1B104561-1Q	NAAR-8661-1Q,Main microprocessor PC board ass'y <A>
U04	1B104564-1U	NAPS-8664-1U, Primary circuit PC board ass'y <D>
	1B104564-1V	NAPS-8664-1V, Primary circuit PC board ass'y <A>

U042	1B104565-1U	NAPS-8665-1U, Secondary circuit PC board ass'y <D>
	1B104565-1V	NAPS-8665-1V, Secondary circuit PC board ass'y <A>
U043	1B104566-1U	NAETC-8666-1U, Speaker terminal PC board ass'y <D>
	1B104566-1V	NAETC-8666-1V, Speaker terminal PC board ass'y <A>

U044	1B104567-1U	NAETC-8667-1U, Speaker terminal C PC board ass'y <D>
	1B104567-1V	NAETC-8667-1V, Speaker terminal C PC board ass'y <A>
U045	1B104568-1U	NAAF-8668-1U, Driver circuit PC board ass'y <D>
	1B104568-1V	NAAF-8668-1V, Driver circuit PC board ass'y <A>
U048	1B104571-1U	NAETC-8671-1U,AC inlet PC board ass'y <D>

	1B104571-1V	NAETC-8671-1V,AC inlet PC board ass'y <A>
U049	1B104573-1U	NAPS-8673-1U,Transformer terminal PC board ass'y <D>
	1B104573-1V	NAPS-8673-1V,Transformer terminal PC board ass'y <A>
U06	1B104578-1G	NAAF-8678-1G, Amplifier PC board ass'y
U062	1B104580-1G	NAETC-8680-1G,Thermal detector PC board ass'y
U063	1B104581-1G	NAETC-8681-1G,Holder PC board ass'y

U064	1B104582-1G	NAAF-8682-1G,Surround back amplifier PC board ass'y
U065	1B104579-1G	NAPS-8679-1G,Transformer terminal PC board ass'y
U07	1B104583-1B	NADIS-8683-1B,Display circuit PC board ass'y
U072	1B104584-1B	NAETC-8684-1B,Front video PC board ass'y
U073	1B104585-1B	NCETC-8685-1B,Headphone terminal PC board ass'y
U075	1B104587-1B	NAETC-8687-1B,Volume PC board ass'y

U076	1B104521-1B	NAETC-8721-1B,Holder PC board ass'y
U077	1B104522-1B	NAETC-8722-1B,Holder PC board ass'y
U08	1B104588-1A	NARF-8688-1A,XM radio PC board ass'y <D>
U11	240155	FAE485-E12EX,Tuner unit <A>
	240152 or	FAE385-A11US or
	240156	ENG06507QFUS,Tuner unit <D>

PACKING VIEW-PARTS LIST

NOTE: THE COMPONENTS IDENTIFIED BY MARK ! ARE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK. REPLACE ONLY WITH PART NUMBER SPECIFIED.

NOTE: <D>: USA model only <A>:Australian model only

REF.NO.	PART NO.	DESCRIPTION
A601	29092286A	Pad

A603	29054470	Carton, accessory
A605	29100153	1020x770,Polybag
A606	29110149	Cellophane tape
A607	29110148	Tape PP
A609	29100097-1A	350*250,Polyabg
A610	29054448A	Carton box <D>
	29054467A	Carton box <A>
A612	29364238	Label EAN <A>
	29364242	Label UPC <D>
A801	29363059A	Label, cable SP
A822	29344101	Instruction manual En
A823	29344102	Instruction manual, digest
A826	29344100	Instruction manual U9
A827	29355538	Instruction sheet XM <D>
A831	24140631	RC-631M,Remote control

A841	3010358		LR6/AA(UM-3),Battery
A843	232140		NMA-3057,AM loop antenna
A845	292191		FM antenna
A846	29100217		t0.1*70*100,Polybag
A851	29365089A		Warranty card <D>
P901	253297KA	!	AS-UC-2 or
	253352TE	!	AS-UC-2,Power supply cord <D>
	253391VC	!	AS-SAA,Power supply cord <A>
U12	1B068MIC		MIC-5000,Microphone