

ONKYO® SERVICE MANUAL

QUARTZ SYNTHESIZED

FM STEREO TUNER

MODEL T-9060

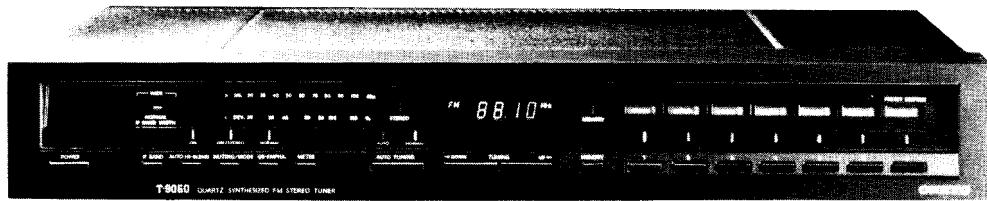


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ONKYO®
AUDIO COMPONENTS

SPECIFICATIONS

D model	
Tuning Range:	87.9 – 107.9 MHz (200 kHz steps)
Usable Sensitivity:	Mono: 10.3 dBf, 1.8 μ V Stereo: 17.2 dBf, 4.0 μ V
50 dB Quieting Sensitivity:	Mono: 14.7 dBf, 3.0 μ V Stereo: 36.1 dBf, 35 μ V
Capture Ratio:	1.0 dB
Image Rejection Ratio:	100 dB
IF Rejection Ratio:	100 dB
Signal-to-Noise Ratio:	Mono: 81 dB (IHF) Stereo: 73 dB (IHF)
Alternate Channel Att.:	80 dB IHF (\pm 400 kHz IF: Normal)
AM Suppression Ratio :	55 dB
Total Harmonic Distortion:	Mono: 0.05% (IF: Wide) Stereo: 0.13% (IF: Wide)
Frequency Response:	30 – 15,000 Hz (+ 0.5 dB, -1.5 dB)
Stereo Separation :	45 dB at 1 kHz (IF: Wide) 33 dB at 70 – 10,000 Hz (IF : Wide)
Output Voltage :	0 – 1.5V
Muting Level:	17.2 dBf, 4.0 μ V
General	
Power Supply:	AC 120V, 60Hz
Antennas:	300 ohms balanced and 75 ohms unbalanced
Semiconductors:	8 FETs, 43 transistors, 18 ICs, 61 diodes, 30 LEDs
Dimensions (W x H x D):	450 x 74 x 355 mm (17-3/4" x 2-29/32" x 13-31/32")
Weight:	5.6 kg, 12.3 lbs.

Specifications and features are subject to change without notice.

G/W model	
Tuning Range:	87.5 – 108.0 MHz (50 kHz steps)
Usable Sensitivity:	Mono: 10.3 dBf, 1.8 μ V, IHF 1.4 μ V (S/N 26 dB, 40kHz Dev.) DIN
50 dB Quieting Sensitivity:	Stereo: 17.2 dBf, 4.0 μ V, (IHF) 50 μ V (S/N 46 dB, 40 kHz Dev.) DIN
Capture Ratio:	Mono: 14.7 dBf, 3.0 μ V Stereo: 36.1 dBf, 35 μ V
Image Rejection Ratio:	1.0 dB
IF Rejection Ratio:	100 dB
Signal-to-Noise Ratio:	100 dB
Selectivity:	Mono: 81 dB (IHF) Stereo: 73 dB (IHF) 70 dB DIN (\pm 300 kHz, 40 kHz Dev.) (IF: Normal)
AM Suppression Ratio:	55 dB
Total Harmonic Distortion:	Mono: 0.05% (IF: Wide) Stereo: 0.13% (IF: Wide)
Frequency Response:	30 – 15,000 Hz (+ 0.5 dB – 1.5 dB)
Stereo Separation:	45 dB at 1 kHz (IF: Wide) 33 dB at 70 – 10,000 Hz (IF: Wide)
Output Voltage:	0 – 1.5 V
Muting Level:	17.2 dBf, 4.0 μ V
General	
Power Supply:	AC 120/220 Volts, 50/60Hz AC 220 Volts, 50Hz
Antennas:	300 ohms balanced and 75 ohms unbalanced
Semiconductors:	8FETs, 43 transistors, 18 ICs, 62 diodes, 30 LEDs
Dimensions (W x H x D):	450 x 74 x 355 mm (17-3/4" x 2-29/32" x 13-31/32")
Weight:	5.6 kg, 12.3 lbs.

Specifications and features are subject to change without notice.

PRECAUTIONS

1. Handling precautions of CMOS IC

1. All MOS devices should be stored or transported in materials that are somewhat conductive. MOS deivces must not be inserted into conventional plastic "snow" or plastic trays.
2. All MOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface.
3. Nylon clothing should not be worn while handling MOS circuits.
4. When lead straightening or hand soldering is necessary, provide ground straps for the apparatus used.
5. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.
6. All unused device inputs should be connected to V_{DD} or V_{SS}.

2. De-Emphasis Switch (bottom panel)

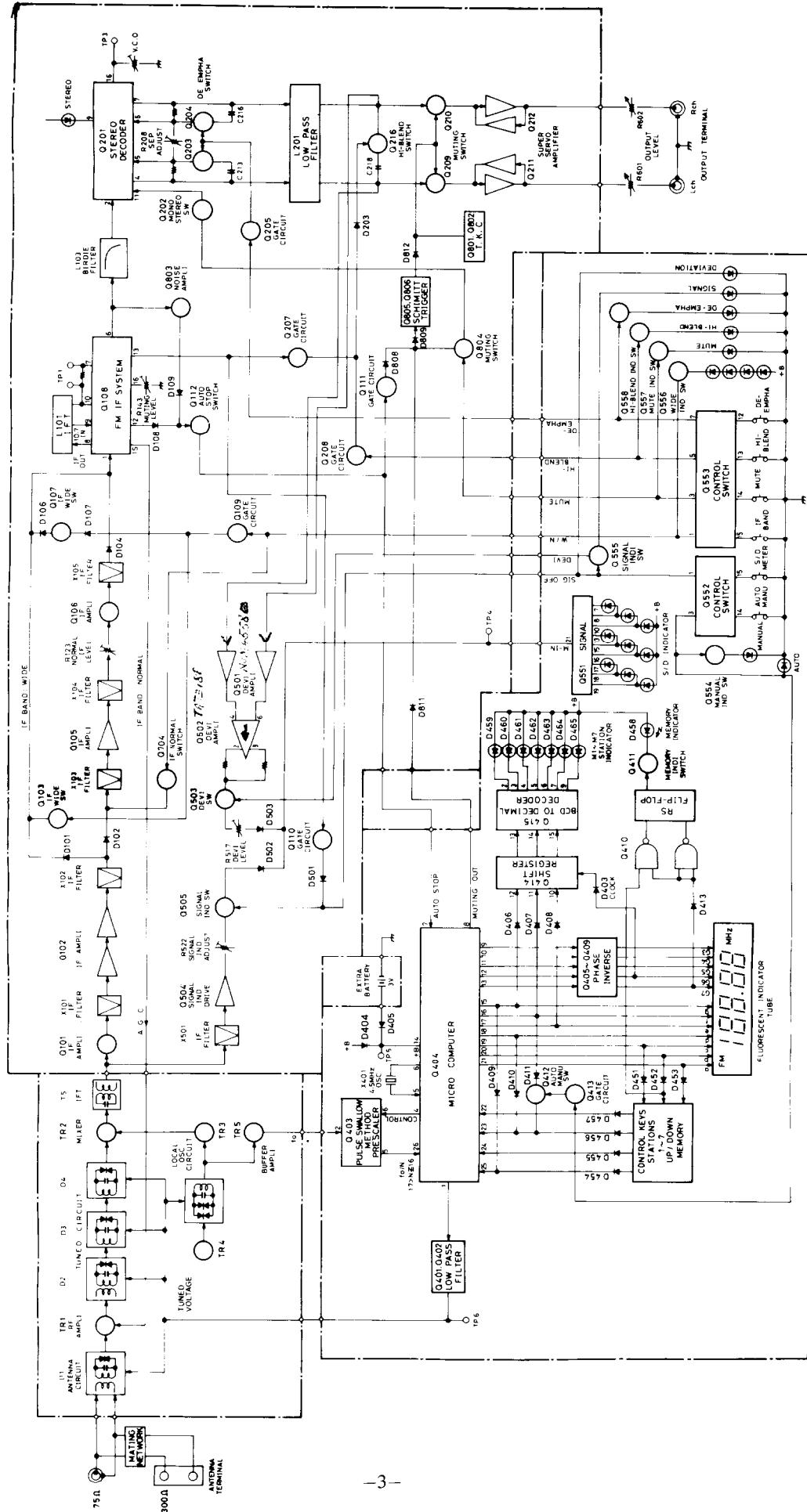
W models are equipped with a 50 μ sec – 75 μ sec selector switch. This is set to 50 μ sec at the factory, but may have to be reset to 75 μ sec depending on the area where the unit is used.

Europe:	50 μ sec
U.S.A.:	75 μ sec

3. FM Tuning Step Frequency Switch (back panel)

W models are equipped with a switch to change the FM tuning step frequency from 50 kHz to 200 kHz. These units are set to 50 kHz at the facotry; change to 200 kHz if this gives better results in your locality.

BLOCK DIAGRAM



CIRCUIT DESCRIPTION AND IC BLOCK DIAGRAMS

1. Micro Computer Operation

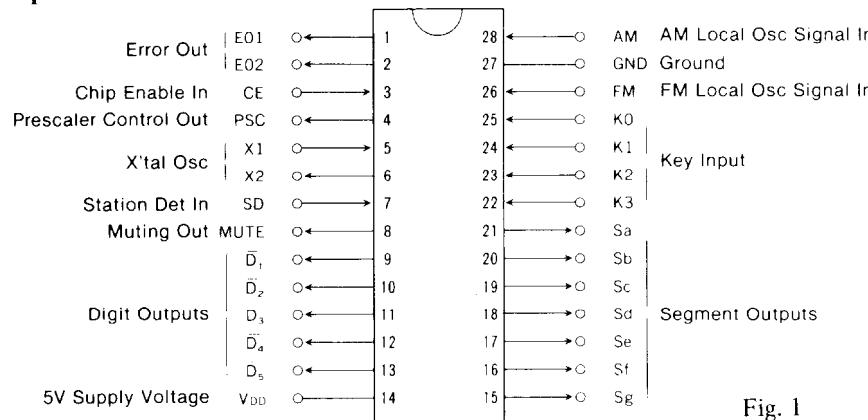


Fig. 1

Pin. No.	Symbol	Terminal	Description
1 2	E01 E02	Error Outputs	Charge pump output of the phase detector which constitutes the PLL. HIGH level is output when the divided oscillation frequency is higher than the reference frequency. In the opposite case, LOW level is output. Floating occurs when the frequencies match. The output is applied to the variable capacitor in the front end through low pass filters Q401 and Q402. The output from both terminals is the same, but only E01 is used.
3	CE	Chip Enable Input	Device selection signal input terminal. HIGH level...normal operation; LOW level...memory preservation.
4	PSC	Preset Control Output	This terminal outputs a signal that switches the prescaler division ratio to 1/16 or 1/17 when the pulse swallow method is used for division (FM only).
5 6	X1 X2	X'tal	Connected to the 4.5MHz crystal oscillator.
7	SD	Station Detector Input	Input terminal for detecting whether or not a broadcast signal is being received during auto-tuning. Stopped by the HIGH level.
8	MUTE	Muting Output	Output terminal which mutes the shock noise occurring when the PLL is released; active HIGH.
9—13	D1—D5	Digit Outputs	Display digit output signal terminals; active LOW.
14	VDD	Supply Voltage	Device power terminal; supplies 5V during normal operation and 3V from the external power source (two batteries) for memory preservation.
15—21	Sa—Sg	Segment Outputs	Display tube segment signal output, key return signal source and station display signal terminals; active HIGH. Since these terminals can handle 30V, they are connected directly to the segment terminals of the fluorescent display tubes.
22—25	K0—K3	Key Return Signal Inputs	Terminals for input of the key return signals from the external key matrix.
26	FM	FM Local Oscillator Signal Inputs	FM signals received are divided by 1/16 or 1/17 by prescaler μPB553AC for input to this terminal.
27	GND	Ground	
28	AM	AM Local Oscillator Signal Input	Terminal for input of AM broadcast signal. (not used.)

2. Control Key Connections

UP, DOWN.....Pressing the UP or DOWN key will cause the frequency to be shifted upward or downward (in 200kHz steps with the D model and in 50kHz steps with the W/G model). If the key is pressed for more than 0.5 seconds, the frequency will be shifted 50kHz every 40ms until it is released. (manual operation)

If the key is pressed, the frequency will be shifted until the terminal SD becomes the high level. (auto operation)
MW, FM, LW.....The MW, FM, LW band switches.

MEMORY.....Pressing this key causes the memory to be placed in the write-enabled state. The frequency displayed will be stored in one of the memories 1–7 if the corresponding memory key is then pressed within 5 seconds. The write-enabled state will be cleared after 5 seconds if none of the memory keys are pressed, or if the UP/DOWN keys are pressed.

M1–M7.....These keys are used to preset and recall the contents of the memory. Positions are provided for keys for reading/writing up to 7 frequencies. See the paragraph on MEMORY for writing frequencies. Pressing one of the keys M1–M7 once will cause the contents of the corresponding memory (a frequency) to be read. A muting signal of about 0.45 seconds duration is output at this time.

TPP (Tracking Point Preset).....Switch is used to write adjustment frequencies into preset memory during set production. Not used with the T-9060. When the IC V_{DD} is first inserted, the lowest FM frequency is placed in the memory.

3. Key Matrix Connections

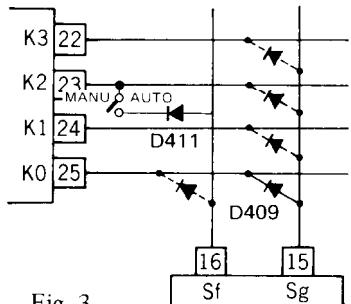


Fig. 3

Not used
High level when the diode is connected

D409 is not used for 120V model.

Input Terminal	K0 (25)	K1 (24)	K2 (23)	K3 (22)
Sf (16)	9kHz/10kHz		AUTO/MANU	
Sg (15)	BAND 0	BAND 1	IF 1	IF 0

table 1

IF1, IF0.....IF offset value settings for FM. See Table 2.

BAND1, BAND0.....Geographical FM band settings. See Table 3.

9kHz, 10kHz.....MW band settings. See Table 4. (not used)

AUTO/MANUAL.....Auto tuning for 1, manual tuning for 0.

IF 1	IF 0	IF Frequency
0	0	10.700MHz
0	1	10.675MHz
1	0	10.750MHz
1	1	10.725MHz

table 2

BAND 1	BAND 0	Band	Frequency Range	Channel Space
0	0	120V model	87.9~107.9MHz	200kHz
0	1	220V model	87.50~108.00MHz	50kHz
1	0	Japan	76.1~89.9MHz	100kHz

table 3

9kHz/10kHz	Frequency range	Channel Space	Reference Frequency
0	530~1620kHz	10kHz	10kHz
1	522~1611kHz	9kHz	9kHz

table 4

4. Auto/Manual tuning circuit

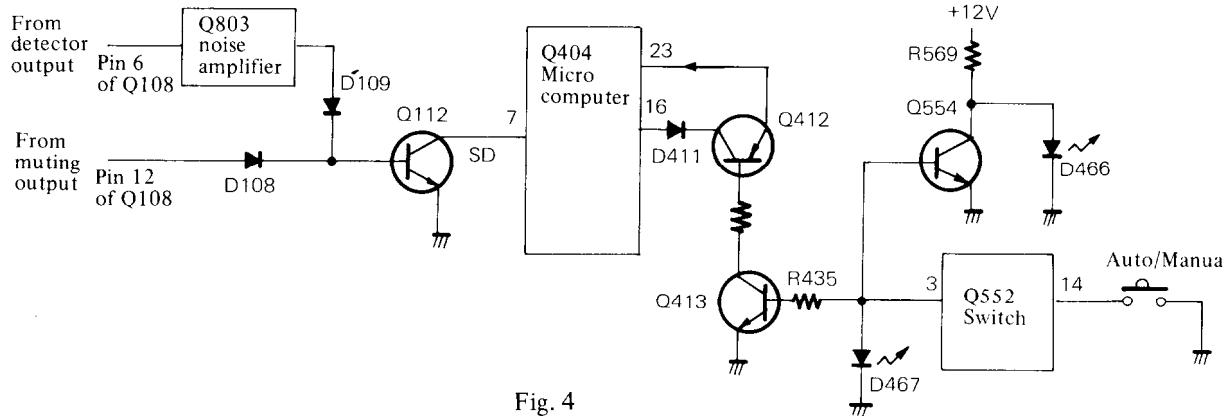


Fig. 4

Detector section

The auto stop detector circuit is activated by the combined effects of the IF level, zero cross detector and noise component. The IF level and zero cross detectors are incorporated in the quadrature IC Q108; output is from pin 12. When the sufficiently strong broadcast is received during the auto tuning, the outputs of noise amplifier and muting of Q108 go the low level and transistor Q112 is turned OFF. The terminal SD goes the high level and auto tuning stop.

Switch section

When the power switch is turned on, the pin 3 of Q552 goes the low level and the tuning switch goes in the manual mode. The pin 3 goes the high level when the auto tuning button is pressed, the transistors Q413 and Q412 are turned on and the tuning becomes the auto mode.

5. Preset Station Indicator Circuit

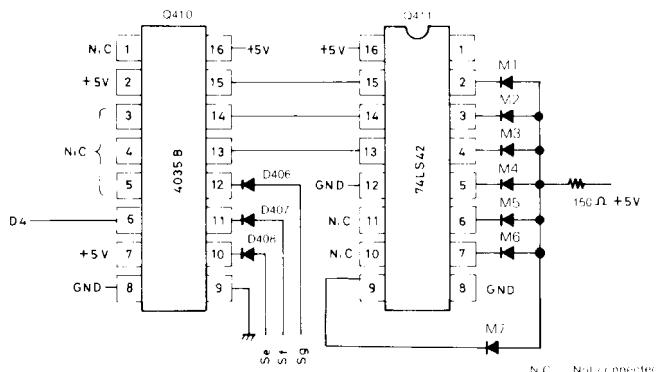


Fig. 5

Preset station indicator connections are shown in Figure 5. BCD codes are output from segment terminals Se—Sg in synchronization with the timing of digit signal D4. The sequence is shown in the timing chart in Figure 6. The display signal for the "1" in the first digit of the frequency display is output from segment terminals Sb and Sc at timing T1 of digit signal D4 (blank codes are output from segment terminals Se—Sg at this time). At timing T2, the BCD code

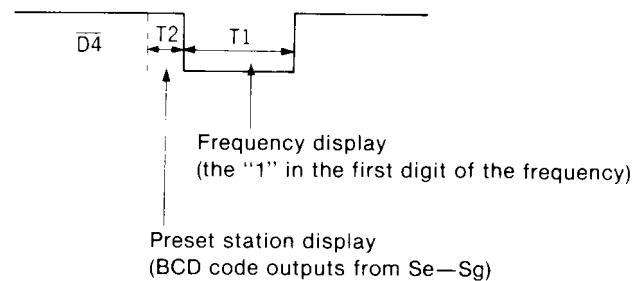
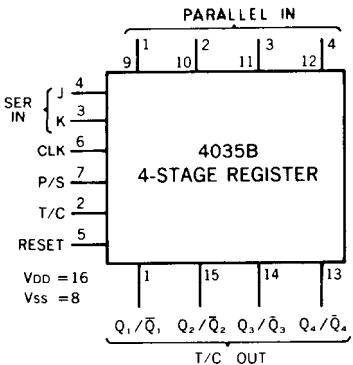


Fig. 6

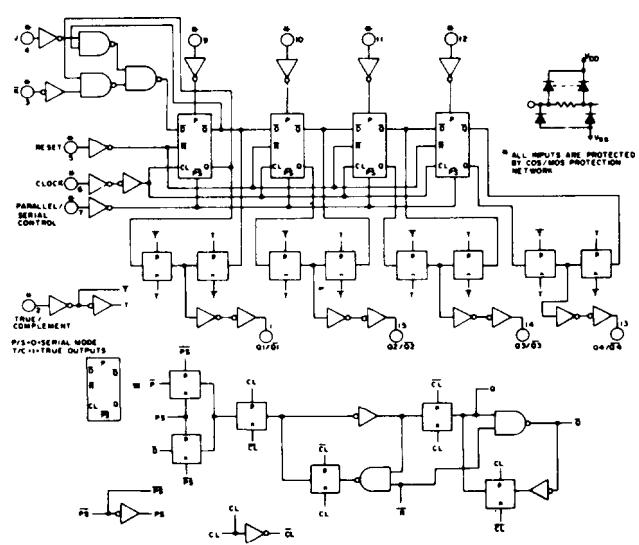
for preset station display is output from segment terminals Se—Sg (at this time, blank codes are output from segment terminals Sa—Sd). Since output is timed as shown in Figure 6, it is replaced with starting output at D—F/F of Q411. This is output as BCD code to the decimal counter to display the frequency.

•4035B (4-Stage Parallel-In/Parallel-Out Shift Register with J-K Input and True/Complement Output)



Pin Connection Diagram

Fig. 7



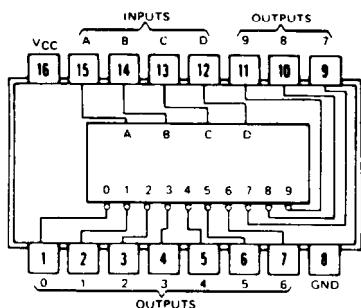
Logic Diagram

Fig. 8

	i_{n-1} (INPUTS)				i_n (OUTPUTS)
CL	J	K	R	Q_{n-1}	Q_n
/	0	X	0	0	0
/	1	X	0	0	1
/	X	0	0	1	0
/	1	0	0	Q_{n-1}	Q_{n-1} TOGGLE MODE
/	X	1	0	1	1
/	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	I	X	0

First Stage Truth Table

•74LS42 (BCD to DECIMAL Decoder)

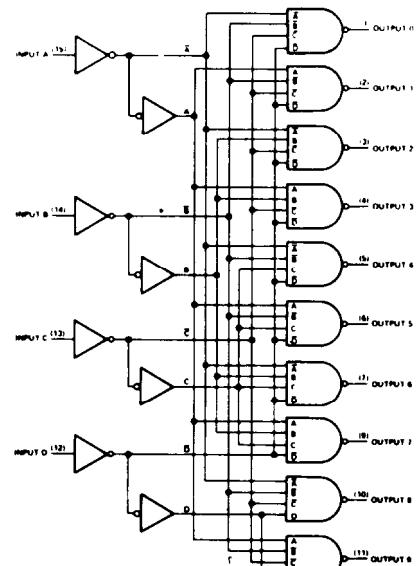


Pin Connection Diagram

Fig. 9

NO	INPUTS				OUTPUTS								
	D	C	B	A	0	1	2	3	4	5	6	7	8
0	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H
3	L	L	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H
7	L	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H
INVALID	H	H	L	H	H	H	H	H	H	H	H	H	H

Function Table



Logic Diagram

Fig. 10

6. PLL Tuned Circuit

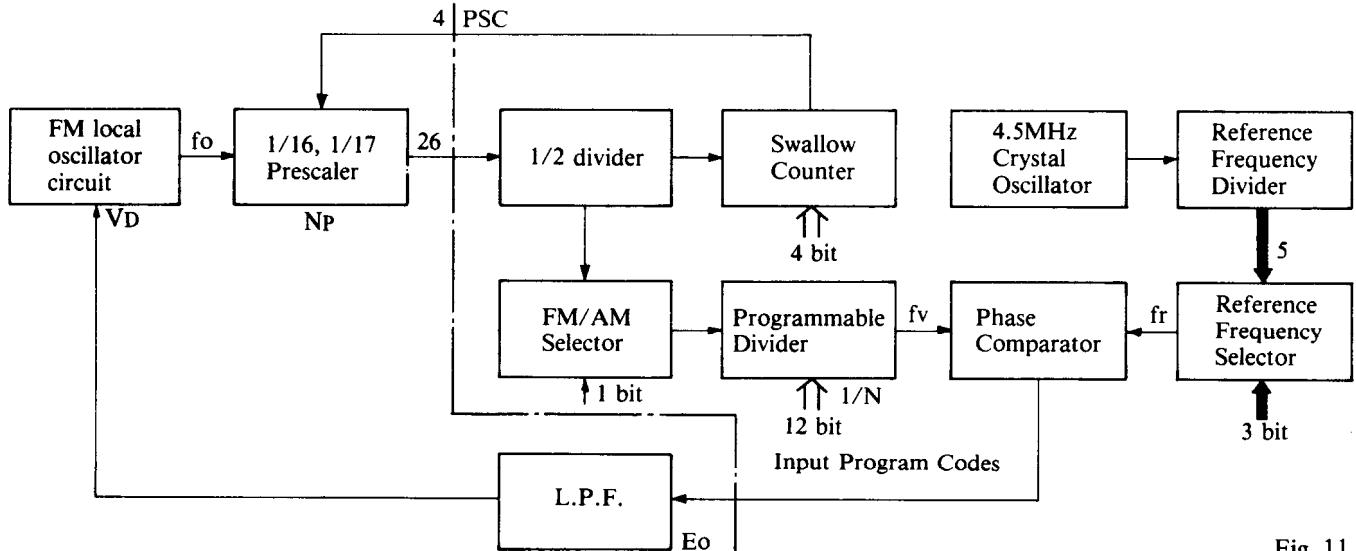


Fig. 11

A block diagram of the tuned circuit of the PLL is shown in Figure 11.

The pulse swallow method is used in the prescaler of the T-9060. In this type of prescaler, a supplementary number (changed according to the program code input) and the divided reception frequency from the prescaler are combined in the control counter and the prescaler's division factor is switched between 1/16 and 1/17 according to external control (1/17 when the PSC terminal is "H" and 1/16 when it is "L").

The station oscillation frequency is applied to the programmable divider, but the programmable divider has an upper frequency limit of only 30MHz, so the pulse swallow-type prescaler, which can be used up to 150MHz, is inserted for division to $1/N_p$.

The signal is then divided to 1/2 in the microcomputer and applied to the programmable divider and divided to $1/N$.

This is applied to the phase detector where it is compared with frequency standard f_r (25kHz). If f_r and f_v differ, E_o equal to the difference in frequency is output. Since error output E_o is a pulse waveform, it is passed through the low pass filter to change it into DC voltage V_D , which is applied to the variable capacitor in the front end to change the reception frequency. This continues until f_v and f_r are the same and $E_o=0$.

μ PB533AC (Prescaler)

Block Diagram

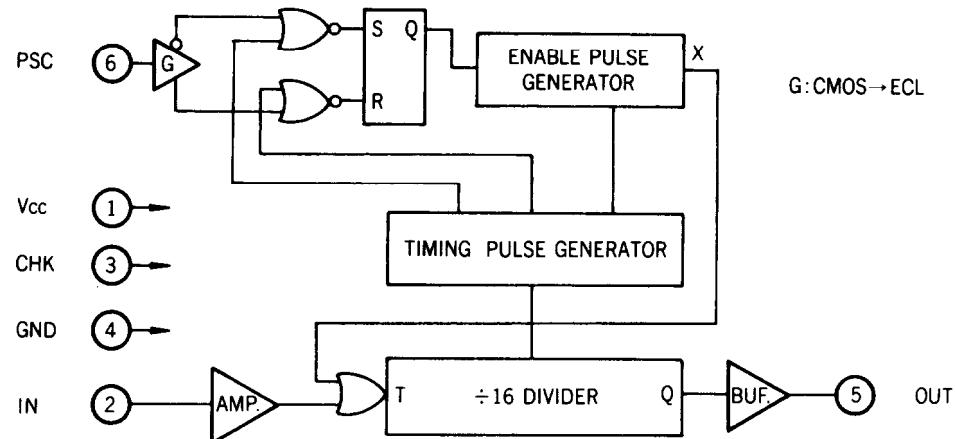


Fig. 12

Pin Connection

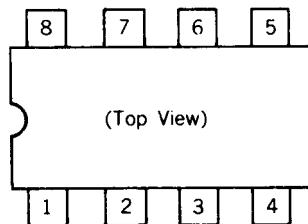


Fig. 13

1. Pin 1 (Vcc)..... + 5 volts supply
2. Pin 2 (IN).....FM local oscillator signal input
3. Pin 3 (CHK).....Check terminal
4. Pin 4 (GND).....Ground terminal
5. Pin 5 (OUT).....Prescaler terminal
6. Pin 6 (PSC).....Prescaler control terminal
7. Pin 7,8.....Not connected

Timing Chart

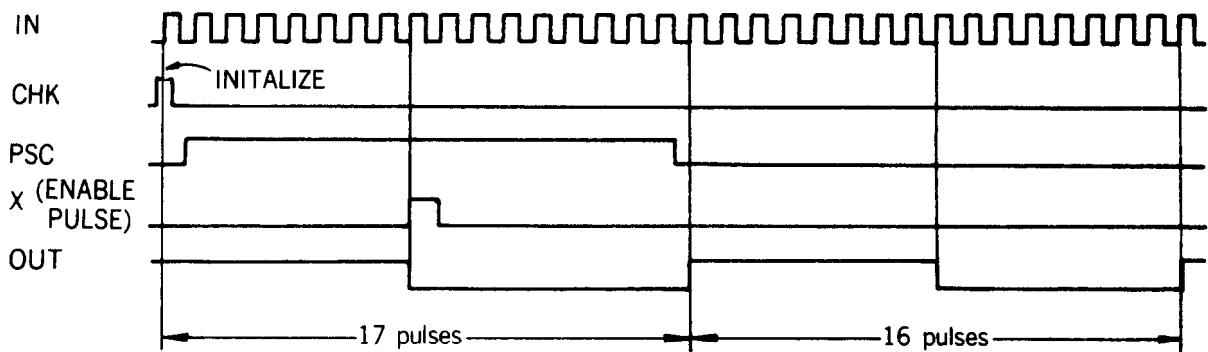


Fig. 14

LA1222 (IF ampli.)

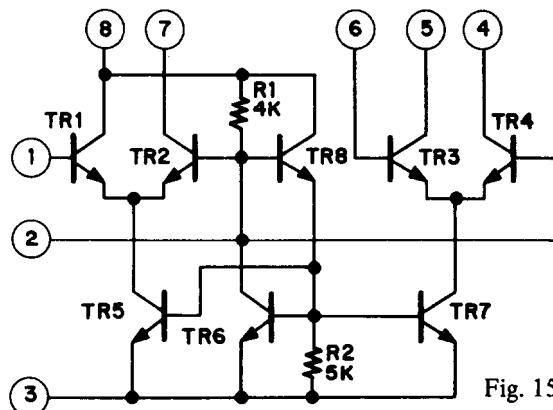


Fig. 15

μ PC555H (IF ampli.)

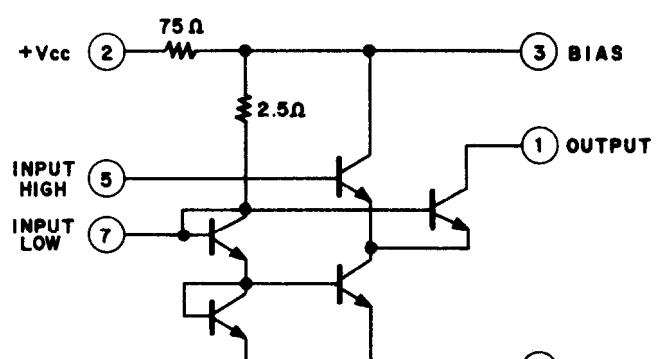


Fig. 16

4011 (Quad, 2-Input NAND gate)

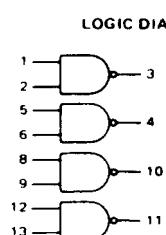
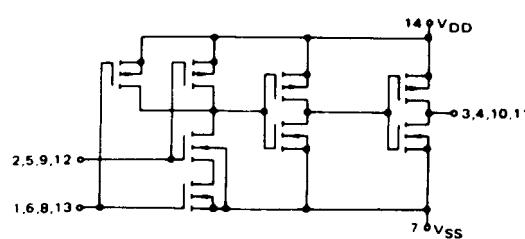
CIRCUIT SCHEMATICS
(1/4 of Device Shown)

Fig. 17

7. Muting Circuit

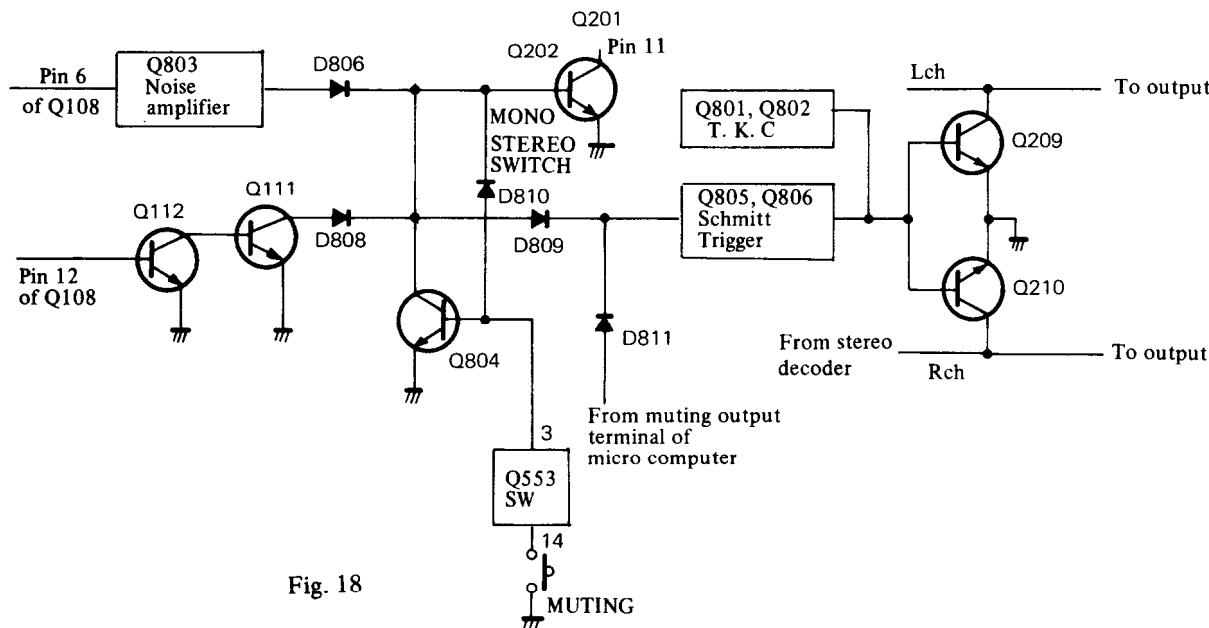


Fig. 18

The muting circuit is activated by the combined effects of the IF component, noise component, and zero cross detector output.

The IF level detector and zero cross detector circuit are incorporated in the IF system IC of Q108, the output appearing at pin 12.

R143 is the variable resistor used to set the muting level, and is set so that muting opens at 17dBf. When the antenna input level exceeds 17dBf, transistor Q112 is turned OFF, Q111 is turned ON.

When the noise amplifier does not detect the noise component above 70kHz in the composite signal, the output becomes the low level.

Consequently, when all detector circuit outputs are switched to low level, the transistor Q805 is cut off, the transistor Q806 is on, and Q209 and Q210 is cut off so that the FM signal is output from the output terminal. At the same time, Q202 is cut off, resulting in the STEREO indicator turning on (if the tuned station is broadcasting in stereo.)

When the STATION, UP to DOWN switches are operated, the pulses shown in Figure 19 are output from pin 8 of Q404 and muting is activated.

HA11225 (FM IF system)

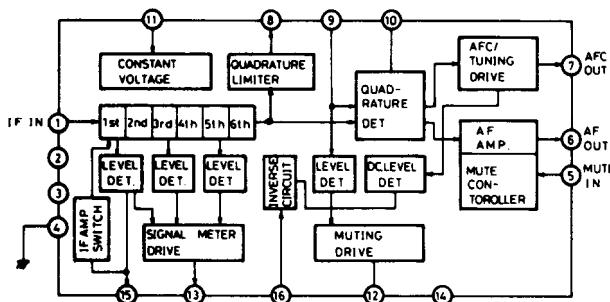


Fig. 20

- ⑧ FM IF output
- ⑨ 10.7MHz signal input
- ⑩ Reference voltage
- ⑪ Muting output
- ⑫ Signal indicator output
- ⑬ AGC output
- ⑭ Muting level input

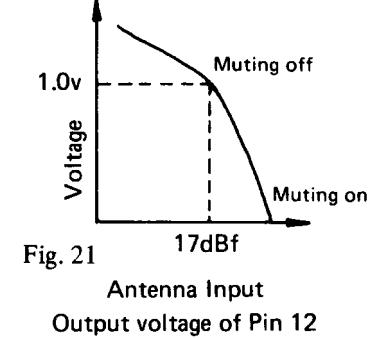
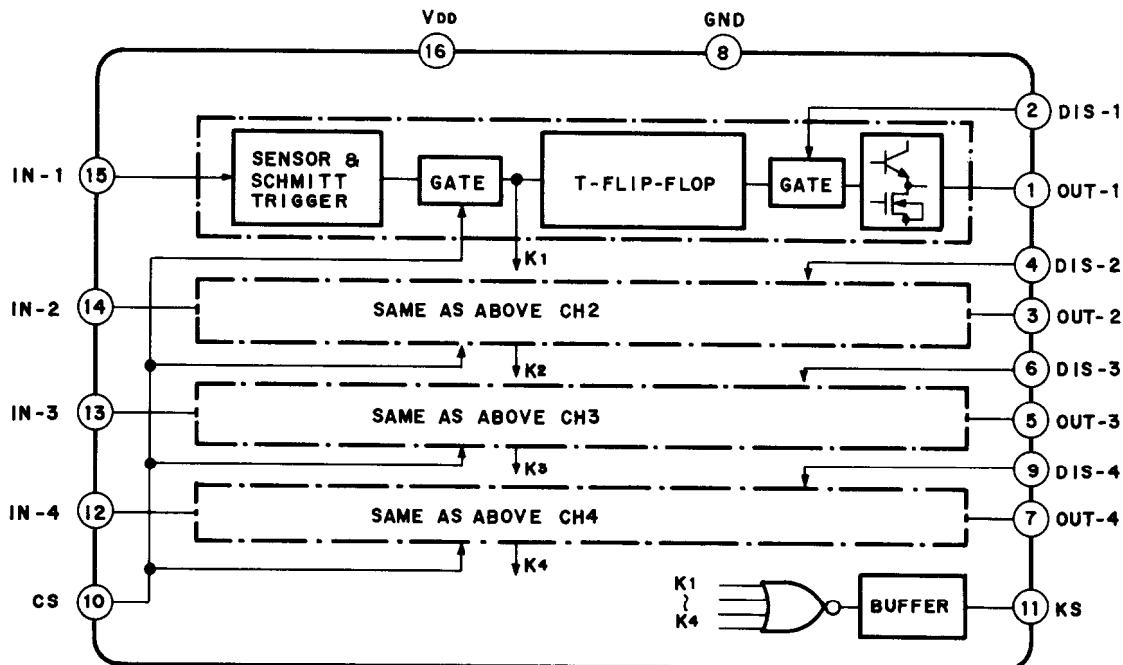


Fig. 21
Antenna Input
Output voltage of Pin 12

TC9130P

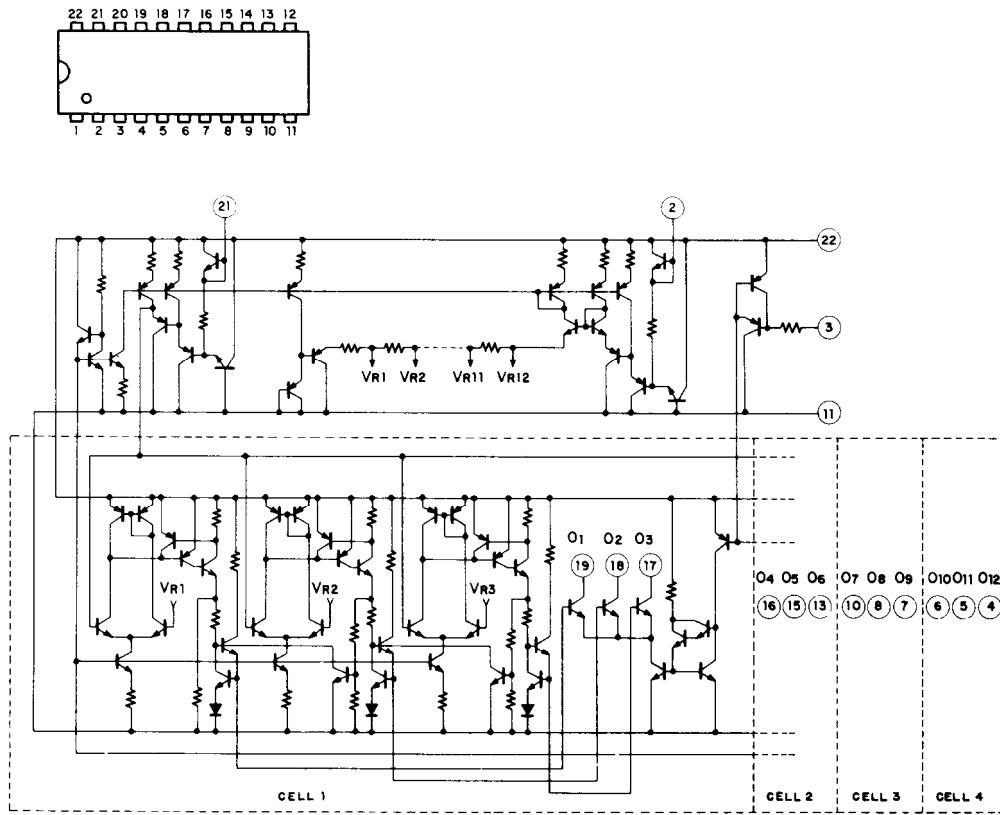


Pin nos.	Mark	Terminal	Descriptions
15 12	IN-1 IN4	Input signal	When the supply voltage of this terminal changes from the high level to low level, the output terminal does the inversion.
1, 3 5, 7	OUT-1 OUT-4	Output	
2, 4 6, 9	DIS-1 DIS-4	Output forbidden	When this terminal does the low level, the output becomes the low level.
10	CS	Input forbidden	When this terminal does the low level, the acceptances of input terminals are forbidden. And the flip-flop of inner holds the before condition.
11	KS	Input detector	When the input terminal becomes the low level, this terminal becomes the low level.
16	V _{DD}	Power supply	
8	GND	Ground	

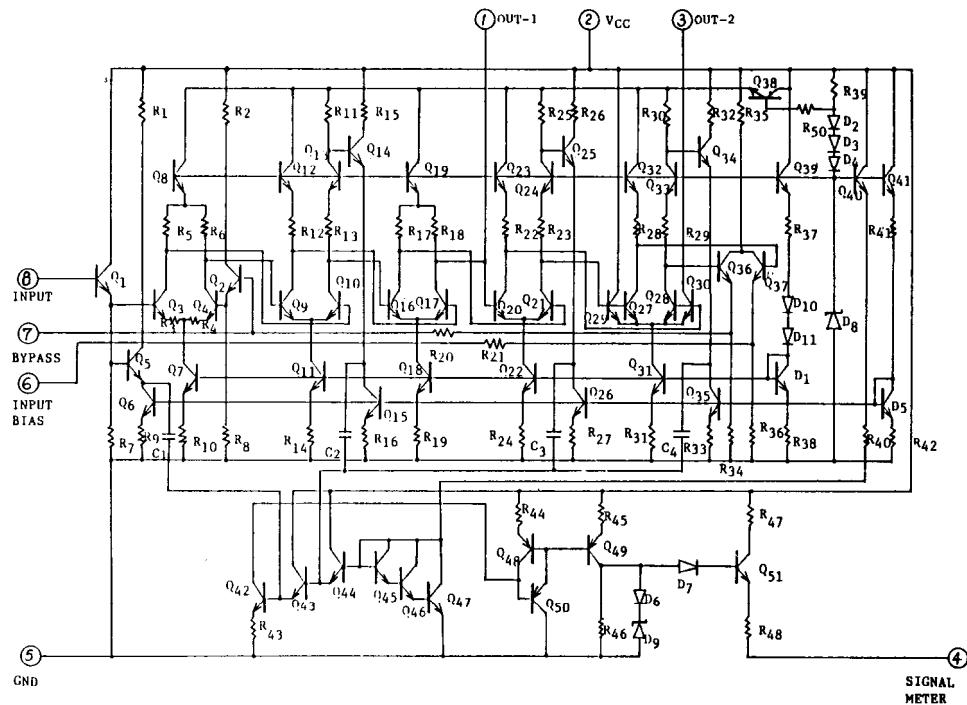
The switch mode when the power switch is turned on.

AUTO TUNING	NORMAL
METER	SIGNAL STRENGTH
IF BAND	NORMAL
MUTING	MUTE ON/STEREO
HI-BLEND	ON
DE-EMPHASIS	NORMAL

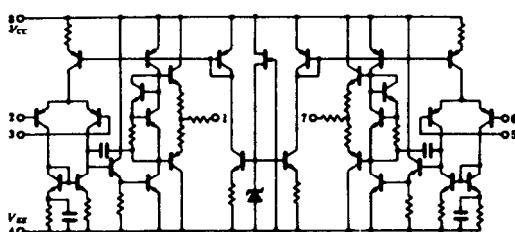
IR2433 (Output Power Indicator Drive)



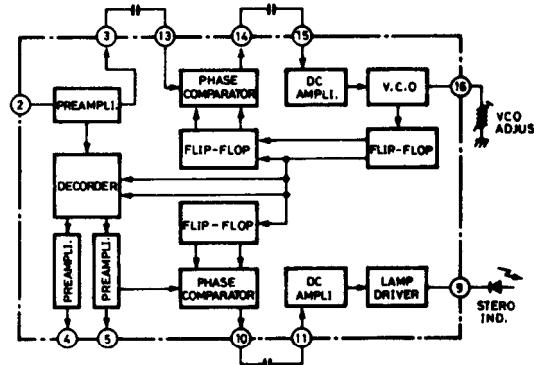
μ PC1198H (Signal Meter Driver)



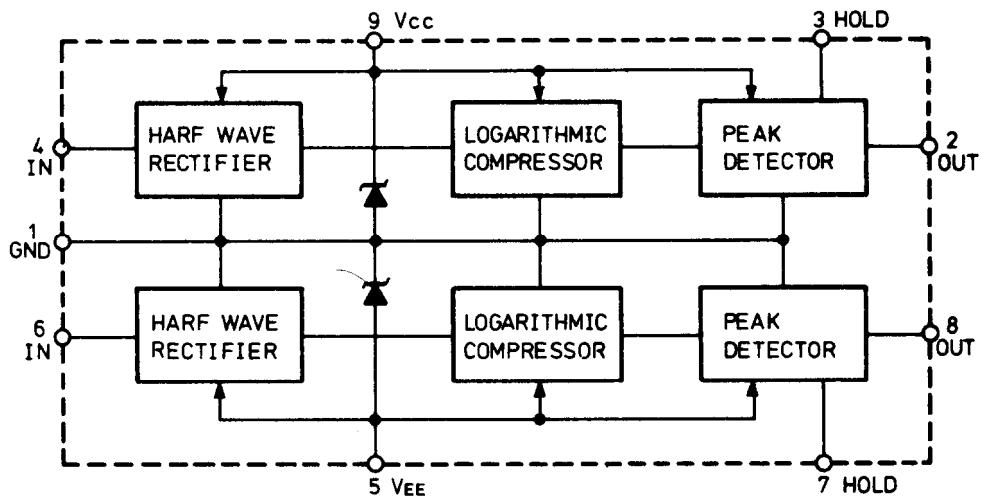
NJM4558D



HA12016 (Stereo decoder)



TA7318P (Deviation indicator driver)



ALIGNMENT PROCEDURES

INSTRUMENTS REQUIRED

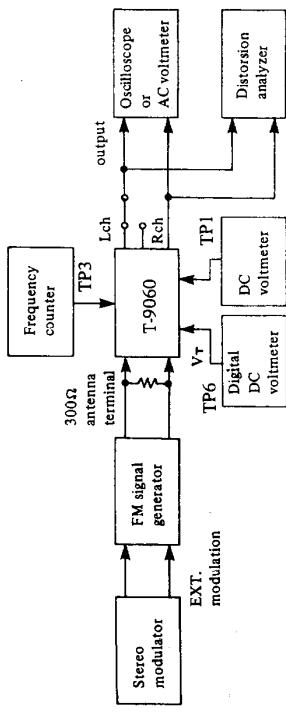
1. Stereo Modulator
2. FM Signal Generator with Frequency Counter
3. Frequency Counter
4. Digital DC Voltmeter
5. DC Voltmeter
6. Distortion Analyzer
7. AC Voltmeter
8. Oscilloscope

GENERAL ALIGNMENT CONDITION

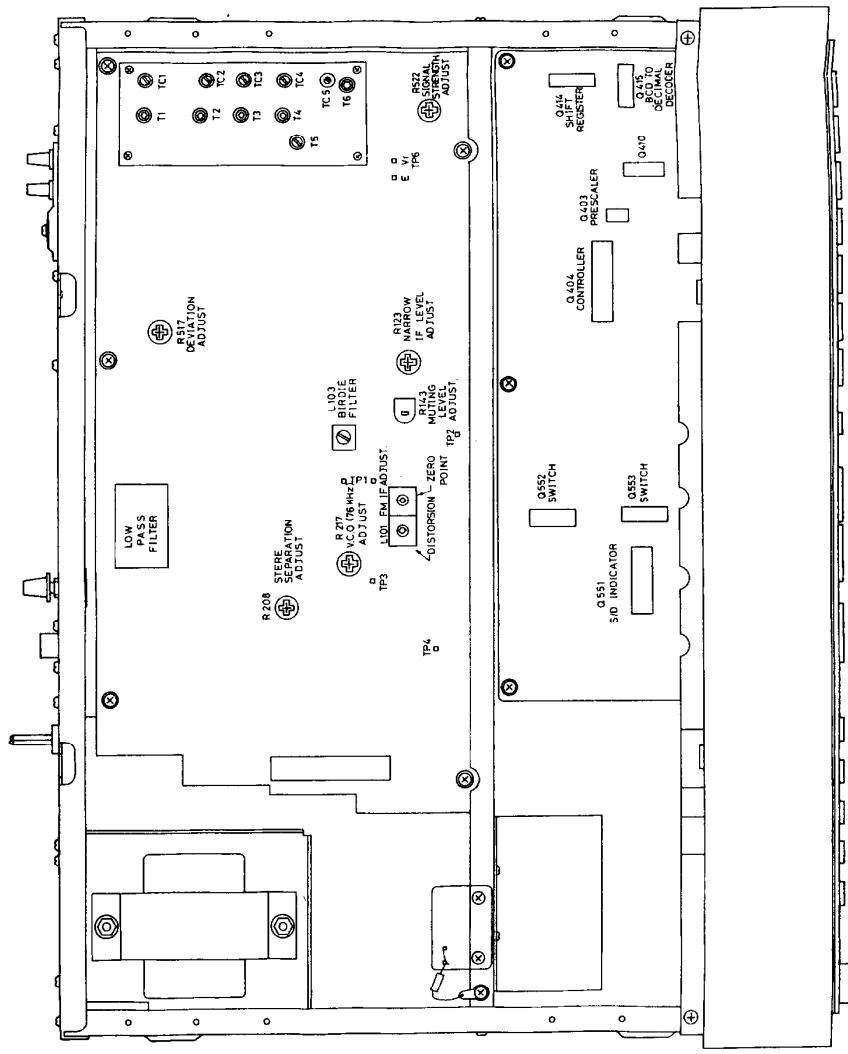
1. Standard modulation is 1 kHz 100% (FM MONO). pilot 9% sub and main 91%. (FM STEREO)
 2. The switches and control should be set as follows unless otherwise specifies.
- | | |
|--------------------------|-----------------|
| IF band | Wide |
| Auto Hi-blend | Off |
| FM muting/Mode | On/Stereo |
| De-emphasis | Normal |
| Output level | Maximum |
| Meter | Signal strength |

Item		FM signal generator	Stereo modulator	Dial to set	Adjust	Output indicator	Adjust for	Remarks
FM IF	1	98.1MHz, 65dBf, 1kHz, 75kHz devi.		98.1MHz	L101	DC voltmeter	0V	Repeat steps 1 and 2 as necessary
	2				L101	Distortion analyzer	Minimum	
FM RF	1	88.1MHz, 65dBf 1kHz, 75kHz devi.		88.1MHz	T6	Digital DC voltmeter	3.03V	Repeat steps 1 and 2 as necessary
	2	107.9MHz, 65dBf 1kHz, 75kHz devi.		107.9MHz	TC5	Digital DC voltmeter	20.8V	
	3	88.1MHz 1kHz, 75kHz devi.		88.1MHz	T1~T4	AC VTVM	Maximum	Repeat steps 3 and 4 as necessary
	4	107.9MHz 1kHz, 75kHz devi.		107.9MHz	TC1~TC4	AC VTVM	Maximum	
	5	98.1MHz 1kHz, 75kHz devi.		98.1MHz	T5	AC VTVM	Maximum	
V.C.O		98.1MHz 65dBf		98.1MHz	R217	Frequency counter	76,000±76Hz	Turn off the modulation
Stereo separation		98.1MHz 65dBf Ext. modulation	Rch	98.1MHz	R208	AC voltmeter (Lch)	Minimum	Maximum and same separation
			Lch			AC voltmeter (Rch)	Minimum	
Muting level		98.1MHz, 17dBf 1kHz, 75kHz devi.		98.1MHz	R143	Oscilloscope	Signal	Set the muting switch to on position
		98.1MHz, 16dBf 1kHz, 75kHz devi.					No signal	
Signal indicator		98.1MHz, 65dBf 1kHz, 75kHz devi.		98.1MHz	R522	Signal indicator	8th L.E.D light on	
Deviation indicator		98.1MHz, 65dBf 1kHz, 75kHz, devi.		98.1MHz	R517	Deviation indicator	8th L.E.D light on	Set the meter switch to deviation
IF level		98.1MHz, 35dBf 1kHz, 75kHz devi.		98.1MHz	R123	Connect the DC voltmeter to terminal TP-2. The levels of Normal and Wide become same.		

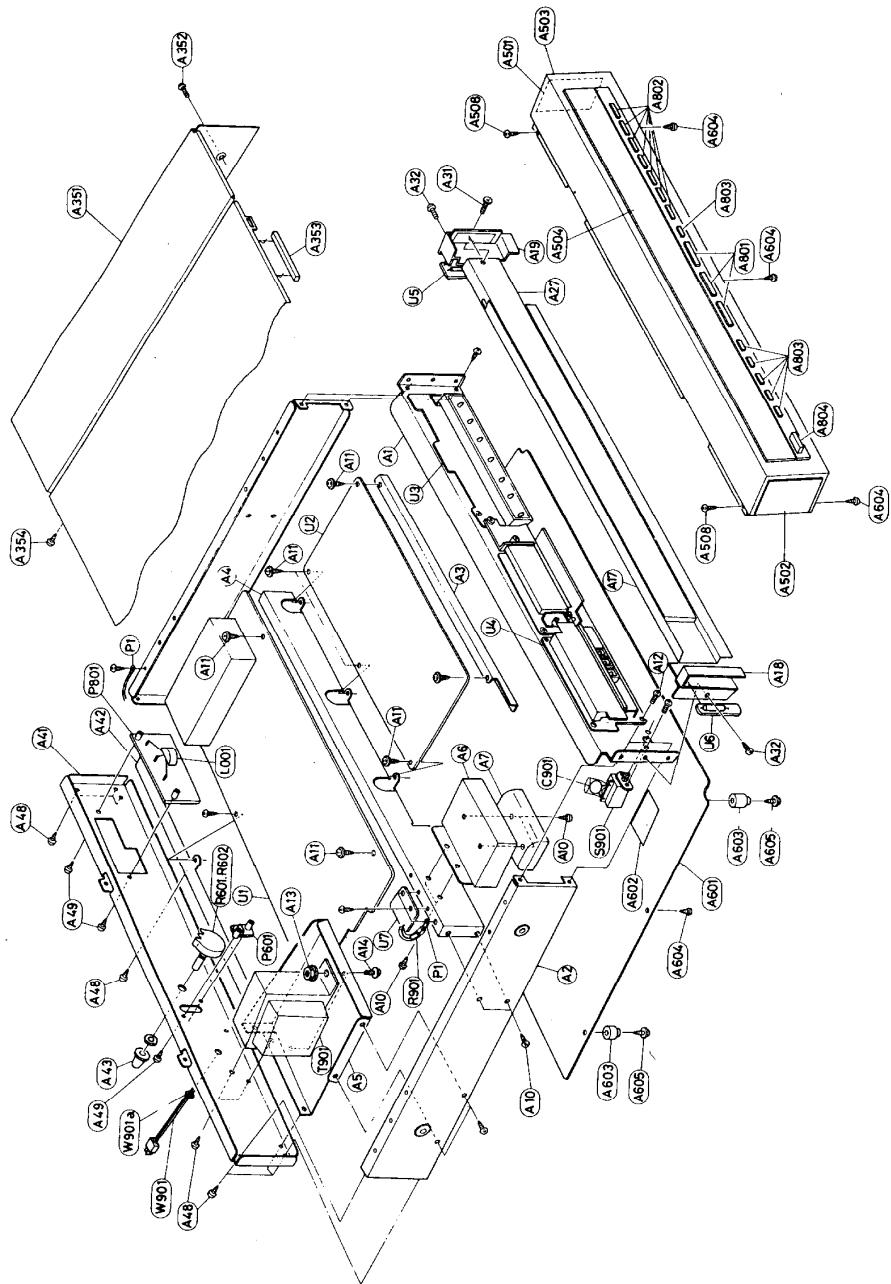
Connection Diagram



COMPONENT LOCATION

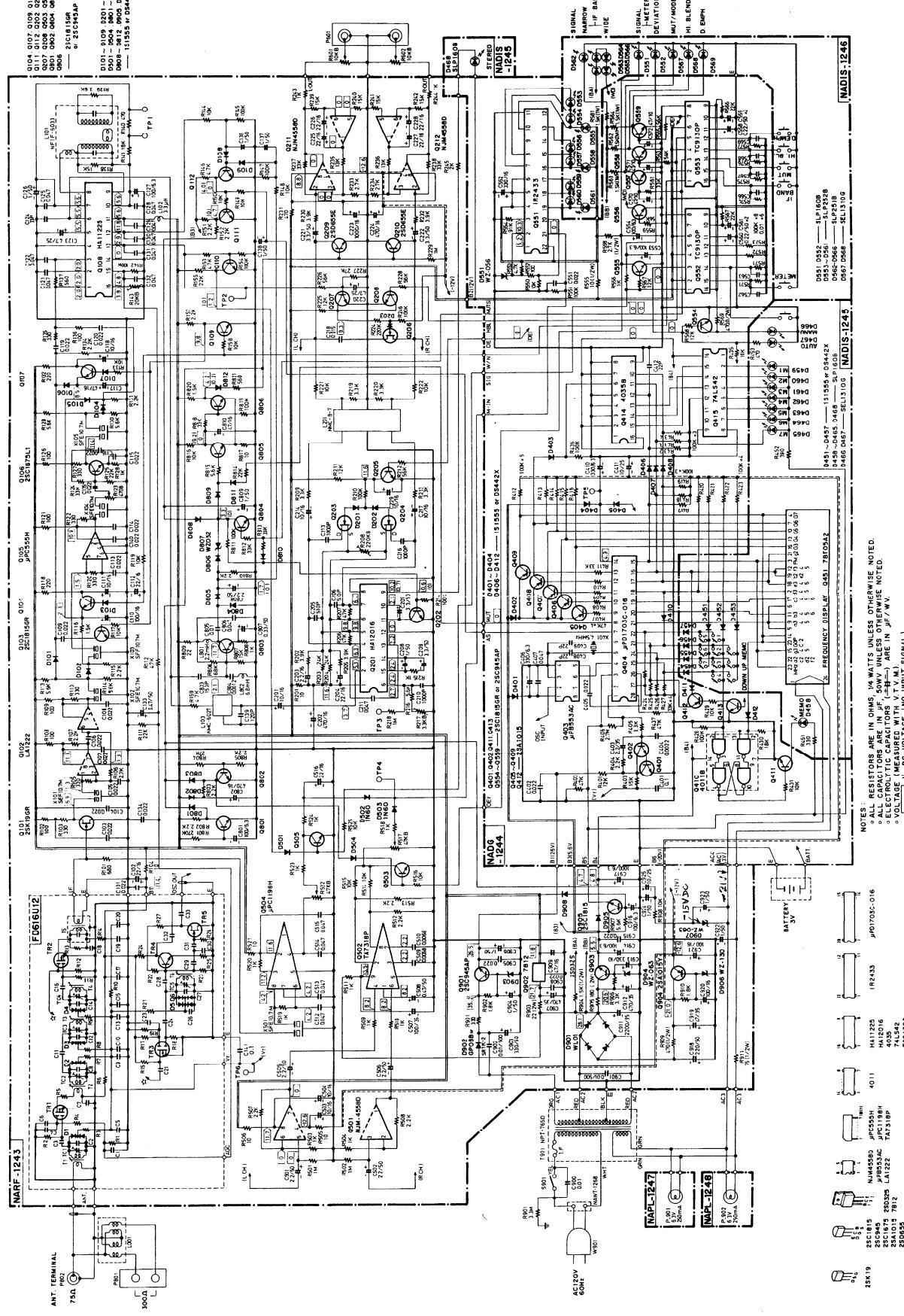


EXPLODED VIEW

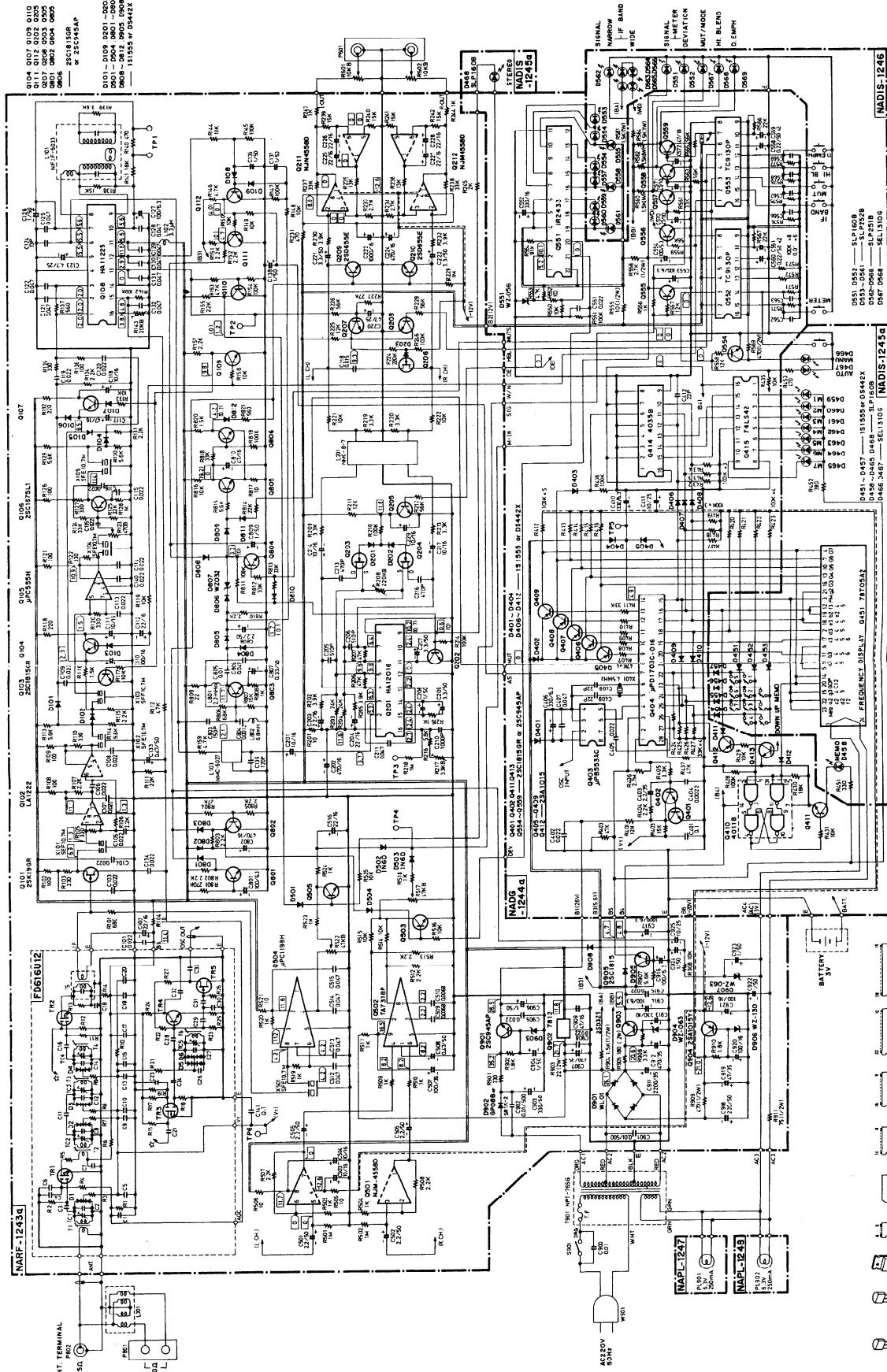


SCHEMATIC DIAGRAM

D model



SCHEMATIC DIAGRAM
G model



NOTES:
 1. ALL RESISTORS ARE IN OHMS, UNLESS OTHERWISE NOTED.
 2. ALL CAPACITORS ARE IN MICROFARADS, UNLESS OTHERWISE NOTED.
 3. ELECTROLYtic CAPACITORS (---) ARE IN MF/W.
 4. VOLTAGE MEASURED WITH VTM.
 5. DC VOLTAGE (NO INPUT SIGNAL).
 6. V DC VOLTS (FM STEREO).

ONKYO CORPORATION

PRINTED CIRCUIT BOARD-PARTS LIST
FM TUNER AND POWER SUPPLY PC BOARD (NARF-1243)

CIRCUIT NO.	PARTS NO.	DESCRIPTION	CIRCUIT NO.	PARTS NO.	DESCRIPTION
	Front end		C123	352750479	4.7μF, 25V, Elect.
TU001	240048	FD616U12	C126	352780109	1μF, 50V, Elect.
	ICs		C127	352721019	100μF, 6.3V, Elect.
Q102	222577	LA1222, IF amplifier	C133	352784799	0.47μF, 50V, Elect.
Q105	222591	μPC555H, IF amplifier	C136-C138	352780109	1μF, 50V, Elect.
Q108	222540	HA11225, FM IF system	C201	352741009	10μF, 16V, Elect.
Q201	222593	HA12016, Stereo decoder	C202	352744719	470μF, 16V, Elect.
Q211, Q212	222465	NJM4558D, Super servo amplifier	C203, C204	352742209	22μF, 16V, Elect.
Q501	222465	NJM4558D, Deviation indicator amplifier	C205, C206	372525114	510pF±5%, 50V, St
Q502	222529	TA7318P(R), Deviation indicator amplifier	C207, C209	352780339	3.3μF, 50V, Elect.
Q504	222657	μPC1198H, Signal indicator amplifier	C208	352780109	1μF, 50V, Elect.
Q902	222780120	7812, Voltage regulator	C210	372521024	1,000pF±5%, 50V, St
	Transistors		C213, C216	372521024	1,000pF±5%, 50V, St [D]
Q101	2211815	2SK19TM (GR)	C213, C216	372524714	470pF±5%, 50V, St [G/W]
Q103	2211255	2SC1815 (GR)	C212, C215	372525114	510pF±5%, 50V, St [W]
Q104, Q107	2211255 or	2SC1815 (GR) or	C214, C217	352741009	10μF, 16V, Elect.
Q109-Q112	2210746	2SC945A(P)	C218	379121534	0.015μF±5%, 50V, DEW
Q106	2210823	2SC1675 (L-1)	C220	352750479	0.47μF, 25V, Elect.
Q202, Q205	2211255 or	2SC1815 (GR) or	C221, C222	352780339	3.3μF, 50V, Elect.
Q207, Q208	2210746	2SC945A (P)	C223	352741029	1,000μF, 16V, Elect.
Q203, Q204	2211303	2SK68A(M)	C224	352744709	47μF, 16V, Elect.
Q206	2211303	2SK68A (M)	C225-C228	352742209	22μF, 16V, Elect.
Q209, Q210	2211705	2SD655 (E)	C229	352741009	10μF, 16V, Elect.
Q503, Q505	2211255 or	2SC1815 (GR) or	C501, C502	352780229	2.2μF, 50V, Elect.
Q801, Q802	2210746	2SC945A (P)	C503, C504	352741009	10μF, 16V, Elect.
Q804-Q806			C505, C506	352780229	2.2μF, 50V, Elect.
Q803, Q901	2210746	2SC945A (P)	C507	352761010	100μF, 35V, Elect.
Q903	2201034 or	2SD325 (D) or	C508	352784799	0.47μF, 50V, Elect.
	2201035	2SD325 (E)	C516	352742209	22μF, 16V, Elect.
Q904	2211454	2SA1015 (Y)	C801	352721019	100μF, 6.3V, Elect.
Q905	2211254 or	2SC1815 (Y) or	C802	352744719	470μF, 16V, Elect.
	2211255	2SC1815 (GR)	C807	352783399	0.33μF, 50V, Elect.
	Diodes		C808	352780229	2.2μF, 50V, Elect.
D101-D109	223105 or	1S1555 or	C809	352780109	1μF, 50V, Elect.
D201-D203	223133	DS442X	C810	352744709	47μF, 16V, Elect.
D501, D504	223105 or	1S1555 or	C903	352783319	330μF, 50V, Elect.
D801-D812	223133	DS442X	C904, C906	352780109	1μF, 50V, Elect.
D502, D503	223103	1N60	C907	352764719	470μF, 35V, Elect.
D901	223862	WL0	C909	352744709	47μF, 16V, Elect.
D902	223848 or	GP08B or	C911	352762229	2,200μF, 35V, Elect.
	223804	SR1K-2	C912	352764719	470μF, 35V, Elect.
D903	223979	RD27EB	C913	352733319	330μF, 10V, Elect.
	223922	WZ270	C914, C916	352721019	100μF, 6.3V, Elect.
D904	224020	WZ063	C917	352721029	1,000μF, 6.3V, Elect.
D905, D908	223105 or	1S1555 or	C918	352782219	220μF, 50V, Elect.
	223133	DS542X	C919	352764709	47μF, 35V, Elect.
D906	223924	WZ-130	C920, C921	352741019	100μF, 16V, Elect.
D907	224020	WZ-063	C922-C924	352780109	1μF, 50V, Elect.
	Transformer		C925	352780339	3.3μF, 50V, Elect.
L101	233255	NFIF-6033, IFT	R123	5225026	Resistors
	Coils		R143	5215003	N10HR470BD, Narrow IF level adjust. semi-fixed
L102	233105 or	NCH-1005 or	R208	5225037	N08HR20KBC, Muting level adjust. semi-fixed
	233024	NCCH-1501	R217	5225029	N10HR220KBD, Stereo separation adjust. semi-fixed
L103	233236	NMC-6027	R517, R522	5225034	N10HR3.3KBD, V.C.O. (76kHz) adjust. semi-fixed
L201	233032A	NMC-8-7	R903	441722204	N10HR47KBD, Deviation/signal indicator level adjust. semi-fixed
L801	233031	NMC-9-1	R904	441521524	22Ω, 2W, Metal oxide film
L802	233122	NCH-3013	R905	441721814	1.5kΩ, 1/2W, Metal oxide film
	Ceramic filters		R909	441524714	180Ω, 2W, Metal oxide film
X101, X102	3010041	SFE10, 7MX	R911	441527504	470Ω, 1/2W, Metal oxide film
X103-X105	3010043	SFE10, 7MM			75Ω, 1/2W, Metal oxide film
X501	3010006	SFE10, 7MA			
	Capacitors				
C102	352742209	22μF, 16V, Elect.			
C110	352741019	100μF, 16V, Elect.			
C111, C118	352741009	10μF, 16V, Elect.			
C112	352742209	22μF, 16V, Elect.			
C117	352744709	47μF, 16V, Elect.			
	Transformer				
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	Ceramic filters				
	Capacitors				
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