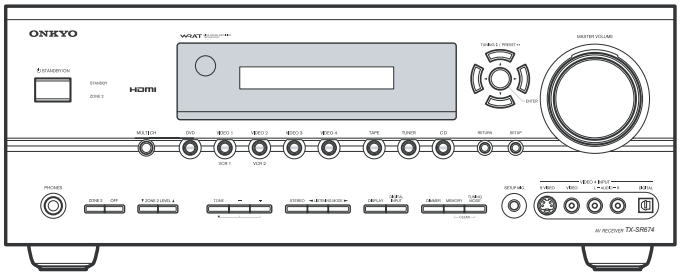
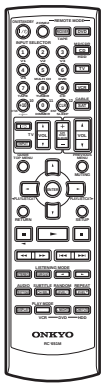
Ref. No. 3949
102006

ONKYO SERVICE MANUAL

AV RECEIVER

MODEL TX-SR674
MODEL TX-SR674E
MODEL TX-SR8467





RC-651M

TX-SR674 Black, Golden and Silver models

B MDD, B MDC, S MDC	120V AC, 60Hz
B MPA, S MPA	230-240V AC, 50Hz
B MWT, B MWO, G MWT, G MWO	120V/220-24 0V AC, 50/60Hz
G MGR, G MGQ, G MGK	220-230V AC, 50/60Hz

TX-SR674E Black and Silver models

B MPP, B MPB, S MPP, S MPB	230-240V AC, 50Hz

TX-SR8467 Golden model

G MGR	220-230V AC, 50/60Hz

SAFETY-RELATED COMPONENT WARNING!!

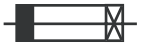
COMPONENTS IDENTIFIED BY MARK ⚠ ON THE SCHEMATIC DIAGRAM AND IN THE PARTS LIST ARE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK. REPLACE THESE COMPONENTS WITH ONKYO PARTS WHOSE PART NUMBERS APPEAR AS SHOWN IN THIS MANUAL.

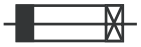
MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

ONKYO®
IMAGINATIVE SIGHT & SOUND

SERVICE PROCEDURE

1. Replacing the fuses


This symbol located near the fuse indicates that the fuse used is show operating type, For continued protection against fire hazard, replace with same type fuse, For fuse rating, refer to the marking adjacent to the symbol.


Ce symbole indique que le fusible utilise est e lent. Pour une protection permanente, n'utiliser que des fusibles de meme type. Ce demier est indique la qu le present symbol est apposre.

<Notes>

<DD> : TX-SR674 USA model
<PA> : TX-SR674 Australian model
<PB> : TX-SR674 U.K. model
<WT> : TX-SR674 World wide model
<WO> : TX-SR674 Saudi model
<DC> : TX-SR674 Canadian model
<PP> : TX-SR674E European model
<GK> : TX-SR674 Korean model
<GQ> : TX-SR674 Hong kong model
<GR> : TX-SR674 & TX-SR8467 Chinese model

REF NO.	PART NAME	DESCRIPTION	PART NO.	REMARKS
F901	FUSE	10A-UL/T-233	252330GR	!, <DD,DC>
F901 or	FUSE	10A-T/UL-ST2	252333GR	!, <DD,DC>
F901	FUSE	5A-SE-EAK	252078GR	!, <WO,WT,GQ,GR,GK,PA,PB,PP>
F901 or	FUSE	5A-SE-TL250V	252278GR	!, <WO,WT,GQ,GR,GK,PA,PB,PP>
F902	FUSE	5A-SE-EAK	252078GR	!, <WO,WT>
F902 or	FUSE	5A-SE-TL250V	252278GR	!, <WO,WT>
F903	FUSE	5A-UL/T-233	252326GR	!, <DD,DC>
F903 or	FUSE	5A-T/UL-ST2	252258GR	!, <DD,DC>
F903	FUSE	2.5A-SE-EAK	252075GR	!, <WO,WT,GQ,GR,GK,PA,PB,PP>
F903 or	FUSE	2.5A-SE-TL250V	252275GR	!, <WO,WT,GQ,GR,GK,PA,PB,PP>
F910	FUSE	5A-UL/T-233	252326GR	!
F910 or	FUSE	5A-T/UL-ST2	252258GR	!
F6901	FUSE	12A-TUL-250V	252301GR	!
F6902	FUSE	12A-TUL-250V	252301GR	!

2. To initialize the unit

1. Press and hold down the VIDEO 1/VCR 1 button, then press the STANDBY/ON button when the unit is Power on.
2. After " *Clear* " is displayed, the preset memory and each mode stored in the memory are initialized and will return to the factory settings.

3. To check the version of microprocessor

Main microprocessor Q701 only.

1. Press and hold down the DISPLAY button , then press the STANDBY/ON button when the unit is Power on. The version is displayed on FL display for 3 seconds.

Ex. *Main1.01/05305A*

2. Press the STANDBY/ON button to Power off.

4. Memory Backup

The AV receiver uses a battery-less memory backup system in order to retain radio presets and other settings when it's unplugged or in the case of a power failure.
Although no batteries are required, the AV receiver must be plugged into an AC outlet in order to charge the backup system. Once it has been charged, the AV receiver will retain the settings for several weeks, although this depends on the environment and will be shorter in humid climates.

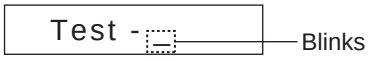
OPERATION CHECK-1

SPEAKER PROTECT-1 (DC VOLTAGE DETECTION)

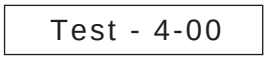
[When]
1. Exchange power transistors (Q6050 - Q6056, Q6060 - Q6066).
2. Exchange amplifier PC board ass'y (NAAF-8911).

[Procedure]
<Note>
No load. No input.

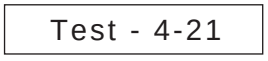
1. Press and hold down the CD button, then press the STANDBY/ON button while the unit is Power ON.
" Test - _ " is displayed only for 5 seconds.



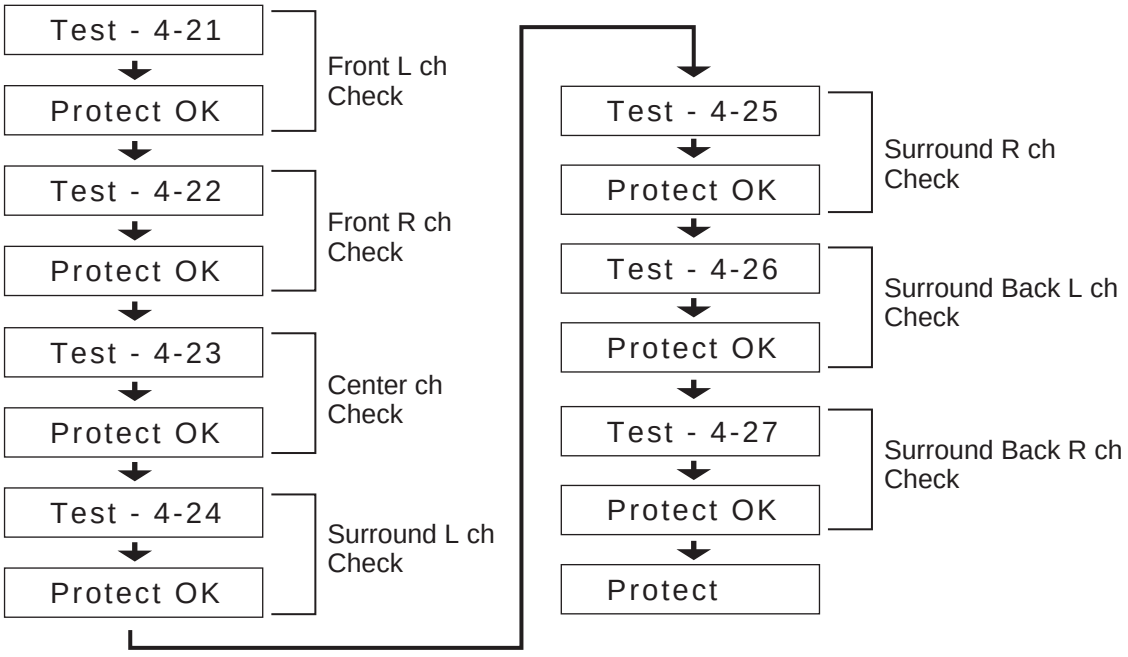
2. Press the VIDEO 3 button, while the characters of " Test - _ " are displayed.
The unit will be in the state of "Test-4-00".



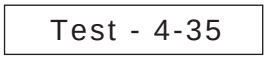
3. Repeatedly press TONE+ button until the characters of " Test-4-21 " are displayed.



Check whether the operation starts and continues automatically as follows.



If all channels are OK, the characters of " Test - 4 - 35 " are displayed.



4. Press the STANDBY/ON button.

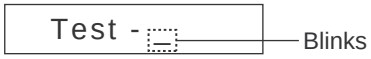
OPERATION CHECK-2

SPEAKER PROTECT-2 (CURRENT DETECTION)

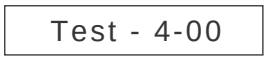
[When]
1. Exchange power transistors (Q6050 - Q6056, Q6060 - Q6066).
2. Exchange amplifier PC board ass'y (NAAF-8911).

[Procedure]
<Note>
No input.
Do not check two or more channels at the same time.
Do not connect a dummy load to speaker terminal longer than 2 seconds.

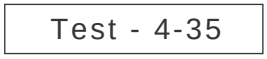
1. Press and hold down the CD button, then press the STANDBY/ON button while the unit is Power ON.
" Test - _ " is displayed only for 5 seconds.



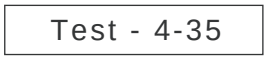
2. Press the VIDEO 3 button, while " Test - _ " is displayed.
The unit will be in the state of " Test-4-00 ".



3. Repeatedly press TONE + button until " Test-4-35 " is displayed.

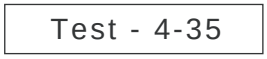


4. Connect the dummy load of 3 ohms to the Front L ch speaker terminal.
At this time, confirm that the speaker relay is not turned off.



5. Connect the dummy load of 1 ohm to the Front L ch speaker terminal.
At this time, confirm that the speaker relay is turned off and" Protect " is displayed.

Disconnect the dummy load immediately after checking the display of " Protect ".



6. Check other channels according to the same procedure as 4 and 5.

7. Press the STANDBY/ON button.

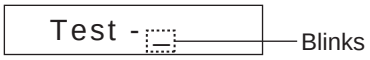
OPERATION CHECK-3

CONTROL OF POWER SUPPLY (OUTPUT SENSOR AND THERMAL SENSOR)

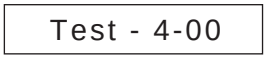
[When]
1. Exchange power transistors (Q6050 - Q6056, Q6060 - Q6066).
2. Exchange power amplifier PC board ass'y (NAAF-8911).
3. Exchange thermal sensor PC board ass'y (NAETC-8913).

[Procedure]
<Note>
No output. No input.

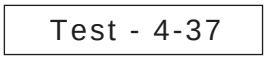
Output sensor
1. Press and hold down the CD button, then press the STANDBY/ON button while the unit is Power ON.
" Test - _ " is displayed only for 5 seconds.



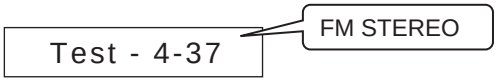
2. Press the VIDEO 3 button while " Test - _ " is displayed.
The unit will be in the state of " Test-4-00".



3. Repeatedly press TONE + button until " Test-4-37 " is displayed.



4. At this time, confirm that the red characters of " FM STEREO " is displayed.
And, check relay RL6901 and RL6902 are turned off in 2 or 3 seconds.

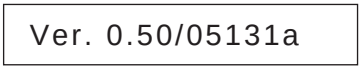


5. Press the STANDBY/ON button.

Thermal sensor

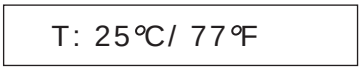
1. Press and hold down the DISPLAY button, then press the STANDBY button when the unit is power ON.
" Ver. 0.50/05131a " is displayed only for 2 seconds.

<Ex.>



2. Press the TONE button while" Ver.0.50/05131a " is displayed.

<Ex.>



3. Confirm that the displayed temperature is within +/-20 degree C from the ambient temperatures.

4. Press STANDBY/ON button.

OPERATION CHECK-4(1/2)
DSP DEBUG MODE

The operation of DSP is able to checked by the information displayed on FL in this debug mode.
This information will help to pursue the cause of trouble.

To set in DSP debug mode

1. Press and hold down the DISPLAY button, then press the STANDBY button while the unit is power ON.
   The version number of microprocessor is displayed only for 2 seconds.

<Ex.> `Ver. 0.50/05131a`

1. Press the TONE+ button within 2 seconds above, the version number of DSP is displayed.

<Ex.> `DSP :06421A`

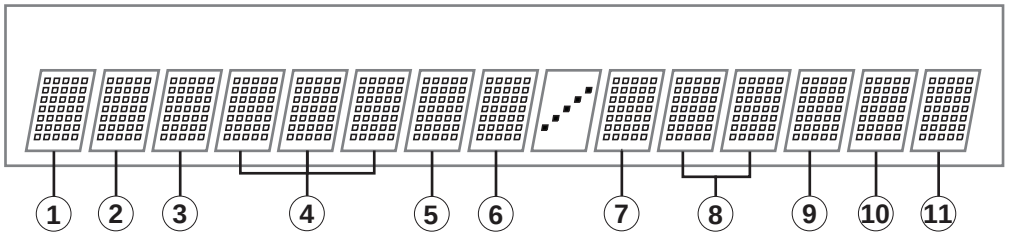
2. Press the DISPLAY button while " DSP :06421A" is displayed. The status of DSP and DIR will be displayed.

<Ex.> `E1A48K0N/OFFPoO`

To exit

Press STANDBY/ON button.

Content of display



---------- DIR ----------

① UNLOCK
- E = UNLOCK
- = LOCK

② Digital Selector
- 0 = None
- 1 = OPT 3
- 2 = OPT 2
- 3 = OPT 1
- 4 = COAX 1
- 5 = COAX 2
- 6 = HDMI
- 7 = FRONT

③ DIR Status
- D = Digital
- A = Analog
- M= Multich
- P = Multich PCM
- p = PCM Fixed
- d = DTS Fixed

④ Sampling Frequency and Emphasis
- 32K = 32 kHz without Emphasis
- 44K = 44.1 kHz without Emphasis
- 48K = 48kHz without Emphasis
- 64K = 64 kHz
- 88K = 88.2 kHz
- 96K = 96 kHz
- 176 = 176.4 kHz
- 192 = 192 kHz
- 32e = 32 kHz with Emphasis
- 44e = 44.1 kHz with Emphasis
- 48e = 48 kHz with Emphasis

⑤ CODEC CLOCK MODE
- N = Normal
- U = Up Sampling
- H = High Sampling (Double Rate)
- D = Down Sampling
- Q = Quad Rate

⑥ DIR Detect Type
- 0 = Analog
- 1 = PCM
- 2 = Not PCM
- 3 = Data
- 4 = DTS CD (Not used)
- 5 = Multich
- 6 = Not Decided

---------- DSP ----------

⑦ DSP Port
- 0 = NIC — (Normal state)
- 1 = DEC
- 2 = BUSY
- 3 = EXEC WAIT — (Abnormal state)

⑧ DSP Sequence
- 04 = Boot
- 11 = Restart
- FF = Free

⑨ DSP Detect Format
- P = PCM (Analog)
- D = Dolby Digital
- d = DTS
- A = AAC
- ? = UNKNOWN

⑩ DSP Decode
- o = Decode OK
- x = Decode NG

------- Main Micro Processor --------

⑪ Mute
- 0 = Selector IC(Q5501)
- 1
- 2 = DSP(Q201)
- 3 = DIR(Q301)

OPERATION CHECK-4(2/2)
DSP DEBUG MODE

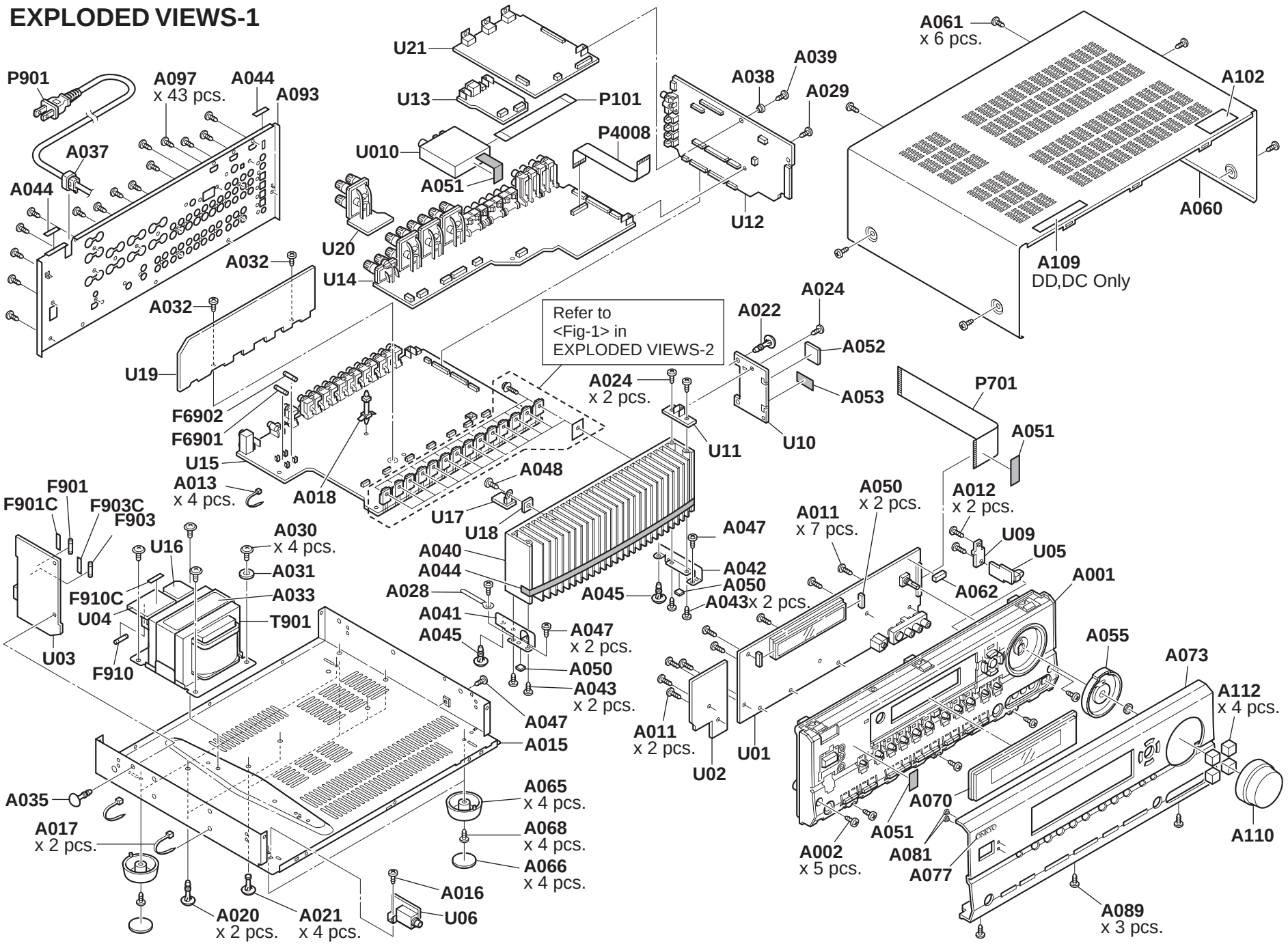
Trouble Cause Analysis by Debug Mode

This debug mode will help in digital audio no sound trouble.

Check information on FL display and the related devices or circuits.

Digit no. on FL	Symptom on display	Cause	Check
①	"E" is displayed	No input signal to DIR	Related devices from digital input to Q301
④	Displayed freq. is different from input	No input signal to DIR	Related devices from digital input to Q301
⑥	Displayed format is different from input	No input signal to DIR	Related devices from digital input to Q301
⑧	"04" or "11" do not change to "FF"	ROM or RAM error	Q281, Q282 & related devices
⑨	Displayed format is different from input	Input signal to DSP is no good	Related devices from Q301 to Q201
⑩	"x" is displayed	Interface between DSP and Micro processor is no good	Related devices from Q701 to Q201
⑪	This identifies IC which outputs error	IC outputs error to main micro processor	Q5501, Q201, Q301 & related devices

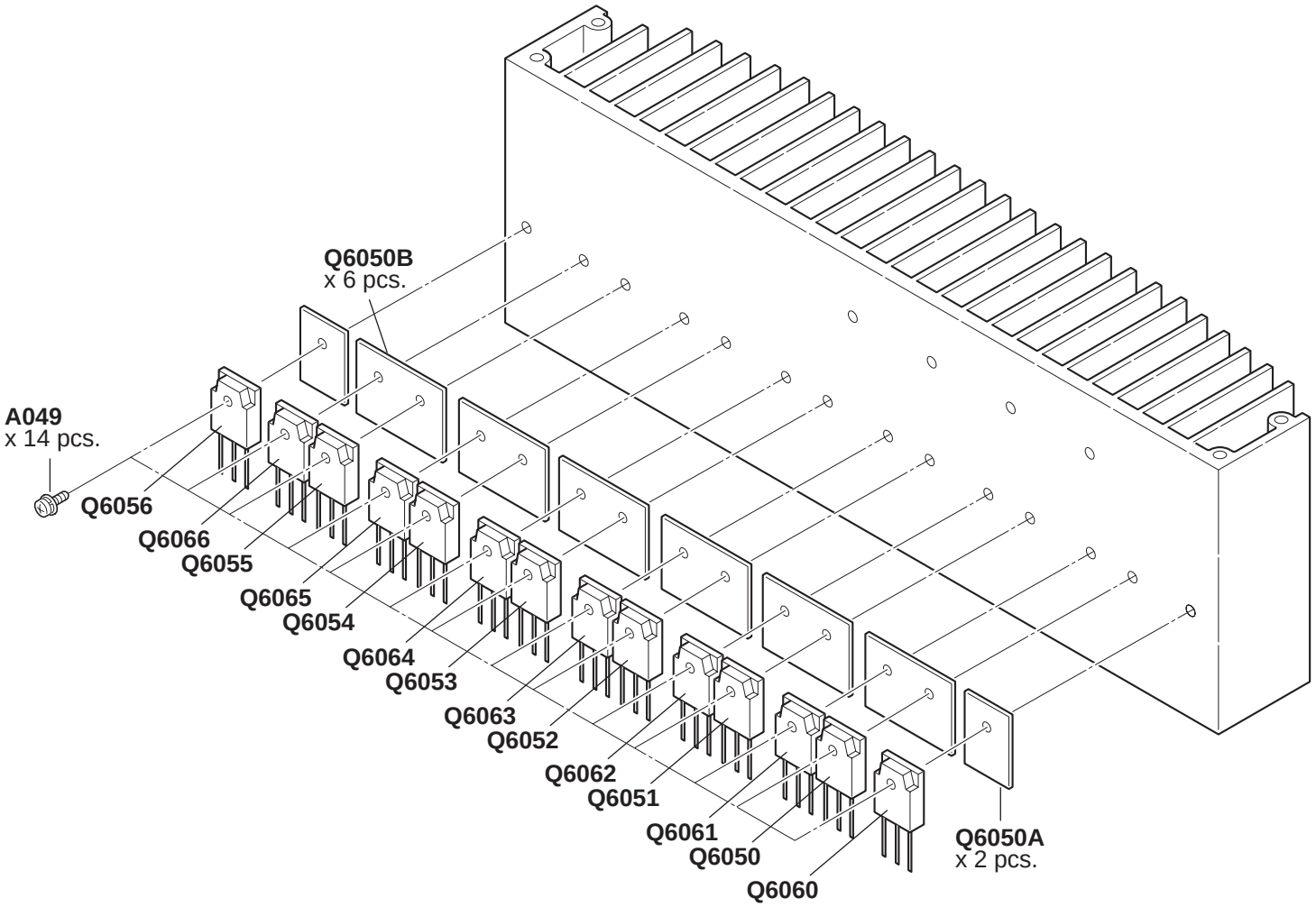
EXPLODED VIEWS-1



TX-SR674/674E/8467

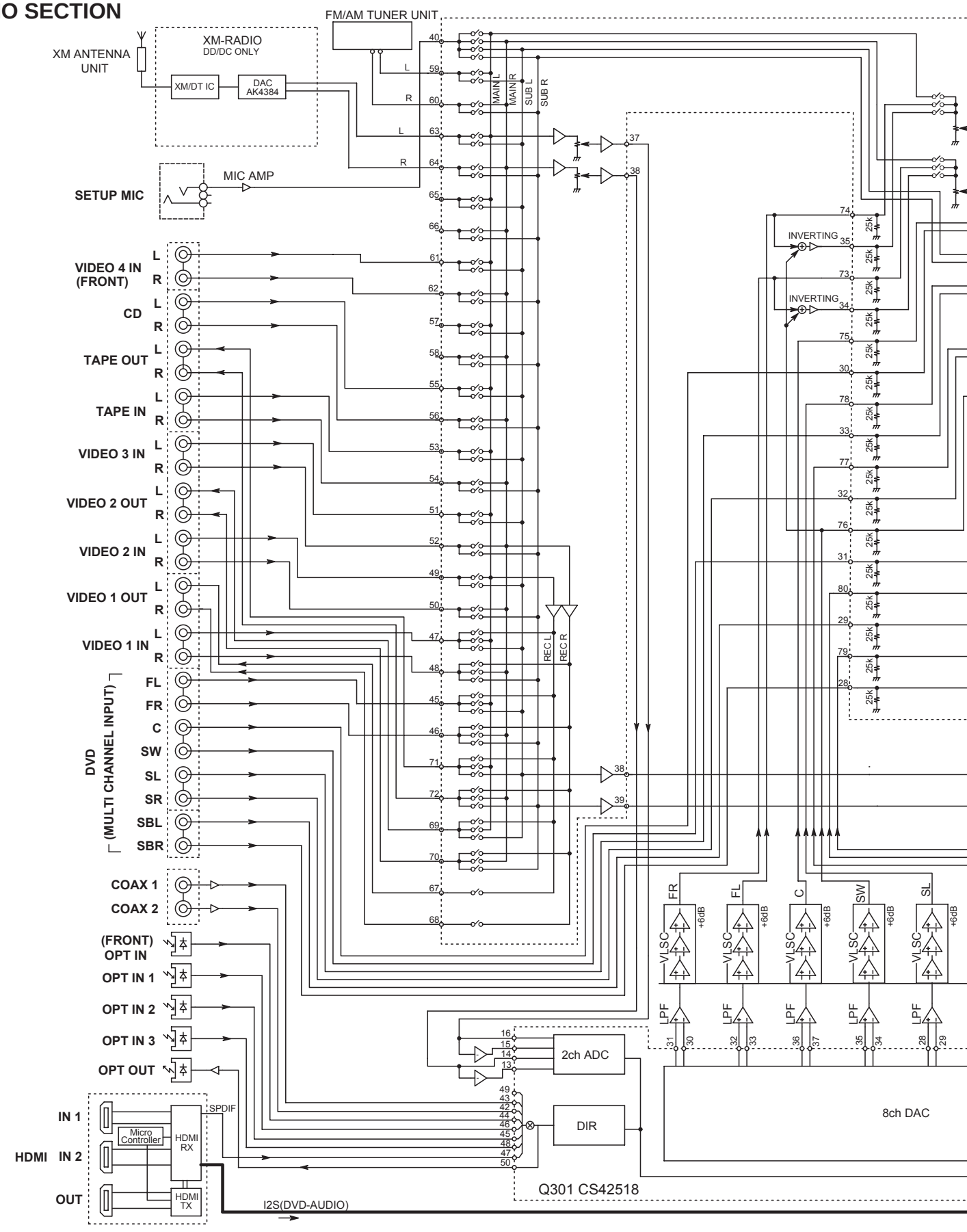
EXPLODED VIEWS-2

<Fig-1>

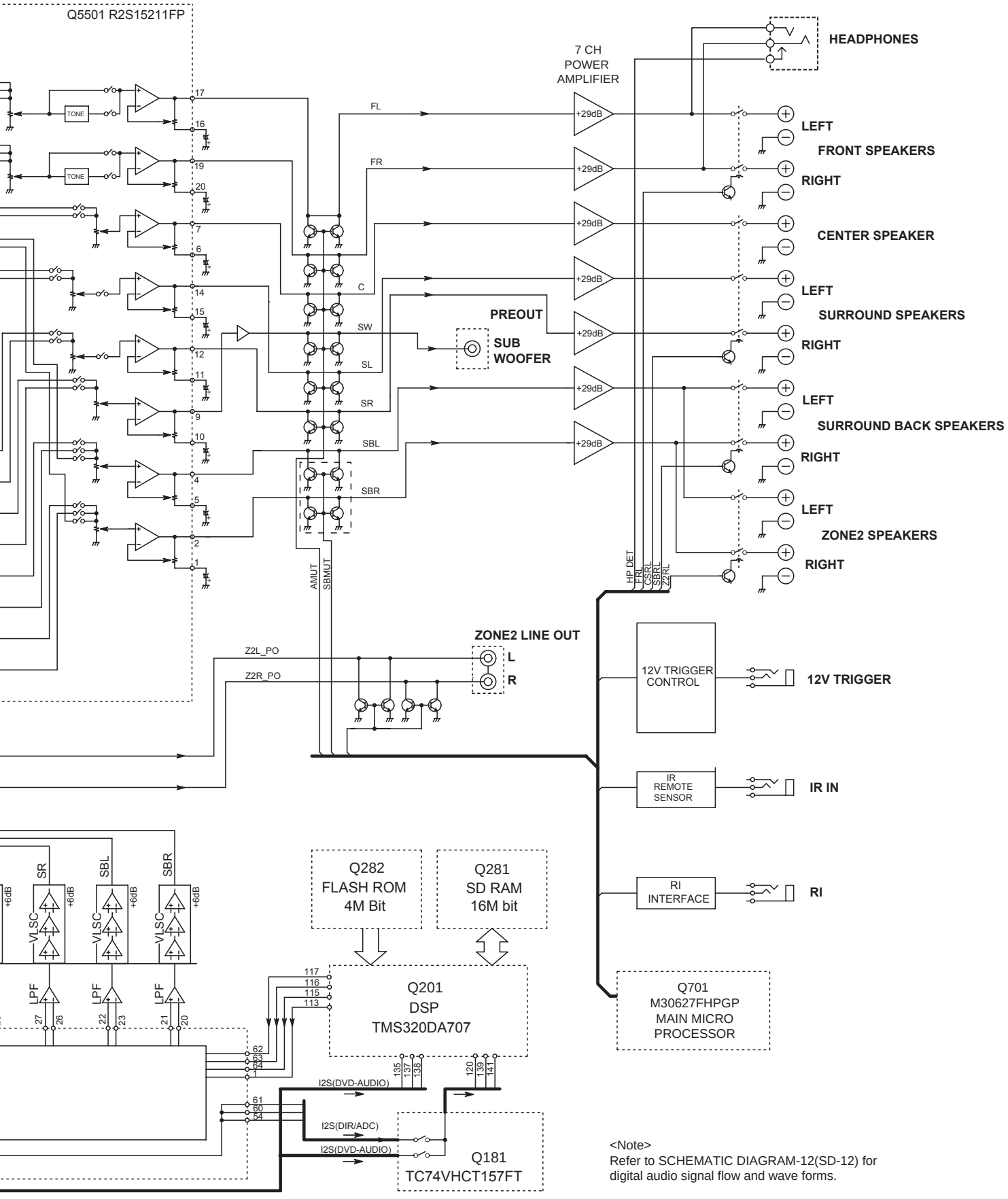


TX-SR674/674E/8467

BLOCK DIAGRAM-1
AUDIO SECTION

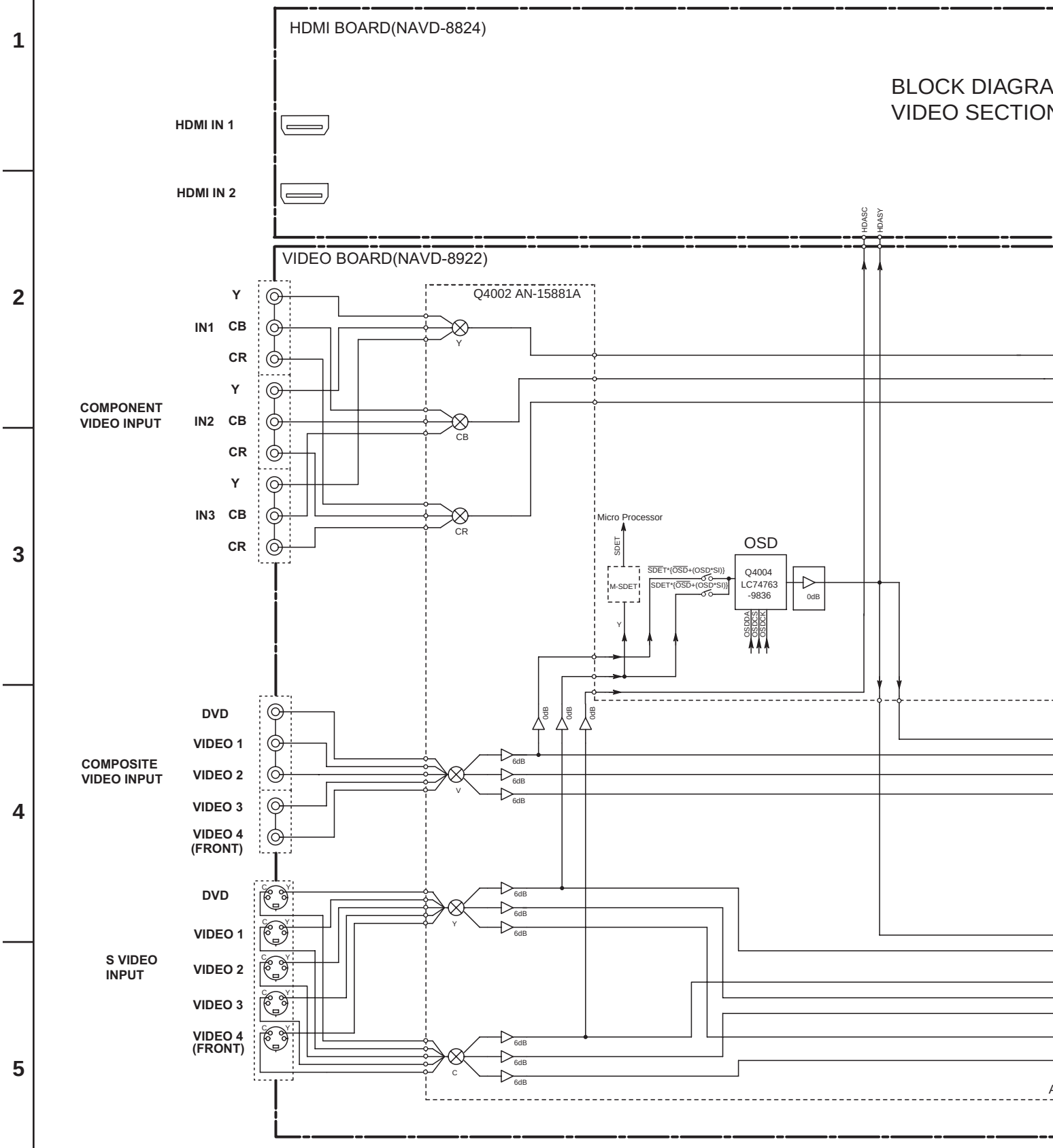


E F G H



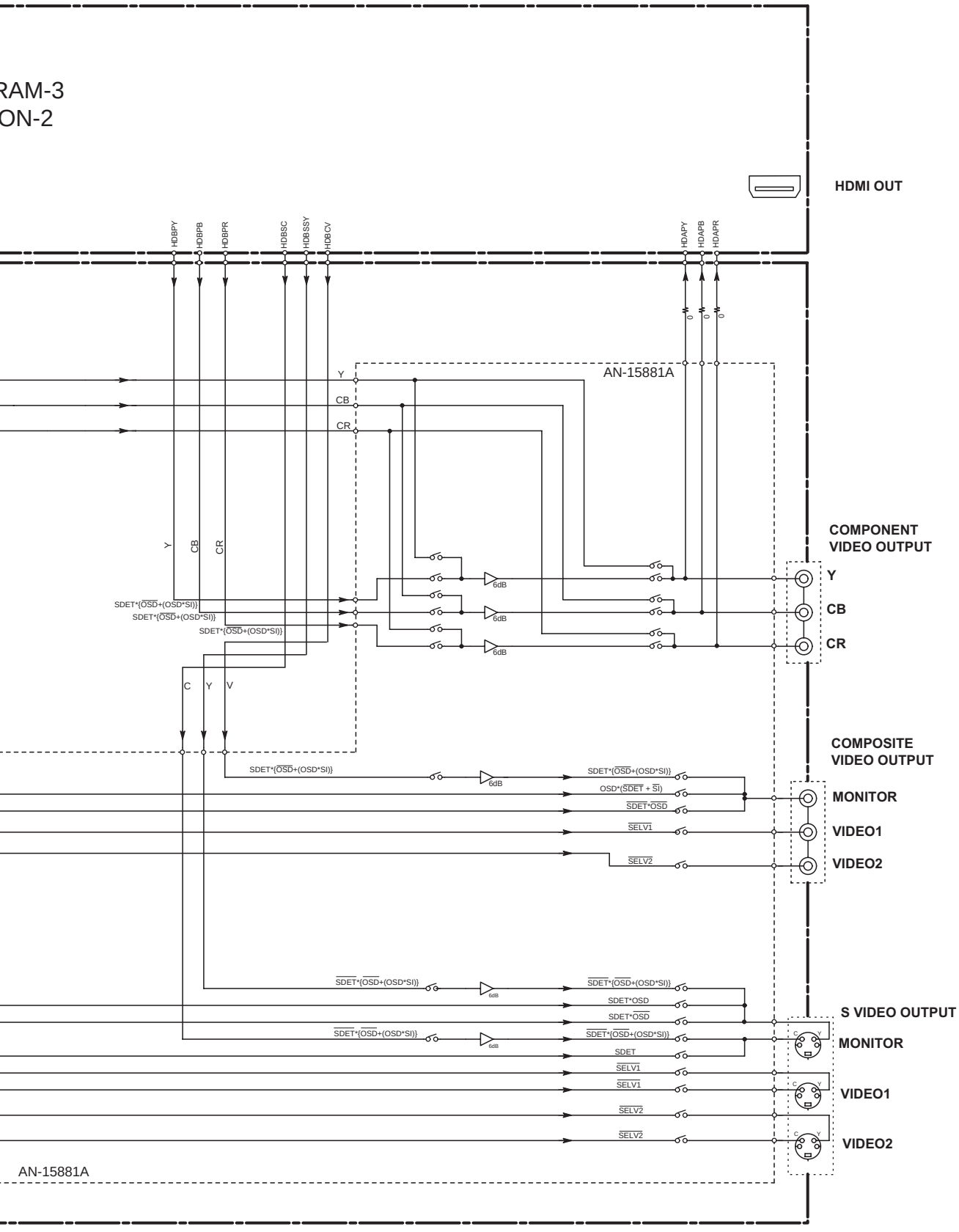
<Note>
Refer to SCHEMATIC DIAGRAM-12(SD-12) for digital audio signal flow and wave forms.

BLOCK DIAGRAM-2
VIDEO SECTION-1

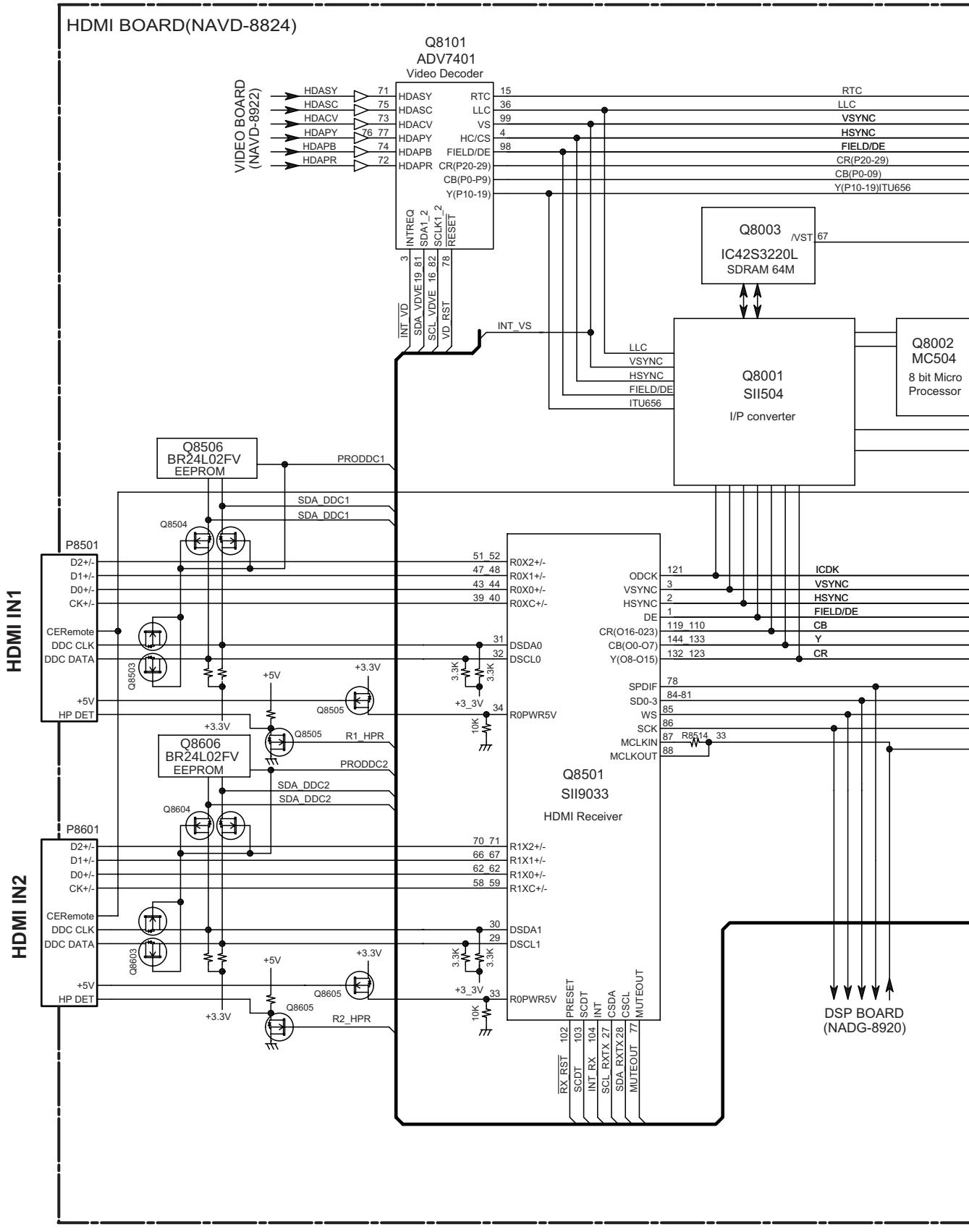


E F G H

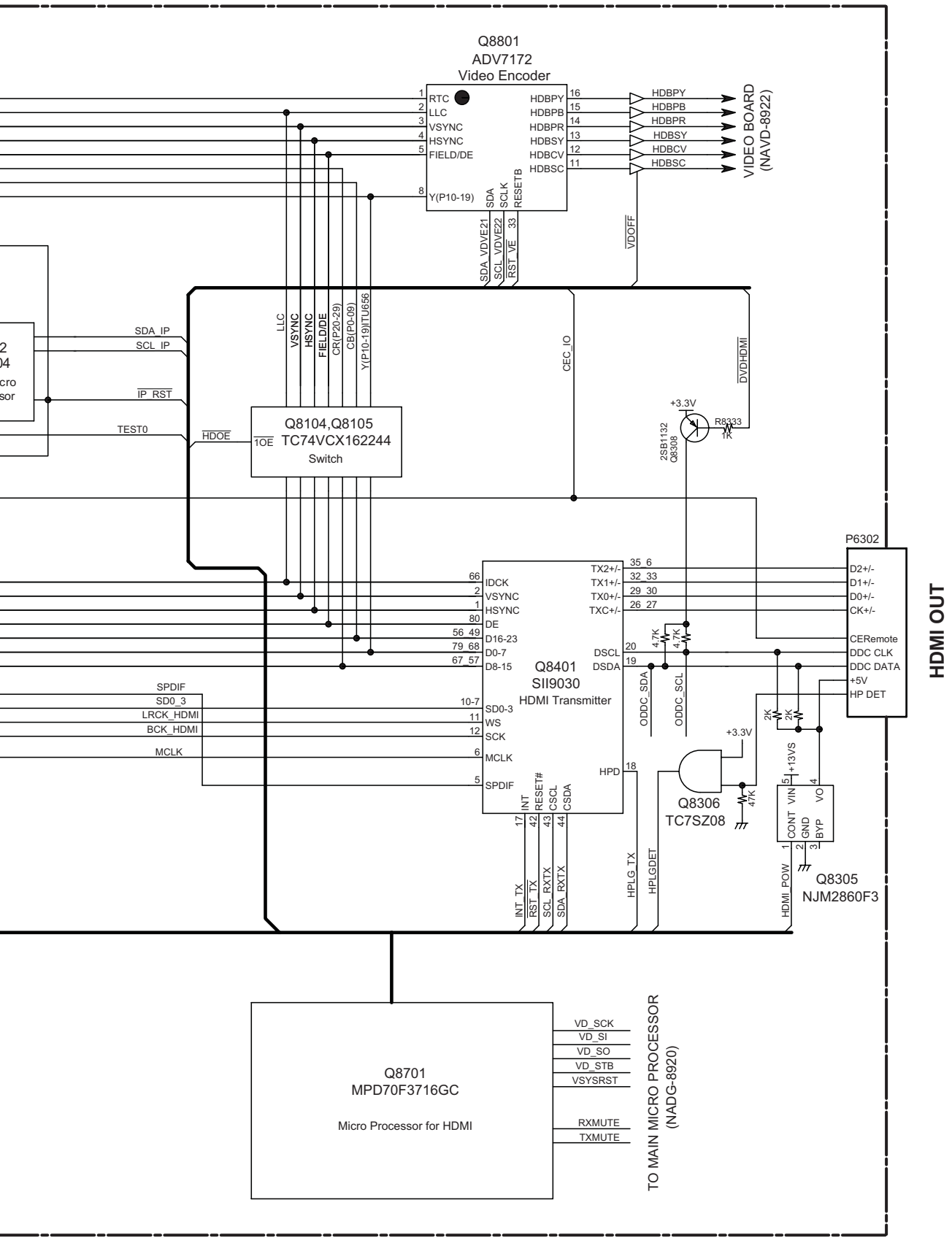
RAM-3
ON-2



BLOCK DIAGRAM-3
VIDEO SECTION-2



E F G H


Q8801
ADV7172
Video Encoder
RTC
LLC
VSYNC
HSYNC
FIELD/DE
Y(P10-19)
SDA
SCLK
RESETB
HDBPY
HDBPB
HDBPR
HDBSY
HDBCV
HDBSC
VIDEO BOARD
(NAVD-8922)
SDA_VDVE21
SCL_VDVE22
RST_VE
33
VDOFF
SDA_IP
SCL_IP
IP_RST
TEST0
HDOE
LLC
VSYNC
HSYNC
FIELD/DE
CR(P20-29)
CB(P0-09)
Y(P10-19)ITU656
Q8104,Q8105
TOE TC74VCX162244
Switch
CEC_IO
DVDHDMI
+3.3V
R8333
1K
2SB1132
Q8308
P6302
HDMI OUT
D2+/-
D1+/-
D0+/-
CK+/-
CERemote
DDC CLK
DDC DATA
+5V
HP DET
IDCK
VSYNC
HSYNC
DE
D16-23
D0-7
D8-15
TX2+/-
TX1+/-
TX0+/-
TXC+/-
DSCL
DSDA
Q8401
SII9030
HDMI Transmitter
4.7K
ODDC_SDA
ODDC_SCL
2K
SPDIF
SD0_3
LRCK_HDMI
BCK_HDMI
MCLK
SD0-3
WS
SCK
MCLK
SPDIF
HPD
INT
RESET#
CSCL
CSDA
Q8306
TC7SZ08
47K
+13VS
CONT
VIN
GND
BYP
VO
Q8305
NJM2860F3
HDMI_POW
INT_TX
RST_TX
SCL_RXTX
SDA_RXTX
HPLG_TX
HPLGDET
Q8701
MPD70F3716GC
Micro Processor for HDMI
VD_SCK
VD_SI
VD_SO
VD_STB
VSYSRST
RXMUTE
TXMUTE
TO MAIN MICRO PROCESSOR
(NADG-8920)

A B C D

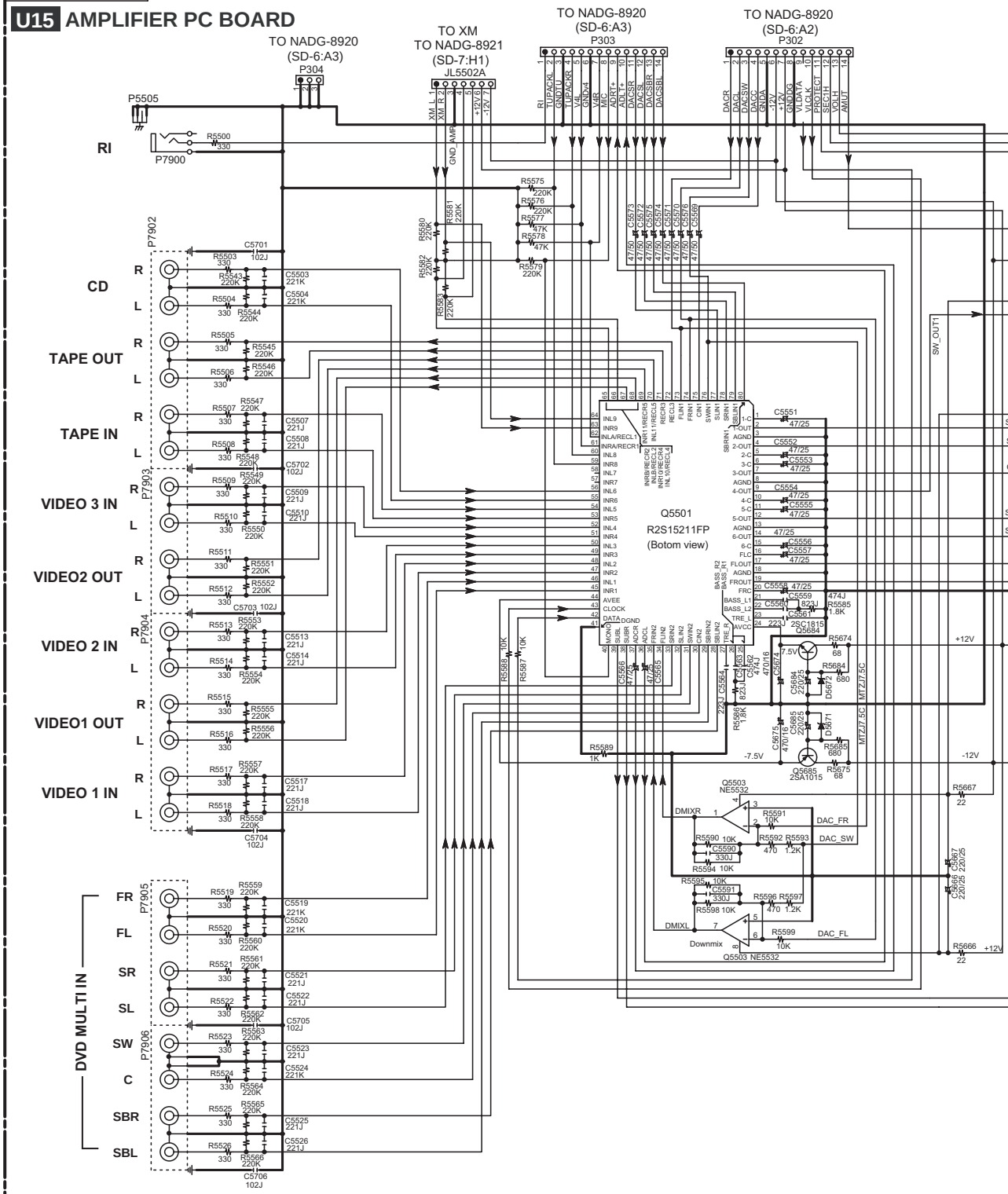
1 2 3 4 5

SCHEMATIC DIAGRAM-1(SD-1)

AUDIO SECTION

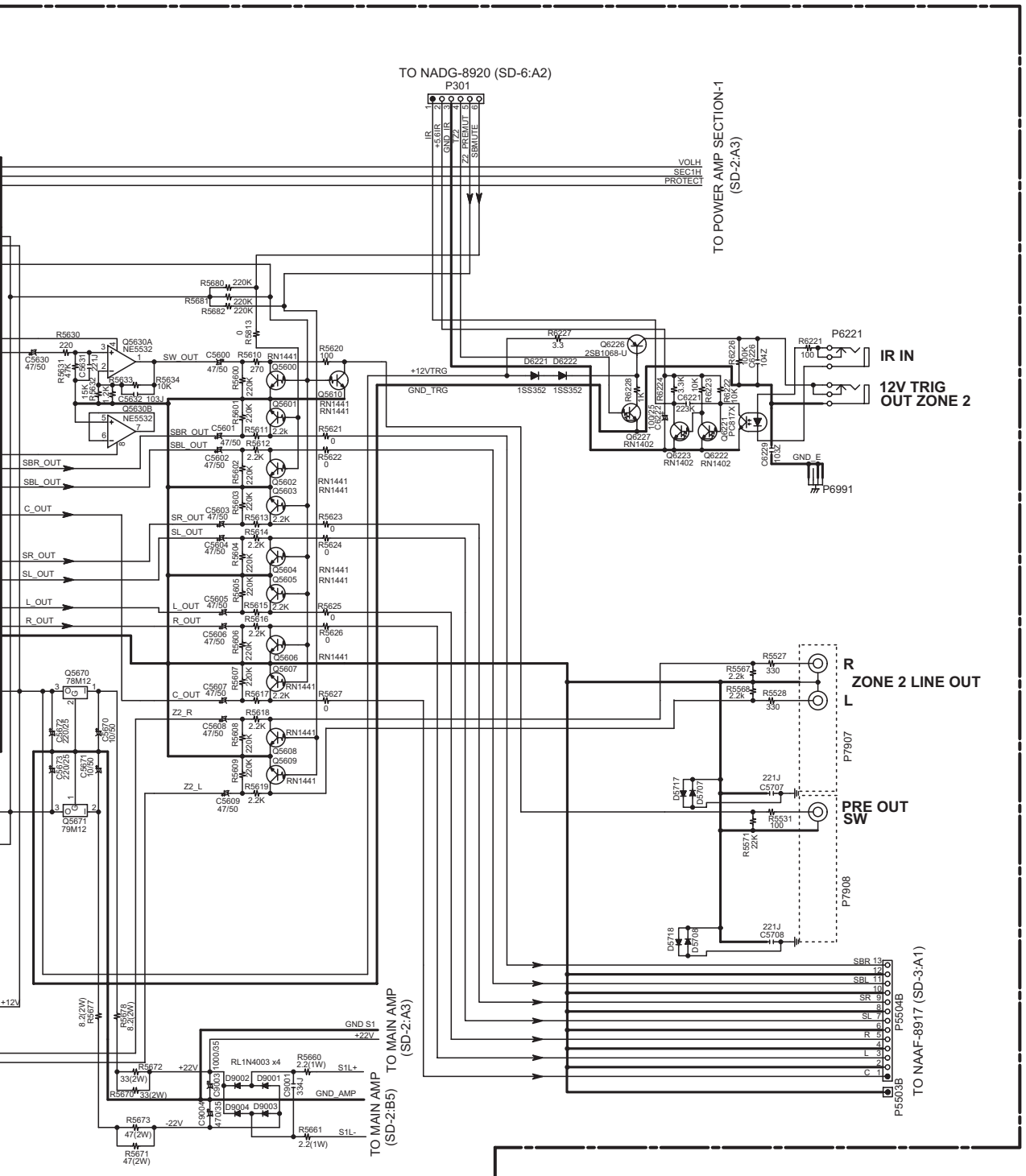
NAAF-8911 (1/2)

U15 AMPLIFIER PC BOARD



<Note>
SD-x:XY is short for Shcematic Diagram-x and each socket's location, X=A to H, Y=1 to 5.

E F G H



NOTE

- THE COMPONENTS IDENTIFIED BY MARK ⚠ ARE CRITICAL FOR SAFETY REPLACE ONLY WITH PART NUMBER SPECIFIED.
- VOLTAGE (MEASURED WITH VOLTMETER) ⟨ ▭ IS DC VOLTAGE.(NO INPUT SIGNAL).
- ALL PNP TRANSISTORS ARE EQUIVALENT TO 2SA1015-GR UNLESS OTHERWISE NOTED.
- ALL NPN TRANSISTORS ARE EQUIVALENT TO 2SC1815-GR UNLESS OTHERWISE NOTED.
- ALL DIODES ARE EQUIVALENT TO 1SS133 UNLESS OTHERWISE NOTED.
- ELECTROLYTIC CAPACITORS (⊣⁺) ARE IN uF/WV.
- ALL CAPACITORS ARE IN pF/50WV UNLESS OTHERWISE NOTED.
  EX) 030- 3pF 330- 33pF 331- 330pF 333- 0.033uF
- ALL RESISTORS ARE IN OHMS 1/4WATTS UNLESS OTHERWISE NOTED.
- THE THICK LINES ON PC BOARD ARE THE PRINTING SIDE OF THE PARTS.
  EX) ▭ ← PRINTING SIDE
- CIRCUIT IS SUBJECT TO CHANGE FOR IMPROVEMENT.

A B C D

SCHEMATIC DIAGRAM-2(SD-2)
POWER AMP SECTION-1

NAAF-8911 (2/2)

U15
AMPLIFIER PC BOARD

POWER TRANSISTOR LIST

TYPE	Q6050-56	Q6060-66
D,W,G,PA	MN130S	MP130S
PP,PB	2SC5242	2SA1962

NOTE

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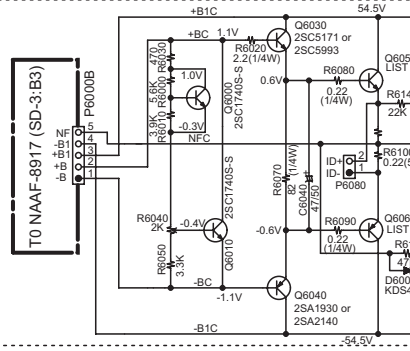
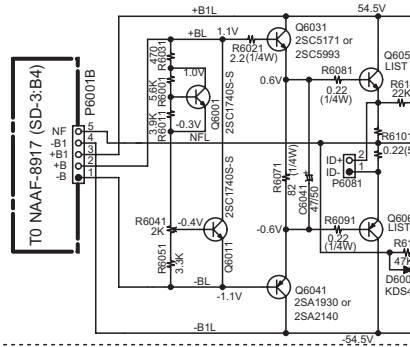
- CIRCUIT IS SUBJECT TO CHANGE FOR IMPROVEMENT.

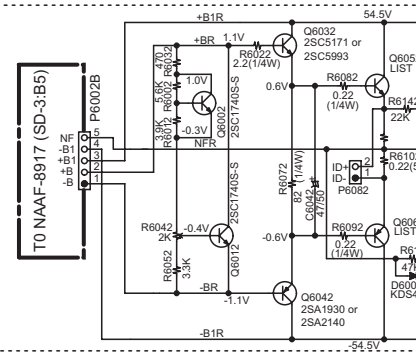
Center ch



Front L ch

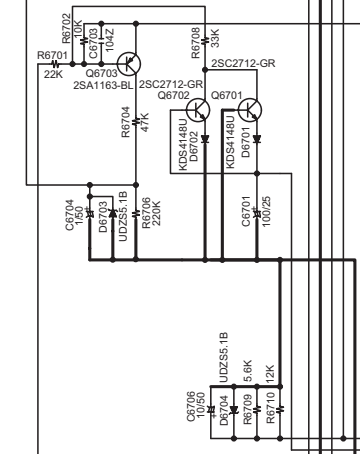


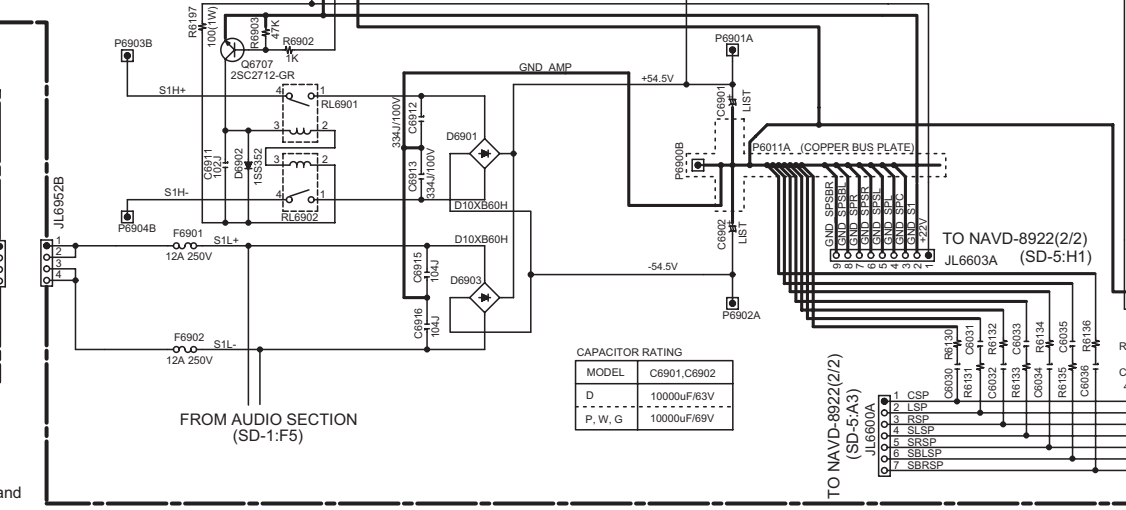
Front R ch



FROM AUDIO SECTION (SD-1:G1&F4)

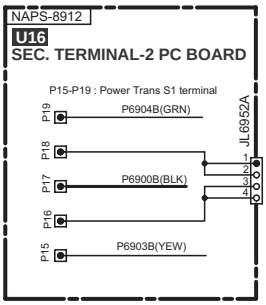
VOLH
SEC1H
GNDS1
+22V
PROTECT





FROM AUDIO SECTION (SD-1:F5)

NAPS-8912
U16
SEC. TERMINAL-2 PC BOARD

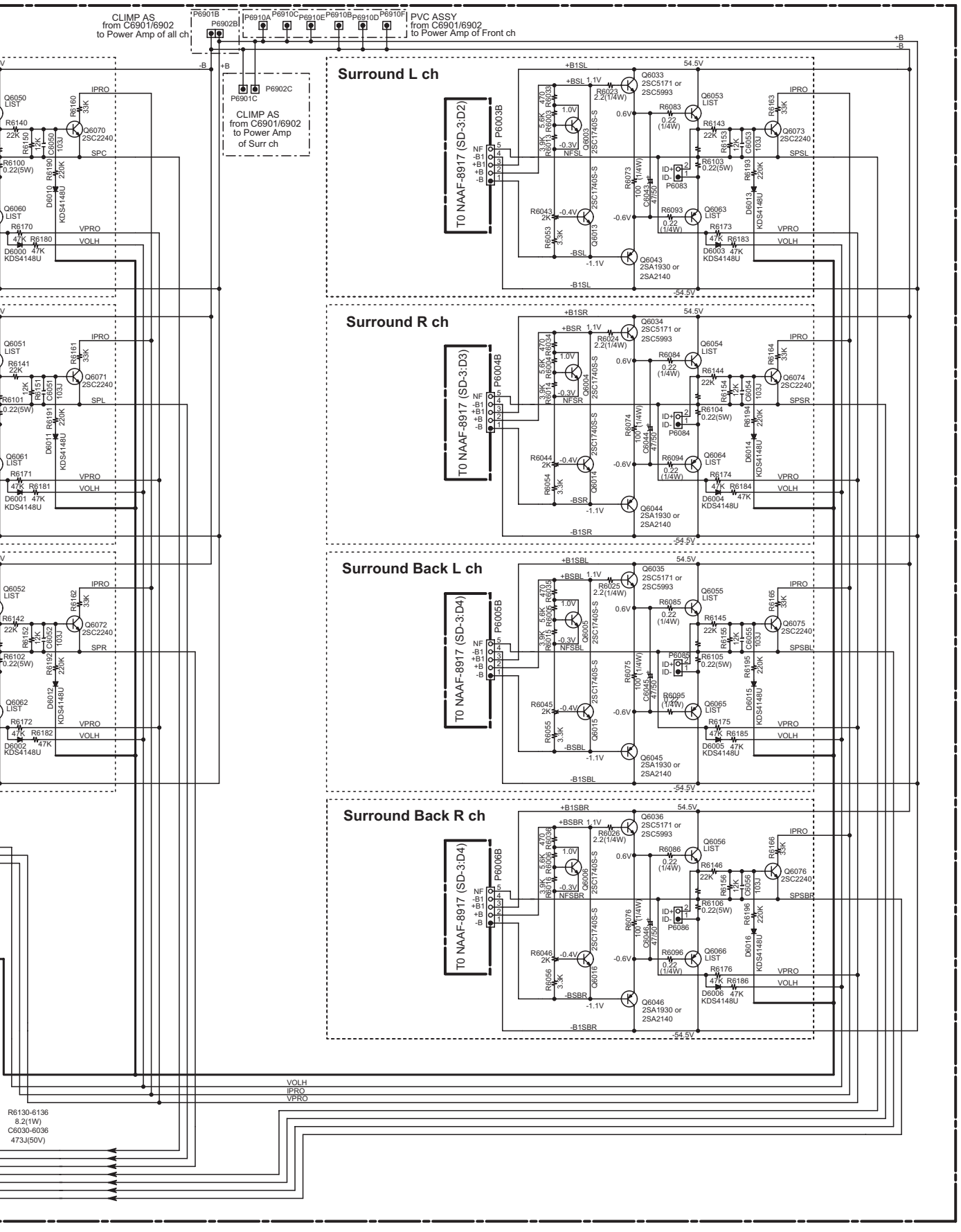


CAPACITOR RATING

MODEL	C6901,C6902
D	10000uF/63V
P, W, G	10000uF/69V

<Note>
SD-x:XY is short for Shcematic Diagram-x and each socket's location, X=A to H, Y=1 to 5.

E F G H


CLIMP AS
from C6901/6902
to Power Amp of all ch
P6901B
P6902B
P6910A
P6910C
P6910E
P6910B
P6910D
P6910F
PVC ASSY
from C6901/6902
to Power Amp of Front ch
+B
-B
P6902C
P6901C
CLIMP AS
from C6901/6902
to Power Amp
of Surr ch
Surround L ch
Surround R ch
Surround Back L ch
Surround Back R ch
T0 NAAF-8917 (SD-3:D2)
T0 NAAF-8917 (SD-3:D3)
T0 NAAF-8917 (SD-3:D4)
P6003B
P6004B
P6005B
P6006B
NF
-B1
+B1
+B
-B
+B1SL
-B1SL
+B1SR
-B1SR
+B1SBL
-B1SBL
+B1SBR
-B1SBR
54.5V
-54.5V
+BSL
-BSL
+BSR
-BSR
+BSBL
-BSBL
+BSBR
-BSBR
1.1V
1.0V
0.6V
-0.3V
-0.4V
-1.1V
NFSL
NFSR
NFSBL
NFSBR
Q6033
2SC5171 or
2SC5993
Q6034
Q6035
Q6036
Q6043
2SA1930 or
2SA2140
Q6044
Q6045
Q6046
Q6003
Q6004
Q6005
Q6006
Q6013
Q6014
Q6015
Q6016
2SC1740S-S
R6023
R6024
R6025
R6026
2.2(1/4W)
R6083
R6084
R6085
R6086
0.22
(1/4W)
R6093
R6094
R6095
R6096
(1/4W)
R6103
R6104
R6105
R6106
0.22(5W)
P6083
P6084
P6085
P6086
ID+
ID-
R6073
R6074
R6075
R6076
100
(1/4W)
C6043
C6044
C6045
C6046
47/50
R6043
R6044
R6045
R6046
2K
R6053
R6054
R6055
R6056
3.3K
R6033
R6034
R6035
R6036
470
R6013
R6014
R6015
R6016
3.9K
R6003
R6004
R6005
R6006
5.6K
Q6053
LIST
Q6054
Q6055
Q6056
Q6063
Q6064
Q6065
Q6066
R6143
R6144
R6145
R6146
R6153
R6154
R6155
R6156
R6163
R6164
R6165
R6166
Q6073
2SC2240
Q6074
Q6075
Q6076
IPRO
SPSL
SPSR
SPSBL
SPSBR
R6173
R6174
R6175
R6176
R6183
R6184
R6185
R6186
D6003
D6004
D6005
D6006
KDS4148U
VPRO
VOLH
Q6050
LIST
Q6051
Q6052
Q6060
Q6061
Q6062
Q6070
2SC2240
Q6071
Q6072
R6140
R6141
R6142
R6150
R6151
R6152
R6160
R6161
R6162
SPC
SPL
SPR
R6100
R6101
R6102
R6170
R6171
R6172
R6180
R6181
R6182
D6000
D6001
D6002
R6190
R6191
R6192
D6010
D6011
D6012
22K
33K
103J
220K
47K
VOLH
IPRO
VPRO
R6130-6136
8.2(1W)
C6030-6036
473J(50V)

SCHEMATIC DIAGRAM-3(SD-3)
POWER AMP SECTION-2

NOTE

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- ALL RESISTORS ARE IN OHMS 1/4WATTS UNLESS OTHERWISE NOTED.
- THE THICK LINES ON PC BOARD ARE THE PRINTING SIDE OF THE PARTS. EX) ○○○ PRINTING SIDE
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NAAF-8917

U19 DRIVER AMPLIFIER PC BOARD

TO NAAF-8911(1/2) (SD-1:G4)

P5503A P5504A

P6011B COPPER BUS PLATE

P5019

Surround L ch

Center ch

Surround R ch

Front L ch

Surround Back L ch

Front R ch

Surround Back R ch

TO NAAF-8911(2/2) (SD-2:F1)

TO NAAF-8911(2/2) (SD-2:D1)

TO NAAF-8911(2/2) (SD-2:F2)

TO NAAF-8911(2/2) (SD-2:D2)

TO NAAF-8911(2/2) (SD-2:F3)

TO NAAF-8911(2/2) (SD-2:D3)

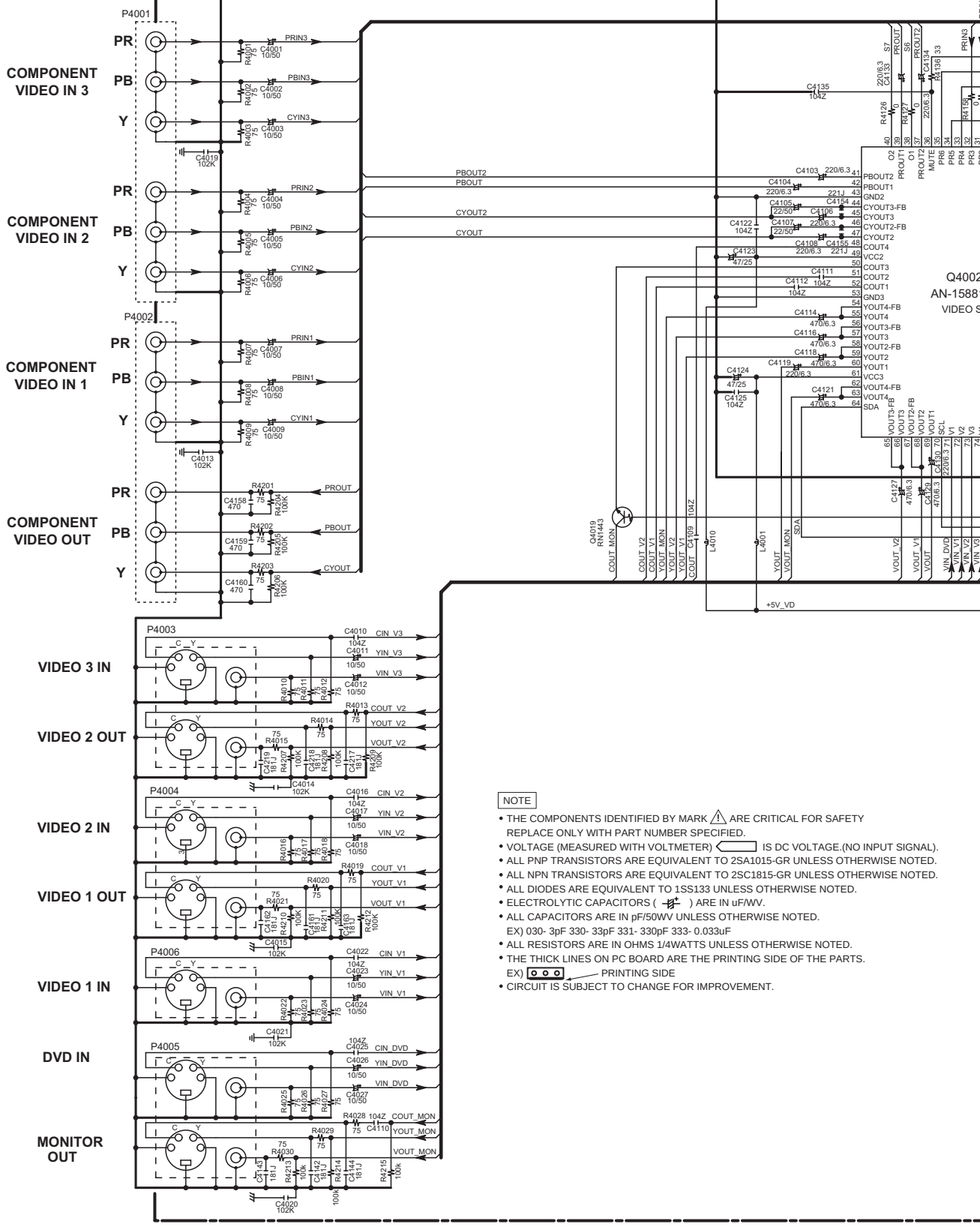
TO NAAF-8911(2/2) (SD-2:F4)

<Note>
SD-x:XY is short for Shcematic Diagram-x and each socket's location, X=A to H, Y=1 to 5.

SCHEMATIC DIAGRAM-4(SD-4)
VIDEO SECTION

NAVD-8922(1/2)

U14 VIDEO PC BOARD



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  EX) ⊙⊙⊙ PRINTING SIDE
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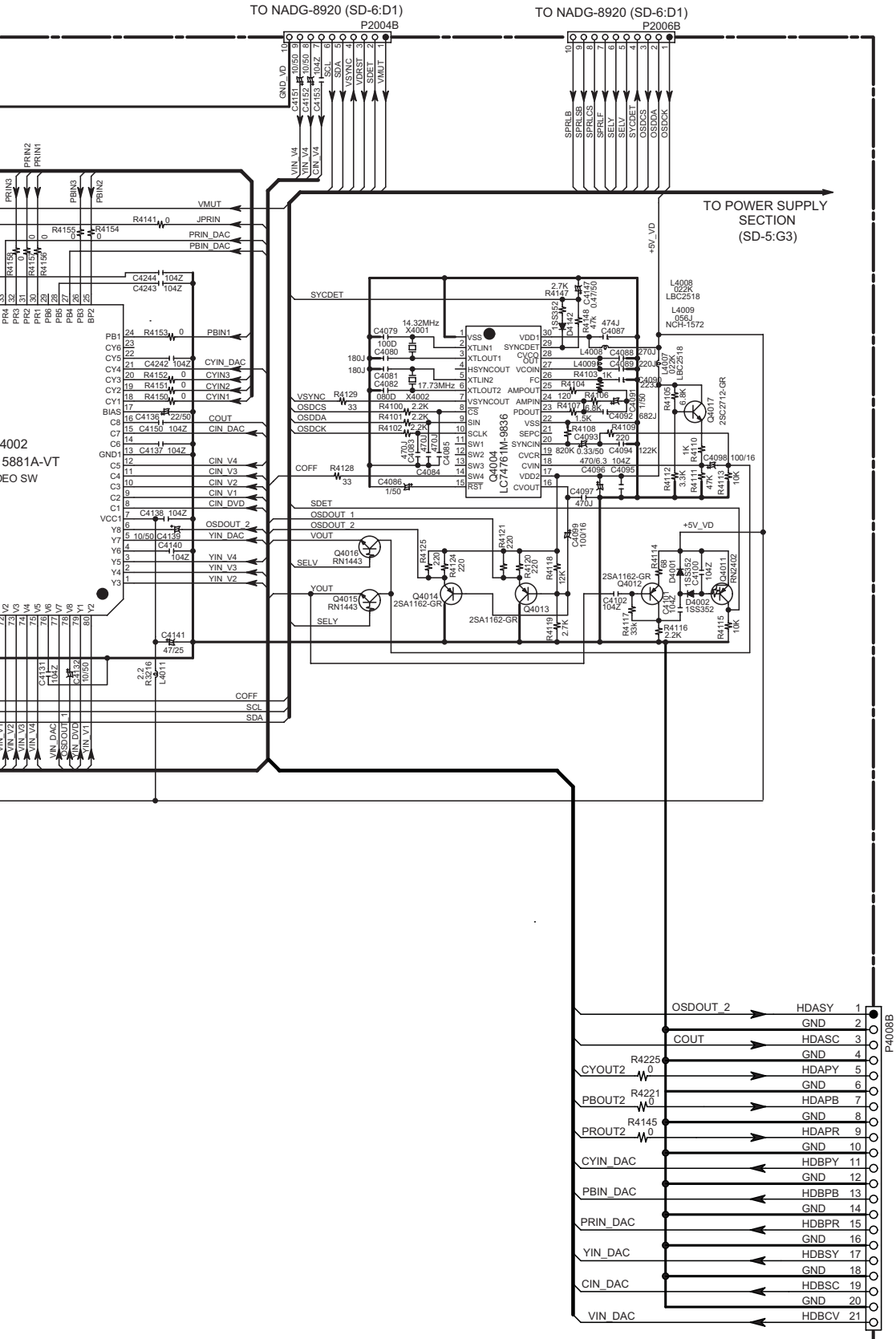
E F G H



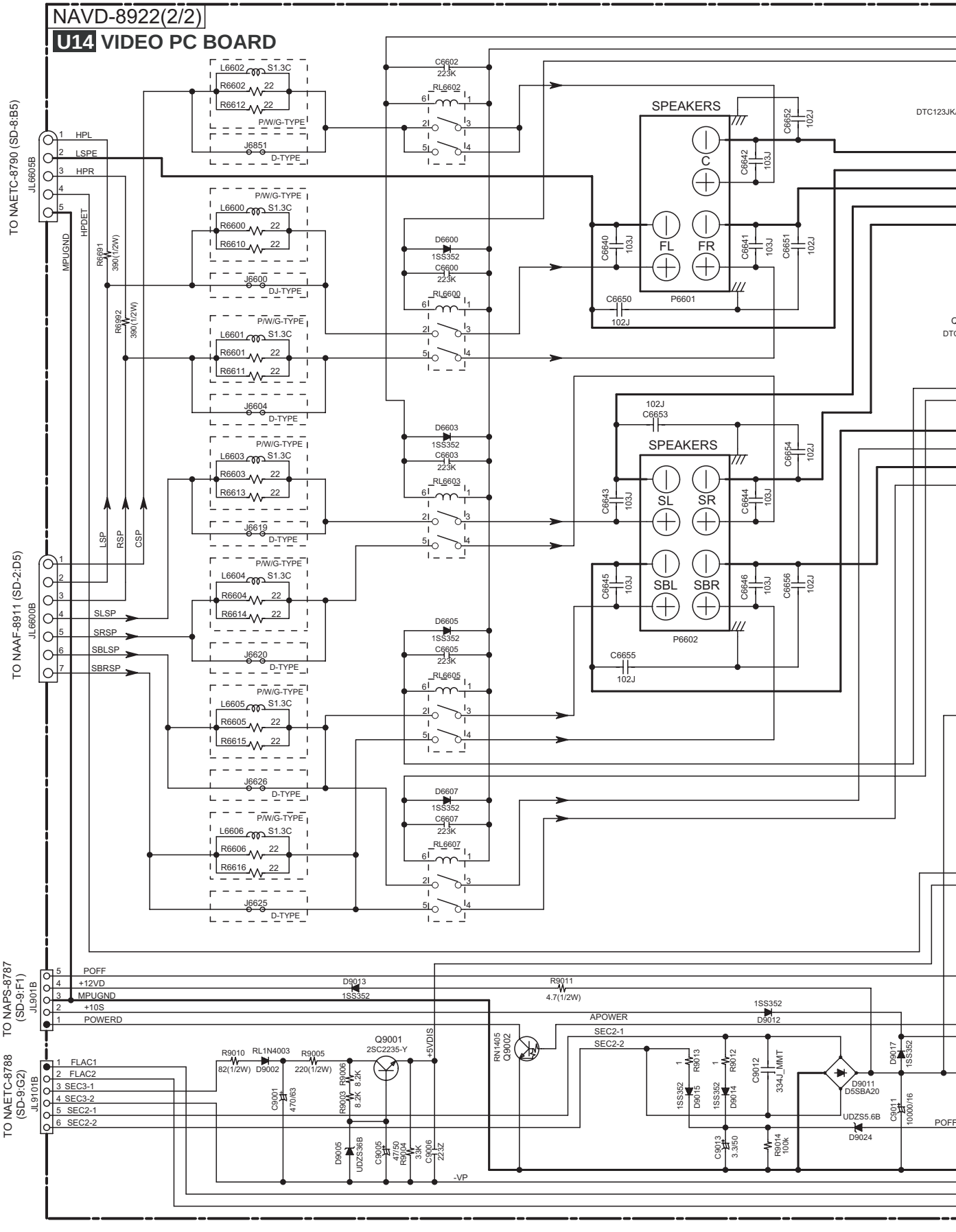
<Note>
SD-x:XY is short for Shcematic Diagram-x and each socket's location, X=A to H, Y=1 to 5.
</Note>

SCHEMATIC DIAGRAM-5(SD-5)
POWER SUPPLY SECTION

<Note>
SD-x:XY is short for Shcematic Diagram-x and each socket's location, X=A to H, Y=1 to 5.

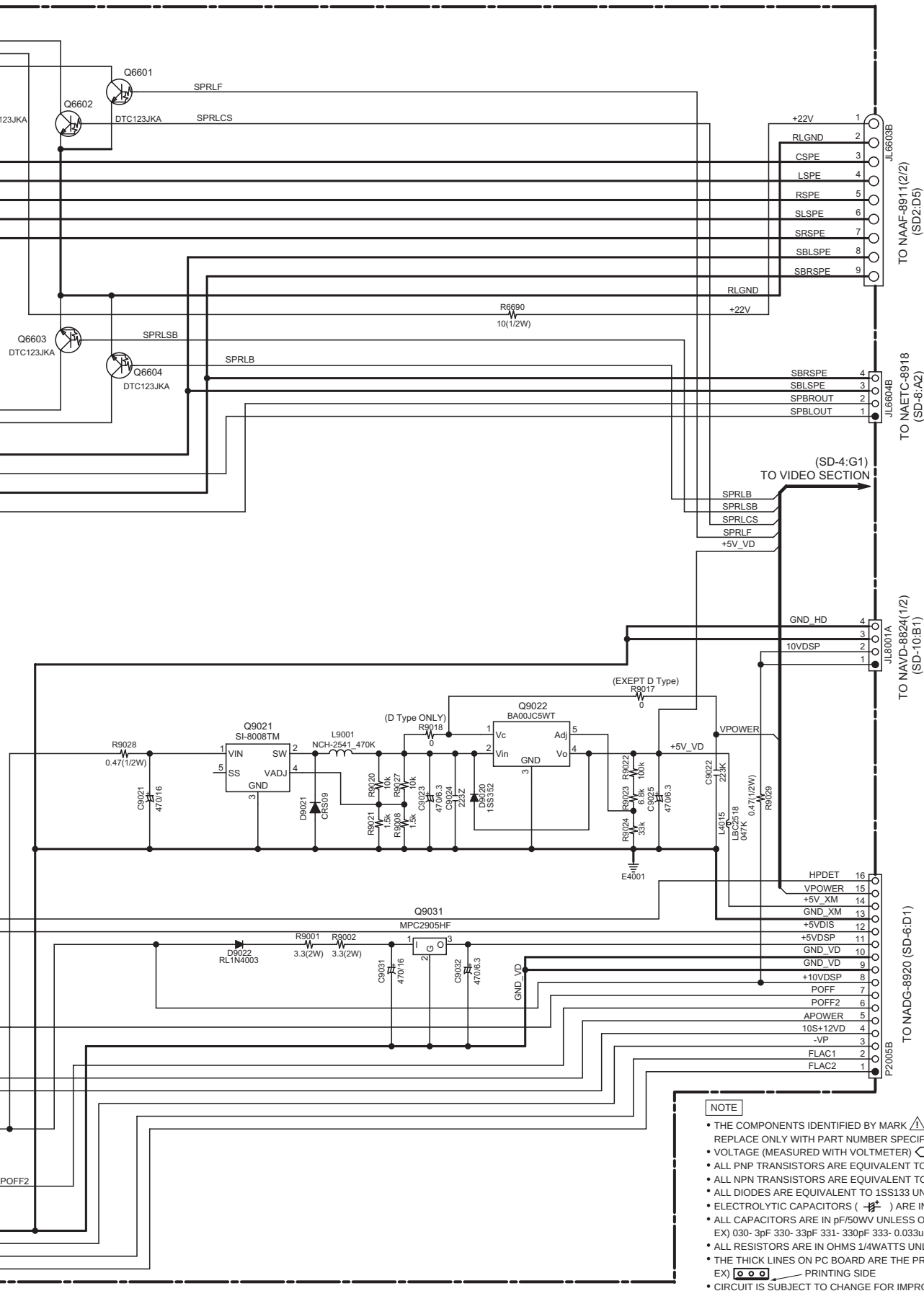
NAVD-8922(2/2)

U14 VIDEO PC BOARD



</Note>

E F G H



NOTE

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  EX) ▭▭▭ PRINTING SIDE
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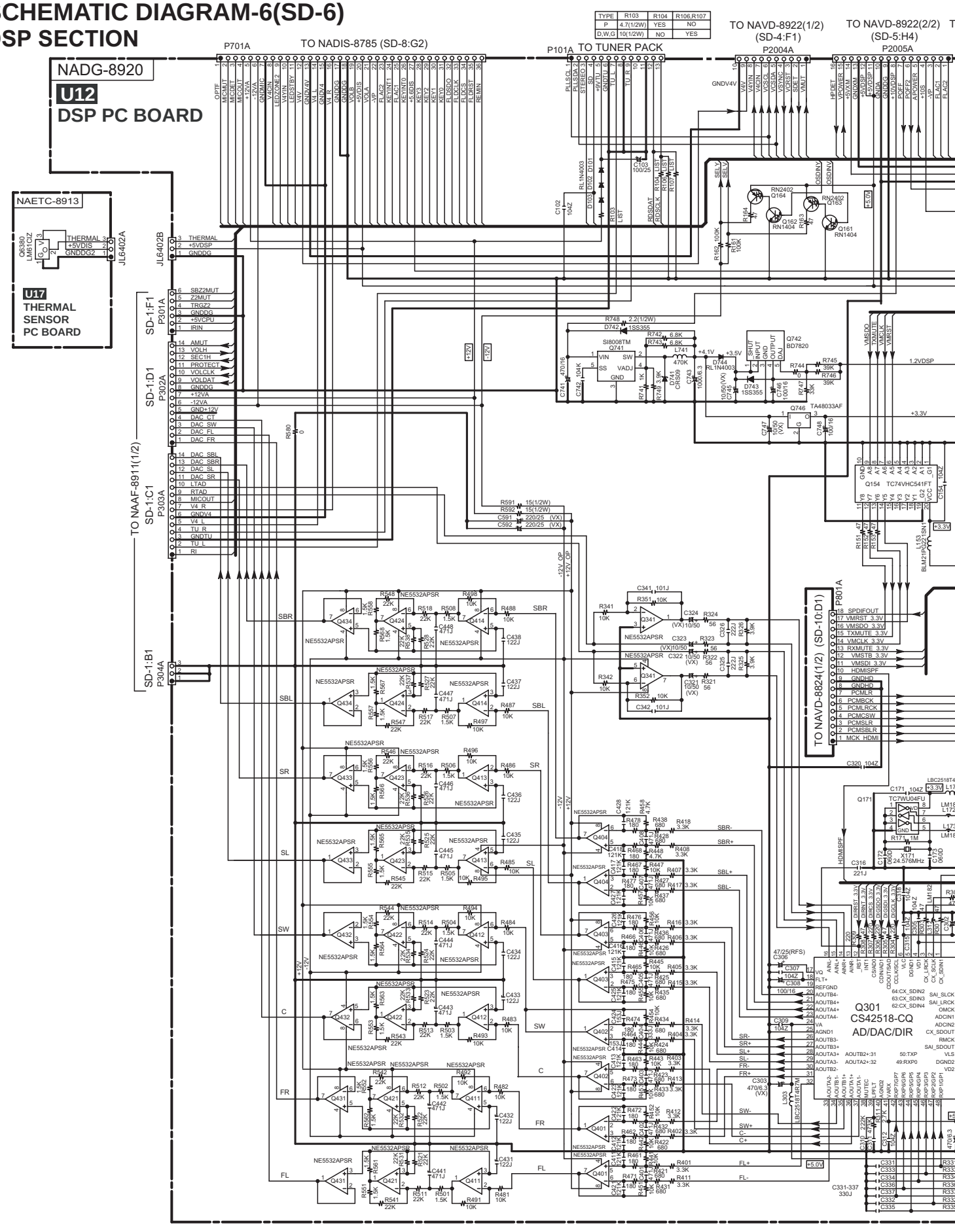
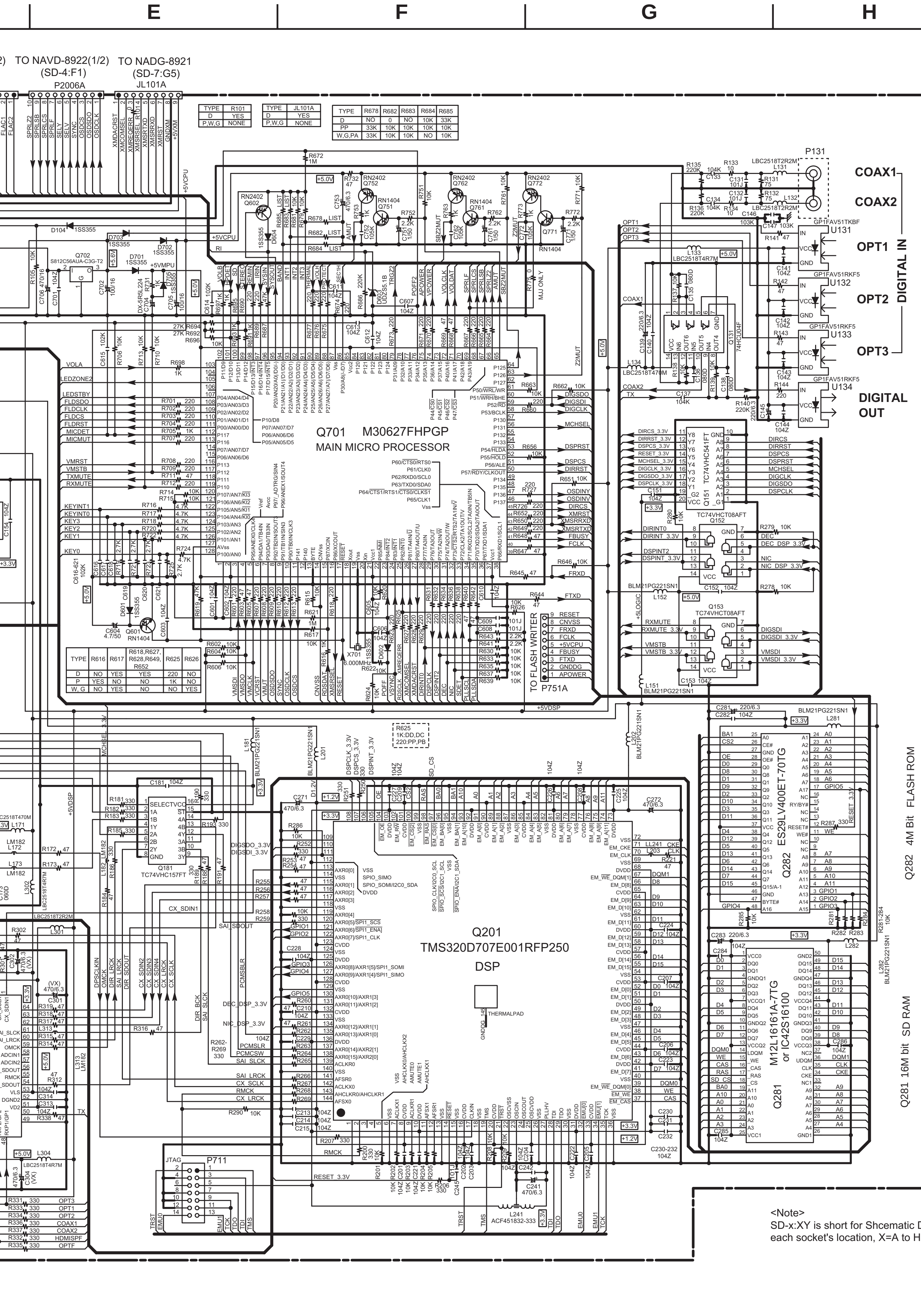
SCHEMATIC DIAGRAM-6(SD-6)
DSP SECTION





TYPE	R101
D	YES
P,W,G	NONE

TYPE	JL101A
D	YES
P,W,G	NONE

TYPE	R678	R682	R683	R684	R685
D	NO	0	NO	10K	33K
PP	33K	10K	10K	10K	10K
W,G,PA	33K	10K	10K	NO	10K

TYPE	R616	R617	R618,R627, R628,R649, R652	R625	R626
D	NO	YES	YES	220	NO
P	YES	NO	NO	1K	NO
W, G	NO	YES	NO	NO	YES

R625
1K:DD,DC
220:PP,PB

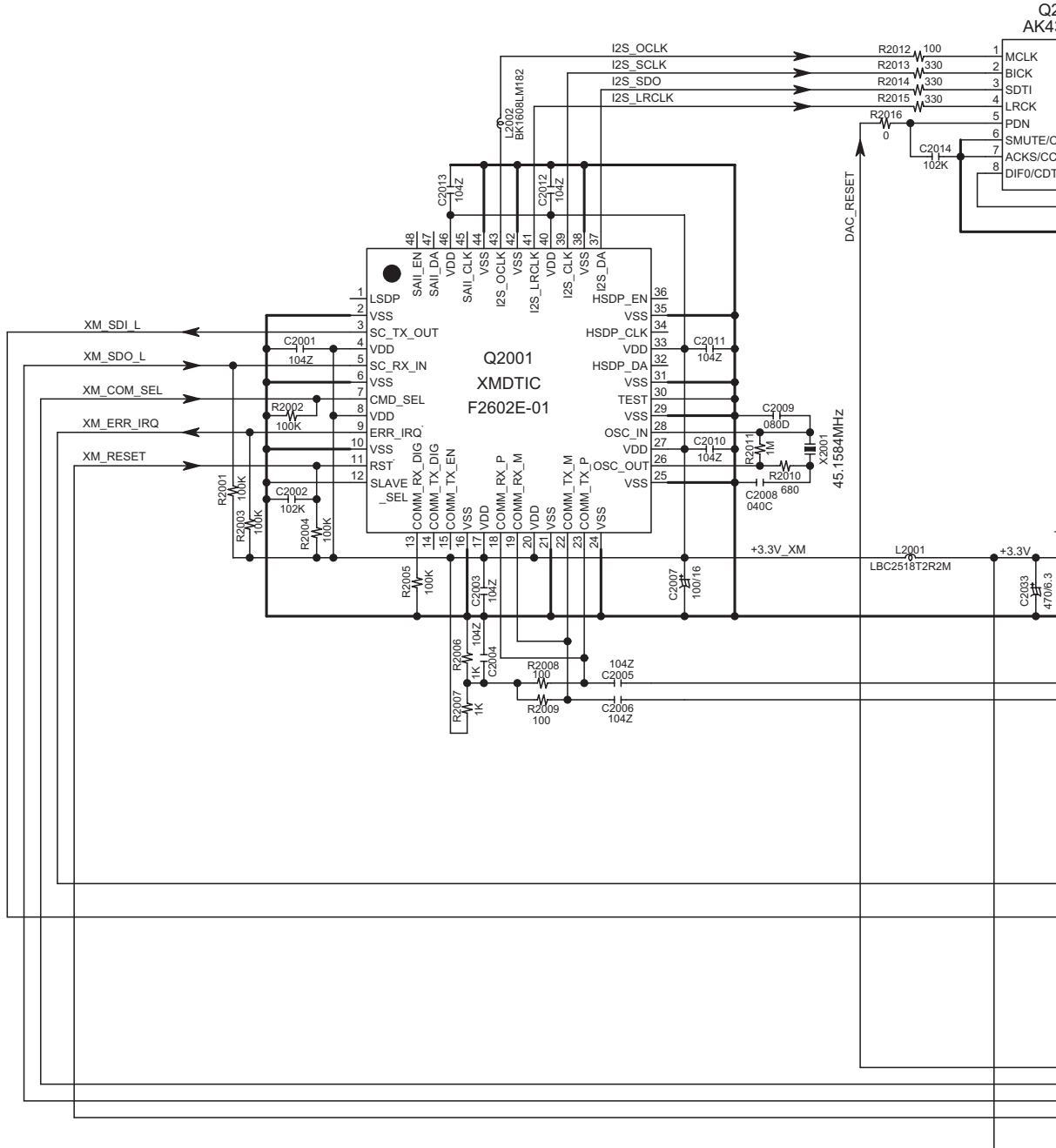
<Note>
SD-x:XY is short for Shcematic Diagram-x and each socket's location, X=A to H, Y=1 to 5.

SCHEMATIC DIAGRAM-7(SD-7)

XM SECTION

NADG-8921

U13 XM PC BOARD



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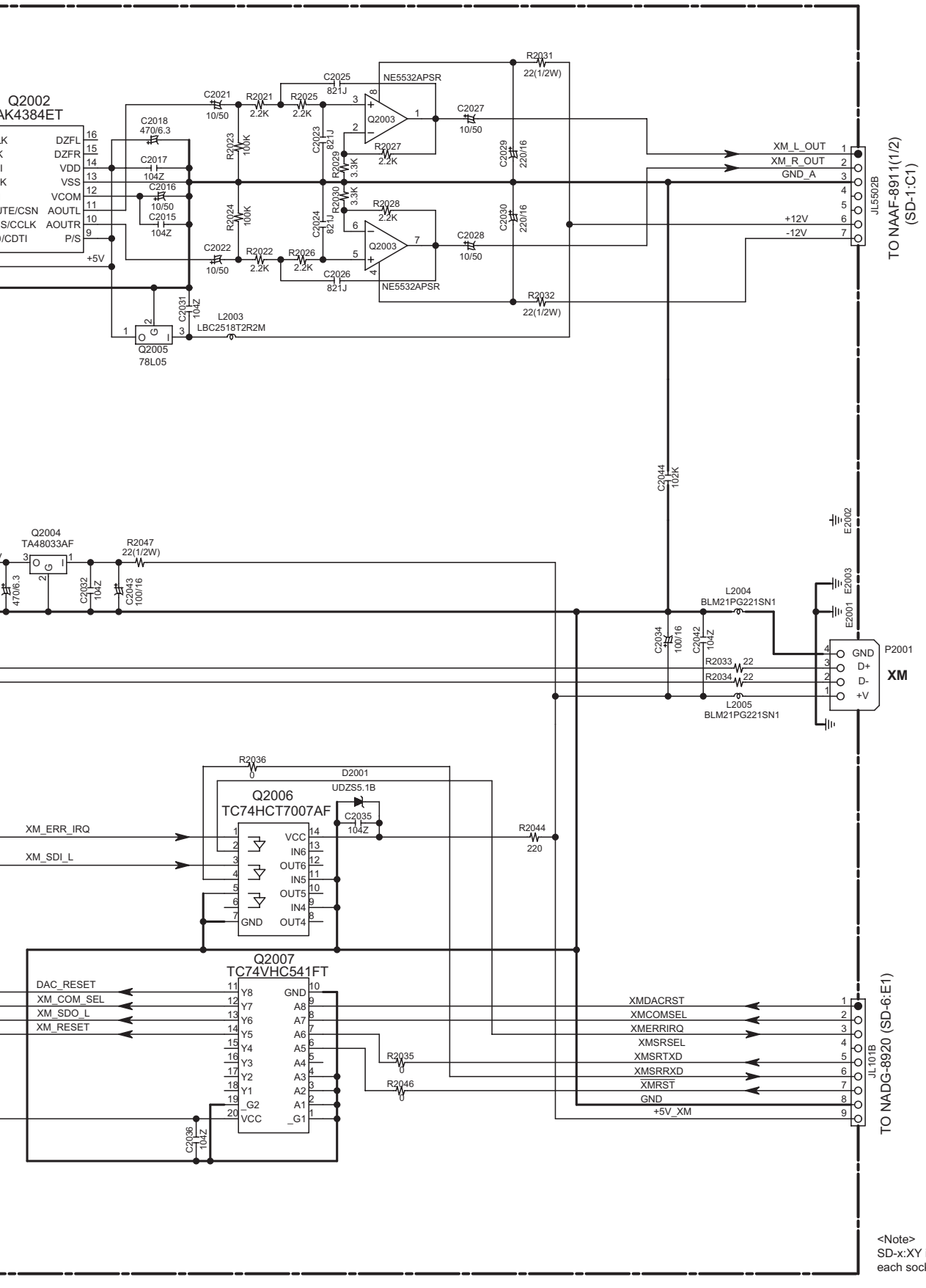
  EX) ▭ ← PRINTING SIDE
- CIRCUIT IS SUBJECT TO CHANGE FOR IMPROVEMENT.

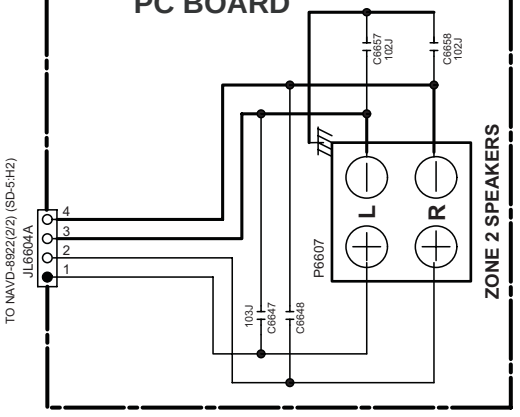
E F G H



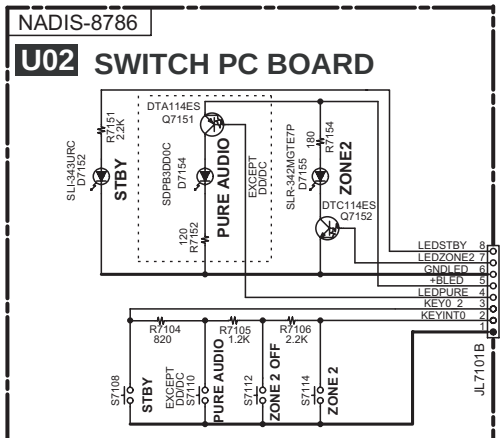
<Note>
SD-x:XY is short for Shcematic Diagram-x and each socket's location, X=A to H, Y=1 to 5.
</Note>

SCHEMATIC DIAGRAM-8(SD-8)
DISPLAY SECTION

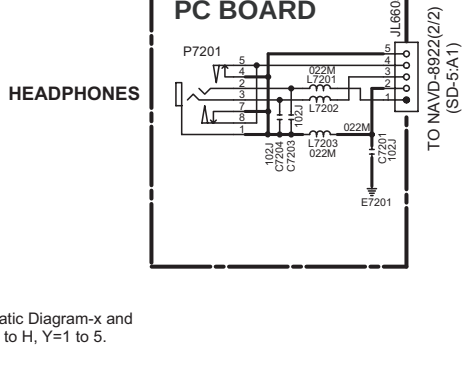
NAETC-8918
U02 SPEAKER TERMINAL PC BOARD



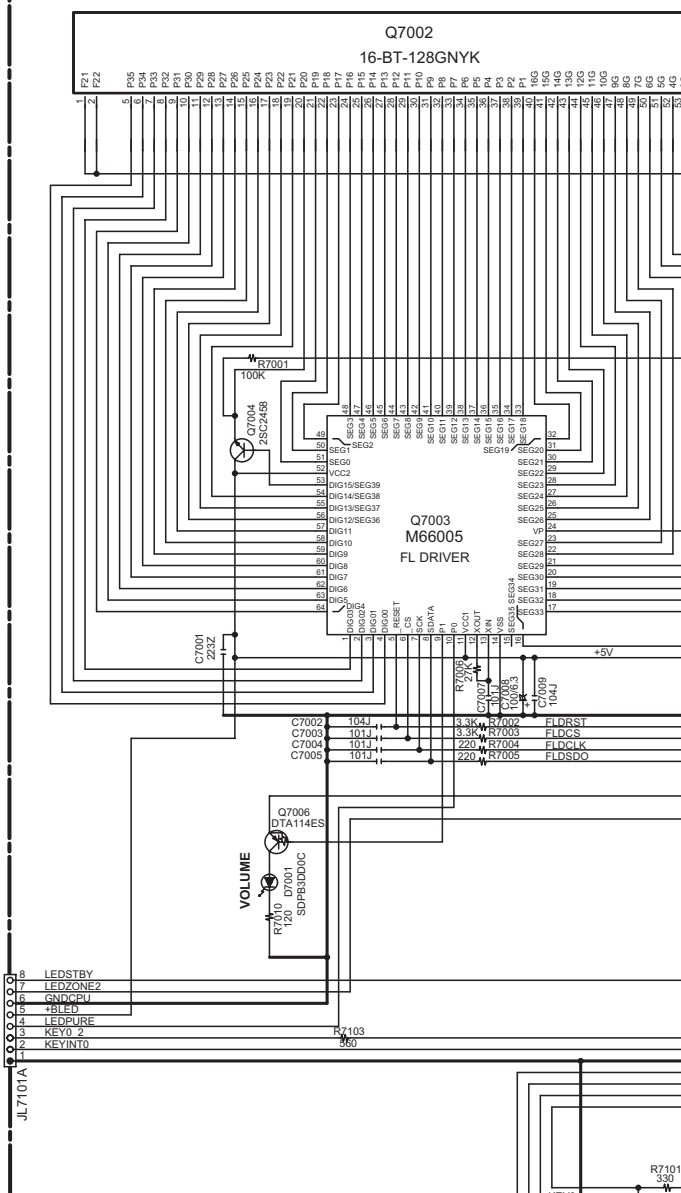
NADIS-8786
U02 SWITCH PC BOARD



NAETC-8790
U06 HEADPHONE PC BOARD

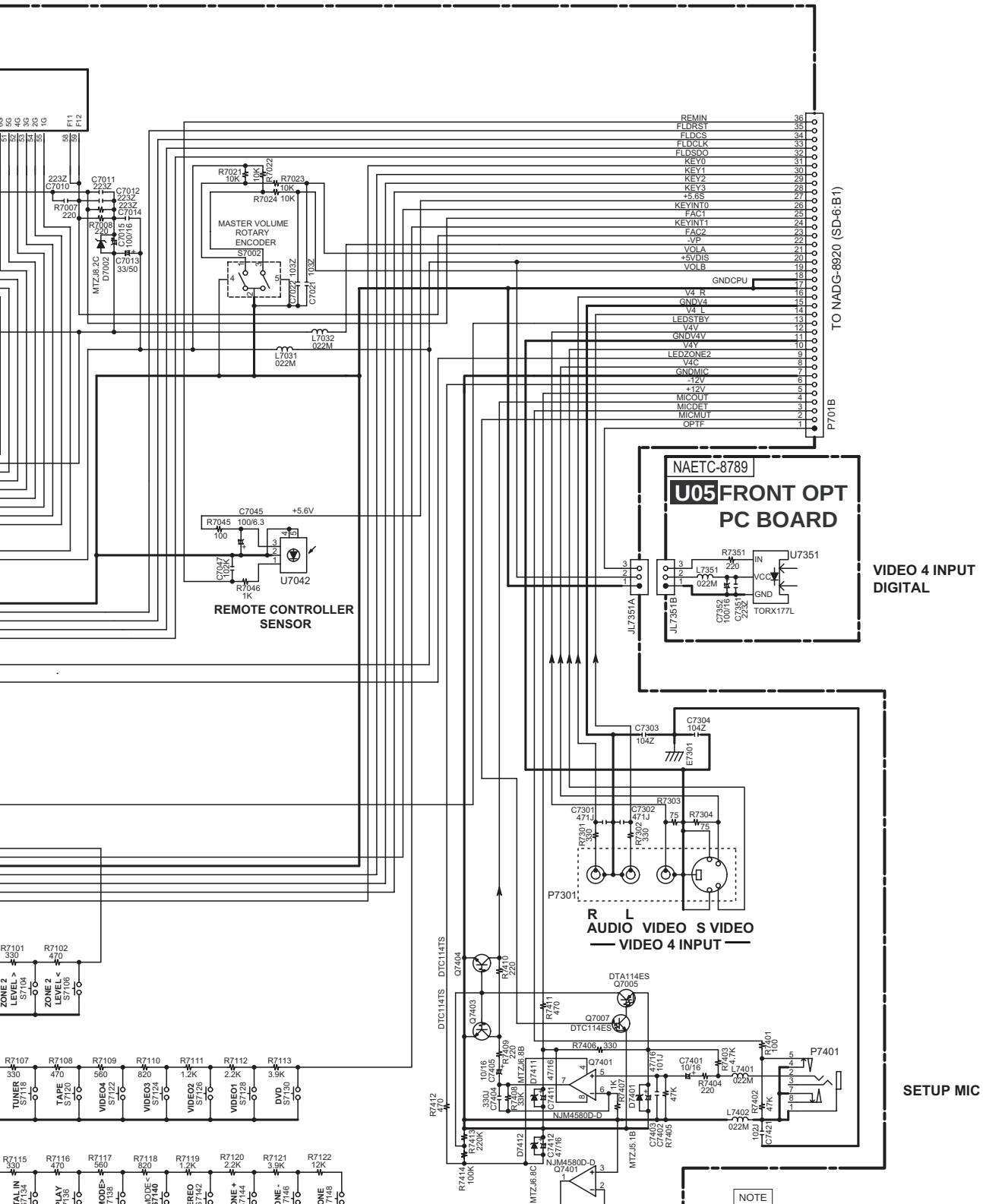


NADIS-8785
U01 DISPLAY PC BOARD



<Note>
SD-x:XY is short for Shcematic Diagram-x and each socket's location, X=A to H, Y=1 to 5.

E F G H



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  EX) 030- 3pF 330- 33pF 331- 330pF 333- 0.033uF
- ALL RESISTORS ARE IN OHMS 1/4WATTS UNLESS OTHERWISE NOTED.
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  EX) ⊙⊙⊙ PRINTING SIDE
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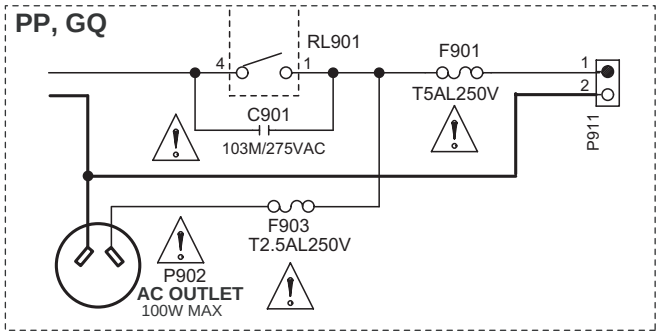
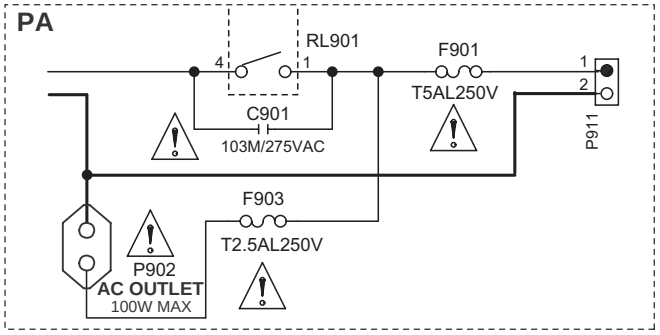
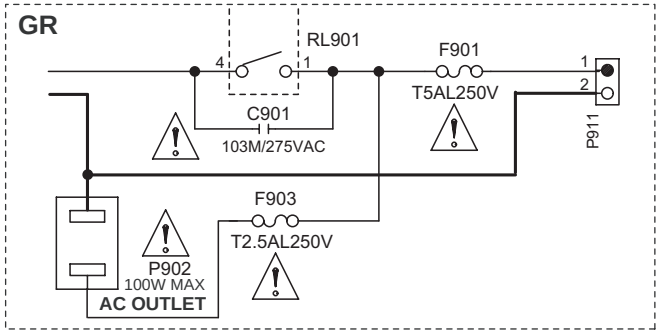
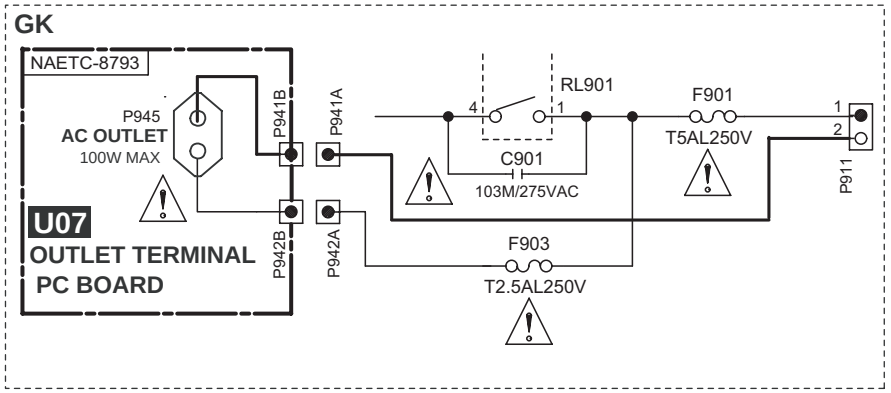
SCHEMATIC DIAGRAM-9(SD-9)

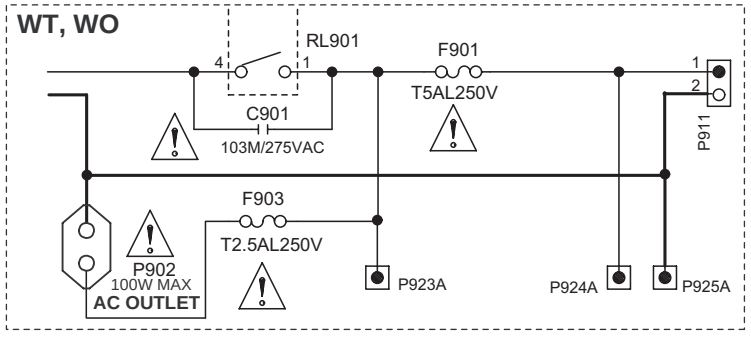
POWER SUPPLY SECTION

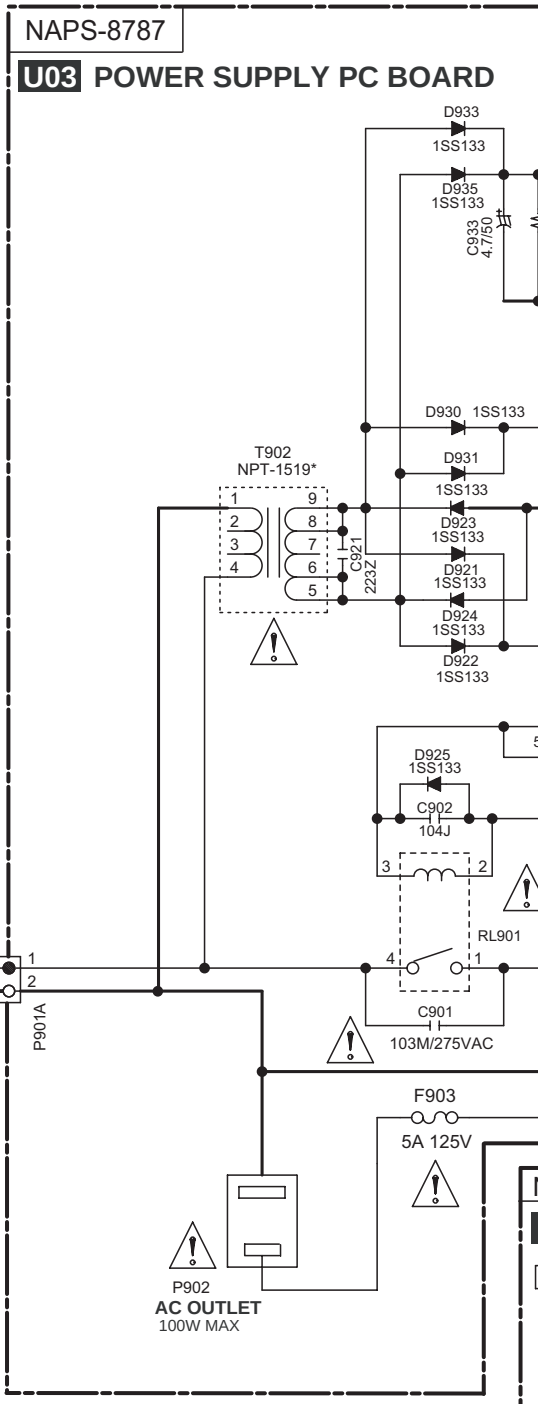












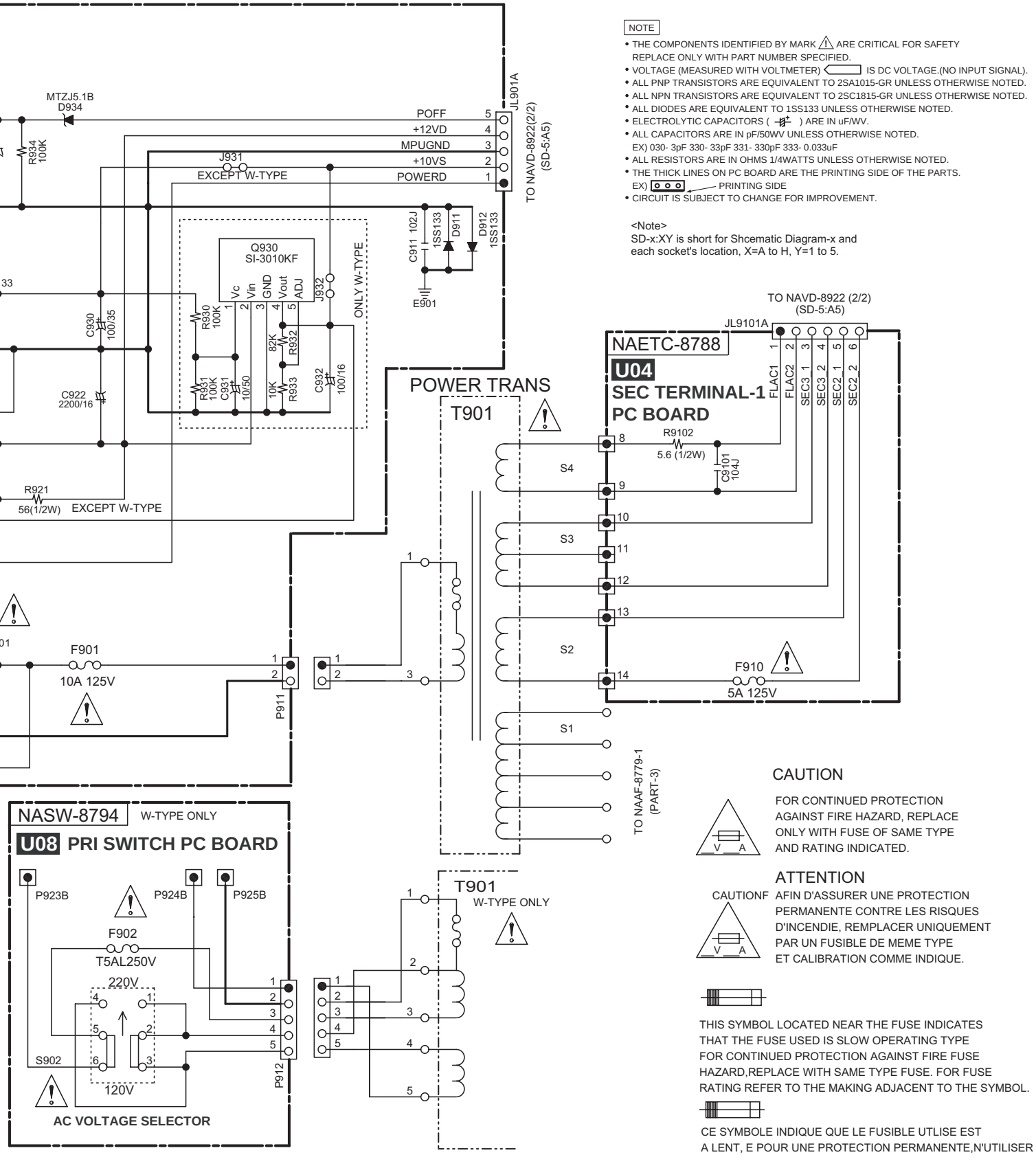
POWER SUPPLY VOLTAGE & FREQ.

TYPE	AC
D	120V 60HZ
P	230-240V 50HZ
G	220-230V 50/60HZ
W	120V/220-240V 50/60HZ

POWER TRANSFORMER

TYPE	T901	T902
D	NPT-1518D	NPT-1520JQ
P	NPT-1518P	NPT-1519GQ
G	NPT-1518G	NPT-1519GQ
W	NPT-1518DQ	NPT-1519JQ

E F G H



NOTE

- THE COMPONENTS IDENTIFIED BY MARK ⚠ ARE CRITICAL FOR SAFETY REPLACE ONLY WITH PART NUMBER SPECIFIED.
- VOLTAGE (MEASURED WITH VOLTMETER) ⟨ ⟩ IS DC VOLTAGE.(NO INPUT SIGNAL).
- ALL PNP TRANSISTORS ARE EQUIVALENT TO 2SA1015-GR UNLESS OTHERWISE NOTED.
- ALL NPN TRANSISTORS ARE EQUIVALENT TO 2SC1815-GR UNLESS OTHERWISE NOTED.
- ALL DIODES ARE EQUIVALENT TO 1SS133 UNLESS OTHERWISE NOTED.
- ELECTROLYTIC CAPACITORS (⊣⊢) ARE IN uF/WV.
- ALL CAPACITORS ARE IN pF/50WV UNLESS OTHERWISE NOTED.
  EX) 030- 3pF 330- 33pF 331- 330pF 333- 0.033uF
- ALL RESISTORS ARE IN OHMS 1/4WATTS UNLESS OTHERWISE NOTED.
- THE THICK LINES ON PC BOARD ARE THE PRINTING SIDE OF THE PARTS.
  EX) ⊙⊙⊙ PRINTING SIDE
- CIRCUIT IS SUBJECT TO CHANGE FOR IMPROVEMENT.

<Note>
SD-x:XY is short for Shcematic Diagram-x and each socket's location, X=A to H, Y=1 to 5.

CAUTION

FOR CONTINUED PROTECTION AGAINST FIRE HAZARD, REPLACE ONLY WITH FUSE OF SAME TYPE AND RATING INDICATED.

ATTENTION

CAUTIONF AFIN D'ASSURER UNE PROTECTION PERMANENTE CONTRE LES RISQUES D'INCENDIE, REMPLACER UNIQUEMENT PAR UN FUSIBLE DE MEME TYPE ET CALIBRATION COMME INDIQUE.

THIS SYMBOL LOCATED NEAR THE FUSE INDICATES THAT THE FUSE USED IS SLOW OPERATING TYPE FOR CONTINUED PROTECTION AGAINST FIRE FUSE HAZARD,REPLACE WITH SAME TYPE FUSE. FOR FUSE RATING REFER TO THE MAKING ADJACENT TO THE SYMBOL.

CE SYMBOLE INDIQUE QUE LE FUSIBLE UTLISE EST A LENT, E POUR UNE PROTECTION PERMANENTE,N'UTILISER QUE DES FUSIBLES DE MEME TYPE. CE DARNIER EST INDIQUE LA QU LE PRESENT SYMBOL EST APPOSE.

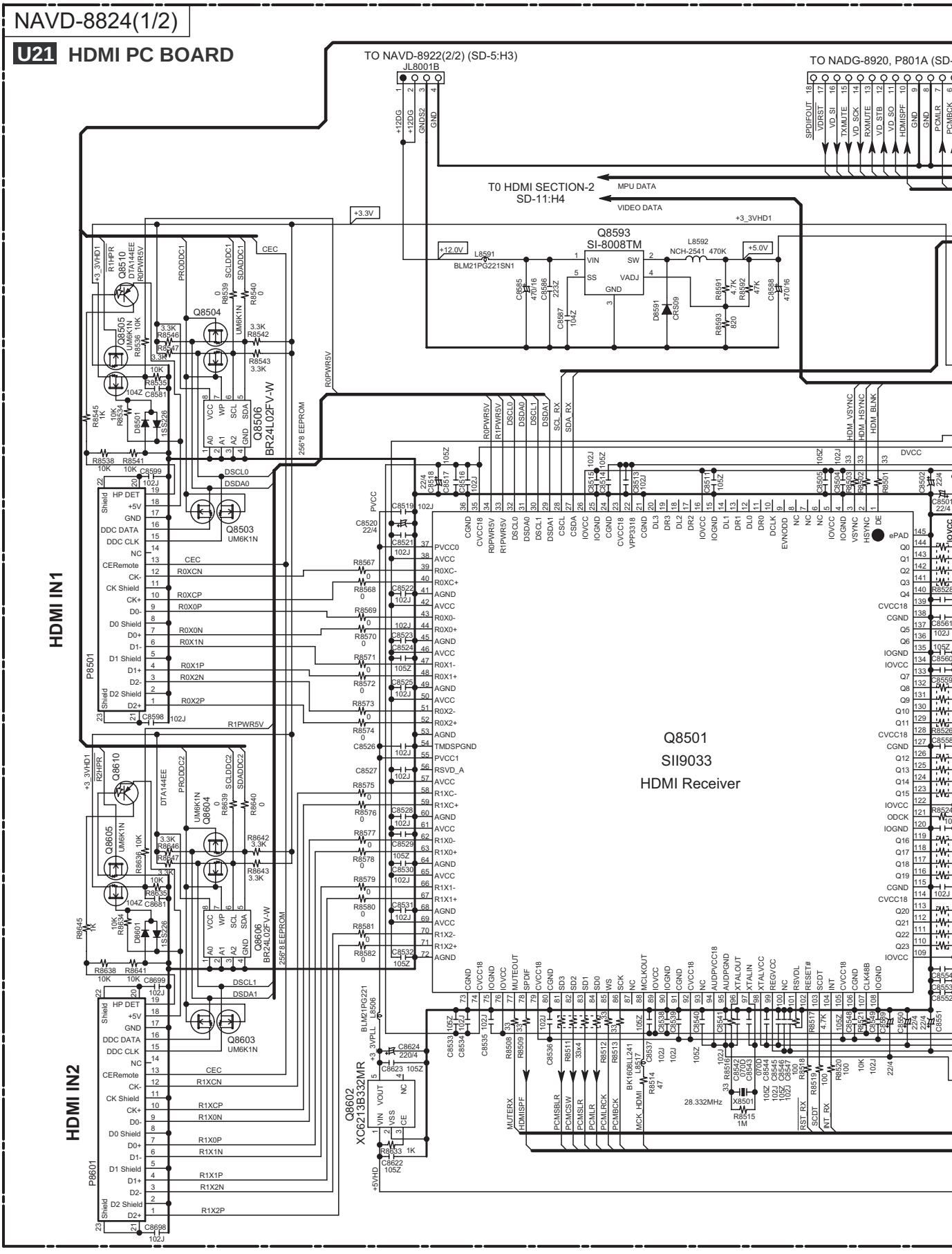
SCHEMATIC DIAGRAM-10(SD-10)

HDMI SECTION-1

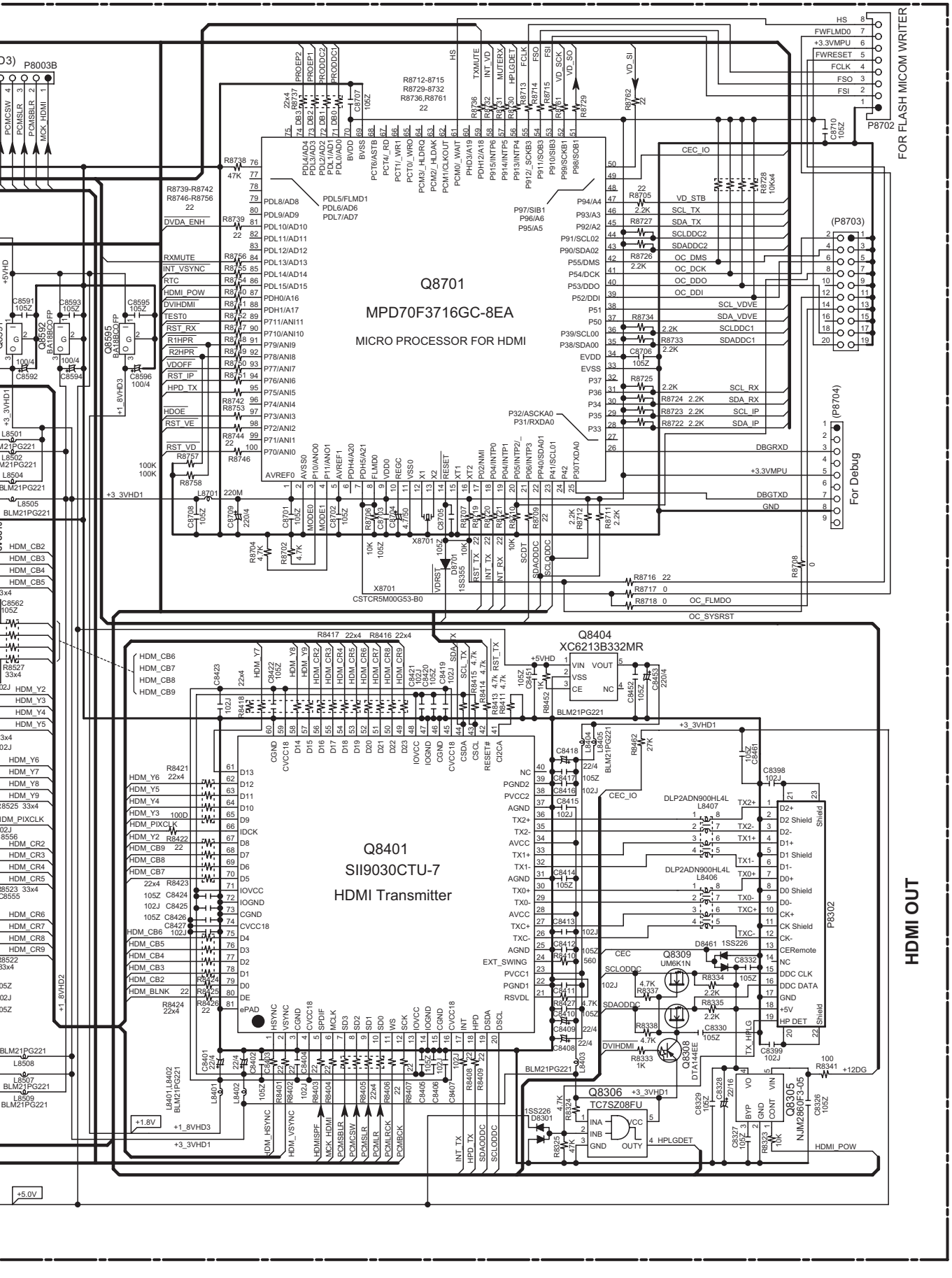
<Note>
SD-x:XY is short for Shcematic Diagram-x and
each socket's location, X=A to H, Y=1 to 5.

NAVD-8824(1/2)

U21 HDMI PC BOARD



E F G H


Q8701
MPD70F3716GC-8EA
MICRO PROCESSOR FOR HDMI
X8701
CSTCR5M00G53-B0
Q8404
XC6213B332MR
Q8401
SII9030CTU-7
HDMI Transmitter
Q8306
TC7SZ08FU
Q8308
DTA144EE
Q8309
UM6K1N
Q8305
NJM2860F33-05
P8003B
P8702
FOR FLASH MICOM WRITER
(P8703)
(P8704)
For Debug
P8302
HDMI OUT
HDMI_POW
+5.0V
+3_3VHD1
+1_8VHD3
+1.8V
+12DG

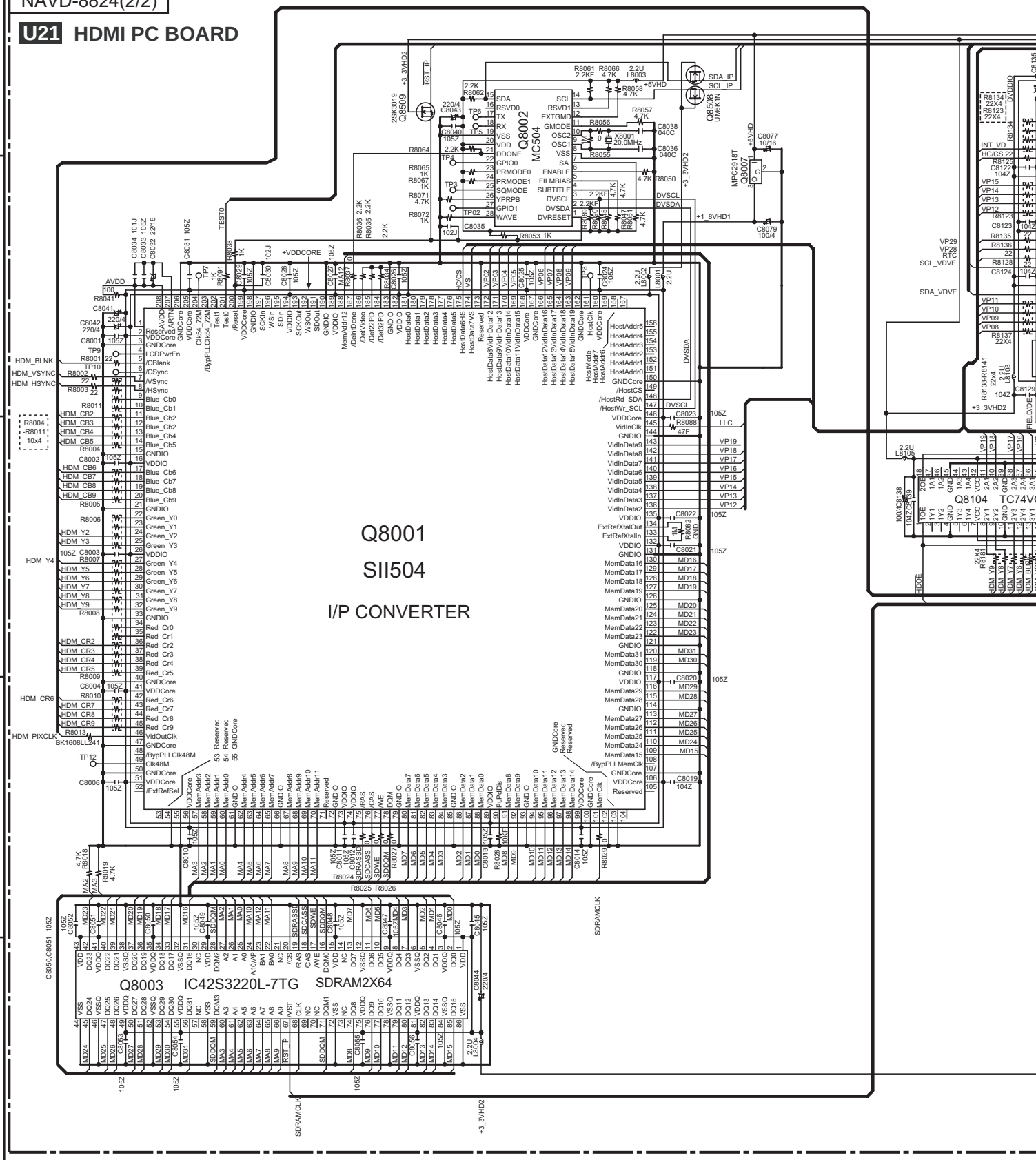
SCHEMATIC DIAGRAM-11(SD-11)

HDMI SECTION-2

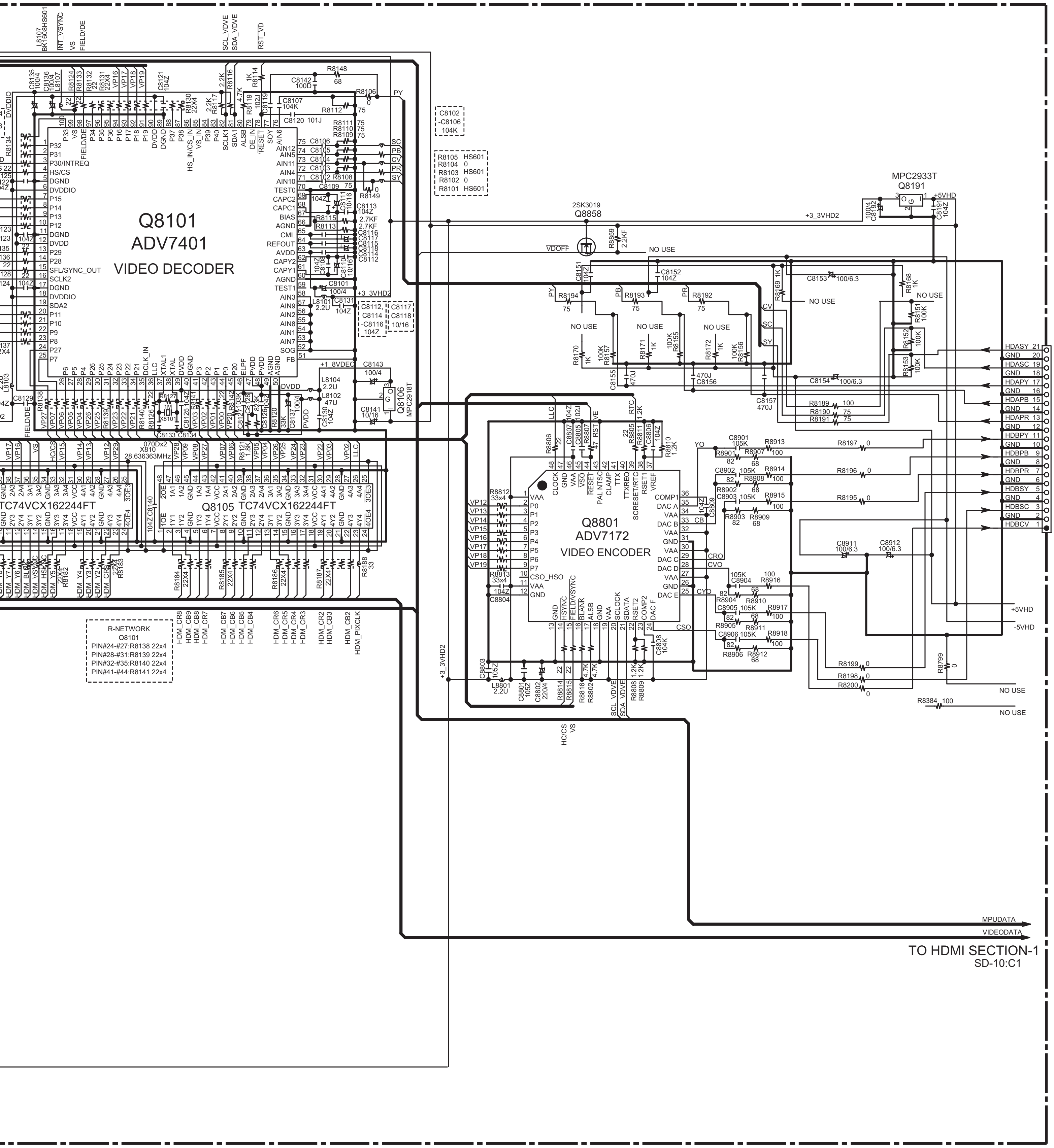
<Note>
SD-x:XY is short for Shcematic Diagram-x and each socket's location, X=A to H, Y=1 to 5.

NAVD-8824(2/2)

U21 HDMI PC BOARD



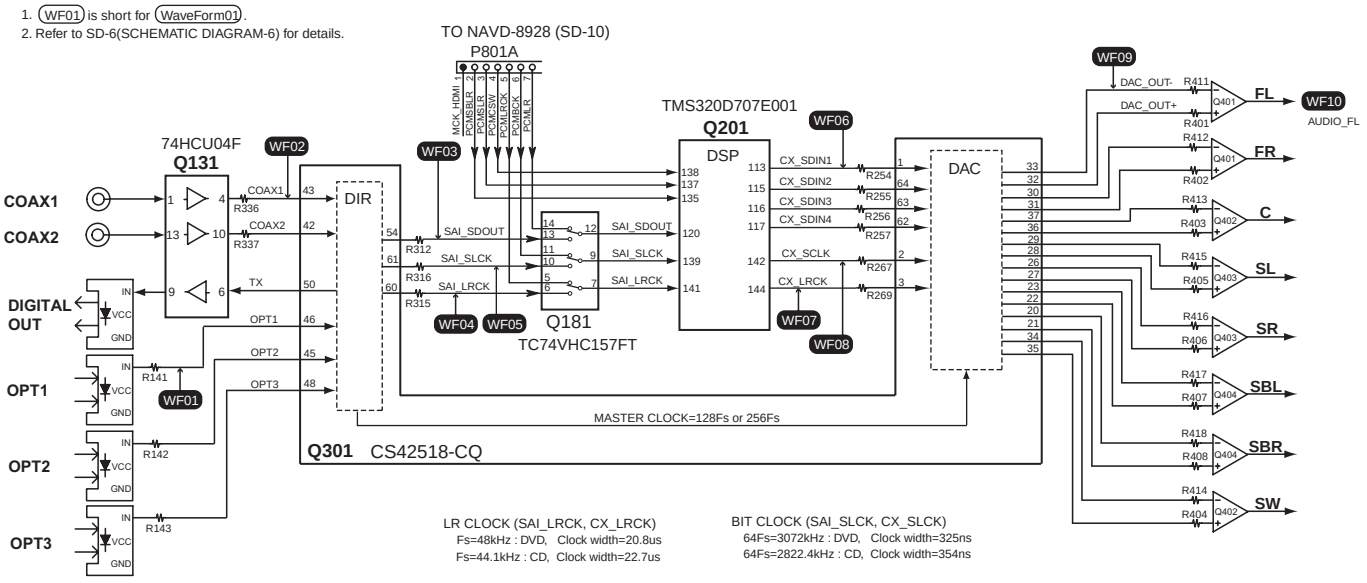
E	F	G	H


Q8101
ADV7401
VIDEO DECODER
Q8801
ADV7172
VIDEO ENCODER
Q8105 TC74VCX162244FT
TC74VCX162244FT
MPC2933T
Q8191
2SK3019
Q8858
Q8106
MPC2918T
R-NETWORK
Q8101
PIN#24-#27:R8138 22x4
PIN#28-#31:R8139 22x4
PIN#32-#35:R8140 22x4
PIN#41-#44:R8141 22x4
P4008A
TO NAVD-8922(1/2) (SD-4:G4)
MPUDATA
VIDEODATA
TO HDMI SECTION-1
SD-10:C1

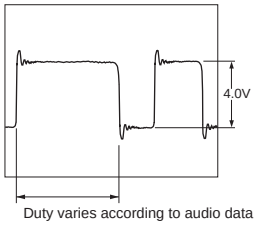
A B C D

SCHEMATIC DIAGRAM-12(SD-12)
DIGITAL AUDIO WAVE FORM SECTION

NOTE:
1. (WF01) is short for (WaveForm01).
2. Refer to SD-6(SCHEMATIC DIAGRAM-6) for details.

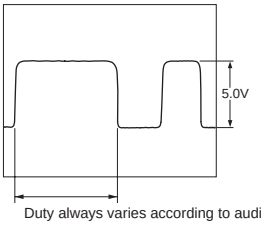


WF01 OPT1



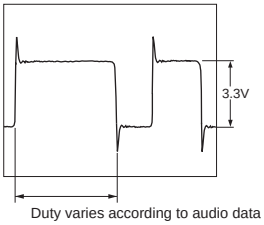
Duty varies according to audio data

WF02 COAX1



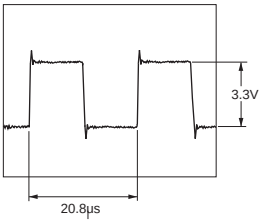
Duty always varies according to audio data

WF03 SAI_SDOUT

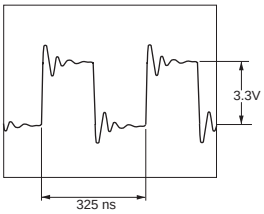


Duty varies according to audio data

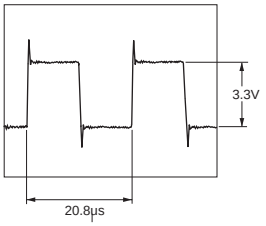
WF04 SAI_LRCK



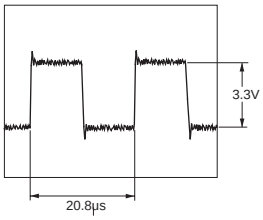
WF05 SAI_SLCK



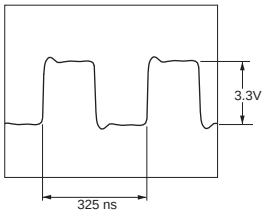
WF06 CX_SDIN1



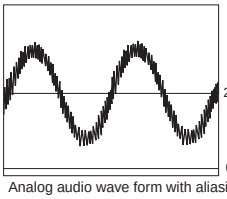
WF07 CX_LRCK



WF08 CX_SCLK

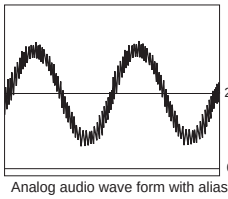


WF09 DAC_OUT-



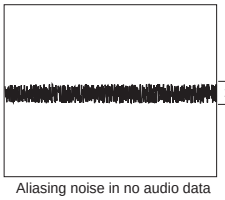
Analog audio wave form with aliasing noise

WF10 AUDIO_FL



Analog audio wave form with aliasing noise

WF10 AUDIO_FL



Aliasing noise in no audio data

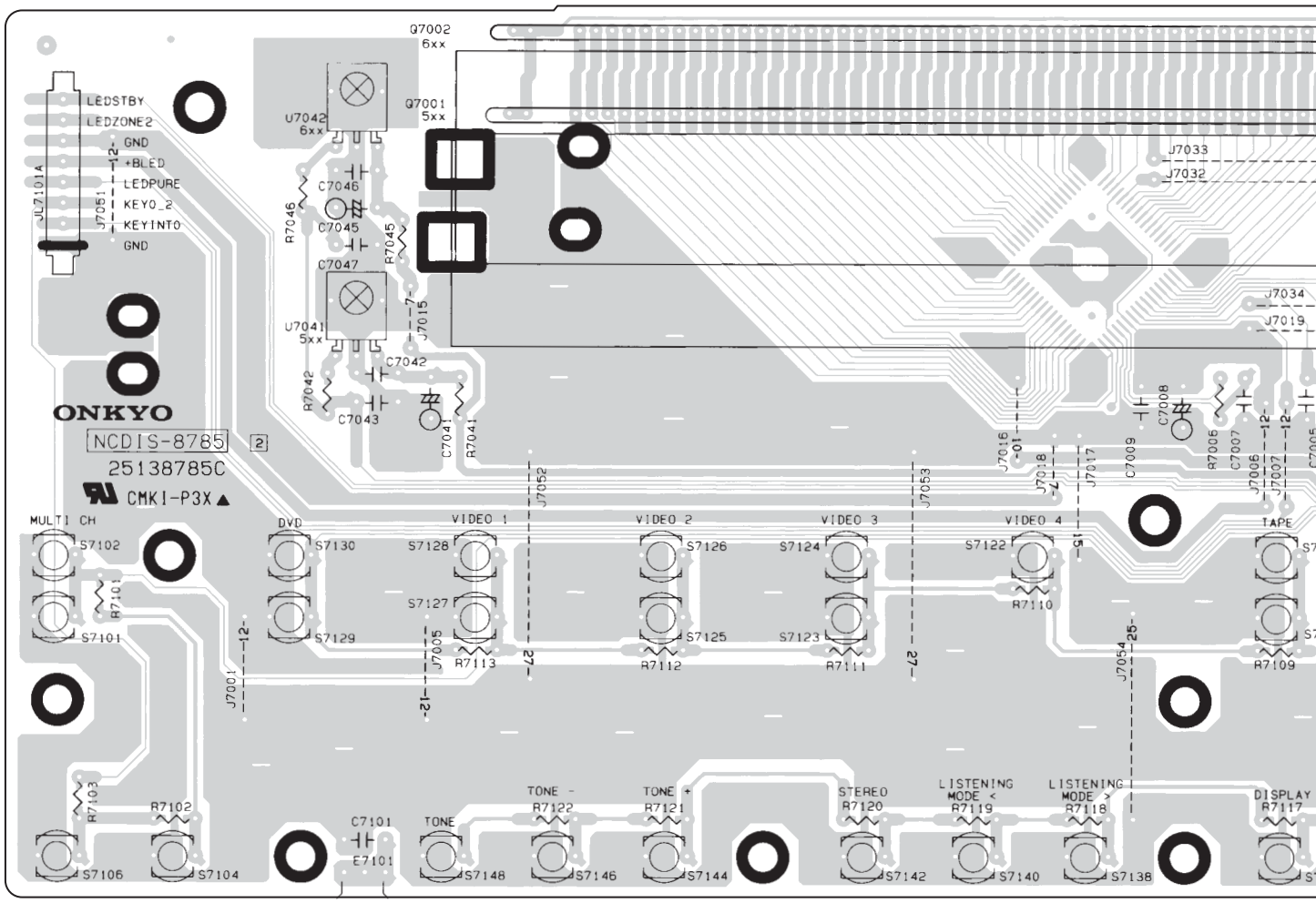
A B C D

PRINTED CIRCUIT BOARD VIEWS-1

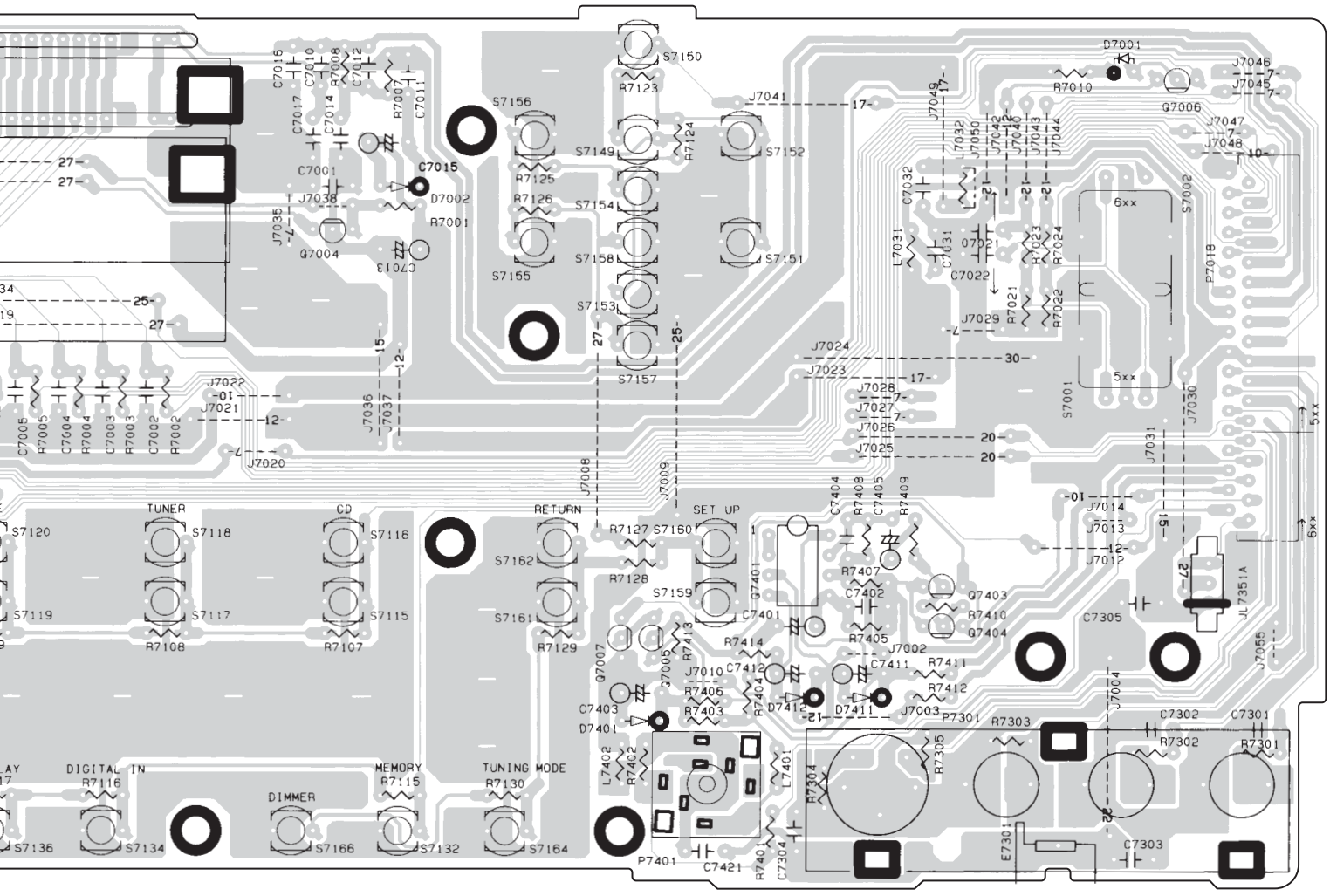
U01 DISPLAY PC BOARD (NADIS-8785)

Component side

1 2 3 4 5



E F G H


TUNER
CD
RETURN
SET UP
DIGITAL IN
DIMMER
MEMORY
TUNING MODE
S7120
S7118
S7116
S7119
S7117
S7115
S7162
S7161
S7159
S7160
S7150
S7156
S7149
S7152
S7154
S7158
S7151
S7155
S7153
S7157
S7136
S7134
S7166
S7132
S7164
R7108
R7107
R7129
R7128
R7127
R7123
R7124
R7125
R7126
R7116
R7115
R7130
C7015
D7002
R7001
C7001
J7038
G7004
C7013
D7001
R7010
G7006
J7046
J7045
J7047
J7048
J7049
J7032
J7050
J7042
J7040
J7043
J7044
C7032
L7031
C7031
Q7021
R7023
R7024
C7022
R7021
R7022
J7029
S7002
P7018
6xx
5xx
S7001
J7030
J7031
J7024
J7023
J7028
J7027
J7026
J7025
J7022
J7021
J7020
J7036
J7037
J7008
J7009
J7014
J7013
J7012
JL7351A
C7305
J7065
C7404
R7408
C7405
R7409
R7407
C7402
Q7403
R7410
Q7404
R7405
J7002
C7411
R7411
R7412
J7003
P7301
R7303
C7302
C7301
R7302
R7301
J7004
R7305
R7304
E7301
C7303
C7401
Q7401
R7414
C7412
J7010
R7406
R7404
D7412
D7411
R7403
C7403
D7401
R7413
Q7007
Q7005
L7402
R7402
L7401
R7401
C7304
P7401
C7421
C7005
R7005
C7604
R7004
C7003
R7003
C7002
R7002

A B C D

PRINTED CIRCUIT BOARD VIEWS-2

U01 DISPLAY PC BOARD (NADIS-8785)

Soldering side

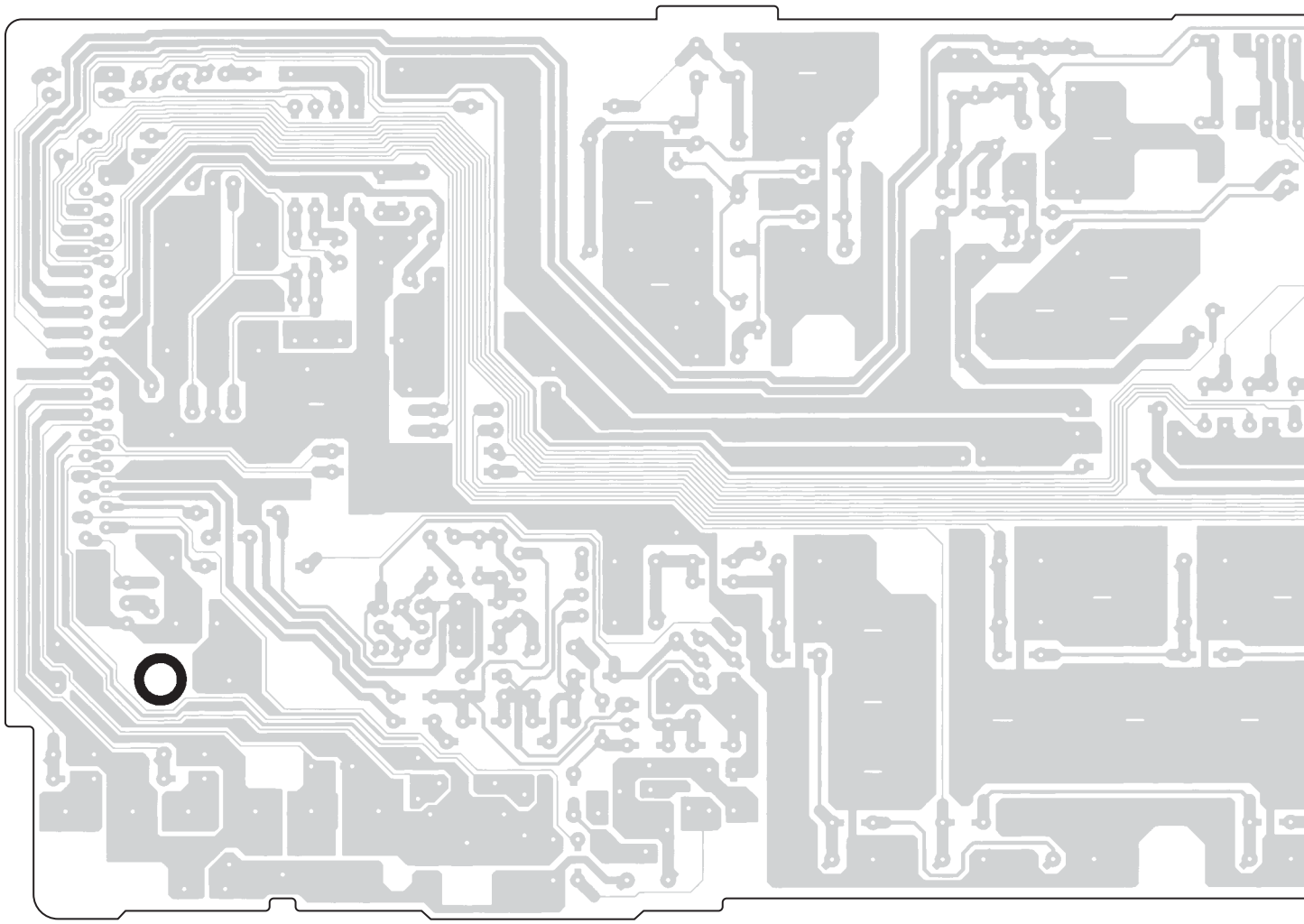
1

2

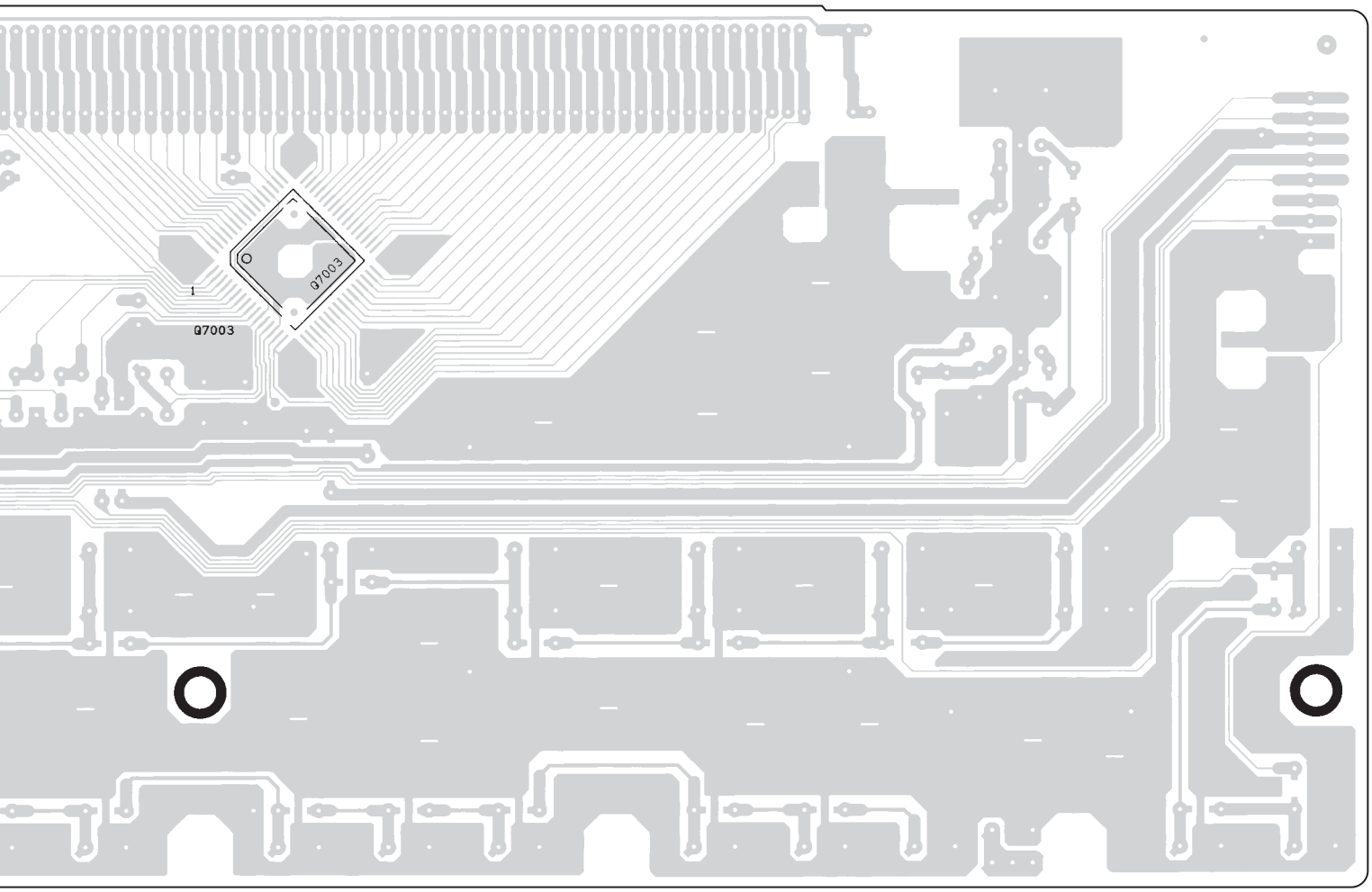
3

4

5



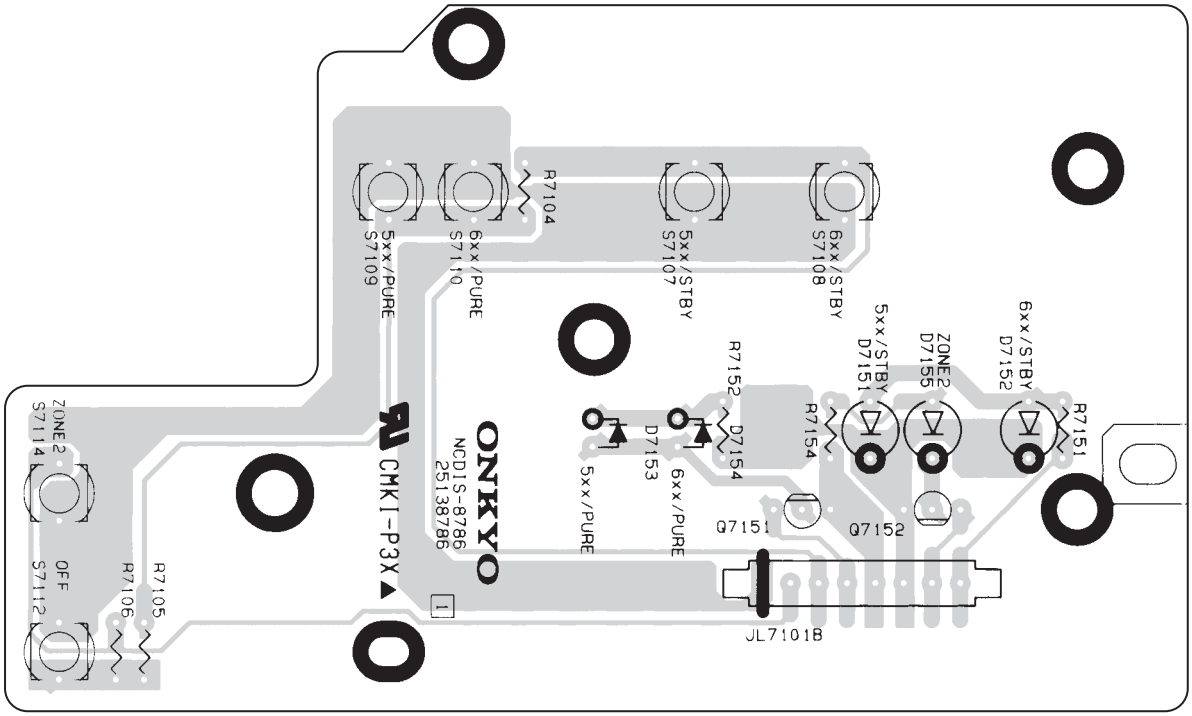
E F G H



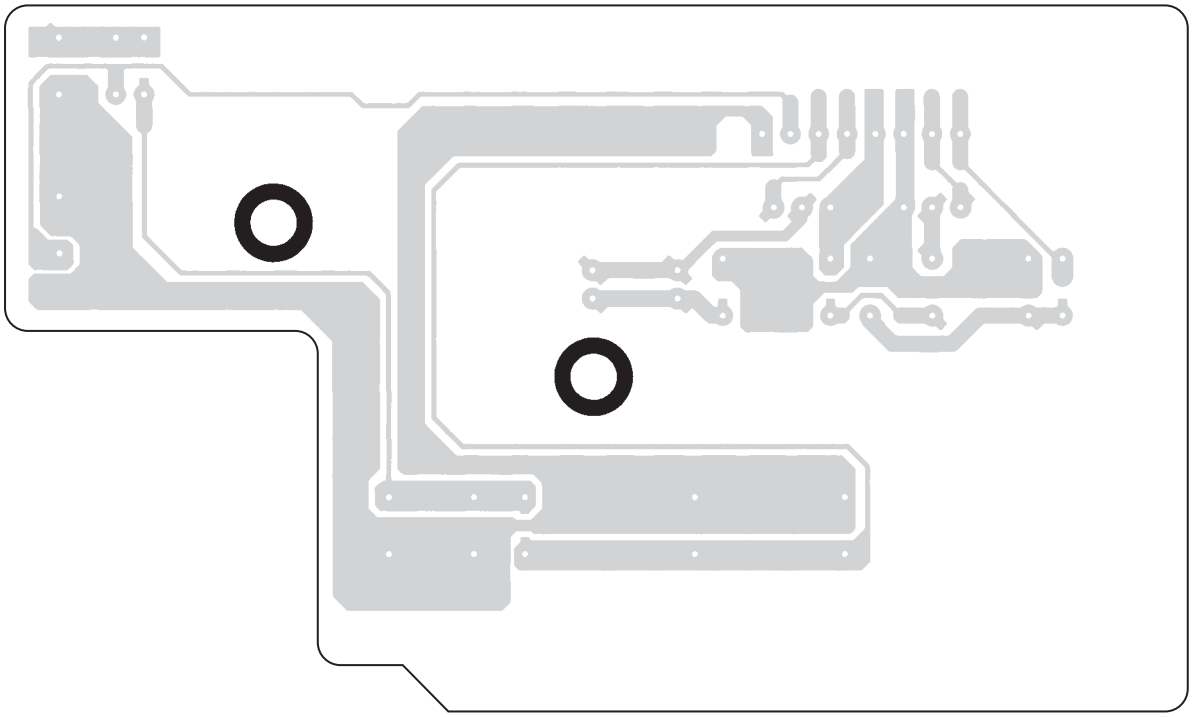
PRINTED CIRCUIT BOARD VIEWS-3

U02 SWITCH PC BOARD (NADIS-8786)

Component side



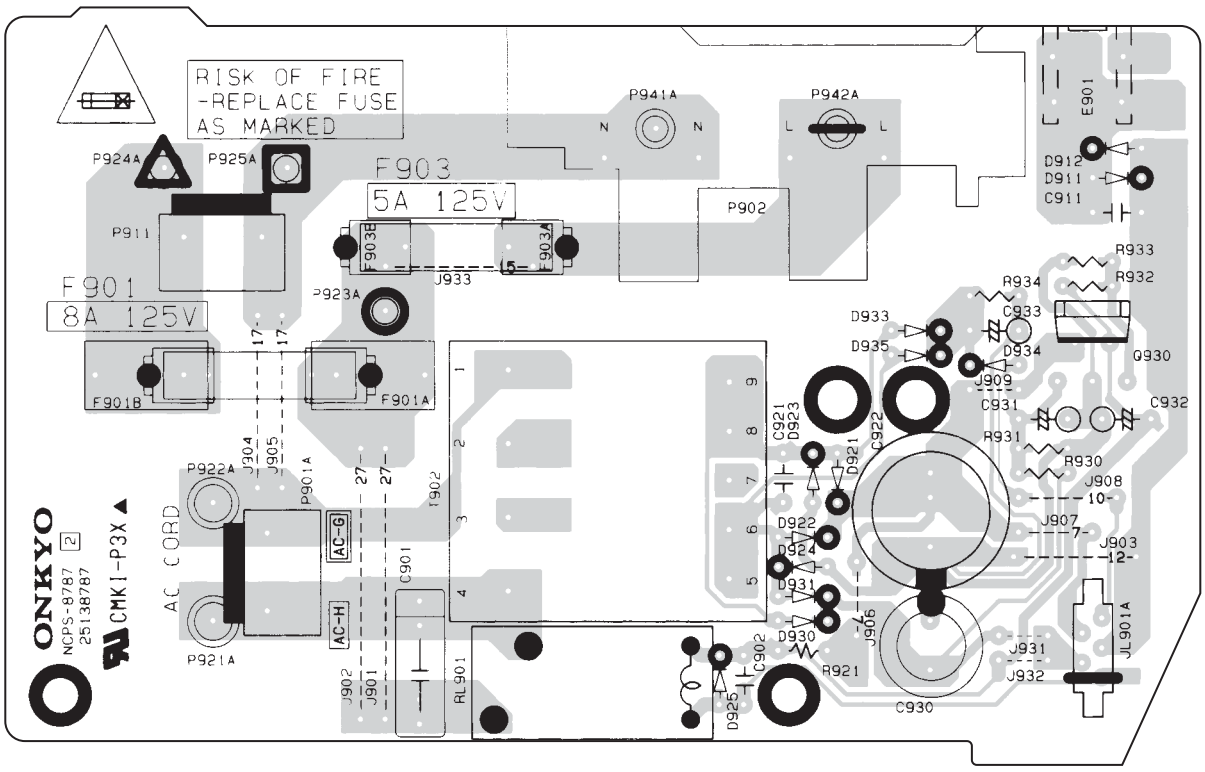
Soldering side



PRINTED CIRCUIT BOARD VIEWS-4

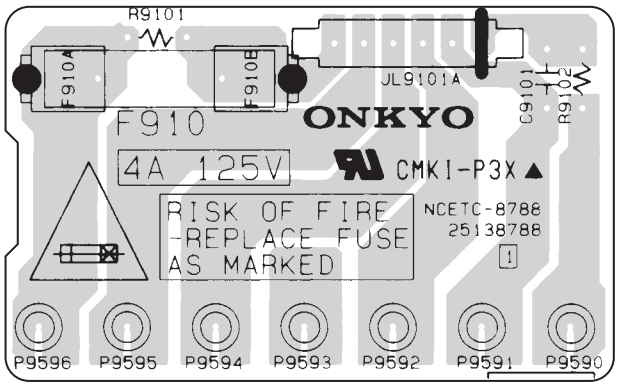
U03 POWER SUPPLY PC BOARD (NAPS-8787)

Component side

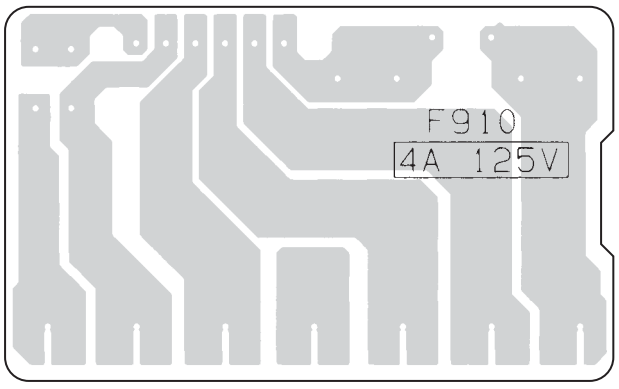


U04 SEC. TERMINAL-1 PC BOARD (NAETC-8788)

Component side



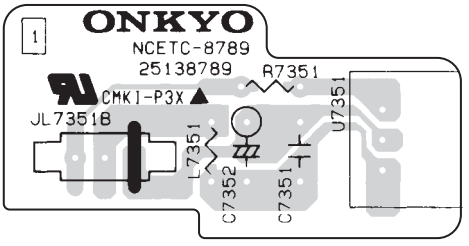
Soldering side



PRINTED CIRCUIT BOARD VIEWS-5

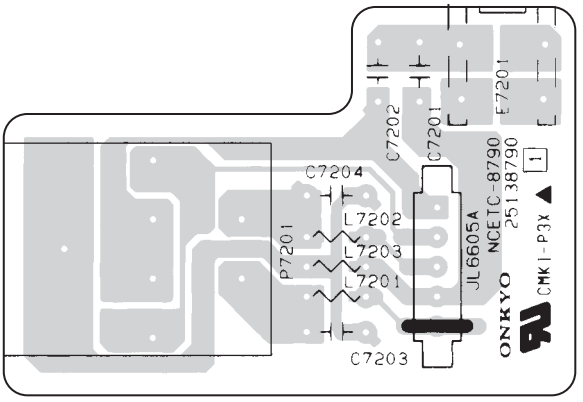
U05 FRONT OPT PC BOARD (NAETC-8789)

Component side



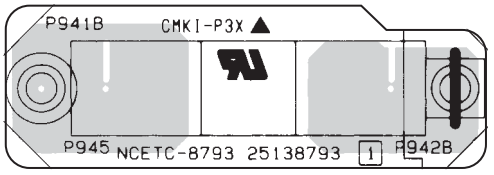
U06 HEADPHONE JACK PC BOARD (NAETC-8790)

Component side



U07 OUTLET TERMINAL PC BOARD (NAETC-8793)

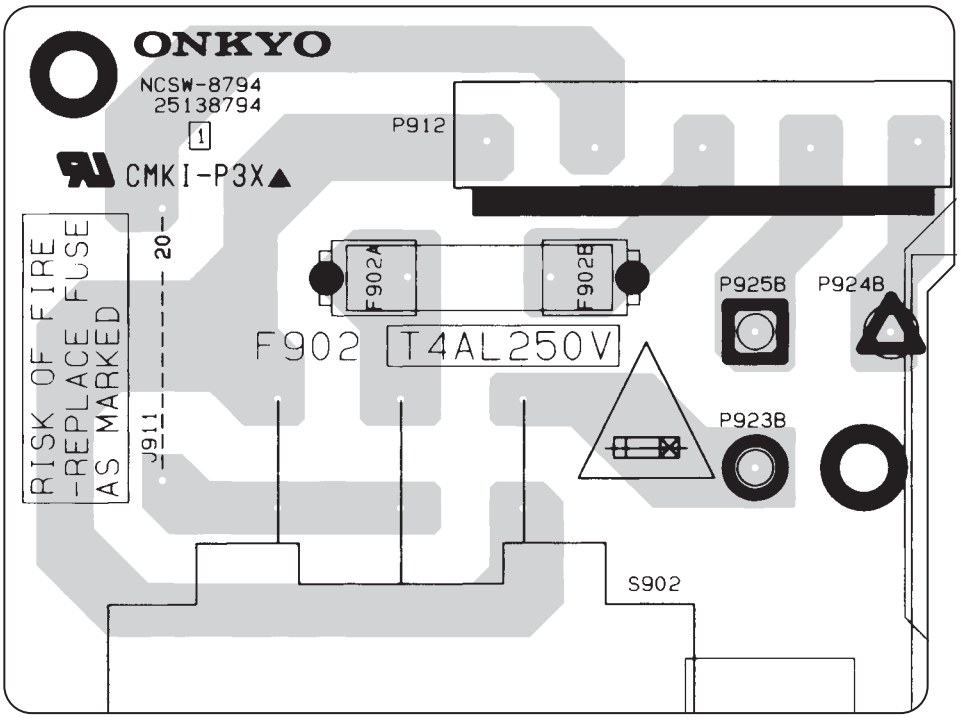
Component side



E F G H

U08 PRI. SWITCH PC BOARD (NASW-8794)

Component side



A B C D

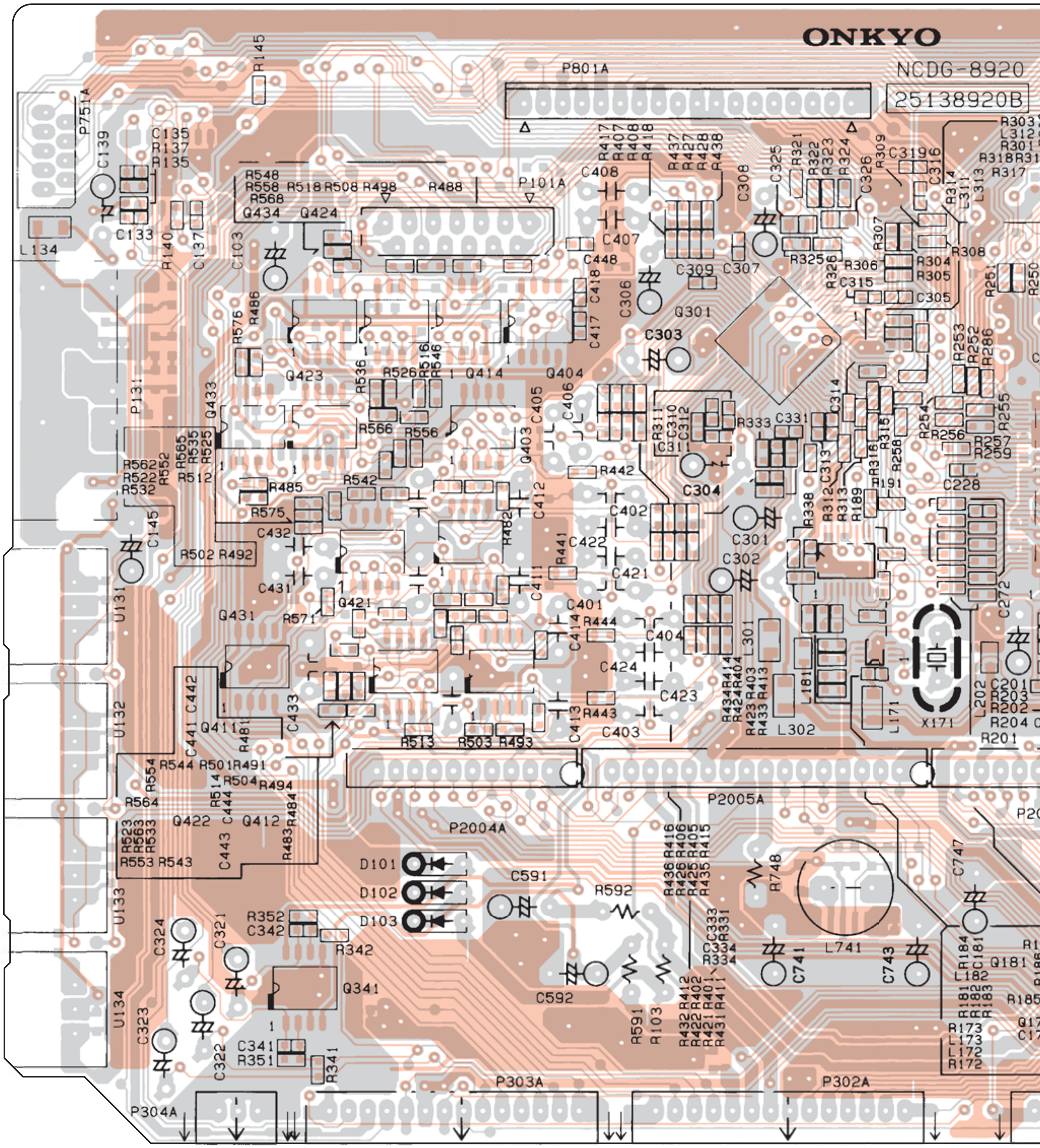
PRINTED CIRCUIT BOARD VIEWS-6

U12 DSP PC BOARD (NADG-8920)

1 **Component side**

2

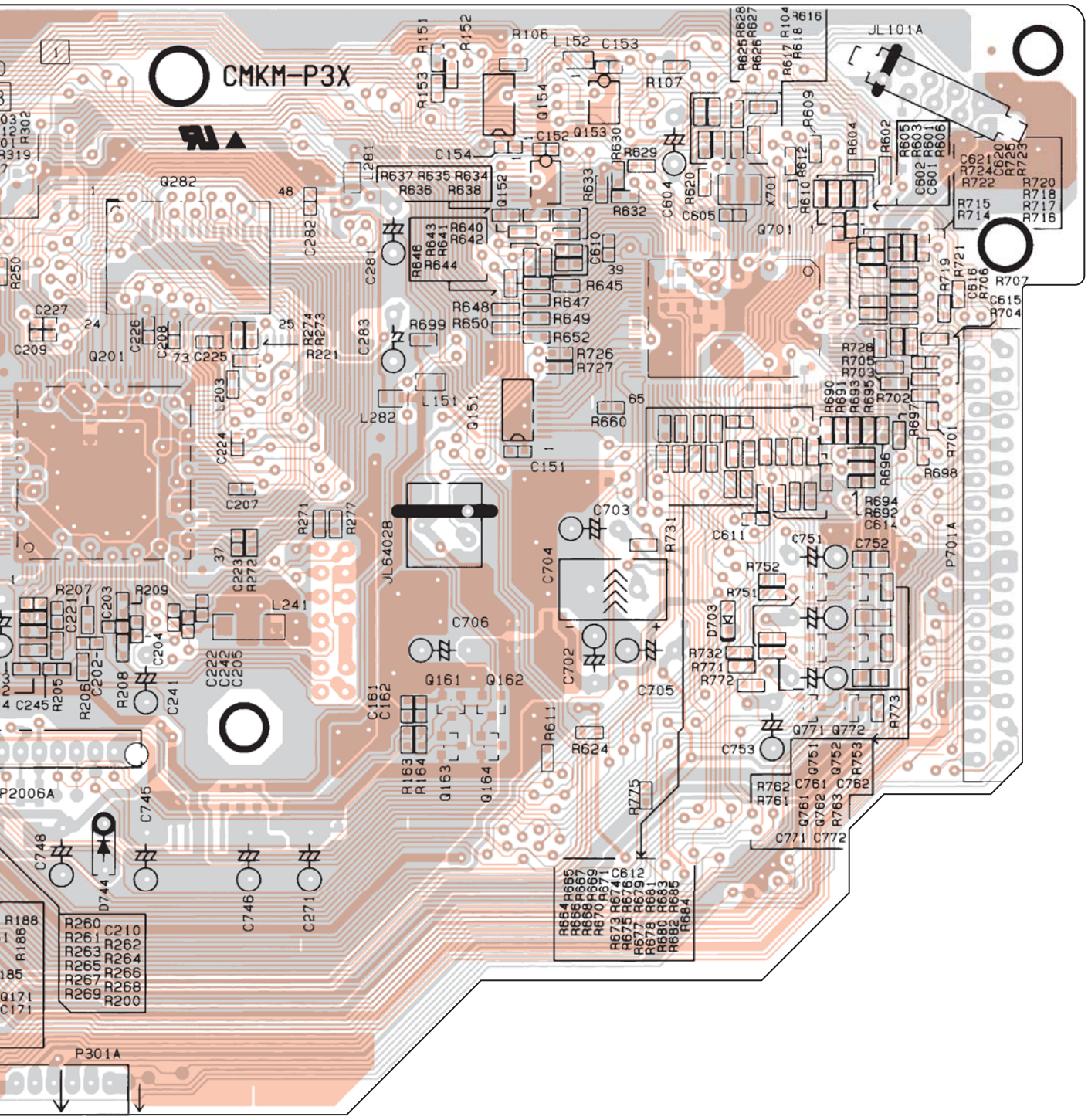
3



4

5

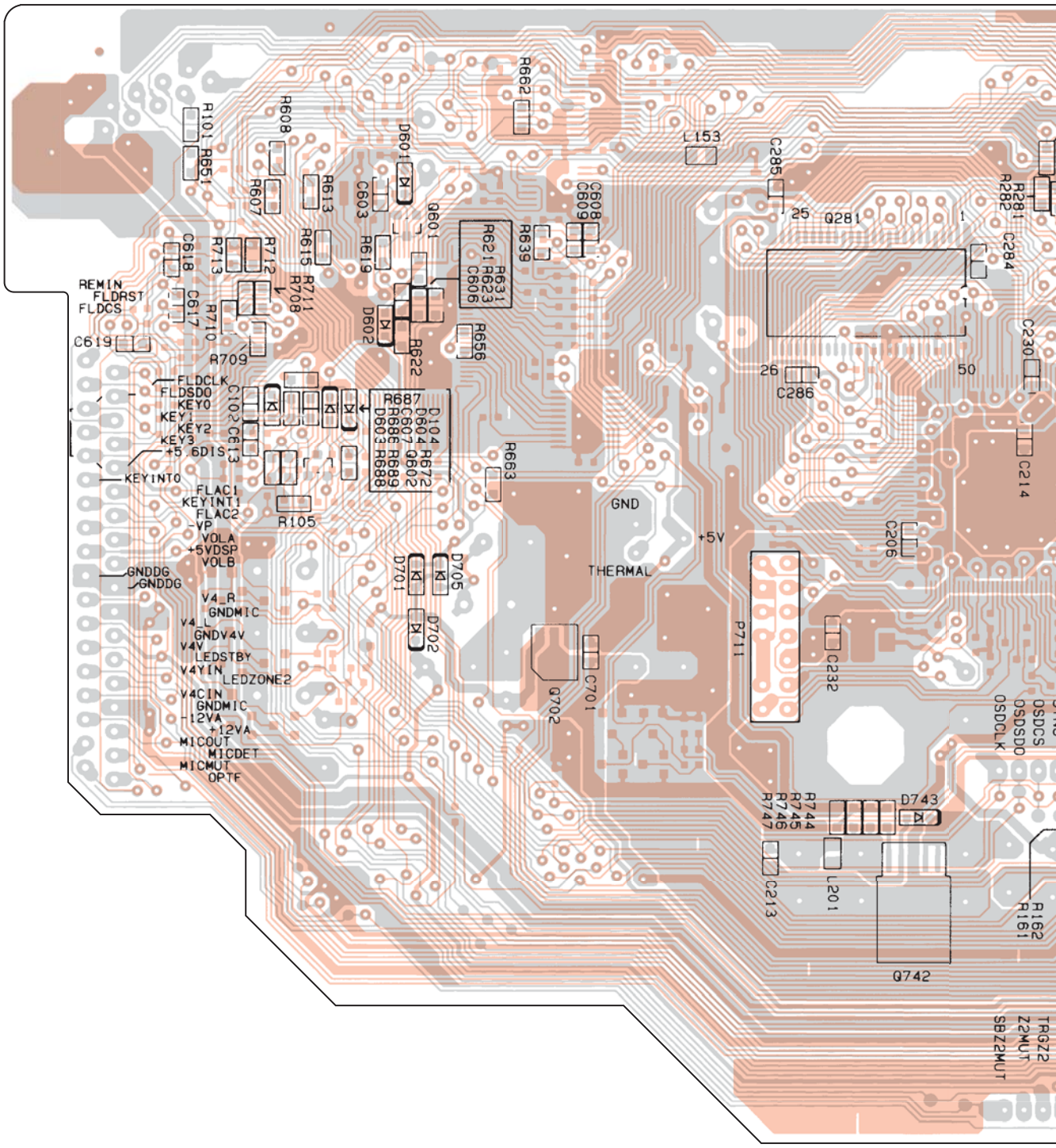
E F G H


CMKM-P3X
JL101A
Q282
Q201
Q701
JL6402B
P2006A
P301A
P701A
Q161
Q162
Q163
Q164
Q151
Q152
Q153
Q154
L151
L152
L153
L241
L281
L282
C151
C152
C153
C154
C703
C704
C705
C706
R106
R107
R660
R699
R731
R732
R771
R772
R775
D703
D744

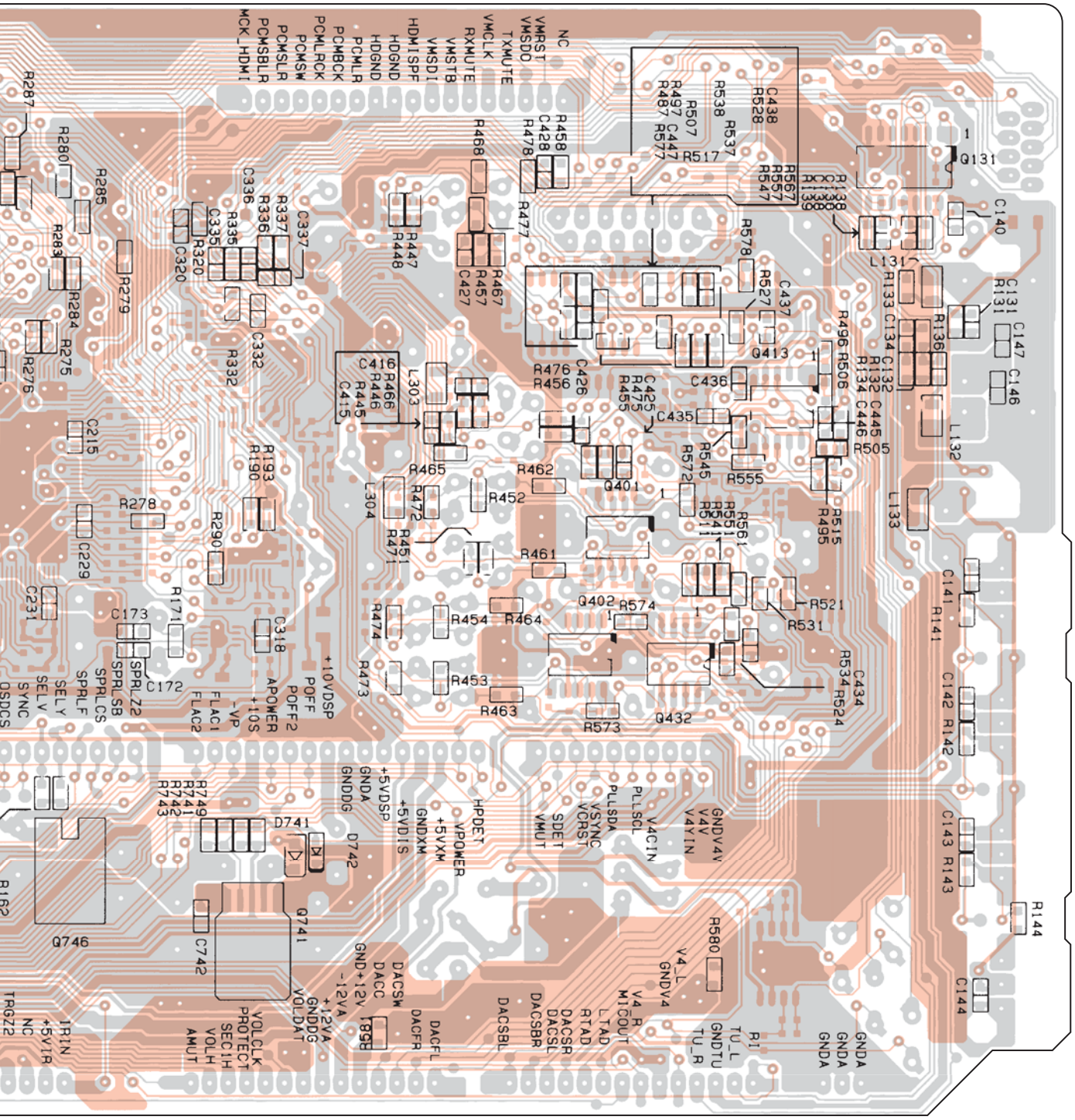
PRINTED CIRCUIT BOARD VIEWS-7

U12 DSP PC BOARD (NADG-8920)

Soldering side



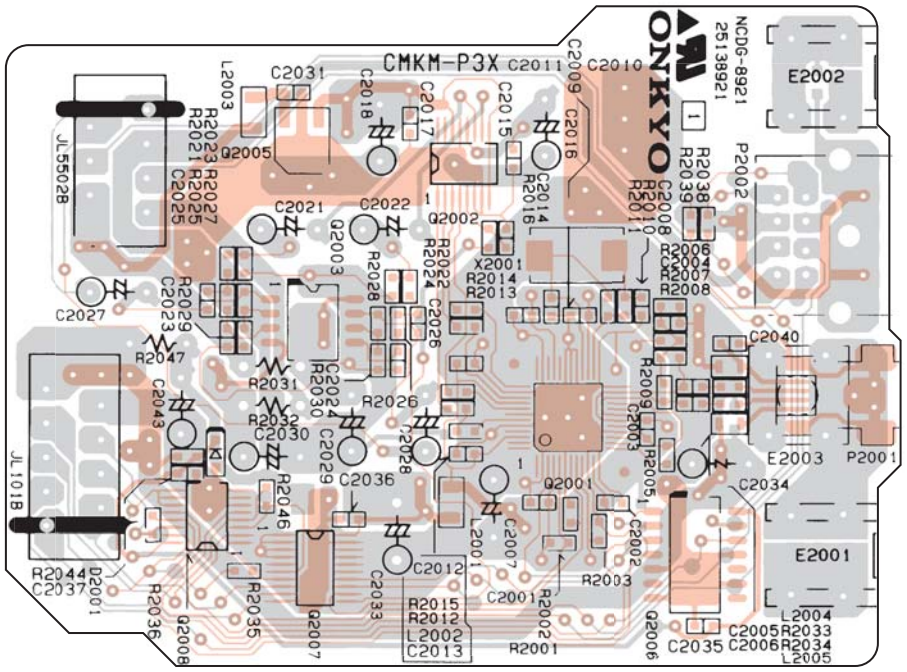
E F G H


Q131
L131
L132
L133
Q401
Q402
Q413
Q432
Q741
Q746
D741
D742
R517
R555
R573
R574
R580
C140
C141
C142
C143
C144
C146
C147
C320
C332
C337
C426
C435
C436
C437
C438
C742
R144
R279
R452
R454
R455
R456
R461
R462
R463
R464
R465
R466
R467
R468
R471
R472
R473
R474
R476
R477
R478
R495
R496
R505
R506
R507
R515
R521
R527
R528
R531
R534
R537
R538
R545
R547
R557
R561
R567
R572
R577
R578
NC
VMRST
VMSDO
TXMUTE
VMCLK
RXMUTE
VMSTB
VMSDI
HDMISPF
HDGND
HDGND
PCMLR
PCMBCK
PCMLRCK
PCMSW
PCMSLR
PCMSBLR
MCK_HDMI
+10VDSP
POFF
POFF2
APOWER
+10S
-VP
FLAC1
FLAC2
SELV
SELY
SPRLF
SPRLCS
SPRLSB
SPRLZ2
SELV
SYNC
OSDCS
+5VDSP
GNDA
GNDDG
HPDET
VPOWER
+5VXM
GNDXM
+5VDIS
PLLSDA
PLLSCL
VSYNC
VCRST
SDET
VMUT
V4CIN
GNDV4V
V4V
V4VIN
V4_L
GNDV4
V4_R
MICOUT
LTAD
RTAD
DACSR
DACSL
DACSBR
DACSBL
DACSW
DACC
DACFL
DACFR
GND+12V
-12VA
+12VA
GNDDG
VOLDAT
VOLCLK
PROTECT
SEC1H
VOLH
AMUT
GNDA
GNDA
GNDA
TU_L
GNDTU
TU_R
RI
IRIN
+5VIR
NC
TRGZ2

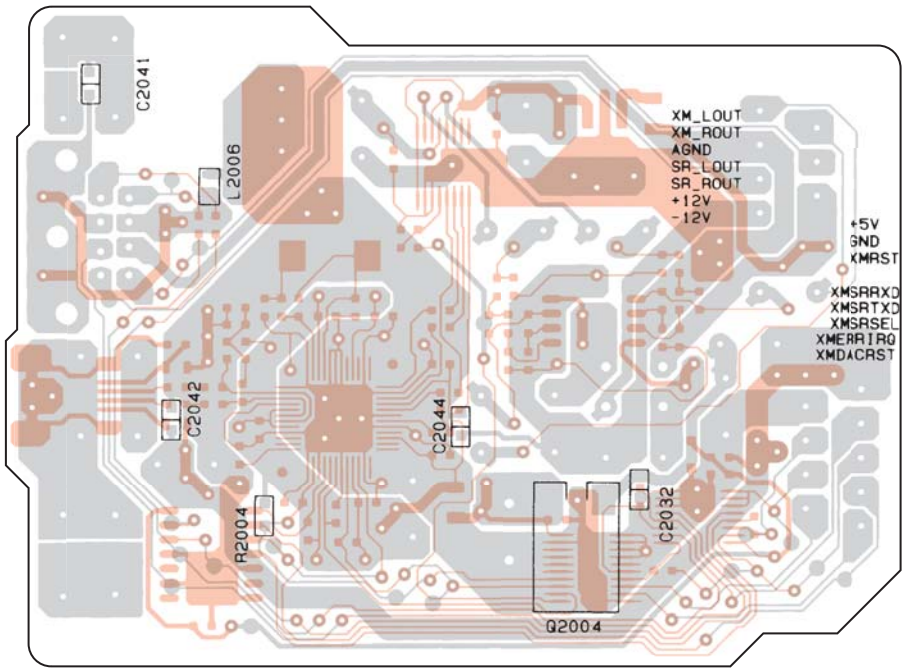
PRINTED CIRCUIT BOARD VIEWS-8

U13 XM PC BOARD (NADG-8921)

Component side



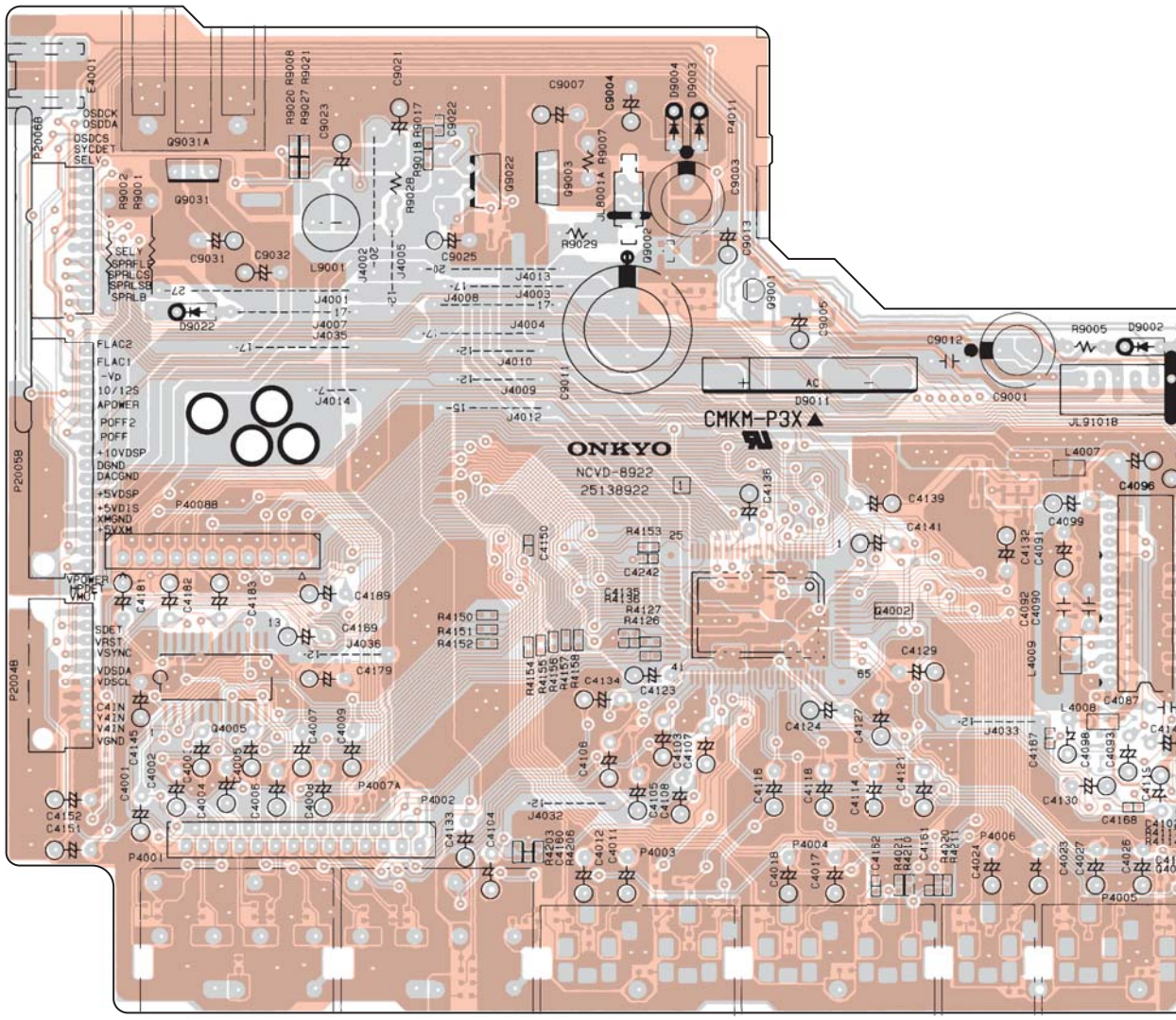
Soldering side



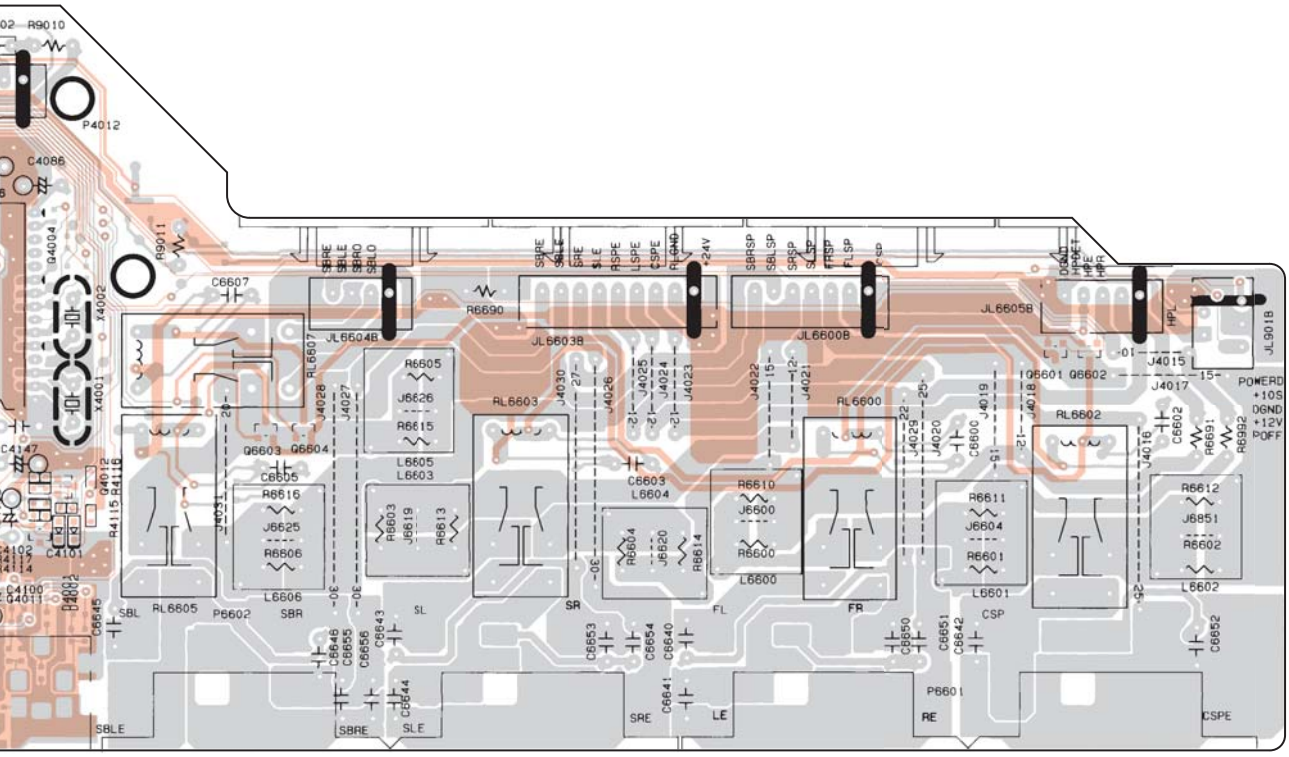
PRINTED CIRCUIT BOARD VIEWS-9

U14 VIDEO PC BOARD (NAVD-8922)

Component side



E F G H


R9010
P4012
C4086
R9011
C6607
R6690
JL6604B
JL6603B
JL6600B
JL6605B
JL901B
RL6607
RL6603
RL6600
RL6602
RL6605
R6605
J6626
R6615
L6605
L6603
R6616
J6625
R6606
L6606
R6603
J6619
R6613
C6603
L6604
R6604
J6620
R6614
R6610
J6600
R6600
L6600
R6611
J6604
R6601
L6601
R6612
J6851
R6602
L6602
C6602
R6691
R6992
J4015
J4017
Q6601 Q6602
Q6603 Q6604
C6605
P6602
P6601
SBL
SL
SR
FL
FR
CSP
SBLE
SBRE
SLE
SRE
LE
RE
CSPE
POWERD
+10S
DGND
+12V
POFF

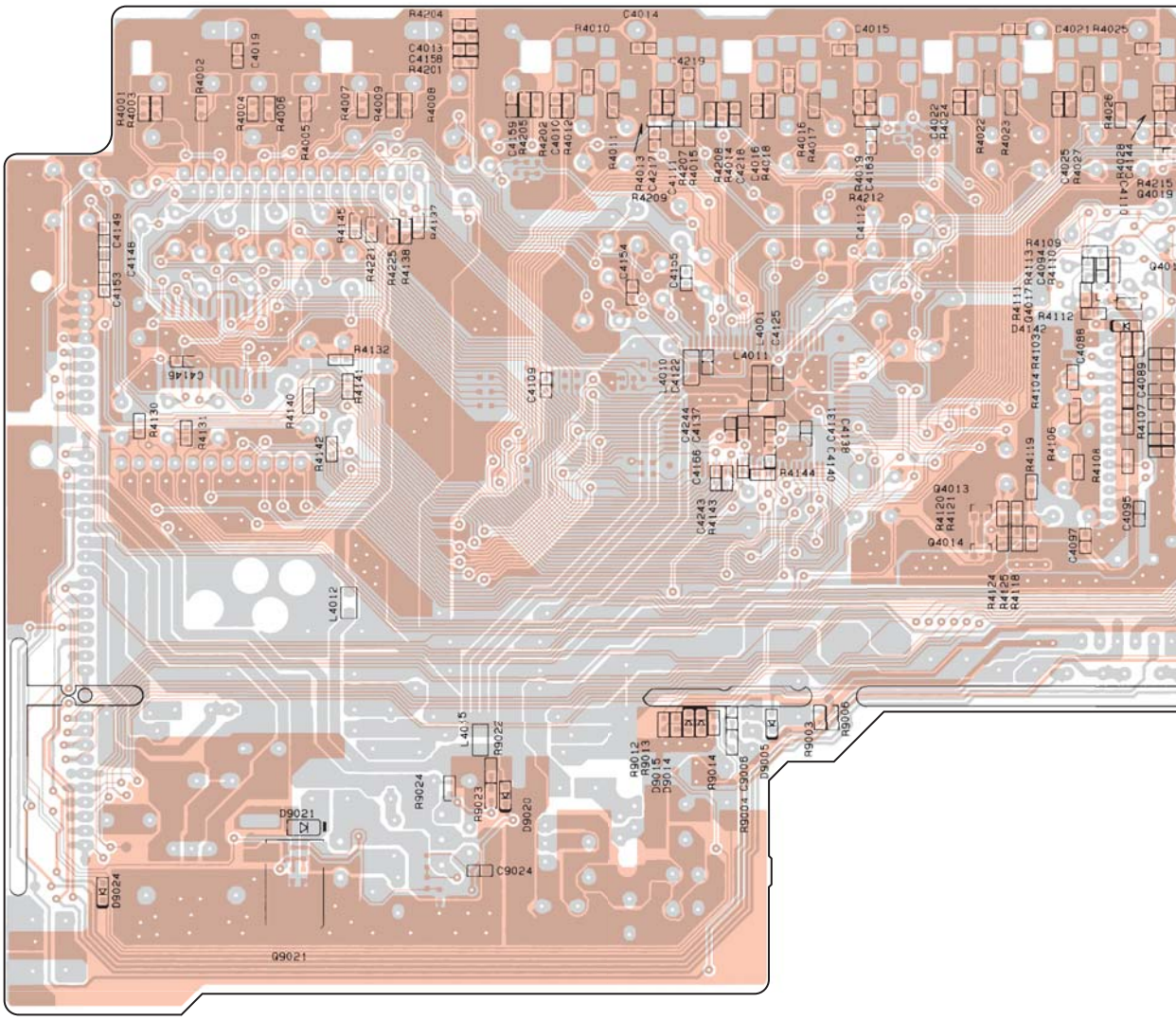
A B C D

1 2 3 4 5

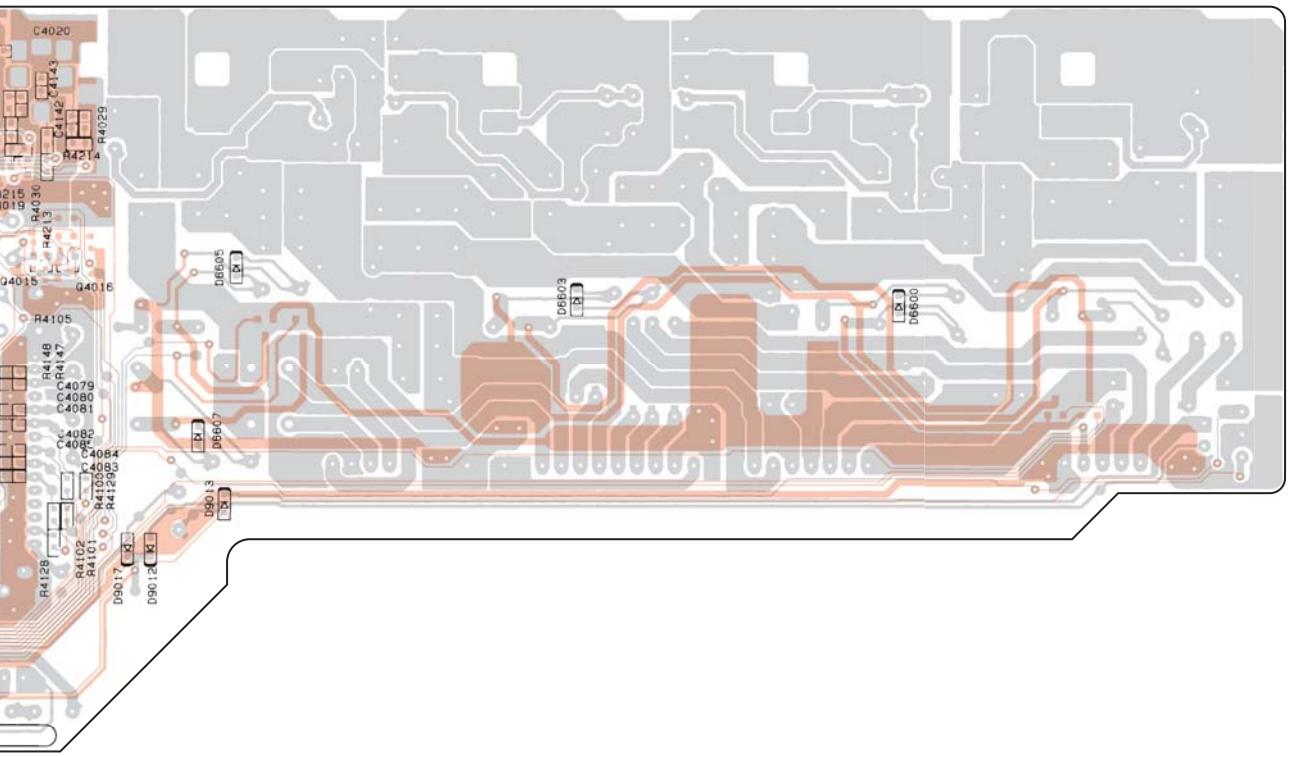
PRINTED CIRCUIT BOARD VIEWS-10

U14 VIDEO PC BOARD (NAVD-8922)

Soldering side



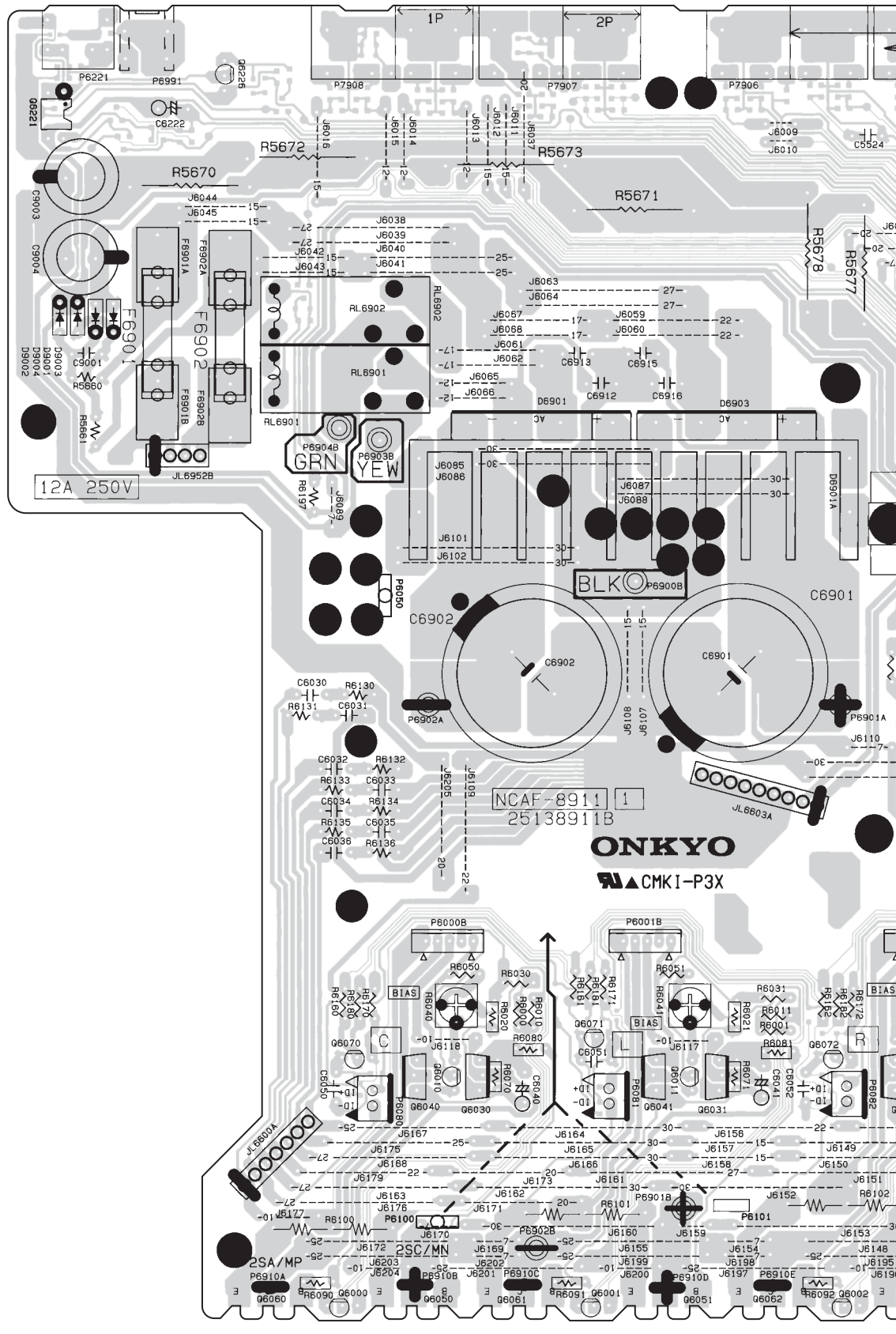
E F G H


C4020
C4143
C4142
R4029
R4214
R4030
R4213
Q4015
Q4016
R4105
R4148
R4147
C4079
C4080
C4081
C4082
C4084
C4083
R4103
R4129
R4102
R4101
R4128
D9017
D9012
D9013
D6605
D6607
D6603
D6600

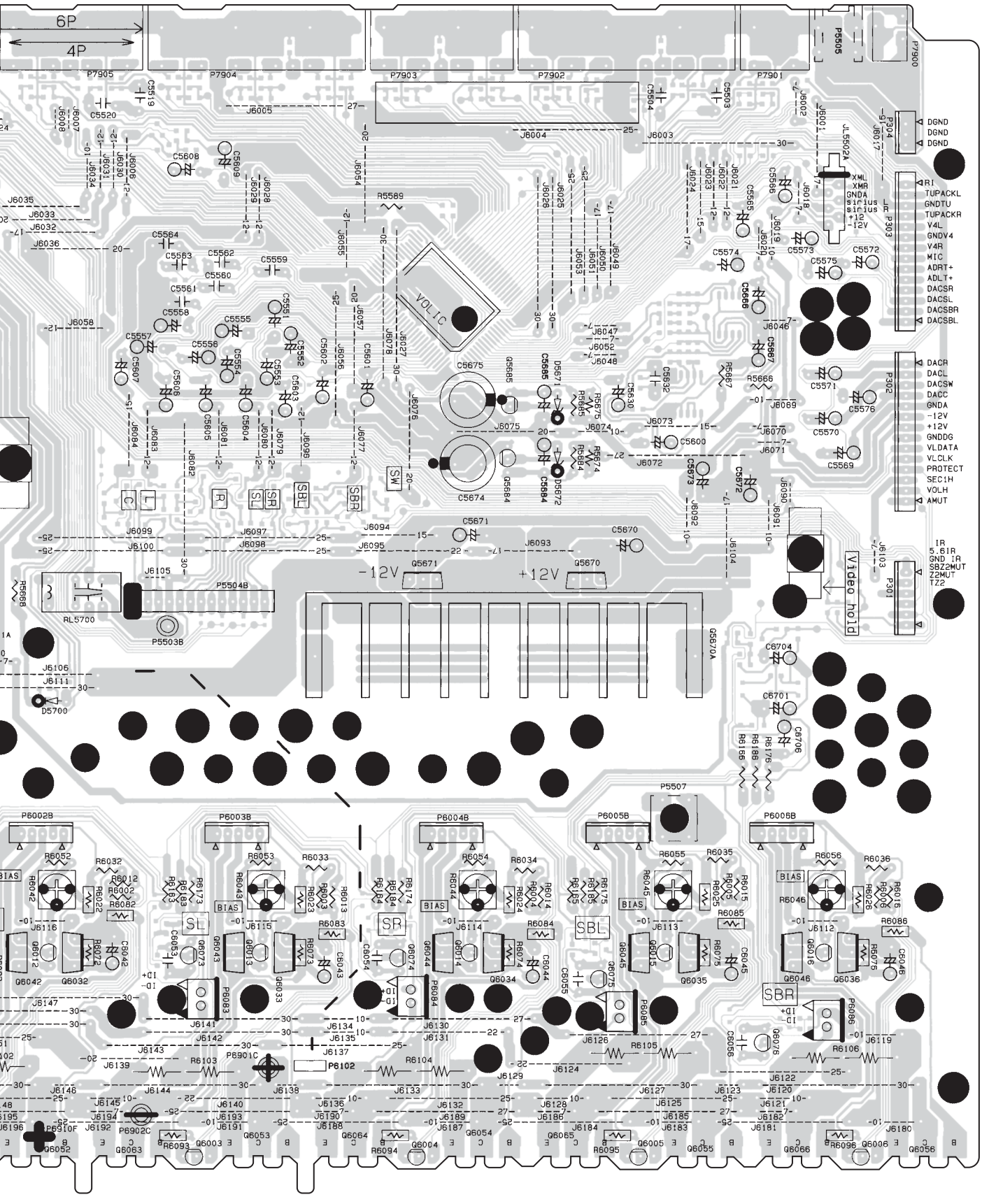
PRINTED CIRCUIT BOARD VIEWS-11

U15 AMPLIFIER PC BOARD (NAAF-8911)

Component side



E F G H


6P
4P
P7905
P7904
P7903
P7902
P7901
P5505
P7900
P304
DGND
DGND
DGND
P303
RI
TUPACKL
GNDTU
TUPACKR
V4L
GNDV4
V4R
MIC
ADRT+
ADLT+
DACSR
DACSL
DACSBR
DACSBL
P302
DACR
DACL
DACSW
DACC
GNDA
-12V
+12V
GNDDG
VLDATA
VLCLK
PROTECT
SEC1H
VOLH
AMUT
P301
IR
5.6IR
GND IR
SBZ2MUT
Z2MUT
TZ2
VOLIC
SW
L
C
R
SL
SR
SBL
SBR
-12V
+12V
Video hold
P5504B
RL5700
P5503B
D5700
P5507
P6002B
P6003B
P6004B
P6005B
P6006B
P6083
P6084
P6085
P6086
P6102
P6901C
P6902C
P6910F

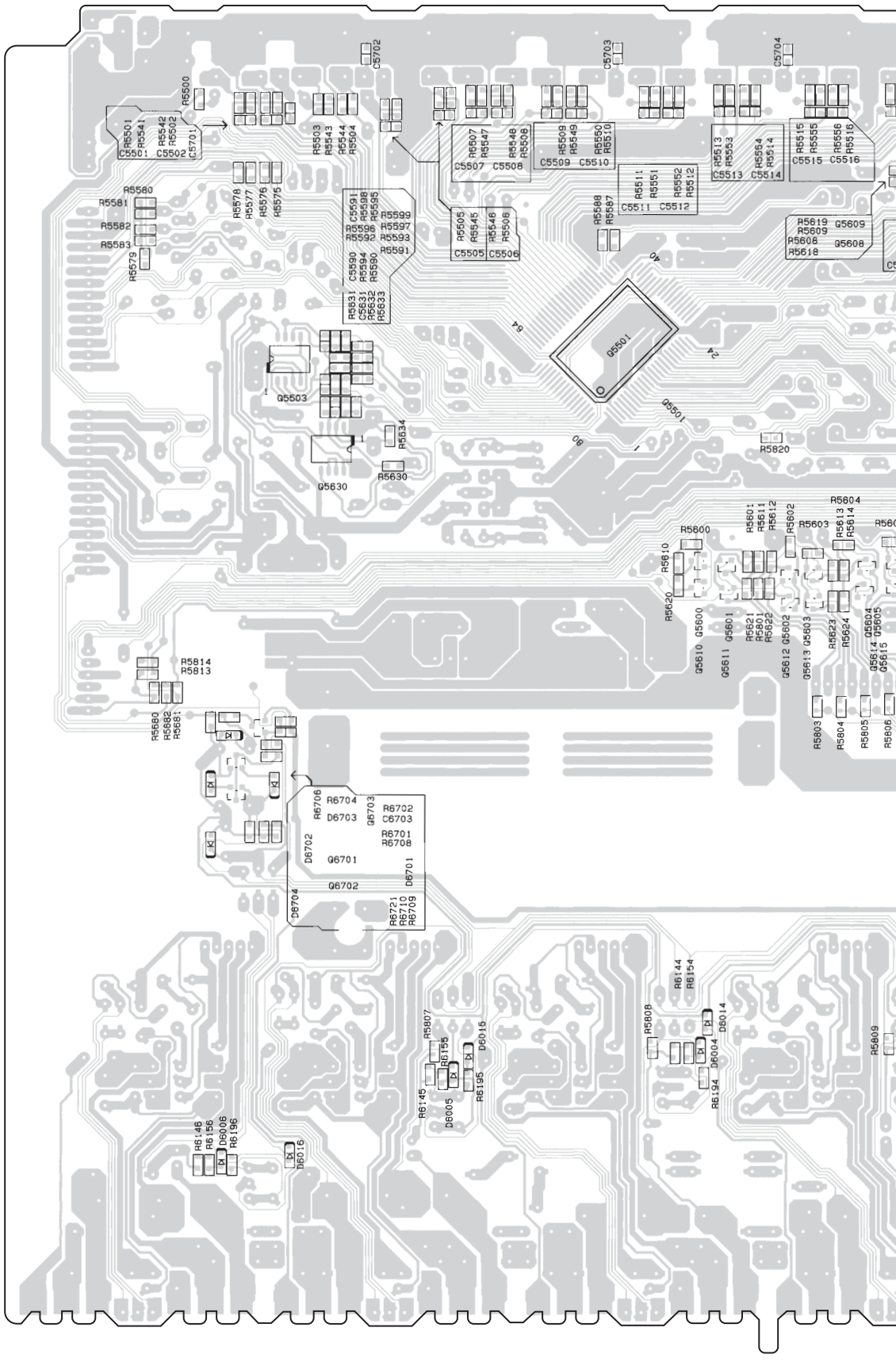
A B C D

1 2 3 4 5

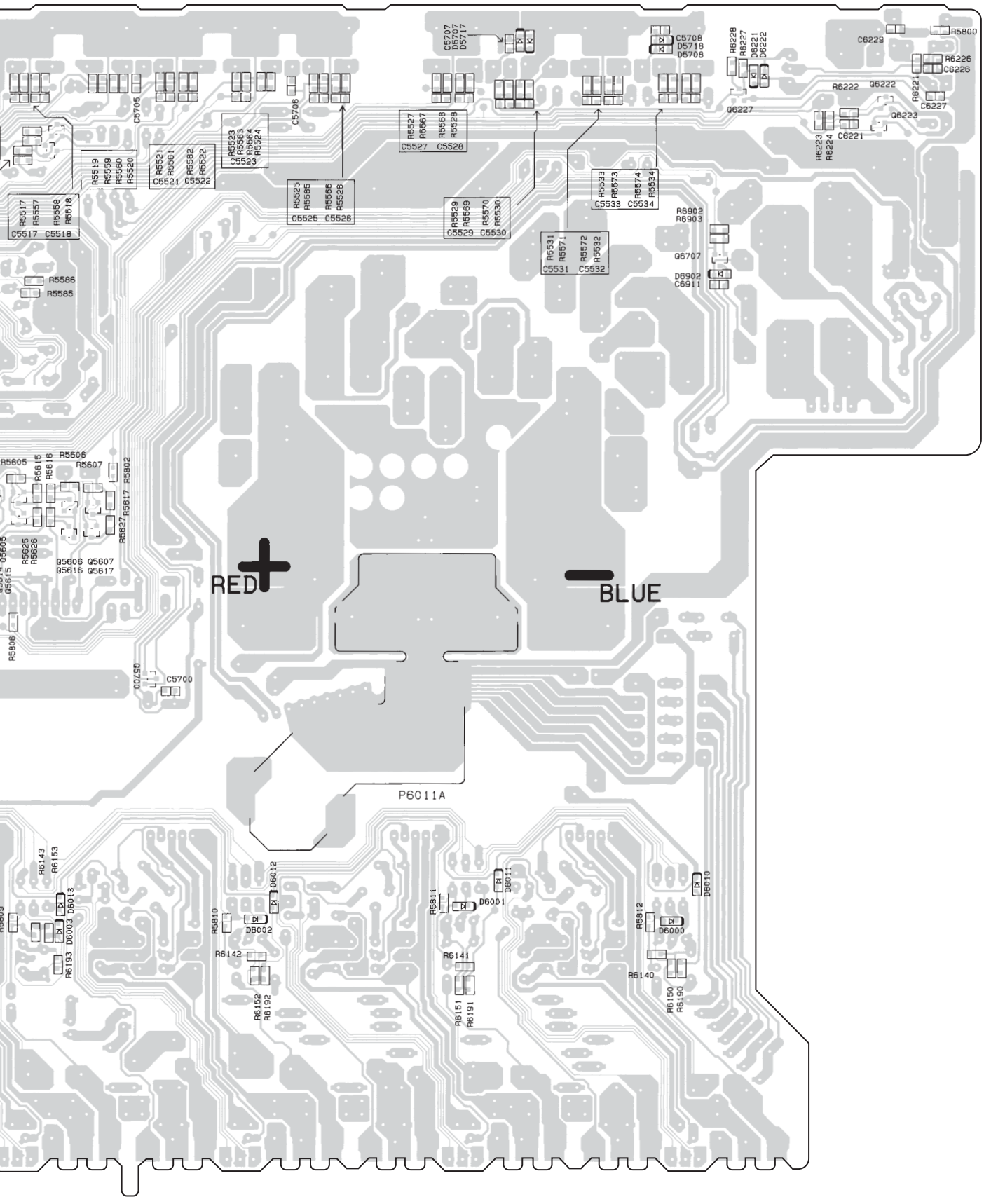
PRINTED CIRCUIT BOARD VIEWS-12

U15 AMPLIFIER PC BOARD (NAAF-8911)

Soldering side



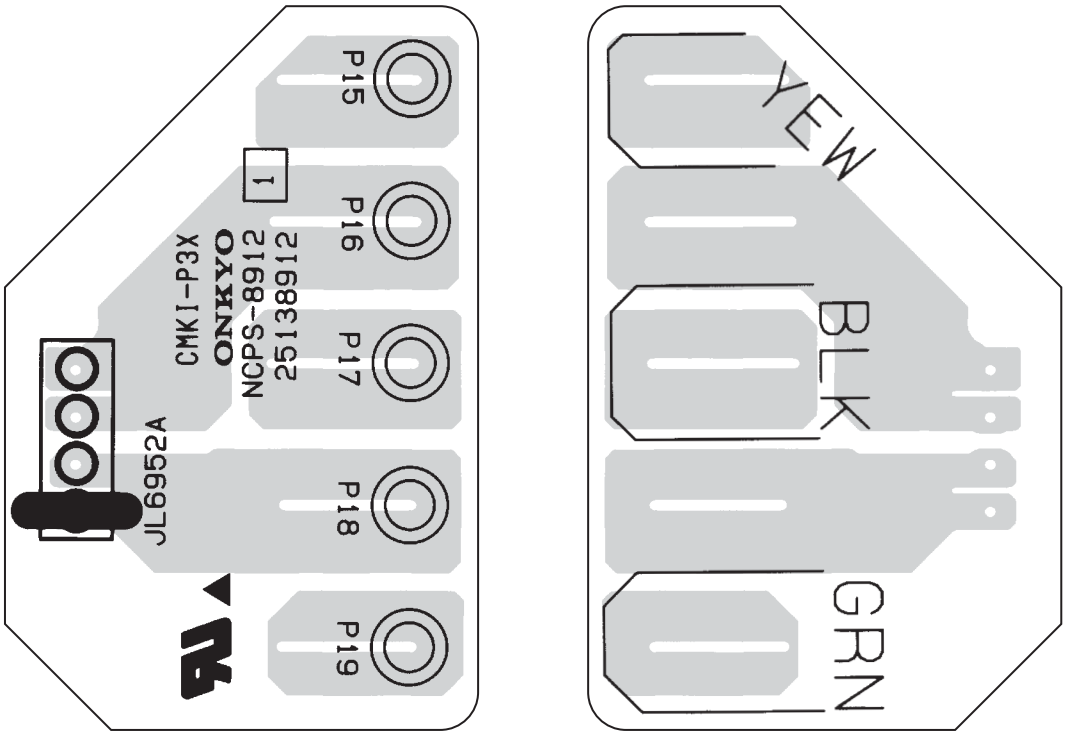
E F G H



PRINTED CIRCUIT BOARD VIEWS-13

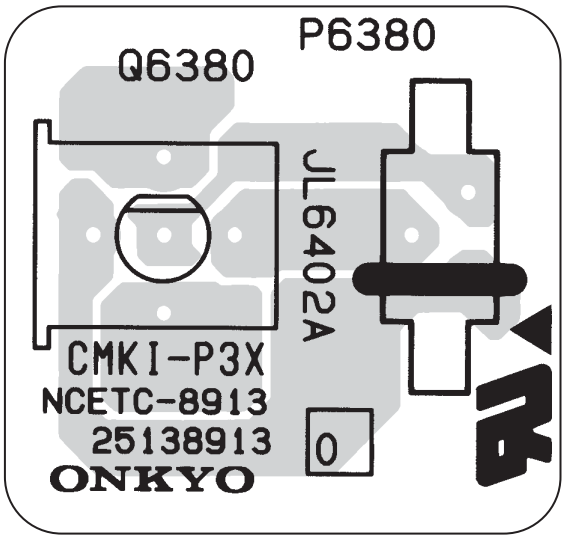
U16 SEC. TERMINAL-2 PC BOARD (NAPS-8912)

Component side **Soldering side**



U17 THERMAL SENSOR PC BOARD (NAETC-8913)

Component side

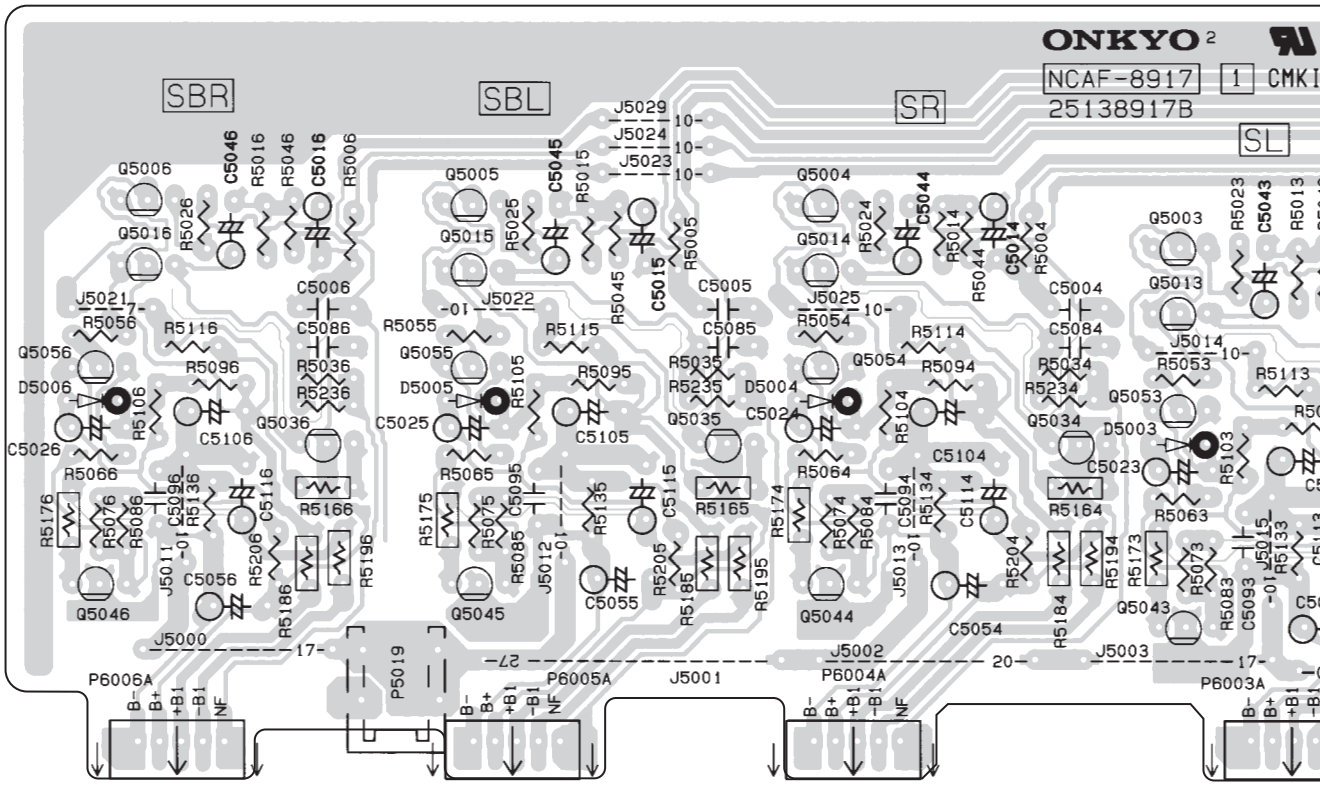


A B C D

PRINTED CIRCUIT BOARD VIEWS-14

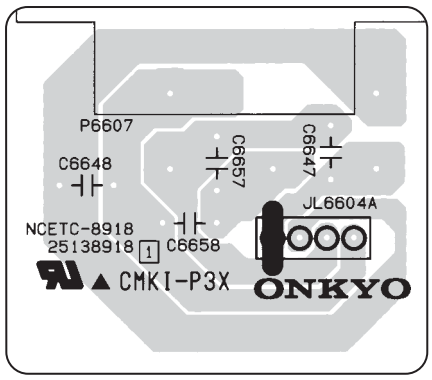
U19 DRIVER AMPLIFIER PC BOARD (NAAF-8917)

Component side

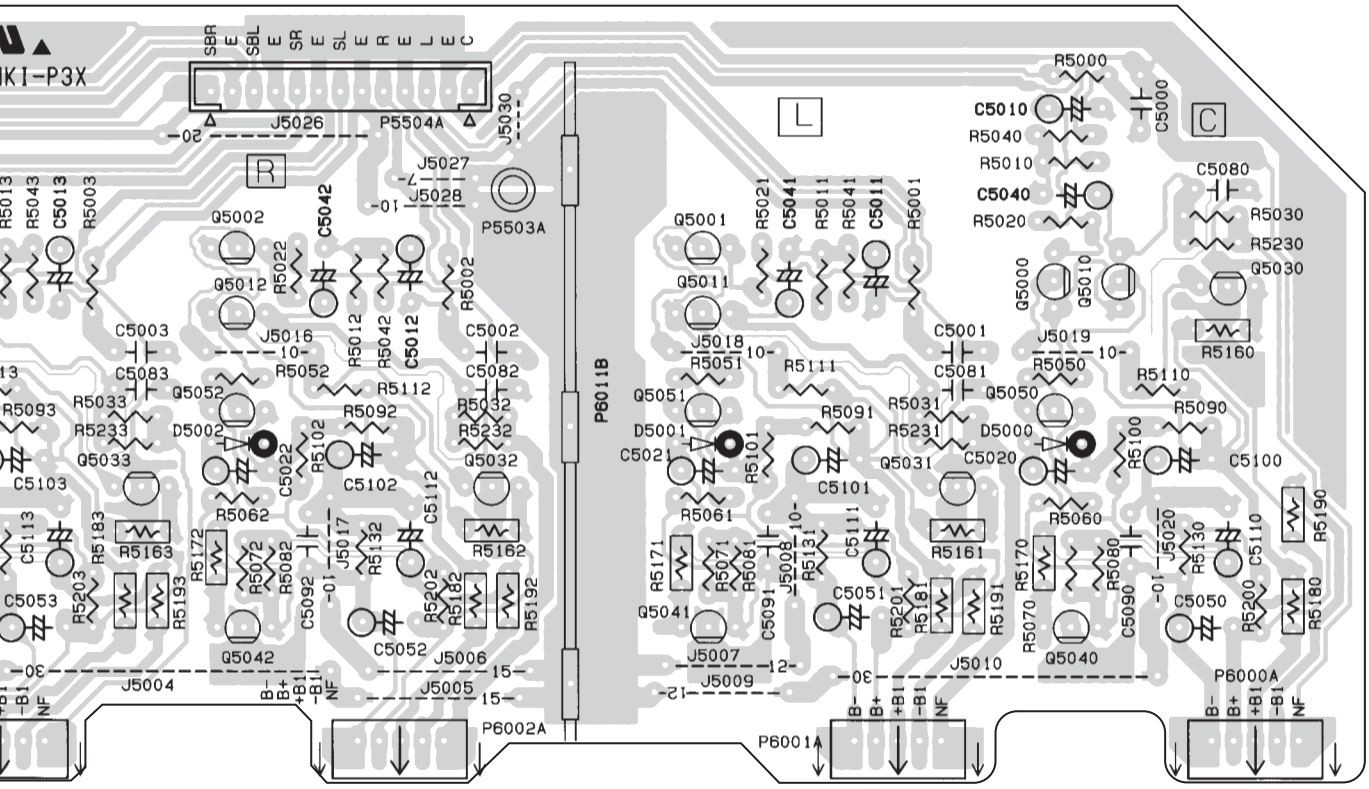


U20 SPEAKER TERMINAL PC BOARD (NAETC-8918)

Component side



E F G H


MKI-P3X
SBR
SBL
SR
SL
RELEC
J5026
P5504A
J5030
P5503A
J5027
J5028
P6011B
P6002A
P6001A
P6000A
J5004
J5005
J5006
J5007
J5009
J5010
J5016
J5017
J5018
J5019
J5020
R
L
C
B-
B+
+B1
-B1
NF

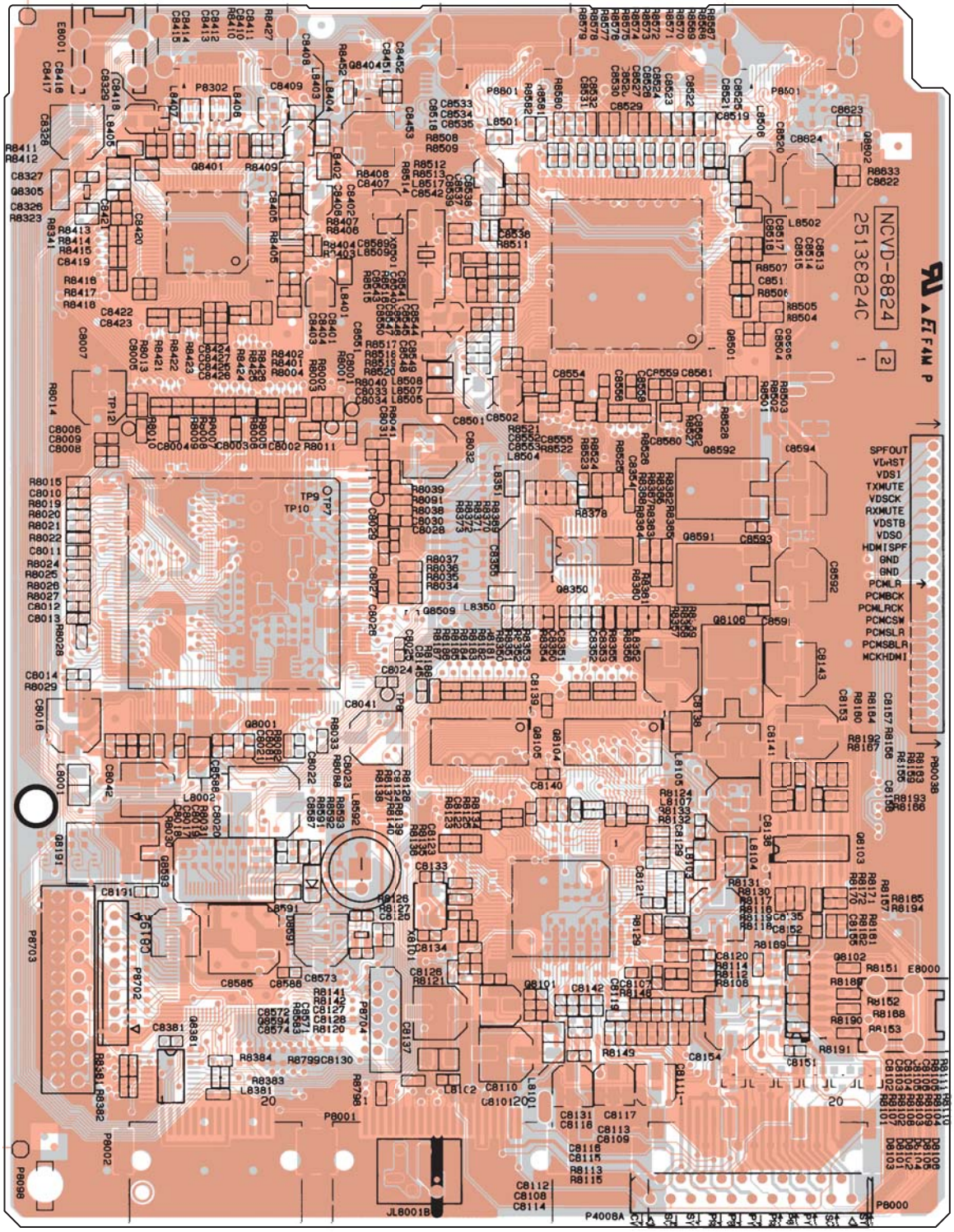
A B C D

PRINTED CIRCUIT BOARD VIEWS-15

U21 HDMI PC SWITCH (NAVD-8824)

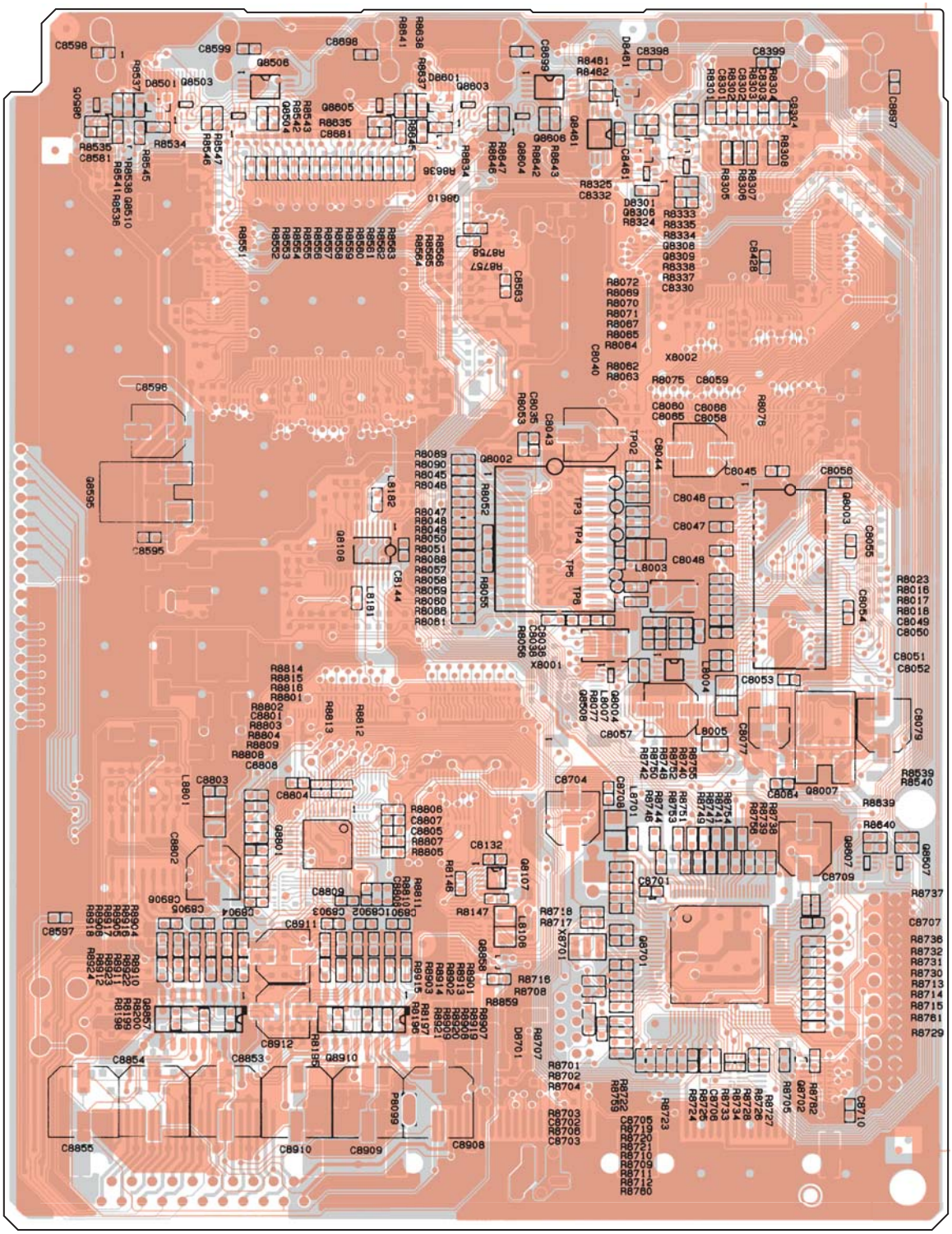
Component side

1 2 3 4 5



E F G H

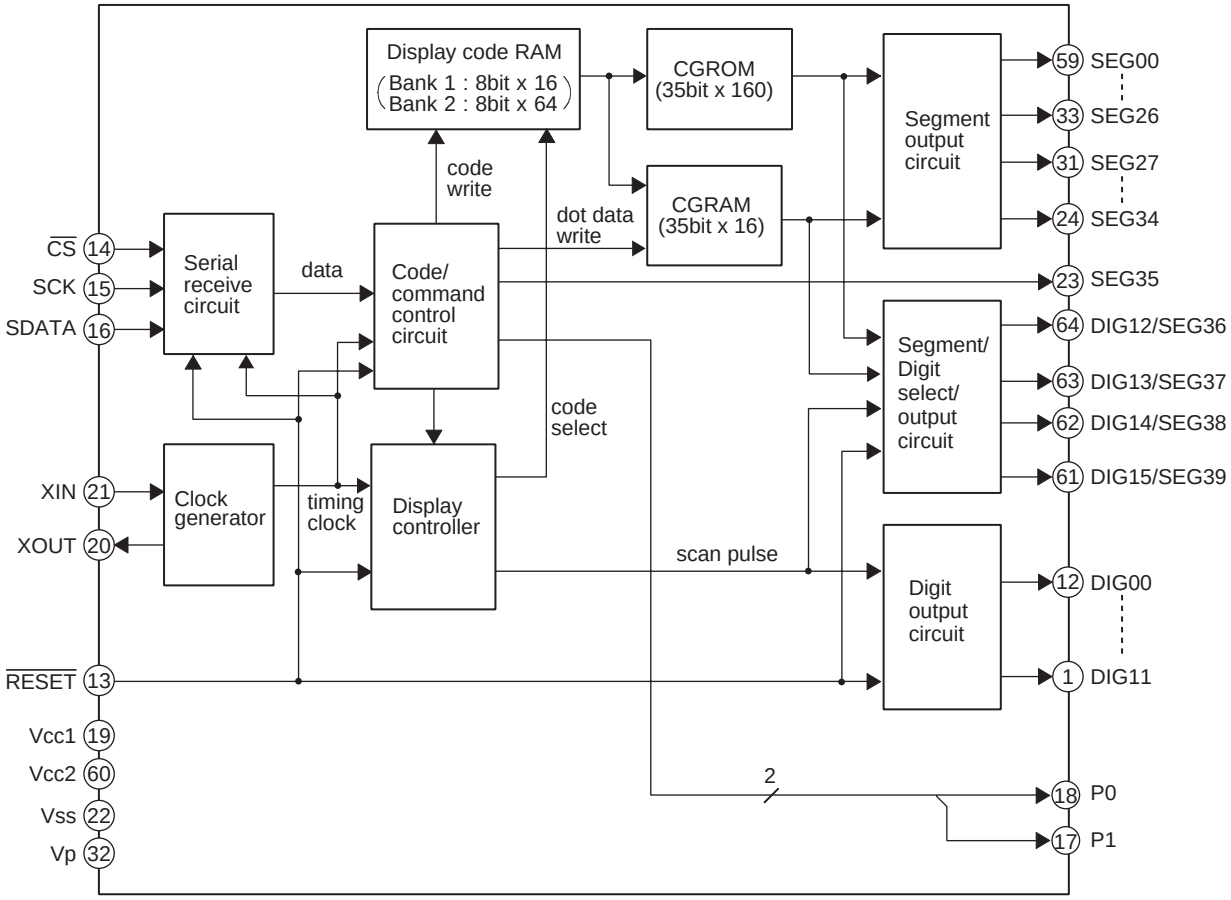
Soldering side



IC BLOCK DIAGRAM AND TERMINAL DESCRIPTIONS -1

Q7003: M66005 (FL Tube Driver)

BLOCK DIAGRAM



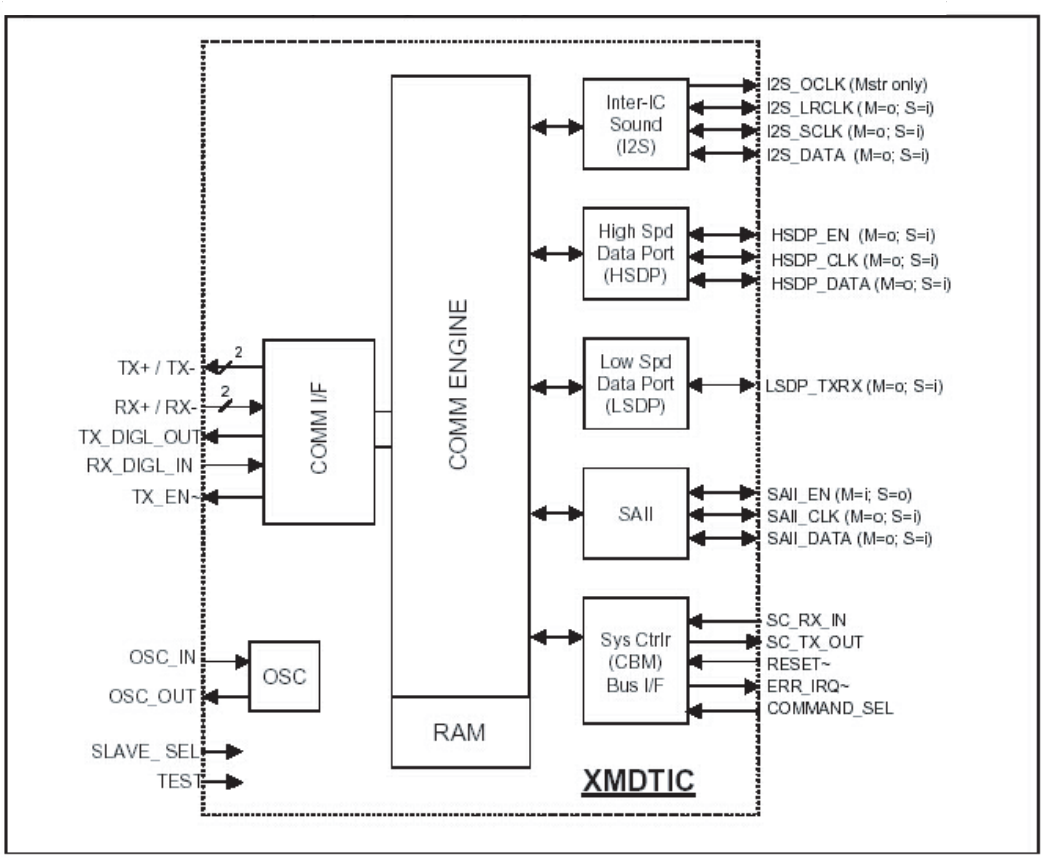
TERMINAL DESCRIPTION

PIN NO.	SYMBOL	PIN NAME	DESCRIPTION
13	$\overline{\text{RESET}}$	Reset input	This pin is used to initialize the internal state of the M66004.
14	$\overline{\text{CS}}$	Chip select input	"L" : Communication with the MCU is possible. "H" : Any instruction from the MCU is neglected.
15	SCK	Shift clock input	At the rising edge from "L" to "H", input data is shifted.
16	SDATA	Serial data input	Character code or command data to display is input from MSB.
21, 20	XIN, XOUT	Clock input Clock output	This pin is used to connect a resister and a capacitor externally to set oscillation frequency.
1~12 61~64	DIG00 ~ DIG15	Digit output	These pins are used to connect to digit pins of VFD.
23~31 33~59	SEG00 ~ SEG39	Segment output	These pins are used to connect to segment pins of VFD.
17, 18	P0, P1		Output port (static operation)
19	VCC1		Positive power supply for internal logic.
60	VCC2		Positive power supply for high-pressure-resistant output port.
22	VSS		GND
32	VP		Negative power supply for VFD drive.

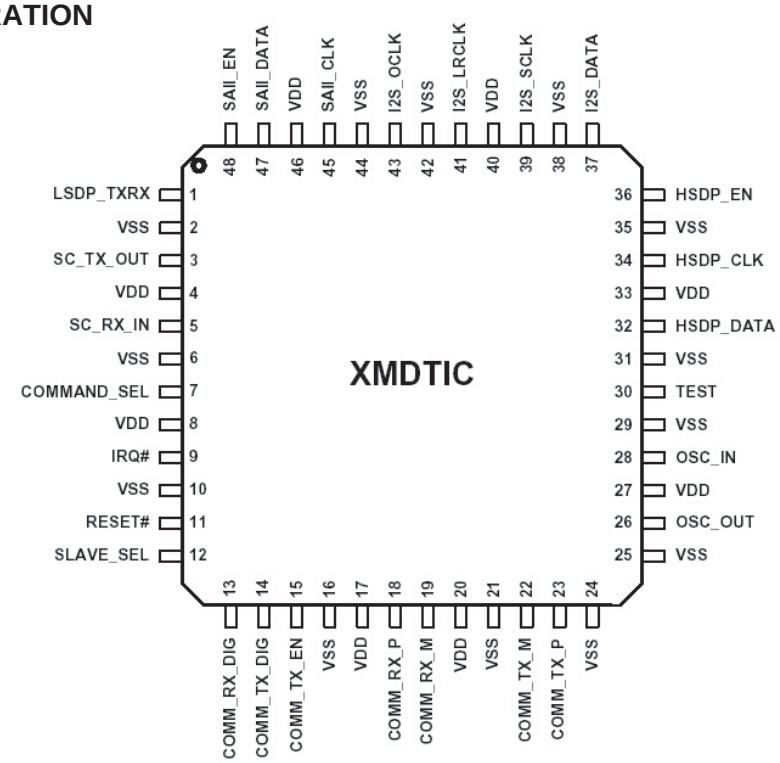
IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -2

Q2001 : F2602E (XM Digital Transceiver)

BLOCK DIAGRAM



PIN CONFIGURATION



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -3

Q2001 : F2602E (XM Digital Transceiver)

TERMINAL DESCRIPTION (1/2)

Pin #	Pin Name	Type	Function in Slave Mode	Function in Master Mode	Notes
1	LSDP_TXRX	S=In M=Out	Low Speed Data Port Output	Low Speed Data Port Input	LVTTL S/T
3	SC_TX_OUT	S=Out M=Out	System Controller Bus (CBM) Transmit Data Out	System Controller Bus (CBM) Transmit Data Out	4mA, SLC
5	SC_RX_IN	S=In M=In	System Controller Bus (CBM) Receive Data In	System Controller Bus (CBM) Receive Data In	LVTTL S/T
7	COMMAND_SEL	S=In M=In	Command Mode Select In (1= Command Mode, 0=Normal Mode)	Command Mode Select In (1= Command Mode, 0=Normal Mode)	LVTTL S/T
9	IRQ#	S=Out M=Out	Interrupt Request Out (Active Low)	Interrupt Request Out (Active Low)	4mA Open Drain
11	RESET#	S=In M=In	Asynchronous Reset In, (Active Low)	Asynchronous Reset In, (Active Low)	LVTTL S/T
12	SLAVE_SEL	S=In M=In	M/S Mode Select In (High = Slave Mode)	M/S Mode Select In (Low = Master Mode)	LVTTL S/T
13	COMM_RX_DIG	S=In M=In	DT Comm Bus External Transceiver Receive Data In	DT Comm Bus External Transceiver Receive Data In	LVTTL S/T
14	COMM_TX_DIG	Output	DT Comm Bus External Transceiver Transmit Data Out	DT Comm Bus External Transceiver Transmit Data Out	LVTTL S/T
15	COMM_TX_EN	Output	DT Comm Bus External Transceiver Direction Out (1=Transmit, 0=Receive)	DT Comm Bus External Transceiver Direction Out (1=Transmit, 0=Receive)	LVTTL S/T
18	COMM_RX_P	S=In M=In	DT Comm Bus Internal Receiver Differential Positive In	DT Comm Bus Internal Receiver Differential Positive In	LVDS in+
19	COMM_RX_M	S=In M=In	DT Comm Bus Internal Receiver Differential Negative In	DT Comm Bus Internal Receiver Differential Negative In	LVDS in–
22	COMM_TX_M	Output	DT Comm Bus Internal Transmitter Differential Negative Out	DT Comm Bus Internal Transmitter Differential Negative Out	LVDS out–
23	COMM_TX_P	Output	DT Comm Bus Internal Transmitter Differential Positive Out	DT Comm Bus Internal Transmitter Differential Positive Out	LVDS out+
26	OSC_OUT	Output	Crystal Output	Crystal Output	Crystal Buffer
28	OSC_IN	S=In M=In	Crystal Input	Crystal Input	Crystal Buffer
30	TEST	S=In M=In	Factory Test Mode Select (1=Test, 0= Normal Oper.)	Factory Test Mode Select (1=Test, 0= Normal Oper.)	LVTTL S/T
32	HSDP_DATA	S=In M=Out	High Speed Data Port Data Input	High Speed Data Port Data Output	Out= 4mA, SLC In=LVTTL S/T
34	HSDP_CLK	S=In M=Out	High Speed Data Port Clock Input	High Speed Data Port Clock Output	Out= 4mA, SLC In=LVTTL S/T
36	HSDP_EN	S=Out M=In	High Speed Data Port Enable Output	High Speed Data Port Enable Input	Out= 4mA, SLC In=LVTTL S/T
37	I2S_DATA	S=In M=Out	I2S Digital Port Data In	I2S Digital Audio Port Data Out	Out= 4mA, SLC In=LVTTL S/T

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -4

Q2001 : F2602E (XM Digital Transceiver)

TERMINAL DESCRIPTION (2/2)

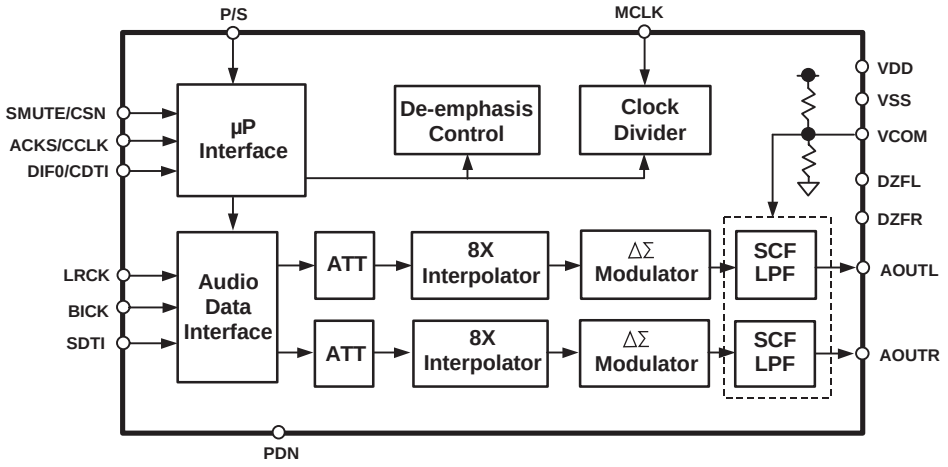
Pin #	Pin Name	Type	Function in Slave Mode	Function in Master Mode	Notes
39	I2S_SCLK	S=In M=Out	I2S Digital Audio Port Bit Clock In	I2S Digital Audio Port Bit Clock Out	Out= 4mA, SLC In=LVTTL S/T
41	I2S_LRCLK	S=In M=Out	I2S Digital Audio Port Left/Right Clock In	I2S Digital Audio Port Left/Right Clock Out	Out= 4mA, SLC In=LVTTL S/T
43	I2S_OCLK	S=In M=Out	I2S Digital Audio Port Oversample Clock (not used - connect to Gnd???)	I2S Digital Audio Port Oversample Clock Out	Out= 4mA, SLC
45	SAII_CLK	S=Out M=In	SAII Port Clock Output	SAII Port Clock Input	Out= 4mA, SLC 3.3V S/T
47	SAII_DATA	S=Out M=In	SAII Port Data Output	SAII Port Data Input	Out= 4mA, SLC In=LVTTL S/T
48	SAII_REQ	S=In M=Out	SAII Port Request Input	SAII Port Request Output	Out= 4mA, SLC In=LVTTL S/T

Pin#	Pin Name	Type	Function in Slave Mode	Function in Master Mode	Notes
4, 8, 17, 20, 27, 33, 40, 46	VDD	PWR	+3.3V Supply Voltage	+3.3V Supply Voltage	
2, 6, 10, 16, 21, 24, 25, 29, 31, 25, 38, 42, 44	VSS	GND	Digital Ground	Digital Ground	

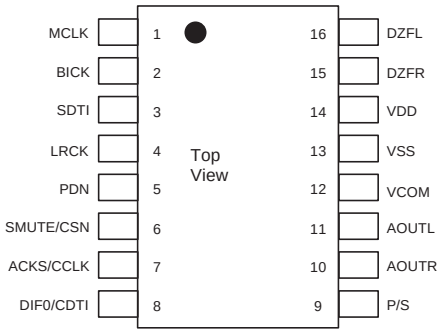
IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -5

Q2002: AK4384 (192kHz 24-Bit 2ch DAC)

BLOCK DIAGRAM



PIN CONFIGURATION



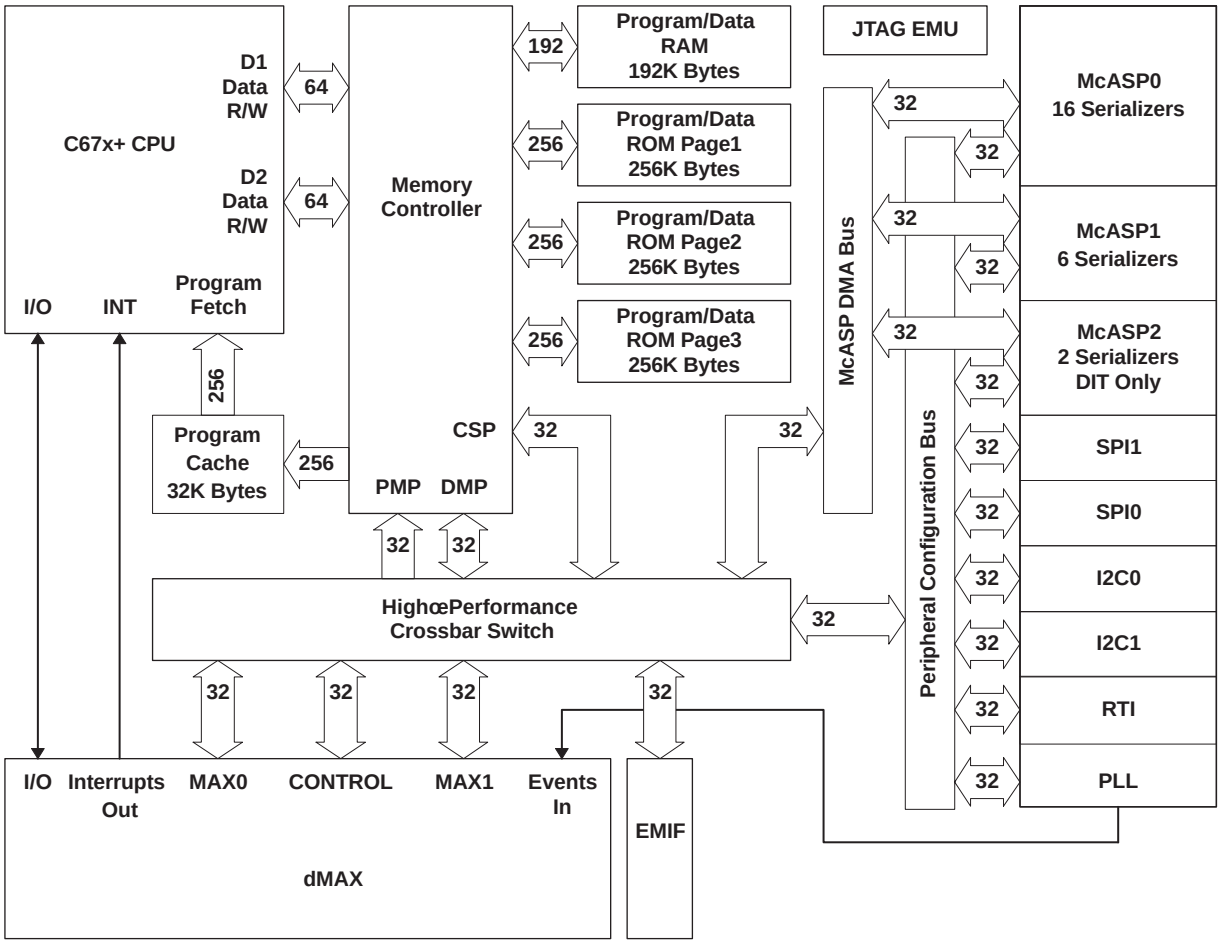
TERMINAL DESCRIPTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin
5	PDN	I	Power -Down Mode Pin When at "L", the AK4384 is in the power-down mode and is held in reset. The AK4384 should always be reset upon power-up.
6	SMUTE	I	Soft Mute Pin in parallel mode "H": Enable,"L": Disable
	CSN	I	Chip Select Pin in serial mode
7	ACKS	I	Auto Setting Mode Pin in parallel mode "L": Manual Setting Mode, "H": Auto Setting Mode
	CCLK	I	Control Data Clock Pin in serial mode
8	DIF0	I	Audio Data Interface Format Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial mode
9	P/S	I	Parallel/Serial Select Pin (Internal pull-up pin) "L": Serial control mode,"H": Parallel control mode
10	AOUTR	O	Rch Analog Output Pin
11	AOUTL	O	Lch Analog Output Pin
12	VCOM	O	Common Voltage Pin, VDD/2 Normally connected to VSS with a 0.1mF ceramic capacitor in parallel with a 10 m F electrolytic cap.
13	VSS	-	Ground Pin
14	VDD	-	Power Supply Pin
15	DZFR	O	Rch Data Zero Input Detect Pin
16	DZFL	O	Lch Data Zero Input Detect Pin

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -6

Q201 : TMS320DA707 (32 bit Floating-Point Digital Signal Processor)

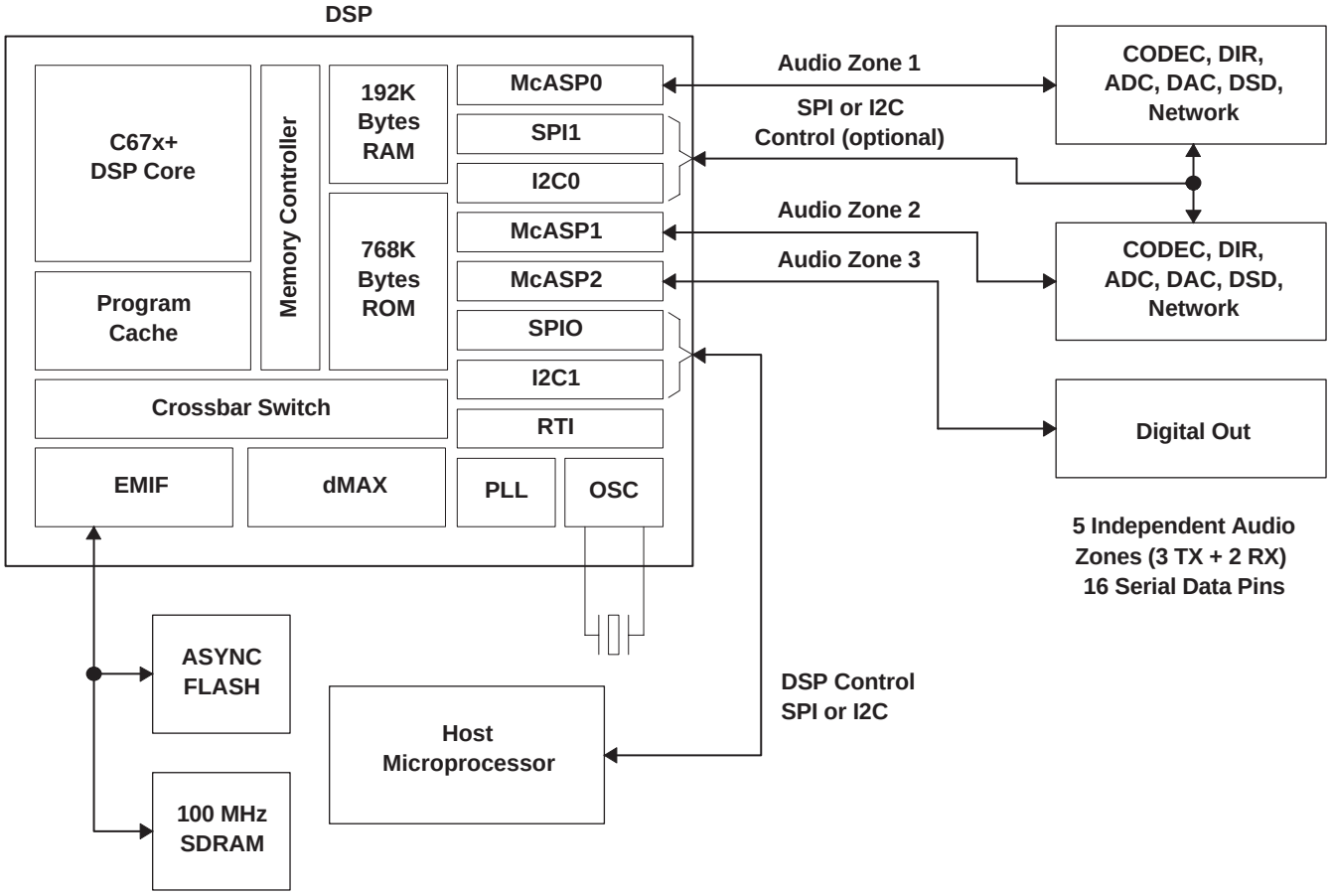
BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -7

Q201 : TMS320DA707 (32 bit Floating-Point Digital Signal Processor)

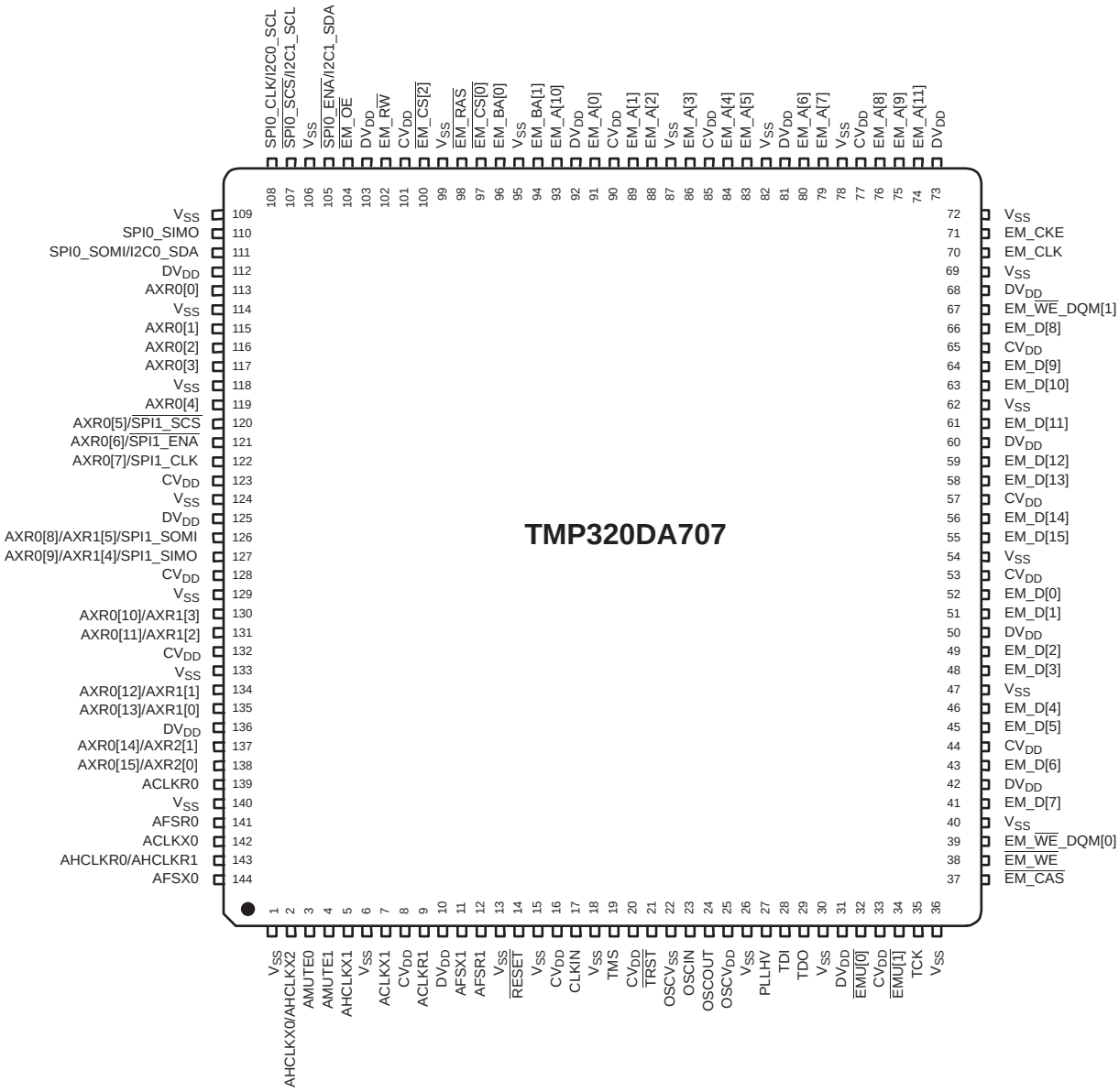
SYSTEM DIAGRAM with PERIPHERALS



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -8

Q201 : TMS320DA707 (32 bit Floating-Point Digital Signal Processor)

PIN CONFIGURATION



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -9

Q201 : TMS320DA707 (32 bit Floating-Point Digital Signal Processor)

TERMINAL DESCRIPTION (1/4)

SIGNAL NAME	PIN NO.	TYPE(1)	PULL(2)	GPIO(3)	DESCRIPTION
External Memory Interface (EMIF) Address and Control					
EM_A[0]	91	O	-	N	EMIF Address Bus
EM_A[1]	89	O	-	N	
EM_A[2]	88	O	-	N	
EM_A[3]	86	O	-	N	
EM_A[4]	84	O	-	N	
EM_A[5]	83	O	-	N	
EM_A[6]	80	O	-	N	
EM_A[7]	79	O	-	N	
EM_A[8]	76	O	-	N	
EM_A[9]	75	O	-	N	
EM_A[10]	93	O	-	N	
EM_A[11]	74	O	-	N	
EM_BA[0]	96	O	-	N	SDRAM Bank Address and Asynchronous Memory Low-Order Address
EM_BA[1]	94	O	-	N	
$\overline{\text{EM\_CS[0]}}$	97	O	-	N	SDRAM Chip Select
$\overline{\text{EM\_CS[2]}}$	100	O	-	N	Asynchronous Memory Chip Select
$\overline{\text{EM\_CAS}}$	37	O	-	N	SDRAM Column Address Strobe
$\overline{\text{EM\_RAS}}$	98	O	-	N	SDRAM Row Address Strobe
$\overline{\text{EM\_WE}}$	38	O	-	N	SDRAM Write Enable
EM_CKE	71	O	-	N	SDRAM Clock Enable
EM_CLK	70	O	-	N	SDRAM Clock
EM_$\overline{\text{WE}}$_DQM[0]	39	O	-	N	Write Enable or Byte Enable for EM_D[7:0]
EM_$\overline{\text{WE}}$_DQM[1]	67	O	-	N	Write Enable or Byte Enable for EM_D[15:8]
$\overline{\text{EM\_OE}}$	104	O	-	N	SDRAM Output Enable
EM_R$\overline{\text{W}}$	102	O	-	N	Asynchronous Memory Read/not Write

(1) TYPE column refers to pin direction in functional mode. If a pin has more than one function with different directions, the functions are separated with a slash (/).
(2) PULL column:
IPD = Internal Pulldown resistor
IPU = Internal Pullup resistor
(3) If the GPIO column is 'Y', then in GPIO mode, the pin is configurable as an IO unless otherwise marked.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -10

Q201 : TMS320DA707 (32 bit Floating-Point Digital Signal Processor)

TERMINAL DESCRIPTION (2/4)

SIGNAL NAME	PIN NO.	TYPE(1)	PULL(2)	GPIO(3)	DESCRIPTION
External Memory Interface (EMIF) Data Bus					
EM_D[0]	52	IO	-	N	EMIF Data Bus [Lower 16 Bits]
EM_D[1]	51	IO	-	N	
EM_D[2]	49	IO	-	N	
EM_D[3]	48	IO	-	N	
EM_D[4]	46	IO	-	N	
EM_D[5]	45	IO	-	N	
EM_D[6]	43	IO	-	N	
EM_D[7]	41	IO	-	N	
EM_D[8]	66	IO	-	N	
EM_D[9]	64	IO	-	N	
EM_D[10]	63	IO	-	N	
EM_D[11]	61	IO	-	N	
EM_D[12]	59	IO	-	N	
EM_D[13]	58	IO	-	N	
EM_D[14]	56	IO	-	N	
EM_D[15]	55	IO	-	N	

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -11

Q201 : TMS320DA707 (32 bit Floating-Point Digital Signal Processor)

TERMINAL DESCRIPTION (3/4)

SIGNAL NAME	PIN NO.	TYPE(1)	PULL(2)	GPIO(3)	DESCRIPTION
McASP0, McASP1, McASP2, and SPI1 Serial Ports					
AHCLKR0/AHCLKR1	143	IO	-	Y	McASP0 and McASP1 Receive Master Clock
ACLKR0	139	IO	-	Y	McASP0 Receive Bit Clock
AFSR0	141	IO	-	Y	McASP0 Receive Frame Sync (L/R Clock)
AHCLKX0/AHCLKX2	2	IO	-	Y	McASP0 and McASP2 Transmit Master Clock
ACLKX0	142	IO	-	Y	McASP0 Transmit Bit Clock
AFSX0	144	IO	-	Y	McASP0 Transmit Frame Sync (L/R Clock)
AMUTE0	3	O	-	Y	McASP0 MUTE Output
AXR0[0]	113	IO	-	Y	McASP0 Serial Data 0
AXR0[1]	115	IO	-	Y	McASP0 Serial Data 1
AXR0[2]	116	IO	-	Y	McASP0 Serial Data 2
AXR0[3]	117	IO	-	Y	McASP0 Serial Data 3
AXR0[4]	119	IO	-	Y	McASP0 Serial Data 4
AXR0[5]/$\overline{\text{SPI1\_SCS}}$	120	IO	-	Y	McASP0 Serial Data 5 ***or*** SPI1 Slave Chip Select
AXR0[6]/$\overline{\text{SPI1\_ENA}}$	121	IO	-	Y	McASP0 Serial Data 6 ***or*** SPI1 Enable (Ready)
AXR0[7]/SPI1_CLK	122	IO	-	Y	McASP0 Serial Data 7 ***or*** SPI1 Serial Clock
AXR0[8]/AXR1[5]/ SPI1_SOMI	126	IO	-	Y	McASP0 Serial Data 8 ***or*** McASP1 Serial Data 5 ***or*** SPI1 Data Pin Slave Out Master In
AXR0[9]/AXR1[4]/ SPI1_SIMO	127	IO	-	Y	McASP0 Serial Data 9 ***or*** McASP1 Serial Data 4 ***or*** SPI1 Data Pin Slave In Master Out
AXR0[10]/AXR1[3]	130	IO	-	Y	McASP0 Serial Data 10 ***or*** McASP1 Serial Data 3
AXR0[11]/AXR1[2]	131	IO	-	Y	McASP0 Serial Data 11 ***or*** McASP1 Serial Data 2
AXR0[12]/AXR1[1]	134	IO	-	Y	McASP0 Serial Data 12 ***or*** McASP1 Serial Data 1
AXR0[13]/AXR1[0]	135	IO	-	Y	McASP0 Serial Data 13 ***or*** McASP1 Serial Data 0
AXR0[14]/AXR2[1]	137	IO	-	Y	McASP0 Serial Data 14 ***or*** McASP2 Serial Data 1
AXR0[15]/AXR2[0]	138	IO	-	Y	McASP0 Serial Data 15 ***or*** McASP2 Serial Data 0
ACLKR1	9	IO	-	Y	McASP1 Receive Bit Clock
AFSR1	12	IO	-	Y	McASP1 Receive Frame Sync (L/R Clock)
AHCLKX1	5	IO	-	Y	McASP1 Transmit Master Clock
ACLKX1	7	IO	-	Y	McASP1 Transmit Bit Clock
AFSX1	11	IO	-	Y	McASP1 Transmit Frame Sync (L/R Clock)
AMUTE1	4	O	-	Y	McASP1 MUTE Output
SPI0, I2C0, and I2C1 Serial Port Pins					
SPI0_SOMI/I2C0_SDA	111	IO	-	Y	SPI0 Data Pin Slave Out Master In ***or*** I2C0 Serial Data
SPI0_SIMO	110	IO	-	Y	SPI0 Data Pin Slave In Master Out
SPI0_CLK/I2C0_SCL	108	IO	-	Y	SPI0 Serial Clock ***or*** I2C0 Serial Clock
$\overline{\text{SPI0\_SCS}}$/I2C1_SCL	107	IO	-	Y	SPI0 Slave Chip Select ***or*** I2C1 Serial Clock
$\overline{\text{SPI0\_ENA}}$/I2C1_SDA	105	IO	-	Y	SPI0 Enable (Ready) ***or*** I2C1 Serial Data

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -12

Q201 : TMS320DA707 (32 bit Floating-Point Digital Signal Processor)

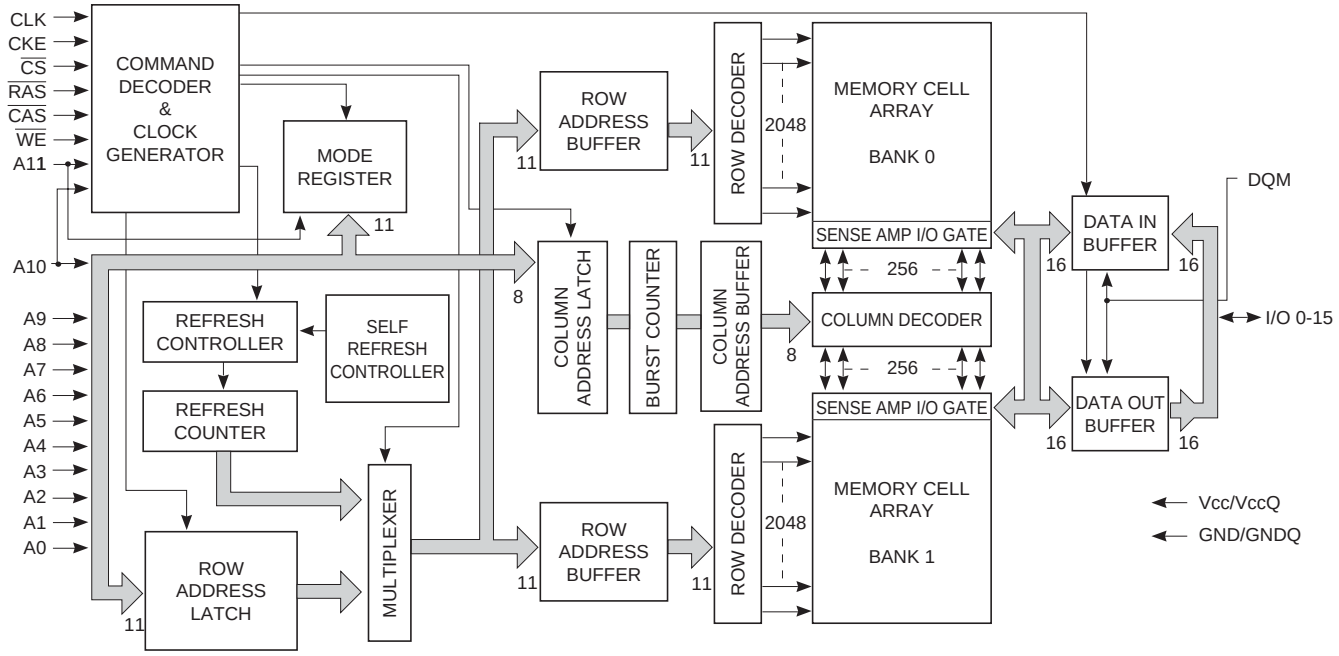
TERMINAL DESCRIPTION (4/4)

SIGNAL NAME	PIN NO.	TYPE(1)	PULL(2)	GPIO(3)	DESCRIPTION
Clocks					
OSCIN	23	I	-	N	1.2-V Oscillator Input
OSCOUT	24	O	-	N	1.2-V Oscillator Output
$OSCV_{DD}$	25	PWR	-	N	Oscillator 1.2-V V_{DD} tap point (for filter only)
$OSCV_{SS}$	22	PWR	-	N	Oscillator V_{SS} tap point (for filter only)
CLKIN	17	I	-	N	Alternate clock input (3.3-V LVCMOS Input)
PLLHV	27	PWR	-	N	PLL 3.3-V Supply Input (requires external filter)
Device Reset					
$\overline{\text{RESET}}$	14	I	-	N	Device reset pin
Emulation/JTAG Port					
TCK	35	I	IPU	N	Test Clock
TMS	19	I	IPU	N	Test Mode Select
TDI	28	I	IPU	N	Test Data In
TDO	29	OZ	IPU	N	Test Data Out
$\overline{\text{TRST}}$	21	I	IPD	N	Test Reset
$\overline{\text{EMU[0]}}$	32	IO	IPU	N	Emulation Pin 0
$\overline{\text{EMU[1]}}$	34	IO	IPU	N	Emulation Pin 1
Power Pins					
Core Supply (CV_{DD})	8, 16, 20, 33, 44, 53, 57, 65, 77, 85, 90, 101, 123, 128, 132				
IO Supply (DV_{DD})	10, 31, 42, 50, 60, 68, 73, 81, 92, 103, 112, 125, 136				
Ground (V_{SS})	1, 6, 13, 15, 18, 26, 30, 36, 40, 47, 54, 62, 69, 72, 78, 82, 87, 95, 99, 106, 109, 114, 118, 124, 129, 133, 140				

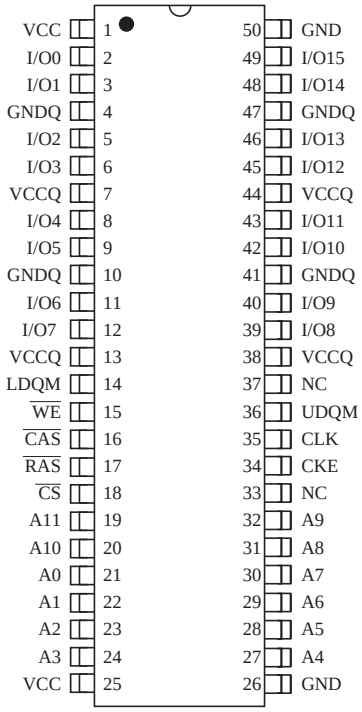
IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -13

Q281: IC42S16100 (16-Mbit Synchronous Dynamic RAM)

BLOCK DIAGRAM



PIN CONFIGURATION



IC BLOCK DIAGRAM AND TERMINAL DESCRIPTIONS -14

Q281: IC42S16100 (16-Mbit Synchronous Dynamic RAM)

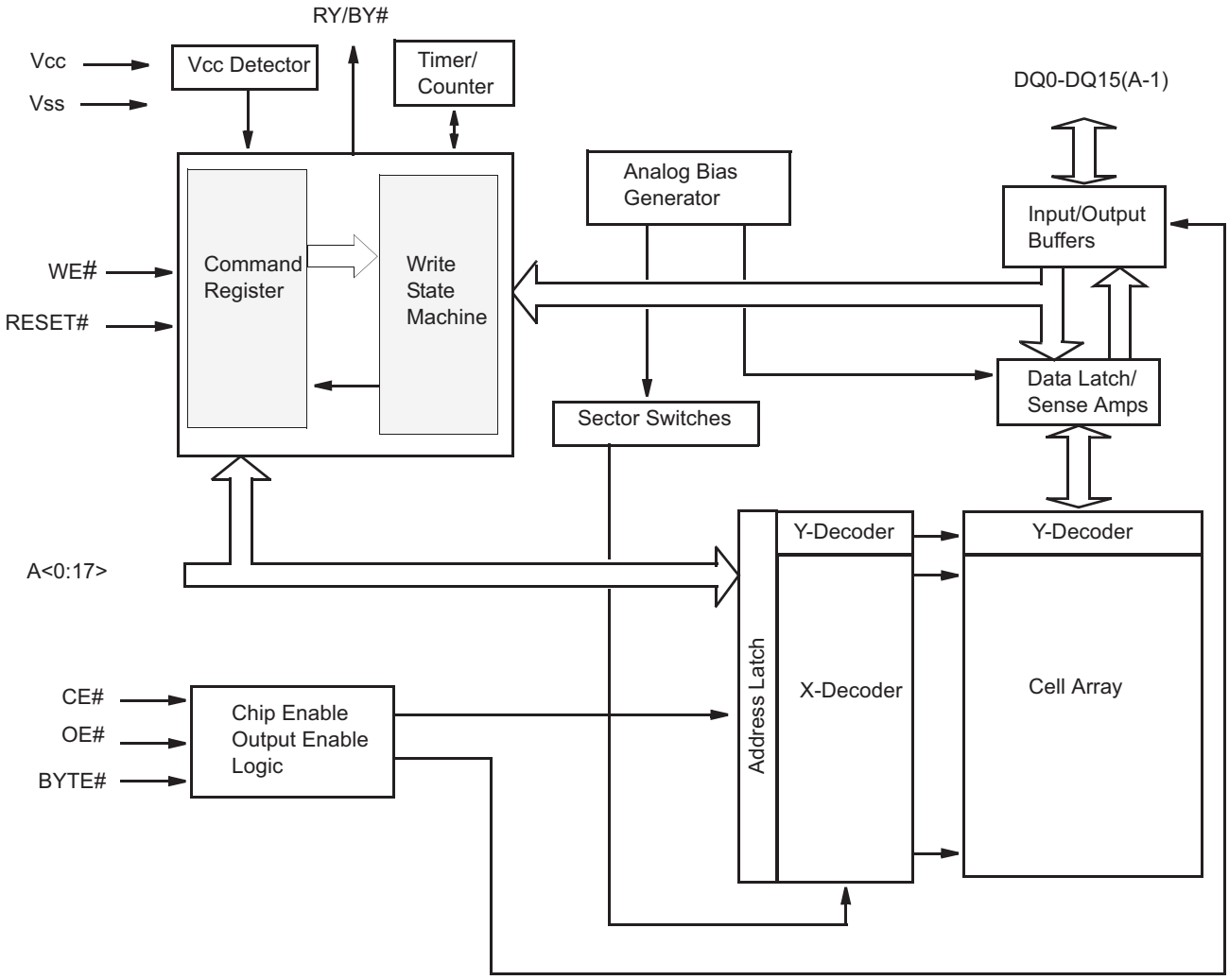
TERMINAL DESCRIPTION

Pin No.	Pin name	Function
20 to 24 27 to 32	A0-A10	A0 to A10 are address inputs. A0-A10 are used as row address inputs during active command input and A0-A7 as column address inputs during read or write command input. A10 is also used to determine the precharge mode during other commands. If A10 is LOW during precharge command, the bank selected by A11 is precharged, but if A10 is HIGH, both banks will be precharged. When A10 is HIGH in read or write command cycle, the precharge starts automatically after the burst access. These signals become part of the OP CODE during mode register set command input.
19	A11	A11 is the bank selection signal. When A11 is LOW, bank 0 is selected and when high, bank 1 is selected. This signal becomes part of the OP CODE during mode register set command input.
16	$\overline{CAS}$	$\overline{CAS}$, in conjunction with the $\overline{RAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
34	CKE	The CKE input determines whether the CLK input is enabled within the device. When is CKE HIGH, the next rising edge of the CLK signal will be valid, and when LOW, invalid. When CKE is LOW, the device will be in either the power-down mode, the clock suspend mode, or the self refresh mode. The CKE is an asynchronous input.
35	CLK	CLK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
18	$\overline{CS}$	The $\overline{CS}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{CS}$ is LOW, and disabled with $\overline{CS}$ is HIGH. The device remains in the previous state when $\overline{CS}$ is HIGH.
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	I/O0 to I/O15	I/O0 to I/O15 are I/O pins. I/O through these pins can be controlled in byte units using the LDQM and UDQM pins.
14, 36	LDQM, UDQM	LDQM and UDQM control the lower and upper bytes of the I/O buffers. In read mode, LDQM and UDQM control the output buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and when HIGH, disabled. The outputs go to theHIGH impedance state when LDQM/UDQM is HIGH. This function corresponds to $\overline{OE}$ in conventional DRAMs. In write mode, LDQM and UDQM control the input buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and data can be written to the device. When LDQM or UDQM is HIGH, input data is masked and cannot be written to the device.
17	$\overline{RAS}$	$\overline{RAS}$, in conjunction with $\overline{CAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
15	$\overline{WE}$	$\overline{WE}$, in conjunction with $\overline{RAS}$ and $\overline{CAS}$, forms the device command. See the "Command Truth Table" item for details on device commands.
7, 13, 38, 44	$V_{CC}Q$	$V_{CC}Q$ is the output buffer power supply.
1, 25	V_{CC}	V_{CC} is the device internal power supply.
4, 10, 41, 47	GNDQ	GNDQ is the output buffer ground.
26, 50	GND	GND is the device internal ground.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -15

Q282 : ES29LV400 (4 Mbit Flash Memory)

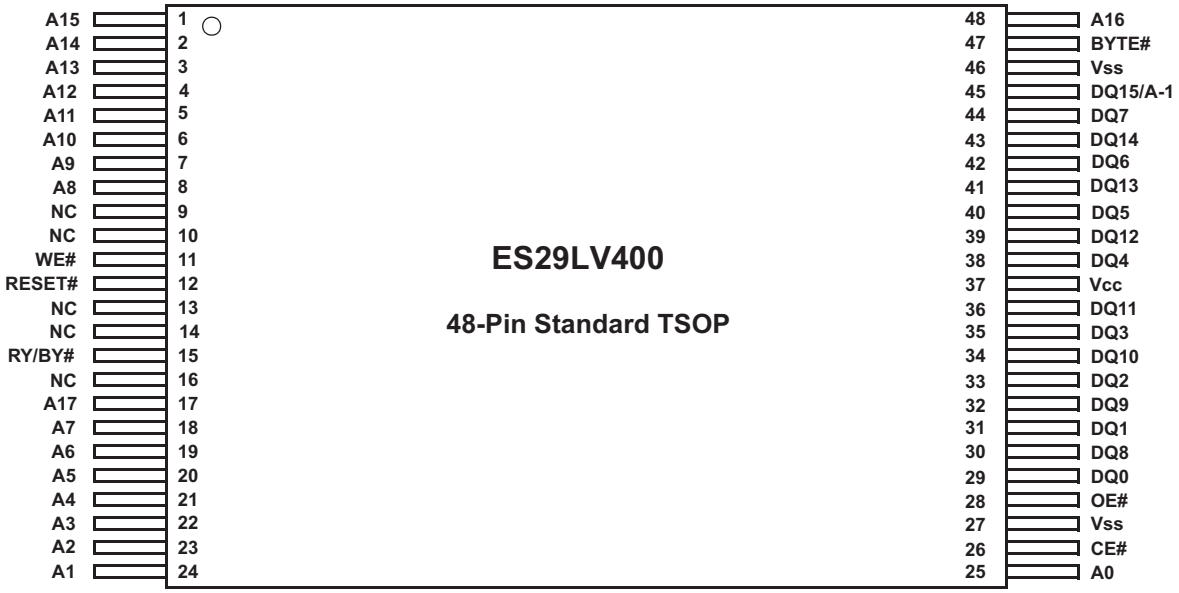
BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -16

Q282 : ES29LV400 (4 Mbit Flash Memory)

PIN CONFIGURATION



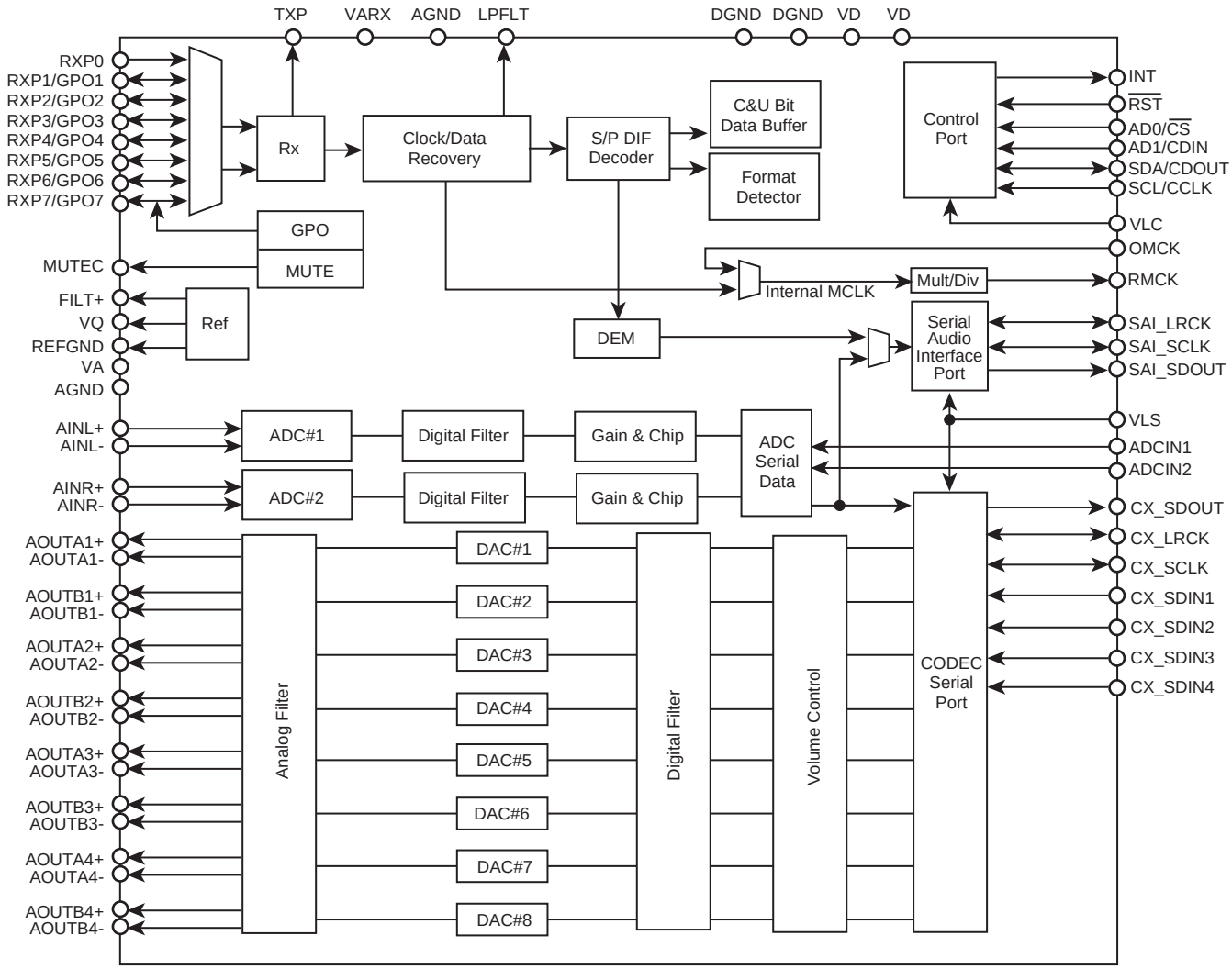
TERMINAL DESCRIPTION

Terminal	Description
A0-A17	18 Addresses
DQ0-DQ14	15 Data Inputs/Outputs
DQ15/A-1	DQ15 (Data Input/Output, Word Mode) A-1 (LSB Address Input, Byte Mode)
CE#	Chip Enable
OE#	Output Enable
WE#	Write Enable
RESET#	Hardware Reset Pin, Active Low
BYTE#	Selects 8-bit or 16-bit mode
RY/BY#	Ready/Busy Output
Vcc	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
Vss	Device Ground
NC	Pin Not Connected Internally

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -17

Q301 : CS42518 (8-Ch Codec with S/PDIF Receiver)

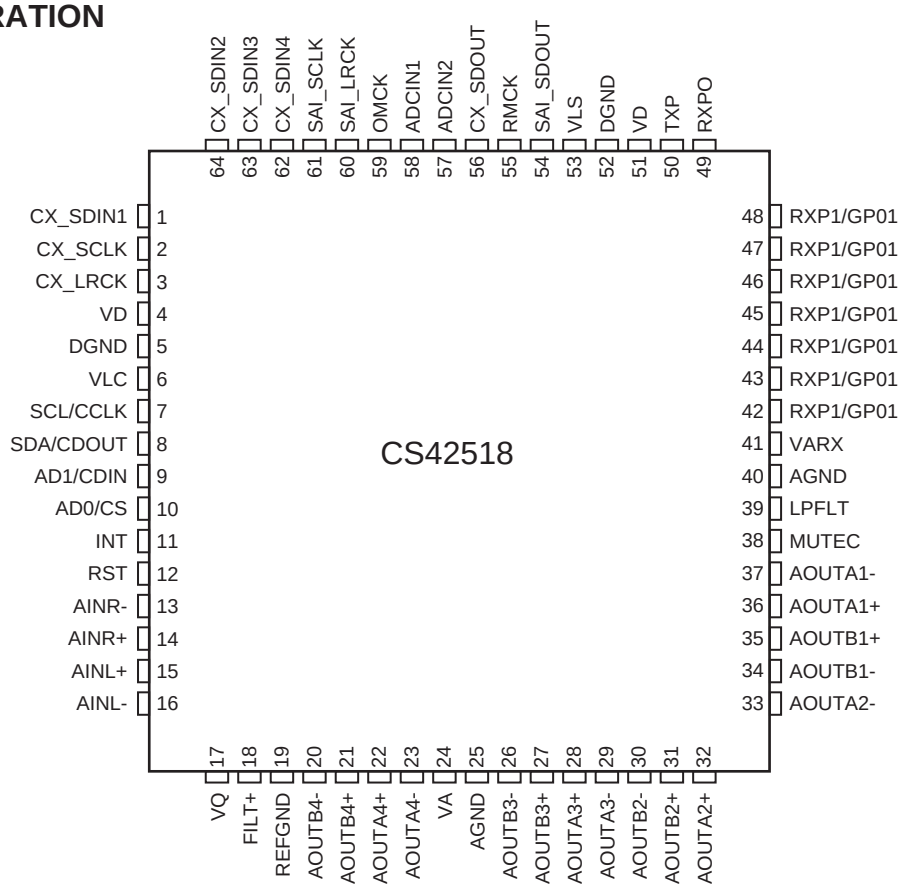
BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -18

Q301 : CS42518 (8-Ch Codec with S/PDIF Receiver)

PIN CONFIGURATION



TERMINAL DESCRIPTION (1/3)

Pin Name	#	Pin Description
CX_SDIN1 CX_SDIN2 CX_SDIN3 CX_SDIN4	1 64 63 62	Codec Serial Audio Data Input (Input) - Input for two's complement serial audio data.
CX_SCLK	2	CODEC Serial Clock (Input/Output) - Serial clock for the CODEC serial audio interface
CX_LRCK	3	CODEC Left Right Clock (Input/ Output) - Determines which channel, Left or Right, is currently active on the CODEC serial audio data line.
VD	4 51	Digital Power (Input) - Positive power supply for the digital section.
DGND	5 52	Digital Ground (Input) - Ground reference. Should be connected to digital ground.
VLC	6	Control Port Power (Input) - Determines the required signal level for the control port.
SCL/CCLK	7	Serial Control Port Clock (Input) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I2C mode as shown in the Typical Connection Diagram.
SDA/CDOUT	8	Serial Control Data (Input/Output) - SDA is a data I/O line in IC mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical connection Diagram. CDOUT is the output data line for the control port interface in SPI mode.
AD1/CDIN	9	Address Bit 1 (I2C)/Serial Control Data (SPI) (Input) - AD1 a chip address pin in I2C mode; CDIN is the input data line for control port interface in SPI mode.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -19

Q301 : CS42518 (8-Ch Codec with S/PDIF Receiver)

TERMINAL DESCRIPTION (2/3)

Pin Name	#	Pin Description
AD0/CS	10	Address Bit 0 (I2C)/Control Port Chip Select (SPI) (INput) - AD0 is a chip address pin in I2C mode; CS is the chip select signal in SPI mode.
INT	11	Interrupt (Ountput) - The CS42518 will generate an interrupt condition as per the Interrupt Mask register.
RST	12	Reset (Input) - The device enters a low power mode and all internal registers are reset to their default settings when low.
AINR- AINR+	13 14	Differential right Channel Analog Input (Input) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
AINL- AINL+	15 16	Differential right Channel Analog Input (Input) - Signals are presented differentially to the delta-sigma modulators via the AINR+/- pins.
VQ	17	Quiescent Voltage (Output) - Filter connection for internal quiescent reference voltage.
FILT+	18	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits.
REFGND	19	Reference Ground (Input) - Ground reference for the internal sampling circuits.
AOUTA1 +, - AOUTB1 +, - AOUTA2 +, - AOUTB2 +, - AOUTA3 +, - AOUTB3 +, - AOUTA4 +, - AOUTB4 +, -	36, 37 35, 34 32, 33 31, 30 28, 29 27, 26 22, 23 21, 20	Differential Analog Output (Output) - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
VA VARX	24 41	Analog Power (Input) - Positive power supply for the analog section.
AGND	25 40	Analog Ground (Input) - Ground reference. Should be connected to analog ground.
MUTEC	38	Mute Control (Output) - The Mute Control pin outputs high impedance following an initial power -on condition or whenever the PDN bit is set to a "1", forcing the codec into power -down mode. The signal will remain in a high impedance state as long as the part is in power-down mode. The Mute Control pin goes to the selected "active" state during reset, muting, or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatoy but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
LPFLT	39	PLL Loop Filer (Output) - An RC network should be connected between this pin and ground.
RXP7/GPO7 RXP6/GPO6 RXP5/GPO5 RXP4/GPO4 RXP3/GPO3 RXP2/GPO2 RXP1/GPO1	42 43 44 45 46 47 48	S/PDIF Receiver Input/ General Purpose Output (Input/ Output) - Receiver inputs for S/PDIF encoded data. The CS42518 has an internal 8:2 multiplexer to select the active receiver port, according to the Receiver Mode Control 2 resister. These pins can also be configured as general purpose output pins, ADC Overflow indicators or Mute Control outputs according to the RXP/General Purpose Pin Control resisters.
RXP0	49	S/PDIF Receiver Input (Input) - Dedicated receiver input for S/PDIF encoded data.
TXP	50	S/PDIF Transmitter Output (Output) - S/PDIF encoded data output, mapped directly from one of the receiver inputs as indicated by the Receiver Mode Control 2 resister.
VLP	53	Serial Port Interface Power (Input) - Determines the required signal level for the serial port interfaces.
SAI_SDOUT	54	Serial Audio Interface Serial Data Output (Output) - Output for two's complement serial audio PCM data from the S/PDIF incoming stream. This pin can also be configured to transmit the output of the internal and external ADCs.
RMCK	55	Recovered Master Clock (Output) - Recovered master clock output from the External Clock Reference

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -20

Q301 : CS42518 (8-Ch Codec with S/PDIF Receiver)

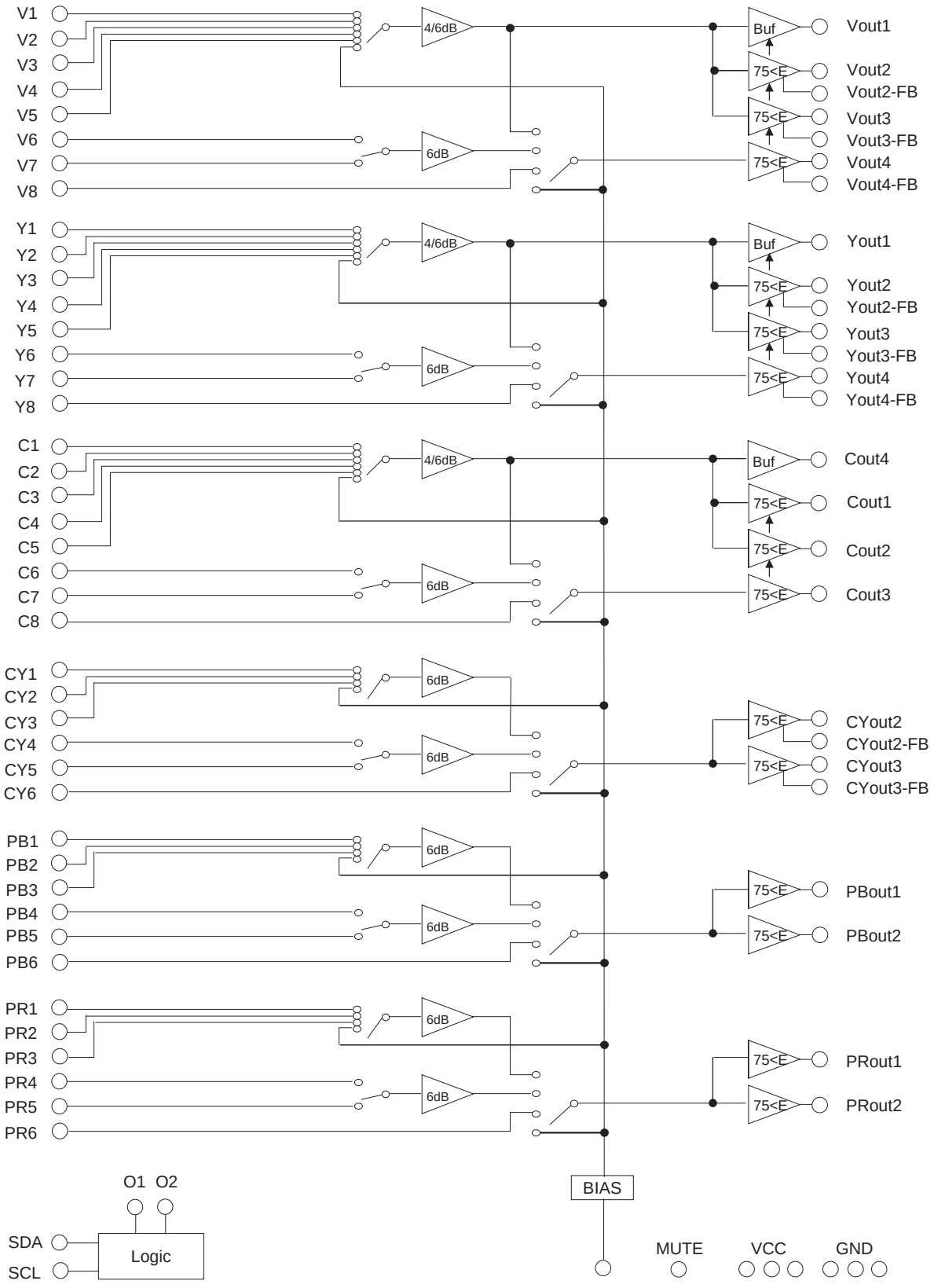
TERMINAL DESCRIPTION (3/3)

Pin Name	#	Pin Description
CL_SDOUT	56	CODEC Serial Data Output (Output) - Output for two's complement serial audio data the internal and external ADCs.
ADCIN1 ADCIN2	58 57	External ADC Serial Input (Input) - The CS42518 provides for up two external stereo analog to digital converter inputs to provide a maximum of six channels on serial data output line when the CS42518 is placed in One Line mode.
OMCK	59	External Reference Clock (Input) - External clock reference that must be within the ranges specified in currently active on the serial audio data line.
SAI_LRCK	60	Serial Audio Interface Left/Right Clock (Input/Output) - Determines which channel, Left of Right, is currently active on the serial audio data line.
SAI_LRCK	61	Serial Audio Interface Serial Clock (Input/Output) - Serial clock for the Serial Audio Interface

IC BLOCK DIAGRAM AND TERMINAL DESCRIPTIONS -21

Q4002: AN15881A (Video SW for TV with Multi-signal 14 Inputs and 4 Outputs)

BLOCK DIAGRAM



IC BLOCK DIAGRAM AND TERMINAL DESCRIPTIONS -22

Q4002: AN15881A (Video SW for TV with Multi-signal 14 Inputs and 4 Outputs)

TERMINAL DESCRIPTION (1/3)

Pin No.	Pin name	Type	Description
1	Y3	In	Luminance signal input 3
2	Y4	In	Luminance signal input 4
3	Y5	In	Luminance signal input 5
4	Y6	In	Luminance signal input 6
5	Y7	In	Luminance signal input 7
6	Y8	In	Luminance signal input 8
7	VCC1	Power supply	5.0V power supply
8	C1	In	Chrominance signal input 1
9	C2	In	Chrominance signal input 2
10	C3	In	Chrominance signal input 3
11	C4	In	Chrominance signal input 4
12	C5	In	Chrominance signal input 5
13	GND1	Ground	Ground
14	C6	In	Chrominance signal input 6
15	C7	In	Chrominance signal input 7
16	C8	In	Chrominance signal input 8
17	BIAS	Output	Bias voltage
18	CY1	In	CY1 signal input
19	CY2	In	CY2 signal input
20	CY3	In	CY3 signal input
21	CY4	In	CY4 signal input
22	CY5	In	CY5 signal input
23	CY6	In	CY6 signal input
24	PB1	In	PB1 signal input
25	PB2	In	PB2 signal input
26	PB3	In	PB3 signal input
27	PB4	In	PB4 signal input
28	PB5	In	PB5 signal input
29	PB6	In	PB6 signal input
30	PR1	In	PR1 signal input
31	PR2	In	PR2 signal input
32	PR3	In	PR3 signal input
33	PR4	In	PR4 signal input
34	PR5	In	PR5 signal input
35	PR6	In	PR6 signal input

IC BLOCK DIAGRAM AND TERMINAL DESCRIPTIONS -23

Q4002: AN15881A (Video SW for TV with Multi-signal 14 Inputs and 4 Outputs)

TERMINAL DESCRIPTION (2/3)

Pin No.	Pin name	Type	Description
36	MUTE	In	Mute control pin
37	PROUT2	Out	PROUT2 signal output
38	O1	Out	General output 1
39	PROUT1	Out	PROUT1 signal output
40	O2	Out	General output 2
41	PBOUT2	Out	PBOUT2 signal output
42	PBOUT1	Out	PBOUT1 signal output
43	GND2	Ground	Ground
44	CYOUT3-FB	In	CYOUT3 feedback input
45	CYOUT3	Out	CYOUT3 signal output
46	CYOUT2-FB	In	CYOUT2 feedback input
47	CYOUT2	Out	CYOUT2 signal output
48	COUT4	Out	COUT4 signal output
49	VCC2	Power supply	5.0V power supply
50	COUT3	Out	COUT3 signal output
51	COUT2	Out	COUT2 signal output
52	COUT1	Out	COUT1 signal output
53	GND3	Ground	Ground
54	YOUT4-FB	In	YOUT4 feedback input
55	YOUT4	Out	YOUT4 signal output
56	YOUT3-FB	In	YOUT3 feedback input
57	YOUT3	Out	YOUT3 signal output
58	YOUT2-FB	In	YOUT2 feedback input
59	YOUT2	Out	YOUT2 signal output
60	YOUT1	Out	YOUT1 signal output
61	VCC3	Power supply	5.0V power supply
62	VOUT4-FB	In	VOUT4 feedback input
63	VOUT4	Out	VOUT4 signal output
64	SDA	In	I^2C bus data input
65	VOUT3-FB	In	VOUT3 feedback input
66	VOUT3	Out	VOUT3 signal output
67	VOUT2-FB	In	VOUT2 feedback input
68	VOUT2	Out	VOUT2 signal output
69	VOUT1	Out	VOUT1 signal output
70	SCL	In	I^2C bus clock input

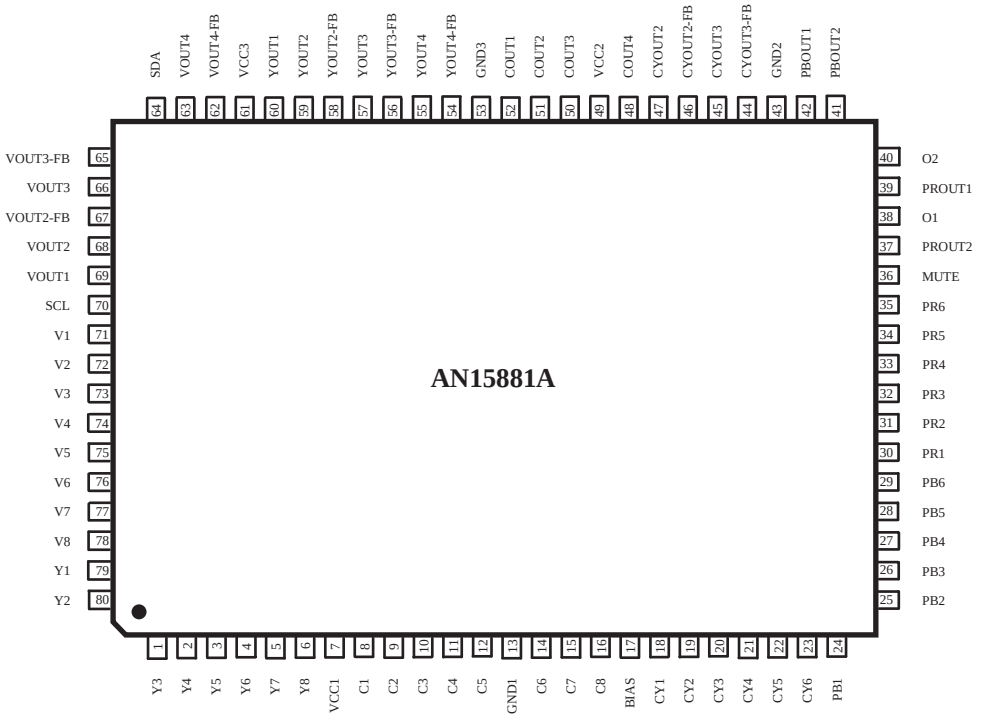
IC BLOCK DIA GRAM AND TERMINAL DESCRIPTIONS -24

Q4002: AN15881A (Video SW for TV with Multi-signal 14 Inputs and 4 Outputs)

TERMINAL DESCRIPTION (3/3)

Pin No.	Pin name	Type	Description
71	V1	In	Video composite signal input 1
72	V2	In	Video composite signal input 2
73	V3	In	Video composite signal input 3
74	V4	In	Video composite signal input 4
75	V5	In	Video composite signal input 5
76	V6	In	Video composite signal input 6
77	V7	In	Video composite signal input 7
78	V8	In	Video composite signal input 8
79	Y1	In	Luminance signal input 1
80	Y2	In	Luminance signal input 2

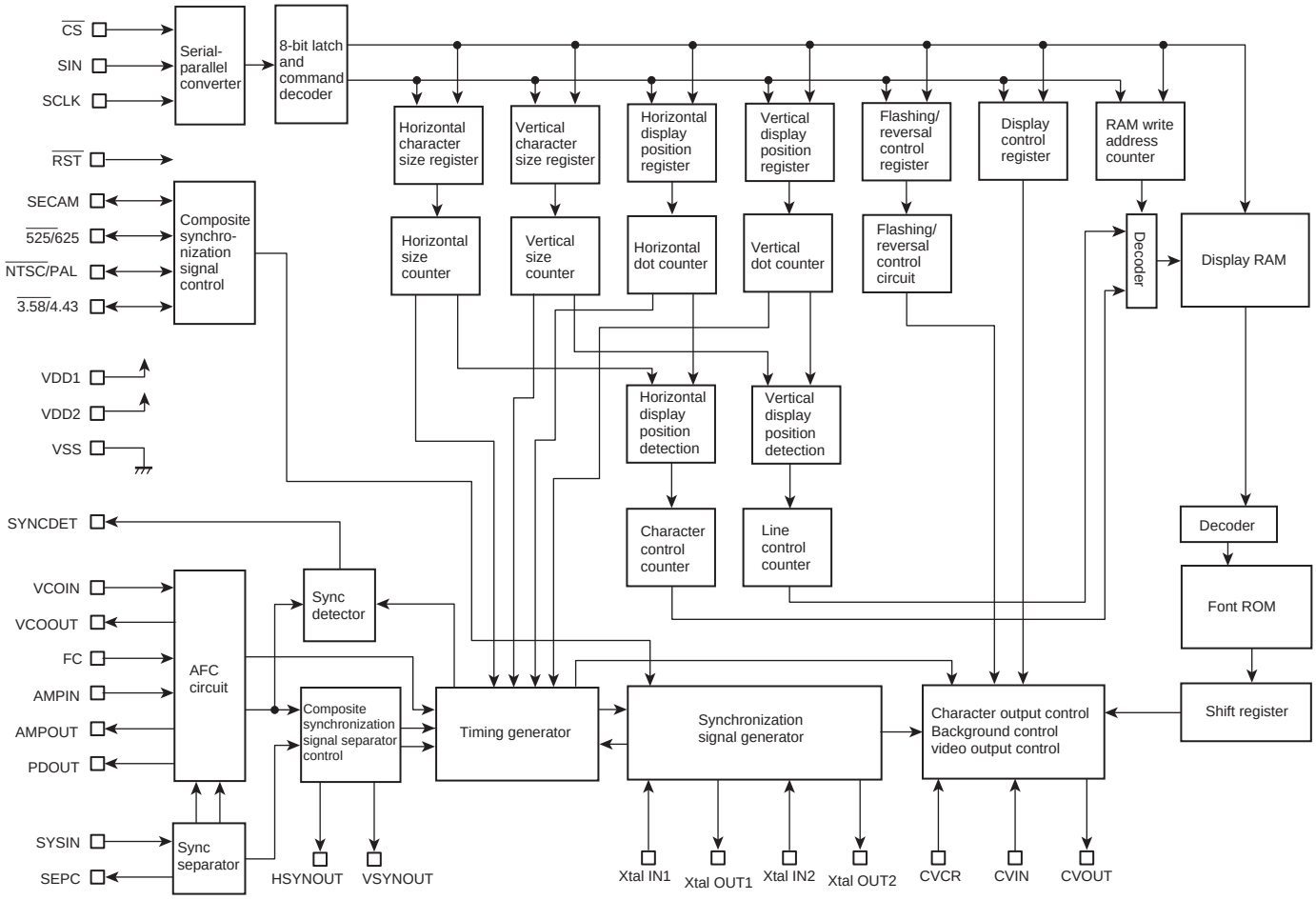
PIN CONFIGURATION



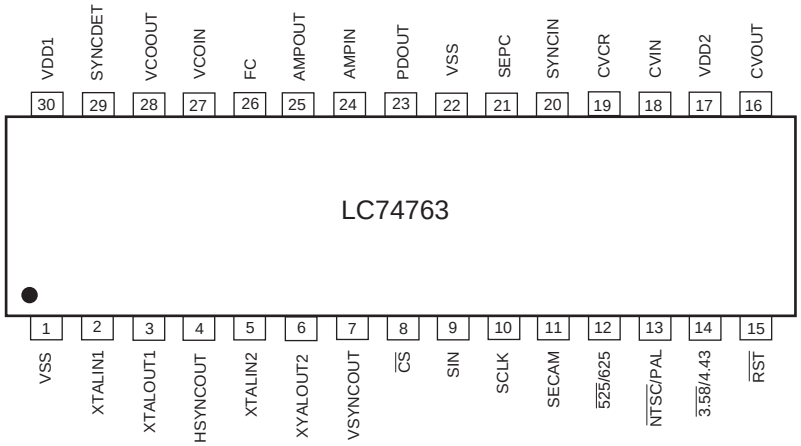
IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -25

Q4004: LC74763-9836 (On-Screen Display IC)

BLOCK DIAGRAM



PIN CONFIGRATION



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -26

Q4004: LC74763-9836 (On-Screen Display IC)

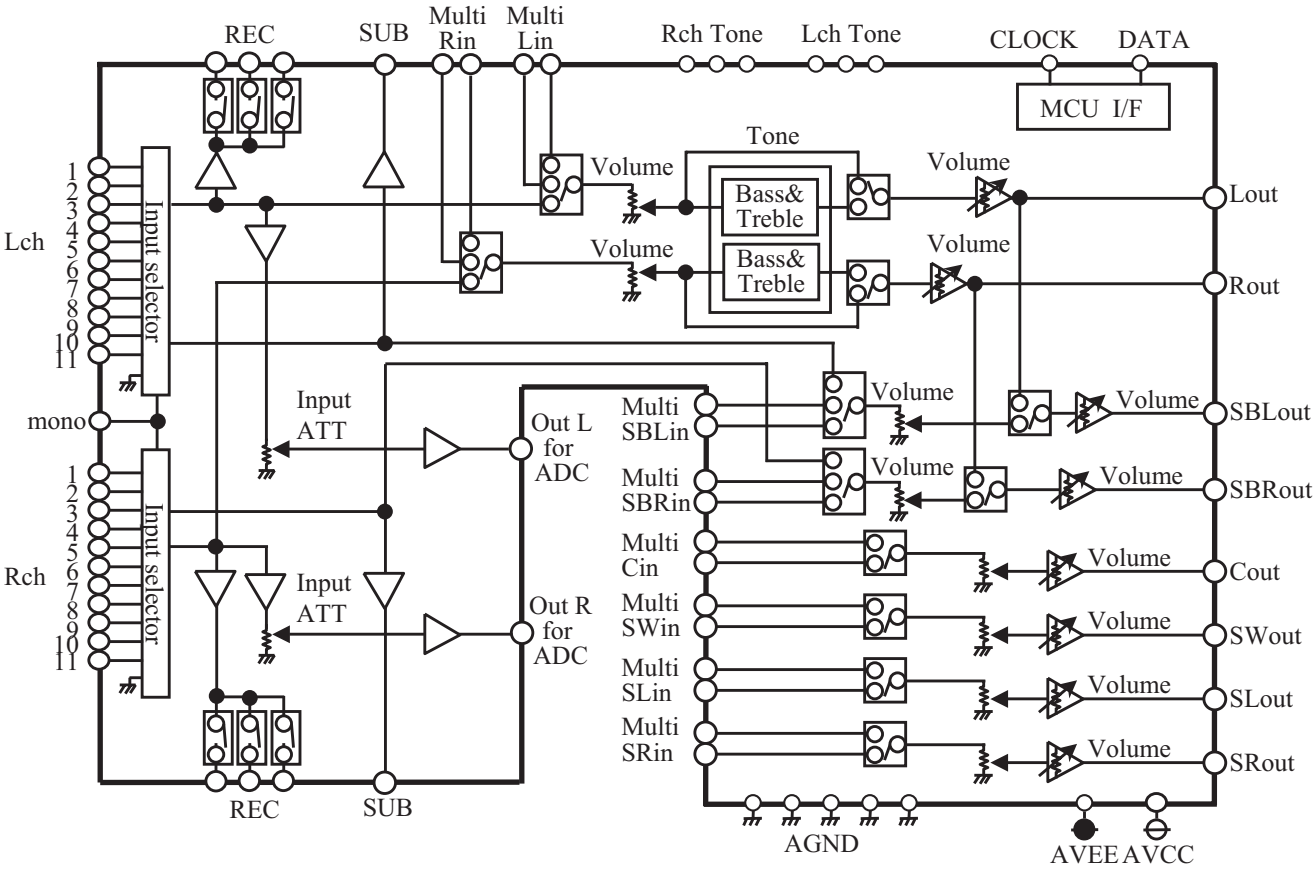
TERMINAL DESCRIPTION

Pin No.	Symbol	Function	Description
1	V_{SS}	Ground	Ground connection
2	$Xtal_{IN1}$	Crystal oscillator connection	Connection for the crystal and capacitor used to form the crystal oscillator that generates the internal synchronization signal. The oscillator can be selected with a command switch.
3	$Xtal_{OUT1}$		
4	$HSYNC_{OUT}$	Horizontal synchronization output	Outputs the horizontal synchronization signal (AFC). The output polarity can be selected (metal option). Also functions as general output port (command switch).
5	$Xtal_{IN2}$	Crystal oscillator connection	Connection for the crystal and capacitor used to form the crystal oscillator that generates the internal synchronization signal.
6	$Xtal_{OUT2}$		
7	$VSYNC_{OUT}$	Vertical synchronization output	Outputs the vertical synchronization signal. The output polarity can be selected (metal option). Also functions as general output port (command switch).
8	$\overline{CS}$	Enable input	Enables/disables serial data input. Serial data is enabled when this pin is low (hysteresis input). Pull-up resistor built in (metal option).
9	SIN	Data input	Serial data input (hysteresis input). Pull-up resistor built in (metal option).
10	SCLK	Clock input	Clock input for serial data input (hysteresis input). Pull-up resistor built in (metal option).
11	SECAM	SECAM mode switch input/ output (command switch)	During input, switches between SECAM and other modes. During output, functions as general output port or internal V output (command switch). Low = other modes, high = SECAM mode
12	$\overline{525}$/625	525/625 switch input/output (command switch)	During input, switches between 525 scan lines and 625 scan lines. During output, functions as general output port or character data output (command switch). Low = 525 lines, high = 625 lines
13	$\overline{NTSC}$/PAL	NTSC/PAL switch input/output (command switch)	Switches the color mode between NTSC and PAL. During output, functions as general output port or frame data output (command switch). Low = NTSC, high = PAL
14	$\overline{3.58}$/4.43	3.58/4.43 switch input/output (command switch)	Switch FSC between 3.58 MHz and 4.43 MHz. During output, functions as general output port or halftone output (command switch). Low = 3.58, high = 4.43
15	$\overline{RST}$	Reset input	System reset input pin, low is active (hysteresis input). Pull-up resistor built in (metal option).
16	CV_{OUT}	Video signal output	Composite video output
17	V_{DD2}	Power supply connection	Power supply connection for composite video signal level generation
18	CV_{IN}	Video signal input	Composite video input
19	CV_{CR}	Video signal input	SECAM chroma signal input
20	$SYNC_{IN}$	Sync separator circuit input	Built-in sync separator circuit video signal input
21	SEP_{C}	Sync separator circuit	Built-in sync separator circuit
22	V_{SS}	Ground	Ground connection
23	PD_{OUT}	Control voltage output	AFC control voltage output
24	AMP_{IN}	AFC filter connection	Filter connection
25	AMP_{OUT}		
26	FC	Control voltage input	AFC control voltage input
27	VCO_{IN}	LC oscillator connection	VCO LC oscillator circuit coil and capacitor connection
28	VCO_{OUT}		
29	$SYNC_{DET}$	External synchronization signal detection output	Outputs the exclusive NOR of the horizontal synchronization signal (AFC) and CSYNC (sync separator). The output polarity can be selected (metal option). Also functions as general output port (command switch).
30	V_{DD1}	Power supply connection	Power supply connection (+5 V: digital system power supply)

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -27

Q5501 : R2S15211FP (8 ch Electronic Volume and 11 Input Selector and Tone Control)

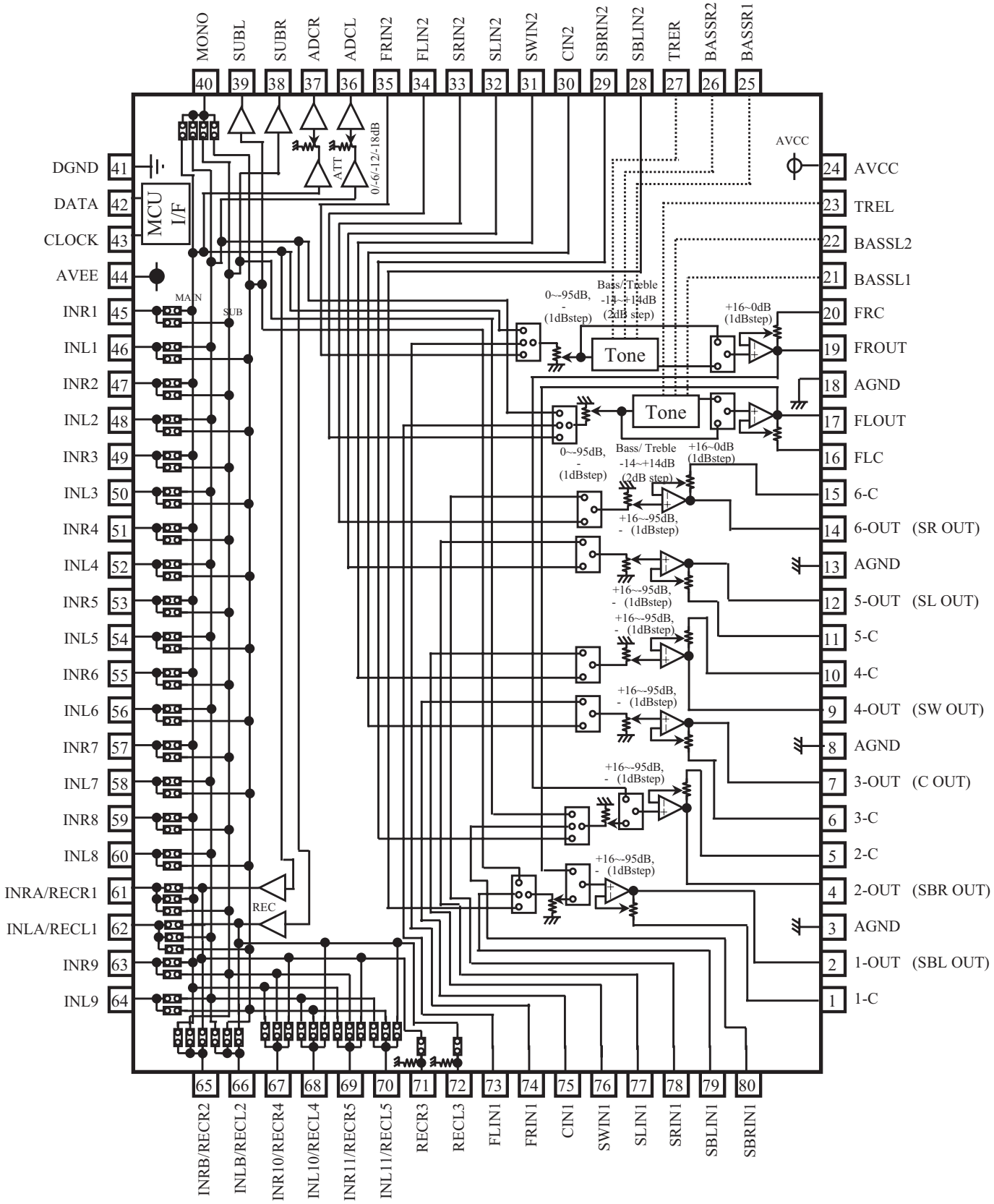
SYSTEM BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -28

Q5501 : R2S15211FP (8 ch Electronic Volume and 11 Input Selector and Tone Control)

BLOCK DIAGRAM AND PIN CONFIGURATION



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -29

Q5501 : R2S15211FP (8 ch Electronic Volume and 11 Input Selector and Tone Control)

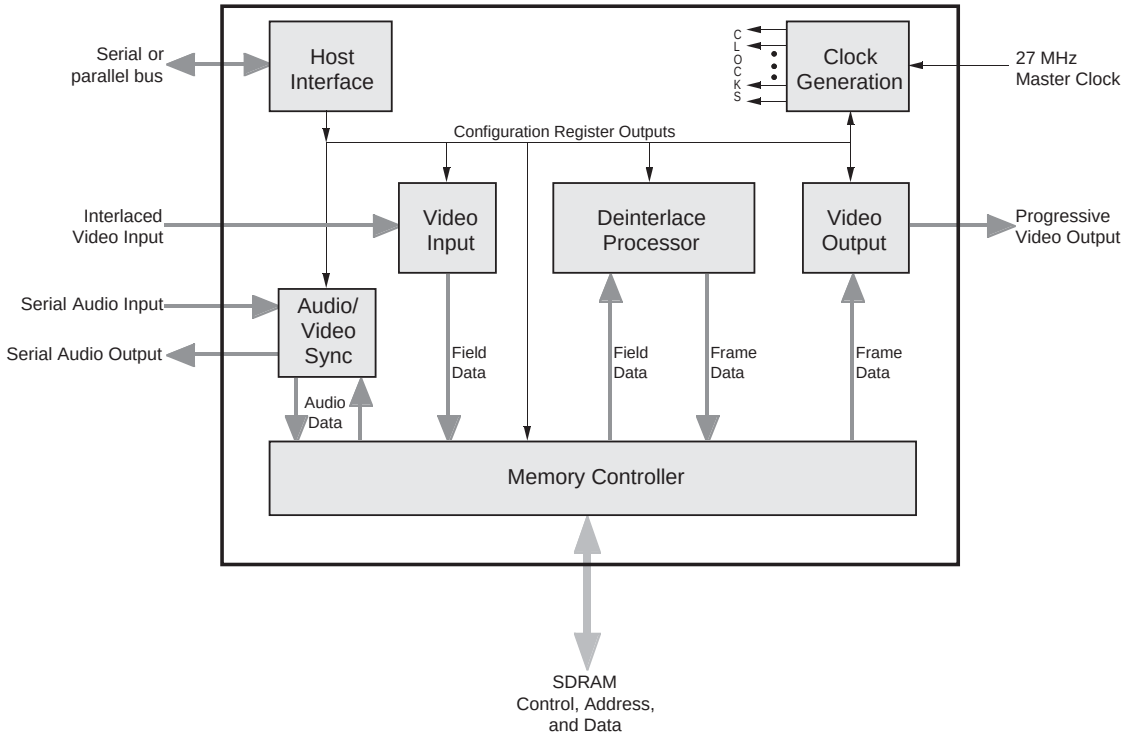
TERMINAL DESCRIPTION

PIN No.	Name	Function
19,17, 14,12, 9,7, 4,2	FROUT,FLOUT, 6-OUT,5-OUT, 4-OUT, 3-OUT, 2-OUT,1-OUT	Output pin of FL/FR/C/SW/SL/SR/SBL/SBR channel
20,16, 15,11, 10,6, 5,1	FRC,FLC, 6-C,5-C, 4-C,3-C, 2-C,1-C	Connects capacitor for reducing click noise of L/R/C/SW/SL/SR/SBL/SBR channel volume
3,8, 13,18	AGND	Analog ground of internal circuit
23,27	TREL, TRER	Frequency characteristic setting pin of L/R channel tone control (Treble)
21,22, 25,26	BASSL1,BASSL2 BASSR1,BASSR2	Frequency characteristic setting pin of L/R channel tone control (Bass)
24	AVCC	Positive power supply to internal circuit
35,34, 33,32, 31,30, 29,28	FRIN2, FLIN2, SRN2,SLIN2, SWIN2,CIN2, SBRIN2,SBLIN2	Input pin of L/R/C/SW/SL/SR/SBL/SBR channel (Multi IN 1/2)
73,74, 75,76, 77,78, 79,80	FLIN1, FRIN1, CIN1,SWIN1, SLIN1,SRIN1, SBLIN1,SBRIN1	
41	DGND	Digital ground of internal circuit
42	DATA	Input pin of control data
43	CLOCK	Input pin of control clock
44	AVEE	Negative power supply to internal circuit
46,48,50, 52,54,56, 58,60,64	INL1,INL2, INL3, INL4,INL5,INL6, INL7,INL8,INL9	Input pin of L/R channel (Input Selector)
45,47,49, 51,53,55, 57,59,63	INR1,INR2, INR3, INR4,INR5,INR6, INR7,INR8,INR9	
40	MONO	Input pin of monaural (Input Selector)
38,39	SUBL,SUBR	Output pin for L/R channel SUB Output
36,37	ADCL, ADCR	Output pin for L/R channel ADC
72	RECL3	Output pin for L/R channel REC Output
71	RECR3	
61,62, 65,66, 67,68, 69,70	INRA/RECR1,INLA/RECL1, INRB/RECR2,INLB/RECL2, INR10/RECR4,INL10/RECL4, INR11/RECR5,INL11/RECL5	Input pin of L/R channel (Input Selector)/ Output pin for L/R channel REC Output

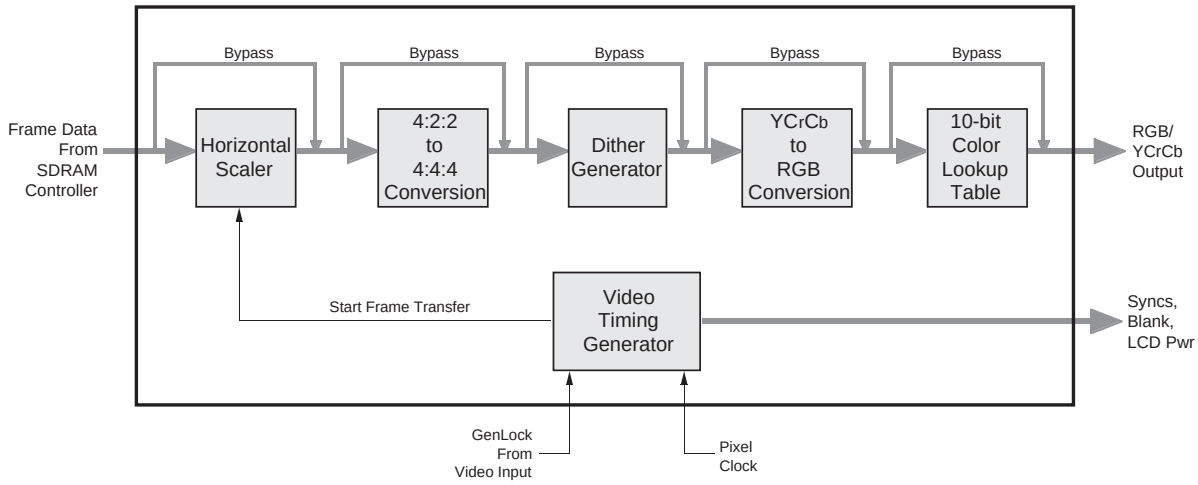
IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -30

Q8001 : SII504 (I/P Video Converter)

BLOCK DIAGRAM



Video Output Section BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -31

Q8001 : SII504 (I/P Video Converter)

TERMINAL DESCRIPTION (1/5)

Signal Group	Signal Name	Notes	Type	Description
Video Input	VidInData[9:2]	5V	In	Multiplexed Video Input Data (ITU-R BT.656, 8-bit & H/V syncs formats); Y (luma) Video Input Data (16-bit & H/V syncs format).
	VidInData[19:12] (HostData[15:8])	5V/PD	In	Chroma Video Input Data (16-bit & H/V syncs format only). See Host Interface pin list for pin functions when not used for video input.
	VS (HostData[7])	5V/PD	In	Vertical Sync input (8/16-bit & H/V syncs format only). See Host Interface pin list for pin function when not used for video input.
	HS (HostData[6])	5V/PD	In	Horizontal Sync input (8/16-bit & H/V syncs format only). See Host Interface pin list for pin function when not used for video input.
	VidInClk	5V	In	Video Input Clock, 27.0 MHz
Video Output	Red_Cr[9:0]		Out	Red Data (RGB output mode); Cr Data (YCrCb output mode)
	Green_Y[9:0]		Out	Green Data (RGB output mode); Y Data (YCrCb output mode)
	Blue_Cb[9:0]		Out	Blue Data (RGB output mode); Cb Data (YCrCb output mode)
	/HSync		Out	Horizontal Sync
	/VSync		Out	Vertical Sync
	/CSync		Out	Composite Sync
	/CBlank		Out	Composite Blank
	LCDPwrEn		Out	LCD Power Enable
	VidOutClk		Out	Video Output Clock, 36, 27 or 24 MHz
	Clk48M	5V	InOut	48 MHz Clock. Normally, this pin is a no-connect, outputting an internal PLL-generated 48.0 MHz clock and receiving that same clock through its input buffer. To bypass the PLL, set /BypPLLClk48M = 0, and supply a 48.0 MHz clock to the Clk48M pin.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -32

Q8001 : SII504 (I/P Video Converter)

TERMINAL DESCRIPTION (2/5)

Signal Group	Signal Name	Notes	Type	Description
Video Output (continued)	/BypPLLClk48M	PU	In	Bypass PLL for Clk48M. Normally, this pin is a no-connect, and the internal pullup ensures that the PLL is enabled. To bypass the PLL, set /BypPLLClk48M = 0, and supply a 48.0 MHz clock to the Clk48M pin.
	Clk54_72M	5V	InOut	54 or 72 MHz Clock. Normally, this pin is a no-connect, outputting an internal PLL-generated 54.0 MHz or 72.0 MHz clock and receiving that same clock through its input buffer. To bypass the PLL, set /BypPLLClk54_72M = 0, and supply a 54.0 or 72.0 MHz clock to the Clk54_72M pin. -
	/BypPLLClk54_72M	5V/PU	In	Bypass PLL for Clk54_72M. Normally, this pin is a no-connect, and the internal pullup ensures that the PLL is enabled. To bypass the PLL, set /BypPLLClk54_72M = 0, and supply a 54.0 MHz or 72.0 MHz clock to the Clk54_72M pin.
Audio/Video Synchronization	SDIn	5V/PD	In	Serial Digital Audio Input Data. See Audio/ Video Synchronization section of Functional Description for audio formats supported.
	WSIn	5V/PD	In	Serial Digital Audio Input Word Select. See Audio/Video Synchronization section for audio formats supported.
	SCKIn	5V/PD	In	Serial Digital Audio Input Clock. Frequency range of clock is 1.411 to 6.144 MHz. See Audio/Video Synchronization section for audio formats supported.
	SDOut		Out	Serial Digital Audio Output Data. Audio output follows audio input, with a delay equal to that of the video processing pipeline.
	WSOut		Out	Serial Digital Audio Output Word Select. Audio output follows audio input, with a delay equal to that of the video processing pipeline.
	SCKOut	5V/PD	In	Serial Digital Audio Output Clock. Same frequency as SCKIn. SDOut and WSOut are generated from SCKOut. See Audio/Video Synchronization section for more details on on audio clocking.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -33

Q8001 : SII504 (I/P Video Converter)

TERMINAL DESCRIPTION (3/5)

Signal Group	Signal Name	Notes	Type	Description
Memory	/RAS		Out	SDRAM Row Address Strobe.
	/CAS		Out	SDRAM Column Address Strobe.
	/WE		Out	SDRAM Write Enable.
	DQM		Out	SDRAM Data Mask.
	MemData[31:0]	5V	InOut	SDRAM Data.
	MemAddr[12:0]	5V/PU/PD	InOut	SDRAM Address when an output. Configuration at reset when and input. See Memory Subsystem an Hardware Configuration sections of Functional Description for details. (Note: MemAddr12 is an output-only pin, does not have an internal pullup or pulldown, and is not part of the startup configuration.)
	MemClk	5V	InOut	SDRAM Clock. Normally, this pin is an InOut, outputting an internal PLL-generated 66.0 MHz or 72.0 MHz clock to the SDRAM and receiving that same clock through its input buffer. To bypass the PLL, set /BypPLLMemClk = 0, and supply a 66.0 MHz or 72.0 MHz clock to MemClk.
	/BypPLLMemClk	5V/PU	In	Bypass PLL for MemClk. Normally, this pin is a no-connect, and the internal pullup ensures that the PLL is enabled. To bypass the PLL, set /BypPLLMemClk = 0, and suppy a 66.0 MHz or 72.0 MHz clock to the MemClk pin
Host Interface	/HostWr_SCL	5V/H	In	186-Compatible Write when HostMode = 0. Serial Clock when HostMode = 1.
	/HostRd_SDA	5V/H	InOut	186-Compatible Read when HostMode = 0. Serial Data (InOut, open drain output) when HostMode = 1.
	/HostCS	5V/PU	In	186-Compatible Chip Select when HostMode=0. When HostMode=1, must be tied to VDD or pulled up to VDD.
	HostAddr[7:0]	5V/PD	In	186-Compatible Address when HostMode = 0. No connect when HostMode = 1.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -34

Q8001 : SII504 (I/P Video Converter)

TERMINAL DESCRIPTION (4/5)

Signal Group	Signal Name	Notes	Type	Description
Host Interface (continued)	HostData[15:8] (VidInData[19:2])	5V/PD	InOut	186-Compatible Data when HostMode = 0. Chroma video input data (16-bit & H/V syncs format) when HostMode = 1.
	HostData[7] (VS)	5V/PD	InOut	186-Compatible Data when HostMode = 0. Vertical sync input (8/16-bit & H/V syncs format) when HostMode = 1.
	HostData[6] (HS)	5V/PD	InOut	186-Compatible Data when HostMode = 0. Horizontal sync input (8/16-bit & H/V syncs format) when HostMode = 1.
	HostData[5:0]	5V/PD	InOut	186-Compatible Data when HostMode = 0. No connnect when HostMode = 1.
	HostClk	5V	InOut	186-Compatible Clock (33.33 MHz max) when HostMode = 0. No Connect (27.0 MHz, InOut) when HostMode = 1. Note that when HostMode= 1, the clock output on HostClk is also received and used internally.
	HostMode	5V/PU	In	Serial Host Interface when HostMode = 1 (internal pullup defaults to this mode). 186-compatible host interface when HostMode = 0.
Video Processing Status	/Det32PD		Out	3:2 Pulldown Sequence Detected.
	/Det22PD		Out	2:2 Pulldown Sequence Detected.
	/DetVideo		Out	Interlaced Video Sequence Detected.
	/DeintDone		Out	Deinterlace processing complete for current field period. Opendrain output.
External APLL Reference Clock	/ExtRefSel	5V/PU	In	External APLL Reference Select. Internal pullup defaults pin to a 1, selecting VidInClk as the APLL reference clock. To select ExtRefXtalIn as the APLL reference clock, set /ExtRefSel to a 0.
	ExtRefXtalIn		In	External APLL Reference Crystal/oscillator Input.
	ExtRefXtalOut		Out	External APLL Reference Crystal Output.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -35

Q8001 : SII504 (I/P Video Converter)

TERMINAL DESCRIPTION (5/5)

Signal Group	Signal Name	Notes	Type	Description
Reset	/Reset	5V/H	In	Hardware Reset.
Test	Test[1:0]	5V/PD	In	Production hardware test support.
	PuPdDis	5V	In	Internal pullup and pulldown disable test function. Connect to ground for normal operation.
Power	AVDD		Pwr	1.8V Analog Power for PLL. (Qty: 1)
	ARTN		Pwr	Analog Return for PLLs. (Qty: 1)
	VDDCore		Pwr	1.8V Core Power. (Qty: 11)
	GNDCore		Pwr	Digital Ground for Core Power. (Qty: 12)
	VDDIO		Pwr	3.3V I/O Power. (Qty: 11)
	GNDIO		Pwr	Digital Ground for I/O Power. (Qty: 18)

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -36

Q8001 : SII504 (I/P Video Converter)

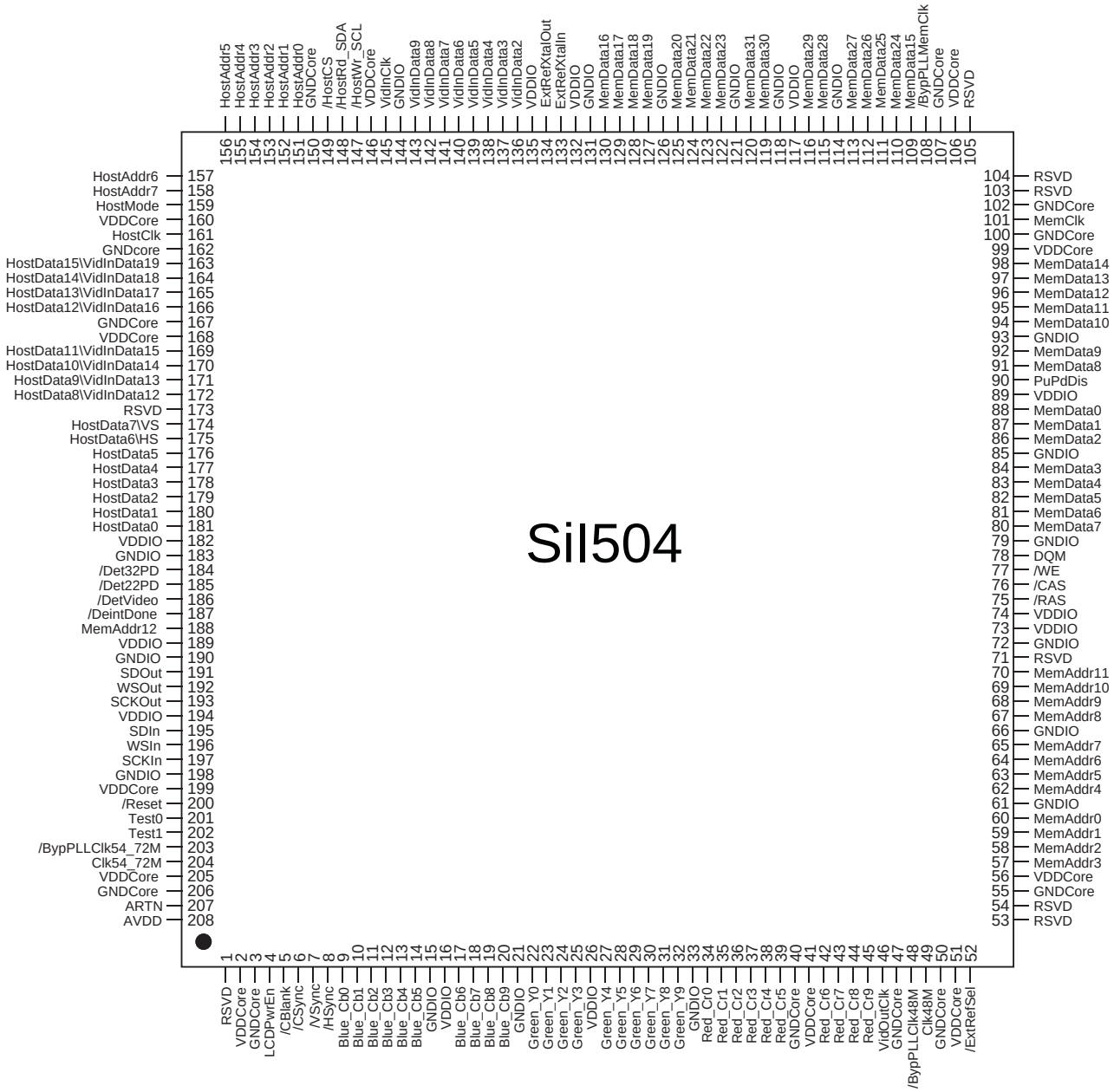
PIN NUMBER

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	Reserved	53	Reserved	105	Reserved	157	HostAddr6
2	VDDCore	54	Reserved	106	VDDCore	158	HostAddr7
3	GNDCore	55	GNDCore	107	GNDCore	159	HostMode
4	LCDPwrEn	56	VDDCore	108	/BypPLLMemClk	160	VDDCore
5	/CBlank	57	MemAddr3	109	MemData15	161	HostClk
6	/CSync	58	MemAddr2	110	MemData24	162	GNDCore
7	/VSync	59	MemAddr1	111	MemData25	163	HostData15\VidInData19
8	/HSync	60	MemAddr0	112	MemData26	164	HostData14\VidInData18
9	Blue_Cb0	61	GNDIO	113	MemData27	165	HostData13\VidInData17
10	Blue_Cb1	62	MemAddr4	114	GNDIO	166	HostData12\VidInData16
11	Blue_Cb2	63	MemAddr5	115	MemData28	167	GNDCore
12	Blue_Cb3	64	MemAddr6	116	MemData29	168	VDDCore
13	Blue_Cb4	65	MemAddr7	117	VDDIO	169	HostData11\VidInData15
14	Blue_Cb5	66	GNDIO	118	GNDIO	170	HostData10\VidInData14
15	GNDIO	67	MemAddr8	119	MemData30	171	HostData9\VidInData13
16	VDDIO	68	MemAddr9	120	MemData31	172	HostData8\VidInData12
17	Blue_Cb6	69	MemAddr10	121	GNDIO	173	Reserved
18	Blue_Cb7	70	MemAddr11	122	MemData23	174	HostData7\VS
19	Blue_Cb8	71	Reserved	123	MemData22	175	HostData6\HS
20	Blue_Cb9	72	GNDIO	124	MemData21	176	HostData5
21	GNDIO	73	VDDIO	125	MemData20	177	HostData4
22	Green_Y0	74	VDDIO	126	GNDIO	178	HostData3
23	Green_Y1	75	/RAS	127	MemData19	179	HostData2
24	Green_Y2	76	/CAS	128	MemData18	180	HostData1
25	Green_Y3	77	/WE	129	MemData17	181	HostData0
26	VDDIO	78	DQM	130	MemData16	182	VDDIO
27	Green_Y4	79	GNDIO	131	GNDIO	183	GNDIO
28	Green_Y5	80	MemData7	132	VDDIO	184	/Det32PD
29	Green_Y6	81	MemData6	133	ExtRefXtalIn	185	/Det22PD
30	Green_Y7	82	MemData5	134	ExtRefXtalOut	186	/DetVideo
31	Green_Y8	83	MemData4	135	VDDIO	187	/DeintDone
32	Green_Y9	84	MemData3	136	VidInData2	188	MemAddr12
33	GNDIO	85	GNDIO	137	VidInData3	189	VDDIO
34	Red_Cr0	86	MemData2	138	VidInData4	190	GNDIO
35	Red_Cr1	87	MemData1	139	VidInData5	191	SDOut
36	Red_Cr2	88	MemData0	140	VidInData6	192	WSOut
37	Red_Cr3	89	VDDIO	141	VidInData7	193	SCKOut
38	Red_Cr4	90	PuPdDis	142	VidInData8	194	VDDIO
39	Red_Cr5	91	MemData8	143	VidInData9	195	SDIn
40	GNDCore	92	MemData9	144	GNDIO	196	WSIn
41	VDDCore	93	GNDIO	145	VidInClk	197	SCKIn
42	Red_Cr6	94	MemData10	146	VDDCore	198	GNDIO
43	Red_Cr7	95	MemData11	147	/HostWr_SCL	199	VDDCore
44	Red_Cr8	96	MemData12	148	/HostRd_SDA	200	/Reset
45	Red_Cr9	97	MemData13	149	/HostCS	201	Test0
46	VidOutClk	98	MemData14	150	GNDCore	202	Test1
47	GNDCore	99	VDDCore	151	HostAddr0	203	/BypPLLClk54_72M
48	/BypPLLClk48M	100	GNDCore	152	HostAddr1	204	Clk54_72M
49	Clk48M	101	MemClk	153	HostAddr2	205	VDDCore
50	GNDCore	102	GNDCore	154	HostAddr3	206	GNDCore
51	VDDCore	103	Reserved	155	HostAddr4	207	ARTN
52	/ExtRefSel	104	Reserved	156	HostAddr5	208	AVDD

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -37

Q8001 : SII504 (I/P Video Converter)

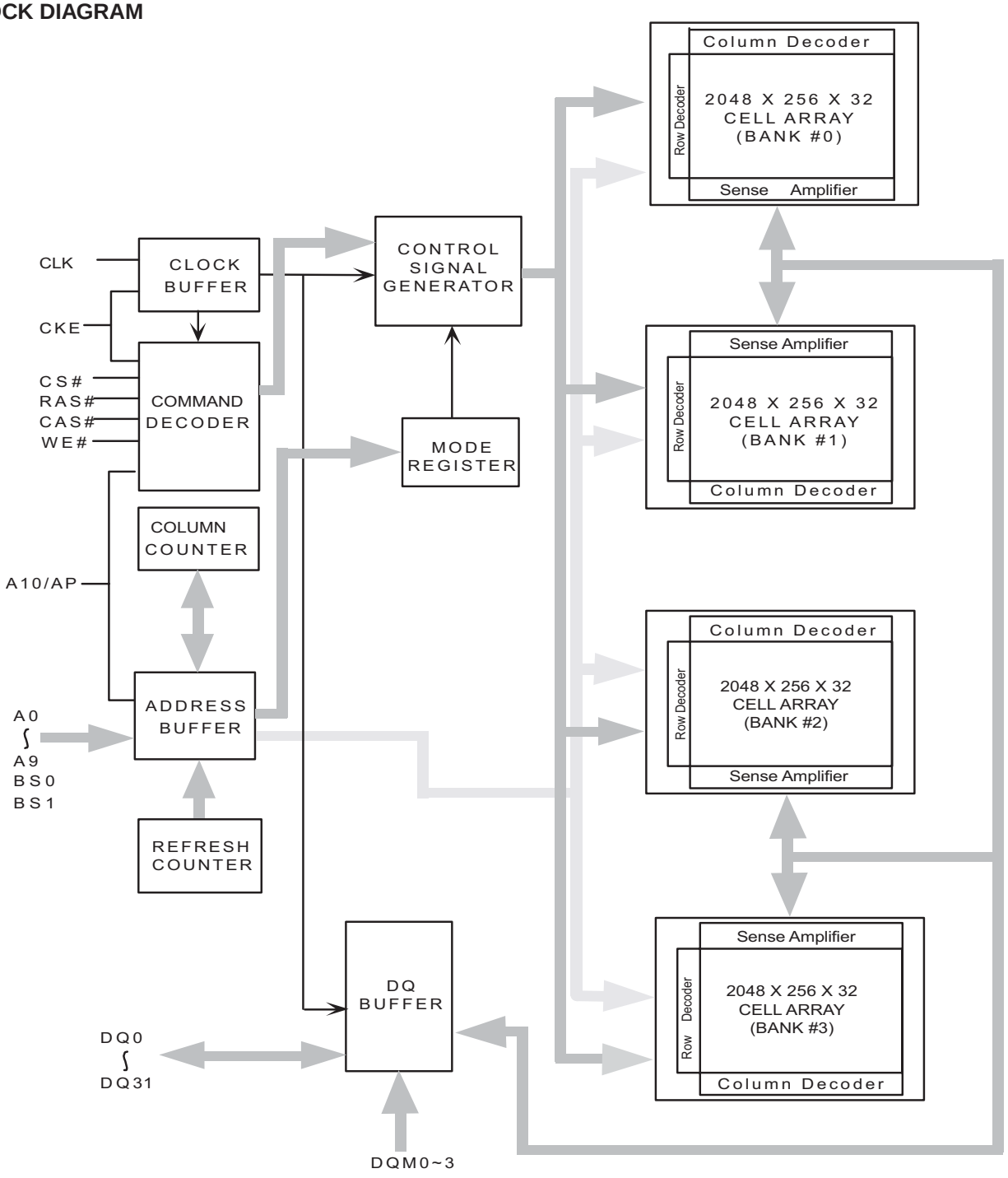
PIN CONFIGURATION



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -38

Q8003: IC42S3200L (64-Mbit Synchronous Dynamic RAM)

BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -39

Q8003: IC42S3200L (64-Mbit Synchronous Dynamic RAM)

TERMINAL DESCRIPTION (1/2)

Symbol	Type	Description
CLK	**Input**	**Clock:**CLK is driven by the system clock.All SDRAM input signals are sampled on the positive edge of CLK.CLK also increments the internal burst counter and controls the output registers.
CKE	**Input**	**Clock Enable:**CKE activates(HIGH)and deactivates(LOW)the CLK signal.If CKE goes low synchronously with clock(set-up and hold time same as other inputs),the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low.When all banks are in the idle state,deactivating the clock controls the entry to the Power Down and Self Refresh modes.CKE is synchronous except after the device enters Power Down and Self Refresh modes,where CKE becomes asynchronous until exiting the same mode. The input buffers,including CLK,are disabled during Power Down and Self Refresh modes,providing low standby power.
BS0,BS1	**Input**	**Bank Select:**BS0 and BS1 defines to which bank the BankActivate,Read,Write,or BankPrecharge command is being applied.
A0-A10	**Input**	**Address Inputs:**A0-A10 are sampled during the BankActivate command (row address A0-A10)and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 256K available in the respective bank.During a Precharge command,A10 is sampled to determine if all banks are to be precharged (A10 =HIGH). The address inputs also provide the op-code during a Mode Register Set .
CS#	**Input**	**Chip Select:**CS#enables (sampled LOW)and disables (sampled HIGH)the command decoder.All commands are masked when CS#is sampled HIGH.CS#provides for external bank selection on systems with multiple banks.It is considered part of the command code.
RAS#	**Input**	**Row Address Strobe:**The RAS#signal defines the operation commands in conjunction with the CAS#and WE#signals and is latched at the positive edges of CLK.When RAS# and CS#are asserted “LOW”and CAS#is asserted “HIGH,”either the BankActivate command or the Precharge command is selected by the WE#signal.When the WE#is asserted “HIGH,”the BankActivate command is selected and the bank designated by BS is turned on to the active state.When the WE#is asserted “LOW,”the Precharge command is selected and the bank designated by BS is switched to the idle state after the precharge operation.
CAS#	**Input**	**Column Address Strobe:**The CAS#signal defines the operation commands in conjunction with the RAS#and WE#signals and is latched at the positive edges of CLK. When RAS#is held “HIGH”and CS#is asserted “LOW,”the column access is started by asserting CAS#”LOW.”Then,the Read or Write command is selected by asserting WE# “LOW”or “HIGH.”
WE#	**Input**	**Write Enable:**The WE#signal defines the operation commands in conjunction with the RAS#and CAS#signals and is latched at the positive edges of CLK.The WE#input is used to select the BankActivate or Precharge command and Read or Write command.
DQM0-3	**Input**	**Data Input/Output Mask:**DQM0-DQM3 are byte specific,nonpersistent I/O buffer controls. The I/O buffers are placed in a high-z state when DQM is sampled HIGH.Input data is masked when DQM is sampled HIGH during a write cycle.Output data is masked (two-clock latency)when DQM is sampled HIGH during a read cycle.DQM3 masks DQ31-DQ24,DQM2 masks DQ23-DQ16,DQM1 masks DQ15-DQ8,and DQM0 masks DQ7-DQ0.
DQ0-31	**Input/Output**	**Data I/O:**The DQ0-31 input and output data are synchronized with the positive edges of CLK.The I/Os are byte-maskable during Reads and Writes.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -40

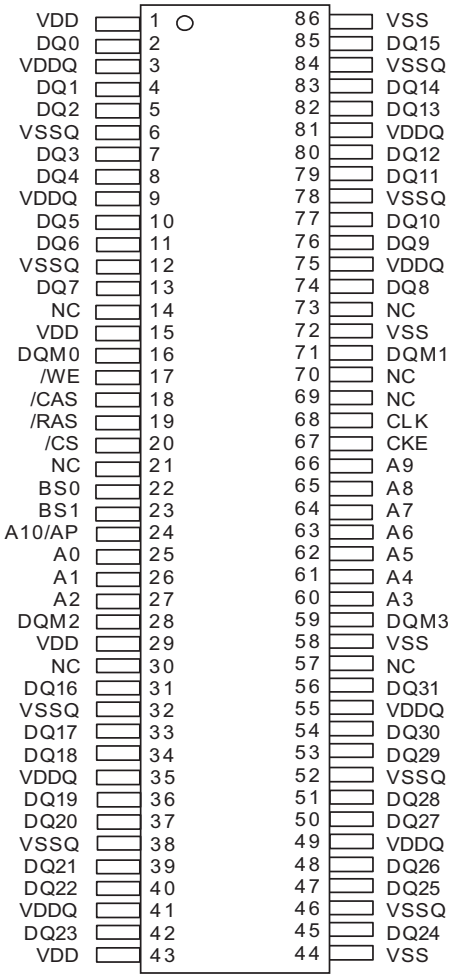
Q8003: IC42S3200L (64-Mbit Synchronous Dynamic RAM)

TERMINAL DESCRIPTION (2/2)

NC	**-**	**No Connect:** These pins should be left unconnected.
VDDQ	Supply	**DQ Power:** Provide isolated power to DQs for improved noise immunity.
VSSQ	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity.
VDD	Supply	**Power Supply:** +3.3V ± 0.3V
VSS	Supply	**Ground**

PIN CONFIGURATION

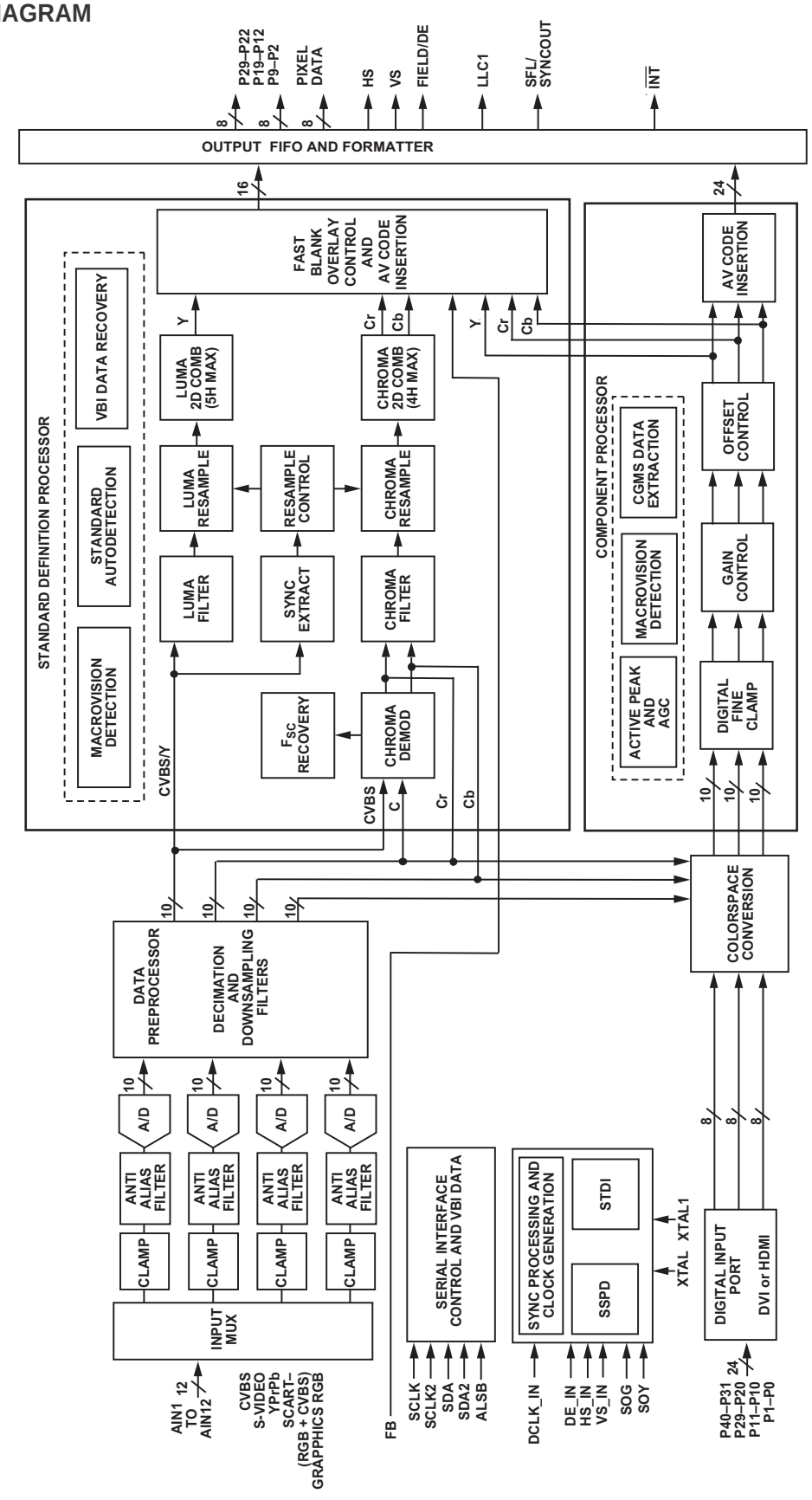
(Top View)



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -41

Q8101: ADV7401 (Multi-Format SDTV/HDTV Video Decoder)

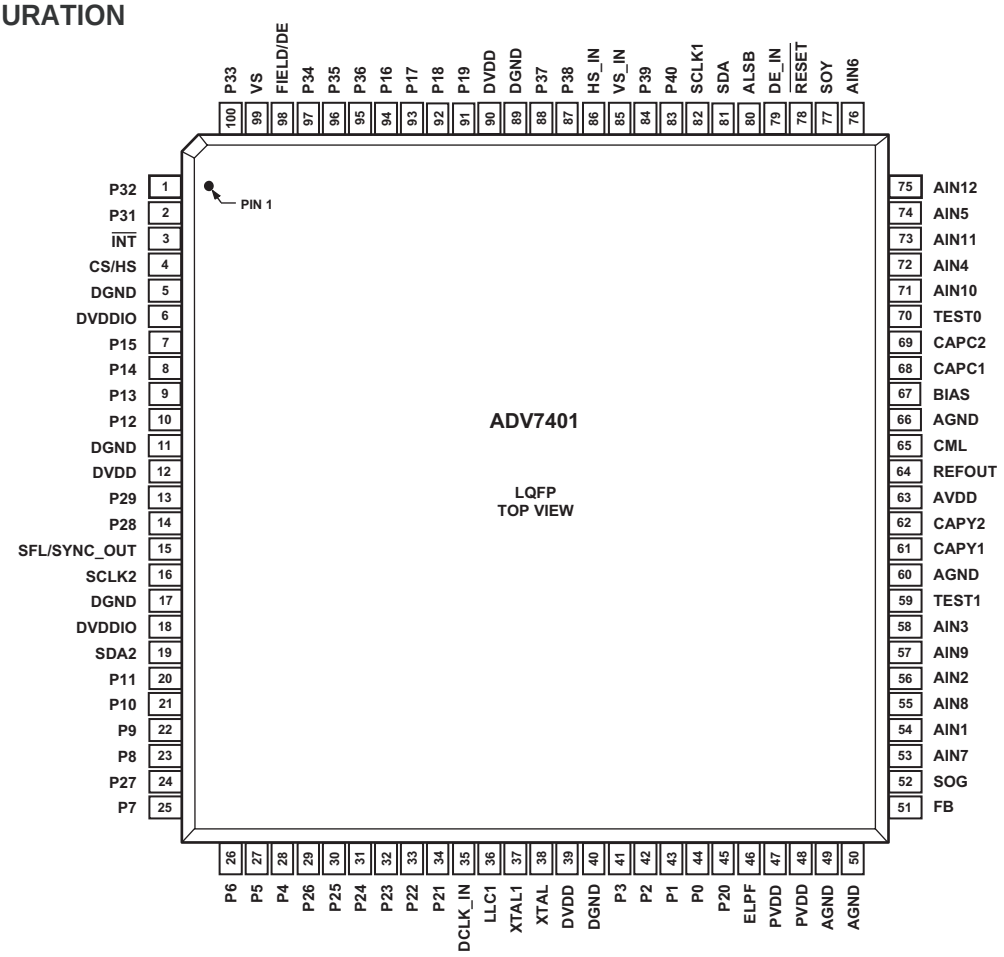
BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -42

Q8101: ADV7401 (Multi-Format SDTV/HDTV Video Decoder)

PIN CONFIGURATION



TERMINAL DESCRIPTION(1/3)

Pin No.	Mnemonic	Type	Function
5, 11, 17, 40, 89	DGND G		Digital ground
49, 50, 60, 66	AGND G		Analog ground
6, 18	DVDDIO	P	Digital I/O supply voltage (3.3 V).
12, 39, 90	DVDD	P	Digital core supply voltage (1.8 V).
63	AVDD	P	Analog supply voltage (3.3 V).
47, 48	PVDD	P	PLL supply voltage (1.8 V).
51	FB	I	FB is a fast switch overlay input that switches between CVBS and RGB analog signals.
54, 56, 58, 72, 74, 76, 53, 55, 57, 71, 73, 75	AIN1–AIN12	I	Analog video input channels.
42, 41, 28, 27, 26, 25, 23, 22, 10, 9, 8, 7, 94, 93, 92, 91	P2–P9, P12–P19	O	Video pixel output port.

IC BLOCK DI AGRAMS AND TERMINAL DESCRIPTIONS -43

Q8101: ADV7401 (Multi-Format SDTV/HDTV Video Decoder)

TERMINAL DESCRIPTION (2/3)

Pin No.	Mnemonic	Type	Function
33, 32, 31, 30, 29, 24, 14, 13	P22-P29 I/O		Video input/output port
44, 43, 21, 20, 45, 34, 2, 1, 100, 97, 96, 95, 88, 87, 84, 83	P0–P1, P10–P11, P20–P21, P31–P40	I	Video pixel input port.
3	$\overline{\text{INT}}$	O	Interrupt pin, can be active low or active high. When SDP/CP status bits change this pin will trigger. The set of events which will trigger an interrupt are under user control.
4	HS/CS	O	HS is a horizontal synchronization output signal in SDP and CP modes. CS is a digital composite synchronization signal that can be selected while in CP mode.
99	VS	O	VS is a vertical synchronization output signal in SDP and CP modes.
98	FIELD/DE	O	FIELD is a field synchronization output signal in all interlaced video modes. This pin also can be enabled as a DE (Data Enable) signal in CP mode to allow direct connection to a HDMI/DVI Tx IC.
81, 19	SDA1, SDA2	I/O	I^2C port serial data input/output pin, SDA1 is the data line for the Control port and SDA2 is the data line for the VBI readback port.
82, 16	SCLK1, SCLK2	I I	^2C port serial clock input (max clock rate of 400 kHz). SCLK1 is the clock line for the Control port and SCLK2 is the clock line for the VBI data readback port.
80	ALSB	I	This pin selects the I^2C address for the ADV7401 Control and VBI readback ports. ALSB set to a logic 0 sets the address for a write to control port of 0x40 and the readback address for the VBI port of 0x21. ALSB set to a logic high sets the address for a write to control port of 0x42 and the readback address for the VBI port of 0x23.
78	$\overline{\text{RESET}}$	I	System reset input, active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7401 circuitry.
36	LLC1	O	LLC1 is a line locked output clock for the pixel data (range is 12.825MHz to 140MHz for ADV7401KSTZ-140; 12.825MHz to 110MHz for ADV7401BSTZ-110; 12.825MHz to 80MHz for ADV7401BSTZ-80).
38	XTAL	I	Input pin for 28.63636 MHz crystal, or can be overdriven by an external 3.3 V 28.63636 MHz clock oscillator source to clock the ADV7401.
37	XTAL1	O	This pin should be connected to the 28.63636 MHz crystal or left as a no connect if an external 3.3 V 28.63636 MHz clock oscillator source is used to clock the ADV7401. In crystal mode the crystal must be a fundamental crystal.
46	ELPF	O	The recommend external loop filter must be connected to this ELPF pin.
70	TEST0		These pins should be left unconnected or alternatively tie to AGND
59	TEST1	O	These pins should be left unconnected

IC BLOCK DI AGRAMS AND TERMINAL DESCRIPTIONS -44

Q8101: ADV7401 (Multi-Format SDTV/HDTV Video Decoder)

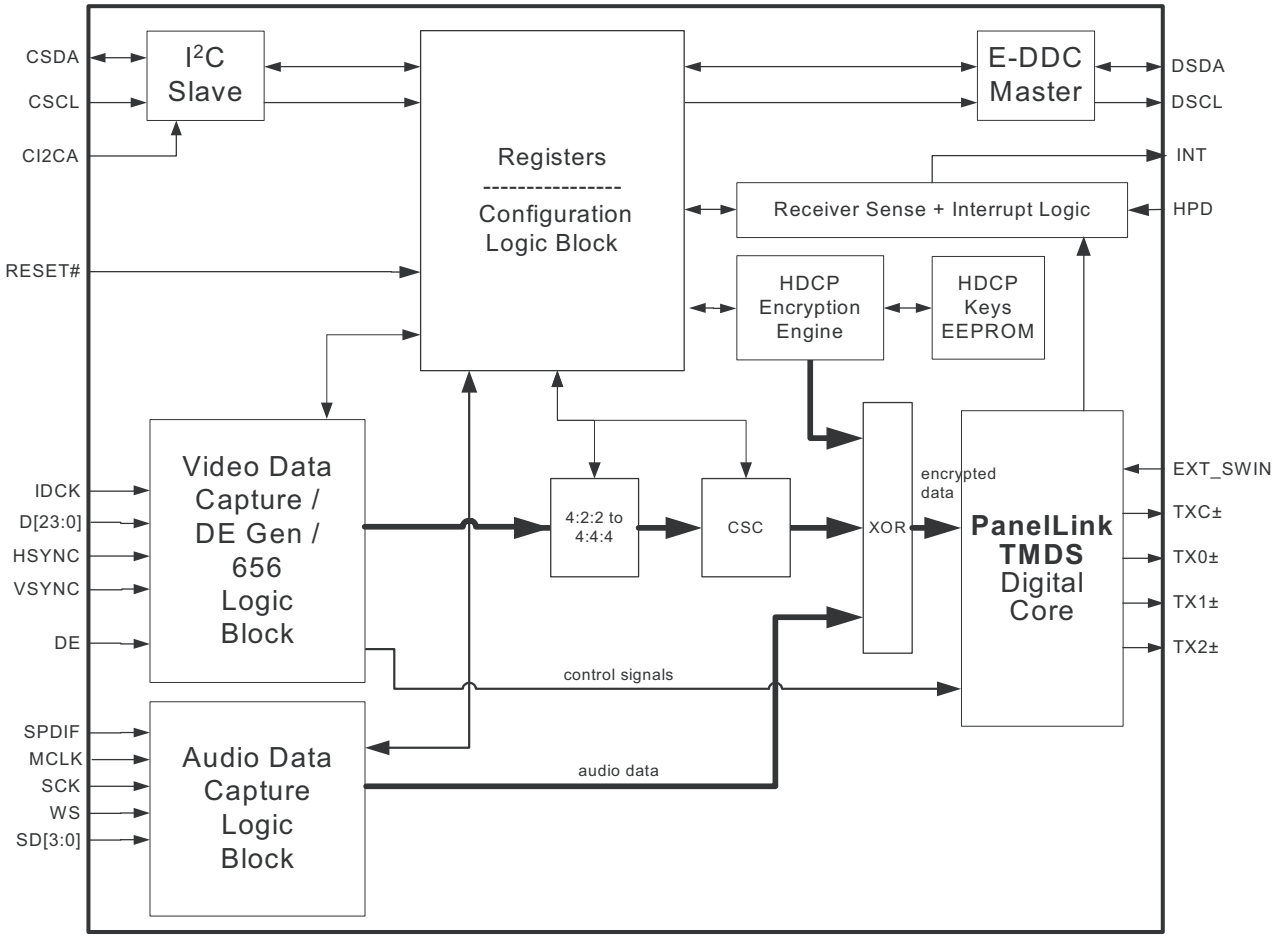
TERMINAL DESCRIPTION (3/3)

Pin No.	Mnemonic	Type	Function
15	SFL/SYNC_ O UT	O	SFL (Subcarrier Frequency Lock); this pin contains a serial output stream which can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder. SYNC_OUT is the sliced sync output signal only available in CP mode.
64	REFOUT	O	Internal voltage reference output.
65	CML	O	The CML pin is a common-mode level for the internal ADCs.
61, 62	CAPY1– CAPY2	I	ADC capacitor network.
68, 69	CAPC1– CAPC2	I	ADC capacitor network.
67	BIAS	O	BIAS is an external bias setting pin. Connect the recommended resistor (1.35k) between pin and ground.
86	HS_IN/CS_IN	I	Can be configured in CP mode to be either a digital HS input signal or a digital CS input signal used to extract timing in a 5-wire or 4-wire RGB mode.
85	VS_IN	I	VS input signal used in CP mode for 5-wire timing mode.
79	DE_IN	I	DE_IN is a data enable input signal used in 24-bit digital input port mode, for example, 24-bit RGB data from a DVI Rx IC.
35	DCLK_IN	I	DCLK_IN is a clock input signal used in 24-bit digital input mode (e.g. 24-bit RGB data from a DVI Rx IC) and also in digital CVBS input mode.
52	SOG	I	SOG is a sync on green input used in embedded sync mode.
77	SOY	I	SOY is a sync on luma input used in embedded sync mode.

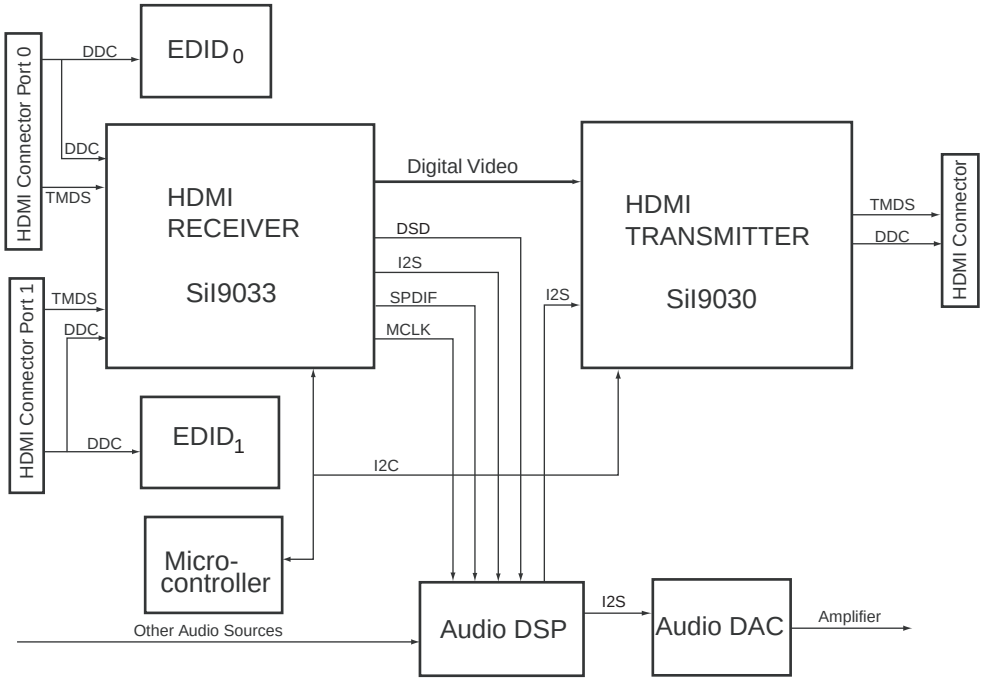
IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -45

Q8401 : SiI9030CTU (HDMI Transmitter)

BLOCK DIAGRAM



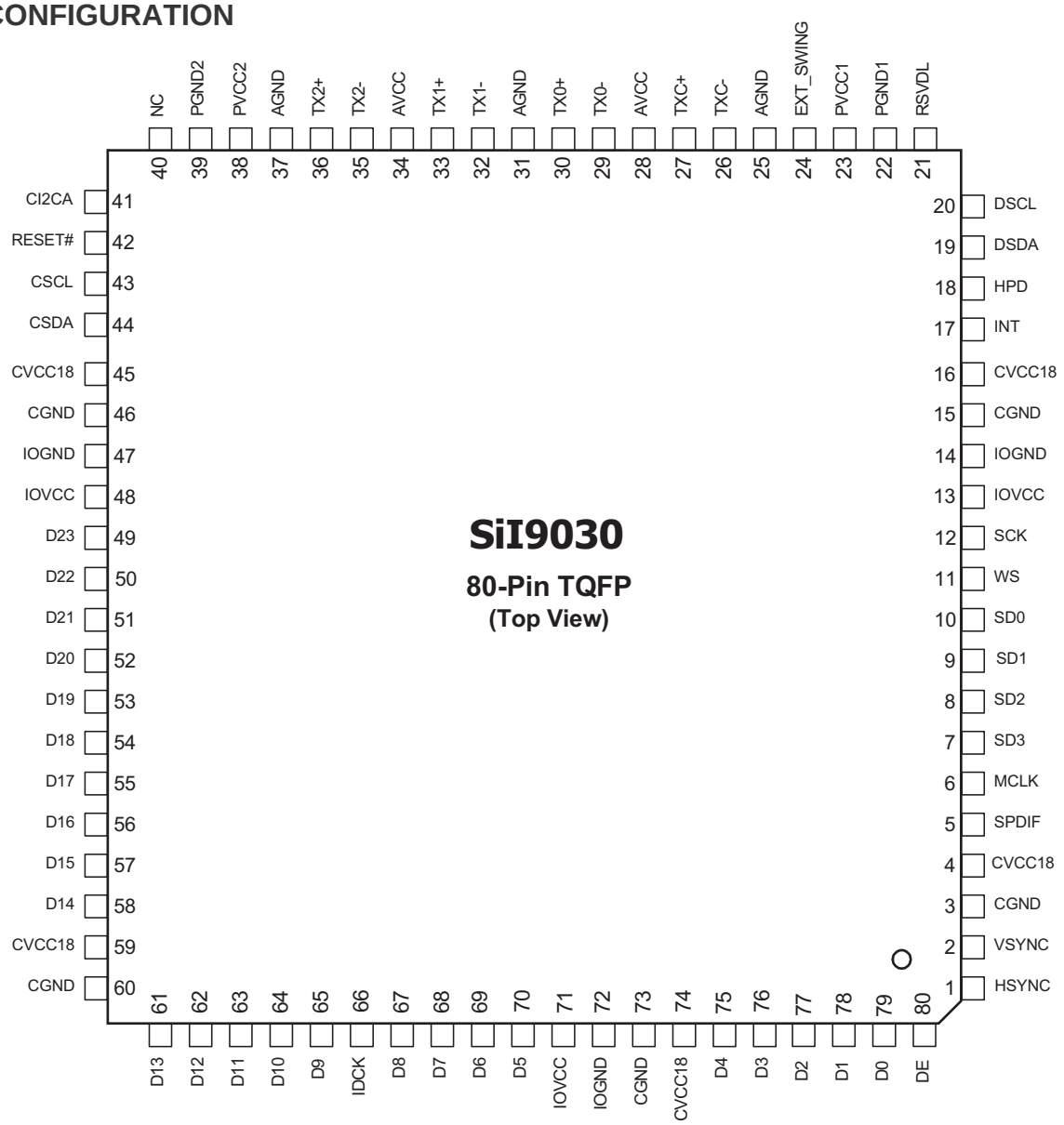
SYSTEM APPLICATION



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -46

Q8401 : SiI9030CTU (HDMI Transmitter)

PIN CONFIGURATION



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -47

Q8401 : SiI9030CTU (HDMI Transmitter)

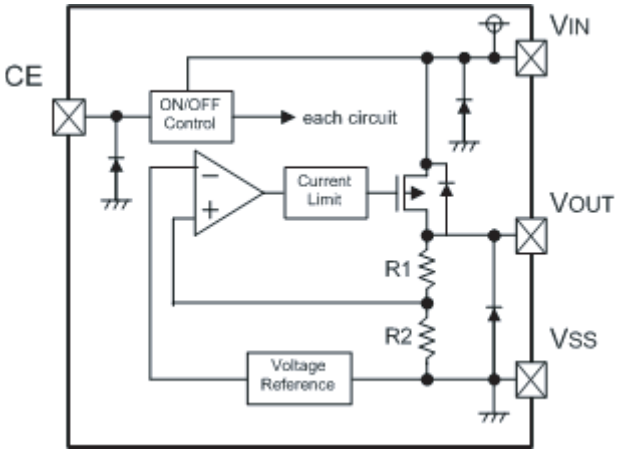
TERMINAL DESCRIPTION

Pin #	Pin Name	I/O	Description	Use
1	HSYNC	I	Horizontal Sync input control signal	Video and Audio
2	VSYNC	I	Vertical Sync input control signal	Video and Audio
3	CGND		Digital core GND.	Ground
4	CVCC18		Digital core VCC. Connect to 1.8V supply.	Power
5	SPDIF	I	S/PDIF Audio input	Video and Audio
6	MCLK	I	Audio Input Master Clock	Video and Audio
7	SD3	I	I2S Serial Data	Video and Audio
8	SD2	I	I2S Serial Data	Video and Audio
9	SD1	I	I2S Serial Data	Video and Audio
10	SD0	I	I2S Serial Data	Video and Audio
11	WS	I	I2S Word Select	Video and Audio
12	SCK	I	I2S Serial Clock	Video and Audio
13	IOVCC		IO Pin VCC. Connect to 3.3V supply.	Power
14	IOGND		IO Pin GND.	Ground
15	CGND		Digital core GND.	Ground
16	CVCC18		Digital core VCC. Connect to 1.8V supply.	Power
17	INT	O	Interrupt Output.	Confirration/Programming
18	HPD	I	Hot Plug Detect Input.	Confirration/Programming
19	DSDA	I/O	DDC data	Control
20	DSCL	I/O	DDC Clock	Control
21	RSVDL	I	Reserved for use by Silicon image, and must be tied LOW.	Confirration/Programming
22	PGND1		TMDS Core PLL Ground.	Ground
23	PVCC1		TMDS Core PLL Power. Connect to 3.3V supply.	Power
24	EXT_SWING	I	Voltage Swing Adjustment. The resistor between AVCC and this pin determines the amplitude of the voltage swing.	Differential signal data
25	AGND		Analog GND.	Ground
26	TXC-	O	TMDS output clock.	Differential signal data
27	TXC+	O		
28	AVCC		Analog VCC. Connect to 3.3Vsupply.	Power
29	TX0-	O	TMDS output data.	Differential signal data
30	TX0+	O		
31	AGND		Analog GND.	Ground
32	TX1-	O	TMDS output data.	Differential signal data
33	TX1+	O		
34	AVCC		Analog VCC. Connect to 3.3Vsupply.	Power
35	TX2-	O	TMDS output data.	Differential signal data
36	TX2+	O		
37	AGND		Analog GND.	Ground
38	PVCC2		Filter PLL Power. Connect to 3.3V supply.	Power
39	PGND2		Filter PLL Ground.	Ground
40	NC		Not connected.	
41	CI2CA	I	I2C device address select	Control
42	RESET	I	Reset Pin. Active LOW	Control
43	CSCL	I	I2C Clock	Control
44	CSDA	I/O	I2C Data	Control
45	CVCC18		Digital core VCC. Connect to 1.8V supply.	Power
46	CGND		Digital core GND.	Ground
47	IOGND		IO Pin GND.	Ground
48	IOVCC		IO Pin VCC. Connect to 3.3V supply.	Power
49	D23	I	12-bit Input Pixel Data Bus. These pins are used in 24-bit mode, single-edge mode.	Video and Audio
50	D22	I		
51	D21	I		
52	D20	I		
53	D19	I		
54	D18	I		
55	D17	I		
56	D16	I		
57	D15	I		
58	D14	I		
59	CVCC18		Digital core VCC. Connect to 1.8V supply.	Power
60	CGND		Digital core GND.	Ground
61	D13	I	12-bit Input Pixel Data Bus. These pins are used in 24-bit mode, single-edge mode.	Video and Audio
62	D12	I		
63	D11	I		
64	D10	I		
65	D9	I		
66	IDCK	I	Input Data Clock	Video and Audio
67	D8	I	12-bit Input Pixel Data Bus. These pins are used in 24-bit mode, single-edge mode.	Video and Audio
68	D7	I		
69	D6	I		
70	D5	I		
71	IOVCC		IO Pin VCC. Connect to 3.3V supply.	Power
72	IOGND		IO Pin GND.	Ground
73	CGND		Digital core GND.	Ground
74	CVCC18		Digital core VCC. Connect to 1.8V supply.	Power
75	D4	I	12-bit Input Pixel Data Bus. These pins are used in 24-bit mode, single-edge mode.	Video and Audio
76	D3	I		
77	D2	I		
78	D1	I		
79	D0	I		
80	DE	I	Data enable	Video and Audio

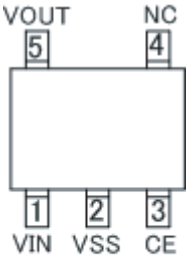
IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -48

Q8404 : XC6213B332MR (Regulator with high-speed ON/OFF switch)

BLOCK DIAGRAM



PIN CONFIGURATION



SOT-25
(TOP VIEW)

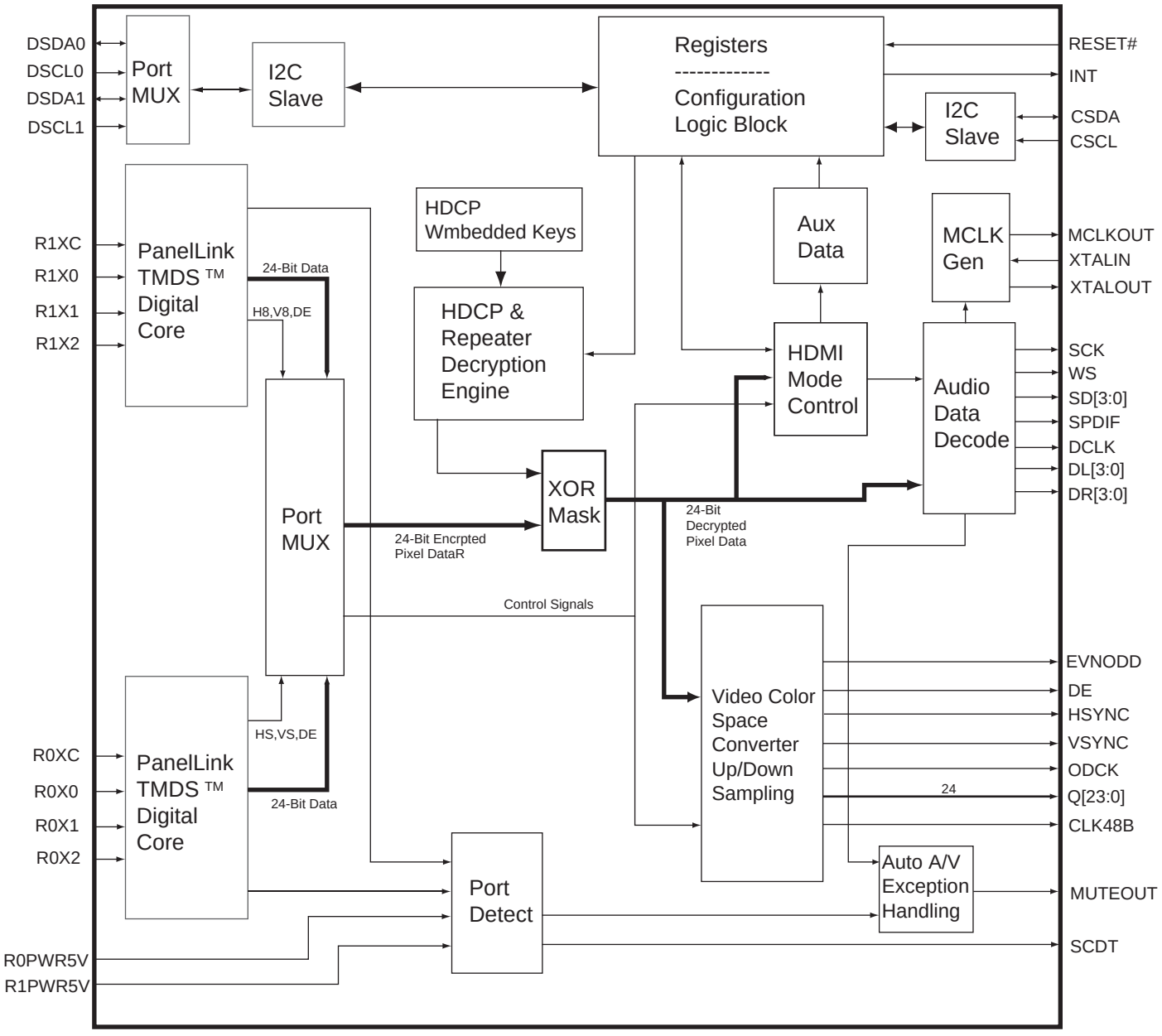
TERMINAL DESCRIPTION

PIN NO	PIN NAME	FUNCTION
1	VIN	INPUT
2	VSS	GND
3	CE	ON/OFF CONTROL PIN
4	NC	NOT USED
5	VOUT	OUTPUT

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -49

Q8501 : SiI9033 (HDMI Receiver)

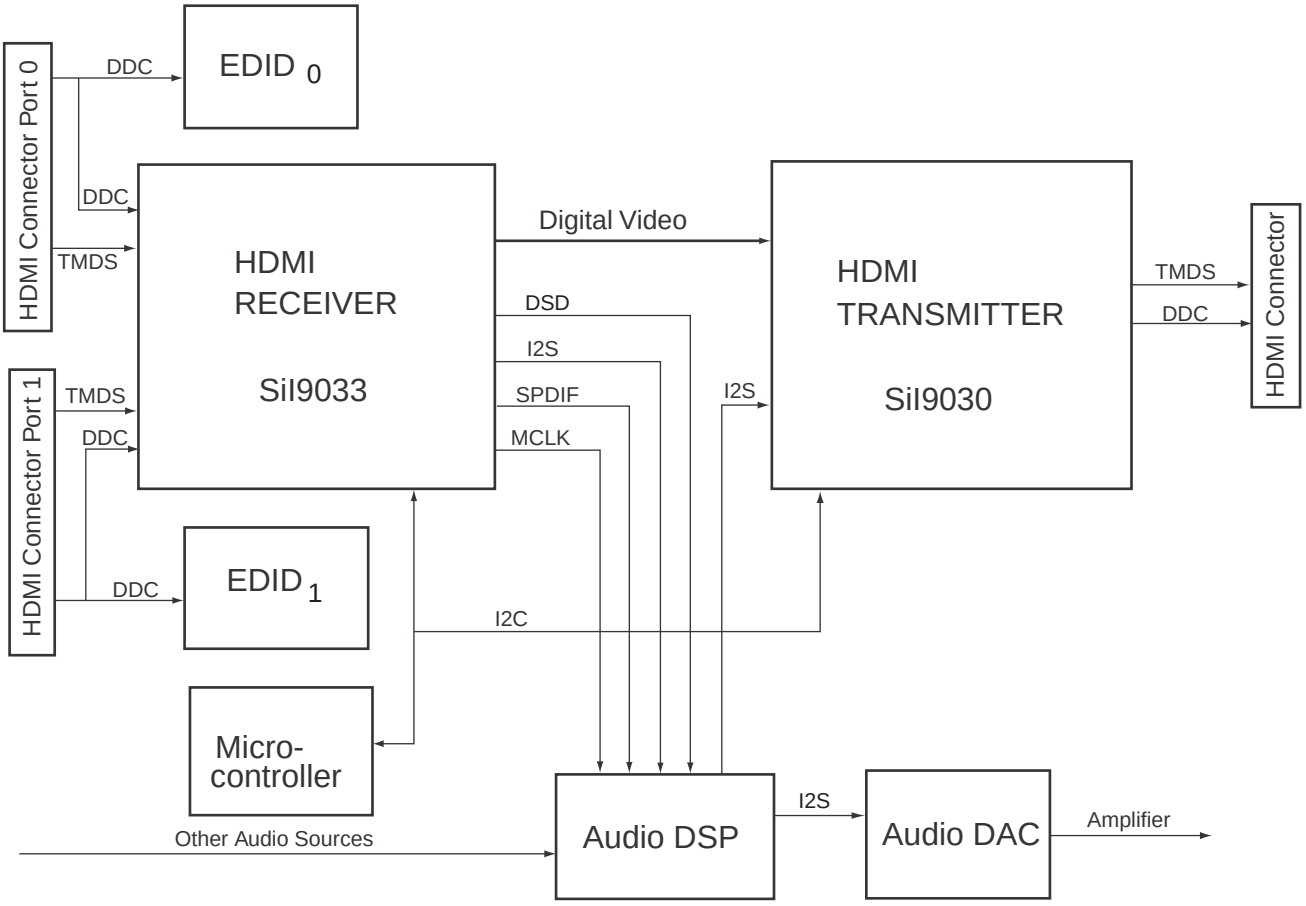
BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -50

Q8501 : SiI9033 (HDMI Receiver)

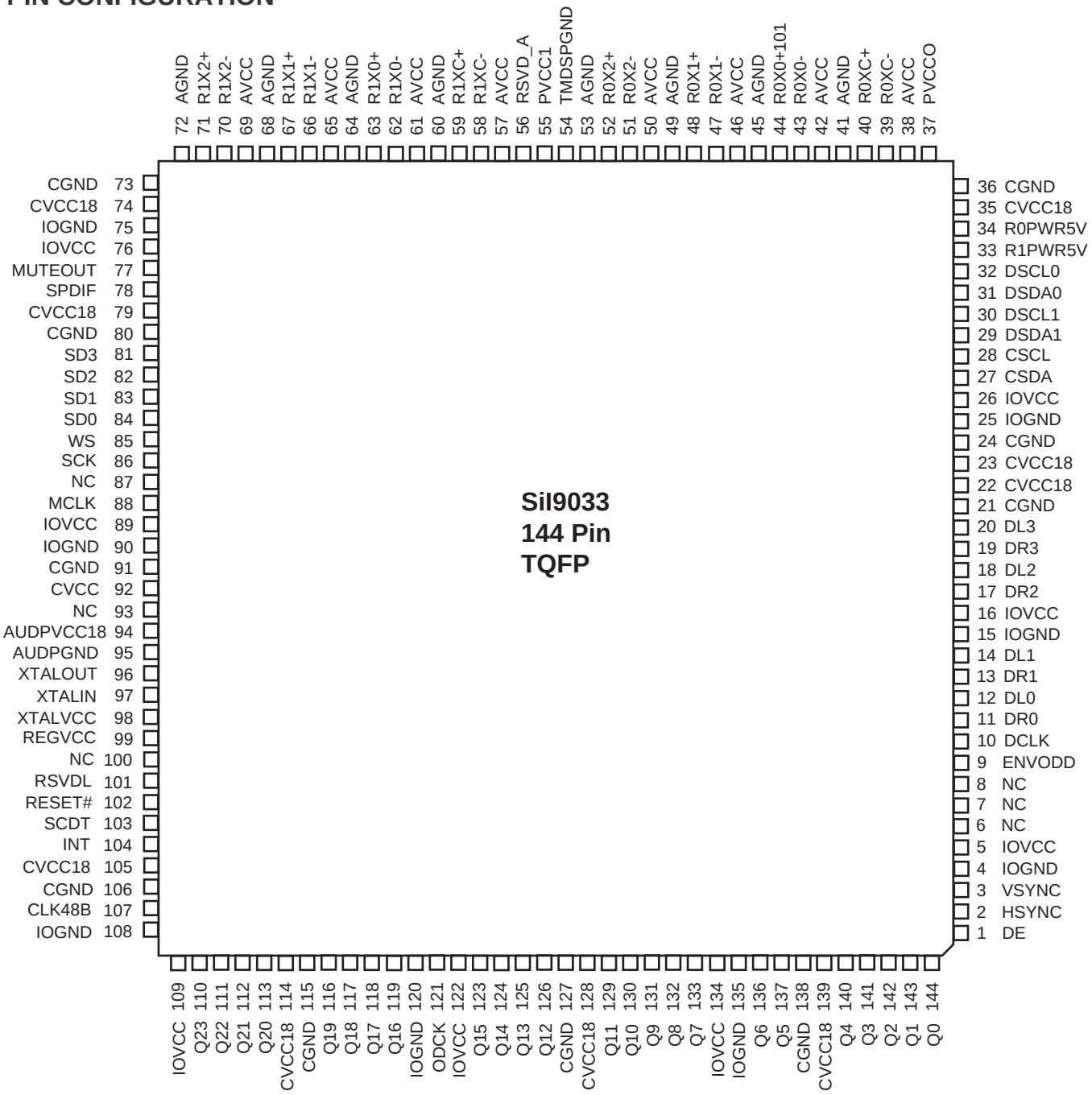
SYSTEM APPLICATION



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -51

Q8501 : SiI9033 (HDMI Receiver)

PIN CONFIGURATION



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -52

Q8501 : SiI9033 (HDMI Receiver)

TERMINAL DESCRIPTION (1/5)

Digital Video Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
Q0	144	8 mA	LVTTL	Output	24-bit Output Pixel Data Bus.
Q1	143		LVTTL	Output	
Q2	142		LVTTL	Output	
Q3	141		LVTTL	Output	
Q4	140		LVTTL	Output	
Q5	137		LVTTL	Output	
Q6	136		LVTTL	Output	
Q7	133		LVTTL	Output	
Q8	132		LVTTL	Output	
Q9	131		LVTTL	Output	
Q10	130		LVTTL	Output	
Q11	129		LVTTL	Output	
Q12	126		LVTTL	Output	
Q13	125		LVTTL	Output	
Q14	124		LVTTL	Output	
Q15	123		LVTTL	Output	
Q16	119		LVTTL	Output	
Q17	118		LVTTL	Output	
Q18	117		LVTTL	Output	
Q19	116		LVTTL	Output	
Q20	113		LVTTL	Output	
Q21	112		LVTTL	Output	
Q22	111		LVTTL	Output	
Q23	110		LVTTL	Output	
DE	1		LVTTL	Output	Data enable.
HSYNC	2		LVTTL	Output	Horizontal Sync Output control signal.
VSYNC	3		LVTTL	Output	Vertical Sync Output control signal.
ODCK	121	12 mA	LVTTL	Output	Output Data Clock.

NOTE

1. HSYNC and VSYNC outputs carry sync signals for both embedded and explicit sync configurations.
2. When transporting video data which uses fewer than 24 bits, the unused bits on the Q[] bus may still carry switching pixel data signals. Unused Q[] bus pins should be unconnected, masked or ignored by downstream devices. For example, carrying YCbCr 4:2:2 data with 16-bit width (see page 50), the bits Q[0] through Q[7] will output switching signals.
3. The output data bus, Q0 to Q23, may be wire-ORed to another device such that one device is always tri-stated. However, the Q0-Q23 pins do not have bus hold internal pull-ups or pull-downs, and so cannot pull the bus when all connected devices are tri-stated.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -53

Q8501 : SiI9033 (HDMI Receiver)

TERMINAL DESCRIPTION (2/5) Digital Audio Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
XTALIN	97	—	LVTTL	In	Crystal Clock Input.
XTALOUT	96	—	LVTTL	Out	Crystal Clock Output.
MCLK	88	8 mA	LVTTL	Out	Audio Master Clock Output.
SCK	86	4 mA	LVTTL	Out	I^2S Serial Clock Output.
WS	85	4 mA	LVTTL	Out	I^2S Word Select Output.
SD0	84	4 mA	LVTTL	Out	I^2S Serial Data Output.
SD1	83	4 mA	LVTTL	Out	
SD2	82	4 mA	LVTTL	Out	
SD3	81	4 mA	LVTTL	Out	
DCLK	10	4 mA	LVTTL	Out	DSD Clock Output
DR0	11	4 mA	LVTTL	Out	DSD Serial Right Channel Data Output
DR1	13	4 mA	LVTTL	Out	
DR2	17	4 mA	LVTTL	Out	
DR3	19	4 mA	LVTTL	Out	
DL0	12	4 mA	LVTTL	Out	DSD Serial Left Channel Data Output
DL1	14	4 mA	LVTTL	Out	
DL2	18	4 mA	LVTTL	Out	
DL3	20	4 mA	LVTTL	Out	
SPDIF	78	4 mA	LVTTL	Out	S/PDIF Audio Output.
MUTEOUT	77	4 mA	LVTTL	Out	Mute Audio Output

NOTE

XTALIN may be driven at LVTTL levels by a clock (leaving XTALOUT unconnected), or connected through a crystal to XTALOUT. Refer to schematic on page 68.

TERMINAL DESCRIPTION (3/5) Configuration/Programming Pins

Pin Name	Pin #	Strength	Type	Dir	Description
INT	104	4 mA	LVTTL[1]	Out	Interrupt Output
RESET#	102	—	Schmitt	In	Reset Pin. Active LOW. 5V Tolerant.
DSCL0	32	—	Schmitt	In	DDC I^2C Clock for Port 0. 5V Tolerant.
DSDA0	31	4 mA	Schmitt	Bi-Di	DDC I^2C Data for Port 0. 5V Tolerant.
DSCL1	30	—	Schmitt	In	DDC I^2C Clock for Port 1. 5V Tolerant.
DSDA1	29	4 mA	Schmitt	Bi-Di	DDC I^2C Data for Port 1. 5V Tolerant.
CSCL	28	—	Schmitt	In	Configuration I^2C Clock. 5V Tolerant.
CSDA	27	4 mA	Schmitt	Bi-Di	Configuration I^2C Data 5V Tolerant.
SCDT	103	12 mA	LVTTL	Out	Indicates active video at HDMI input port.
CLK48B	107	12 mA	LVTTL	Bi-Di	Data Bus Latch Enable.[2]
R0PWR5V	34	—	Schmitt	In	Port 0 Transmitter Detect. 5V Tolerant.
R1PWR5V	33	—	Schmitt	In	Port 1 Transmitter Detect. 5V Tolerant.
RSVDL	101	—	LVTTL	In	Reserved, must be tied LOW.
RSVD_A	56				Reserved Pin, leave unconnected.
NC	6,7,8,87, 93,100		—	—	No internal connection.
EVNODD	9	8 mA	LVTTL	Out	Indicates Even or Odd field for interlaced formats. Polarity programmable in register.

NOTE

The INT pin is programmable as either a push-pull LVTTL output, or as an open-drain output.
CLK48B is used to clock external 24-to-48 bit latches. CLK48B is also latched on the rising edge of RESET# to set the I^2C device addresses for CSCL/CSDA. Refer to Table 11. CLK48B has a weak internal pull-down, and so will be latched as a LOW if not otherwise connected.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -54

Q8501 : SiI9033 (HDMI Receiver)

TERMINAL DESCRIPTION (4/5) Differential Signal Data Pins

Pin Name	Pin #	Type	Description	
R0XC+	40	Analog	TMDS input clock pair.	HDMI Port 0
R0XC-	39	Analog		
R0X0+	44	Analog	TMDS input data pair.	
R0X0-	43	Analog		
R0X1+	48	Analog	TMDS input data pair.	
R0X1-	47	Analog		
R0X2+	52	Analog	TMDS input data pair.	
R0X2-	51	Analog		
R1XC+	59	Analog	TMDS input clock pair.	HDMI Port 1
R1XC-	58	Analog		
R1X0+	63	Analog	TMDS input data pair.	
R1X0-	62	Analog		
R1X1+	67	Analog	TMDS input data pair.	
R1X1-	66	Analog		
R1X2+	71	Analog	TMDS input data pair.	
R1X2-	70	Analog		

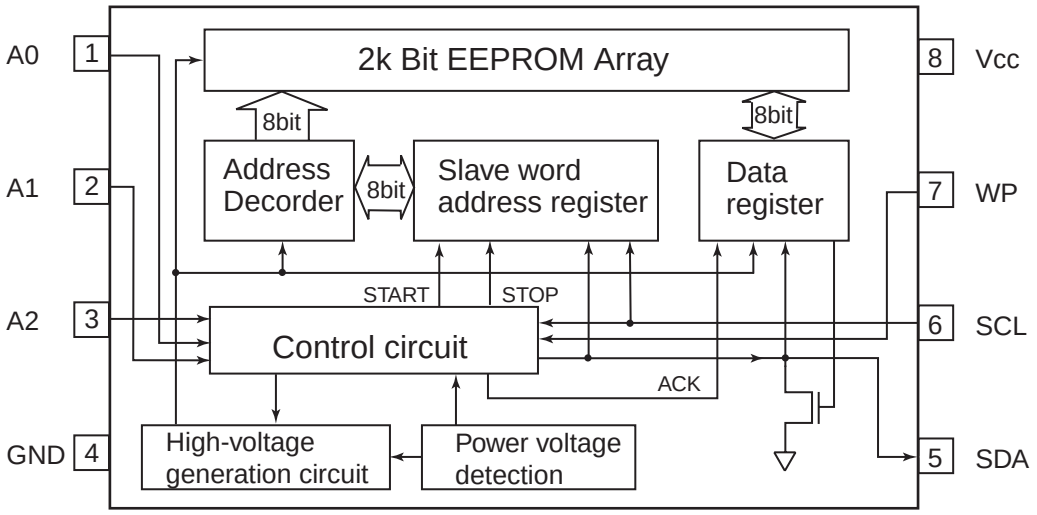
TERMINAL DESCRIPTION (5/5) Power and Ground Pins

Pin Name	Pin #	Type	Description	Supply
CVCC18	22, 23, 35, 74, 79, 92, 105, 114, 128, 139	Power	Digital Logic VCC	1.8V
CGND	21, 24, 36, 73, 80, 91, 106, 115, 127, 138	Ground	Digital Logic GND	
IOVCC	5, 16, 26, 76, 89, 109, 122, 134	Power	Input/Output Pin VCC	3.3V
IOGND	4, 15, 25, 75, 90, 108, 120, 135	Ground	Input/Output Pin GND	
AVCC	38, 42, 46, 50, 57, 61, 65, 69	Power	TMDS Analog VCC	3.3V
AGND	41, 45, 49, 53, 60, 64, 68, 72	Ground	TMDS Analog GND	
PVCC0	37	Power	TMDS Port 0 PLL VCC	3.3V
PVCC1	55	Power	TMDS Port 1 PLL VCC	3.3V
TMDSPGND	54	Ground	TMDS PLL GND	
AUDPVCC18	94	Power	ACR PLL VCC	1.8V
AUDPGND	95	Ground	ACR PLL GND	
XTALVCC	98	Power	ACR PLL Crystal Input VCC	3.3V
REGVCC	99	Power	ACR PLL Regulator VCC	3.3V

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -55

Q8506,Q8606: BR24L02FV-W(256X8 bit EEPROM)

BLOCK DIAGRAM AND PIN CONFIGURATION



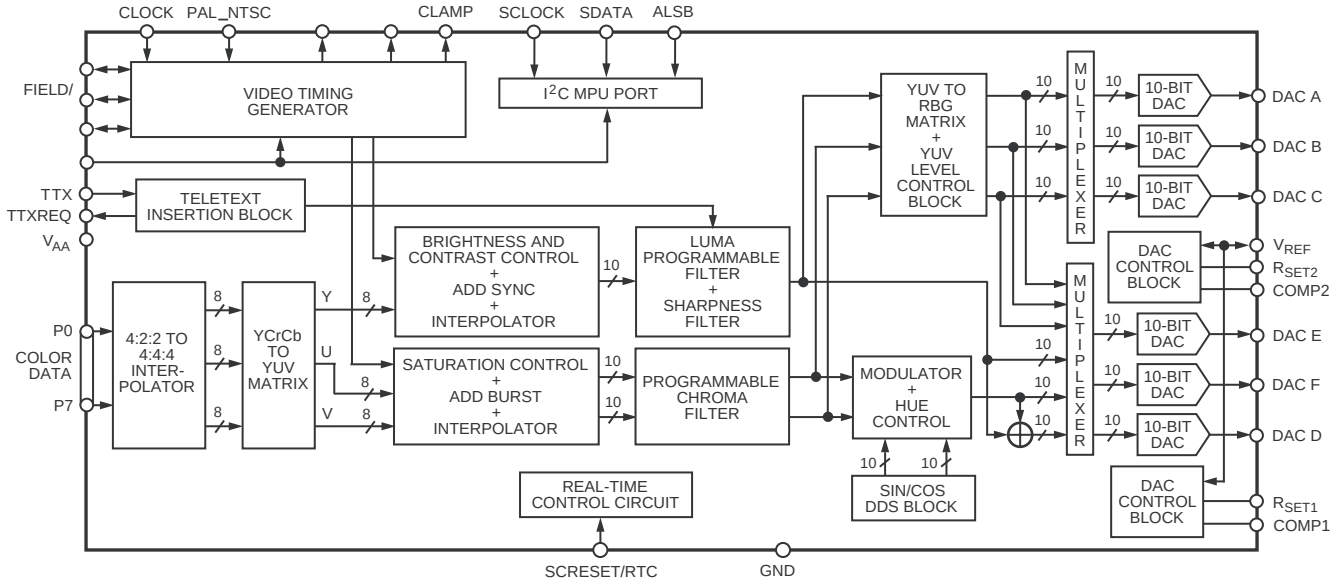
TERMINAL DESCRIPTION

Terminal	I/O	Function
Vcc	-	Apply a power source.
GND	-	Ground terminal
A0,A1,A2	I	Slave address setting terminal
SCL	I	Serial clock input
SDA	I/O	Slave and word address. Serial data input and output
WP	I	Write protect terminal

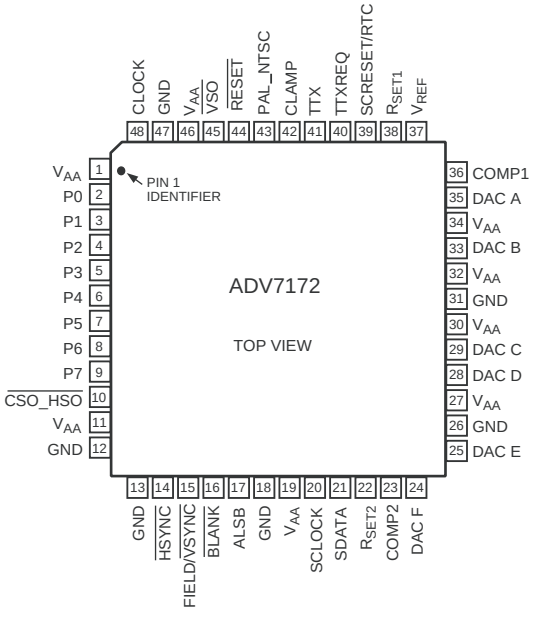
IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -56

Q8801: ADV7172 (Digital PAL/NTSC Video Encoder with six DACs)

BLOCK DIAGRAM



PIN CONFIGURATION



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS -57

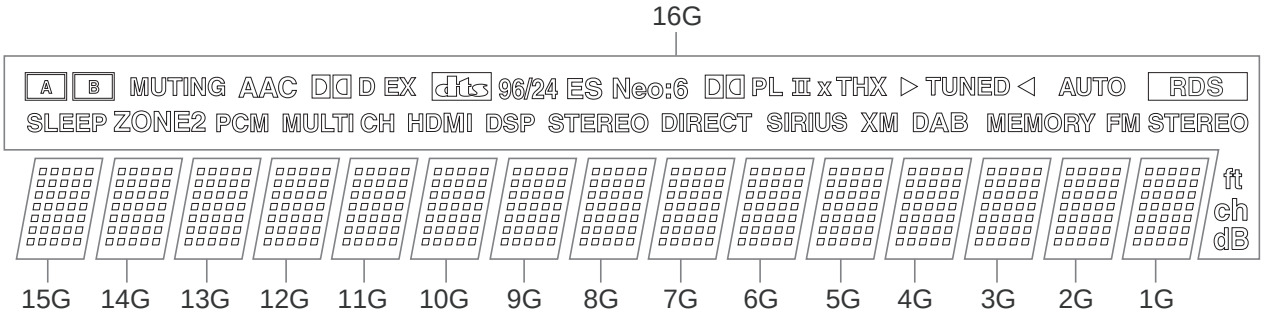
Q8801: ADV7172 (Digital PAL/NTSC Video Encoder with six DACs)

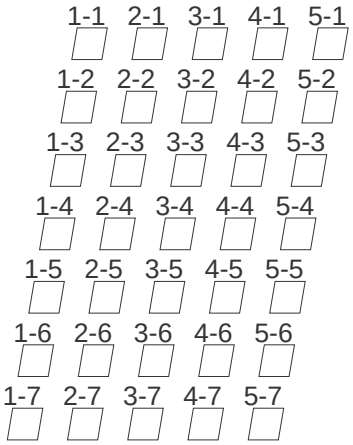
TERMINAL DESCRIPTION

Mnemonic	Input/Output	Function
P7–P0	I	8-Bit 4:2:2 Multiplexed YCrCb Pixel Port (P7ÐP0) P0 represents the LSB.
CLOCK	I	TTL Clock Input. Requires a stable 27 MHz reference clock for standard operation. Alternatively, a 24.5454 MHz (NTSC) or 29.5 MHz (PAL) can be used for square pixel operation.
$\overline{\text{HSYNC}}$	I/O	$\overline{\text{HSYNC}}$ (Modes 1 and 2) Control Signal. This pin may be configured to output (Master Mode) or as an input and accept (Slave Mode) Sync signals.
FIELD/$\overline{\text{VSYNC}}$	I/O	Dual Function FIELD (Mode 1) and $\overline{\text{VSYNC}}$ (Mode 2) Control Signal. This pin may be configured to output (Master Mode) or as an input (Slave Mode) and accept these control signals.
$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. The pixel inputs are ignored when this is Logic Level "0." This signal is optional.
SCRESET/RTC	I	This pin can be configured as an input by setting MR42 and MR41 of Mode Register 4. It can be configured as a subcarrier reset pin, in which case a low-to-high transition on this pin will reset the subcarrier phase to Field 0. Alternatively it may be configured as a Real-Time Control (RTC) Input.
V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
R_{SET1}	I	A 150 resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals from DACs A, B, and C (the "large" DACs).
R_{SET2}	I	A 600 resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals from DACs D, E, and F (the "small" DACs).
COMP1	O	Compensation Pin for DACs A, B, and C. Connect a 0.1 uF Capacitor from COMP to V_{AA}. For Optimum Dynamic Performance in Low Power Mode, the value of the COMP1 capacitor can be lowered to as low as 2.2 nF.
COMP2	O	Compensation Pin for DACs D, E, and F. Co nnect a 0.1 uF Capacitor from COMP to V_{AA}.
DAC A	O	GREEN/Composite/Y Analog Output. This DAC is capable of providing 34.66 mA output.
DAC B	O	BLUE/S-Video Y/U Analog Output. This DAC is capable of providing 34.66 mA output.
DAC C	O	RED/S-Video C/V Analog Output. This DAC is capable of providing 34.66 mA output.
DAC D	O	GREEN/Composite/Y Analog Output. This DAC is capable of providing 8.66 mA output.
DAC E	O	BLUE/S-Video Y/U Analog Output. This DAC is capable of providing 8.66 mA output.
DAC F	O	RED/S-Video C/V Analog Output. This DAC is capable of providing 8.66 mA output.
SCLOCK	I	MPU Port Serial Interface Clock Input.
SDATA	I/O	MPU Port Serial Data Input/Output.
CLAMP	O	TTL Output Signal to external circuitry to enable clamping of all video signals.
PAL_NTSC	I	Input signal to select PAL or NTSC mode of operation, pin set to Logic "1" selects PAL.
$\overline{\text{VSO}}$	O	$\overline{\text{VSO}}$ TTL Output Sync Signal.
$\overline{\text{CSO}}$_$\overline{\text{HSO}}$	O	Dual Function $\overline{\text{CSO}}$ or $\overline{\text{HSO}}$ TTL Output Sync Signal.
ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address.
$\overline{\text{RESET}}$	I	The input resets the on-chip timing generator and sets the ADV7172/ADV7173 into default mode. This is NTSC operation, Timing Slave Mode 0, DACs A, B, and C powered OFF, DACs D, E, and F powered ON, Composite and S-Video out.
TTX	I	Teletext Data Input Pin.
TTXREQ	O	Teletext Data Request output signal used to control teletext data transfer.
V_{AA}	P	Power Supply (3 V to 5 V).
GND	G	Ground Pin.

FL TUBE VIEW

Q7002: 16BT128GNYK





(1G-15G)

	16G	15G-1G
P1	A	1-1
P2	B	2-1
P3	SLEEP	3-1
P4	MUTING	4-1
P5	AAC	5-1
P6	ZONE2	1-2
P7	PCM	2-2
P8	D D	3-2
P9	D	4-2
P10	MULTI CH	5-2
P11	EX	1-3
P12	HDMI	2-3
P13	dts	3-3
P14	DSP	4-3
P15	96/24	5-3
P16	ES	1-4
P17	STEREO	2-4
P18	Neo:6	3-4

	16G	15G-1G
P19	DIRECT	4-4
P20	D PL	5-4
P21	II	1-5
P22	x	2-5
P23	SIRIUS	3-5
P24	THX	4-5
P25	XM	5-5
P26	DAB	1-6
P27	▷ ◁	2-6
P28	TUNED	3-6
P29	MEMORY	4-6
P30	AUTO	5-6
P31	FM STEREO	1-7
P32	RDS	2-7
P33	ft	3-7
P34	ch	4-7
P35	dB	5-7

MICROPROCESSOR TERMINAL DESCRIPTIONS

Q701: M30627FHPGP

No.	Pin Name	Function	I/O	Act.	Description
1	Vref	Vref			A/D Reference Voltage (Vcc)
2	AVcc	AVcc			A/D Power supply
3	P97/~ADTRG/SIN4	VMSDI	I	H	Data input pin from HDMI microprosessor
4	P96/ANEX1/SOUT4	VMSDO	O	H	Data output pin to HDMI microprosessor
5	P95/ANEX0/CLK4	VMCLK	O	CLK	Clock output pin to HDMI microprosessor
6	P94/DA1/TB4IN	VCRST	O	H	Reset cotrol pin to Video Encoder/Decoder
7	P93/DA0/TB3IN	~VMUT	O	L	VIDEO MUTE control pin
8	P92/TB2IN/SOUT3	OSDSDO	O	H	Data output pin to OSD
9	P91/TB1IN/SIN3	SYNC	I	H	VIDEO SYNC detect pin
10	P90/TB0IN/CLK3	OSDCLK	O	CLK	Clock output pin to OSD
11	P141	~OSDCS	O	L	OSD chip select pin
12	P140		O	H	No use
13	BYTE	BYTE			External bus width select pin. Connect to Ground.
14	CNVSS	CNVss			Processor mode select pin. Connect to the ground via resistor.
15	P87/XCIN	RDSDATA	I	H	RDS data input from LA72725 in tuner pack
16	P86/XCOUT	XMSRSEL	O	H	XM/SIRIUS select pin
17	~RESET	~RESET	I	L	Reset input
18	XOUT	Xout			Ceramic oscillator connection pin.
19	VSS	Vss			Power supply Ground pin
20	XIN	Xin			Ceramic oscillator connection pin.
21	VCC1	Vcc1			Power supply pin
22	P85/~NMI	~NMI	I	L	No use
23	P84/~INT2	POFF	I	L	Power failure detection input
24	P83/~INT1	VSYNC	I	L	Vertical sync signal detection input.
25	P82/~INT0	~XMERRIRQ/~RDSCLK	I	L	(D-type)XM IC interrupt input / (P-type)RDS clock input / (Other type)No use
26	P81/TA4IN/~U	XMCOMSEL	O	H	Control output to XM IC
27	P80/TA4OUT/U	~XMDACRST	O	L	XM DAC reset pin
28	P77/TA3IN	~DIRINT0	I	H	DIR/Codec unlock detect pin
29	P76/TA3OUT	DSPCLK	O	L	Clock output for DSP
30	P75/TA2IN/~W	~DSPINT2	I	L	DSP BUSY detect pin
31	P74/TA2OUT/W	~DSPINT1	I	L	DSP DEC detect pin
32	P73/~CTS2/~RTS2/TA1IN/~V	~DSPINT0	I	L	DSP NIC detect pin
33	P72/CLK2/TA1OUT/V	~SDET	I	L	S-VIDEO detect pin
34	P71/RXD2/SCL2/TA0IN/TB5IN	VDSCL/PLLSCL	O	CLK	I2C clock output to tuner pack
35	P70/TXD2/SDA2/TA0OUT	VDSDA/PLLSDA	I/O	H	I2C data input/output from/to tuner pack
36	P67/TXD1/SDA1	FTXD	O	H	Flash microprocessor rewrite port
37	Vcc1			H	
38	P66/RXD1/SCL1	FRXD	I	H	Flash microprocessor rewrite port
39	Vss			H	
40	P65/CLK1	FCLK	O	CLK	Flash microprocessor rewrite port
41	P64/~CTS1/~RTS1/~CTS0/CLKS1	FBUSY	O	H	Flash microprocessor rewrite port
42	P63/TXD0/SDA0	XMSRTXD	O	H	XM/SIRIUS data output pin
43	P62/RXD0/SCL0	XMSRRXD	I	H	XM/SIRIUS data input pin
44	P61/CLK0	~XMRST	O	L	XM IC reset pin
45	P60/~CTS0/~RTS0	~DIRCS	O	L	DIR/Codec chip select pin
46	P137	OSDINV	O	H	OSD IC input select pin(Video)
47	P136	OSDINY	O	H	OSD IC input select pin(S Video)
48	P135		O	H	No use
49	P134		O	H	No use
50	P57/~RDY/CLKOUT	~DIRRST	O	L	DIR/Codec reset pin
51	P56/ALE	~DSPCS	O	L	DSP chip select pin
52	P55/~HOLD	~FEPM	O	H	Flash microprocessor rewrite port
53	P54/~HLDA	~DSPRST	O	L	DSP reset pin
54	P133		O	H	No use
55	P132		O	H	No use
56	P131	MCHSEL	O	H	ANALOG/HDMI MCLK select pin
57	P130		O	H	No use
58	P53/BCLK	DIGCLK	O	CLK	DIR/Codec/DSP clock output pin
59	P52/~RD	DIGSDI	I	H	DIR/Codec/DSP data input pin
60	P51/~WRH/~BHE	DIGSDO	O	H	DIR/Codec/DSP data output pin
61	P50/~WRL/~WR	~FCE	I	H	Flash microprocessor rewrite port
62	P127		O	H	No use
63	P126	Z2MUT	O	H	Mute control output for ZONE2
64	P125	SBZ2MUT	O	H	Mute control output for SB/ZONE2

MICROPROCESSOR TERMINAL DESCRIPTIONS

Q701: M30627FHPGP

No.	Pin Name	Function	I/O	Act.	Description
65	P47/~CS3	AMUT	O	H	Audio mute control pin
66	P46/~CS2	SPRLZ2	O	H	ZONE speaker relay control pin
67	P45/~CS1	SPRLSB	O	H	Surround Back speaker relay control pin
68	P44/~CS0	SPRLCS	O	H	Center/Surround Back speaker relay control pin
69	P43/A19	SPRLF	O	H	Front speaker relay control pin
70	P42/A18		O	H	No use
71	P41/A17	VOLDATA	O	H	Data output to R2S15211
72	P40/A16	VOLCLK	O	ELK	Clock output to R2S15211
73	P37/A15		O	H	No use
74	P36/A14	VPOWER	O	H	Power control output to video section
75	P35/A13	APOWER	O	H	Power source control output
76	P34/A12	~POFF2	I	L	POFF detect pin
77	P33/A11	~FANH	O	L	No use
78	P32/A10	~FANCTRL	O	L	No use
79	P31/A09	TRGZ2	O	H	ZONE 12V trigger output
80	P124	TRGB	O	H	No use
81	P123	TRGA	O	H	No use
82	P122	Z2VOLMUT	O	H	No use
83	P121	Z2VOLCLK	O	H	No use
84	P120	Z2VOLDAT	O	H	No use
85	VCC2	Vcc2			Power supply
86	P30/A8(/-/D7)	SEC1H	O	H	Voltage-select control pin
87	VSS	Vss			Power supply Ground
88	P27/AN27/A7(/D7/D6)	PROTECT	I	H	Protection detect pin
89	P26/AN26/A6(/D6/D5)	VOLH	I	A/D	Signal level protection detect pin
90	P25/AN25/A5(/D5/D4)	THERMAL	I	A/D	Thermal protection detect pin
91	P24/AN24/A4(/D4/D3)	INIT3	I	A/D	Initializing pin 3
92	P23/AN23/A3(/D3/D2)	INIT2	I	A/D	Initializing pin 2
93	P22/AN22/A2(/D2/D1)	INIT1	I	A/D	Initializing pin 1
94	P21/AN21/A1(/D1/D0)	BAND	I	A/D	Initializing pin for tuner frequency
95	P20/AN20/A0(/D0/-)	~SYSOUT	O	L	RI output pin
96	P17/D15/~INT5	SYSIN	I	H	RI input pin
97	P16/D14/~INT4	~IRIN	I	L	IRIN remote control input pin
98	P15/D13/~INT3	~REMIN	I	L	Remote controller signal input pin
99	P14/D12	~STEREO	I	H	FM Stereo detect pin
100	P13/D11	~SD	I	H	FM/AM TUNED detect pin
101	P12/D10	HPDET	I	H	Headphone detection input
102	P11/D9	VOLB	I	H	Master volume rotary encoder input
103	P10/D8	VOLA	I	H	Master volume rotary encoder input
104	P07/AN07/D7		O	H	No use
105	P06/AN06/D6	LEDZONE2	O	H	Zone LED control pin
106	P05/AN05/D5		O	H	No use
107	P04/AN04/D4	LEDSTBY	O	H	STANDBY LED control pin
108	P03/AN03/D3	FLDSDO	O	H	Serial data output for FL driver
109	P02/AN02/D2	FLDCLK	O	ELK	Serial clock output for FL driver
110	P01/AN01/D1	~FLDCS	O	L	Chip select output for FL driver
111	P00/AN00/D0	~FLDRST	O	L	Reset output for FL driver
112	P117	~MICDET	I	L	Microphone detection input
113	P116	MICMUT	O	H	Microphone mute output
114	P115		O	H	No use
115	P114		O	H	No use
116	P113	~VMRST	O	L	HDMI microprocessor reset pin
117	P112	VMSTB	I	H	HDMI microprocessor strobe input
118	P111	TXMUTE	O	H	HDMI microprocessor mute pin
119	P110	RXMUTE	I	H	HDMI microprocessor RXMUTE detect pin
120	P107/AN7/~KI3	~KEYINT3	I	L	Key input interrupt 3
121	P106/AN6/~KI2	~KEYINT2	I	L	Key input interrupt 2
122	P105/AN5/~KI1	~KEYINT1	I	L	Key input interrupt 1
123	P104/AN4/~KI0	~KEYINT0	I	L	Key input interrupt 0
124	P103/AN3	KEY	I	A/D	Key input 3
125	P102/AN2	KEY	I	A/D	Key input 2
126	P101/AN1	KEY	I	A/D	Key input 1
127	AVIS	AVss			Ground for A/D
128	P100/AN0	KEY	I	A/D	Key input 0

ADJUSTMENT PROCEDURE-1

IDLING CURRENT ADJUSTMENT

[When]

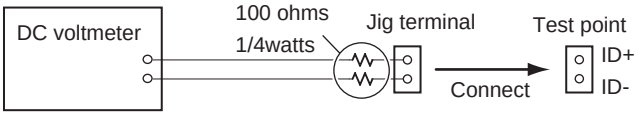
Exchange Power transistor (Q6050 - Q6056, Q6060 - Q6066) and Amplifier PC board (NAAF-8911).

[Procedure]

<Note> No load and No signal

Refer to <Fig-1> in " ADJUSTMENT PROCEDURE-2 " for the adjustment points and the test points.

1. Before idling adjustment, turn the trimming resistors to counter clockwise.
2. Connect the dc voltmeter to test points,
   using two 100 ohm resistors between the poles of the jig terminal and the dc voltmeter terminals.



3. Connect the ac power cord to wall outlet.
4. Press the STANDBY/ON button to turn the power on.
5. Adjust the trimming resistors as the following procedure immediately after power on.

Channel	Mark	Adjustment point (Trimming resistor)	Measuring point (Test point)	Adjustment value
Center	C	R6040	P6080	2.5 mV
Front Left	L	R6041	P6081	2.5 mV
Front Right	R	R6042	P6082	2.5 mV
Surround Left	SL	R6043	P6083	1.5 mV
Surround Right	SR	R6044	P6084	1.5 mV
Surround Back Left	SBL	R6045	P6085	1.5 mV
Surround Back Right	SBR	R6046	P6086	1.5 mV

6. Wait for 4 - 6 minutes. (Heat running)
7. Re-adjust the trimming resistors as the following procedure.

Channel	Adjustment point	Measured value →	Adjustment value	Specifications (＊In a stable state)
Front Left, Right and Center	R6041, R6042 and R6040	In case below 9 mV →	9 mV	12 +/- 3 mV
		In case 9 - 11 mV →	No re-adjustment	
		In case over 11 mV →	11 mV	
Surround Left Surround Right Surround Back Left Surround Back Right	R6043, R6044, R6045 and R6046	In case below 6 mV →	6 mV	9 +/- 3 mV
		In case 6 - 8 mV →	No re-adjustment	
		In case over 8 mV →	8 mV	

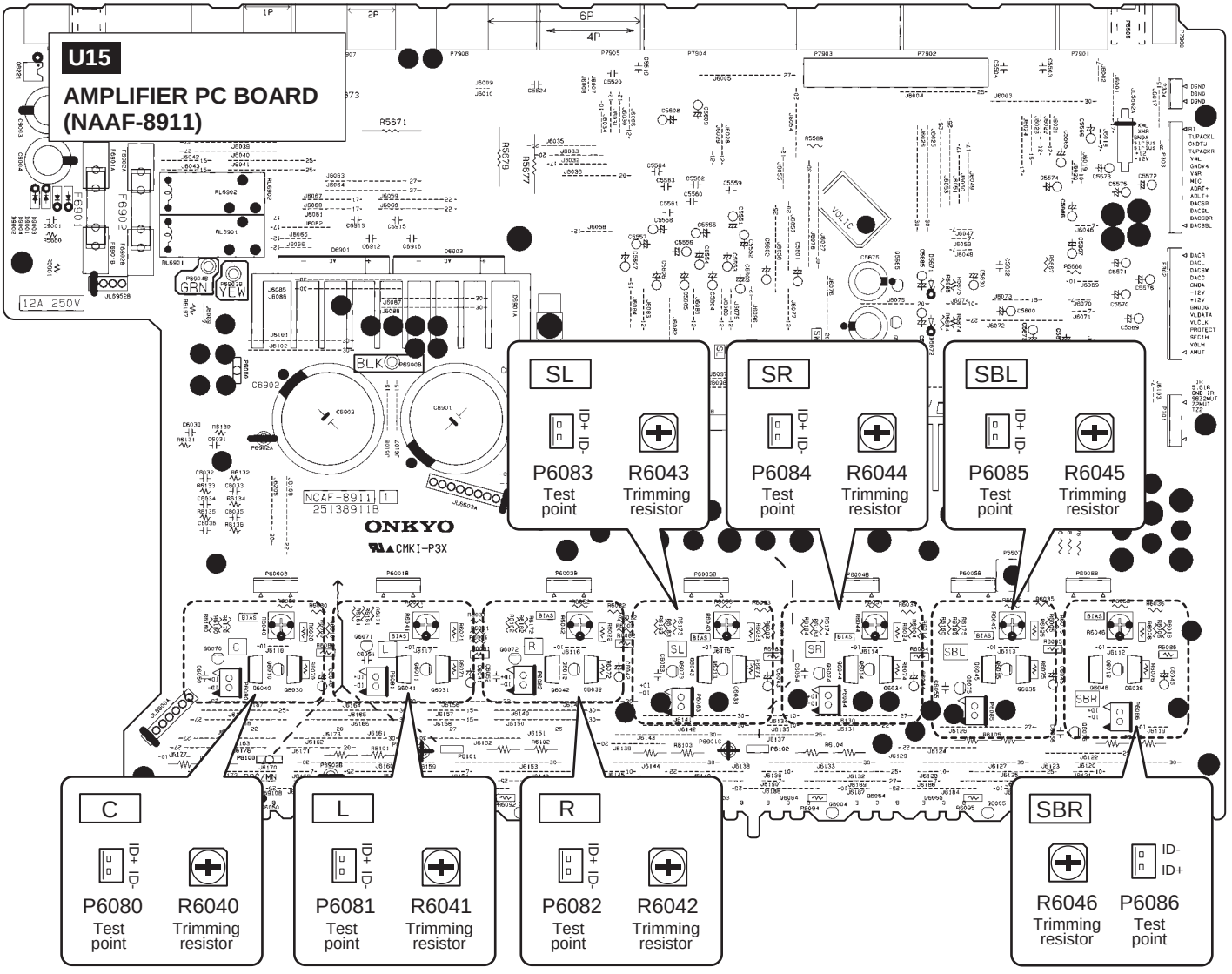
8. Disconnect the dc voltmeter.
9. Press the STANDBY/ON button to turn the power off.
10. Disconnect the ac power cord of the unit.

＊ Idling currents are stabilized in about 10 minutes after power on.

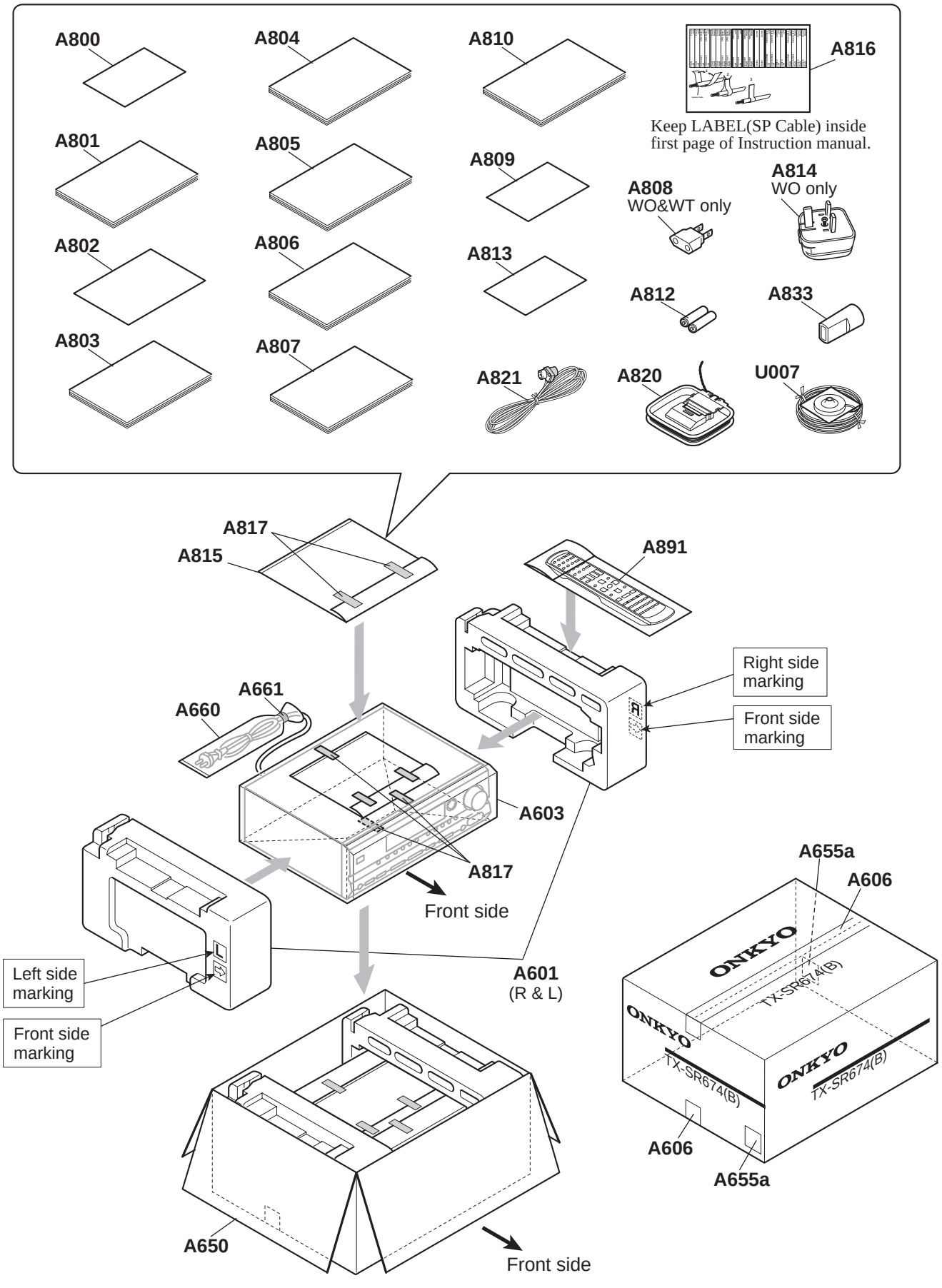
ADJUSTMENT PROCEDURE-2

IDLING CURRENT ADJUSTMENT

<Fig-1>



PACKING PROCEDURE



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