

THIS IS NOT INTENDED AS A PROJECT AND WILL NOT BE SUPPORTED AS SUCH.
DO NOT CALL US.

Service manual for D-1 DAC

The D-1 Dac contains 3 separate printed circuit boards in it's chassis. They are the motherboard, receiver board and front panel display and control board.

The motherboard has test points for all the on board power supply voltages. These points are located by the heat sinks and labeled on the silk screen. The plus and minus 20 digital are unregulated and are approximate voltages. There are separate 5-volt regulators on the motherboard for VCO and PLL circuits. The receiver board and front panel boards have their own 5-volt regulators.

The receiver-input selection is controlled by the front panel microprocessor via Mosfets. These switch one of four relays on the receiver board. The signal is routed to a Crystal 8412 receiver chip. The output of the Crystal chip is feed to the NPC digital filter and also to U7 PLL on the motherboard for the PLL reference. The master clock from the 8412 is feed to the front panel board and used to determine sampling frequency. The sampling frequency determines the selection of signals F0 and F1 for proper VCO crystal selection and digital filter deemphasis selection. F0 and F1 come from the microprocessor on the front panel to the motherboard and the receiver board via a ribbon cable. The front panel also sends the polarity signal to the receiver board.

U7 and U4 along with VCO module U3 form a secondary PLL circuit to clock the digital filter and DAC's. U5 and U2 are separate regulators for the VCO and PLL chips. R5 and R6 along with C13 form the PLL filter. When the system is locked U7 pins 3 and 14 are at the word clock rate (44.1 for cd).

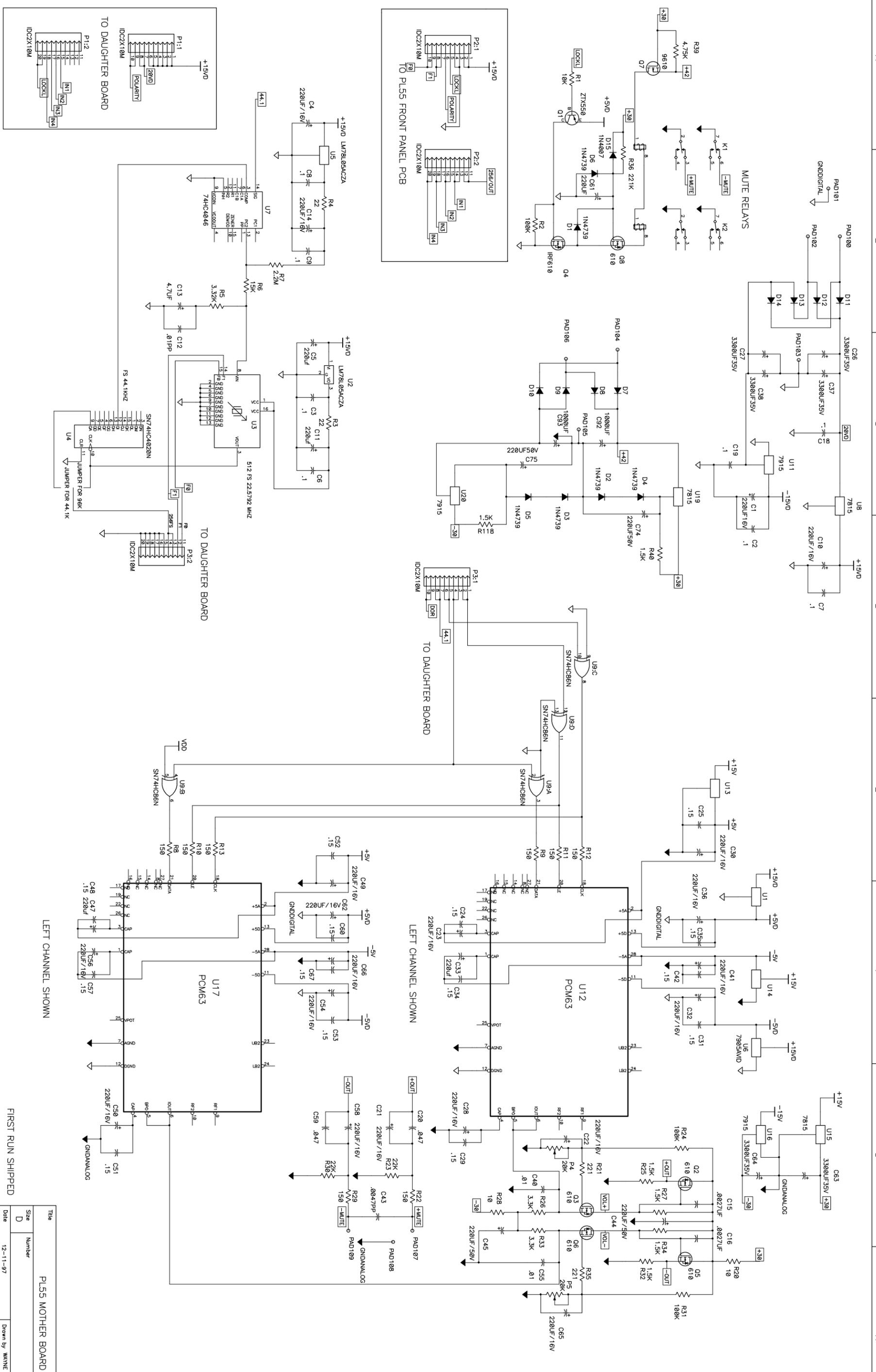
The receiver boards digital filter feeds buffers U9 and U10 on the mother. These signals are then routed to the PCM 63's via resistors. The left and right channels are identical.

The analog section consists of four matched Mosfets for each channel. Two for current to voltage conversion and two for output buffers. The current to voltage converter transistors Q3 and Q6 have their sources adjusted to 0 volts + or - 50 mV with trim pots.

The drains run at about 17 volts. The output buffers Q2 and Q5 have their drains at the supply rails of 33 volts. The sources run at about 14 volts. The volume control works by coupling the drains of the current to voltage converter transistors through fixed resistors and a switch. This sums opposite phases and cancels some of the signal. The analog signal is then routed to the buffers gates and out it's sources to the output jacks. The signal is muted with two relays in case of a power failure or when the Crystal receiver has lost lock.

Revision notes

REV1: PC board physical layout changes for better parts fit.
Silk screen now lists component values instead of reference designators.
Mute circuit has delay added on U3 receiver board.



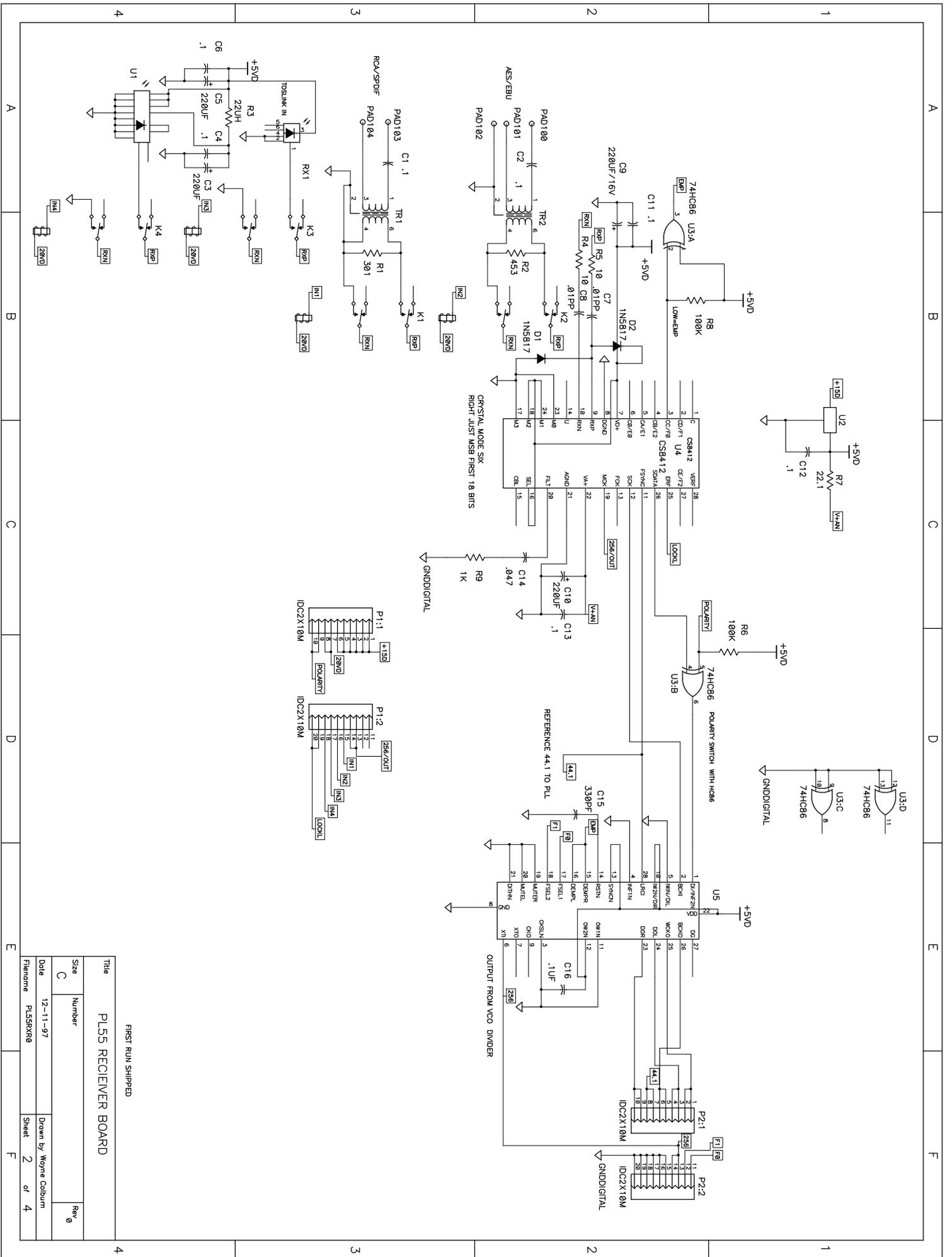
LEFT CHANNEL SHOWN

LEFT CHANNEL SHOWN

PLS5 MOTHER BOARD

FIRST RUN SHIPPED

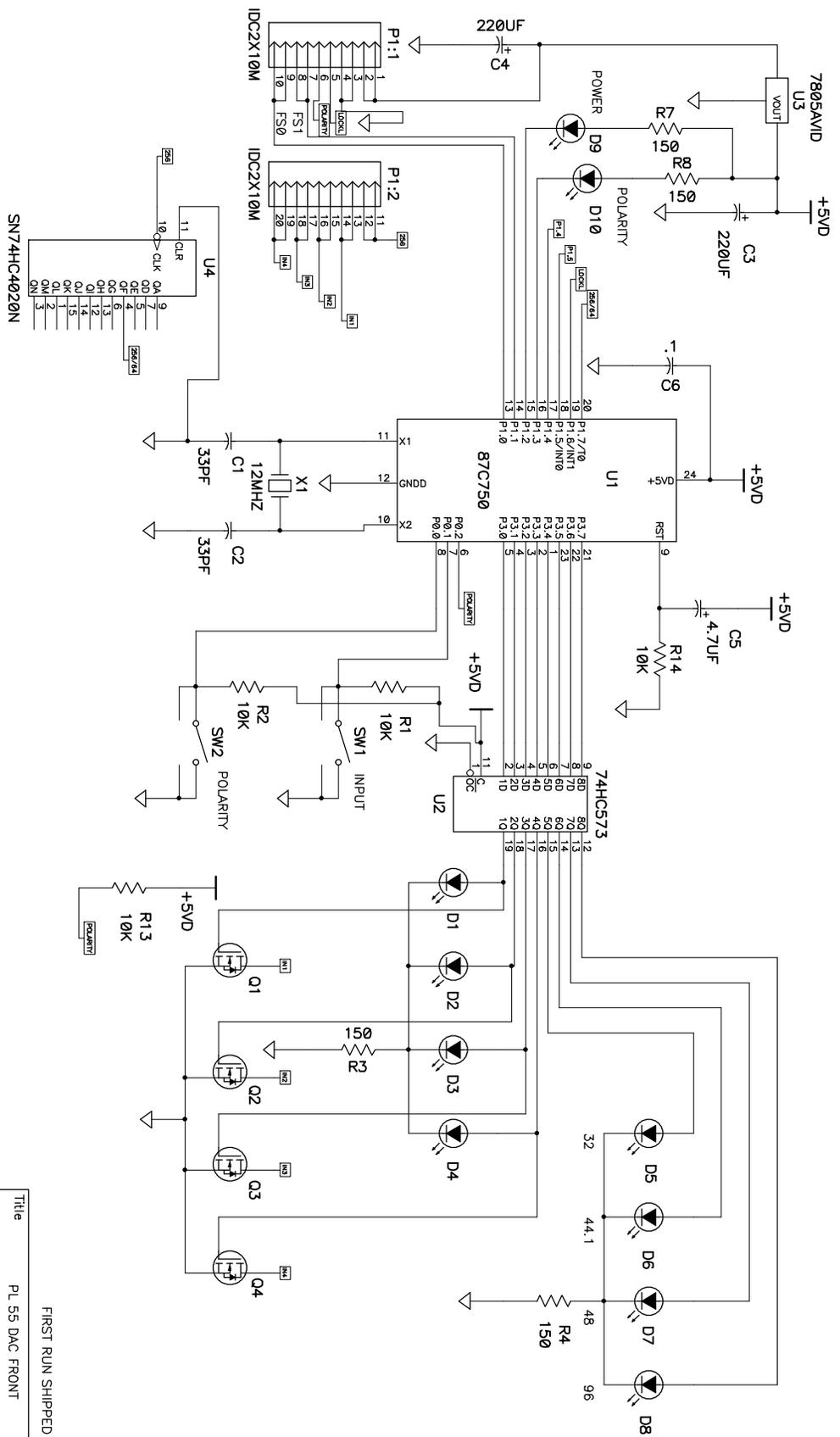
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PLSS RECEIVER BOARD

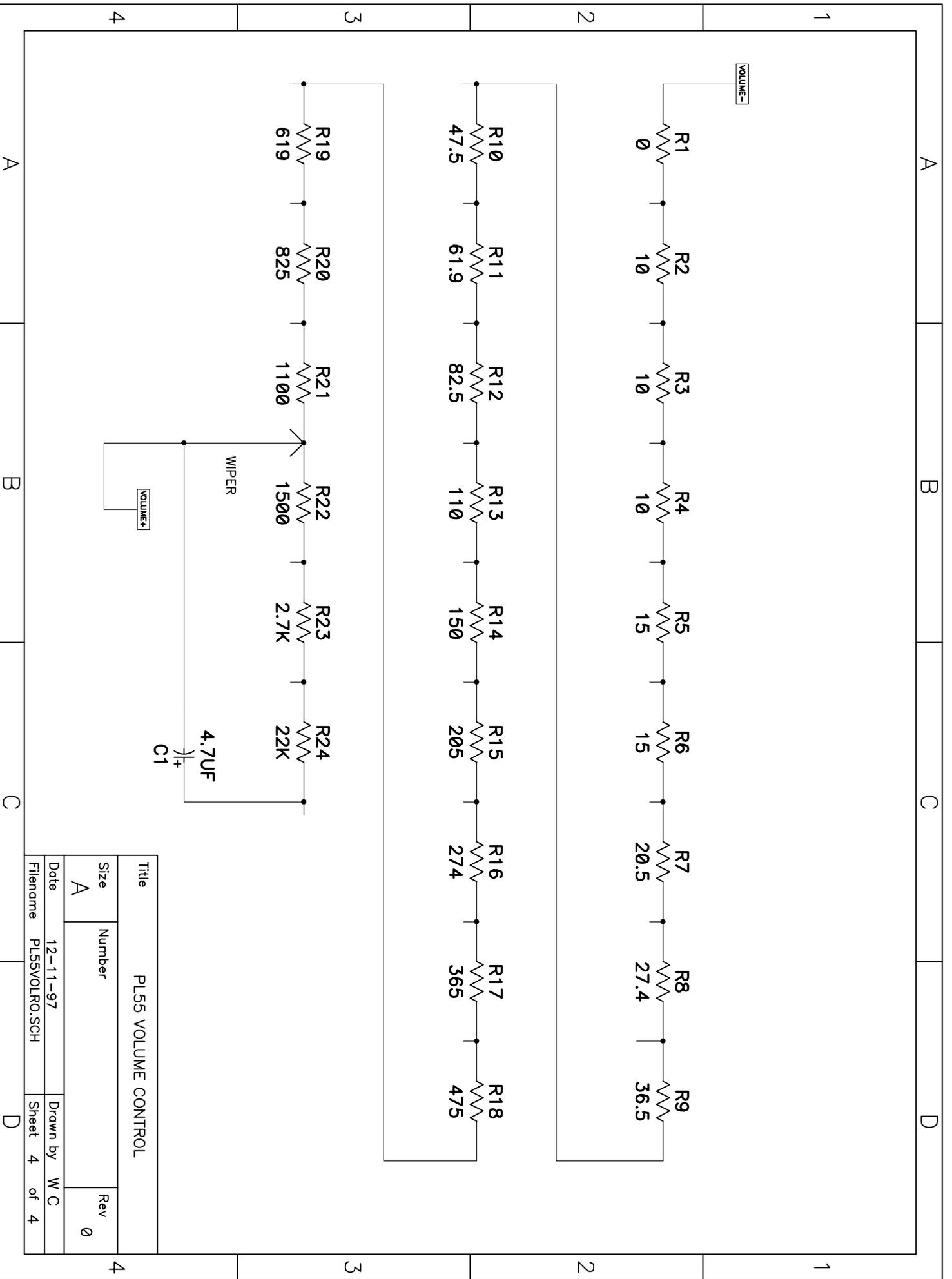
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Title		PL55 VOLUME CONTROL	
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