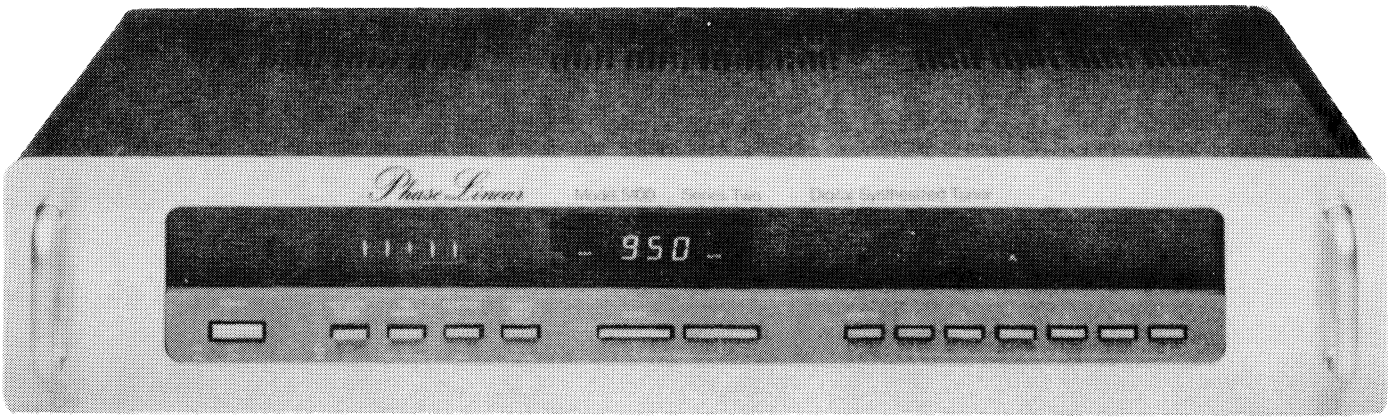
MODEL 5100 SERIES TWO
DIGITAL SYNTHESIZED TUNER

Service Manual



Phase Linear®

5100 SERIES TWO
FM/AM DIGITAL SYNTHESIZED TUNER

SERVICE MANUAL

CONTENTS

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THIS MANUAL IS INTENDED FOR USE ONLY BY QUALIFIED TECHNICAL SERVICE PERSONNEL. HAZARDOUS VOLTAGES MAY BE ENCOUNTERED IN THE TEST AND SERVICING OF THE 5100II. USE EXTREME CAUTION; READ ALL INSTRUCTIONS.

PHASE LINEAR SERVICE DEPARTMENT
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prepared 2/80
revised 6/81

1. SPECIFICATIONS

FM Section:
Frequency Range: 87.55–108.0MHz
Usable Sensitivity:
  Mono; 10.8dBf(1.9uV)
50dB Quieting Sensitivity:
  Mono; 16.2dBf(3.5uV)
  Stereo; 38.5dBf(46.2uV)
Signal-to-Noise Ratio
  at 80dBf: Mono; 72dB
            Stereo; 70dB
Distortion
  at 65dBf: Mono; 100Hz 0.05%
                  1KHz 0.05%
                 10KHz 0.10%
          Stereo; 100Hz 0.08%
                  1KHz 0.08%
                 10KHz 0.25%
Capture Ratio: 1.0dB
Alternate Channel Selectivity:
  60dB(400KHz)
Stereo Separation: 1KHz; 55dB
          50Hz to 10KHz; 40dB
Frequency Response:
  20Hz to 15KHz $^{+0.2}_{-0.5}$dB
Spurious Response Ratio: 80dB
Image Response Ratio: 80dB
IF Response Ratio: 90dB
AM Supression Ratio: 60dB
Subcarrier Product Ratio: 55dB
Muting Threshold: 25.0dBf(8.1uV)
SCA Rejection Ratio: 50dB
De-Emphasis Switch:
  -75uS(domestic de-emphasis)
  -50uS(export model only)
  -25uS(Dolby de-emphasis)
Antenna Input: 300-ohms balanced
               75-ohms unbalanced

AM Section:
Frequency Range:
  531–1602KHz(AMIF switch:9KHz)
  525–1605KHz(AM IF switch:10KHz)
Sensitivity:
  IHF, ferrite antenna: 300uV/m
  IHF, external antenna: 30uV
Selectivity: 30dB
Signal-to-Noise Ratio: 45dB
Image Response Ratio: 30dB
IF Response Ratio: 60dB
Antenna: Built-in Ferrite Antenna

Audio Section:
Output(level/impedance):
  FM(100% mod.).....600mV/100-ohms
  AM(30% mod.)......200mV/100-ohms
  REC level.........325mV/100-ohms

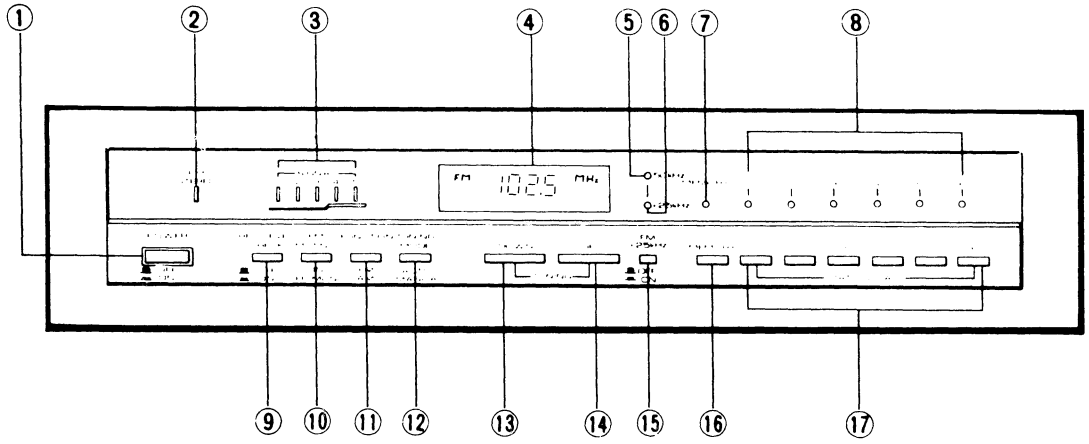
Semiconductors:
IC's.............15
FET.............. 8
Transistors.....46
Diodes.........110

Miscellaneous:
Power Requirements:
  120v, 50/60Hz(domestic)
  120/220v, 50/60Hz(export only)
Power Consumption: 10 watts
Dimensions:
  475(w) x 97(h) x 335.5(d)mm
  19(w) x 3-13/16(h) x 13-13/16(d)in
Weight (without packing):
  4.8kg (10lb 9oz)

Furnished Parts:
FM T-type dipole antenna........1
Phono plug patch cord...........1
Fuse:
 (Domestic model); 1-amp........1
 (Export model); 0.5-amp.......1
Operating Instructions..........1

NOTE:
Specifications and design subject to possible modification without notice due to improvements.

2. FRONT PANEL FACILITIES



1. POWER SWITCH
   Set this switch to ON to supply power to the tuner.
2. FM STEREO INDICATOR
   This indicator lights up when the tuner is receiving a stereo program if the FM MUTING switch is set to "ON".
3. SIGNAL INDICATORS
   These indicators "1" through "5" light up in accordance with strength of signal.
4. FREQUENCY DISPLAY
   This indicates the tuned frequency.
5. 50kHz INDICATOR(export model only)
   When this indicator comes on, it means that the frequency of the station being received is the value indicated on the frequency display plus 50kHz.

   NOTE: The 50kHz indicator goes off when the function indicator is returned to FM after having been set to AM. In this case, depress the UP tuning switch one.
6. 25kHz INDICATOR(export model only)
   When this indicator comes on, it means that the frequency of the station being received is the value indicated on the frequency display plus 25kHz.

   NOTE: When both the 25kHz and 50kHz indicators come on, it means that the frequency of the station being received is the value indicated on the frequency display plus 75kHz.
7. MEMORY INDICATOR
   This indicator lights up when the memory switch is depressed. Operate the station call switches while this indicator is on. Frequencies can not be stored when it goes off.
8. STATION INDICATORS
   These indicators light up when corresponding station switch is depressed.

9. RECORDING LEVEL CHECK SWITCH
   Set this switch to OFF for normal FM reception and to ON for a recording reference level used for FM broadcasts.

10. FM MUTING/MODE SWITCH
    Set this wtich to ON, the muting switch is actuated for FM reception,and the OFF position the program is received in mono when the broadcast station is located far away or when the signals are weak.

11. FUNCTION SWITCH
    Set this switch to FM for tuning an FM broadcast.
    Set this switch to AM for tunign an AM broadcast.

12. TUNING MODE SWITCH
    Set this switch to AUTO for auto scan tuning.
    Set this switch to MANUAL for manual tuning. When the tuning switches are depressed, the frequencies will change in 50kHz steps for FM reception and 1kHz steps for AM reception.

13. TUNING SWITCH DOWN
    Depress when tuning a station with a frequency lower than that indicated on the frequency display.

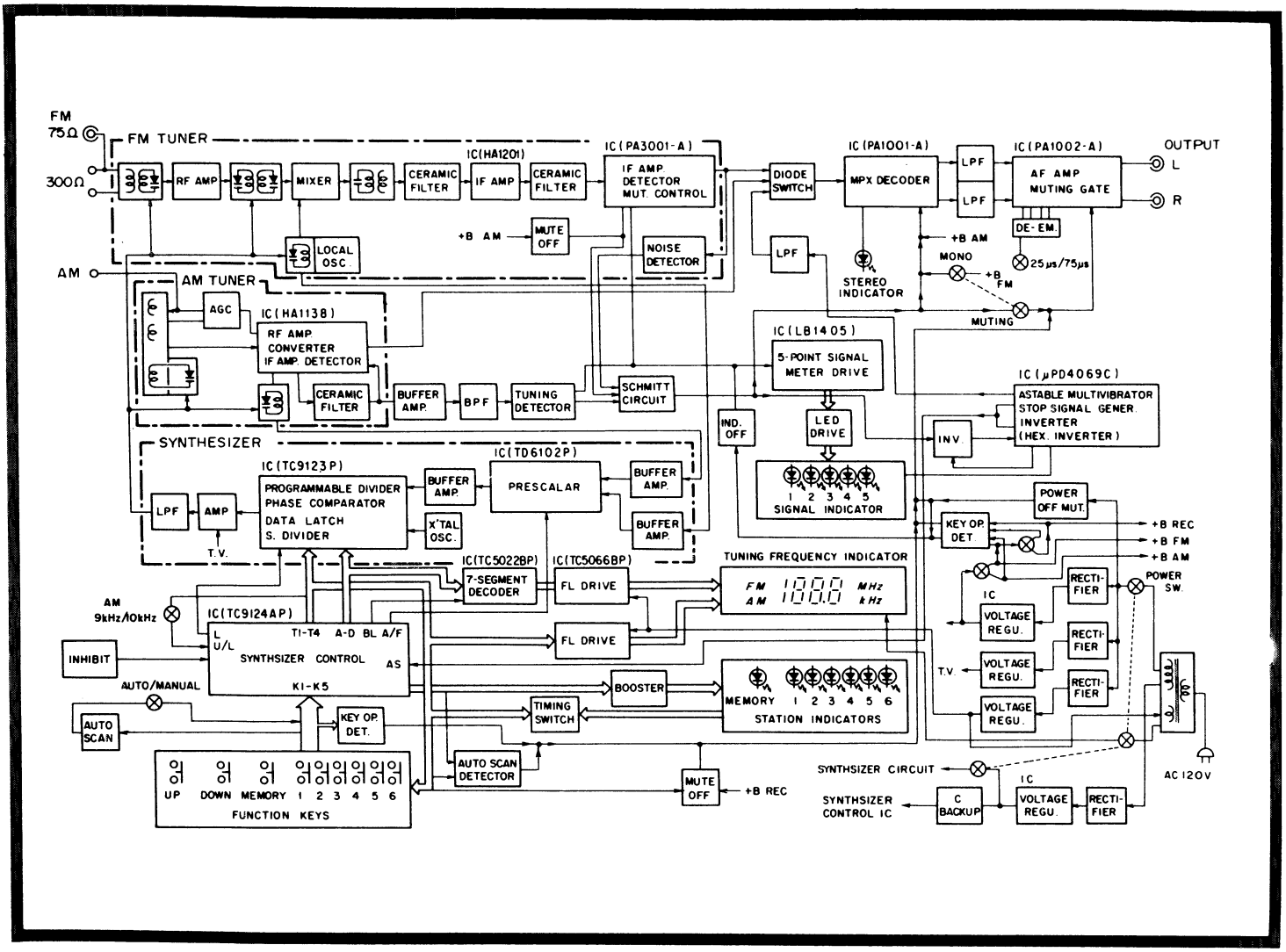
14. TUNING SWITCH UP
    Depress when tuning a station with a frequency higher than that indicated on the frequency display.

15. FM +25kHz OFFSET SWITCH (export model only)
    When this switch is set to the depressed position, a frequency of 25kHz is added to the value indicated on the frequency display(the 25kHz indicator comes on).

16. MEMORY SWITCH
    Use this switch to store frequency of broadcast station in the memory.

17. STATION CALL SWITCHES
    Depress these switches when tuning a preset station or call out the station.

3. BLOCK DIAGRAM



4. CIRCUIT DESCRIPTIONS

The 5100 is a crystal oscillator Phase Locked Loop Digital Synthesizer tuner. Major functions are enumerated briefly below.

1. FREQUENCY RANGE

FM: 87.55MHz to 108MHz in 50kHz steps.

NOTE: On the export model the +25kHz offset switch permits frequencies to be shifted by +25kHz.

AM: 531kHz to 1602kHz in 1kHz steps.

NOTE: The 5100 domestic and export models have been equipped with an AM frequency lock selector (9kHz or 10kHz) on the back panel of the unit. When set in the 10kHz position, the 525kHz to 1605kHz frequency range is employed, and frequencies are changed in 10kHz steps during auto scan tuning mode.

2. TUNING

* Frequency is changed by 1 step for every push operation of the TUNING UP and TUNING DOWN keys. (Each push operation changes the frequency by 50kHz in the FM band, and by 1kHz in the AM band.)
* Frequency scanning is achieved by depressing the TUNING UP or TUNING DOWN key continuously when in the MANUAL mode. If either the TUNING UP or TUNING DOWN key is pressed and held, after an approximate 0.5 second delay tuning frequencies will be continuously scanned until the key is released.
* For auto scan tuning mode, set the TUNING MODE switch to the AUTO position and press either the TUNING UP or TUNING DOWN button once. In this mode, the frequency band will be scanned automatically, coming to a stop when the frequency of a sufficiently strong broadcasting station (input level above a specific value) is tuned.
* Preselected tuning by memory read-out(preset frequency read out from memory for direct tuning).

3. MEMORY

* A total of 6 FM frequencies and 6 AM frequencies may be stored in the memory.
* Also auto memory of the previous tuned frequency when switching back and forth between FM and AM bands(FM frequency set to the nearest 100kHz position).

  NOTE(export model only):
  This memory has not been designed to store 50kHz units in FM frequencies. If FUNCTION is switched over to AM when a frequency of 98.15MHz has been tuned, for example, and then later back to FM, this frequency will be retrieved as 98.1MHz). The preset memory(for 6 FM and 6 AM frequencies)on the other hand, can and does store frequencies to the nearest 50kHz.
* Last-one memory(the last frequency tuned when the power is switched off will be automatically retuned when the power is switched back on).

* Memory maintained by a separate power supply when the main power is turned off (i.e. when the POWER switch is switched off).

4. INDICATORS

* The received frequency is displayed in digital form by flourescent indicator tube. The FM 50kHz and 25kHz displays(export models only)however, are by LED indicator lamps.
* Signal strength is indicated by the SIGNAL indicator composed of an array of 5 LED lamps.
* Memory read-out indicator.
* Memory write-in indicator.
* FM STEREO/LINE indicator.

5. RECORDING LEVEL CHECK

* The 5100 also generates a 330Hz signal at a level corresponding to 50% modulation for use in calibrating a recording level.

4.1. FM TUNER SECTION

Front End:
The 5100 front end includes a dual-gate MOS FET RF amplifier (single stage) and a variable capacitance diode corresponding to a 4-ganged tuning capacitor. The local oscillator signal is applied to the synthesizer circuit for comparison with a reference signal, the resultant tuning voltage then being applied to the variable capacitance diode for determination of the oscillator frequency (tuning frequency).

IF Amplifier and Detector:
The output IF signal from the front end is passed via a dual-element ceramic filter, a limiter amplifier IC(HA1201), and another dual-element ceramic filter before being applied to the IF system IC(PA3001-A). In this way the IF signal is both amplified and detected.

Multiplex Decoder:
The MPX IC(PA1001-A) employed here contains a PLL type subcarrier generator circuit, an NFB type demodulator, an automatic pilot canceller, an LR shorting circuit for monophonic mode, an automatic stereo/mono switching circuit, and a stereo indicator drive circuit.

Audio Output Circuit:
The demodulated stereo signals are applied via low-pass filters to the audio muting IC(PA1002-A) which contains an audio amplifier circuit, an electronic muting gate, and the muting control circuit employed when the power is switched on.
De-emphasis involves the use of the audio amplifier NFB circuit, while the muting gate is opened and closed according to the various muting signals from the internal control circuit and other external circuits.

4.2. AM TUNER SECTION

See fig. 4-1 for an outline of the AM tuner IC(HA1138). The tuning circuit employs a variable capacitance diode(vari-cap) which corresponds to a 2-ganged tuning capacitor. The local oscillator signal is compared with a reference signal in the synthesizer circuit, and the resultant tuning frequency then applied to the vari-cap for determination of the oscillator frequency (tuning frequency). And in order to improve performance with strong input signals, the IC has been equipped with an AGC(automatic gain control)circuit, and the bar antenna fitted with a damping coil. The AGC varies the damping current by means of an FET according to the RF amplifier output level.

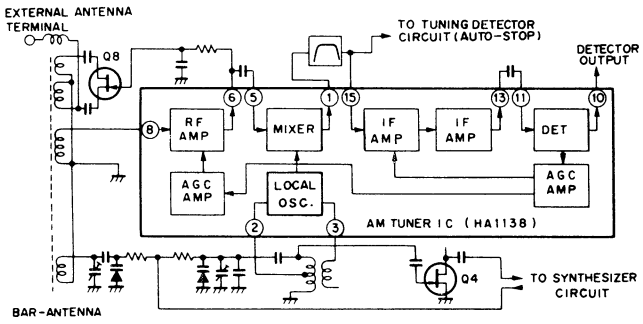


Fig. 4-1 AM Tuner

4.3. SYNTHESIZER CIRCUIT

Outline of Basic Operating Principles:

An outline of the basic composition of the PLL digital synthesizer circuit is shown in fig. 4-2. Although the actual circuit also includes a high speed scaling circuit because of the restrictions imposed by the IC operational frequency limits, the basic principles are the same, and the circuit has therefore been ommitted.

The output signal fs of the voltage controlled local osci-lator (VCO) undergoes 1/N frequency division in the programmable counter, followed by phase comparison with the output signal fr from the crystal controlled reference oscillator.

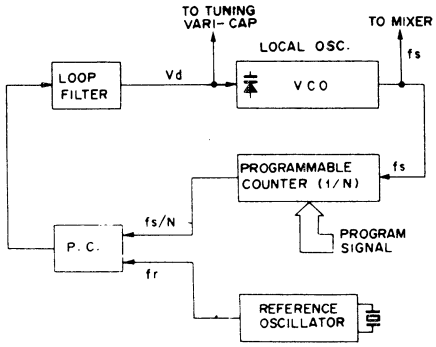


Fig. 4-2 Basic Composition of the PLL Synthesizer Circuit

The output from the phase comparator is then passed through a loop filter to become a DC voltage Vd which in turn controls the VCO. And since fs/N=fr in this closed loop, the VCO output frequency will be N times the reference frequency where N is an integer. Since the programmable counter varies the frequency division numerator N according to program signal, the VCO output frequency fs(local oscillator frequency)will be determined according to the program signal, becoming N times(integer multiple)the reference frequency fr.

Synthesizer Circuit in the 5100:

The composition of the synthesizer circuit employed in the 5100 is outlined in fig. 4-3. The major component in this circuit is the TC9123-GR C-MOS IC. Because of the restrictions imposed by the operational frequency limits of this IC, the frequency of the local oscillator during FM reception is divided by 8 in the ECL(emmitter-coupled logic)prescalar IC(TD6102P) prior to being applied to the TC9123-GR IC.
The data program signals used to designate FM/AM operation and the programmable counter frequency division ratio consists of BCD code pulse(A–D), time division pulse(T1–T4), and load pulse(L) signals. See fig.4-4 for an outline of the data program signal time chart.

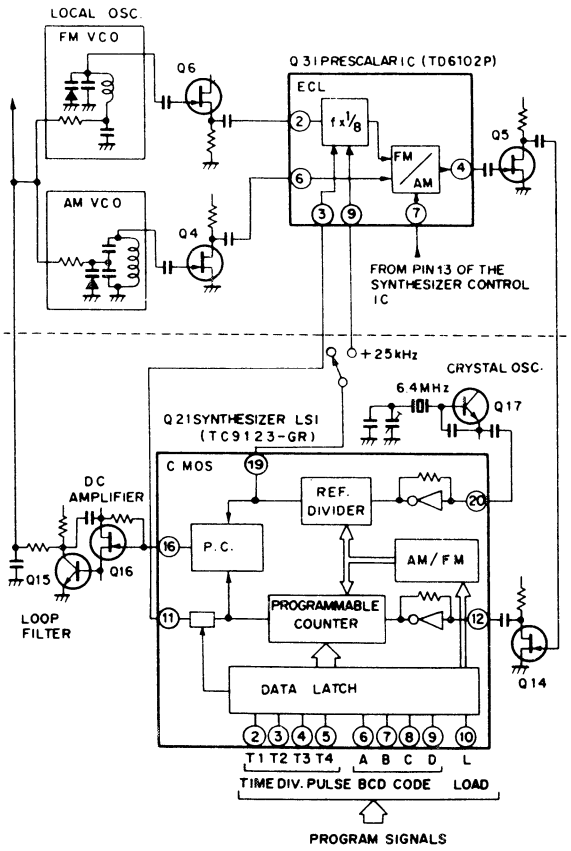


Fig. 4-3 5100 Synthesizer Circuit

Numbers 0 to 9 are applied in BCD (binary coded decimal)code to the synthesizer IC(TC9123-GR) A–D inputs according to the T1–T4 timing. The unit digit of the reception frequency is applied at time T1, the ten digit at T2, the hundred digit at T3, and the thousand digit at T4. This time shared data is then assembled by the latch circuit to form the frequency division data. And since the thousand digit will not involve any number except 1, frequency data is applied only to input A at time T4, the B, C, and D inputs serving as inputs for data designating the FM/AM operational mode. Input L is the load pulse input employed to prevent mis-reading of input data. Data latching starts with the down stroke of the load pulse.
The 5100 synthesizer system is operated on the basis of time division pulses(T1–T4)prepared by the synthesizer control IC(TC9124AP). Data transfer and indicator lamp drive is based on dynamic time division.

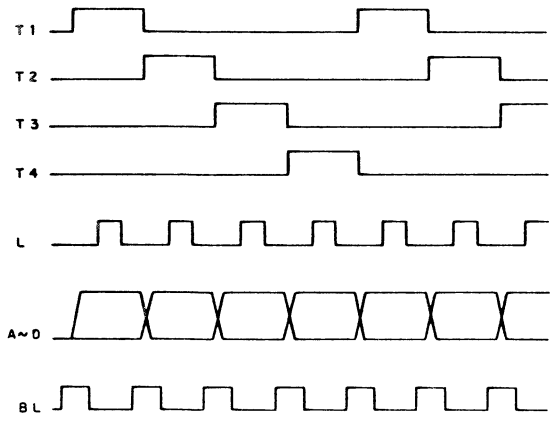


Fig. 4-4 Data Program Signal Time Chart

Operation During FM Reception:

Fig.4-5 outlines the block diagram of the 5100 synthesizer stage during FM reception. The basic operational step for this circuit is 100kHz. (In export models only the 50kHz tuning and 25kHz offset tuning involves a special operation in the prescalar IC(TD6102P) which shifts the PLL locked frequency.

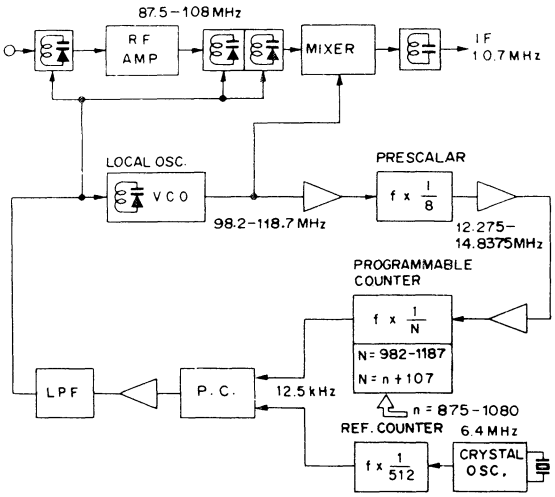


Fig. 4-5 Outline During FM Reception (100kHz Steps)

100kHz Step Operation:
With the basic operational step at 100kHz in fig.4-5, and the prescalar dividing the frequency by 8, the phase comparison frequency will be 12.5kHz. The reference frequcnsy signal is obtained by dividing the 6.4MHz crystal oscillator output by 512. And since the reception band is 87.5MHz to 108MHz and IF 10.7MHz, the local oscillator frequency will range from 98.2MHz to 118.7MHz. After dividing by 8 in the prescalar, this range will be 12.275MHz to 14.8375MHz. Hence, the 12.5kHz may be obtained by setting the programmable counter frequency division ratio N to 982—1187 for comparison with the reference signal in the phase comparator. The phase comparator output is passed via a low-pass filter to the tuning circuit vari-cap, resulting in the local oscillator frequency being locked to 8N times the reference frequency(12.5kHz), or in other words, N times 100kHz.
Since the reception frequency data (n) applied to the synthesizer IC(TC9123-GR) is shown in the FL indicator tube(frequency display) as 875—1080, the required frequency division ratio may be obtained from the reception frequency data by programming for frequency division ratio N=n+107 during FM reception.

50kHz Step Operation(Export Models Only):
The circuit shown in fig.4-5 will only change the reception frequency in 100kHz steps unless otherwise modified. By altering the frequency division ratio N, a 50kHz shift circuit may be activated with every second 100kHz frequency shift, resulting in the reception frequency being changed in 50kHz steps.

The fig.4-5 circuit forms a PLL(phase locked loop)where the local oscillator signal is sampled, divided, and then locked to a frequency 8N times the reference frequency(12.5kHz). Consequently, any attempt to vary the local oscillator frequency will result in the voltage applied to the vari-cap being changed in a way that will tend to cancel this variation. If then by some means a count can be obtained 50kHz lower than the actual frequency when the local oscillator is being sampled, it will be possible to alter the voltage applied to the vari-cap so that the oscillation frequency is increased by 50kHz.

The prescalar IC(TD6102P) shown in fig.4-6 contains 3 separate ½ frequency dividers for a total frequency division of 1/8. If a single shift pulse is applied to pin 3, a pulse count at the ¼ division stage will be eliminated. And if the shift pulse frequency is 12.5kHz, a total of 12,500 pulses will not be counted during the 1 second period. In terms of the IC input terminal (pin 2), this is equivalent to not counting 50,000 pulses within the same period, which in turn is equivalent to applying an input frequency which is 50kHz lower than the actual input frequency. The PLL consequently attempts to cancel this change, thereby increasing the voltage applied to the vari-cap so that the oscillation frequency is increased by 50kHz. The local oscillator frequency is thus locked at a frequency increased by 50kHz, thereby shifting the reception frequency by +50kHz.

The TC9123-GR synthesizer IC has been designed to produce a 12.5kHz output signal(comparator signal)at pin 11 with every second step. By connecting this signal to pin 3 of the prescalar IC(TD6102P), inpur frequencies may be received in 50kHz steps.

Table 1: Decimal Numbers and BCD Code

Decimal Numbers	8-4-2-1 Code (BCD)			
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

+25kHz Offset Circuit(Export Models Only):

When the FM +25kHz offset switch is turned on the 5100 reception frequency is shifted by +25kHz. The operating principles are basically the same as for the 50kHz step operation. When a single shift pulse is applied to pin 9, a pulse count at the ½ division stage will be eliminated. By selecting a shift pulse frequency of 12.5kHz, a total of 12,500 pulses per second will not be counted. And this is equivalent to not counting 25,000 pulses at the input terminal(pin 2), or in other words, the same as counting a frequency which is 25kHz lower than the actual input frequency. As a result, the voltage applied to the vari-cap is altered to a value which would increase the oscillation frequency by 25kHz, and is subsequently locked by the PLL circuit. In this way, the reception frequency is shifted by +25kHz.

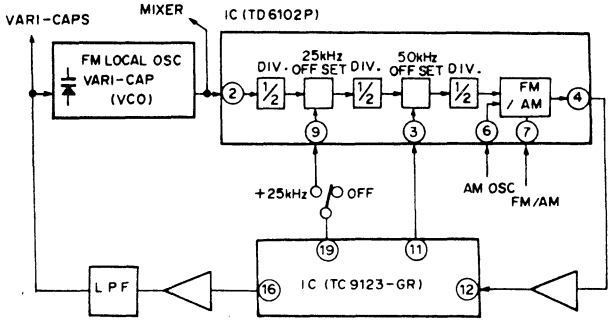


Fig. 4-6 50kHz/25kHz Shift Circuit

In the synthesizer IC(TC9123-GR) a reference signal(12.5kHz) is continuously being generated at pin 19, and is connected to pin 9 of the prescalar IC(TD6102P) via the FM =25kHz offset switch in order to shift the reception frequency by +25kHz.

Operation During AM Reception:

Fig.4-7 is a block diagram of the relevant parts of the synthesizer circuit involved in the reception of AM frequencies. With the reception band covering the 531kHz to 1602kHz range, and the IF signal set to 459kHz, the prescalar circuit is not required. Since frequencies are shifted in 1kHz steps, the phase comparator frequency will be 1kHz. The reference signal is obtained by dividing the crystal oscillator frequency (6.4MHz) by 6400. With the local oscillator frequency ranging from 990kHz to 2061kHz, 1kHz is acheived by setting the programmable counter frequency division ratio to the 990 to 2061 range, and this is compared with the reference signal in the phase comparator. The output of this comparator is then applied to the tuning circuit vari-cap via a low-pass filter, resulting in the local oscillator frequency being locked to N times the reference frequency(1kHz).

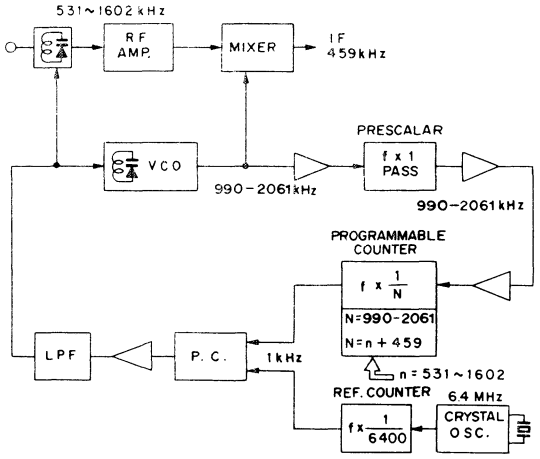


Fig. 4-7 Synthesizer Circuit for AM Reception

Again, since the reception frequency data (n) applied to the synthesizer IC(TC9123-GR)is shown in the FL indicator tubes(frequency display)as 531—1602, the required frequency division ratio may be obtained from this reception frequency data by programming the frequency division ratio as N=n+459 during AM reception.

NOTE: The 5100 has been designed with an AM frequency lock selector (9kHz/10kHz). When switched to the 10kHz position, the reception band becomes 525kHz—1602kHz, the IF signal 460kHz, and the programmable counter frequency division ratio N=n+460=985—2065.

4.4. SYNTHESIZER SYSTEM CONTROL CIRCUIT

The synthesizer control IC(TC9124AP) is an extremely complex IC, so the block diagram shown in fig.4-8 includes only the more important components. The IC input and output terminals are bfiefly described below.

Time Division Pulse Terminals(T1—T4):
The time division pulse generated by TC9124AP(outlined in fig.4-4) is a time-sharing timing signal used in synchronizing almost all TC9124AP inputs and outputs.

Reception Frequency Data Terminals(A—D):
The A—D terminals are employed in the transfer of reception

frequency data in BCD code, and are synchronized with the time division pulse. The reception frequency data is handled in BCD code by the A–D terminals during the T1–T3 timing, and by the A terminal during the T4 timing(see Table 2). Furthermore, during the T4 timing, the B, C, and D terminals are utilized in designating the operational mode of the synthesizer IC(TC9123-GR) as shown in Table 3.

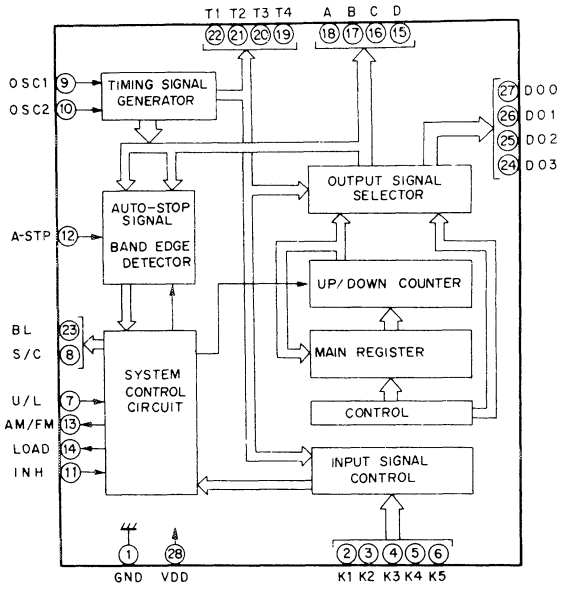


Fig. 4-8 Block Diagram of the Synthesizer Control LSI

Input Terminals(K1–K5):

K1–K5 handle the different command inputs according to the function key input and the relevant T1–T4 timing.

Operation Designation:

A K5 input determined according to T2 timing corresponds to FM mode, while a similar input determined according to T1 timing corresponds to AM mode. By applying an input to U/L according to T3 timing, the FM reception band is switched to FMU(87.5–108MHz), while applying an input to K1 according to T1 timing switches the operation over to FME mode(50kHz steps). Unless otherwise specified, AM reception is in AM2 mode.

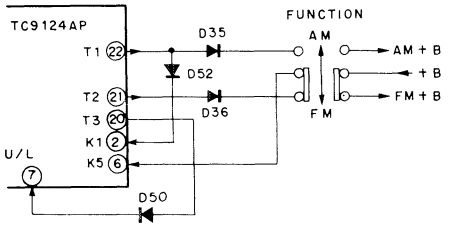


Fig. 4-9 Operation Designation

Table 2: Reception Frequency Data

Code	T1		T2		T3		T4
A	frequency	1		10		100	1000
B	data unit	2		20	hundred	200	reception
C		4		40		400	mode
D	digit:	8	ten digit	80	digit	800	designation

Table 3: Operation Designation Data

Mode	B	C	D	Remarks
FMU	1	1	1	FM 87.5–108MHz
FME	(0 or 1)	1	1	FM Europe: 50kHz steps
FML	1	0	1	FM 76–90MHz
AM1	0	1	0	AM inter-station steps:10kHz
AM2	0	0	0	AM inter-station steps: 9kHz

Manual Tuning:

With an input applied to K4 according to T3 timing for a short period of time, the reception frequency is shifted downwards in steps of 50kHz during the FM mode, and 1kHz during the AM mode. If the input is applied longer than a specified length of time, the down shift will proceed at a rapid rate, coming to a stop only when the input is stopped. Likewise, when an input is applied to K4 according to T4 timing, the reception frequency is shifted upwards(see fig.4-10). Note that during manual tuning, the reception frequency shift will stop when either the upper or lower band edge is reached.

Auto Scan Tuning:

The auto scan tuning mode is activated when an input is applied to K1 according to T2 timing.

When the AUTO/MANUAL (TUNING MODE) switch (see fig.4-10) is set to the AUTO position, the emmitter of Q4 is connected to K1. If Q3 has been turned off with the base of Q4 connected to T2, Q4 will subsequently turn on and off synchronized by T2. When either the UP or DOWN key is pressed, T3 or T4 will charge up C9 via D4, resulting in Q2 being turned on once the base voltage has reached a certain value. Q3 will consequently be turned off, and Q4 will operate according to T2 synchronization. An input synchronized by T2 will then be applied to K1, resulting in the start of the reception frequency scanning. This scanning action will commence almost as soon as either the UP or DOWN key is pressed, and will continue after the key is released. If either band edge is reached, the reception frequency scanning will not stop, but proceed in the reverse direction.

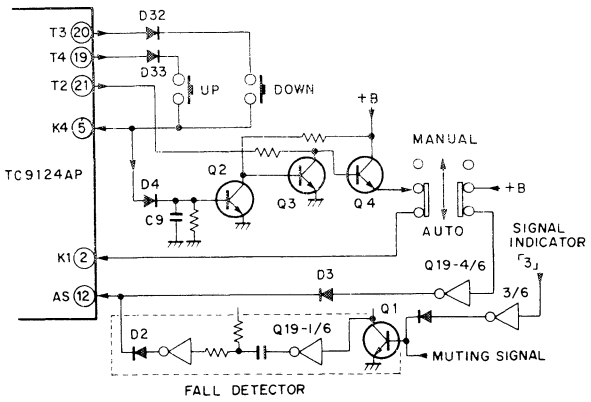


Fig. 4-10 Scan Command Circuit

The scanning will stop as soon as the AS terminal of the IC is switched to H(high level). If the SIGNAL indicator(5-point display)reads "3" or more, and if there is no muting signal, a stop pulse will be applied to the AS terminal to stop the scanning. The generation of the stop pulse is described later under section 4.6, "Muting Control Circuit".

Since there is no means for detecting the carrier frequency during the reception of AM broadcasts, the scanning operation would be likely to stop 1 or 2kHz prior to the actual central frequency when the input signal is very strong. So in order to avoid the this, the auto scan mode has been programmed to stop only at frequencies which are integer multiples of 9kHz (AM2 mode) or 10kHz (AM1 mode), depending on the position of the frequency lock selector switch.

Preset Tuning:

The 5100 can store up to 6 FM frequencies and 6 AM frequencies in it's memory. When an input is applied to K2 according to T2 timing(MEMORY key), and then an input applied to K1–K3 according to T3 and T4 timing within a prescribed length of time (a few

seconds) (STATION CALL key), the tuned frequency will be stored in one of the memories 1 to 6(see fig.4-11 and Table 4). By switching the FM/AM FUNCTION key, frequencies may also be stored in memories 7 to 12.

Then when a station call key (1–6)only is pressed, the frequency data stored in the corresponding memory may be retrieved for immediate tuning to that frequency.

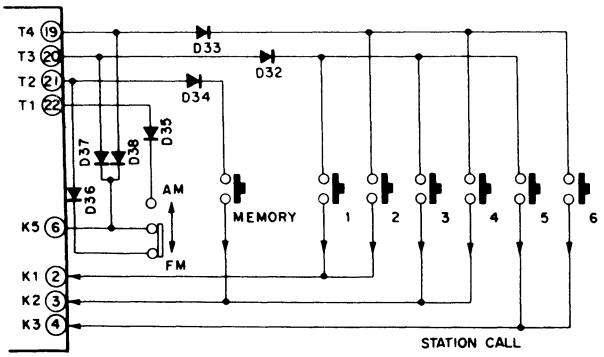


Fig. 4-11 Memory Write-In

Table 4: Memory Designations

	T3	T4	T2
K1	Memory (1)	Memory (2)	.....
K2	(3)	(4)	Memory write-in
K3	(5)	(6)	.....

Auto Memory:

When the FM/AM FUNCTION key is switched back and forth, the reception frequency data(in the main register)is automatically transferred to the sub register, and the contents of the sub register automatically transferred to the main register(i.e. exchange of data). This operation is program controlled. Consequently, whenever the FM/AM key is switched over, the formerly tuned frequency is retuned automatically, thereby eliminating the need to repeat tuning procedures again for that station.

NOTE: In export models, FM frequencies tuned to the nearest 50kHz cannot be sotred in the sub register. The final digit is automatically dropped off.

Memory Holding When Power Switched Off:

When the synthesizer control IC(TC9124AP)INH terminal is switched to L(low level), an inhibit function is activated. The complete supply of operation clock signals within the IC is consequently stopped, thereby putting the IC into a complete static condition. And this condition is maintained as long as the inhibition is applied - there being no inputs or outputs handled whatsoever, even when any of the operation keys is depressed. Since this is a C-MOS IC, the power consumption during inhibition mode is extremely small(measured in microamps).

The 5100 power switch is mounted in the secondary side of the power transformer, and this maintains the TC9124AP power supply even after the power switch has been turned off(see fig.4-12). In this case, if the AM+B and FM+B supplies are stopped, the memories will be maintained under inhibit mode. Furthermore, if the AC line supply is disconnected altogether, the memories will still be maintained(for 3 to 4 days) by means of a large capacitor(C130).

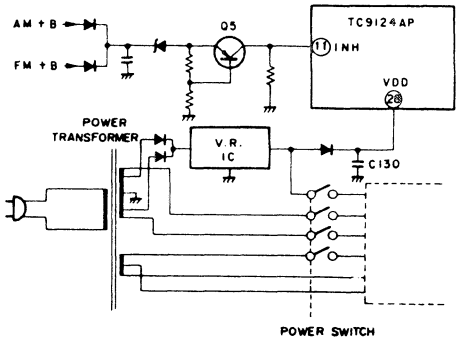


Fig. 4-12 Memory Power Supply Circuit

4.5. DISPLAY CIRCUITS

Frequency Display:

Frequencies received in the 5100 are displayed by a 4-digit digital display made up of flourescent indicator tubes.(In export models, the FM 50kHz and +25kHz offset are indicated by LED lamps.) Each digit consists of 7 segments(a to g as shown in fig.4-13) used to display numbers from 0 to 9(the first digit, however, consists of only 2 segments, b anc c).

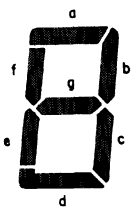


Fig. 4-13 7-Segment Digit Display

TC9124AP transfers the T1—T4 time-shared reception frequency data in BCD code from the A, B, C, and D terminals as shown in Table 2(p.14). This data is then converted into decimal number 7-segment display signals by a BCD-to-7-segment decoder IC (TC5022BP)(see fig.4-14). The 7-segment display data is passed via the non-invert buffer IC(TC5066BP)and applied to the anode of each segment(a—g)of the flourescent indicator tube. The same segments in each digit are connected in paralled, while each digit has an independent grid. T1, T2, T3, and T4 are applied independently to that grid, each digit being turned on following sequential scanning to produce the frequency display.

Since the T4 timing B, C and D do not handle frequency data(but are used for designating the TC9123-GR operational mode instead), Q26 has been designed to turn on at T4 timing, and B, C and D then grounded via D27—D29 to thereby prevent unwanted input signals from being applied to TC5022BP.

Display blanking signals appear at the BL terminal of TC9124AP during the T1—T4 switching periods(see fig.4-4). When these signals are then connected to the BI terminal of TC5022BP, all TC5022BP output signals are switched to L(low level)when the display blanking signals are applied. The a—g segments are thus turned off, thereby preventing any blurring occurring in the frequency display.

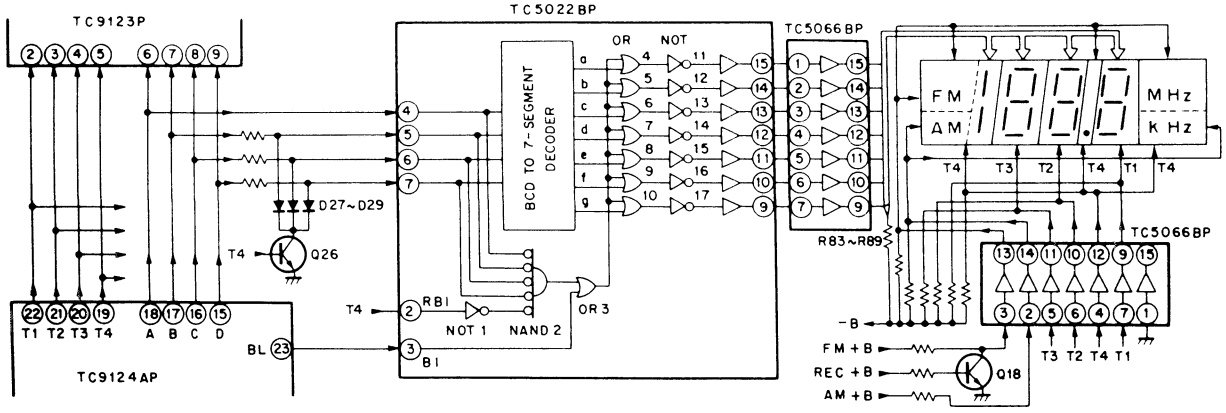


Fig. 4-14 Reception Frequency Display Circuit

* Supression of 1st Digit Zero:

Since there are 4 digits in the frequency display, the 1st digit will be 0 for any frequency under AM 1000kHz and FM 100.0MHz. In order to eliminate this zero(which in fact would turn out to be a "1" since the 1st digit only contains the b and c segments), T4 is applied to the RBI terminal of TC5022BP.

The 1st digit would be set to 0 when A is switched to L(low level), but set to 1 when A is switched to H(high level)according to T4 timing. And since Q26 is turned on at T4 timing, B, C and D are switched to L. The RBI terminal input (T4) is inverted by NOT1 to L. So if A is switched to L at T4 timing, the NAND2 inputs will both become L, and the output H. The OR3 output will thus be switched to H, resulting in all TC5022BP outputs being switched to L. Hence, there will be no zero display at the 1st digit.

*50kHz Indicator(Export Model Only):

By shifting the reception frequency by +50kHz with every second step during FM reception, the 5100 is capable of receiving frequencies in 50kHz steps(basic operation in 100kHz steps). With every second step a shift signal (12.5kHz)appears at pin 11 of the of the synthesizer IC TC9123-GR (see fig.4-15). Q31 is subsequently turned on and off by this shift signal, thereby turning the 50kHz indicator LED on and off. (Q31 is turned on when pin 11 is switched to H in the absence of a shift signal.)

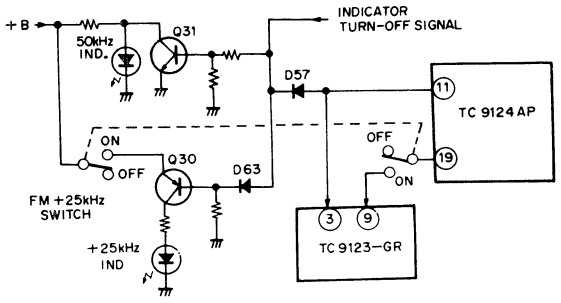


Fig. 4-15 50kHz and +25kHz Indicator Circuit

*25kHz Offset Indicator(Export Model Only):

When the FM +25kHz offset switch is turned on, Q30 is turned on and the +25kHz indicator (LED) lights up. Q30 is turned off by the indicator turn-off signal passed via D63, resulting in the indicator lamp being turned off. The voltage applied to the base of Q30 from pin 11 via D63 does not reach a level sufficient to turn the Q30 transistor off.

*AM and kHz Indicators:

During AM reception AM + B is passed via a buffer amplifier and applied to the flourescent indicator tube AM and kHz display segment anodes. T4 is applied to the grid for the tube to light up in T4 timing.

*FM, MHz and Decimal Point:

During FM reception FM + B is passed via a buffer IC(TC5066BP) and applied to the anodes of the flourescent indicator tube FM, MHz and decimal point indicator segments. When the REC LEVEL CHECK switch is turned on, REC + B is applied to the base of Q18 resulting in the transistor being turned on, and blocking the FM + B applied to the segment anodes. T4 is applied to the grid, and the segments light up in T4 timing.

Station Memory Display

D01—D03 of TC9124AP obtain the memory(1—12) call indicator output according to T1—T4 timing(see Table 5). Since the 5100 stores up to 6 AM frequencies(in memories 1—6) and 6 FM frequencies(in memories 7—12), and indicates these by means of 6 indicator lamps (ST1—ST6), memories n and n + 6 (n=1—6)will be shown by the same LED indicator(see fig.4-16).

Table 5: Memory Display

	T1	T2	T3	T4
D01	Memory (1)	Memory (2)	Memory (3)	Memory (4)
D02	(5)	(6)	(11)	(12)
D03	(7)	(8)	(9)	(10)

The memory write-in display output is obtained from D00 according to T4 timing. When the MEMORY key is pressed and the MEMORY indicator LED (D43)lights up, data may be written into the memory. If a STATION key is then pressed during this condition the tuned frequency will be stored in the memory, and the MEMORY indicator lamp subsequently turned off. If none of the STATION keys are pressed within 2 to 3 seconds, the write-in enable status will be released and the MEMORY indicator LED turn off.

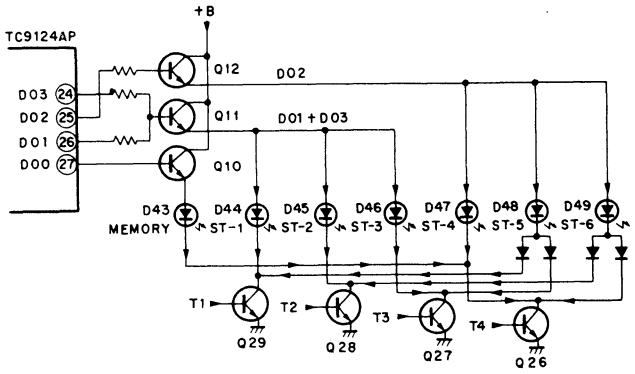


Fig. 4-16 Station Indicator Circuit

Signal Indicator:

The 5100 signal meter is a 5-point LED display meter driven by the meter drive IC(LB1405)(see fig.4-17). The signal meter drive signals from the FM and AM tuner sections are applied to a set of 5 voltage comparators which are activated according to the difference between the applied signal level and the respective reference voltage levels allotted to each comparator. Q51—Q55 are thus turned on according to a priority basis, resulting in the corresponding LED's

(1–5) being turned on.

Lighting up of the SIGNAL 3 lamp denotes stop data whereby H(high level)is transferred to the stop signal generator circuit.

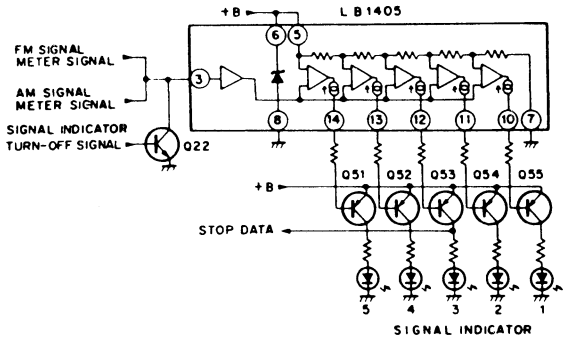


Fig. 4-17 Signal Indicator Circuit

4.6. MUTING CONTROL CIRCUIT

A block diagram outline of the muting control circuit is shown in fig.4-18. By various combinations of the 1–9 detector circuits, the auto-stop signal and stereo/mono switching signal, the muting signal and the signal indicator turn-off signal may be obtained.

* When Signal Indicator Reads (3) or More:

This stop data is used to halt the auto scan mode. When SIGNAL 3 lights up(see fig.4-17), an H output(high level) is obtained.

*FM Noise Detector:

This detector is employed in preventing mis-operation of the muting and auto-stop circuits caused by strong FM input signals and TV interference. High frequency noise components in the FM detector output(pin 6 of PA3001-A)are detected by a high-pass filter, and rectified into a DC output(see fig.4-19).

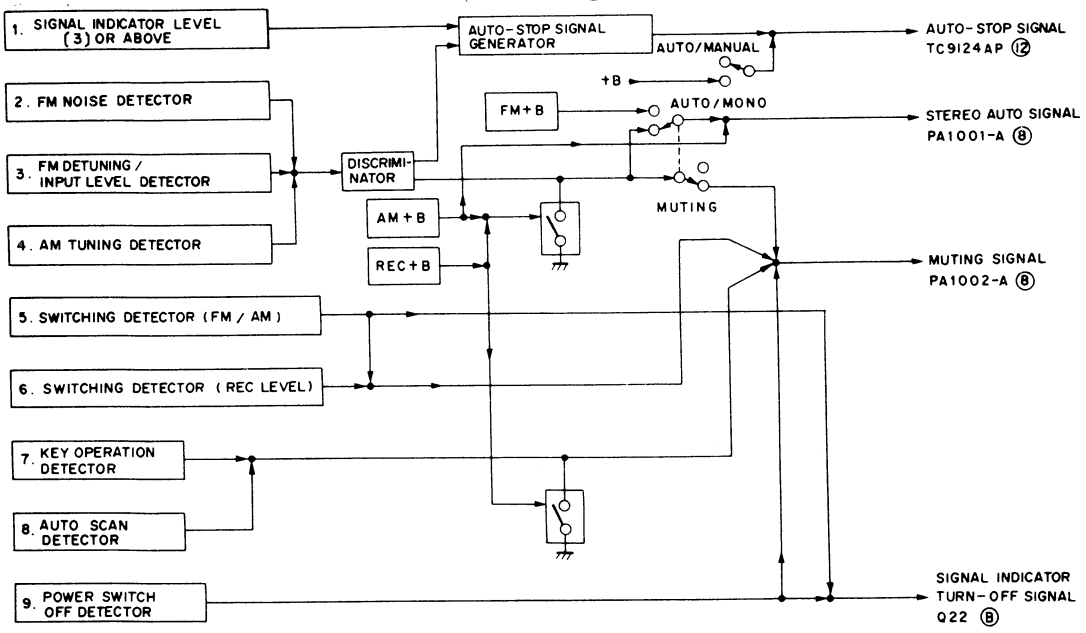


Fig. 4-18 Outline of the Muting Control Circuit

*FM Detuning/Input Level Detector

When the input level is very weak, or when tuning away from a station, a DC voltage appears at pin 12 of the FM IF system IC(PA3001-A). This voltage serves as a signal source. During AM reception Q12 is turned on by AM + B, thereby stopping the output from this detector(see fig.4-19).

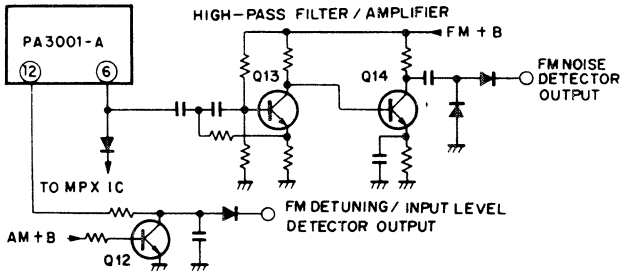


Fig. 4-19 FM Muting Signal Detector

*AM Tuning Detector

This circuit detects the auto scan stop data signal during AM reception(see fig.4-20). The tuning condition is detected by applying the AM IF signal to a narrow band filter and then amplifying and rectifying the signal. In order to simpligy tuning discrimination, Q20 is employed in automatic gain control(positive feedback)for more precise detector performance. The rectified output is inverted by Q23, and the AM tuning detector output is switched to L(low level) when the frequency is tuned. The rectified output is also passed via Q21 to become the AM tuner signal meter drive output.

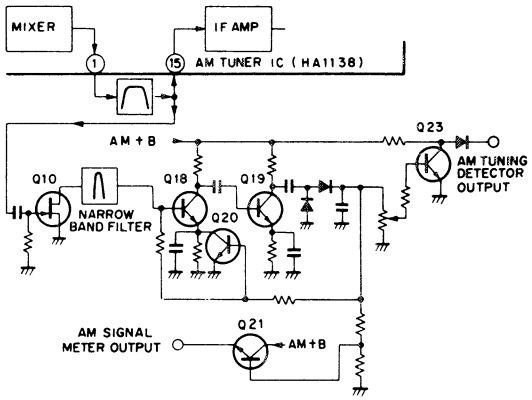


Fig. 4-20 AM Tuning Detector

NOTE: Although accurate tuning cannot be detected by this circuit alone, the mechanism by which the auto scan tuning mode is stopped only at frequencies which are multiples of 9kHz or 10kHz(depending on selection)does enable accurate tuning.

*Switching Detector:

When the FUNCTION switch(S4), the REC LEVEL switch(S2), or the FM +25kHz offset switch(S15 - export models only)are pressed, this circuit detects the switching of the power supply, and activates the relevant muting circuit during that period(see fig. 4-21).

When S2, S4, and S15(export models only)are in their normal positions, Q6, Q7, and Q25 will be turned off because of the reverse bias applied via D10, D11, D13, D15, D53, or D54. Note that S2, S4, and S15(export model)are all non-shorting type switches.

When S4 is switched over, the Q6 and Q7 transistors are turned on temporarily due to the loss of reverse bias to their bases. During this brief period, C14 and C15 are charged up rapidly thereby increasing the Q6 and Q7 collector voltages. These voltages thus serve as the detector signals and are passed via D16 and D17. Q6 and Q7 are turned off again soon after, but because of the charge on C14 anc C15, the outputs are maintained for a

longer fixed period of time.

When S2 is switched with S4 in the FM position, the reverse bias applied to the base of Q7 is cut, resulting in the transistor being turned on temporarily. Consequently, C15 is charged up rapidly thereby increasing the Q7 collector voltage. This voltage is then passed via D16 as the detector signal. When S4 is in the AM position, reverse bias will be applied to Q17 via D13 irrespective of the S2 switching, so no detector signal will be obtained.

When S15 is switched, the reverse bias applied to the base of Q25 is cut, resulting in the transistor being turned on temporarily. C37 will consequently be charged up rapidly, resulting in the increase of the Q25 collector voltage which subsequently serves as the detector signal passed via D56.

Note that the S4 switching detector signal is also used as the SIGNAL indicator turn-off signal passed via D12(the connection to the base of Q22 in fig.4-17).

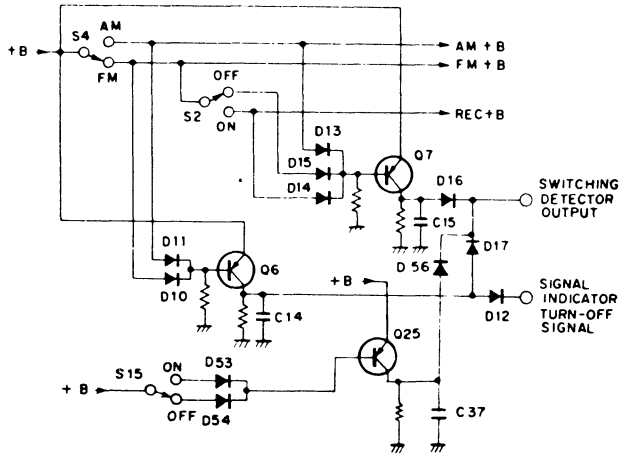


Fig. 4-21 Switching Detector

*Key Operation Detector:

This circuit is designed to detect operation of the UP, DOWN, MEMORY 1, 2, 3, 4, 5 and 6 STATION CALL keys, and to subsequently activate the relevant muting circuits.

The various command input signals generated by key operation are applied to K1–K4 of TC9124AP according to T2–T4 timing. These command signals are detected by being passed via D20–D23, and then converted into a continuous detector output signal by D9 and C12(command signal:T2–T4 timing pulse). Note, however, that in order that the muting circuits be not activated for the command signal applied to K2 at T2 timing(memory write-in) and the command signal applied to K1 at T1 timing(in export models, FM 50kHz step operation designation - not a command signal generated by key operation), Q9 is designed to turn on at T2 and T1 timing, thereby blocking any detector output signal (refer to NOTE below). Furthermore, since muting is not required for key operation during RED LEVEL CHECK operation, REC+B is used to turn Q9 on to again block any output signal.

NOTE: Although muting is required for the command signal(auto scan)applied to K1 at T2 timing, the UP or DOWN key is pressed to start the auto scan mode, resulting in the command signal being applied to K4 at T4 or T3 timing prior to the auto scan command. And this is sufficient to generate the detector signal.

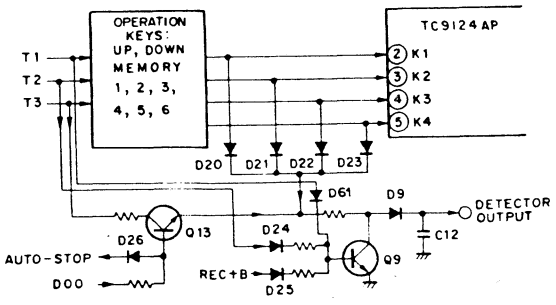


Fig. 4-22 Key Operation/Auto Scan Detector

*Auto Scan Operation Detector:

This circuit is responsible for muting during auto scan mode. During this mode the display signal output appears at the DO0 terminal of TC9124AP at T3 timing. This output is synchronized by Q13, and converted into a continuous output signal by D9 and C12 following detection(see fig.4-22). When a particular frequency is tuned, the D26 cathode voltage is decreased(connected to the inverter (1)–(2) output in fig.4-24), resulting in the output being blocked by Q13.

*Power Off Detector:

Transient noise generated when the power switch is turned off is muted as a result of this detector circuit(see fig.4-23). When the power is on, the AC voltage applied via C113 is rectified by D28 to form the forward bias used to turn Q25 on. Since the time constant for this bias circuit is very short, Q25 is turned off almost immediately as the power is turned off, resulting in the B+ residual voltage being passed via D27 to form the output detectir signal.

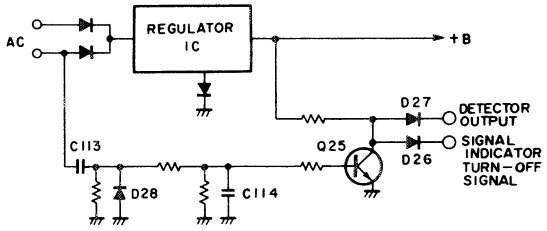


Fig. 4-23 Power Off Detector

This detector signal is also passed via D26 to be used as the SIGNAL indicator turn-off signal(connected to the base of Q22 in fig.4-17).

Auto Stop Signal Generator Circuit:

The auto-stop signal is used to half the auto scan mode(fig. 4-24). Detector data 1(see fig.4-18 for data numbers)is inverted by inverter(5)–(6), and applied to the base of Q1. Since data 1 is the H(high level) obtained from the SIGNAL indicator circuit (fig.4-17)when SIGNAL 3 is lit up, the inverter(5)–(6)output is switched to L(low level)by SIGNAL 3 and above. Detector data 2 and 3 correspond to correct runing during FM reception, and L (low level)output during AM reception. Furthermore, detector data 4 corresponds to tuned status during AM reception, and low level output during FM recpetion. Consequently, when a frequency is tuned during either AM or FM reception, the Schmitt circuit output is switched to L. As a result, if SIGNAL 3 indicator lights up when an AM or FM frequency is tuned, Q1 is turned off, and the collector voltage increased. This voltage is then inverted by inverter(1)–(2), and differentiated by C2/R6 in order to detect the voltage change. The resultant voltage is inverted by inverter(3)–(4), rectified, and then applied via D2 to the AS terminal of TC9124AP as a positive pulse(detected when Q1 is turned off). The auto scan mode is thus brought to a stop.

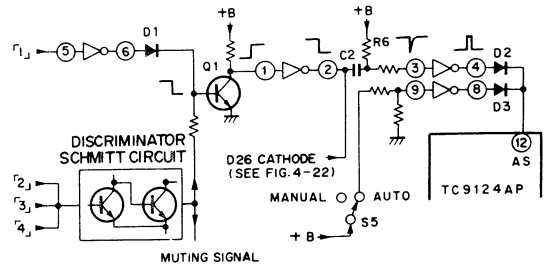


Fig. 4-24 Auto-Stop Signal Generator Circuit

If S5(TUNING MODE switch)is set to the MANUAL position, the AS terminal is switched to high

level via D3, thereby preventing commencement of the auto scan operation.

Muting Gate Control:

The 5100 muting gate is incorporated in the AF IC(PA1002-A). Besides gate control by ecternal input signals(via pin 8), this circuit is also involved in the delayed connection when the power switch is turned on(making use of an external timing capacitor C106).

Detector data 2, 3, and 4 is applied to S3(MUTING switch) via the Schmitt circuit. During AM reception and REC LEVEL CHECK operation, Q8 is turned on, thereby blocking the detector data 2, 3 and 4. During FM reception, S3 is turned on, and the detector data 2, 3 and 4 switched to L once a particular frequency is tuned, thereby releasing the muting status (data 4 switched to L since AM tuning detector citcuit is not operated during FM reception).

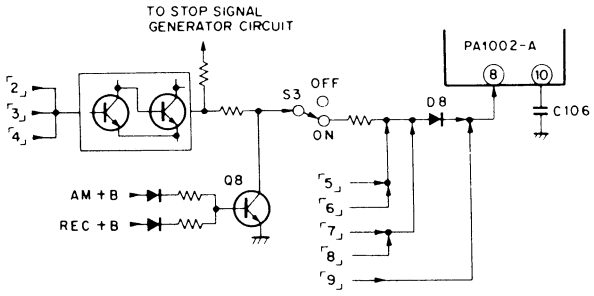


Fig.-4-25 Muting Signal Circuit

Detector data 5–9 is employed in opening and closing the muting gate irrespective of the S3(MUTING switch)position. Note, however, that detector data 7 and 8 is blocked during REC LEVEL CHECK operations.

4.7. REC LEVEL CHECK SIGNAL GENERATOR CIRCUIT

The astable multivibrator composed of two C-MOS inverters generates a signal of approximately 330Hz.

Points A and B in fig.4-26 are maintained at opposite phase by inverter(so the 2 points are either H and L or L and H). And since point C is also maintained at opposite phase point A by inverter, C3 is charged up(or discharged)via R8, thereby bringing the level closer to that at point A. When the level at point A meets the inverter threshold level, inverter (13)–(12) is inverted, resulting in the level at point A being inverted as well. As a result, inverter (11)–(10) is also inverted, thereby inverting the level at point B. Continuous repetition of this procedure results in the generation of a square wave signal. The sharpness of this signal is blunted by C4 and C5, and the resultant signal then applied to VR1 for use in level adjustments.

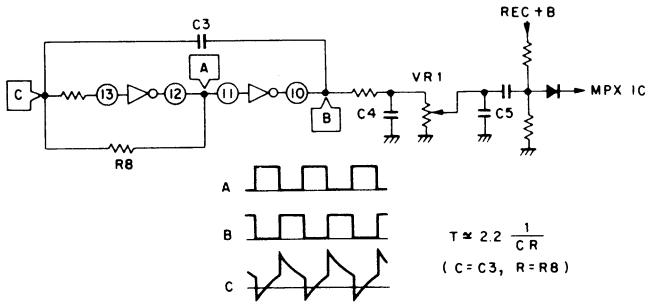


Fig. 4-26 REC LEVEL CHECK Signal Generator

5. DISASSEMBLY

TOP COVER:

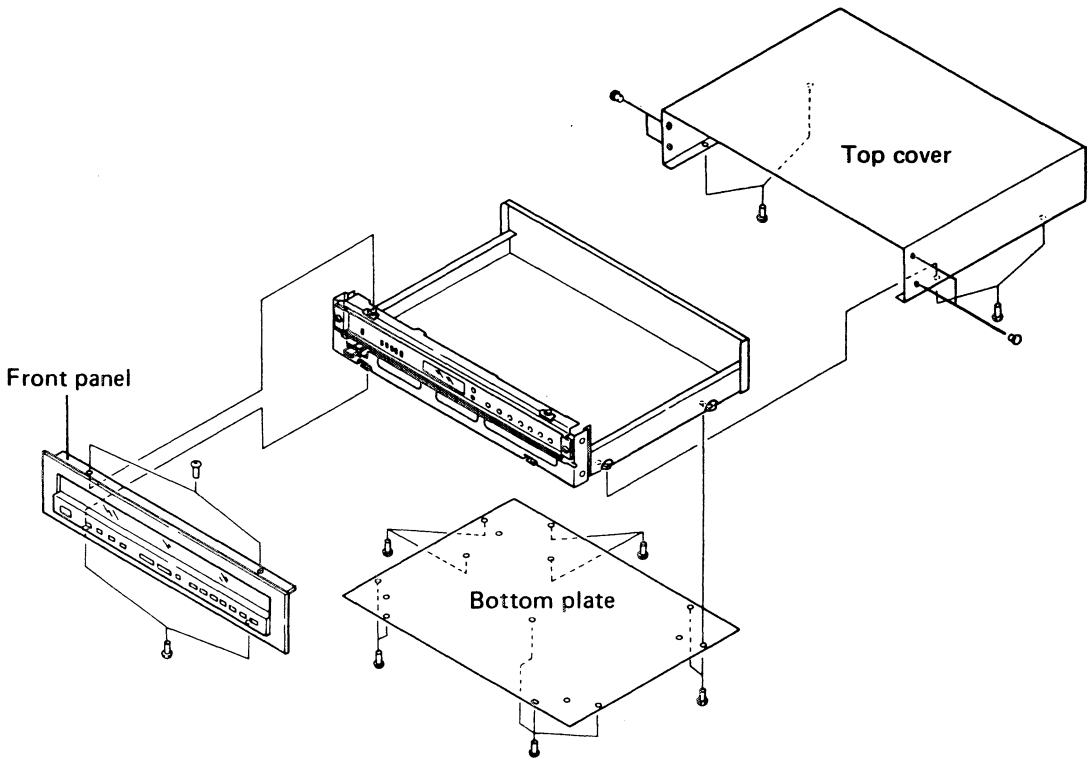
1. Pull off the two caps on each side of the top cover.
2. Remove the four screws from the bottom edge of the top cover.

BOTTOM PLATE:

Remove the eleven screws to detach the bottom plate.

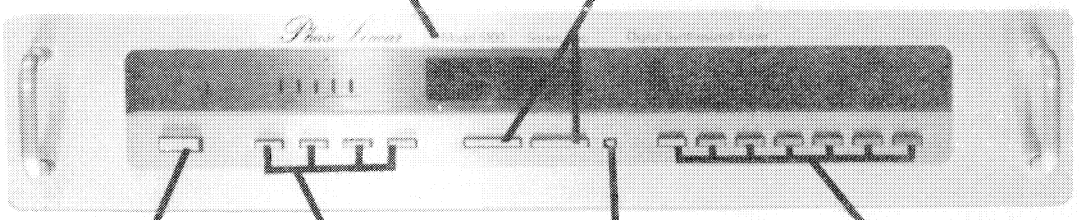
FRONT PANEL:

Remove the four screws from the top and bottom edges.

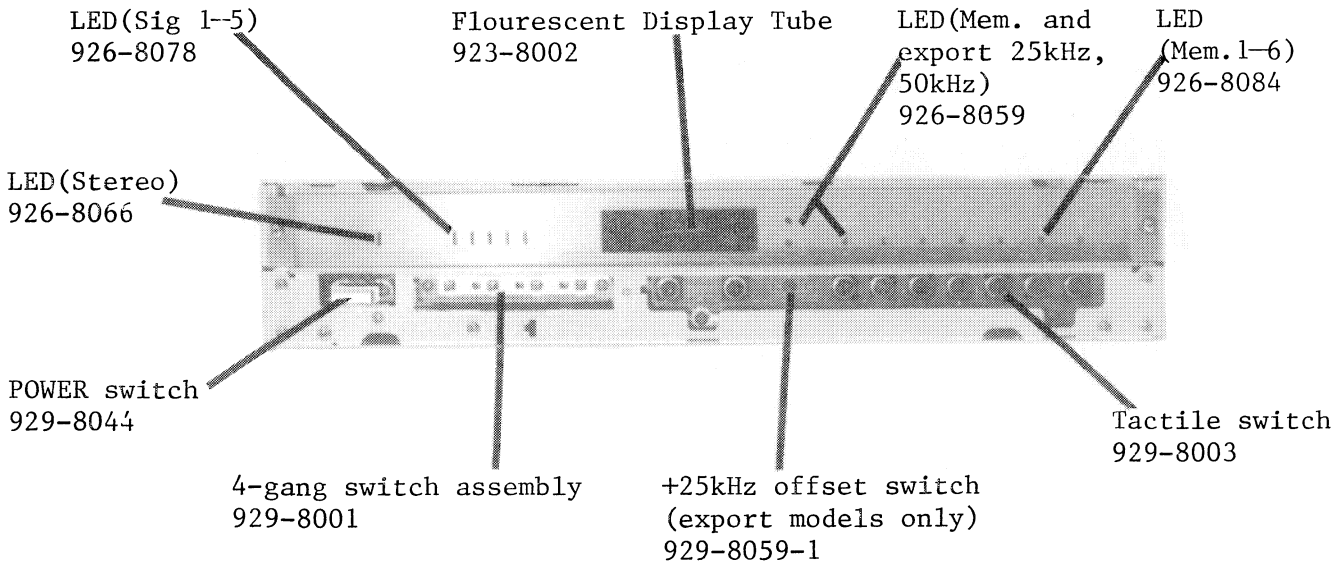


6-0. PARTS LOCATION
with PART NUMBERS

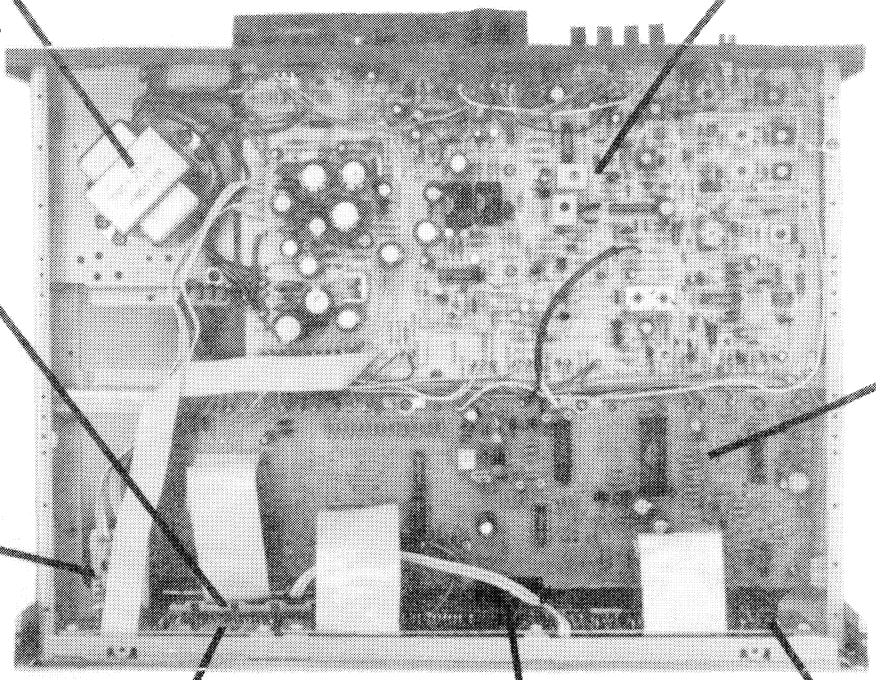
Front Panel View



Front Panel View with Panel Assembly Removed



Top View



Power transformer
925-8012
(export model,
925-8031-1)

Tuner PCB assembly
901-8020
(export model,
901-8030-1)

Function switch
PCB assembly
901-8015
(export model,
901-8029-1)

Synthesizer PCB
901-8014
(export model,
901-8027-1)

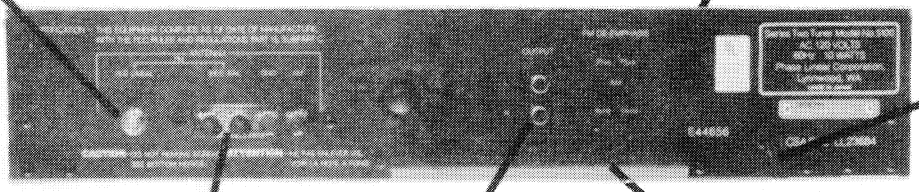
POWER switch
PCB assembly
901-8021
(export model,
901-8025-1)

LED PCB assembly
901-8022
(export model,
901-8028-1)

+25kHz Switch PCB
(export model only)
901-8024-1

Display PCB assembly
901-8013
(export model,
901-8026-1)

Rear Panel View



Coaxial connector socket
921-8063

Top/side cover
941-8013

AC line cord
921-8061

Antenna terminal assembly
921-8065

Output jack assembly
921-8009

Bar antenna assembly
930-8017

7.ADJUSTMENTS

7.1. AM TUNER

1. Connect an AM signal generator(AM SG) to the AM ANTENNA terminal via a lk-ohm resistor.
2. Set the FUNCTION switch to the AM position.
3. Set the 5100 frequency display to 531kHz(with no input signal).
4. Adjust the core of L5 to obtain a DC 2V reading between ground and no.1 terminal of the tuner assembly.
5. Then set the 5100 frequency display to 1602kHz(again with no input signal).
6. Adjust TC5 to obtain a DC 25V reading between ground and no.1 terminal of the tuner PCB assembly.
7. Repeat steps 3 through 6 until both specification requirements are satisfied.
8. Set the 5100 frequency display to 600kHz.
9. Set the AM SG output level to 30dB(modulation 400Hz, 30%) and the AM SG output frequency to 600kHz(fine adjust the AM SG output frequency to the position which gives maximum DC voltage level between ground and no.6 terminal of the tuner PCB assembly).

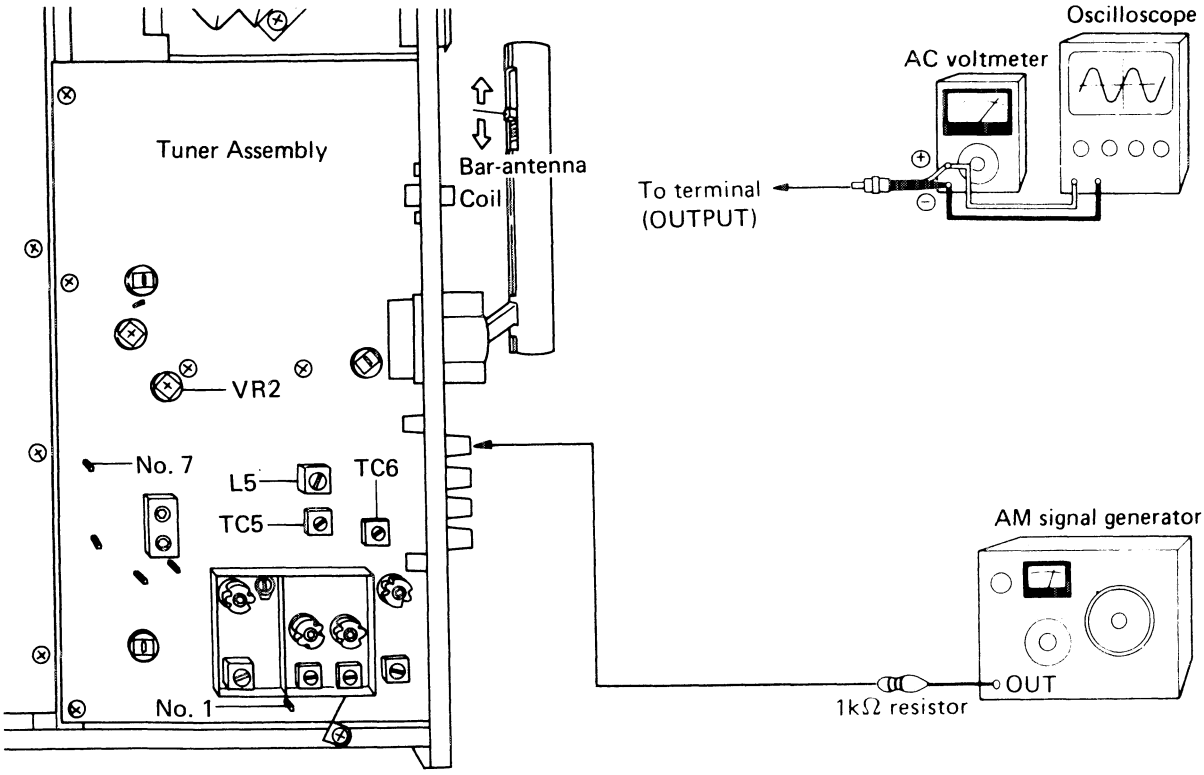


Fig. 7-1 AM Tuner Adjustment

10. Slide the bar antenna coil along the core to find the position which gives the maximum demodulated output(at the OUTPUT terminal).
11. Set the 5100 frequency display to 1400kHz, and tune the AM SG output frequency also to 1400kHz(fine tune the AM SG output frequency to obtain maximum DC voltage between ground and

no.6 terminal of the tuner PCB assembly).

12. Adjust TC6 to obtain maximum demodulated output at the OUTPUT terminal.
13. Repeat steps 8 through 12 until both requirements are satisfied.
14. Then set the 5100 frequency display to 1000kHz, and tune the AM SG output frequency to the same frequency(1000kHz). Fine tune this output frequency to obtain maximum DC voltage reading between ground and tuner assembly no.6 terminal.
15. Vary the AM SG output level continuously, and adjust VR7 so as to obtain voltage readings at no.7 terminal in the tuner PCB assembly of less than 0.5V(low level)when the 5-point SIGNAL indicator reads either 4 or 5, and at least 8V(high level)when the indicator reads 3 or less.

NOTE: When adjusting the 5100 export model, set the AM frequency lock selector to the 9kHz position.

7.2. FM TUNER

1. Set the FUNCTION switch to FM, and turn the REC LEVEL CHECK, FM MUTING, and FM +25kHz offset(only on export models) switches off.
2. Set the 5100 frequency display to 87.5MHz(87.55MHz on export model)with no input signal.
3. Adjust the core of L4 so that DC 6V registers between ground and no.1 terminal of the tuner PCB assembly.
4. Then set the 5100 frequency display to 108MHz, again with no input signal.
5. Adjust TC4 to obtain a reading of DC 20V between ground and no.1 terminal of the tuner PCB assembly.
6. Adjust the N core of T2 so that the voltage between no.4 and no.5 terminals on the tuner PCB assembly is reduced to DC 0V.
7. Tune to a well-known local broadcasting station or, if the exact frequency can be obtained, an FM signal generator output may be used.
8. Set the voltage between no.4 and no.5 terminals of the tuner PCB to DC 0V by means of the synthesizer PCB assembly VC1.
9. Repeat steps 2 through 6 above until both specification requirements are satisfied.
10. Connect an FM signal generator(FM SG)to the 300-ohm FM ANTENNA terminals via a 300-ohm dummy antenna.
11. Set eht 5100 frequency display to 90MHz.
12. Set the FM SG output level to 20dB(modulation 400Hz, ±75kHz deviation)and tune the FM SG output frequency to 90MHz(fine adjust the FM SG output frequency to obtain a voltage reading across no.4 and no.5 terminals of the tuner PCB of DC 0V).
13. Adjust L1, L2 and L3 to obtain maximum DC voltage reading between ground and no.6 terminal of the tuner PCB.
14. Next set the 5100 frequency display to 106MHz.
15. Also tune the FM SG output frequency to 106MHz and fine adjust the FM SG output frequency again to insure a DC 0V reading between no.4 and no.5 terminals of the tuner PCB.
16. Adjust TC1, TC2 and TC3 to obtain maximum DC voltage between no.6 terminal of the tuner PCB and ground.

17. Repeat steps 11 through 16 above until both specification requirements are satisfied.
18. Set the frequency display to 98MHz with no input signal.
19. Adjust the N core of T2 so that the voltage between no.4 and no.5 terminals of the tuner PCB reads DC 0V.
20. Raise the FM SG output level to 60dB(modulation 400Hz, ±75kHz deviation)and tune the FM SG output frequency to 98MHz. Fine tune the FM SG output frequency to obtain a voltage reading between no.4 and no.5 terminals of the tuner PCB of DC 0V.
21. Then adjust the D core of T2 to obtain minimum distortion in the demodulated output(OUTPUT terminal).
22. Repeat steps 18 through 21 until both requirements are satisfied.
23. Turn the FM MUTING switch on, and set the FM SG output level to 25dB.
24. Adjust VR1 to a position just prior to activation of the muting circuit at the same level.
25. Connect an FM multiplex generator(MPX SG)to the external demodulation terminal of the FM SG.
26. Withe the FM SG output level at 60dB, set it to zero demodulation.
27. Adjust VR3 to obtain a frequency reading at no.52 terminal on the tuner PCB of 76kHz(±250Hz).
28. Switch the FM SG modulation mode over to external, and set the MPX SG to Main Off and pilot signal ±7.5kHz deviation.
29. Adjust VR4 to obtain minimum leakage of the 19kHz pilot signal at the OUTPUT terminal.
30. Raise the FM SG output level to 80dB, and set the MPX SG to Main 1kHz L + R , ±67.5kHz deviation, and pilot signal ±7.5kHz deviation.
31. Adjust T1 to within ±90 degrees to obtain minimum distortion in the demodulated output (OUTPUT terminal).
32. Reduce the FM SG output level to 60dB, and reset the MPX SG to Main 1kHz L(or R)±33.75kHz, pilot signal ±7.5kHz.
33. Adjust VR5 to obtain minimum crosstalk between left and right channels.
34. Turn the REC LEVEL CHECK switch on.
35. Adjust VR1 in the synthesizer assembly to obtain a -6dB reading when the check signal(330Hz)output level is 100% modulated(±75kHz deviation).

NOTE: *The voltage on tuner assembly no.1 terminal is the tuning DC voltage applied to the tuning vari-cap (variable capacitance diode).

*Tuner PCB assembly no.4 and no.5 terminals handle the center tuning indicator meter deive output.

*Tuner PCB assembly no.6 terminal handles the signal strength indicator meter drive output.

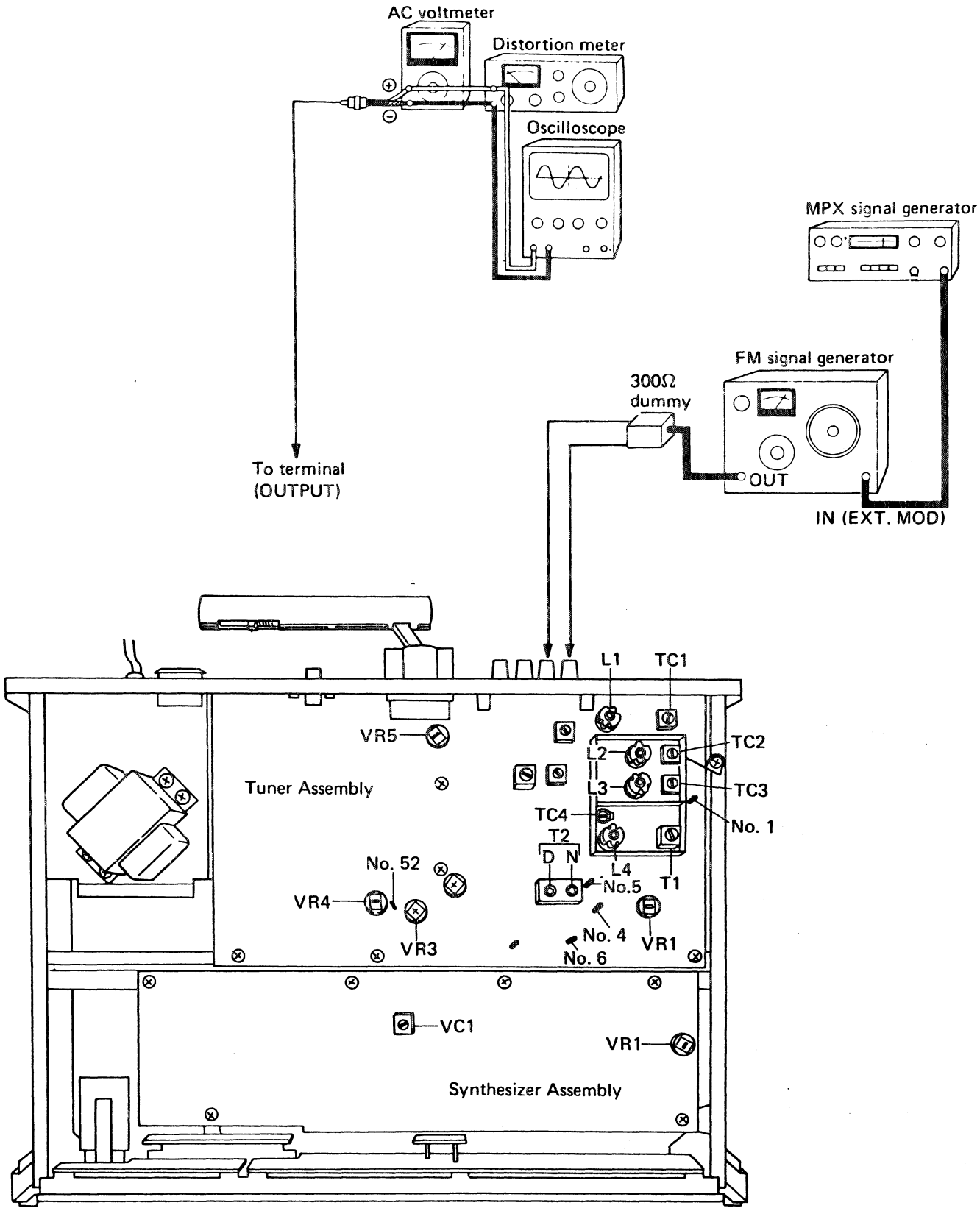
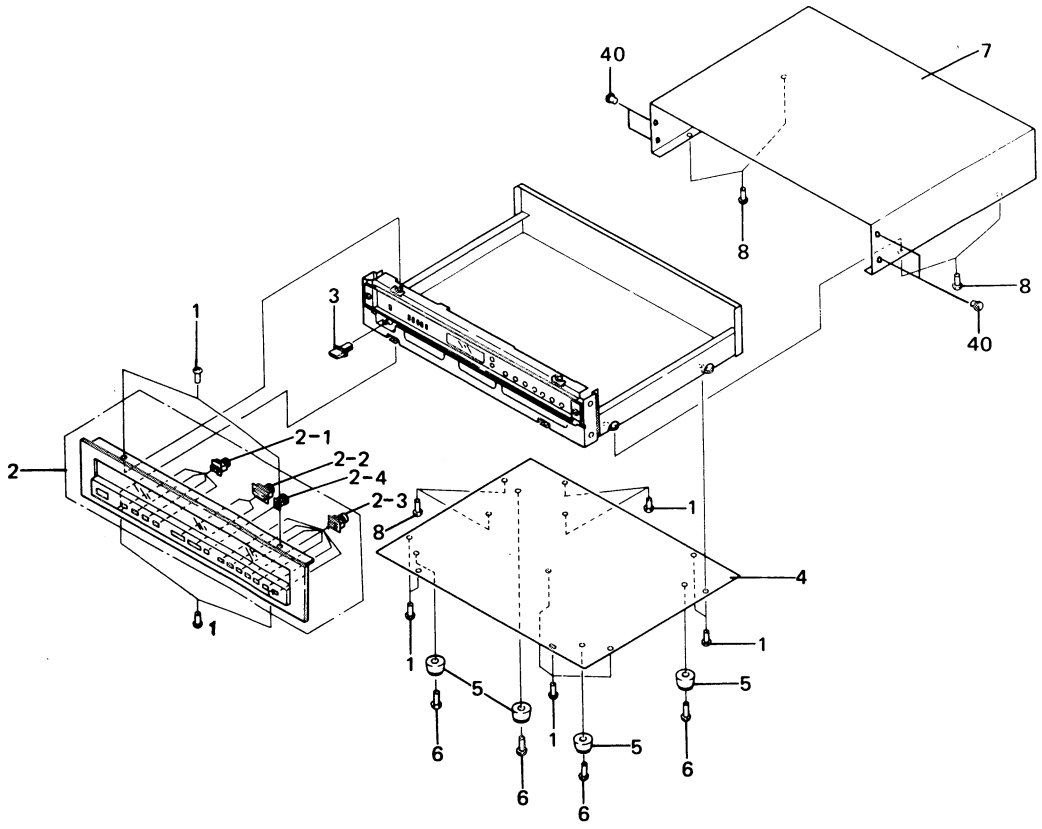


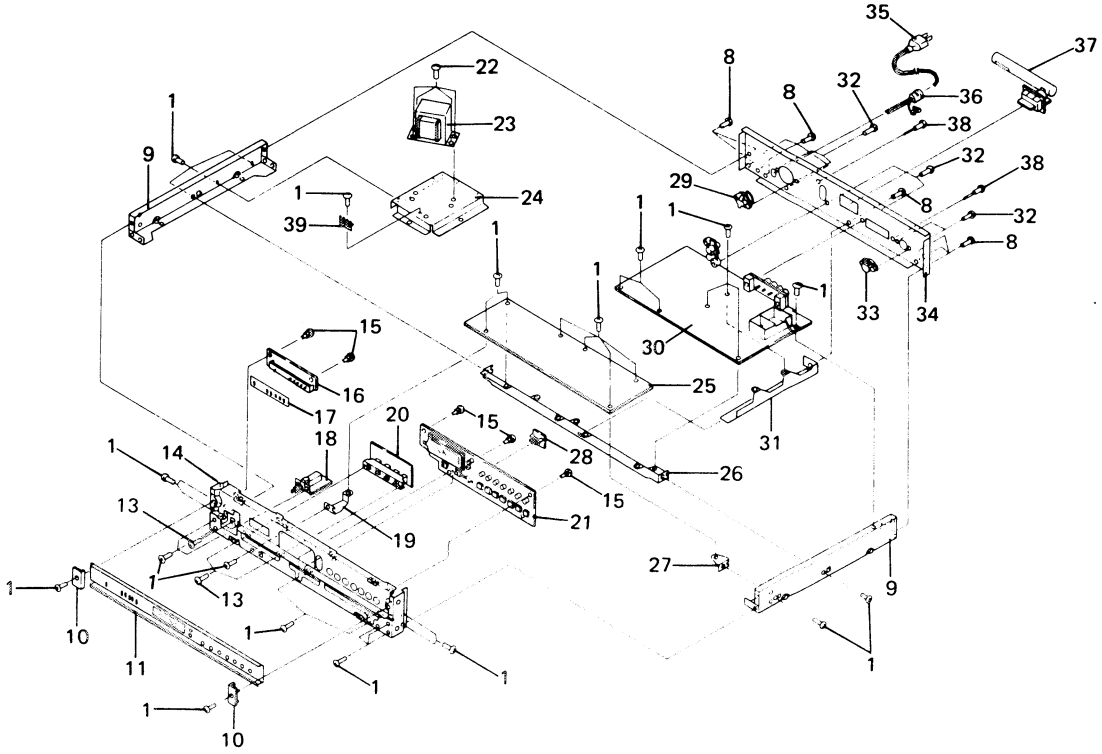
Fig. 7-2 FM Tuner Adjustment

8. EXPLODED VIEW

Exterior Components



Interior Components



PARTS LIST

NOTE: *Parts without part numbers CANNOT be supplied.

*The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.

Key No.	Part No.	Description
1	922-8001	Screw:PM3 x 6
2	930-8004	Front panel assy
	930-8038	Front panel assy (export model)
2-1	930-8002	Button assy (B)
2-2	930-8003	Button assy (C)
2-3	930-8001	Button assy (A)
2-4	930-8037	Button assy (D) (export model)
3	942-8034	Power button
4	941-8025	Bottom cover
5	942-8058	Foot
6	922-8086	Screw:RT4 x 16
7	941-8013	Top cover
8	922-8009	Screw:PM3 x 8
9		Side frame
10		Side retainer
11	930-8021	Display panel assy(not available for export model)
12	. . . . .	
13	922-8007	Screw:PM3 x 6
14		Sub panel
15	922-8023	Nylon rivet
16	901-8022	LED PC board
	901-8028	LED PC board(export model)
17		Mask
18	901-8021	Power switch PCB
	901-8025	Power switch PCB (export model)
19		PC board holder
20	901-8015	Function switch PC board
	901-8029	Function switch PCB(export model)
21	901-8013	Display PC board
	901-8026	Display PC board (export model)
22	922-8002	Screw:TT4 x 8
⚠ 23	925-8012	Power transformer
	925-8031	Power transformer (export model)
24		Transformer base
25	901-8014	Synthesizer PC board
	901-8027	Synthesizer PC board (export model)
26		Center frame
27		PC board holder
28	901-8024	Offset switch PCB (export model only)
⚠ 29	921-8062	Voltage selector (export model only)
30	901-8020	Tuner PC board
	901-8030	Tuner PC board(export model)
31		Sub frame
32	922-8006	Screw:BT3 x 10
33	921-8063	Coaxial connector socket
34		Rear panel
⚠ 35	921-8061	Line cord
36	921-8064	Strain relief
37	930-8017	Bar antenna assy
38	922-8008	Special screw
39		Ground terminal 4P
40	N/A	Plug(N/A)

11. PARTS LIST

NOTES: *When ordering parts, refer to ordering instructions on the separate price list.

*The ! mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.

MISCELLANEOUS PARTS:

Part No.	Symbol	& Description
925-8015	L1	RF choke coil
925-8012	T1	Power transformer
925-8031	T1	Power transformer (export model)
925-8017		Bar antenna assy
921-8062	S17	Voltage selector, (export model)
921-8061		AC line cord
921-8063		Coaxial connector socket
901-8020		Tuner PCB
901-8030		Tuner PCB, (export model)
901-8014		Synthesizer PCB
901-8027		Synthesizer PCB, (export model)
901-8022		LED PCB
901-8028		LED PCB, (export model)
901-8021		Power switch PCB
901-8025		Power switch PCB, (export model)
901-8015		Function switch PCB
901-8029		Function switch PCB(export model)
901-8013		Display PCB
901-8026		Display PCB, (export model)
901-8024		Frequency offset PCB(export only)

TUNER PCB ASSEMBLY(901-8020) (901-8030-exprt)

Coil, filters:

925-8032	T1	FM IF X-fmr
925-8002	T2	Detector X-fmr
925-8023	L1	FM antenna coil
925-8028	L2	FM RF coil
925-8025	L3	FM RF coil
925-8001	L4	FM osc. coil
925-8024	L5	AM osc. coil

coils, filters(cont.)

Part No.	Symbol	& Description
925-8015	L6–L8, L11	RF choke coil
925-8022	F1,F2	FM ceramic fltr.
925-8026	F3	AM ceramic fltr.
925-8034	F3	AM ceramic fltr. (export model)
925-8014	F4	AM ceramic fltr.
925-8033	F4	AM ceramic fltr. (export model)
925-8027	F5,F6	Low-pass filter

Semiconductors:

926-8064	Q1	3SK73-GR
926-8074	Q2	2SC535-B
926-8075	Q3	HA1201
926-8072	Q4–Q6, Q10	2SC1923-0
926-8086	Q8	2SK34
926-8082	Q9	HA1138
926-8098	Q11	PA3001-A
926-8095	Q12–Q16, Q21–Q23, Q25,Q27, Q28	2SC945A
926-8073	Q17	PA1001-A
926-8085	Q18–Q20	2SC461-B
926-8083	Q24	PA1002-A
! 926-8077	Q26	uPC78M12H
! 926-8047	Q29	uPC78M08H
926-8060	Q30	2SA684A
926-8070	Q31	TD6102P
926-8065	Q32	2SA733A-Q
926-8001	D1–D4	1SV68-04
926-8116	D6,D7 (twin-pack)	KV1226-Y
926-8037	D5,D8–D13, D16–D19, D22–D24	1S2473,
(926-8045	D26, D41–D43	1S2076)
925-8037	D27–D29,	
(926-8045)	D36,D37	1S2473 (1S2076)

Tuner Assembly
semiconductors(cont.)

Part No.	Symbol & Description	
926-8067	D14,D15, D20,D21	2-1K261
926-8054	D25,D40	WZ-061
926-8080	D39	WZ-240
926-8071	D30–D35, D38	10E2

Capacitors:

927-8008	TC1–TC3	Film trimmer
927-8006	TC4	Ceramic trim
927-8009	TC5,TC6	Film trimmer
927-8010	C100,C101	1650p/50v:poly
927-8011	C115–C120	.01/150v

Resistors:

929-8037	VR1	Trim:33k-B
929-8005	VR2	Trim:10k-B
929-8042	VR3	Trim:4.7k-B
929-8002	VR4	Trim:22k-B
929-8043	VR5	Trim:150k-B

Misc. Tuner PCB Components:

921-8065	Antenna terminal assy.
921-8009	Phono jack: dual:PCB-mount

SYNTHESIZER PCB ASSEMBLY(901-8014)
(901-8027–export)

Semiconductors:

926-8002	Q1–Q4, Q8–Q13, Q15,Q18	2SC945A-Q
926-8065	Q5–Q7, Q25	2SA733A-Q
926-8079	Q14,Q16	2SK61-GR
926-8085	Q17	2SC461-B
926-8058	Q19	uPD4069C
926-8099	Q20	TC9124AP
926-8063	Q21	TC9123-GR
926-8068	Q22	TC5022BP
926-8076	Q23,Q24	TC5066BP
926-8037	D1–D4, D6–D9, D12, D16–D29, D50,D61, D55–D57	1S2473

Synthesizer PCB
semiconductors(cont.)

Part No.	Symbol & Description	
926-8054	D5	WZ-061
926-8067	D10,D11, D13–D15, D53,D54	2-1K261

Capacitors:

927-8007	VC1	Film trimmer

Resistors:

929-8058	VR1	Trim:33k-B

Misc.Synthesizer PCB Components:

926-8105		Crystal resonator
925-8015	L2	RF choke coil

LED PCB ASSEMBLY(901-8022)
(901-8028-export)

Semiconductors:

926-8069	Q50	LB1405
926-8065	Q51–Q55	2SA733A-Q
926-8078	D50–D54	LED:yellow
926-8066	D55	LED:red

POWER SWITCH PCB(901-8021)
(901-8025-export)

929-8001	S2–S5	Switch assy: 4-station
926-8037	D30,D31, D58	1S2473

DISPLAY PCB ASSEMBLY(901-8013)
(901-8026-export)

Semiconductors:

926-8002	Q26–Q29, Q31	2SC945A-Q
926-8065	Q30	2SA733A-Q
926-8037	D32–D42, D52,D63	1S2473
926-8059	D43,D59 D60	LED:red
926-8084	D44–D49	LED:green

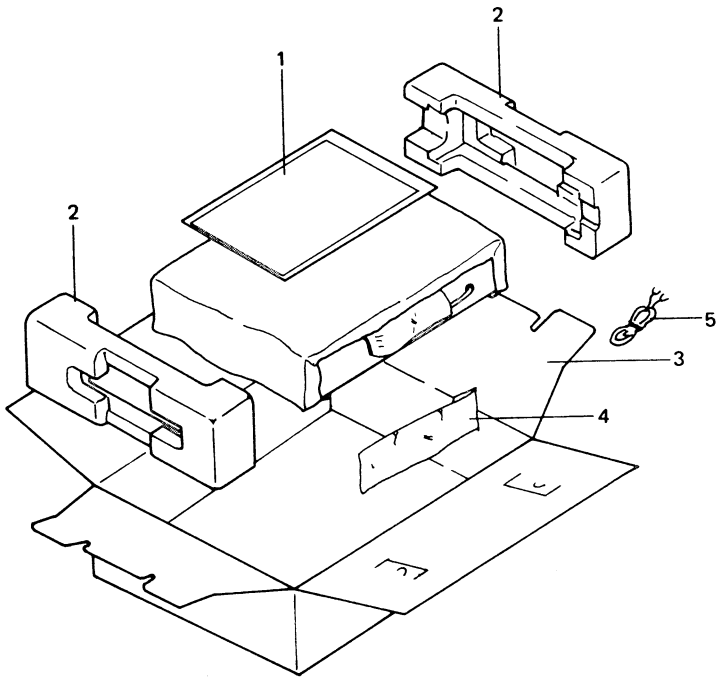
Misc.Display PCB Components:

929-8003	S6–S14	Switch:tactile
923-8002		FL display tube

SWITCH PCB(901-8024-export only)

929-8059	Switch:+25kHz

12. PACKING



Parts List:

Key No.	Part No.	Description
1	. . . .	Owner's manual
2	952-8010	Side liner
3	952-8009	Shipping box
4	921-8066	Patch cord
5	921-8067	T-type FM antenna

Phase Linear CORPORATION
20121 - 48th Avenue West, LYNNWOOD, WASHINGTON 98036 U.S.A. Telephone: (206) 774-3571

SERVICE BULLETIN 5/80

Model 5100II Tuner

The following are part number corrections in section 11(PARTS LIST)of the 5100 Series Two service manual:

1. p.36 MISCELLANEOUS PARTS:

currently reads		should read	
Part No.	Symbol & Description	Part No.	Symbol & Description
925-8017	Bar antenna assy	930-8017	Bar antenna assy

2. p.36 TUNER PCB ASSEMBLY

currently reads		should read	
Part No.	Symbol & Description	Part No.	Symbol & Description
Semiconductors:			
926-8116	D6,D7 (twin-pack) KV1226-Y	926-8119	D6,D7 (twin-pack) KV1226-Y

3. p.37 TUNER PCB ASSEMBLY

currently reads		should read	
Part No.	Symbol & Description	Part No.	Symbol & Description
Capacitors:			
927-8008	TC1—TC3 Film trimmer	927-8017	TC1—TC3 Film trimmer

4. p.37 TUNER PCB ASSEMBLY

currently reads		should read	
Part No.	Symbol & Description	Part No.	Symbol & Description
Misc. Tuner PCB Components:			
921-8065	Antenna terminal assy.	921-8019	Antenna terminal assy.

Please make these part number corrections in your 5100II service manual. Thank you.

-Phase Linear Service Department

Phase Linear CORPORATION
20121 - 48th Avenue West, LYNNWOOD, WASHINGTON 98036 U.S.A. Telephone: (206) 774-3571

SERVICE BULLETIN 11/1/80
Model 5100

SUBJECT: 5100 Audio Output/Muting IC Part Number Change

The 5100 tuner audio output and muting IC has been re-designed for improved reliability with an accompanying Pioneer part number change from PA1002 to PA4004. The Phase Linear part number, 926-8083, remains the same.

The two IC's are interchangeable, therefore only PA4004 IC's will be shipped in the future, regardless of which of the two IC's are ordered.

Please make the necessary above changes to your model 5100 Service Manual.