

CDP-497

SERVICE MANUAL

*US Model
Canadian Model
AEP Model
UK Model
E Model
Australian Model*



Photo: AEP Model

Model Name Using Similar Mechanism	CDP-295
CD Mechanism Type	CDM14-5BD8A
Optical Pick-Up Block Type	BU-5BD8A

SPECIFICATIONS

Compact disc player

Frequency response	2 Hz to 20 kHz \pm 0.5 dB
Signal-to-noise ratio	More than 100dB
Dynamic range	More than 98 dB
Harmonic distortion	Less than 0.0035%
Channel separation	More than 100 dB

Outputs

LINE OUT (FIXED) (phono jacks)	Output level 2V (at 50 kilohms) Load impedance over 10 kilohms
LINE OUT (VARIABLE) (phono jack) (only for the UK and AEP model)	Output level max. 2V (at 50 kilohms) Load impedance over 50 kilohms
PHONES (stereo phone jack)	Output level max. 10 mW Load impedance 32 ohms

General

Power requirements	AEP model: 220V - 230V AC, 50/60Hz UK, Australian model: 240V AC, 50/60 Hz US, Canadian model: 120V AC, 60 Hz E model: 110 - 120V/220 - 240V AC, adjustable with the voltage selector, 50/60 Hz
Power consumption	12W

Dimensions (approx., including projections)	430 \times 100 \times 295 mm (w/h/d) (17 \times 4 \times 11 5/8 inches)
Weight (approx.)	3.5 kg (7 lbs 12 oz)

Remote commander

(AEP, G, UK model: RM-D597

US, Canadian, E, Australian model: RM-D297)

Remote control system	Infrared control
Power requirements	3V DC with two R6 (size AA) batteries
Dimensions (approx., including projections)	40 \times 20 \times 175 mm (w/h/d) (1 5/8 \times 13/16 \times 7 inches)
Weight (approx.)	95g (4oz)

Supplied accessories

Audio cord	(1) (2 phono plugs - 2 phono plugs)
Remote commander	(1)
R6 (AA) batteries	(2)

Design and specifications are subject to change without notice.

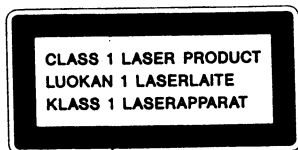
COMPACT DISC PLAYER
SONY[®]



1. Laser Diode Properties
- Material: GaAlAs
 - Wavelength: 780 nm
 - Emission Duration: continuous

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For the United Kingdom and European countries



This Compact Disc player is classified as a CLASS 1 LASER product. The CLASS 1 LASER PRODUCT label is located on the rear exterior.

SAFETY-RELATED COMPONENT WARNING!!

COMPONENTS IDENTIFIED BY MARK \triangle OR DOTTED LINE WITH MARK \triangle ON THE SCHEMATIC DIAGRAMS AND IN THE PARTS LIST ARE CRITICAL TO SAFE OPERATION. REPLACE THESE COMPONENTS WITH SONY PARTS WHOSE PART NUMBERS APPEAR AS SHOWN IN THIS MANUAL OR IN SUPPLEMENTS PUBLISHED BY SONY.

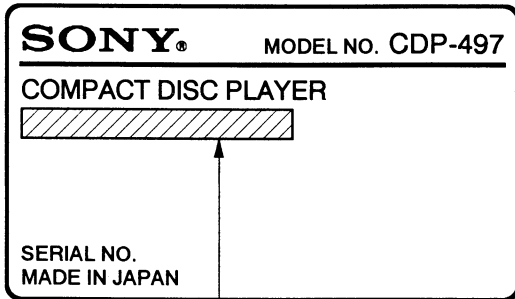
ATTENTION AU COMPOSANT AYANT RAPPORT À LA SÉCURITÉ!

LES COMPOSANTS IDENTIFIÉS PAR UNE MARQUE \triangle SUR LES DIAGRAMMES SCHÉMATIQUES ET LA LISTE DES PIÈCES SONT CRITIQUES POUR LA SÉCURITÉ DE FONCTIONNEMENT. NE REMPLACER CES COMPOSANTS QUE PAR DES PIÈCES SONY DONT LES NUMÉROS SONT DONNÉS DANS CE MANUEL OU DANS LES SUPPLÉMENTS PUBLIÉS PAR SONY.

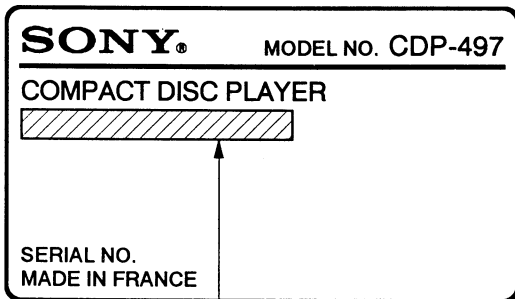
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MODEL IDENTIFICATION

— SPECIFICATION LABEL —



US, Canadian MODEL: AC:120V 60Hz 12W
 AEP MODEL: AC:220-230V~ 50/60Hz
 Australian MODEL: AC:240V~ 50/60Hz
 E MODEL: AC:110-120, 220-240V~ 50/60Hz 12W



AEP MODEL: AC:220-230V~ 50/60Hz
 UK MODEL: AC:240V~ 50/60Hz

SAFETY CHECK-OUT

After correcting the original service problem, perform the following safety check before releasing the set to the customer:

Check the antenna terminals, metal trim, "metallized" knobs, screws, and all other exposed metal parts for AC leakage. Check leakage as described below.

LEAKAGE TEST

The AC leakage from any exposed metal part to earth ground and from all exposed metal part to any exposed metal part having a return to chassis, must not exceed 0.5 mA (500 microamperes). Leakage current can be measured by any one of three methods.

1. A commercial leakage tester, such as the Simpson 229 or RCA WT-540A. Follow the manufacturers' instructions to use these instruments.
2. A battery-operated AC milliammeter. The Data Precision 245 digital multimeter is suitable for this job.
3. Measuring the voltage drop across a resistor by means of a VOM or battery-operated AC voltmeter. The "limit" indication is 0.75V, so analog meters must have an accurate low-voltage scale. The Simpson 250 and Sanwa SH-63Trd are examples of a passive VOM that is suitable. Nearly all battery operated digital multimeters that have a 2V AC range are suitable. (See Fig. A)

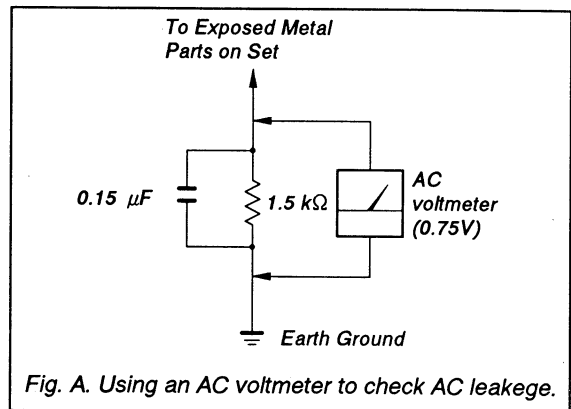
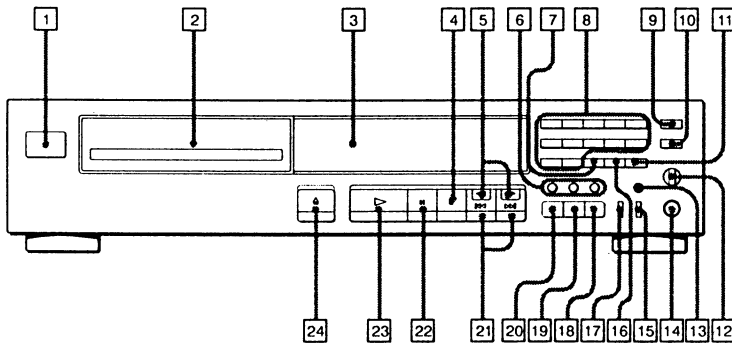


Fig. A. Using an AC voltmeter to check AC leakage.

SECTION 1
GENERAL

Identifying the
Parts

Front Panel



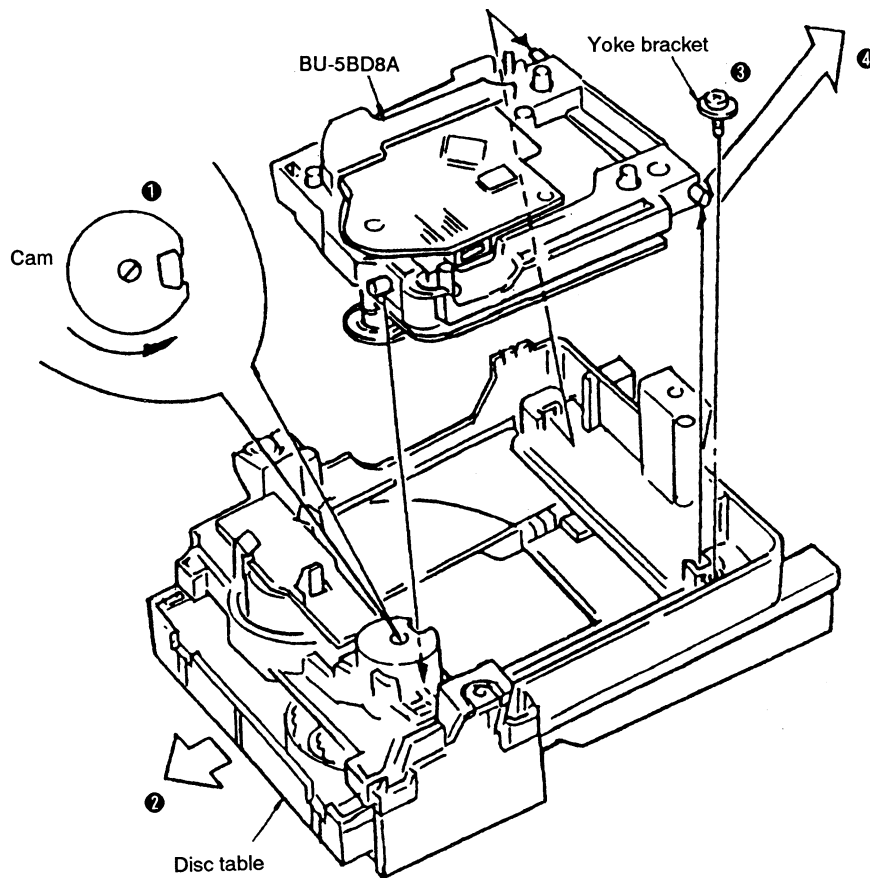
- 1 POWER switch
- 2 Disc tray
- 3 Display window
- 4 ■ (stop) button
- 5 ◀▶ (manual search) buttons
- 6 Play mode buttons
CONTINUE button
SHUFFLE button
PROGRAM button
- 7 CHECK (program check) button
- 8 Numeric buttons
- 9 EDIT/TIME FADE button
- 10 TIME SET button
- 11 > 12 (over 12) button
- 12 LINE OUT/PHONE LEVEL control
(for the model for the United Kingdom
and European countries)
PHONE LEVEL control
(for the model for other countries)
- 13 AUTO SPACE/AUTO CUE button
- 14 PHONES jack
- 15 PEAK SEARCH button
- 16 CLEAR (program clear) button
- 17 MUSIC SCAN button
- 18 FADER button
- 19 REPEAT button
- 20 TIME button
- 21 ◀▶▶▶ (AMS*) buttons
- 22 || (pause) button
- 23 ▶ (play) button
- 24 ▲ OPEN/CLOSE button

* AMS is the abbreviation of Automatic Music Sensor.

SECTION 2 DISASSEMBLY

Note: Follow the disassembly procedure in the numerical order given.

- ① Turn the cam to the direction of arrow (Counter clock wise) by minus screw driver.
- ② Take off the disc table.
- ③ Remove the yoke bracket.
- ④ Remove the MD (BU-5BD8A) to the direction of arrow.

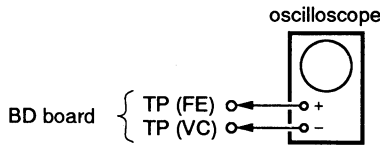


SECTION 3 ELECTRICAL BLOCK CHECKING

Note:

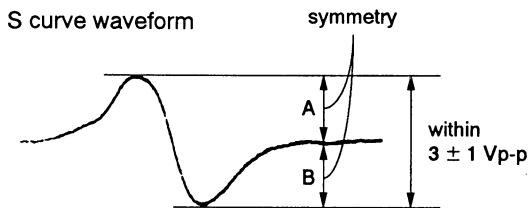
1. CD Block basically constructed to operate without adjustment. Therefore, check each item in order given.
2. Use YDES-18 disc (3-702-101-01) unless otherwise indicated.
3. Use the oscilloscope with more than $10M\Omega$ impedance.
4. Clean an object lens by an applicator with neutral detergent with the signal level is low than specified value with the following checks.

S Curve Check



Procedure:

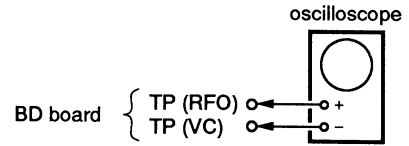
1. Connect oscilloscope to test point TP (FE) on BD board.
2. Connect between test point TP (FEI) and TP (VC) by lead wire.
3. Turn Power switch on and actuate the focus search. (actuate the focus search when disc table is moving in and out.)
4. Check the oscilloscope waveform (S curve) is symmetrical between A and B. And confirm peak to peak level within 3 ± 1 Vp-p.



5. After check, remove the lead wire connected in step 2.

- Note:**
- Try to measure several times to make sure that the ratio of A:B or B:A is more than 10:7.
 - Take sweep time as long as possible and light up the brightness to obtain best waveform.

RF Level Check

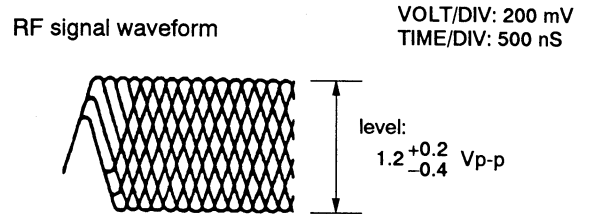


Procedure:

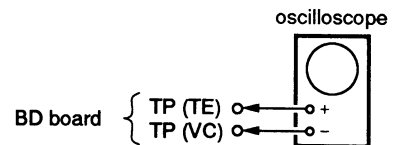
1. Connect oscilloscope to test point TP (RFO) on BD board.
2. Turn Power switch on.
3. Put disc (YEDS-18) in and playback.
4. Confirm that oscilloscope waveform is clear and check RF signal level is correct or not.

Note:

Clear RF signal waveform means that the shape "◇" can be clearly distinguished at the center of the waveform.

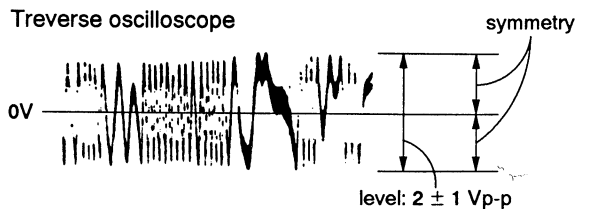


E-F Balance Check



Procedure:

1. Connect test point TP (ADJ) to ground and TP (TEI) to TP (VC) with lead wire.
2. Connect oscilloscope to test point TP (TE) on BD board.
3. Turn Power switch on.
4. Put disc (YEDS-18) in and playback.
5. Confirm that the oscilloscope waveform is symmetrical on the top and bottom in relation to 0V, and check this level.

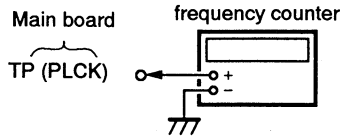


6. Remove the lead wire connected in step 1.

RF PLL Free-run Frequency Check

Procedure:

1. Connect frequency counter to test point (PLCK) with lead wire.



2. Turn Power switch on.
3. Confirm that reading on frequency counter is 4.3218 MHz.

Focus/Tracking Gain

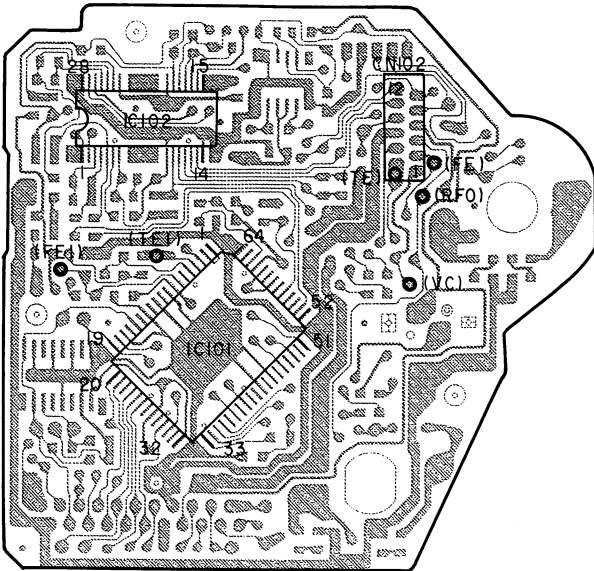
This gain has a margin, so even if it is slightly off.

There is no problem.

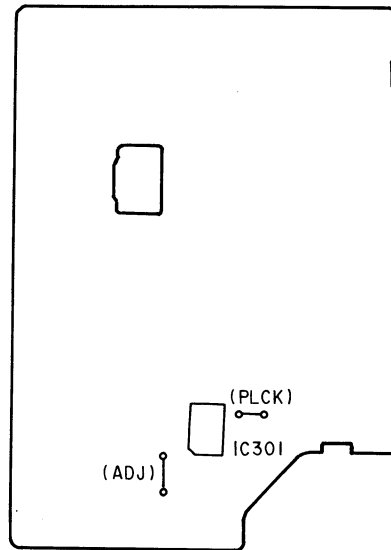
Therefore, do not perform, this adjustment.

Please note that it should be fixed to mechanical center position when you moved and do not know original position.

[BD BOARD] — Conductor Side —



[MAIN BOARD] — Component Side —



SECTION 4 DIAGRAMS

4-1. PIN FUNCTIONS

• IC101 (CXD2501Q) PIN FUNCTION

Pin No.	Pin Name	I/O	Function
1	ADII	I	A/D signal input.
2	ADIO	O	Analog switch output.
3	RF	I	RF signal input.
4	TE	I	Tracking error signal input.
5	SE	I	SE signal input.
6	NC		Not used.
7	FE	I	Focus error signal input.
8	VC	I	Center voltage (2.5V) input.
9	DVss		Digital GND.
10	NC		Not used.
11	ATSK		
12	NC		
13	DFSW	I	Prevents the DFCT circuit from operating at "H".
14	DFCT	O	DFCT signal output.
15	XTAL	I	Master clock signal input.
16	NC		Not used.
17	XTSL	I	Frequency switching of input master clock signal. 22 MHz at "H". 11 MHz at "L".
18	LOCK	I	Lock signal input.
19	FOK	O	Focus OK signal output.
20	MIRR	O	Mirror signal output.
21	CLK	I	Clock signal when transmitting data from micro processor.
22	NC		Not used.
23	XLT	I	Latch signal when transmitting data from micro processor.
24	DATA	I	Data from micro processor.
25	COUT	O	Track jump number count signal output.
26	NC		Not used.
27	DVDD		Digital +5V.
28	NC		Not used.
29	SENS	O	SENS signal output.
30	SCLK	I	Serial data reading clock.
31	NC		Not used.
32	DIRC	I	DIRC signal input.
33	XRST	I	Reset signal input.
34	SOCK		Not used.
35	XOLT		
36	SOUT		
37	NC		
38	SFDR	O	Sled drive signal output (FWD).
39	SRON		Not used.
40	SRDR	O	Sled drive signal output (REVERSE).
41	SFON		Not used.
42	NC		
43	DVss		Digital GND.
44	NC		Not used.

Pin No.	Pin Name	I/O	Function
45	TEST		Fixed at "L".
46	NC		Not used.
47	TRDF	O	Tracking drive signal output (FWD).
48	TRON		Not used.
49	TRDR	O	Tracking drive signal output (REVERSE).
50	TFON		Not used.
51	FFDR	O	Focus drive signal output (FWD).
52	FRON		Not used.
53	FRDR	O	Focus drive signal output (REVERSE).
54	FFON		Not used.
55	NC		
56	SSTP	I	Limit switch detection.
57	NC		Not used.
58	CDS	I	Used at "H".
59	NC		Not used.
60	DVDD		Digital +5V.
61	AVDD		Analog +5V.
62	IGEN		Input for the ope-amp current supply.
63	NC		Not used.
64	AVss		Analog GND.

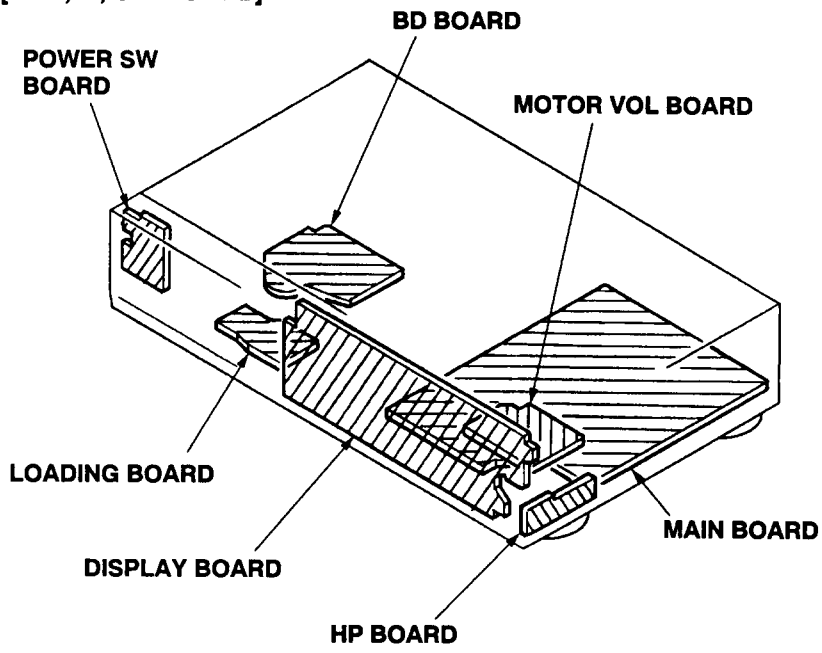
• IC301 (CXD2500QA) PIN FUNCTION

Pin No.	Pin Name	I/O	Function
1	FOK	I	Focus OK input pin. Used for SENS output and servo auto sequencer.
2	FSW	O	Spindle motor output filter switching output.
3	MON	O	Spindle motor ON-OFF control output.
4	MDP	O	Spindle motor servo control.
5	MDS	O	Spindle motor servo control.
6	LOCK	O	Samples GFS at 460 Hz, and outputs H when GFS is H. Outputs L if L continues eight times.
7	NC	—	
8	VCOO	O	Oscillation circuit output for analog EFM PLL.
9	VCOI	I	Oscillation circuit input for analog EFM PLL. f _{LOCK} =8.6436 MHz.
10	TEST	I	TEST pin. Normally GND.
11	PDO	O	Charge pump output for analog EFM and PLL.
12	Vss		GND
13	NC	—	
14	NC	—	
15	NC	—	
16	VPCO	O	PLL charge pump output for variable pitch.
17	VCKI	I	Clock input from the external VCO for variable pitch. f _{center} =16.9344 MHz.
18	FILO	O	Filter output for master PLL (Slave=Digital PLL).
19	FILI	I	Filter input for master PLL.
20	PCO	O	PLL charge pump output for master PLL.
21	AVss		Analog GND
22	CLTV	I	Master VCO control voltage input.
23	AVDD		Analog power supply (+5V)
24	RF	I	EFM signal input.
25	BIAS	I	Asymmetry circuit regulated current input.
26	ASYI	I	Asymmetry comparative voltage input.
27	ASYO	O	EFM full swing output (L=Vss, H=VDD)
28	ASYE	I	L:Asymmetry circuit OFF H:Asymmetry circuit ON.
29	NC	—	Not used.
30	PSSL	I	Audio data output mode switching input. Serial output at L, parallel output at H.
31	WDCK	O	D/A interface for 48 bit slot. Word-clock f=2Fs.
32	LRCK	O	D/A interface for 48 bit slot. LR clock f=Fs.
33	VDD		Power supply (+5V).
34	DA16	O	DA16 (MSB) output when PSSL=1. 48 bit slot serial data when PSSL=0 (2s'COMP, MSB first).
35	DA15	O	DA15 output when PSSL=1. 48 bit slot bit clock when PSSL=0.
36	DA14	O	DA14 output when PSSL=1. 64 bit slot serial data when PSSL=0 (2s'COMP, LSB first)
37	DA13	O	DA13 output when PSSL=1. 64 bit slot bit clock when PSSL=0.
38	DA12	O	DA12 output when PSSL=1. 64 bit slot LR clock when PSSL=0.
39	DA11	O	DA11 output when PSSL=1. GTOP output when PSSL=0.
40	AD10	O	DA10 output when PSSL=1. XUGF output when PSSL=0.
41	DA09	O	DA09 output when PSSL=1. XPLCK output when PSSL=0.
42	DA08	O	DA08 output when PSSL=1. GFS output when PSSL=0.
43	DA07	O	DA07 output when PSSL=1. RFCK output when PSSL=0.
44	DA06	O	DA06 output when PSSL=1. C2P0 output when PSSL=0.
45	DA05	O	DA05 output when PSSL=1. XRAOF output when PSSL=0.

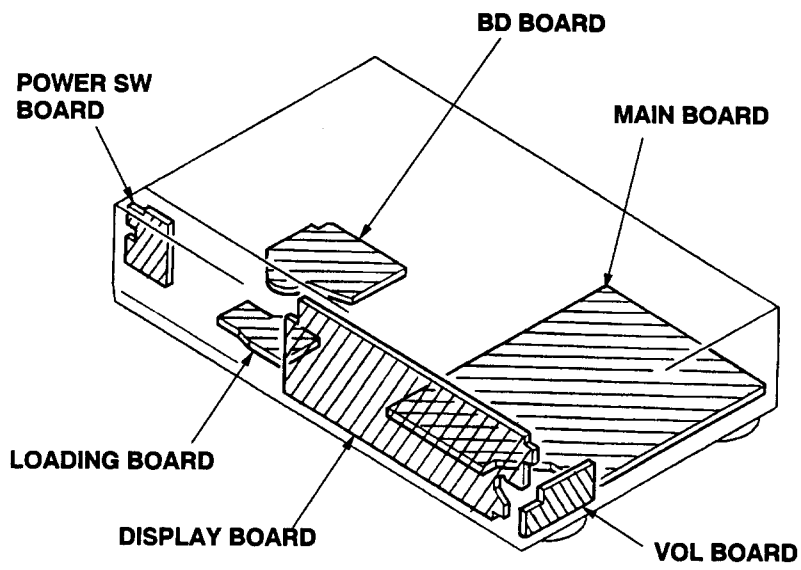
Pin No.	Pin Name	I/O	Function
46	DA04	O	DA04 output when PSSL=1. MNT3 output when PSSL=0.
47	DA03	O	DA03 output when PSSL=1. MNT2 output when PSSL=0.
48	DA02	O	DA02 output when PSSL=1. MNT1 output when PSSL=0.
49	DA01	O	DA01 output when PSSL=1. MNT0 output when PSSL=0.
50	APTR	O	Aperture correction control output. H when Rch.
51	APTL	O	Aperture correction control output. H when Lch.
52	Vss		GND
53	XTAI	I	16.9344 MHz crystal oscillation circuit input. Or 33.8688 MHz input.
54	XTAO	O	16.9344 MHz crystal oscillation circuit input.
55	XTSL	I	Crystal selection input pin. Set to L when crystal is 16.9344 MHz. Set to H when 33.8688 MHz.
56	FSTT	O	2/3 frequency division output of Pins ⑤ and ④. Will not change by variable pitch.
57	C4M	O	4.2336 MHz output. Varies simultaneously with pitch.
58	C16M	O	16.9344 MHz output. Varies simultaneously with pitch.
59	MD2	I	Digital-Out ON/OFF control. ON at H, OFF at L.
60	DOUT	O	Digital-Out output pin.
61	EMPH	O	Outputs H if emphasis is present in the playback disc. Outputs L when it is absent.
62	WFCK	O	WFCK (Write Frame Clock) output.
63	SCOR	O	Outputs H when either sub-code sync S0 or S1 has been detected.
64	SBSO	O	SubP to W serial output.
65	EXCK	I	SBSO read-out clock input.
66	SQSO	O	SubQ 80 bit and PCM peak level data 16 bit output.
67	SQCK	I	SQSO read-out clock input.
68	MUTE	I	Mute at H, release at L.
69	SENS	—	SENS output. Outputs to CPU.
70	XRST	I	System reset. Resets at "L".
71	DATA	I	Serial data input from CPU.
72	XLAT	I	Latch input from CPU. Latches the serial data at falling.
73	VDD		Power supply (+5V).
74	CLOK	I	Serial data transmission clock input from CPU.
75	SEIN	I	SENS input from SSP.
76	CNIN	I	Track jump number count signal input.
77	DATO	O	Outputs the serial data to SSP.
78	XLTO	O	Outputs the serial data latch to SSP. Latches at falling.
79	CLKO	O	Outputs the serial data transmission clock to SSP.
80	MIRR	I	Mirror signal input. Uses for a jump above 128 track with auto sequencer. 1, 0

4-2. CIRCUIT BOARDS LOCATION

[AEP, G, UK MODEL]

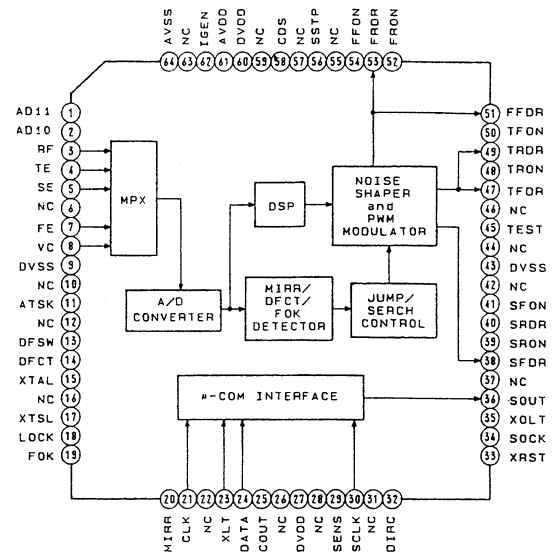


[US, Canadian, E, Australian MODEL]

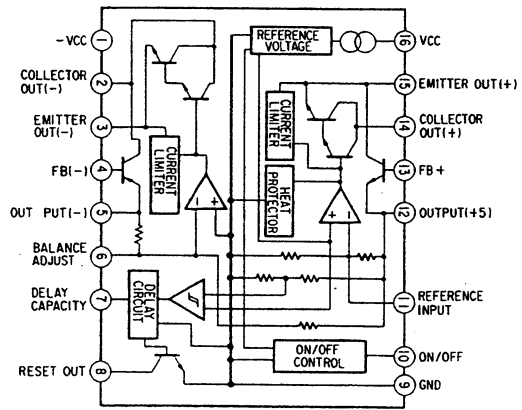


4-9. IC BLOCK DIAGRAMS

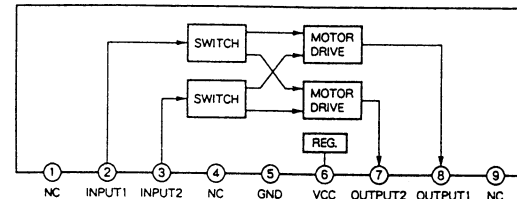
IC101 CXD2501Q



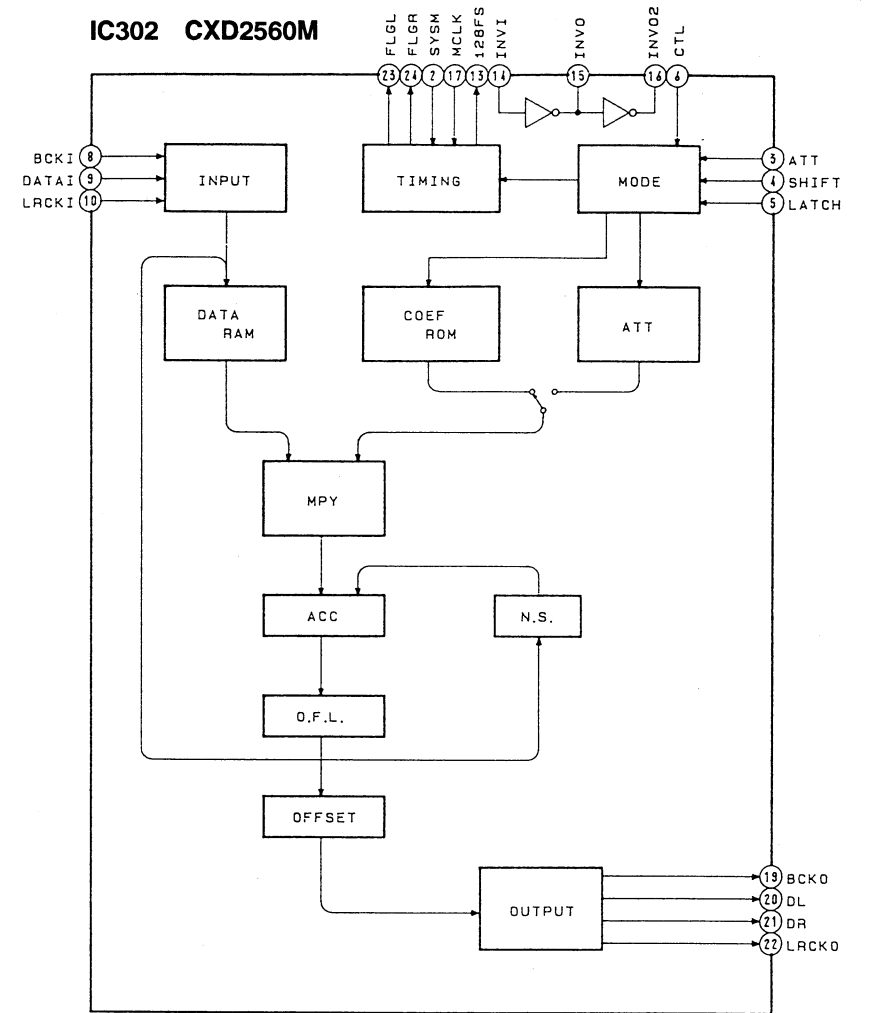
IC202 M5290P-16



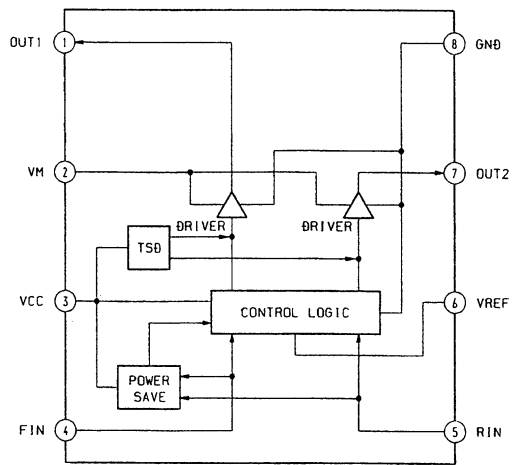
IC471 BA6208



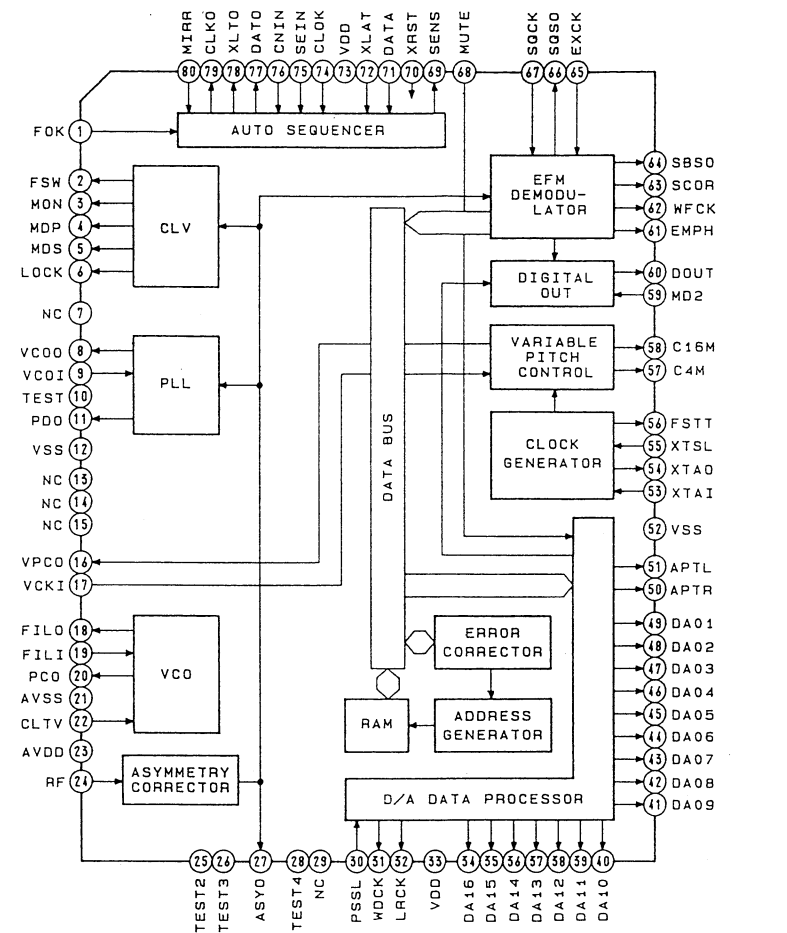
IC302 CXD2560M



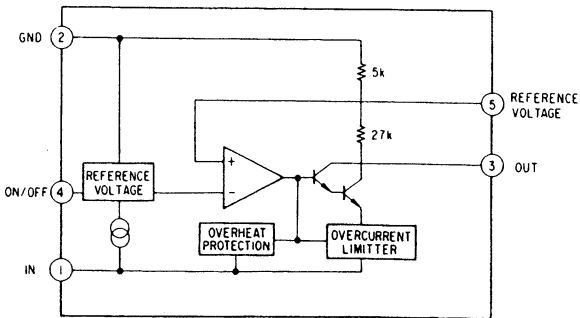
IC103 BA6287F



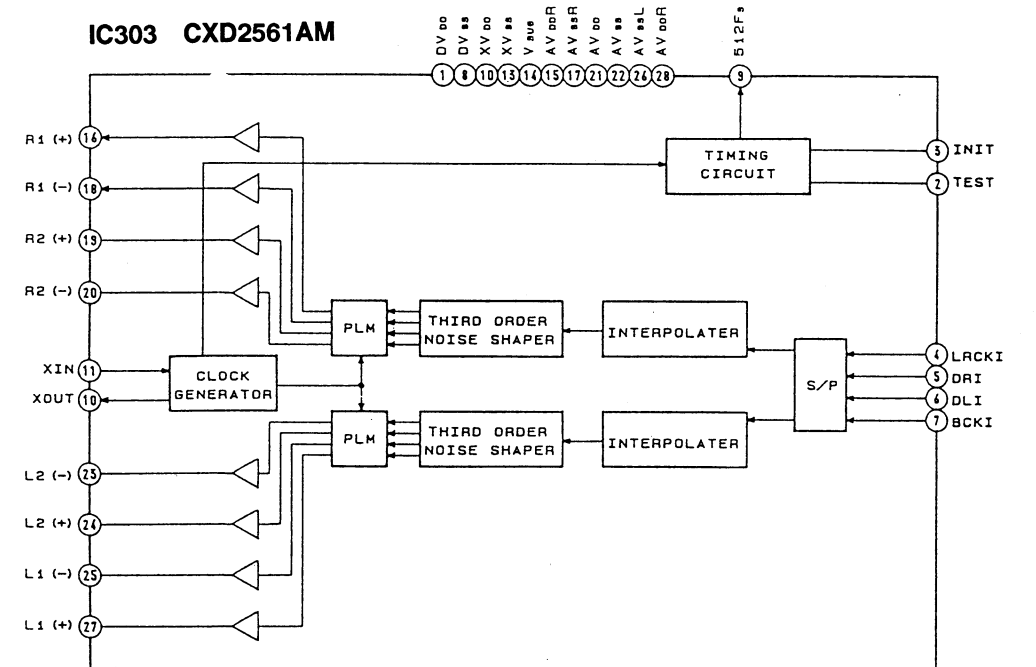
IC301 CXD2500AQ



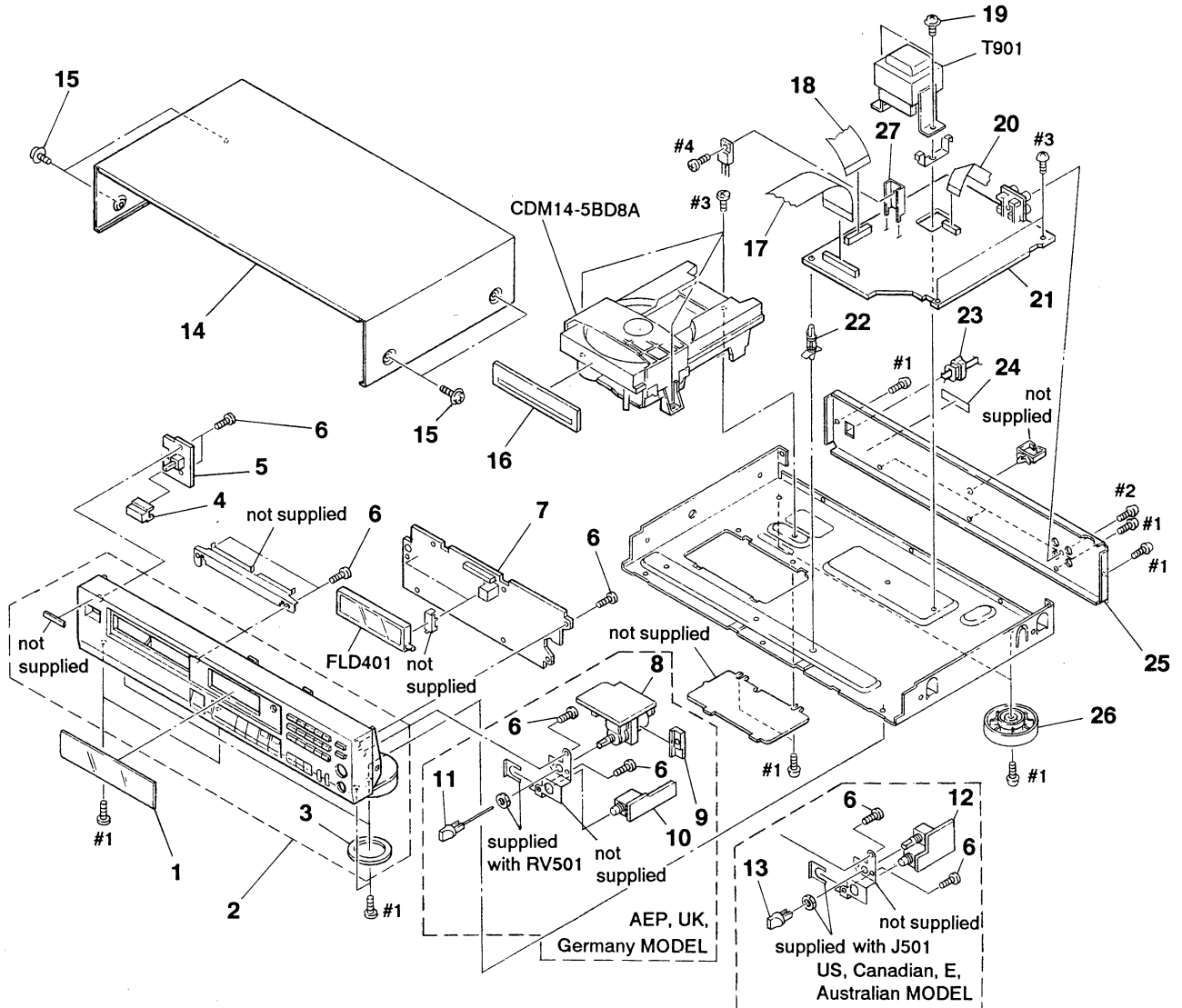
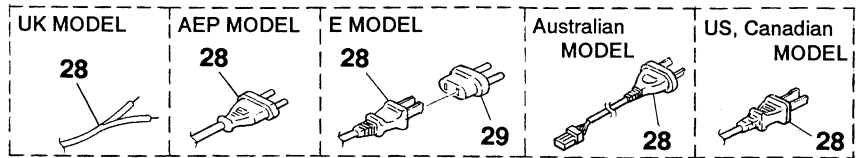
IC201 M5293L



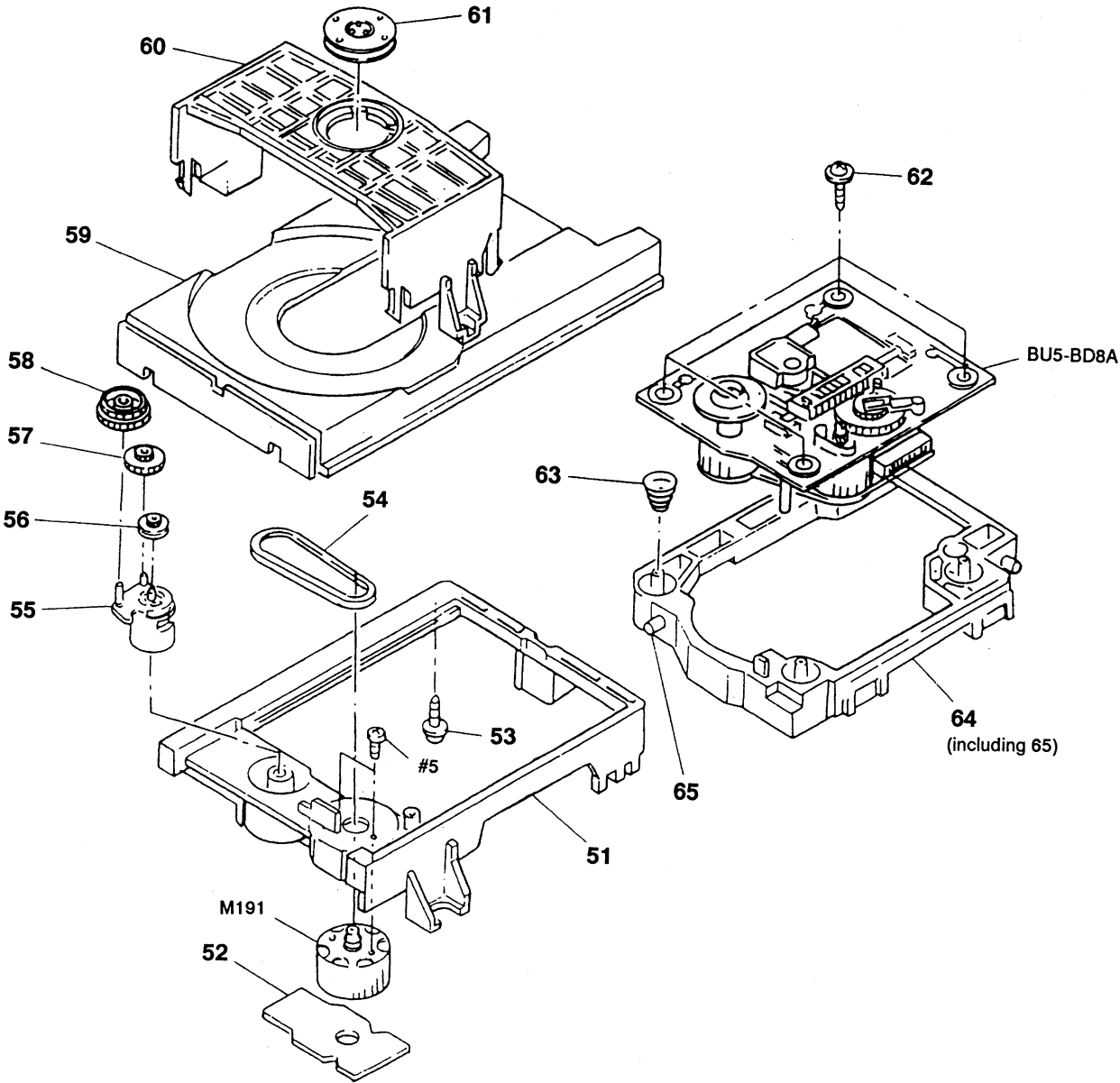
IC303 CXD2561AM



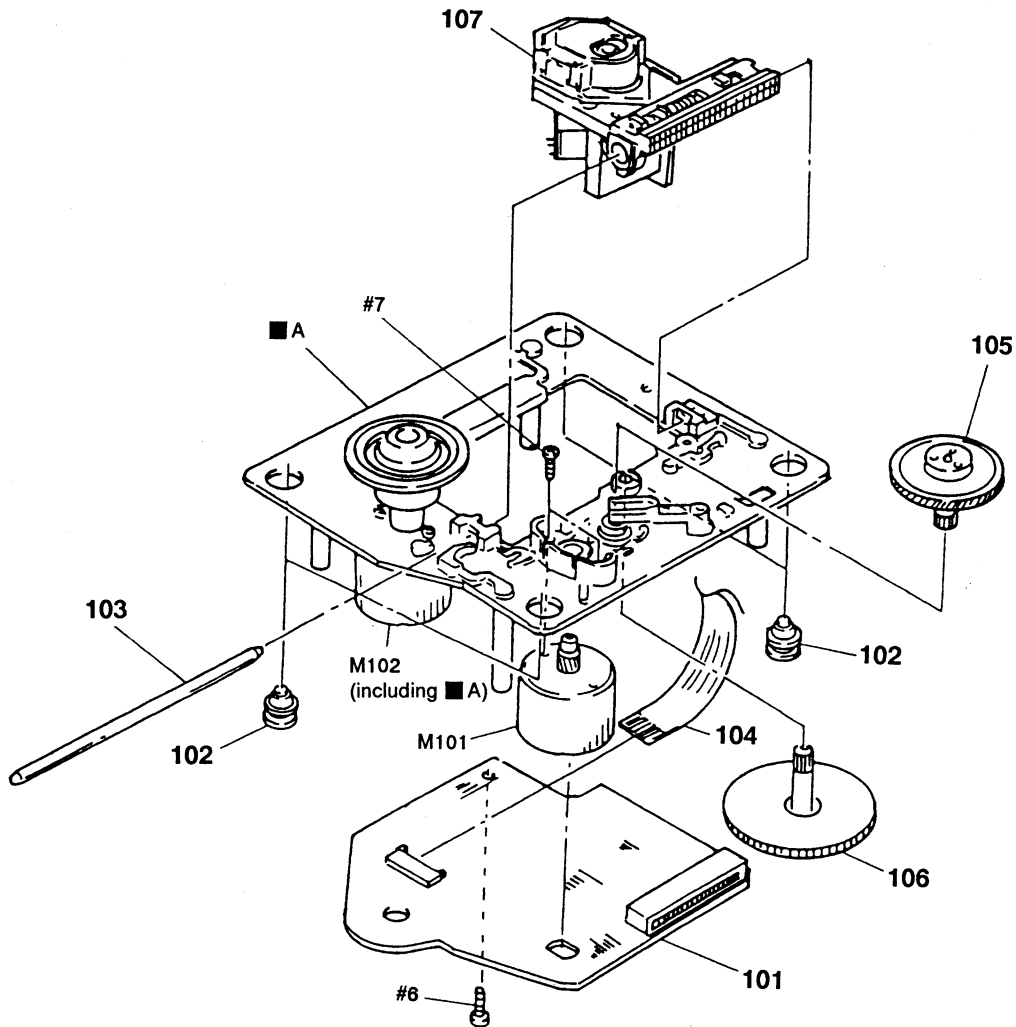
5-1. CABINET SECTION






5-2. MD SECTION (CDM14-5BD8A)



5-3. PIC-UP BLOCK (BU5BD8A)



The components identified by mark  or dotted line with mark  are critical for safety. Replace only with part number specified.

Les composants identifiés par une marque  sont critiques pour la sécurité. Ne les remplacer que par une pièce portant le numéro spécifié.