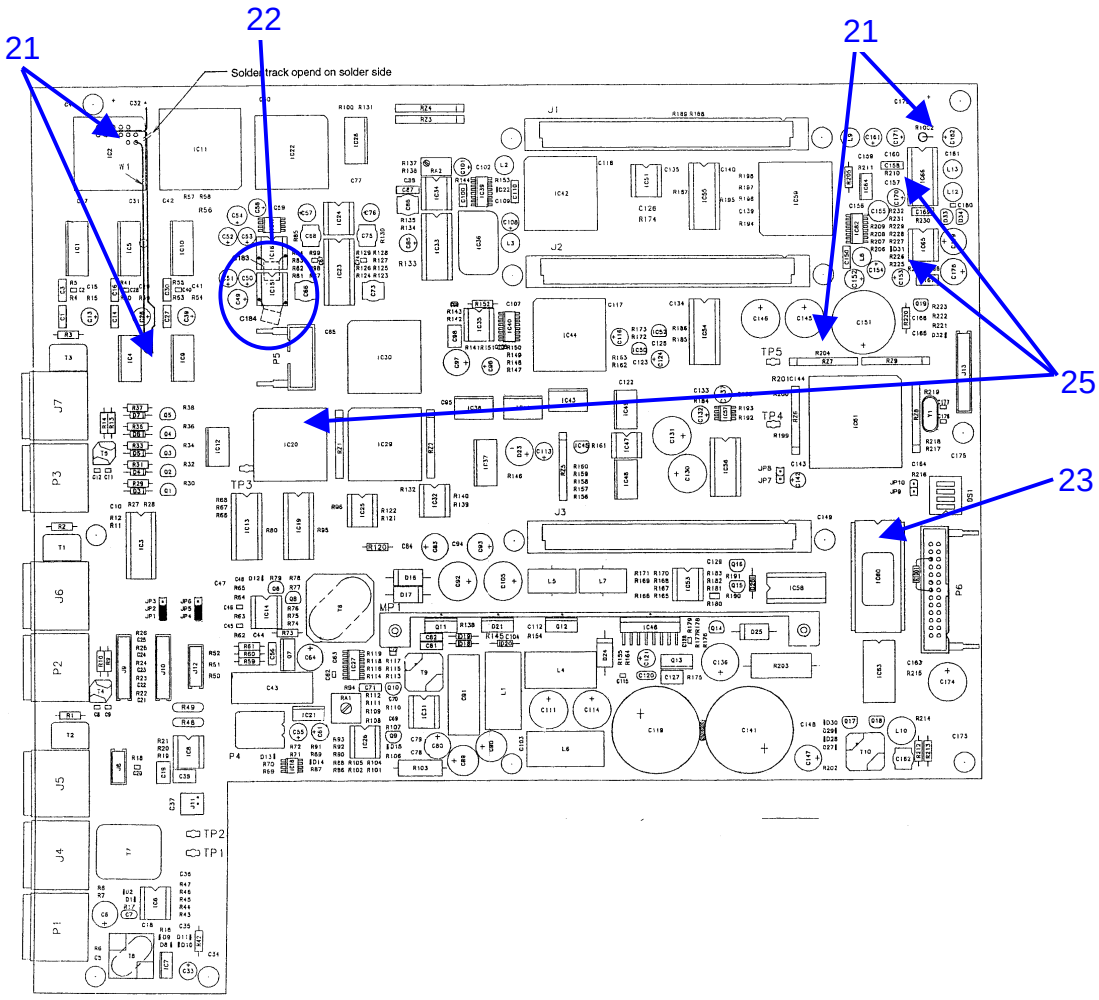
Hardware History D424

Mother Board 1.866.120

Index 20		**shipped with prototype and promotion series only (S/N 00xx, 01xx)** *subsequent modifications :* - R19=68k, Pulldown R1001: P6.14->P6.22, - Upgrades 1.866.910/911/914
Index 21	14.8.1996	*correct CLK polarity for AES out :* connect IC4.5, IC9.5 with IC2.6 *R204 (0 Ohm) no longer used* *improved CLK quality* : replace L11 (100mH) with R1002 (22Ohm) replace C182 (10uF) with 100 uF
Index 22	5.2.1997	*SW Upgrade V1.1 :* IC60: 1.866.120.21 > 22, 1.866.905.20 -> 21 *reliable Desktop Controller operation :* additional C183/184 on soldering side: 47nF IC15.3-5, IC16.3-6
Index 23	30.6.1997	*SW Upgrade V1.2 :* IC60: 1.866.905.21 -> 22
Index 24	26.11.1997	*new layout Index 12, includes above modifications C183/184, R1001*
Index 25	22.6.1998 (S/N 1194	*improved clock jitter :* R210: 3k3 -> 1k, R226: 1k -> 5k6 *improved TC readability :* Software 120 MOTCC IC20: 1.866.915.20 -> 21

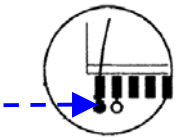


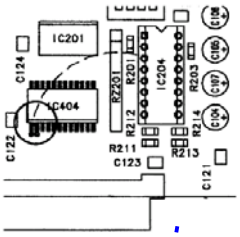
SCSI Board 1.866.130

Index 20		**shipped with prototype and promotion series only (S/N 00xx, 01xx)** *subsequent modifications :* wire bridge, see drawing below
Index 21	5.9.1996	**shipped with prototype and promotion series only (S/N 00xx, 01xx)** *sample accurate timecode sync :* - wire bridge P201.23C to RZ301.3
	21.9.1996	*new layout Index 12* without above wire bridges
Index 22	5.2.1997	*SW Upgrade V1.1 :* (factory upgrade required for SW 1.866.903.21) Main Software IC105/104*:* 1.866.900/901.20 -> 21
Index 23	30.6.1997	*SW Upgrade V1.2 :* Main Software IC105/104*:* 1.866.900/901.21 -> 22
Index 24	30.10.1997	*SW Upgrade V1.3 :* Main Software IC105/104*:* 1.866.900/901.22 -> 23 Frontpanel SW ICxx*:* 1.866.902.20 -> 21 *decoupled SCSI Termination Power* - additional diode D501: BAV20 in series with R502 *correct termination of IRTS3 processor port* new R232 (2k7) at P201.30B to 32C
Index 25	14.4.1998	*SW Upgrade V1.3.1 :* Main Software IC105/104: 1.866.900/901.23 -> 24
Index 26	13.8.2001	*SW Upgrade V1.6 :* Main Software IC105/104: 1.866.900/901.24 -> 25 *lower temperature operation of Altera circuits for extended lifetime* - IC 601/701 with mounted heat sink (50.20.3013)

Index 20 modification (for boards with layout 11 only) :

- cut track between IC 404 pin 1 and nearby contact hole
- solder wire to IC404.1, feed it through contact hole, and connect it to IC 204.3 on soldering side

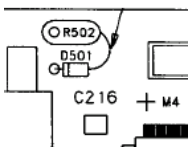




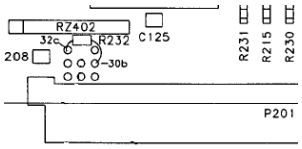
Index 21 modification (for boards with layout 11 only) :

- add wire bridge P201.23C to RZ301.3

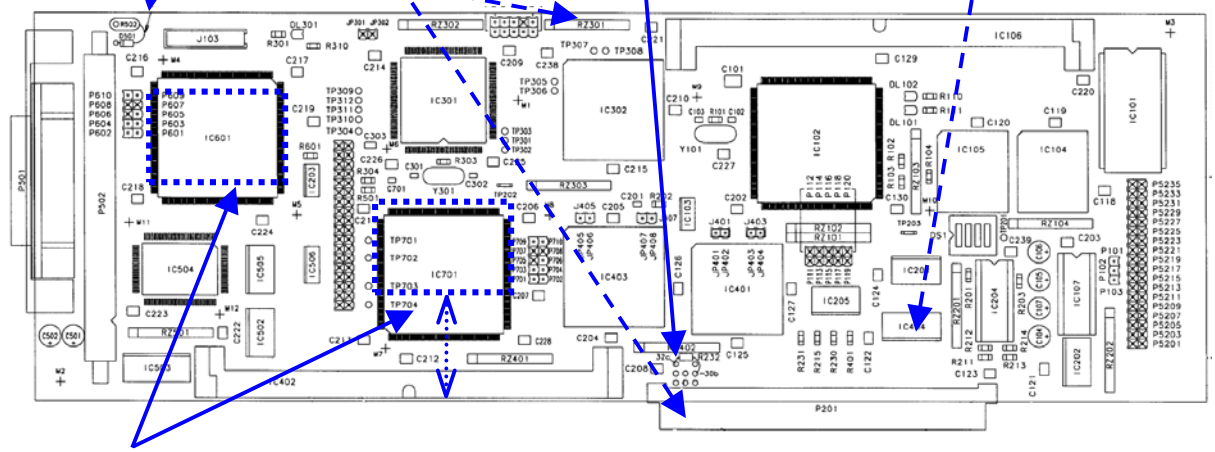
Index 24 : Diode D501



Index 24 : R232



SCSI Board 1.866.130.24

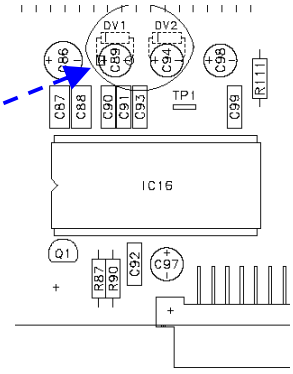


Index 26: Heatsink for IC 601/701, mounted with thermally conductive adhesive (99.01.3252)
IC 701 : min distance to bottom edge : 29 mm

Analog Input/Output 1.866.140

Index 20		
Rev A	22.3.2001	*protection of AD Converter CS-5390 in power-up phase :* - with additional zener diodes D10/11 (5.6V) in parallel to C89/C94 on soldering side

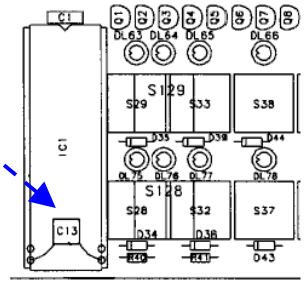
Add diodes
on soldering side



Keyboard 1.866.160

Index 00	
8.6.1998	*improved crosstalk immunity for reliable IC2 function (Key/Display I/O)* with additional C13 (47pF) between IC1.20-21

Add capacitor C13
on soldering side



Clock I/O Board 1.866.170

Index 00	29.7.1996	*Correct Termination Switch position (modified in series production) :* print modification (wires) to reverse termination switch position, for matching with backpanel label
		new layout 12, fixes above bug

Headphone Connector

	23.8.1996	additional 1000p capacitor for improved noise figures.

Shipping Schedule :

Prototypes/ADR	12/95
Pre-Series 101-131	06/96-08/96
Series	09/96-today