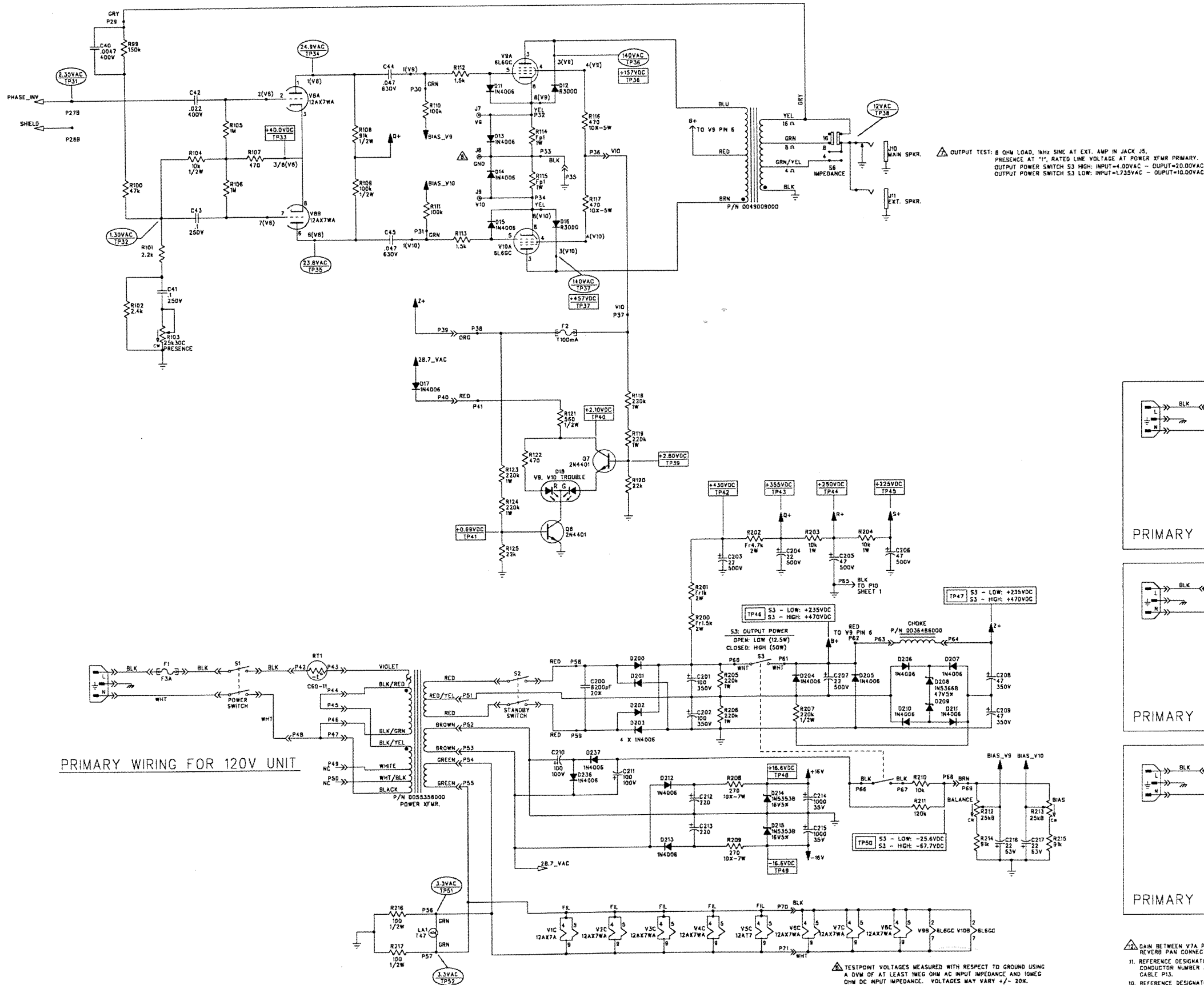


REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
A	PR425	10-AUG-99	M.J.C.
B	EC 2367	25-OCT-99	M.J.C.



OUTPUT TEST: 8 OHM LOAD, 1MHz SINE AT EXT. AMP IN JACK J5.
 PRESENCE AT "1", RATED LINE VOLTAGE AT POWER XFMR PRIMARY.
 OUTPUT POWER SWITCH S3 HIGH: INPUT=4.00VAC - OUTPUT=20.00VAC
 OUTPUT POWER SWITCH S3 LOW: INPUT=1.735VAC - OUTPUT=10.00VAC

PRIMARY WIRING FOR 120V UNIT

PRIMARY WIRING FOR 100V UNIT

PRIMARY WIRING FOR 230V UNIT

PRIMARY WIRING FOR 240V UNIT

- NOTES: (UNLESS OTHERWISE NOTED)
- THIS SCHEMATIC IS FOR PCB FABRICATIONS P/N 0055364000 AND 0055365000, AND PCB ASSEMBLIES P/N 0055365000 AND 0055365000.
 - ALL DIODES ARE 1N4006.
 - ALL POLARIZED CAPACITORS IN W.F., 20% 50V MINIMUM.
 - ALL UNPOLARIZED CAPACITORS IN W.F., 10% OR BETTER; 50V MINIMUM. (POWER SUPPLY BYPASS CAPACITORS ARE 20%).
 - ALL RESISTORS IN OHMS, S%: 1/4W.
 - TESTPOINT VOLTAGES MEASURED WITH RESPECT TO GROUND USING A 50M OHM AT LEAST 100 OHM DC INPUT IMPEDANCE AND 100HZ OHM DC INPUT IMPEDANCE. VOLTAGES MAY VARY +/- 20%.
 - UNIT AT RATED LINE VOLTAGE.
 - ALL CONTROLS SET TO "1" (50% ROTATION) EXCEPT CH. 1 VOL. AT "3" CH. 2 GAIN AT "2-3" CH. 3 VOL. AT "B". REVERSE AT "1" PRESENCE AT "1" EFFECTS LOOP ENGAGE, LOOP CONTROLS SET FOR UNITY GAIN (APPROX. "5-1/2").
 - BIAS SET FOR 30mv PER TUBE. SEE NOTE 8.
 - ALL AC VOLTAGES MEASURED WITH INPUT SIGNALS NORMALIZED TO PRODUCE 2.50V AT TP18 WHICH PRODUCES 12.0Vrms INTO AN 8 OHM RESISTIVE LOAD AT TP38. PCB'S CONNECTED TOGETHER VIA RIBBON CABLE/HEADER P13.

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TITLE: SERVICE DIAGRAM, COMBINED (schematic)
SUNN T50C

CHECKED BY: *AMW*
 DATE: 25-OCT-99
 APPROVED BY: *MS*
 DATE: 10-22-99
 DRAWN: M. COZZA (ENGR: M. COZZA)
 DATABASE FILE: 24258.SCH

SIZE: **D** DRAWING NUMBER: **0055375000** REV: **B**
 RELEASE DATE: 11-AUG-99 SHEET: 2 OF 4